CL-GD7556

Advance Hardware Reference Manual

OVERVIEW

The CL-GD7556 is the second product in a new family of 64-bit GUI and video-accelerated LCD/CRT controllers. It supports all of the highest operating modes of the CL-GD7555, but it does it at 3.3 V to save operating power. It offers 64-bit graphics performance and superb video quality with its trend-setting video-color adjustment, MVA features, and scaling engine. With on-chip video-acceleration features and V-Port™ support, the CL-GD7556 is an extremely flexible and cost-effective multimedia solution for premium portable computer designs. The CL-GD7556 surpasses desktop-system equivalency by providing 'desktop-replacement' performance, features, and display mode support for the office.

FEATURES

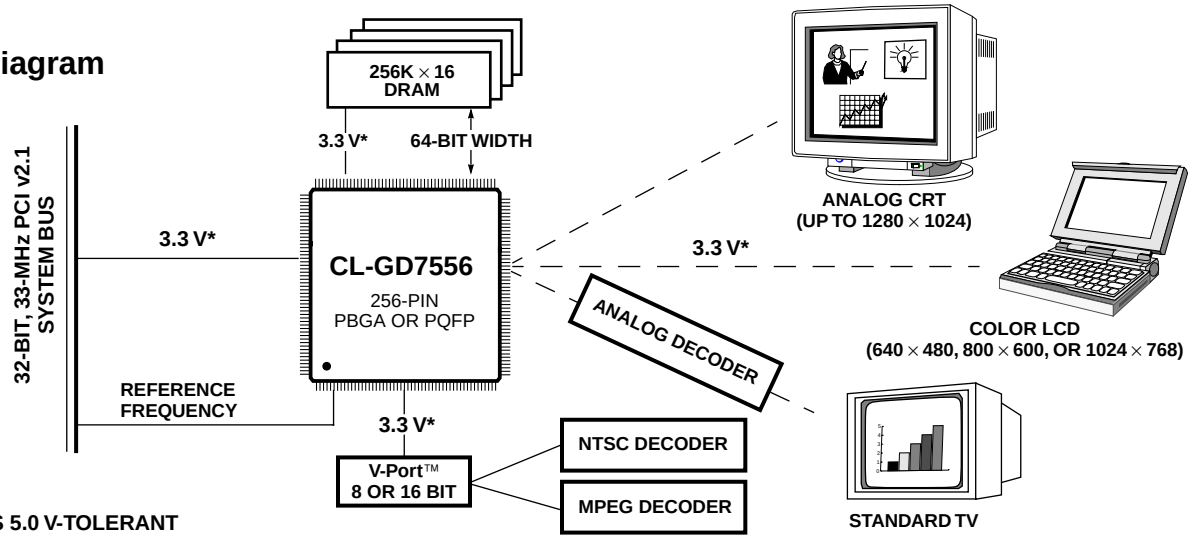
- **True 64-bit acceleration**
  - — 64-bit BitBLT acceleration engine
  - — 64-bit display memory interface
  - — 64-bit data paths
- **GUI acceleration**
  - — BitBLT setup register double buffering with autostart
  - — Transparent BitBLT (source color key)
  - — Memory-mapped I/O
  - — True packed-pixel addressing for 8, 16, and 24 bpp
- **Direct-connect 32-bit PCI v2.1 host bus interface**
  - — Multiple apertures to support simultaneous high-performance graphics and video
  - — Extended burst cycle and automatic bus retry support for high data transfer rates

Low-Power, High-Performance 64-Bit Video- and Graphics-Accelerated LCD/CRT Controller

- **Enhanced video acceleration**
  - — X and Y interpolated scaling engine
  - — EST (edge-sharpening technology) option with upscaling
  - — Continuous video upscaling to 1024 × 768
  - — Easy, independent end-user control of color, brightness, and contrast of the video window to compensate for the various color characteristics of the display and media
  - — DirectDraw™/DirectVideo™ (Windows® 95) and DCI1.X (display control interface for Windows® 3.X) support for full-motion video playback acceleration
  - — Integrated color space converter for 4:2:2 YCrCb to RGB 8:8:8
  - — Hardware destination color- and chroma-key support (hardware occlusion)
  - — V-Port™ and VPM (video port manager) support for PC Card ZV-Port specification
  - — Acceleration of MPEG-1, True Motion™, CinePak™, and Indeo™ software-coded video
  - — Video format support for 24- and 16-bpp RGB, 4:2:2 YCrCb, and proprietary compressed formats — AccuPak™ and DYUV 8-bpp YCrCb
- **Scalable, high-performance memory interface**
  - — 64-bit interface supporting 1, 2, and 4 Mbytes
  - — Optimized for EDO (extended-data-out) DRAM
  - — Single design can support 2-Mbyte (four 256K × 16) and 1-Mbyte (four 128K × 16) memory configurations

(cont.)

System Block Diagram



FEATURES (cont.)

Portable-Specific Features

- **Display device support**
  - TFT: 1024 × 768, 800 × 600, 640 × 480
  - DSTN: 1024 × 768, 800 × 600, 640 × 480
  - CRT: 1280 × 1024, 1024 × 768, 800 × 600, 640 × 480
  - NTSC and PAL TV through analog encoder
- **Flat panel-specific support**
  - Color TFT flat panels: 1-pixel/shift clock (9-, 12-, 18-, and 24-bit interfaces); 2-pixel/shift clock (18-bit direct-connect interface)
  - Enhanced hardware expansion of lower-resolution VGA display modes up to 800 × 600 on higher-resolution flat panels
  - Automatic centering of lower-resolution VGA display modes on higher-resolution flat panels
  - Dithering algorithm automatically adds up to 8 bits per primary color without decreasing resolution
  - Enhanced frame-rate modulation algorithm improves display quality with fast-response DSTN flat panels
- **Integration**
  - 24-bit true-color palette and DAC with support for gamma/color adjustment in High- and True-Color modes
  - Programmable frequency synthesizer: up to 80-MHz MCLK at 3.3 V; up to 135-MHz VCLK at 3.3 V
- **Power-management capabilities**
  - Low operating power, since all modes supported at 3.3 V
  - All 3.3-V I/O pins can interface to 5.0-V TTL logic
  - Active power management provides power-down control of select unused internal functional blocks during display
  - Suspend and Standby mode support
  - VESA® DPMS (display power management signaling) support
  - DDC-2B (display data channel) support
- **Packaging**
  - 256-pin PBGA (plastic ball grid array) 27 mm × 27 mm
  - 256-pin PQFP (plastic quad flat pack) 28 mm × 28 mm

PRODUCT DESCRIPTION

The outstanding GUI performance of the CL-GD7556 is accomplished with 64-bit architecture (64-bit BitBLT engine, memory interface, and data paths), and an ability to effectively eliminate setup latency during BitBLT operations by double-buffering BitBLT setup registers. In addition, optimizing support for the burst capabilities of PCI v2.1 (with multiple apertures, extended burst cycle support, auto bus retry, and a properly sized write buffer) boosts CL-GD7556 performance in all environments.

With its MVA (MotionVideo™ Acceleration) features, the CL-GD7556 leads the industry in multimedia video quality. In addition, the CL-GD7556 provides graphics color/brightness correction and a powerful scaling engine with EST (edge-sharpening technology). The color/brightness adjustment allows the CL-GD7556 to compensate for color and brightness variations of display devices (for example, TFT, DSTN, CRT, TV), resulting in consistent image display on various display devices and from various sources.

The CL-GD7556 also allows separate end-user color and brightness adjustment of the video window, independent of the overall display (the first portable graphics controller to offer this feature). This adjustment is important because almost all recorded video (including video recorded by camcorders) is gamma pre-corrected for a TV display. The end user can adjust the color and brightness of the video window in much the same way as it can be adjusted on a color TV. The end user can compensate for both the characteristics of the specific display device to be used and for loss of color fidelity caused by video recording, compression, and decompression.

To support multimedia special effects, the CL-GD7556 provides hardware occlusion (destination color/chroma keying) and transparent BitBLT (source color/chroma keying). Windows® 95 and DirectDraw™ emulate these functions in software; however, DirectDraw can recognize and use hardware support for these operations, greatly accelerating them.

The CL-GD7556 also offers flexibility for implementation. V-Port support allows cost-effective implementation of many multimedia features (MPEG video playback, TV tuner, video capture, and teleconferencing). These V-Port–related functions can be implemented on the motherboard or added later as ZV-Port–enabled PC Cards.

In most high-end implementations, the CL-GD7556 is likely to be implemented with a 2-Mbyte frame buffer using four 256K × 16 DRAMs. However, a more cost-effective mid-range 1-Mbyte product can be implemented using the same board design and replacing the four 256K × 16 DRAMs with four pin-compatible 128K × 16 DRAMs. The graphics benchmark performance of the 1-Mbyte configuration is the same, but fewer modes are supported.

To summarize, the CL-GD7556 is an industry-leading portable graphics solution with exceptional graphics performance and superb video quality, allowing much flexibility in implementation.

FEATURES	CL-GD7556	BENEFITS
Performance		
■ Winmark® 95 expectation (Pentium® 166, Windows® 95, Winbench 96)	>30M Winmarks	❒ Better end-user responsiveness.
■ BitBLT engine	Second-generation 64-bit	❒ Proven core design and driver base.
■ Transparent BitBLT	✓	❒ Enhances Windows® 95 game performance; enables non-rectangular BitBLTs.
■ Memory-mapped I/O	✓	❒ Improves performance by reducing host CPU cycles.
■ Double-Buffer BitBLT registers (BitBLAST)	✓	❒ Allows one BitBLT register to be set up while another BitBLT register is executing; eliminates BitBLT setup latency.
■ Optimized PCI host interface	PCI v2.1; 33 MHz	❒ High-performance industry-standard interface.
■ PCI bus retry	✓	❒ Automatically monitors the bus for an opening to transmit multimedia data.
■ Multiple PCI apertures	✓	❒ Accelerates PCI bus master video transfers. Dedicated aperture for multimedia use, while other apertures service normal PCI traffic.
■ Optimized write buffer	32-bit × 8-level-deep	❒ Sized to optimize PCI burst bandwidth.
■ Burst support	✓	❒ Significantly enhances PCI bandwidth.
■ Proprietary FasText™ text acceleration	✓	❒ Maintains true VGA compatibility (two fonts in plane 2). ❒ Enables high refresh rate in text display modes with 800 × 600 DSTN flat panels.
Multimedia Video		
■ ZV-Port (V-Port™)	✓	❒ Allows flexible after-market multimedia upgrade of portable PCs. ❒ Off-loads video bandwidth from the PCI bus, which improves system performance.
■ Independent color adjustment of graphics display and video window; independent brightness control of video window	✓	❒ Normalizes color fidelity between vendor's flat panels and other display device types. ❒ Allows end user to adjust color and brightness to their preference in the video window and the graphics background.
■ Hardware source (transparent BitBLT) and destination (occlusion) color and chroma key support to 1024 × 768	✓	❒ Allows video data to maintain frame data rate when video window is occluded by graphics data. ❒ Required to accelerate video in Windows® 95 games. ❒ Source and destination color and chroma key support complies with DirectDraw™ specification.
■ Continuous X and Y interpolated scaling to 1024 × 768, scaling option to use algorithm that maintains edge sharpness during upscaling	✓	❒ Smooth upscaling of video up to 1024 × 768 while reducing image aliasing (that is, blockiness of image). ❒ Reduces host CPU bandwidth by off-loading scaling function to graphics controller. ❒ Greatly reduces PCI and memory bandwidth by transferring video in its native resolution (352 × 240 rather than 1024 × 768).
■ Color space conversion	✓	❒ Converts 16-bpp YUV to 24-bpp true-color RGB. ❒ Converts compressed 8-bpp AccuPak™ or DYUV to high-color RGB. ❒ Frees host CPU, PCI, and memory bandwidth, which would otherwise be required for color space conversion.
■ Frame buffer support for mixed formats and color depth	✓	❒ RGB, YUV, AccuPak™, and compressed YUV can coexist in the frame buffer — important because YUV, AccuPak™, and compressed YUV are more efficient formats for memory size and bandwidth. ❒ Allows the color depth of video to be independent of background graphics color depth, reducing memory and bandwidth requirements for quality video.

SOFTWARE SUPPORT

Operating System and Application Software Drivers

Software Drivers[a]	Resolution Supported	
Microsoft® Windows® v3.X Microsoft® Windows® 95	CRT Only	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024
	SimulSCAN™	640 × 480, 800 × 600, 1024 × 768
Microsoft®/Intel® DCI™	SimulSCAN	640 × 480, 800 × 600, 1024 × 768
DirectDraw™/DirectVideo™ for Windows® 95 Includes low-resolution support for game applications	SimulSCAN	320 × 200, 320 × 240, 512 × 384, 640 × 400, 640 × 480, 800 × 600, 1024 × 768
Cirrus Logic VPM (video port manager) for ZV-Port and V-Port™ solutions	SimulSCAN	640 × 480, 800 × 600, 1024 × 768
Microsoft® Windows NT™ v3.5X, 4.0	SimulSCAN	640 × 480, 800 × 600, 1024 × 768
OS/2®, WARP 4.0	CRT Only	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024
	SimulSCAN	640 × 480, 800 × 600, 1024 × 768
AutoCAD® v11, v12, Autoshade® v2.0, 3D Studio® v1, v2	CRT Only	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024
	SimulSCAN	640 × 480, 800 × 600, 1024 × 768

[a] Driver support for additional applications is provided by independent software vendors, either with specific drivers or through VESA® mode support. For more information concerning driver support, contact the software manufacturer.

BIOS

Feature	Benefit
■ 48-Kbyte VGA BIOS	❒ Provides optimum performance with VGA and VESA® extended display mode support. ❒ Provides system design options for the best combination of performance and functionality.
■ Fully IBM®-compatible VGA BIOS	❒ Compatible with the existing base of PC applications.
■ VESA® VBE (VGA BIOS extensions) v1.2, DDC-2B, and power management	❒ Compatible with industry standards for extended display mode support beyond VGA, intelligent monitor sensing, and power-management control.

Software Utilities

Utility	Function
WinMode and CLMode	Windows® 3.X and DOS utilities (available in various foreign-language translations) for configuration of graphics display modes and display device type.
	Windows® 95 utilities (available in various foreign-language translations.) – Refresh rate selection – Display device selection
OEMSI	VGA BIOS-customization utility for OEM development use.
PCLRegs	DOS-based VGA register viewer/editor for OEM development use.
V-Port™ Regs	Windows®-based VGA register viewer/editor and V-Port™/video window display-configuration utility for OEM development use.
Color balance utility for color and brightness adjustment	End-user utility allowing color and brightness adjustments of both the graphics CLUT and the video-window CLUT to compensate for both the color/brightness variations of the display device, and any color fidelity variations in the video media being displayed.

Ordering Part Number:	**CL-GD7556 – 135BC**	Where: B = Ball-Grid Array Package C = Commercial Temp. (0°C to 70°C)

TABLE OF CONTENTS

CONVENTIONS AND TRADEMARKS

This section explains the conventions and trademarks that are used in this *Hardware Reference Manual*.

Abbreviations

Abbreviation (For Unit of Measure)	Explanation of Abbreviation
bpp	bits per pixel
bps	bits per second
°C	degree celsius
fps	frames per second
Hz	hertz (cycles per second)
Kbyte	kilobyte (1024 bytes)
kHz	kilohertz (1000 hertz)
kΩ	kilohm (1000 ohms)
Mbyte	megabyte (1024 bytes)
MHz	megahertz (1000 hertz)
µF	microfarad (10^{-6} farads)
µs	microsecond (10^{-6} seconds)
mA	milliampere (10^{-3} amps)
ms	millisecond (10^{-3} seconds)
n/a	A value that is ‘not available’
ns	nanosecond (10^{-9} seconds)
pF	picofarad (10^{-12} farads)
pV	picovolt (10^{-12} volts)
tbd	A value that is ‘to be determined’

Acronyms

Acronym	Definition
AC	alternating current
.API	application program interface
ASCII	American (National) Standard Code for Information Interchange
.AVI	audio-video interleaved
BGA	ball grid array
BIOS	basic input output system
BitBLAST	bit block accelerated setup transfer
BitBLT	bit-boundary block transfer
CAD	computer-aided design
CAS	column-address strobe
CGA	Color Graphics Adapter
CLUT	color look-up table
CMOS	complementary metal-oxide semiconductor
CPU	central processing unit
CRT	cathode ray tube
DAC	digital-to-analog converter
DC	direct current
DCI	display control interface
DDC 2B	Display Data Channel level 2B
DPMS	Display Power Management Specification
DRAM	dynamic random-access memory
DSTN	dual-scan super-twist nematic
EDO	extended-data-out
EGA	Enhanced Graphics Adapter
EIAJ	Electronics Industries Association of Japan
EMI	electro-magnetic interference
EPROM	erasable programmable read-only memory
EST	edge-sharpening technology
FIFO	first in, first out
FRM	frame-rate modulation
GDI	graphical device interface
GUI	graphical user interface
GUIX	graphical user interface accelerator
HDR	hidden DAC register
HIGH-Z	high-impedance
ID	identification
JPEG	Joint Picture Experts Group
LCD	liquid crystal display
LVDS	low-voltage differential signal
MD	memory data

Acronym	Definition *(cont.)*
MDA	monochrome display adapter
MPEG	Motion Picture Experts Group
MVA™	MotionVideo™ Acceleration
n/a	not applicable
nc	no connection
NTSC	National Television Standards Committee
OEM	original equipment manufacturer
OEMSI	Original Equipment Manufacturer System Integration
PAL	Phase Alternation Line
PC	personal computer
PCI	Peripheral Component Interconnect
POST	power-on self-test
PQFP	plastic quad flat pack
PRGB	primary red, green, blue
RAM	random-access memory
RAS	row-address strobe
RGB	red, green, blue
ROM	read-only memory
ROP	raster operation
R/W	read/write
SECAM	systeme electronique couleur avec memoire
SIF	source image format
STN	super-twist nematic
SVGA	super video graphics array
tbd	to be determined
TFT	thin-film transistor
TV	television
VBE	VGA BIOS Extensions
VCO	voltage-controlled oscillator
VCR	video cassette recorder
VESA®	Video Electronics Standards Association
VGA	video graphics array
VPM	Video Port Manager
VW	video window

Pin Labeling Conventions: Logic States

The use of an asterisk (that is, the * symbol) or a pound sign (that is, the # symbol) after a signal name (for example, WE*, or WE#) indicates the signal is active-low on a bus.

Pin Labeling Conventions: Pin Numbers

Within a range of pin numbers:

- A dash (such as –) indicates the pin numbers are ascending.
- A colon (such as :) indicates the pin numbers are descending.

Tables

Within tables, a row with a double line indicates the end of the table.

Use of Numerics

Hexadecimal numbers are represented with all letters in uppercase and with a lowercase ‘h’ appended to them. For example, ‘14h’, ‘3A7h’, and ‘C000h’ are hexadecimal numbers. Numbers not indicated by an ‘h’ are decimal.

Trademarks

The following list gives registration marks and trademarks that are used in this manual.

Apple Computer, Inc.: Apple®

Cirrus Logic, Inc.:

- AccuPak™
- MVA (MotionVideo™ Acceleration)
- SimulSCAN™
- V-Port™

Intel® Corporation:

- Indeo™
- Intel®
- Pentium®

International Business Machines, Inc.:

- IBM®
- OS/2®

Microsoft®, Inc.:

- DirectDraw™
- DirectVideo™
- Microsoft®
- NT™
- Windows® 3.X
- Windows® 95

VESA® (the Video Electronics Standards Association):

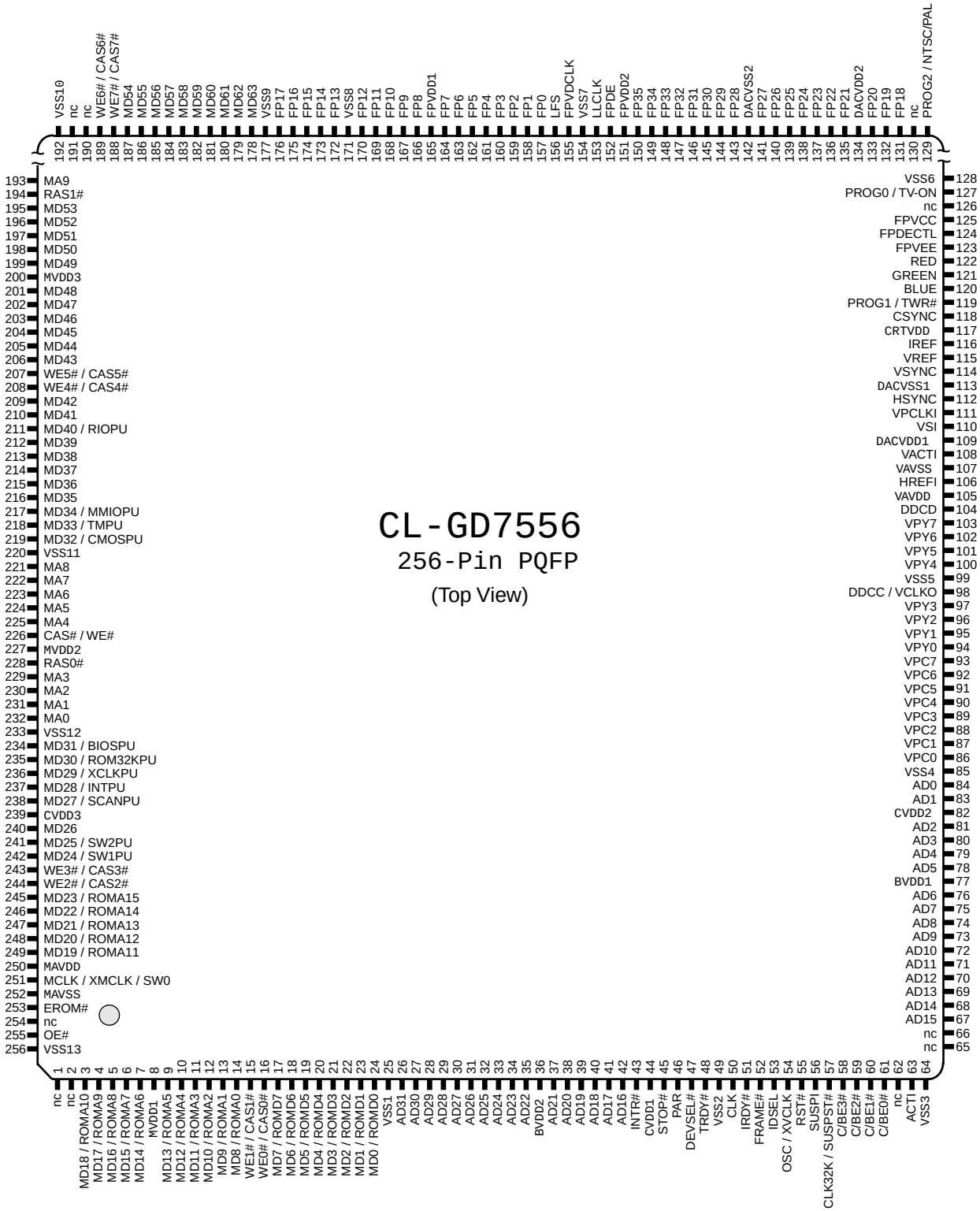
- DDC
- DPMS
- PM
- VBE
- VESA®

Other trademarks in this document belong to their respective companies.

Notes

1. PIN INFORMATION

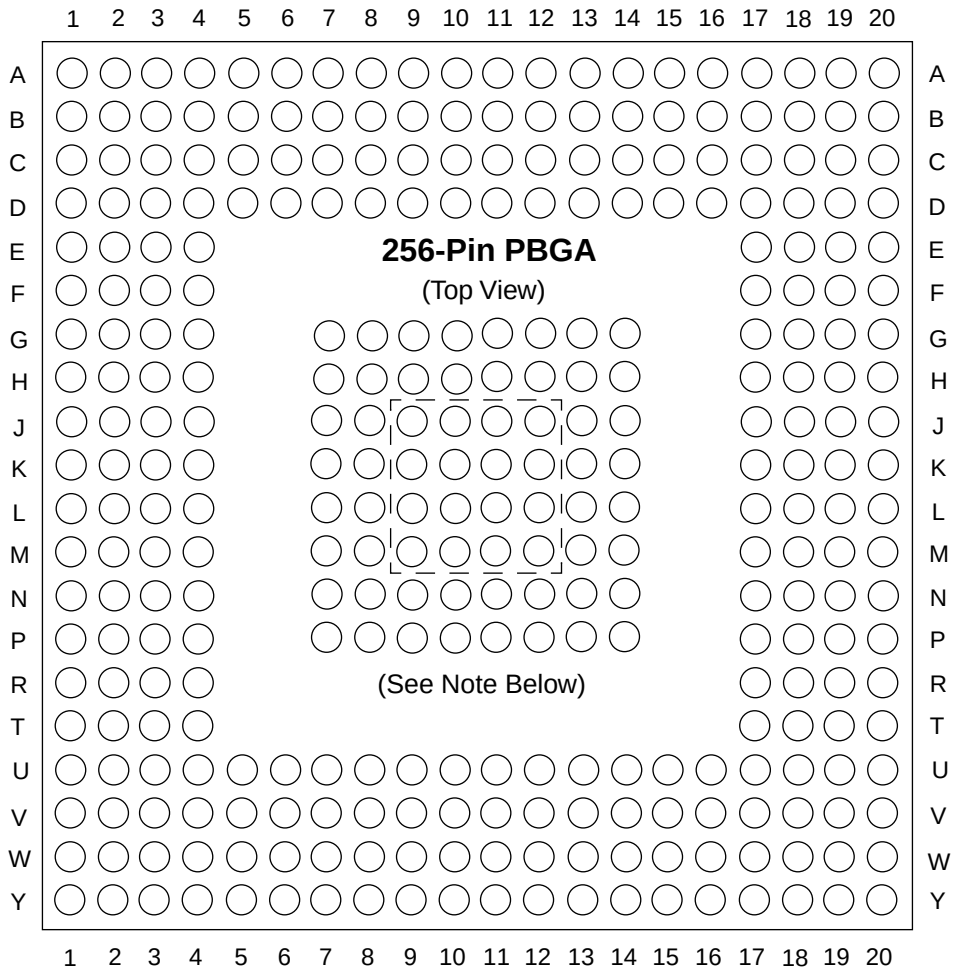
1.1 Pin Diagram of Plastic Quad Flat Package



1.2 Pin Diagram of Plastic Ball Grid Array

The pins for this 256-pin package are identified in Table 1-1.

- For detailed information about the pin identification for the Plastic Ball Grid Array (PBGA), refer to the appendixes.
- For detailed information about the ball/contact configuration and specific board layout considerations, refer to Chapter 14 and the *CL-GD7556 Application Book*.



NOTE: The ball contacts in the center of the package (either 16 or 64) are not counted in the pin count. However, they must be soldered to the digital ground plane of the motherboard to properly ground the CL-GD7556 die substrate and to facilitate heat dissipation.

1.3 Pin Tables

The following definitions apply to Table 1-1:

- Numbers in the 'PQFP Pin. No.' column refer to a Plastic Quad Flat Package.
- Numbers in the 'PBGA Ball Position' column refer to a Plastic Ball Grid Array package.
- Pins are identified with the following abbreviations and symbols:
  - I Input function
  - O Output function
  - I/O A function that is an input or output depending on the mode
  - I or O Either an input or output, depending on the pin function selected
  - OD An open-drain output that is electrically equivalent to open-collector
  - TS A tristate function that is configured as either an input, output, or high-impedance
  - S-TS A sustained-tristate output that goes to an inactive state and then to high-impedance
  - # Active-low function
- Pin names ending with 'PU' have pull-up options, which are discussed in Section 2.7.

Table 1-1. Pin Definitions

PQFP Pin No.	PBGA Ball Position	Pin Type	Pin Name
1	B1	—	No connect
2	B2	—	No connect
3	C1	I/O	MD18 / ROMA10
4	C2	I/O	MD17 / ROMA9
5	C3	I/O	MD16 / ROMA8
6	D3	I/O	MD15 / ROMA7
7	D1	I/O	MD14 / ROMA6
8	D2	Pwr	**MVDD1**
9	E3	I/O	MD13 / ROMA5
10	E2	I/O	MD12 / ROMA4
11	E1	I/O	MD11 / ROMA3
12	E4	I/O	MD10 / ROMA2
13	F3	I/O	MD9 / ROMA1
14	F2	I/O	MD8 / ROMA0
15	F1	O	WE1# / CAS1#
16	F4	O	WE0# / CAS0#
17	G3	I/O	MD7 / ROMD7
18	G2	I/O	MD6 / ROMD6
19	G1	I/O	MD5 / ROMD5
20	G4	I/O	MD4 / ROMD4
21	H3	I/O	MD3 / ROMD3
22	H2	I/O	MD2 / ROMD2

Table 1-1. Pin Definitions *(cont.)*

PQFP Pin No.	PBGA Ball Position	Pin Type	Pin Name
23	H1	I/O	MD1 / ROMD1
24	H4	I/O	MD0 / ROMD0
25	J3	GND	**VSS1**
26	J2	I/O	AD31
27	J1	I/O	AD30
28	J4	I/O	AD29
29	K3	I/O	AD28
30	K2	I/O	AD27
31	K1	I/O	AD26
32	K4	I/O	AD25
33	L3	I/O	AD24
34	L2	I/O	AD23
35	L1	I/O	AD22
36	L4	Pwr	**BVDD2**
37	M3	I/O	AD21
38	M2	I/O	AD20
39	M1	I/O	AD19
40	M4	I/O	AD18
41	N3	I/O	AD17
42	N2	I/O	AD16
43	N1	TS	INTR#
44	N4	Pwr	**CVDD1**

Table 1-1. Pin Definitions *(cont.)*

PQFP Pin No.	PBGA Ball Position	Pin Type	Pin Name
45	P3	TS	STOP#
46	P2	I/O	PAR
47	P1	TS	DEVSEL#
48	P4	TS	TRDY#
49	R3	GND	**VSS2**
50	R2	I	CLK
51	R1	I	IRDY#
52	R4	I	FRAME#
53	T3	I	IDSEL
54	T2	I	OSC / XVCLK
55	T1	I	RST#
56	T4	I	SUSPI
57	U3	I/O	CLK32K / SUSPST#
58	U2	I	C/BE3#
59	U1	I	C/BE2#
60	U4	I	C/BE1#
61	V2	I	C/BE0#
62	V1	—	No connect
63	Y1	I	ACTI
64	W1	GND	**VSS3**
65	Y2	—	No connect
66	W2	—	No connect
67	Y3	I/O	AD15
68	W3	I/O	AD14
69	V3	I/O	AD13
70	V4	I/O	AD12
71	Y4	I/O	AD11
72	W4	I/O	AD10
73	V5	I/O	AD9
74	W5	I/O	AD8
75	Y5	I/O	AD7
76	U5	I/O	AD6
77	V6	Pwr	**BVDD1**
78	W6	I/O	AD5
79	Y6	I/O	AD4
80	U6	I/O	AD3
81	V7	I/O	AD2
82	W7	Pwr	**CVDD2**
83	Y7	I/O	AD1
84	U7	I/O	AD0

Table 1-1. Pin Definitions *(cont.)*

PQFP Pin No.	PBGA Ball Position	Pin Type	Pin Name
85	V8	GND	**VSS4**
86	W8	I	VPC0
87	Y8	I	VPC1
88	U8	I	VPC2
89	V9	I	VPC3
90	W9	I	VPC4
91	Y9	I	VPC5
92	U9	I	VPC6
93	V10	I	VPC7
94	W10	I	VPY0
95	Y10	I	VPY1
96	U10	I	VPY2
97	V11	I	VPY3
98	W11	OD	DDCC / VCLKO
99	Y11	GND	**VSS5**
100	U11	I	VPY4
101	V12	I	VPY5
102	W12	I	VPY6
103	Y12	I	VPY7
104	U12	OD	DDCD
105	V13	Pwr	**VAVDD**
106	W13	I	HREFI
107	Y13	GND	**VAVSS**
108	U13	I	VACTI
109	V14	Pwr	**DACVDD1**
110	W14	I	VSI
111	Y14	I	VPCLKI
112	U14	TS	HSYNC
113	V15	GND	**DACVSS1**
114	W15	TS	VSYNC
115	Y15	O	VREF
116	U15	I	IREF
117	V16	Pwr	**CRTVDD**
118	W16	O	CSYNC
119	Y16	O	PROG1 / TWR#
120	U16	O	BLUE
121	V17	O	GREEN
122	W17	O	RED
123	Y17	O	FPVEE
124	U17	O	FPDECTL

Table 1-1. Pin Definitions *(cont.)*

PQFP Pin No.	PBGA Ball Position	Pin Type	Pin Name
125	W18	O	FPVCC
126	Y18	—	No connect
127	Y20	O	PROG0 / TV-ON
128	Y19	GND	**VSS6**
129	W20	O	PROG2 / NTSC/PAL
130	W19	—	No connect
131	V20	O	FP18
132	V19	O	FP19
133	V18	O	FP20
134	U18	Pwr	**DACVDD2**
135	U20	O	FP21
136	U19	O	FP22
137	T18	O	FP23
138	T19	O	FP24
139	T20	O	FP25
140	T17	O	FP26
141	R18	O	FP27
142	R19	GND	**DACVSS2**
143	R20	O	FP28
144	R17	O	FP29
145	P18	O	FP30
146	P19	O	FP31
147	P20	O	FP32
148	P17	O	FP33
149	N18	O	FP34
150	N19	O	FP35
151	N20	Pwr	**FPVDD2**
152	N17	O	FPDE
153	M18	O	LLCLK
154	M19	GND	**VSS7**
155	M20	O	FPVDCLK
156	M17	O	LFS
157	L18	O	FP0
158	L19	O	FP1
159	L20	O	FP2
160	L17	O	FP3
161	K18	O	FP4
162	K19	O	FP5
163	K20	O	FP6
164	K17	O	FP7

Table 1-1. Pin Definitions *(cont.)*

PQFP Pin No.	PBGA Ball Position	Pin Type	Pin Name
165	J18	Pwr	**FPVDD1**
166	J19	O	FP8
167	J20	O	FP9
168	J17	O	FP10
169	H18	O	FP11
170	H19	O	FP12
171	H20	GND	**VSS8**
172	H17	O	FP13
173	G18	O	FP14
174	G19	O	FP15
175	G20	O	FP16
176	G17	O	FP17
177	F18	GND	**VSS9**
178	F19	I/O	MD63
179	F20	I/O	MD62
180	F17	I/O	MD61
181	E18	I/O	MD60
182	E19	I/O	MD59
183	E20	I/O	MD58
184	E17	I/O	MD57
185	D18	I/O	MD56
186	D19	I/O	MD55
187	D20	I/O	MD54
188	D17	O	WE7# / CAS7#
189	C19	O	WE6# / CAS6#
190	C20	—	No connect
191	A20	—	No connect
192	B20	GND	**VSS10**
193	A19	O	MA9
194	B19	O	RAS1#
195	A18	I/O	MD53
196	B18	I/O	MD52
197	C18	I/O	MD51
198	C17	I/O	MD50
199	A17	I/O	MD49
200	B17	Pwr	**MVDD3**
201	C16	I/O	MD48
202	B16	I/O	MD47
203	A16	I/O	MD46
204	D16	I/O	MD45

Table 1-1. Pin Definitions *(cont.)*

PQFP Pin No.	PBGA Ball Position	Pin Type	Pin Name
205	C15	I/O	MD44
206	B15	I/O	MD43
207	A15	O	WE5# / CAS5#
208	D15	O	WE4# / CAS4#
209	C14	I/O	MD42
210	B14	I/O	MD41
211	A14	I/O	MD40 / RIOPU
212	D14	I/O	MD39
213	C13	I/O	MD38
214	B13	I/O	MD37
215	A13	I/O	MD36
216	D13	I/O	MD35
217	C12	I/O	MD34 / MMIOPU
218	B12	I/O	MD33 / TMPU
219	A12	I/O	MD32 / CMOSPU
220	D12	GND	**VSS11**
221	C11	O	MA8
222	B11	O	MA7
223	A11	O	MA6
224	D11	O	MA5
225	C10	O	MA4
226	B10	O	CAS# / WE#
227	A10	Pwr	**MVDD2**
228	D10	O	RAS0#
229	C9	O	MA3
230	B9	O	MA2

Table 1-1. Pin Definitions *(cont.)*

PQFP Pin No.	PBGA Ball Position	Pin Type	Pin Name
231	A9	O	MA1
232	D9	O	MA0
233	C8	GND	**VSS12**
234	B8	I/O	MD31 / BIOSPU
235	A8	I/O	MD30 / ROM32KPU
236	D8	I/O	MD29 / XCLKPU
237	C7	I/O	MD28 / INTPU
238	B7	I/O	MD27 / SCANPU
239	A7	Pwr	**CVDD3**
240	D7	I/O	MD26
241	C6	I/O	MD25 / SW2PU
242	B6	I/O	MD24 / SW1PU
243	A6	O	WE3# / CAS3#
244	D6	O	WE2# / CAS2#
245	C5	I/O	MD23 / ROMA15
246	B5	I/O	MD22 / ROMA14
247	A5	I/O	MD21 / ROMA13
248	D5	I/O	MD20 / ROMA12
249	C4	I/O	MD19 / ROMA11
250	B4	Pwr	**MAVDD**
251	A4	I/O	MCLK / XMCLK / SW0
252	D4	GND	**MAVSS**
253	B3	O	EROM#
254	A3	—	No connect
255	A1	O	OE#
256	A2	GND	**VSS13**

Table 1-2 lists the CL-GD7556 pins that connect to the corresponding pins of the specified flat panels. Pin numbers and names for specific flat panels are given in the “Panel Interface Guide” in the *CL-GD7556 Application Book*.

Table 1-2. CL-GD7556 Interface Pins to Flat Panels[a]

CL-GD7556			Flat Panel Type with Corresponding Pin Connections							
			TFT Types						STN Types	
Pin Name	PQFP Pin No.	PBGA Ball Position	TFT with 1-Pixel/Clock				TFT with 2-Pixels/Clock		Color	
			24-Bit	18-Bit	12-Bit	9-Bit	18-Bit	12-Bit	16-Bit	8-Bit
FP17	176	G17	R7	R5	R3	R2	R_A5	R_A3	SUD3	—
FP16	175	G20	R6	R4	R2	R1	R_A4	R_A2	SUD2	—
FP15	174	G19	R5	R3	R1	R0	R_A3	R_A1	SUD1	—
FP14	173	G18	R4	R2	R0	—	R_A2	R_A0	SUD0	—
FP13	172	H17	R3	R1	—	—	R_A1	—	SUD7	—
FP12	170	H19	R2	R0	—	—	R_A0	—	SUD6	—
FP31	146	P19	R1	—	—	—	R_B1	—	—	—
FP30	145	P18	R0	—	—	—	R_B0	—	—	—
FP11	169	H18	G7	G5	G3	G2	G_A5	G_A3	SLD7	SUD3
FP10	168	J17	G6	G4	G2	G1	G_A4	G_A2	SLD6	SUD2
FP9	167	J20	G5	G3	G1	G0	G_A3	G_A1	SLD5	SUD1
FP8	166	J19	G4	G2	G0	—	G_A2	G_A0	SLD4	SUD0
FP7	164	K17	G3	G1	—	—	G_A1	—	SUD5	—
FP6	163	K20	G2	G0	—	—	G_A0	—	SUD4	—
FP25	139	T20	G1	—	—	—	G_B1	—	—	—
FP24	138	T19	G0	—	—	—	G_B0	—	—	—
FP5	162	K19	B7	B5	B3	B2	B_A5	B_A3	SLD3	SLD3
FP4	161	K18	B6	B4	B2	B1	B_A4	B_A2	SLD2	SLD2
FP3	160	L17	B5	B3	B1	B0	B_A3	B_A1	SLD1	SLD1
FP2	159	L20	B4	B2	B0	—	B_A2	B_A0	SLD0	SLD0
FP1	158	L19	B3	B1	—	—	B_A1	—	—	—
FP0	157	L18	B2	B0	—	—	B_A0	—	—	—
FP19	132	V19	B1	—	—	—	B_B1	—	—	—
FP18	131	V20	B0	—	—	—	B_B0	—	—	—
FPVDCLK	155	M20	FPVDCLK				FPVDCLK		SCLK	
LLCLK	153	M18	LLCLK				—		LP	
LFS	156	M17	LFS				LFS		FLM	
FPDE	152	N17	DE				DE		—	
FPDECTL	124	U17	(Optional)				(Optional)		(Optional)	

Table 1-2. CL-GD7556 Interface Pins to Flat Panels[a] *(cont.)*

CL-GD7556			Flat Panel Type with Corresponding Pin Connections							
			TFT Types						STN Types	
Pin Name	PQFP Pin No.	PBGA Ball Position	TFT with 1-Pixel/Clock				TFT with 2-Pixels/Clock		Color	
			24-Bit	18-Bit	12-Bit	9-Bit	18-Bit	12-Bit	16-Bit	8-Bit
FP35	150	N19	—	—	—	—	R_B5	R_B3	—	—
FP34	149	N18	—	—	—	—	R_B4	R_B2	—	—
FP33	148	P17	—	—	—	—	R_B3	R_B1	—	—
FP32	147	P20	—	—	—	—	R_B2	R_B0	—	—
FP31**[b]	146	P19	—	—	—	—	R_B1	—	—	—
FP30**	145	P18	—	—	—	—	R_B0	—	—	—
FP29	144	R17	—	—	—	—	G_B5	G_B3	—	—
FP28	143	R20	—	—	—	—	G_B4	G_B2	—	—
FP27	141	R18	—	—	—	—	G_B3	G_B1	—	—
FP26	140	T17	—	—	—	—	G_B2	G_B0	—	—
FP25**	139	T20	—	—	—	—	G_B1	—	—	—
FP24**	138	T19	—	—	—	—	G_B0	—	—	—
FP23	137	T18	—	—	—	—	B_B5	B_B3	—	—
FP22	136	U19	—	—	—	—	B_B4	B_B2	—	—
FP21	135	U20	—	—	—	—	B_B3	B_B1	—	—
FP20	133	V18	—	—	—	—	B_B2	B_B0	—	—
FP19**	132	V19	—	—	—	—	B_B1	—	—	—
FP18**	131	V20	—	—	—	—	B_B0	—	—	—

[a] **Important:**
Previous documentation for the CL-GD7556 mislabeled the FP0–FP35 pins. However, in the previous documentation, within this table the interconnections for the pins were correct. The current Table 1-2 gives the correct pin names for the FP0–FP35 pins.

[b] Pin names that have two asterisks (**) also appear in the first part of this table. These pins are repeated in the second part of this table for completeness.

Table 1-3 lists the power connections for the CL-GD7556 interface pin groups. All of the power supply pins of the CL-GD7556 must receive 3.3 V ± 5%. However, the power pins must be isolated from the motherboard power plane to minimize crosstalk. Also, each of the Frequency Synthesizer power pins are further isolated from the others with a 33-ohm series resistor. See *Application Note — 7556-AN-11, Layout Guidelines* and *Application Note — 7556-AN-3, Analog Voltage Filtering Requirements* for details.

Table 1-3. Power Connections for Interface Pin Groups

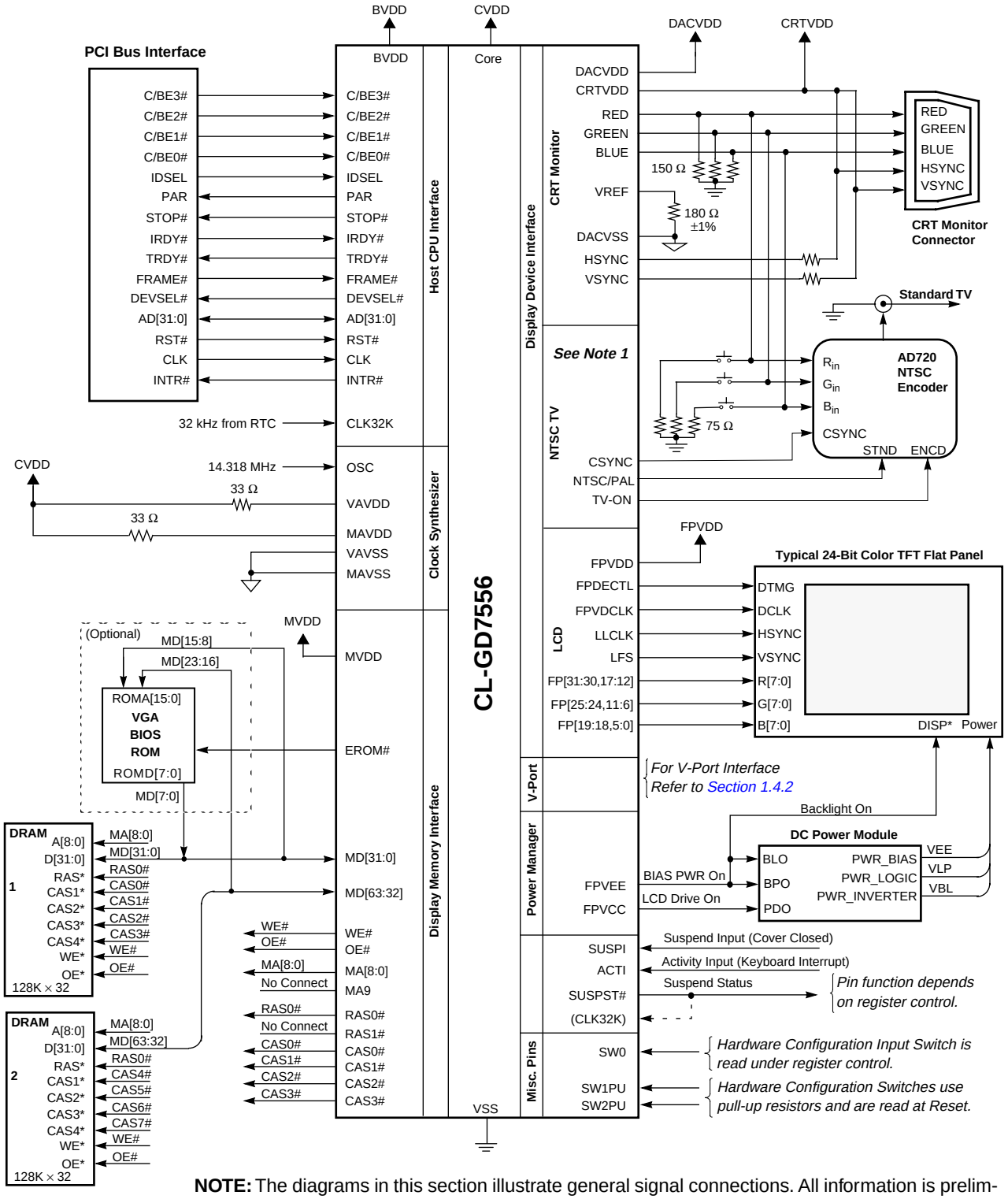
Name of Interface Pin Group		Power Pin to the Interface Pin Group		Termination Requirements[a]	CL-GD7556 PQFP Pins in Interface Pin Group
		Power Pin Name	Power Pin Number[b]		
Frequency Synthesizer	MCLK (Memory Clock)	MAVDD	250 (B4)	33 Ω Series isolation, 0.1 µF, 1.0 µF	251–252
	VCLK (Video Clock)	VAVDD	105 (V13)	33 Ω Series isolation, 0.1 µF, 1.0 µF	107
Core Logic		CVDD1	44 (N4)	0.1 µF	No external signal pins are affected by the CVDD power pins.
		CVDD2	82 (W7)	0.1 µF	
		CVDD3	239 (A7)	0.1 µF	
Host CPU Bus		BVDD1	77 (V6)	0.1 µF	26–84
		BVDD2	36 (L4)	0.1 µF	
CRT		CRTVDD	117 (V16)	0.1 µF	86–104, 106, 108, 110–112, 114, 117–119, 123–130
Digital-to-Analog (DAC)		DACVDD1	109 (V14)	0.1 µF, 1.0 µF	113, 115, 116, 120–122, 142
		DACVDD2	134 (U18)	0.1 µF, 1.0 µF	
Flat Panel		FPVDD1	165 (J18)	0.1 µF	131–133, 135–141, 143–176
		FPVDD2	151 (N20)	0.1 µF	
Display Memory		MVDD1	8 (D2)	0.1 µF, 1.0 µF	3–24, 178–238, 240–249, 253–256
		MVDD2	227 (A10)	0.1 µF, 1.0 µF	
		MVDD3	200 (B17)	0.1 µF, 1.0 µF	

[a] The capacitors are connected from the power pins (or BGA pads) to the ground plane. The capacitors should have proper high-frequency characteristics, and be mounted as close to each pin (pad) as possible.

[b] The numbers in parenthesis are the BGA pad locations.

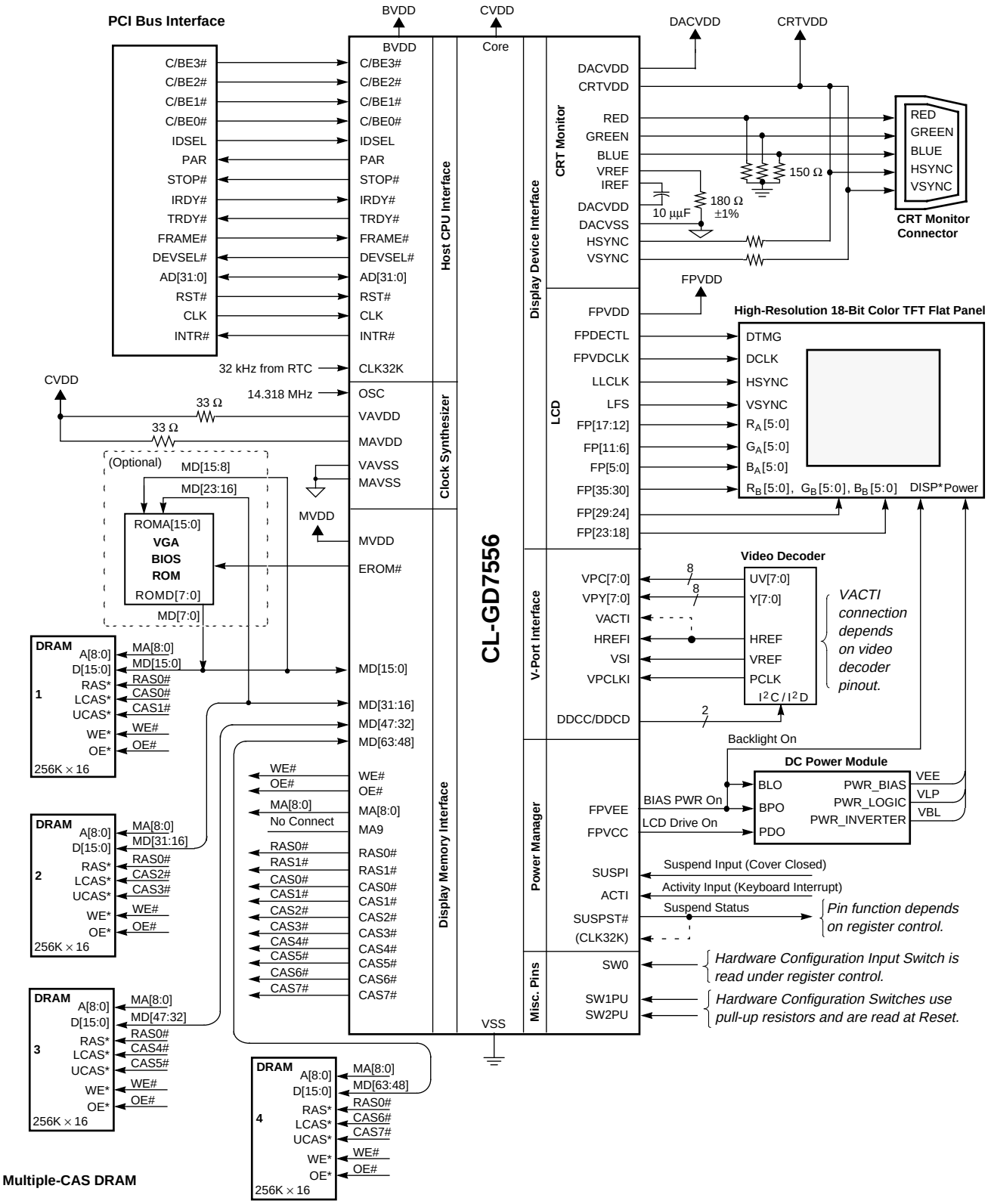
1.4 Block Diagrams: CL-GD7556 Interfaces to PCI Bus

1.4.1 1-Mbyte 128K × 32 DRAM, 24-Bit, 640 × 480 Color TFT

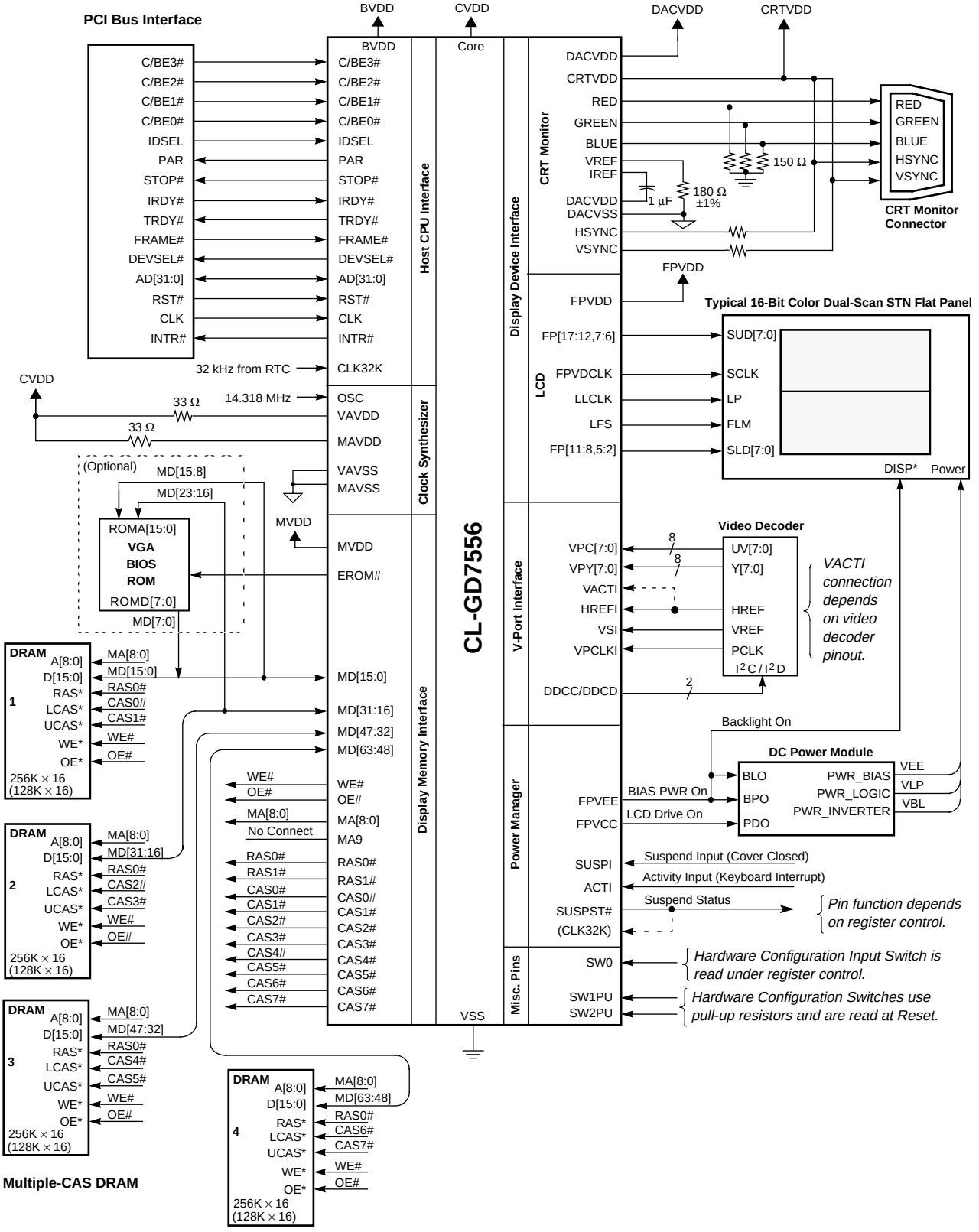


NOTE: The diagrams in this section illustrate general signal connections. All information is preliminary and subject to change. For design examples, refer to Cirrus Logic *Application Books*.

1.4.2 2-Mbyte 256K × 16 DRAM, 18-Bit Color TFT with 2-Pixels/Clock



1.4.3 2-Mbyte 256K × 16 DRAM (or 1-Mbyte 128K × 16 DRAM), 800 x 600 Color Dual-Scan



2. PIN DESCRIPTIONS

The tables in this chapter give a detailed description of the pin functions of the CL-GD7556. The pin names and pin numbers are reflected in the drawings and tables in Chapter 1. In general, the pin numbers are referenced to the PQFP version of the CL-GD7556. However, some PBGA pin numbers are shown in parenthesis (for example, “the STOP# output is on pin 45 (P3)”). For other equivalent PBGA pin numbers refer to Table 1-1 on page 1-3.

The tables are organized by the following functional categories:

The following abbreviations and symbols are used for pins in the following sections:

- I Input function
- O Output function
- I/O A function that is an input or output depending on the mode
- I or O Either an input or output, depending on the pin function selected
- OD An open-drain output that is electrically equivalent to open-collector
- TS A tristate function that is configured as either an input, output, or high-impedance
- S-TS A sustained-tristate output that goes to an inactive state and then to high-impedance
- # Active-low function
- ( ) Under the Pin Description column, within the boldface name of the pin, terms in parentheses indicate terms that are not indicated in the mnemonic for the pin name.

2.1 PCI Bus Interface

Pin Name	Pin No.	Type	Pin Description
AD[31:22], AD[21:16], AD[15:6], AD[5:2], AD[1:0]	26–35, 37–42, 67–76, 78–81, 83–84	I/O	**ADDRESS AND DATA [31:0]:** These multiplexed, bidirectional pins are used to transfer system address and data during any memory or I/O operation on the PCI bus. During the first clock of a transaction, these pins are inputs that contain the 32-bit physical byte address. During subsequent clocks, they contain data. These pins connect directly to the PCI bus AD[31:0] pins.
C/BE[3:0]#	58–61 (U2,U1, U4,V2)	I	**COMMAND AND BYTE ENABLE [3:0]#:** These active-low multiplexed inputs are used to transfer Bus Command and Byte Enables to the CL-GD7556 during any memory or I/O operation on the PCI bus. During the address phase of the operation, these pins act as inputs that define the bus command (C). For supported commands, refer to Table 2-1. During the data phase, these pins are used as active-low Byte Enable (BE#) inputs. BE0# applies to byte 0, BE1# applies to byte 1, and so forth. These pins connect directly to the PCI bus C/BE[3:0]# pins.

Table 2-1. Commands Supported

C				Command Type	Supported by CL-GD7556?
[3]	[2]	[1]	[0]		
0	0	0	0	Interrupt Acknowledge	–
0	0	0	1	Special Cycle	–
0	0	1	0	I/O Read	Yes
0	0	1	1	I/O Write	Yes
0	1	0	0	Reserved	–
0	1	0	1	Reserved	–
0	1	1	0	Memory Read	Yes
0	1	1	1	Memory Write	Yes
1	0	0	0	Reserved	–
1	0	0	1	Reserved	–
1	0	1	0	Configuration Read	Yes
1	0	1	1	Configuration Write	Yes
1	1	0	0	Memory Read Multiple	–
1	1	0	1	Dual Address Cycle	–
1	1	1	0	Memory Read Line	–
1	1	1	1	Memory Write and Invalidate	–

2.1 PCI Bus Interface *(cont.)*

Pin Name	Pin No.	Type	Pin Description
CLK	50 (R2)	I	**CLOCK:** This input is the timing reference for the CL-GD7556. This pin must be connected directly to the PCI bus CLK pin.
DEVSEL#	47 (P1)	S-TS	**DEVICE SELECT#:** This active-low sustained tristate output is driven low to indicate that the CL-GD7556 is responding to the current PCI bus cycle.
FRAME#	52 (R4)	I	**FRAME#:** This active-low input indicates the beginning and duration of a PCI bus transaction. When FRAME# goes: • *Low*, it indicates the beginning of a PCI bus transaction. While FRAME# is low, data transfers continue. • *High*, the PCI bus transaction is in its final data phase.
IDSEL	53 (T3)	I	**INITIALIZATION DEVICE SELECT:** This input, during configuration PCI bus read and write cycles, is used as a chip select in place of the upper 24 address lines.
INTR#	43 (N1)	O-TS	**INTERRUPT REQUEST#:** This active-low tristate output is controlled by CRT Controller register CR11[3:0]. When low, it indicates the CL-GD7556 has reached the end of an active field. The transition occurs at the beginning of the bottom border. This pin is inactive when there is a pull-up resistor on MD28 / INTPU.
IRDY#	51 (R1)	I	**INITIATOR READY#:** This active-low input establishes a handshake between the CL-GD7556 and PCI bus so that the CL-GD7556 can detect the end of a cycle. The CL-GD7556 inserts wait states until both IRDY# and TRDY# are low.
PAR	46 (P2)	I/O	**PARITY:** This bidirectional pin provides even parity across AD[31:0] and C/BE[3:0]#. The CL-GD7556 samples this signal during PCI bus write cycles and transmits the correct parity for PCI bus read cycles.
RST#	55 (T1)	I	**RESET#:** This active-low input, when low, initializes the CL-GD7556 to a known state. The trailing (rising) edge of this input loads Extension registers SR22[7:0] and SR24[7,2:1] with the data on MD[40,34:24], which is determined by internal pull-down resistors or optional external pull-up resistors.
STOP#	45 (P3)	S-TS	**STOP#:** This active-low sustained tristate output, when low, requests the PCI bus master to stop the current transaction.
TRDY#	48 (P4)	S-TS	**TARGET READY#:** This active-low sustained tristate output is connected to the PCI TRDY# input. When low, it indicates the end of a CL-GD7556 PCI bus cycle. (See IRDY# pin description)

2.2 Flat Panel Interface and Control Pins

The flat panel interface is determined by the type of flat panel used. For specific connection information, refer to Table 1-3 on page 1-9, and the Cirrus Logic "Panel Interface Guide" in the *CL-GD7556 Application Book.*

2.2.1 TFT Flat Panel Interface Pins

NOTE: For TFT flat panels, all references to R,G,B[0] bits refer to the least-significant bit of that color.

Pin Name	Pin Type	Pin Function	Pin Description
FP[17:12] FP[31:30] FP[11:6] FP[25:24] FP[5:0] FP[19:18]	O	R[7:2] R[1:0] G[7:2] G[1:0] B[7:2] B[1:0]	**24-BIT TFT WITH ONE PIXEL PER CLOCK:** These 24 outputs drive the red, green, and blue inputs of a 24-bit color TFT flat panel.
FP[17:12] FP[11:6] FP[5:0]	O	R[5:0] G[5:0] B[5:0]	**18-BIT TFT WITH ONE PIXEL PER CLOCK:** These 18 outputs drive the red, green, and blue inputs of an 18-bit color TFT flat panel.
FP[17:14] FP[11:8] FP[5:2]	O	R[3:0] G[3:0] B[3:0]	**12-BIT TFT WITH ONE PIXEL PER CLOCK:** These 12 outputs drive the red, green, and blue inputs of a 12-bit color TFT flat panel.
FP[17:15] FP[11:9] FP[5:3]	O	R[2:0] G[2:0] B[2:0]	**9-BIT TFT WITH ONE PIXEL PER CLOCK:** These 9 outputs drive the red, green, and blue inputs of a 9-bit color TFT flat panel.
FP[17:12] FP[11:6] FP[5:0]	O	R_A[5:0] G_A[5:0] B_A[5:0]	**18-BIT TFT WITH TWO PIXELS PER CLOCK:** These 18 outputs drive the first (A) red, green, and blue pixels of an 18-bit, 2-pixel/clock color TFT flat panel.
FP[35:30] FP[29:24] FP[23:18]		R_B[5:0] G_B[5:0] B_B[5:0]	These 18 outputs drive the second (B) red, green, and blue pixels of an 18-bit, 2-pixel/clock color TFT flat panel.
FP[17:14] FP[11:8] FP[5:2]	O	R_A[3:0] G_A[3:0] B_A[3:0]	**12-BIT TFT WITH TWO PIXELS PER CLOCK:** These 12 outputs drive the first (A) red, green, and blue pixels of a 12-bit, 2-pixel/clock color TFT flat panel.
FP[35:32] FP[29:26] FP[23:20]		R_B[3:0] G_B[3:0] B_B[3:0]	These 12 outputs drive the second (B) red, green, and blue pixels of a 12-bit, 2-pixel/clock color TFT flat panel.

2.2.2 Dual-Scan STN Flat Panel Interface Pins

Pin Name	Pin Type	Pin Function	Pin Description
FP[13:12] FP[7:6] FP[17:14]	O	SUD[7:6] SUD[5:4] SUD[3:0]	**16-BIT DUAL-SCAN STN:** These 8 outputs drive the upper data bits of an 16-bit, color dual-scan STN flat panel. Bit [0] is the least-significant bit.
FP[11:8] FP[5:2]		SLD[7:4] SLD[3:0]	These 8 outputs drive the lower data bits of an 16-bit, color dual-scan STN flat panel. Bit [0] is the least-significant bit.
FP[11:8]	O	SUD[3:0]	**8-BIT DUAL-SCAN STN:** These 4 outputs drive the upper data bits of an 8-bit, color dual-scan STN flat panel. Bit [0] is the least-significant bit.
FP[5:2]		SLD[3:0]	These 4 outputs drive the lower data bits of an 8-bit, color dual-scan STN flat panel. Bit [0] is the least-significant bit.

2.2.3 Flat Panel Control Pins

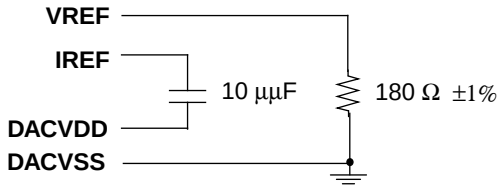
Pin Name	Pin No.	Type	Pin Description
FPDE	152 (N17)	O	**FLAT PANEL DISPLAY ENABLE:** For those flat panels that require an external display enable, this output is used to provide a display enable signal that is active when flat panel data is valid.
FPDECTL	124 (U17)	O	**FLAT PANEL DISPLAY ENABLE CONTROL:** This output is used for those flat panels that require an external display enable that is sequenced during power sequencing. For programming details, refer to Extension register CR8C[2:0].
FPVDCLK	155 (M20)	O	**FLAT PANEL VIDEO CLOCK:** This output is used to drive the flat panel shift clock. Depending on the flat panel manufacturer, on the flat panel the FPVDCLK signal can have other names, including SHIFT, CP2 (Clock Pulse 2) or SCLK (Shift Clock).
LFS	156 (M17)	O	**LCD FRAME START:** This output provides a pulse, the 'LCD Frame Start' signal, to start a new frame on flat panels. Depending on the flat panel manufacturer, on the flat panel the LFS signal can have other names, including FRAME, FLM (First Line Marker), or S (Start). **NOTE:** When Extension register CR86[6] is 1, this output is active low.
LLCLK	153 (M18)	O	**LCD LINE CLOCK:** This output is used to drive the LCD line clock. Depending on the flat panel manufacturer, on the flat panel the LLCLK signal can have other names, including LINE, LP (Line Pulse), or CP1 (Clock Pulse 1).

2.3 CRT Monitor Interface Pins

This section lists the CRT monitor interface pins. For more information on the CRT monitor interfaces, refer to the section on the CRT controller in Section 3.3.10.

Pin Name	Pin No.	Type	Pin Description
BLUE	120 (U16)	O	**BLUE:** This analog output supplies current that corresponds to the blue value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, the 8-bit value from the lookup table is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to the IREF signal as follows: $$I_{full\text{-}scale} = (63/30) \times IREF = 14\ mA$$ To maintain IBM VGA compatibility, each DAC output is typically terminated to CRT monitor ground with a 150-Ω 2% resistor. This resistor, in parallel with the 75-Ω resistor in the CRT monitor, yields a 50-Ω resistance to ground. For a 700-mV full-scale voltage, full-scale current output must be 14 mA. For details on the current source, within this table refer to the IREF signal description.
GREEN	121 (V17)	O	**GREEN:** This analog output supplies current corresponding to the green value of the pixel being displayed. To terminate this pin, within this table refer to information under BLUE.
HSYNC	112 (U14)	O	**HORIZONTAL SYNC:** This output supplies the horizontal synchronization pulse to the CRT monitor. The polarity of this output is programmable using External/General register bit MISC[6]. When MISC[6] is: • 0, HSYNC is active low, which is the default. A low-to-high transition indicates the beginning of horizontal sync time. • 1, HSYNC is active high. A high-to-low transition indicates the beginning of horizontal sync time. This pin can be connected directly to the corresponding pin on the CRT monitor connector.

2.3 CRT Monitor Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
IREF	116 (U15)	I	**(DAC) CURRENT REFERENCE:** The CL-GD7556 has an on-chip constant-current source to supply a reference for the on-chip DACs. The constant-current source is enabled when Extension register bits SR32[5] = 1 and CR8F[1] = 0. As shown in the figure in the VREF pin description, for normal operation, the IREF pin is connected through a 10-µµF filter capacitor to DACVDD, and the VREF pin is connected through a 180-Ω ±1% resistor to DACVSS.
RED	122 (W17)	O	**RED:** This analog output supplies current corresponding to the red value of the pixel being displayed. To terminate this pin, within this table refer to information under BLUE.
VREF	115 (Y15)	O	**VOLTAGE REFERENCE:** This pin is used to set the reference voltage for the on-chip current source. Normally, a 180-Ω ±1% resistor is connected from VREF to DACVSS. When an optional external constant-current source is used, this pin is not connected. 
VSYNC	114 (W15)	O	**VERTICAL SYNC:** This output supplies the vertical synchronization pulse to the CRT monitor. The polarity of this output is programmable using External/General register MISC[7]. When MISC[7] is: • 0, VSYNC is active low, which is the default. A low-to-high transition indicates the beginning of sync time. • 1, VSYNC is active high. A high-to-low transition indicates the beginning of sync time. This pin can be connected directly to the corresponding pin on the CRT monitor connector.

2.4 NTSC and PAL TV Interface Pins

This section lists the interface pins used to connect a TV (NTSC/PAL) encoder to the CL-GD7556. This mode, called TV-OUT, is controlled by Extension register CR30[6]. When CR30[6] is 0, the TV-OUT mode is disabled, and the TV-ON and NTSC/PAL pins are defined as programmable output pins PROG0 and PROG2 respectively. When CR30[6] is set to 1, the TV-OUT mode is enabled, and these pins are active. Since the RED, GREEN and BLUE pins are used by both the CRT monitor and the TV encoder, extra resistors may be required when a TV encoder is installed to maintain the reference load for the DAC. See Blue Video description below, and Section 1.4.1 for a schematic of the typical resistor connections.

Pin Name	Pin No.	Type	Pin Description
BLUE	120 (U16)	O	**BLUE VIDEO:** This analog output supplies current that corresponds to the **blue** value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, the 8-bit value from the lookup table is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to the IREF signal as follows: $I_{full\text{-}scale} = (63/30) \times IREF = 14\ mA$ To maintain the required 14 mA DAC output current, each DAC output pin is typically terminated with 50 ohms to ground. Each R,G,B output pin is terminated to DACVSS with a 150-Ω 2% resistor. An additional parallel resistor of 75-Ω is usually supplied by the CRT monitor to yield an equivalent 50-Ω resistance to ground. If the R,G,B inputs to the TV-encoder chip are high impedance, the additional 75-Ω termination resistance is added on the motherboard using Q switches to maintain the required 50-Ω load.
CSYNC	118 (W16)	O	**COMPOSITE SYNC:** This output supplies the composite SYNC signal for the analog TV (NTSC/PAL) encoder. This output pin is controlled by CR30[6]. When CR30[6] is: • 0, TV-OUT mode is disabled, and this pin is not active. • 1, TV-OUT mode is enabled, and this pin provides the CSYNC signal to the TV encoder. The encoding format is chosen by CR30[2]; see NTSC/PAL pin description below.
GREEN	121 (V17)	O	**GREEN VIDEO:** This analog output supplies current corresponding to the **green** value of the pixel being displayed. To terminate this pin, refer to information under BLUE VIDEO within this table.

2.4 NTSC and PAL TV Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
NTSC/PAL	129 (W20)	O	**NTSC/PAL ENCODING SELECTION:** This output is used to select the required NTSC or PAL TV encoding format. This function is controlled by CR30[6,2]. When CR30[6] is: • 0, TV-OUT is disabled, and this pin is the PROG2 output. • 1, TV-OUT is enabled, and the level on this pin is controlled by CR30[2]. When CR30[2] is: — 0, this pin is low, and CSYNC is generated in PAL format. — 1, this pin is high, and CSYNC is generated in NTSC format.
RED	122 (W17)	O	**RED VIDEO:** This analog output supplies current corresponding to the **red** value of the pixel being displayed. To terminate this pin, refer to information under BLUE VIDEO within this table.
TV-ON	127 (Y20)	O	**TV-ON:** This pin is used to enable an external TV encoder chip. This function is controlled by CR30[6,3]. When CR30[6] is: • 0, TV-OUT is disabled, and this pin is the PROG0 output. • 1, TV-OUT is enabled, and the level on this pin is controlled by CR30[3]. When CR30[3] is: — 1, this pin is high. — 0, this pin is low.

2.5 Dual-Frequency Synthesizer Interface Pins

For more information on the dual-frequency synthesizer, refer to Section 3.3.23.

Pin Name	Pin No.	Type	Pin Description
CLK32K	57 (U3)	I	**32-kHz CLOCK:** When Extension register CR8D[4] is: • 0, the CLK32K / SUSPST# pin is configured for CLK32K. In this case, this pin functions as an input that must be connected to an externally supplied 32-kHz clock signal. This signal is used for memory refresh during Suspend mode and panel sequencing. • 1, the CLK32K / SUSPST# pin is configured for SUSPST#. (For information on the SUSPST# pin function, refer to Section 2.11.)
MCLK	251 (A4)	O	**MEMORY CLOCK:** When MD29 / XCLKPU pin 236 (D8): • *Does not have a pull-up resistor connected*, the MCLK / XMCLK / SW0 pin is configured according to the settings on Extension register bits SR23[2,0]. When these bits are set for the MCLK function, MCLK is derived internally. *The MCLK pin function is intended primarily for test purposes.* • *Has a pull-up resistor connected*, the MCLK / XMCLK / SW0 pin is configured for XMCLK. (Within this table refer to pin name XMCLK.)
OSC	54 (T2)	I	**OSCILLATOR:** When MD29 / XCLKPU pin 236 (D8): • *Does not have a pull-up resistor connected*, the OSC / XVCLK pin is configured for the OSC function, and VCLK is derived internally. In this case, the OSC / XVCLK input pin supplies the reference frequency for the dual-frequency synthesizer. It requires an input frequency of 14.318 MHz ± 0.01% with a duty cycle of 50% ± 10%. • *Has a pull-up resistor connected*, the OSC / XVCLK pin is configured for XVCLK. (Within this table refer to pin name XVCLK.)
SW0	251 (A4)	I	**SWITCH 0:** For information on the SW0 pin function of the SW0 / MCLK / XMCLK pin, refer to Section 2.10.
VCLKO	98 (W11)	O	**VIDEO CLOCK OUTPUT:** When Extension register bit SR23[4] is: • 0, the DDCC / VCLKO pin is configured for DDCC. (For information on the DDCC pin function, refer to Section 2.7.) • 1, the DDCC / VCLKO pin is configured for VCLKO. In this case, this pin functions as an output so that VCLK can be read externally. *The VCLKO pin function is intended only for test purposes.*

2.5 Dual-Frequency Synthesizer Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
XMCLK	251 (A4)	I	**EXTERNAL MEMORY CLOCK:** When MD29 / XCLKPU pin 236 (D8): • *Does not have a pull-up resistor connected*, the MCLK / XMCLK / SW0 pin is configured according to the settings on Extension register bits SR23[2,0]. When these bits are set for the MCLK function, MCLK is derived internally. *The MCLK pin function is intended primarily for test purposes.* • *Has a pull-up resistor connected*, the MCLK / XMCLK / SW0 pin is configured for XMCLK, an external clock input. In this case, MCLK is driven by an input on the MCLK / XMCLK / SW0 pin. *The XMCLK pin function is intended only for test purposes.*
XVCLK	54 (T2)	I	**EXTERNAL VIDEO CLOCK:** When MD29 / XCLKPU pin 236 (D8): • *Does not have a pull-up resistor connected*, the OSC / XVCLK pin is configured for the OSC function, and VCLK is derived internally. For more information, within this table refer to pin name OSC. • *Has a pull-up resistor connected*, the OSC / XVCLK pin is configured for XVCLK, an external clock input. In this case, instead of VCLK being derived internally, it is driven by an input on the OSC / XVCLK pin. *This pin function is intended only for test purposes.*

2.6 Display Memory Interface Pins

For more information on display memory, refer to Section 3.2.2, Section 3.3.6, and the appendixes.

Pin Name	Pin No.	Type	Pin Description
CAS# / WE#	226 (B10)	O	**COLUMN ADDRESS STROBE# / WRITE ENABLE#:** This active-low output is used to control whether CAS# (or WE#) inputs from MA[9:0] are latched into the DRAMs. The pin function depends on the state of Extension register SRF[0]. When SRF[0] is: • 0, the CL-GD7556 is configured for multiple-WE# DRAMs and: — Pin 226 is defined as CAS# and must be connected to the CAS# inputs of the DRAMS. — Pins 188–189, 207–208, 243–244, and 15–16 are defined as WE[7:0]# respectively. • 1, the CL-GD7556 is configured for multiple-CAS# DRAMs and: — Pin 226 is defined as WE# and must be connected to the WE# inputs of the DRAMS. — Pins 188–189, 207–208, 243–244, and 15–16 are defined as CAS[7:0]# respectively.
CAS[7:6]#, CAS[5:4]#, CAS[3:2]#, CAS[1:0]#	188-189, 207-208, 243-244, 15-16	O	**COLUMN ADDRESS STROBE [7:0]# / WRITE ENABLE [7:0]#:** These active-low outputs are used to latch the CAS# (or WE#) inputs from MA[9:0] into the DRAMs. The pin functions depend on the state of Extension register SRF[0]. (For more information, refer to the previous pin description of CAS# / WE#.)
WE[7:6]#, WE[5:4]#, WE[3:2]#, WE[1:0]#	188-189, 207-208, 243-244, 15-16	O	
MA9, MA[8:4], MA[3:0]	193, 221-225, 229-232	O	**MEMORY ADDRESS [9:0]:** These outputs drive the address inputs of the DRAMs. **NOTE:** In certain configurations, the MA9 (pin 193) output is not connected. For sample DRAM configurations, refer to the block diagrams of Section 1.4 on page 1-10.
MD[63:54], MD[53:49], MD[48:43], MD[42:32], MD[31:27], MD[26:24], MD[23:19], MD[18:14], MD[13:8], MD[7:0]	178-187, 195-199, 201-206, 209-219, 234-238, 240-242, 245-249, 3-7, 9-14, 17-24	I/O	**MEMORY DATA [63:0]:** These bidirectional pins are used to transfer data between the CL-GD7556 and display memory. These pins must be connected to the data pins of the display memory DRAMs. For sample DRAM configurations, refer to the block diagrams of Section 1.4.

2.6 Display Memory Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
OE#	255 (A1)	O	**OUTPUT ENABLE#:** This active-low output is used to control the Output Enable inputs of the DRAMs. This pin must be connected to the OE# pins of all the DRAMs in the display memory array.
RAS[1:0]#	194, 228 (B19, D10)	O	**ROW ADDRESS STROBE [1:0]#:** These active-low outputs are used to latch the row address from MA[9:0] into the DRAMs. Each RAS pin is used for one bank of memory, for a total of two banks. Extension register bit SRF[7] selects one or two banks of memory. When SRF[7] is: • 0, one bank of memory is selected, and it is controlled by RAS0#. • 1, two banks of memory are selected, with the second bank controlled by RAS1#. These pins must be connected to the RAS# pins of all the DRAMs in each bank of the display memory array.
WE#		O	**WRITE ENABLE#:** For information on WE# output pins, within this table refer to CAS# pin descriptions.

2.7 V-Port Interface Pins

The CL-GD7556 is normally configured to support the V-Port signals in this section. However, this port is not enabled until Extension register CR51[3] is set to 1. (For control of the V-Port functions, refer to Extension registers CR50–CR5F.)

Pin Name	Pin No.	Type	Pin Description
DDCC	98 (W11)	OD	**DISPLAY DATA CHANNEL CLOCK:** When Extension register bit SR23[4] is: • 0, the DDCC / VCLKO pin is configured for DDCC. In this case, this pin functions as an open-drain (open-collector) output that provides the serial data that is sent through the DDC channel to communicate with external TV and MPEG encoder/decoder devices. When the V-Port is enabled, the level on this pin is set by Extension register SR8[0], and it is read back on SR8[2]. • 1, the DDCC / VCLKO pin is configured for VCLKO. (For information on the VCLKO pin function, refer to Section 2.5.)
DDCD	104 (V12)	OD	**DISPLAY DATA CHANNEL DATA:** This open-drain (open-collector) output provides the serial data that is sent through the DDC channel to communicate with external TV and MPEG encoder/decoder devices. When the V-Port is enabled, the level on this pin is set by Extension register SR8[1], and it is read back on SR8[7].
HREFI	106 (W13)	I	**HORIZONTAL REFERENCE INPUT:** This input is from an external video source horizontal synchronization signal.
VACTI	108 (V13)	I	**VIDEO (DATA) ACTIVE INPUT:** When this pin is: • *Not used*, connect this pin to the HREFI pin. • *Used*, the input for this pin typically comes from a video decoder chip, such as the CL-PX4072.
VPC[7:0], VPY[7:4] VPY[3:0]	93:86 (V10, U9, Y9, W9, V9, U8, Y8, W8) 103:100 97:94 (Y12, W12, V12, U11, V11, U10, Y10, W10)	I I	**V-Port (PIXEL DATA) VPC[7:0], VPY[7:0]:** When the V-Port is enabled (that is, Extension register SR24[7] = 0, which is the default), these inputs are used to provide a total of 16 bits of data from the V-Port. • In a 16-bit/pixel V-Port configuration, the VPC inputs provide chrominance data bits, and the VPY inputs provide luminance data. • In an 8-bit/pixel V-Port configuration, all the data enters through the VPY inputs. The chrominance data (U and V) is loaded on one clock edge, and the luminance data (Y) is loaded on the opposite clock edge.

2.7 V-Port Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
VPCLKI	111 (Y14)	I	**V-Port CLOCK INPUT:** This input comes from a video source pixel clock. This video clock input clocks video data from an external video decoder into the CL-GD7556.
VPY[7:4], VPY[3:0]	103:100 97:94	I	**V-Port (PIXEL DATA) VPY[7:0]:** For the description of the VPY pins within this table refer to pin name VPC.
VSI	110 (W14)	I	**VERTICAL SYNC INPUT:** This input is from an external video source vertical sync.

2.8 Configuration Input Pins

For all configuration input pins, their state can be latched under either hardware or software control. When the configuration input pins are under:

- *Hardware control*, all external pull-up resistors on the memory data pins (MD[40:24]) have their state read and latched by the CL-GD7556 only during hardware reset. (The external pull-up resistors have a value that ranges from 4.7-kΩ to 10-kΩ .)
- *Software control*, any low-to-high-to-low (that is, 0-1-0) transition of Extension register bit SR24[3] allows the state of all external pull-up resistors on the memory data pins (MD40:24), to be read and latched by the CL-GD7556 at any time.
  - — Software control is used whenever it is desired to read configuration pins independent of system reset.
  - — In particular, software control is appropriate when the system reset pulse is too short to read the switches that have large pull-up or pull-down resistance.

Pin Name	Pin No.	Type	Pin Description
BIOSPU	234 (B8)	I	**(ON-CHIP PCI) BIOS PULL-UP:** When this input pin is: • *Not connected* to a pull-up resistor, the CL-GD7556 does not have on-chip BIOS support. • *Connected* to a pull-up resistor, a logic high is read during system reset, and Extension register bit SR22[4] is set to 1. This high level configures the CL-GD7556 to enable on-chip PCI BIOS support. For more information, refer to Section 2.9.
CMOSPU	219 (A12)	I	**PCI-Bus CMOS Threshold Enable:** When this input is: • *Not connected* to an external pull-up resistor, most of the PCI-Bus pads are configured for a TTL threshold. (The exception is the PCI-Bus CLK pad, which is always set for a CMOS threshold.) • *Connected* to a pull-up resistor, a logic high is read during system reset, and Extension register bit SR22[5] is set to 1 which configures the PCI-Bus pads for a CMOS threshold.
INTPU	237 (C7)	I	**INTERRUPT (DISABLE) PULL-UP:** When this input pin is: • *Not connected* to a pull-up resistor, the Interrupt Request (INTR#) pin functions normally, and External/General register bit PCI3C[8] is 1. • *Connected* to a pull-up resistor, a logic high is read during system reset, Extension register bit SR22[1] is set to 1, and External/General register bit PCI3C[8] is cleared to 0. When PCI3C[8] is 0, the Interrupt Request function of the INTR# pin 43 (N1) is disabled, and the INTR# pin must not be connected. In other words: if there is a pull-up resistor on pin 237 (C7), the INTR# pin 43 (N1) must not be connected.

2.8 Configuration Input Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
MMIOPU	217 (C12)	I	**MEMORY-MAPPED I/0 PULL-UP:** When this input pin is: • *Not connected* to a pull-up resistor, the CL-GD7556 does not support memory-mapping. • *Connected* to a pull-up resistor, a logic high is read during system reset, and Extension register bit SR22[7] is set to 1. This high level configures the CL-GD7556 to enable memory-mapping of the VGA registers. This configuration supports non-PC-type host CPU buses such as the PowerPC. **NOTE:** This memory-map I/O function is not the same as, and must not be confused with, the BitBLT memory-map I/O function.
RIOPU	211 (A14)	I	**RELOCATABLE I/O PULL-UP:** When this input pin is: • *Not connected* to a pull-up resistor, the CL-GD7556 does not support relocatable I/O. • *Connected* to a pull-up resistor, a logic high is read during system reset, and External/General register bit PCI14[0] is set to 1. This high level configures the CL-GD7556 to enable the PCI relocatable I/O effect.
ROM32KPU	235 (A8)	I	**32-KBYTE ROM PULL-UP:** When this input pin is: • *Not connected* to a pull-up resistor, a default 64-Kbyte EPROM BIOS is selected. (Presently, a 48-Kbyte EPROM BIOS is used.) • *Connected* to a pull-up resistor, a logic high is read during system reset, and Extension register bit SR22[3] is set to 1. This high level configures the CL-GD7556 to enable support for a 32-Kbyte PCI BIOS EPROM. **IMPORTANT:** This configuration is *not* recommended for CL-GD7556 applications, since the standard Cirrus Logic VGA BIOS requires a minimum of 48 Kbytes.
SCANPU	238 (B7)	I	**(PIN)-SCAN (TEST) PULL-UP:** When this input pin is: • *Not connected* to a pull-up resistor, pin-scan testing is not available. • *Connected* to a pull-up resistor, a logic high is read during system reset, and Extension register bit SR22[0] is set to 1. This high level configures the CL-GD7556 to enable pin-scan testing. **NOTE:** To configure the PROG1 / TWR# pin 119 (Y16) for TWR#, which is used for pin-scan testing, the TMPU pin 218 (B12) must be connected to a pull-up resistor. For details on pin-scan testing, refer to the appendixes.

2.8 Configuration Input Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
TMPU	218 (B12)	I	**TEST MODE PULL-UP:** When this input pin is: • *Not connected* to a pull-up resistor, the Test mode is disabled. • *Connected* to a pull-up resistor, a logic high is read during system reset, and Extension register bit SR22[6] is set to 1. This high level configures the CL-GD7556 to enable Test mode. *This configuration is intended only for pin-scan and factory test purposes.* **NOTE:** When Test mode is enabled, the PROG1 / TWR# pin 119 (Y16) is configured for TWR#, which is used for pin-scan testing. For details on pin-scan testing, refer to the appendixes.
XCLKPU	236 (D8)	I	**EXTERNAL CLOCK PULL-UP:** When this input pin is: • *Not connected* to a pull-up resistor, the CL-GD7556 uses internal clock sources. • *Connected* to a pull-up resistor, a logic high is read during system reset, and the CL-GD7556 is configured for external clock inputs on the SW0 / MCLK / XMCLK and OSC / XVCLK pins. *This configuration is intended only for factory test purposes*.

2.9 On-Chip PCI VGA BIOS Support Pins

These pins are enabled when the following conditions are both true:

- The CL-GD7556 is configured for on-chip VGA BIOS support with a pull-up resistor on the BIOSPU pin.
- External/General register bit PCI30[0] is set to 1.

Pin Name	Pin No.	Type	Pin Description
EROM#	253 (B3)	O	**ENABLE ROM:** When the CL-GD7556 is configured for on-chip PCI VGA BIOS support, this output pin provides the active-low EPROM enable signal.
ROMA[15:11]	245-249 (C5, B5, A5, D5, C4)	O	**ROM ADDRESS [15:0]:** When the CL-GD7556 is configured for on-chip PCI VGA BIOS support, these output pins provide 16-bit address to the EPROM.
ROMA[10:6]	3-7 (C[1–3], D3, D1)		
ROMA[5:0]	9-14 (E[3:1], E4, F[3:2])		
ROMD[7:0]	17-24 G[3:1], G4, H[3:1], H4	I	**ROM DATA [7:0]:** When the CL-GD7556 is configured for on-chip PCI VGA BIOS support, these input pins provide an 8-bit wide data port from the EPROM.

2.10 Programmable-Output, Switch, and Test Mode Pins

The general-purpose programmable-output pins PROG[2:0] are used to control external peripherals for the V-Port and various test configurations. The Switch pins SW2PU, SW1PU, and SW0 are normally for VGA BIOS use.

Pin Name	Pin No.	Type	Pin Description
PROG2 PROG1 PROG0	129 (W20) 119 (Y16) 127 (Y20)	O O O	**PROGRAMMABLE [2:0]:** These pins are controlled by Extension registers CR30[6] and SR2F[7:5]. When CR30[6] is 0, these pins are enabled, and the level on these output pins is controlled by Extension register bits SR2F[7:5] respectively. When CR30[6] is set to 1, the TV-OUT mode is enabled, and pins PROG0 and PROG2 are defined as programmable output pins TV-ON and NTSC/PAL respectively. These programmable pins are normally used to control external peripheral devices and power-supply controllers. When the SR2F[7:5] bits are set to: • 0, the corresponding PROG output pin is forced low. • 1, the corresponding PROG output pin is forced high. **NOTE:** For pin-scan testing, PROG1 is configured as the TWR# pin. For more information, within this table refer to the TWR# pin name.
SW2PU	241 (C6)	I	**SWITCH 2 PULL-UP:** This pin is configured as a hardware input at reset. The level on this pin is determined by a pull-up resistor that is connected to this pin during power-on reset. When a pull-up resistor is: • *Not connected* to this pin, a 0 is stored in Extension register SR24[2]. • *Connected* to this pin, a 1 is stored in Extension register SR24[2].
SW1PU	242 (B6)	I	**SWITCH 1 PULL-UP:** This pin is configured as a hardware input at reset. The level on this pin is determined by a pull-up resistor that is connected to this pin during power-on reset. When a pull-up resistor is: • *Not connected* to this pin, a 0 is stored in Extension register SR24[1]. • *Connected* to this pin, a 1 is stored in Extension register SR24[1].
SW0	251 (A4)	I	**SWITCH 0:** This pin has multiple input functions. When this pin is configured as SW0 (that is, when Extension register SR23[0] = 0), the level on this pin is reflected in Extension register SR24[0]. When configured as SW0, this pin status is loaded into SR24[0] during every horizontal retrace period.
TWR#	119 (Y16)	O	**TEST WRITE:** When a pull-up resistor is connected to the MD33 / TMPU pin 218 (B12) at power-on reset, the PROG1 / TWR# pin is configured for TWR#. In this case, if the Pin-Scan Test mode is enabled [that is, external pull-up resistors are on both of the following pins: the MD33 / TMPU pin 218 (B12) and MD27 / SCANPU pin 238 (B7)], the TWR# pin function is used for pin-scan testing. For details on pin-scan testing, refer to the appendixes.

2.11 Power-Management Pins

For more information on power management, refer to the appendixes.

Pin Name	Pin No.	Type	Pin Description
ACTI	63 (Y1)	I	**ACTIVITY SENSE INPUT**: When Extension register CR8D[6] = 1, any low-to-high transition on this pin resets the internal Standby mode power-down timer.
CLK32K	57 (U3)	I	**32-kHz CLOCK:** When Extension register CR8D[4] is: • 0, the CLK32K / SUSPST# pin is configured for CLK32K. In this case, this pin functions as an input which must be connected to an externally supplied 32-kHz clock signal. This signal is used for memory refresh during Suspend mode and panel sequencing. • 1 (which is the default), the CLK32K / SUSPST# pin is configured for SUSPST#. (Within this table refer to pin name SUSPST#.)
FPVCC	125 (W18)	O	**FLAT PANEL VCC:** This output is part of flat panel power sequencing. This pin must be connected to the flat panel logic-power enable.
FPVEE	123 (Y17)	O	**FLAT PANEL VEE:** This output is part of flat panel power sequencing. This pin must be connected to the flat panel bias-power enable.
SUSPI	56 (T4)	I	**SUSPEND (MODE) INPUT:** A high on this internally de-bounced input initiates hardware-controlled Suspend mode. The hardware-controlled Suspend mode is the most-efficient power-saving mode for the system. This pin is enabled when Extension register CR8D[2] is set to 1. The pin polarity can be changed to active low (SUSPI#) by setting CR8D[3] to 1.
SUSPST#	57 (U3)	O	**SUSPEND (MODE) STATUS#**: When Extension register CR8D[4] is: • 0, the CLK32K / SUSPST# pin is configured for CLK32K. (Within this table refer to pin name CLK32K.) • 1 (which is the default), the CLK32K / SUSPST# pin is configured for SUSPST#. In this case, this pin functions as an active-low output, that when low, indicates the CL-GD7556 is in Suspend mode.

2.12 Ground Pins

This section lists the ground pins for the CL-GD7556. However, other sections in this chapter also list information on correct grounding procedures and must also be consulted. For more information on layout guidelines for the ground plane, refer to the application note “Layout Guidelines” in the *CL-GD7556 Application Book*.

Pin Name	Pin No.	Pin Description
DACVSS2, DACVSS1	142, 113 (R19, V15)	**DIGITAL-TO-ANALOG CONVERTER VSS GROUND [2:1]:** These two pins are used to supply ground reference to the palette DAC of the CL-GD7556. Each pin *must* be connected to the analog ground plane, which must be isolated from VSS (digital) ground.
MAVSS	252 (D4)	**MCLK ANALOG VSS GROUND:** This pin is used to supply ground reference to the memory clock synthesizer of the CL-GD7556. This pin *must* be connected to the analog ground plane, which must be isolated from VSS (digital) ground.
VAVSS	107 (Y13)	**VCLK ANALOG VSS GROUND:** This pin is used to supply ground reference to the video clock synthesizer of the CL-GD7556. This pin *must* be connected to the analog ground plane, which must be isolated from VSS (digital) ground.
VSS13,VSS12 VSS11,VSS10, VSS9,VSS8, VSS7,VSS6, VSS5,VSS4, VSS3,VSS2, VSS1	256, 233, 220, 192, 177, 171, 154, 128, 99, 85, 64, 49, 25 (A2, C8, B20, D12, F18, H20, M19, Y19, Y11, V8, W1, R3, J3)	**VSS (DIGITAL) GROUND [13:1]:** These pins are used to supply ground reference for the core logic and pin interface groups of the CL-GD7556. • Each pin *must* be connected directly to the ground plane. • When a multi-layer board is used, each VSS pin *must* be connected to the ground plane.

2.13 Power Pins

For more information on layout guidelines for the power plane, refer to the application note “Layout Guidelines” in the *CL-GD7556 Application Book.*

Pin Name	Pin No.	Pin Description
BVDD2, BVDD1	36, 77 (L4, V6)	**BUS VDD [2:1]:** These pins are used to supply +3.3 V to the bus interface pin group of the CL-GD7556. • Each pin *must* be connected directly to the VDD rail. • Each pin *must* be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. • When a multi-layer board is used, connect BVDD pins to the power plane.
CRTVDD	117 (V16)	**CRT VDD:** This pin is used to supply +3.3 V to the CRT interface pin group of the CL-GD7556. • This pin *must* be connected directly to the VDD rail. • This pin *must* be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to the pin as possible. • When a multi-layer board is used, connect the CRTVDD pin to the power plane.
CVDD3, CVDD2, CVDD1	239, 82, 44 (A7, W7, N4)	**CORE VDD [3:1]:** These three pins are used to supply +3.3 V to the internal core logic of the CL-GD7556. • Each pin *must* be connected directly to the VDD rail. • Each pin *must* be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. • When a multi-layer board is used, connect CVDD pins to the power plane.
DACVDD2, DACVDD1	134, 109 (U18, V14)	**DIGITAL-TO-ANALOG CONVERTER VDD [2:1]:** These two pins are used to supply voltage to the palette DAC of the CL-GD7556. • Each pin *must* be connected directly to the CVDD rail. • Each pin *must* be bypassed with 0.1-µF and 10-µF capacitors that have the proper high-frequency characteristics and are as close to each pin as possible. • When a multi-layer board is used, connect DACVDD pins to the power plane.

2.13 Power Pins *(cont.)*

Pin Name	Pin No.	Pin Description
FPVDD2, FPVDD1	151, 165 (N20, J18)	**FLAT PANEL VDD [2:1]:** These two pins are used to supply +3.3 V to the flat panel interface pin group of the CL-GD7556. • Each pin *must* be connected directly to the VDD rail. • Each pin *must* be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to the pin as possible. • When a multi-layer board is used, connect FPVDD pins to the power plane.
MAVDD	250 (B4)	**MCLK ANALOG VDD:** This pin is used to supply +3.3 V to the memory clock synthesizer of the CL-GD7556. • This pin *must* be connected to the CVDD rail through a 33-Ω resistor. • This pin *must* be bypassed with 0.1-µF and 10-µF capacitors that have the proper high-frequency characteristics and are as close to the pin as possible.
MVDD3, MVDD2, MVDD1	200, 227, 8 (B17, A10, D2)	**MEMORY VDD [3:1]:** These three pins are used to supply +3.3 V to the display memory interface pin group of the CL-GD7556. • Each pin *must* be connected directly to the VDD rail. • Each pin *must* be bypassed with 0.1-µF and 10-µF capacitors that have the proper high-frequency characteristics and are as close to each pin as possible. • When a multi-layer board is used, connect MVDD pins to the power plane.
VAVDD	105 (V13)	**VCLK ANALOG VDD:** This pin is used to supply +3.3 V to the video clock synthesizer of the CL-GD7556. • This pin *must* be connected to the CVDD rail through a 33-Ω resistor. • This pin *must* be bypassed with 0.1-µF and 10-µF capacitors that have the proper high-frequency characteristics and are as close to the pin as possible.

3. FUNCTIONAL DESCRIPTION

This section provides functional information and design guidelines for the CL-GD7556 low-power high-performance 64-bit video- and graphics-accelerated LCD/CRT controller.

3.1 Introduction

The CL-GD7556 provides a high-performance flat-panel/CRT-monitor graphics subsystem which provides all of the signals necessary to drive flat panels up to 1024 x 768, and it can simultaneously drive a CRT monitor with up to 1280 x 1024 resolution. It supports color depths up to 16.8 million colors in most VGA and video formats.

The CL-GD7556 uses a high bandwidth 64-bit graphics RAM interface to provide a wide range of cost-effective multimedia capabilities. These multimedia capabilities include acceleration of video playback for MPEG, Cinepak™, Indeo™, or TrueMotion™ files, as well as video capture, live-video presentation, and other video applications — all with continuous upscaling to resolutions up to 1024 × 768.

The CL-GD7556 has a 16-bit V-Port™ (video port) that supports the recently released ZV-Port standard. The V-Port takes video data directly from an external decoder device (such as the CL-PX4072) and transfers the video data stream into the display memory, bypassing the host CPU. The V-Port supports a low-cost multimedia solution without the need for external video processing hardware and additional display memory. By using a ZV-Port implementation, the V-Port can support high-quality low-cost multimedia options such as a live-video preview/capture, TV-in-a-window, hardware-assisted MPEG, and video conferencing.

The CL-GD7556 also supplies the outputs necessary to drive an NTSC or PAL television through an inexpensive TV-encoder chip. The encoder shares the same RGB outputs used by the CRT monitor. A special “composite SYNC” output is provided to control the required timing signals of the TV-encoder. The only limitation, when using the internal TV-OUT function, is that there is no SimulSCAN. When the TV-OUT is selected, no other displays can be driven.

The CL-GD7556 offers a tightly integrated, high-performance solution. Designs can be developed ranging from a relatively simple add-in daughterboard GUIX solution to an integrated portable multimedia system (capable of displaying 64-bit accelerated graphics combined with high-quality full-motion video playback or live video). The CL-GD7556 contains all the hardware necessary for the host CPU to update display memory contents, display screen refresh, and display memory refresh.

High-performance multimedia solutions can be implemented either on a motherboard or on a PC Card. A high-performance 1-Mbyte display subsystem solution can be implemented using only the CL-GD7556 and four 128K × 16 EDO (extended data out) DRAMs. A 2-Mbyte configuration can be implemented with the same basic design by substituting four pin-compatible 256K × 16 EDO DRAMs, so a single motherboard can be manufactured to address a range of product segments. By eliminating the need for an additional frame buffer for video data and providing a dedicated path to a PC Card, the CL-GD7556 V-Port enables high-quality, low-cost multimedia options such as a single-chip NTSC/PAL decoder or MPEG decoder.

High-Performance Interface and Processing Design

The CL-GD7556 has these major features and capabilities:

- 64-bit display memory interface with optimized support for EDO DRAMs, for high-performance high-resolution display modes with 64K or 16M colors. This 64-bit display memory interface offers twice the throughput of a 32-bit interface, at the same MCLK (memory clock) frequency. It can be implemented to support 1- or 2-Mbyte configurations.
- 64-bit BitBLT engine with 24-bit-per-pixel packed-pixel mode support for desktop-level GUI acceleration
  - — Programmable memory-mapped I/O
  - — BitBLT register double buffering and auto start
  - — Fast memory clock: MCLK of 80 MHz at 3.3 V
- Support for color TFT flat panels with up to 1024 × 768 resolution and color dual-scan STN flat panels with up to 800 × 600 resolution
  - — Direct connection for 24-bit TFT flat panels using 1-pixel/clock interfaces
  - — Direct connection for up to 18-bit TFT flat panels using 2-pixel/clock interfaces
  - — Improved expansion algorithm for text display modes produces smooth, attractive fonts on 1024 × 768 flat panels
  - — Automatic centering of the display image on 800 × 600 or 1024 × 768 flat panels and on a CRT monitor (when SimulSCAN is enabled)
- PCI bus interface, 32-bit data interface, and 33-MHz clock rate
  - — Compliant with the PCI bus v2.1 specification
  - — Multiple PCI apertures
  - — Optimized write buffer (32 bit × 8 levels deep)
  - — Supports extended burst cycles
  - — PCI bus retry, I/O remapping, and big-endian byte ordering for bytes, words, and doublewords for PowerPCs
- Low active power while supporting all operating modes at 3.3 V
- Active power management, including Standby and Suspend modes
- Protection against electrical flat panel damage by continuously monitoring flat panel signals
- Hardware cursor and hardware icons for all graphics display modes
- Hardware dithering and frame-rate modulation for flat panels that have a resolution up to 1024 × 768
- Integrated RAMDAC, frequency synthesizer, IREF, and filters
- Programmable gamma/color correction in High- and True-Color display modes to adjust for flat panel gamma characteristics
- Programmable video window gamma/color adjustment of video brightness, contrast, and color

- Enhanced MVA™
  - — Multi-format frame buffer with mixed-color depth capability allows handling of both RGB and YUV data formats in display memory and simultaneous display of graphics and video data at different color depths, for more efficient use of display memory
  - — Integrated color space converter
  - — Continuous horizontal and vertical interpolated upscaling to support high-quality, full-motion video playback at display time
  - — EST (edge-sharpening technology) maintains image contrast during upscaling
  - — Occlusion of a video window, using destination color or chroma keying
  - — Single-pixel alignment for a video window
  - — Support for the following color space formats:
    - — CCIR 601 specification for 4:2:2 YUV
    - — RGB 5-5-5 and RGB 5-6-5
    - — AccuPak (an 8-bit color space format output option, used by MPEG-1 software decoders and the CL-PX4072)
    - — DYUV compression (a proprietary Cirrus Logic compression algorithm for the V-Port and video window data)
  - — DirectDraw™/DirectVideo™ drivers for Windows® 95
  - — DCI (display control interface) drivers for Windows® 3.1
- 8- or 16-bit V-Port interface for dedicated video path to display memory
  - — High-performance, low-cost multimedia interface can be implemented either as a motherboard solution or as a multimedia PC Card that is compliant with the new ZV-Port standard
  - — Support for AccuPak or compressed YUV color space format options when bandwidth of display memory is limited. (The compression/decompression is transparent to application software.)
  - — V-Port Manager for DCI 1.x and DirectDraw™/DirectVideo™
  - — Eliminates the need for a separate video windowing controller and an additional frame buffer for video data, enabling cost-effective live-video and video-capturing solutions
- Support for DDC 2B (the VESA® display data channel level-2B serial interface protocol) allows serial programming interface to decoders (that is, video, audio, and MPEG devices)

3.2 Enhanced MotionVideo™ Acceleration

3.2.1 MVA Feature Set: Overview

MVA (MotionVideo Acceleration) is the proprietary Cirrus Logic architecture that enables the CL-GD7556 to incorporate a wide range of cost-effective multimedia video capabilities. These multimedia video capabilities, which can be implemented with a graphics subsystem that has 1 or 2 Mbytes of display memory, include:

- Full-screen, high-quality accelerated playback of Video for Windows .AVI (audio-video interleaved) video clips that are compressed using a CinePak™, Indeo™, TrueMotion™, or MPEG software codec (compressor/decompressor). MVA is accessed through DirectDraw™/DirectVideo™ drivers for Windows® 95 or through DCI for Windows® 3.1. This integrated capability requires no additional hardware and consequently, no incremental cost.
- A hardware MPEG decoder for video playback of MPEG files from a CD-ROM or hard disk drive. The MPEG decoder can be located either on the motherboard or as part of a PC Card enabled with the ZV-Port option. With this option, a hardware MPEG solution (for example, an MPEG decoder, 256K × 16 DRAM, and an ASIC) can be implemented at minimal cost and with minimum use of board space, since the V-Port™ and MVA eliminate the need for a separate video windowing controller and an additional frame buffer for video data.
- Realtime preview and capture of live video from an analog source (for example, a standard television set, a VCR, or camcorder). Video data from a single-chip NTSC/PAL decoder is transferred directly to display memory, where it can be previewed realtime and then sent over the host CPU bus for storage. Such a cost-effective solution can be implemented on the motherboard or as part of a PC Card enabled with the ZV-Port option.
- Playback of live video that has been sent over the host CPU bus. This option is useful for adding multimedia features to a docking station that has an interface to the notebook motherboard.

With MVA, video is displayed with 32K, 64K, or 16M colors in a video window. Simultaneously, a GUI environment (such as Windows) can run in a 256-color graphics display mode, which uses the available display memory efficiently. MVA is supported on the following types of flat panels, all of which can use the SimulSCAN option:

- 640 × 480 color TFT or dual-scan STN flat panels
- 800 × 600 color TFT or dual-scan STN flat panels
- 1024 × 768 color TFT flat panels

MVA continuously scales video data, from the original resolution of the video data as it comes from the video source up to the 1024 × 768 resolution of a full XGA display screen. As it scales, MVA maintains both the original frame data rate of the video data (typically, 24 to 30 frames per second) and the original color depth (typically, 32K, 64K, or 16M colors).

As shown in Figure 3-1, the CL-GD7556 MVA feature set consists of the front-end video pipeline, the part of display memory that is reserved for video window(s), and the back-end video pipeline.

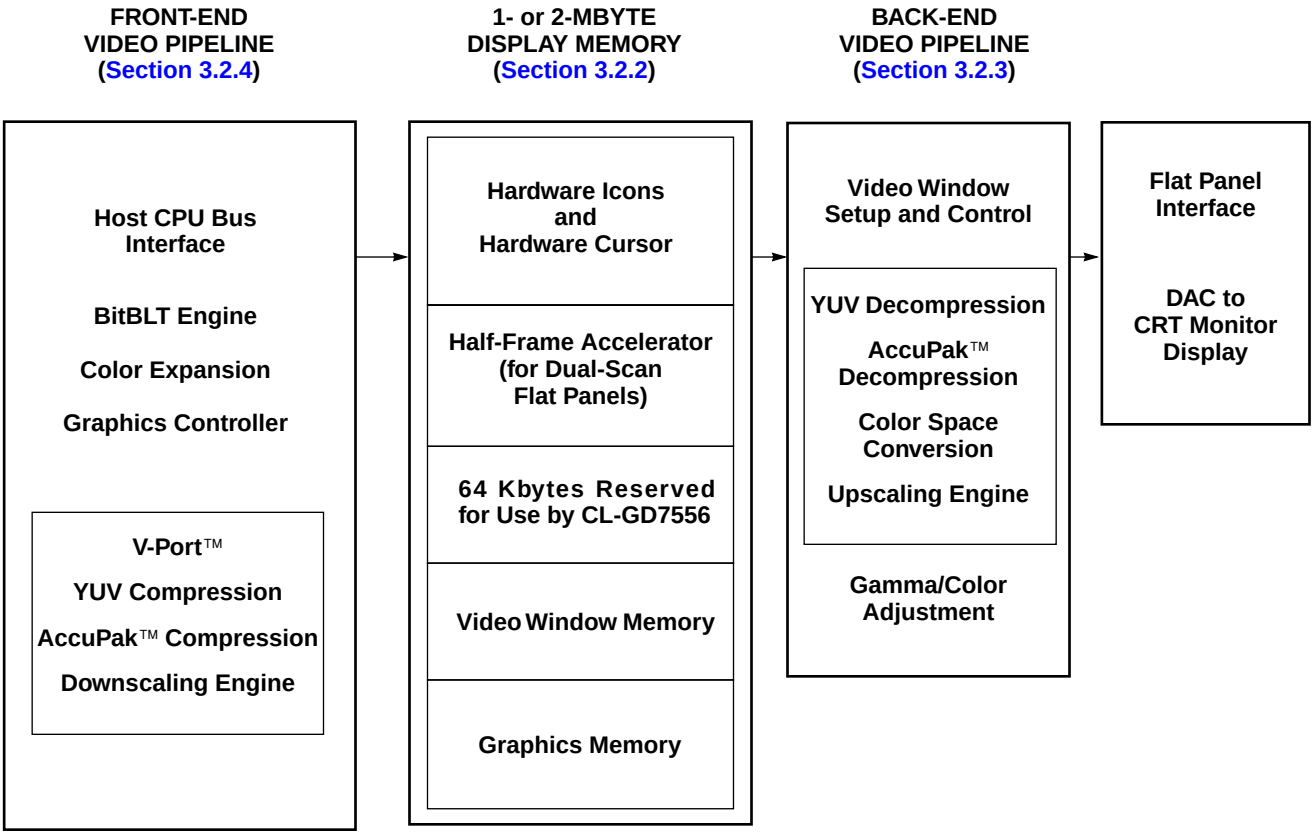


Figure 3-1. MVA™ Feature Set

3.2.2 MVA™ Feature Set: Display Memory

The CL-GD7556 display memory is organized as a shared frame buffer for surrounding-graphics and video-window data. As shown in Figure 3-2, the video window memory portion of this shared frame buffer is an area of off-screen memory that is above graphics memory (which is where data for standard and extended VGA display modes is stored).

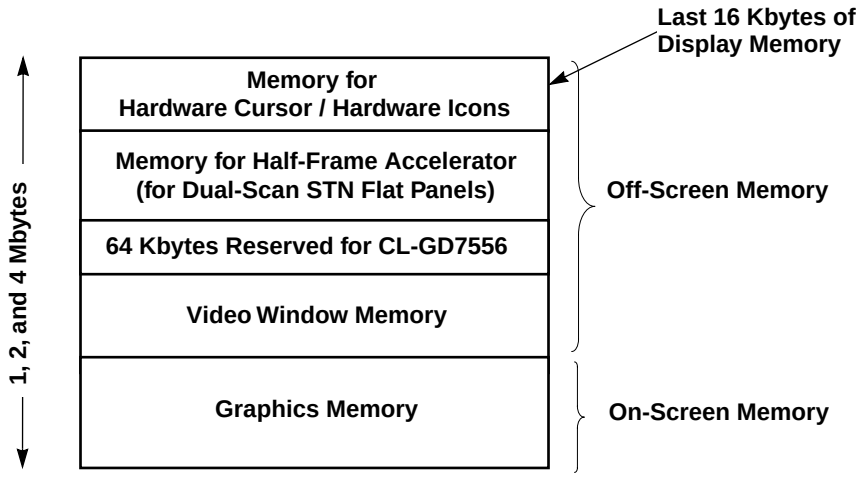


Figure 3-2. Display Memory Organization

Because the data format of video window memory is independent from the data format of graphics memory, the CL-GD7556 supports:

- Elimination of the need for a separate video windowing controller and an additional frame buffer for video data to perform the de-interlacing and timing synchronization of the video and graphics data streams. As a result, a hardware MPEG or NTSC/PAL decoder can be implemented with a minimum of cost, power consumption, and board space.
  - — For video input from an analog source (such as cable television signals, a VCR, or a camcorder), the only external hardware required is a low-cost, single-chip NTSC/PAL TV decoder (such as the CL-PX4072 or the Philips® SAA7110).
  - — For MPEG video, the only required external hardware is a single-chip MPEG decoder and MPEG frame buffer (for example, the Zoran™ 36100 or C-CUBE™ CL-480 decoders, along with a single 256K × 16 DRAM).
- A multi-format frame buffer, which allows video to be stored in more efficient color space formats than that of the graphics RGB color space format. These formats reduce the amount of display memory required to support both video and graphics.
  - — The 4:2:2 YUV color space format requires 16 bpp to store video data. However, upon color space conversion to display the data, the 4:2:2 YUV color space format yields 24 bpp RGB.
  - — The AccuPak- and DYUV-compressed data formats require 8 bpp to store video data. However, upon color space conversion to display the data, they both yield 15 bpp RGB.
- Mixed-color depths to allow a video window to display video data in a higher color depth (from 32K to 16M colors) than the surrounding graphics display mode (typically set by Windows drivers for 256 colors). As a result, memory storage and bandwidth requirements are reduced, and graphics performance is increased.

The video data for a video window is stored in video window memory, which is located in any available contiguous off-screen display memory space. The amount of display memory available for video window memory is calculated with the following equation.

$$\text{Video window memory} = \text{DMEM} - \text{GMEM} - \text{ACEL} - 16\ \text{Kbytes} - 64\ \text{Kbytes} \qquad \textbf{Equation 3-1}$$

where:

DMEM	=	Total available display memory
GMEM	=	Memory required for graphics data
ACEL	=	Memory required to support the half-frame accelerator required for dual-scan STN flat panels, when used
16 Kbytes	=	Memory reserved for hardware cursor and hardware icon
64 Kbytes	=	Memory reserved for use by the CL-GD7556

During display refresh, on a pixel-by-pixel basis, data is accessed from either video window memory or graphics memory, with options for either 1-, 2-, or 4-pixel alignment. No double accesses to display memory are required, alleviating the display memory bandwidth bottleneck. Consequently, the MVA optimizes display memory bandwidth usage while minimizing the overall display memory required. High-quality video windows can be displayed in high-resolution graphics display modes with only 1 Mbyte of display memory (typically using four 128K x 16 DRAMs).

3.2.2.1 Display Memory Color Space Formats (Extension Register CR3C)

The display memory supports the following color space formats:

- YUV color space format (typically used for MPEG or live video from a TV decoder)
- RGB 5-5-5 or RGB 5-6-5 color space formats (typically used for Indeo™, Cinepak™, or TrueMotion™)
- AccuPak™, a Cirrus Logic proprietary color space format that results from the conversion of 4:2:2 YUV source video data to 8 bpp (bits per pixel). This conversion enables the capture and display of quality color video.
  - For video data coming from the V-Port, AccuPak provides a 2:1 video data compression by encoding 4 pixels into 32 bits (averaging 8 bpp) before it is sent to display memory.
  - The CL-GD7556 accepts AccuPak video data coming from the host CPU bus. However, the data must be pre-compressed before it is sent to the CL-GD7556 for storage in the frame buffer. (Some MPEG-1 software decoders do provide video data in the AccuPak compressed format.)
  - To display the video image on either a CRT monitor or a flat panel, the CL-GD7556 fetches the AccuPak 8-bpp color space format data from display memory and decompresses it to an RGB 5-5-5 color space format prior to display.
- DYUV, a Cirrus Logic proprietary color space format that results from the compression of 4:2:2 YUV source video data to 8 bpp. This alternative to the AccuPak option is available only in the V-Port-to-Memory mode.
  - Selection of either the AccuPak format or this alternative DYUV format depends upon the source of the video data and the resultant display quality.
  - For video data coming from the V-Port, this format provides a 2:1 video data compression by encoding 4 pixels into 32 bits (averaging 8 bpp) before it is sent to display memory.
  - To display the YUV-compressed video image on either a CRT monitor or a flat panel, the CL-GD7556 fetches the 8-bpp color space format data from display memory, and decompresses it to an RGB 5-5-5 color space format.

3.2.2.2 Display Memory for Video Windows (Extension Registers CR31–CR3F)

The MVA hardware creates video windows that use off-screen memory. When a video window runs, it is displayed on top of the VGA graphics display mode data, and the hardware icons and hardware cursor are displayed on top of the video window. When necessary, the graphics data can be moved in front of the video window by using a color key.

A video window functions as an overlay image that can be positioned anywhere on the display screen. The position and resolution of a video window are programmable by using Extension registers CR31–CR3F, with options for either 1-, 2- or 4-pixel horizontal resolution and 1-scanline vertical resolution. Using SimulSCAN, a video window can be displayed simultaneously on both CRT monitors and flat panels that have one of the following resolutions:

- 640×480
- 800×600
- 1024×768

The video window resolution is determined by the source image. By using hardware scaling, the resolution of a video window can be upscaled horizontally and vertically on the display screen without a corresponding decrease in performance.

NOTE: Video windows can use several aspect ratios and are not limited to a 4:3 aspect ratio.

With MVA, the display memory becomes a multi-format display memory. As a result, different color depths and data formats can be mixed in display memory, as explained below:

- The color depth of a video window is independent of the color depth of surrounding graphics. For example, a video window can operate in a 16M-color mode, while the surrounding graphics operate in a 256-color mode.
- The data format of a video window is independent of the data format of the surrounding graphics. For example, video data in a YUV format can be stored in display memory together with graphics data in an 8-bit RGB format. In contrast to RGB data, YUV data requires less storage size. (That is, for television-quality color images, the YUV format uses 16 bpp on average to provide the same color quality as the RGB format, which uses 24 bpp.)

If the flat panel color depth is less than 24 bpp, the MVA dithering algorithm can be used by programming Extension registers CR87–CR89 to increase the displayed color depth to 24 bpp, independent of the graphics color depth.

3.2.3 MVA™ Feature Set: Back-End Video Pipeline

During display time, all video processing and conversion of color space formats is done in the MVA back-end video pipeline, which includes the following features:

- Control logic for flexible positioning of a video window
- A YUV-to-RGB color space converter. Storing video data in the YUV color space format reduces by 33% the memory storage and bandwidth requirements. (However, even though the CL-GD7556 can store data in the YUV color space format, data must be converted to the RGB color space format before it can be displayed on a flat panel or CRT monitor.)
- Decompression engines for decompressing AccuPak- and YUV-compressed video data. The CL-GD7556 converts the previously compressed AccuPak or YUV video data that comes from the V-Port (or from the MPEG-1 software decoders that support these data formats) into RGB data for display by a flat panel or CRT monitor.
- Upscaling engine that can scale a video window from the original resolution of the video data up to a 1024 x 768 display screen. During upscaling:
  - — The upscaling engine maintains the color depth and frame data rate of the source of the video data.
  - — Interpolation of both horizontal and vertical data effectively eliminates artifacts that can occur when enlarging the video. Interpolation is done on a matrix of four pixels, which allow weighting of the interpolated pixels in the x and y directions.
- Video window dithering logic. This dithering logic is independent of the dithering logic for surrounding graphics. Spatial dithering can be used to eliminate contouring in images.
- Video-window color, contrast and brightness control

3.2.3.1 Video Window Control Logic (Extension Registers CR31–CR41)

The control logic for a video window defines the dimensions and positioning of the video window as well as the color space format for the video window. It allows for flexible positioning of the video window within the surrounding graphics, with 1-, 2- or 4-pixel horizontal alignment and 1-scanline vertical alignment.

In addition, special video window control logic features include the following:

- Independent definition of the horizontal and vertical ‘start position’ of a video window
- Independent definition of the horizontal width and vertical height of a video window
- Options for reading video data from display memory with the following encoding defined in Extension register bits CR3C[3:0]:
  - — 15-bit RGB 5-5-5 and 16-bit RGB 5-6-5
  - — 4:2:2 YUV (UY0 VY1 on host CPU bus)
  - — AccuPak
  - — DYUV
- The data from display memory can be:
  - — Decompressed from either AccuPak or DYUV
  - — Upscaled from 1x to 4x
  - — Expanded by using replication or interpolation, in either the horizontal direction or vertical direction, or both
- Options for 2’s complement notation
- Brightness control of a video window independent of the surrounding graphics
- Color adjustment capability within a video window
- Simultaneous graphics and video are possible in a video window using either a color key or chroma key

3.2.3.2 Video Window YUV-to-RGB Color Space Converter

The internal YUV-to-RGB color space converter converts 4:2:2 YUV video data that is stored in the display memory to RGB 8-8-8 for display. As a result, the converter reduces memory storage and bandwidth requirements by 33% since the 4:2:2 YUV color space format, which stores only 16 bpp, is more efficient than the RGB 8-8-8 color space format, which stores 24 bpp. The converter, which is in the 'excess 128' data format, is compatible with the CCIR 601-2 specification.

3.2.3.3 Video Window Upscaling Engine (Extension Registers CR31, CR32, and CR39)

The upscaling engine, programmed in Extension registers CR31, CR32, and CR39 can continuously scale a video window from the original resolution of the video data (for example, 320×240, 352×240, or 640×480) up to a full-size display screen (for example, 640×480, 800×600, or 1024×768). During upscaling, the upscaling engine maintains the original video data color depth (typically 32K or 16M colors) and frame data rate (typically 24 to 30 frames per second).

Scaling of horizontal pixels and vertical scanlines occurs through the hardware as follows:

- The upscaling coefficient for the horizontal pixels is defined in Extension registers CR31 and CR39[7:4]. When Extension register bit CR3F[7] is:
  - — 0, the horizontal pixels are replicated
  - — 1, the horizontal pixels are interpolated
- The upscaling coefficient for the vertical scanlines is defined in Extension registers CR32 and CR39[3:0]. By using an on-chip line buffer, the CL-GD7556 can either replicate or interpolate between scanlines. When Extension register bit CR3F[6] is:
  - — 0, the vertical scanlines are replicated
  - — 1, the vertical scanlines are interpolated

EST (edge-sharpening technology) is available in Extension register bit CR40[7]. EST is used with video windows to eliminate the fuzzy edges (that is, edges that are ragged or unclear) that can occur when interpolation is used for scaling.

When sharply contrasting boundaries are encountered within a video window, between adjacent pixels, the CL-GD7556 automatically substitutes replication for interpolation. In this case, as a result, the CL-GD7556 automatically detects the difference if it is outside a predetermined limit so that replication can be substituted for interpolation.

3.2.3.4 Video Window Dithering Logic (Extension Registers CR88 and CR89)

The dithering logic for a video window defines the correct dithering matrix (that is, the number of bits for each primary red, green, blue color) to use, depending upon the combination of the color mode being displayed and the type of display device being used. The matrix selected (that is, the output resolution for dithering that is shown in Table 3-1) is determined automatically if the following are true:

- Dithering for a video window has been enabled
- The VGA BIOS is programmed for the correct flat panel type and parameters

Table 3-1. Output Resolution for Dithering Flat Panels

CR88[7:4] (Programmed by VGA BIOS)	TFT Flat Panels (No Modulation of Frame Data Rate)	STN Flat Panels (Modulation Occurs for Frame Data Rate)
'0000'	Not applicable	2-shade STN flat panels: 1 bit/PRGB[a]
'0010'	Not applicable	4-shade STN flat panels: 2 bits/PRGB
'0011'	3 bits/PRGB	8-shade STN flat panels: 3 bits/PRGB
'0100'	4 bits/PRGB	16-shade STN flat panels: 4 bits/PRGB
'0110'	6 bits/PRGB	Not applicable
'1000'	8 bits/PRGB	Not applicable

[a] PRGB = primary red, green, blue.

The resolution for input data to the dithering block is set automatically as 5 bits for each PRGB (primary red, green, blue color). However, by using Extension register bits CR89[7] and CR89[3:0], the automatic setting can be overridden and the automatic input resolution can be replaced.

The dithering logic for a video window (which is controlled by Extension register bits CR88[7:4] is independent of the dithering logic for the surrounding graphics (which is controlled by Extension registers CR87 and CR88[3:0]). Spatial dithering can be used on a flat panel to increase the color depth of a video window without affecting the dithering used for the surrounding graphics. By using spatial dithering, the CL-GD7556 can increase the flat panel color palette by creating up to 6 bits per PRGB color. When using a video window to display images, spatial dithering is effective for eliminating contouring. However, when using a video window to display text, spatial dithering can create artifacts.

3.2.3.5 Video-Window Color and Brightness Control

The CL-GD7556 provides independent adjustment controls for colors and brightness. These controls provide video windows that have consistently high-quality video playback, regardless of the type of display device being used (either CRT monitor or flat panel).

NOTE: The color and brightness control for a video window is independent of the color and brightness control for the graphics/background display.

For display devices, there is a nonlinear relationship between light intensity (that is, the amount of brightness that appears on a display screen) and the applied video signal that comes from broadcast stations or recorded media. For **CRT monitors**, this nonlinear relationship (referred to as gamma) can be expressed by the following equation, in which gamma (γ) is the exponent of the gamma-curve power-transfer function (also, see Appendix I):

$$\text{Light Intensity} = (\text{Video Signal, in mV})^{\gamma} \qquad \textbf{Equation 3-2}$$

To correct for gamma (that is, to compensate for the nonlinear relationship of a display device), a signal that is the inverse of the curve caused by the gamma can be applied to the recording or capturing of the source video data. The typical pre-corrected gamma curve equation is:

$$\text{Pre-corrected Light Intensity} = (\text{Video Signal, in mV})^{1/\gamma} \qquad \textbf{Equation 3-3}$$

For typical gamma-corrected video-intensity characteristics for CRT Monitors, refer to Figure 3-3.

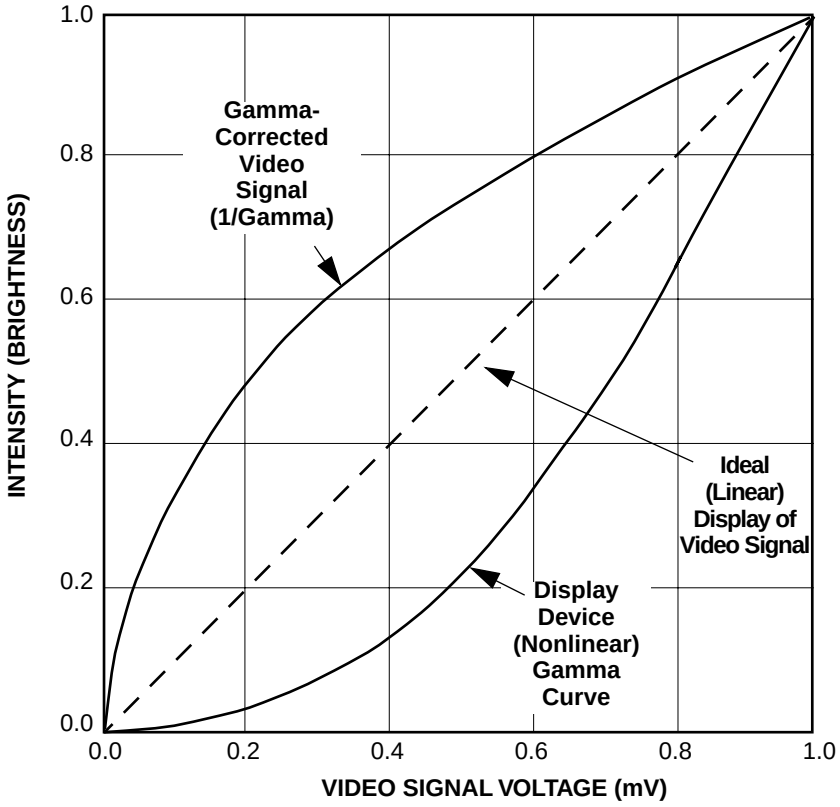


Figure 3-3. Effect of Gamma Correction – Applies to CRT Monitors only

Gamma Characteristics of Display Devices and Recording Media

Most recorded video is corrected for the typical gamma of standard television displays. The NTSC correction for gamma is 2.2, and the PAL correction for gamma is 2.8. Most professional electronic recording media are corrected for a gamma of 1.8, which is an approximation for CRT monitors. However, the color/brightness versus signal strength characteristics of a flat panel display screen are different than for a CRT monitor, and there are differences in flat panels between manufacturers. To maintain color fidelity of the source media, adjusting for individual colors and effective brightness at the final display is important. Using the CL-GD7556 'Color Balance' utility, color and brightness can be adjusted to better reproduce the original image or to meet a user's preference.

Color, Brightness and Contrast Controls

Gamma-pre-corrected images lose color intensity and brightness and look dim and flat. The CL-GD7556 uses a 24-bit by 256 deep RAM for a CLUT (color-look-up table) to redefine the R,G,B video colors of the video-window. The video-window CLUT is enabled by Extension register bit CR36[6]. Color adjustment is made by the end user with the 'Color Balance' utility to map the desired colors into the CLUT.

In addition to color adjustment, the CL-GD7556 provides brightness and contrast (or luminance) adjustments for a video window. Extension register CR35[7:0] is programmed with a 2's compliment number that either increases or decreases the luminance value of each pixel. The 'Color Balance' utility uses this register to adjust the video display for the end user.

NOTES:

1) The 'Color Balance' utility functions are explained in the *CL-GD7556 Software Reference Manual.*
2) The brightness and contrast controls for the graphics display are independent of the brightness and contrast controls for a video window, but they are controlled by the same utility. See Section 3.3.16 on page 3-44 for details.
3) On a display screen, brightness is the measure of the light intensity, and contrast is the delta between white and black colors.

3.2.4 MVA™ Feature Set: Front-End Video Pipeline

The MVA front-end video pipeline can handle simultaneous input video data streams, as long as they have the same video format (for example, 4:2:2 YUV, RGB 5-5-5, and so forth). The CL-GD7556 supports two types of video input ports: Video Input Port 1, which uses the host CPU bus to transfer video data, and Video Input Port 2, which uses the V-Port to transfer video data.

Both of these video input ports support occlusion of a video window (that is, the event that occurs when a graphics window overwrites and hides a portion of a video window). Also, both video input ports support hardware occlusion (which is also referred to as 'destination color keying'). Hardware occlusion support allows video windows to be overlapped with graphics. The 'key', which defines the area(s) on the graphics display area where the video window is to be displayed, can be defined either in the RGB color space (that is, using color keying) or the YUV color space (that is, using chroma keying).

Typically, when a video window is occluded, it maintains the same color depth and playback speed. The only limitation on destination occlusion occurs when memory bandwidth is not available, such as for high-resolution display modes or for display modes that have a high refresh rate.

In the front-end video pipeline, the video data is not processed (except for optional AccuPak or DYUV compression in the V-Port-to-Display Memory mode, and except for downscaling of the original video data). As a result, data can be transferred without the risk of imposing wait states on the host CPU bus.

Video Input Port 1: Video Data Input through the PCI Bus

With this video input port, video data input sources operate on files that are stored on mass storage devices (for example, CD-ROM or hard disk drives) that are connected to the PCI bus. The video input sources must decode the video data before it can go through the PCI bus or other bus master and into display memory. Examples of video data input sources for this video input port include the following:

- .AVI or software-decoded MPEG-1 files that are transferred to the CL-GD7556 through the PCI bus.
- DCI-compatible files that are transferred to the CL-GD7556 through the PCI bus.
- An MPEG decoder
- An NTSC/PAL TV decoder

With this video input port, occlusion can occur in two ways:

- When display memory bandwidth is sufficient, occlusion is achieved through hardware by using source or destination keying. (For more information on destination color keying, refer to Section 3.2.4.1.)
- When display memory bandwidth is limited, occlusion is achieved through software.

Video Input Port 2: Video Data Input through the V-Port™

With this video input port, the V-Port transfers video data directly from video data input sources to display memory for storage. The V-Port can be configured for either an 8-bit or a 16-bit data path. The V-Port eliminates the need for a separate video windowing controller and an additional frame buffer for video data. As a result, an inexpensive video input port can be implemented. Examples of video data input sources for this video input port include the following, both of which provide 8- or 16-bit data in a color space format:

- An MPEG decoder
- An NTSC/PAL TV decoder

With this video input port, hardware occlusion is supported, as discussed in Section 3.2.4.2.

3.2.4.1 Video Data Input through the PCI Bus

Video data can be delivered through a PCI bus from hardware/software decoders (such as MPEG, Cinepak, or Indeo decoders), that operate on files stored on mass storage devices connected to the bus (for example, CD-ROM or hard disk drives).

PCI Bus Video Data Input: Apertures (External/General Register PCI10)

The handling of different formats of pixel data is common in multimedia applications. Transforming data from one format to another format is done to reduce both data-rate and storage-area requirements and to simplify numerical manipulation. To support multiple formats simultaneously in a display memory area, the PCI bus architecture introduced the concept of 'apertures' (that is, logical partitions).

An aperture is a 'logical' view of display memory. Apertures have attributes that distinguish them from each other and which specify the actions of the CL-GD7556 as well as its driver software when accesses to the aperture are made. Among these attributes are:

- Logical pixel format — Includes color space format, and big-endian/little-endian logic
- Logical display memory organization and size — Includes base address, read-write attributes, width, and height
- Physical mapping — Location of the logical view within the frame buffer

The CL-GD7556 supports four 4-Mbyte PCI apertures of the physical 16-Mbyte linear-addressed area for display memory. (That is, multiple apertures are available only in linear addressing mode when Extension register bits SR7 [7:4] do not equal 0.)

- Aperture 0 is the standard aperture used for normal pixel data (that is, for non-video data).
- Apertures 1 and 2 are used for big-endian byte swapping (for both words and doublewords) in PowerPC implementations when Extension register bit SR2C[6] is set to 1.
- Aperture 3, which supports PCI bus retry, is used to transfer video data from PCI bus master devices.

PCI Bus Video Data Input: Universal Bus Retry

When transferring bus video data over the host CPU bus, an important feature of Aperture 3, which is the aperture used for video data transfer, is the 'universal bus retry' mechanism. When a PCI bus master attempts to send video data over the PCI bus at the same time that a BitBLT with graphics data is in progress, contention for access to the bus must be resolved.

One method for resolving the bus contention is to try to avoid it. For example, before writing data to the address for Aperture 3, a video software driver constantly polls to see if a BitBLT is in progress. However, this method of resolving bus contention is slow, and performance suffers.

A better method for resolving the bus contention is to support a PCI bus universal retry function. With this method, while a BitBLT operation is in progress in the standard aperture (that is, Aperture 0), the universal retry function automatically asserts a PCI bus retry for any memory write attempts to Aperture 3, which is used for video data. This PCI bus retry function is available even in the case of system-to-screen BitBLTs.

PCI Bus Video Data Input: Video Playback

Video playback is the display of digitally stored video from a CD-ROM or hard disk drive onto a CRT monitor and/or flat panel display screen. Typically, video playback involves the following:

- Digitally stored video data is captured at 24-bpp RGB or 16-bpp YUV color depth.
- The typical frame rate of digitally stored video data varies from 15 to 30 fps (frames per second). A frame rate of 24 to 30 fps is considered full-motion video (that is, video that appears to be smooth and natural, without excessive jerking).
- The resolution of the typical source (that is, the original resolution of the captured video clip) ranges from 160 × 120 pixels up to 352 × 240 pixels (or larger).

Through DirectDraw/DirectVideo drivers for Windows 95 and the DCI standard for Windows 3.1, the CL-GD7556 supports video playback acceleration with Video for Windows .AVI and software-decoded MPEG-1 files. Codecs supported by the CL-GD7556 include the following:

- **Cinepak™, Indeo™, and TrueMotion™ codecs:** These software-based codecs support the DirectDraw/DirectVideo and DCI standards. Typically, these codecs can capture and play back original video data with a resolution of up to 320 × 240 and with a frame data rate of up to 24 to 30 fps. The CL-GD7556 supports Cinepak, Indeo, and TrueMotion codecs, all of which provide 8-, 15-, and 24-bit RGB video data output formats.
- **MPEG-1 codecs:** The MPEG-1 SIF (source image format) standard specifies either 320 × 240 or 352 × 240 source video data that has been captured at frame data rates of up to 30 fps. Typically, MPEG-1 decoders have been hardware-based. However, software-based decoders running on a computer that has a 90-MHz or faster Pentium® host CPU can also provide acceptable video playback rates.

To enhance video playback, the following features have been added to the CL-GD7556:

- **Continuous upscaling:** Interpolated horizontal and vertical upscaling of source video during video playback.
- **Enhancements to color space conversion:** The CL-GD7556 hardware can convert AccuPak- and YUV-compressed video data that has been supplied by codecs to provide 32K-color video display outputs without using the host CPU to do the software conversion.
- **Display of mixed color depths:** While running graphics data in the Windows environment in, for example, a 256-color mode, there can be opened simultaneously a video window that displays either 32K/64K/16M colors in 15-, 16-, or 24-bpp RGB color space format.

For video playback, a video window can be upscaled both horizontally and vertically. The hardware scaling engine independently controls the horizontal and vertical scale factors. Interpolation can be selected for either the horizontal axis, or the vertical axis, or for both axes, providing a high-quality upscaled image. To display video data that is stored in a YUV color space format, the integrated YUV-to-RGB color space converter converts 4:2:2 YUV to RGB 8-8-8.

Figure 3-4 shows a 320 × 240 video clip with a 4:2:2 YUV color space format that is resized and centered to display as a 16M-color 640 × 480 video window on a 256-color 800 × 600 display screen. This video operation can be accomplished using just 1 Mbyte of display memory.

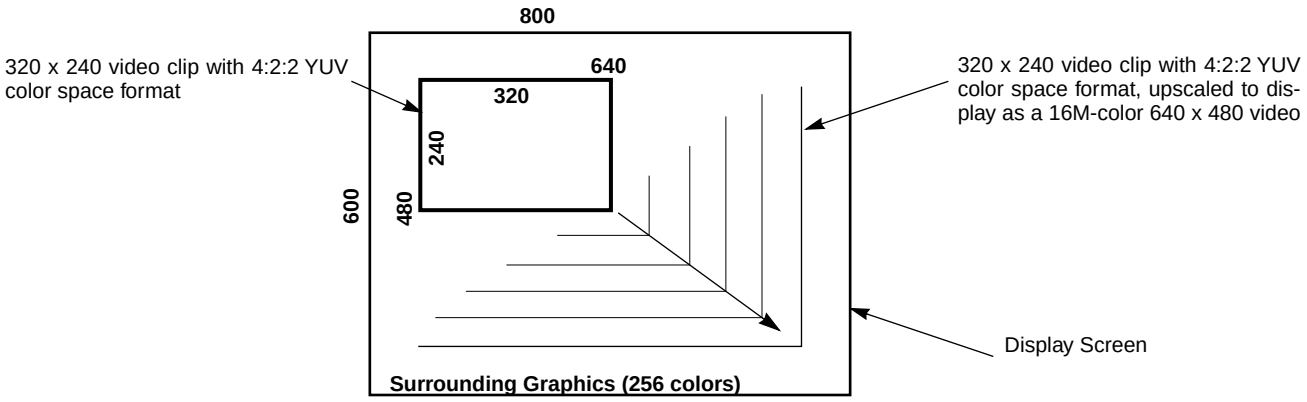


Figure 3-4. Resizing and Centering a Video Window

PCI Bus Video Data Input: Performance Tables

Table 3-2 through Table 3-5 show the video performance that is possible when video data are delivered from a video source through the PCI bus to a display screen video window of a system that has 1 or 2 Mbytes of display memory. In the Tables 3-2 through Table 3-5 the following information applies:

- The AccuPak and DYUV formats generate more than 32K colors. The 4:2:2 YUV color space format is equivalent to RGB 8-8-8 with 16M colors.
- As set by the Cirrus Logic VGA BIOS, register settings for a random-access cycle are:
  - 8 MCLKs at 66 MHz
  - 9 MCLKs at 80 MHz
- Upscaling:
  - N/A = acronym for ‘not applicable’
  - US = acronym for upscaling
  - 1:1 US = no upscaling (resolution of displayed video is the same as video stored in display memory)
  - 1:2 US = 2x upscaling
  - FS US = full screen upscaling (that is, to the full resolution of the display device)

Table 3-2. PCI Bus Video Performance with Occlusion in Flat-Panel-Only or SimulSCAN™ Modes[a]

Flat Panel[b] Resolution (pixels)	Color Depth (number of colors)	Video Data Format	MCLK (MHz)	Upscaled Video Resolution	
				Upscaling on TFT Flat Panel or in SimulSCAN™ Mode	Upscaling on DSTN Flat Panel or in SimulSCAN™ Mode
640 × 480	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
	64K	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
800 × 600	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
	64K	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
1024 × 768	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:2 through FS US
	64K	AccuPak™ or DYUV	80	1:1 through FS US	N/A
		4:2:2 YUV or RGB 5-5-5	80	1:2 through FS US	N/A

[a] The notation used in this table is discussed in the section, "PCI Bus Video Data Input: Performance Tables" on page 3-18.

[b] When the flat panel expansion mode is enabled, hardware acceleration of the video display is not supported.

Table 3-3. PCI Bus Video Performance without Occlusion in Flat-Panel-Only or SimulSCAN™ Modes[a]

Flat Panel[b] Resolution (pixels)	Color Depth (number of colors)	Video Data Format	MCLK (MHz)	Upscaled Video Resolution	
				Upscaling on TFT Flat Panel or in SimulSCAN™ Mode	Upscaling on DSTN Flat Panel or in SimulSCAN™ Mode
640 × 480	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
	64K	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
800 × 600	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
	64K	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
1024 × 768	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
	64K	AccuPak™ or DYUV	80	1:1 through FS US	N/A
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A

[a] The notation used in this table is discussed in the section, "PCI Bus Video Data Input: Performance Tables" on page 3-18.

[b] When the flat panel expansion mode is enabled, hardware acceleration of the video display is not supported.

Table 3-4. PCI Bus Video Performance with Occlusion In CRT-Only Modes[a]

CRT Monitor Resolution (pixels)	Color Depth (number of colors)	Video Data Format	MCLK (MHz)	Upscaled Video Resolution When Vertical Frequency of CRT Monitor Is:				
				60 Hz	70 Hz	72 Hz	75 Hz	85 Hz
640 × 480	256	AccuPak™ or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
	64K	AccuPak™ or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
800 × 600	256	AccuPak™ or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
	64K	AccuPak™ or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		1:2 through FS US
1024 × 768	256	AccuPak™ or DYUV	80	1:1 through FS US				1:2 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:2 through FS US			N/A
	64K	AccuPak™ or DYUV	80	1:1 through FS US	N/A	N/A	N/A	N/A
		4:2:2 YUV or RGB 5-5-5	80	1:2 through FS US	N/A	N/A	N/A	N/A

[a] The notation used in this table is discussed in the section, "PCI Bus Video Data Input: Performance Tables" on page 3-18.

Table 3-5. PCI Bus Video Performance without Occlusion In CRT-Only Modes[a]

CRT Monitor Resolution (pixels)	Color Depth (number of colors)	Video Data Format	MCLK (MHz)	Upscaled Video Resolution When Vertical Frequency of CRT Monitor Is:				
				60 Hz	70 Hz	72 Hz	75 Hz	85 Hz
640 × 480	256	AccuPak™ or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
	64K	AccuPak™ or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
800 × 600	256	AccuPak™ or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
	64K	AccuPak™ or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
1024 × 768	256	AccuPak™ or DYUV	80	1:1 through FS US				
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US				
	64K	AccuPak™ or DYUV	80	1:1 through FS US				
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US				

[a] The notation used in this table is discussed in the section, "PCI Bus Video Data Input: Performance Tables" on page 3-18.

3.2.4.2 Video Data Input through the V-Port™ (Extension Registers CR50–CR5F)

The CL-GD7556 V-Port-to-Memory mode transfers video data directly from the V-Port to display memory for storage. Effectively, the video and graphics data share the same display memory and a dedicated high-bandwidth video path is opened, eliminating the need for extra display memory and providing a low-cost, high-performance multimedia video solution.

In addition, without violating any connector specification, the CL-GD7556 supports video windows in graphics display modes that have a 1024 × 768 resolution. This support is possible because the rate at which video data comes through the V-Port is totally independent from the surrounding graphics VCLK of 65 MHz (for a 1024 × 768 display running at 60 Hz). Normally, any video window loaded through the V-Port is on top of the surrounding graphics, but color key support allows the graphics to occlude the video window, with insignificant or no loss of video performance. (For more information on color key support, refer to Section 3.2.4.3).

The CL-GD7556 V-Port design is an improvement over previous VGA controllers that include in their design either a Video Overlay or a Feature Connector. These older designs do not have a direct data path to the frame buffer. In addition, these older designs clock the video data coming from the overlay port at the VCLK rate of the current display device. The video data is then dynamically switched directly to the display device, and the video data overlays (that is, replaces) the graphics data coming from display memory.

In contrast, the CL-GD7556 does not have to clock video data at the VCLK rate of the current display device. Instead, the CL-GD7556 accepts video data through the V-Port at the rate of the original video data and stores it in display memory either directly or in a compressed format. The data transfer rate can be different (and typically lower) than the VCLK rate at which the display device is operating. As a result, the data can be simultaneously read out of the frame buffer and displayed at the VCLK rate for the display screen, with realtime decompression, if needed.

Table 3-6. V-Port™ Versus Video Overlay: A Comparison

Item	V-Port™	Video Overlay Mode
Clocking	Video data loaded through the V-Port can have a different data transfer rate (typically lower) than the data transfer rate at which the display is operating. This decoupling of video storage and video playback clock rates allows more flexible design options and reduces EMI. Power consumption is also decreased, since clock rates are lower.	Video data loaded through a video port must be clocked in at the current display VCLK rate. Data bits are then dynamically switched directly to the display device, replacing data coming from display memory.
Data path	Direct data path to the display memory with video data transfer rates of 27 Mbytes/sec (that is, 640 × 480 × 24 bpp × 30 fps).	Does not use a direct data path to the display memory.
Memory	Shares display memory with the graphics memory area.	Requires a distinct memory area and a separate video memory controller.

The 8-/16-bit V-Port provides the hardware required to implement a high-performance video/graphics solution that can be quite cost effective. For example, the V-Port can be configured to interface with various external devices in various modes, described in the sections that follow. The V-Port eliminates the need for a separate video windowing controller and an additional frame buffer for video data to perform the de-interlacing and timing synchronization of the video and graphics data streams. As a result, a hardware MPEG or NTSC/PAL TV decoder can be implemented with minimal cost, power consumption, and board space.

V-Port Video Data Input: V-Port Width (Extension Register CR50)

The CL-GD7556 can operate with either an 8-bit V-Port interface (that is, Extension register bit CR50[4] is 0) or a 16-bit V-Port interface (that is, CR50[4] is 1). The 16-bit V-Port, which requires a minimum of external logic, provides an ideal interface to standard 16-bit video or MPEG decoders. The V-Port method of handling video data is intended to support either a source of live video or playback from interfaces to various sources of video data. The V-Port can accept data in several different formats (such as interlaced, non-interlaced, and so forth).

The V-Port data path has an optional color space converter that compresses CCIR 601-compatible YUV data to either an AccuPak-compressed or a YUV-compressed data format prior to storage in the frame buffer. The CL-GD7556 back-end video pipeline fetches the compressed data from the display memory, decompresses it, and provides YUV-to-RGB conversion prior to displaying it on the display screen. Because compression and decompression occur within the CL-GD7556 controller, this option is transparent to application software, and it requires only driver support for the hardware connecting through the V-Port.

V-Port Video Data Input: Signal Definitions

- VPCLKI (V-Port clock input)
  - This signal is used to clock valid pixel data into the CL-GD7556. The data transfer rate varies according to the type of data format that is used by the external video decoder.
  - One VPCLKI is generated for each 16-bit pixel, whether the video data is scaled or not, during both display time and non-display time. VPCLKI is active during the entire vertical refresh interval.
  - VPCLKI is free-running at up to 20.25 MHz. The trailing edge of VPCLKI is used to clock the data into the CL-GD7556. The VACTI input, which comes from an external decoder such as the CL-PX4072, is forced high when data is available on the V-Port data bus. This VACTI input indicates that data being transferred through the V-Port is valid.
- VSI (vertical sync input)
  - The CL-GD7556 V-Port vertical control circuitry has programmable registers that use the trailing edge of the VSI signal as a reference for the start offset. (The start offset is a signal that delays the start of the signal delineating the width for a video window.)
  - The 9-bit field in Extension register bits CR57[7:0] and CR58[5] controls the number of scanlines to be captured.
- HREFI (horizontal reference input)
  - Horizontally, no programming is required for the CL-GD7556, as each falling edge of VPCLKI corresponds to valid data for one pixel.
- VACTI (video active input)
  - VACTI enables valid data from the CL-PX4072.
  - VACTI goes high when pixel data is valid on the Y and UV lines and goes low when the data is invalid.
  - VACTI allows the VPCLKI signal to be free running. When the CL-GD7556 is configured for a 16-bit-wide V-Port, the leading edge of VACTI is synchronized with the trailing edge of VPCLKI to capture valid data.
  - When the CL-GD7556 is configured for a V-Port that is 8 bits wide and double-edge clocking is selected, only 8 bits of data are used. In this case, VACTI must bracket both VPCLKI edges. The CL-PX4072 can use the VACTI and VPCLKI signals to scale down the data from the video source.
- VPY[7:0] (luminance data)
  - These signals are 8 bits of luminance data from the external video controller.
  - When the CL-GD7556 is configured for a V-Port that is 8 bits wide and double-edge clocking is selected, both luminance and chrominance data are routed to these pins, and VPC is not used.
- VPC[7:0] (chrominance data)
  - These signals are 8 bits of chrominance data from the external video controller.
  - There is a 9-bit programmable delay to skip ‘n’ number of HREFI pulses, before the internal V-Port Vertical Display Enable signal is asserted.

V-Port Video Data Input: Implementation

Communication between the CL-GD7556 and an external decoder device is based upon a synchronous data flow. The external decoder device drives all the V-Port interfaces, including the VPCLKI. Video data are loaded through the V-Port in one of either two different modes, depending on how data are latched relative to the VPCLKI clock edge as follows:

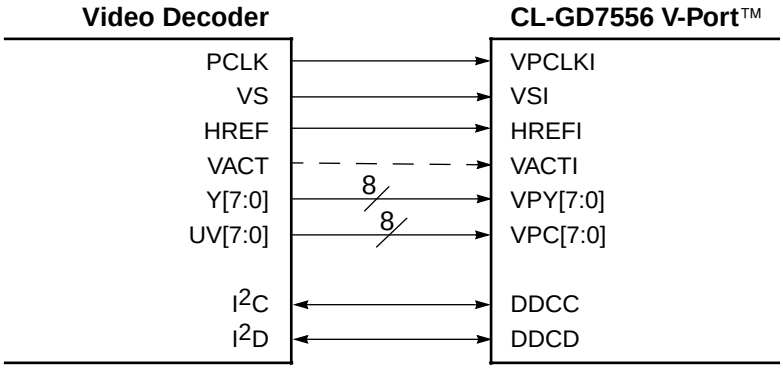
- V-Port Mode 1: Data are latched on the VPCLKI trailing edge
- V-Port Mode 2: Data are latched on the VPCLKI leading edge

This flexibility allows a direct connection between the CL-GD7556 and various TV/MPEG decoder chips. Also, the CL-GD7556 has a serial interface consisting of a clock pin (that is, DDCC) and a data pin (that is, DDCD), both of which are open-drain and support serial programming interfaces to those chips.

A. V-Port-to-Memory Mode 1: Data Latched on VPCLKI Trailing Edge

In V-Port-to-Memory Mode 1, video data are latched on the VPCLKI trailing edge (that is, the falling edge). An example of an implementation of this mode is the interface to the CL-PX4072, as shown in Figure 3-5. Full implementation of the V-Port-to-Memory Mode-1 interface requires the following 20 active pins:

- VPCLKI (V-Port clock input signal). With this mode, the high-to-low transition of VPCLKI latches the data bits.
- VSI (vertical sync input signal)
- HREFI (horizontal reference input signal)
- VACTI (video active signal, used to indicate the transfer of active video data)
- 16 data bits (8 data bits of Y-luminance on VPY[7:0] and 8 data bits of UV-chrominance on VPC[7:0])



NOTE: The DDCC and DDCD pins are not required for the V-Port. However, when the CL-GD7556 is used in certain motherboard implementations, the DDCC and DDCD pins output signals are used to program a NTSC/PAL TV decoder (such as the CL-PX4072 or the Philips® SAA7110).

Figure 3-5. V-Port™-to-Memory Mode-1 Interface Signals

The CL-PX4072 provides only interlaced video data streams that support the following analog video data standards:

- NTSC
- PAL
- SECAM
- S-VHS

B. V-Port-to-Memory Mode 2: Data Latched on VPCLKI Leading Edge

In V-Port-to-Memory Mode 2, video data are latched on the VPCLKI leading edge (that is, the rising edge). In contrast to V-Port-to-Memory Mode 1, V-Port-to-Memory Mode 2 does not require the additional VACTI signal in the interface. Full implementation of the V-Port-to-Memory Mode 2 interface requires only the following 19 active pins:

- VPCLKI (V-Port clock input signal). With this mode, the low-to-high transition of VPCLKI latches the data bits.
- VSI (vertical sync input signal)
- HREFI (horizontal reference input signal)
- 16 data bits (8 data bits for luminance and 8 data bits for chrominance)

In V-Port-to-Memory Mode 2, the CL-GD7556 can support both interlaced and non-interlaced video data streams.

- The interlaced video data stream supports a direct connection with decoder chips, such as the Philips® SAA7110 or the CL-PX4072.
- The non-interlaced video data stream supports a direct connection with MPEG decoder chips, such as the C-CUBE CL-480. In this type of operation, the relationship of the VSI signal to the HREFI signal is 'non-interlaced' and the frame buffer addresses for the video data are generated sequentially.

V-Port Video Data Input: Performance Tables

The CL-GD7556 can continuously upscale the video data that appears in a video window. In addition, by using simple decimation, it can also downscale the incoming video data from the V-Port. As a result, the resolution of the video data stored in display memory can be smaller than the resolution of the video data that is output from a video decoder device. At display time, the CL-GD7556 can convert data from the V-Port, which is in the 4:2:2 YUV color space format (that is, 16 bpp) to the AccuPak or DYUV color space formats (that is, 8 bpp).

Table 3-7 through Table 3-10 show the video performance that is possible when video data are transferred from a video source through the V-Port to a display screen video window of a system that has 1 or 2 Mbytes of display memory. In the tables, the following information applies:

- The AccuPak and DYUV formats generate more than 32K colors. The 4:2:2 YUV color space format is equivalent to RGB 8-8-8 with 16M colors.
- As set by the Cirrus Logic VGA BIOS, register settings for a random-access cycle are:
  - 8 MCLKs at 66 MHz
  - 9 MCLKs at 80 MHz
- Upscaling:
  - N/A = acronym for 'not applicable'
  - US = acronym for upscaling
  - 1:1 US = no upscaling (resolution of displayed video is the same as video stored in display memory)
  - 1:2 US = 2x upscaling
  - FS US = full screen upscaling (that is, to the full resolution of the display device)

Table 3-7. V-Port™ Video Performance with Occlusion in Flat-Panel-Only or SimulSCAN™ Modes[a]

Flat Panel[b] Resolution (pixels)	Color Depth (number of colors)	Video Data Format	MCLK (MHz)	Upscaled Video Resolution	
				Upscaling On TFT Flat Panel or in SimulSCAN™ Mode	Upscaling On DSTN Flat Panel or in SimulSCAN™ Mode
640 x 480	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
	64K	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
800 x 600	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
	64K	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
1024 x 768	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:2 through FS US
	64K	AccuPak™ or DYUV	80	N/A	N/A
		4:2:2 YUV or RGB 5-5-5	80	N/A	N/A

[a] The notation used in this table is discussed in the section, "PCI Bus Video Data Input: Performance Tables" on page 3-18.

[b] When the flat panel expansion mode is enabled, hardware acceleration of the video display is not supported.

Table 3-8. V-Port™ Video Performance without Occlusion in Flat Panel-Only or SimulSCAN™ Modes[a]

Flat Panel[b] Resolution (pixels)	Color Depth (number of colors)	Video Data Format	MCLK (MHz)	Upscaled Video Resolution	
				Upscaling On TFT Flat Panel or in SimulSCAN™ Mode	Upscaling On DSTN Flat Panel or in SimulSCAN™ Mode
640 x 480	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
	64K	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
800 x 600	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
	64K	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
1024 x 768	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:1 through FS US
	64K	AccuPak™ or DYUV	80	1:1 through FS US	N/A
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A

[a] The notation used in this table is discussed in the section, "PCI Bus Video Data Input: Performance Tables" on page 3-18.

[b] When the flat panel expansion mode is enabled, hardware acceleration of the video display is not supported.

Table 3-9. V-Port™ Video Performance with Occlusion In CRT-Only Modes[a]

CRT Monitor Resolution (pixels)	Color Depth (number of colors)	Video Data Format	MCLK (MHz)	Upscaled Video Resolution When Vertical Frequency of CRT Monitor Is:				
				60 Hz	70 Hz	72 Hz	75 Hz	85 Hz
640 × 480	256	AccuPak™ or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
	64K	AccuPak™ or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
800 × 600	256	AccuPak™ or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
	64K	AccuPak™ or DYUV	80	1:1 through FS US	N/A	1:1 through FS US	1:1 through FS US	N/A
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:2 through FS US	1:2 through FS US	N/A
1024 × 768	256	AccuPak™ or DYUV	80	1:1 through FS US	1:1 through FS US	1:1 through FS US	1:1 through FS US	1:1 through FS US
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	1:2 through FS US	1:2 through FS US	1:2 through FS US	N/A
	64K	AccuPak™ or DYUV	80	N/A	N/A	N/A	N/A	N/A
		4:2:2 YUV or RGB 5-5-5	80	N/A	N/A	N/A	N/A	N/A

[a] The notation used in this table is discussed in the section, "PCI Bus Video Data Input: Performance Tables" on page 3-18.

Table 3-10. V-Port™ Video Performance without Occlusion In CRT-Only Modes[a]

CRT Monitor Resolution (pixels)	Color Depth (number of colors)	Video Data Format	MCLK (MHz)	Upscaled Video Resolution When Vertical Frequency of CRT Monitor Is:				
				60 Hz	70 Hz	72 Hz	75 Hz	85 Hz
640 × 480	256	AccuPak or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
	64K	AccuPak or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
800 × 600	256	AccuPak or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
	64K	AccuPak or DYUV	80	1:1 through FS US	N/A	1:1 through FS US		
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US	N/A	1:1 through FS US		
1024 × 768	256	AccuPak or DYUV	80	1:1 through FS US				
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US				
	64K	AccuPak or DYUV	80	1:1 through FS US				
		4:2:2 YUV or RGB 5-5-5	80	1:1 through FS US				

[a] The notation used in this table is discussed in the section, "PCI Bus Video Data Input: Performance Tables" on page 3-18.

3.2.4.3 Source and Destination Color Key Occlusion of Video (Extension Registers GRC, GRD, GR1C–GR1F, CR1D, CR3F, and CR42)

Occlusion refers to the event that occurs when one window of display data sits on top of (that is, it hides or 'occludes') another window of display data.

The following sequence of events is an example of how occlusion occurs:

1. The Microsoft® Windows® application, Video for Windows®, is selected.
2. Within a video window, a video clip is played.
3. While the video clip is still playing, another window of graphics display data (such as a pull-down menu from the Microsoft® Windows® application, Media Player) is selected. The pull-down menu occludes the video clip, which continues to play normally in the window background.

The video data that appears in a video window resides in an off-screen area of display memory that is referred to as 'video window memory'. The graphics data, including the pull-down menu, resides in the on-screen area of display memory that is referred to as 'graphics memory'. Therefore, a method is needed to define where video data is to be displayed in place of the graphics data.

The method supported by Video for Windows and the DirectDraw .API for Windows 95 is called 'color keying'. Color keying is the process of using either a color or a color space format to 'key' (that is, define an area of data that is to be manipulated or changed). The CL-GD7556 supports both destination or source color keying.

- A *destination color key* (that is, a 'color key') specifies a color that is used to define the destination area to be used for the video window display. In the defined destination area, only those pixels that have a color that matches the destination color key are replaced by video data at display time.
  - — For example, when a destination area is defined and masked with black, and the destination color key used is also black, the black area of the graphics display is replaced by the data in the video window.
  - — Destination color keying typically uses RGB for keying data because the data for a CRT monitor or flat panel (which is the destination) is always in RGB format.
- A *source color key* specifies a color that is used to define what is not to be copied from the source (that is, display memory), and therefore, is not copied or visible on a destination area. (Some applications of source color keying are referred to as 'transparent BitBLTs'.)
  - — For example, when a source area of a video window has as its source color key the color blue, then any blue data in the source area is not copied into the destination area of a video window. The blue data can be specified either as the 'B' in RGB (typically referred to as 'color keying') or as a YUV value (typically referred to as 'chroma keying') that is equivalent to the color blue.
  - — Source color keying can support use of either RGB or YUV color space formats.

3.3 Functional Blocks

Section 3.3.1 through Section 3.3.23 describe the functional blocks that are integrated in the CL-GD7556. Figure 3-6 shows a simplified block diagram of the CL-GD7556 controller.

3.3.1 PCI Bus Interface (External/General Register PCI00)

The CL-GD7556 connects directly to a PCI host CPU bus. Full support of the PCI v2.1 specification is provided, including support for external VGA BIOS decode to allow the CL-GD7556 to work in an external add-in daughterboard environment. No additional logic circuitry is required to support the CL-GD7556 multiplexed address and data pins for the host CPU interface. The CL-GD7556 executes 32-bit I/O and memory accesses at speeds up to 33 MHz. The CL-GD7556 also supports extended memory burst cycles. These extended cycles result in faster system-to-screen BitBLTs, since the overhead incurred in starting a burst cycle is spread over more host CPU transfers. The PCI bandwidth is at least 33% more efficiently used with burst cycles.

3.3.1.1 PCI Bus Apertures

The CL-GD7556 supports big-endian word swapping for byte, word, and doubleword data sizes through use of four 4-Mbyte partitions (that is, logical address apertures) of the 16-Mbyte display memory address space. This allows 'X86 little-endian data or PowerPC big-endian data to load into display memory, depending upon the application requirements. (For more information on the CL-GD7556 PCI apertures, refer to Section 3.2.4.1.)

3.3.1.2 Linear Display Memory Addressing

The CL-GD7556 supports linear display memory addressing, as an alternative to the standard VGA method of accessing display memory with a 64-Kbyte-segment limitation. The CL-GD7556 uses linear display memory addressing to access display memory as a 1-, 2-, or 4-Mbyte linearly addressed string of bytes.

For applications or drivers that support linear display memory addressing, graphics performance is improved by simplifying access to display memory. It is not necessary to calculate offsets into a relatively small window, nor is it necessary to test for a crossing of the window boundary.

The CL-GD7556 host CPU interface pins are connected to similarly named pins on the PCI bus, which provides a complete 32-bit address bus (16-Mbyte address space). No external address decoding is necessary. When the high-order eight bits of the address on the AD pins match the bits of External/General register PCI10 (the Display Memory Base Address register), and Extension register bits SR7[7:4] are non-zero, the CL-GD7556 is in Linear Addressing mode.

3.3.2 Host CPU Write Buffer

The host CPU write buffer contains a queue of host CPU write accesses to display memory that, because of memory arbitration, have not been executed. Maintaining this queue of write accesses allows the CL-GD7556 to release the host CPU bus as soon as it has recorded the address and data. The CL-GD7556 executes the operation when display memory is available, which increases host CPU performance.

For all text and graphics display modes, the write buffer depth is eight 32-bit levels. The CL-GD7556 has the capability to page host CPU cycles, when they are accumulated in the host CPU write buffer.

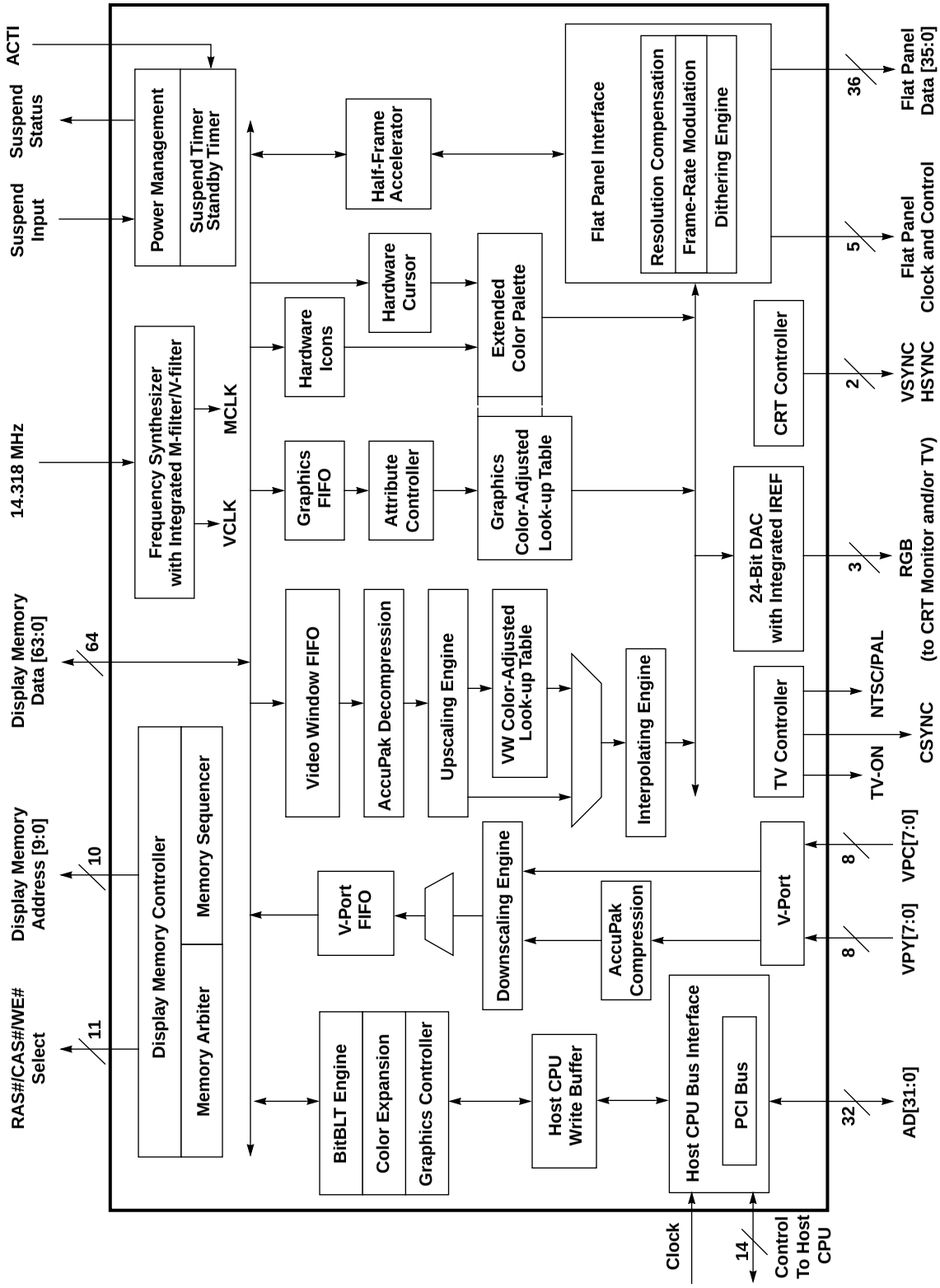


Figure 3-6. CL-GD7556 Block Diagram

3.3.3 Graphics Controller

The graphics controller operates in either text or graphics display modes and performs the following major functions:

- Provides the host CPU a read/write access path to display memory
- Controls all four memory planes in planar modes
- Allows data to be manipulated prior to being written to display memory
- Formats data for use in various backward compatibility display modes
- Provides color read comparators for use in color painting modes
- Reads/writes 64-bit words through the 64-bit display memory interface

The graphics controller directs data between the display memory to the host CPU. Figure 3-7 and Figure 3-8 illustrate typical write and read operations, respectively.

For a write operation, the data from the host CPU bus are combined with the data from the set/reset logic in the host CPU, depending on the Write mode. In addition, the data can be combined with the contents of the read latches, and some bits or planes can be masked (that is, prevented from being changed) by using the Graphics Controller register GR8. For more information, refer to the Graphics Controller registers.

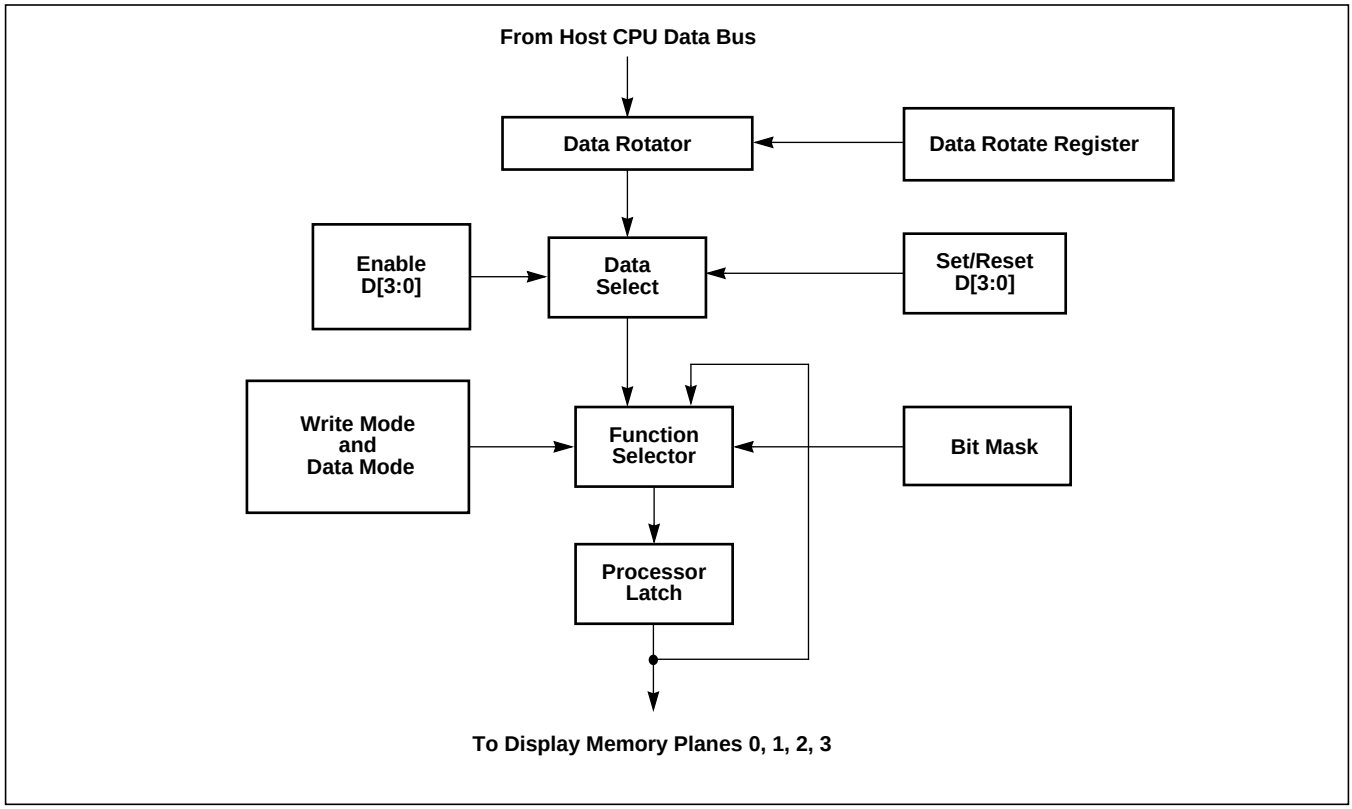


Figure 3-7. Graphics Controller Write Operation

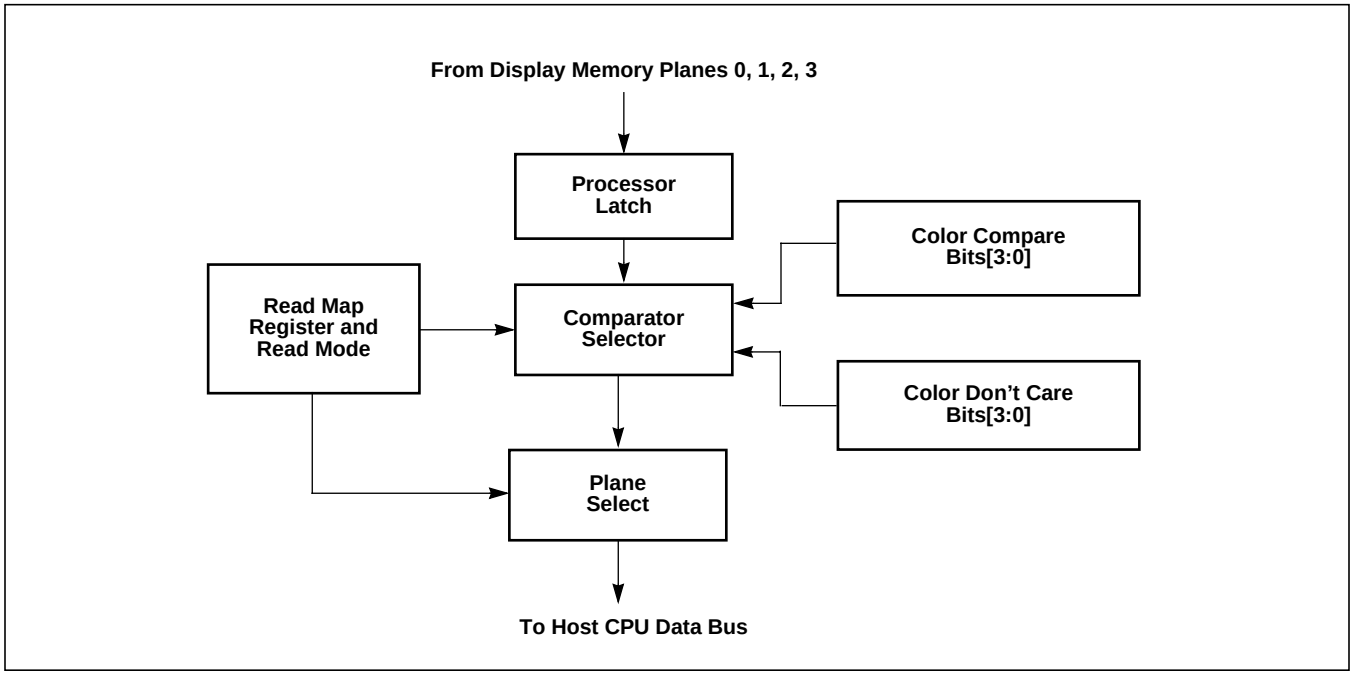


Figure 3-8. Graphics Controller Read Operation

3.3.4 Color Expansion (Extension Registers GR10–GR11, GR13, and GR30)

Color expansion is the automatic conversion of a monochrome bit map (which typically defines a character, icon, or pattern) into foreground and background color values. These values are then written into display memory and held in a CL-GD7556 register.

Color expansion improves host CPU write performance by optimizing use of the available host CPU bandwidth. It expands single bits across the host CPU bus into complete 8-, 16-, or 24-bit pixels.

When color expansion is used, only monochrome bit maps must be transferred across the host CPU bus. Each bit of the monochrome map is converted into 8-, 16-, or 24-bit pixel modes. The bus traffic is reduced by factors from 8 to 24, making it possible to use nearly all of the available display memory bandwidth.

3.3.5 BitBLT Engine (Extension Registers GR20–GR35)

The CL-GD7556 BitBLT engine moves a rectangle of data either within display memory or between system memory and display memory, with minimal host CPU intervention. The BitBLT engine can also perform pattern fills (that is, filling an area with a repeating pattern), raster operations (combining source bytes with destination bytes, using various logic operations), and color expansion or transparency.

The BitBLT engine provides 16 two-operand ROPs (raster operations) to move data in Packed-Pixel modes from the source area to the destination area. This operation occurs in Packed-Pixel modes with 8-, 16-, or 24-bit pixel transfers. Transfers from the host CPU are always taken in 4-byte increments. For screen-to-system transfers, the BitBLT operation acts as a read cache. The BitBLT accelerates GUIs, such as Microsoft Windows 95, Windows 3.1, and OS/2 3.0 ‘Warp’. For more information, refer to the appendixes.

3.3.5.1 BitBLAST Operation (Extension Registers GR28–GR2A and GR31[7])

The BitBLAST (bit block accelerated setup transfer) operation is a CL-GD7556 feature that was first introduced in the CL-GD5436 controller. With BitBLAST, the BitBLT control registers are duplicated, and a status bit is provided. Application programs can monitor this status bit to determine when to program the parameters for a new BitBLT operation. This programming is done before the current BitBLT completes execution, in a second set of registers that are transparent to the software.

This action allows the setup time of the new BitBLT to overlap the execution time of the previous BitBLT. Because the BitBLT setup time is done with 16-bit I/O accesses, the BitBLAST can eliminate the amount of time needed by software overhead. In addition, this overlap greatly speeds up procedures (such as Windows drivers) that use multiple successive BitBLTs. (The CL-GD7556 auto-start feature can start the BitBLT even faster and save additional BitBLT setup time.)

If the BitBLAST feature is enabled (that is, Extension register bit GR31[7] = 1), BitBLTs start every time Extension register GR2A is written (which occurs as soon as the current BitBLT completes).

3.3.5.2 Transparent BitBLT (Extension Registers — GR34 and GR35)

The CL-GD7556 supports a transparent BitBLT operation. This operation allows the CL-GD7556 to define a ‘key’ color of source data that does not transfer when the BitBLT executes. As a result, the background color of the source graphics data does not have to match the background color of the destination, which reduces software overhead. Also, as opposed to normal BitBLT operations that result in transfers of only rectangular blocks of data, the transparent BitBLT operation allows transfers of irregularly shaped objects.

3.3.6 Memory Arbiter

The memory arbiter allocates bandwidth to the following functions, which compete for the limited bandwidth of display memory:

- Host CPU access
- Display screen refresh
- Display memory refresh
- BitBLAST
- Half-frame accelerator (for dual-scan STN flat panels)
- V-Port™
- Hardware cursor and hardware icons

Display memory refresh is handled transparently by allocating a selectable number of CAS#-before-RAS# refresh cycles at the beginning of each scanline. Refresh cycles are allocated to display screen refresh and to host CPU access to the display memory and BitBLT operations, according to the FIFO-control parameters. Priority is given to display screen refresh.

3.3.7 Memory Sequencer

The memory sequencer generates all the timing and control signals needed by display memory, including RAS#, CAS#, multiplexed-address timing, and WE# and OE# timing. The sequencer generates CAS#-before-RAS# refresh, random-read, random-early-write, fast-page-mode read, and early-write cycles.

The memory sequencer generates multiple-CAS# or multiple-WE# signals, depending on the memory type being used. The CL-GD7556 supports both multiple-CAS# and multiple-WE# 256K × 16 DRAMs. The CL-GD7556 supports the following memory configurations, all with a 64-bit-wide memory interface:

- Two 128K × 32 EDO (extended data out, also known as 'Hyper-page') DRAMs for 1-Mbyte display memory
- Four 128K × 16 EDO DRAMs for 1-Mbyte display memory
- Four 256K × 16 EDO DRAMs for 2-Mbyte display memory (pin-compatible to 128K × 16 EDO DRAM pads)

The memory sequencer ensures that the necessary display refresh transfer cycles and dynamic memory refresh cycles are executed and that the remaining memory cycles are made available for host CPU read/write operations. For more information, refer to the appendixes.

EDO DRAM Support (Extension Register GR18)

EDO DRAM technology allows the read data from DRAM to be held past the leading (that is, the rising) edge of CAS#. Consequently, EDO DRAMs have a short page-mode cycle time relative to the corresponding RAS# cycle times. The CL-GD7556 provides support for EDO (Hyper-page) DRAMs in three ways:

1) When the VGA core is running with an MCLK of 80 MHz at 3.3 V, this MCLK rate corresponds to an EDO DRAM with 60-ns access time and a 25-ns page-cycle time.

2) The CL-GD7556 can generate random cycles with 6-, 7-, 8-, or 9-MCLK RAS#, allowing flexibility for the relatively slow RAS# times.

3) The CL-GD7556 latches data following the leading edge of CAS#, taking advantage of the extended data hold time.

3.3.8 CRT FIFO

The CRT FIFO is a register stack that is 24 levels deep by 64 bits wide. It allows the memory sequencer to execute display memory accesses needed for display screen refresh at maximum display memory speed, rather than at the display screen refresh rate. This register makes it possible to collect screen refresh accesses near the beginning of the scanline and execute them in Fast-Page mode rather than Random-Read mode.

3.3.9 Attribute Controller

The attribute controller formats the display for the screen. It performs the following:

- Serialization of memory data
- Display color selection
- Text blinking
- Underlining in both text and graphics display modes

Figure 3-9 is a functional block diagram of the Attribute Controller with input and output ports.

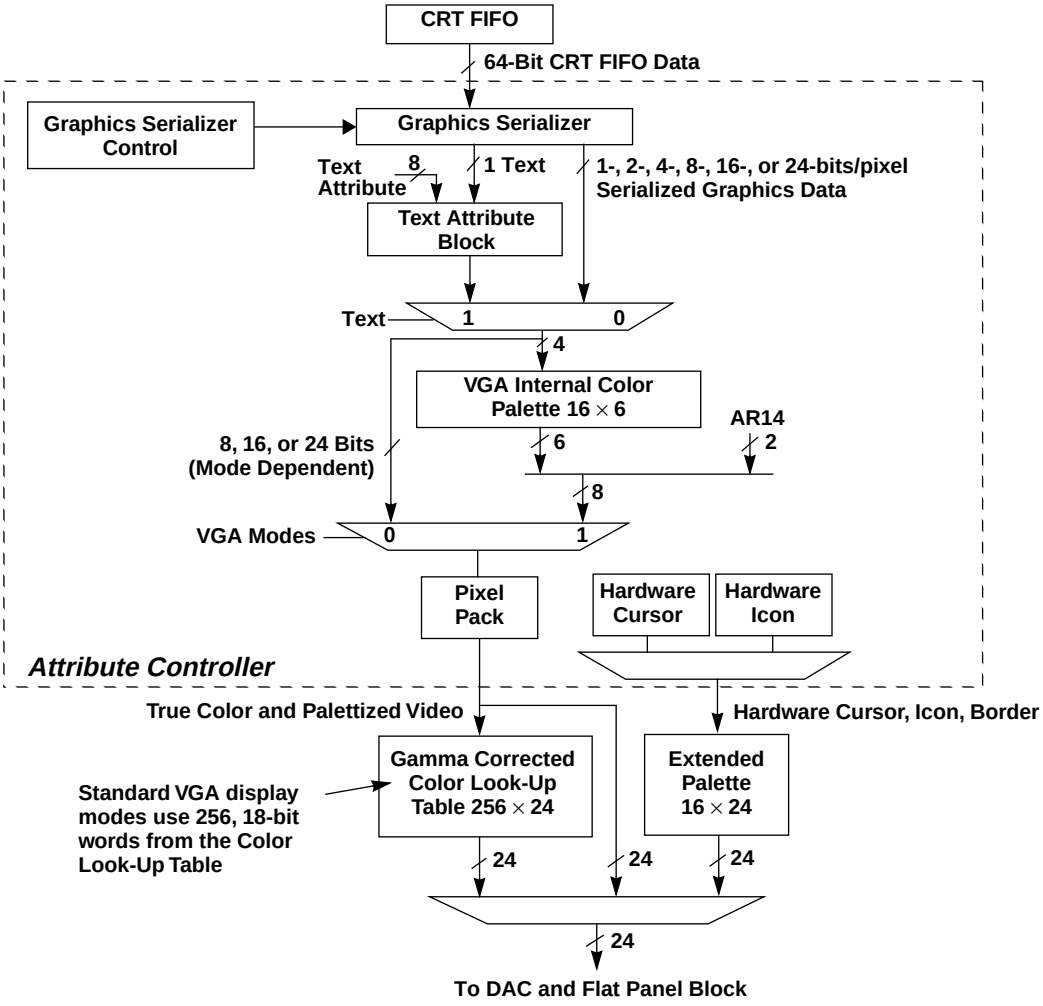


Figure 3-9. Attribute Controller Functional Block Diagram

3.3.10 CRT Controller

The CRT controller generates horizontal and vertical synchronization signals (that is, HSYNC and VSYNC) for a CRT monitor. The CRT controller registers generate BLANK# signals required by the palette DAC. They also support standard VGA-compatible modes and extended modes and provide for the following:

- Configuration options, including user-configurable horizontal/vertical timing and polarity
- Cursor positioning
- Horizontal scanlines
- Pixel and byte panning
- Split-screen capability
- Smooth scrolling

The CL-GD7556 supports standard 640 × 480 text display mode resolutions and the extended 132 × 25 and 132 × 43 text display mode resolutions. The CL-GD7556 also supports standard 640 × 480 graphics display mode resolutions and the following extended graphics display mode resolutions:

- For CRT monitors: Up to 1280 × 1024, with up to 256 colors
- For CRT monitors and flat panels:
  - 1024 × 768, up to 64K colors
  - 800 × 600, up to 16M colors
  - 640 × 480, up to 16M colors

The CL-GD7556 fully supports all the standard IBM VGA memory organizations, along with the following extended color modes:

- 256-color packed-pixel modes (8 bpp)
- Mixed 32K- and 256-color packed-pixel modes (15 bpp)
- Direct Color packed-pixel modes:
  - High Color
    - 15-bit High Color (5 bits each of red, green, and blue color information for 32K simultaneously displayed colors)
    - 16-bit High Color (5 bits each of red and blue, and 6 bits of green color information for 64K simultaneously displayed colors)
  - True Color (24 bpp for 16M simultaneously displayed colors)

In true packed-pixel addressing, consecutive pixels are stored at consecutive addresses. This storage method is in contrast with the storage method used by chain-4 addressing, which is a type of addressing that stores consecutive pixels at every fourth byte address in display memory. For more information, refer to the appendixes in this manual and the appendix on “True Color Modes” in the *CL-GD7556 Software Reference Manual*.

The SimulSCAN mode is supported for panel resolutions of 640 × 480, 800 x 600, or 1024 × 768. With 24-bit packed-pixel support, 24-bpp display modes (that is, RGB 8-8-8 True-Color mode) are supported at the VCLK rate. For a complete listing of all display modes supported by the CL-GD7556, refer to Chapter 4. Figure 3-10 is a functional block diagram of the CRT controller.

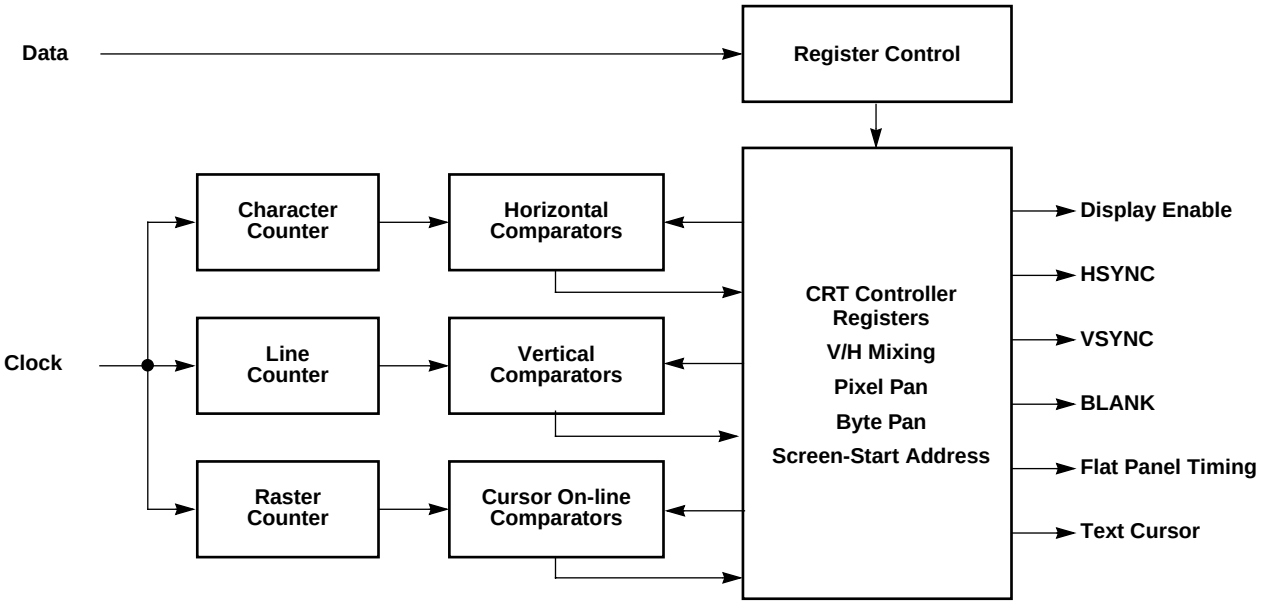


Figure 3-10. CRT Controller Functional Block Diagram (Signals Are Internal to CL-GD7556)

3.3.11 Internal TV-OUT

A TV-OUT mode is supported, when neither the CRT or flat-panel is being used. See Extension register CR30 for details. With the addition of an analog encoder and minimal additional logic circuitry, the CL-GD7556 can supply digital RGB data to a standard TV monitor or VCR (video cassette recorder) in an interlaced format using one of the following encoding schemes:

- An external composite encoder, such as a NTSC (National Television Standards Committee) encoder
- An external encoder such as a PAL (phase alternation line-rate) encoder
- An external component encoder such as S-VHS

The CL-GD7556 can operate in a locked interlaced mode. In this case, the LCD support shadowing mechanism (which shadows the Horizontal and Vertical CRTC registers) is used to prevent an application from changing any part of the CRT Controller setup, including the dot clock frequency. Horizontal and vertical display enable is open to the application.

The CL-GD7556 provides analog RGB, a composite synchronization signal, an NTSC/PAL standard select signal, and TV-On (a power-management signal). Due to differences in the standards between PC displays and CRT monitors, the NTSC/PAL output is limited to graphics modes 1h, 3h, 12h, 13h, 5Fh, and 64h. (A special windows driver allows use of graphics mode 5Fh for Windows®.)

Because televisions use interlaced display refresh and have an aspect ratio different than many standard VGA modes, support for additional VGA modes was not included in the CL-GD7556, as such support would result in unusable displays.

The NTSC/PAL functionality provided in the CL-GD7556 is targeted primarily for entertainment use, for display of graphic images, and within certain guidelines, for presentations. However, this functionality was not intended as a direct replacement for a PC CRT. For more information on internal and external TV-OUT modes and NTSC/PAL functionality, refer to application notes.

3.3.12 Hardware Cursor (Extension Registers SR10–SR12, SR2A, and SR2E)

The hardware cursor replaces the software cursor (that is, a mouse pointer) commonly used by GUI applications. The hardware cursor eliminates the need for application software to save and restore the display data as the cursor position changes. Typically, the application software initializes the hardware cursor once, and from that point it needs only to update the cursor hot spot (that is, the cursor x, y position on the display screen) to move it on the display screen.

The hardware cursor offers a smoothly moving cursor with improved performance, as compared to a software cursor. The hardware cursor is always displayed on top of graphics, video, or the hardware icons.

The hardware cursor consists of either 64 × 64 two-bit pixels or 32 × 32 two-bit pixels. Each pixel in the hardware cursor can be either transparent or one of two colors from the 16 × 18-bit extended color palette, which is separate from the VGA color palette. The first bit of each pixel in the hardware cursor defines whether or not the pixel is transparent. If the pixel is not transparent, the second bit defines the color depth. In which case, the second bit selects one of two 18-bit colors in the extended color palette.

The following types of 2-bit hardware cursor patterns can be loaded into upper display memory:

- 64 × 64 hardware cursor patterns — up to 8 patterns
- 32 × 32 hardware cursor patterns — up to 32 patterns

After the hardware cursor patterns are loaded into upper display memory, application programs can quickly select one pattern as the active cursor pattern. For more information, refer to the appendixes.

NOTE: The hardware cursor is available in all display modes except text display modes.

3.3.13 Hardware Icons (Extension Registers SR10–SR11 and SR2A–SR2E)

The CL-GD7556 provides hardware icons for displaying small, on-screen symbols that indicate system status (for example, a battery 'fuel gauge'). These hardware icons are stored in upper display memory and can be displayed at the touch of a key. Hardware icon(s) are supported in all text and graphics display modes. The hardware icons are independent of both the graphics display mode being used and the hardware cursor. Typically, the application software initializes the hardware icon once, and from that point it needs only to update the icon hot spot (that is, the icon x, y position on the display screen) to move it on the display screen.

When both a hardware cursor and hardware icon(s) are displayed, the hardware cursor passes on top of the hardware icon(s). The CL-GD7556 priority of display overlays is as follows:

1) Hardware cursor (always displayed on top)

2) Hardware icon

3) Video window data (a video window can be moved forward or backward in the sequence using a color key)

4) VGA graphics data or text data

The CL-GD7556 supports two hardware icon modes:

Hardware Icon Mode 1

With Hardware Icon mode 1, up to four icons, each 64 × 64 pixels in size, can be displayed simultaneously in a vertical column. Each icon is independently controlled for color. Either the four-color mode or the three-colors-and-transparent mode can be used. Each icon can be expanded either horizontally by pixel doubling, vertically by scanline doubling, or both horizontally or vertically to a maximum size of 128 × 128 pixels per icon.

- When one of the icons is doubled vertically, that icon extends down, which forces the icons below it down.
- When one of the icons is doubled horizontally, that icon expands to the right.
- Each of the four icons is allocated two memory maps. (A total of eight hardware icon memory maps can be stored in display memory.)
- The icons can be made to blink at one-half the cursor blink rate.

Hardware Icon Mode 2

With Hardware Icon mode 2, one 64 × 64 pixel hardware icon, from a menu of eight hardware icon memory maps, can be displayed. Either the four-color mode or the three-colors-and-transparent mode can be used. The icon is independently controlled for all other icon attributes (for example, blink, horizontal and vertical doubling, icon enable, and memory map selection).

3.3.14 Color Palette

The color palette is a 256 × 24-bit-word CLUT (color look-up table). In standard VGA modes, the CLUT is configured as a 256 × 18-bit-word table. (Refer to Figure 3-11.)

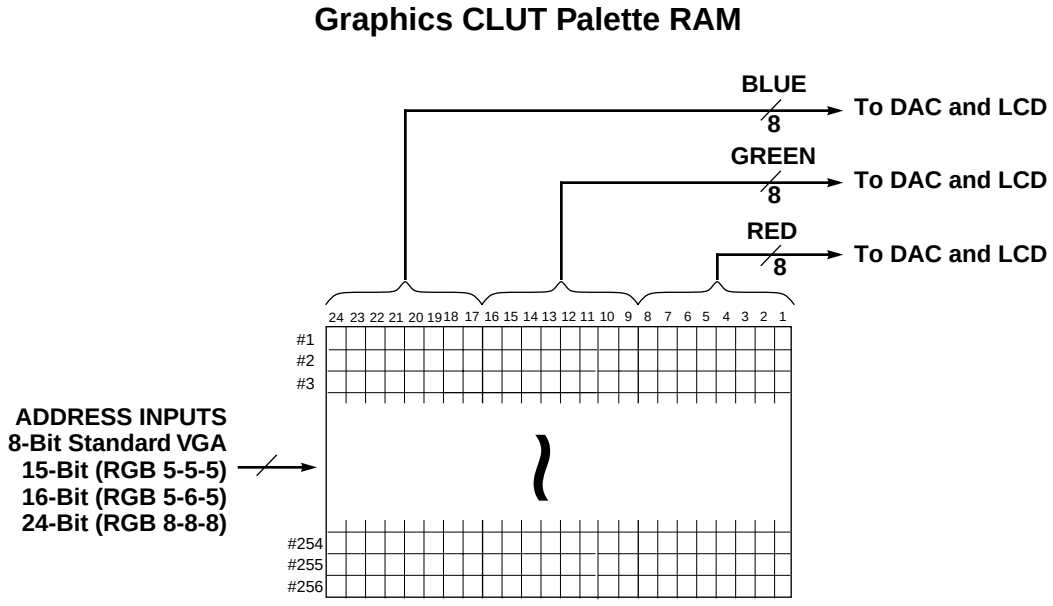


Figure 3-11. Graphics Color Look-Up Table (Palette)

In 24-bpp True-Color display modes, three 8-bit addresses are used to simultaneously select independent red, green, and blue data from different locations in the 256 entries for each color in the CLUT. The 24-bit output of the CLUT consists of three 8-bit values, one for each primary R,G,B color. The 24-bit word defines one of 2^{24} (that is, one of 16M) colors.

In 16-bpp High-Color display modes, three addresses consisting of 5 bits, 6 bits, and 5 bits are used to select independent red, green, and blue data bits respectively from different locations in the 256 entries for each color in the CLUT. The 16-bit address defines one of 2^{16} (that is, one of 64K) colors. The CLUT converts the 16-bit color code (or CLUT address) that specifies the color of a pixel into a 24-bit value, such that 64K simultaneous colors are displayed from a color palette of 16M colors.

In 15-bpp High-Color display modes, three addresses, each consisting of 5 bits, are used to select independent red, green, and blue data bits respectively from different locations in the 256 entries for each color in the CLUT. The 15-bit address defines one of 2^{15} (that is, one of 32K) colors. The CLUT converts the 15-bit color code (or CLUT address) that specifies the color of a pixel into a 24-bit value, such that 32K simultaneous colors are displayed from a color palette of 16M colors.

In standard 8-bpp VGA display modes, each 18-bit word consists of three 6-bit values, one for each primary R,G,B color. The 18-bit word defines one of 2^{18} (that is, one of 256K) colors. The CLUT converts an 8-bit color code (or CLUT address) that specifies the color of a pixel into an 18-bit value, such that 256 simultaneous colors are displayed from a color palette of 256K colors. An 8-bit-wide host CPU interface address applied to the pixel address inputs defines the display memory location for reading the 18-bit color data word from the CLUT. To send a 24-bit word to the DAC, the CL-GD7556 converts each 6-bit output to 8 bits by shifting the data left two bits and adding two least-significant zeros.

An internal synchronizing circuit allows the color value accesses to be completely asynchronous to the pixel display operation. Special display operations, such as flashing objects and overlays, are possible because the color palette incorporates a pixel word mask to allow the incoming pixel address to be altered. As a result, changes to the contents of the CLUT can be made immediately. The CLUT has circuitry to reduce random noise on the display screen during host CPU accesses to the color palette.

High-Color and True-Color Modes

In addition to graphics display modes that use the CLUT RAM, the CL-GD7556 supports the following High-Color and True-Color modes, which are useful in graphics and multimedia applications:

- **RGB 5-5-5 32K High-Color Mode:** Each pixel is represented by 15 bits, consisting of 5 bits each of red, green, and blue color information to provide 32K simultaneously displayed colors.
- **RGB 5-6-5 64K High-Color Mode:** Each pixel is represented by 16 bits, consisting of 5 bits each of red and blue, and 6 bits for green color information to provide 64K simultaneously displayed colors.
- **RGB 8-8-8 16M True-Color Mode:** Each pixel is represented by 24 bits, consisting of 8 bits each of red, green, and blue color information to provide 16M simultaneously displayed colors.

For more information on High-Color and True-Color modes, refer to the appendixes.

3.3.15 Extended Color-Palette RAM

The extended color-palette RAM provides up to 16×24-bpp data (RGB 8-8-8) for the following functions:

- Hardware cursor
- Hardware icon
- Overscan border color

The extended color-palette RAM enables the colors of the hardware cursor, hardware icons, and the border to be programmed independently from the standard CLUT RAM.

3.3.16 Gamma-Correction or Color-Adjustment Using a CLUT

The CL-GD7556 uses a 256 × 24 RAM for a CLUT (color palette) that can produce gamma-corrected or color-adjusted values to compensate for gamma characteristics of the surrounding graphics display for color modes that are 15 bits (32K-color) or greater.

NOTE: The color adjustment/correction for the surrounding graphics part of a display screen is independent from the color adjustment for a video window; see Section 3.2.3.5 on page 3-13.

Color adjustment can be used to produce a consistent color output on various types of display devices. As discussed in Section 3.2.3.5, various display devices have different gamma or color/brightness characteristics. Furthermore, flat panels of various types and from various manufacturers can have different color/brightness characteristics. Given the gamma or color/brightness curve of the display device to be used, a gamma or color/brightness correction curve can be programmed into the CLUT to produce a color image that most closely approximates that of its source.

Following POST (power-on self test), the CL-GD7556 VGA BIOS provides a standard set of default color/brightness-corrected values for the CLUT RAM. When display modes that have less than 15 bpp are called, the VGA BIOS subsequently locks the CL-GD7556 registers that allow the CLUT RAM to be modified. When an application modifies the CLUT RAM values, and when the application is properly terminated and exited, the VGA BIOS restores the default CLUT RAM values.

3.3.16.1 Software Control of the Color and Brightness

An application can modify gamma or color/brightness values by direct register programming through the use of hardware-specific drivers provided by an application vendor or by utilities. Cirrus Logic provides a Windows 95 based ‘Color Balance’ software utility that is used to independently adjust the red, green and blue colors of both the surrounding graphics and the video window. The utility also provides for a separate ‘brightness’ adjustment. This utility is described in the *CL-GD7556 Software Reference Manual*.

3.3.17 Triple DAC

The DAC subsystem includes three 8-bit DACs. The DAC outputs drive the red, green, and blue color display inputs to the CRT monitor. The DAC outputs are designed to produce a 0.7-V peak-white amplitude when supplied with a reference current (IREF). To reduce system component costs and simplify designs, the CL-GD7556 offers an internally generated IREF. To supply the internally generated IREF, only a pull-up resistor is necessary to produce the required reference current.

As an option, an external IREF circuit can also be implemented. If the external IREF is used, the IREF current is supplied with the circuit shown in the IREF pin description in Chapter 2. For all IREF values and output loading:

- $V_{Black\ Level} = 0.0\ V$
- $V_{Maximum\ White} = 0.7\ V$

To detect the type of CRT monitor that is connected, two sense methods can be used — analog and digital. With the analog sense method, the CL-GD7556 places specific color values on the RGB lines and then compares the resulting voltage level against a known internal reference voltage.

3.3.18 Half-Frame Accelerator

The CL-GD7556 integrates a half-frame accelerator, required by dual-scan STN flat panels. With the half-frame accelerator, a dual-scan STN flat panel runs at twice the refresh rate of a CRT monitor. The CL-GD7556 provides SimulSCAN operation for the following dual-scan STN flat panels:

- For 640 × 480 dual-scan STN flat panels, the half-frame accelerator provides all the standard and extended VGA display modes that have a screen format of up to 640 × 480.
- For 800 × 600 dual-scan STN flat panels, the half-frame accelerator provides all the standard and extended VGA display modes that have a screen format of up to 800 × 600.

3.3.19 Flat Panel Interface (Extension Registers CR80–CR91 and CRA0–CRBF)

The CL-GD7556 can directly connect to a variety of flat panels by programming Extension register bits CR83[6:4]. The flat panels include the following:

- Color dual-scan STN (640 × 480 or 800 × 600 resolution), with 8- or 16-bit interfaces
- Color TFT (640 × 480, 800 × 600, or 1024 × 768 resolution), with direct connection to the following interfaces:
  - 9-bit (3 bits each for red, green, and blue)
  - 12-bit (4 bits each for red, green, and blue) with either:
    - A 1-pixel/clock interface
    - A 2-pixel/clock interface requiring 24 data pins to handle the transfer of 12 bits of data on each edge of the clock
  - 18-bit (6 bits each for red, green, and blue) with either:
    - A 1-pixel/clock interface
    - A 2-pixel/clock interface requiring 36 data pins to handle the transfer of 18 bits of data on each edge of the clock
  - 24-bit (8 bits each for red, green, and blue) with a one pixel/clock interface

3.3.19.1 Support for 1024 × 768 TFT Flat Panel

When the CL-GD7556 is used with a 1024 × 768 TFT flat panel, support consists of the following:

- Support for graphics display modes that have a resolution of either 640 × 480, 800 × 600, or 1024 × 768 (for both Centered and Expanded modes)
- Direct connect to a 2-pixel/clock interface for 1024 × 768 flat panels. This type of interface is often used with flat panels that have a 1024 × 768 resolution because the normal pixel clock (that is, VCLK) rate is 65 MHz. Sending two pixels per clock allows the flat panel interface to operate at the lower speed of 32.5 MHz, while still providing the same amount of data. However, it does require more data pins between the flat panel and the CL-GD7556.
- EMI reduction (that is, a reduction of the voltage swing by supporting a 3.3-V flat panel interface)
- Support for all SimulSCAN display modes
- Support for the control signals for TFT flat panels with a resolution of 1024 × 768:
  - FPVDCLK, a shift clock that is used to latch the flat panel pixel data)
  - The flat panel frame clock (vertical sync) signal
  - The flat panel line clock (horizontal sync) signal
  - FPDE, the flat panel display enable signal
- Hardware expansion of display modes with a 640 × 480 resolution to an 800 × 600 resolution, with centering
- Automatic centering, in SimulSCAN mode, of an image that appears on the display screen of both a flat panel and CRT monitor

3.3.19.2 Support for 1024 × 768 TFT Flat Panel (and CRT Monitor in SimulSCAN™ Operation)

The CL-GD7556 has timing control registers that allow the CL-GD7556 to simultaneously support both a flat panel (which has a fixed set of timing parameters) and a CRT monitor (which needs different timing parameters for each operational mode).

- When only a CRT monitor is used to display an image, the standard CRT Controller registers CR0–CR16 that are provided by the CL-GD7556 are used.
- When both a flat panel and a CRT monitor are used to display an image, Extension registers CRA0–CRAC, which replace the standard CRT Controller registers, are used. These registers apply to both expanded and non-expanded display modes.

Table 3-11, Figure 3-12, and Figure 3-13 show display screen format options that are possible on an 1024 × 768 flat panel (and on a CRT monitor as well, in SimulSCAN). For expansion details, refer to section 3.3.19.5.

Table 3-11. Display Screen Options on a 1024 × 768 Flat Panel (and CRT Monitor, in SimulSCAN™)

Display Mode	Display Mode Resolution	Corresponding Display Screen Format Options for 1024 × 768 Flat Panels and CRT Monitors	
		Expansion up to 640 × 480 and Centering	Expansion up to 800 × 600 and Centering
10h	640 × 350	640 × 475	800 × 525
5Fh	640 × 480	640 × 480	800 × 600
Text Display Modes 02+h, 03+h, 7h	720 × 400	640 × 480	800 × 600
5Ch	800 × 600	An 800 × 600 image that is centered (Non-expanded)	An 800 × 600 image that is centered (Non-expanded)
60h	1024 × 768	1024 × 768 (Native mode)	1024 × 768 (Native mode)

NOTES:

1) In Table 3-11, the term ‘Native mode’ refers to an image that is running at the same resolution as the resolution of a flat panel or CRT monitor and which consequently fills the entire display screen.

2) For CRT-only operation, the expansion and centering options are not necessary.

3.3.19.3 Graphics and Text Display Modes Centering Option

Figure 3-12 shows how various graphics and text display modes appear when the CL-GD7556 is driving a 1024 × 768 TFT flat panel and one of the centering options is used (that is, Extension register bit CR81[0] for centering text or Extension register bit CR82[0] for centering graphics).

Example A

The CL-GD7556 is programmed for a graphics display mode that has a resolution of 1024 × 768. In this case, the entire display screen is used.

Example B

The CL-GD7556 is programmed for either (1) 640 × 480 text expansion or (2) an 800 × 600 centered text display mode. In both these cases, an 800 × 600 display image appears centered within the 1024 × 768 display screen. Also, blanking occurs on that portion of the display screen that is not used (that is, the 84 top scanlines, 84 bottom scanlines, 112 left columns, and 112 right columns).

Example C

The CL-GD7556 is programmed for a centered text display mode that has a resolution of 640 × 480. In this case, a 640 × 480 display image appears centered within the 1024 × 768 display screen. Also, blanking occurs on that portion of the display screen that is not used (that is, the 144 top scanlines, 144 bottom scanlines, 192 left columns, and 192 right columns).

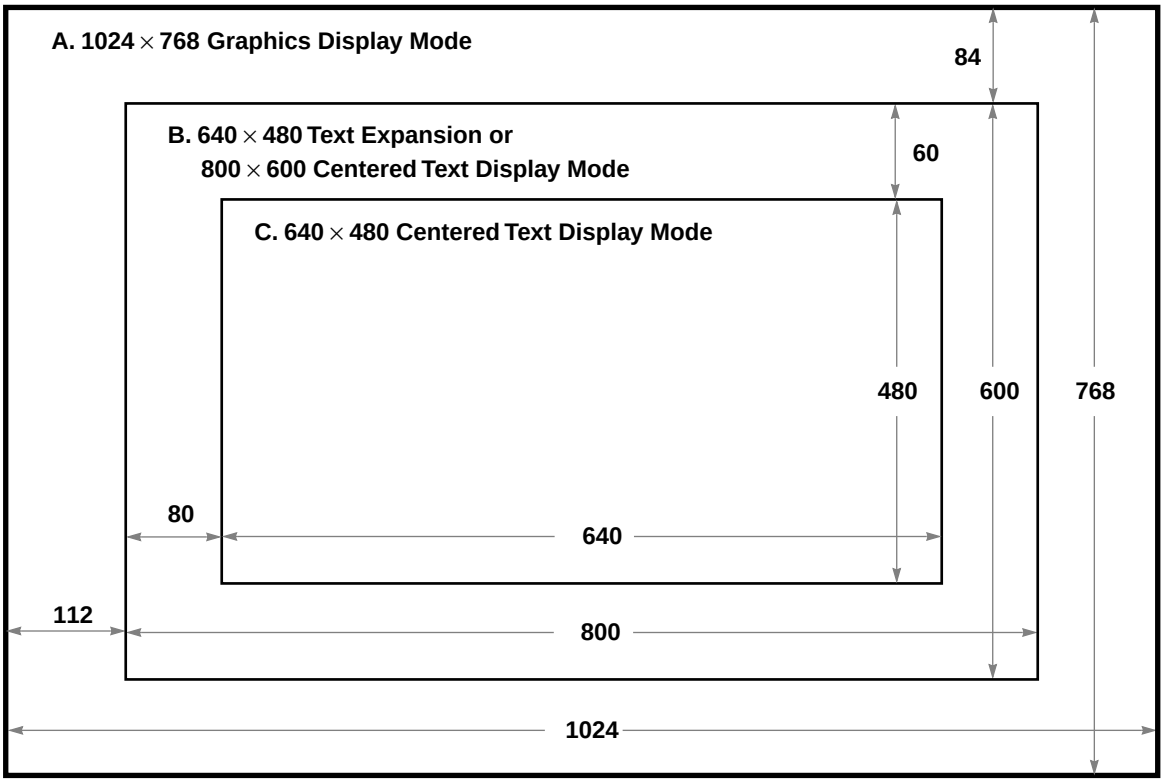


Figure 3-12. 1024 × 768 TFT Flat Panel: Appearance of Centered Display Modes

3.3.19.4 Top-Left-Aligned Option

Figure 3-13 shows how various graphics and text display modes appear when the CL-GD7556 is driving a 1024 × 768 TFT flat panel and the top-left-aligned option is used. In this case, all display modes start at the top-left corner of the display screen.

Example A

The CL-GD7556 is programmed for a graphics display mode that has a resolution of 1024 × 768. In this case, the entire display screen is used.

Example B

The CL-GD7556 is programmed for 640 × 480 text expansion and the 800 × 600 image is expanded. In this case, the display image starts at the top-left corner and is not centered. Also, blanking occurs on that portion of the display screen that is not used (that is, the bottom 168 scanlines and the 224 columns to the right of the used portion of the display screen).

Example C

The CL-GD7556 is programmed for a non-centered text display mode with a resolution of 640 × 480. In this case, the display image starts at the top-left corner and is not centered. Also, blanking occurs on that portion of the display screen that is not used (that is, the bottom 288 scanlines and the 384 columns to the right of the used portion of the display screen).

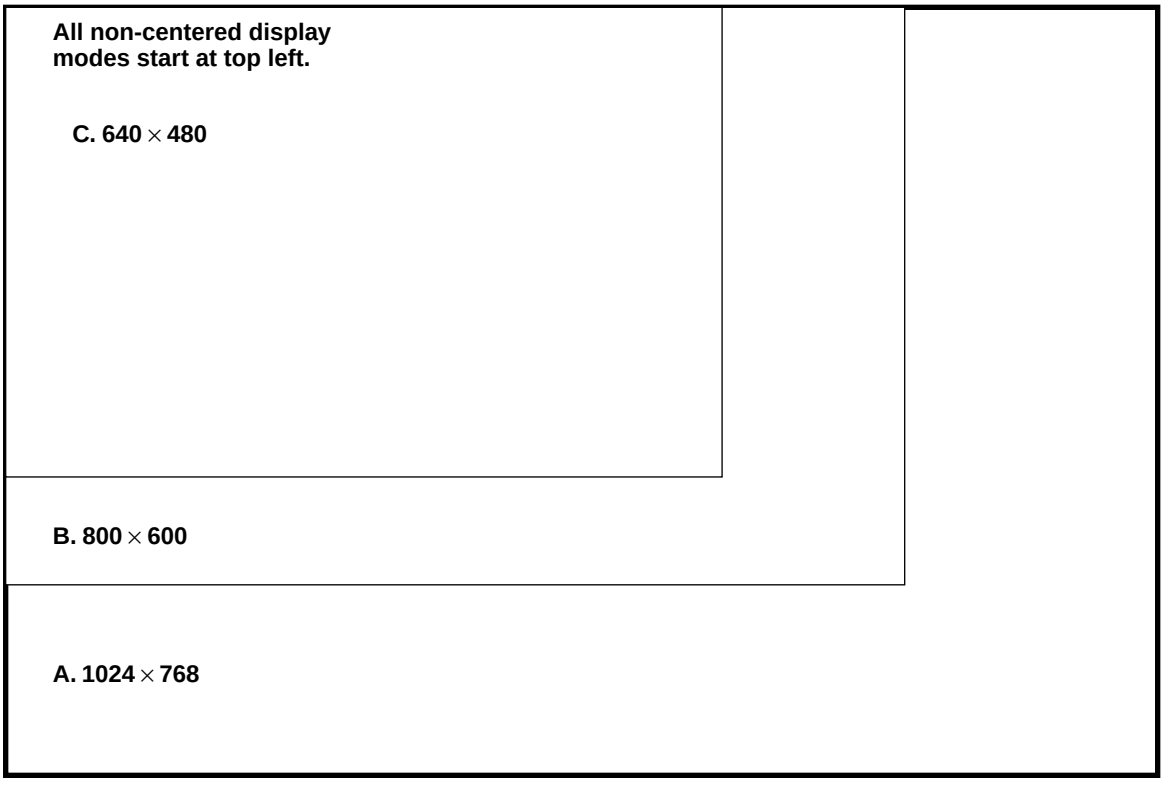


Figure 3-13. Appearance of Display Screen when Graphics/Text is Not Centered

3.3.19.5 Flat Panel Resolution Compensation

The CL-GD7556 uses its resolution compensation feature to allow PC applications that were originally written for analog CRT monitors to run transparently on flat panels. Unlike CRT monitors, flat panels have a fixed horizontal and vertical resolution. However, for standard VGA display modes, the horizontal and vertical resolution can range from 320 × 200 to 720 × 400.

As a result, when a PC application that uses standard VGA display modes is activated, the VGA display mode being used can have a resolution that is lower than the fixed resolution of the flat panel. Consequently, unless flat panel resolution compensation is used, a section of the flat panel is left blank.

For example, when VGA text display mode 3h, which consists of 400 scanlines, is displayed on a 640 × 480 flat panel that does not have flat panel resolution compensation, 80 blank scanlines remain at the bottom of the flat panel. (For a list of various horizontal and vertical resolutions for standard VGA modes, refer to Chapter 4.)

The CL-GD7556 flat panel resolution compensation presents these options:

- Automatic centering of VGA text and graphics display modes on a CRT monitor when SimulSCAN mode is used
- Horizontal expansion of VGA text and graphics display modes
- Vertical expansion of VGA text and graphics display modes
- Horizontal centering of VGA text and graphics display modes
- Vertical centering of VGA text and graphics display modes

NOTES:

1) For 640 × 480 and 800 × 600 flat panels either expansion or automatic centering must be enabled.
   1a) If Extension register CR82 has bits set for expansion, then the CR82 bits for automatic centering must be cleared.
   1b) If Extension register CR82 has bits set for automatic centering, then the CR82 bits for expansion must be cleared
2) When graphics display modes are expanded to either 475 or 525 scanlines, the display image on a flat panel or CRT monitor is top-aligned.

GUI-based applications, such as Windows or OS/2, use a CL-GD7556 driver that selects the proper display mode (such as those using 256-, 32K-, 64K-, or 16M-color modes) to run application programs at the full resolution of 640 × 480, 800 × 600, or 1024 × 768 flat panels. Graphics expansion is used with either DOS-based applications, such as still-image viewers, or with games when these products do not supply hardware-specific device drivers that match the resolution of the flat panel used.

Resolution Compensation for 640 × 480 Flat Panels

For 640 × 480 flat panels, the CL-GD7556 provides the following flat panel resolution-compensation options to display lower-resolution VGA text and graphics:

- **Automatic Text Expansion (Extension Register CR81):**

  Automatic expansion of VGA text makes the text font consistent across the flat panel and eliminates any breaks or artifacts in adjacent text.

  — For 9-pixel-wide VGA text , which is used by VGA text display modes 3h and 7h, characters are horizontally displayed as 8-pixel-wide text. As a result, 80 characters fill all 640 pixels across.

  — The following methods automatically expand VGA character text vertically to 19 pixels. As a result, 475 of the 480 vertical scanlines are filled.

    — For 8 × 8 (200-scanline) VGA text display modes, the text characters are double-scanned, vertically expanding the text from 8 scanlines to 16 scanlines. An extra top scanline and two extra bottom scanlines are added to each character, further vertically expanding the text to equal 19 scanlines.

    — For 8 × 14 (350-scanline) VGA text display modes, two extra top scanlines and three extra bottom scanlines are added to each 14-scanline character, to vertically expand the text to 19 scanlines.

    — For 8 × 16 (400-scanline) VGA text display modes, an extra top scanline and two extra bottom scanlines are added to each 16-scanlines character to vertically expand the text to 19 scanlines.

- **Automatic Horizontal and Vertical Centering of Graphics and Text (Extension Registers CR81–CR82):**

  — When standard VGA display modes are displayed and expansion of graphics or text is not used, then register control can be used for the automatic horizontal and vertical centering of a 200-, 350-, or 400-scanline VGA graphics or text display mode.

  — During SimulSCAN, when expansion is not selected, the image on a CRT monitor is automatically centered. For the CRT monitor, top-left alignment can be selected as an option.

- **Vertical Graphics Expansion (Extension Register CR82):**

  On a 640 × 480 flat panel, vertical graphics expansion can be used to run PC application programs that use lower-resolution VGA graphics display modes.

  — The 200-scanline VGA graphics display modes are vertically expanded to 475 scanlines by expanding every 8 scanlines to 19 scanlines, using a pattern of 0,0,1,1,2,2,2,3,3,4,4,5,5,5,6,6,7,7,7, (double and triple scan).

  — The 350-scanline VGA graphics display modes are vertically expanded to 475 scanlines by expanding every 14 scanlines to 19 scanlines, using a pattern of 0,1,2,2,3,4,5,5,6,7,7,8,9,a,a,b,c,d,d (single and double scan).

Resolution Compensation for 800 × 600 Flat Panels

For 800 × 600 flat panels, the CL-GD7556 provides the following flat panel resolution-compensation options to display lower-resolution VGA text and graphics.

NOTE: Resolution compensation applies to modes less than or equal to 8 bpp.

- **Automatic Text Expansion (Extension Register CR81):**

  Automatic expansion of VGA text makes the text font consistent across the flat panel and eliminates any breaks or artifacts in adjacent text.

  — The following methods horizontally expand the VGA text:
    — For 9-pixel-wide VGA text, which is used by VGA text display modes 3h and 7h, characters are horizontally displayed as 10-pixel-wide text, by replicating the last pixel once. As a result, 80 characters fill 800 pixels across.
    — In the case of 1024 × 768 flat panels, each character displayed is also centered horizontally in addition to being expanded to fill 800 pixels across.
  — The following methods vertically expand VGA text. As a result, all 600 vertical scanlines are filled.
    — For 8 × 8 (200-scanline) VGA text display modes, the characters are double-scanned, and then four extra blank scanlines are added to both the top and bottom of each character.
    — For 8 × 14 (350-scanline) VGA text display modes, extra blank scanlines are added to each character, four scanlines on the top and six scanlines on the bottom.
    — For 8 × 16 (400-scanline) VGA text display modes, extra blank scanlines are added to each character, four scanlines on the top and four scanlines on the bottom.

- **Automatic Horizontal and Vertical Centering of Graphics and Text (Extension Registers CR81–CR82):**
  — When standard VGA display modes are displayed and expansion of graphics or text is not used, then register control can be used for the automatic horizontal and vertical centering of a 200-, 350-, or 400-scanline VGA graphics or text display mode on a 600-scanline flat panel.
  — During SimulSCAN, when expansion is not selected, the image on a CRT monitor is automatically centered. For the CRT monitor, top-left alignment can be selected as an option.

- **Horizontal Graphics Expansion (Extension Register CR82):**

  VGA graphics display modes that are 640 pixels wide can be horizontally expanded to 800 pixels by replicating every fourth pixel.

- **Vertical Graphics Expansion (Extension Register CR82):**

  On a 800 × 600 flat panel, vertical graphics expansion can be used to run PC application programs that use lower-resolution VGA graphics display modes. For example, VGA graphics display modes that are:

  — 200 scanlines are vertically expanded to 600 scanlines by triple scanning every scanline.
  — 350 scanlines are vertically expanded to 525 scanlines by replicating all odd scanlines.
  — 480 scanlines are vertically expanded to 600 scanlines by replicating every fourth scanline.

3.3.20 FasText™ – Font Loading Option (Extension Registers CR1B and SR25)

On flat panels with a resolution greater than 640 × 480 and a 60-Hz or higher refresh rate, support for quality-looking VGA text display mode can be difficult to provide, because it requires a large graphics memory bandwidth for the part of display memory reserved for graphics. This difficulty stems from two problem areas:

1) Because of VGA architecture limitations, character fonts for VGA text display modes are fetched using random-read cycles. Also, for the exact same character, each of the eighty 8 × 16 or 9 × 16 character scanlines needs different data from the font table. In addition, text display mode scrolling requires first, a read from display memory of the entire display screen starting from the second character line on down, and then a write to display memory of the first character line. This process is repeated for each scrolled character line. Furthermore, as the display resolution increases to 800 × 600 and 1024 × 768, a larger amount of data must be fetched because of pixel expansion and increased scanlines. As a result, the amount of data that must be moved to and from display memory using random-read cycles increases considerably.

2) On CRT monitors and 640 × 480 flat panels, VGA text display modes run at a 25- to 28-MHz VCLK rate. However, on higher-resolution flat panels, these same display modes must run at higher VCLK rates (that is, 40 MHz for 800 × 600 flat panels and 65 MHz for 1024 × 768 flat panels). The higher VCLK rates compound the first problem area because, in order to to prevent CRT FIFO underflow, they increase the amount of data that must be retrieved from display memory.

The CL-GD7556 provides two solutions to the problem areas:

1) Increased memory bandwidth, that is, a 64-bit display memory interface. This bandwidth essentially doubles the amount of data that can be fetched on each clock cycle, compared to 32-bit memory interfaces.

2) FasText™ mode, an automated page-mode memory font access for text display modes. The page-mode memory cycles, which use fewer clock cycles than random-read memory cycles, provide a much faster and more efficient memory access. FasText mode is a user-selectable option that configures the font memory so that, instead of random-read memory accesses, page-mode memory accesses are used to fetch the font data during display time. Because the FasText option operates transparent to the software, this option is VGA compatible.

3.3.21 Frame Rate Modulation for Color Dual-Scan STN Panels

The CL-GD7556 employs a FRM (frame-rate modulation) algorithm to create shades on color dual-scan STN flat panels. The FRM algorithm modulates the 'on' and 'off' times of individual pixels in the flat panel over multiple frames, such that the eye integrates the superimposed pixels as perceptible color shades.

Proprietary techniques reduce or eliminate entirely the grayscale artifacts (for example, flicker, noise, and pattern motion). Outstanding display quality on state-of-the-art dual-scan STN flat panels with fast response times of approximately 100 ms, can be achieved.

The CL-GD7556 provides three FRM options. These options allow masking of undesirable color shading artifacts such as flicker or pattern motion.

- **16-frame FRM:** This FRM option modulates the pixel over 16 frames in time to create 16 shades for each primary R,G,B color, for a total of 4,096 (16^3) colors. This option is intended to support dual-scan STN flat panels currently available and in development, including dual-scan STN flat panels with very fast response times of approximately 100 ms.
  - — If two color shades are masked, the FRM algorithm produces 2,744 (14^3) colors.
  - — If four color shades are masked, the FRM algorithm produces 1,728 (12^3) colors.
- **8-frame FRM:** This FRM option modulates the pixel over 8 frames in time to create 8 shades for each primary R,G,B color, for a total of 512 (8^3) colors. This option is intended to reduce flicker and 'submarining' (that is, the temporary disappearance of the mouse pointer) on future dual-scan STN flat panels that have response times that are too fast for the 16-frame FRM option.
- **4-frame FRM:** This FRM option modulates the pixel over 4 frames in time to create 4 shades for each primary R,G,B color, for a total of 64 (4^3) colors. This option is intended to reduce flicker and 'submarining' on future dual-scan STN flat panels that have response times that are too fast for both the 16- and 8-frame FRM options.

In summary, the FRM algorithm produces 2, 3, or 4 bits of color depth for each primary R,G,B color on dual-scan STN flat panels. Greater color depth can be accomplished as follows:

- To add up to 6 bits of color depth to each primary R,G,B color, the dithering engine can be used with an FRM algorithm.
- To add up to 8 bits of color depth to each primary R,G,B color (that is, to add 256 color shades to each primary R,G,B color) for a total of 16M colors, the dithering engine can be used with only a 4-frame FRM algorithm.

3.3.22 Dithering Engine (Extension Registers CR87–CR89)

The dithering engine increases the number of perceived colors displayed on the flat panel and/or CRT monitor, relative to what the display can physically produce without dithering.

A proprietary spatial dithering technique preserves the resolution of the displayed image. For example, when a 640 × 480 resolution image is dithered, its resolution is maintained, instead of being reduced to 320 × 240.

The dithering engine works by automatically selecting a dithering pattern. As shown in Table 3-12, an increase in the dithering pattern increases the number of displayed bits per primary R,G,B color, depending upon the color depth of the source image.

Table 3-12. Effective Dithering Patterns

Effective Dithering Pattern	Increased Number of Displayed Bits per Primary R,G,B Color
2 × 1	1 bit
2 × 2	2 bits
4 × 2	3 bits
4 × 4	4 bits
8 × 4	5 bits
8 × 8	6 bits

The dithering engine can automatically add up to 6 bits per primary R,G,B color, and it can be used for color dual-scan STN and TFT flat panels. By programming Extension register bit CR87[7], this automatic feature can be overridden and the number of bits per primary R,G,B color limited to a programmable number.

As shown in the block diagram, Figure 3-6 on page 3-33, the dithering engine function comes after the flat panel resolution compensation in the data path, so that dithering is applied to the expanded image.

The dithering engine contains these separate dithering registers:

- Dithering register for standard/extended VGA modes (Extension registers CR87 and CR88[3:0])
- Dithering register for a video window (Extension registers CR88[7:4] and CR89)

To render the appropriate colors, the CL-GD7556 dynamically switches dithering between surrounding graphics and the video window.

Table 3-13 illustrates the number of displayed colors on a color dual-scan STN flat panel that has various FRM and dithering options. The total number of colors is equal to three times the number of colors per primary R,G,B color.

Table 3-13. Number of Colors on Color Dual-Scan STN Flat Panels

Primary R,G,B Color			Resulting Image on Color Dual-Scan STN Flat Panel When Source Is:	
Frame-Rate Modulation Option	Generated by Flat Panel		32K Colors (15 bits)	16M Colors (24 bits)
	Dithering Pattern	Number of Bits		
4 frames (2 bits)	None	0	64 (2^6)	
	2×1	1	512 (2^9)	
	2×2	2	4K (2^{12})	
	4×2	3	32K (2^{15})	
	4×4	4	NA[a]	256K (2^{18})
	8×4	5	NA[a]	2M (2^{21})
	8×8	6	NA[a]	16M (2^{24})
8 frames (3 bits)	None	0	512 (2^9)	
	2×1	1	4K (2^{12})	
	2×2	2	32K (2^{15})	
	4×2	3	NA[a]	256K (2^{18})
	4×4	4	NA[a]	2M (2^{21})
	4×8	5	NA[a]	16M (2^{24})
16 frames (4 bits)	None	0	4K (2^{12})	
	2×1	1	32K (2^{15})	
	2×2	2	NA[a]	256K (2^{18})
	4×2	3	NA[a]	2M (2^{21})
	4×4	4	NA[a]	16M (2^{24})

[a] 'NA' indicates a combination that is not applicable (that is, the result cannot be a higher resolution than the source).

Table 3-14 shows the number of colors that various dithering patterns produce on 512-color TFT flat panels. If an image using the standard VGA 18-bit color palette is displayed on a 512-color TFT flat panel (that is, one which has only a 9-bit color palette), artifacts such as contour lines or significant banding are readily apparent on the display screen.

Consequently, the dithering engine automatically uses a 4×2 pattern to increase the number of displayed colors from the 3 bits per primary R,G,B color that the flat panel produces to the full 6 bits per primary R,G,B color, in order to meet the 18-bit VGA color palette requirement for the color depth of the displayed image.

Table 3-14. Number of Colors Produced by Dithering Patterns on 512-Color TFT Flat Panels

Primary R,G,B Color Generated by Flat Panel		Resulting Image on Color TFT Flat Panel When Source Is:		
Dithering Pattern	Number of Bits	32K Colors (15 bits)	64K Colors (16 bits)	16M Colors (24 bits)
None	0	512 (2^9)		
2×1	1	4K (2^{12})		
2×2	2	32K (2^{15})		
4×2	3	NA[a]	256K (2^{18})	256K (2^{18})
4×4	4	NA[a]	2M (2^{21})	2M (2^{21})
8×4	5	NA[a]	16M (2^{24})	16M (2^{24})

[a] 'NA' indicates a combination that is not applicable (that is, the result cannot be a higher resolution than the source).

Table 3-15 shows the number of colors that various dithering patterns produce on 4K-color TFT flat panels.

Table 3-15. Number of Colors Produced by Dithering Patterns on 4K-Color TFT Flat Panels

Primary R,G,B Color Generated by Flat Panel		Resulting Image on Color TFT Flat Panel When Source Is:		
Dithering Pattern	Number of Bits	32K Colors (15 bits)	64K Colors (16 bits)	16M Colors (24 bits)
None	0	4K (2^{12})		
2×1	1	32K (2^{15})		
2×2	2	NA[a]	256K (2^{18})	256K (2^{18})
4×2	3	NA[a]	2M (2^{21})	2M (2^{21})
4×4	4	NA[a]	16M (2^{24})	16M (2^{24})

[a] 'NA' indicates a combination that is not applicable (that is, the result cannot be a higher resolution than the source).

Table 3-16 shows the number of colors that various dithering patterns produce on 256K-color TFT flat panels.

Table 3-16. Number of Colors Produced by Dithering Patterns on 256K-Color TFT Flat Panels

Primary R,G,B Color Generated by Flat Panel		Resulting Image on Color TFT Flat Panel When Source Is:		
Dithering Pattern	**Number of Bits**	**32K Colors (15 bits)**	**64K Colors (16 bits)**	**16M Colors (24 bits)**
None	0	32K (2^{15})	64K (2^{16})	256K (2^{18})
2 × 1	1			2M (2^{21})
2 × 2	2			16M (2^{24})

3.3.23 Frequency Synthesizer

The frequency synthesizer generates all clock frequencies for the operation of VGA display modes and VGA extension display modes. Using a single reference frequency of 14.318 MHz that is supplied from an external TTL-level source, the frequency synthesizer generates two fully programmable clocks — VCLK (the video clock) and MCLK (the memory clock). In addition, the CL-GD7556 has integrated support for MFILTER and VFILTER, which are used to stabilize these clock signals from the frequency synthesizer.

For a functional diagram of the frequency synthesizer, refer to Figure 3-14.

- VCLK
  - — VCLK is the fundamental video timing clock that generates all clocks needed for video display timing signals (for example, HSYNC and VSYNC).
  - — VCLK must be changed to support various display mode resolutions and refresh rates.
  - — The VCLK frequencies are programmed with Extension registers SRB–SRE and SR1B–SR1F.
  - — The CL-GD7556 supports VCLKs up to 135 MHz at 3.3 V.
- MCLK
  - — MCLK generates all clocks needed for memory timing signals (for example, RAS# and CAS#).
  - — MCLK must be optimized for the speed of the display memory used.
  - — MCLK frequencies are programmed with Extension register SR1F.
  - — The CL-GD7556 supports MCLKs up to 80 MHz at 3.3 V.

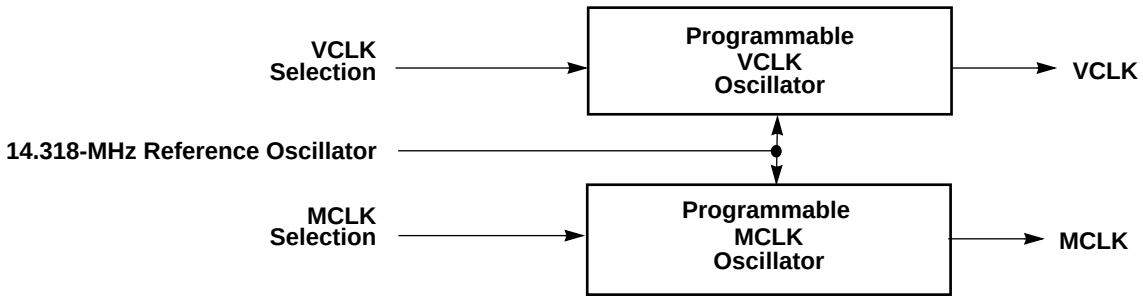


Figure 3-14. Programmable Dual-Frequency Synthesizer Functional Diagram

3.4 CL-GD7556 Controller Operation

Section 3.4.1 through Section 3.4.5 describe the CL-GD7556 controller operation.

3.4.1 Power Management (Extension Registers CR80 and CR8A–CR8D)

The CL-GD7556 supports power-management techniques to maximize battery life, including:

- **Flat panel-only power savings:** During flat panel-only operations, the DAC (including its CRT monitor sense comparators) is powered down, and VCLK can be reduced to a level that still minimizes flicker.
- **Flat panel power-up/down sequence control:** To protect the flat panel, the FPVEE and FPVCC output signals control the flat panel power-up and power-down sequence. Extension register bit CR8A[5] provides the status of the power-down sequence.

  CAUTION: Damage can occur if VEE (the flat panel high-voltage power) is applied without VDD (the flat panel logic power).

- **Mixed-voltage interfaces:** The host CPU bus, display memory, flat panel, and CRT monitor interfaces can each be operated at either 3.3 V or 5.0 V. The CL-GD7556 I/O pins all communicate using a CMOS 3.3 V signal. However, these I/O pins are 5.0 V tolerant, and can drive TTL 5.0 V logic with the normal TTL high and low threshold levels.
- **Active power management:** The CL-GD7556 controller has large functional sections (such as the MVA and the internal hardware for flat panels) that are not active all the time but do consume power while other activity is going on in the CL-GD7556 controller. The CL-GD7556 allows these areas to be essentially 'turned off' by disabling the clocks to these sections, reducing the amount of power the CL-GD7556 uses while active. After initialization, the VGA BIOS must turn these clocks off at POST, if they are not in use. Drivers (or display configuration utilities such as WinMode, in the case of a flat panel) can then turn on the clocks when these functional sections are needed, and subsequently, turn off the clocks when these functional sections are not needed.
- **Standby mode:** This mode reduces power consumption by turning off the display screen while allowing application programs to continue to run normally in the background.
  - Standby mode is entered either by a time-out of the internal Standby Counter, or by programming Extension register bit CR80[3] to 1.
  - During Standby mode, by using proper flat panel power sequencing, either the flat panel, the CRT monitor, or both are turned off, VCLK is stopped, and the video DAC is powered down. The host CPU can still access and modify the display memory, palette RAM, and Attribute registers.
  - Standby mode is exited by resetting either the timer for the Standby Counter or the bit that initiated the Standby mode.
    - The internal Standby Counter can be reset either by activity on the ACTI pin or by a VGA memory access, which is controlled by Extension register bits CR8D[4:3].
    - Software-controlled Standby is exited by clearing Extension register bit CR80[3] to 0.
  - Standby mode status is provided by Extension register bit CR8A[4].

- **Suspend mode:** This mode reduces power consumption when the system remains inactive for a relatively long period of time, while maintaining the contents of the CL-GD7556 registers, palette, and display memory. However, unlike the Standby mode, during the Suspend mode, applications are suspended and do not continue to run normally in the background.
  - — Suspend mode is entered either through hardware or software.
    - — Hardware-controlled Suspend is entered by way of the SUSPI pin, which has programmable polarity. During hardware-controlled Suspend, the display is turned off, the VCLK and MCLK clocks are both stopped, and host CPU accesses to the display memory, palette, and I/O registers cease. The CL-GD7556 configures display memory for self-refresh or uses the 32-kHz clock for memory refresh.
    - — Software-controlled Suspend is entered by setting Extension register bit CR80[2] to 1. In contrast to hardware-controlled Suspend, software-controlled Suspend allows the host CPU to access the CL-GD7556 internal registers, which requires an active clock and I/O capability, and consequently, more power.
  - — Once the Suspend mode is activated, the CL-GD7556 first initiates Standby power-down sequencing. The Suspend status pin (that is, SUSPST#) is then asserted and MCLK is stopped. In the case of hardware-controlled Suspend, the host CPU bus is put into high-impedance mode.
  - — Suspend mode must be exited in the same manner that it was entered. When Suspend mode is exited, any application programs that were previously running can be quickly re-started from the point at which they suspended.
    - — Hardware-controlled Suspend is exited by setting SUSPI pin high.
    - — Software-controlled Suspend is exited by resetting CR80[2] to 0.
- **VESA DPMS:** The CL-GD7556 supports the VESA DPMS (display power management specification) for CRT monitor power management. Systems can easily comply with the U.S. Environmental Protection Agency's Energy Star Computer qualifications. For more information, refer to the appendixes.

3.4.2 Surrounding-Graphics Color-Palette Operation

3.4.2.1 Writing to the CLUT

To write a color definition to the CLUT (color-palette), a value specifying an address location in the CLUT is first written to External/General register 3C8 (the Pixel Address Write Mode register). The color values for the red, green, and blue intensities are then written in succession to External/General register 3C9 (the Pixel Data register). After the blue data bits are latched, the new color data bits are then written into the CLUT at the defined address, and the CL-GD7556 automatically increments the 3C8 register. Since the CL-GD7556 increments the 3C8 register after each transfer of data to the CLUT, it is best to write a set of consecutive locations at once.

As explained in Section 3.3.16 on page 3-44, the values for the RGB data in the CLUT can be modified for extended color applications to account for gamma variations between the graphics source and destination systems.

3.4.2.2 Reading from the CLUT

To read color data from the CLUT, a value specifying the address location of the data is written to External/General register 3C7 (the Pixel Address Read Mode register). After the address is latched, data bits from this location are automatically read out to External/General register 3C9 (the Pixel Data register), and the CL-GD7556 automatically increments External/General register 3C8 (the Pixel Address Write Mode register).

The color intensity values are then read from register 3C9 by a sequence of three read (RD#) commands. After the blue value is transferred out, new data bits are read from the CLUT current address to register 3C9, which causes the CL-GD7556 to automatically increment register 3C8.

If the CL-GD7556 loads the Address register with a new starting address while an unfinished sequence is in progress, the system resets and starts a new sequence. This action occurs for both read and write operations.

3.4.3 Compatibility

The CL-GD7556 includes all registers and data paths required for standard VGA controllers. It also supports various 132-column text display modes as well as the following extended VGA display modes:

- 800 × 600 with 16M colors in flat panel-only mode and SimulSCAN (with CRT monitor non-interlaced)
- 1024 × 768 with 64K colors in flat panel-only mode and SimulSCAN (with CRT monitor non-interlaced)
- 1280 × 1024 with 256 colors in CRT-only mode

3.4.4 Testability

The CL-GD7556 is tested by using pin-scan testing and a signature generator. Pin-scan testing checks the signal state of every pin on the chip. The test detects any pins that are not connected to the board, or that are shorted to a neighboring pin or trace. The signature generator allows the entire system, including display memory, to be tested at full speed. For more information, refer to the appendixes.

3.4.5 Configuration Inputs

The CL-GD7556 is configured for operation with a combination of hardware pins and software registers.

3.4.5.1 Hardware Configuration Inputs

Pull-up resistors can be connected to some memory data pins, which are read either during the low-to-high transition of the system reset or when Extension register bit SR24[3] is toggled.

- **On-chip PCI BIOS support for external BIOS decode.** This configuration selects on-chip PCI BIOS for use.
- **Memory mapped I/O.** This configuration selects the ability to memory map the CL-GD7556 VGA registers for support of non-PC environments.
- **Relocatable I/O.** This configures the CL-GD7556 to enable the PCI relocatable I/O.
- **Pin Scan.** This configuration enables pin-scan testing.
- **Test Mode.** This configuration enables pin-scan testing and some factory-only tests.
- **External Clock on VCLK and MCLK.** This configures these two pins for external clock synthesizer operation.
- **32K BIOS ROM Size.** This configuration selects a physical BIOS ROM size of 32 Kbytes, which is normally not used. The default is a physical BIOS ROM size of 64 Kbytes, since the actual size requirement for the VGA BIOS code is 48 Kbytes.

If a hardware configuration pin does not have a pull-up resistor connected to it, it is read as low because of the CL-GD7556 internal pull-down resistors. The status of the inputs on these pins is stored in Extension registers SR22 and SR24 at system reset.

Two hardware switch inputs (SW2PU and SW1PU) are controlled by external pull-up resistors and read during system reset. One hardware switch input (SW0) is read during each horizontal retrace period. These inputs are used by the VGA BIOS to monitor external activities that can affect the chip operation. The status of these three inputs is stored in Extension register bits SR24[2:0].

3.4.5.2 Software Configuration Inputs

Software-programmable registers are used to select the desired function of some multi-function pins as defined below:

- **CAS[1:0]# / WE[1:0]#.** Depending on the type of DRAM used, these pins are configured as CAS# or WE# by programming Extension register bit SRF[0].
- **MCLK VCO Output select.** Extension register bits SR23[2,0] select whether the MCLK or MCLK VCO output is used.
- **MCLK on SWO/MCLK/XMCLK.** Extension register bits SR22[2] and SR23[2,0] select whether the SW0, MCLK, or XMCLK output is used.
- **VCLKO output enable.** When Extension register bit SR23[4] is 1, the DDCC/VCLKO output (pin 98) reflects the voltage level of the internal VCLK.

For more configuration information, refer to Chapter 2 and the appendixes.

3.5 Software Support

The CL-GD7556 VGA BIOS is a high-quality, feature-rich firmware product designed to take maximum advantage of the CL-GD7556 controller, especially in the areas of display quality, power management, and graphics performance. The key features of the VGA BIOS are:

- Compatible with Super VGA BIOS
- Supports SimulSCAN operation
- Supports the power-management modes
- Supports enhancement features for display modes
- Can be integrated with the system BIOS
- Supports switchless configuration
- Can be customized without source code by using Cirrus Logic utility programs such as OEMSI
- Provides VESA-compatible modes and 1.2-function support for VBE (VGA BIOS Extensions)
- Supports multiple refresh rates for CRT monitors

A VGA BIOS, compatible with the standard IBM VGA BIOS and the INT 10h graphics service functions, is available from Cirrus Logic and third-party BIOS vendors. The CL-GD7556 controller and its VGA BIOS can be implemented as an add-in daughterboard or placed directly on the system motherboard. The core of the VGA BIOS requires 48-Kbyte linear addressing. The VGA BIOS can be located at either C000h or E000h. The VGA BIOS can also be used for host CPU bus implementations.

3.5.1 Software Utilities for OEM Development

This section lists CL-GD7556 software utilities that Cirrus Logic provides for OEM development use.

OEMSI

The OEM System Integration utility allows the Cirrus Logic VGA BIOS to be customized to support unique OEM system functions and features.

Regs7555

This utility is a Windows-based VGA controller register viewer/editor utility that provides the following:

- Regs7555 enables the CL-GD7556 standard and extension VGA registers and the color palette to be displayed and edited from within Windows.
- The Regs7555 Help screen provides a brief explanation of each bit in each register.
- Regs7555 enables register values to be changed either by typing in a new hex value or toggling individual bits.
- Regs7555 allows manipulation of a video window regarding its position, data format, resolution, and so forth.

PCLRegs

This utility is a DOS-based VGA controller register viewer/editor utility that provides the following:

- PCLRegs enables the CL-GD7556 standard and extension VGA registers and the color palette to be displayed and edited.
- The PCLRegs Help screen provides a brief explanation of each bit in each register.
- PCLRegs enables register values to be changed either by typing in a new hex value or toggling individual bits.
- PCLRegs displays a variety of CL-GD7556 configuration data, including the status of the CRT controller, the graphics display mode being used, information about the VGA BIOS, and hardware cursor information.

3.5.2 Software Support for End Users

Cirrus Logic provides the following CL-GD7556 software for distribution to end users. See the *CL-GD7556 Software Reference Manual* for details.

Drivers

The CL-GD7556 simplifies driver support for third-party sources because the CL-GD7556 design is based on the industry-leading CL-GD5436 VGA controller. As a result, a driver supplier can easily modify an existing CL-GD5436 driver to support the CL-GD7556. At a minimum, this utility allows the CL-GD7556 to operate within the restrictions of the older CL-GD5436 driver. The CL-GD7556 supports the following drivers:

- Windows 95 driver
- Windows NT, version 3.5x
- Windows 3.1X driver
- DirectDraw/DirectVideo for Video for Windows under Windows 95
- DCI 1.x drivers for Video to Windows 1.1.2 or later under Windows 3.1
- OS/2®, version 3.0
- AutoCAD®

NOTE: Driver support for the Japanese version of Windows and OS/2 is also available.

Windows 95 Utilities

This utility is a Windows 95 application for configuring the display screen. The Cirrus Logic CL-GD7556 utilities are located in the 'Display Properties' folder under the 'Refresh' tab. With these utilities, end users can enable the following options:

- Set high refresh rates for CRT monitors
- Select from among the display device options: CRT monitor, flat panel, or SimulSCAN
- Select between either the NTSC or PAL television encoding schemes
- Select from among the language options for displaying the Win 95 utilities

CLMode

This utility, a DOS-based graphics display mode and display-configuration utility, provides the following:

- Through its user-friendly VGA Configuration menu, CLMode enables users to turn 'on' and 'off' a variety of graphics configuration options, including the following:
  - — Automatic text expansion
  - — Power-management options
  - — Reverse video
  - — Selection between display options: CRT-only, flat panel-only, and SimulSCAN
  - — Selection between NTSC and PAL television modes
  - — Shading of graphics and text
  - — Text enhancement
  - — Vertical position of display
- The CLMode Monitor Type Setup menu enables users to set CRT monitor resolution and refresh rate.
- The CLMode Video Modes Preview menu enables users to display the various VGA display modes.
- The CLMode utility enables new settings of the above options by using the AUTOEXEC.BAT file.

WinMode

This utility is a Windows 3.1x and OS/2 based application for configuring the display screen. A unique feature of the WinMode utility is the ability to automatically switch the resolution of the display screen without relaunching Windows. This feature ensures that a user of a flat panel always sees a Windows display, even when the user dynamically switches from using a high-resolution CRT monitor to a flat panel that has a lower resolution. This feature also enables the user to avoid running the Windows Setup application in order to find and switch driver resolutions. (However, to change the number of colors used by the display screen, Windows must still be restarted.)

With WinMode, users have the following options (and can use the AUTOEXEC.BAT file to enable new settings for the options):

- Set high refresh rates for CRT monitors.
- Set the resolution for a CRT monitor to one of the following:
  - 640 × 480
  - 800 × 600
  - 1024 × 768
  - 1280 × 1024
- Select the color depth for either a CRT monitor or a flat panel to one of the following:
  - 256
  - 64K
  - 16M
- Turn the hardware cursor ‘on’ or ‘off’.
- Make the font size normal or large.

The WinMode utility, which defines the resolution and color depth of the CL-GD7556 Windows driver, also provides the following:

- Selection between display options: CRT monitor, flat panel, or SimulSCAN
- Selection between NTSC or PAL television modes, when a TV encoder is attached
- Selection to display WinMode in different foreign languages
- Selection for virtual display – the flat-panel display is panned and scrolled to allow an oversize image area to be viewed using normal resolutions

4. DISPLAY MODES

This chapter lists tables for configuring the CL-GD7556 for various CRT monitor and flat panel graphics and text display modes. For detailed information on specific flat panels that the CL-GD7556 can drive, refer to the “Panel Interface Guide” in the *CL-GD7556 Application Book*.

NOTE: The parameters detailed in the tables of this chapter define standard capabilities of the CL-GD7556 when it is used with the Cirrus Logic VGA BIOS. Consult with the appropriate BIOS vendor for information about display modes and parameters that are supported by BIOSs that are not from Cirrus Logic.

The following symbols and abbreviations are used for display modes in the following sections:

–	A minus sign (or no sign at all) after a display mode number indicates CGA display mode. (Table 4-1 only.)
*	EGA display mode. (Table 4-1 only.)
+	VGA display mode. (Table 4-1 only.)
‡	Indicates a 32K direct-color packed-pixel display mode
DSTN	Dual-scan STN flat panel
i	Indicates a display mode that uses an interlaced frequency
tbd	to be determined

4.1 CRT-Only Display Modes

This section lists tables for standard VGA and Cirrus Logic Extended VGA CRT-only display modes.

4.1.1 Standard VGA CRT-Only Display Modes

The CL-GD7556 VGA BIOS supports all standard VGA CRT-only display modes, listed in Table 4-1.

Table 4-1. Standard VGA CRT-Only Display Modes

Standard VGA Display Mode No. (hex)	VESA Display Mode Number	Color Depth (number of colors)	Characters × Rows	Character Cell (pixels)	Resolution (pixels)	Type of Display Mode	Horizontal Frequency (kHz)	Vertical Frequency (Hz)
00, 01	–	16/256K	40 × 25	8 × 8	320 × 200	Text	31.5	70
00*, 01*	–	16/256K	40 × 25	8 × 14	320 × 350	Text	31.5	70
00+, 01+	–	16/256K	40 × 25	9 × 16	360 × 400	Text	31.5	70
02, 03	–	16/256K	80 × 25	8 × 8	640 × 200	Text	31.5	70
02*, 03*	–	16/256K	80 × 25	8 × 14	640 × 350	Text	31.5	70
02+, 03+	–	16/256K	80 × 25	9 × 16	720 × 400	Text	31.5	70
04, 05	–	4/256K	40 × 25	8 × 8	320 × 200	Graphics	31.5	70
06	–	2/256K	80 × 25	8 × 8	640 × 200	Graphics	31.5	70
07*	–	Mono.	80 × 25	9 × 14	720 × 350	Text	31.5	70
07+	–	Mono.	80 × 25	9 × 16	720 × 400	Text	31.5	70
0D	–	16/256K	40 × 25	8 × 8	320 × 200	Graphics	31.5	70
0E	–	16/256K	80 × 25	8 × 8	640 × 200	Graphics	31.5	70
0F	–	Mono.	80 × 25	8 × 14	640 × 350	Graphics	31.5	70
10	–	16/256K	80 × 25	8 × 14	640 × 350	Graphics	31.5	70
11	–	2/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	60
12	–	16/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	60
13	–	256/256K	40 × 25	8 × 8	320 × 200	Graphics	31.5	70

4.1.2 Cirrus Logic Extended VGA CRT-Only Display Modes

Table 4-2 shows the extended VGA and VESA display modes that the CL-GD7556 VGA BIOS supports. For all display modes, the required CVDD is 3.3 V.

- Within the table:
  - The 'MCLK Minimum' column gives the recommended memory clock frequency at which the CL-GD7556 can run without adverse effects to functionality. Better benchmarks can be achieved with an MCLK frequency higher than the frequency specified.
  - Some of the display modes are not supported by all CRT monitors.
  - Unless otherwise noted, the display modes are supported with 1 Mbyte of display memory.
- Text display mode 54h is actually 1056 x 344 addressable pixels. However, it uses 1056 x 350 timing.
- Graphics display modes 11h and 12h are high-refresh derivations of the standard VGA CRT-only display modes 11h and 12h in Table 4-1. The graphics display modes 11h and 12h in this table have been enhanced by Cirrus Logic for a higher vertical frequency.
- Graphics display mode 6Ah must be used, rather than graphics display mode 58h, for application programs to retain compatibility with other VGA BIOS products.
- For the CRT monitor type that is selected, the fastest vertical refresh rate is automatically used.

Table 4-2. Cirrus Logic Extended VGA CRT-Only Display Modes

Extended VGA Display Mode No. (hex)	VESA Display Mode No. (hex)	Color Depth (number of colors)	Characters × Rows	Character Cell (pixels)	Resolution (pixels)	Horizontal Freq. (kHz)	Vertical Freq. (Hz)	VCLK (MHz)	MCLK Minimum (MHz)
Text Display Modes									
14	–	16/256K	132 × 25	8 × 16	1056 × 400	31.5	70	41.5	50
54	10A	16/256K	132 × 43	8 × 8	1056 × 350	31.5	70	41.5	50
55	109	16/256K	132 × 25	8 × 14	1056 × 350	31.5	70	41.5	50
Graphics Display Modes									
11	–	2/256K	80 × 30	8 × 16	640 × 480	37.9	72	31.5	50
						37.5	75	31.5	50
						43.269	85	36	50
12	–	16/256K	80 × 30	8 × 16	640 × 480	37.9	72	31.5	50
						37.5	75	31.5	50
						43.269	85	36	50
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	35.2	56	36	50
						37.8	60	40	50
						48.1	72	50	50
						46.875	75	50	50

Table 4-2. Cirrus Logic Extended VGA CRT-Only Display Modes *(cont.)*

Extended VGA Display Mode No. (hex)	VESA Display Mode No. (hex)	Color Depth (number of colors)	Characters × Rows	Character Cell (pixels)	Resolution (pixels)	Horizontal Freq. (kHz)	Vertical Freq. (Hz)	VCLK (MHz)	MCLK Minimum (MHz)
5C	103	256/256K	100 × 37	8 × 16	800 × 600	35.2	56	36	50
						37.9	60	40	50
						48.1	72	50	50
						46.875	75	50	50
						53.674	85	56.25	50
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	35.5	43i	44.9	50
						48.3	60	65	50
						56	70	75	50
						58	72	77	50
						60	75	78.75	50
5E	100	256/256K	80 × 25	8 × 16	640 × 400	31.5	70	25	50
5F	101	256/256K	80 × 30	8 × 16	640 × 480	31.5	60	25	50
						37.9	72	31.5	50
						37.5	75	31.5	50
						43.269	85	36	50
60	105	256/256K	128 × 48	8 × 16	1024 × 768	35.5	43i	44.9	50
						48.3	60	65	50
						56	70	75	50
						58	72	77	50
						60	75	78.75	50
						68.677	85	94.5	50
64	111	64K	–	–	640 × 480	31.5	60	25	50
						37.9	72	31.5	50
						37.5	75	31.5	50
						43.269	85	36	50
65	114	64K	–	–	800 × 600	35.2	56	36	50
						37.8	60	40	50
						48.1	72	50	50
						46.875	75	50	50
						53.674	85	56.25	50

Table 4-2. Cirrus Logic Extended VGA CRT-Only Display Modes *(cont.)*

Extended VGA Display Mode No. (hex)	VESA Display Mode No. (hex)	Color Depth (number of colors)	Characters × Rows	Character Cell (pixels)	Resolution (pixels)	Horizontal Freq. (kHz)	Vertical Freq. (Hz)	VCLK (MHz)	MCLK Minimum (MHz)
66	110	32K‡	–	–	640 × 480	31.5	60	25	50
						37.9	72	31.5	50
						37.5	75	31.5	50
						43.269	85	36	50
67	113	32K‡	128 x 48	8 × 16	800 × 600	35.2	56	36	50
						37.8	60	40	50
						48.1	72	50	50
						47	75	49.5	50
						53.674	85	56.25	50
68[a]	116	32K‡	128 x 48	8 × 16	1024 × 768	35.5	43i	44.9	50
						48.2	60	65	50
						56	70	75	60
						60	75	78.7	60
						68.677	85	94.5	66
69[b]	106	32K‡	160 × 64	8 × 16	1280 × 1024	48	43i	75	60
						63.981	60	108	80
6C	106	16/256K	160 × 64	8 × 16	1280 × 1024	48	43i	75	50
6D[a]	107	256/256K	160 × 64	8 × 16	1280 × 1024	48	43i	75	50
						64	60	108	50
						79.976	75	135	50
71	112	16M	80 × 30	8 × 16	640 × 480	31.5	60	25	50
						37.9	72	31.5	50
						37.5	75	31.5	50
						43.269	85	36	50
74[a]	117	64K	128 × 48	8 × 16	1024 × 768	35.5	43i	44.9	50
						48.3	60	65	50
						56	70	75	60
						60	75	78.7	60
						68.677	85	94.5	80
75[b]	11A	64K	160 × 64	8 × 16	1280 × 1024	48	43.5i	75	60
						63.981	60	108	66

Table 4-2. Cirrus Logic Extended VGA CRT-Only Display Modes *(cont.)*

Extended VGA Display Mode No. (hex)	VESA Display Mode No. (hex)	Color Depth (number of colors)	Characters × Rows	Character Cell (pixels)	Resolution (pixels)	Horizontal Freq. (kHz)	Vertical Freq. (Hz)	VCLK (MHz)	MCLK Minimum (MHz)
78[a]	115	16M	100 x 37	8 × 16	800 × 600	35.2	56	36	50
						37.8	60	40	50
						48.1	72	50	60
						47	75	49.5	60
						53.674	85	56.25	66
79[b]	118	16M	128 × 48	8 × 16	1024 × 768	35.5	43i	44.9	60
						48.3	60	65	80
						56	70	75	80

[a] A minimum of 2 Mbytes of display memory are required to support all of the capabilities of this display mode.

[b] This display mode requires 4 Mbytes of display memory.

4.2 Flat Panel-Only and SimulSCAN™ Display Modes

The CL-GD7556 VGA BIOS supports flat panel-only and SimulSCAN operations with the standard VGA display modes listed in Section 4.1. In addition, the CL-GD7556 VGA BIOS supports flat panel-only and SimulSCAN operations with the extended display modes listed in this section.

4.2.1 Flat Panel-Only and SimulSCAN 640 x 480 (VGA) Display Modes

For 640 x 480 flat panels, the Cirrus Logic VGA BIOS supports flat panel-only and SimulSCAN operations with the standard VGA display modes listed in Section 4.1 and the extended VGA display modes in Table 4-3. For all display modes, the required CVDD is 3.3 V.

- Within the table, the 'MCLK Minimum' column gives the recommended memory clock frequency at which the CL-GD7556 can run without adverse effects to functionality. Better benchmarks can be achieved with an MCLK frequency higher than the frequency specified.
- DSTN flat panels require display memory for frame accelerator functionality.
- For SimulSCAN operation:
  - — Both the flat panel and the CRT monitor must be configured at a minimum to support the resolution of a given SimulSCAN display mode.
  - — The expanded display mode is disabled by default.

Table 4-3. Flat Panel-Only and SimulSCAN™ Display Modes for 640 x 480 Flat Panels

Extended VGA Display Mode Number (hex)	VESA Display Mode Number (hex)	Color Depth (number of colors)	Characters × Rows	Character Cell (pixels)	Resolution (pixels)	Type of Flat Panel	VCLK[a] (MHz)	MCLK Minimum (MHz)
5E	100	256/256K	80 × 25	8 × 16	640 × 400	DSTN/TFT	25	50
5F	101	256/256K	80 × 30	8 × 16	640 × 480	DSTN/TFT	25	50
64	111	64K	80 × 30	8 × 16	640 × 480	DSTN/TFT	25	50
66[b]	110	32K	80 × 30	8 × 16	640 × 480	DSTN/TFT	25	50
71[c]	112	16M	80 × 30	8 × 16	640 × 480	DSTN/TFT	25	50

[a] VCLK is the rate shown when the vertical refresh rate is 60 Hz.

[b] This display mode is 32K direct-color packed-pixel.

[c] This display mode requires a minimum of 2 Mbytes of display memory to support a DSTN flat panel.

4.2.2 Flat Panel-Only and SimulSCAN 800 x 600 (SVGA) Display Modes

For 800 x 600 flat panels, the Cirrus Logic VGA BIOS supports flat panel-only and SimulSCAN operations with the standard VGA display modes listed in Section 4.1 and the extended VGA display modes in Table 4-4. For all display modes, the required CVDD is 3.3 V.

- Within the table, the 'MCLK Minimum' column gives the recommended memory clock frequency at which the CL-GD7556 can run without adverse effects to functionality. Better benchmarks can be achieved with an MCLK frequency higher than the frequency specified.
- DSTN flat panels require display memory for frame accelerator functionality.
- Graphics display mode 6Ah must be used, rather than graphics display mode 58h, for application programs to retain compatibility with other VGA BIOS products.
- On 800 x 600 flat panels, when expansion to 800 x 600 is disabled, display modes with resolutions less than 800 x 600 are displayed at a 640 x 480 resolution.
- For SimulSCAN operation with a CRT monitor and an 800 x 600 flat panel:
  - — Both the CRT monitor and the flat panel must be configured at a minimum to support the resolution of a given display mode during SimulSCAN operation.
  - — For the 800 x 600 flat panels, all resolutions use 800 x 600 timing. As a result, even if an 800 x 600 flat panel displays a 640 x 480 display mode, the SimulSCAN operation is not allowed when using a CRT monitor that is configured to a maximum resolution of 640 x 480.

Table 4-4. Flat Panel-Only and SimulSCAN™ Display Modes for 800 x 600 Flat Panels

Extended VGA Display Mode No. (hex)	VESA Display Mode No. (hex)	Color Depth (number of colors)	Characters × Rows	Character Cell (pixels)	Resolution (pixels)	Expand from 640 × 480 to 800 × 600?	Type of Flat Panel	VCLK[a] (MHz)	MCLK Minimum (MHz)
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	–	DSTN	40	50
							TFT	40	50
5C	103	256/256K	100 × 37	8 × 16	800 × 600	–	DSTN	40	50
							TFT	40	50
5E	100	256/256K	80 × 25	8 × 16	640 × 400	Yes	DSTN	40	50
							TFT	40	50
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Yes	DSTN	40	50
							TFT	40	50
64	111	64K	80 × 30	8 × 16	640 × 480	Yes	DSTN	40	50
							TFT	40	50
65[b]	114	64K	100 × 37	8 × 16	800 × 600	–	DSTN	40	50
							TFT	40	50
66	110	32K[c]	80 × 30	8 × 16	640 × 480	Yes	DSTN	40	50
							TFT	40	50
67[a]	113	32K[b]	100 × 37	8 × 16	800 × 600	–	DSTN	40	50
							TFT	40	50
71[a]	112	16M	80 × 30	8 × 16	640 × 480	Yes	DSTN	40	66
							TFT	40	50
78[d]	115	16M	100 × 37	8 × 16	800 × 600	–	DSTN	40	66
							TFT	40	50

[a] VCLK is the rate shown when the vertical refresh rate is 60 Hz.

[b] This display mode requires a minimum of 2 Mbytes of display memory to support a DSTN flat panel.

[c] This display mode is 32K direct-color packed-pixel.

[d] This display mode requires a minimum of 2 Mbytes of display memory to support all of its display mode capabilities.

4.2.3 Flat Panel-Only and SimulSCAN™ 1024 x 768 (XGA) Display Modes

For 1024 x 768 flat panels, the Cirrus Logic VGA BIOS supports flat panel-only and SimulSCAN operations with the standard VGA display modes listed in Section 4-1 and the extended VGA display modes in Table 4-5. For all display modes, the required CVDD is 3.3 V.

- Within the table, the 'MCLK Minimum' column gives the recommended memory clock frequency at which the CL-GD7556 can run without adverse effects to functionality. Better benchmarks can be achieved with an MCLK frequency higher than the frequency specified.
- Graphics display mode 6Ah must be used, rather than graphics display mode 58h, for application programs to retain compatibility with other VGA BIOS products.
- For SimulSCAN operation with 1024 x 768 panels, both the CRT monitor and the flat panel must be configured at a minimum to support the resolution of a given display mode during SimulSCAN operation.

Table 4-5. Flat Panel-Only and SimulSCAN™ Display Modes for 1024 x 768 Flat Panels

Extended VGA Display Mode Number (hex)	VESA Display Mode Number (hex)	Color Depth (number of colors)	Characters × Rows	Character Cell (pixels)	Resolution (pixels)	Expand from 640 × 480 to 800 × 600?	Type of Flat Panel	VCLK[a] (MHz)	MCLK Minimum (MHz)
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	–	DSTN	65	50
							TFT	65	50
5C	103	256/256K	100 × 37	8 × 16	800 × 600	–	DSTN	65	50
							TFT	65	50
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	–	DSTN	65	50
							TFT	65	50
5E	100	256/256K	80 × 25	8 × 16	640 × 400	Yes	DSTN	65	50
							TFT	65	50
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Yes	DSTN	65	50
							TFT	65	50
60	105	256/256K	128 × 48	8 × 16	1024 × 768	–	DSTN	65	50
							TFT	65	50
64	111	64K	80 × 30	8 × 16	640 × 480	Yes	DSTN	65	80
							TFT	65	50
65	114	64K	100 × 37	8 × 16	800 × 600	–	DSTN	65	80
							TFT	65	50
66	110	32K[b]	80 × 30	8 × 16	640 × 480	Yes	DSTN	65	80
							TFT	65	50
67	113	32K[a]	100 × 37	8 × 16	800 × 600	–	DSTN	65	80
							TFT	65	50
68	116	32K[a]	128 × 48	8 × 16	1024 × 768	–	DSTN	65	80
							TFT	65	50

Table 4-5. Flat Panel-Only and SimulSCAN™ Display Modes for 1024 x 768 Flat Panels *(cont.)*

Extended VGA Display Mode Number (hex)	VESA Display Mode Number (hex)	Color Depth (number of colors)	Characters × Rows	Character Cell (pixels)	Resolution (pixels)	Expand from 640 × 480 to 800 × 600?	Type of Flat Panel	VCLK[a] (MHz)	MCLK Minimum (MHz)
71	112	16M	80 × 30	8 × 16	640 × 480	Yes	TFT	–	N/A
								65	80
74	117	64K	128 × 48	8 × 16	1024 × 768	–	DSTN	65	80
							TFT	65	50
78[c]	115	16M	100 × 37	8 × 16	800 × 600	–	TFT	–	N/A
								65	80
79	118	16M	128 × 48	8 × 16	1024 × 768	–	TFT	–	N/A
								65	80

[a] VCLK is the rate shown when the vertical refresh rate is 60 Hz.

[b] This display mode is 32K direct-color packed-pixel.

[c] A minimum of 2 Mbytes of display memory are required to support all the capabilities of this display mode.

Notes

5. VGA REGISTER PORT MAP

Address	Port	Port Type
3B4	CRT Monitor Controller Index — Monochrome	Read/Write
3B5	CRT Monitor and Flat Panel Controller Data — Monochrome	Read/Write
3BA	Feature Control — Monochrome	Write
	Input Status Register 1 — Monochrome	Read
3C0	Attribute Controller Index / Data (Write)	Write
3C1	Attribute Controller Index / Data (Read)	Read
3C2	Miscellaneous Output Write	Write
	Input Status Register 0	Read
3C4	Sequencer Index	Read/Write
3C5	Sequencer Data	Read/Write
3C6	DAC Pixel Mask (Read/Write), Hidden DAC Register	Read/Write
3C7	Pixel Address Read Mode (Write Only)	Write
	DAC State	Read
3C8	Pixel Address Write Mode	Read/Write
3C9	Pixel Data	Read/Write
3CA	Feature Control Read	Read
3CC	Miscellaneous Output Read	Read
3CE	Graphics Controller Index	Read/Write
3CF	Graphics Controller Data	Read/Write
3D4	CRT Monitor Controller Index — Color	Read/Write
3D5	CRT Monitor and Flat Panel Controller Data — Color	Read/Write
3DA	Feature Control — Color	Write
	Input Status Register 1 — Color	Read
00	PCI Device ID and PCI Vendor ID	Read
04	PCI Status and Command	Read/Write
08	PCI Class Code	Read
10	PCI Display Memory Base Address	Read/Write
14	PCI Relocatable I/O	Read/Write
2C	PCI Subsystem ID for PC97	Read/Write
30	PCI Expansion ROM BIOS Base Address	Read/Write
3C	PCI Interrupt Pin Status and Interrupt Line	Read/Write

Notes

6. REGISTER SUMMARY

This chapter is a summary of the standard VGA registers in Chapter 7 through Chapter 11, as well as the Extension registers in Chapter 12 that have been added by Cirrus Logic.

6.1 Summary of VGA External/General Registers in Chapter 7

The VGA External/General registers in the CL-GD7556 are summarized in the following table.

Abbreviation	Register Name	Index	Port	Page
MISC	Miscellaneous Output	–	3C2 (Write)	7-1
MISC	Miscellaneous Output	–	3CC (Read)	7-1
FC	Feature Control	–	3?A (Write)	7-3
FC	Feature Control	–	3CA (Read)	7-3
FEAT	Input Status Register 0	–	3C2	7-4
STAT	Input Status Register 1	–	3?A	7-5
3C6	Pixel Mask	–	3C6	7-6
3C7	Pixel Address Read Mode	–	3C7 (Write)	7-7
3C7	DAC State	–	3C7 (Read)	7-8
3C8	Pixel Address Write Mode	–	3C8	7-9
3C9	Pixel Data	–	3C9	7-10
PCI00	PCI Device ID / PCI Vendor ID	–	00	7-11
PCI04	PCI Status	–	04	7-12
PCI04	PCI Command	–	04	7-13
PCI08	PCI Class Code High	–	08	7-14
PCI08	PCI Class Code Low (Revision ID)	–	08	7-15
PCI10	PCI Display Memory Base Address	–	10	7-16
PCI14	PCI Relocatable I/O	–	14	7-17
PCI2C	PCI Subsystem ID for PC97	–	2C	7-19
PCI30	PCI Expansion ROM BIOS Base Address	–	30	7-20
PCI3C	PCI Bus Interrupt Status Pin and PCI Bus Interrupt Line	–	3C	7-22

6.2 Summary of VGA Sequencer Registers in Chapter 8

The CL-GD7556 VGA Sequencer registers are summarized in the following table.

NOTE: Some Extension registers are accessed using the Sequencer ports.

Abbreviation	Register Name	Index	Port	Page
SRX	Sequencer Index	–	3C4	8-1
SR0	Sequencer Reset	0	3C5	8-2
SR1	Clocking Mode	1	3C5	8-3
SR2	Bit Map Plane Mask Write Enable	2	3C5	8-5
SR3	Character Map Set Select	3	3C5	8-6
SR4	Display Memory Mode	4	3C5	8-8

6.3 Summary of VGA CRT Controller Registers in Chapter 9

The CL-GD7556 VGA CRT Controller registers are summarized in the following table.

NOTES:

1) Some Extension registers are accessed using the CRT Controller ports.

2) In the register addresses, a '?' is 'B' in Monochrome mode and 'D' in Color mode.

Abbreviation	Register Name	Index	Port	Page
CRX	CRT Controller Index	–	3?4	9-1
CR0	Horizontal Total	0	3?5	9-2
	For Description of All CRT Timing Registers			9-2
CR1	Horizontal Display End	1	3?5	9-5
CR2	Horizontal Blanking Start	2	3?5	9-6
CR3	Horizontal Blanking End	3	3?5	9-7
CR4	Horizontal Sync Start	4	3?5	9-9
CR5	Horizontal Sync End	5	3?5	9-10
CR6	Vertical Total	6	3?5	9-12
CR7	Overflow	7	3?5	9-13
CR8	Screen A Preset Row Scan	8	3?5	9-15
CR9	Character Cell Height	9	3?5	9-16
CRA	Text Cursor Start	A	3?5	9-17
CRB	Text Cursor End	B	3?5	9-18
CRC	Screen A Start Address High	C	3?5	9-19
CRD	Screen A Start Address Low	D	3?5	9-20
CRE	Text Cursor Location High	E	3?5	9-21
CRF	Text Cursor Location Low	F	3?5	9-22
CR10	Vertical Sync Start	10	3?5	9-23
CR11	Vertical Sync End	11	3?5	9-24
CR12	Vertical Display End	12	3?5	9-26
CR13	Scanline Offset	13	3?5	9-27
CR14	Scanline Underline Row	14	3?5	9-28
CR15	Vertical Blanking Start	15	3?5	9-29
CR16	Vertical Blanking End	16	3?5	9-30
CR17	CRT Controller Mode Control	17	3?5	9-31
CR18	Line Compare	18	3?5	9-33
CR22	Graphics Controller Data Latch Readback	22	3?5	9-34
CR24	Attribute Controller Toggle Readback	24	3?5	9-35
CR26	Attribute Controller Index Readback	26	3?5	9-36

6.4 Summary of VGA Graphics Controller Registers in Chapter 10

The CL-GD7556 VGA Graphics Controller registers are summarized in the following table.

NOTE: Some Extension registers are accessed using the Graphics Controller port.

Abbreviation	Register Name	Index	Port	Page
GRX	Graphics Controller Index	–	3CE	10-1
GR0	Display Memory Plane Set / Reset	0	3CF	10-2
GR1	Display Memory Plane Set / Reset Enable	1	3CF	10-3
GR2	Color Compare	2	3CF	10-4
GR3	Data Rotate	3	3CF	10-5
GR4	Display Memory Plane Select	4	3CF	10-6
GR5	Graphics Controller Mode Control	5	3CF	10-7
GR6	Miscellaneous	6	3CF	10-11
GR7	Color Don't-Care Plane	7	3CF	10-12
GR8	Display Memory Bit Mask	8	3CF	10-13

6.5 Summary of VGA Attribute Controller Registers in Chapter 11

The CL-GD7556 VGA Controller registers are summarized in the following table.

Abbreviation	Register Name	Index	Port	Page
ARX	Attribute Controller Index	–	3C0/3C1	11-1
AR0-ARF	Attribute Controller Palette	0-F	3C0/3C1	11-2
AR10	Attribute Controller Mode Control	10	3C0/3C1	11-3
AR11	Overscan (Border) Color	11	3C0/3C1	11-5
AR12	Color Plane Enable	12	3C0/3C1	11-6
AR13	Pixel Panning	13	3C0/3C1	11-8
AR14	Color Select	14	3C0/3C1	11-9

6.6 Summary of Extension Registers in Chapter 12

The CL-GD7556 Extension registers are summarized in the following table.

NOTE: In the register addresses, a '?' is 'B' in Monochrome mode and 'D' in Color mode.

Abbreviation	Register Name	Index	Port	Page
SR6	Unlock All Extension Registers	6	3C5	12-1
SR7	Extended Sequencer Mode	7	3C5	12-2
SR8	DDC2B Control Register	8	3C5	12-5
SR9	Scratch Pad #0	9	3C5	12-6
SRA	Scratch Pad #1	A	3C5	12-6
SRB	VCLK0 Numerator	B	3C5	12-7
SRC	VCLK1 Numerator	C	3C5	12-7
SRD	VCLK2 Numerator	D	3C5	12-7
SRE	VCLK3 Numerator	E	3C5	12-7
SRF	Display Memory Control	F	3C5	12-9
SR10	Hardware Cursor and Icon Coarse Horizontal Position	10	3C5	12-11
SR11	Hardware Cursor and Icon Coarse Vertical Position	11	3C5	12-15
SR12	Hardware Cursor Attributes	12	3C5	12-16
SR13	Hardware Cursor Pattern Address Select	13	3C5	12-18
SR14	Scratch Pad #2	14	3C5	12-19
SR15	Scratch Pad #3	15	3C5	12-19
SR16	Reserved	–	–	–
SR17	BitBLT Memory Map I/O Address Control	17	3C5	12-20
SR18	Signature Generator Control	18	3C5	12-21
SR19	Signature Generator Result Low	19	3C5	12-23
SR1A	Signature Generator Result High	1A	3C5	12-24
SR1B	VCLK0 Denominator and Post-Scalar	1B	3C5	12-25
SR1C	VCLK1 Denominator and Post-Scalar	1C	3C5	12-25
SR1D	VCLK2 Denominator and Post-Scalar	1D	3C5	12-25
SR1E	VCLK3 Denominator and Post-Scalar	1E	3C5	12-25
SR1F	MCLK Frequency and VCLK Source Select	1F	3C5	12-27
SR20	Miscellaneous Control Register 2	20	3C5	12-29
SR21	Test Bus Color Control	21	3C5	12-31
SR22	Hardware Configuration Read Register 1	22	3C5	12-32
SR23	Software Configuration Register 1	23	3C5	12-35
SR24	Flat Panel Type Switches Enable	24	3C5	12-36
SR25	FasText™ Mode Control	25	3C5	12-38
SR26	Shader Signature Low	26	3C5	12-41
SR27	Shader Signature High	27	3C5	12-42
SR28	Scratch Pad # 4	28	3C5	12-43
SR29	Scratch Pad # 5	29	3C5	12-43
SR2A	Hardware Icon #0 Control and Cursor/Icon Select	2A	3C5	12-44
SR2B	Hardware Icon #1 Control and Flat Panel Clock Drive	2B	3C5	12-46
SR2C	Hardware Icon #2 Control and Byte-Swap Enable	2C	3C5	12-48
SR2D	Hardware Icon #3 Control and Icon/Cursor Memory Access	2D	3C5	12-50
SR2E	Hardware Cursor Horizontal Position Extension	2E	3C5	12-52
SR2F	Half-Frame Accel. FIFO Threshold for Surround. Graphics	2F	3C5	12-53
SR30–SR31	Reserved	–	–	–
SR32	HFA FIFO Threshold in VW and DAC IREF Power Control	32	3C5	12-54
SR33	Spare Sequencer Register	33	3C5	12-55
SR34	CPU Stop Control	34	3C5	12-56

6.6 Summary of Extension Registers in Chapter 12 *(cont.)*

Abbreviation	Register Name	Index	Port	Page
Graphics Controller Extension Registers				
GR9	Display Memory Offset 0	9	3CF	12-57
GRA	Display Memory Offset 1	A	3CF	12-59
GRB	Graphics Controller Mode Extensions	B	3CF	12-60
GRC	Color Key Compare Value and Chroma Key Y Minimum	C	3CF	12-62
GRD	Color Key Compare Mask and Chroma Key Y Maximum	D	3CF	12-64
GRE	DPMS Control and VCLK/2 Enable	E	3CF	12-65
GRF	Reserved	–	–	–
GR10	Background Color Expansion #1 Register	10	3CF	12-67
GR11	Foreground Color Expansion #1 Register	11	3CF	12-68
GR12	Reserved	–	–	–
GR13	Foreground Color Expansion #2 Register	13	3CF	12-69
GR14–GR15	Reserved	–	–	–
GR16	Scanline Counter Readback Low	16	3CF	12-70
GR17	Scanline Counter Readback High	17	3CF	12-71
GR18	EDO RAM Control	18	3CF	12-72
GR19	Reserved	–	–	–
GR1A	Scratch Pad #6	1A	3CF	12-74
GR1B	Scratch Pad #7	1B	3CF	12-74
GR1C	Chroma Key U Minimum	1C	3CF	12-75
GR1D	Chroma Key U Maximum	1D	3CF	12-76
GR1E	Chroma Key V Minimum	1E	3CF	12-77
GR1F	Chroma Key V Maximum	IF	3CF	12-78
GR20	BitBLT Width Low	20	3CF	12-79
GR21	BitBLT Width High	21	3CF	12-80
GR22	BitBLT Height Low	22	3CF	12-81
GR23	BitBLT Height High	23	3CF	12-82
GR24	BitBLT Destination Pitch Low	24	3CF	12-83
GR25	BitBLT Destination Pitch High	25	3CF	12-84
GR26	BitBLT Source Pitch Low	26	3CF	12-85
GR27	BitBLT Source Pitch High	27	3CF	12-86
GR28	BitBLT Destination Start Address Low	28	3CF	12-87
GR29	BitBLT Destination Start Address Middle	29	3CF	12-88
GR2A	BitBLT Destination Start Address High	2A	3CF	12-89
GR2B	Reserved	–	–	–
GR2C	BitBLT Source Start Address Low	2C	3CF	12-90
GR2D	BitBLT Source Start Address Middle	2D	3CF	12-91
GR2E	BitBLT Source Start Address High	2E	3CF	12-92
GR2F	BitBLT Destination Write Mask	2F	3CF	12-93
GR30	BitBLT Mode	30	3CF	12-94
GR31	BitBLT Start/Status	31	3CF	12-97
GR32	BitBLT Raster Operation Function	32	3CF	12-99
GR33	BitBLT Mode Extensions	33	3CF	12-101
GR34–GR35	Reserved	–	–	–

6.6 Summary of Extension Registers in Chapter 12 *(cont.)*

Abbreviation	Register Name	Index	Port	Page
CRT Controller Extension Registers				
CR19	Interlace End	19	3?5	12-102
CR1A	Miscellaneous Control	1A	3?5	12-103
CR1B	Extended Display Control	1B	3?5	12-104
CR1C	Horizontal Total and Horizontal Sync Start Adjust	1C	3?5	12-106
CR1D	Color Key Compare Type	1D	3?5	12-107
CR1E–CR21	Reserved	–	–	–
CR22	Graphics Controller Data Latch Readback	22	3?5	12-109
CR23	Reserved	–	–	–
CR24	Attribute Controller Index/Data Status Readback	24	3?5	12-110
CR25	Manufacturing Revision Identification	25	3?5	12-111
CR26	Attribute Controller Index Readback	26	3?5	12-112
CR27	Device Identification	27	3?5	12-113
CR28–CR29	Reserved	–	–	–
CR30	TV-Out Control	30	3?5	12-114
Video Window Control Registers				
NOTE: In the register addresses, a '?' is 'B' in Monochrome mode and 'D' in Color mode.				
CR31	VW Horizontal Upscaling Coefficient	31	3?5	12-116
CR32	VW Vertical Upscaling Coefficient	32	3?5	12-117
CR33	VW Horizontal Start High	33	3?5	12-118
CR34	VW Horizontal Start Low	34	3?5	12-119
CR35	VW Brightness Control	35	3?5	12-120
CR36	VW Vertical Position Extension	36	3?5	12-121
CR37	VW Vertical Start	37	3?5	12-123
CR38	VW Vertical Height	38	3?5	12-124
CR39	VW Upscaling Coefficients Low	39	3?5	12-125
CR3A	VW Memory Start Address High	3A	3?5	12-126
CR3B	VW Memory Address Offset	3B	3?5	12-127
CR3C	VW Data Format	3C	3?5	12-128
CR3D	VW Horizontal Pixel Width	3D	3?5	12-129
CR3E	VW Memory Start Address Middle	3E	3?5	12-130
CR3F	VW Interpolation and Memory Start Address Low	3F	3?5	12-131
CR40	VW Vertical Interpolation and Edge-Sharpening Control	40	3?5	12-133
CR41	VW Right-Side Memory Cycle Control	41	3?5	12-136
CR42	VW FIFO Threshold and Chroma Key Mode Select	42	3?5	12-137
CR43–CR4F	Reserved	–	–	–

V-Port Control Registers

Flat Panel Control Registers

NOTE: In the register addresses, a '?' is 'B' in Monochrome mode and 'D' in Color mode.

CRT Monitor Horizontal Control Registers when Flat Panel Enabled

NOTE: In the register addresses, a '?' is 'B' in Monochrome mode and 'D' in Color mode.

Flat Panel and CRT Monitor Miscellaneous Control Registers

NOTE: In the register addresses, a '?' is 'B' in Monochrome mode and 'D' in Color mode.

7. EXTERNAL/GENERAL REGISTERS

The registers in this chapter apply to CRT monitors.

NOTE: Within this chapter, some registers have a '?' in the I/O port address. This question mark implies a 'B' for Monochrome mode and 'D' for Color mode, depending on the setting of External/General register bit MISC[0].

7.1 MISC: Miscellaneous Output Register

I/O Port Address: 3C2 (Write) 3CC (Read)

Index: (n/a)

Bit	Description	Reset State
7	VSYNC Polarity	0
6	HSYNC Polarity	0
5	Page Select	0
4	Reserved	
3	VCLK Frequency Select [1]	0
2	VCLK Frequency Select [0]	0
1	Display Memory Access Enable	0
0	CRT Controller I/O Address	0

This standard VGA register has an assortment of bits that have nothing in common.

Bit **Description**

7 **VSYNC Polarity:**
- When this bit is programmed to:
  - — 0, VSYNC (pin 114) is active-low. A high indicates beginning sync time.
  - — 1, VSYNC is active-high. A low indicates beginning sync time.
- For information on static sync signals, refer to Extension register GRE [2:1].

6 **HSYNC Polarity:**
- When this bit is programmed to:
  - — 0, HSYNC (pin 112) is active-low. A high indicates beginning sync time.
  - — 1, HSYNC is active-high. A low indicates beginning sync time.
- For some CRT monitors, the combined polarity of VSYNC and HSYNC is used to indicate the number of scanlines per frame, as shown in the table.

MISC		Vertical Size: Scanlines appearing on screen	Vertical Overscan: Scanlines appearing off screen	Vertical Total = (Vertical Size + Vertical Overscan)
[7] VSYNC Polarity	[6] HSYNC Polarity			
0 (+)	0 (+)	Reserved	Reserved	Reserved
0 (+)	1 (–)	400	14	414
1 (–)	0 (+)	350	12	362
1 (–)	1 (–)	480	16	496

7.1 MISC: Miscellaneous Output Register *(cont.)*

Bit | **Description**

5 — **Page Select:**
- When Sequencer register SR4[2] is 1 *and* this bit MISC[5] is:
  - — 0, only odd-page display memory locations are selected.
  - — 1, only even-page display memory locations are selected.
- This bit takes effect for graphics display modes 6h, Dh, Eh, 11h, and 12h.
- This bit is ignored when either of the following are true:
  - — Graphics Controller register GR6[1] is 1.
  - — Sequencer register SR4[3] is 1.

4 — **Reserved**

3:2 — **VCLK Frequency Select [1:0]:**
This 2-bit field is used to select from among the four VCLK frequencies that are available, as shown in the following table:

MISC		VCLK	Corresponding Default Frequency
[3]	[2]		
0	0	VCLK0	25.180 MHz
0	1	VCLK1	28.325 MHz
1	0	VCLK2	41.165 MHz
1	1	VCLK3	36.082 MHz

1 — **Display Memory Access Enable:**
- When the host CPU is attempting to access display memory and this bit is:
  - — 0, the CL-GD7556 does not respond to the host CPU attempts.
  - — 1, the CL-GD7556 responds normally to the host CPU attempts.
- Extension register bit GRE[4] overrides this bit. When GRE[4] is 1, the host CPU cannot access display memory.

0 — **CRT Controller I/O Address:**
This bit selects CRT Controller I/O addresses. When this bit is:
- 0, it selects I/O addresses for monochrome display device controllers (3Bx).
- 1, it selects I/O addresses for color display device controllers (3Dx).

MISC[0]	Mode	Input Status / Feature Control	CRT Controller Index	CRT Controller Data
0	Monochrome	3BA (Input Status)	3B4	3B5
1	Color	3DA (Feature Control)	3D4	3D5

7.2 FC: Feature Control Register

I/O Port Address: 3?A (Write) 3CA (Read)

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	CRT Monitor VSYNC Control	0
2	Reserved	
1	Reserved	
0	Reserved	

This register is one of the original IBM PC registers. Bit[3] is the only one still used.

Bit	Description
7:4	**Reserved**
3	**CRT Monitor VSYNC Control:** This bit is normally used for CRT monitors that have an internal vertical display enable signal pin. Program this bit to: • 0 to keep the CRT monitor VSYNC signal unchanged in order to maintain IBM compatibility. • 1 to logically OR the CRT monitor VSYNC signal with the CL-GD7556 internal vertical display enable signal prior to sending it to the VSYNC pin.
2:0	**Reserved**

7.3 FEAT: Input Status Register 0

I/O Port Address: 3C2

Index: –

Bit	Description	Access	Reset State
7	Vertical Retrace Interrupt Request Status	R	0
6	Reserved		
5	Reserved		
4	DAC Switch Sensing Status	R	0
3	Reserved		
2	Reserved		
1	Reserved		
0	Reserved		

The bits in this read-only register are nearly all undefined.

Bit	Description
7	**Vertical Retrace Interrupt Request Status:** • When this read-only bit is: — 0, there is no vertical retrace interrupt request pending. — 1, there is a vertical retrace interrupt request pending. • For more information on the CL-GD7556 vertical interrupt system, refer to CRT Controller register CR11.
6:5	**Reserved**
4	**DAC Switch Sensing Status:** This read-only bit is used by the Cirrus Logic VGA BIOS to report the on-off status of one of four analog comparator RAMDAC sense switches, as selected by External/General register MISC[3:2]. This bit is: • 0 when the selected DAC sense switch is off. • 1 when the selected DAC sense switch is on.
3:0	**Reserved**

7.4 STAT: Input Status Register 1

I/O Port Address: 3?A

Index: –

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	Diagnostic Status [1]	R	0
4	Diagnostic Status [0]	R	0
3	Vertical Retrace Status	R	0
2	Reserved		
1	Reserved		
0	Display Data Enable Status	R	0

This read-only register contains some status bits.

Bit — **Description**

7:6 — **Reserved**

5:4 — **Diagnostic Status [1:0]:**
As a standard VGA feature, these read-only bits reflect the status of 2 bits selected from the 8 output bits of Attribute Controller register bits AR12[5:4]. The following table indicates how the 2 bits are selected. (The Pixel bus is a bus that is internal to the CL-GD7556.)

Attribute Controller Register AR12		STAT	
[5]	**[4]**	**[5]**	**[4]**
0	0	Pixel Bus Bit [2] (Red)	Pixel Bus Bit [0] (Blue)
0	1	Pixel Bus Bit [5] (Secondary Blue)	Pixel Bus Bit [4] (Green)
1	0	Pixel Bus Bit [3] (Secondary Red)	Pixel Bus Bit [1] (Secondary Green)
1	1	Pixel Bus Bit [7]	Pixel Bus Bit [6]

3 — **Vertical Retrace Status**:
This bit gives the status of vertical retrace for a display device. When this bit is:
- 0, the display device is in a display mode.
- 1, the display device is in the vertical retrace mode (that is, a vertical retrace is in progress).

2:1 — **Reserved**

0 — **Display Data Enable Status:**
This bit gives the status of the display device. When this bit is:
- 0, data are being enabled and displayed on the display screen.
- 1, either vertical or horizontal blanking is active for the display screen.

7.5 3C6: Pixel Mask Register

I/O Port Address: 3C6

Index: –

Bit	Description	Reset State
7	Pixel Mask [7]	0
6	Pixel Mask [6]	0
5	Pixel Mask [5]	0
4	Pixel Mask [4]	0
3	Pixel Mask [3]	0
2	Pixel Mask [2]	0
1	Pixel Mask [1]	0
0	Pixel Mask [0]	0

The bits in this register form the pixel mask for the palette DAC. Typically, the Cirrus Logic VGA BIOS programs all these bits to 1. This same 3C6 address is used to access Extension register HDR (the Hidden DAC register).

Bit	Description
7:0	**Pixel Mask [7:0]:** These read-only bits form pixel mask for the palette DAC. When a bit in this register is cleared to 0, the corresponding bit in the pixel data is ignored in looking up an entry in the CLUT (color look-up table).

7.6 3C7: Pixel Address Read Mode Register (Write Only)

I/O Port Address: 3C7

Index: –

Bit	Description	Access	Reset State
7	Pixel Address Read Mode [7]	W	0
6	Pixel Address Read Mode [6]	W	0
5	Pixel Address Read Mode [5]	W	0
4	Pixel Address Read Mode [4]	W	0
3	Pixel Address Read Mode [3]	W	0
2	Pixel Address Read Mode [2]	W	0
1	Pixel Address Read Mode [1]	W	0
0	Pixel Address Read Mode [0]	W	0

The bits in this write-only register form the pixel address read mode for the palette DAC. This pixel address is then used to specify the CLUT entry that is to be read.

Bit	Description
7:0	**Pixel Address Read Mode [7:0]:** This write-only field is the pixel address read mode for the CLUT. At the conclusion of every third read of External/General register 3C9 (the Pixel Data register), this address is automatically incremented by one.

7.7 3C7: DAC State Register (Read Only)

I/O Port Address: 3C7

Index: –

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	DAC State [1]	R	0
0	DAC State [0]	R	0

The bits in this read-only register indicate whether a read or a write to the CLUT occurred last.

Bit	Description
7:2	**Reserved**
1:0	**DAC State [1:0]:** This 2-bit read-only field indicates which pixel address register was accessed last. • Both bits in this field are always the same digit. • When the bits are: — '00', a write operation is in progress, meaning that the last accessed register for the CLUT was External/General register 3C8 (the Pixel Address Write Mode register). — '11', a read operation is in progress, meaning that the last accessed register for the CLUT was External/General register 3C7 (the Pixel Address Read Mode register).

7.8 3C8: Pixel Address Write Mode Register

I/O Port Address: 3C8

Index: –

Bit	Description	Access	Reset State
7	Pixel Address Write Mode [7]	R/W	0
6	Pixel Address Write Mode [6]	R/W	0
5	Pixel Address Write Mode [5]	R/W	0
4	Pixel Address Write Mode [4]	R/W	0
3	Pixel Address Write Mode [3]	R/W	0
2	Pixel Address Write Mode [2]	R/W	0
1	Pixel Address Write Mode [1]	R/W	0
0	Pixel Address Write Mode [0]	R/W	0

The bits in this register form the pixel address write mode for the palette DAC. This pixel address is then used to specify the CLUT entry that is to be written.

Bit	Description
7:0	**Pixel Address Write Mode [7:0]:** This field is the pixel address write mode for an entry in the CLUT. At the conclusion of every third write to External/General register 3C9 (the Pixel Data register), this address is automatically incremented by one.

7.9 3C9: Pixel Data Register

I/O Port Address: 3C9

Index: –

Bit	Description	Access	Reset State
7	Pixel Data [7]	R/W	0
6	Pixel Data [6]	R/W	0
5	Pixel Data [5]	R/W	0
4	Pixel Data [4]	R/W	0
3	Pixel Data [3]	R/W	0
2	Pixel Data [2]	R/W	0
1	Pixel Data [1]	R/W	0
0	Pixel Data [0]	R/W	0

This register contains the pixel data for the palette DAC.

Bit	Description
7:0	**Pixel Data [7:0]**: These read/write register bits store the pixel data for the palette DAC. Writing to this register occurs as follows: 1. Prior to writing to this register, External/General register 3C8 (the Pixel Address Write Mode register) is written with the first (or only) pixel address. 2. Three values, corresponding to the red, green, and blue values for the pixel, are then written to this address. 3. Following the third write, values are transferred to the CLUT. 4. The Pixel Address is incremented, in case new values for the next pixel address are to be written. Reading from this register occurs as follows: 1. Prior to reading from this register, External/General register 3C7 (the Pixel Address Read Mode register) is written with the first (or only) pixel address. 2. Three values, corresponding to the red, green, and blue values for the pixel, are then read from this address. 3. Following the third read, the Pixel Address is incremented, in case new values for the next pixel address are to be read.

7.10 PCI00: PCI Device ID / PCI Vendor ID Register

PCI Configuration Address: 00

Index: –

Bit	Description	Access	Reset State
31	PCI Device ID [15]	R	0
30	PCI Device ID [14]	R	0
29	PCI Device ID [13]	R	0
28	PCI Device ID [12]	R	0
27	PCI Device ID [11]	R	0
26	PCI Device ID [10]	R	0
25	PCI Device ID [9]	R	0
24	PCI Device ID [8]	R	0
23	PCI Device ID [7]	R	0
22	PCI Device ID [6]	R	1
21	PCI Device ID [5]	R	0
20	PCI Device ID [4]	R	0
19	PCI Device ID [3]	R	1
18	PCI Device ID [2]	R	1
17	PCI Device ID [1]	R	0
16	PCI Device ID [0]	R	0
15	PCI Vendor ID [15]	R	0
14	PCI Vendor ID [14]	R	0
13	PCI Vendor ID [13]	R	0
12	PCI Vendor ID [12]	R	1
11	PCI Vendor ID [11]	R	0
10	PCI Vendor ID [10]	R	0
9	PCI Vendor ID [9]	R	0
8	PCI Vendor ID [8]	R	0
7	PCI Vendor ID [7]	R	0
6	PCI Vendor ID [6]	R	0
5	PCI Vendor ID [5]	R	0
4	PCI Vendor ID [4]	R	1
3	PCI Vendor ID [3]	R	0
2	PCI Vendor ID [2]	R	0
1	PCI Vendor ID [1]	R	1
0	PCI Vendor ID [0]	R	1

This 32-bit register contains the PCI Device and Vendor ID (identification) for PCI compliance.

Bit	Description
31:16	**PCI Device ID [15:0]:** This read-only field returns the PCI device ID assigned by Cirrus Logic. The CL-GD7556 PCI device ID is 004Ch.
15:0	**PCI Vendor ID [15:0]:** This read-only field returns the PCI vendor ID assigned to Cirrus Logic by the PCI Special Interest Group, which is 1013h.

7.11 PCI04: PCI Status Register

PCI Configuration Address: 04

Index: –

Bit	Description	Access	Reset State
31	Reserved		
30	Reserved		
29	Reserved		
28	Reserved		
27	Target Abort	R/W	0
26	DEVSEL# Timing [1]	R	0
25	DEVSEL# Timing [0]	R	1
24	Reserved		
23	Reserved		
22	Reserved		
21	Reserved		
20	Reserved		
19	Reserved		
18	Reserved		
17	Reserved		
16	Reserved		

This 16-bit register contains the most-significant 2 bytes of the 4-byte PCI Status / Command register. See next page for the PCI04[15:0] bit description.

Bit	Description
31:28	**Reserved**
27	**Target Abort:** This read-write bit is used if there is an I/O cycle in which byte enables are illegal. In this case, the CL-GD7556 signals to abort the target (that is, the target is allowed to terminate the transaction) and the CL-GD7556 sets this bit. The PCI bridge (that is, the combination of the PCI host CPU chip and the core-logic chipset) must then reset this bit.
26:25	**DEVSEL# Timing [1:0]:** • These are bits [26:25] of the 32-bit PCI Status / Command register. • This 2-bit read-only field always returns the value ‘01’ to indicate medium timing for DEVSEL# (pin 47).
24:16	**Reserved**

7.12 PCI04: PCI Command Register

PCI Configuration Address: 04

Index: –

Bit	Description	Access	Reset State
15	Reserved	R/W	0
14	Reserved	R/W	0
13	Reserved	R/W	0
12	Reserved	R/W	0
11	Reserved	R/W	0
10	Reserved	R/W	0
9	Reserved	R/W	0
8	Reserved	R/W	0
7	Reserved	R/W	0
6	Reserved	R/W	0
5	PCI Bus DAC Shadowing Enable	R/W	0
4	Reserved	R/W	0
3	Reserved	R/W	0
2	Reserved	R/W	0
1	Display Memory Access Enable	R/W	0
0	I/O Access Enable	R/W	0

This 16-bit register contains the least-significant 2 bytes of the 4-byte PCI Status / Command register.

Bit	Description
15:6	**Reserved:** These bits are reserved and *must* be programmed to 0.
5	**PCI Bus DAC Shadowing Enable:** When this bit is set to 1: • PCI bus DAC shadowing is enabled. • Read accesses are executed normally. • Write accesses to the CL-GD7556 are executed, in that data bits are latched into the appropriate palette register. However, the CL-GD7556 does not acknowledge the access.
4:2	**Reserved:** These bits are reserved and *must* be programmed to 0.
1	**Display Memory Access Enable:** Display memory access is controlled with this bit. When this bit is: • 0, display memory accesses are *not* enabled on the CL-GD7556 • 1, display memory accesses are enabled on the CL-GD7556.
0	**I/O Access Enable:** • When this bit is: — 0, I/O accesses are not enabled to the CL-GD7556. — 1, I/O accesses are enabled to the CL-GD7556. • Regardless of the state of this bit, I/O accesses to all PCI configuration registers are always enabled.

7.13 PCI08: PCI Class Code High Register

PCI Configuration Address: 08

Index: –

Bit	Description	Access	Reset State
31	PCI Class Code [23]	R	0
30	PCI Class Code [22]	R	0
29	PCI Class Code [21]	R	0
28	PCI Class Code [20]	R	0
27	PCI Class Code [19]	R	0
26	PCI Class Code [18]	R	0
25	PCI Class Code [17]	R	1
24	PCI Class Code [16]	R	1
23	PCI Class Code [15]	R	0
22	PCI Class Code [14]	R	0
21	PCI Class Code [13]	R	0
20	PCI Class Code [12]	R	0
19	PCI Class Code [11]	R	0
18	PCI Class Code [10]	R	0
17	PCI Class Code [9]	R	0
16	PCI Class Code [8]	R	0
15	PCI Class Code [7]	R	0
14	PCI Class Code [6]	R	0
13	PCI Class Code [5]	R	0
12	PCI Class Code [4]	R	0
11	PCI Class Code [3]	R	0
10	PCI Class Code [2]	R	0
9	PCI Class Code [1]	R	0
8	PCI Class Code [0]	R	0

This 24-bit read-only PCI Class Code field is assigned to a VGA-compatible controller. This class code is required for PCI Bus 2.0 compliance.

Bit **Description**

31:8 **PCI Class Code [23:0]:**

- Bits [31:8], the most-significant bits of the 4-byte PCI Class Code, are in this register.
  - — Bits [31:24] contain the Base Class Code, which is 03h.
  - — Bits [23:16] contain the Sub Class Code, which is 00h.
  - — Bits [15:8] contain the Programming Interface Code, which is 00h.
- Bits [7:0], the least-significant bits on the following page, contain the revision ID.

Register Format for PCI Class Code and Revision ID

Base Class Code		Sub Class Code		Programming Interface		Revision ID	
PCI08[31:24]		PCI08[23:16]		PCI08[15:8]		PCI08[7:0]	
23	16	15	8	7	0	7	0

7.14 PCI08: PCI Class Code Low (Revision ID) Register

PCI Configuration Address: 08

Index: –

Bit	Description	Access	Reset Value
7	PCI Class Code (Revision ID) [7]	R	X
6	PCI Class Code (Revision ID) [6]	R	X
5	PCI Class Code (Revision ID) [5]	R	X
4	PCI Class Code (Revision ID) [4]	R	X
3	PCI Class Code (Revision ID) [3]	R	X
2	PCI Class Code (Revision ID) [2]	R	X
1	PCI Class Code (Revision ID) [1]	R	X
0	PCI Class Code (Revision ID) [0]	R	X

This 8-bit register consists of the least-significant byte of the 4-byte PCI Class Code register. This register contains the revision ID assigned by Cirrus Logic.

Bit	Description
7:0	**PCI Class Code (Revision ID) [7:0]:** This read-only field contains a revision ID assigned by Cirrus Logic. This register is reserved for the exclusive use of the CL-GD7556 VGA BIOS and must never be written by any application program. It is listed here only for chip identification.

7.15 PCI10: PCI Display Memory Base Address Register

PCI Configuration Address: 10

Index: –

Bit	Description	Access	Reset Value
31	PCI Display Memory Base Address [31]	R/W	0
30	PCI Display Memory Base Address [30]	R/W	0
29	PCI Display Memory Base Address [29]	R/W	0
28	PCI Display Memory Base Address [28]	R/W	0
27	PCI Display Memory Base Address [27]	R/W	0
26	PCI Display Memory Base Address [26]	R/W	0
25	PCI Display Memory Base Address [25]	R/W	0
24	PCI Display Memory Base Address [24]	R/W	0
23:1	Reserved		
0	Display Memory or I/O Indicator	R/W	0

This 32-bit register contains the PCI bus base address for display memory.

Bit	Description
31:24	**PCI Display Memory Base Address [31:24]:** This 8-bit field contains the base address of the contiguous 16-Mbyte memory block reserved for the CL-GD7556 display memory. • The display memory occupies the first 4 Mbytes of this block. • All 16 Mbytes are addressable, as four 4-Mbyte byte-swapping apertures.
23:1	**Reserved**
0	**Display Memory or I/O Indicator:** This read-write bit is used to indicate the type of address space requested, either display memory or I/O. When this bit is: • 0, a display memory address space is requested. • 1, an I/O address space is requested.

7.16 PCI14: PCI Relocatable I/O Register

PCI Configuration Address: 14

Index: –

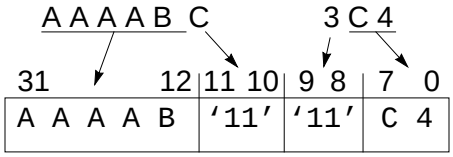
Bit	Description	Reset State
31	Memory-Mapped I/O Address Offset [31]	0
30	Memory-Mapped I/O Address Offset [30]	0
29	Memory-Mapped I/O Address Offset [29]	0
28	Memory-Mapped I/O Address Offset [28]	0
27	Memory-Mapped I/O Address Offset [27]	0
26	Memory-Mapped I/O Address Offset [26]	0
25	Memory-Mapped I/O Address Offset [25]	0
24	Memory-Mapped I/O Address Offset [24]	0
23	Memory-Mapped I/O Address Offset [23]	0
22	Memory-Mapped I/O Address Offset [22]	0
21	Memory-Mapped I/O Address Offset [21]	0
20	Memory-Mapped I/O Address Offset [20]	0
19	Memory-Mapped I/O Address Offset [19]	0
18	Memory-Mapped I/O Address Offset [18]	0
17	Memory-Mapped I/O Address Offset [17]	0
16	Memory-Mapped I/O Address Offset [16]	0
15	Memory-Mapped I/O Address Offset [15] / Relocatable I/O Base Address [15]	0
14	Memory-Mapped I/O Address Offset [14] / Relocatable I/O Base Address [14]	0
13	Memory-Mapped I/O Address Offset [13] / Relocatable I/O Base Address [13]	0
12	Memory-Mapped I/O Address Offset [12] / Relocatable I/O Base Address [12]	0
11	Memory-Mapped I/O Address Offset [11] / Relocatable I/O Base Address [11]	0
10	Memory-Mapped I/O Address Offset [10] / Relocatable I/O Base Address [10]	0
9:1	Reserved	
0	Relocatable I/O Enable= MD40	

This register contains the PCI bus relocatable I/O base address and a bit for enabling the PCI bus relocatable I/O. In addition, it contains bits for a memory-mapped I/O address offset.

Bit	Description
31:10	**Memory-Mapped I/O Address Offset [31:10]:** These bits work in combination with MD34 / MMIOPU (pin 217) and Extension register bit SR22[7]. When MD34 / MMIOPU: • Is not connected to an external pull-up resistor, SR22[7] is 0, and the VGA I/O address space operates normally. • Is connected to an external pull-up resistor, SR22[7] is 1, and these bits are read/write bits that are used for Memory-Mapped I/O support. *(Continued)*

7.16 PCI14: PCI Relocatable I/O Register *(cont.)*

Bit	Description
31:10 *(cont.)*	**Memory-Mapped I/O Address Offset [31:10]:** For example, to use the 22-bit offset in PCI14[31:10] to access I/O port 3C4: — Bits PCI14[31:10] act as a memory pointer to an address, such as AAAABC. — Bits PCI14[31:12] = AAAAB. — Bits PCI14[11:10] = the first two bits of 'C'. (The last two bits are masked out and discarded.) — The address AAAABC is concatenated with bits [9:0] of the I/O port 3C4 address. — The 2 most-significant bits of the I/O port 3C4 address are masked out and discarded. — In this example, the result of adding bits PCI14[11:10] and bits [9:8] of the I/O port address is Fh. — The address that results from the concatenation is AAAAB F C4.
15:10	**Relocatable I/O Base Address [15:10]:** When PCI14[0] is: • 0, relocatable I/O is disabled. • 1 *and* Extension register SR22[7] = 0, these bits act as a 6-bit field that contains the base address for the relocatable 512-byte I/O address range. These bits correspond to the address bits AD[15:10]. This offset, combined with the linear address offset, provides hardware hooks for multiple display device controllers in a single PCI system.
9:1	**Reserved**
0	**Relocatable I/O Enable:** This read-only bit works in combination with MD40 / RIOPU (pin 211) and Extension register SR22[7]. When an external pull-up resistor: • Is not connected to MD40 / RIOPU, this bit reads back a 0, and Relocatable I/O is disabled. • Is connected to MD40 / RIOPU, this bit reads back a 1. In this case, when Extension register SR22[7] is 0, Relocatable I/O is enabled.



For this example:
The last two bits of the offset (that is, 'C') are discarded.
The first two bits of the port address (that is, '3') are discarded.
The resulting hex for [11:8] is 'F'.

The resulting memory address is: AAAAB F C4

7.17 PCI2C: PCI Subsystem ID and Subsystem Vendor ID for PC97

PCI Configuration Address: 2C

Index: –

Bit	Description	Access	Reset State
31	Subsystem ID [15]	R/W	0
30	Subsystem ID [14]	R/W	0
29	Subsystem ID [13]	R/W	0
28	Subsystem ID [12]	R/W	0
27	Subsystem ID [11]	R/W	0
26	Subsystem ID [10]	R/W	0
25	Subsystem ID [9]	R/W	0
24	Subsystem ID [8]	R/W	0
23	Subsystem ID [7]	R/W	0
22	Subsystem ID [6]	R/W	0
21	Subsystem ID [5]	R/W	0
20	Subsystem ID [4]	R/W	0
19	Subsystem ID [3]	R/W	0
18	Subsystem ID [2]	R/W	0
17	Subsystem ID [1]	R/W	0
16	Subsystem ID [0]	R/W	0
15	Subsystem Vendor ID [15]	R/W	0
14	Subsystem Vendor ID [14]	R/W	0
13	Subsystem Vendor ID [13]	R/W	0
12	Subsystem Vendor ID [12]	R/W	0
11	Subsystem Vendor ID [11]	R/W	0
10	Subsystem Vendor ID [10]	R/W	0
9	Subsystem Vendor ID [9]	R/W	0
8	Subsystem Vendor ID [8]	R/W	0
7	Subsystem Vendor ID [7]	R/W	0
6	Subsystem Vendor ID [6]	R/W	0
5	Subsystem Vendor ID [5]	R/W	0
4	Subsystem Vendor ID [4]	R/W	0
3	Subsystem Vendor ID [3]	R/W	0
2	Subsystem Vendor ID [2]	R/W	0
1	Subsystem Vendor ID [1]	R/W	0
0	Subsystem Vendor ID [0]	R/W	0

Bit	Description
31:16	**Subsystem ID [31:16]:** These 16 bits contains the 2 byte PCI Subsystem ID code provided by the Original Equipment Manufacturer. This register can be written, when Extension register SR17[3] is 1.
15:0	**Subsystem Vendor ID [15:0]:** These 16 bits contains the 2 byte PCI Subsystem Vendor ID code provided by the Original Equipment Manufacturer. This register can be written, when Extension register SR17[3] is 1.

7.18 PCI30: PCI Expansion ROM BIOS Base Address Register

PCI Configuration Address: 30

Index: –

Bit	Description	Access	Reset State
31	Expansion ROM BIOS Base Address [31]	R/W	0
30	Expansion ROM BIOS Base Address [30]	R/W	0
29	Expansion ROM BIOS Base Address [29]	R/W	0
28	Expansion ROM BIOS Base Address [28]	R/W	0
27	Expansion ROM BIOS Base Address [27]	R/W	0
26	Expansion ROM BIOS Base Address [26]	R/W	0
25	Expansion ROM BIOS Base Address [25]	R/W	0
24	Expansion ROM BIOS Base Address [24]	R/W	0
23	Expansion ROM BIOS Base Address [23]	R/W	0
22	Expansion ROM BIOS Base Address [22]	R/W	0
21	Expansion ROM BIOS Base Address [21]	R/W	0
20	Expansion ROM BIOS Base Address [20]	R/W	0
19	Expansion ROM BIOS Base Address [19]	R/W	0/1
18	Expansion ROM BIOS Base Address [18]	R/W	0/1
17	Expansion ROM BIOS Base Address [17]	R/W	0
16	Expansion ROM BIOS Base Address [16]	R/W	0
15	32-Kbyte EPROM BIOS VGA Memory Allocation	R/W	0
14:1	Reserved		
0	EPROM BIOS Enable	R/W	0

This 32-bit register contains the 16-bit base address of ROM BIOS memory.

Bit	Description
31:16	**Expansion ROM BIOS Base Address [31:16]:** This field, which is programmed by the PCI system BIOS, contains the base address of the contiguous 64-Kbyte memory block reserved for the CL-GD7556 during POST (power-on self-test). During POST, the following sequence occurs only once: • The PCI system BIOS shadows the VGA BIOS through the programmed address range. • The PCI system BIOS copies the run-time portion of the VGA BIOS to C000:0h. After POST: • All VGA BIOS calls are routed to the system memory.
19:18	**Expansion ROM BIOS Base Address [19:18]:** When MD31 / BIOSPU (pin 234) is connected to an external pull-up resistor, then bits 19:18 are set to ‘11’ at reset.

7.18 PCI30: PCI Expansion ROM BIOS Base Address Register *(cont.)*

Bit	Description
15	**32-Kbyte EPROM BIOS VGA Memory Allocation:** This bit works in combination with Extension register SR22[3] to control the amount of memory allocated to the EPROM BIOS (that is, the VGA BIOS). When MD30 / ROM32KPU (pin 235): • Is not connected to an external pull-up resistor, then SR22[3] is 0. In this case: — This bit is read-only. — This bit is cleared to 0 during system reset, and it is always 0 (that is, reserved). — This bit allocates 64 Kbytes of VGA memory for the VGA BIOS, which is the default setting. • Is connected to an external pull-up resistor, then SR22[3] is 1. In this case: — This bit is read-write. — This bit allocates 32 Kbytes of VGA memory for the VGA BIOS, using bits PCI30[31:15]. **IMPORTANT:** When the Cirrus Logic VGA BIOS is used, this bit must be always be 0, since the CL-GD7556 Cirrus Logic VGA BIOS requires a minimum of 48 Kbytes.
14:1	**Reserved**
0	**EPROM BIOS Enable:** This bit works in combination with Extension register SR22[4] to control the EPROM BIOS (that is, the VGA BIOS). When MD31 / BIOSPU (pin 234): • Is not connected to an external pull-up resistor, SR22[4] is 0 and: — This bit is read-only. — This bit is cleared to 0 during system reset, and it is always 0. — The VGA BIOS at C0000:CFFFFh is disabled. • Is connected to an external pull-up resistor, SR22[4] is 1 and: — This bit is read/write. — This bit is reset to 0 at system reset. — When this bit is written to a 1 by POST, the VGA BIOS at C0000:CFFFFh is enabled, *and*: — Display memory access is disabled (that is, CAS# / WE# is forced high). — The MD pins are AD, for ROMA (that is, the EPROM Address) and for ROMD (that is, the EPROM Data).

7.19 PCI3C: PCI Bus Interrupt Status Pin and PCI Bus Interrupt Line Register

PCI Configuration Address: 3C

Index: –

Bit	Description	Access	Reset State
15	PCI Bus Interrupt Status Pin [7]	R	0
14	PCI Bus Interrupt Status Pin [6]	R	0
13	PCI Bus Interrupt Status Pin [5]	R	0
12	PCI Bus Interrupt Status Pin [4]	R	0
11	PCI Bus Interrupt Status Pin [3]	R	0
10	PCI Bus Interrupt Status Pin [2]	R	0
9	PCI Bus Interrupt Status Pin [1]	R	0
8	PCI Bus Interrupt Status Pin [0]	R	= #MD28
7	PCI Bus Interrupt Line [7]	R/W	0
6	PCI Bus Interrupt Line [6]	R/W	0
5	PCI Bus Interrupt Line [5]	R/W	0
4	PCI Bus Interrupt Line [4]	R/W	0
3	PCI Bus Interrupt Line [3]	R/W	0
2	PCI Bus Interrupt Line [2]	R/W	0
1	PCI Bus Interrupt Line [1]	R/W	0
0	PCI Bus Interrupt Line [0]	R/W	0

This 16-bit register contains data from the PCI bus interrupt status pin and PCI bus interrupt line.

Bit	Description
15:8	**PCI Bus Interrupt Status Pin [7:0]:** When CL-GD7556 pin 237 (MD28 / INTPU): • Does not have a pull-up resistor connected to it, this read-only field returns the value 01h. • Is *connected* to a pull-up resistor during system reset, Extension register bit SR22[1] is set to 1, and bit PCI3C[8] is cleared to 0. When PCI3C[8] is 0, the Interrupt Request function of the INTR# pin 43 (N1) is disabled. In this case, the INTR# pin must not be connected. In other words: if there is a pull-up resistor on pin 237 (C7), the INTR# pin 43 (N1) must not be connected.
7:0	**PCI Bus Interrupt Line [7:0]:** This read/write field contains an 8-bit value that has no direct effect on the CL-GD7556. This field is used to transfer an interrupt pointer from the PCI system BIOS to the CL-GD7556 VGA BIOS.

8. SEQUENCER REGISTERS

NOTE: The registers in this chapter apply to CRT monitors.

8.1 SRX: Sequencer Index Register

I/O Port Address: 3C4

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Sequencer Index [4]	0
3	Sequencer Index [3]	0
2	Sequencer Index [2]	0
1	Sequencer Index [1]	0
0	Sequencer Index [0]	0

This index register is used to specify the register in the Sequencer block to be accessed by the next I/O read or I/O write to I/O port address 3C5.

Bit	Description
7:5	**Reserved**
4:0	**Sequencer Index [4:0]:** This 5-bit field selects the register to be accessed by the next I/O read or I/O write to I/O Port Address 3C5. When an index number is: • Equal to or less than 5, the index points to a VGA standard Sequencer register in this chapter. • More than 5, the index points to the registers that are defined in the Extension registers in Chapter 12.

8.2 SR0: Sequencer Reset Register

I/O Port Address: 3C5

Index: 0

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Synchronous Reset of Sequencer	1
0	Asynchronous Reset of Sequencer	1

This register is used to reset the CL-GD7556 sequencer. These bits are for standard VGA compatibility only, and after reset they need never be used.

Bit	Description
7:2	**Reserved**
1	**Synchronous Reset of Sequencer:** When this bit is programmed to: • 0, the sequencer is cleared and halted, which disables refresh for display memory and the display screen. • 1 *and* when SR0[0] is 1, the sequencer operates normally.
0	**Asynchronous Reset of Sequencer:** When this bit is programmed to: • 0, the sequencer is cleared and halted, and SR3 is cleared. • 1 *and* when SR0[1] is 1, the sequencer operates normally.

8.3 SR1: Clocking Mode Register

I/O Port Address: 3C5

Index: 1

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Full Display Memory Bandwidth	0
4	Shift and Load 32 Data Bits	0
3	Dot Clock Generation	0
2	Shift and Load 16 Data Bits	0
1	Reserved	
0	8/9 Dot Clock	0

This register is used to control miscellaneous functions in the CL-GD7556 sequencer.

Bit — **Description**

7:6 — **Reserved**

5 — **Full Display Memory Bandwidth:**

- When this bit is programmed to:
  - — 0, the CRT monitor screen refresh operates normally.
  - — 1, the CRT monitor screen refresh stops. In addition:
    - — The host CPU can use nearly 100% of the display memory bandwidth.
    - — Horizontal Sync and Vertical Sync continue normally.
    - — Refresh for display memory continues normally.
- Extension register GRE[4] overrides this bit. When GRE[4] is 1, the CRT monitor screen refresh is disabled.

4 — **Shift and Load 32 Data Bits:**

This bit, in combination with SR1[2], controls how often 8-bit, 16-bit, and 32-bit graphics controller display memory data shifters are loaded, according to the following table:

SR1 [4]	SR1 [2]	Frequency with which Graphics Controller Display Memory Data Shifters Are Loaded	Display Memory Data Width
0	0	Every character clock	8 bits
0	1	Every 2nd character clock	16 bits
1	X	Every 4th character clock	32 bits

8.3 SR1: Clocking Mode Register *(cont.)*

Bit	Description
3	**Dot Clock Generation:** When this bit is programmed to: • 0, VCLK (the master clock) is not divided. In this case, DCLK (the internal clock that is used as the dot clock) is the same frequency as the master clock. This dot clock is used for higher-resolution display modes. • 1, VCLK (the master clock) is divided by 2 to generate DCLK, a dot clock that in this case is half the frequency of the master clock. This dot clock is used for low-resolution display modes such as 0h, 1h, 4h, 5h, and Dh.
2	**Shift and Load 16 Data Bits:** This bit is used with SR1[4] to define the display memory data width. (For more information, refer to the description of bit [4] of this register.)
1	**Reserved**
0	**8/9 Dot Clock:** For display modes with 80 characters per horizontal scanline, this bit must be: • 0 to generate character clocks that are 9 dots wide, as required by display modes that use 360 or 720 horizontal dots. • 1 to generate character clocks that are 8 dots wide, as required by display modes that use 320 or 640 horizontal dots.

8.4 SR2: Bit Map Plane Mask Write Enable Register

I/O Port Address: 3C5

Index: 2

Bit	Description	Reset State
7	Pixel Data Write Enable [7] / Reserved	0
6	Pixel Data Write Enable [6] / Reserved	0
5	Pixel Data Write Enable [5] / Reserved	0
4	Pixel Data Write Enable [4] / Reserved	0
3	Pixel Data Write Enable [3] / Bit Map Plane 3 Mask Write Enable	0
2	Pixel Data Write Enable [2] / Bit Map Plane 2 Mask Write Enable	0
1	Pixel Data Write Enable [1] / Bit Map Plane 1 Mask Write Enable	0
0	Pixel Data Write Enable [0] / Bit Map Plane 0 Mask Write Enable	0

This register has two uses.

1) Its first use is to control the writing of up to eight pixels.

2) Its second use is to enable or disable writing to the four bit map planes of display memory.

Bit	Description
7:0	**Pixel Data Write Enable [7:0]:** When Extension register GRB[2] is 1, this register is extended from 4 bits to this 8-bit field. • This field is used to enable pixel data writes. When Extension register GRB[2] is 1 *and* Graphics Controller register bits GR5[2:0] are set to: — '001' *and* Extension register bit GRB[1] is 1, these SR2[7:0] bits control whether corresponding individual pixel data bits [7:0] can be written with Write mode 1. Example: When Extension register GRB[2] is 1 *and* bit 7 of this SR2 register is set to 1, the corresponding associated pixel data bit 7 is written. — '10X', these SR2[7:0] bits control whether corresponding individual pixel data bits [7:0] can be written with Extended Write modes 4 or 5. • This field is also used to write-protect the BitBLT (Bit Block Transfer) engine.
7:4	**Reserved:** When Extension register GRB[2] is 0 *and* Graphics Controller register bit GR5[2] is 0, these 4 bits are reserved. **NOTE:** These bit settings are used for VGA-compatibility modes.
3:0	**Bit Map Plane Mask Write Enable [3:0]:** When Extension register GRB[2] is 0, these 4 bits are used to control whether corresponding individual display memory bit map planes [3:0] are written with one of the Write modes 0–3 selected by Graphics Controller register bits GR5[2:0].

8.5 SR3: Character Map Set Select Register

I/O Port Address: 3C5

Index: 3

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Secondary Character Map Set Select [2]	0
4	Primary Character Map Set Select [2]	0
3	Secondary Character Map Set Select [1]	0
2	Secondary Character Map Set Select [0]	0
1	Primary Character Map Set Select [1]	0
0	Primary Character Map Set Select [0]	0

This register is used to specify the primary and the secondary character map sets (fonts). This register applies only to text display modes.

Bit **Description**

7:6 **Reserved**

5, 3:2 **Secondary Character Map Set Select:**
These 3 bits select from among the secondary character map sets, according to the following table:

SR3			Secondary Character Map Set	Address Offset (Kbytes)
[5]	[3]	[2]		
0	0	0	0	0
0	0	1	1	16
0	1	0	2	32
0	1	1	3	48
1	0	0	4	8
1	0	1	5	24
1	1	0	6	40
1	1	1	7	56

8.5 SR3: Character Map Set Select Register *(cont.)*

Bit	Description
4, 1:0	**Primary Character Map Set Select:** These 3 bits select from among the primary character map sets, according to the following table:

SR3			Primary Character Map Set	Address Offset (Kbytes)
[4]	[1]	[0]		
0	0	0	0	0
0	0	1	1	16
0	1	0	2	32
0	1	1	3	48
1	0	0	4	8
1	0	1	5	24
1	1	0	6	40
1	1	1	7	56

NOTES:

1) In text display modes:
   1. Character Map Plane 0 stores the ASCII text character code.
   2. Character Map Plane 1 stores the attribute byte.
   3. Character Map Plane 2 stores the character map set (the font).
   4. Character Map Plane 3 stores fonts that are wider than 8 dots per character line.

2) Bit 3 of the attribute byte normally controls the intensity of the foreground color. This bit can be redefined to be a switch between character sets, allowing 512 displayable characters. This switch is enabled whenever SR4[1] is a 1 *and* there is a difference between the values of the Primary Character Map Set and the values of the Secondary Character Map Set.

3) The format for the Character Map Plane 2 font address bits [15:0] is:

   F2 F1 F0 C7 C6 C5 C4 C3 C2 C1 C0 R4 R3 R2 R1 R0

   where:

   F[2:0] is the character map set (that is, the font)
   C[7:0] is the ASCII text character code
   R[4:0] is the character row (that is, the scanline within the character cell)

8.6 SR4: Display Memory Mode Register

I/O Port Address: 3C5

Index: 4

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Display Memory Chain-4 Addressing Mode	0
2	Display Memory Odd/Even Addressing Mode	0
1	Display Memory Extended Size	0
0	Reserved	

This register is used to control miscellaneous display memory functions.

Bit	Description
7:4	**Reserved**
3	**Display Memory Chain-4 Addressing Mode:** When this bit is programmed to: • 0, display memory planes are selected with Sequencer register SR2 and Graphics Controller register GR4. • 1, display memory planes are selected with addresses C/BE[3:0]#. — The effect of this bit is similar to SR4[2], except addresses are as follows: — Address C/BE0# provides Display Memory Plane Select bit [0]. — Address C/BE1# provides Display Memory Plane Select bit [1], and so forth. — This bit takes priority over SR4[2] and Graphics Controller register bit GR5[4], and Graphics Controller register GR4 is ignored.
2	**Display Memory Odd/Even Addressing Mode:** • The value of this bit must track Graphics Controller register GR5[4], and the value of this register must be opposite the value of GR5[4]. — The even CPU addresses access display memory planes 0 and 2. — The odd CPU addresses access display memory planes 1 and 3. • When this bit is programmed to: — 0, the Odd/Even addressing mode is enabled. This bit *must* be programmed to 0 for text display modes. — 1, the Odd/Even addressing mode is disabled, and a sequential addressing mode is enabled. • This bit can be overridden by the SR4[3] bit.
1	**Display Memory Extended Size:** When this bit is programmed to: • 0, effective display memory size is 64 Kbytes, regardless of actual installed display memory. (EGA display modes require this to be the case.) • 1, effective display memory size equals actual installed display memory.
0	**Reserved**

9. CRT CONTROLLER REGISTERS

WARNING: The timing registers given in Figure 9-1 must never be programmed by any application program. Incorrect timing can cause permanent damage to some CRT monitors. The correct way to program a display mode is to use the appropriate INT 10h BIOS Video Service routines.

NOTES:

1) The registers in this chapter apply to CRT monitors.
2) While reading this chapter, refer to Figure 9-1 on page 9-3 and Table 9-1 on page 9-4 for a detailed summary of CRT Controller registers.
3) Within this chapter, some registers have a '?' in the I/O port address. This question mark implies a 'B' for Monochrome mode (that is, 3B5) and 'D' for Color mode (that is, 3D5), depending on the setting of External/General register bit MISC[0].

9.1 CRX: CRT Controller Index Register

I/O Port Address: 3?4

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	CRT Controller Index [5]	0
4	CRT Controller Index [4]	0
3	CRT Controller Index [3]	0
2	CRT Controller Index [2]	0
1	CRT Controller Index [1]	0
0	CRT Controller Index [0]	0

This index register is used to specify the register in the CRT Controller block to be accessed by the next I/O read or I/O write to I/O port address 3?5.

Bit	Description
7:6	**Reserved**
5:0	**CRT Controller Index [5:0]:** The value resulting from these bits point to the register to be accessed in the next I/O read or I/O write to address 3?5. • Registers above index 18 were never documented by IBM. • Registers at indexes 19, 1A, 1B, 25, and 27 are described in the Extension registers in Chapter 12.

9.2 CR0: Horizontal Total Register

I/O Port Address: 3?5

Index: 0

Bit	Description	Reset State
7	Horizontal Total [7]	0
6	Horizontal Total [6]	0
5	Horizontal Total [5]	0
4	Horizontal Total [4]	0
3	Horizontal Total [3]	0
2	Horizontal Total [2]	0
1	Horizontal Total [1]	0
0	Horizontal Total [0]	0

This register is used to specify the total number of character clocks per horizontal period.

NOTE: This register can be write-protected by CRT Controller register bit CR11[7].

Bit **Description**

7:0 **Horizontal Total:**

- This 8-bit field specifies the total number of character clocks per horizontal period as follows:

  1. The VCLK signal provides the character clock. (The character clock is derived from VCLK, according to the character width.)
  2. The character counter counts the total number of character clocks.
  3. The value in the character counter is then compared with the value in this register to provide the basic horizontal timing. (All horizontal and vertical timing is eventually derived from the basic horizontal timing in this register.)

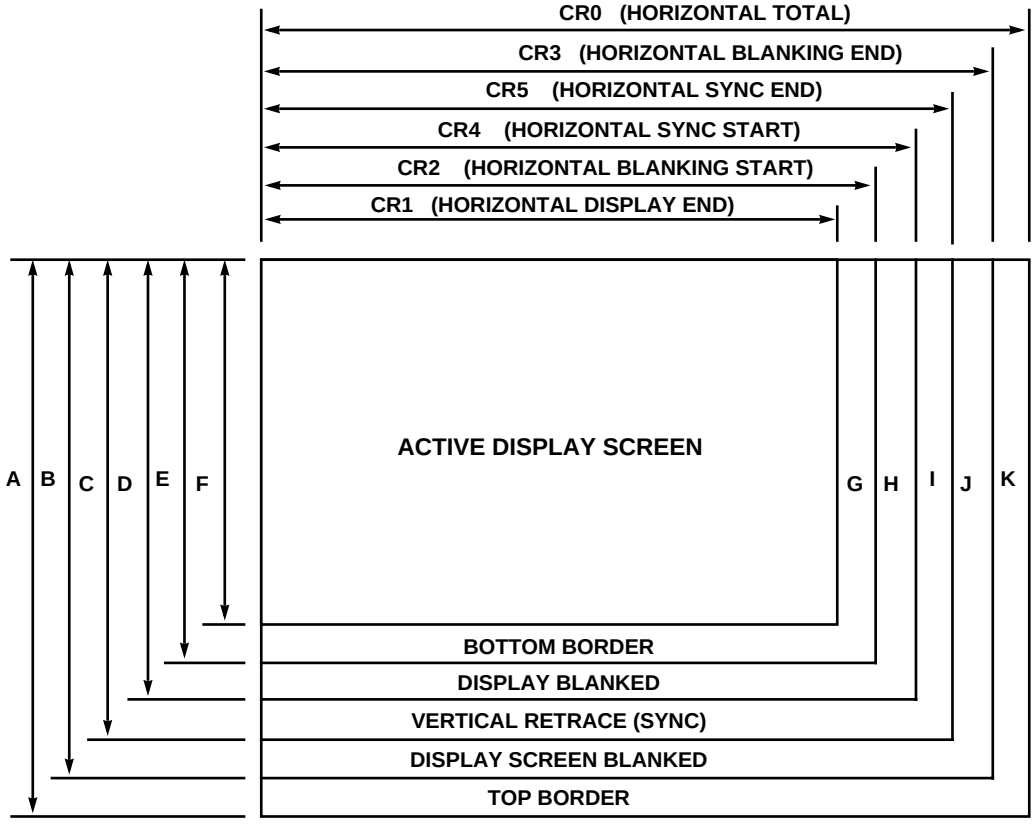
- The value of the horizontal total for this register is calculated as follows:

  FROM: Total number of character clocks (from character counter)
  SUBTRACT: – 5 character clocks (for standard VGA compatibility)
  TO OBTAIN: = Horizontal total

  Example:
  If 80 characters are desired per horizontal scanline, then a value of 75 must be loaded into this register.

- Figure 9-1 indicates the way the horizontal and vertical timing is defined.
  — The horizontal timing is calculated in terms of character clock periods.
  — The vertical timing is calculated in terms of horizontal periods.
- Table 9-1 indicates how the various CRT Controller registers are extended.

9.2 CR0: Horizontal Total Register *(cont.)*



A - CR6 (VERTICAL TOTAL)

B - CR16 (VERTICAL BLANKING END)

C - CR11 (VERTICAL SYNC END)

D - CR10 (VERTICAL SYNC START)

E - CR15 (VERTICAL BLANKING START)

F - CR12 (VERTICAL DISPLAY END)

G - RIGHT BORDER

H - DISPLAY SCREEN BLANKED

I - HORIZONTAL RETRACE (SYNC)

J - DISPLAY SCREEN BLANKED

K - LEFT BORDER

Figure 9-1. CRT Controller Timing Registers

9.2 CR0: Horizontal Total Register *(cont.)*

Table 9-1 is a guide to the location of the CRT Controller registers and accompanying extension and overflow bits.

- An extension bit is a bit added by Cirrus Logic to the standard VGA controller bits.
- An overflow bit is a standard VGA controller bit that results from using more than 8 bits to define a field.

Table 9-1. Summary of CRT Controller Register Bits[a]

Parameter	CRT Controller Register Bit Position					
	[9]	**[8]**	**[7]**	**[6]**	**[5]**	**[4:0]**
Horizontal Total			CR0[7]	CR0[6]	CR0[5]	CR0[4:0]
Horizontal Display End			CR1[7]	CR1[6]	CR1[5]	CR1[4:0]
Horizontal Blanking Start			CR2[7]	CR2[6]	CR2[5]	CR2[4:0]
Horizontal Blanking End			**CR1A[5]**	**CR1A[4]**	CR5[7]	CR3[4:0]
Horizontal Sync Start			CR4[7]	CR4[6]	CR4[5]	CR4[4:0]
Horizontal Sync End						CR5[4:0]
Vertical Total	CR7[5]	CR7[0]	CR6[7]	CR6[6]	CR6[5]	CR6[4:0]
Vertical Sync Start	CR7[7]	CR7[2]	CR10[7]	CR10[6]	CR10[5]	CR10[4:0]
Vertical Sync End						CR11[3:0]
Vertical Display End	CR7[6]	CR7[1]	CR12[7]	CR12[6]	CR12[5]	CR12[4:0]
Vertical Blanking Start	CR9[5]	CR7[3]	CR15[7]	CR15[6]	CR15[5]	CR15[4:0]
Vertical Blanking End	**CR1A[7]**	**CR1A[6]**	CR16[7]	CR16[6]	CR16[5]	CR16[4:0]
Line Compare	CR9[6]	CR7[4]	CR18[7]	CR18[6]	CR18[5]	CR18[4:0]
Scanline Offset		**CR1B[4]**	CR13[7]	CR13[6]	CR13[5]	CR13[4:0]
	[19]	**[18]**	**[17]**	**[16]**	**[15:8]**	**[7:0]**
Screen A Start Address, Bits [19:0]	**CR1D[7]**	**CR1B[3]**	**CR1B[2]**	**CR1B[0]**	CRC[7:0]	CRD[7:0]

[a] Bits shown in **bold** text are Cirrus Logic extensions (that is, bits that appear in the Extension registers in Chapter 12).

9.3 CR1: Horizontal Display End Register

I/O Port Address: 3?5

Index: 1

Bit	Description	Reset State
7	Horizontal Display End [7]	0
6	Horizontal Display End [6]	0
5	Horizontal Display End [5]	0
4	Horizontal Display End [4]	0
3	Horizontal Display End [3]	0
2	Horizontal Display End [2]	0
1	Horizontal Display End [1]	0
0	Horizontal Display End [0]	0

This register is used to specify the number of character clocks during horizontal display time.

NOTES:

1) This register can be write-protected by CRT Controller register bit CR11[7].

2) For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7:0	**Horizontal Display End [7:0]:** For the horizontal display time, this register specifies the number of character clocks, *minus 1*, as calculated for both text and graphics display modes. • For text display modes: CR1[7:0] = “Number of character clocks” – 1 Where number of character clocks = Number of characters • For graphics display modes: CR1[7:0] = “Number of character clocks” – 1 Where number of character clocks = (Number of pixels/scanline) ÷ (Number of pixels/character clock)

9.4 CR2: Horizontal Blanking Start Register

I/O Port Address: 3?5

Index: 2

Bit	Description	Reset State
7	Horizontal Blanking Start [7]	0
6	Horizontal Blanking Start [6]	0
5	Horizontal Blanking Start [5]	0
4	Horizontal Blanking Start [4]	0
3	Horizontal Blanking Start [3]	0
2	Horizontal Blanking Start [2]	0
1	Horizontal Blanking Start [1]	0
0	Horizontal Blanking Start [0]	0

This register is used to specify the character count at which horizontal blanking starts.

NOTES:

1) This register can be write-protected by CRT Controller register bit CR11[7].

2) For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** This register specifies the character count at which horizontal blanking starts. • For text display modes: Character count at which horizontal blanking starts = Number of characters • For graphics display modes: Character count at which horizontal blanking starts = (Number of pixels/scanline) ÷ (Number of pixels/character clock) • For both text and graphics display modes: The value programmed into CR2 must always be larger than the value programmed into CRT Controller register CR1.

9.5 CR3: Horizontal Blanking End Register

I/O Port Address: 3?5

Index: 3

Bit	Description	Reset State
7	Compatible Read	0
6	Display Enable Delay [1]	0
5	Display Enable Delay [0]	0
4	Horizontal Blanking End [4]	0
3	Horizontal Blanking End [3]	0
2	Horizontal Blanking End [2]	0
1	Horizontal Blanking End [1]	0
0	Horizontal Blanking End [0]	0

This register is used to determine the horizontal blanking period width. Also, this register controls access to CRT Controller registers CR10 and CR11 and the display enable delay.

NOTES:

1) This register can be write-protected by CRT Controller register bit CR11[7].

2) For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit — **Description**

7 — **Compatible Read:**
When this bit is:
- 0, CRT Controller registers CR10 and CR11 are write-only registers.
- 1, CRT Controller registers CR10 and CR11 are read/write registers.

6:5 — **Display Enable Delay [1:0]:**
This 2-bit field is used to specify the number of character clocks that the display enable signal is delayed from the horizontal total. This delay is necessary to compensate for the accesses of the character code, attribute byte, font, and so forth. The following table indicates programming for the display enable signal delay:

CR3		Delay for Display Enable Signal (in number of character clocks)
[6]	[5]	
0	0	No delay
0	1	1 character clock (typical setting)
1	0	2 character clocks
1	1	3 character clocks

NOTE: If the delay is programmed too low, the left-most character repeats. If the delay is programmed too high, one or more characters disappear at the left of each character row.

9.5 CR3: Horizontal Blanking End Register *(cont.)*

Bit	Description
4:0	**Horizontal Blanking End [4:0]:** The 8-bit Horizontal Blanking End field determines the end of the horizontal blanking period by specifying the width of the horizontal blanking period. • Bits [7:6], the most-significant bits, are in Extension register CR1A[5:4]. These bits are available when either of the following conditions are true: — Extension register CR1B[5] is 1. — Extension register CR1B[7] is 1. • Bit 5, which is available as needed, is in CR5[7]. • Bits [4:0], the least-significant bits, are in this register.

Register Format for 8-Bit Horizontal Blanking End

CR1A[5:4]		CR5[7]	CR3[4:0]	
7	6	5	4	0

The Horizontal Blanking End register is programmed as follows:

1. When Extension register bit CR1B[5] is 0 *and* CR1B[7] is 0, the least-significant 5 (or 6) bits of the character counter are compared with the contents of this field.

2. When Extension register bit CR1B[5] is 1 *or* CR1B[7] is 1, all 8 bits of the character counter are compared with the contents of this field.

3. When a match occurs, the horizontal blanking period ends.

FROM:		Horizontal Blanking Start (value programmed into CR2)
ADD:	+	Horizontal blanking period (as desired)
TO OBTAIN:		Horizontal Blanking End

- The horizontal blanking period:
  — Must never be programmed to extend past the horizontal total.
  — Is limited to 63 character-clock times.

9.6 CR4: Horizontal Sync Start Register

I/O Port Address: 3?5

Index: 4

Bit	Description	Reset State
7	Horizontal Sync Start [7]	0
6	Horizontal Sync Start [6]	0
5	Horizontal Sync Start [5]	0
4	Horizontal Sync Start [4]	0
3	Horizontal Sync Start [3]	0
2	Horizontal Sync Start [2]	0
1	Horizontal Sync Start [1]	0
0	Horizontal Sync Start [0]	0

This register specifies the time when horizontal synchronization becomes active.

NOTES:

1) This register can be write-protected by CRT Controller register bit CR11[7].

2) For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** This field specifies the character count at which Horizontal Sync becomes active. Adjusting the value in this field moves the display horizontally on the screen. • The Horizontal Sync Start must be programmed to a value either equal to or greater than Horizontal Display End value specifed in CR1. • The time from Horizontal Sync Start to Horizontal Total must be either equal to or greater than four character-clock times.

9.7 CR5: Horizontal Sync End Register

I/O Port Address: 3?5

Index: 5

Bit	Description	Reset State
7	Horizontal Blanking End [5]	0
6	Horizontal Sync Delay [1]	0
5	Horizontal Sync Delay [0]	0
4	Horizontal Sync End [4]	0
3	Horizontal Sync End [3]	0
2	Horizontal Sync End [2]	0
1	Horizontal Sync End [1]	0
0	Horizontal Sync End [0]	0

This register specifies the position where the horizontal synchronization pulse ends, effectively specifying the width of the pulse. In addition, this register contains an overflow bit and a field for the horizontal synchronization delay.

NOTES:

1) This register can be write-protected by CRT Controller register bit CR11[7].
2) For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit **Description**

7 **Horizontal Blanking End [5]:**
This overflow bit increases by 1 bit the horizontal blanking end value of CR3[4:0]. For details, refer to CR3[4:0].

Register Format for 8-Bit MHorizontal Blanking End

CR1A[5:4]		CR5[7]	CR3[4:0]	
7	6	5	4	0

6:5 **Horizontal Sync Delay [1:0]:**
This 2-bit field is used to specify the number of character clocks that the external horizontal synchronization pulse is delayed from the horizontal synchronization start position implied in CR4. In some graphics display modes, this horizontal synchronization delay is necessary to allow internal timing signals that are triggered from horizontal synchronization start to begin, prior to display enable. The following table summarizes programming for the horizontal synchronization delay:

CR5		Delay for Horizontal Synchronization Pulse (in number of character clocks)
[6]	[5]	
0	0	No delay
0	1	1 character-clock delay
1	0	2 character-clock delay
1	1	3 character-clock delay

9.7 CR5: Horizontal Sync End Register *(cont.)*

Bit	Description
4:0	**Horizontal Sync End [4:0]:** • This 5-bit field determines the end of the Horizontal Sync pulse by specifying the width of the Horizontal Sync pulse. • The least-significant 5 bits of the character counter are compared with the contents of this field. When a match occurs, the horizontal synchronization pulse ends. • The horizontal synchronization end value to be programmed into this register is calculated as follows: FROM: Horizontal Sync Start (value programmed in CR4) ADD: + Horizontal Sync Width (as desired) TO OBTAIN: = Horizontal Sync End • The horizontal synchronization pulse: — Has a width limited to 31 character-clock times. — Must never be programmed to extend past the horizontal total of CR0. — Must always end during the horizontal blanking period.

9.8 CR6: Vertical Total Register

I/O Port Address: 3?5

Index: 6

Bit	Description	Reset State
7	Vertical Total [7]	0
6	Vertical Total [6]	0
5	Vertical Total [5]	0
4	Vertical Total [4]	0
3	Vertical Total [3]	0
2	Vertical Total [2]	0
1	Vertical Total [1]	0
0	Vertical Total [0]	0

This register contains the least-significant 8 bits of the 10-bit Vertical Total field.

NOTES:

1) This register can be write-protected by CRT Controller register bit CR11[7].
2) For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit **Description**

7:0 **Vertical Total [7:0]:**
The 10-bit Vertical Total field specifies the total number of scanlines per frame.

- Bits [9,8], the most-significant bits, are in register CR7[5,0].
- Bits [7:0], the least-significant bits, are in this register.

Register Format for 10-Bit Vertical Total

CR7[5]	CR7[0]	CR6[7:0]	
9	8	7	0

- The value of the Vertical Total field to be programmed is calculated as follows:

  FROM: Total number of horizontal scanlines
  SUBTRACT: – 2 scanlines
  TO OBTAIN: = Vertical Total field (total number of scanlines per frame)

  When the value in the scanline counter equals the value of the Vertical Total field, a vertical retrace period begins.

9.9 CR7: Overflow Register

I/O Port Address: 3?5

Index: 7

Bit	Description	Reset State
7	Vertical Sync Start [9]	0
6	Vertical Display End [9]	0
5	Vertical Total [9]	0
4	Line Compare [8]	0
3	Vertical Blanking Start [8]	0
2	Vertical Sync Start [8]	0
1	Vertical Display End [8]	0
0	Vertical Total [8]	0

This register contains overflow bits for various vertical count fields.

NOTES:

1) This register can be write-protected by CRT Controller register bit CR11[7].

2) For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit **Description**

7 **Vertical Sync Start [9]:**
This is bit 9, the most-signficant bit of the 10-bit Vertical Sync Start field.

Register Format for 10-Bit Vertical Sync Start

CR7[7]	CR7[2]	CR10[7:0]	
9	8	7	0

For details on this field, refer to CRT Controller register CR10.

6 **Vertical Display End [9]:**
This is bit 9, the most-significant bit of the 10-bit Vertical Display End field.

Register Format for 10-Bit Vertical Display End

CR7[6]	CR7[1]	CR12[7:0]	
9	8	7	0

For details on this field, refer to CRT Controller register CR12.

5 **Vertical Total [9]:**
This is bit 9, the most significant bit of the 10-bit Vertical Total field.

Register Format for 10-Bit Vertical Total

CR7[5]	CR7[0]	CR6[7:0]	
9	8	7	0

For details on this field, refer to CRT Controller register CR6.

9.9 CR7: Overflow Register *(cont.)*

Bit	Description
4	**Line Compare [8]:** This is bit 8 of the 10-bit Line Compare field. This bit can always be written. **Register Format for 10-Bit Line Compare** CR9[6] | CR7[4] | CR18[7:0] 9 | 8 | 7 0 For details on this field, refer to CRT Controller register CR18.
3	**Vertical Blanking Start [8]:** This is bit 8 of the 10-bit Vertical Blanking Start field. **Register Format for 10-Bit Vertical Blanking Start** CR9[5] | CR7[3] | CR15[7:0] 9 | 8 | 7 0 For details on this field, refer to CRT Controller register CR15.
2	**Vertical Sync Start [8]:** This is bit 8 of the 10-bit Vertical Sync Start field. **Register Format for 10-Bit Vertical Sync Start** CR7[7] | CR7[2] | CR10[7:0] 9 | 8 | 7 0 For details on this field, refer to CRT Controller register CR10.
1	**Vertical Display End [8]:** This is bit 8 of the 10-bit Vertical Display End field. **Register Format for 10-Bit Vertical Display End** CR7[6] | CR7[1] | CR12[7:0] 9 | 8 | 7 0 For details on this field, refer to CRT Controller register CR12.
0	**Vertical Total [8]:** This is bit 8 of the 10-bit Vertical Total field. **Register Format for 10-Bit Vertical Total** CR7[5] | CR7[0] | CR6[7:0] 9 | 8 | 7 0 For details on this field, refer to CRT Controller register CR6.

9.10 CR8: Screen A Preset Row Scan Register

I/O Port Address: 3?5

Index: 8

Bit	Description	Reset State
7	Reserved	
6	Byte (Coarse) Panning [1]	0
5	Byte (Coarse) Panning [0]	0
4	Screen A Preset Row Scan [4]	0
3	Screen A Preset Row Scan [3]	0
2	Screen A Preset Row Scan [2]	0
1	Screen A Preset Row Scan [1]	0
0	Screen A Preset Row Scan [0]	0

This register specifies the row scanline at which Screen A starts, which provides scrolling on a scanline basis. In addition, this register specifies byte (coarse) panning.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit **Description**

7 **Reserved**

6:5 **Byte (Coarse) Panning [1:0]:**
This 2-bit field controls coarse panning on a character basis. (For fine panning on a pixel-by-pixel basis, refer to Attribute Controller register AR13.)
- This field can specify a coarse pan of up to 24 pixels, with 8-pixel resolution.
- Values for CR8[6:5] are interpreted as indicated in the following table:

CR8		Resulting Pan (in bytes and corresponding pixels)
[6]	[5]	
0	0	0 bytes (0 pixels)
0	1	1 byte (8 pixels)
1	0	2 bytes (16 pixels)
1	1	3 bytes (24 pixels)

4:0 **Screen A Preset Row Scan [4:0]:**
This field specifies the scanline at which the first character row of Screen A begins.
- This specification provides scrolling on a scanline basis (which is also called ‘soft’ scrolling).
- The contents of this field must be changed only during vertical retrace.

9.11 CR9: Character Cell Height Register

I/O Port Address: 3?5

Index: 9

Bit	Description	Reset State
7	Scanline Doubling Control	0
6	Line Compare [9]	0
5	Vertical Blanking Start [9]	0
4	Character Cell Height [4]	0
3	Character Cell Height [3]	0
2	Character Cell Height [2]	0
1	Character Cell Height [1]	0
0	Character Cell Height [0]	0

This register specifies the character cell height (that is, the number of scanlines in the character cell). In addition, this register contains two overflow bits and one control bit.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit — **Description**

7 — **Scanline Doubling Control:**
When this bit is 1, every scanline is displayed twice in succession.
- Scanlines double for those specifications based on scanline counter addressing, such as Character Cell Height, Text Cursor Start, Text Cursor End, and Underline location.
- Typically, this bit is used to double a 200-scanline display to 400 scanlines.
- The scanline doubling function is not available in interlaced graphics modes.

6 — **Line Compare [9]:**
This is bit 9, the most-significant bit of the 10-bit Line Compare field.

Register Format for 10-Bit Line Compare

CR9[6]	CR7[4]	CR18[7:0]	
9	8	7	0

For details on this field, refer to CRT Controller register CR18.

5 — **Vertical Blanking Start [9]:**
This is bit 9, the most-significant bit of the 10-bit Vertical Blanking Start field.

Register Format for 10-Bit Vertical Blanking Start

CR9[5]	CR7[3]	CR15[7:0]	
9	8	7	0

For details on this field, refer to CRT Controller register CR15.

4:0 — **Character Cell Height [4:0]:**
This 5-bit field specifies the vertical size of the character cell in terms of scanlines. The value programmed into this field equals the actual size of the character cell (in scanlines) minus 1.

9.12 CRA: Text Cursor Start Register

I/O Port Address: 3?5

Index: A

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Text Cursor Disable	0
4	Text Cursor Start [4]	0
3	Text Cursor Start [3]	0
2	Text Cursor Start [2]	0
1	Text Cursor Start [1]	0
0	Text Cursor Start [0]	0

This register contains a bit that can disable the text cursor. In addition, this register specifies the scanline at which the text cursor is to start.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7:6	**Reserved**
5	**Text Cursor Disable:** When this bit is: • 0, the text cursor functions normally • 1, the text cursor is disabled (that is, it is removed).
4:0	**Text Cursor Start [4:0]:** This field specifies the scanline within the character cell at which the text cursor is to start. When, compared to the the Text Cursor End value specified in CRT Controller register CRB, the Text Cursor Start value is: • Greater than the Text Cursor End value, no text cursor displays. • Equal to the Text Cursor End value, the text cursor displays on a single scanline.

9.13 CRB: Text Cursor End Register

I/O Port Address: 3?5

Index: B

Bit	Description	Reset State
7	Reserved	
6	Text Cursor Delay [1]	0
5	Text Cursor Delay [0]	0
4	Text Cursor End [4]	0
3	Text Cursor End [3]	0
2	Text Cursor End [2]	0
1	Text Cursor End [1]	0
0	Text Cursor End [0]	0

This register specifies the scanline at which the text cursor is to end. It also contains a field that allows the text cursor display to be delayed from the location specified in CRE and CRF.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7	**Reserved**
6:5	**Text Cursor Delay [1:0]:** This 2-bit field specifies a delay, given in character clocks, from the text cursor location specified in registers CRE and CRF to the actual display of the text cursor.
4:0	**Text Cursor End [4:0]:** This field specifies the scanline within the character cell at which the text cursor is to end. When, compared to the Character Cell Height specified in CRT Controller register CR9, the Text Cursor End value is: • Less than or equal to the Character Cell Height, no text cursor displays. • Greater than the Character Cell Height, the effective Text Cursor End value is equal to the Character Cell Height.

9.14 CRC: Screen A Start Address High Register

I/O Port Address: 3?5

Index: C

Bit	Description	Reset State
7	Screen A Start Address [15]	0
6	Screen A Start Address [14]	0
5	Screen A Start Address [13]	0
4	Screen A Start Address [12]	0
3	Screen A Start Address [11]	0
2	Screen A Start Address [10]	0
1	Screen A Start Address [9]	0
0	Screen A Start Address [8]	0

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7:0	**Screen A Start Address [15:8]:** These bits are bits [15:8] of the 20-bit Screen A Start Address field. **Register Format for 20-Bit Screen A Start Address** For details on this field, refer to Extension register CR1D.

CR1D[7]	CR1B[3:2]		CR1B[0]	CRC[7:0]		CRD[7:0]	
19	18	17	16	15	8	7	0

9.15 CRD: Screen A Start Address Low Register

I/O Port Address: 3?5

Index: D

Bit	Description	Reset State
7	Screen A Start Address [7]	0
6	Screen A Start Address [6]	0
5	Screen A Start Address [5]	0
4	Screen A Start Address [4]	0
3	Screen A Start Address [3]	0
2	Screen A Start Address [2]	0
1	Screen A Start Address [1]	0
0	Screen A Start Address [0]	0

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7:0	**Screen A Start Address [7:0]:** These bits are bits [7:0] of the 20-bit Screen A Start Address field. **Register Format for 20-Bit Screen A Start Address** For details on this field, refer to Extension register CR1D.

CR1D[7]	CR1B[3:2]		CR1B[0]	CRC[7:0]		CRD[7:0]	
19	18	17	16	15	8	7	0

9.16 CRE: Text Cursor Location High Register

I/O Port Address: 3?5

Index: E

Bit	Description	Reset State
7	Text Cursor Location [15]	0
6	Text Cursor Location [14]	0
5	Text Cursor Location [13]	0
4	Text Cursor Location [12]	0
3	Text Cursor Location [11]	0
2	Text Cursor Location [10]	0
1	Text Cursor Location [9]	0
0	Text Cursor Location [8]	0

This register contains the most-significant 8 bits of the 16-bit Text Cursor Location field.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7:0	**Text Cursor Location [15:8]:** The 16-bit Text Cursor Location field specifies the display memory location where the text cursor is to be displayed. • Bits [15:8], the most-significant bits, are in this register. • Bits [7:0], the least-significant bits, are in register CRF. **Register Format for 16-Bit Text Cursor Location** CRE[15:8] (15 … 8) | CRF[7:0] (7 … 0) • The value contained in the Text Cursor Location field specifies an address in display memory, not an offset from the beginning of the screen. When the value of the Screen A Start is changed without a compensating change in the Text Cursor Location field, the text cursor moves on the screen.

9.17 CRF: Text Cursor Location Low Register

I/O Port Address: 3?5

Index: F

Bit	Description	Reset State
7	Text Cursor Location [7]	0
6	Text Cursor Location [6]	0
5	Text Cursor Location [5]	0
4	Text Cursor Location [4]	0
3	Text Cursor Location [3]	0
2	Text Cursor Location [2]	0
1	Text Cursor Location [1]	0
0	Text Cursor Location [0]	0

This register contains the least-significant 8 bits of the 16-bit Text Cursor Location field.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7:0	**Text Cursor Location [7:0]:** These bits are bits [7:0] of the 16-bit Text Cursor Location field. **Register Format for 16-Bit Text Cursor Location** CRE[15:8] (bits 15–8) | CRF[7:0] (bits 7–0) For details on this field, refer to Extension register CRE.

9.18 CR10: Vertical Sync Start Register

I/O Port Address: 3?5

Index: 10

Bit	Description	Reset State
7	Vertical Sync Start [7]	0
6	Vertical Sync Start [6]	0
5	Vertical Sync Start [5]	0
4	Vertical Sync Start [4]	0
3	Vertical Sync Start [3]	0
2	Vertical Sync Start [2]	0
1	Vertical Sync Start [1]	0
0	Vertical Sync Start [0]	0

This register contains the least-significant 8 bits of the 10-bit Vertical Sync Start field.

NOTES:

1) For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.
2) Access to this register is controlled by CRT Controller register CR3[7]. When CR3[7] is:
   a) 0, this register is write-only
   b) 1, this register is read/write

Bit	Description
7:0	**Vertical Sync Start [7:0]:** The 10-bit Vertical Sync Start field specifies the scanline at which the Vertical Sync pulse is to become active. • Bits [9,8], the most-significant bits, are in CRT Controller register CR7[7,2]. • Bits [7:0], the least-significant bits, are in this register.

Register Format for 10-Bit Vertical Sync Start

CR7[7]	CR7[2]	CR10[7:0]	
9	8	7	0

9.19 CR11: Vertical Sync End Register

I/O Port Address: 3?5

Index: 11

Bit	Description	Reset State
7	CRT Controller Registers CR0–CR7 Write Protect	0
6	Refresh Cycle Control	0
5	Vertical Interrupt Disable	0
4	Vertical Interrupt Clear	0
3	Vertical Sync End [3]	0
2	Vertical Sync End [2]	0
1	Vertical Sync End [1]	0
0	Vertical Sync End [0]	0

This register specifies the scanline at which the Vertical Sync pulse is to become inactive, thereby effectively specifying the Vertical Sync pulse width. In addition, this register contains controls for the vertical interrupt as well as two miscellaneous control bits, CR11[7:6].

NOTES:

1) For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.
2) Access to this register is controlled by CRT Controller register CR3[7]. When CR3[7] is:
   a) 0, this register is write-only
   b) 1, this register is read/write

Bit	Description
7	**CRT Controller Registers CR0–CR7 Write Protect:** When this bit is: • 0, CRT Controller registers CR0–CR7 can be written normally. • 1, CRT Controller registers CR0–CR7 cannot be written, except for CR7[4], which can always be written.
6	**Refresh Cycle Control:** When this bit is: • 0, three refresh cycles execute per scanline. • 1, five refresh cycles execute per scanline.
5	**Vertical Interrupt Disable:** When this bit is: • 0, vertical interrupt is enabled and functions normally. • 1, vertical interrupt is disabled, and the INTR# pin cannot go active.

9.19 CR11: Vertical Sync End Register *(cont.)*

Bit	Description
4	**Vertical Interrupt Clear:** When this bit is: • 0, the External/General register FEAT[7] clears to 0, and the INTR# pin is forced inactive (high). • 1, the next occurrence of the INTR# pin interrupt occurs. (This bit can be set to 1 immediately after this bit is cleared to 0.)
3:0	**Vertical Sync End [3:0]:** This field determines the end of the Vertical Sync pulse by specifying the width of the Vertical Sync pulse. • The value of this field is compared with the least-significant 4 bits of the Scan-line Counter. When a match occurs, the Vertical Sync pulse is ended. • The Vertical Sync pulse is limited to 15 scanlines. • The Vertical Sync End value for this register can be calculated as follows: FROM: Vertical Sync Start (value programmed in CR10 and CR7[7,2]) SUBTRACT: – Vertical Sync Width (as desired) TO OBTAIN: = Vertical Sync End • The Vertical Sync End must never be programmed to extend past the Vertical Total.

9.20 CR12: Vertical Display End Register

I/O Port Address: 3?5

Index: 12

Bit	Description	Reset State
7	Vertical Display End [7]	0
6	Vertical Display End [6]	0
5	Vertical Display End [5]	0
4	Vertical Display End [4]	0
3	Vertical Display End [3]	0
2	Vertical Display End [2]	0
1	Vertical Display End [1]	0
0	Vertical Display End [0]	0

This register contains the least-significant 8 bits of the 10-bit Vertical Display End field.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7:0	**Vertical Display End [7:0]:** The 10-bit Vertical Display End field is used to specify the scanline at which the display is to end. • Bits [9,8], the most-significant bits, are in CRT Controller register CR7[6,1]. • Bits [7:0], the least-significant bits, are in this register.

Register Format for 10-Bit Vertical Display End

CR7[6]	CR7[1]	CR12[7:0]	
9	8	7	0

9.21 CR13: Scanline Offset Register

I/O Port Address: 3?5

Index: 13

Bit	Description	Reset State
7	Scanline Offset [7]	0
6	Scanline Offset [6]	0
5	Scanline Offset [5]	0
4	Scanline Offset [4]	0
3	Scanline Offset [3]	0
2	Scanline Offset [2]	0
1	Scanline Offset [1]	0
0	Scanline Offset [0]	0

This register contains the least-significant 8 bits of the 9-bit Scanline Offset field.

NOTES:

1) For information on extension offset registers, refer to Extension registers GR9 and GRA.

2) For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit **Description**

7:0 **Scanline Offset [7:0]:**
The 9-bit Scanline Offset field specifies the display 'pitch', which is the distance in the display memory between the beginnings of adjacent character rows or scanlines.

- Bit 8, the most-significant bit, is in Extension register CR1B[4].
- Bits [7:0], the least-significant bits, are in this register.

Register Format for 9-Bit Scanline Offset

CR1B[4]	CR13[7:0]	
8	7	0

- Except for the first scanline, to get the address from which to begin fetching data:

  TO: The contents of this field (CR13[7:0] and CR1B[4])
  ADD: + The beginning address of previous scanline or character row
  TO OBTAIN: = The scanline offset

- When CRT Controller register CR17[6] is:
  — 0, the scanline offset shifts left one bit position.
  — 1, the scanline offset is not shifted.

9.22 CR14: Underline Row Scanline Register

I/O Port Address: 3?5

Index: 14

Bit	Description	Reset State
7	Reserved	0
6	Doubleword Address Mode for Display Memory	0
5	Count by Four	0
4	Scanline Underline Row [4]	0
3	Scanline Underline Row [3]	0
2	Scanline Underline Row [2]	0
1	Scanline Underline Row [1]	0
0	Scanline Underline Row [0]	0

This register is used to specify the underline row scanline for text display modes.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7	**Reserved**
6	**Doubleword Address Mode for Display Memory:** When this bit is: • 0, *and* CRT Controller register CR17[6] is a: — 0, the Word Address mode is enabled. — 1, the Byte Address mode is enabled. • 1, Doubleword Address mode is selected. — The CRT Controller Memory Address Counter is rotated left for 2 bit positions. — As a result, display memory address bits MA[1] and MA[0] are sourced from CRT Controller Address Counter bits [13] and [12], respectively.
5	**Count by Four:** When Doubleword Address mode is: • Disabled (that is, CR14[6] is 0), this bit must be cleared to 0. • Enabled (that is, CR14[6] is 1), this bit must be set to 1 to enable a divide-by-4 character clock to the Memory Address Counter.
4:0	**Scanline Underline Row [4:0]:** Within a character cell, this field specifies the scanline at which the underline occurs.

9.23 CR15: Vertical Blanking Start Register

I/O Port Address: 3?5

Index: 15

Bit	Description	Reset State
7	Vertical Blanking Start [7]	0
6	Vertical Blanking Start [6]	0
5	Vertical Blanking Start [5]	0
4	Vertical Blanking Start [4]	0
3	Vertical Blanking Start [3]	0
2	Vertical Blanking Start [2]	0
1	Vertical Blanking Start [1]	0
0	Vertical Blanking Start [0]	0

This register contains the least-significant 8 bits of the 10-bit Vertical Blanking Start field.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7:0	**Vertical Blanking Start [7:0]:** The 10-bit Vertical Blanking Start field specifies the scanline at which vertical blanking is to start (that is, the scanline at which blanking is to become active). • Bit 9, the most-significant bit, is in CRT Controller register CR9[5]. • Bit 8 is in CRT Controller register CR7[3]. • Bits [7:0], the least-significant 8 bits of this field, are in this register.

Register Format for 10-Bit Vertical Blanking Start

CR9[5]	CR7[3]	CR15[7:0]	
9	8	7	0

9.24 CR16: Vertical Blanking End Register

I/O Port Address: 3?5

Index: 16

Bit	Description	Reset State
7	Vertical Blanking End [7]	0
6	Vertical Blanking End [6]	0
5	Vertical Blanking End [5]	0
4	Vertical Blanking End [4]	0
3	Vertical Blanking End [3]	0
2	Vertical Blanking End [2]	0
1	Vertical Blanking End [1]	0
0	Vertical Blanking End [0]	0

The Vertical Blanking End field specifies the scanline at which vertical blanking is to end.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit **Description**

7:0 **Vertical Blanking End [7:0]:**
The Vertical Blanking End field specifies the scanline at which vertical blanking is to end. The length of the Vertical Blanking End field depends on the settings of Extension register bits CR1B[7,5].

- When Extension register bit CR1B[7] is 0 *and* CR1B[5] is 0:
  - The entire Vertical Blanking End field is only the 8 bits of CRT Controller register CR16[7:0].
- When either Extension register bit CR1B[7] is 1 *or* CR1B[5] is 1:
  - The Vertical Blanking End field is extended to 10 bits.
  - Bits [9:8] are in Extension register bits CR1A[7:6].
  - Bits [7:0], the least-significant bits, are in this register.

Register Format for 10-Bit Vertical Blanking End

CR1A[7:6]		CR16[7:0]	
9	8	7	0

The contents of the Vertical Blanking End field are compared to the scanline counter to determine when to terminate vertical blanking.

- When Extension register bit CR1B[7] is 0 *and* CR1B[5] is 0, vertical blanking terminates at 255 scanlines.
- When either Extension register bit CR1B[7] is 1 *or* CR1B[5] is 1, vertical blanking terminates at 1023 scanlines.

9.25 CR17: CRT Controller Mode Control Register

I/O Port Address: 3?5

Index: 17

Bit	Description	Reset State
7	CRT Controller Timing Logic Enable	0
6	Byte/Word Address Mode Control	0
5	Address Rotation	0
4	Reserved	
3	Count by Two	0
2	Multiply Vertical Registers by Two	0
1	Compatibility-Mode (Hercules) Support	0
0	Compatibility-Mode (CGA) Support	0

This register contains a number of miscellaneous control bits.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7	**CRT Controller Timing Logic Enable:** When this bit is: • 0, CRT controller timing logic is disabled, forcing a reset condition. • 1, CRT controller timing logic is enabled and functions normally.
6	**Byte/Word Address Mode Control:** When this bit is: • 0, the Word Address mode is enabled. — In this case, before the contents of the CRT Controller Address Counter are sent to display memory, they are rotated left one bit position. • 1, the Byte Address mode is enabled. — In this case, the contents of the CRT Controller Address Counter are not rotated before they are sent to display memory.
5	**Address Rotation:** • When CR17[6] is 0 *and* this bit is: — 0, the left rotation described in CR17[6] above involves 14 bits of the CRT Controller Address Counter. — 1, the left rotation described in CR17[6] above involves 16 bits of the CRT Controller Address Counter. • When CR17[6] is 1, this bit is ignored.
4	**Reserved**

9.25 CR17: CRT Controller Mode Control Register

Bit	Description
3	**Count by Two:** When this bit is: • 0, the CL-GD7556 clocks the Memory Address Counter with the character clock. • 1, the CL-GD7556 clocks the Memory Address Counter with the character clock, divided by two.
2	**Multiply Vertical Registers by Two:** When this bit is: • 0, the Scanline Counter is clocked with Horizontal Sync. — As a result, the number of scanlines is 1024. • 1, the Scanline Counter is clocked with Horizontal Sync, divided by two. (In effect, the Vertical registers are multiplied by two.) — This division by two allows the number of scanlines to be doubled to 2048. — All periods become even multiples of two scanlines.
1	**Compatibility-Mode (Hercules) Support:** When this bit is: • 0, Scanline Counter bit 1 is substituted for CRT Controller Address Counter bit 14. This substitution provides for Hercules™ compatibility. • 1, the substitution described above does not occur. **NOTE:** The Cirrus Logic VGA BIOS does not support Hercules™ compatibility.
0	**Compatibility-Mode (CGA) Support:** When this bit is: • 0, Scanline Counter bit 0 is substituted for CRT Controller Address Counter bit 14. This substitution provides for CGA compatibility. • 1, the substitution described above does not occur.

9.26 CR18: Line Compare Register

I/O Port Address: 3?5

Index: 18

Bit	Description	Reset State
7	Line Compare [7]	0
6	Line Compare [6]	0
5	Line Compare [5]	0
4	Line Compare [4]	0
3	Line Compare [3]	0
2	Line Compare [2]	0
1	Line Compare [1]	0
0	Line Compare [0]	0

This register contains the least-significant 8 bits of the 10-bit Line Compare field.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit **Description**

7:0 **Line Compare [7:0]:**
The 10-bit Line Compare field is used to implement a vertically split screen by specifying where Screen A ends and Screen B starts.
- Bit 9, the most-significant bit, is in CRT Controller register CR9[6].
- Bit 8 is in CRT Controller register CR7[4]. This bit can always be written.
- Bits [7:0], the least-significant 8 bits of this field, are in this register.

Register Format for 10-Bit Line Compare

CR9[6]	CR7[4]	CR18[7:0]	
9	8	7	0

The top portion of the split screen is called Screen A.
- Screen A can start anywhere in display memory.
- Screen A can be panned and scrolled on a pixel-by-pixel basis.

The bottom portion of the split screen is called Screen B.
- Screen B always starts at location 0 in display memory.
- Screen B cannot be panned or scrolled.

9.27 CR22: Graphics Controller Data Latch Readback Register

I/O Port Address: 3?5

Index: 22

Bit	Description	Reset State
7	Graphics Controller Data Latch *n* Readback [7]	0
6	Graphics Controller Data Latch *n* Readback [6]	0
5	Graphics Controller Data Latch *n* Readback [5]	0
4	Graphics Controller Data Latch *n* Readback [4]	0
3	Graphics Controller Data Latch *n* Readback [3]	0
2	Graphics Controller Data Latch *n* Readback [2]	0
1	Graphics Controller Data Latch *n* Readback [1]	0
0	Graphics Controller Data Latch *n* Readback [0]	0

This register address is used to read the graphics controller data latches.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7:0	**Graphics Controller Data Latch *n* Readback [7:0]:** This read-only register is used to read back the contents of one of the four VGA graphics controller display memory data latches. • The number *n* of the display memory data latch that is read back is selected with Graphics Controller register GR4[1:0]. • The graphics controller data latches are loaded whenever display memory is read by the host CPU.

9.28 CR24: Attribute Controller Toggle Readback Register

I/O Port Address: 3?5

Index: 24

Bit	Description	Reset State
7	Attribute Controller Data/Index Toggle Readback	0
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

This read-only register provides access to the attribute controller toggle readback.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7	**Attribute Controller Data-Index Toggle Readback:** When this bit is: • 0, on the next access, the attribute controller reads or writes an index value. • 1, on the next access, the attribute controller reads or writes a data value.
6:0	**Reserved**

9.29 CR26: Attribute Controller Index Readback Register

I/O Port Address: 3?5

Index: 26

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Attribute Controller ARX[5] Readback	0
4	Attribute Controller Index Readback [4]	0
3	Attribute Controller Index Readback [3]	0
2	Attribute Controller Index Readback [2]	0
1	Attribute Controller Index Readback [1]	0
0	Attribute Controller Index Readback [0]	0

This read-only register provides access to the current attribute controller index.

NOTE: For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

Bit	Description
7:6	**Reserved**
5	**Attribute Controller ARX[5] Readback:** This bit reads back the value in Attribute Controller register bit ARX[5].
4:0	**Attribute Controller Index Readback [4:0]:** This field reads back the value in Attribute Controller register bits ARX[4:0].

10. GRAPHICS CONTROLLER REGISTERS

The registers in this chapter apply to CRT monitors.

10.1 GRX: Graphics Controller Index Register

I/O Port Address: 3CE

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Graphics Controller Index [5]	0
4	Graphics Controller Index [4]	0
3	Graphics Controller Index [3]	0
2	Graphics Controller Index [2]	0
1	Graphics Controller Index [1]	0
0	Graphics Controller Index [0]	0

This index register is used to specify the register in the Graphics Controller block to be accessed by the next I/O read or I/O write to I/O port address 3CF.

Bit	Description
7:6	Reserved
5:0	Graphics Controller Index [5:0]: This field specifies an index value for a particular Graphics Controller register that is accessed by the next I/O read or I/O write to I/O port address 3CF. When the value in this field is: • Less than or equal to 8, the index points to a Graphics Controller register in this chapter. • Greater than 8, the index points to an extension Graphics Controller register in the Extension registers of Chapter 12.

10.2 GR0: Display Memory Plane Set / Reset Register

I/O Port Address: 3CF

Index: 0

Bit	Description	Reset State
7	Write Mode 5 Background Color [7] / Reserved	0
6	Write Mode 5 Background Color [6] / Reserved	0
5	Write Mode 5 Background Color [5] / Reserved	0
4	Write Mode 5 Background Color [4] / Reserved	0
3	Write Mode 5 Background Color [3] / Display Memory Plane 3 Set/Reset	0
2	Write Mode 5 Background Color [2] / Display Memory Plane 2 Set/Reset	0
1	Write Mode 5 Background Color [1] / Display Memory Plane 1 Set/Reset	0
0	Write Mode 5 Background Color [0] / Display Memory Plane 0 Set/Reset	0

This register specifies:

- Background color bits [7:0], when Extended Write mode 5 is selected. (For a description of color expansion and Extended Write modes, refer to the *CL-GD7556 Software Reference Manual*.)
- Values to be written into the corresponding display memory planes, when the host CPU executes a Write mode 0 or Write mode 3 operation. (For an overview of the Write modes, refer to the description in Graphics Controller register GR5.)

Bit	Description
7:0	**Write Mode 5 Background Color [7:0]:** When GR5[2:0] is programmed to '101' (for Extended Write mode 5) *and* Extension register GRB[2] is set to: • 0, bits GR0[7:0] specify background color bits [7:0] (that is, Background Color byte 0) for Extended Write mode 5 and for BitBLTs that use color expansion. • 1, bits GR0[7:0] specify the least-significant background color bits [7:0] (that is, Background Color byte 0) and Extension register bits GR10[7:0] specify the most-significant background color bits [15:8] (that is, Background Color byte 1) for Extended Write mode 5 and for BitBLTs that use color expansion.
7:4	**Reserved:** • When GR5[2:0] is not programmed to '101', bits GR0[7:4] are not used. • When Extension register GRB[2] is: — 0, writes to bits GR0[7:4] are ignored, and reads return zeroes. — 1, bits GR0[7:4] are read/write, but bit contents are not used.
3:0	**Display Memory Plane [3:0] Set/Reset:** When Extension register SR7[0] is set to: • 0, *and* GR5[2:0] is not programmed to '101' (for Extended Write mode 5) *and* any bit or bits in the field GR1[3:0] is: — 0, the corresponding bit value from the CPU data bus is written into the corresponding display memory plane for Write mode 3 and Write mode 0. — 1, the corresponding bit value in GR0[3:0] is written into the corresponding display memory plane for Write mode 3 and Write mode 0. • 1, the set/reset logic function for display memory is disabled, and both GR0 and GR1 function only as color registers.

10.3 GR1: Display Memory Plane Set / Reset Enable Register

I/O Port Address: 3CF

Index: 1

Bit	Description	Reset Stat
7	Write Modes 4, 5 Foreground Color [7] / Reserved	0
6	Write Modes 4, 5 Foreground Color [6] / Reserved	0
5	Write Modes 4, 5 Foreground Color [5] / Reserved	0
4	Write Modes 4, 5 Foreground Color [4] / Reserved	0
3	Write Modes 4, 5 Foreground Color [3] / Disp. Memory Plane 3 Set/Reset Enable	0
2	Write Modes 4, 5 Foreground Color [2] / Disp. Memory Plane 2 Set/Reset Enable	0
1	Write Modes 4, 5 Foreground Color [1] / Disp. Memory Plane 1 Set/Reset Enable	0
0	Write Modes 4, 5 Foreground Color [0] / Disp. Memory Plane 0 Set/Reset Enable	0

This register specifies:

- Foreground color bits [7:0], when Extended Write mode 4 or 5 is selected. (For a description of color expansion and Extended Write modes, refer to the *CL-GD7556 Software Reference Manual*.)
- Values to be written into the corresponding display memory planes, when the host CPU executes a Write mode 0 operation. (For an overview of the Write modes, refer to the description in Graphics Controller register GR5.)

Bit	Description
7:0	**Write Modes 4, 5 Foreground Color [7:0]:** When GR5[2:0] is programmed either to '100' (for Extended Write mode 4) or to '101' (for Extended Write mode 5), *and* Extension register GRB[2] is set to: • 0, bits GR1[7:0] specify foreground color bits [7:0] (that is, Foreground Color byte 0) for Extended Write mode 4 or 5 and for BitBLTs that use color expansion. • 1, bits GR1[7:0] specify the least-significant foreground color bits [7:0] (that is, Foreground Color byte 0) and Extension register bits GR11[7:0] specify the most-significant foreground color bits [15:8] (that is, Foreground Color byte 1) for Extended Write mode 4 or 5 and for BitBLTs that use color expansion.
7:4	**Reserved:** • When GR5[2:0] is not programmed to '100' or to '101', bits GR1[7:4] are reserved. • When Extension register GRB[2] is: — 0, writes to bits GR1[7:4] are ignored, and reads return zeroes. — 1, bits GR1[7:4] are read/write, but bit contents are not used.
3:0	**Display Memory Plane [3:0] Set/Reset Enable:** When Extension register SR7[0] is set to: • 0 *and* GR5[2:0] is not programmed either to '100' (for Extended Write mode 4) or to '101' (for Extended Write mode 5), *and* any bit in the field GR1[3:0] is: — 0, the corresponding bit value from the CPU data bus is written into the corresponding display memory plane for Write mode 0. — 1, the corresponding bit value in GR0[3:0] is written into the corresponding display memory plane for Write mode 0. • 1, the set/reset logic function for display memory is disabled, and both GR0 and GR1 function only as color registers.

10.4 GR2: Color Compare Register

I/O Port Address: 3CF

Index: 2

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Color Compare Plane [3]
2	Color Compare Plane [2]
1	Color Compare Plane [1]
0	Color Compare Plane [0]

This register specifies the color compare value for Read mode 1. (For an overview of the Read modes, refer to the description in Graphics Controller register GR5.)

Bit	Description
7:4	Reserved
3:0	Color Compare Plane [3:0]: • When a Read mode 1 occurs (that is, GR5[3] is set to 1), these 4 bits are compared with each of 8 bits from the corresponding display memory planes under the mask in GR7. • For display memory planes that are not chosen (that is, the corresponding bit in GR7[3:0] is 0), their data is forced to match the values of the other display memory planes, becoming a ‘don’t care’ in the process.

10.5 GR3: Data Rotate Register

I/O Port Address: 3CF

Index: 3

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Logical Function Select [1]	0
3	Logical Function Select [0]	0
2	Data Rotate Count [2]	0
1	Data Rotate Count [1]	0
0	Data Rotate Count [0]	0

This register contains two fields that are used with Write modes 0 and 3. (For an overview of the Write modes, refer to the description in Graphics Controller register GR5.)

Bit — Description

7:5 — Reserved

4:3 — Logical Function Select [1:0]:

- This 2-bit field is used only when Write mode 0 is selected (that is, Graphics Controller register GR5[2:0] is programmed to '000'). This field:
  - — Selects the logical function operation that occurs between the following: (1) the data in the host CPU data latches and (2) either the data from the host CPU or the set/reset logic (as determined by GR0[3:0] and GR1[3:0]).
  - — The result of the functional operation is written into display memory.
- The logical function operations are summarized in the following table:

GR3 [4]	GR3 [3]	Logical Function Operation
0	0	None: The data in the latches are ignored.
0	1	Data in latches is logically AND'ed with data from CPU or set/reset logic
1	0	Data in latches is logically OR'ed with data from CPU or set/reset logic
1	1	Data in latches is logically XOR'ed with data from CPU or set/reset logic

2:0 — Data Rotate Count [2:0]:

This 3-bit field allows data from the host CPU bus to be rotated to the right up to 7 bit positions prior to being altered by the set/reset logic of GR0[3:0] and GR1[3:0]).

- The bit setting:
  - — '000' (the default) does not rotate data from the host CPU bus.
  - — '111' rotates the data 7 bit positions to the right.
- When host CPU data is rotated, this rotation occurs before any other operations (including set/reset operations) are performed on the data, and before it is sent to display memory.

10.6 GR4: Display Memory Plane Select Register

I/O Port Address: 3CF

Index: 4

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Display Memory Plane Select [1]	0
0	Display Memory Plane Select [0]	0

This register is used to select a display memory plane for Read mode 0. (For an overview of the Write modes, refer to the description in Graphics Controller register GR5.)

Bit	Description
7:2	Reserved
1:0	Display Memory Plane Select [1:0]: This 2-bit field is used only when Read mode 0 is selected (that is, Graphics Controller register GR5[3] is set to 1). This field selects a display memory plane for a read by Read mode 0, as shown in the following table:

GR4		Display Memory Plane Selected for Read by Read Mode 0
[1]	[0]	
0	0	Display Memory Plane 0
0	1	Display Memory Plane 1
1	0	Display Memory Plane 2
1	1	Display Memory Plane 3

10.7 GR5: Graphics Controller Mode Control Register

I/O Port Address: 3CF

Index: 5

Bit	Description	Reset State
7	Reserved	
6	256-Color Graphics Display Mode	0
5	Graphics Data Shift Register Mode	0
4	Odd/Even Addressing Mode	0
3	Read Mode	0
2	Write Mode Select [2]	0
1	Write Mode Select [1]	0
0	Write Mode Select [0]	0

This register specifies the Write mode and Read mode. In addition, it controls the configuration of the graphics data shift registers.

Bit	Description
7	Reserved
6	256-Color Graphics Display Mode: When this bit is: • 0, graphics data shift registers are configured for 16-, 4-, or 2-color graphics display modes. • 1, graphics data shift registers are configured for 256-color graphics display modes, and GR5[5] is ignored.
5	Graphics Data Shift Register Mode: When this bit is: • 0, graphics data shift registers are configured for EGA compatibility. • 1, graphics data shift registers are configured for CGA compatibility, which is used for graphics display modes 4 and 5.
4	Odd/Even Addressing Mode: When this bit is: • 0, this function is disabled. • 1, the CL-GD7556 is configured for odd/even addressing mode. • This bit must always be programmed to the opposite value of Sequencer register bit SR4[2].

10.7 GR5: Graphics Controller Mode Control Register (Reg.)

Bit — Description

3 — **Read Mode:**
This bit specifies whether the CL-GD7556 is in Read mode 0 or Read mode 1.

GR5[3]	Read Mode	CPU Read Source
0	Read mode 0	CPU reads data directly from display memory
1	Read mode 1	CPU reads data that results from the color-compare logic of GR2

Read Mode 0:
- During Read mode 0, the host CPU reads data directly from display memory.
- Read mode 0 returns an adjacent 8 bits of the display memory plane specified in GR4[1:0].
- Read mode 0 does *not* use the color-compare logic of GR2.
- Read mode 0 can be forced with an I/O read of CRT Controller register CR22.

Read Mode 1:
- During Read mode 1, the host CPU reads data that results from the color-compare logic of Graphics Controller register GR2[3:0].
- Read mode 1 allows eight adjacent pixels (in 16-color modes) to be compared to a specified color value in a single operation. Each of the 8 bits returned to the host CPU indicates the result of a comparison between the 4 bits of the Color Compare (GR2[3:0]) and the bits from the four display memory planes.
- When any bit of the 4-bit Color Compare operation of GR2[3:0] matches its corresponding bit from the four display memory planes, a 1 is returned for the corresponding bit position.
- When any bit in GR7[3:0] is 0, the value in the corresponding display memory plane is forced to match the values of the other planes, becoming a ‘don’t care’ in the process.

10.7 GR5: Graphics Controller Mode Control Register (cont.)

Bit	Description
2:0	**Write Mode Select [2:0]:** These bits, in combination with Extension register bit GRB[2], specify when the CL-GD7556 is in Write or Extended Write mode. When GRB[2] is: • 0, GR5[2] is forced to 0. • 1, GR5[2] is enabled to be written to either 0 or 1.

GRB[2]	GR5 [2]	GR5 [1]	GR5 [0]	Write Mode Selected
When GRB[2] is 0, GR5[2] is forced to 0.	0	0	0	Write mode 0
	0	0	1	Write mode 1
	0	1	0	Write mode 2
	0	1	1	Write mode 3
GRB[2] must be 1 for GR5[2] to be set to 1.	1	0	0	Extended Write mode 4
	1	0	1	Extended Write mode 5
	1	1	0	Reserved
	1	1	1	Reserved

Write Mode 0:

- Each of the four display memory planes is written with the host CPU data rotated by the number of counts in Graphics Controller register GR3[2:0].
- When Extension register bit SR7[0] is:
  - 0 *and* a bit in Graphics Controller register GR1[3:0] is:
    - 0, the corresponding display memory plane is written with the contents of the corresponding value from the host CPU.
    - 1, the corresponding display memory plane is written with the contents of the corresponding bit in GR0[3:0].
  - 1, the corresponding display memory plane is written with the contents of the corresponding host CPU value, regardless of GR1[3:0].
- Under the control of GR3[4:3], the contents of host CPU data latches can be logically combined with data from the set/reset logic of GR0[3:0] and GR1[3:0].
  - Bit planes are enabled with Sequencer register SR2[3:0].
  - Bit positions are enabled with Graphics Controller register GR8.

NOTE: Write Mode 0 does not support By-8 addressing.

Write Mode 1:

- Each of the four display memory planes is written with data in host CPU data latches, loaded from display memory by a previous read.
- Write mode 1 ignores Graphics Controller register GR8.

NOTE: Write Mode 1 does not support By-8 addressing.

10.7 GR5: Graphics Controller Mode Control Register (cont.)

Bit	Description
2:0 *(cont.)*	**Write Mode 2:** • Display memory planes [3:0] are written with host CPU data values [3:0]. The four data values are replicated eight times each, to write up to eight adjacent pixels. • Bit planes are enabled with Sequencer register SR2[3:0]. • Bit positions are enabled with Graphics Controller register GR8. • Write mode 2 ignores these fields: — Data rotator (GR3[2:0]) — Set/reset (GR0[3:0] and GR1[3:0]) — Logical function select (GR3[4:3]) **Write Mode 3:** • Display memory plane data comes from corresponding bits of GR0[3:0]. • The bit-position-enable field is formed with the logical AND of Graphics Controller register GR8 and the rotated host CPU data. • Write mode 3 ignores the logical function select (GR3[4:3]) **Extended Write Mode 4:** • This mode can be used for 256-color or 64K-color text expansion for which the background is to be preserved. • The contents of Graphics Controller registers GR1[7:0] and GR11[7:0] are written into up to eight adjacent pixels per byte of source data. • The host CPU data bits are used to control whether a pixel is written. When a CPU data bit is: — 0, the corresponding pixel is not changed. — 1, the corresponding pixel is written. **Extended Write Mode 5:** • This mode is intended for 256-color or 64K-color text expansion, for which both the foreground and background are to be written. • Depending on the setting of Extension register bits GRB[2,4], the contents of either (1) Graphics Controller register GR0[7:0] and Extension register GR10[7:0], *or* (2) Graphics Controller register GR1[7:0] and Extension register GR11[7:0] are written into each of eight adjacent pixels per byte of source data. • For each of the 8/16 pixels, the choice between either GR0/GR10 or GR1/GR11 is made according to the value of the corresponding bit of the host CPU data, summarized in the following table.

Host CPU Data	GR0/GR10 or GR1/GR11
0	GR0/GR10 (Background)
1	GR1/GR11 (Foreground)

10.8 GR6: Miscellaneous Register

I/O Port Address: 3CF

Index: 6

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Display Memory Map [1]	0
2	Display Memory Map [0]	0
1	Chain Odd Maps to Even	0
0	Graphics Display Mode Enable	0

This register contains miscellaneous control bits.

Bit — Description

7:4 — Reserved

3:2 — Display Memory Map [1:0]:
This field specifies the beginning address and size of the display memory in the host CPU address space. This field is summarized in the following table:

GR6 [3]	GR6 [2]	Display Memory Map Plane	Display Memory Address in Host CPU Address Space (hex)	Display Memory Size (Kbytes)	Affected Mode(s)
0	0	0	A000:0 to BFFF:F	128	Extended
0	1	1	A000:0 to AFFF:F	64	EGA / VGA
1	0	2	B000:0 to B7FF:F	32	Hercules™
1	1	3	B800:0 to BFFF:F	32	CGA

NOTE: The Cirrus Logic VGA BIOS does not support Hercules™ compatibility.

1 — Chain Odd Maps to Even:
- When this bit is 1, host CPU Address bit AD[0] is replaced with a higher-order address bit. As a result of this replacement, when a host CPU address is:
  - — 'Even', it accesses Display Memory Plane Select bits 0 and 2.
  - — 'Odd', it accesses Display Memory Plane Select bits 1 and 3.
- This mode is useful for MDA emulation.

0 — Graphics Display Mode Enable:
When this bit is:
- 0, the CL-GD7556 functions in text (alphanumeric) display modes.
- 1, the CL-GD7556 functions in graphics (all-points-addressable) display modes.

10.9 GR7: Color Don't-Care Plane Register

I/O Port Address: 3CF

Index: 7

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Don't-Care Plane [3]	0
2	Color Don't-Care Plane [2]	0
1	Color Don't-Care Plane [1]	0
0	Color Don't-Care Plane [0]	0

This register is used with Graphics Controller register GR2 for Read mode 1 accesses. (For an overview of the Read modes, refer to the description in Graphics Controller register GR5.)

Bit	Description
7:4	Reserved
3:0	Color Don't-Care Plane [3:0]: These 4 bits are used to control color compare logic for the four Color Don't-Care Planes. When a bit is: • 0, the corresponding display memory plane is not involved in color compares. • 1, the corresponding display memory plane is involved in color compares.

10.10 GR8: Display Memory Bit Mask Register

I/O Port Address: 3CF

Index: 8

Bit	Description	Reset State
7	Display Memory Bit Write Enable [7]	0
6	Display Memory Bit Write Enable [6]	0
5	Display Memory Bit Write Enable [5]	0
4	Display Memory Bit Write Enable [4]	0
3	Display Memory Bit Write Enable [3]	0
2	Display Memory Bit Write Enable [2]	0
1	Display Memory Bit Write Enable [1]	0
0	Display Memory Bit Write Enable [0]	0

This register is used to control writing to display memory on a bit basis in Write modes 0, 2, and 3.

Bit	Description
7:0	Display Memory Bit Write Enable [7:0]: Each bit in this register controls whether the corresponding bit in a display memory plane is written in Write modes 0, 2, or 3 as selected by GR5[2:0]. When a bit in this register is: • 0, the corresponding bit in a display memory plane is not written. As a result: — The least-significant bit of this register corresponds to the far-right pixel. — The most-significant bit of this register corresponds to the far-left pixel. — When all bits in this register are set to 0, writing data has no effect in display memory because all bits are masked out. — This write protection is only in relation to a read-modify-write sequence. • 1, the corresponding bit in a display memory plane is written.

Notes

11. ATTRIBUTE CONTROLLER REGISTERS

NOTE: The registers in this chapter apply to CRT monitors.

11.1 ARX: Attribute Controller Index Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	AR11 Video Source Enable	0
4	Attribute Controller Index [4]	0
3	Attribute Controller Index [3]	0
2	Attribute Controller Index [2]	0
1	Attribute Controller Index [1]	0
0	Attribute Controller Index [0]	0

This register is used to specify the register in the Attribute Controller block that is accessed with the next I/O write to 3C0 or I/O read to 3C1.

For the Attribute Controller block, both the index and data registers are at the same port addresses, unlike other blocks, for which index and data registers are at different port addresses.

Alternate writes to ARX toggle between index and data. The CRT Controller register bit CR24[7] provides a status of whether an index value or a data value is selected.

Bit	Description
7:6	**Reserved**
5	**AR11 Video Source Enable:** When this bit is: • 0, the screen displays the color in Attribute Controller register AR11. • 1, the screen displays normal video.
4:0	**Attribute Controller Index [4:0]:** This field is the index to the Attribute Controller data registers. When CRT Controller register bit CR24[7] = 0, the CRT Controller register bits CR26[4:0] read back these index bits.

11.2 AR0–ARF: Attribute Controller Palette Registers

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 0–F

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Secondary Red	0
4	Secondary Green / Intensity	0
3	Secondary Blue / Monochrome	0
2	Red	0
1	Green	0
0	Blue	0

These bits act as pointers to palette entries.

Bit	Description
7:6	**Reserved**
5:0	**Palette Entries:** In 16-color text and graphics display modes, the digital attribute controller palette entries in this register are chosen by the four bits of pixel data, and they point to palette memory entries. • The palette memory entries are normally programmed so that DAC outputs reflect these values. • As a result, palette memory is programmed to simulate standard EGA colors.

11.3 AR10: Attribute Controller Mode Control Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 10

Bit	Description	Reset State
7	AR14 Video Source Enable	0
6	Pixel Double-Clock Select	0
5	Pixel Panning Compatibility	0
4	Reserved	
3	Character Blink Enable	0
2	Line Graphics Enable	0
1	Display Type	0
0	Graphics Display Mode Enable	0

This register contains some miscellaneous control bits for the Attribute Controller.

Bit	Description
7	**AR14 Video Source Enable:** • When an 8-, 16-, or 24-bit pixel mode is chosen, this bit is ignored. • When this bit is: — 0, Attribute Controller register bits AR0[5:4]–ARF[5:4] are the source for the CLUT address bits [5:4]. — 1, Attribute Controller register bits AR14[1:0] are the source for CLUT address bits [5:4], which allows rapid selection of four 16-color palettes.
6	**Pixel Double-Clock Select:** When this bit is: • 0, pixels are clocked on every cycle. • 1, pixels are clocked on every other clock cycle. Also: — Attribute Controller registers AR0–ARF are bypassed. — This bit setting is used with graphics mode 13h. — The CL-GD7556 sequencer logic operates at twice the pixel clock rate.
5	**Pixel Panning Compatibility:** When this bit is: • 0, the two parts of a split screen pan together. • 1, a line compare match in the CRT Controller forces the output of Attribute Controller register bits AR13[3:0] to a 0h until the next Vertical Sync occurs. This action allows the panning of Screen A without panning Screen B.
4	**Reserved**
3	**Character Blink Enable:** When this bit is: • 0, character blinking is disabled. • 1, character blinking is enabled at the frequency rate of vertical refresh, divided by 32.

11.3 AR10: Attribute Controller Mode Control Register *(cont.)*

Bit | **Description**

2 — **Line Graphics Enable:**
When this bit is:
- 0, bit 9 of a 9-bit-wide character cell is the same as the background.
- 1, bit 9 of a 9-bit-wide character cell is made the same value as bit 8. This value is used for those character sets that have special characters associated with line graphics, for characters codes in the range C0h through DFh.

1 — **Display Type:**
This bit is used only when the CL-GD7556 is in text display mode. When this bit is:
- 0, the Attribute Byte contents are treated as color attributes.
- 1, the Attribute Byte contents are treated as MDA-compatible attributes.

The following table shows examples of monochrome attributes.

Bit Definitions for Attribute Byte								Hex Code of Attribute Byte	Monochrome Attribute Byte
Blink Bit	Background Bits			Intensity Bit	Foreground Bits				
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]		
0	0	0	0	0	1	1	1	07h	Normal
0	0	0	0	1	1	1	1	0Fh	Intense
0	0	0	0	0	0	0	1	01h	Underline
0	0	0	0	1	0	0	1	09h	Underline Intense
0	1	1	1	0	0	0	0	70h	Reverse
1	1	1	1	0	0	0	0	F0h	Blinking Reverse

0 — **Graphics Display Mode Enable:**
When this bit is:
- 0, the attribute controller functions in text display modes (which are also called ‘alphanumeric’ display modes).
- 1, the attribute controller functions in graphics display modes (which are also called ‘all-points-addressable’ display modes).

11.4 AR11: Overscan (Border Color) Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 11

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	(Border Color) Secondary Red	0
4	(Border Color) Secondary Green	0
3	(Border Color) Secondary Blue	0
2	(Border Color) Red	0
1	(Border Color) Green	0
0	(Border Color) Blue	0

This register points to the entry in the CLUT (Color Look-up Table) that defines the border color.

- As shown in Figure 9-1 on page 9-3 at the description of CRT Controller register CR0, the border is defined as that portion of the raster between blanking and active video, on all four sides of the screen.
- Typically, the CLUT entries are programmed so that the color defined by the bits in this register is the color that results.

Bit	Description
7:6	**Reserved**
5:0	**Border Color [5:0]:** These bits are used to select the CLUT entry for the border color in CGA and EGA modes. • When the mode in use is a: — CGA mode, 4 bits (AR11 [3:0]) are used to select the CLUT entry for the border color. — EGA mode, 6 bits (AR11 [5:0]) are used to select the CLUT entry for the border color. • For overscan color protection, refer to Extension register SR12[7].

11.5 AR12: Color-Plane Enable Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 12

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Diagnostic Status Multiplexor [1]	0
4	Diagnostic Status Multiplexor [0]	0
3	Color-Plane Enable [3]	0
2	Color-Plane Enable [2]	0
1	Color-Plane Enable [1]	0
0	Color-Plane Enable [0]	0

This register contains:

- One field that chooses the inputs for diagnostic bits in External/General register STAT[5:4].
- Another field that enables the 4 color planes in Attribute Controller registers AR0–ARF.

Bit **Description**

7:6 **Reserved**

5:4 **Diagnostic Status Multiplexor [1:0]:**
This field chooses the Attribute Controller inputs for the diagnostic status bits in External/General register bits STAT[5:4] as indicated in the following table. (The Pixel bus is a bus that is internal to the CL-GD7556.)

AR12		STAT	
[5]	[4]	[5]	[4]
0	0	Pixel Bus Bit [2] (Red)	Pixel Bus Bit [0] (Blue)
0	1	Pixel Bus Bit [5] (Secondary Red)	Pixel Bus Bit [4] (Secondary Green)
1	0	Pixel Bus Bit [3] (Secondary Blue)	Pixel Bus Bit [1] (Green)
1	1	Pixel Bus Bit [7]	Pixel Bus Bit [6]

11.5 AR12: Color-Plane Enable Register *(cont.)*

Bit	Description
3:0	**Color-Plane Enable [3:0]:** This field controls which display memory plane sends data to a corresponding Attribute Controller register (that is, AR0–ARF, the color palette registers), as shown in the following table:

AR12	AR12 Bit State	Result
[3]	0	Display Memory Plane 3 disabled.
	1	Display Memory Plane 3 data selected for Color Palette register 3.
[2]	0	Display Memory Plane 2 disabled.
	1	Display Memory Plane 2 data selected for Color Palette register 2.
[1]	0	Display Memory Plane 1 disabled.
	1	Display Memory Plane 1 data selected for Color Palette register 1.
[0]	0	Display Memory Plane 0 disabled.
	1	Display Memory Plane 0 data selected for Color Palette register 0.

11.6 AR13: Pixel Panning Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 13

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Pixel Panning [3]	0
2	Pixel Panning [2]	0
1	Pixel Panning [1]	0
0	Pixel Panning [0]	0

This register:

- Specifies the number of pixels that the display data are shifted to the left.
- Functions both in the graphics and text modes.

Bit	Description
7:4	**Reserved**
3:0	**Pixel Panning [3:0]:** This field controls fine panning on a pixel-by-pixel basis by specifying the number of pixels the display data are shifted to the left. (For coarse panning, refer to CRT Controller register bits CR8[6:5].) AR13[3:0] programmed values are interpreted as indicated in the following table:

AR13				Hex Code	Shift for 9-Bit Characters	Shift for 8-Bit Characters	Shift for Display Mode 13h
[3]	[2]	[1]	[0]				
0	0	0	0	0h	1 bit left	No shift	No shift
0	0	0	1	1h	2 bits left	1 bit left	–
0	0	1	0	2h	3 bits left	2 bits left	1 bit left
0	0	1	1	3h	4 bits left	3 bits left	–
0	1	0	0	4h	5 bits left	4 bits left	2 bits left
0	1	0	1	5h	6 bits left	5 bits left	–
0	1	1	0	6h	7 bits left	6 bits left	3 bits left
0	1	1	1	7h	8 bits left	7 bits left	–
1000 to 1111				8h - Fh	No shift	1 bit right	–

11.7 AR14: Color Select Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 14

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Bit C [7]	0
2	Color Bit C [6]	0
1	Color Bit C [5]	0
0	Color Bit C [4]	0

This register contains two fields that are involved in the selection of addresses into the CLUT.

Bit	Description
7:4	**Reserved**
3:2	**Color Bits C [7:6]:** • In 8-, 16-, and 24-bit pixel modes, these bits are ignored. • These 2 bits are concatenated with the 6 bits from AR0–ARF to form the address into the CLUT.
1:0	**Color Bits C [5:4]:** • In 8-, 16-, and 24-bit pixel modes, these bits are ignored. • When AR10[7] is: — 0, these 2 bits are ignored. — 1, these 2 bits replace the corresponding 2 bits from AR0–ARF to form the address into the CLUT.

Notes

12. EXTENSION REGISTERS

The registers in this chapter apply to CRT monitors and flat panels.

NOTE: Within this chapter, some registers have a '?' in the I/O port address. This question mark implies a 'B' for Monochrome mode and 'D' for Color mode, depending on the setting of External/General register bit MISC[0].

12.1 SR6: Unlock All Extension Registers

I/O Port Address: 3C5

Index: 6

Bit	Description	Reset State
7	Not Used	Not applicable
6	Not Used	Not applicable
5	Not Used	Not applicable
4	Unlock All Extension Registers	1
3	Not Used	Not applicable
2	Unlock All Extension Registers	0
1	Unlock All Extension Registers	1
0	Unlock All Extension Registers	0

This register is used to enable or disable access to the CL-GD7556 Extension registers.

Bit	Description
7:5, 3	**Reserved**
4, 2:0	**Unlock All Extension Registers (Access Value):** All Extension registers are: • Unlocked (enabled) for read/write access when bits 4, 2:0 equal the following: — Bit 4 = 1 — Bit 2 = 0 — Bit 1 = 1 — Bit 0 = 0 • Locked (disabled) for read/write access when bits 4, 2:0 are any other value other than the ones shown above.

12.2 SR7: Extended Sequencer Mode Register

I/O Port Address: 3C5

Index: 7

Bit	Description	Reset State
7	Display Memory Segment Select [3]	0
6	Display Memory Segment Select [2]	0
5	Display Memory Segment Select [1]	0
4	Display Memory Segment Select [0]	0
3	CRT Controller Character Clock Divider [2] Select	0
2	CRT Controller Character Clock Divider [1] Select	0
1	CRT Controller Character Clock Divider [0] Select	0
0	High-Resolution Packed-Pixel Mode Select	0

This register has several functions which are identified in the following bit descriptions.

Bit **Description**

7:4 **Display Memory Segment Select [3:0]:**
When the value of this 4-bit field is programmed to:

- '0000':
  - — The CL-GD7556 is configured for standard VGA segmented addressing of display memory, responding to memory accesses at Axxx:x, or Bxxx:x, or both, as specified by Graphics Controller register bits GR6[3:2].
- Other than '0000':
  - — The contents of the PCI Base Address register specify the beginning of the 16-Mbyte area assigned for display memory. The CL-GD7556 responds to all 16 Mbytes as four 4-Mbyte byte-swapping apertures that are selected by host CPU address bits AD[23:22].
  - — The CL-GD7556 is configured for up to 4 Mbytes of linear memory addressing.

  NOTE: In linear memory addressing, Extension registers GR9 (Display Memory Offset 0) and GRA (Display Memory Offset 1) can be used.
- Other than '0000' *and*:
  - — There are 4 Mbytes of display memory installed *and* the CL-GD7556 is configured for extended 256-color Chain-4 addressing, then the 4-Mbyte address range has one-to-one mapping to the 4 Mbytes of installed display memory.
  - — There is 1 Mbyte of display memory installed *and* the CL-GD7556 is configured for unchained, By-8, or By-16 addressing, then the CL-GD7556 responds to the entire 1-Mbyte range, but address wrapping takes place.

12.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit **Description**

3:1 **CRT Controller Character Clock Divider Select [2:0]:**
This field selects how the CRT Controller Character Clock is divided down, resulting in various pixel data rates, as indicated in the following table:

SR7			Resulting Pixel Data
[3]	[2]	[1]	
0	0	0	8-bit/pixel data with 1× VCLK. Normal operation. (CRT Controller Character Clock is not divided down.)
0	0	1	For the CL-GD7556 this setting has the same affect as '011'.
0	1	0	24-bit/packed-pixel data with 1× VCLK (CRT Controller Character Clock is not divided down.)
0	1	1	16-bit/pixel data with 1× VCLK (CRT Controller Character Clock is not divided down.)
1	x	x	Reserved

SR7[3:1] is '010' (24-Bit/Packed-Pixel Data with 1× VCLK)
When this mode is selected:
- The DAC and the internal CL-GD7556 video shift registers are clocked at the VCLK pixel rate.
- The CRT Controller is clocked with a character clock of 8 pixels (8 VCLKs).

The above clocking allows:
- The CRT Controller timing value for 640 × 480 modes with 24-bit pixels to be programmed in units of an 8-pixel character clock.
- CRT Controller register CR13 to be set to display mode F0h or 71h.
- The hardware cursor to be supported in this configuration.

SR7[3:1] is '011' (16-Bit/Pixel Data with 1× VCLK)
When this mode is selected:
- The sequencer provides 16-bit data to the palette DAC at the displayed pixel data rate. This action allows RGB 5-5-5 color modes to be selected with a 1x VCLK.
- The data output on the VPY[7:0] pins is only the low byte of the pixel data. (In this case, the high byte of the pixel data is not available externally.)
- This mode provides for 1024 × 768 display modes, with either RGB 5-5-5 or RGB 5-6-5 color, and with the VCLK equal to the pixel data rate.
- This mode also provides for 1024 × 768 display modes, with RGB 5-5-5 color, and with the VCLK equal to the pixel data rate.
- The hardware cursor is supported.

12.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit	Description
0	**High-Resolution Packed-Pixel Mode Select:** When this bit is: • 0, the following standard VGA 256-color modes are supported: — Low-resolution text display modes. — For a graphics display mode 13h that is: — Low-resolution, program Attribute Controller register bit AR10[6] to 0. — High-resolution, program Attribute Controller register bit AR10[6] to 1. • 1, all display memory configured in Extension register SRF is available, and the CRT FIFO is 28 levels. This bit is must always be set to 1 for high-resolution packed-pixel mode. With this bit setting: — The CL-GD7556 internal video shift registers are configured so that one character clock equals 8 pixels. — Graphics Controller registers GR0 and GR1: — Function as color registers only. — Have their VGA set/reset function for display memory disabled. — This mode is used with 8-, 16-, and 24-bit packed-pixel modes. (Refer to SR7[3:1].) — True packed-pixel display memory addressing is enabled. **NOTE:** In true packed-pixel memory addressing, consecutive pixels are stored at consecutive addresses in display memory. In contrast, with Chain-4 memory addressing, consecutive pixels are stored at every fourth address in display memory.

12.3 SR8: DDC2B Control Register

I/O Port Address: 3C5

Index: 8

Bit	Description	Access	Reset State
7	DDCD Output Status	R	0
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	DDCC Output Status	R	0
1	DDCD Output Control	R/W	0
0	DDCC Output Control	R/W	0

This register provides DDC2B control.

NOTE: The V-Port function and pins, including DDCD (pin 104) and DDCC (pin 98), are activated when Extension register bit SR24[7] is 0.

Bit	Description
7	**DDCD Output Status:** The status of this bit determines when the DDCD pin is ready for the CL-GD7556 to drive it. When Extension register bit SR24[7] is 0 *and* this read-only bit reads a: • 0, the DDCD output is low. In this case, one of two conditions are possible: — The CL-GD7556 is pulling this bit low. — A peripheral on the bus is pulling down the DDCD bus signal. • 1, the DDCD output is high. In this case, there is no peripheral controlling the bus. Instead, an external bus-termination pull-up resistor is driving the bus high.
6:3	**Reserved**
2	**DDCC Output Status:** The status of this bit determines when the DDCC pin is ready for the CL-GD7556 to drive it. When Extension register bit SR24[7] is 0 *and* this read-only bit reads a: • 0, the DDCC output is low. In this case, one of two conditions is possible: — The CL-GD7556 is pulling this bit low. — A peripheral on the bus is pulling down the DDCC bus signal. • 1, the DDCC output is high. In this case, there is no peripheral controlling the bus. Instead, an external bus-termination pull-up resistor is driving the bus high.
1	**DDCD Output Control**: When SR24[7] is 0 *and* this bit is: • 0, DDCD output is low. • 1, DDCD output is off (that is, high-impedance).
0	**DDCC Output Control:** When SR24[7] is 0 *and* this bit is: • 0, DDCC output is low. • 1, DDCC output is off (that is, high-impedance).

12.4 SR9, SRA: Scratch Pad #0 and #1 Registers

I/O Port Address: 3C5

Index: 9, A

Bit	Description	Access	Reset State
7	Scratch Pad #0 and #1 [7]	R/W	0
6	Scratch Pad #0 and #1 [6]	R/W	0
5	Scratch Pad #0 and #1 [5]	R/W	0
4	Scratch Pad #0 and #1 [4]	R/W	0
3	Scratch Pad #0 and #1 [3]	R/W	0
2	Scratch Pad #0 and #1 [2]	R/W	0
1	Scratch Pad #0 and #1 [1]	R/W	0
0	Scratch Pad #0 and #1 [0]	R/W	0

These two registers are reserved for the exclusive use of the CL-GD7556 VGA BIOS and must never be written by any application program. They are listed here only for reference.

Bit	Description
7:0	**Reserved**

12.5 SRB, SRC, SRD, SRE: VCLK0,1,2,3 Numerator Registers

I/O Port Address: 3C5

Index: B, C, D, E

Bit	Description	Access	Reset State
7	Reserved		
6	VCLK Numerator [6]	R/W	See following table
5	VCLK Numerator [5]	R/W	See following table
4	VCLK Numerator [4]	R/W	See following table
3	VCLK Numerator [3]	R/W	See following table
2	VCLK Numerator [2]	R/W	See following table
1	VCLK Numerator [1]	R/W	See following table
0	VCLK Numerator [0]	R/W	See following table

These registers are used in combination with Extension registers SR1B to SR1E to establish the frequency of the four possible VCLK signals. The VCLK used is selected by External/General register bits MISC[3:2].

This register establishes the Numerator value. For information on Denominator and Post-Scalar values, refer to Section 12.16. For more information on clock options, refer to Appendix B.

VCLK2, which uses registers SRD and SR1D with MISC[3:2] = '10', is the default for flat panel operation.

Bit	Description
7	**Reserved**
6:0	**VCLK Numerator [6:0]:** These bits determine the Numerator value in the equation that is used to select the VCLK frequency. Each VCLK frequency is determined with the following calculation: $\text{DIVIDE:} \quad \frac{\text{OSC} \times \text{Numerator}}{\text{Denominator} \times (\text{Post-Scalar} + 1)}$ $\text{BY:} \quad \div$ TO OBTAIN: = VCLK*n* (MHz) where: VCLK*n* = VCLK frequency *n*, where *n* = 0, 1, 2, 3 OSC = Input clock frequency of 14.318 MHz Numerator = Value of register bits SRi [6:0], where *i* = B, C, D, E Denominator = Value of register bits SR1i [5:1], where *i* = B, C, D, E Post-Scalar = Value of register bits SR1i [0], where *i* = B, C, D, E If *n* = 0, then *i* = B. If *n* = 1, then *i* = C. If *n* = 2, then *i* = D. If *n* = 3, then *i* = E.

12.5 SRB, SRC, SRD, SRE: VCLK0,1,2,3 Numerator Registers *(cont.)*

The following table shows the reset values of the registers that determine the VCLK frequency. The table also shows the corresponding VCLK frequency at system reset.

VCLK*n* and Reset Frequency		Numerator			Denominator			Post-Scalar
VCLK*n*	VCLK*n* Frequency at System Reset (MHz)	Numerator Register and Its Hex Value		Numerator Value Used in Equation	Denominator Register and Its Hex Value		Denominator Value Used in Equation[a]	Post-Scalar Value Used in Equation
		Register (SRi)	Hex	Decimal Equivalent of Hex Value	Register (SR1i)	Hex	Decimal	Decimal
VCLK0	25.180	SRB	66h	102	SR1B	3Bh	29	1
VCLK1	28.325	SRC	5Bh	91	SR1C	2Fh	23	1
VCLK2[b]	41.165	SRD	45h	69	SR1D	30h	24	0
VCLK3	36.082	SRE	7Eh	126	SR1E	33h	25	1

[a] These values result from the Post-Scalar and are not the decimal equivalent of the hex values in the previous column.

[b] VCLK2 is the default for flat panel operation.

12.6 SRF: Display Memory Control Register

I/O Port Address: 3C5

Index: F

Bit	Description	Reset State
7	Display Memory Bank Select	0
6	Host CPU Write FIFO Fast-Page-Detection Mode Disable	0
5	Reserved	
4	Display Memory Data Bus Width [1]	1
3	Display Memory Data Bus Width [0]	1
2	Display Memory RAS# Cycle Select	0
1	Display Memory Configuration Symmetry	0
0	Display Memory Multiple-CAS# / Multiple-WE# Select	1

This register is used to control the display memory.

Bit **Description**

7 **Display Memory Bank Select:**
This bit is used with SRF[4:3] to specify the display memory data bus configuration according to the number of banks of display memory used. Since the CL-GD7556 supports only 64-bit wide display memory, bits SRF[4:3] are always set to the default setting of '11'.
When this bit is:

- 0, the CL-GD7556 is configured for one bank of display memory, which is controlled by RAS0#.
- 1, the CL-GD7556 is configured for two banks of display memory.
  - — RAS0# enables the DRAMs in the first bank.
  - — RAS1# enables the DRAMs in the second bank.

SRF			Display Memory Data Bus Width	Display Memory Organization	Total Display Memory
[7]	[4]	[3]			
0	1	1	64 bits wide	Two 128K x 32 DRAMs	1 Mbyte
				Four 256K × 16 DRAMs	2 Mbytes
1	1	1	64 bits wide (two banks)	Four 128K × 32 DRAMs	2 Mbytes

12.6 SRF: Display Memory Control Register *(cont.)*

Bit	Description
6	**Host CPU Write FIFO Fast-Page-Detection Mode Disable:** To avoid host CPU write buffer under-runs, this bit *must* be set to 1, either when loading text data for page-mode access or when performing multiple color-expand writes in 16-bit pixel modes. • When this bit is: — 0, fast-page detection mode is enabled, and consecutive host CPU writes to display memory are executed as fast-page mode writes, whenever possible. — 1, fast-page detection mode is disabled, and host CPU writes to display memory take place as random cycles.
5	**Reserved**
4:3	**Display Memory Data Bus Width [1:0]:** This 2-bit field is used with SRF[7] to specify the display memory data bus configuration. Since the CL-GD7556 supports only 64-bit display memory, these bits are always set to the default setting of '11'.
2	**Display Memory RAS# Cycle Select:** This bit, in combination with SR20[6] and GR18[2], defines the display memory RAS# cycle timing in terms of MCLKs. The 7-MCLK cycle is the default. • To achieve optimal performance, the display memory RAS# cycle timing must match the total number of MCLKs used.
1	**Display Memory Configuration Symmetry:** This bit selects whether the DRAM (display memory) configuration is symmetrical or asymmetrical. When this bit is: • 0, the CL-GD7556 is configured for symmetric DRAM. • 1, the CL-GD7556 is configured for asymmetric DRAM.
0	**Display Memory Multiple-CAS# / Multiple-WE# Select:** This bit selects the type of display-memory select. When this bit is: • 0, it selects multiple-WE# and one CAS# display-memory support. • 1, it selects multiple-CAS# and one WE# display-memory support, which is the default.

SR20[6]	GR18[2]	SRF[2]	Length of RAS# Cycle	Type of RAS# Cycle
0	0	0	7 MCLKs	4 MCLKs low and 3 MCLKs high
0	0	1	6 MCLKs	3.5 MCLKs low and 2.5 MCLKs high
0	1	0	8 MCLKs	5 MCLKs low and 3 MCLKs high
1	1	0	9 MCLKs	5 MCLKs low and 4 MCLKs high

12.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position Register

I/O Port Address: 3C5

Index: 10, 30, 50, 70, 90, B0, D0, F0

Bit	Description	Reset State
7	HW Cursor and HW Icon Coarse Horizontal Position [10]	0
6	HW Cursor and HW Icon Coarse Horizontal Position [9]	0
5	HW Cursor and HW Icon Coarse Horizontal Position [8]	0
4	HW Cursor and HW Icon Coarse Horizontal Position [7]	0
3	HW Cursor and HW Icon Coarse Horizontal Position [6]	0
2	HW Cursor and HW Icon Coarse Horizontal Position [5]	0
1	HW Cursor and HW Icon Coarse Horizontal Position [4]	0
0	HW Cursor and HW Icon Coarse Horizontal Position [3]	0

This register, and the Sequencer register index bits SRX[7:5] that are used to access it, is used to define in character clocks the coarse horizontal (X axis) pixel offset of the hardware cursor and icon. For more information on the hardware cursor and icon, refer to the *CL-GD7556 Software Reference Manual*.

For all 8-bit text display modes and non-expanded graphics display modes and for text display modes that do not require the fourth expansion bit, the entire 11-bit cursor or icon horizontal position can be written in a single 16-bit I/O write as follows:

- Extension register bits SR2A[6] and SR2E[0], which are cleared to 0, are ignored.
- The offset must be placed in AX[15:5].
- AX[4:0] must be '10000'.
- DX must be 3C4h.

When 10, 30, 50...F0 is written to 3C4h without writing to 3C5h (a byte write), then a read of 3C4h returns the previously stored 3 bits of the cursor or icon horizontal position.

NOTE: Changes programmed in register SR10 do not take effect until register SR11 has been written.

Bit	Description
7:0	**Hardware Cursor and Hardware Icon Coarse Horizontal Position [10:3]:** Extension register SR2A[7] selects whether the value in this register controls the hardware cursor or the hardware icon. When SR2A[7] is: • 0, the value in SR10 controls the horizontal position of the hardware cursor. • 1, the value in SR10 controls the horizontal position of the hardware icon. *(Continued)*

12.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position Register *(cont.)*

Bit	Description
7:0 *(cont.)*	**HW Cursor and HW Icon Coarse Horizontal Position [10:3]** *(cont.):*

In programming the 11-/12-bit horizontal position of the hardware cursor:

- Programming SR2A[7] to 0 enables modification of the hardware cursor (instead of the hardware icon).
- Bits [10:3] in SR10[7:0] are the most-significant 8 bits of the 11-bit hardware cursor coarse horizontal position. (For the 12-bit hardware cursor coarse horizontal position, these same bits in SR10[7:0] become bits [11:4], the most-significant 8 bits.)
- Bits [2:0], the least-significant 3 bits of the hardware cursor fine horizontal position bits, are in Sequencer register bits SRX[7:5]. These bits are defined in dot clocks.
- Extension register bit SR2E[0] extends the hardware cursor fine horizontal position by an extra bit for horizontally expanded graphics display modes. This extra bit is valid only with a 10-dot character clock.
- For text display modes and graphics display mode 13h, the hardware cursor is not available.

Register Format for the 11-Bit HW Cursor Horizontal Position

SR10[7:0]		SRX[7:5]	
10	3	2	0

Register Format for the 12-Bit HW Cursor Horizontal Position

SR10[7:0]		SR2E[0]	SRX[7:5]	
11	4	3	2	0

(Continued)

12.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position Register *(cont.)*

Bit	Description
7:0 *(cont.)*	**HW Cursor and HW Icon Coarse Horizontal Position [10:3]** *(cont.):*

In programming the 12-bit horizontal position of the hardware icon:

- Programming SR2A[7] to 1 enables modification of the hardware icon (instead of the hardware cursor).
- Bits [10:3] in SR10[7:0] are the most-significant 8 bits of the 11-bit hardware icon horizontal position. (For the 12-bit hardware icon horizontal position, these same bits in SR10[7:0] become bits [11:4], the most-significant 8 bits.)
- Bits [2:0], the least-significant bits of the hardware icon 11/12-bit horizontal position, are in Sequencer register bits SRX[7:5].
- Extension register bit SR2A[6] is bit 4 of a delay used with 9-dot or 10-dot text display modes, when in text or horizontally expanded graphics display modes. The delay is measured in dot clock units.
- The hardware icon is supported in all modes, except interlaced.

Register Format for 11-Bit Hardware Icon Horizontal Position

SR10[7:0]		SRX[7:5]	
10	3	2	0

Register Format for 12-Bit Hardware Icon Horizontal Position

SR10[7:0]		SR2A[6]	SRX[7:5]	
11	4	3	2	0

(Continued)

12.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position Register *(cont.)*

Bit	Description
7:0 *(cont.)*	**HW Cursor and HW Icon Coarse Horizontal Position [10:3]** *(cont.):*

To program the horizontal position of the hardware icon:

1. Set SR2A[7] to 1 to modify the horizontal position of the hardware icon (instead of the hardware cursor).
2. Place the hot spot for the icon (that is, the top left position of the icon) at pixel position n (with pixel position 0 counted as the first pixel).
3. Program the coarse horizontal position as: Integer {[n + (k – 1)] ÷ k}. (where k = the number of dots in a character clock.)
4. Program the fine horizontal position as: Remainder {[n + (k – 1)] ÷ k}.

For example, to place the icon:

- At pixel 10, which is 11 pixels from the left (that is, n = 10),
- With an 8-dot character clock, as in graphics display mode 12h (that is, k = 8),

Then program:

- The coarse position = Integer {[10 + (8 – 1)] ÷ 8} = Integer (17 ÷ 8) = 2h
- The fine position = Remainder (17 ÷ 8) = 1h

An example of programming for an 8-dot character clock is in the following table:

Pixel Position	Coarse Horizontal Position (hex)	Fine Horizontal Position (hex)
0	0	7
1	1	0
2	1	1
3	1	2
4	1	3
5	1	4
6	1	5
7	1	6
8	1	7
9	2	0
10	2	1

There are only three cases of character clock width.

- 10 dots — used for text and graphics expansion on 800 × 600 flat panel
- 9 dots — used for text on 800 × 600 and 1024 x 768 flat panels, when 720 dots are displayed
- 8 dots — used in all other cases

12.8 SR11: Hardware Cursor and Hardware Icon Coarse Vertical Position Register

I/O Port Address: 3C5

Index: 11, 31, 51, 71, 91, B1, D1, F1

Bit	Description	Reset State
7	HW Cursor and HW Icon Coarse Vertical Position [10]	0
6	HW Cursor and HW Icon Coarse Vertical Position [9]	0
5	HW Cursor and HW Icon Coarse Vertical Position [8]	0
4	HW Cursor and HW Icon Coarse Vertical Position [7]	0
3	HW Cursor and HW Icon Coarse Vertical Position [6]	0
2	HW Cursor and HW Icon Coarse Vertical Position [5]	0
1	HW Cursor and HW Icon Coarse Vertical Position [4]	0
0	HW Cursor and HW Icon Coarse Vertical Position [3]	0

This register, and the Sequencer register index bits SRX[7:5] that are used to access it, is used to define in scanlines the coarse vertical (Y axis) scanline offset of the hardware cursor and icon. For more information on the hardware cursor and icon, refer to the *CL-GD7556 Software Reference Manual*.

The entire 11-bit cursor or icon vertical position can be written in a single 16-bit I/O write as follows:

- The offset must be placed in AX[15:5].
- AX[4:0] must be '10001'.
- DX must be 03C4h.

When 11, 31, 51...F1 is written to 3C4h without writing to 3C5h (a byte write), then a read of 3C4h returns the previously stored 3 bits of the cursor or icon vertical position.

Bit	Description
7:0	**HW Cursor and HW Icon Coarse Vertical Position [10:3]:** Extension register SR2A[7] selects whether the value in this register controls the hardware cursor or the hardware icon. When SR2A[7] is: • 0, the value in SR11 controls the vertical position of the hardware cursor. • 1, the value in SR11 controls the vertical position of the hardware icon. When programming the cursor or the icon vertical position: • Bits [10:3], the most-significant 8 bits of the 11-bit vertical position, are in SR11[7:0]. • Bits [2:0], the least-significant 3 bits of the 11-bit vertical position, are in Sequencer register bits SRX[7:5]. These bits are defined in scanlines.

Register Format for 11-Bit Hardware Cursor/Icon Vertical Position

SR11[7:0]		SRX[7:5]	
10	3	2	0

12.9 SR12: Hardware Cursor Attributes Register

I/O Port Address: 3C5

Index: 12

Bit	Description	Reset State
7	Overscan Color Protect	0
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Hardware Cursor Size Select	0
1	Host CPU Access to DAC Extended Colors	0
0	Hardware Cursor Enable	0

This register is used to enable or disable the hardware cursor, as well as to set the hardware cursor size and to enable the palette DAC table entries used to define the colors. For a complete programming guide for the hardware cursor, refer to the *CL-GD7556 Software Reference Manual*.

Bit	Description
7	**Overscan Color Protect:** When this bit is: • 0, the overscan area color (that is, the border color) is determined by Attribute Controller register bits AR11[5:0], which select the entry in the CLUT that defines the border color. • 1, the overscan area color comes from DAC CLUT entry 258. Access to this entry is enabled by setting SR12[1] to 1.
6:3	**Reserved**
2	**Hardware Cursor Size Select:** When this bit is: • 0, the 32 × 32-pixel hardware cursor is selected. • 1, the 64 × 64-pixel hardware cursor is selected.

12.9 SR12: Hardware Cursor Attributes Register *(cont.)*

Bit **Description**

1 **Host CPU Access to DAC Extended Colors:**
When this bit is:
- 0, the host CPU accesses the standard VGA 256 × 18 CLUT.
- 1, the host CPU accesses the extended VGA CLUT, which contains DAC extended colors that are included in 16 additional 18-bit wide RAMDAC RAM locations.
  - — Some locations have a specific purpose, such as hardware cursor colors (2 locations), hardware icon colors (4 locations), and border color (1 location).
  - — Other locations are not used, or they can be used as scratch pad registers by the VGA BIOS and drivers.
  - — Two DAC CLUT entries provide for a cursor that is completely independent of the display colors.
    - — Entry 256 (accessible as location X0h) is used as the cursor background.
    - — Entry 257 (accessible as location XFh) is used as the cursor foreground.

The address map for the DAC extended colors is given in the following table:

I/O Address	Physical RAM Location Entry	Function
X0h	256	Sets hardware cursor background color
XFh	257	Sets hardware cursor foreground color
X2h	258	Sets border color (color for overscan area)
X3h	259	Sets hardware icon color #0. (This function is reserved, when in 3-colors-and-transparent mode.)
X4h	260	Sets hardware icon color #1. (This function is reserved, when in 3-colors-and-transparent mode.)
X5h	261	Sets hardware icon color #2. (This function is reserved, when in 3-colors-and-transparent mode.)
X6h	262	Sets hardware icon color #3. (This function is reserved, when in 3-colors-and-transparent mode.)
XAh, XBh, XCh, XDh	266, 267, 268, 269	Reserved

0 **Hardware Cursor Enable:**
- When this bit is:
  - — 0, the hardware cursor is disabled and does not appear on-screen.
  - — 1, the hardware cursor is enabled and appears on-screen.
- To select the hardware cursor size, refer to SR12[2].

12.10 SR13: Hardware Cursor Pattern Address Select Register

I/O Port Address: 3C5

Index: 13

Bit	Description	Reset State
7	Not Used	Not applicable
6	Not Used	Not applicable
5	Reserved (Read-only Bit)	1
4	Hardware Cursor Pattern Select [4] / [2]	0
3	Hardware Cursor Pattern Select [3] / [1]	0
2	Hardware Cursor Pattern Select [2] / [0]	0
1	Hardware Cursor Pattern Select [1] / Reserved	0
0	Hardware Cursor Pattern Select [0] / Reserved	0

This register is used to select one of the following:

- One of the 32 possible cursor patterns for the 32 × 32 hardware cursor.
- One of the 8 possible cursor patterns for the 64 × 64 hardware cursor.

For a complete programming guide for the hardware cursor, refer to the *CL-GD7556 Software Reference Manual*.

Bit	Description
7:6	**Reserved**
5	**Reserved:** This read-only bit always reads back a 1.
4:0	**Hardware Cursor Pattern Select [4:0] (32 × 32 Cursor):** When SR12[2] is 0: • This 5-bit field can select one of 32 cursor patterns for the 32 × 32 cursor. • The patterns are stored in 8 Kbytes within the highest 32 Kbytes of display memory.
4:2	**Hardware Cursor Pattern Select [2:0] (64 × 64 Cursor):** When SR12[2] is 1: • This 3-bit field can select one of 8 cursor patterns for the 64 × 64 cursor. • The patterns are stored in 8 Kbytes within the highest 32 Kbytes of display memory.
1:0	**Reserved:** When SR12[2] is 1, these bits are reserved.

12.11 SR14, SR15: Scratch Pad #2 and #3 Registers

I/O Port Address: 3C5

Index: 14, 15

Bit	Description	Access	Reset State
7	Scratch Pad #2 and #3 [7]	R/W	0
6	Scratch Pad #2 and #3 [6]	R/W	0
5	Scratch Pad #2 and #3 [5]	R/W	0
4	Scratch Pad #2 and #3 [4]	R/W	0
3	Scratch Pad #2 and #3 [3]	R/W	0
2	Scratch Pad #2 and #3 [2]	R/W	0
1	Scratch Pad #2 and #3 [1]	R/W	0
0	Scratch Pad #2 and #3 [0]	R/W	0

These two registers are reserved for the exclusive use of the CL-GD7556 VGA BIOS and must never be written by any application program. They are listed here only for reference.

Bit	Description
7:0	**Reserved**

12.12 SR17: BitBLT Memory Map I/O Address Control Register

I/O Port Address: 3C5

Index: 17

Bit	Description	Reset State
7	Memory Read Retry if Time-Out Occurs	0
6	BitBLT Memory Map I/O Address Control	0
5	Reserved	
4	Reserved	
3	Enable Write to PC2C for Subsystem ID	0
2	BitBLT Memory Map I/O Address Control Enable	0
1	Reserved	
0	Reserved	

This register is used to control the placement of the BitBLT memory map, in order to allow the BitBLT to be programmed in 32-bit segments.

Bit	Description
7	**Memory Read Retry if Time-Out Occurs:** When this bit is: • 0, no memory read retry is attempted. • 1, a PCI bus memory read retry is enabled. If a time-out occurs during a memory read cycle, the PCI bus attempts to re-read the same location in memory.
6	**BitBLT Memory Map I/O Address Control:** When memory-mapped I/O is enabled (that is, SR17[2] is 1), this bit works in combination with Extension register SR7[7:4] to select either segmented or linear addressing. When this bit is: • 0, *and* Extension register bits SR7[7:4] are '0000', *and* Graphics Controller register bits GR6[3:2] are '01', the address space is segmented. • 1 *and* Extension register bits SR7[7:4] are other than '0000' (that is, non-zero), the address space for memory-mapped I/O is the last 256 bytes of linear address space starting at 3FFF00. For details, refer to Appendix H.
5:4	**Reserved**
3	**Enable Write to PC2C for Subsystem ID:** When this bit is: • 1, the Subsystem ID and Subsystem Vendor ID can be written to External/General register PCI2C. This register is for PC97 compatibility. • 0, the Subsystem ID and Subsystem Vendor ID can be read from External/General register PCI2C.
2	**BitBLT Memory Map I/O Address Control Enable:** When this bit is: • 0, the BitBLT memory map I/O address is disabled. • 1, the BitBLT registers (that is, Graphics Controller registers GR0–1 and Extension registers GR10–13, and GR20–33) are addressable as a 36-byte block of memory, allowing faster access.
1:0	**Reserved**

12.13 SR18: Signature Generator Control Register

I/O Port Address: 3C5

Index: 18

Bit	Description	Reset State
7	Signature Generator Control for BitBLT	0
6	VCLK/Pixel Bus Driver Disable	0
5	Signature Generator Display Memory Data Enable	0
4	Signature Generator Input from V-Port [2]	0
3	Signature Generator Input from V-Port [1]	0
2	Signature Generator Input from V-Port [0]	0
1	Signature Generator Reset	0
0	Signature Generator for CRT Monitor Enable / Status	0

This register is used to control and monitor the status of the CL-GD7556 signature generator, which is used for board-level testing of the video sub-system. For a complete description of the signature generator, refer to Appendix D.

NOTE: This register is intended to be used only for test purposes.

Bit	Description
7	**Signature Generator Control for BitBLT:** This bit is used to disable the MCLK only for test purposes. When this bit is: • 0, the Signature Generator for the BitBLT is disabled. • 1, the Signature Generator for the BitBLT is enabled.
6	**VCLK/Pixel Bus Driver Disable:** This bit is used to disable the VCLK and internal pixel bus drivers only for test purposes. (This bit does not affect the Signature Generator.) When this bit is: • 0, the VCLK is enabled and operates normally. • 1, the VCLK and pixel bus drivers are disabled.
5	**Signature Generator Display Memory Data Enable:** This bit is intended to generate data for the display memory data bus only for test purposes. When this bit is set to: • 0, data is placed on the display memory data bus as normal. • 1, pseudo-random data is placed on the display memory data bus.

12.13 SR18: Signature Generator Control Register *(cont.)*

Bit **Description**

4:2 **Signature Generator Input from V-Port [2:0]:**
As shown in the following table, this field can be used in one of two ways:
- SR18[4:2] can be used to select V-Port bits that are used as the input for the CRT monitor signature generator.
- SR18[3:2] can be used to select a color for a flat panel signature generator.

SR18			Input from V-Port to CRT Monitor Signature Generator	Select Color for Flat Panel Signature Generator
[4]	[3]	[2]		
0	0	0	VPY[0]	Red
0	0	1	VPY[1]	Green
0	1	0	VPY[2]	Blue
0	1	1	VPY[3]	—
1	0	0	VPY[4]	Red
1	0	1	VPY[5]	Green
1	1	0	VPY[6]	Blue
1	1	1	VPY[7]	—

1 **Signature Generator Reset:**
When this bit is:
- 0, the signature generator is allowed to run under the control of SR18[0].
- 1, the signature generator is reset to an initial, defined condition.

0 **Signature Generator for CRT Monitor Enable / Status:**
When this bit is set to 1, the signature generator is enabled for a CRT monitor.
- The signature generator begins operation on the next vertical sync period from the V-Port bit chosen by SR18[4:2].
- The signal generator accumulates a signature for one frame, and then it stops, forcing this bit to 0.

By monitoring the status of this bit, a program can determine when the signature is complete for the CRT monitor.

NOTE: SR18[0] must be a 1 to start the Signature Generator.
SR18[0] is cleared to 0, when the Signature Generator is complete.

12.14 SR19: Signature Generator Result Low Register

I/O Port Address: 3C5

Index: 19

Bit	Description	Reset State
7	Signature Generator Result [7]	0
6	Signature Generator Result [6]	0
5	Signature Generator Result [5]	0
4	Signature Generator Result [4]	0
3	Signature Generator Result [3]	0
2	Signature Generator Result [2]	0
1	Signature Generator Result [1]	0
0	Signature Generator Result [0]	0

This register contains the least-significant 8 bits of the 16-bit Signature Generator Result field.

Bit	Description
7:0	**Signature Generator Result [7:0]:** These bits are the least-significant 8 bits of the 16-bit Signature Generator Result field. **16-Bit Signature-Generator-Result-Register Format** SR1A[7:0] (15–8) | SR19[7:0] (7–0) For details on this field, refer to SR1A.

12.15 SR1A: Signature Generator Result High Register

I/O Port Address: 3C5

Index: 1A

Bit	Description	Reset State
7	Signature Generator Result [15]	0
6	Signature Generator Result [14]	0
5	Signature Generator Result [13]	0
4	Signature Generator Result [12]	0
3	Signature Generator Result [11]	0
2	Signature Generator Result [10]	0
1	Signature Generator Result [9]	0
0	Signature Generator Result [8]	0

This register contains the most-significant 8 bits of the 16-bit Signature Generator Result field. For a complete description of the signature generator, refer to Appendix D.

Bit	Description
7:0	**Signature Generator Result [15:8]:** • These bits [15:8], the most-significant 8 bits of the Signature Generator Result field, are used to read the most-significant 8 bits of the signature generator result. • Bits [7:0], the least-significant 8 bits, are in SR19. They are used to read the least-significant 8 bits of the signature generator result.

16-Bit Signature-Generator-Result-Register Format

SR1A[7:0]		SR19[7:0]	
15	8	7	0

12.16 SR1B,SR1C,SR1D,SR1E: VCLK0,1,2,3 Denominator and Post-Scalar Register

I/O Port Address: 3C5

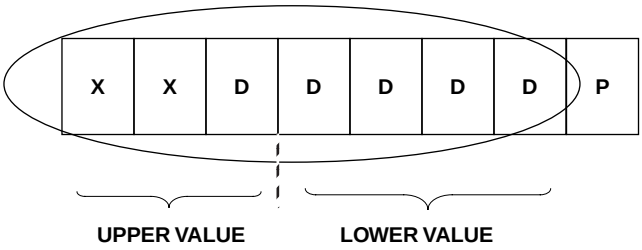
Index: 1B, 1C, 1D, 1E

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	VCLK Denominator [4]	R/W	See following table
4	VCLK Denominator [3]	R/W	See following table
3	VCLK Denominator [2]	R/W	See following table
2	VCLK Denominator [1]	R/W	See following table
1	VCLK Denominator [0]	R/W	See following table
0	VCLK Post-Scalar	R/W	See following table

These registers are used in combination with Extension registers SRB to SRE to establish the frequency of the four possible VCLK signals. The VCLK used is selected by Extension/General register MISC[3:2].

These registers establish the Denominator and Post-Scalar values. For information on the Numerator value, refer to Section 12.5. For more information on clock options, refer to Appendix B.

VCLK2, which uses registers SRD and SR1D with MISC[3:2] = '10', is the default for flat panel operation.

Bit	Description
7:6	**Reserved**
5:1	**VCLK Denominator [4:0]:** These bits determine the Denominator value in the equation that is used to determined the VCLK frequency. In calculating the Denominator value, the Post-Scalar bit is ignored, which has the effect of shifting all bits in the register to the right.  **UPPER VALUE = VALUES IN XXD LOWER VALUE = VALUES IN DDDD** **Circled area contains the value that is extracted, converted to decimal, and substituted in the equation.**
0	**VCLK Post-Scalar:** This bit, which defines either a divide-by-one or a divide-by-two operator, determines the Post-Scalar value in the equation that is used to determine the VCLK frequency. (When the Post-Scalar value is 1, then the voltage-controlled oscillator is running at two times OSC, the input clock frequency.) *(Continued)*

12.16 SR1B, SR1C, SR1D, SR1E: VCLK0,1,2,3 Denominator and Post-Scalar *(cont.)*

Each VCLK frequency is determined with the following calculation:

$$\text{DIVIDE: } \frac{\text{OSC} \times \text{Numerator}}{\text{Denominator} \times (\text{Post-Scalar Value} + 1)} \text{ BY:}$$

TO OBTAIN: = VCLK*n* (MHz)

where:

VCLK*n*	=	VCLK frequency *n*, where *n* = 0, 1, 2, 3
OSC	=	Input clock frequency of 14.318 MHz
Numerator	=	Value of register bits SRi [6:0], where *i* = B, C, D, E
Denominator	=	Value of register bits SR1i [5:1], where *i* = B, C, D, E
Post-Scalar	=	Value of register bits SR1i [0], where *i* = B, C, D, E

If *n* = 0, then *i* = B.
If *n* = 1, then *i* = C.
If *n* = 2, then *i* = D.
If *n* = 3, then *i* = E.

The following table shows the reset values of the registers that determine the VCLK frequency. The table also shows the corresponding VCLK frequency at system reset.

VCLK*n* and Reset Frequency		Numerator			Denominator			Post-Scalar
VCLK*n*	VCLK*n* Frequency at System Reset (MHz)	Numerator Register and Its Hex Value		Numerator Value Used in Equation	Denominator Register and Its Hex Value		Denominator Value Used in Equation[a]	Post-Scalar Value Used in Equation
		Register (SRi)	Hex	Decimal Equivalent of Hex Value	Register (SR1i)	Hex	Decimal	Decimal
VCLK0	25.180	SRB	66h	102	SR1B	3Bh	29	1
VCLK1	28.325	SRC	5Bh	91	SR1C	2Fh	23	1
VCLK2[b]	41.165	SRD	45h	69	SR1D	30h	24	0
VCLK3	36.082	SRE	7Eh	126	SR1E	33h	25	1

[a] These values result from the Post-Scalar and are not the decimal equivalent of the hex values in the previous column.

[b] VCLK2 is the default for flat panel operation.

12.17 SR1F: MCLK Frequency and VCLK Source Select Register

I/O Port Address: 3C5

Index: 1F

Bit	Description	Reset State
7	Not Used	Not applicable
6	VCLK Source Select	0
5	MCLK Frequency [5]	(Refer to MCLK Table)
4	MCLK Frequency [4]	(Refer to MCLK Table)
3	MCLK Frequency [3]	(Refer to MCLK Table)
2	MCLK Frequency [2]	(Refer to MCLK Table)
1	MCLK Frequency [1]	(Refer to MCLK Table)
0	MCLK Frequency [0]	(Refer to MCLK Table)

This register is used to program the MCLK frequency. This register must never be programmed by an application program. It is listed here only for reference.

Bit **Description**

7 **Reserved**

6 **VCLK Source Select:**
This bit works in combination with SR1E[0] to select the VCLK source. When this bit is:

- 0, the VCLK synthesizer operates normally.
- 1, VCLK is derived from MCLK as shown in the following table:

SR1F[6]	SR1E[0]	VCLK Source
0	X	VCLK (Normal Operation)
1	0	VCLK = MCLK
1	1	VCLK = (MCLK ÷ 2)

12.17 SR1F: MCLK Frequency and VCLK Source Select Register *(cont.)*

Bit	Description
5:0	**MCLK Frequency [5:0]:** This 6-bit field, which must never be programmed by an application program, is used to set the desired MCLK frequency as follows: MULTIPLY: The hex value in SR1F[5:0] BY: × (Reference Frequency of 14.318 MHz ÷ 8) TO OBTAIN: = Desired MCLK Frequency • For DRAM requirements for MCLK frequencies, refer to Appendix A. • As shown in the following table, this field can be programmed with values from 21 to 45 (decimal). The table assumes a reference frequency of 14.318 MHz.

SR1F[5:0] in Decimal and (Hex)	(Reference Frequency ÷ 8) =	Desired MCLK Frequency
21 (15h)	14.318 ÷ 8 = 1.79	37.585 MHz
23 (17h)		41.165 MHz
24 (18h, the default value at reset)		**42.955 MHz**
25 (19h)		44.744 MHz
26 (1Ah)		46.534 MHz
28 (1Ch)		50.114 MHz
31 (1Fh)		55.5 MHz
33 (21h)		59.1 MHz
37 (25h)		66.2 MHz
40 (28h)		71.6 MHz
42 (2Ah)		75.2 MHz
45 (2Dh)		80.5 MHz

12.18 SR20: Miscellaneous Control Register 2

I/O Port Address: 3C5

Index: 20

Bit	Description	Reset State
7	PCI Bus CMOS/TTL Toggle Enable	0
6	Select 9-MCLK RAS# Cycles for EDO DRAMs	0
5	Force Flat Panel Data and Control Pins to High Impedance	0
4	V-Port CMOS Threshold Enable	0
3	Force Flat Panel Power-Sequence Pins to High Impedance	0
2	320 × 240 Display Mode Enable at 16 Bpp	0
1	Set VCLK0,1 Source to VCLK VCO/4	0
0	Set MCLK Source to MCLK VCO/2	0

This register is reserved exclusively for the CL-GD7556 VGA BIOS and must never be written by an application program. It is listed here only for reference.

Bit **Description**

7 **PCI Bus CMOS/TTL Toggle Enable:**
This bit toggles the threshold of most pads related to the PCI bus. (The exception is the PCI bus CLK pad, which is always set for a CMOS threshold.) When this bit is 1, it toggles the pad threshold from its previous state to the alternative state (that is, either from CMOS to TTL, or from TTL to CMOS). This bit is intended to be used only for test purposes.

6 **Select 9-MCLK RAS# Cycles for EDO DRAMs:**
This bit, in combination with Extension register bits SRF[2] and GR18[2], defines the RAS# cycle timing in terms of MCLKs.

SR20[6]	GR18[2]	SRF[2]	Length of RAS# Cycle	Type of RAS# Cycle
0	0	0	7 MCLKs	4 MCLKs low and 3 MCLKs high
0	0	1	6 MCLKs	3.5 MCLKs low and 2.5 MCLKs high
0	1	0	8 MCLKs	5 MCLKs low and 3 MCLKs high
1	1	0	9 MCLKs	5 MCLKs low and 4 MCLKs high

12.18 SR20: Miscellaneous Control Register 2 *(cont.)*

Bit	Description
5	**Force Flat Panel Data and Control Pins to High Impedance:** When this bit is: • 0, flat panel data and control pins operate normally. (This condition is the default.) • 1, flat panel data and control pins are off (that is, high-impedance). **CAUTION:** This setting, which is used normally only for test purposes, can cause damage to a flat panel. Under normal circumstances, the flat panel data and control pins must not be in a high-impedance state. To enable or disable a flat panel, use instead Extension register bit CR80[0]. — For all flat panels, the following flat panel data and control pins are off: FP[17:0], FPDE, FPVDCLK, LFS, LLCLK — When a 24-bit TFT (thin-film transistor) flat panel with 1x clock is selected, (that is, Extension register bits CR83[3:2] are set to '11'), the following additional flat panel data and control pins are off: FP[31:30], FP[25:24], FP[19:18] — Although the following flat panel power-management pins are panel-related, they are not affected by this bit and are instead controlled by SR20[3]: FPVCC, FPVEE
4	**V-Port CMOS Threshold Enable:** When this bit is: • 0, a TTL threshold is enabled for pads related to the V-Port. (This bit setting is the default.) • 1, a CMOS threshold is enabled for pads related to the V-Port.
3	**Force Flat Panel Power-Sequence Pins to High Impedance:** This bit affects the flat panel power pins FPVCC and FPVEE. When this bit is: • 0, the above-mentioned flat panel power pins operate normally and are active. • 1, the above-mentioned flat panel power pins are off (that is, high-impedance). The caution mentioned in SR20[5] also applies to this bit setting.
2	**320 × 240 Display Mode Enable at 16 Bpp:** When this bit is 1, it enables the 320 × 240 graphics display mode at 16 bpp.
1	**Set VCLK0,1 Source to VCLK VCO/4:** When this bit is: • 0, all VCLKs (that is, VCLK0,1,2,3) operate normally. • 1, *and* bit 0 of Extension registers SR1B and SR1C is 1, then either VCLK0 or VCLK1 is set equal to the VCLK VCO/4. — VCLK0 is selected by setting External/General register bits MISC[3:2] to '00'. — VCLK1 is selected by setting External/General register bits MISC[3:2] to '01'.
0	**Set MCLK Source to MCLK VCO/2:** When this bit is: • 0, MCLK operates normally. • 1, MCLK is set equal to the MCLK VCO/2.

12.19 SR21: Test Bus Control Register

I/O Port Address: 3C5

Index: 21

Bit	Description	Reset State
7	Reserved	
6	Flat Panel Signature Generator Enable	0
5	Reserved	
4	Test Bus Select [2]	0
3	Inverted Voltage-Controlled Oscillator Output Used as VCLK	0
2	Test Bus Enable	0
1	Test Bus Select [1]	0
0	Test Bus Select [0]	0

This register contains bits that control different functions as described in the text that follows.

NOTE: This register is intended to be used only for factory test purposes.

Bit	Description
7	**Reserved**
6	**Flat Panel Signature Generator Enable:** When this bit is: • 0, the flat panel signature generator is disabled. • 1, the flat panel signature generator is enabled.
5	**Reserved**
4	**Test Bus Select [2]:** This is bit 2, the most-significant bit of the 3-bit Test Bus Select field. The selected test bus is enabled, when SR21[2] is 1. • Bits [1:0], the least-significant bits, are in SR21[1:0]. **Register Format for 3-Bit Test Bus Select** SR21[4] | SR21[1:0] (2 | 1 0) • This field is used to select various buses on the CL-GD7556 for factory testing.
3	**Inverted Voltage-Controlled Oscillator Output Used as VCLK:** When this bit is: • 0, VCLK is normal. • 1, VCLK is the inverse of the output from the voltage-controlled oscillator.
2	**Test Bus Enable:** This bit applies to the test bus that is selected by SR21[4,1:0]. When this bit is: • 0, the selected test bus is disabled. • 1, the selected test bus is enabled.
1:0	**Test Bus Select [1:0]:** • These bits [1:0] are the least-significant 2 bits of the 3-bit Test Bus Select field. • For details of this field, refer to SR21[4].

12.20 SR22: Hardware Configuration Read Register 1

I/O Port Address: 3C5

Index: 22

Bit	Description	Access	Reset State
7	Memory-Mapped I/O Status	R	= MD34
6	Test Mode Status	R	= MD33
5	PCI-Bus CMOS Threshold Status	R	= MD32
4	On-Chip PCI VGA BIOS Support Status	R	= MD31
3	32-Kbyte EPROM BIOS Status	R	= MD30
2	External Clock on VCLK and MCLK Status	R	= MD29
1	Interrupt Request Pin (INTR#) Status	R	= MD28
0	Pin-Scan Test Mode Status	R	= MD27

This register contains a read-only field that allows the VGA BIOS to determine configuration information for the system. The contents of the bits in this field mirror the status of pull-up resistors on the indicated MD pins at system reset.

- All these MD pins have pull-down resistors internally, and so the default readings are all ‘0’.
- All these MD pins require an external pull-up resistor to establish a high (‘1’) reading.

For more configuration details, refer to Section 2.8.

Bit	Description
7	**Memory-Mapped I/O Status:** When MD34 / MMIOPU (pin 217): • Is not connected to an external pull-up resistor: — This read-only bit is cleared to 0 during system reset. — The VGA I/O address space operates normally. • Is connected to an external pull-up resistor: — This read-only bit is set to 1 during system reset. — The VGA I/O address space is defined as memory-mapped I/O. **NOTE:** This memory-map I/O function is not the same as, and must not be confused with, the BitBLT memory-map I/O function of Extension register SR17[6,2].
6	**Test Mode Status:** When MD33 / TMPU (pin 218): • Is not connected to an external pull-up resistor: — This read-only bit is cleared to 0 during system reset. — All chip functions operate as defined in Chapter 2. • Is connected to an external pull-up resistor: — This read-only bit is set to 1 during system reset. — The chip is configured for factory test purposes and the pin-scan test that is discussed in Appendix E. — PROG1 / TWR# (pin 119) is configured for TWR#.

12.20 SR22: Hardware Configuration Read Register 1*(cont.)*

Bit	Description
5	**PCI-Bus CMOS Threshold Status:** When MD32 / CMOSPU (pin 219): • Is not connected to an external pull-up resistor, most of the PCI bus pads are configured for a TTL threshold. (The exception is the PCI bus CLK pad, which is always set for a CMOS threshold.) • Is connected to an external pull-up resistor, the PCI bus pads are configured for a CMOS threshold.
4	**On-Chip PCI VGA BIOS Support Status:** When MD31 / BIOSPU (pin 234): • Is not connected to an external pull-up resistor: — This read-only bit is cleared to 0 during system reset. — On-Chip PCI VGA BIOS is disabled. • Is connected to an external pull-up resistor: — This read-only bit is set to 1 during system reset. — On-Chip PCI VGA BIOS is enabled. — External/General register PCI30[0] is set to 1.
3	**32-Kbyte EPROM BIOS Status:** When MD30 / ROM32KPU (pin 235): • Is not connected to an external pull-up resistor: — This read-only bit is cleared to 0 during system reset. — 64-Kbyte EPROM BIOS (that is, the VGA BIOS) is supported. **IMPORTANT:** When the Cirrus Logic VGA BIOS is used, this bit must be always be 0, since the CL-GD7556 Cirrus Logic VGA BIOS requires a minimum of 48 Kbytes. • Is connected to an external pull-up resistor: — This read-only bit is set to 1 during system reset. — 32-Kbyte EPROM BIOS is supported.
2	**External Clock on VCLK and MCLK Status:** When MD29 / XCLKPU (pin 236): • Is not connected to an external pull-up resistor: — This read-only bit is cleared to 0 during system reset. — VCLK and MCLK are derived internally. • Is connected to an external pull-up resistor: — This read-only bit is set to 1 during system reset. — VCLK is driven by an input on OSC / XVCLK (pin 54). — MCLK is driven by an input on SW0 / MCLK / XMCLK (pin 251).

12.20 SR22: Hardware Configuration Read Register 1*(cont.)*

Bit	Description
1	**Interrupt Request Pin (INTR#) Status:** When MD28 / INTPU (pin 237): • Is not connected to an external pull-up resistor: — This read-only bit is cleared to 0 during system reset. — External/General register PCI3C[8] reads back a 1. — INTR# (pin 43) is enabled. • Is connected to an external pull-up resistor: — This read-only bit is set to 1 during system reset. — External/General register PCI3C[8] reads back a 0. — INTR# (pin 43) is disabled and must not be connected to the CPU bus.
0	**Pin-Scan Test Mode Status:** When MD27 / SCANPU (pin 238): • Is not connected to an external pull-up resistor: — This read-only bit is cleared to 0 during system reset. — The Pin-Scan Test is not enabled. • Is connected to an external pull-up resistor: — This read-only bit is set to 1 during system reset. — The Pin-Scan Test is enabled.

12.21 SR23: Software Configuration Register 1

I/O Port Address: 3C5

Index: 23

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Adaptive Write-Buffer Depth Control Disable	0
4	DDCC/VCLKO Output Select and Enable	0
3	Reserved	
2	MCLK VCO Output Select on SW0 / MCLK / XMCLK Pin	0
1	Reserved	
0	SW0 / MCLK / XMCLK Function Select	0

Bit — **Description**

7:6 — **Reserved**

5 — **Adaptive Write-Buffer Depth Control Disable:**
When this bit is:
- 0, Adaptive Write-Buffer Depth Control is enabled. The write buffer depth is varied automatically, depending on the bus clock speed.
- 1, Adaptive Write-Buffer Depth Control is disabled. The write buffer depth is varied under software control.

4 — **DDCC/VCLKO Output Select and Enable:**
When this bit is:
- 0, DDCC/VCLKO (pin 98) is enabled for V-Port DDCC, and VCLKO is disabled.
- 1, DDCC/VCLKO is enabled for VCLKO, and V-Port DDCC is disabled.

3 — **Reserved**

2 — **MCLK VCO Output Select on SW0 / MCLK / XMCLK Pin:**
This bit is used with SR22[2] and SR23[0] to configure the SW0 / MCLK / XMCLK pin (pin 251) for the MCLK VCO output function. For details, refer to SR23[0].

1 — **Reserved**

0 — **SW0 / MCLK / XMCLK Function Select**:
This bit works in combination with SR22[2] and SR23[2] to select the function of the SW0 / MCLK / XMCLK (pin 251), as shown in the following table:

SR22[2]	SR23		SW0 / MCLK/ XMCLK Pin Function
	[2]	[0]	
0	X	0	SW0 Input
0	0	1	MCLK Output
0	1	1	MCLK VCO Output
1	X	X	XMCLK Input

12.22 SR24: Flat Panel Type Switches Enable Register

I/O Port Address: 3C5

Index: 24

Bit	Description	Access	Reset State
7	V-Port Select	R	0
6	VPCLKI Invert Enable	R/W	0
5	Reserved		
4	VCLKO Clock Output Select	R/W	0
3	External Pull-Ups Read under Software Control	R/W	Pull-up Acknowledge
2	SW2PU Pin Readback	R	= MD25
1	SW1PU Pin Readback	R	= MD24
0	SW0 Pin Readback	R	

Bit	Description
7	**V-Port Select:** This read-only bit monitors the status of MD26 (pin 240) during power-on reset. As long as pin 240 is not forced high with a pull-up resistor or other connection, this bit reads back a 0, which confirms that the V-Port is selected. **NOTE:** V-Port is not enabled until Extension register CR51[3] is set to 1.
6	**VPCLKI Invert Enable:** When this bit is 1, the normally active-high VPCLKI signal is inverted to active-low. This bit is used internally to latch data.
5	**Reserved**
4	**VCLKO Clock Output Select:** When SR23[4] is 1 (that is, the DDCC/VCLKO pin is enabled for VCLKO), this bit is used to select the clock that appears on the VCLKO pin. When this bit is: • 0, the clock selected is PCLKO, which is a dot clock that is *not* divided-by-2 by the Sequencer register bit SR1[3]. • 1, the clock selected is VCLK, which is the internal voltage-controlled oscillator output clock.
3	**External Pull-Ups Read under Software Control:** This bit controls the reading of external pull-up resistors after system reset is completed. (For information on the value of the external pull-ups, refer to Section 2.9.) • This bit is normally 0 (the default). This bit is for reading external pull-ups during the system reset. • A 0-1-0 transition of this bit reads all the external pull-up resistors and loads their state into the appropriate registers. This bit manipulation is used when the system reset pulse is too short to read inputs that have too large pull-up or pull-down resistance.

12.22 SR24: Flat Panel Type Switches Enable Register *(cont.)*

Bit	Description
2:1	**SW2PU and SW1PU Pin Readback**: These read-only bits (SR24[2:1]) echo the level of switch input pins SW2PU and SW1PU respectively. • When an external pull-up resistor: — Is not connected on the SW2PU and SW1PU pins (that is, inputs are low), these bits are set to 0 during system reset. — Is connected on any one of these SW2PU and SW1PU pins (that is, inputs are high), the corresponding bit in this register is set to 1 during system reset. • These bits are normally for VGA BIOS use.
0	**SW0 Pin Readback**: When the SW0 / MCLK / XMCLK pin is configured for the SW0 function (refer to SR23[0]), this read-only bit reflects the level of switch input pin SW0 as follows: — Low = 0. — High = 1. • This bit is normally for VGA BIOS use.

12.23 SR25: FasText™ Mode Control Register

I/O Port Address: 3C5

Index: 25

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	External XVCLK Input Enable	0
3	Reserved	
2	Disable Effect of CR1B[1] on CRT Monitor Address Access	0
1	FasText Text Display Mode Enable	0
0	FasText Graphics Display Mode Enable	0

Bit	Description
7:5	**Reserved**
4	**External XVCLK Input Enable:** This bit is used to enable simulation and test vector generation. When Extension register SR22[2] is: • 0 *and* this bit is: — 0, both MCLK and VCLK are derived from the internal CL-GD7556 MCLK VCO source. — 1, an external 14.318-MHz input must be connected to OSC / XVCLK (pin 54). In this case: — MCLK does not use this input. Instead, it uses the internal CL-GD7556 MCLK VCO source. — On VCLK generation, this bit is OR'ed with SR22[2]. • 1, MCLK and VCLK both use external clock sources. — MCLK uses the external clock source XMCLK, which is supplied on pin 251. — VCLK uses the external clock source XVCLK, which is supplied on pin 54.
3	**Reserved**

12.23 SR25: FasText™ Mode Control Register *(cont.)*

Bit	Description
2	**Disable Effect of CR1B[1] on CRT Monitor Address Access:** This bit works in combination with Extension register bit CR1B[1] to define the range of display memory addresses that can be accessed by the CRT controller and the host CPU. When CR1B[1] is: • 0, this bit is disabled and becomes a 'don't care' bit. — As a result, both the CRT controller and the host CPU can access only the standard VGA display memory, which is limited to a 64-Kbyte boundary and which totals 256 Kbytes. — This bit setting is used to force the standard VGA memory to support 64-Kbyte address wrapping, which is used by some applications for fast scrolling. • 1, *and* this bit is: — 0, the CRT controller is limited to the display-memory access range for standard VGA display modes (that is, 256K bytes). In contrast, the host CPU can access the total available display memory. — This bit setting is used to update hardware icon and hardware cursor mapping in standard VGA display modes. — 1, both the CRT controller and the host CPU can access the entire display memory. — This bit setting is used with extended graphics display modes that require more display memory than the display memory for standard VGA graphics display modes. — This bit setting is necessary to allow the CRT controller access to the hardware icon and hardware cursor • The following table lists the bit settings that result in extended display memory access for the CRT monitor and host CPU.

CR1B[1]	SR25[2]	Display Memory Address Range	
		Accessed By CRT Controller	Accessed By Host CPU
0	X	VGA Compatible – Total of 256 Kbytes display memory	VGA Compatible – Total of 256 Kbytes display memory
1	0	VGA Compatible – Total of 256 Kbytes display memory	Range is extended to include total available display memory
1	1	Range is extended to include total available display memory	Range is extended to include total available display memory

12.23 SR25: FasText™ Mode Control Register *(cont.)*

Bit	Description
1	**FasText Text Display Mode Enable:** This display mode is fully VGA compatible. Because it requires less memory bandwidth than standard text display modes, it is useful with high-resolution flat panels. When this bit is: • 0, FasText Mode for text display modes (both CRT and CPU) is disabled. • 1, FasText Mode for text display modes (both CRT and CPU) is enabled.
0	**FasText Graphics Display Mode Enable:** This display mode is fully VGA compatible. Because it requires less memory bandwidth than standard graphics display modes, it is useful with high-resolution flat panels. When this bit is: • 0, FasText Mode for graphics display modes (that is, CPU only) is disabled. • 1, FasText Mode for graphics display modes (that is, CPU only) is enabled.

12.24 SR26: Shader Signature Low Register

I/O Port Address: 3C5

Index: 26

Bit	Description	Reset State
7	Shader Signature [7]	0
6	Shader Signature [6]	0
5	Shader Signature [5]	0
4	Shader Signature [4]	0
3	Shader Signature [3]	0
2	Shader Signature [2]	0
1	Shader Signature [1]	0
0	Shader Signature [0]	0

The Shader Signature field is used only for factory testing of the CL-GD7556 shader logic. Application programs must not use the Shader Signature registers, which are listed here only for reference.

Bit	Description
7:0	**Shader Signature [7:0]:** These bits are the least-significant 8 bits of the 16-bit Shader Signature field. **Register Format for 16-Bit Shader Signature** SR27[7:0] (15 – 8) | SR26[7:0] (7 – 0) • For details on this field, refer to SR27.

12.25 SR27: Shader Signature High Register

I/O Port Address: 3C5

Index: 27

Bit	Description	Reset State
7	Shader Signature [15]	0
6	Shader Signature [14]	0
5	Shader Signature [13]	0
4	Shader Signature [12]	0
3	Shader Signature [11]	0
2	Shader Signature [10]	0
1	Shader Signature [9]	0
0	Shader Signature [8]	0

The Shader Signature field is used only for factory testing of the CL-GD7556 shader logic. Application programs must not use the Shader Signature registers, which are listed here only for reference.

Bit	Description
7:0	**Shader Signature [15:8]:** These bits [15:8] are the most-significant 8 bits of the 16-bit Shader Signature field. • Bits [7:0], the least-significant 8 bits, are in SR26.

Register Format for 16-Bit Shader Signature

SR27[7:0]		SR26[7:0]	
15	8	7	0

12.26 SR28, SR29 Scratch Pad #4 and #5 Registers

I/O Port Address: 3C5

Index: 28, 29

Bit	Description	Access	Reset State
7	Scratch Pad #4 and #5 [7]	R/W	0
6	Scratch Pad #4 and #5 [6]	R/W	0
5	Scratch Pad #4 and #5 [5]	R/W	0
4	Scratch Pad #4 and #5 [4]	R/W	0
3	Scratch Pad #4 and #5 [3]	R/W	0
2	Scratch Pad #4 and #5 [2]	R/W	0
1	Scratch Pad #4 and #5 [1]	R/W	0
0	Scratch Pad #4 and #5 [0]	R/W	0

These two registers are reserved for the exclusive use of the CL-GD7556 VGA BIOS. They must never be written by any application program. They are listed here only for reference.

Bit	Description
7:0	**Reserved**

12.27 SR2A: Hardware Icon #0 Control and Cursor/Icon Select Register

I/O Port Address: 3C5

Index: 2A

Bit	Description	Reset State
7	Hardware Cursor or Hardware Icon Select	0
6	Hardware Icon Fine Horizontal Position [3]	0
5	Hardware Icon #0 Display Memory Map Select	0
4	Hardware Icon #0 Vertical Scanline Double	0
3	Hardware Icon #0 Horizontal Pixel Double	0
2	Hardware Icon #0 Blink Enable	0
1	Hardware Icon #0 Display Mode Select	0
0	Hardware Icon #0 Display Enable	0

Bit **Description**

7 **Hardware Cursor or Hardware Icon Select:**
When this bit is**:**
- 0, the hardware cursor is selected, updated, and displayed.
- 1, the hardware icon is selected, updated, and displayed.

6 **Hardware Icon Fine Horizontal Position [3]:**
This bit is part of a 4-bit fine-adjustment field for the hardware icon. This field is used with text that has 9- or 10-dot fonts (that is, character clocks), when in text or horizontally expanded graphics display modes.
- This bit [3] is the most-significant fine-adjustment bit of this field.
- Bits [2:0], the least-significant fine-adjustment bits of this field, are in Sequencer register SRX[7:5].
- Bits [10:3], the coarse horizontal position bits, are in Extension register SR10.

Register Format for 12-Bit Hardware Icon Horizontal Position

SR10[7:0]		SR2A[6]	SRX[7:5]	
11	4	3	2	0

- To extend the hardware icon horizontal position from 11 bits to 12 bits, and for details on this field, refer to Extension register SR10.
- When SR2A[7] is 1, the CPU can modify the hardware icon horizontal position.

NOTE: When enabling a horizontal expansion from 640 to 800, the hardware icon must be positioned within 10 dots.

5 **Hardware Icon #0 Display Memory Map Select:**
When this bit is:
- 0, display memory map 0 is selected for icon #0.
- 1, display memory map 1 is selected for icon #0.

4 **Hardware Icon #0 Vertical Scanline Double:**
When this bit is:
- 0, this function is disabled.
- 1, the following occurs:
  - — Icon #0 displays 128 scanlines, and each scanline is replicated vertically.
  - — Icon #0 extends down and forces all other icons down.

12.27 SR2A: Hardware Icon #0 Control and Cursor/Icon Select Register *(cont.)*

Bit	Description
3	**Hardware Icon #0 Horizontal Pixel Double:** When this bit is: • 0, this function is disabled. • 1, the following occurs: — Icon #0 displays 128 pixels, and each pixel is replicated horizontally. — Icon #0 expands to the right on the display.
2	**Hardware Icon #0 Blink Enable:** When this bit is: • 0, icon #0 is steady state. • 1, icon #0 blinks at one-half the text-cursor blink rate.
1	**Hardware Icon #0 Display Mode Select:** The hardware icon is always 2 bits/pixel, which is fetched from display memory and interpreted by the hardware icon in one of the following two ways. When this bit is: • 0, the 4-color mode for icon #0 is selected. • 1, the 3-colors-and-transparent mode is selected.
0	**Hardware Icon #0 Display Enable:** When this bit is: • 0, icon #0 is disabled. • 1, icon #0 is enabled.

12.28 SR2B: Hardware Icon #1 Control and Flat Panel Clock Drive Register

I/O Port Address: 3C5

Index: 2B

Bit	Description	Reset State
7	FPVDCLK and LLCLK High Output Drive Enable	0
6	CRT Monitor Sense Assist	0
5	Hardware Icon #1 Display Memory Map Select	0
4	Hardware Icon #1 Vertical Scanline Double	0
3	Hardware Icon #1 Horizontal Pixel Double	0
2	Hardware Icon #1 Blink Enable	0
1	Hardware Icon #1 Display Mode Select	0
0	Hardware Icon #1 Display Enable	0

Bit	Description
7	**FPVDCLK and LLCLK High Output Drive Enable:** When this bit is 1, FPVDCLK and LLCLK have double the normal output drive current to support high-load flat panels.
6	**CRT Monitor Sense Assist:** When this bit is: • 0, this function is disabled. • 1, the internal BLANK# signal to the DAC is disabled, thus allowing border color during the entire non-display time. • 1 *and* Attribute Controller register ARX[5] is 0, this bit can be used to force a CRT monitor display for accurate monitor sense, independent of the following: — Host CPU speed — Host CPU interrupts — The graphics display mode
5	**Hardware Icon #1 Display Memory Map Select:** When this bit is: • 0, display memory map 0 is selected for icon #1. • 1, display memory map 1 is selected for icon #1.
4	**Hardware Icon #1 Vertical Scanline Double:** When this bit is: • 0, this function is disabled. • 1, the following occurs: — Icon #1 displays 128 scanlines, and each scanline is replicated vertically. — Icon #1 extends down and forces all other icons down.
3	**Hardware Icon #1 Horizontal Pixel Double:** When this bit is: • 0, this function is disabled. • 1, the following occurs: — Icon #1 displays 128 pixels, and each pixel is replicated horizontally. — Icon #1 expands to the right on the display.

12.28 SR2B: Hardware Icon #1 Control and Flat Panel Clock Drive Register *(cont.)*

Bit	Description
2	**Hardware Icon #1 Blink Enable:** When this bit is: • 0, icon #1 is steady state. • 1, icon #1 blinks at one-half the text-cursor blink rate.
1	**Hardware Icon #1 Display Mode Select:** The hardware icon is always 2 bits/pixel, which is fetched from display memory and interpreted by the hardware icon in one of the following two ways. When this bit is: • 0, the 4-color mode for icon #1 is selected. • 1, the 3-colors-and-transparent mode is selected.
0	**Hardware Icon #1 Display Enable:** When this bit is: • 0, icon #1 is disabled. • 1, icon #1 is enabled.

12.29 SR2C: Hardware Icon #2 Control and Byte-Swap Enable Register

I/O Port Address: 3C5

Index: 2C

Bit	Description	Reset State
7	Hardware Cursor Vertical Expansion Tracking Enable	0
6	Partitions 1 and 2 Byte-Swap Enable	0
5	Hardware Icon #2 Display Memory Map Select	0
4	Hardware Icon #2 Vertical Scanline Double	0
3	Hardware Icon #2 Horizontal Pixel Double	0
2	Hardware Icon #2 Blink Enable	0
1	Hardware Icon #2 Display Mode Select	0
0	Hardware Icon #2 Display Enable	0

Bit **Description**

7 **Hardware Cursor Vertical Expansion Tracking Enable:**
When this bit is:
- 0, the hardware cursor vertical position does not automatically track hardware expansion.
- 1, the hardware cursor vertical position automatically tracks hardware vertical expansion.

6 **Partitions 1 and 2 Byte-Swap Enable:**
This bit enables byte swapping for Aperture Partitions 1 and 2, as shown in the following table.

SR2C[6]	Result	Partition 1 Byte Orientation	Partition 2 Byte Orientation
0	No byte swapping	1,2,3,4	1,2,3,4
1	Byte swapping take place	2,1,4,3	4,3,2,1

5 **Hardware Icon #2 Display Memory Map Select:**
When this bit is:
- 0, display memory map 0 is selected for icon #2.
- 1, display memory map 1 is selected for icon #2.

4 **Hardware Icon #2 Vertical Scanline Double:**
When this bit is:
- 0, this function is disabled.
- 1, the following occurs:
  - — Icon #2 displays 128 scanlines, and each scanline is replicated vertically.
  - — Icon #2 extends down and forces all other icons down.

12.29 SR2C: Hardware Icon #2 Control and Byte-Swap Enable Register *(cont.)*

Bit	Description
3	**Hardware Icon #2 Horizontal Pixel Double:** When this bit is: • 0, this function is disabled. • 1, the following occurs: — Icon #2 displays 128 pixels, and each pixel is replicated horizontally. — Icon #2 expands to the right on the display.
2	**Hardware Icon #2 Blink Enable:** When this bit is: • 0, icon #2 is steady state. • 1, icon #2 blinks at one-half the text-cursor blink rate.
1	**Hardware Icon #2 Display Mode Select:** The hardware icon is always 2 bits/pixel, which is fetched from display memory and interpreted by the hardware icon in one of the following two ways. When this bit is: • 0, the 4-color mode for icon #2 is selected. • 1, the 3-colors-and-transparent mode is selected.
0	**Hardware Icon #2 Display Enable:** When this bit is: • 0, icon #2 is disabled. • 1, icon #2 is enabled for display.

12.30 SR2D: Hardware Icon #3 Control and Icon/Cursor Memory Access Register

I/O Port Address: 3C5

Index: 2D

Bit	Description	Reset State
7	Hardware Icon and Cursor 64-Bit Memory Access Enable	0
6	Hardware Icon and Cursor 32-Bit Memory Access Enable	0
5	Hardware Icon #3 Display Memory Map Select	0
4	Hardware Icon #3 Vertical Scanline Double	0
3	Hardware Icon #3 Horizontal Pixel Double	0
2	Hardware Icon #3 Blink Enable	0
1	Hardware Icon #3 Display Mode Select	0
0	Hardware Icon #3 Display Enable	0

Bit	Description
7	**Hardware Icon and Cursor 64-Bit Memory Access Enable:** This bit enables 64-bit writes and reads for hardware icons and cursor in standard VGA display modes. When linear addressing is selected (that is, Extension register CR36[7] is 1), *and* this bit is: • 0, the host CPU can access only 32-bit display memory for hardware icons and cursors. With this bit setting, SR2D[6] must be set to 1. • 1, the host CPU can access the entire 64-bit display memory so that icons and cursors can attain the proper icon/cursor display.
6	**Hardware Icon and Cursor 32-Bit Memory Access Enable:** This bit enables either 32- or 64-bit reads, for the display of icons and cursors that use 64-bit-wide memory. When this bit is: • 0, the icons/cursors can be stored in 64-bit-wide display memory, regardless if the display device is using a VGA display mode or not. • 1, the icons/cursors are displayed according to the type of display mode the display device is using. (That is, the icons/cursors are displayed in either a VGA display mode or an extended VGA display mode, depending on how wide the memory access is). For example, when a display device is using a VGA display mode, by using SR2D[7], the icon and cursor map can be stored as either 32 bits wide (that is, SR2D[7] is 0) or 64 bits wide (that is, SR2D[7] is 1).
5	**Hardware Icon #3 Display Memory Map Select:** When this bit is: • 0, display memory map 0 is selected for icon #3. • 1, display memory map 1 is selected for icon #3.
4	**Hardware Icon #3 Vertical Scanline Double:** When this bit is: • 0, this function is disabled. • 1, the following occurs: — Icon #3 displays 128 scanlines, and each scanline is replicated vertically. — Icon #3 extends down and forces all other icons down.

12.30 SR2D: Hardware Icon #3 Control and Icon/Cursor Memory Access Register *(cont.)*

Bit	Description
3	**Hardware Icon #3 Horizontal Pixel Double:** When this bit is: • 0, this function is disabled. • 1, the following occurs: — Icon #3 displays 128 pixels, and each pixel is replicated horizontally. — Icon #3 extends down and forces all other icons down.
2	**Hardware Icon #3 Blink Enable:** When this bit is: • 0, icon #3 is steady state. • 1, icon #3 blinks at one-half the text-cursor blink rate.
1	**Hardware Icon #3 Display Mode Select:** The hardware icon is always 2 bits/pixel, which is fetched from display memory and interpreted by the hardware icon in one of the following two ways. When this bit is: • 0, the 4-color mode for icon #3 is selected. • 1, the 3-colors-and-transparent mode is selected.
0	**Hardware Icon #3 Display Enable:** When this bit is: • 0, icon #3 is disabled. • 1, icon #3 is enabled for display.

12.31 SR2E: Hardware Cursor Horizontal Position Extension Register

I/O Port Address: 3C5

Index: 2E

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Hardware Icon #0 Address Map Select [1]	0
1	Hardware Icon #0 Address Map Select [0]	0
0	Hardware Cursor Fine Horizontal Position [3]	0

Bit **Description**

7:3 **Reserved**

2:1 **Hardware Icon #0 Address Map Select [1:0]:**
When this field is:
- '00', each icon has two memory maps assigned to it.
- 'non-zero', only hardware icon #0 can be used.
  - — Hardware icon #0 can have up to eight memory maps.
  - — The other hardware icons (#1, #2, and #3) must be disabled.
  - — The number in SR2E[2:1] points to the pair of two icon maps selected by SR2A[5], but in this case, all maps go to icon #0 for display.
  - — In this order of significance, SR2E[2:1] and SR2A[5] select the eight memory maps for hardware icon #0.

0 **Hardware Cursor Fine Horizontal Position [3]:**
This bit is part of a 4-bit fine-adjustment field for a 12-bit hardware cursor. This field is used with text that has fonts that use character clocks that are 10 dot-clocks long, when in text or horizontally expanded graphics display modes.
- This bit [3] is the most-significant fine-adjustment bit of this field.
- Bits [2:0], the least-significant fine-adjustment bits of this field, are in Sequencer register SRX[7:5].
- Bits [10:3], the coarse horizontal position bits, are in Extension register SR10.

Register Format for the 12-Bit HW Cursor Horizontal Position

SR10[7:0]		SR2E[0]	SRX[7:5]	
11	4	3	2	0

- To extend the hardware cursor horizontal position from 11 bits to 12 bits, and for details on this field, refer to Extension register SR10.
- When Extension register SR2A[7] is 0, the CPU can modify the hardware cursor horizontal position.
- In non-expanded graphics display modes, this bit is always 0.

NOTE: When enabling a horizontal expansion from 640 to 800, the hardware cursor must be positioned within 10 dots.

12.32 SR2F: HFA FIFO Threshold for Surrounding Graphics Register

I/O Port Address: 3C5

Index: 2F

Bit	Description	Reset State
7	Programmable Output Pin PROG2	0
6	Programmable Output Pin PROG1	0
5	Programmable Output Pin PROG0	0
4	PCLKO Disable	0
3	HFA FIFO Threshold for Surrounding Graphics [3]	0
2	HFA FIFO Threshold for Surrounding Graphics [2]	0
1	HFA FIFO Threshold for Surrounding Graphics [1]	0
0	HFA FIFO Threshold for Surrounding Graphics [0]	0

Bit	Description
7:5	**Programmable Output Pins PROG[2:0]:** When CR30[6] is 0, these bits control the active logic level of the PROG[2:0] output pins, which are used to control peripheral devices. When these bits are: • 0, the associated PROG output pin is forced low. • 1, the associated PROG output pin is forced high. When CR30[6] is 1, the PROG2 pin is the NTSC/PAL output, and the PROG0 pin is the TV-ON output. However, PROG1 is still programmable with SR2F[6].
4	**PCLKO Disable:** The PCLKO clock is selected when SR23[4] is 1 and SR24[4] is 0. When this bit is: • 0, PCLKO is enabled at all times. • 1, PCLKO is disabled in CRT-only mode; it is enabled only when Extension register CR80[0] = 1 (that is, the flat panel is enabled).
3:0	**Half-Frame Accelerator FIFO Threshold for Surrounding Graphics [3:0]:** This 4-bit field affects the half-frame accelerator read FIFO for dual-scan STN flat panels. The half-frame accelerator read FIFO is 8 data-stages deep and 64 bits wide, but it is configured as 16 data-stages deep by 32 bits wide. This field controls how many 32-bit data stages are empty in the half-frame accelerator read FIFO before a new request is made for a refill of the half-frame accelerator read FIFO. (At the same time that the half-frame accelerator read FIFO is emptied, it is refilled. Example: If SR2F[3:0] = 4h, after only 4 of the 16 half-frame accelerator read FIFO stages are empty, a new request is made for new half-frame accelerator cycles. For this example, program a read FIFO threshold that is: • Never lower than 4h. • Low (4h) for 4 data stages for 16-bpp and 24-bpp modes, even for a color dual-scan STN flat panel, in order to minimize CRT-FIFO latency. • Medium (6h) for 6 data stages for 4-bpp and 8-bpp modes. • Up to Fh (that is, the FIFO is empty) for all other cases. • Never higher than Fh.

12.33 SR32: HFA FIFO Threshold in VW and DAC IREF Power Control Register

I/O Port Address: 3C5

Index: 32

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	On-Chip DAC IREF Power Control	0
4	Reserved	
3	Reserved	
2	Half-Frame Accelerator FIFO Threshold in VW [2]	0
1	Half-Frame Accelerator FIFO Threshold in VW [1]	0
0	Half-Frame Accelerator FIFO Threshold in VW [0]	0

This register controls PCI bus access speed parameters and half-frame accelerator memory bandwidth usage.

Bit	Description
7:6	**Reserved**
5	**On-Chip DAC IREF Power Control:** When this bit is: • 0, the power to the on-chip DAC IREF circuit is turned off. • 1, the power to the on-chip DAC IREF circuit is turned on.
4:3	**Reserved**
2:0	**Half-Frame Accelerator FIFO Threshold in VW [2:0]:** • This 3-bit field allows another level of memory bandwidth optimization when using dual-scan STN flat panels with the VW (Video Window). • This field determines the number of CAS# cycles in the half-frame accelerator FIFO cycle in the VW. That is: — '000' = no CAS# cycles. — '001' = one CAS# cycle. — '111' = seven CAS# cycles, and so forth.

12.34 SR33: Spare Sequencer Register

I/O Port Address: 3C5

Index: 33

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

Bit	Description
7:0	**Reserved**

12.35 SR34: Host CPU Cycle Stop Control Register

I/O Port Address: 3C5

Index: 34

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Terminate Paged Host CPU Cycles when Re-starting is Disabled	0
3	Stop Host CPU Cycle before Half-Frame Accelerator Cycle	0
2	Stop Host CPU Cycle before V-Port Cycle	0
1	Stop Host CPU Cycle before VW Cycle	0
0	Stop Host CPU Cycle before CRT Monitor Cycle	0

Bit	Description
7:5	**Reserved**
4	**Terminate Paged Host CPU Cycles when Re-starting Is Disabled:** When this bit is: • 0, this function is disabled. • 1, then for each register bit SR34[3:0] that is set to 1 so that the host CPU cycle is prevented from re-starting, the host CPU cycle is stopped immediately.
3	**Stop Host CPU Cycle before Half-Frame Accelerator Cycle:** When this bit is: • 0, this function is disabled. • 1, a host CPU cycle is prevented from starting when *n*-1 Half-Frame Accelerator FIFO levels are empty. (The *n* value is the threshold value programmed in Extension register bits SR2F[3:0] and SR32[2:0].)
2	**Stop Host CPU Cycle before V-Port Cycle:** When this bit is: • 0, this function is disabled. • 1, a host CPU cycle is prevented from starting when *n*-1 V-Port FIFO levels are filled. (The *n* value is the threshold value programmed in Extension register bit CR51[7:5] for the VW and in Extension register bits CR5A[2:0] for the surrounding graphics.)
1	**Stop Host CPU Cycle before VW Cycle:** When this bit is: • 0, this function is disabled. • 1, a host CPU cycle is prevented from starting immediately before VW circuitry generates a cycle request.
0	**Stop Host CPU Cycle before CRT Monitor Cycle:** When this bit is: • 0, this function is disabled. • 1, a host CPU cycle is prevented from starting immediately before the CRT FIFO circuitry generates a cycle request.

12.36 GR9: Display Memory Offset 0 Register

I/O Port Address: 3CF

Index: 9

Bit	Description	Reset State
7	Display Memory Offset 0 [7]	0
6	Display Memory Offset 0 [6]	0
5	Display Memory Offset 0 [5]	0
4	Display Memory Offset 0 [4]	0
3	Display Memory Offset 0 [3]	0
2	Display Memory Offset 0 [2]	0
1	Display Memory Offset 0 [1]	0
0	Display Memory Offset 0 [0]	0

This register is used to access up to 2 Mbytes of display memory with up to 16-Kbyte granularity. See Appendix F for more information on memory mapping techniques.

Bit **Description**

7:0 **Display Memory Offset 0 [7:0]:**
This register is enabled only when one of the following conditions is true:
- GRB[0] is 0.
- GRB[0] is 1, *and* CPU address bit AD15 is 0.

When this register is enabled, *and* GRB[5] is:
- 0, then:
  - — The GR9 offset value is added to the contents of XA (bus addresses AD[19:12]) to provide XMA, an address into display memory.
  - — Access is for 1 Mbyte of display memory with 4-Kbyte granularity.
- 1, then:
  - — The GR9 offset value is added to the contents of XA (bus addresses AD[20:14]) to provide XMA, an address into display memory.
  - — Access is for up to 2 Mbytes of display memory with 16-Kbyte granularity.

XMA. XMA is the display memory address, prior to modification by address wrap controls.

XMA = (Bus Address XA) + (value from Extension register GR9 or GRA).

XA. XA is the address on the bus, with bits AD16 and AD15 possibly forced to a 0 as indicated in the following table.

(Continued)

12.36 GR9: Display Memory Offset 0 Register *(cont.)*

Bit	Description
7:0 *(cont.)*	**Display Memory Offset 0 [7:0]** *(cont.)*:

Configuration		Bus Address XA Is:		
When Display Memory Is:	**And Register Setting:**	**16**	**15**	**14:0**
128 Kbytes	GR6[3:2] is '00'	AD16	AD15	AD[14:0]
64 Kbytes	GR6[3:2] is '01' *and* GRB[0] is 0 (Display Memory Offset 1 disabled)	0	AD15	AD[14:0]
64 Kbytes	GR6[3:2] is '01' *or* GRB[0] is 1 (Display Memory Offset 1 enabled)	0	0	AD[14:0]

The XA bus address is summed with the contents of a Display Memory Offset register with one of three relative alignments, according to the configuration indicated in the three tables that follow:

1 Mbyte Memory, 4-Kbyte Granularity, VGA Mapping								
Bus Address (XA)	0	0	0	XA16	XA15	AD14	AD13	AD12
+ Display Memory Offset Value	Offset[7]	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]
= Display Memory Address (XMA)	XMA19	XMA18	XMA17	XMA16	XMA15	XMA14	XMA13	XMA12

2 Mbytes Memory, 16-Kbyte Granularity, VGA Mapping									
Bus Address	0	0	0	0	XA16	XA15	AD14	AD13	AD12
+ Display Memory Offset Value	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]	0	0
= Display Memory Address	XMA20	XMA19	XMA18	XMA17	XMA16	XMA15	XMA14	XMA13	XMA12

1 or 2 Mbytes Memory, 16-Kbyte Granularity, Linear Addressing									
Bus Address	AD20	AD19	AD18	AD17	AD16	AD15	AD14	AD13	AD12
+ Display Memory Offset Value	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]	0	0
= Display Memory Address	XMA20	XMA19	XMA18	XMA17	XMA16	XMA15	XMA14	XMA13	XMA12

12.37 GRA: Display Memory Offset 1 Register

I/O Port Address: 3CF

Index: A

Bit	Description	Reset State
7	Display Memory Offset 1 [7]	0
6	Display Memory Offset 1 [6]	0
5	Display Memory Offset 1 [5]	0
4	Display Memory Offset 1 [4]	0
3	Display Memory Offset 1 [3]	0
2	Display Memory Offset 1 [2]	0
1	Display Memory Offset 1 [1]	0
0	Display Memory Offset 1 [0]	0

This register is used to access up to 2 Mbytes of display memory with up to 16-Kbyte granularity.

Bit	Description
7:0	**Display Memory Offset 1 [7:0]:** When Extension register bit GRB[0] is: • 0, this register is disabled. • 1, this register is enabled. In addition, when: — CPU bus address bit AD15 is 1: — The contents of GRA[7:0] are added to the contents of host CPU bus address bits AD[19:12]. — This action provides access to up to 1 Mbyte of addresses into display memory, with 4-Kbyte granularity. — Extension register bit GRB[5] is 1: — The contents of GRA[6:0] are added to the contents of host CPU bus address bits AD[20:14]. — This action provides access to up to 2 Mbytes of addresses into display memory, with 16-Kbyte granularity.

12.38 GRB: Graphics Controller Mode Extensions Register

I/O Port Address: 3CF

Index: B

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Display Memory Offset Granularity	0
4	16-Bit Pixel Enhanced Write Enable	0
3	Reserved	
2	Extended Write Mode Enable	0
1	By-8 Addressing Enable	0
0	Display Memory Offset 1 Enable	0

This register is used to enable or disable extended write modes, for enhanced performance.

Bit — **Description**

7:6 — **Reserved**

5 — **Display Memory Offset Granularity:**
When this bit is set to:
- 0, the offset granularity for the display memory address is set to 4 Kbytes.
- 1, the following conditions are true:
  - — The offset granularity for the display memory address is set to 16 Kbytes.
  - — Extension registers GR9 and GRA are redefined as containing host CPU bus address bits AD[6:0]. In this case:
    - — The GR9 and GRA bits are added to CPU bus address bits AD[20:14] to provide access to 2 Mbytes of display memory with 16-Kbyte granularity.
    - — Extension register SR7[4] (the least-significant bit of a 1-Mbyte address page) becomes a ‘don’t care’.
    - — Linear address memory mapping becomes 2 Mbytes on any 2-Mbyte boundary.

4 — **16-Bit Pixel Enhanced Write Enable:**
GRB[2] must be 1 in order to enable this bit. When both GRB[2] and GRB[4] are set to 1, the CL-GD7556 executes the following enhanced write modes when Extended Write modes 4 and 5 are enabled and executed:
- **By-16 Addressing Enabled:**
  The system address is shifted by 4, relative to true packed-pixel addressing, so that each system byte address points to a different 8-pixel (that is, 16-byte) block in display memory.
- **16-Byte Transfer Enabled:**
  Up to 16 bytes (that is, eight 2-byte pixels) can be written into display memory for each CPU byte transfer.
- **Extension Registers GR10 and GR11 Enabled:**
  GR10 and GR11 are enabled as foreground and background color extensions.
- **Sequencer Register SR2 Doubling Enabled:**
  Each bit of SR2 is used as a pixel write mask for two bytes (that is, 1 pixel).

12.38 GRB: Graphics Controller Mode Extensions Register *(cont.)*

Bit	Description
3	**Reserved**
2	**Extended Write Mode Enable:** When this bit is 1: • GRB[4] is enabled. When GRB[4] = 1, it enables enhanced writes for 16-bit pixels. • Graphics Controller register: — GR0 is extended from 4 bits to 8 bits. — GR1 is extended from 4 bits to 8 bits. — Bit GR5[2] is enabled. When GR5[2] = 1, it enables Extended Write modes 4 and 5. • Sequencer register SR2 is extended from 4 bits to 8 bits. • 8-Byte transfer is enabled. In this case, up to 8 bytes (that is, 8 pixels) can be written into display memory for each CPU byte transferred. • *And* GRB[4] is 1, up to 16 bytes (that is, eight 2-byte pixels) can be written into display memory for color expansion. • *And* it is then cleared to 0, Graphics Controller register bits GR0[7:4] and GR1[7:4] are cleared to 0.
1	**By-8 Addressing Enable:** When GRB[4] is: • 0 *and* this bit is: — 0, this function is disabled. — 1, the system address is shifted by 3, relative to true packed-pixel addressing, so that each system byte address points to a different 8-pixel (that is, 8-byte) block in display memory. • 1, this bit is a ‘don’t care’.
0	**Display Memory Offset 1 Enable:** When this bit is programmed to • 0, the value in system address AD15 is ignored. — As a result, Extension register GR9 (that is, Display Memory Offset 0) is always selected. As a result, one 64-Kbyte segment of display memory is selected (and never two 32-Kbyte segments). — This bit must always be cleared to 0 for 1 Mbyte of linear addressing. • 1, the value in system address AD15 is used to select either Display Memory Offset 0 (that is, Extension register GR9) or Display Memory Offset 1 (that is, Extension register GRA). — When system address AD15 is 0, Display Memory Offset 0 is selected. — When system address AD15 is 1, Display Memory Offset 1 is selected.

12.39 GRC: Color Key Compare Value and Chroma Key Y Minimum Register

I/O Port Address: 3CF

Index: C

Bit	Description	Reset State
7	Color Key Compare Value / Chroma Key Y Minimum [7]	1
6	Color Key Compare Value / Chroma Key Y Minimum [6]	1
5	Color Key Compare Value / Chroma Key Y Minimum [5]	1
4	Color Key Compare Value / Chroma Key Y Minimum [4]	1
3	Color Key Compare Value / Chroma Key Y Minimum [3]	1
2	Color Key Compare Value / Chroma Key Y Minimum [2]	1
1	Color Key Compare Value / Chroma Key Y Minimum [1]	1
0	Color Key Compare Value / Chroma Key Y Minimum [0]	1

The 8-bit value in this register is compared to graphics/video data when occlusion is enabled for a VW.

Bit **Description**

7:0 **Color Key Compare Value [7:0]:**
This register is enabled for a color key compare when the following are *both* true:
- Extension register bit CR42[0] is 0 (that is, the chroma key is disabled).
- Extension register CR3F[5] is 1 (that is, occlusion is enabled).

A color key compare is possible for one of two types of pixel modes:
- 8-bit/pixel mode.
  - — An 8-bit color key compare occurs when one of the following is true:
    - — Extension register SR7[3:1] = ‘000’.
    - — Extension register SR7[3:1] = ‘011’ *and* Extension register CR1D[3] = 0 (so that only the low byte of a 16-bit pixel is selected).
  - — In this case, only 8 bits are used for the color key compare.
  - — When there is a match between the 8-bit value in this register and the graphics data value, the graphics data pixel is replaced with video data, using the GRD color mask.
- 16-bit/pixel mode.
  - — A 16-bit color key compare occurs when the following are *both* true: Extension register SR7[3:1] = ‘011’ *and* Extension register CR1D[3] = 1.
  - — In this case, all 16 bits of a 16-bit pixel are used for the color key compare.
    - — The low byte of the VGA data is compared to the value in GRC.
    - — The high byte of the VGA data is compared to the value in GRD.
    - — No mask is available.

Pixel Mode	Color Key Bytes Are Compared to:		Setup and Control Bits
	GRC[7:0]	GRD[7:0]	
8 bit/pixel	Every Byte	Byte Mask	SR7[3:1] = ‘000’
16 bit/pixel	Low Byte	Byte Mask	SR7[3:1] = ‘011’, CR1D[3] = 0
16 bit/pixel	Low Byte	High Byte	SR7[3:1] = ‘011’, CR1D[3] = 1

12.39 GRC: Color Key Compare Value and Chroma Key Y Minimum Register *(cont.)*

Bit	Description
7:0	**Chroma Key Y Minimum [7:0]:** When occlusion is enabled (that is, Extension register CR3F[5] is 1), this 8-bit field is used in combination with GRD[7:0] to determine when the VW displays graphics instead of video. On a pixel-by-pixel basis, the VW displays graphics instead of video under the following conditions: • The chroma key is selected (that is, Extension register bit CR42[0] is 1). • The Y luminance value in the VW is in the range defined by the following: — The chroma key Y luminance minimum of GRC[7:0]. — The chroma key Y luminance maximum of GRD[7:0].

12.40 GRD: Color Key Compare Mask and Chroma Key Y Maximum Register

I/O Port Address: 3CF

Index: D

Bit	Description	Reset State
7	Color Key Compare Mask / Chroma Key Y Maximum [7]	0
6	Color Key Compare Mask / Chroma Key Y Maximum [6]	0
5	Color Key Compare Mask / Chroma Key Y Maximum [5]	0
4	Color Key Compare Mask / Chroma Key Y Maximum [4]	0
3	Color Key Compare Mask / Chroma Key Y Maximum [3]	0
2	Color Key Compare Mask / Chroma Key Y Maximum [2]	0
1	Color Key Compare Mask / Chroma Key Y Maximum [1]	0
0	Color Key Compare Mask / Chroma Key Y Maximum [0]	0

The 8-bit value in this register is compared to graphics/video data when occlusion is enabled for a VW.

Bit **Description**

7:0 **Color Key Compare Mask [7:0]:**

This register is enabled for a color key compare when the following are *both* true:

- Extension register bit CR42[0] is 0 (that is, the chroma key is disabled).
- Extension register CR3F[5] is 1 (that is, occlusion is enabled).

This register is used for two types of pixel modes:

- 8-bit/pixel mode.
  - — An 8-bit/pixel mode occurs when one of the following is true:
    - — Extension register SR7[3:1] is '000'.
    - — Extension register SR7[3:1] is '011' *and* Extension register CR1D[3] is 0 (so that only the low byte of a 16-bit pixel is selected).
  - — In this case, this register contains an 8-bit mask under which the color key compare of GRC is made for occlusion.
  - — When any GRD bit is 1, the corresponding graphics data bit in GRC[7:0] is masked out and *does not* participate in the color comparison.
- 16-bit/pixel mode.
  - — A 16-bit/pixel mode occurs when the following are *both* true: Extension register SR7[3:1] is '011' *and* Extension register CR1D[3] is 1.
  - — In this case, this register is the color-key compare for the high byte. For details, refer to Extension register GRC[7:0].

Register Format for the 16-Bit Color Key Compare Mask

GRD[7:0]		GRC[7:0]	
15	8	7	0

7:0 **Chroma Key Y Maximum [7:0]:**

When occlusion is enabled (that is, Extension register CR3F[5] is 1), this 8-bit field is used in combination with GRC[7:0] to determine when the VW displays graphics instead of video.

- For details, refer to GRC[7:0]

12.41 GRE: DPMS Control and VCLK/2 Enable Register

I/O Port Address: 3CF

Index: E

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	System-Level Power Management	0
3	Reserved	
2	Display Power Management Signaling (Green PC) Control [1]	0
1	Display Power Management Signaling (Green PC) Control [0]	0
0	VCLK Output Divided By Two	0

This register contains an 8-bit value that is compared to graphics data when occlusion is enabled for a VW.

Bit	Description
7:5	**Reserved**
4	**System-Level Power Management:** When this bit is set to 1, it overrides the following: • External/General register bit MISC[1] (that is, it does not allow the host CPU to access display memory). • Sequencer register bit SR1[5] (that is, the CRT monitor screen refresh is disabled).
3	**Reserved**
2:1	**Display Power Management Signaling (Green PC) Control [1:0]:** These 2 bits control the CRT monitor power as required by the VESA DPMS (Display Power Management Signaling) specification, as shown in the following table:

DPMS Proposed States		GRE		VSYNC Activity	HSYNC Activity	DAC Power	CL-GD7556 Comparison
Name[a]	Power Level for CRT Monitor Display Screen	[2]	[1]				
On	Full operation	0	0	Pulsing	Pulsing	On	Active
Standby	Optional state with minimum power reduction	0	1	62.5 Hz	Static at MISC[6] inactive level	Off	Active, Standby, Suspend
Suspend	Significant reduction of power consumption	1	0	Static at MISC[7] inactive level	32 kHz	Off	Active, Suspend
Off	Lowest level of power consumption	1	1	Static at MISC[7] inactive level	Static at MISC[6] inactive level	Off	Active, Suspend

[a] These DPMS Standby and Suspend power levels are not the same as the CL-GD7556 power management modes with the same names. For details, refer to the appendixes.

(Continued)

12.41 GRE: DPMS Control and VCLK/2 Enable Register *(cont.)*

Bit	Description
2:1 (*cont.*)	**Display Power Management Signaling (Green PC) Control [1:0]** *(cont.)*: Because the DPMS CRT power-management modes are not related to the CL-GD7556 controller power-management modes, they can be independently programmed, except for the following restrictions: • DPMS Suspend mode: — The VGA BIOS can program any DPMS power-saving mode for the CRT, but the VGA BIOS programming must be done prior to placing the CL-GD7556 into Suspend mode. — Extension register CR8D[4] must be 0 (that is, the 32-kHz input to the CL-GD7556 must be used). This bit setting provides any synchronization pulse required by the DPMS. • DPMS Standby mode: — The CL-GD7556 Standby mode is timer-driven (that is, hardware-controlled). As a result, — The DPMS Standby signal must be forced by hardware. — Software control of the DPMS Standby mode is not allowed. • Flat panel-only mode: — When the CL-GD7556 is in flat panel-only mode, the VGA BIOS must set GRE[2:1] to '11' to power off any CRT monitor that can be connected to the notebook computer. • The inactive (that is, static) and active signal levels for VSYNC and HSYNC are determined by the polarity selection in External/General register MISC[7:6]. — When MISC[7] = 1, the VSYNC signal is active-high. — When MISC[6] = 1, the HSYNC signal is active-high.
0	**VCLK Output, Divided By Two:** When this bit is: • 0, the CL-GD7556 operates normally. • 1, the CL-GD7556 emulates external DAC Clocking Mode 1. — The VCLK leading edge can be used to clock a 16-bit data pixel low byte. — The VCLK trailing edge can be used to clock a 16-bit data pixel high byte. — The option of setting this bit to 1: — Works only for the CRT-only mode. — Does not work for the flat panel-only or SimulSCAN mode. When this bit is 1, the clock to the flat panel section is divided by two, which prevents the flat panel from working properly.

12.42 GR10: Background Color Expansion #1 Register

I/O Port Address: 3CF

Index: 10

Bit	Description	Reset State
7	Background Color [15]	0
6	Background Color [14]	0
5	Background Color [13]	0
4	Background Color [12]	0
3	Background Color [11]	0
2	Background Color [10]	0
1	Background Color [9]	0
0	Background Color [8]	0

For 16-bit color expansion of background color, this register contains the most-significant 8 bits. For more information on color expansion, refer to the *CL-GD7556 Software Reference Manual*.

Bit **Description**

7:0 **Background Color [15:8]:**

For 16-bit color expansion of the background color:

- The following bits must be set:
  - — Extension register bits SR7[3:1] must be set to '011'.
  - — Extension register bit GRB[4] must be set to 1.
- Bits [15:8] in this register GR10 are Background Color byte 1, the most-significant 8 bits of the 16-bit background color field. These bits are sent to display memory map planes 1 and 3.
- Bits [7:0] in Graphics Controller register GR0 are Background Color byte 0, the least-significant 8 bits of the background color field. These bits are sent to display memory map planes 0 and 2.

Register Format for 16-Bit Background Color Expansion

High Byte		Low Byte	
GR10[7:0]		GR0[7:0]	
15	8	7	0

12.43 GR11: Foreground Color Expansion #1 Register

I/O Port Address: 3CF

Index: 11

Bit	Description	Reset State
7	Foreground Color [15]	0
6	Foreground Color [14]	0
5	Foreground Color [13]	0
4	Foreground Color [12]	0
3	Foreground Color [11]	0
2	Foreground Color [10]	0
1	Foreground Color [9]	0
0	Foreground Color [8]	0

For 16-bit color expansion of foreground color, this register contains the most-significant 8 bits. For 24-bit color expansion of foreground color, this register contains the green color byte. For more information on color expansion, refer to the *CL-GD7556 Software Reference Manual*.

Bit **Description**

7:0 **Foreground Color [15:8]:**

For 16-bit color expansion of the foreground color:

- The following bits must be set:
  - — Extension register bits SR7[3:1] must be set to '011'.
  - — Extension register bits GRB[4] must be set to 1.
- Bits [15:8] in this register GR11 are Foreground Color byte 1, the most-significant 8 bits of the 16-bit foreground color field. These bits are sent to display memory map planes 1 and 3.
- Bits [7:0] in Graphics Controller register GR1 are Foreground Color byte 0, the least-significant 8 bits of the 16-bit foreground color field. These bits are sent to display memory map planes 0 and 2.

For 24-bit color expansion of foreground color:

- Extension register bits SR7[3:1] must be set to '010'.
- Bits [23:16], in Extension register GR13, represent the red color byte.
- Bits [15:8], in this register GR11, represent the green color byte.
- Bits [7:0], in Graphics Controller register GR1, represent the blue color byte.

Register Format for 16-Bit Foreground Color Expansion

High Byte		Low Byte	
GR11[7:0]		GR1[7:0]	
15	8	7	0

Register Format for 24-Bit Foreground Color Expansion

RED		GREEN		BLUE	
GR13[7:0]		GR11[7:0]		GR1[7:0]	
23	16	15	8	7	0

12.44 GR13: Foreground Color Expansion #2 Register

I/O Port Address: 3CF

Index: 13

Bit	Description	Reset State
7	Foreground Color [23]	0
6	Foreground Color [22]	0
5	Foreground Color [21]	0
4	Foreground Color [20]	0
3	Foreground Color [19]	0
2	Foreground Color [18]	0
1	Foreground Color [17]	0
0	Foreground Color [16]	0

For 24-bit color expansion of foreground color, this register contains the red color byte. For more information on color expansion, refer to the *CL-GD7556 Software Reference Manual*.

Bit **Description**

7:0 **Foreground Color [23:16]:**

For 24-bit color expansion of foreground color:

- Extension register bits SR7[3:1] must be set to ‘010’.
- Bits [23:16] in this register GR13 are Foreground Color byte 2, the red color byte.
- Bits [15:8] in Extension register GR11 are Foreground Color byte 1, the green color byte.
- Bits [7:0] in Graphics Controller register GR1 are Foreground Color byte 0, the blue color byte.

Register Format for 24-Bit Foreground Color Expansion

RED	GREEN	BLUE
GR13[7:0]	GR11[7:0]	GR1[7:0]
23 16	15 8	7 0

12.45 GR16: Scanline Counter Readback Low Register

I/O Port Address: 3CF

Index: 16

Bit	Description	Access	Reset State
7	Scanline Counter Readback [7]	R	0
6	Scanline Counter Readback [6]	R	0
5	Scanline Counter Readback [5]	R	0
4	Scanline Counter Readback [4]	R	0
3	Scanline Counter Readback [3]	R	0
2	Scanline Counter Readback [2]	R	0
1	Scanline Counter Readback [1]	R	0
0	Scanline Counter Readback [0]	R	0

This register contains the least-significant 8 bits of a 10-bit field that reads back the 10-bit Scanline Counter field.

Bit	Description
7:0	**Scanline Counter Readback [7:0]:** These bits [7:0] are the least-significant 8 bits of the 10-bit read-only Scanline Counter Readback field. These bits echo the value of the 8 least-significant bits of the 10-bit value for the Scanline Counter. • Bits [9:8], the most-significant 2 bits of the 10-bit Scanline Counter Readback field, echo the value of the 2 most-significant bits of the 10-bit value for the Scanline Counter. These bits are in GR17[1:0].

Register Format for 10-Bit Scanline Counter Readback

GR17[1:0]		GR16[7:0]	
9	8	7	0

12.46 GR17: Scanline Counter Readback High Register

I/O Port Address: 3CF

Index: 17

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Scanline Counter Readback [9]	R	0
0	Scanline Counter Readback [8]	R	0

This register contains the most-significant 2 bits of a 10-bit field that reads back the 10-bit Scanline Counter field.

Bit	Description
7:2	**Reserved**
1:0	**Scanline Counter Readback [9:8]:** These bits are the most-significant 2 bits of the 10-bit read-only Scanline Counter Readback field.

Register Format for 10-Bit Scanline Counter Readback

GR17[1:0]		GR16[7:0]	
9	8	7	0

- For details on this field, refer to GR16.

12.47 GR18: EDO RAM Control Register

I/O Port Address: 3CF

Index: 18

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Force DRAM Pins to High Impedance	0
3	Perform One DRAM Refresh per Scanline	0
2	EDO DRAM Long RAS# Cycle Enable	0
1	Decreased Timing for Write CAS# Following Read CAS#	0
0	Decreased Timing for WE# Active Following a Read Cycle	0

Bit	Description
7:5	**Reserved**
4	**Force DRAM Pins to High Impedance:** This bit controls when the following pins are high impedance: • DRAM address and data pins: MA[9:0] and MD[63:0] • DRAM control pins: — CAS#/WE# — CAS[7:0]# — RAS[1:0]# — WE[7:0]# When this bit is set to: • 0, the DRAM interface is normal operation. • 1, the DRAM address, data, and control pins are forced to high impedance following the next low-to-high transition of RAS#.
3	**Perform One DRAM Refresh per Scanline:** When this bit is: • 0, CRT Controller register CR11[6] controls whether three or five DRAM refresh cycles per HSYNC scanline are selected. • 1, CRT Controller register CR11[6] is overridden and one CAS#-before-RAS# DRAM refresh cycle is performed for each HSYNC scanline. (This option must not be selected unless HSYNC is greater than 56 kHz.)

12.47 GR18: EDO RAM Control Register *(cont.)*

Bit **Description**

2 **EDO DRAM Long RAS# Cycle Enable:**
When this bit is set to 1:

- The CL-GD7556 generates EDO DRAM timing.
- This bit forces an extra MCLK cycle between the read and write CAS# of BitBLT operations (such as DSTINVERT) that modify the destination using extended page cycles.
- This bit works in combination with Extension register bits SRF[2] and SR20[6] to determine the number of MCLKs used for each RAS# cycle, as shown in the following table:

SR20[6]	GR18[2]	SRF[2]	Length of RAS# Cycle	Type Of RAS# Cycle
0	0	0	7 MCLKs	4 MCLKs low and 3 MCLKs high
0	0	1	6 MCLKs	3.5 MCLKs low and 2.5 MCLKs high
0	1	0	8 MCLKs	5 MCLKs low and 3 MCLKs high
1	1	0	9 MCLKs	5 MCLKs low and 4 MCLKs high

1 **Decreased Timing for Write CAS# Following Read CAS#:**
When this bit is 1, the timing for a write CAS# immediately following a read CAS# is decreased by one MCLK cycle as shown in the following table:

GR18[1]	MCLK Cycles	
	GR18[2] = 0	GR18[2] = 1 (EDO DRAM setting)
0	3 MCLKs	4 MCLKs
1	3 MCLKs – 1 MCLK = 2 MCLKs	4 MCLKs – 1 MCLK = 3 MCLKs

0 **Decreased Timing for WE# Active Following a Read Cycle:**
When this bit is 1, the timing to make WE# active for a cycle immediately following a read cycle is decreased by one MCLK cycle as shown in the following table:

GR18[0]	MCLK Cycles	
	GR18[2] = 0	GR18[2] = 1 (EDO DRAM setting)
0	2 MCLKs	3 MCLKs
1	2 MCLKs – 1 MCLK = 1 MCLK	3 MCLKs – 1 MCLK = 2 MCLKs

12.48 GR1A, GR1B: Scratch Pad #6 and #7 Registers

I/O Port Address: 3CF

Index: 1A, 1B

Bit	Description	Access	Reset State
7	Scratch Pad #6 and #7 [7]	R/W	0
6	Scratch Pad #6 and #7 [6]	R/W	0
5	Scratch Pad #6 and #7 [5]	R/W	0
4	Scratch Pad #6 and #7 [4]	R/W	0
3	Scratch Pad #6 and #7 [3]	R/W	0
2	Scratch Pad #6 and #7 [2]	R/W	0
1	Scratch Pad #6 and #7 [1]	R/W	0
0	Scratch Pad #6 and #7 [0]	R/W	0

These two registers are reserved for the exclusive use of the CL-GD7556 VGA BIOS. They must never be written by any application program. They are listed here only for reference.

Bit	Description
7:0	**Reserved**

12.49 GR1C: Chroma Key U Minimum Register

I/O Port Address: 3CF

Index: 1C

Bit	Description	Access	Reset State
7	Chroma Key U Minimum [7]	R/W	0
6	Chroma Key U Minimum [6]	R/W	0
5	Chroma Key U Minimum [5]	R/W	0
4	Chroma Key U Minimum [4]	R/W	0
3	Chroma Key U Minimum [3]	R/W	0
2	Chroma Key U Minimum [2]	R/W	0
1	Reserved		
0	Reserved		

Bit	Description
7:2	**Chroma Key U Minimum [7:2]:** When occlusion is enabled (that is, Extension register CR3F[5] is 1), this 6-bit field is used in combination with GR1D[7:2] to determine when the VW displays graphics instead of video. On a pixel-by-pixel basis, the VW displays graphics instead of video under the following conditions: • The chroma key is selected (that is, Extension register bit CR42[0] is 1). • The U chrominance value in the VW is in the range defined by the following: — The chroma key U chrominance minimum of GR1C[7:2]. — The chroma key U chrominance maximum of GR1D[7:2]. To get the range of U chrominance for the occluded area in the VW: FROM: Chroma key U chrominance maximum (GR1D[7:2]) SUBTRACT: – Chroma key U chrominance minimum (GR1C[7:2]) TO OBTAIN: Range for U chrominance value in Video Window
1:0	**Reserved**

12.50 GR1D: Chroma Key U Maximum Register

I/O Port Address: 3CF

Index: 1D

Bit	Description	Access	Reset State
7	Chroma Key U Maximum [7]	R/W	0
6	Chroma Key U Maximum [6]	R/W	0
5	Chroma Key U Maximum [5]	R/W	0
4	Chroma Key U Maximum [4]	R/W	0
3	Chroma Key U Maximum [3]	R/W	0
2	Chroma Key U Maximum [2]	R/W	0
1	Reserved		
0	Reserved		

Bit	Description
7:2	**Chroma Key U Maximum [7:2]:** When occlusion is enabled (that is, Extension register CR3F[5] is 1), this 6-bit field is used in combination with GR1C[7:2] to determine when the VW displays graphics instead of video. • For details, refer to GR1C[7:2].
1:0	**Reserved**

12.51 GR1E: Chroma Key V Minimum Register

I/O Port Address: 3CF

Index: 1E

Bit	Description	Access	Reset State
7	Chroma Key V Minimum [7]	R/W	0
6	Chroma Key V Minimum [6]	R/W	0
5	Chroma Key V Minimum [5]	R/W	0
4	Chroma Key V Minimum [4]	R/W	0
3	Chroma Key V Minimum [3]	R/W	0
2	Chroma Key V Minimum [2]	R/W	0
1	Reserved		
0	Reserved		

Bit	Description
7:2	**Chroma Key V Minimum [7:2]:** When occlusion is enabled (that is, Extension register CR3F[5] is 1), this 6-bit field is used in combination with GR1F[7:2] to determine when the VW displays graphics instead of video. On a pixel-by-pixel basis, the VW displays graphics instead of video under the following conditions: • The chroma key is selected (that is, Extension register bit CR42[0] is 1). • The V chrominance value in the VW is in the range defined by the following: — The chroma key V chrominance minimum of GR1E[7:2]. — The chroma key V chrominance maximum of GR1F[7:2]. To get the range of V chrominance for the occluded area in the VW: FROM: Chroma key V chrominance maximum (GR1F[7:2]) SUBTRACT: – Chroma key V chrominance minimum (GR1E[7:2]) TO OBTAIN: Range for V chrominance value in Video Window
1:0	**Reserved**

12.52 GR1F: Chroma Key V Maximum Register

I/O Port Address: 3CF

Index: 1F

Bit	Description	Access	Reset State
7	Chroma Key V Maximum [7]	R/W	0
6	Chroma Key V Maximum [6]	R/W	0
5	Chroma Key V Maximum [5]	R/W	0
4	Chroma Key V Maximum [4]	R/W	0
3	Chroma Key V Maximum [3]	R/W	0
2	Chroma Key V Maximum [2]	R/W	0
1	Reserved		
0	Reserved		

Bit	Description
7:2	**Chroma Key V Maximum [7:2]:** When occlusion is enabled (that is, Extension register CR3F[5] is 1), this 6-bit field is used in combination with GR1E[7:2] to determine when the VW displays graphics instead of video. • For details, refer to GR1E[7:2].
1:0	**Reserved**

12.53 GR20: BitBLT Width Low Register

I/O Port Address: 3CF

Index: 20

Bit	Description	Reset State
7	BitBLT Width [7]	0
6	BitBLT Width [6]	0
5	BitBLT Width [5]	0
4	BitBLT Width [4]	0
3	BitBLT Width [3]	0
2	BitBLT Width [2]	0
1	BitBLT Width [1]	0
0	BitBLT Width [0]	0

This register contains the least-significant 8 bits of the 13-bit BitBLT (bit block transfer) width field.

Bit	Description
7:0	**BitBLT Width [7:0]:** These bits make up the BitBLT Width byte 0, the least-significant 8 bits of the 13-bit value BitBLT width field. **Register Format for 13-Bit BitBLT Width** GR21[4:0] (12 … 8) | GR20[7:0] (7 … 0) • For details on this field, refer to Extension register GR21.

12.54 GR21: BitBLT Width High Register

I/O Port Address: 3CF

Index: 21

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	BitBLT Width [12]	0
3	BitBLT Width [11]	0
2	BitBLT Width [10]	0
1	BitBLT Width [9]	0
0	BitBLT Width [8]	0

This register contains the most-significant 5 bits of the 13-bit BitBLT width field. For more information on the BitBLT, refer to the *CL-GD7556 Software Reference Manual.*

Bit	Description
7:5	**Reserved**
4:0	**BitBLT Width [12:8]:** These bits [12:8] make up the BitBLT Width byte 1, the most-significant 5 bits of the 13-bit value specifying in bytes the areas involved in the BitBLT width field. • Bits [7:0], the least-significant 8 bits, are in Extension register GR20.

Register Format for 13-Bit BitBLT Width

GR21[4:0]		GR20[7:0]	
12	8	7	0

12.55 GR22: BitBLT Height Low Register

I/O Port Address: 3CF

Index: 22

Bit	Description	Reset State
7	BitBLT Height [7]	0
6	BitBLT Height [6]	0
5	BitBLT Height [5]	0
4	BitBLT Height [4]	0
3	BitBLT Height [3]	0
2	BitBLT Height [2]	0
1	BitBLT Height [1]	0
0	BitBLT Height [0]	0

This register contains the least-significant 8 bits of the 11-bit BitBLT height field.

Bit	Description
7:0	**BitBLT Height [7:0]:** These bits make up the BitBLT Height byte 0, the least-significant 8 bits of the 11-bit value of the BitBLT height field. **Register Format for 11-Bit BitBLT Height Register** GR23[2:0] (10 8) | GR22[7:0] (7 0) • For details on this field, refer to Extension register GR23.

12.56 GR23: BitBLT Height High Register

I/O Port Address: 3CF

Index: 23

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	BitBLT Height [10]	0
1	BitBLT Height [9]	0
0	BitBLT Height [8]	0

This register contains the most-significant 3 bits of the 11-bit BitBLT height field. For more information on the BitBLT, refer to the *CL-GD7556 Software Reference Manual*.

Bit	Description
7:3	**Reserved**
2:0	**BitBLT Height [10:8]:** These bits [10:8] make up the BitBLT Height byte 1, the most-significant 3 bits of the 11-bit value specifying in scanlines the areas involved in the BitBLT height field. • Bits [7:0], the least-significant 8 bits, are in Extension register GR22.

Register Format for 11-Bit BitBLT Height Register

GR23[2:0]		GR22[7:0]	
10	8	7	0

12.57 GR24: BitBLT Destination Pitch Low Register

I/O Port Address: 3CF

Index: 24

Bit	Description	Reset State
7	BitBLT Destination Pitch [7]	0
6	BitBLT Destination Pitch [6]	0
5	BitBLT Destination Pitch [5]	0
4	BitBLT Destination Pitch [4]	0
3	BitBLT Destination Pitch [3]	0
2	BitBLT Destination Pitch [2]	0
1	BitBLT Destination Pitch [1]	0
0	BitBLT Destination Pitch [0]	0

This register contains the least-significant 8 bits of the 13-bit BitBLT destination pitch field.

Bit	Description
7:0	**BitBLT Destination Pitch [7:0]:** These bits make up the BitBLT Destination Pitch byte 0, the least-significant 8 bits of the 13-bit value BitBLT destination pitch field. **Register Format for 13-Bit BitBLT Destination Pitch** GR25[4:0] (12–8) | GR24[7:0] (7–0) • For details on this field, refer to Extension register GR25.

12.58 GR25: BitBLT Destination Pitch High Register

I/O Port Address: 3CF

Index: 25

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	BitBLT Destination Pitch [12]	0
3	BitBLT Destination Pitch [11]	0
2	BitBLT Destination Pitch [10]	0
1	BitBLT Destination Pitch [9]	0
0	BitBLT Destination Pitch [8]	0

This register contains the most-significant 5 bits of the 13-bit BitBLT destination pitch field. For more information on the BitBLT, refer to the *CL-GD7556 Software Reference Manual*.

Bit	Description
7:5	**Reserved**
4:0	**BitBLT Destination Pitch [12:8]:** These bits [12:8] make up the BitBLT Destination Pitch byte 1, the most-significant 5 bits of the 13-bit value specifying the destination pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT. • Bits [7:0], the least-significant 8 bits, are in Extension register GR24.

Register Format for 13-Bit BitBLT Destination Pitch

GR25[4:0]		GR24[7:0]	
12	8	7	0

12.59 GR26: BitBLT Source Pitch Low Register

I/O Port Address: 3CF

Index: 26

Bit	Description	Reset State
7	BitBLT Source Pitch [7]	0
6	BitBLT Source Pitch [6]	0
5	BitBLT Source Pitch [5]	0
4	BitBLT Source Pitch [4]	0
3	BitBLT Source Pitch [3]	0
2	BitBLT Source Pitch [2]	0
1	BitBLT Source Pitch [1]	0
0	BitBLT Source Pitch [0]	0

This register contains the least-significant 8 bits of the 13-bit BitBLT source pitch field.

Bit	Description
7:0	**BitBLT Source Pitch [7:0]:** These bits make up the BitBLT Source Pitch byte 0, the least-significant 8 bits of the BitBLT source pitch field.

Register Format for 13-Bit BitBLT Source Pitch

GR27[4:0]		GR26[7:0]	
12	8	7	0

- For details on this field, refer to Extension register GR27.

12.60 GR27: BitBLT Source Pitch High Register

I/O Port Address: 3CF

Index: 27

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	BitBLT Source Pitch [12]	0
3	BitBLT Source Pitch [11]	0
2	BitBLT Source Pitch [10]	0
1	BitBLT Source Pitch [9]	0
0	BitBLT Source Pitch [8]	0

This register contains the most-significant 5 bits of the 13-bit BitBLT source pitch field. For more information on the BitBLT, refer to the *CL-GD7556 Software Reference Manual*.

Bit	Description
7:5	**Reserved**
4:0	**BitBLT Source Pitch [12:8]:** These bits [12:8] make up the BitBLT Source Pitch byte 1, the most-significant 5 bits of the 13-bit value specifying the source pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT. • Bits [7:0], the least-significant 8 bits, are in Extension register GR26.

Register Format for 13-Bit BitBLT Source Pitch

GR27[4:0]		GR26[7:0]	
12	8	7	0

12.61 GR28: BitBLT Destination Start Address Low Register

I/O Port Address: 3CF

Index: 28

Bit	Description	Reset State
7	BitBLT Destination Start Address [7]	0
6	BitBLT Destination Start Address [6]	0
5	BitBLT Destination Start Address [5]	0
4	BitBLT Destination Start Address [4]	0
3	BitBLT Destination Start Address [3]	0
2	BitBLT Destination Start Address [2]	0
1	BitBLT Destination Start Address [1]	0
0	BitBLT Destination Start Address [0]	0

This register contains the least-significant 8 bits of the 22-bit BitBLT destination start address field.

Bit	Description
7:0	**BitBLT Destination Start Address [7:0]:** These bits make up the BitBLT Destination Start Address byte 0, the least-significant 8 bits of the 22-bit BitBLT destination start address field. **Register Format for 22-Bit BitBLT Destination Start Address** GR2A[5:0] (21–16) | GR29[7:0] (15–8) | GR28[7:0] (7–0) • For details on this field, refer to Extension register GR2A.

12.62 GR29: BitBLT Destination Start Address Middle Register

I/O Port Address: 3CF

Index: 29

Bit	Description	Reset State
7	BitBLT Destination Start Address [15]	0
6	BitBLT Destination Start Address [14]	0
5	BitBLT Destination Start Address [13]	0
4	BitBLT Destination Start Address [12]	0
3	BitBLT Destination Start Address [11]	0
2	BitBLT Destination Start Address [10]	0
1	BitBLT Destination Start Address [9]	0
0	BitBLT Destination Start Address [8]	0

This register contains the middle 8 bits of the 22-bit BitBLT destination start address field.

Bit	Description
7:0	**BitBLT Destination Start Address [15:8]:** These bits make up the BitBLT Destination Start Address byte 1, the middle 8 bits of the 22-bit BitBLT destination start address field. **Register Format for 22-Bit BitBLT Destination Start Address** GR2A[5:0] (21–16) | GR29[7:0] (15–8) | GR28[7:0] (7–0) • For details on this field, refer to Extension register GR2A.

12.63 GR2A: BitBLT Destination Start Address High Register

I/O Port Address: 3CF

Index: 2A

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	BitBLT Destination Start Address [21]	0
4	BitBLT Destination Start Address [20]	0
3	BitBLT Destination Start Address [19]	0
2	BitBLT Destination Start Address [18]	0
1	BitBLT Destination Start Address [17]	0
0	BitBLT Destination Start Address [16]	0

This register contains the most-significant 6 bits of the 22-bit BitBLT destination start address field. For more information on the BitBLT, refer to the *CL-GD7556 Software Reference Manual*.

Bit	Description
7:6	**Reserved**
5:0	**BitBLT Destination Start Address [21:16]:** These bits [21:16] make up the BitBLT Destination Start Address byte 2, the most-significant 6 bits of the 22-bit BitBLT destination start address value that specifies the byte address of the beginning destination pixel for a BitBLT. • Bits [15:8] are in Extension register GR29. • Bits [7:0], the least-significant 8 bits, are in Extension register GR28. **Register Format for 22-Bit BitBLT Destination Start Address** When Extension register GR31[7] is set to 1, a write to this register starts a BitBLT operation. When a BitBLT operation is in progress, the BitBLT posts a start that triggers another BitBLT operation as soon as the current BitBLT finishes. **NOTE:** In setting up a BitBLT, the GR2A[5:0] bits must be written last.

GR2A[5:0]		GR29[7:0]		GR28[7:0]	
21	16	15	8	7	0

12.64 GR2C: BitBLT Source Start Address Low Register

I/O Port Address: 3CF

Index: 2C

Bit	Description	Reset State
7	BitBLT Source Start Address [7]	0
6	BitBLT Source Start Address [6]	0
5	BitBLT Source Start Address [5]	0
4	BitBLT Source Start Address [4]	0
3	BitBLT Source Start Address [3]	0
2	BitBLT Source Start Address [2]	0
1	BitBLT Source Start Address [1]	0
0	BitBLT Source Start Address [0]	0

This register contains the least-significant 8 bits of the 22-bit BitBLT source start address field.

Bit	Description
7:0	**BitBLT Source Start Address [7:0]:** These bits make up the BitBLT Source Start Address byte 0, the least-significant 8 bits of the 22-bit BitBLT source start address field.

Register Format for 22-Bit BitBLT Source Start Address

GR2E[5:0]		GR2D[7:0]		GR2C[7:0]	
21	16	15	8	7	0

- For details on this field, refer to Extension register GR2E.

12.65 GR2D: BitBLT Source Start Address Middle Register

I/O Port Address: 3CF

Index: 2D

Bit	Description	Reset State
7	BitBLT Source Start Address [15]	0
6	BitBLT Source Start Address [14]	0
5	BitBLT Source Start Address [13]	0
4	BitBLT Source Start Address [12]	0
3	BitBLT Source Start Address [11]	0
2	BitBLT Source Start Address [10]	0
1	BitBLT Source Start Address [9]	0
0	BitBLT Source Start Address [8]	0

This register contains the middle 8 bits of the 22-bit BitBLT source start address field.

Bit	Description
7:0	**BitBLT Source Start [15:8]:** These bits make up the BitBLT Source Start Address byte 1, the middle 8 bits of the 22-bit BitBLT source start address field. **Register Format for 22-Bit BitBLT Source Start Address** GR2E[5:0] (21–16) | GR2D[7:0] (15–8) | GR2C[7:0] (7–0) • For details on this field, refer to Extension register GR2E.

12.66 GR2E: BitBLT Source Start Address High Register

I/O Port Address: 3CF

Index: 2E

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	BitBLT Source Start Address [21]	0
4	BitBLT Source Start Address [20]	0
3	BitBLT Source Start Address [19]	0
2	BitBLT Source Start Address [18]	0
1	BitBLT Source Start Address [17]	0
0	BitBLT Source Start Address [16]	0

This register contains the most-significant 6 bits of the 22-bit BitBLT source start address field. For more information on the BitBLT, refer to the *CL-GD7556 Software Reference Manual*.

Bit	Description
7:6	**Reserved**
5:0	**BitBLT Source Start Address [21:16]:** These bits [21:16] make up the BitBLT Source Start Address byte 2, the most-significant 6 bits of the 22-bit BitBLT source start address value that specifies the byte address of the beginning source pixel for a BitBLT. • Bits [15:8] are in Extension register GR2D. • Bits [7:0], the least-significant bits, are in Extension register GR2C. **Register Format for 22-Bit BitBLT Source Start Address** GR2E[5:0] (21–16) | GR2D[7:0] (15–8) | GR2C[7:0] (7–0) • When Extension register GR31[1] is set to 1, the BitBLT can be started: — By accessing data from the memory location specified in these registers. — Automatically whenever the BitBLT engine is not busy *and* there is data available in the BitBLT registers.

12.67 GR2F: BitBLT Destination Write Mask Register

I/O Port Address: 3CF

Index: 2F

Bit	Description	Reset State
7	Reserved	
6	System-to-Screen Doubleword [1]	0
5	System-to-Screen Doubleword [0]	0
4	24-Bit Packed-Pixel Write Mask [1]	0
3	24-Bit Packed Pixel Write Mask [0]	0
2	BitBLT Destination Write Mask [2]	0
1	BitBLT Destination Write Mask [1]	0
0	BitBLT Destination Write Mask [0]	0

This register supports color expansion with left-edge clipping. For details, refer to the *CL-GD7556 Software Reference Manual*.

Bit	Description
7	**Reserved**
6:5	**System-to-Screen Doubleword Pointer [1:0]:** This 2-bit field specifies the byte alignment (that is, the position) of the first byte within the first doubleword of each destination scanline. This specification allows data that is unaligned in system memory to be transferred without the overhead of unaligned bus cycles. • When this field is programmed to a non-zero value for a color-expand BitBLT, Extension register GR33[0] must be set to 1.
4:3	**24-Bit Packed-Pixel Write Mask [4:3]:** For 24-bit packed-pixel modes, this 2-bit field expands the write mask contained in GR2F[2:0] for color expansion. The resulting 5-bit field is a byte mask.
2:0	**BitBLT Destination Write Mask [2:0]:** This 3-bit field can be used to prevent writing the first *n* pixels (up to 7 pixels) of each scanline for a color-expanded or pattern-copy BitBLT. • In 24-bit packed-pixel modes, this 3-bit field can be expanded to 5 bits with GR2F[4:3]. In these modes, the field is a count of bytes, not pixels.

12.68 GR30: BitBLT Mode Register

I/O Port Address: 3CF

Index: 30

Bit	Description	Reset State
7	BitBLT Color Expand Enable	0
6	BitBLT Pattern Copy (8 × 8) Enable	0
5	BitBLT Color Expand Width [1]	0
4	BitBLT Color Expand Width [0]	0
3	BitBLT Color Expand with Transparency Enable	0
2	BitBLT Source (Display Memory or System Memory)	0
1	Reserved	
0	BitBLT Direction	0

This register contains the bits that specify the BitBLT (bit block transfer) details, but not the BitBLT raster operation. For more information on the BitBLT, refer to the *CL-GD7556 Software Reference Manual*.

Bit **Description**

7 **BitBLT Color Expand Enable:**
When this bit is:

- 0, the source can be either system memory or display memory, depending on the setting of GR30[2].
- 1, the source is the expanded result from a monochrome bit-mapped source.
  - — GR30[0] must be 0 (that is, the direction of the progression of the BitBLT operation must be incremental).
  - — Both the source area and the destination area must be display memory.
    - — When the source data is expanded, the most-significant bit of the first source byte is the first pixel in the display memory destination.
    - — The source starting address must be on a 8-byte boundary, and the source is taken as a string of bytes (that is, the addressing is linear). The source pitch is ignored.
  - — For color-expanded BitBLTs (that is, the source is system memory or display memory), each logical scanline must be an even byte.
  - — The color registers for Extended Write modes 4 and 5 are GR0 and GR1.
  - — For color-expanded BitBLT operations that use:
    - — 16-bit mapping, use Graphics Controller registers GR0 and GR1 and Extension registers GR10–GR11.
    - — 32-bit-mapping, use Graphics Controller registers GR0–GR2 and Extension registers GR10–GR13.
  - — For information regarding color expansion, refer to the *CL-GD7556 Software Reference Manual*.

12.68 GR30: BitBLT Mode Register *(cont.)*

Bit **Description**

6 **BitBLT Pattern Copy (8 × 8) Enable:**
When this bit is 1, the source pattern of 8 columns (that is, 8 pixels) × 8 rows (that is, 8 scanlines) is copied repeatedly to the destination rectangular area.

- The source pattern must be aligned on a boundary that is equal to the size of the pattern.
- The source and destination must be display memory.
- This bit works in combination with GR30[7] and GR30[5:4] to provide a source pattern of linear-addressed data that is in one of four arrangements, as shown in the table that follows.

GR30				Case	Source Pattern Arrangement	Display Size	Pad Required
[7]	[6]	[5]	[4]				
0	1	0	0	8-bit pixels	8 columns of 8-bit/pixel = 64 bytes of color data		
0	1	0	1	16-bit pixels	8 columns of 16-bits/pixel = 128 bytes of color data		
0	1	1	0	24-bit pixels	8 columns of 24 bits/pixel, with padding added to each scanline	640 x 480	128 Bytes
						800 x 600	672 Bytes
						1024 x 768	0 Bytes
1	1	X	X	Color expansion enabled	8 bytes of monochrome bit map data for 64 pixels		

5:4 **BitBLT Color Expand Width [1:0]:**
This 2-bit field is enabled when GR30[7] = 1, and it controls the width of color-expand BitBLTs according to the following table:

GR30		Color Expansion Width	Display Size	Pad Required
[5]	[4]			
0	0	8 bits per pixel		
0	1	16 bits per pixel		
1	0	24 bits per pixel, with padding added to each scanline	640 x 480	128 Bytes
			800 x 600	672 Bytes
			1024 x 768	0 Bytes
1	1	Reserved		

12.68 GR30: BitBLT Mode Register *(cont.)*

Bit	Description
3	**BitBLT Color Expand with Transparency Enable:** When a monochrome image is being expanded, this bit takes effect on a pixel-by-pixel basis. When an individual pixel making up the monochrome image has a value of 0 and this bit is: • 0, the background color is written to the corresponding expansion pixel. • 1, the background color is not written to the corresponding expansion pixel.
2	**BitBLT Source (Display Memory or System Memory):** When this bit is: • 0, the BitBLT source is display memory. • 1, the BitBLT source is system memory. — The CPU performs the system bus transfers, but the CL-GD7556 ignores the address provided with such transfers. — The CPU must transfer data in increments of 4 bytes (that is, doublewords). When the total number of bytes moved for a BitBLT is not a multiple of four, the CPU must write 'dummy' bytes to make a multiple of four bytes. — For system-to-screen BitBLTs that: — Do not have color expansion, up to 3 bytes of the last doubleword for each scanline is ignored. — Have color expansion, bytes that are left over at the end of a scanline are used to start a new scanline. However, individual bits that are left over at the end of a scanline are ignored. For granularity control of the source data, refer to GR33[0]. **NOTE:** System-memory to system-memory BitBLTs are not allowed.
1	**Reserved:** This bit must always be programmed to 0.
0	**BitBLT Direction:** When this bit is: • 0, the following occur: — The source and destination addresses are incremented. — The BitBLT proceeds from lower addresses to higher addresses. • 1, the following occur: — The source and destination addresses are decremented. — The BitBLT proceeds from higher addresses to lower addresses. — Operations proceed from right-to-left and bottom-to-top. — This setting is intended only for screen-to-screen BitBLTs. — The starting address is the highest addressed byte in each area. **NOTE:** Neither color-expansion nor pattern-copy can be used with this setting.

12.69 GR31: BitBLT Start/Status Register

I/O Port Address: 3CF

Index: 31

Bit	Description	Access	Reset State
7	BitBLT Automatic Start	R/W	0
6	Reserved		
5	Pause	R/W	0
4	Buffered Registers Status	R	0
3	BitBLT Reset Status	R	0
2	BitBLT Reset	R/W	0
1	BitBLT Start	R/W	0
0	BitBLT Status	R	0

This register contains bits for starting a BitBLT and monitoring its status. For more information on the BitBLT, refer to the *CL-GD7556 Software Reference Manual*.

Bit — **Description**

7 — **BitBLT Automatic Start:**
This bit is used in combination with GR2A to allow a fast BitBLT start. When Extension register GR2A is written *and* this bit is:

- 0, the BitBLT does not start automatically. In this case, to start the BitBLT, GR31[1] must be set to 1.
- 1, the BitBLT starts automatically, using data in the buffered BitBLT registers.
  - — The buffered BitBLT registers are the following:
    - — For BitBLT color expansion, buffered registers are Graphics Controller registers GR0 and GR1 and Extension registers GR10–GR11 and GR13.
    - — For BitBLT control, buffered registers are Graphics Controller registers GR0 and GR1 and Extension registers GR10–GR13, GR20–GR2A, GR2C–GR2E, GR30, and GR32–GR33.
  - — After the BitBLT starts, GR31[4] is reset to 0.
  - — When a BitBLT is in progress and GR2A is written, GR31[7] posts a start, which triggers another BitBLT.
  - — In setting up a BitBLT, Extension register bits GR2A[5:0] must be written last.

6 — **Reserved**

5 — **Pause:**
When this bit is:

- 0, *and* if a system-to-screen BitBLT requires additional data to complete, then writes to the display memory address range go to the BitBLT engine.
- 1, a system-to-screen BitBLT pauses.
  - — Writes to the display memory address range are taken as ordinary display memory writes. The address supplied by the processor is used as the entire address. This process can be used to change the hardware cursor in response to a mouse interrupt during a system-to-screen BitBLT.
  - — Reads to the display memory address range are not permitted and return invalid data.

12.69 GR31: BitBLT Start/Status Register *(cont.)*

Bit	Description
4	**Buffered Registers Status:** When this read-only bit reads a: • 0, the CL-GD7556 signals to the software driver that buffered registers are available (that is, a BitBLT can be programmed). This bit is reset to 0 when: — GR31[7] is reset to 0. — GR31[7] is set to 1 *and* GR2A[5:0] is written. • 1, the CL-GD7556 signals to the software driver that buffered registers are not available and cannot be programmed, as they are already loaded with data and waiting for the start of a BitBLT. **NOTE:** Bit GR31[2], the BitBLT reset bit, does not affect this bit GR31[4].
3	**BitBLT Reset Status:** This read-only bit is set to 1 at the start of a BitBLT (that is, GR31[1] = 1). When the BitBLT operation: • Completes, this bit is reset to 0. • Resets, this bit is reset to 0 (refer to GR31[2]). • Suspends, this bit remains a 1 (refer to GR31[5]).
2	**BitBLT Reset:** This bit must be reset to 0, before any BitBLT operations are attempted. When this bit is set to 1: • The entire BitBLT engine is immediately reset, and any operation in progress is terminated. The operation cannot be restarted. • GR31[3] is reset to 0.
1	**BitBLT Start:** This bit resets to 0 automatically, when the BitBLT completes. When this bit is set to 1, the BitBLT starts with the next available display memory cycle. — GR31[0] must be monitored to determine when the BitBLT completes. — For proper operation, the write buffer must be empty when a BitBLT is started. — Any required writes to DRAM must occur before the BitBLT registers are programmed. This process allows the write buffer to empty before the BitBLT operation starts.
0	**BitBLT Status:** When this read-only bit reads a: • 0, it indicates a BitBLT operation is complete or has been suspended. • 1, it indicates a BitBLT operation is in progress.

12.70 GR32: BitBLT Raster Operation Function Register

I/O Port Address: 3CF

Index: 32

Bit	Description	Reset State
7	BitBLT Raster Operation Function [7]	0
6	BitBLT Raster Operation Function [6]	0
5	BitBLT Raster Operation Function [5]	0
4	BitBLT Raster Operation Function [4]	0
3	BitBLT Raster Operation Function [3]	0
2	BitBLT Raster Operation Function [2]	0
1	BitBLT Raster Operation Function [1]	0
0	BitBLT Raster Operation Function [0]	0

This register selects a raster operation function.

Bit **Description**

7:0 **BitBLT Raster Operation Function [7:0]:**
This 8-bit value selects from 1 to 16 two-operand ROP (raster operation) functions, as indicated in the table that follows.

NOTES:

1) Source and Pattern use the same ROP number for the same logical operation.

2) Raster operations that do not use the Source (such as ~D), must not be used when color expansion is selected.

3) S = Source
D = Destination
P = Pattern
+ = OR
• = AND
~ = Inversion (not)
x = Exclusive OR
≠ = Not equal

Logical Function		GR32 [7:0] ROP Number (hex)	Microsoft® Name	Microsoft® ROP
Z (Reverse Polish Notation)	Z (Algebraic Notation)			
0	0	00	BLACKNESS	00000042
1	1	0E	WHITENESS	00FF0062
S	S	0D	SRCCOPY	00CC0020
P	P	0D	PATCOPY	00F00021
D	D	06	–	00AA0029
S~	~S	D0	NOTSRCCOPY	00330008
P~	~P	D0	–	000F0001

12.70 GR32: BitBLT Raster Operation Function Register *(cont.)*

Bit **Description**

7:0 *(cont.)* **Raster Operation Function [7:0]:** *(cont.)*

Logical Function		GR32 [7:0] ROP Number (hex)	Microsoft® Name	Microsoft® ROP
Z (Reverse Polish Notation)	Z (Algebraic Notation)			
D~	~D	0B	DSTINVERT	00550009
DS•	S • D	05	SRCAND	008800C6
DP•	P • D	05	–	00A000C9
SD~•	S • ~D	09	SRCERASE	00440328
PD~•	P • ~D	09	–	00500325
DS~•	~S • D	50	–	00220326
DP~•	~P • D	50	–	000A0329
DS+~	~S • ~D	90	NOTSCERASE	001100A6
DP+~	~P • ~D	90	–	000500A9
DS+	S + D	6D	SRCPAINT	00EE0086
DP+	P + D	6D	–	00FF0062
SD~+	S + ~D	AD	–	00DD0228
PD~+	P + ~D	AD	–	00F50225
DS~+	~S + D	D6	MERGEPAINT	00BB0226
DP~+	~P + D	D6		00AF0229
DS•~	~S + ~D	DA	–	007700E6
DP•~	~P + ~D	DA	–	005F00E9
DSx~	S = D	95	–	00990066
DPx~	P = D	95	–	00A50065
DSx	S ≠ D	59	SRCINVERT	00660046
DPx	P ≠ D	59	PATINVERT	005A0049

Examples:

- Reverse Polish notation: (DP+~) means Destination {enter}, Pattern, OR, NOT.
- Algebraic notation: (~P • ~D) means NOT-Pattern AND NOT-Destination.
- DeMorgan's theorem states that these two functions are equivalent: $(\overline{D + P} = \overline{P} \bullet \overline{D})$

12.71 GR33: BitBLT Mode Extensions Register

I/O Port Address: 3CF

Index: 33

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Solid Color Fill Enable	0
1	Source Data Sense Invert for BitBLT	0
0	Source Data Granularity for BitBLT	0

This register contains some extended mode controls.

Bit	Description
7:3	**Reserved**
2	**Solid Color Fill Enable:** When this bit is programmed to: • 0, this function is disabled. • 1, the destination area (rectangle) is filled with the foreground color. — GR30[7:6] must be set to '11'. — GR30[3] must be set to 0 (that is, no transparency). **NOTE:** This function yields identical results as a color-expanded, pattern-fill BitBLT with a pattern of all 1s, but this method is faster.
1	**Source Data Sense Invert for BitBLT:** For a color-expanded BitBLT with transparency, when this bit is programmed to: • 0, color expansion is normal. • 1, for color expansion, the sense of host CPU source data is inverted as follows: — A 0 causes the foreground color to be written. — A 1 causes the pixel not to be written.
0	**Source Data Granularity for BitBLT:** When this bit is programmed to: • 0, unused source data to the end of the current byte is not discarded at the end of each scanline. — This process affects only color-expanded system-to-screen BitBLTs. — System-to-screen BitBLTs, which do not use color expansion, always discard to the end of the current doubleword. • 1, doubleword granularity is enabled for color-expanded system-to-screen BitBLTs. — At the end of each scanline, unused source data is discarded to the end of the current doubleword. The next scanline begins with the next doubleword. Up to 31 bits can be discarded. — This bit must be set to 1 for any color expand BitBLT for which Extension register bits GR2F[6:5] are non-zero.

12.72 CR19: Interlace End Register

I/O Port Address: 3?5

Index: 19

Bit	Description	Reset State
7	Interlace End [7]	0
6	Interlace End [6]	0
5	Interlace End [5]	0
4	Interlace End [4]	0
3	Interlace End [3]	0
2	Interlace End [2]	0
1	Interlace End [1]	0
0	Interlace End [0]	0

This register contains the ending horizontal character count for the odd field for VSYNC.

Bit	Description
7:0	**Interlace End:** In interlaced timing, the value in this field equals the number of characters in the last scanline of the odd field. • To center the scanlines in the odd field, this value can be adjusted half-way between scanlines in the even field. • This register is typically programmed to approximately half the Horizontal Total.

12.73 CR1A: Miscellaneous Control Register

I/O Port Address: 3?5

Index: 1A

Bit	Description	Reset State
7	Vertical Blanking End Extension [9]	0
6	Vertical Blanking End Extension [8]	0
5	Horizontal Blanking End Extension [7]	0
4	Horizontal Blanking End Extension [6]	0
3	Reserved	
2	Reserved	
1	Double-Buffer Display Start Address Enable	0
0	Interlaced Timing Enable	0

Bit **Description**

7:6 **Vertical Blanking End Extension [9:8]:**
These 2 bits are used to extend the Vertical Blanking End field to 10 bits.
- These bits are enabled only when CR1B[7] is 1, or CR1B[5] is 1, or both are 1.

Register Format for 10-Bit Vertical Blanking End

CR1A[7:6]		CR16[7:0]	
9	8	7	0

- For details on this field, refer to CRT Controller register CR16.

5:4 **Horizontal Blanking End Extension [7:6]:**
These 2 bits are used to extend the Horizontal Blanking End field to 8 bits.
- These bits are enabled only when CR1B[7] is 1, or CR1B[5] is 1, or both are 1.

Register Format for 8-Bit Horizontal Blanking End

CR1A[5:4]		CR5[7]	CR3[4:0]	
7	6	5	4	0

- For details on this field, refer to CRT Controller register CR3[4:0].

3:2 **Reserved**

1 **Double-Buffer Display Start Address Enable:**
When this bit is 1, the Display Start Address is updated on the VSYNC following a write to Start Address Low register (that is, CRT Controller register CRD). This update provides control of frame switching for the display screen, without the need to explicitly monitor VSYNC.

0 **Interlaced Timing Enable**:
When this bit is 1, interlaced timing is enabled.
- In text display mode, interlaced synchronization is enabled.
- In graphics display mode:
  - — Both interlaced synchronization and display data are enabled.
  - — For both interlaced synchronization and display data, CRT Controller register bit CR9[7] must be 0.
  - — Graphics display modes 4h and 6h must always be non-interlaced.
- Interrupt requests are generated only at the end of odd fields (that is, at the end of a frame).

12.74 CR1B: Extended Display Control Register

I/O Port Address: 3?5

Index: 1B

Bit	Description	Reset State
7	Vertical and Horizontal Blanking End Extension Enable	0
6	Text Display Mode Fast-Page Enable	0
5	Blanking Control	0
4	Scanline Offset [8]	0
3	Screen A Start Address [18]	0
2	Screen A Start Address [17]	0
1	Extended Address Wrap Enable	0
0	Screen A Start Address [16]	0

This register contains miscellaneous bits that control extended display functions.

Bit	Description
7	**Vertical and Horizontal Blanking End Extension Enable**: When this bit is: • 0, *and* CR1B[5] is 0, then the Vertical and Horizontal Blanking End Extension bits of CR1A[7:6] and CR1A[5:4] are disabled. • 1, the following are enabled, regardless of the CR1B[5] level: — Vertical Blanking End Extension bits [9:8], in CR1A[7:6] — Horizontal Blanking End Extension bits [7:6], in CR1A[5:4]
6	**Text Display Mode Fast-Page Enable**: When Attribute Controller register bit AR10[0] is 0 *and* this bit is: • 0, all text display mode fetch cycles take place as random-read cycles. This bit must be 0 for standard VGA dual-font operation. • 1, text display modes use fast-page-mode cycles. This setting allows for text display modes with a VCLK greater than 30 MHz, as is required for 132-column display modes.
5	**Blanking Control:** When this bit is: • 0, (which is used for the standard VGA display modes): — The blanking signal generated by the CRT Controller controls DAC blanking. — The border can be used. (For details, refer to Attribute Controller register AR11.) • 1, the following occur: — The display enable signal controls DAC blanking. — Blanking starts at the end of the horizontal display. — The following are enabled, regardless of the CR1B[7] level: — Vertical Blanking End Extension bits [9:8], in CR1A[7:6] — Horizontal Blanking End Extension bits [7:6], in CR1A[5:4]

12.74 CR1B: Extended Display Control Register *(cont.)*

Bit	Description
4	**Scanline Offset [8]:** This bit is the most-significant bit of the 9-bit Scanline Offset field. **Register Format for 9-Bit Scanline Offset** CR1B[4] = 8; CR13[7:0] = 7 0 • For details on this field, refer to CRT Controller register CR13.
3:2	**Screen A Start Address [18:17]:** These bits are bits [18:17] of the 20-bit Screen A Start Address field. **Register Format for 20-Bit Screen A Start Address** CR1D[7] = 19; CR1B[3:2] = 18 17; CR1B[0] = 16; CRC[7:0] = 15 8; CRD[7:0] = 7 0 • For details on this field, refer to Extension register CR1D.
1	**Extended Address Wrap Enable:** When this bit is: • 0, VGA compatibility is offered as follows: — The CRT Controller character counter address is 16 bits wide. — The display memory address wraps at 64K maps (for 256K total memory). • 1, — The CRT Controller character counter address is 19 bits wide. — The CRT Controller character counter addresses CA16 and CA18 provide up to 256K bytes in each bit plane, or 1 Mbyte of packed-pixel memory. — The display memory address wraps at the total available memory size. • 1 *and* Sequencer register SR4[3] is 1 (that is, Chain-4 addressing is selected): — DRAM addresses MA[1:0] are supplied from addresses XMA[17:16]. — The other DRAM addresses are supplied from addresses XMA[18:12]. These addresses result from the sum of bus addresses XA[16:12] and the contents of either Graphics Controller register GR9 or GRA. • 1 *and* CRT Controller register CR14[6] is 1 (that is, CRT Controller doubleword addressing is selected): — DRAM addresses MA[1:0] are supplied from the internal CL-GD7556 CRT Controller address counter CR[15:14]. — The other DRAM addresses are supplied from addresses XMA[18:12], in the same manner as Chain-4 addressing. — This action provides four displayable pages in graphics display mode 13h.
0	**Screen A Start Address [16]:** This bit is bit 16 of the 20-bit Screen A Start Address field. **Register Format for 20-Bit Screen A Start Address** CR1D[7] = 19; CR1B[3:2] = 18 17; CR1B[0] = 16; CRC[7:0] = 15 8; CRD[7:0] = 7 0 • For details on this field, refer to CR1B[3:2] and Extension register CR1D.

12.75 CR1C: Horizontal Total and Horizontal Sync Start Adjust Register

I/O Port Address: 3?5

Index: 1C

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Horizontal Total Adjust [2]	0
4	Horizontal Total Adjust [1]	0
3	Horizontal Total Adjust [0]	0
2	Horizontal Sync Start Adjust [2]	0
1	Horizontal Sync Start Adjust [1]	0
0	Horizontal Sync Start Adjust [0]	0

This register is used to adjust horizontal timing.

Bit **Description**

7:6 **Reserved**

5:3 **Horizontal Total Adjust [2:0]:**
This field allows the Horizontal Total to be adjusted from –3 to +4 VCLKs.

- The length of the character, which occurs two character clocks after the Horizontal Counter has reached the value programmed into Horizontal Total, is adjusted according to the following table:

CR1C			Character Clock Adjustment
[5]	[4]	[3]	
0	0	0	0 (No adjustment. This is the normal setting.)
0	0	1	–3 VCLKs
0	1	0	–2 VCLKs
0	1	1	–1 VCLKS
1	0	0	+1 VCLKS
1	0	1	+2 VCLKS
1	1	0	+3 VCLKs
1	1	1	+4 VCLKS

2:0 **Horizontal Sync Start Adjust [2:0]:**
This 3-bit field allows the Horizontal Sync Start position (relative to BLANK) to be adjusted from 0 to 7 VCLKs.

- Horizontal Sync is delayed the additional number of VCLKs programmed in this field.
- The Horizontal Sync width is still adjustable only in character clock increments.

12.76 CR1D: Color Key Compare Type Register

I/O Port Address: 3?5

Index: 1D

Bit	Description	Reset State
7	Screen A Start Address [19]	0
6	Reserved	
5	Color Key Compare Type [1]	0
4	Color Key Compare Type [0]	0
3	Color Key Compare Width	0
2	Reserved	
1	Reserved	
0	Reserved	

This register contains controls for the color key compare modes.

Bit **Description**

7 **Screen A Start Address [19]:**
The 20-bit Screen A Start Address field contains a value that specifies the starting display memory location for data to be displayed on the display screen.

- This bit 19 is the most-significant bit of the 20-bit Screen A Start Address field.
- Bits [18:16] are in Extension register CR1B[3:2,0].
- Bits [15:8] are in CRT Controller register CRC[7:0].
- Bits [7:0], the least-significant bits, are in CRT Controller register CRD.

Register Format for 20-Bit Screen A Start Address

CR1D[7]	CR1B[3:2]		CR1B[0]	CRC[7:0]		CRD[7:0]	
19	18	17	16	15	8	7	0

6 **Reserved**

5:4 **Color Key Compare Type [1:0]:**
This 2-bit field chooses the type of comparison done between the pixel data and the Extension register GRC color key data according to the following table:

CR1D[5:4]	Comparison	Type of Comparison
00	Pixel Data = GRC	Logical
01	Pixel Data < GRC	Arithmetic
1x	Pixel Data > GRC	Arithmetic

12.76 CR1D: Color Key Compare Type Register *(cont.)*

Bit	Description
3	**Color Key Compare Width:** When Extension register bits SR7[3:1] = '011' (that is, the 16-bit per pixel mode), *and* this bit is programmed to: • 0, the following occur: — The low byte of the 16-bit pixel is compared to Extension register GRC. — Extension register GRD is used as a mask for that byte. • 1, the following occur: — All 16 bits of the pixel are used for the color key compare. — The low byte of the 16-bit pixel is compared to Extension register GRC. — The high byte of the 16-bit pixel is compared to Extension register GRD. — Since GRD is used for the high-byte, no mask is available.
2:0	**Reserved**

12.77 CR22: Graphics Controller Data Latch Readback Register

I/O Port Address: 3?5

Index: 22

Bit	Description	Access	Reset State
7	Graphics Controller Data Latch *n* Readback [7]	R	0
6	Graphics Controller Data Latch *n* Readback [6]	R	0
5	Graphics Controller Data Latch *n* Readback [5]	R	0
4	Graphics Controller Data Latch *n* Readback [4]	R	0
3	Graphics Controller Data Latch *n* Readback [3]	R	0
2	Graphics Controller Data Latch *n* Readback [2]	R	0
1	Graphics Controller Data Latch *n* Readback [1]	R	0
0	Graphics Controller Data Latch *n* Readback [0]	R	0

This register is used to read the contents of a Graphics Controller Data Latch.

Bit	Description
7:0	**Graphics Controller Data Latch *n* Readback [7:0]:** This read-only register can be used to read back the contents of one of the four Graphics Controller Data Latches. • The number *n* of the display memory data latch that is read back is selected with Graphics Controller register bits GR4[1:0]. • These latches are loaded whenever display memory is read by the host CPU.

12.78 CR24: Attribute Controller Index/Data Status Readback Register

I/O Port Address: 3?5

Index: 24

Bit	Description	Access	Reset State
7	Attribute Controller Index/Data Status	R	0
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Reserved		
0	Reserved		

This read-only register provides access to the Attribute Controller Toggle, either Index or Data.

NOTE: This is a standard VGA register. It is duplicated in this section only for reference.

Bit	Description
7	**Attribute Controller Index/Data Status:** When this read-only bit reads a: • 0, the Attribute Controller reads or writes an index value on the next access. • 1, the Attribute Controller reads or writes a data value on the next access.
6:0	**Reserved**

12.79 CR25: Manufacturing Revision Identification Register

I/O Port Address: 3?5

Index: 25

Bit	Description	Access	Reset State
7	Manufacturing Revision Identification [7]	R	'MFG revision'
6	Manufacturing Revision Identification [6]	R	'MFG revision'
5	Manufacturing Revision Identification [5]	R	'MFG revision'
4	Manufacturing Revision Identification [4]	R	'MFG revision'
3	Manufacturing Revision Identification [3]	R	'MFG revision'
2	Manufacturing Revision Identification [2]	R	'MFG revision'
1	Manufacturing Revision Identification [1]	R	'MFG revision'
0	Manufacturing Revision Identification [0]	R	'MFG revision'

This read-only register contains the least-significant 8 bits of the 10-bit Manufacturing Revision Identification field. This register must never be written by any application program. It is listed here only for reference.

Bit	Description
7:0	**Manufacturing Revision Identification [7:0]:** These bits [7:0] are the least-significant 8 read-only bits of the 10-bit Manufacturing Revision Identification field. • Bits [9:8], the two most-significant read-only bits, are in Extension register CR27[1:0]. **Register Format for 10-Bit Manufacturing Revision Identification** CR27[1:0] (9 8) | CR25[7:0] (7 0) • The Manufacturing Revision Identification field uniquely identifies the CL-GD7556 manufacturing revision level. • *This field is used only for factory testing and internal tracking purposes*.

12.80 CR26: Attribute Controller Index Readback Register

I/O Port Address: 3?5

Index: 26

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	Video Source Enable Readback	R	0
4	Attribute Controller Index Readback [4]	R	0
3	Attribute Controller Index Readback [3]	R	0
2	Attribute Controller Index Readback [2]	R	0
1	Attribute Controller Index Readback [1]	R	0
0	Attribute Controller Index Readback [0]	R	0

This read-only register provides access to the current Attribute Controller Index.

NOTE: This is a standard VGA register. It is duplicated in this section only for reference.

Bit	Description
7:6	**Reserved**
5	**Video Source Enable Readback:** This read-only bit echoes Attribute Controller register bit ARX[5].
4:0	**Attribute Controller Index Readback [4:0]:** This read-only field echoes Attribute Controller register bits ARX[4:0].

12.81 CR27: Device Identification Register

I/O Port Address: 3?5

Index: 27

Bit	Description	Access	Reset State
7	Device ID [5]	R	0
6	Device ID [4]	R	1
5	Device ID [3]	R	0
4	Device ID [2]	R	0
3	Device ID [1]	R	1
2	Device ID [0]	R	1
1	Manufacturing Revision Identification [9]	R	'MFG revision'
0	Manufacturing Revision Identification [8]	R	'MFG revision'

This read-only register returns a value in bits [7:2] that uniquely identifies the CL-GD7556. Application programs are not required to read this register when the Cirrus Logic VGA BIOS is used.

Bit	Description
7:2	**Device ID [5:0]:** This read-only 6-bit field contains a unique value '010011' (4Ch) that identifies the CL-GD7556 as a Cirrus Logic product.
1:0	**Manufacturing Revision ID [9:8]:** These read-only bits are the most-significant 2 bits of the 10-bit Manufacturing Revision ID field. **Register Format for 10-Bit Manufacturing Revision Identification** CR27[1:0] (9 8) | CR25[7:0] (7 0) • For details on this field, refer to Extension register CR25.

12.82 CR30: TV-OUT Control Register

I/O Port Address: 3?5

Index: 30

Bit	Description	Reset State
7	Reserved	
6	TV-OUT Mode Enable	0
5	Horizontal Total Dot Clock Delay Control [1]	0
4	Horizontal Total Dot Clock Delay Control [0]	0
3	TV-ON Level Select	0
2	NTSC / PAL Output Control	0
1	CSYNC Dot Clock Delay Control [1]	0
0	CSYNC Dot Clock Delay Control [0]	0

Bit **Description**

7 **Reserved**

6 **TV-OUT Mode Enable:**
Before TV-OUT mode is enabled, the panel must be disabled by setting CR85[5] to 1, and the CRT must be disabled.
When this bit is:

- 0, the TV-OUT mode is disabled. Extension register bits SR2F[7:5] control the output level on the PROG2, PROG1, PROG0 pins respectively, and CSYNC is disabled (active low).
- 1, the SR2F[7,5] bits are disabled, and:
  - — PROG0 pin 127 (Y20) is the TV-ON control pin whose level is controlled by CR30[3].
  - — PROG2 pin 129 (W20) is the NTSC/PAL control pin whose level is controlled by CR30[2].
  - — The CSYNC pin 118 (W16) is enabled. The format is controlled by CR30[2].

5:4 **Horizontal Total Dot Clock Delay Control [1:0]:**
The value in these bits control the dot clock delay for the horizontal total signal according to the following table:

CR30		Dot-Clock Delay for Horizontal Total
[5]	[4]	
0	0	No delay
0	1	Delay is 2 dot clocks.
1	0	Delay is 4 dot clocks.
1	1	Delay is 6 dot clocks.

12.82 CR30: TV-OUT Control Register *(cont.)*

Bit	Description
3	**TV-ON Level Select:** When CR30[6] is 0, this bit is disabled. When CR30[6] is 1, and this bit is: • 0, the TV-ON output is low. • 1, the TV-ON output is high.
2	**NTSC / PAL Output Control:** This bit is programmed to reflect required input levels to the NTSC/PAL encoder. • When CR30[6] is 0, this bit is disabled. • When CR30[6] is 1, *and* this bit is: — 0, the NTSC/PAL output pin is forced low, and CSYNC timing is generated in accordance with PAL timing requirements. — 1, the NTSC/PAL output pin is forced high, and CSYNC timing is generated in accordance with NTSC timing requirements.
1:0	**CSYNC Dot Clock Delay Control [1:0]:** The value in these bits control the dot clock delay for the generation of a composite synchronization signal (CSYNC) according to the following table.

CR30		Dot Clock Delay for CSYNC Start
[1]	[0]	
0	0	No delay
0	1	Delay is 2 dot clocks.
1	0	Delay is 4 dot clocks.
1	1	Delay is 6 dot clocks.

12.83 CR31: VW Horizontal Upscaling Coefficient Register

I/O Port Address: 3?5

Index: 31

Bit	Description	Reset State
7	VW Horizontal Upscaling Coefficient [11]	0
6	VW Horizontal Upscaling Coefficient [10]	0
5	VW Horizontal Upscaling Coefficient [9]	0
4	VW Horizontal Upscaling Coefficient [8]	0
3	VW Horizontal Upscaling Coefficient [7]	0
2	VW Horizontal Upscaling Coefficient [6]	0
1	VW Horizontal Upscaling Coefficient [5]	0
0	VW Horizontal Upscaling Coefficient [4]	0

This register controls the horizontal upscaling of the VW.

Bit **Description**

7:0 **VW Horizontal Upscaling Coefficient [11:4]:**
These bits [11:4] are the most-significant 8 bits of the 12-bit field for the VW HU (VW Horizontal Upscaling) Coefficient.

- Bits [3:0], the least-significant 4 bits, are in Extension register CR39[7:4].

Register Format for 12-Bit VW Horizontal Upscaling Coefficient

CR31[7:0]		CR39[7:4]	
11	4	3	0

- The VW HU range that the CL-GD7556 supports is from 1x to 4x.
- The VW HU is calculated as follows:

$$\text{VW HU} = \frac{4096 \text{ (The VW HU field is 12 bits and } 2^{12} = 4096.)}{\text{Value programmed in CR31[7:0] and CR39[7:4] (Range is 1024 -4095)}}$$

- When the value programmed for the VW HU coefficient is:
  - — 0h (the default, and an exception), the horizontal upscaling coefficient is 1x. [The horizontal upscaling coefficient is (4096 ÷ 4096) = 1x, and the resulting VW image is unchanged from the image source.]
  - — 400h (1024 decimal), the horizontal upscaling coefficient is 4x. [The horizontal upscaling coefficient is (4096 ÷ 1024) = 4x, and the resulting VW image is four times as large as the image source.]
  - — 800h (2048 decimal), the horizontal upscaling coefficient is 2x. [The horizontal upscaling coefficient is (4096 ÷ 2048) = 2x, and the resulting VW image is two times as large as the image source.]
- When horizontal upscaling of greater than 1x is chosen:
  - — Some pixels are generated by horizontal interpolation of source image pixels.
  - — As a result of this generation, the VW includes the extra pixels and is wider than it would be if upscaling was not enabled. That is, horizontal upscaling is accomplished by making the VW physically wider rather than by keeping the VW width constant and displaying fewer source pixels.

12.84 CR32: VW Vertical Upscaling Coefficient Register

I/O Port Address: 3?5

Index: 32

Bit	Description	Reset State
7	VW Vertical Upscaling Coefficient [11]	0
6	VW Vertical Upscaling Coefficient [10]	0
5	VW Vertical Upscaling Coefficient [9]	0
4	VW Vertical Upscaling Coefficient [8]	0
3	VW Vertical Upscaling Coefficient [7]	0
2	VW Vertical Upscaling Coefficient [6]	0
1	VW Vertical Upscaling Coefficient [5]	0
0	VW Vertical Upscaling Coefficient [4]	0

This register controls the vertical upscaling of the VW.

Bit **Description**

7:0 **VW Vertical Upscaling Coefficient [11:4]:**
These bits [11:4] are the most-significant 8 bits of the 12-bit field for the VW VU (VW Vertical Upscaling) Coefficient.

- Bits [3:0], the least-significant 4 bits, are in Extension register CR39[3:0].

Register Format for 12-Bit VW Vertical Upscaling Coefficient

CR32[7:0]		CR39[3:0]	
11	4	3	0

- The VW VU range that the CL-GD7556 supports is from 1x to 4x.
- The VW VU is calculated as follows:

$$\text{VW VU} = \frac{4096 \text{ (The VW VU field is 12 bits and } 2^{12} = 4096.)}{\text{Value programmed in CR32[7:0] and CR39[3:0] (Range is 1024–4095)}}$$

- When the value programmed for the VW VU coefficient is:
  - — 0h (the default, and an exception), the vertical upscaling coefficient is 1x. [The vertical upscaling coefficient is 4096 ÷ 4096) = 1x, and the resulting VW image is unchanged from the image source.]
  - — 400h (1024 decimal), the vertical upscaling coefficient is 4x. [The vertical upscaling coefficient is (4096 ÷ 1024) = 4x, and the resulting VW image is four times as large as the image source.]
  - — 800h (2048 decimal), the vertical upscaling coefficient is 2x. [The vertical upscaling coefficient is (4096 ÷ 2048) = 2x, and the resulting VW image is two times as large as the image source.]
- When vertical upscaling of greater than 1x is chosen:
  - — Some scanlines are generated by vertical replication of source image scanlines.
  - — As a result of this generation, since the physical height of the VW is fixed by the Vertical Start and Vertical End values, some scanlines at the bottom of the source image do not display. In contrast to horizontal upscaling, with vertical upscaling, the VW dimension (in this case, height) is kept constant and the extra source scanlines are not displayed.

12.85 CR33: VW Horizontal Start High Register

I/O Port Address: 3?5

Index: 33

Bit	Description	Reset State
7	VW Horizontal Start [10]	0
6	VW Horizontal Start [9]	0
5	VW Horizontal Start [8]	0
4	Reserved	
3	MotionVideo Controller Test Mode [3]	0
2	MotionVideo Controller Test Mode [2]	0
1	MotionVideo Controller Test Mode [1]	0
0	MotionVideo Controller Test Mode [0]	0

This register controls the horizontal start of the VW. In the VW, the horizontal start is programmed using the number of memory cycles used by the surrounding pixel-depth resolution.

Bit **Description**

7:5 **VW Horizontal Start [10:8]:**
These bits are the most-significant 3 bits of a 11-bit field that defines the horizontal start of the VW.

Register Format for 11-Bit VW Horizontal Start Position in Pixels

CR33[7:5]		CR34[7:0]	
10	8	7	0

- For details on this field, refer to Extension register CR34.

4 **Reserved**

3:0 **MotionVideo Controller Test Mode [3:0]:**
This 4-bit field is used only for factory testing of the internal CL-GD7556 MotionVideo Controller.

12.86 CR34: VW Horizontal Start Low Register

I/O Port Address: 3?5

Index: 34

Bit	Description	Reset State
7	VW Horizontal Start [7]	0
6	VW Horizontal Start [6]	0
5	VW Horizontal Start [5]	0
4	VW Horizontal Start [4]	0
3	VW Horizontal Start [3]	0
2	VW Horizontal Start [2]	0
1	VW Horizontal Start [1]	0
0	VW Horizontal Start [0]	0

This register contains the least-significant 8 bits of the 11-bit VW horizontal start field.

Bit **Description**

7:0 **VW Horizontal Start [7:0]:**
Bits [10:8], the most-significant 3 bits of a 11-bit field that defines the horizontal start of the VW, are in CR33[7:5].

- These bits [7:0] are the least-significant 8 bits.

Register Format for 11-Bit VW Horizontal Start Position in Pixels

CR33[7:5]		CR34[7:0]	
10	8	7	0

- These bits program the actual horizontal start position, in pixels. The CL-GD7556 calculates all variables that effect the final value used internally.

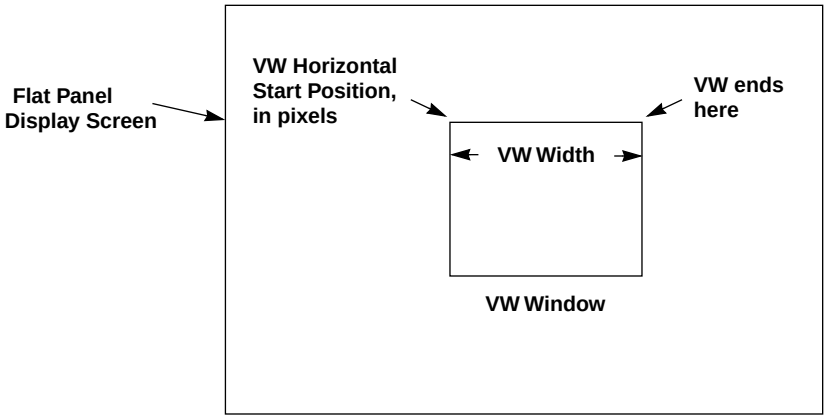


Figure 12-1. Flat Panel Display Screen with VW

12.87 CR35: VW Brightness Control Register

I/O Port Address: 3?5

Index: 35

Bit	Description	Reset State
7	VW Brightness Control [7]	0
6	VW Brightness Control [6]	0
5	VW Brightness Control [5]	0
4	VW Brightness Control [4]	0
3	VW Brightness Control [3]	0
2	VW Brightness Control [2]	0
1	VW Brightness Control [1]	0
0	VW Brightness Control [0]	0

This register controls the VW brightness.

Bit	Description
7:0	**VW Brightness Control [7:0]:** The value in this register: • Is added to the luminance value of each data pixel to enhance the brightness quality of an image within the VW. • Is expressed in terms of 2's complement. • When positive (such as Ah), increases the luminance value of each pixel. • When negative (such as –Ah), decreases the luminance value of each pixel.

12.88 CR36: VW Vertical Position Extension Register

I/O Port Address: 3?5

Index: 36

Bit	Description	Reset State
7	Force Packed-Pixel Addressing for Display Memory Map	0
6	VW CLUT-RAM Enable	0
5	Excess 128 Data Format Select	1
4	VW Memory Address Offset [8]	0
3	VW Vertical Height [9]	0
2	VW Vertical Height [8]	0
1	VW Vertical Start [9]	0
0	VW Vertical Start [8]	0

Bit **Description**

7 **Force Packed-Pixel Addressing for Display Memory Map:**
This bit is used to update a hardware icon when the display mode being used is not a packed-pixel mode (for example, mode 3h, mode 12h, and so forth). To write to a hardware icon display memory area when the display mode:
- Is not a packed-pixel mode, this bit must be set to 1. The bit must be cleared to 0 after the hardware icon is updated.
- Is a packed-pixel mode, this bit can be set to any value.

6 **VW CLUT-RAM Enable:**
When the VW is enabled (that is, CR3C[4] is 1) *and* this bit is:
- 0, the VW CLUT (color look-up table) RAM is disabled.
  - — In this case, the video data bypasses the VW CLUT-RAM and is instead routed directly to the display screen(s).
- 1, the VW CLUT-RAM is enabled.
  - — In this case, the video data is altered by changing the values stored in the VW CLUT-RAM.
  - — A ‘Color Balance’ utility is available from Cirrus Logic to program the CLUT-RAM with values that change the color and brightness of the video image.

5 **Excess 128 Data Format Select:**
When this bit is:
- 0, the selected data format is 2’s complement.
- 1, the selected data format is excess 128 data format (which is the default).

4 **VW Memory Address Offset [8]:**
This bit is the most-significant bit of the 9-bit VW Memory Address Offset field.

Register Format for 9-Bit VW Memory Address Offset

CR36[4]	CR3B[7:0]	
8	7	0

- For details on this field, refer to Extension register CR3B.

12.88 CR36: VW Vertical Position Extension Register *(cont.)*

Bit	Description
3:2	**VW Vertical Height [9:8]:** These bits are the most-significant 2 bits of the 10-bit VW Vertical Height field. **Register Format for 10-Bit VW Vertical Height** CR36[3:2] (9 8) | CR38[7:0] (7 0) • For details on this field, refer to Extension register CR38.
1:0	**VW Vertical Start [9:8]:** These bits are the most-significant 2 bits of the 10-bit VW Vertical Start field. **Register Format for 10-Bit VW Vertical Start** CR36[1:0] (9 8) | CR37[7:0] (7 0) • For details on this field, refer to Extension register CR37.

12.89 CR37: VW Vertical Start Register

I/O Port Address: 3?5

Index: 37

Bit	Description	Reset State
7	VW Vertical Start [7]	0
6	VW Vertical Start [6]	0
5	VW Vertical Start [5]	0
4	VW Vertical Start [4]	0
3	VW Vertical Start [3]	0
2	VW Vertical Start [2]	0
1	VW Vertical Start [1]	0
0	VW Vertical Start [0]	0

Bit	Description
7:0	**VW Vertical Start [7:0]:** Bits [9:8], the most-significant bits of the 10-bit VW Vertical Start field, are in Extension register CR36[1:0]. • These bits [7:0] are the least-significant 8 bits. **Register Format for 10-Bit VW Vertical Start** CR36[1:0] (9 8) | CR37[7:0] (7 0) • The 10 bits of this field: — Define the first scanline of the VW. — Are not affected by scanline doubling or flat panel vertical expansion.

12.90 CR38: VW Vertical Height Register

I/O Port Address: 3?5

Index: 38

Bit	Description	Reset State
7	VW Vertical Height [7]	0
6	VW Vertical Height [6]	0
5	VW Vertical Height [5]	0
4	VW Vertical Height [4]	0
3	VW Vertical Height [3]	0
2	VW Vertical Height [2]	0
1	VW Vertical Height [1]	0
0	VW Vertical Height [0]	0

Bit **Description**

7:0 **VW Vertical Height [7:0]:**
Bits [9:8], the most-significant bits of the 10-bit VW Vertical Height field, are in Extension register CR36[3:2].

- These bits [7:0] are the least-significant 8 bits.

Register Format for 10-Bit VW Vertical Height

CR36[3:2]		CR38[7:0]	
9	8	7	0

- The 10 bits of this field:
  - — Define the height of the VW.
  - — Are not affected by scanline doubling or flat panel vertical expansion.
  - — Are programmed before upscaling the VW vertically, based on the size of the image in memory that is to be displayed.
- To program this field, the value that must be used is (*n*-1), where *n* is the vertical height. For example, for a vertical height of 240, the number to be programmed is 240 – 1 = 239 (that is, EFh).

12.91 CR39: VW Upscaling Coefficients Low Register

I/O Port Address: 3?5

Index: 39

Bit	Description	Reset State
7	VW Horizontal Upscaling Coefficient [3]	0
6	VW Horizontal Upscaling Coefficient [2]	0
5	VW Horizontal Upscaling Coefficient [1]	0
4	VW Horizontal Upscaling Coefficient [0]	0
3	VW Vertical Upscaling Coefficient [3]	0
2	VW Vertical Upscaling Coefficient [2]	0
1	VW Vertical Upscaling Coefficient [1]	0
0	VW Vertical Upscaling Coefficient [0]	0

This register contains the least-significant 4 bits for both the 12-bit VW Horizontal and Vertical Upscaling Coefficient fields.

Bit — **Description**

7:4 **VW Horizontal Upscaling Coefficient [3:0]:**
These bits are the least-significant 4 bits of the 12-bit field for the VW HU (VW Horizontal Upscaling) Coefficient.

Register Format for 12-Bit VW Horizontal Upscaling Coefficient

CR31[7:0]		CR39[7:4]	
11	4	3	0

- For details on this field, refer to Extension register CR31.

3:0 **VW Vertical Upscaling Coefficient [3:0]:**
These bits are the least-significant 4 bits of the 12-bit field for the VW VU (VW Vertical Upscaling) Coefficient.

Register Format for 12-Bit VW Vertical Upscaling Coefficient

CR32[7:0]		CR39[3:0]	
11	4	3	0

- For details on this field, refer to Extension register CR32.

12.92 CR3A: VW Memory Start Address High Register

I/O Port Address: 3?5

Index: 3A

Bit	Description	Reset State
7	Invert MVA Clock (Factory testing bit)	0
6	VW Memory Start Address [19]	0
5	VW Memory Start Address [18]	0
4	VW Memory Start Address [17]	0
3	VW Memory Start Address [16]	0
2	VW Memory Start Address [15]	0
1	VW Memory Start Address [14]	0
0	VW Memory Start Address [13]	0

Bit **Description**

7 **Invert MVA Clock (Factory testing bit):**
When this bit is 1, the MVA clock is inverted.

6:0 **VW Memory Start Address [19:13]:**
The 20-bit VW Memory Start Address field consists of the following bits:

- Bits [19:13], the 7 most-significant bits, are in this register.
- Bits [12:5] are in CR3E[7:0].
- Bits [4:1] are in CR3F[3:0].
- Bit 0, the least-significant bit, is in CR40[0].

Register Format for 20-Bit VW Memory Start Address

CR3A[6:0]		CR3E[7:0]		CR3F[3:0]		CR40[0]
19	13	12	5	4	1	0

- When bit 0 of this field is:
  - — 0, all doubleword accesses occur on a 64-bit boundary.
  - — 1, all doubleword accesses occur on a 32-bit boundary.
- The VW Memory Start address is programmed in increments of quadwords on 64-bit boundaries. As an example of how to program this field, for:
  - — 1 Mbyte, the physical address is 00000h:1FFFFh from the display memory start.
  - — 2 Mbytes, the physical address is 00000h:3FFFFh from the display memory start.
- When this register is the only one of the four that is set to a non-zero value, the VW is aligned at a 16-Kbyte boundary in the host CPU address space.

CAUTION: Updates to the VW Memory Start Address registers must be done in the following sequence for the new address to take effect:
1. CR40[0]
2. CR3A[6:0]
3. CR3E[7:0]
4. CR3F[3:0] (These 4 bits must be written, even when they are not changed, for any new VW Memory Start Address to take effect.)

12.93 CR3B: VW Memory Address Offset Register

I/O Port Address: 3?5

Index: 3B

Bit	Description	Reset State
7	VW Memory Address Offset [7]	0
6	VW Memory Address Offset [6]	0
5	VW Memory Address Offset [5]	0
4	VW Memory Address Offset [4]	0
3	VW Memory Address Offset [3]	0
2	VW Memory Address Offset [2]	0
1	VW Memory Address Offset [1]	0
0	VW Memory Address Offset [0]	0

This register, along with the most-significant bit in Extension register bit CR36[4], defines the VW memory address offset value.

Bit **Description**

7:0 **VW Memory Address Offset [7:0]:**
Bit 8, the most-significant bit of the 9-bit VW memory address offset field, is in Extension register CR36[4].

- These bits [7:0] are the least-significant 8 bits.

Register Format for 9-Bit VW Memory Address Offset

CR36[4]	CR3B[7:0]	
8	7	0

- This offset value is expressed as a doubleword, and is added to the present VW Memory Start Address to obtain the next VW Memory Start Address.

  ADD: Present VW Memory Start Address
  TO: + VW Memory Address Offset (9-bit value) × 2
  TO OBTAIN: = Next VW Memory Start Address

- Using the VW Memory Address Offset to define the next memory-start address of the VW allows panning through a large area of the VW. The actual image stored in memory can be as large as 2K pixels at 16 bits/pixel.

12.94 CR3C: VW Data Format Register

I/O Port Address: 3?5

Index: 3C

Bit	Description	Reset State
7	VW Horizontal Pixel Width [10]	0
6	VW Horizontal Pixel Width [9]	0
5	VW Horizontal Pixel Width [0]	0
4	VW Enable	0
3	VW Data Encoding Format [3]	0
2	VW Data Encoding Format [2]	0
1	VW Data Encoding Format [1]	0
0	VW Data Encoding Format [0]	0

Bit — **Description**

7:6 **VW Horizontal Pixel Width [10:9]:**
These bits are the most-significant of the 11-bit VW Horizontal Pixel Width field.
- For details on this field, refer to CR3D.

5 **VW Horizontal Pixel Width [0]:**
This bit is the least-significant bit of the 11-bit VW Horizontal Pixel Width field.
- For details on this field, refer to CR3D.

4 **VW Enable:**
When this bit is:
- 0, the VW is not shown on the display screen.
- 1, the VW controller is enabled to fetch data from off-screen display memory and display it on the screen, based on current programming for VW registers. This bit takes effect on the leading edge of the next VSYNC signal.

3:0 **VW Data Encoding Format [3:0]:**
This 4-bit field defines the data encoding format for the VW data.

CR3C[3:0]		Encoding Format for VW
Hex	**Binary**	**Description**
0h	‘0000’	VW power-down (default)
1h	‘0001’	15-bit RGB 5-5-5
2h	‘0010’	AccuPak
3h	‘0011’	YUV 4:2:2 Y0U Y1V (On the CPU bus, this encoding format appears as UY0 VY1.)
4h	‘0100’	16-bit RGB 5-6-5
5h	‘0101’	DYUV
6h-Fh	all others	Reserved

NOTE: Reserved bit-patterns must not be programmed, as results are indeterminate.

12.95 CR3D: VW Horizontal Pixel Width Register

I/O Port Address: 3?5

Index: 3D

Bit	Description	Reset State
7	VW Horizontal Pixel Width [8]	0
6	VW Horizontal Pixel Width [7]	0
5	VW Horizontal Pixel Width [6]	0
4	VW Horizontal Pixel Width [5]	0
3	VW Horizontal Pixel Width [4]	0
2	VW Horizontal Pixel Width [3]	0
1	VW Horizontal Pixel Width [2]	0
0	VW Horizontal Pixel Width [1]	0

Bit **Description**

7:0 **VW Horizontal Pixel Width [8:1]:**
Bits [10:9], the most-significant 2 bits of the 11-bit VW Horizontal Pixel Width field, are in Extension register CR3C[7:6].

- These bits [8:1], along with bit 0 in CR3C[5], are the least-significant 9 bits.

Register Format for 11-Bit VW Horizontal Pixel Width

CR3C[7:6]		CR3D[7:0]		CR3C[5]
10	9	8	1	0

- The VW Horizontal Pixel Width field:
  - — Contains a hex value used to define the VW width for each scanline, when the VW is enabled. The hex value represents the VW width as it is to be displayed, before on-chip upscaling. (Refer to Figure 12-2.)
  - — Must be at least 32 pixels wide.
  - — Must have a value that is one less than the true width of the VW pixel width.

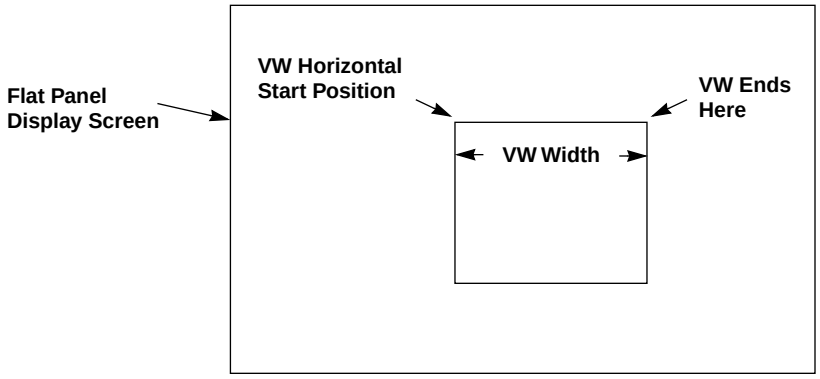


Figure 12-2. Flat Panel Display Screen with VW

12.96 CR3E: VW Memory Start Address Middle Register

I/O Port Address: 3?5

Index: 3E

Bit	Description	Reset State
7	VW Memory Start Address [12]	0
6	VW Memory Start Address [11]	0
5	VW Memory Start Address [10]	0
4	VW Memory Start Address [9]	0
3	VW Memory Start Address [8]	0
2	VW Memory Start Address [7]	0
1	VW Memory Start Address [6]	0
0	VW Memory Start Address [5]	0

The VW Memory Start Address is updated on every write to the CR3F register.

Bit	Description
7:0	**VW Memory Start Address [12:5]:** These bits are the middle 8 bits of the VW Memory Start Address field.

Register Format for 20-Bit VW Memory Start Address

CR3A[6:0]		CR3E[7:0]		CR3F[3:0]		CR40[0]
19	13	12	5	4	1	0

- For details on this field, refer to Extension register CR3A.

12.97 CR3F: VW Interpolation and Memory Start Address Low Register

I/O Port Address: 3?5

Index: 3F

Bit	Description	Reset State
7	VW Horizontal Pixel Interpolation Enable	0
6	VW Vertical Scanline Interpolation Enable	0
5	VW Occlusion Enable	0
4	VW/Graphics Palette RAM I/O R/W Select	0
3	VW Memory Start Address [4]	0
2	VW Memory Start Address [3]	0
1	VW Memory Start Address [2]	0
0	VW Memory Start Address [1]	0

The VW Memory Start Address is updated on every write to this register.

Bit	Description
7	**VW Horizontal Pixel Interpolation Enable:** When this bit is: • 0 *and* Extension register bits CR31[7:0] and CR39[7:4] are not zero, the VW upscaling engine horizontally replicates pixels selectively, based on the coefficient programmed in Extension registers CR31 and CR39. For details, refer to Extension register CR31. • 1, horizontal upscaling is done by pixel interpolation.
6	**VW Vertical Scanline Interpolation Enable:** When this bit is: • 0 *and* Extension register bits CR32[7:0] and CR39[3:0] are not zero, the VW upscaling engine vertically replicates scanlines selectively, based on the coefficient programmed in Extension registers CR32 and CR39. For details, refer to Extension register CR32. • 1, vertical upscaling is done by scanline interpolation.
5	**VW Occlusion Enable:** Within the VW, occlusion can be used to allow graphics data to be superimposed over video data. When this bit is: • 0, occlusion is disabled. In this case, when the VW is enabled, the VW video data is always on top. • 1, occlusion is enabled. In this case, the areas of video data within the VW that are to be occluded (that is, replaced by graphics data) are determined by either the color key or the chroma key. When the VW is enabled *and* CR42[0] is: — 0, the VW color key is selected. As a result, the color key that is specified by the GRC and GRD registers is used in combination with the VW controls (such as the horizontal and vertical position controls) to select, on a pixel-by-pixel basis, the data that appears on top within the VW (that is, either graphics or video data). — 1, the VW chroma key is selected and it selects, on a pixel-by-pixel basis, the graphics data that appears on top of the video data within the VW. Graphics is displayed in the VW in those areas specified by the chroma key ranges defined for the YUV data in Extension registers GRC, GRD, GR1C, GR1D, GR1E, and GR1F.

12.97 CR3F: VW Interpolation and Memory Start Address Low Register *(cont.)*

Bit	Description
4	**VW/Graphics Palette RAM I/O R/W Select:** This bit selects which of two palette CLUT RAMs is written or updated by the host CPU. The data written to these CLUT RAMs reflects either a gamma correction or a gamma adjustment value that modifies either the graphics data or the video data that is sent to flat panel and CRT monitor display screens. When this bit is: • 0, the graphics CLUT RAM is accessible by the host CPU. • 1, the VW CLUT RAM is accessible by the host CPU.
3:0	**VW Memory Start Address [4:1]:** These are bits [4:1] of the 20-bit VW Memory Start Address field. **Register Format for 20-Bit VW Memory Start Address** CR3A[6:0] (19–13) | CR3E[7:0] (12–5) | CR3F[3:0] (4–1) | CR40[0] (0) • For details on this field, refer to Extension register CR3A.
CAUTION:	These 4 bits must be written, even when they are not changed, for any new VW Memory Start Address to take effect.

12.98 CR40: VW Vertical Interpolation and Edge-Sharpening Control Register

I/O Port Address: 3?5

Index: 40

Bit	Description	Reset State
7	Edge Sharpening Enable	0
6	Simultaneous RGB Edge Adjustment	0
5	Line Buffer Compression Disable	0
4	Line Buffer Readout	0
3	Line Buffer Gain Control [1]	0
2	Line Buffer Gain Control [0]	0
1	VW AccuPak Dithering Enable	0
0	VW Memory Start Address [0]	0

This register is used to control the VW mechanism for edge sharpening and line buffer vertical interpolation. When high-color-contrast boundaries occur in the VW (that is, adjacent pixels within the VW have much different color intensities), the CL-GD7556 automatically detects the difference so that between adjacent pixels, replication is used instead of interpolation. This action has the effect of sharpening the color-intensity boundaries within the upscaled video image.

Bit **Description**

7 **Edge Sharpening Enable:**
When a VW is being upscaled (refer to Extension registers CR30, CR31, and CR39), this bit can be used to sharpen (that is, increase) the color contrast between adjacent pixels. When vertical interpolation is selected (that is, CR3F[6] is 1) *and* this bit is:

- 0, the edge-sharpening function is disabled. In this case, line buffer pixel data is expanded by always using vertical interpolation between the adjacent pixels.
- 1, the edge-sharpening function is enabled and takes effect on a pixel-by-pixel basis. The CL-GD7556 monitors the amount of color contrast between adjacent pixels. If, for adjacent pixels, the amount of color contrast:
  - — Does not exceed a predetermined limit:
    Edge sharpening does not occur between the adjacent pixels. In this case, line buffer pixel data is expanded by using vertical interpolation between the adjacent pixels.
  - — Exceeds the predetermined limit:
    Edge sharpening occurs between the adjacent pixels. In this case, line buffer pixel data is expanded by using vertical replication instead of vertical interpolation between the adjacent pixels. Using vertical replication has the effect of increasing the amount of color contrast between the adjacent pixels and therefore, increasing the clarity of the image.

12.98 CR40: VW Vertical Interpolation and Edge-Sharpening Control Register *(cont.)*

Bit	Description
6	**Simultaneous RGB Edge Adjustment:** When a VW is being upscaled (refer to Extension registers CR30, CR31, and CR39), this bit can be used to smooth (that is, decrease) the amount of color intensity contrast between adjacent pixels. When vertical interpolation is selected (that is, CR3F[6] is 1) *and* this bit is: • 0, the simultaneous RGB edge adjustment mechanism is disabled. In this case, when upscaling occurs: — The vertical interpolation mechanism attempts to proportionately adjust all of the red, blue, and green color components of a pixel in order to create the next pixel. — The vertical interpolation mechanism can fail when one pixel has one color (for example, red) that is much more intense compared to that same color for an adjacent pixel. In this case, the amount of color-intensity contrast exceeds a predetermined limit, and the interpolated pixels do not provide a smooth transition between the original pixel and the adjacent pixels. • 1, the simultaneous RGB edge adjustment mechanism is enabled and takes effect on a pixel-by-pixel basis. The CL-GD7556 monitors the amount of color intensity between adjacent pixels. If, for adjacent pixels, the amount of color intensity: — Does not exceed a predetermined limit: Edge smoothing does not occur between the adjacent pixels. In this case, line buffer pixel data is expanded by using vertical interpolation between the adjacent pixels. — Exceeds the predetermined limit: The vertical interpolation mechanism adjusts all of the red, blue, and green color components at the same time and in the same proportion. This adjustment has the effect of decreasing the amount of color contrast between the adjacent pixels and therefore, smoothing the appearance of the color of the image.
5	**Line-Buffer Compression Disable:** This bit is used only for **factory testing**. When this bit is: • 0, line-buffer data is compressed. • 1, line-buffer data is un-compressed.
4	**Line-Buffer Readout:** This bit is used only for **factory testing**. When this bit is: • 0, line-buffer data is interpolated before it is read. • 1, line-buffer data is not interpolated (that is, it is read directly).

12.98 CR40: VW Vertical Interpolation and Edge-Sharpening Control Register *(cont.)*

Bit | **Description**

3:2 **Line-Buffer Gain Control [1:0]:**
These 2 bits control the line-buffer gain control for vertical interpolation.

CR40		Line-Buffer Gain Control156
[3]	[2]	
0	0	Low gain
0	1	High gain
1	0	Full-range
1	1	Reserved. (Currently, this bit setting is the same setting as when bits CR40[3:2] are set to '01'.)

1 **VW AccuPak Dithering Enable:**
This bit enables noise addition in AccuPak mode. When this bit is:
- 0, packed-pixel RGB data is not affected.
- 1, the least-significant bits of decoded packed-pixel RGB data has pseudo-random noise from the CL-GD7556 internal linear feedback shift registers added to it.

0 **VW Memory Start Address [0]:**
This bit is the least-significant bit of the 20-bit VW Memory Start Address field.

Register Format for 20-Bit VW Memory Start Address

CR3A[6:0]		CR3E[7:0]		CR3F[3:0]		CR40[0]
19	13	12	5	4	1	0

- For details on this field, refer to Extension register CR3A.
- When this bit is:
  — 0, all doubleword accesses occur on a 64-bit boundary.
  — 1, all doubleword accesses occur on a 32-bit boundary.

12.99 CR41: VW Right-Side Memory Cycle Control Register

I/O Port Address: 3?5

Index: 41

Bit	Description	Reset State
7	VW and V-Port Chroma Quantization Gain Control	0
6	VW and V-Port Luminance Quantization Gain Control	0
5	VW Right-Side Transition Threshold Enable	0
4	VW Right-Side Transition Threshold without Occlusion [4]	0
3	VW Right-Side Transition Threshold without Occlusion [3]	0
2	VW Right-Side Transition Threshold without Occlusion [2]	0
1	VW Right-Side Transition Threshold without Occlusion [1]	0
0	VW Right-Side Transition Threshold without Occlusion [0]	0

Bit	Description
7	**VW and V-Port Chroma Quantization Gain Control:** When this bit is: • 0, normal gain is used for VW and V-Port chroma quantization. • 1, high gain is used for VW and V-Port chroma quantization.
6	**VW and V-Port Luminance Quantization Gain Control:** When this bit is: • 0, normal gain is used for VW and V-Port luminance quantization. • 1, high gain is used for VW and V-Port luminance quantization.
5	**VW Right-Side Transition Threshold Enable:** When the data for the VW is being fetched *and* this bit is: • 0, the pre-fetch for the background data is set at 8 cycles. • 1, the pre-fetch for the background data is set by the value in CR41[4:0].
4:0	**VW Right-Side Transition Threshold without Occlusion [4:0]:** This 5-bit field programs the number of cycles before the end of the VW for the background pre-fetch on the right side of the VW. • If CR41[5] is 0, this field is unused. • If CR41[5] is 1, to program a number for this field: — For 0 cycles, program '00000'. — For 1 cycle, program '10001' and so forth. — This field must always be more than 16 (that is, 10h). — This field must never be more than 23 (that is, 17h).

12.100 CR42: VW FIFO Threshold and Chroma Key Mode Select Register

I/O Port Address: 3?5

Index: 42

Bit	Description	Reset State
7	Line-buffer Clock Delay Selection [1]	0
6	Line-buffer Clock Delay Selection [0]	0
5	Invert Line-buffer Clock	0
4	VW Memory Start Address Update/Status	0
3	VW FIFO Threshold [1]	0
2	VW FIFO Threshold [0]	0
1	VW Chroma Key Reverse Mode Enable	0
0	VW Chroma Key Select	0

Bit **Description**

7:6 **Line-buffer Clock Delay Selection [1:0]: (Factory testing bits)**
The Line-buffer clock can be delayed to adjust the relative position of the data. These bits are set by the BIOS.

CR42		Line-Buffer Clock Delay
[7]	[6]	
0	0	1 Delay
0	1	2 Delay
1	0	3 Delay
1	1	no Delay

5 **Invert Line-buffer Clock: (Factory testing bit)**
When this bit is 1, the line-buffer clock is inverted. This bit is set by the BIOS.

4 **VW Memory Start Address Update/Status:**
This bit is:

- Set to 1 by software when any of the VW Memory Start Address registers are updated. (For information on these registers, refer to Extension register CR3A.)
- Reset to 0 automatically when the display screen is updated with a new VW Memory Start Address position.

12.100 CR42: VW FIFO Threshold and Chroma Key Mode Select Register *(cont.)*

Bit **Description**

3:2 **VW FIFO Threshold [1:0]:**
These 2 bits define the threshold (that is, the useful depth) of the VW FIFO buffer as shown in the following table:

CR42		VW FIFO Threshold
[3]	[2]	
0	0	32 levels
0	1	16 levels
1	0	8 levels
1	1	Reserved

1 **VW Chroma Key Reverse Mode Enable:**
This bit is enabled for use when all of the following conditions occur:

Bit Setting	Condition
Extension register CR3C[4] = 1	VW is active.
Extension register CR3F[5] = 1	Occlusion is enabled.
Extension register CR42[0] = 1	VW chroma key is selected.

- When this bit is enabled for use and it is:
  - — 0, within the VW, graphics are displayed in the area defined by the chroma key range. (For details, refer to CR3F[5].)
  - — 1, within the VW, video is displayed in the area defined by the chroma key range. (In this case, graphics are displayed outside the area defined by the chroma key range.)

0 **VW Chroma Key Select:**
This bit is enabled for use when all of the following conditions occur.

Bit Setting	Condition
Extension register CR3C[4] = 1	VW is active.
Extension register CR3F[5] = 1	Occlusion is enabled.

- When this bit is enabled for use and it is:
  - — 0, the color key is used to determine the graphics area that is either occluded or replaced by video data.
  - — 1, the VW chroma key is used to determine the VW area that is either occluded or replaced by graphics data. (For details, refer to CR3F[5].)

12.101 CR50: V-Port Hardware Configuration Register

I/O Port Address: 3?5

Index: 50

Bit	Description	Access	Reset State
7	V-Port Double-Edge Latch Enable	R/W	0
6	V-Port Non-Interlaced Mode Enable	R/W	0
5	V-Port Data Latch Control	R/W	0
4	V-Port Width Control	R/W	0
3	V-Port Byte-Order Swap	R/W	0
2	V-Port Pinout and Hardware Configuration [2]	R/W	0
1	V-Port Pinout and Hardware Configuration [1]	R/W	0
0	V-Port Pinout and Hardware Configuration [0]	R/W	0

This register is used to configure the V-Port pinout and hardware. However, V-Port operation does not become enabled until CR51[3] is set to 1.

Bit	Description
7	**V-Port Double-Edge Latch Enable:** When the V-Port width is 8 bits and this bit is: • 0, data are latched on only one edge of the V-Port clock. • 1, data are latched on both edges of the V-Port clock.
6	**V-Port Non-Interlaced Mode Enable:** When the this bit is: • 0, the V-Port is in the interlaced mode. • 1, the V-Port is in the non-interlaced mode.
5	**V-Port Data Latch Control:** When this bit is: • 0, the V-Port latches data on the leading edge of VPCLKI (pin 111). • 1, the V-Port latches data on the trailing edge of VPCLKI.
4	**V-Port Width Control:** When this bit is: • 0, the V-Port consists of VPY[7:0], and it is 8 bits wide. • 1, the V-Port consists of both VPC[7:0] and VPY[7:0], and it is 16 bits wide.
3	**V-Port Byte-Order Swap:** When the V-Port width is 8 bits and this bit is: • 0, for each pixel, the CL-GD7556 expects Y data first, followed by either U or V data. • 1, for each pixel, the CL-GD7556 expects either U or V data first, followed by Y data.

12.101 CR50: V-Port Hardware Configuration Register *(cont.)*

Bit	Description
2:0	**V-Port Pinout and Hardware Configuration [2:0]:** When Extension register CR51[3] is set to 1, (that is, the V-Port operation is enabled), the V-Port data and control pins are configured as shown in the following table. **NOTES:** 1) The V-Port configuration bits in CR50[2:0] must be set before CR51[3] is set to 1. 2) The configuration for the DDCC / VCLKO and DDCD pins is not affected by these bits.

CR51	CR50			Configuration
[3]	[2]	[1]	[0]	
0	X	X	X	V-Port disabled
1	0	0	0	V-Port disabled
1	0	0	1	V-Port enabled
1	0	1	X	Reserved
1	1	X	X	Reserved

12.102 CR51: V-Port Data Format Register

I/O Port Address: 3?5

Index: 51

Bit	Description	Reset State
7	V-Port FIFO Threshold in VW [2]	0
6	V-Port FIFO Threshold in VW [1]	0
5	V-Port FIFO Threshold in VW [0]	0
4	V-Port Downscaling Enable	0
3	V-Port Enable	0
2	V-Port Data Format Select [2]	0
1	V-Port Data Format Select [1]	0
0	V-Port Data Format Select [0]	0

This register is used to configure the CL-GD7556 V-Port data format.

Bit	Description
7:5	**V-Port FIFO Threshold in VW [2:0]:** The value programmed in these 3 bits determines the number of CAS# cycles in each V-Port FIFO fill cycle within the Capture Window, except for V-Port FIFO flush cycles.
4	**V-Port Downscaling Enable:** When this bit is: • 0, V-Port downscaling is disabled. • 1, V-Port downscaling is enabled, and the following color space formats can be downscaled with the appropriate bit settings of CR51[2:0]: — YUV 4:2:2 — YUV 4:2:2 compressed to AccuPak — YUV 4:2:2 compressed to DYUV **NOTE:** Video data from AccuPak cannot be downscaled within the V-Port. Instead, the data must be scaled down within the original source of the video data.
3	**V-Port Enable:** This bit enables the V-Port operations. When this bit is: • 0, the V-Port is disabled. • 1, the V-Port is enabled. (Before this bit can be set to 1, the V-Port configuration bits in CR50[2:0] must be set to '001'.) — Memory cycles occur based on the current V-Port configuration, and the V-Port data is displayed. — This bit takes effect on the trailing edge of the V-Port VSI (vertical sync input) signal.

12.102 CR51: V-Port Data Format Register *(cont.)*

Bit	Description
2:0	**V-Port Data Format Select:** These bits select the format of the V-Port data, according to the following table.

CR51			V-Port Data Format
[2]	[1]	[0]	
0	0	0	YUV 4:2:2
0	0	1	RGB 5-5-5
0	1	0	AccuPak
0	1	1	YUV 4:2:2, compressed to AccuPak by the CL-GD7556 before being sent to frame buffers
1	0	0	YUV 4:2:2, compressed to DYUV by the CL-GD7556 before being sent to frame buffers
1	0	1	Reserved
1	1	X	

12.103 CR52: V-Port Horizontal Downscaling Coefficient High Register

I/O Port Address: 3?5

Index: 52

Bit	Description	Reset State
7	V-Port Horizontal Downscaling Coefficient [11]	0
6	V-Port Horizontal Downscaling Coefficient [10]	0
5	V-Port Horizontal Downscaling Coefficient [9]	0
4	V-Port Horizontal Downscaling Coefficient [8]	0
3	V-Port Horizontal Downscaling Coefficient [7]	0
2	V-Port Horizontal Downscaling Coefficient [6]	0
1	V-Port Horizontal Downscaling Coefficient [5]	0
0	V-Port Horizontal Downscaling Coefficient [4]	0

This register is used to set the coefficient for the V-Port horizontal downscaling.

Bit **Description**

7:0 **V-Port Horizontal Downscaling Coefficient [11:4]:**
These bits [11:4] are the most-significant 8 bits of the coefficient for V-Port horizontal downscaling, which is done through pixel decimation.

- Bits [3:0], the least-significant bits, are in CR5B[3:0]. (These bits are for fine tuning and are not included in the calculation.)

Register Format for 12-Bit V-Port Horizontal Downscaling Coefficient

CR52[7:0]		CR5B[3:0]	
11	4	3	0

To calculate the V-Port horizontal downscaling coefficient:

DIVIDE: The value in CR52[7:0] (in its decimal form)
BY: ÷ 256 (This register is an 8-bit register, and $2^8 = 256$.)

TO OBTAIN: = V-Port Horizontal Downscaling Coefficient

NOTE: When the value in CR52[7:0] is 00h and the value in CR5B[3:0] is 0h, no downscaling can occur.

12.104 CR53: V-Port Vertical Downscaling Coefficient High Register

I/O Port Address: 3?5

Index: 53

Bit	Description	Reset State
7	V-Port Vertical Downscaling Coefficient [11]	0
6	V-Port Vertical Downscaling Coefficient [10]	0
5	V-Port Vertical Downscaling Coefficient [9]	0
4	V-Port Vertical Downscaling Coefficient [8]	0
3	V-Port Vertical Downscaling Coefficient [7]	0
2	V-Port Vertical Downscaling Coefficient [6]	0
1	V-Port Vertical Downscaling Coefficient [5]	0
0	V-Port Vertical Downscaling Coefficient [4]	0

This register is used to set the coefficient for the V-Port Vertical downscaling.

Bit **Description**

7:0 **V-Port Vertical Downscaling Coefficient [11:4]:**
These bits [11:4] are the most-significant 8 bits of the coefficient for V-Port vertical downscaling, which is done through pixel decimation.

- Bits [3:0], the least-significant bits, are in CR5B[7:4]. (These bits are for fine tuning, and are not included in the calculation.)

Register Format for 12-Bit V-Port Vertical Downscaling Coefficient

CR53[7:0]		CR5B[7:4]	
11	4	3	0

To calculate the V-Port vertical downscaling coefficient:

DIVIDE: The value in CR53[7:0] (in its decimal form)
BY: ÷ 256 (This register is an 8-bit register, and $2^8 = 256$.)

TO OBTAIN: = V-Port Vertical Downscaling Coefficient

NOTE: When the value in CR53[7:0] is 00h and the value in CR5B[7:4] is 0h, no downscaling can occur.

12.105 CR54: V-Port Capture Window Horizontal Start Register

I/O Port Address: 3?5

Index: 54

Bit	Description	Reset State
7	V-Port Capture Window Horizontal Start [7]	0
6	V-Port Capture Window Horizontal Start [6]	0
5	V-Port Capture Window Horizontal Start [5]	0
4	V-Port Capture Window Horizontal Start [4]	0
3	V-Port Capture Window Horizontal Start [3]	0
2	V-Port Capture Window Horizontal Start [2]	0
1	V-Port Capture Window Horizontal Start [1]	0
0	V-Port Capture Window Horizontal Start [0]	0

This register is used to set a delay for the Horizontal start position of the V-Port Capture Window.

Bit **Description**

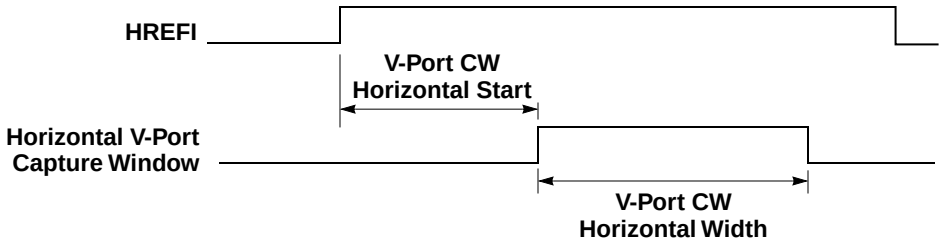
7:0 **V-Port Capture Window Horizontal Start [7:0]:**
Bits [9:8], the most-significant 2 bits of the 10-bit V-Port Capture Window Horizontal Start field, are in CR58[1:0].

- These bits [7:0] are the least-significant bits.

Register Format for 10-Bit V-Port Capture Window Horizontal Start

CR58[1:0]		CR54[7:0]	
9	8	7	0

- This field expresses a value for the position of the horizontal start of the V-Port Capture Window. The start value:
  - — In contrast to CR55 (the V-Port Capture Window Horizontal Width register), is expressed in pixels *before* the video data is scaled down.
  - — Must always be a multiple of two.
- The following timing diagram shows the relationship of the V-Port Capture Window Horizontal start signal to the HREFI signal (which is generated by the decoder).



12.106 CR55: V-Port Capture Window Horizontal Width Register

I/O Port Address: 3?5

Index: 55

Bit	Description	Reset State
7	V-Port Capture Window Horizontal Width [7]	0
6	V-Port Capture Window Horizontal Width [6]	0
5	V-Port Capture Window Horizontal Width [5]	0
4	V-Port Capture Window Horizontal Width [4]	0
3	V-Port Capture Window Horizontal Width [3]	0
2	V-Port Capture Window Horizontal Width [2]	0
1	V-Port Capture Window Horizontal Width [1]	0
0	V-Port Capture Window Horizontal Width [0]	0

This register is used to set the horizontal width of the V-Port Capture Window.

Bit **Description**

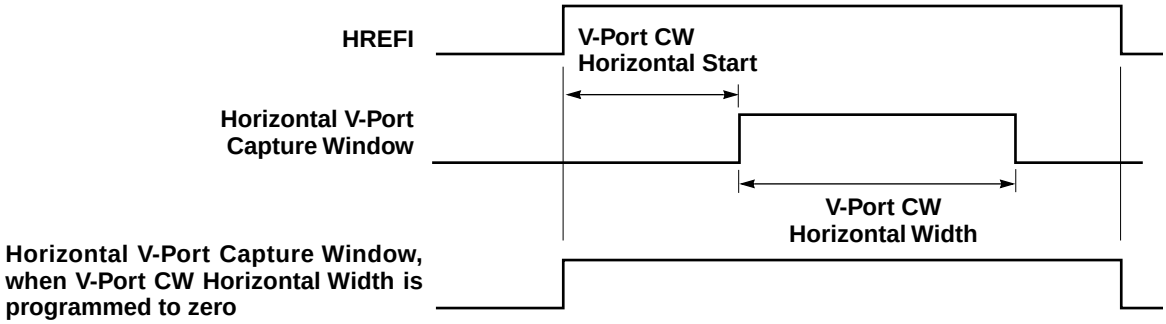
7:0 **V-Port Capture Window Horizontal Width [7:0]:**
Bits [9:8], the most-significant 2 bits of the 10-bit V-Port Capture Window Horizontal Width field, are in CR58[3:2].

- These bits [7:0] are the least-significant 8 bits.

Register Format for 10-Bit V-Port Capture Window Horizontal Width

CR58[3:2]		CR55[7:0]	
9	8	7	0

- This field expresses a value for the horizontal width of the V-Port Capture Window. The width value:
  - — In contrast to CR54 (the V-Port Capture Window Horizontal Start register), is expressed in pixels *after* the video data is scaled down.
  - — Must always be a multiple of two.
- When the value in this field is zero, then the HREFI signal defines the horizontal width of the V-Port Capture Window.
- The following timing diagram shows the relationship of the V-Port Capture Window horizontal width signal to the horizontal start signal.



12.107 CR56: V-Port Capture Window Vertical Start Register

I/O Port Address: 3?5

Index: 56

Bit	Description	Reset State
7	V-Port Capture Window Vertical Start [7]	0
6	V-Port Capture Window Vertical Start [6]	0
5	V-Port Capture Window Vertical Start [5]	0
4	V-Port Capture Window Vertical Start [4]	0
3	V-Port Capture Window Vertical Start [3]	0
2	V-Port Capture Window Vertical Start [2]	0
1	V-Port Capture Window Vertical Start [1]	0
0	V-Port Capture Window Vertical Start [0]	0

This register is used to set a delay for the vertical start of the V-Port Capture Window.

Bit **Description**

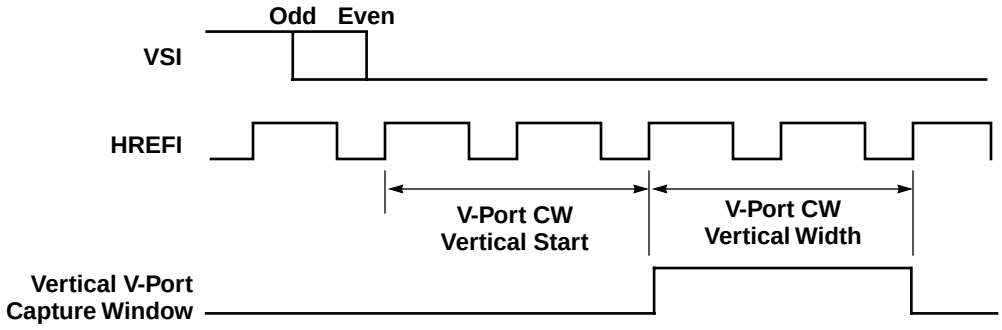
7:0 **V-Port Capture Window Vertical Start [7:0]:**
Bit 8, the most-significant bit of the 9-bit V-Port Capture Window Vertical Start field, is in CR58[4].

- These bits [7:0] are the least-significant 8 bits.

Register Format for 9-Bit V-Port Capture Window Vertical Start

CR58[4]	CR56[7:0]	
8	7	0

- This field expresses a value for the vertical start of the V-Port Capture Window. This value, based on the trailing edge of the VSI signal, shows how many HREFI pulses are skipped until the beginning of the Capture Window.
  - — The value for this field is expressed in the number of scanlines *before* the video lines have been scaled down.
  - — The value for this field is programmed as *n*, where *n* is the number of full HREFI signals to be skipped.
- The following timing diagram shows the relationship of the vertical start signal to the HREFI and the trailing edge of the VSI signal.



12.108 CR57: V-Port Capture Window Vertical Height Register

I/O Port Address: 3?5

Index: 57

Bit	Description	Reset State
7	V-Port Capture Window Vertical Height [7]	0
6	V-Port Capture Window Vertical Height [6]	0
5	V-Port Capture Window Vertical Height [5]	0
4	V-Port Capture Window Vertical Height [4]	0
3	V-Port Capture Window Vertical Height [3]	0
2	V-Port Capture Window Vertical Height [2]	0
1	V-Port Capture Window Vertical Height [1]	0
0	V-Port Capture Window Vertical Height [0]	0

This register is used to set the vertical height of the V-Port Capture Window.

Bit **Description**

7:0 **V-Port Capture Window Vertical Height [7:0]:**
Bit 8, the most-significant bit of the 9-bit V-Port Capture Window Vertical Height field, is in CR58[5].

- These bits [7:0] are the least-significant 8 bits.

Register Format for 9-Bit V-Port Capture Window Vertical Height

CR58[5]	CR57[7:0]	
8	7	0

- This 9-bit field expresses a value for the vertical height of the V-Port Capture Window. When CR51[2] is:
  - — 0, the value from this field controls how many scanlines per frame of V-Port data are captured in display memory.
  - — 1, the value from this field controls how many scanlines per field of V-Port data are captured in display memory.
- The value for this 9-bit field is expressed in the number of scanlines *after* the video data has been scaled down.
  - — Program this register for the quantity (*n* – 1), where *n* is the number of scanlines to be captured.
  - — When this register is cleared to 0, the result is 1 HREFI capture window.

12.109 CR58: V-Port Capture Window Extension Register

I/O Port Address: 3?5

Index: 58

Bit	Description	Reset State
7	Reserved	
6	V-Port Interlaced Mode Odd/Even Meaning Invert	0
5	V-Port Capture Window Vertical Height [8]	0
4	V-Port Capture Window Vertical Start [8]	0
3	V-Port Capture Window Horizontal Width [9]	0
2	V-Port Capture Window Horizontal Width [8]	0
1	V-Port Capture Window Horizontal Start [9]	0
0	V-Port Capture Window Horizontal Start [8]	0

This register contains extension bits for other V-Port Capture Window registers.

Bit **Description**

7 **Reserved**

6 **V-Port Interlaced Mode Odd/Even Meaning Invert:**
When the VSI trailing edge occurs while HREFI is high, *and* this bit is:
- 0, this condition indicates an odd field.
- 1, this condition indicates an even field.

5 **V-Port Capture Window Vertical Height [8]:**
This bit is the most-significant bit of the 9-bit V-Port Capture Window Vertical Height field.

Register Format for 9-Bit V-Port Capture Window Vertical Height

CR58[5]	CR57[7:0]	
8	7	0

- For details on this field, refer to Extension register CR57.

4 **V-Port Capture Window Vertical Start [8]:**
This bit is the most-significant bit of the 9-bit V-Port Capture Window Vertical Start field.

Register Format for 9-Bit V-Port Capture Window Vertical Start

CR58[4]	CR56[7:0]	
8	7	0

- For details on this field, refer to Extension register CR56.

12.109 CR58: V-Port Capture Window Extension Register *(cont.)*

3:2 **V-Port Capture Window Horizontal Width [9:8]:**
These bits are the most-significant 2 bits of the 10-bit V-Port Capture Window Horizontal Width field.

Register Format for 10-Bit V-Port Capture Window Horizontal Width

CR58[3:2]		CR55[7:0]	
9	8	7	0

- For details on this field, refer to Extension register CR55.

1:0 **V-Port Capture Window Horizontal Start [9:8]:**
These bits are the most-significant 2 bits of the 10-bit V-Port Capture Window Horizontal Start field.

Register Format for 10-Bit V-Port Capture Window Horizontal Start

CR58[1:0]		CR54[7:0]	
9	8	7	0

- For details on this field, refer to Extension register CR54.

12.110 CR59: V-Port Capture Window Start Address High Register

I/O Port Address: 3?5

Index: 59

Bit	Description	Reset State
7	V-Port Capture Window Start Address [19]	0
6	V-Port Capture Window Start Address [18]	0
5	V-Port Capture Window Start Address [17]	0
4	V-Port Capture Window Start Address [16]	0
3	V-Port Capture Window Start Address [15]	0
2	V-Port Capture Window Start Address [14]	0
1	V-Port Capture Window Start Address [13]	0
0	V-Port Capture Window Start Address [12]	0

This register sets the starting address in memory for data from the capture window.

Bit **Description**

7:0 **V-Port Capture Window Start Address [19:12]:**
These bits [19:12] are the 8 most-significant bits of the 20-bit field for the V-Port Capture Window Start Address field.

- Bits [11:4] are in Extension register CR5E.
- Bits [3:0], the least-significant bits, are in Extension register bits CR5F[5:2].

Register Format for 20-Bit V-Port Capture Window Start Address

CR59[7:0]		CR5E[7:0]		CR5F[5:2]	
19	12	11	4	3	0

- The value programmed in the entire 20-bit field gives the value for the address start for the V-Port Capture Window.
  - — This address start value can be changed to a new value at any time.
  - — New address start values take effect in the following vertical retrace period of the V-Port.

12.111 CR5A: V-Port Cycle and V-Port FIFO Control Register

I/O Port Address: 3?5

Index: 5A

Bit	Description	Reset State
7	V-Port Cycle Control after Non-Aligned VW FIFO Cycle [1]	0
6	V-Port Cycle Control after Non-Aligned VW FIFO Cycle [0]	0
5	Reserved	
4	Reserved	
3	V-Port FIFO Underrun Status	0
2	V-Port FIFO Threshold in Surrounding Graphics [2]	0
1	V-Port FIFO Threshold in Surrounding Graphics [1]	0
0	V-Port FIFO Threshold in Surrounding Graphics [0]	0

This register controls:

- V-Port cycles after non-aligned VW/CRT FIFO cycles
- V-Port FIFO threshold in the surrounding graphics.

Bit **Description**

7:6 **V-Port Cycle Control After Non-Aligned VW FIFO Cycle [1:0]:**
This 2-bit field controls the number of V-Port CAS# cycles that occur after the VW FIFO cycle in which a display memory page miss occurred, as indicated in the following table.

CR5A		Number of Completed V-Port Cycles Before VW FIFO Sequence Stops
[7]	[6]	
0	0	V-Port cycle is skipped.
0	1	1 V-Port CAS# cycle occurs.
1	0	2 V-Port CAS# cycles occur.
1	1	3 V-Port CAS# cycles occur.

5:4 **Reserved**

3 **V-Port FIFO Underrun Status:**
This bit reflects the V-Port FIFO underrun status. When this bit reads a:
- 0, the V-Port FIFO does not have an underrun.
- 1, the V-Port FIFO had an underrun. (That is, the V-Port did not obtain sufficient cycles to empty the V-Port FIFO to the display memory.)
- After this bit is read, it is cleared to 0.

2:0 **V-Port FIFO Threshold in Surrounding Graphics:**
These bits specify the number of V-Port CAS# cycles in the surrounding graphics during each V-Port cycle.

12.112 CR5B: V-Port Horizontal and Vertical Downscaling Low Register

I/O Port Address: 3?5

Index: 5B

Bit	Description	Reset State
7	V-Port Vertical Downscaling Coefficient [3]	0
6	V-Port Vertical Downscaling Coefficient [2]	0
5	V-Port Vertical Downscaling Coefficient [1]	0
4	V-Port Vertical Downscaling Coefficient [0]	0
3	V-Port Horizontal Downscaling Coefficient [3]	0
2	V-Port Horizontal Downscaling Coefficient [2]	0
1	V-Port Horizontal Downscaling Coefficient [1]	0
0	V-Port Horizontal Downscaling Coefficient [0]	0

Bit **Description**

7:4 **V-Port Vertical Downscaling Coefficient [3:0]:**
These bits are the least-significant 4 bits of the 12-bit V-Port Vertical Downscaling Coefficient.

Register Format for 12-Bit V-Port Vertical Downscaling Coefficient

CR53[7:0]		CR5B[7:4]	
11	4	3	0

- For details on this field, refer to Extension register CR53.

3:0 **V-Port Horizontal Downscaling Coefficient [3:0]:**
These bits are the least-significant 4 bits of the 12-bit V-Port Horizontal Downscaling Coefficient.

Register Format for 12-Bit V-Port Horizontal Downscaling Coefficient

CR52[7:0]		CR5B[3:0]	
11	4	3	0

- For details on this field, refer to Extension register CR52.

12.113 CR5C: V-Port Capture Control Register

I/O Port Address: 3?5

Index: 5C

Bit	Description	Reset State
7	Reserved	
6	V-Port Capture Window Odd-Field Enable for MPEG Fields	0
5	V-Port Capture Window Two-Field Enable	0
4	V-Port IRQ Enable and IRQ Source	0
3	V-Port IRQ Reset	0
2	V-Port Capture Window Vertical Height Definition	0
1	V-Port Interrupt Request Status	0
0	Reserved	

Bit	Description
7	**Reserved**
6	**V-Port Capture Window Odd-Field Enable for MPEG Fields:** This bit enables high-quality MPEG field capture. When this bit is: • 0, both the odd and even MPEG fields are captured. • 1, *and* Extension register CR58[6] is: — 0, this bit enables only the capture of an odd MPEG field. — 1, this bit enables only the capture of an even MPEG field.
5	**V-Port Capture Window Two-Field Enable:** When this bit is set to 1, *and* Extension register CR51[3] is 0 (that is, the V-Port is disabled for normal operation), this bit allows one frame to be captured through the V-Port for debug purposes. • In this case, this bit enables a V-Port Capture Window for two full V-Port fields (that is, one frame). • This bit remains set to 1 for only two full V-Port fields, after it is initially set by I/O. • At the end of the two full fields of video capture, this bit automatically clears to 0, and the V-Port is disabled (that is, as long as CR51[3] is 0).
4	**V-Port IRQ Enable and IRQ Source:** When this bit is: • 0, the V-Port IRQ (interrupt request) is disabled. In this case, the IRQ source is the CRT monitor VSYNC signal on the INTR# pin. • 1, the V-Port IRQ is enabled. In this case, the IRQ source is the V-Port VSI signal on the INTR# pin, which overrides the CRT monitor VSYNC IRQ input.
3	**V-Port IRQ Reset:** When this bit is set to: • 0, V-Port IRQ is enabled. • 1, the V-Port IRQ is reset to 0.

12.113 CR5C: V-Port Capture Control Register *(cont.)*

Bit	Description
2	**V-Port Capture Window Vertical Height Definition:** When this bit is: • 0, the V-Port Capture Window vertical height value in Extension register bits CR58[5] and CR57[7:0] define the number of scanlines per frame. • 1, the V-Port Capture Window vertical height value in Extension register bits CR58[5] and CR57[7:0] define the number of scanlines per field.
1	**V-Port Interrupt Request Status:** When this read-only bit is: • 0, the V-Port interrupt request has not occurred. • 1, the V-Port interrupt request has occurred.
0	**Reserved**

12.114 CR5D: Number of Memory Cycles per Scanline Override Register

I/O Port Address: 3?5

Index: 5D

Bit	Description	Reset State
7	Number of Memory Cycles per Scanline Override [7]	0
6	Number of Memory Cycles per Scanline Override [6]	0
5	Number of Memory Cycles per Scanline Override [5]	0
4	Number of Memory Cycles per Scanline Override [4]	0
3	Number of Memory Cycles per Scanline Override [3]	0
2	Number of Memory Cycles per Scanline Override [2]	0
1	Number of Memory Cycles per Scanline Override [1]	0
0	Number of Memory Cycles per Scanline Override [0]	0

Bit	Description
7:0	**Number of Memory Cycles per Scanline Override [7:0]:** This 8-bit field is used to redefine the number of display memory fetches allocated for each scanline of display data. When CR5F[7] is: • 0, this field is disabled. • 1, this field is enabled, and the standard VGA display-scanline memory-fetch-allocation registers are disabled.

12.115 CR5E: V-Port Capture Window Start Address Middle Register

I/O Port Address: 3?5

Index: 5E

Bit	Description	Reset State
7	V-Port Capture Window Start Address [11]	0
6	V-Port Capture Window Start Address [10]	0
5	V-Port Capture Window Start Address [9]	0
4	V-Port Capture Window Start Address [8]	0
3	V-Port Capture Window Start Address [7]	0
2	V-Port Capture Window Start Address [6]	0
1	V-Port Capture Window Start Address [5]	0
0	V-Port Capture Window Start Address [4]	0

Bit **Description**

7:0 **V-Port Capture Window Start Address [11:4]:**
These bits are the middle 8 bits of the 20-bit V-Port Capture Window Start Address field.

Register Format for 20-Bit V-Port Capture Window Start Address

CR59[7:0]		CR5E[7:0]		CR5F[5:2]	
19	12	11	4	3	0

- For details on this field, refer to Extension register CR59.

12.116 CR5F: V-Port Capture Window Start Address Low Register

I/O Port Address: 3?5

Index: 5F

Bit	Description	Reset State
7	Number of Memory Cycles per Scanline Override Enable	0
6	HREFI Invert	0
5	V-Port Capture Window Start Address [3]	0
4	V-Port Capture Window Start Address [2]	0
3	V-Port Capture Window Start Address [1]	0
2	V-Port Capture Window Start Address [0]	0
1	Reserved	
0	V-Port AccuPak Dithering Enable	0

Bit **Description**

7 **Number of Memory Cycles per Scanline Override Enable:**
When this bit is:
- 0, this function is disabled.
- 1, this bit:
  - — Enables CR5D[7:0].
  - — Disables the standard VGA display-scanline memory-fetch-allocation registers.

6 **HREFI Invert**
When this bit is 1, the sense input to the HREFI pin is inverted.

NOTE: When the HREFI signal from a video decoder is low during the horizontal display period, set this bit to 1.

5:2 **V-Port Capture Window Start Address [3:0]:**
These bits are the least-significant 4 bits of the 20-bit V-Port Capture Window Start Address field.

Register Format for 20-Bit V-Port Capture Window Start Address

CR59[7:0]		CR5E[7:0]		CR5F[5:2]	
19	12	11	4	3	0

- For details on this field, refer to Extension register CR59.

1 **Reserved**

0 **V-Port AccuPak Dithering Enable:**
When this bit is 1 *and* the VW data is in the AccuPak format on the data-compression side of the VW, dithering is enabled for data sent to the display memory.

12.117 CR80: Power Management Control Register

I/O Port Address: 3?5

Index: 80

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Standby Mode Activate (Timer Control Override)	0
2	Suspend Mode Activate	0
1	CRT Monitor Enable	1
0	Flat Panel Enable	0

Bit	Description
7:4	**Reserved**
3	**Standby Mode Activate (Timer Control Override):** When this bit is programmed to: • 0, the current internal hardware-controlled Standby mode timer setting of CR8B[3:0] controls when the CL-GD7556 is placed into Standby mode. • 1, the CL-GD7556 is placed immediately into a software-controlled Standby mode, overriding the internal hardware-controlled Standby mode timer.
2	**Suspend Mode Activate:** This bit takes effect only when no hardware-controlled Suspend mode is in effect. When this bit is programmed to: • 0, hardware control of the Suspend mode is enabled when CR8D[2] is 1. In this case, the input on SUSPI (pin 56) controls when the CL-GD7556 is placed into Suspend mode. • 1, software control of the Suspend mode is enabled. The power-down sequence starts and the flat panel display screen is blanked. (When a CRT monitor is on, the CRT monitor display screen is blanked as well.)
1	**CRT Monitor Enable**: When this bit is: • 0, the analog CRT output from the DAC is disabled, along with the CRT monitor timing control signals, HSYNC and VSYNC. • 1, the analog CRT output from the DAC is enabled, and so a CRT monitor can be enabled. • 1 *and* CR80[0] is 1, the SimulSCAN mode (that is, the simultaneous operation of a CRT monitor and a flat panel) is enabled.
0	**Flat Panel Enable:** When this bit is: • 0, the flat panel interface is disabled. • 1, the flat panel interface is enabled. • 1 *and* CR80[1] is 1, the SimulSCAN mode is enabled. *(Continued)*

12.117 CR80: Power Management Control Register *(cont.)*

Bit	Description
0 *(cont.)*	**Flat Panel Enable** *(cont.)*:

As shown in the following figure, when this bit is set to 1 and has a:

- 0-to-1 transition, the CL-GD7556 flat panel power-up sequence occurs, which enables the following signals in the proper sequence: the FPVCC signal, the drive signals (FPVDCLK, LFS, LLCLK, and Panel Data), and the logic supply signal (FPVEE).
- 1-to-0 transition, the CL-GD7556 flat panel power-down sequence occurs, which disables, in the proper sequence, FPVEE, the drive signals, and FPVCC.

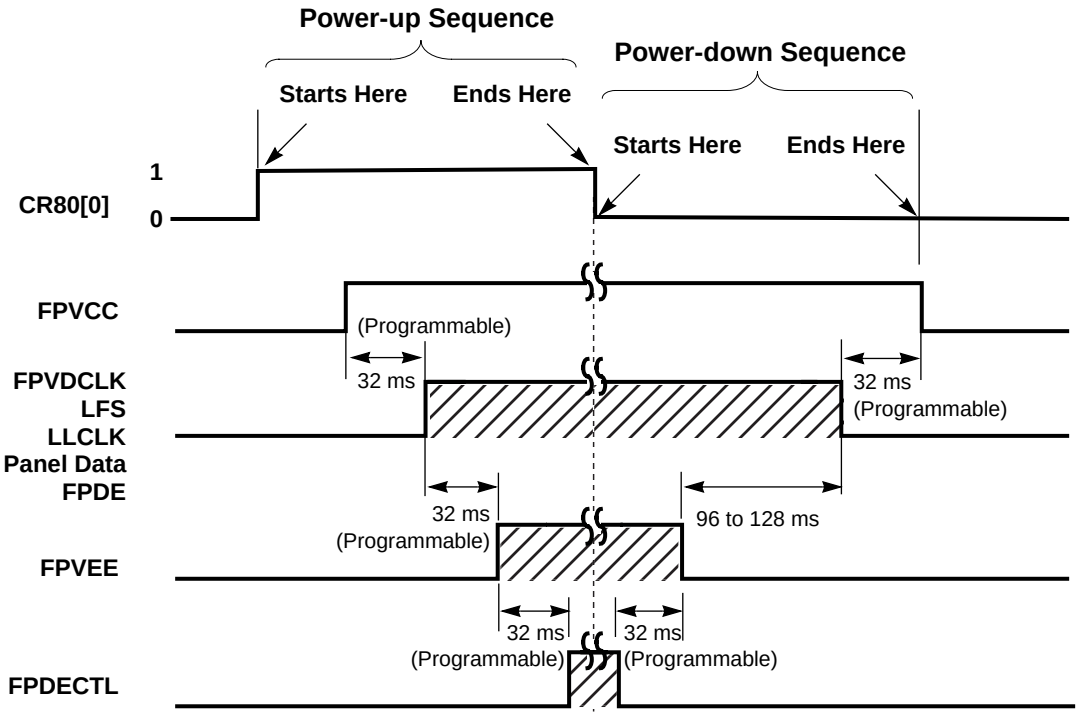


Figure 12-3. Normal Power-Up/Power-Down Sequence

NOTES:

1) The flat panel power-up sequence begins when any of the following occur:
   a) When CR80[0] transitions from 0 to 1
   b) When Standby or Suspend modes are terminated, and the flat panel was 'on' prior to entering the Standby or Suspend mode
   c) When switching from CRT-only mode to flat panel-only or SimulSCAN mode
2) The flat panel power-down sequence begins when any of the following occur:
   a) When CR80[0] transitions from 1 to 0
   b) When software-controlled Standby or Suspend modes are entered and the flat panel was previously 'on'
   c) When switching from a flat panel-only or SimulSCAN mode to a CRT-only mode
3) For information on programming the delay settings, refer to Extension register CR8C.

12.118 CR81: Flat Panel Text Automatic Centering and Expansion Register

I/O Port Address: 3?5

Index: 81

Bit	Description	Reset State
7	Reserved	
6	Flat Panel Text Vertical Expansion [1]	0
5	Flat Panel Text Vertical Expansion [0]	0
4	Flat Panel Text Automatic Vertical Centering Enable	0
3	CRT Monitor Automatic Centering Disable	0
2	Flat Panel Text Horizontal Expansion [1]	0
1	Flat Panel Text Horizontal Expansion [0]	0
0	Flat Panel Text Automatic Horizontal Centering Enable	0

Bit **Description**

7 **Reserved**

6:5 **Flat Panel Text Vertical Expansion [1:0]:**
These bits enable vertical expansion of text as shown in the following table.

Flat Panel Text Vertical Expansion:

CR81		Original Number of Scanlines	Vertical Expansion Method
[6]	[5]		
0	0	Native VGA	No vertical expansion of text when the original number of scanlines is 'native VGA'. (As an example of what is meant by 'native VGA', an 800 x 600 flat panel is set for a display mode that is also 800 x 600.)
0	1	200 (8 x 8 text)	When CRT Controller register CR9 = 07h: Normal double-scan is applied, and extra scanlines (1 top and 2 bottom) are added to each character row for a total of 475 scanlines.
		350 (8 x 14 text)	When CRT Controller register CR9 = 0Dh: Extra scanlines (2 top and 3 bottom) are added to each character row for a total of 475 scanlines.
		400 (9 x 16 text)	When CRT Controller register CR9 = 0Fh: Extra scanlines (1 top and 2 bottom) are added to each character row for a total of 475 scanlines.
1	0	200 (8 x 8 text)	When CRT Controller register CR9 = 07h: Normal double-scan is applied, and extra scanlines (4 top and 4 bottom) are added to each character row for a total of 600 scanlines.
		350 (8 x 14 text)	When CRT Controller register CR9 = 0Dh: Extra scanlines (4 top and 6 bottom) are added to each character row for a total of 600 scanlines.
		400 (9 x 16 text)	When CRT Controller register CR9 = 0Fh: Extra scanlines (4 top and 4 bottom) are added to each character row for a total of 600 scanlines.
1	1	Reserved	Reserved for future flat panel display modes.

12.118 CR81: Flat Panel Text Automatic Centering and Expansion Register *(cont.)*

Bit — **Description**

4 — **Flat Panel Text Automatic Vertical Centering Enable:**
When this bit is:
- 0, automatic vertical centering of text is disabled.
- 1 *and* when standard VGA text display mode is selected, automatic vertical centering of text is enabled.

3 — **CRT Monitor Automatic Centering Disable:**
When standard VGA display mode is selected and this bit is:
- 0, the CRT monitor image is automatically centered, which is the default.
- 1, automatic CRT vertical and horizontal centering is disabled, and the CRT monitor display starts in the top-left corner of the display screen.

2:1 — **Flat Panel Text Horizontal Expansion [1:0]:**
When standard VGA text display mode is selected, these bits enable horizontal expansion of text as shown in the following table:

Flat Panel Text Horizontal Expansion:

CR81 [2]	CR81 [1]	Original Number of Character Clocks	Expanded Number of Character Clocks	Horizontal Expansion Method
0	0	Native VGA	Native VGA	No horizontal expansion of text
0	1	640 x (8x text)	640 x (8x text)	No horizontal expansion of text (640 pixels)
		720 x (9x text)	640 x (8x text)	Force to 8-dot text (640 pixels)
1	0	640 x (8x text)	800 x (10x text)	2 pixels (9th, 10th) are added to each column when character data is within C0h–DFh
		720 x (9x text)	800 x (10x text)	1 pixel (10th) is added to each column when character data is within C0h–DFh

0 — **Flat Panel Text Automatic Horizontal Centering Enable:**
When a standard VGA text display mode is selected and this bit is:
- 0, automatic horizontal centering of text is disabled for all flat panels.
- 1, automatic horizontal centering of text is enabled for all flat panels.

12.119 CR82: Flat Panel Graphics Automatic Centering and Expansion Register

I/O Port Address: 3?5

Index: 82

Bit	Description	Reset State
7	Reserved	
6	Flat Panel Graphics Vertical Expansion [1]	0
5	Flat Panel Graphics Vertical Expansion [0]	0
4	Flat Panel Graphics Automatic Vertical Centering Enable	0
3	Reserved	
2	Flat Panel Graphics Horizontal Expansion [1]	0
1	Flat Panel Graphics Horizontal Expansion [0]	0
0	Flat Panel Graphics Automatic Horizontal Centering Enable	0

Bit **Description**

7 **Reserved**

6:5 **Flat Panel Graphics Vertical Expansion [1:0]:**
These bits enable vertical expansion of graphics as shown in the following table.

Flat Panel Graphics Vertical Expansion:

CR82 [6]	CR82 [5]	Original Number of Scanlines	Vertical Expansion Method
0	0	Native VGA	No vertical expansion of graphics
0	1	200	Pattern used is 0,0,1,1,2,2,2,3,3,4,4,5,5,5,6,6,7,7,7. Double- and triple-scan expands 200 scanlines to 475 scanlines by expanding every 8 scanlines to 19 scanlines.
		350	Pattern used is 0,1,2,2,3,4,5,5,6,7,7,8,9,a,a,b,c,d,d. Single- and double-scan expands 350 scanlines to 475 scanlines by expanding every 14 scanlines to 19 scanlines.
1	0	200	Pattern used is 0,0,0,1,1,1,2,2,2,3,3,3,4,4,4,5,5,5,6,6,6,7,7,7. Double- and triple-scan expands 200 scanlines to 600 scanlines by expanding every 1 scanline to 3 scanlines.
		350	Pattern used is 0,1,1. Double-scan of every odd scanline expands 350 scanlines to 525 scanlines by expanding every 2 scanlines to 3 scanlines.
		480	Pattern used is 0,1,2,3,3. Double-scan of every fifth scanline expands 480 scanlines to 600 scanlines by expanding every 4 scanlines to 5 scanlines.
1	1	Reserved	Reserved for future flat panel display modes.

NOTE: When an 800 x 600 flat panel has vertical expansion set for 600 scanlines (that is, bits CR82[6:5] are set to '10'), CR82[4] must be 0.

12.119 CR82: Flat Panel Graphics Automatic Centering and Expansion Register *(cont.)*

Bit | **Description**

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4 — **Flat Panel Graphics Automatic Vertical Centering Enable:**
When standard graphics display mode is selected and this bit is:
- 0, automatic vertical centering of graphics is disabled for all flat panels.
- 1, automatic vertical centering of graphics is enabled for all flat panels, up to and including panels of size 1024 x 768.

NOTES:

1) Even when a flat panel size is greater than 800 x 600, graphics can be expanded only up to 800 x 600.
2) When an 800 x 600 flat panel has vertical expansion set for 600 scanlines (that is, bits CR82[6:5] are set to '10'), bit CR82[4] must be 0.

---

3 — **Reserved**

2:1 — **Flat Panel Graphics Horizontal Expansion [1:0]:**
When a graphics display mode is selected, these bits enable horizontal expansion of graphics as shown in the following table:

NOTE: When an 800 x 600 flat panel has horizontal expansion set for 800 pixels (that is, bits CR82[2:1] are set to '01'), bit CR82[0] must be 0.

Flat Panel Graphics Horizontal Expansion:

CR82		Original Number of Character Clocks	Expanded Number of Character Clocks	Horizontal Expansion Method
[2]	[1]			
0	0	640	640	No horizontal expansion of graphics.
0	1	640	800	Every fourth pixel is replicated.
1	x	–	–	Reserved.

---

0 — **Flat Panel Graphics Automatic Horizontal Centering Enable:**
When a standard VGA graphics display mode is selected and this bit is:
- 0, automatic horizontal centering of graphics is disabled for all flat panels.
- 1, automatic horizontal centering of graphics is enabled for all flat panels, up to and including panels of size 1024 x 768.

NOTE: When an 800 x 600 flat panel has horizontal expansion set for 800 pixels (that is, bits CR82[2:1] are set to '01'), bit CR82[0] must be 0.

12.120 CR83: Flat Panel Type Register

I/O Port Address: 3?5

Index: 83

Bit	Description	Reset State
7	Flat Panel Shift Clock Select	0
6	Flat Panel Type Select [2]	0
5	Flat Panel Type Select [1]	0
4	Flat Panel Type Select [0]	0
3	Flat Panel Data Format Select [1]	0
2	Flat Panel Data Format Select [0]	0
1	Flat Panel Size Select [1]	0
0	Flat Panel Size Select [0]	0

Bit **Description**

7 **Flat Panel Shift Clock Select:**
This bit selects the shift clocks for TFT and STN flat panels. The clocking modes and affected clock pins are different for each flat panel type that is selected with bits CR83[6:4]. When the flat panel type selected is a:

- Dual-Scan STN color flat panel and this bit is:
  - — 0, the FPVDCLK pin supplies a 1-pixel/shift clock.
  - — 1, both the FPVDCLK and the FPDE pins are needed to supply a 2-pixel/shift clock.
- TFT color flat panel and this bit is:
  - — 0, the FPVDCLK pin supplies a 1-pixel/shift clock.
  - — 1, the FPVDCLK pin supplies a 2-pixel/shift clock.

6:4 **Flat Panel Type Select [2:0]:**
These 3 bits select the type of flat panel to be connected. The following table lists available choices:

CR83			Flat Panel Type Selected
[6]	[5]	[4]	
0	0	0	Dual-Scan STN Color Flat Panels
0	0	1	Reserved
0	1	0	TFT Color Flat Panels
0	1	1	Reserved
1	x	x	Reserved

12.120 CR83: Flat Panel Type Register *(cont.)*

Bit **Description**

3:2 **Flat Panel Data Format Select [1:0]:**
These 2 bits select the data format for TFT and dual-scan STN flat panels as shown in the following table. For detailed connection information for specific flat panel types, refer to the Cirrus Logic “Panel Interface Guide” in the *CL-GD7556 Application Book*.

CR83		TFT/Dual-Scan STN Panel Data Format
[3]	[2]	
0	0	9-bit (RGB 3-3-3) TFT / 8-bit Dual-Scan STN
0	1	12-bit (RGB 4-4-4) TFT / 16-bit Dual-Scan STN
1	0	18-bit (RGB 6-6-6) TFT / 24-bit Dual-Scan STN
1	1	24-bit (RGB 8-8-8) TFT

1:0 **Flat Panel Size Select [1:0]:**
These 2 bits select the size for flat panels as shown in the following table. For detailed connection information for specific flat panel types, refer to the Cirrus Logic “Panel Interface Guide” in the *CL-GD7556 Application Book*.

CR83		Flat Panel Size
[1]	[0]	
0	0	640 x 480 (VGA)
0	1	800 x 600 (SVGA)
1	0	1024 x 768 (XGA)
1	1	Reserved

12.121 CR84: Flat Panel FPVDCLK Format Select Register

I/O Port Address: 3?5

Index: 84

Bit	Description	Reset State
7	FPVDCLK Output Invert	0
6	FPVDCLK Source Selection Enable	0
5	FPVDCLK Free-Run Enable	0
4	Reserved	
3	FPVDCLK Delay Control [3]	0
2	FPVDCLK Delay Control [2]	0
1	FPVDCLK Delay Control [1]	0
0	FPVDCLK Delay Control [0]	0

Bit	Description
7	**FPVDCLK Output Invert:** This bit can be used with all flat panels. • When this bit is: — 0, flat panel data are latched on the 1-to-0 transition of the CL-GD7555 FPVDCLK output. — 1, flat panel data are latched on the 0-to-1 transition of the CL-GD7555 FPVDCLK output. • During Suspend mode, FPVDCLK is forced low, independent of this bit polarity.
6	**FPVDCLK Source Selection Enable:** This bit selects a VCLK value that is the source of the FPVDCLK signal for flat panels. When this bit is: • 0, the default VCLK is the value selected when External/General register bits MISC[3:2] = '10', independent of the actual bit levels of MISC[3:2]. • 1, the VCLK value can be selected from one of the four possible values the MISC[3:2] bits can provide.
5	**FPVDCLK Free-Run Enable:** This bit can be set to 1 for flat panels that require a free-running FPVDCLK. When this bit is: • 0, the CL-GD7556 FPVDCLK signal is gated with the CL-GD7556 FPDE signal, and FPVDCLK remains active only during display time (that is, when data is valid). • 1, *and* power is on to the flat panel, the FPVDCLK is free running (that is, it remains active at all times).
4	**Reserved**
3:0	**FPVDCLK Delay Control [3:0]:** This 4-bit field controls the shift clock delay relative to the pixel data, which can be from 0 to 15 ns in 1-ns increments. • A value of: — '0000' programs a 0-ns delay. — '0001' programs a 1-ns delay. — '1111' programs a 15-ns delay, and so forth.

12.122 CR85: Flat Panel LLCLK / HSYNC Control Register

I/O Port Address: 3?5

Index: 85

Bit	Description	Reset State
7	CRT Monitor HSYNC on LLCLK Select	0
6	Flat Panel LLCLK Output Invert	0
5	External TV-Out Support	0
4	Flat Panel LLCLK / HSYNC Width Control [4]	0
3	Flat Panel LLCLK / HSYNC Width Control [3]	0
2	Flat Panel LLCLK / HSYNC Width Control [2]	0
1	Flat Panel LLCLK / HSYNC Width Control [1]	0
0	Flat Panel LLCLK / HSYNC Width Control [0]	0

Bit **Description**

7 **CRT Monitor HSYNC on LLCLK Select:**
When this bit is:
- 0, LLCLK (pin 153) operates normally.
- 1, the CRT monitor HSYNC signal is supplied on the CL-GD7556 LLCLK pin.
  - — During flat panel power-down sequencing, the LLCLK output pin is forced low, independent of this bit level.
  - — The CRT monitor HSYNC signal is not controlled by DPMS.
  - — This bit is set to 1 primarily for TFT flat panels that have timing similar to a CRT monitor.

6 **Flat Panel LLCLK Output Invert:**
When this bit is:
- 0, the LLCLK pin operates normally.
- 1, the LLCLK output is inverted.

5 **External TV-Out Support:**
When this bit is set to:
- 0 *and* the flat panel enable bit is on (that is, Extension register CR80[0] = 1), the flat panel interface pads are enabled.
- 1, even when CR80[0] = 1, the flat panel interface pads are disabled. In this case, extended flat panel timing registers can be used to provide optimum timing signals to an external TV encoder through the CRT monitor interface. As a result, an external TV encoder can be supported without modifying standard VGA registers and without damaging the flat panel.

12.122 CR85: Flat Panel LLCLK / HSYNC Control Register *(cont.)*

Bit	Description
4:0	**Flat Panel LLCLK / HSYNC Width Control [4:0]:** • This field controls the width of LLCLK / HSYNC signals for flat panels. • The width of the signals can be increased in increments of 4 pixels clocks, according to the following table.

CR85					Resulting Widths of Flat Panel LLCLK / HSYNC Signals (In pixel clocks)
[4]	[3]	[2]	[1]	[0]	
0	0	0	0	0	Signal width is 4 pixel clocks.
0	0	0	0	1	Signal width is 8 pixel clocks.
0	0	0	1	0	Signal width is 12 pixel clocks.
0	0	0	1	1	Signal width is 16 pixel clocks.
0	0	1	0	0	Signal width is 20 pixel clocks.
0	0	1	0	1	Signal width is 24 pixel clocks.
					Selected Resulting Widths of Flat Panel LLCLK / HSYNC Signals
0	1	0	0	0	Signal width is 36 pixel clocks.
1	0	0	0	0	Signal width is 68 pixel clocks.
1	1	1	1	1	Signal width is 128 pixel clocks.

12.123 CR86: Flat Panel LFS / VSYNC Control Register

I/O Port Address: 3?5

Index: 86

Bit	Description	Reset State
7	CRT Monitor VSYNC on LFS Select	0
6	Flat Panel LFS Output Invert	0
5	Reserved	
4	Reserved	
3	Flat Panel VSYNC Width Control [3]	0
2	Flat Panel VSYNC Width Control [2]	0
1	Flat Panel VSYNC Width Control [1]	0
0	Flat Panel VSYNC Width Control [0]	0

Bit	Description
7	**CRT Monitor VSYNC on LFS Select:** When this bit is: • 0, LFS (pin 156) operates normally. • 1, the CRT monitor VSYNC signal is supplied on the CL-GD7556 LFS pin. — During flat panel power-down sequencing, the LFS output pin is forced low, independent of this bit level. — The CRT monitor VSYNC is not controlled by DPMS. — This bit is set to 1 primarily for TFT flat panels that have timing similar to a CRT monitor.
6	**Flat Panel LFS Output Invert:** When this bit is: • 0, the CL-GD7556 LFS pin operates normally. • 1, the CL-GD7556 LFS output is inverted.
5:4	**Reserved**
3:0	**Flat Panel VSYNC Width Control [3:0]:** • This field controls the width of VSYNC signals for TFT flat panels. (This field does not apply to dual-scan flat panels.) • The width of the signals can be increased in increments of 1 line clock, for a total of up to 16 line clocks. • A value of: — ‘0000’ programs a 1-line clock width. — ‘0001’ programs a 2-line clock width. — ‘1111’ programs a 16-line clock width, and so forth.

12.124 CR87: Graphics Input Resolution for Dithering Register

I/O Port Address: 3?5

Index: 87

Bit	Description	Reset State
7	Graphics Input Resolution Override Enable	0
6	Graphics (16-Color) Dither Enable	0
5	Graphics (256-Color) Dither Enable	0
4	Graphics (64K- or 16M-Color) Dither Enable	0
3	Graphics Input Resolution for Dithering [3]	0
2	Graphics Input Resolution for Dithering [2]	0
1	Graphics Input Resolution for Dithering [1]	0
0	Graphics Input Resolution for Dithering [0]	0

This register, which is used with both TFT and dual-scan STN flat panels, changes the CL-GD7556 default input resolution settings for graphics data sent to the dither block. (For input resolution for VW, refer to Extension register CR89.)

- When the VW is enabled, this override register affects only the surrounding graphics area.
- The VW display is controlled by independent input and output resolution control bits.
- This register supports a maximum of 6 × 6 dithering.

Bit **Description**

7 **Graphics Input Resolution Override Enable:**
When this bit is 0:

- The CL-GD7556 has default input resolution settings for dithering that maximizes the number of colors displayed on a flat panel.
- The settings from Extension register HDR (the Hidden DAC register) apply, including the default input resolution settings shown in the following table:

Dithering Matrix (Bits Per Primary R,G,B Color)	Color Depth	Default Input Resolution Settings
8 bits / R,G,B	24 colors	RGB 8-8-8 True-color mode
6 bits / R,G,B	18 colors	All VGA-compatible color modes
		All Extended-color modes (Go through the palette RAMDAC)
5 bits / R,G,B	15 colors	RGB 5-5-5 and RGB 5-6-5 True-color modes
3 bits R, 3 bits G, 2 bits B	8 colors	RGB 3-3-2 Color mode (Does not go through the palette RAMDAC)

(Continued)

12.124 CR87: Graphics Input Resolution for Dithering Register *(cont.)*

Bit	Description
7 *(cont.)*	**Graphics Input Resolution Override Enable** *(cont.)*: When this bit is 1: • The default input resolution settings are overridden, and new input resolution values are defined in CR87[3:0]. • When the default input resolution settings are not desired, the VGA BIOS can override them by programming any number between 0h and Fh. As a result, the CL-GD7556 can dither more or less than the default case. • As long as the dithering matrix is smaller than or equal to 6 × 6, the CL-GD7556 supports a combination of input and output resolutions.
6	**Graphics (16-Color) Dither Enable:** For 16-color graphics display modes, when Attribute Controller register bit AR10[0] is 1, *and* Graphics Controller register bit GR5[6] is 0, *and* this bit is: • 0, dithering is disabled. • 1, dithering is enabled.
5	**Graphics (256-Color) Dither Enable:** For 256-color graphics display modes, when Attribute Controller register bit AR10[0] is 1, *and* Graphics Controller register bit GR5[6] is 1, *and* this bit is: • 0, dithering is disabled. • 1, dithering is enabled.
4	**Graphics (64K- or 16M-Color) Dither Enable:** For either 64K- or 16M-color graphics display modes, when Attribute Controller register bit AR10[0] is 1, *and* Extension register bits SR7[3:1] are '001' or '01X', *and* this bit is: • 0, dithering is disabled. • 1, dithering is enabled.
3:0	**Graphics Input Resolution for Dithering [3:0]:** When CR87[7] is 1, the CR87[3:0] bits define the new input resolution values for data sent to the dithering block. These bits define the number of bits per color that the CL-GD7556 uses to control the dithering on a flat panel, independent of: • The output resolution • The dithering state (enabled vs. disabled) • The CL-GD7556 display mode (graphics vs. text)

CR87				Dithering Matrix for Flat Panel (Bits Per Primary R,G,B Color)	Color Depth
[3]	[2]	[1]	[0]		
0	0	1	1	3 bits/R,G,B	9 colors
0	1	0	0	4 bits/R,G,B	12 colors
0	1	0	1	5 bits/R,G,B	15 colors
0	1	1	0	6 bits/R,G,B	18 colors
0	1	1	1	7 bits/R,G,B	21 colors
1	0	0	0	8 bits/R,G,B	24 colors

12.124 CR87: Graphics Input Resolution for Dithering Register *(cont.)*

Bit	Description
3:0 *(cont.)*	**Graphics Input Resolution for Dithering [3:0]:**

Example 1:
When the given conditions are:
- Data comes from the 18-bit palette DAC CLUT as 6 bits for each PRGB (primary R,G,B) color.
- Colors displayed are 256.
- There are 8 bits/pixel.
- Flat panel is a 3-bits/PRGB color TFT.

Then:
- The default input resolution is 6 bits/PRGB color.
- The output resolution is 3 bits/PRGB color.
- The dithering engine dithers 3 bits (2 x 4) in order to get 2^6 = 64 equivalent colors per PRGB color for a total of 256K colors.

When 2×2 dithering is enough:
- The 6 bits/PRGB color default input resolution is overridden with one of 5 bits/PRGB color.
- Since 5 bits/PRGB color – 3 bits/PRGB color = 2 bits/PRGB color, this leads to a 2×2 dithering and the equivalent of 5 bits/PRGB (that is, 2^5 = 32K colors).

When 256K colors is not enough and a better effect is desired:
- More dithering is possible by programming an input resolution of 7 bits/PRGB.
- Since 7 bits/PRGB – 3 bits/PRGB = 4 bits/PRGB, this leads to a 4×4 dithering and the equivalent of 7 bits/PRGB (that is, 2^7 = 128 colors per PRGB, or 2M colors).

Example 2:
When the given conditions are:
- Colors displayed are 16.
- There are 8 bits/pixel.
- Flat panel is a color dual-scan STN.
- The output resolution is programmed as 4 bits/PRGB color (that is, 2^4 = 16).

Then:
- The default input resolution is 6 bits/PRGB color. (Combining 2^4 = 16 colors with 2^2 = 4 color dithering results in $2^4 \times 2^2 = 2^6$ = 6 bits/PRGB color.)
- By changing the output resolution to 3 bits/PRGB color, the CL-GD7556 generates 2^3 = 8 colors.
- When the input resolution is 6 bits/PRGB color, the CL-GD7556 does more dithering to get 6 bits/PRGB color.
- When the input resolution is 4 bits/PRGB color, the CL-GD7556 needs only 1×1 dithering to get a total of 16 equivalent colors per PRGB color.

12.125 CR88: Output Resolution for Dithering Register

I/O Port Address: 3?5

Index: 88

Bit	Description	Reset State
7	VW Output Resolution for Dithering [3]	0
6	VW Output Resolution for Dithering [2]	0
5	VW Output Resolution for Dithering [1]	0
4	VW Output Resolution for Dithering [0]	0
3	Graphics Output Resolution for Dithering [3]	0
2	Graphics Output Resolution for Dithering [2]	0
1	Graphics Output Resolution for Dithering [1]	0
0	Graphics Output Resolution for Dithering [0]	0

Bit **Description**

7:4 **VW Output Resolution for Dithering [3:0]:**
These bits define the output resolution value for dithering exactly in the same way as CR88[3:0], except they apply to the VW. The dithering is active even when the VW fills the entire display screen.

3:0 **Graphics Output Resolution for Dithering [3:0]:**
These bits define typical output resolution values for dithering various flat panels. The hex value programmed in these bits define the number of bits per PRGB (primary red, green, blue color) used by the CL-GD7556.

CR88				Output Resolution for Dithering Flat Panels:	
[7]	[6]	[5]	[4]	TFT Flat Panels (No Modulation of Frame Data Rate)	STN Flat Panels (Modulation Occurs for Frame Data Rate)
[3]	[2]	[1]	[0]		
0	0	0	1	Not applicable	2-shade STN flat panels: 1 bit/PRGB
0	0	1	0	Not applicable	4-shade STN flat panels: 2 bits/PRGB
0	0	1	1	3 bits/PRGB	8-shade STN flat panels: 3 bits/PRGB
0	1	0	0	4 bits/PRGB	16-shade STN flat panels: 4 bits/PRGB
0	1	1	0	6 bits/PRGB	Not applicable
1	0	0	0	8 bits/PRGB	Not applicable

NOTE: Programming values other than the ones specified in the above table can have unpredictable results.

CAUTION: This register must be programmed at start-up with the correct output resolution for the flat panel used (TFT or STN), since the system reset value of zero is not a valid selection.

12.126 CR89: VW Input Resolution for Dithering Register

I/O Port Address: 3?5

Index: 89

Bit	Description	Reset State
7	VW Input Resolution Override Enable	0
6	VW Dithering Enable	0
5	Reserved	
4	Reserved	
3	VW Input Resolution Override [3]	0
2	VW Input Resolution Override [2]	0
1	VW Input Resolution Override [1]	0
0	VW Input Resolution Override [0]	0

This register is used to change the CL-GD7556 default resolution settings for the video data sent to the dithering block, either for only the VW, or for when the VW fills the entire display screen.

Bit **Description**

7 **VW Input Resolution Override Enable:**
When this bit is:
- 0, the default input resolution for video data in the VW is 5 bits/PRGB, which supports RGB 5-5-5 and RGB 5-6-5 modes.
- 1, the default input resolution settings for the VW are overridden, and new values are defined in bits CR89[3:0] of this register.

6 **VW Dithering Enable:**
When this bit is:
- 0, VW dithering is disabled.
- 1, VW dithering is enabled.

5:4 **Reserved**

3:0 **VW Input Resolution Override [3:0]:**
When CR89[7] is 1, the CR89[3:0] bits define the new input-resolution values for data sent to the dithering block, so that the amount of colors in the VW can differ from the surrounding area.
- The hex value programmed can be any number between 1h and Fh.

CR89				Dithering Result for Flat Panel
[3]	[2]	[1]	[0]	
0	0	1	1	3 bits/PRGB (that is, RGB 3-3-2)
0	1	0	1	5 bits/PRGB (that is, RGB 5-5-5)
0	1	1	0	6 bits/PRGB (all palettize modes)
0	1	1	1	7 bits/PRGB
1	0	0	0	8 bits/PRGB. Includes: RGB 8-8-8 mode and YUV 4:2:2.
1	1	1	1	15 bits/PRGB

12.127 CR8A: Miscellaneous Status Register

I/O Port Address: 3?5

Index: 8A

Bit	Description	Access	Reset State
7	Suspend Mode Status	R	0
6	32-kHz Clock Status	R	0
5	Flat Panel Power-Sequence Active Status	R	0
4	Standby Mode Active Status	R	0
3	Reserved		
2	V-Port Interlaced Odd/Even Field Status	R	0
1	Horizontal Graphics Expansion Status	R	0
0	Vertical Graphics Expansion Status	R	0

NOTE: This register can be read only when extension registers are unlocked, using Extension register SR6.

Bit	Description
7	**Suspend Mode Status:** When this read-only bit reads a: • 0, the CL-GD7556 is not in the Suspend mode, which is the default. • 1, the CL-GD7556 is in the Suspend mode.
6	**32-kHz Clock Status:** When this read-only bit reads a: • 0, the 32-kHz clock is neither selected nor active. • 1, the 32-kHz clock is selected and it is supplying a signal.
5	**Flat Panel Power-Sequence Active Status:** When this read-only bit reads a: • 0, the flat panel is either all the way ‘on’ or ‘off’. • 1, the flat panel is in the middle of a power-up or power-down sequence.
4	**Standby Mode Active Status:** When this read-only bit reads a: • 0, the flat panel (and CRT monitor) are active and displaying data. • 1, the flat panel (and CRT monitor) are powered-down in the Standby mode.
3	**Reserved**
2	**V-Port Interlaced Odd/Even Field Status:** When this read-only bit reads a: • 0, even status applies to the current field marked by the VSI trailing edge. • 1, odd status applies to the current field marked by the VSI trailing edge.
1	**Horizontal Graphics Expansion Status:** When this read-only bit reads a: • 0, horizontal graphics expansion is not selected (that is, CR82[2:1] is ‘00’). • 1, horizontal graphics expansion is selected (that is, CR82[2:1] is non-zero).
0	**Vertical Graphics Expansion Status:** When this read-only bit reads a: • 0, vertical graphics expansion is not selected (that is, CR82[6:5] is ‘00’). • 1, vertical graphics expansion is selected (that is, CR82[6:5] is non-zero).

12.128 CR8B: Standby Timer Control and FPVCC/FPVEE Override Register

I/O Port Address: 3?5

Index: 8B

Bit	Description	Reset State
7	FPVEE Control Override Enable	0
6	FPVEE Output State	0
5	FPVCC Control Override	0
4	FPVCC Output State	0
3	Standby Mode Timer Control [3]	0
2	Standby Mode Timer Control [2]	0
1	Standby Mode Timer Control [1]	0
0	Standby Mode Timer Control [0]	0

Bit	Description
7	**FPVEE Control Override Enable**: Setting this bit to 1: • Overrides the normal output state of FPVEE (pin 123). • Enables CR8B[6] to directly control the output state of FPVEE.
6	**FPVEE Output State:** When CR8B[7] is 1 *and* this bit is: • 0, the output state of FPVEE is low. • 1, the output state of FPVEE is high.
5	**FPVCC Control Override**: Setting this bit to 1: • Overrides the normal output state of FPVCC (pin 125). • Enables CR8B[4] to directly control the output state of FPVCC. **CAUTION:** Setting this bit to 1 can cause excessive power consumption and damage the flat panel. It is *strongly recommended* that this bit be left in the 0 state.
4	**FPVCC Output State:** When CR8B[5] is 1 *and* this bit is: • 0, the output state of FPVCC is low. • 1, the output state of FPVCC is high.

12.128 CR8B: Standby Timer Control and FPVCC/FPVEE Override Register *(cont.)*

Bit	Description
3:0	**Standby Mode Timer Control [3:0]:** These bits program the value for the internal timer for the hardware-controlled Standby mode as shown in the table that follows. Whenever the timer reaches the programmed value, the following actions occur: • The CRT clock is stopped. • The DAC is disabled. • The flat panel power-down sequence is started. For a description of the flat panel power-down sequence, refer to Extension register bit CR80[0]. The timer for the Standby mode can be reset by the following: • Activity on ACTI (pin 63). For details, refer to CR8D[6]. • An access to standard VGA memory. For details, refer to CR8D[5].

CR8B Standby Timer Control Bits				Hex Code	Actual Seconds Programmed for Delay Time (seconds)	Approximate Corresponding Delay Time (minutes)
[3]	[2]	[1]	[0]			
0	0	0	0	0h	Disabled	Disabled
0	0	0	1	1h	32	0.5
0	1	0	1	5h	288	4.8
0	1	1	1	7h	416	6.9
1	0	1	0	Ah	608	10.1
1	1	1	1	Fh	928	15.5

12.129 CR8C: Programmable Power Sequencing Register

I/O Port Address: 3?5

Index: 8C

Bit	Description	Reset State
7	FPVEE-FPDECTL Delay [1]	0
6	FPVEE-FPDECTL Delay [0]	0
5	Data and Clock Controls-FPVEE Delay [1]	0
4	Data and Clock Controls-FPVEE Delay [0]	0
3	FPVCC-Data and Clock Controls Delay [1]	0
2	FPVCC-Data and Clock Controls Delay [0]	0
1	Power Enable-FPVCC/FPDECTL Delay [1]	0
0	Power Enable-FPVCC/FPDECTL Delay [0]	0

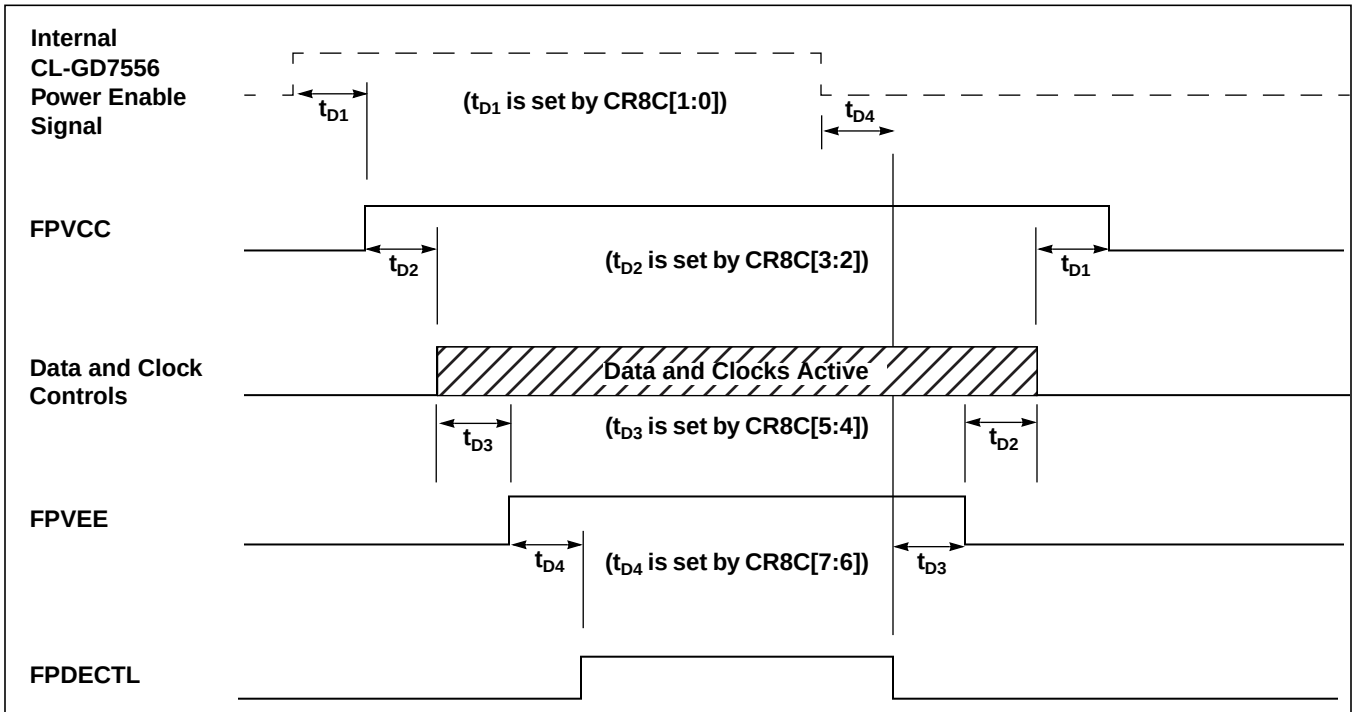
Bit	Description
7:6	**FPVEE-FPDECTL Delay [1:0]:** According to the table that follows, and as shown in the figure that follows, these 2 bits select the t_{D4} delays between FPVEE and FPDECTL.
5:4	**Data and Clock Controls-FPVEE Delay [1:0]:** According to the table that follows, and as shown in the figure that follows, these 2 bits select the t_{D3} delays between the CL-GD7556 data and clock control signals (that is, FPVDCLK, LFS, LLCLK, the Panel Data signals, and FPDE) and FPVEE.
3:2	**FPVCC-Data and Clock Controls Delay [1:0]:** According to the table that follows, and as shown in the figure that follows, these 2 bits select the t_{D2} delays between FPVCC and the CL-GD7556 data and clock control signals
1:0	**Power Enable-FPVCC/FPDECTL Delay [1:0]:** According to the table that follows, and as shown in the figure that follows, these 2 bits select the following delays: • CL-GD7556 (internal) Power Enable-FPVCC t_{D1} delay • CL-GD7556 (internal) Power Enable-FPDECTL t_{D1} delay *(Continued)*

12.129 CR8C: Programmable Power Sequencing Register *(cont.)*

Bit **Description**

Programmable Power-Sequence Delays

Bit Setting for Specified Delay	Amount of Delay Between Beginning of Specified Signals
CR8C[7:6] = t_{D4}	
CR8C[5:4] = t_{D3}	
CR8C[3:2] = t_{D2}	
CR8C[1:0] = t_{D1}	
'00'	32 ms (that is, 1024 periods of the CLK32K pin)
'01'	4 ms (that is, 128 periods of the CLK32K pin)
'10'	1 ms (that is, 32 periods of the CLK32K pin)
'11'	256 ms (that is, 4096 periods of the CLK32K pin)



NOTE: For each of the t_{D1}, t_{D2}, t_{D3}, and t_{D4} delays, the Cirrus Logic VGA BIOS default values are 32 ms.

Figure 12-4. Flat Panel Power-Up and Power-Down Delay Settings

12.130 CR8D: Miscellaneous Flat-Panel Control Register

I/O Port Address: 3?5

Index: 8D

Bit	Description	Reset State
7	Automatic Flat-Panel Power-Down Disable	0
6	Standby Mode Timer Reset by ACTI	0
5	Standby Mode Timer Reset by VGA Memory Access	0
4	Suspend Mode Clock Source	0
3	Suspend Mode SUSPI Pin Polarity	0
2	Suspend Mode SUSPI Pin Enable	0
1	Suspend Mode Memory Refresh [1]	0
0	Suspend Mode Memory Refresh [0]	0

Bit	Description
7	**Automatic Flat Panel Power-Down Disable:** When this bit is: • 0, all automatic flat panel power-down mechanisms are enabled. • 1, all automatic flat panel power-down mechanisms are disabled. This mode is intended only for testing and must not be set by the VGA BIOS.
6	**Standby Mode Timer Reset by ACTI:** When this bit is: • 0, activity on ACTI (pin 63) has no effect on the Standby mode timer. • 1, activity on ACTI resets the internal timer for the hardware-controlled Standby mode. When the CL-GD7556 is already in Standby mode, this activity restarts the CRT clock, enables the DAC, and starts the flat panel power-up sequence.
5	**Standby Mode Timer Reset by VGA Memory Access**: When this bit is: • 0, an access to standard VGA memory has no effect on the Standby mode timer. • 1, any valid access to standard VGA memory resets the internal timer for the hardware-controlled Standby mode. When the CL-GD7556 is already in Standby mode, as a result of this access to standard VGA memory, the following actions occur: — The CRT clock is restarted. — The DAC is enabled. — The flat panel power-up sequence is started. For a description of the flat panel power-up sequence, refer to Extension register bit CR80[0].
4	**Suspend Mode Clock Source:** This bit selects the clock source used during Suspend mode. When this bit is: • 0, a 32-kHz clock must be connected to CLK32K / SUSPST# (pin 57). As a result, when the CL-GD7555 is in Suspend mode, the OSC input is disabled. • 1, during the Suspend mode a 32-kHz clock is derived by dividing the OSC input pin by 432. As a result, when the CL-GD7555 is in Suspend mode, the CLK32K / SUSPST# pin is configured for SUSPST# (that is, the active-low output, Suspend Mode Status).

12.130 CR8D: Miscellaneous Flat Panel Control Register *(cont.)*

Bit | **Description**

3 — **Suspend Mode SUSPI Pin Polarity:**
When this bit is:
- 0, the polarity for SUSPI (pin 56) is active high.
- 1, the polarity for SUSPI is active low (that is, SUSPI#).

2 — **Suspend Mode SUSPI Pin Enable:**
This bit enables hardware control for the Suspend mode. When this bit is:
- 0, activity on SUSPI (pin 56) has no effect.
- 1, either of the following transitions can start the Suspend mode power-down sequence:
  - — A low-to-high transition on the SUSPI pin (when CR8D[3] is 0)
  - — A high-to-low transition on the SUSPI pin (when CR8D[3] is 1)

1:0 — **Suspend Mode Memory Refresh Select [1:0]:**
The programming of these 2 bits controls the type of refresh applied to the display memory during Suspend mode as follows.

CR8D		Display Memory Refresh Type
[1]	[0]	
0	0	Auto-refresh (that is, CAS# before RAS#). Refresh cycle is 8 ms.
0	1	Auto-refresh. Refresh cycle is 64 ms.
1	0	Self-refresh. CAS# and RAS# are driven low.
1	1	No refresh. All clock inputs are disabled, and display memory outputs are high-impedance.

12.131 CR8E: Miscellaneous Hardware Control Register

I/O Port Address: 3?5

Index: 8E

Bit	Description	Reset State
7	Shader Vertical-Crosstalk Reduction Enable	0
6	Shader Horizontal-Crosstalk Reduction Enable	0
5	Registers for Flat-Panel Vertical Timing	0
4	Invert VW-FIFO Increment Pointer	0
3	GR5, GR1, and GR0 Direct Update	0
2	Graphics CLUT RAM Bypass for Direct Color Modes	0
1	Half-Frame Accelerator Frame Data Select [1]	0
0	Half-Frame Accelerator Frame Data Select [0]	0

Bit	Description
7	**Shader Vertical-Crosstalk Reduction Enable:** When this bit is 1, vertical crosstalk is reduced for STN flat panels only for test purposes.
6	**Shader Horizontal-Crosstalk Reduction Enable:** When this bit is 1, horizontal crosstalk is reduced for STN flat panels only for test purposes.
5	**Registers for Flat-Panel Vertical Timing:** When this bit is: • 0, vertical timing for flat panels is derived from timing registers for flat panels. • 1, vertical timing for flat panels is derived from timing registers for CRT monitors.
4	**Invert VW-FIFO Increment Pointer: (Factory testing bit)** When this bit is 1, the active level of the VW-FIFO increment pointer is inverted.
3	**GR5, GR1, and GR0 Direct Update:** When this bit is: • 0, Graphics Controller registers GR5, GR1, and GR0 are updated as soon as the host CPU I/O cycle is complete. • 1, Graphics Controller registers GR5, GR1, and GR0 are updated after the host CPU write buffer is emptied. (For more information, refer to Section 3.3.2.)
2	**Graphics CLUT RAM Bypass for Direct Color Modes:** In Direct Color modes, this bit is used to bypass graphics CLUT RAM. When this bit is: • 0, the pixel data go through the graphics CLUT RAM, and then either to the DAC or to the flat-panel interface logic circuitry. • 1, the pixel data bypass the graphics CLUT RAM. Instead, the pixel data go directly either to the DAC or to the flat-panel interface logic circuitry.

12.131 CR8E: Miscellaneous Hardware Control Register *(cont.)*

Bit	Description
1:0	**Half-Frame Accelerator Frame Data Select [1:0]:** These two bits are used to control selection of frame data only for test purposes.

CR8E		Frame Data Select
[1]	[0]	
0	0	Normal operation.
0	1	Select data from current frame.
1	0	Select data from next frame.
1	1	Select internal test data.

12.132 CR8F: Request Generation Disable Register

I/O Port Address: 3?5

Index: 8F

Bit	Description	Reset State
7	Dithering Pipeline Stage Insert	0
6	V-Port Request Generation Disable	0
5	VW Request Generation Disable	0
4	DRAM Refresh Request Generation Disable	0
3	CRT Monitor Cycle Request Generation Disable	0
2	Pixel Data Forced to Zero during Blanking	0
1	Internal/External IREF Select	0
0	Half-Frame Accelerator Frame Data Select Request Generation Disable	0

Bit	Description
7	**Dithering Pipeline Stage Insert:** When this bit is 1, an extra pipeline stage is inserted for the dithering engine. This bit is only for test purposes.
6	**V-Port Request Generation Disable:** When a request is generated to enable the CL-GD7556 V-Port interface and this bit is 1, the request is disabled.
5	**VW Request Generation Disable:** When a request is generated to enable a VW on a display screen and this bit is 1, the request is disabled.
4	**DRAM Refresh Request Generation Disable:** When a request is generated to refresh the DRAM and this bit is 1, the request is disabled.
3	**CRT Monitor Cycle Request Generation Disable:** When a CRT monitor cycle request is generated to the memory arbiter and this bit is 1, the request is disabled.
2	**Pixel Data Forced to Zero during Blanking:** When this bit is 1, pixel data are forced to zero during a blanking period.
1	**Internal/External IREF Select:** When this bit is: • 0 (the default), the IREF circuit that is selected for the DAC is internal to the CL-GD7556. • 1, the IREF circuit that is selected for the DAC is external to the CL-GD7556. This bit setting is only for test purposes.
0	**Half-Frame Accelerator Frame Data Select Request Generation Disable:** When a request is generated to select frame data and this bit is 1, the request is disabled.

12.133 CR90: Dithering Counter Offset Register

I/O Port Address: 3?5

Index: 90

Bit	Description	Reset State
7	TFT Flat Panel Display Enable Delay [1]	0
6	TFT Flat Panel Display Enable Delay [0]	0
5	Dithering Vertical Counter Offset [2]	0
4	Dithering Vertical Counter Offset [1]	0
3	Dithering Vertical Counter Offset [0]	0
2	Dithering Horizontal Counter Offset [2]	0
1	Dithering Horizontal Counter Offset [1]	0
0	Dithering Horizontal Counter Offset [0]	0

Bit **Description**

7:6 **TFT Flat Panel Display Enable Delay [1:0]:**
This 2-bit field defines the number of flat panel shift clocks that can be used to delay the display enable for a TFT flat panel.

CR90		Line-Buffer Clock Delay
[7]	[6]	
0	0	No Delay
0	1	1 Shift-clock Delay
1	0	2 Shift-clock Delay
1	1	3 Shift-clock Delay

5:3 **Dithering Vertical Counter Offset [2:0]:**
This 3-bit field specifies the vertical offset for the dithering matrix. It is used to set up the most effective dithering start position for each flat panel size. Once this field is set up by the VGA BIOS, it must not be changed.

2:0 **Dithering Horizontal Counter Offset [2:0]:**
This 3-bit field specifies the horizontal offset for the dithering matrix. It is used to set up the most effective dithering start position for each flat panel size. Once this field is set up by the VGA BIOS, it must not be changed.

12.134 CR91: Shading Map Offset Register

I/O Port Address: 3?5

Index: 91

Bit	Description	Reset State
7	Blue Shading Map Offset [3]	0
6	Blue Shading Map Offset [2]	0
5	Blue Shading Map Offset [1]	0
4	Blue Shading Map Offset [0]	0
3	Green Shading Map Offset [3]	0
2	Green Shading Map Offset [2]	0
1	Green Shading Map Offset [1]	0
0	Green Shading Map Offset [0]	0

This register contains two 4-bit fields that are used only with STN flat panels to improve the display screen appearance and to minimize crosstalk.

Bit **Description**

7:4 **Blue Shading Map Offset [3:0]:**
This 4-bit field is used only with STN flat panels. When an STN flat panel is selected (that is, CR83[6:4] is '000') *and* frame data rate modulation occurs (that is, either CR88[7:4] or CR88[3:0] are set to anything except '0110' or '1000'), *and* these bits are programmed to:

- '0000', each primary RGB shade is derived from the same shading map. As a result, all RGB shades have the same value. Consequently, crosstalk can occur on some panels.
- Anything except '0000', this field uses the following formula to create an inequality between the values used for primary RGB shading:

  B value = G (Used as a reference value) + CR91[7:4]

For the particular type of flat panel that is being used, the appearance of the display screen image can be improved and crosstalk can be minimized by specifying an appropriate number of frame delays after the green shading map is used. For example:

- '0001' programs 1 frame delay from the green shading map.
- '0010' programs 2 frame delays from the green shading map.
- '0111' programs 7 frame delays, and so forth.

To further improve the display screen image and crosstalk, these bits can be used in combination with CR91[3:0].

3:0 **Green Shading Map Offset [3:0]:**
This 4-bit field is used in the same way that bits CR91[7:4] are used, except that when these bits are programmed to anything except '0000', this field:

- Uses the formula:

  G value = R (Used as a reference value) + CR91[3:0]

- Can be used to specify an appropriate number of frame delays after the red shading map is used.
- To further improve the display screen image and crosstalk, these bits can be used in combination with CR91[7:4].

12.135 CRA0: CRT Horizontal Total 8-Dot Character Clock (High Resolution) Register

I/O Port Address: 3?5

Index: A0

Bit	Description	Reset State
7	CRT Horizontal-Total 8-Dot Character Clock (High Resolution) [7]	0
6	CRT Horizontal-Total 8-Dot Character Clock (High Resolution) [6]	0
5	CRT Horizontal-Total 8-Dot Character Clock (High Resolution) [5]	0
4	CRT Horizontal-Total 8-Dot Character Clock (High Resolution) [4]	0
3	CRT Horizontal-Total 8-Dot Character Clock (High Resolution) [3]	0
2	CRT Horizontal-Total 8-Dot Character Clock (High Resolution) [2]	0
1	CRT Horizontal-Total 8-Dot Character Clock (High Resolution) [1]	0
0	CRT Horizontal-Total 8-Dot Character Clock (High Resolution) [0]	0

This register specifies the total number of 8-dot character clocks per horizontal period when a flat panel is enabled and is in a high-resolution display mode.

Bit **Description**

7:0 **CRT Horizontal-Total 8-Dot Character Clock (High Resolution) [7:0]:**
When this register is enabled, it specifies the total number of 8-dot character clocks per horizontal period when a flat panel is enabled and is in a high-resolution display mode.

- The value in this register equals the total number of characters, minus five. (For example, when the total number of characters is 80, then 80 - 5 = 75.)
- This register performs the same function as CRT Controller register bits CR0[7:0] in CRT-only mode.
- This register is enabled when all of the following conditions occur.

Bit Setting	Condition
Sequencer register SR1[0] = 1	8-dot character clock is selected.
Sequencer register SR1[3] = 0	VCLK is set for high-resolution display modes.
Extension register CR80[0] = 1	A flat panel interface is enabled.
Extension register CR81[2:1] = ‘00’	Horizontal expansion of text is disabled.
Extension register CR82[2:1] = ‘00’	Horizontal expansion of graphics is disabled.

12.136 CRA1: CRT HSync-Start 8-Dot Character Clock (High Resolution) Register

I/O Port Address: 3?5

Index: A1

Bit	Description	Reset State
7	CRT HSync-Start 8-Dot Character Clock (High Resolution) [7]	0
6	CRT HSync-Start 8-Dot Character Clock (High Resolution) [6]	0
5	CRT HSync-Start 8-Dot Character Clock (High Resolution) [5]	0
4	CRT HSync-Start 8-Dot Character Clock (High Resolution) [4]	0
3	CRT HSync-Start 8-Dot Character Clock (High Resolution) [3]	0
2	CRT HSync-Start 8-Dot Character Clock (High Resolution) [2]	0
1	CRT HSync-Start 8-Dot Character Clock (High Resolution) [1]	0
0	CRT HSync-Start 8-Dot Character Clock (High Resolution) [0]	0

This register specifies when the Horizontal Sync becomes active when a flat panel is enabled and is in a high-resolution display mode.

Bit **Description**

7:0 **CRT Horizontal-Sync-Start 8-Dot Character Clock (High Resolution) [7:0]:** When this register is enabled, it contains the 8-dot character count that specifies when the Horizontal Sync becomes active when a flat panel is enabled and is in a high-resolution display mode.

- Adjusting the value in this field moves the display image horizontally on the display screen.
- This register performs the same function as CRT Controller register bits CR4[7:0].
- The value in this register is derived from the following formula:

$$\text{HSync Start} = \frac{\text{Character Counter} + (\text{Flat Panel Size} \div 8)}{2}$$

- This register is enabled when all of the following conditions occur:

Bit Setting	Condition
Sequencer register SR1[0] = 1	8-dot character clock is selected.
Sequencer register SR1[3] = 0	VCLK is set for high-resolution display modes.
Extension register CR80[0] = 1	A flat panel interface is enabled.
Extension register CR81[2:1] = ‘00’	Horizontal expansion of text is disabled.
Extension register CR82[2:1] = ‘00’	Horizontal expansion of graphics is disabled.

12.137 CRA2: CRT Horizontal Total 8-Dot Character Clock (Low Resolution) Register

I/O Port Address: 3?5

Index: A2

Bit	Description	Reset State
7	CRT Horizontal-Total 8-Dot Character Clock (Low Resolution) [7]	0
6	CRT Horizontal-Total 8-Dot Character Clock (Low Resolution) [6]	0
5	CRT Horizontal-Total 8-Dot Character Clock (Low Resolution) [5]	0
4	CRT Horizontal-Total 8-Dot Character Clock (Low Resolution) [4]	0
3	CRT Horizontal-Total 8-Dot Character Clock (Low Resolution) [3]	0
2	CRT Horizontal-Total 8-Dot Character Clock (Low Resolution) [2]	0
1	CRT Horizontal-Total 8-Dot Character Clock (Low Resolution) [1]	0
0	CRT Horizontal-Total 8-Dot Character Clock (Low Resolution) [0]	0

This register specifies the total number of 8-dot character clocks per horizontal period when a flat panel is enabled and is in a low-resolution display mode.

Bit **Description**

7:0 **CRT Horizontal-Total 8-Dot Character Clock (Low Resolution) [7:0]:**
When this register is enabled, it specifies the total number of 8-dot character clocks per horizontal period when a flat panel is enabled and is in a low-resolution display mode.

- The value in this register equals the total number of characters, minus five. (For example, if the total number of characters is 80, then 80 - 5 = 75.)
- This register performs the same function as CRT Controller register bits CR0[7:0] in CRT-only mode.
- This register is enabled when all of the following conditions occur:

Bit Setting	Condition
Sequencer register SR1[0] = 1	8-dot character clock is selected.
Sequencer register SR1[3] = 1	VCLK is set for low-resolution display modes.
Extension register CR80[0] = 1	A flat panel interface is enabled.
Extension register CR81[2:1] = ‘00’	Horizontal expansion of text is disabled.
Extension register CR82[2:1] = ‘00’	Horizontal expansion of graphics is disabled.

12.138 CRA3: CRT HSync-Start 8-Dot Character Clock (Low Resolution) Register

I/O Port Address: 3?5

Index: A3

Bit	Description	Reset State
7	CRT HSync-Start 8-Dot Character Clock (Low Resolution) [7]	0
6	CRT HSync-Start 8-Dot Character Clock (Low Resolution) [6]	0
5	CRT HSync-Start 8-Dot Character Clock (Low Resolution) [5]	0
4	CRT HSync-Start 8-Dot Character Clock (Low Resolution) [4]	0
3	CRT HSync-Start 8-Dot Character Clock (Low Resolution) [3]	0
2	CRT HSync-Start 8-Dot Character Clock (Low Resolution) [2]	0
1	CRT HSync-Start 8-Dot Character Clock (Low Resolution) [1]	0
0	CRT HSync-Start 8-Dot Character Clock (Low Resolution) [0]	0

This register specifies when the Horizontal Sync becomes active when a flat panel is enabled and is in a low-resolution display mode.

Bit **Description**

7:0 **CRT Horizontal-Sync Start 8-Dot Character Clock (Low Resolution) [7:0]:** When this register is enabled, it contains the 8-dot character count that specifies when the Horizontal Sync becomes active when a flat panel is enabled and is in a low-resolution display mode.

- Adjusting the value in this field moves the display image horizontally on the display screen.
- This register performs the same function as CRT Controller register bits CR4[7:0].
- The value in this register is derived from the following formula:

$$\text{HSync Start} = \frac{\text{Character Counter} + (\text{Flat Panel Size} \div 16)}{2}$$

- This register is enabled when all of the following conditions occur:

Bit Setting	Condition
Sequencer register SR1[0] = 1	8-dot character clock is selected.
Sequencer register SR1[3] = 1	VCLK is set for low-resolution display modes.
Extension register CR80[0] = 1	A flat panel interface is enabled.
Extension register CR81[2:1] = ‘00’	Horizontal expansion of text is disabled.
Extension register CR82[2:1] = ‘00’	Horizontal expansion of graphics is disabled.

12.139 CRA4: CRT Horizontal-Total 9-Dot Character Clock (High Resolution) Register

I/O Port Address: 3?5

Index: A4

Bit	Description	Reset State
7	CRT Horizontal-Total 9-Dot Character Clock (High Resolution) [7]	0
6	CRT Horizontal-Total 9-Dot Character Clock (High Resolution) [6]	0
5	CRT Horizontal-Total 9-Dot Character Clock (High Resolution) [5]	0
4	CRT Horizontal-Total 9-Dot Character Clock (High Resolution) [4]	0
3	CRT Horizontal-Total 9-Dot Character Clock (High Resolution) [3]	0
2	CRT Horizontal-Total 9-Dot Character Clock (High Resolution) [2]	0
1	CRT Horizontal-Total 9-Dot Character Clock (High Resolution) [1]	0
0	CRT Horizontal-Total 9-Dot Character Clock (High Resolution) [0]	0

This register specifies the total number of 9-dot character clocks per horizontal period when a flat panel is enabled and is in a high-resolution display mode.

Bit **Description**

7:0 **CRT Horizontal-Total 9-Dot Character Clock (High Resolution) [7:0]:**
When this register is enabled, it specifies the total number of 9-dot character clocks per horizontal period when a flat panel is enabled and is in a high-resolution display mode.

- The value in this register equals the total number of characters, minus five. (For example, if the total number of characters is 80, then 80 - 5 = 75.)
- This register performs the same function as CRT Controller register bits CR0[7:0] in CRT-only mode.
- This register is enabled when all of the following conditions occur:

Bit Setting	Condition
Sequencer register SR1[0] = 0	9-dot character clock is selected.
Sequencer register SR1[3] = 0	VCLK is set for high-resolution display modes.
Extension register CR80[0] = 1	A flat panel interface is enabled.
Extension register CR81[2:1] = ‘00’	Horizontal expansion of text is disabled.
Extension register CR82[2:1] = ‘00’	Horizontal expansion of graphics is disabled.

12.140 CRA5: CRT HSync-Start 9-Dot Character Clock (High Resolution) Register

I/O Port Address: 3?5

Index: A5

Bit	Description	Reset State
7	CRT HSync-Start 9-Dot Character Clock (High Resolution) [7]	0
6	CRT HSync-Start 9-Dot Character Clock (High Resolution) [6]	0
5	CRT HSync-Start 9-Dot Character Clock (High Resolution) [5]	0
4	CRT HSync-Start 9-Dot Character Clock (High Resolution) [4]	0
3	CRT HSync-Start 9-Dot Character Clock (High Resolution) [3]	0
2	CRT HSync-Start 9-Dot Character Clock (High Resolution) [2]	0
1	CRT HSync-Start 9-Dot Character Clock (High Resolution) [1]	0
0	CRT HSync-Start 9-Dot Character Clock (High Resolution) [0]	0

This register specifies when the Horizontal Sync becomes active when a flat panel is enabled and is in a high-resolution display mode.

Bit **Description**

7:0 **CRT Horizontal-Sync-Start 9-Dot Character Clock (High Resolution) [7:0]:** When this register is enabled, it contains the 9-dot character count that specifies when the Horizontal Sync becomes active when a flat panel is enabled and is in a high-resolution display mode.

- Adjusting the value in this field moves the display image horizontally on the display screen.
- This register performs the same function as CRT Controller register bits CR4[7:0].
- The value in this register is derived from the following formula:

$$\text{HSync Start} = \frac{\text{Character Counter} + (\text{Flat Panel Size} \div 9)}{2}$$

- This register is enabled when all of the following conditions occur:

Bit Setting	Condition
Sequencer register SR1[0] = 0	9-dot character clock is selected.
Sequencer register SR1[3] = 0	VCLK is set for high-resolution display modes.
Extension register CR80[0] = 1	A flat panel interface is enabled.
Extension register CR81[2:1] = ‘00’	Horizontal expansion of text is disabled.
Extension register CR82[2:1] = ‘00’	Horizontal expansion of graphics is disabled.

12.141 CRA6: CRT Horizontal-Total 9-Dot Character Clock (Low Resolution) Register

I/O Port Address: 3?5

Index: A6

Bit	Description	Reset State
7	CRT Horizontal-Total 9-Dot Character Clock (Low Resolution) [7]	0
6	CRT Horizontal-Total 9-Dot Character Clock (Low Resolution) [6]	0
5	CRT Horizontal-Total 9-Dot Character Clock (Low Resolution) [5]	0
4	CRT Horizontal-Total 9-Dot Character Clock (Low Resolution) [4]	0
3	CRT Horizontal-Total 9-Dot Character Clock (Low Resolution) [3]	0
2	CRT Horizontal-Total 9-Dot Character Clock (Low Resolution) [2]	0
1	CRT Horizontal-Total 9-Dot Character Clock (Low Resolution) [1]	0
0	CRT Horizontal-Total 9-Dot Character Clock (Low Resolution) [0]	0

This register specifies the total number of 9-dot character clocks per horizontal period when a flat panel is enabled and is in a low-resolution display mode.

Bit **Description**

7:0 **CRT Horizontal-Total 9-Dot Character Clock (Low Resolution) [7:0]:**
When this register is enabled, it specifies the total number of 9-dot character clocks per horizontal period when a flat panel is enabled and is in a low-resolution display mode.

- The value in this register equals the total number of characters, minus five. (For example, if the total number of characters is 80, then 80 - 5 = 75.)
- This register performs the same function as CRT Controller register bits CR0[7:0] in CRT-only mode.
- This register is enabled when all of the following conditions occur:

Bit Setting	Condition
Sequencer register SR1[0] = 0	9-dot character clock is selected.
Sequencer register SR1[3] = 1	VCLK is set for low-resolution display modes.
Extension register CR80[0] = 1	A flat panel interface is enabled.
Extension register CR81[2:1] = ‘00’	Horizontal expansion of text is disabled.
Extension register CR82[2:1] = ‘00’	Horizontal expansion of graphics is disabled.

12.142 CRA7: CRT HSync-Start 9-Dot Character Clock (Low Resolution) Register

I/O Port Address: 3?5

Index: A7

Bit	Description	Reset State
7	CRT HSync-Start 9-Dot Character Clock (Low Resolution) [7]	0
6	CRT HSync-Start 9-Dot Character Clock (Low Resolution) [6]	0
5	CRT HSync-Start 9-Dot Character Clock (Low Resolution) [5]	0
4	CRT HSync-Start 9-Dot Character Clock (Low Resolution) [4]	0
3	CRT HSync-Start 9-Dot Character Clock (Low Resolution) [3]	0
2	CRT HSync-Start 9-Dot Character Clock (Low Resolution) [2]	0
1	CRT HSync-Start 9-Dot Character Clock (Low Resolution) [1]	0
0	CRT HSync-Start 9-Dot Character Clock (Low Resolution) [0]	0

This register specifies when the Horizontal Sync becomes active when a flat panel is enabled and is in a low-resolution display mode.

Bit **Description**

7:0 **CRT Horizontal-Sync-Start 9-Dot Character Clock (Low Resolution) [7:0]:** When this register is enabled, it contains the 9-dot character count that specifies when the Horizontal Sync becomes active when a flat panel is enabled and is in a low-resolution display mode.

- Adjusting the value in this field moves the display image horizontally on the display screen.
- This register performs the same function as CRT Controller register bits CR4[7:0].
- The value in this register is derived from the following formula:

$$\text{HSync Start} = \frac{\text{Character Counter} + (\text{Flat Panel Size} \div 18)}{2}$$

- This register is enabled when all of the following conditions occur:

Bit Setting	Condition
Sequencer register SR1[0] = 0	9-dot character clock is selected.
Sequencer register SR1[3] = 1	VCLK is set for low-resolution display modes.
Extension register CR80[0] = 1	A flat panel interface is enabled.
Extension register CR81[2:1] = ‘00’	Horizontal expansion of text is disabled.
Extension register CR82[2:1] = ‘00’	Horizontal expansion of graphics is disabled.

12.143 CRA8: CRT Horizontal Total for Expansion (High Resolution) Register

I/O Port Address: 3?5

Index: A8

Bit	Description	Reset State
7	CRT Horizontal Total for Expansion (High Resolution) [7]	0
6	CRT Horizontal Total for Expansion (High Resolution) [6]	0
5	CRT Horizontal Total for Expansion (High Resolution) [5]	0
4	CRT Horizontal Total for Expansion (High Resolution) [4]	0
3	CRT Horizontal Total for Expansion (High Resolution) [3]	0
2	CRT Horizontal Total for Expansion (High Resolution) [2]	0
1	CRT Horizontal Total for Expansion (High Resolution) [1]	0
0	CRT Horizontal Total for Expansion (High Resolution) [0]	0

This register specifies the total number of 10-dot character clocks per horizontal period when a flat panel is enabled and is in a high-resolution display mode.

Bit **Description**

7:0 **CRT Horizontal Total for Expansion (High Resolution) [7:0]:**
When this register is enabled, it specifies the total number of 10-dot character clocks per horizontal period when a flat panel is enabled and is in a high-resolution display mode.

- The value in this register equals the total number of characters, minus five. (For example, if the total number of characters is 80, then 80 - 5 = 75.)
- This register performs the same function as CRT Controller register bits CR0[7:0] in CRT-only mode.
- This register is enabled when all of the following conditions occur:

Bit Setting	Condition
Sequencer register SR1[0] = X	Either an 8- or 9-dot character clock is selected.
Sequencer register SR1[3] = 0	VCLK is set for high-resolution display modes.
CRT Controller register CR1[7:0] < 6Fh	Horizontal Display End standard VGA operation.
Extension register CR80[0] = 1	A flat panel interface is enabled.
Extension register CR81[2:1] = '1X'. When CR81[2:1] = • '10', 10-dot character clocks are selected and enabled. • '11', 12-dot character clocks are selected, but this setting is not supported.	Horizontal expansion of text is enabled.
Extension register CR82[2:1] = '01'	Horizontal expansion of graphics is enabled.

12.144 CRA9: CRT HSync Start for Expansion (High Resolution) Register

I/O Port Address: 3?5

Index: A9

Bit	Description	Reset State
7	CRT HSync Start for Expansion (High Resolution) [7]	0
6	CRT HSync Start for Expansion (High Resolution) [6]	0
5	CRT HSync Start for Expansion (High Resolution) [5]	0
4	CRT HSync Start for Expansion (High Resolution) [4]	0
3	CRT HSync Start for Expansion (High Resolution) [3]	0
2	CRT HSync Start for Expansion (High Resolution) [2]	0
1	CRT HSync Start for Expansion (High Resolution) [1]	0
0	CRT HSync Start for Expansion (High Resolution) [0]	0

This register specifies when the Horizontal Sync becomes active when a flat panel is enabled and is in a high-resolution display mode.

Bit **Description**

7:0 **CRT Horizontal-Sync Start for Expansion (High Resolution) [7:0]:**
When this register is enabled, it contains the 10-dot character count that specifies when the Horizontal Sync becomes active when a flat panel is enabled and is in a high-resolution display mode.

- Adjusting the value in this field moves the display image horizontally on the display screen.
- This register performs the same function as CRT Controller register bits CR4[7:0] in CRT-only mode.
- The value in this register is derived from the following formula:

$$\text{HSync Start} = \frac{\text{Character Counter} + (\text{Flat Panel Size} \div 10)}{2}$$

- This register is enabled when all of the following conditions occur:

Bit Setting	Condition
Sequencer register SR1[0] = X	Either an 8- or 9-dot character clock is selected.
Sequencer register SR1[3] = 0	VCLK is set for high-resolution display modes.
CRT Controller register CR1[7:0] < 6Fh	Horizontal Display End standard VGA operation.
Extension register CR80[0] = 1	A flat panel interface is enabled.
Extension register CR81[2:1] = '1X'. When CR81[2:1] = • '10', 10-dot character clocks are selected and enabled. • '11', 12-dot character clocks are selected, but this setting is not supported.	Horizontal expansion of text is enabled.
Extension register CR82[2:1] = '01'	Horizontal expansion of graphics is enabled.

12.145 CRAA: CRT Horizontal Total for Expansion (Low Resolution) Register

I/O Port Address: 3?5

Index: AA

Bit	Description	Reset State
7	CRT Horizontal Total for Expansion (Low Resolution) [7]	0
6	CRT Horizontal Total for Expansion (Low Resolution) [6]	0
5	CRT Horizontal Total for Expansion (Low Resolution) [5]	0
4	CRT Horizontal Total for Expansion (Low Resolution) [4]	0
3	CRT Horizontal Total for Expansion (Low Resolution) [3]	0
2	CRT Horizontal Total for Expansion (Low Resolution) [2]	0
1	CRT Horizontal Total for Expansion (Low Resolution) [1]	0
0	CRT Horizontal Total for Expansion (Low Resolution) [0]	0

This register specifies the total number of 10-dot character clocks per horizontal period when a flat panel is enabled and is in a low-resolution display mode.

Bit **Description**

7:0 **CRT Horizontal Total for Expansion (Low Resolution) [7:0]:**
When this register is enabled, it specifies the total number of 10-dot character clocks per horizontal period when a flat panel is enabled and is in a low-resolution display mode.

- The value in this register equals the total number of characters, minus five. (For example, if the total number of characters is 80, then 80 - 5 = 75.)
- This register performs the same function as CRT Controller register bits CR0[7:0] in CRT-only mode.
- This register is enabled when all of the following conditions occur:

Bit Setting	Condition
Sequencer register SR1[0] = X	Either an 8- or 9-dot character clock is selected.
Sequencer register SR1[3] = 1	VCLK is set for low-resolution display modes.
CRT Controller register CR1[7:0] < 6Fh	Horizontal Display End standard VGA operation.
Extension register CR80[0] = 1	A flat panel interface is enabled.
Extension register CR81[2:1] = '1X'. When CR81[2:1] = • '10', 10-dot character clocks are selected and enabled. • '11', 12-dot character clocks are selected, but this setting is not supported.	Horizontal expansion of text is enabled.
Extension register CR82[2:1] = '01'	Horizontal expansion of graphics is enabled.

12.146 CRAB: CRT HSync Start for Expansion (Low Resolution) Register

I/O Port Address: 3?5

Index: AB

Bit	Description	Reset State
7	CRT HSync Start for Expansion (Low Resolution) [7]	0
6	CRT HSync Start for Expansion (Low Resolution) [6]	0
5	CRT HSync Start for Expansion (Low Resolution) [5]	0
4	CRT HSync Start for Expansion (Low Resolution) [4]	0
3	CRT HSync Start for Expansion (Low Resolution) [3]	0
2	CRT HSync Start for Expansion (Low Resolution) [2]	0
1	CRT HSync Start for Expansion (Low Resolution) [1]	0
0	CRT HSync Start for Expansion (Low Resolution) [0]	0

This register specifies when the Horizontal Sync becomes active when a flat panel is enabled and is in a low-resolution display mode.

Bit **Description**

7:0 **CRT Horizontal Sync Start for Expansion (Low Resolution) [7:0]:**
When this register is enabled, it contains the 10-dot character count that specifies when the Horizontal Sync becomes active when a flat panel is enabled and is in a low-resolution display mode.

- Adjusting the value in this field moves the display image horizontally on the display screen.
- This register performs the same function as CRT Controller register bits CR4[7:0] in CRT-only mode.
- The value in this register is derived from the following formula:

$$\text{HSync Start} = \frac{\text{Character Counter} + (\text{Flat Panel Size} \div 20)}{2}$$

- This register is enabled when all of the following conditions occur:

Bit Setting	Condition
Sequencer register SR1[0] = X	Either an 8- or 9-dot character clock is selected.
Sequencer register SR1[3] = 1	VCLK is set for low-resolution display modes.
CRT Controller register CR1[7:0] < 6Fh	Horizontal Display End standard VGA operation.
Extension register CR80[0] = 1	A flat panel interface is enabled.
Extension register CR81[2:1] = '1X'. When CR81[2:1] = • '10', 10-dot character clocks are selected and enabled. • '11', 12-dot character clocks are selected, but this setting is not supported.	Horizontal expansion of text is enabled.
Extension register CR82[2:1] = '01'	Horizontal expansion of graphics is enabled.

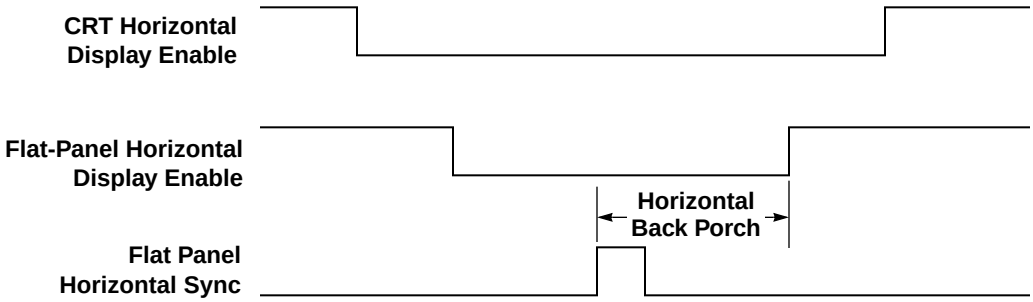
12.147 CRAC: Flat-Panel Horizontal Back Porch Register

I/O Port Address: 3?5

Index: AC

Bit	Description	Reset State
7	Flat-Panel Horizontal Back Porch [7]	0
6	Flat-Panel Horizontal Back Porch [6]	0
5	Flat-Panel Horizontal Back Porch [5]	0
4	Flat-Panel Horizontal Back Porch [4]	0
3	Flat-Panel Horizontal Back Porch [3]	0
2	Flat-Panel Horizontal Back Porch [2]	0
1	Flat-Panel Horizontal Back Porch [1]	0
0	Flat-Panel Horizontal Back Porch [0]	0

Bit	Description
7:0	**Flat-Panel Horizontal Back Porch [7:0]:** This 8-bit field defines the Horizontal Back Porch for the flat panel.



12.148 CRAD: Flat-Panel Horizontal Width Register

I/O Port Address: 3?5

Index: AD

Bit	Description	Reset State
7	Flat-Panel Horizontal Width [7]	0
6	Flat-Panel Horizontal Width [6]	0
5	Flat-Panel Horizontal Width [5]	0
4	Flat-Panel Horizontal Width [4]	0
3	Flat-Panel Horizontal Width [3]	0
2	Flat-Panel Horizontal Width [2]	0
1	Flat-Panel Horizontal Width [1]	0
0	Flat-Panel Horizontal Width [0]	0

This register defines the horizontal width for the following flat-panel resolutions: 640 x 480, 800 x 600, and 1024 x 768.

Bit **Description**

7:0 **Flat-Panel Horizontal Width [7:0]:**

- Bit 8, the most-significant bit of the 9-bit Flat-Panel Horizontal Width field, is in CRAF.
- These bits [7:0] are the least-significant 8 bits.

Register Format for 9-Bit Flat-Panel Horizontal Width

CRAF[1]	CRAD[7:0]	
8	7	0

- When a flat panel is enabled (that is, Extension register CR80[0] is 1) and it:
  - — Is an XGA (that is, a 1024 x 768 flat panel), these 8 bits are used in combination with the most-significant bit 9, in Extension register CRAF[1].
  - — Is not an XGA flat panel, only these 8 bits are used.
- The value programmed in this register:
  - — Defines the flat panel horizontal width. This width can be different from the width of the display image, stored in display memory.
  - — Must be the desired width (expressed in 4-dot-clock increments, minus 1), all expressed in hex.
  - — Is used to compensate for internal delays when displaying a narrow image on a wide display screen.
  - — Is never expressed in units of dot clock ÷ 2.

For example,

When:	A flat panel is 800 (horizontal) x 600 (vertical).
Then:	The desired horizontal width is 800 pixels. The desired horizontal width, when expressed in 4-dot-clock increments, is 800 ÷ 4 = 200, minus 1 = 199 decimal.
Program:	C7h (the hex equivalent of 199 decimal) into the flat panel horizontal width field.

12.149 CRAE: Flat-Panel Horizontal Display Enable Start Register

I/O Port Address: 3?5

Index: AE

Bit	Description	Reset State
7	Flat-Panel Horizontal Display Enable Start [7]	0
6	Flat-Panel Horizontal Display Enable Start [6]	0
5	Flat-Panel Horizontal Display Enable Start [5]	0
4	Flat-Panel Horizontal Display Enable Start [4]	0
3	Flat-Panel Horizontal Display Enable Start [3]	0
2	Flat-Panel Horizontal Display Enable Start [2]	0
1	Flat-Panel Horizontal Display Enable Start [1]	0
0	Flat-Panel Horizontal Display Enable Start [0]	0

This register contains the 8 least-significant bits of the 9-bit Flat-Panel Horizontal Display Enable Start field.

Bit **Description**

7:0 **Flat-Panel Horizontal Display Enable Start [7:0]:**
Bit 8, the most-significant bit of the 9-bit Flat-Panel Horizontal Display Enable field, is in CRAF.

- These bits [7:0] are the 8 least-significant bits.

Register Format for 9-Bit Flat-Panel Horizontal Display Enable Start

CRAF[0]	CRAE[7:0]	
8	7	0

- The Flat-Panel Horizontal Display Enable Start field provides centering of a 640-dot display by defining the present flat panel Horizontal Display Enable start signal, relative to the previous Horizontal Display Enable start signal, in 4-dot clock increments.
  - — The dot clock is never divided by 2.
  - — The value programmed in this field is one less than the Horizontal Display Enable start parameter.
  - — A fine dot-clock adjustment for this field is in Extension register bits CRAF[3:2].

12.150 CRAF: Flat-Panel and CRT Horizontal Timing and Overflow Register

I/O Port Address: 3?5

Index: AF

Bit	Description	Reset State
7	CRT Horizontal Sync Width [3]	0
6	CRT Horizontal Sync Width [2]	0
5	CRT Horizontal Sync Width [1]	0
4	CRT Horizontal Sync Width [0]	0
3	Flat-Panel Horizontal Display Enable Start Skew [1]	0
2	Flat-Panel Horizontal Display Enable Start Skew [0]	0
1	Flat-Panel Horizontal Width [8]	0
0	Flat-Panel Horizontal Display Enable Start [8]	0

Bit **Description**

7:4 **CRT Horizontal Sync Width [3:0]:**
This field determines the width of the Horizontal Sync pulse.
- The Horizontal Sync pulse is limited to 16 character clock periods.
- The hex value is programmed as shown below:
  - — 0h = 16 character clock periods (the default).
  - — 1h = 1 character clock period.
  - — 2h = 2 character clock periods.
  - — Fh = 15 character clock periods, and so forth.

3:2 **Flat-Panel Horizontal Display Enable Start Skew [1:0]:**
These 2 bits allow for fine control of the Horizontal Display Enable Start. These bits allow a skew of up to 3 dot clocks, in contrast to the coarse control of the Horizontal Display Enable Start, which uses increments of 4 dot clocks.

NOTE: The coarse control of the Horizontal Display Enable Start is controlled by Extension register bits CRAE[7:0] and CRAF[0].

1 **Flat-Panel Horizontal Width [8]:**
This bit is the most-significant bit of the 9-bit Flat-Panel Horizontal Width field.

Register Format for 9-Bit Flat-Panel Horizontal Width

CRAF[1]	CRAD[7:0]	
8	7	0

- For details on this field, refer to CRAD.

0 **Flat-Panel Horizontal Display Enable Start [8]:**
This bit is the most-significant bit of the 9-bit Flat-Panel Horizontal Display Enable Start field.

Register Format for 9-Bit Flat-Panel Horizontal Display Enable Start

CRAF[0]	CRAE[7:0]	
8	7	0

- For details on this field, refer to CRAE.

12.151 CRB0: CRT Vertical Total Register

I/O Port Address: 3?5

Index: B0

Bit	Description	Reset State
7	CRT Vertical Total [7]	0
6	CRT Vertical Total [6]	0
5	CRT Vertical Total [5]	0
4	CRT Vertical Total [4]	0
3	CRT Vertical Total [3]	0
2	CRT Vertical Total [2]	0
1	CRT Vertical Total [1]	0
0	CRT Vertical Total [0]	0

This register contains the least-significant bits of a 10-bit field that defines the total number of scanlines per frame when the flat panel is enabled.

Bit **Description**

7:0 **CRT Vertical Total [7:0]:**
Bits [9:8], the most-significant 2 bits of the 10-bit CRT Vertical Total field, are in CRB1.

- These bits [7:0] are the least-significant 8 bits.

Register Format for 10-Bit CRT Vertical Total

CRB1[1:0]		CRB0[7:0]	
9	8	7	0

- The CRT Vertical Total field is enabled when Extension register CR80[0] is 1.
  - — The value programmed into the Vertical Total field is the total number of scanlines minus two.
  - — This register, which supports flat panel-only mode and SimulSCAN mode, performs the same function as CRT Controller register bits CR6[7:0], which are used in the CRT-only mode.

12.152 CRB1: CRT Vertical Extension Register

I/O Port Address: 3?5

Index: B1

Bit	Description	Reset State
7	CRT Monitor Sense Assist in SimulSCAN	0
6	Reserved	
5	Reserved	
4	CRT Vertical Sync Start in SimulSCAN [9]	0
3	CRT Vertical Sync Start in SimulSCAN [8]	0
2	VCLKO on EPROM#	
1	CRT Vertical Total [9]	0
0	CRT Vertical Total [8]	0

This register contains the most-significant bits for CRT vertical count fields.

Bit **Description**

7 **CRT Monitor Sense Assist in SimulSCAN:**
When the SimulSCAN mode is enabled (that is, both Extension register bits CR80[1] and CR80[0] are set to 1) *and* Extension register SR2B[6] is 1, *and* this bit is 1, this bit forces a CRT monitor display for an accurate CRT monitor sense routine.
- This bit must be cleared to 0 before the CRT monitor sense routine is exited.

NOTE: In SimulSCAN mode, the timing for the CRT monitor is controlled by the timing for the flat panel.

6:5 **Reserved**

4:3 **CRT Vertical Sync Start in SimulSCAN [9:8]:**
These bits are the most-significant 2 bits of a 10-bit field, the CRT Vertical Sync Start in SimulSCAN.

Register Format for 10-Bit CRT Vertical Sync Start in SimulSCAN

CRB1[4:3]		CRB2[7:0]	
9	8	7	0

- For details on this field, refer to CRB2.

2 **VCLKO on EPROM#:**
- When SR2F[4] is set to 1, the VCLKO signal is disabled.
- When the following conditions are both true, the VCLKO signal appears on EPROM# (pin 253) and this bit setting can be used to support an LVDS solution for DSTN panels.
  - — CRB1[2] = 1
  - — Extension register bit SR22[4] = 0 (that is, there is no pull-up resistor on MD31 and as a result, there is no VGA BIOS EPROM support)

12.152 CRB1: CRT Vertical Extension Register *(cont.)*

Bit	Description
1:0	**CRT Vertical Total [9:8]:** These bits are the most-significant 2 bits of the 10-bit CRT Vertical Total field. **Register Format for 10-Bit CRT Vertical Total** CRB1[1:0] (9 8) | CRB0[7:0] (7 0) • For details on this field, refer to CRB0.

12.153 CRB2: CRT Vertical Sync Start in SimulSCAN Register

I/O Port Address: 3?5

Index: B2

Bit	Description	Reset State
7	CRT Vertical Sync Start in SimulSCAN [7]	0
6	CRT Vertical Sync Start in SimulSCAN [6]	0
5	CRT Vertical Sync Start in SimulSCAN [5]	0
4	CRT Vertical Sync Start in SimulSCAN [4]	0
3	CRT Vertical Sync Start in SimulSCAN [3]	0
2	CRT Vertical Sync Start in SimulSCAN [2]	0
1	CRT Vertical Sync Start in SimulSCAN [1]	0
0	CRT Vertical Sync Start in SimulSCAN [0]	0

This CRT Vertical Sync Start field specifies the scanline at which the CRT Vertical Sync pulse becomes active, when the CL-GD7556 is in SimulSCAN mode.

Bit **Description**

7:0 **CRT Vertical Sync Start in SimulSCAN [7:0]:**
Bits [9:8], the most-significant bits of the 10-bit CRT Vertical Sync Start in SimulSCAN field, are in CRB1.

- These bits [7:0] are the least-significant 8 bits.

Register Format for 10-Bit CRT Vertical Sync Start in SimulSCAN

CRB1[4:3]		CRB2[7:0]	
9	8	7	0

- This field is enabled when the device is in SimulSCAN mode. The CRT Vertical Sync Start field specifies the scanline at which the CRT Vertical Sync pulse becomes active.
- For proper CRT display screen vertical position in centering, expansion, or native modes, the CRT Vertical Sync Start register must be programmed as follows:

$$\text{CRT VSync Start} = \frac{\text{Vertical Sync Start} + (\text{Flat Panel Vertical Size})}{2}$$

12.154 CRB3: CRT Vertical Sync End in SimulSCAN Register

I/O Port Address: 3?5

Index: B3

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	CRT Vertical Sync End in SimulSCAN [3]	0
2	CRT Vertical Sync End in SimulSCAN [2]	0
1	CRT Vertical Sync End in SimulSCAN [1]	0
0	CRT Vertical Sync End in SimulSCAN [0]	0

Bit	Description
7:4	**Reserved**
3:0	**CRT Vertical Sync End in SimulSCAN [3:0]:** This field can program any value between 0 and 15. When the CL-GD7556 is in: • SimulSCAN mode, this field determines the CRT Vertical Sync pulse width. • CRT-only mode, this field performs the same function as CRT Controller register bits CR11[3:0].

12.155 CRBB: Flat-Panel Vertical Size Register

I/O Port Address: 3?5

Index: BB

Bit	Description	Reset State
7	Flat-Panel Vertical Size [7]	0
6	Flat-Panel Vertical Size [6]	0
5	Flat-Panel Vertical Size [5]	0
4	Flat-Panel Vertical Size [4]	0
3	Flat-Panel Vertical Size [3]	0
2	Flat-Panel Vertical Size [2]	0
1	Flat-Panel Vertical Size [1]	0
0	Flat-Panel Vertical Size [0]	0

This register contains the least-significant 8 bits of the 10-bit Flat-Panel Vertical Size field.

Bit **Description**

7:0 **Flat-Panel Vertical Size [7:0]:**
Bits [9:8], the most-significant bits of the 10-bit Flat-Panel Vertical Size field, are in CRBE.

- These bits [7:0] are the least-significant 8 bits.

Register Format for 10-Bit Vertical Size

CRBE[4:3]		CRBB[7:0]	
9	8	7	0

- The Flat-Panel Vertical Size field defines the overall vertical size in scanlines for one of the following:
  - — The lower half of a dual-scan STN flat panel
  - — The total size of a TFT flat panel
- The vertical display position is relative to:
  - — The start of the vertical midpoint on dual-scan STN flat panels
  - — The first vertical pulse on TFT flat panels
- The actual value in this register must be 2 scanlines less than the total scanlines to be displayed. (For example, for a 480-scanline display, program 478 scanlines.)
- Dual-scan STN flat panels normally have the same amount of scanlines in both the upper and lower halves of the flat panel.

12.156 CRBC: Flat-Panel Vertical Size Increment Register

I/O Port Address: 3?5

Index: BC

Bit	Description	Reset State
7	Flat-Panel Vertical Size Increment [7]	0
6	Flat-Panel Vertical Size Increment [6]	0
5	Flat-Panel Vertical Size Increment [5]	0
4	Flat-Panel Vertical Size Increment [4]	0
3	Flat-Panel Vertical Size Increment [3]	0
2	Flat-Panel Vertical Size Increment [2]	0
1	Flat-Panel Vertical Size Increment [1]	0
0	Flat-Panel Vertical Size Increment [0]	0

This field defines the vertical size increment in scanlines for the flat panel. This position is relative to the start of the vertical midpoint on dual-scan STN flat panels or the first vertical pulse on TFT flat panels.

Bit	Description
7:0	**Flat-Panel Vertical Size Increment [7:0]:** These 8 bits are added to the value in CRBB to increase the vertical size of flat panels as follows: • Extra LLCLKs are added to dual-scan STN flat panels. • Extra FPDEs are added to TFT flat panels.

12.157 CRBD: Flat-Panel LFS Vertical Position Register

I/O Port Address: 3?5

Index: BD

Bit	Description	Reset State
7	Flat-Panel LFS Vertical Position [7]	0
6	Flat-Panel LFS Vertical Position [6]	0
5	Flat-Panel LFS Vertical Position [5]	0
4	Flat-Panel LFS Vertical Position [4]	0
3	Flat-Panel LFS Vertical Position [3]	0
2	Flat-Panel LFS Vertical Position [2]	0
1	Flat-Panel LFS Vertical Position [1]	0
0	Flat-Panel LFS Vertical Position [0]	0

This register defines the vertical position of the frame relative to the LFS (LCD Frame Start) in scanlines.

Bit	Description
7:0	**Flat-Panel LFS Vertical Position [7:0]:** Bits [9:8], the most-significant bits of the 10-bit LFS Vertical Position field, are in CRBE. • These bits [7:0] are the least-significant 8 bits. **Register Format for 10-Bit LFS Vertical Position** CRBE[1:0] (9 8) | CRBD[7:0] (7 0) • This field defines the vertical position of the frame relative to the LFS, in scanlines.

12.158 CRBE: Flat-Panel Vertical Extension Register

I/O Port Address: 3?5

Index: BE

Bit	Description	Reset State
7	Select Read Pulse Delay for Graphics CLUT [1]	0
6	Select Read Pulse Delay for Graphics CLUT [0]	0
5	Reserved	
4	Flat-Panel Vertical Size [9]	0
3	Flat-Panel Vertical Size [8]	0
2	Reserved – Applications must not program this bit	0
1	Flat-Panel LFS Vertical Position [9]	0
0	Flat-Panel LFS Vertical Position [8]	0

Bit **Description**

7:6 **Select Read Pulse Delay for Graphics CLUT [1:0]:**
These bits select the Read pulse delay for the graphics CLUT.

CRBE		Read Pulse Clock Delay
[7]	[6]	
0	0	2 Delay
0	1	1 Delay
1	0	3 Delay
1	1	no Delay

5 **Reserved**

4:3 **Flat-Panel Vertical Size [9:8]:**
These are the most-significant 2 bits of the 10-bit Flat-Panel Vertical Size field.

Register Format for 10-Bit Vertical Size

CRBE[4:3]		CRBB[7:0]	
9	8	7	0

- For details on this field, refer to CRBB.

2 **Reserved:** Applications must not program this bit

1:0 **Flat-Panel LFS Vertical Position [9:8]:**
These are the most-significant 2 bits of the 10-bit LFS Vertical Position field.

Register Format for 10-Bit LFS Vertical Position

CRBE[1:0]		CRBD[7:0]	
9	8	7	0

- For details on this field, refer to CRBD.

12.159 CRBF: CRT Vertical Back Porch Register

I/O Port Address: 3?5

Index: BF

Bit	Description	Reset State
7	CRT Vertical Back Porch [7]	0
6	CRT Vertical Back Porch [6]	0
5	CRT Vertical Back Porch [5]	0
4	CRT Vertical Back Porch [4]	0
3	CRT Vertical Back Porch [3]	0
2	CRT Vertical Back Porch [2]	0
1	CRT Vertical Back Porch [1]	0
0	CRT Vertical Back Porch [0]	0

Bit	Description
7:0	**CRT Vertical Back Porch [7:0]:** This register defines the Vertical Back Porch for a CRT monitor in scanlines. This register takes effect when vertical auto-centering is enabled (that is, Extension register CR81[3] is 0, which is the default).

12.160 HDR: Hidden DAC Register

I/O Port Address: 3C6

Index: (n/a)

Bit	Description	Reset State
7	RGB 5-5-5 Extended Color Mode Enable	0
6	Extended Color Mode Select Enable	0
5	Reserved	
4	Reserved	
3	Extended Color Mode Select [3]	0
2	Extended Color Mode Select [2]	0
1	Extended Color Mode Select [1]	0
0	Extended Color Mode Select [0]	0

The Hidden DAC Register (HDR) is 'hidden' because it shares its I/O address with External/General register 3C6. The HDR:

- Is used to enable extended color modes, including the following:
  - 15-bit/pixel extended color mode
  - 16-bit/pixel extended color mode
  - 24-bit/pixel extended color mode
- Is accessed by reading four times in succession External/General register 3C6 (the Pixel Mask register). The next write or read of the 3C6 register then accesses the HDR.
  - A *write* to the HDR resets the internal counter, and the four dummy reads of the 3C6 register must be executed again.
  - A *read* from the HDR resets the internal counter, and the four dummy reads of the 3C6 register must be executed again.
  - Reads from the 3C6 register do not lock the HDR.
- Is cleared to all zeroes at reset, putting the CL-GD7556 in VGA-compatibility mode.
- Does not affect Video-Window modes.

Bit	Description
7	**RGB 5-5-5 Extended Color Mode Enable:** When this bit is: • 0, extended color modes are disabled and the palette DAC is VGA-compatible. • 1, extended color modes are enabled (including the RGB 5-5-5 extended color mode), as chosen by HDR bits [6, 3:0].
6	**Extended Color Mode Select Enable:** When HDR bit [7] is 1 *and* this bit is: • 0, HDR bits [3:0] are disabled and the extended color mode is the RGB 5-5-5 mode. • 1, HDR bits [3:0] are enabled to select an extended color mode (other than the RGB 5-5-5 mode).
5:4	**Reserved –** These bits should always be programmed to '0'

12.160 HDR: Hidden DAC Register *(cont.)*

Bit	Description
3:0	**Extended Color Mode Select [3:0]:** When HDR[7:6] is '11', this 4-bit field selects an extended color mode according to the following table:

HDR								Color Mode	
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]		
0	X	X	X	X	X	X	X	VGA compatibility color mode	
1	0	0	0	X	X	X	X	Extended VGA color modes	RGB 5-5-5
1	1	0	0	0	0	0	1		RGB 5-6-5 XGA
1	1	0	0	0	1	0	1		RGB 8-8-8 16M color
1	1	0	0	0	1	1	X		DAC power-down
1	1	0	0	1	0	0	0		8-bit grayscale

NOTE: Any undefined settings are reserved.

Notes

13. ELECTRICAL SPECIFICATIONS

The following abbreviations, acronyms, symbols, and terms are used in the following sections:

- CFG Abbreviation for 'Configuration'
- CMD Abbreviation for Command
- CMOS Acronym for 'complementary metal-oxide semiconductor'
- High-Z A term used to indicate a high-impedance state
- MCLK An abbreviation used to indicate the CL-GD7556 internal memory clock
- T A symbol used to indicate the period for the CL-GD7556 internal MCLK
- T_A A symbol used to indicate ambient temperature
- tbd Acronym for 'to be determined'
- TYP An abbreviation used to indicate a 'typical' value
- V An abbreviation for 'volts'
- VCLK An abbreviation used to indicate the CL-GD7556 internal graphics/video clock

13.1 Absolute Maximum Ratings

Specification	Maximum Rating
Ambient temperature while operating (T_A)	0°C to 70°C
Storage temperature	–65°C to 150°C
Voltage on any I/O pin	– 0.5 V to +5.5 V
Operating power dissipation	2.75 Watts
Power supply voltage (V_{DD})	3.5 V
Injection current (latch-up testing)	100 mA

NOTES:

1) System components must be operated within the limits of the absolute maximum ratings. If system components are run at ratings at or outside these limits, the system components can be permanently damaged.
2) Functional operation at, or outside, any of the conditions indicated in the absolute maximum ratings is not implied.
3) Exposure to absolute maximum rating conditions for extended periods can affect system reliability.
4) All voltages are referenced to V_{SS}, which is tied to system ground.
5) 'Positive' currents are currents going into the CL-GD7556. 'Negative' currents are currents coming out of the CL-GD7556.

13.2 DC Specifications

13.2.1 DC Specifications — Digital Values

In the table below, V_{DD} = 3.3 ± 0.15 V and T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Conditions	Note
V_{DD}	Power Supply Voltage	3.15	3.45	Volts	Normal operation	
V_{IH}	Input High Voltage	$0.7V_{DD}$	V_{DD} + 0.5	Volts	3.15 V < V_{DD} < 3.45 V	1
V_{IL}	Input Low Voltage	–0.5	$0.3V_{DD}$	Volts	3.15 V < V_{DD} < 3.45 V	1
V_{OH}	Output High Voltage	2.8	V_{DD}	Volts	I_{OH} = (see Table 13-1), V_{DD} = 3.15 V	
V_{OH}	MD[63:0] Output High Voltage	2.0	V_{DD}	Volts	I_{OH} = –12 mA, V_{DD} = 3.3 V	2
V_{OL}	Output Low Voltage		0.33	Volts	I_{OL} = (see Table 13-1), V_{DD} = 3.15 V	
V_{OL}	MD[63:0] Output Low Voltage		0.6	Volts	I_{OL} = 12 mA, V_{DD} = 3.3 V	3
I_{DD1}	Power Supply Current		345	mA	CRT-only operation: 1280 × 1024, 8 bpp, 60-Hz vertical refresh. Video window, V-Port, and BitBLT running simultaneously.	4
I_{DD2}	Power Supply Current		475	mA	Flat panel-only operation: XGA DSTN panel. Video window, V-Port, and BitBLT running simultaneously.	4
I_{DD3}	Power Supply Current		2	mA	Hardware-controlled Suspend mode	4
I_{IL}	Input Low Current		–10	µA	V_{IN} = 0.0 V	
I_{IH}	Input High Current		10	µA	V_{IN} = 5.25 V	5
I_{OZ}	Output Leakage Current	–10	10	µA	0 < V_{OUT} < 5.25 V	5,6
C_{IN}	Input Capacitance		10	pF		7
C_{OUT}	Output Capacitance		10	pF		7

NOTES:

1) All CL-GD7556 inputs are CMOS compatible, which means the threshold is approximately in the center of the voltage swing from V_{SS} (that is, ground) to V_{DD}.
2) When V_{DD} = 3.3 V, outputs MD[63:0] rated at V_{OH} = 2.4 V at I_{OH} = –3 mA can source I_{OH} = –12 mA at V_{OH} = 2.0 V.
3) When V_{DD} = 3.3 V, outputs MD[63:0] rated at V_{OL} = 0.4 V at I_{OL} = 4 mA can sink I_{OL} = 12 mA at V_{OL} = 0.6 V.
4) These power supply current values occur when V_{DD} = 3.3 V and MCLK = 80 MHz.
5) The I/O inputs of the CL-GD7556 are 5.0-V tolerant.
6) This current is a measure of tristate output leakage current when in high-impedance mode.
7) This capacitance is periodically sampled and tested.

Table 13-1. Loading Values for Digital Output Pins

PQFP Pin Number[a]	Pin Name	I_{OH} (mA)	I_{OL} (mA)	Load (pF)
26–35, 37–42, 67–76, 78–81, 83–84	AD[31:0]	–3	2	240
43	INTR#	–4	6	200
45	STOP#	–4	10	200
46	PAR	–4	10	200
47	DEVSEL#	–6	10	200
48	TRDY#	–6	10	200
57	SUSPST#	–4	6	35
98	DDCC / VCLKO	—	6	35
104	DDCD	—	4	50
112	HSYNC	–4	6	50
114	VSYNC	–4	6	50
115	VREF	Analog Output		
118	CSYNC	–4	6	50
119	PROG1	–3	6	50
120	BLUE	Analog Output		
121	GREEN	Analog Output		
122	RED	Analog Output		
123	FPVEE	–3	6	35
124	FPDECTL	–4	6	50
125	FPVCC	–3	6	35
127	PROG0 / TV-ON	–3	6	50
129	PROG2 / NTSC/PAL	–3	6	50
150:143, 141:135, 133:131, 176:172, 170:166, 164:157	FP[35:0]	–3	6	50
152	FPDE	–3	6	50
153	LLCLK[b]	–4	6	50
155	FPVDCLK[a]	–4	6	50
156	LFS	–3	6	50
178–187, 195–199, 201–206, 209–219, 234–238, 240–242, 245–249, 3–7, 9–14, 17–24	MD[63:0]	–3	4	50
188–189, 207–208, 243–244, 15–16	CAS[7:0]#	–3	4	50
	WE[7:0]#	–3	4	50
193, 221–225, 229–232	MA[9:0]	–3	4	50
194, 228	RAS[1:0]#	–3	4	50
226	CAS# / WE#	–3	4	50
245–249, 3–7, 9–14	ROMA[15:0]	–3	4	50
253	EROM#	–3	4	50
255	OE#	–3	4	50

[a] See Table 1-1 for the equivalent PBGA ball-position numbers.

[b] The LLCLK and FPVDCLK I_{OH} and I_{OL} values depend on the setting of Extension register bit SR2B[7]. The default is SR2B[7] = 0. When this bit = 1, the values for these pins are: I_{OH} = –8 mA, I_{OL} = 12 mA, and the load remains 50 pF.

13.2.2 DC Specifications — Palette DAC

In the table below, V_{DD} = 3.3 ± 0.15 V and T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Conditions
DACVDD	DAC Supply Voltage	3.15	3.45	Volts	Normal Operation
$AI_{DD2,3}$	Analog Supply Current		60	mA	$AV_{DD2,3}$ = 3.45 V
I_{REF} [a] (Externally Generated)	DAC Reference Current (Nominal)	6.20	7.14	mA	Refer to note a.

[a] The standard IREF current is generated internally. However, if the internal IREF current is not used, an external source can be supplied by clearing Extension register SR32[5] to 0 and following the directions in the application note “IREF Current Source” in the *CL-GD7556 Application Book*, using the values in this table.

13.2.3 DC Specifications — Frequency Synthesizer

In the table below, V_{DD} = 3.3 ± 0.15 V and T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Conditions
MAVDD VAVDD	Synthesizer Supply Voltage	3.15	3.45	Volts	V_{DD} = 3.3 ± 0.15 V

13.3 DAC Characteristics

In the table below, V_{DD} = 3.3 ± 0.15 V and T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Units	Notes
	Resolution		8	bits	
I_O	Output Current		30	mA	1
t_D	Analog Output Delay		tbd	ns	2, 3
t_r, t_f	Analog Output Rise/Fall Time		5	ns	3, 4
t_s	Analog Output Settling Time		15	ns	3, 5
t_{SK}	Analog Output Skew		tbd	ns	3, 6
FT	Clock and Data Feed-Through		tbd	MHz	3, 6
DT	DAC-to-DAC Correlation		tbd		6, 7
GI	Glitch Impulse		tbd		3, 6
CT	DAC-to-DAC Crosstalk		tbd		3, 4

NOTES:

1) I_O, the output current measure, occurs under the condition V_O < 1 volt.
2) t_D is measured from the 50% point of VCLK to 50% point of full-scale transition.
3) Per analog output, the load is 50 Ω and 30 pF.
4) t_r and t_f are measured from 10% to 90% full-scale.
5) t_s is measured from 50% of full-scale transition to output remaining within 2% of final value.
6) Outputs are loaded identically.
7) About the mid-point of the distribution of the three DACs, measured at full-scale output.

13.4 AC Parameters — List of Timing Relationships

13.5 Chip Configuration — System Reset Timing

The timing diagram in this section is for the CL-GD7556 configuration, which takes place during system reset. Table 13-2 and Figure 13-1 refer to information from the MD[40:24] and SW0 pins, which are read by Extension register bits SR22[7:0] and SR24[7,2:0] and used by the memory data lines to configure the CL-GD7556.

Table 13-2. Chip Configuration — System Reset Timing

Symbol	Parameter	MIN	MAX	Units
t_1	System reset pulse width	12	–	MCLKs
t_2	Memory data setup time to system reset rising edge	2	–	ns
t_3	Memory data hold time from system reset rising edge	5	–	ns
t_4	System reset high to first PCI bus command	12	–	MCLKs

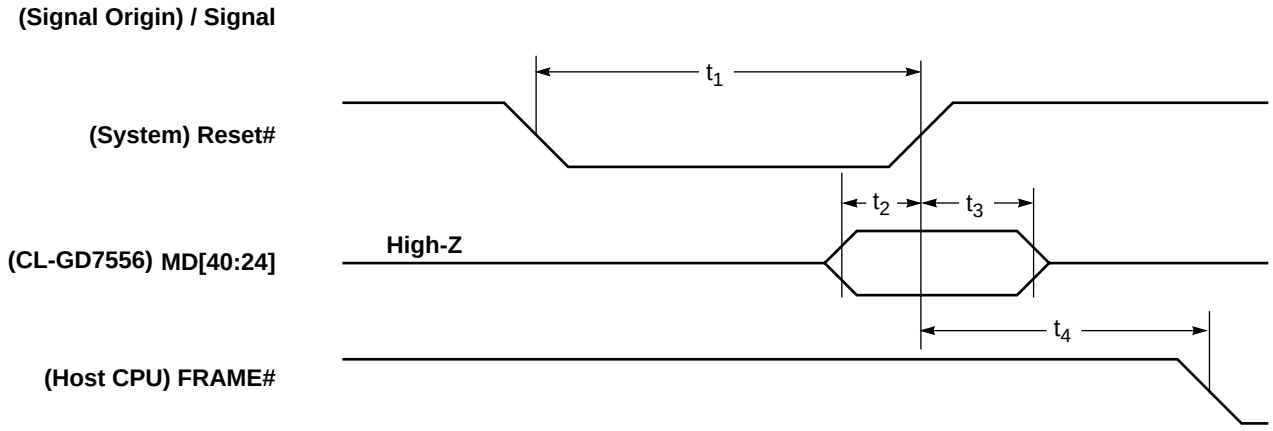


Figure 13-1. Bus Configuration — System Reset Timing

13.6 Timing Diagrams — CL-GD7556 to PCI Bus

The timing diagrams in this section apply to the interface from the CL-GD7556 to the PCI bus.

Table 13-3. PCI Bus — Clock Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Rise time (10% to 90%)	0.5	4.0	ns
t_2	Fall time (90% to 10%)	0.5	4.0	ns
t_3	High pulse width	40%	60%	T_{PCI}
t_4	Low pulse width	40%	60%	T_{PCI}
T_{PCI}	Period	30	tbd	ns

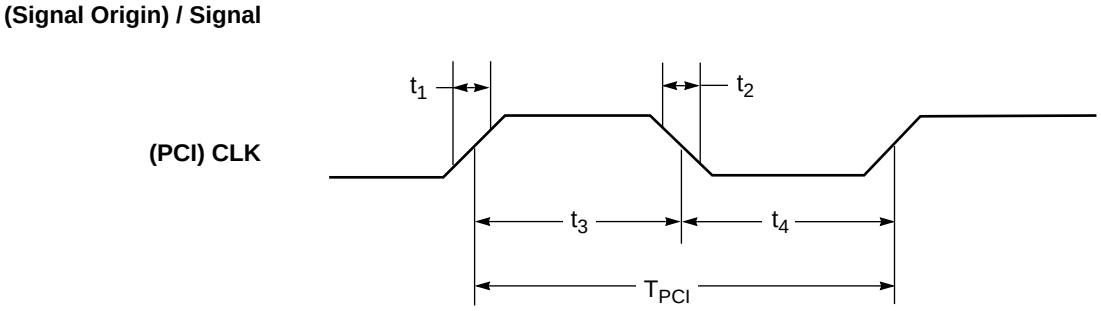


Figure 13-2. PCI Bus — Clock Timing

Table 13-4. PCI Bus — FRAME#, AD[31:0], C/BE[3:0]#, DEVSEL#, and TRDY# Timing

Symbol	Parameter	MIN	MAX	Units
t_1	FRAME# setup to CLK	7	–	ns
t_2	AD[31:0] (Address) setup to CLK	7	–	ns
t_3	AD[31:0] (Address) hold from CLK	0	–	ns
t_4	AD[31:0] (Data) setup to CLK (write)	7	–	ns
t_5	AD[31:0] (Data) hold from CLK (write)	0	–	ns
t_6	C/BE[3:0]# (Bus Command) or (Byte Enable) setup to CLK	7	–	ns
t_7	C/BE[3:0]# (Bus Command) hold from CLK	0	–	ns
t_8	AD[31:0] (Data) delay from CLK (read)	2	11	ns
t_9	AD[31:0] or C/BE[3:0]# to high-impedance delay from CLK (read)	0	28	ns
t_{10}	DEVSEL# delay from CLK	2	15	ns
t_{11}	DEVSEL# and TRDY# high before high-Z	1	–	T_{PCI}
t_{12}	TRDY# delay from CLK	2	18	ns

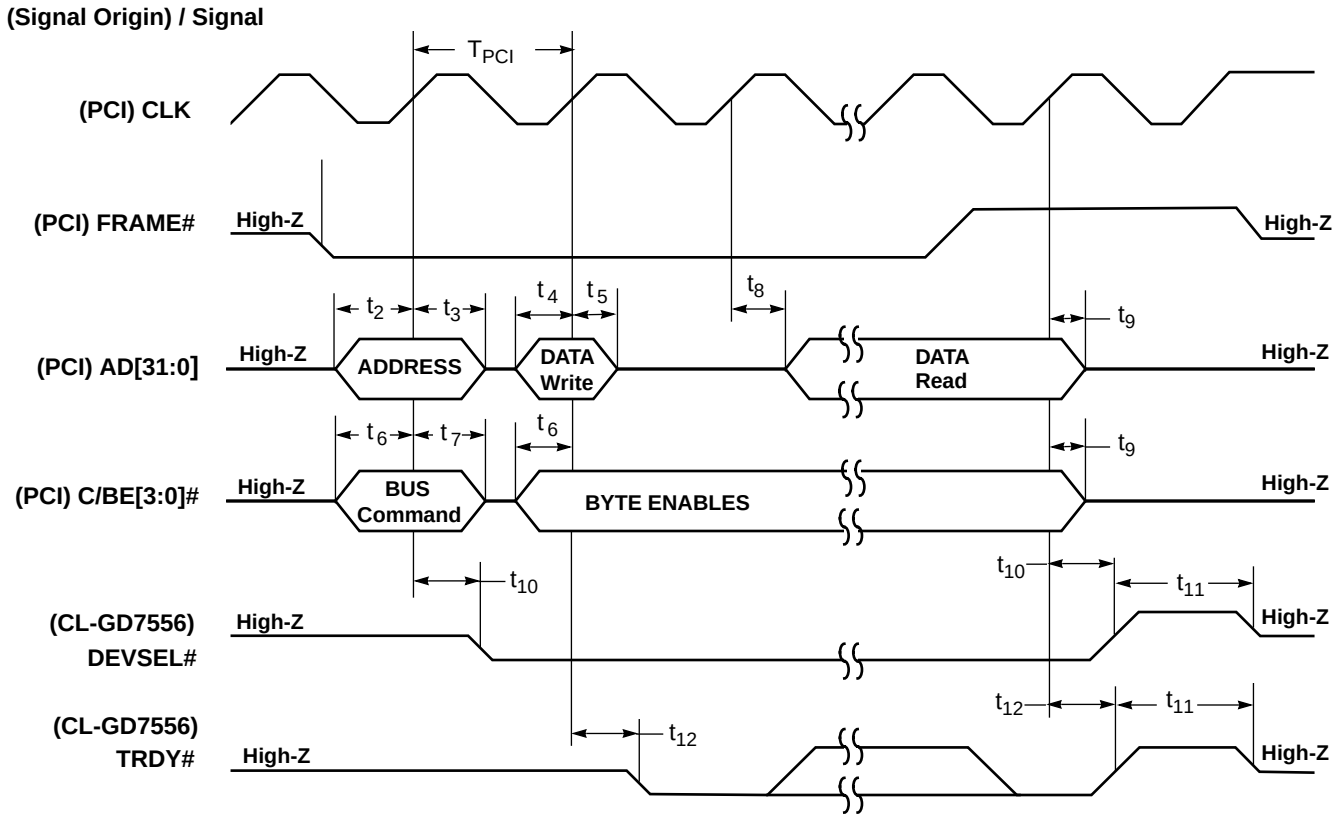


Figure 13-3. PCI Bus — FRAME#, AD[31:0], C/BE[3:0]#, DEVSEL#, and TRDY# Timing

Table 13-5. PCI Bus — STOP# Delay Timing

Symbol	Parameter	MIN	MAX	Units
t_1	STOP# low delay from CLK	2	15	ns
t_2	STOP# high delay from CLK	2	15	ns
t_3	STOP# high pulse before high-Z	1	–	T_{PCI}

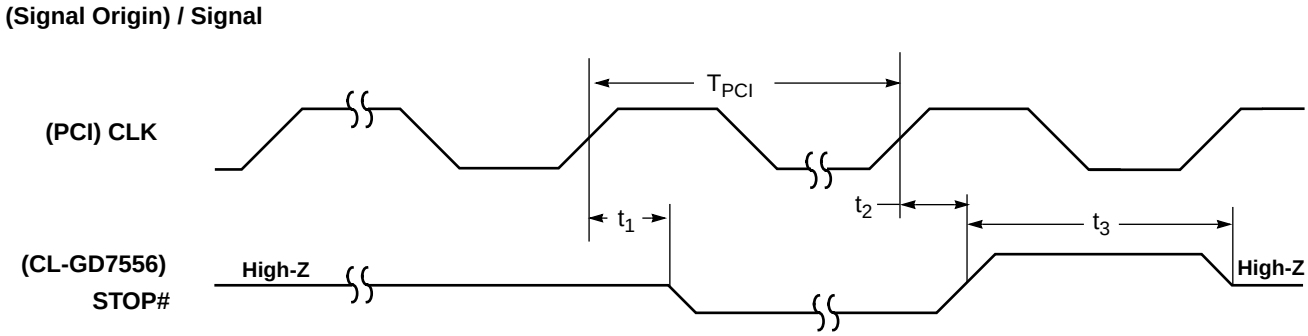


Figure 13-4. PCI Bus — STOP# Delay and Read Data / IRDY# Timing

Table 13-6. PCI Bus — Read Data / TRDY# and IRDY# Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Read Data setup to TRDY# active	7	–	ns
t_2	Read Data hold from TRDY# inactive	0	–	ns
t_3	IRDY# setup to CLK	7	–	ns
t_4	IRDY# hold from CLK	0	–	ns

[Signal Origin) / Signal

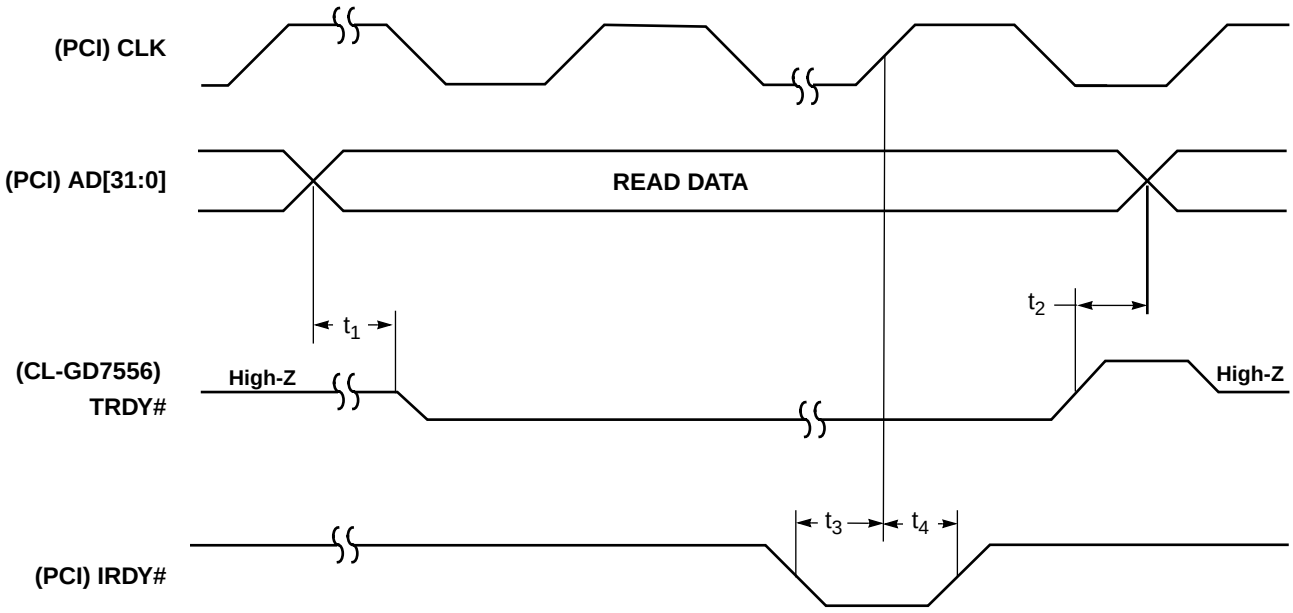


Figure 13-5. PCI Bus — TRDY# Delay and Read Data / IRDY# Timing

Table 13-7. PCI Bus — IDSEL Timing

Symbol	Parameter	MIN	MAX
t_1	IDSEL setup to CLK	7 ns	–
t_2	IDSEL hold from CLK	0 ns	–

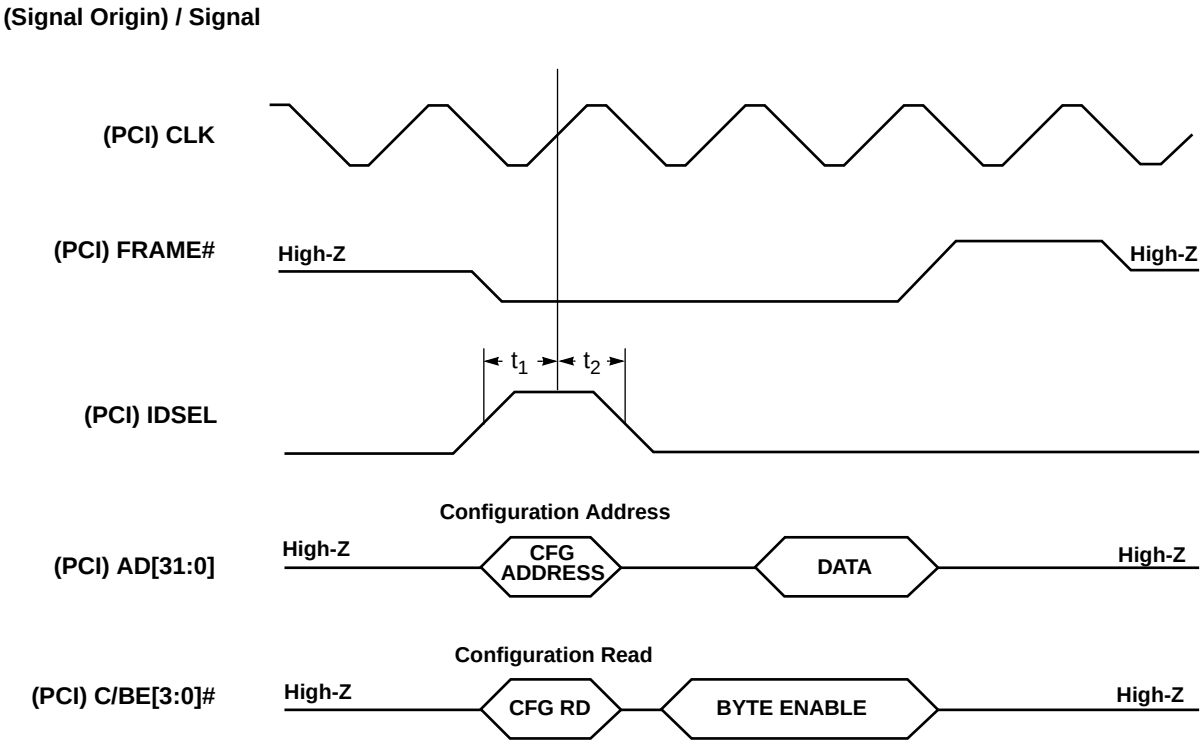


Figure 13-6. PCI Bus — IDSEL Timing

Table 13-8. PCI Bus — Parity Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Address and Command PAR setup from CLK (input to CL-GD7556)	7	–	ns
t_2	Address and Command PAR hold from CLK (input to CL-GD7556)	0	–	ns
t_3	Data In and Byte Enable PAR setup from CLK (input to CL-GD7556)	7	–	ns
t_4	Data In and Byte Enable PAR hold from CLK (input to CL-GD7556)	0	–	ns
t_5	Data output PAR delay from CLK (output from CL-GD7556)	2	12	ns
t_6	Data output PAR 'off' delay from CLK (output from CL-GD7556)	–	28	ns

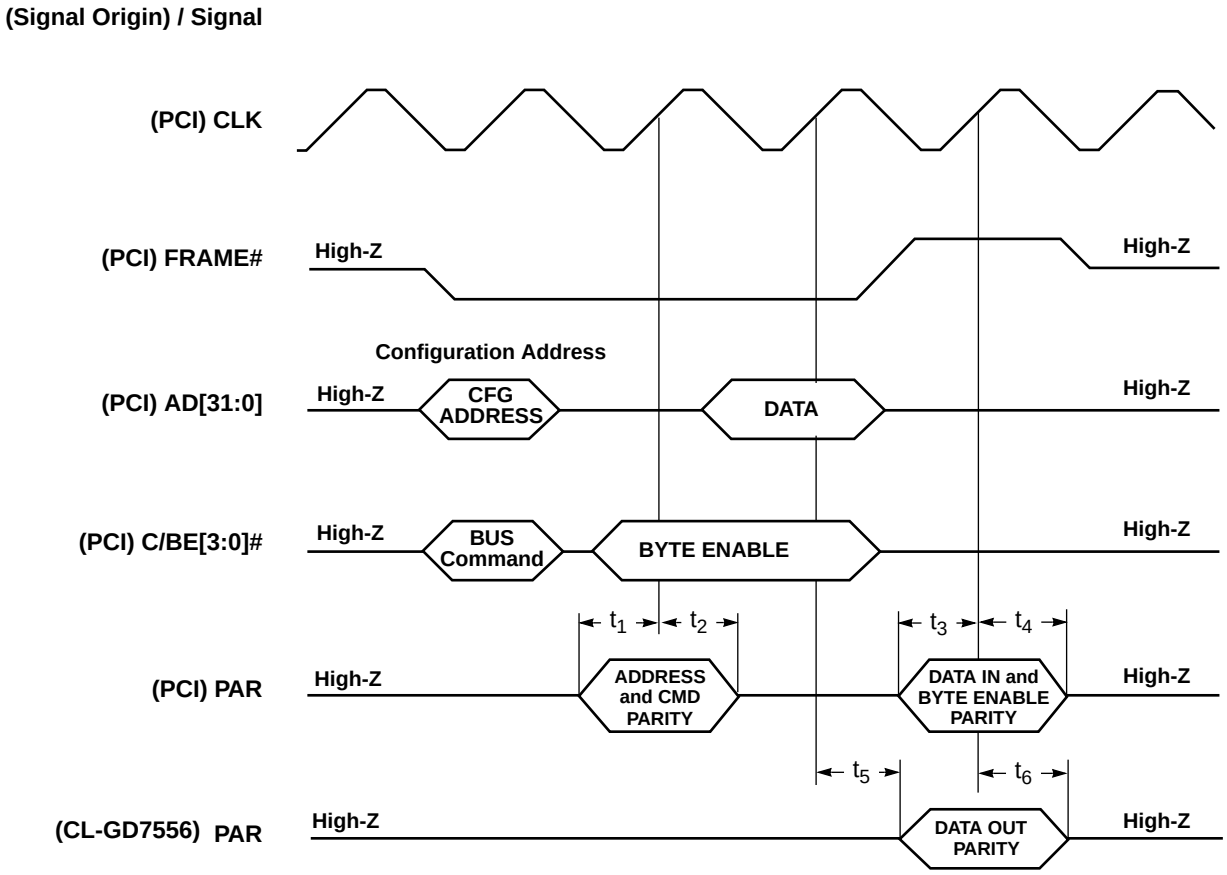


Figure 13-7. PCI Bus — Parity Timing

13.7 Timing Diagrams — CL-GD7556 to Display Memory Bus

The timing diagrams in this section apply to the interface from the CL-GD7556 to a display memory bus. Table 13-9 and Figure 13-8 apply to the interface from the CL-GD7556 to a display memory bus for EDO (extended data out) DRAMs. For the display memory bus interface for EDO DRAMs, the data bus does not go to high-impedance between paged read or write cycles.

Table 13-9. Display Memory Bus — EDO (Hyper-page-mode) DRAM Read and Write Timing

Symbol	Parameter	MIN	MAX
T	MCLK period		
t_1	RAS# pulse width low	5 T	–
t_2	RAS# precharge (t_8 = 8 MCLKs)	3 T – 1 ns	–
	RAS# precharge (t_8 = 9 MCLKs)	4 T – 1 ns	–
t_3	CAS# precharge to RAS# low	1 T – 2 ns	–
t_4	RAS# low to CAS# low delay	4 T – 2 ns	–
t_5	CAS# pulse width low	1 T	–
t_6	CAS# precharge (CAS# pulse width high)	1 T	–
t_7	CAS# (EDO Hyper-page mode) cycle time	2 T	–
t_8	Random read cycle time. (Extension register bits SR20[6] = 0 and GR18[2] = 1.)	8 T	–
	Random read cycle time. (Extension register bits SR20[6] = 1 and GR18[2] = 1.)	9 T	–
t_9	Row address setup to RAS# low	2 T	–
t_{10}	Row address hold from RAS# low	3 T – 3 ns	–
t_{11}	Column address setup to CAS# low	1 T – 3 ns	–
t_{12}	Column address hold from CAS# low	1 T – 2 ns	–
t_{13}	CAS# pulse width low for last cycle of paged read	3 T	–
EDO DRAM Read Timing			
t_{14}	WE# read command setup time	3 T – 2 ns	–
t_{15}	WE# read command hold time	1 T – 2 ns	–
t_{16}	Read data hold CAS# low	5 ns	–
t_{17}	CAS# access time	2 T – 3 ns	–
EDO DRAM Write Timing			
t_{18}	WE# write command setup time	2 T – 4 ns	–
t_{19}	WE# write command hold time	2 T – 4 ns	–
t_{20}	Write data setup time to CAS# low	1 T – 2 ns	–
t_{21}	Write data hold from CAS# low	1 T – 2 ns	–

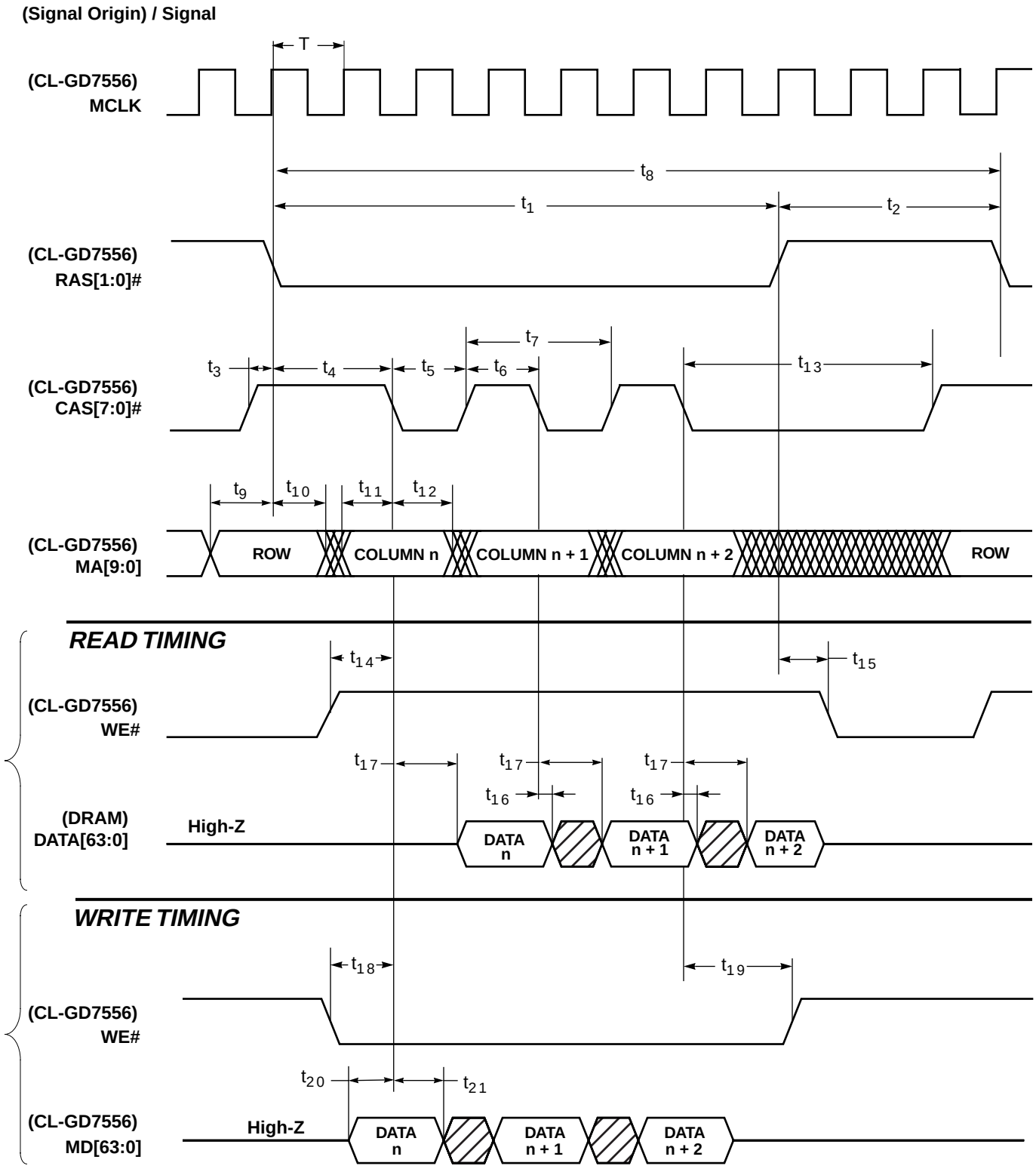


Figure 13-8. Display Memory Bus — Read and Write Timing for EDO DRAMs

Table 13-10. Display Memory Bus — Typical BitBLT Read/Write Cycle Timing

Symbol	Parameter		Nominal Cycle When Extension Register GR18[2] = 1 (EDO DRAM)
T	MCLK period		
t_1	WE# low delay from CAS# high	GR18[0] = 0	3 T
		GR18[0] =1	2 T
t_2	Read CAS# to Write CAS# delay	GR18[1] = 0	4 T
		GR18[1] = 1	3 T
t_3	WE# low setup time to CAS# low		1 T

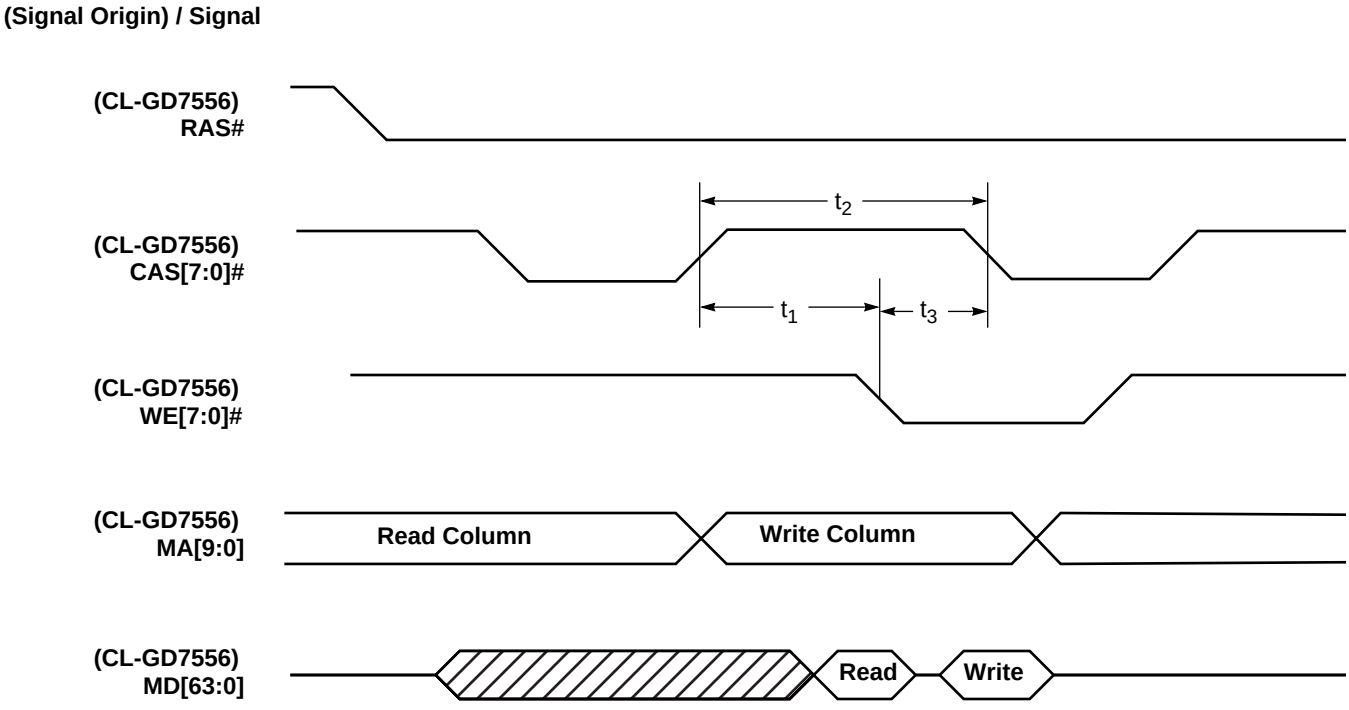


Figure 13-9. Display Memory Bus — Typical BitBLT Read/Write Cycle Timing

Table 13-11. Display Memory Bus — CAS#-before-RAS# Refresh Timing

Symbol	Parameter	MIN	MAX
T	MCLK period		
t_1	RAS# Precharge (RAS# Pulse Width High)	3 T – 1 ns	–
t_2	RAS# Pulse Width Low	5 T	–
t_3	RAS# to CAS# Precharge Time	1 T – 2 ns	–
t_4	CAS# Precharge Time	1 T – 2 ns	–
t_5	CAS# Setup Time	1 T – 2 ns	–
t_6	CAS# Hold Time	1 T – 2 ns	–

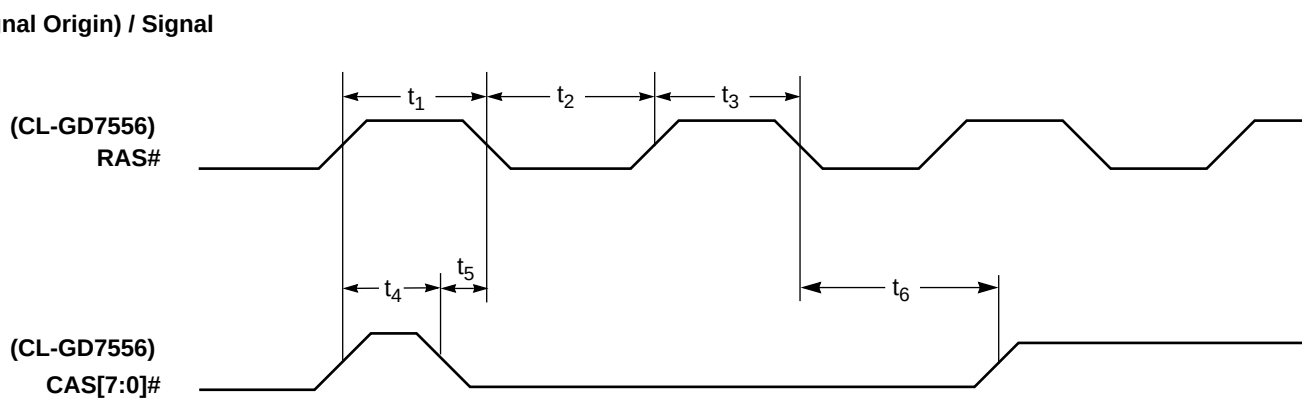


Figure 13-10. Display Memory Bus — CAS#-before-RAS# Refresh Timing

13.8 Timing Diagrams — CL-GD7556 to Flat Panel

The timing diagrams in this section apply to the interface from the CL-GD7556 to flat panels.

Typical Flat Panels Supported by the CL-GD7556

Flat Panel Code	Flat Panel Type	Flat Panel Maximum Resolution	Number of Colors Supported	Data Interface	Timing Diagram Reference
C8DD-16	Dual-Scan STN	800 × 600	8	16-bit	Figure 13-11
C8DD-8	Dual-Scan STN	800 × 600	8	8-bit	Figure 13-11
C512SS-9	1-Pixel/Clock TFT	1024 × 768	512	9-bit	Figure 13-12
C4KSS-12	1-Pixel/Clock TFT	1024 × 768	4K	12-bit	Figure 13-12
C256KSS-18	1-Pixel/Clock TFT	1024 × 768	256K	18-bit	Figure 13-12
C16MSS-24	1-Pixel/Clock TFT	1024 × 768	64K	24-bit	Figure 13-12
C4KSS-24	2-Pixel/Clock TFT	1024 × 768	4K	24-bit	Figure 13-12
C256KSS-36	2-Pixel/Clock TFT	1024 × 768	256K	36-bit	Figure 13-12

Table 13-12. Flat Panels — High-Resolution Color Dual-scan STN Timing

Symbol	Parameter	C8DD-16		C8DD-8	
		MIN	MAX	MIN	MAX
T_D	Dot Clock Period for DSTN Panel				
t_1	FPVDCLK period	$2.5T_D$ – 6 ns		T_D – 6 ns	
t_2	FPVDCLK high time	T_D – 6 ns		$0.5T_D$ – 6 ns	
t_3	FPVDCLK low time	T_D – 6 ns		$0.5T_D$ – 6 ns	
t_4	FPVDCLK rise and fall time		6 ns		6 ns
t_5	Pixel Data setup time	T_D – 6 ns		$0.5T_D$ – 6 ns	
t_6	Pixel Data hold time	T_D – 6 ns		$0.5T_D$ – 6 ns	
t_7	FPVDCLK low to LLCLK low	T_D – 6 ns		$2T_D$ – 10 ns	
t_8	FPVDCLK low from LLCLK low	T_D – 6 ns		$2T_D$ – 10 ns	
t_9	LLCLK high time	$4T_D$ – 6 ns		$4T_D$ – 6 ns	
t_{10}	LFS high setup to LLCLK low (typical)	$2T_D$ (TYP)		$2T_D$ (TYP)	
t_{11}	LFS high hold time from LLCLK low (typical)	$2T_D$ (TYP)		$2T_D$ (TYP)	

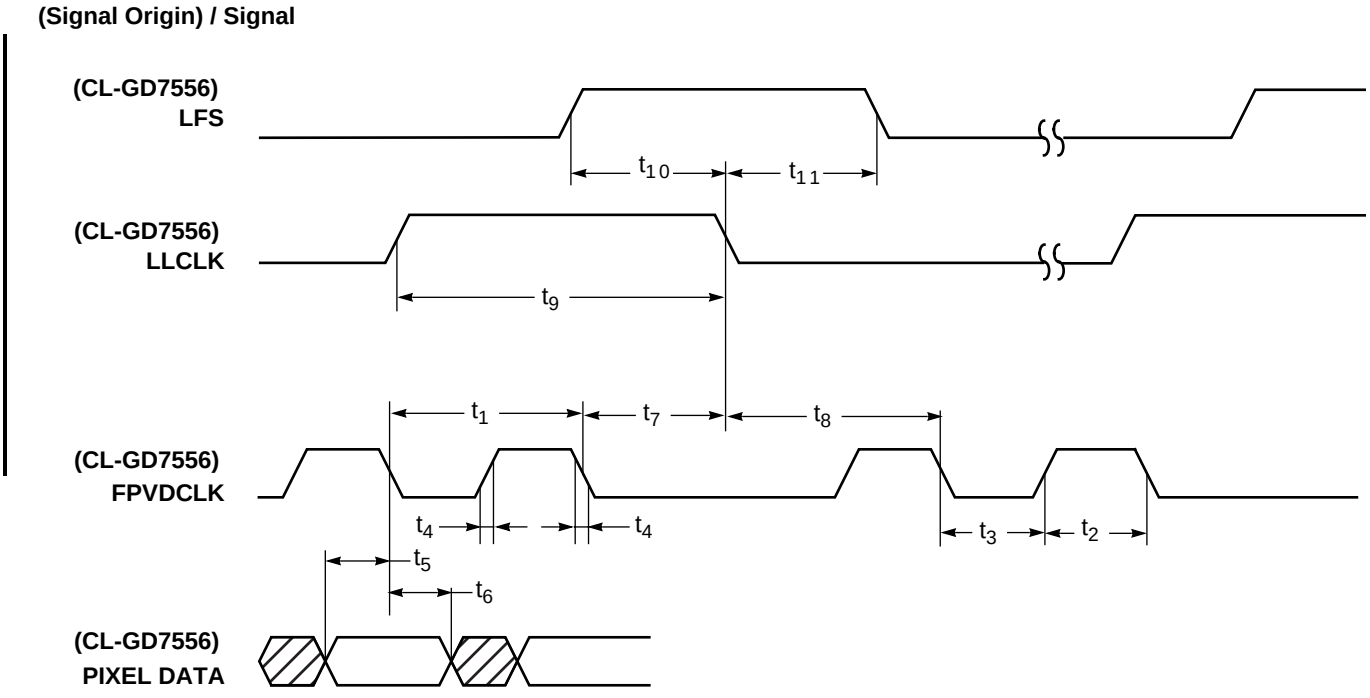


Figure 13-11. Timing Diagram for High-Resolution Color Dual-Scan STN Panels

Table 13-13. Flat Panels — High-Resolution Color TFT Timing

Symbol	Parameter	TFT C512SS / C4KSS / C256KSS / C16MSS		TFT 2-Pixel/Clock C4KSS / C256KSS	
		MIN	MAX	MIN	MAX
T_D	Dot Clock Period for TFT Panel				
t_1	FPVDCLK period	T_D – 6 ns		$2T_D$ – 6 ns	
t_2	FPVDCLK high pulse width	$0.5T_D$ – 6 ns		T_D – 6 ns	
t_3	FPVDCLK low pulse width	$0.5T_D$ – 6 ns		T_D – 6 ns	
t_4	FPVDCLK rise and fall time		6 ns		6 ns
t_5	Pixel Data setup time	$0.5T_D$ – 6 ns		T_D – 6 ns	
t_6	Pixel Data hold time	$0.5T_D$ – 6 ns		T_D – 6 ns	
t_7	FPDE setup to FPVDCLK	$0.5T_D$ – 6 ns		T_D – 6 ns	
t_8	FPDE hold to FPVDCLK	$0.5T_D$ – 6 ns		T_D – 6 ns	
t_9	LLCLK pulse width	$4T_D$ – 6 ns		$4T_D$ – 6 ns	
t_{10}	Horizontal front porch	0 ns	FPDE low period	0 ns	FPDE low period
t_{11}	Horizontal back porch	0 ns	256T	0 ns	256T
t_{12}	LFS pulse width	1 scanline	16 scanlines	1 scanline	16 scanlines
t_{13}	Vertical back porch	1 scanline		1 scanline	

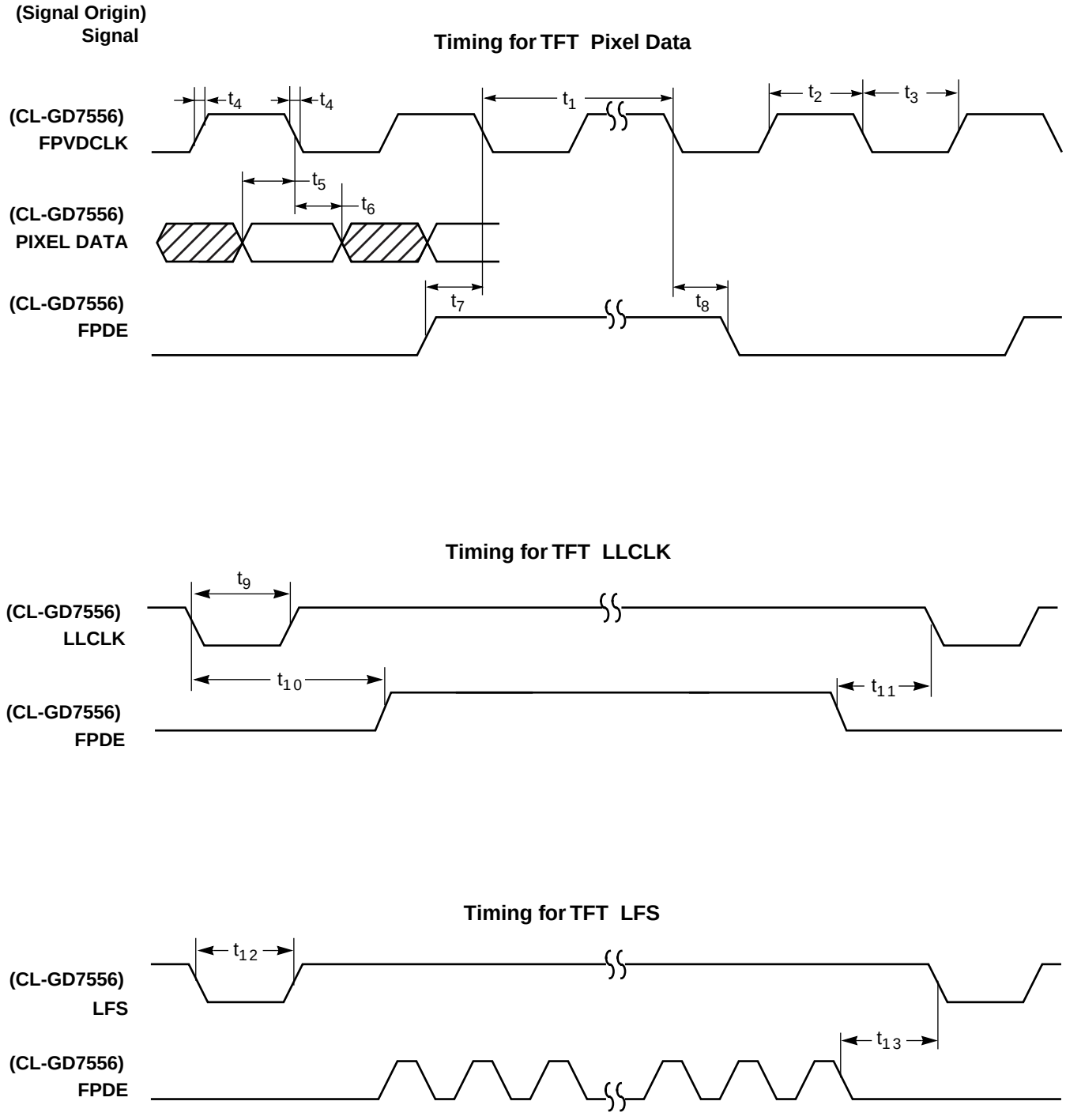


Figure 13-12. Timing Diagrams for High-Resolution Color TFT Flat Panels

Table 13-14. V-Port Timing

Symbol	Parameter	MIN	MAX	Units
t1	HREFI setup time for odd field	50		ns
t2	HREFI hold time for odd field	50		ns
t3	HREFI setup time for even field	50		ns
t4	HREFI hold time for even field	50		ns
t5	VPCLKI rise time	5	8	ns
t6	VPCLKI fall time	5	8	ns
t7	VPCLKI high pulse width	20		ns
t8	VPCLKI low pulse width	20		ns
t9	Data, VACTI setup time to VSI and VPCLKI	30		ns
t10	Data, VACTI hold time to VSI and VPCLKI	10		ns

NOTE: At 20 MHz, the maximum time for the VPCLKI period is 50 ns.

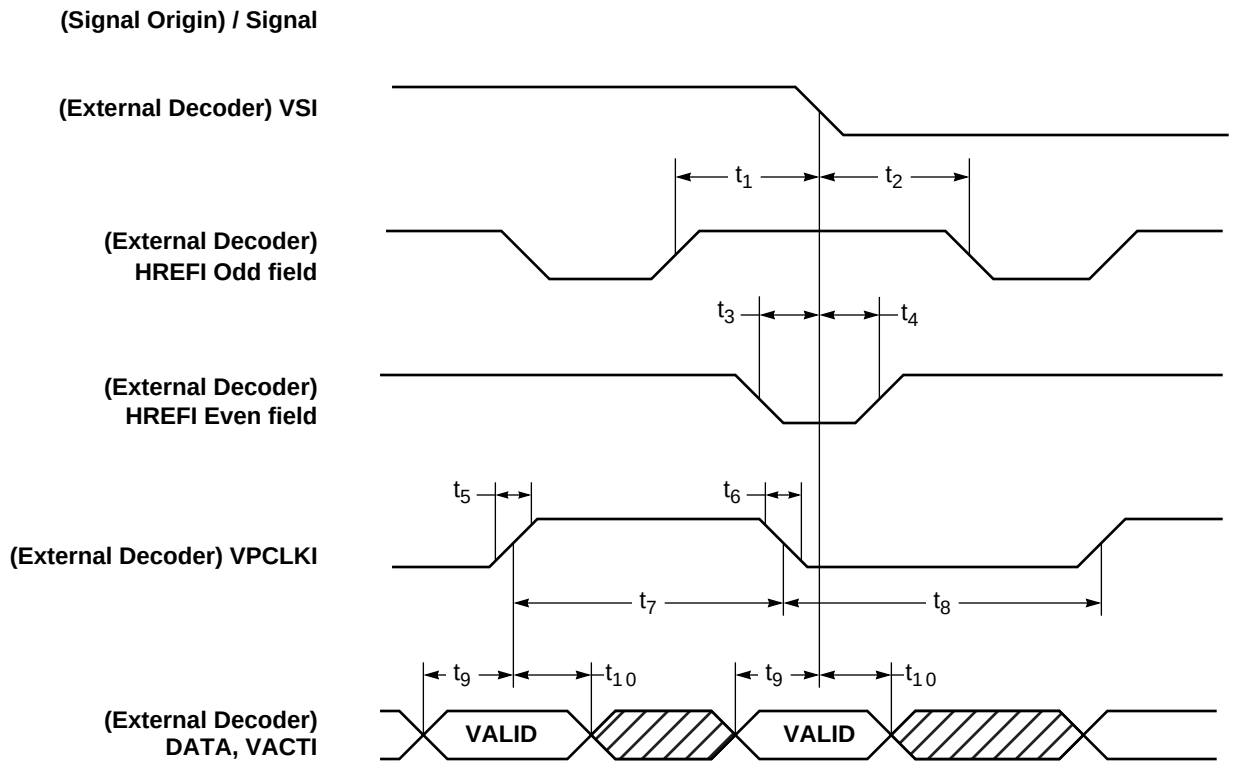


Figure 13-13. V-Port Timing Diagram

13.9 Timing Diagrams — Frequency Synthesizer Inputs

The timing diagram in this section applies to the inputs to the frequency synthesizer. The nominal frequency of the frequency synthesizer is 14.318 MHz, and the nominal period is 69.84 ns.

Table 13-15. Frequency Synthesizer (14.318 MHz) Input Timing

Symbol	Parameter	3.3 V	
		MIN	MAX
t_1	Input clock rise time	1 ns	7 ns
t_2	Input clock fall time	1 ns	7 ns
t_3	Input clock low period	$[T_{OS} / 2] – 10\% T_{OS}$	$[T_{OS} / 2] + 10\% T_{OS}$
t_4	Input clock high period	$[T_{OS} / 2] – 10\% T_{OS}$	$[T_{OS} / 2] + 10\% T_{OS}$
T_{OS}	Input clock period	69.84 ns – [0.1% of 69.84 ns] = 69.77 ns	69.84 ns +[0.1% of 69.84 ns] = 69.91 ns
V_{IH}	Input high voltage	$0.7V_{DD}$	V_{DD}
V_{IL}	Input low voltage	GND	$0.3V_{DD}$

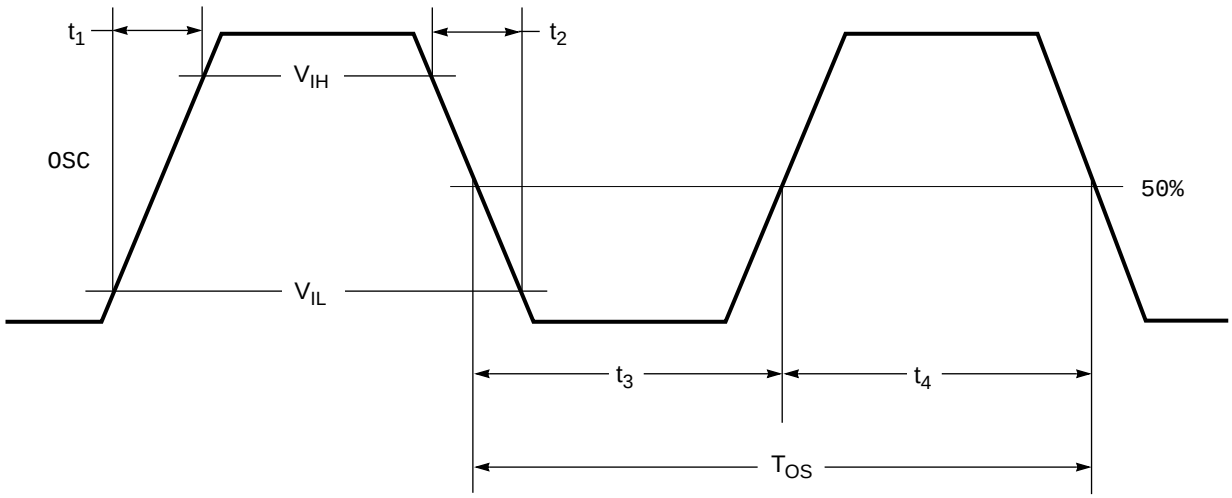
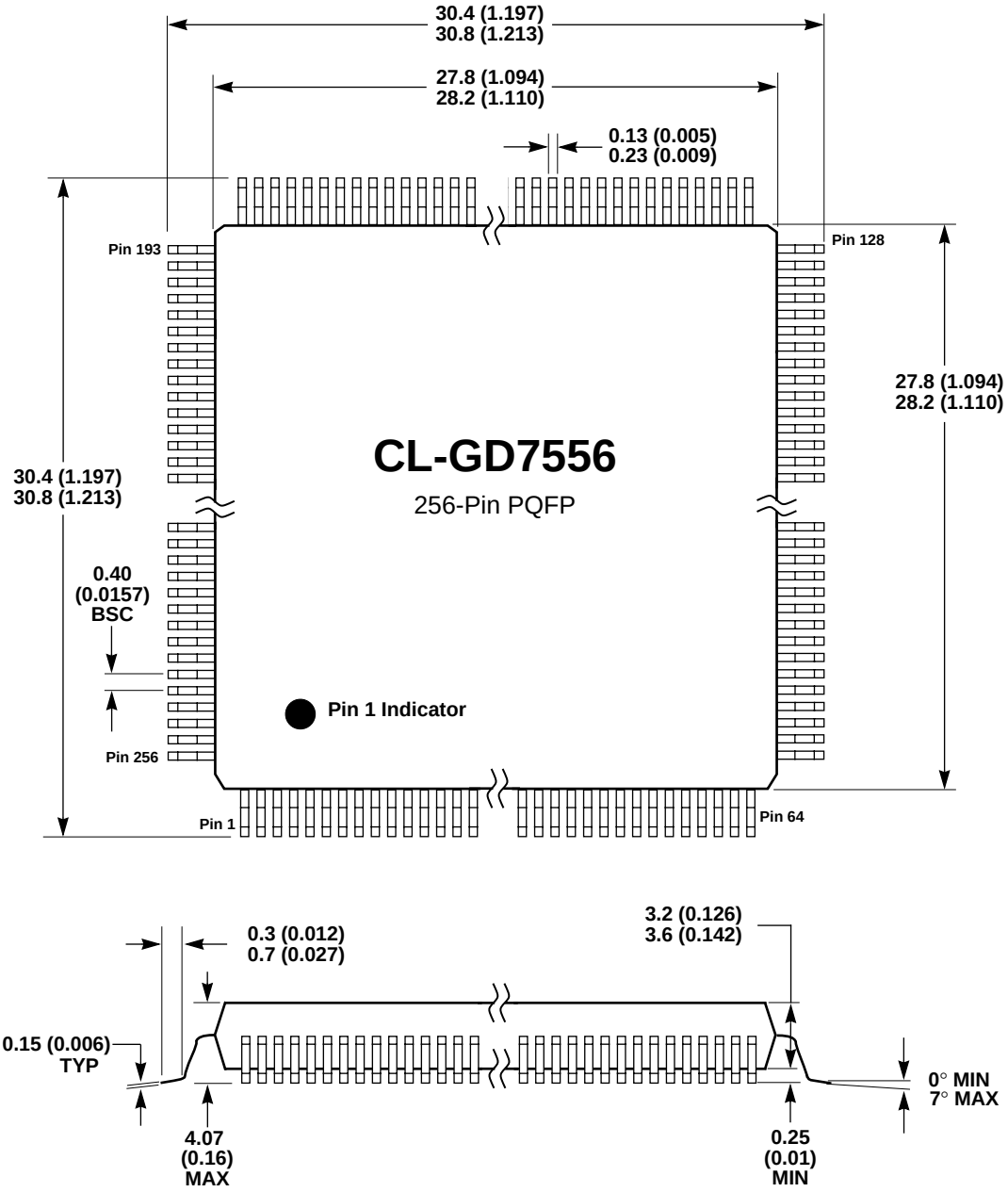


Figure 13-14. Frequency Synthesizer — Input Timing Diagram

Notes

14. PACKAGE SPECIFICATIONS

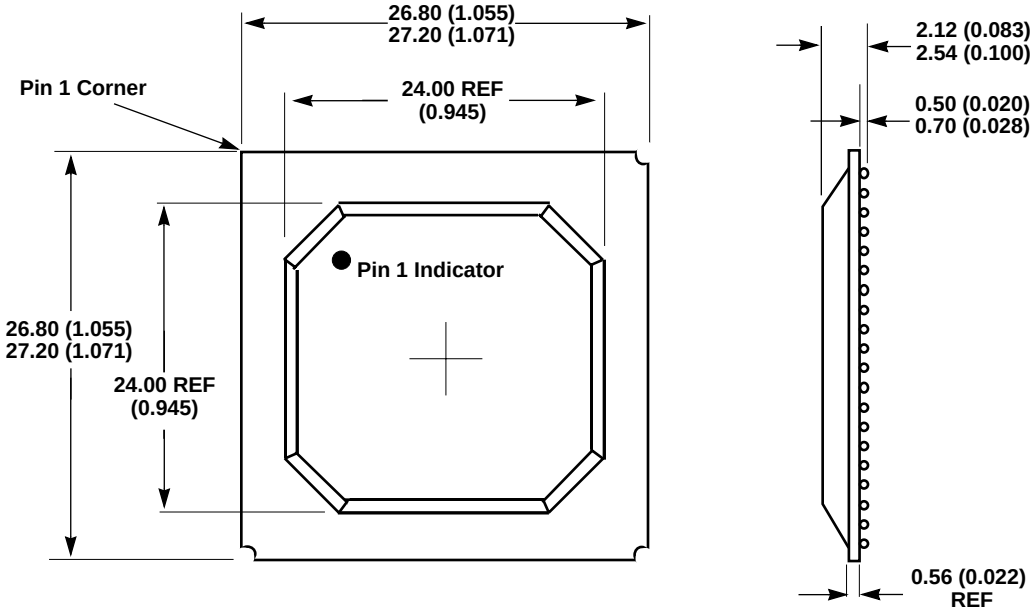
14.1 256-Pin PQFP Package Outline Drawing



NOTES:

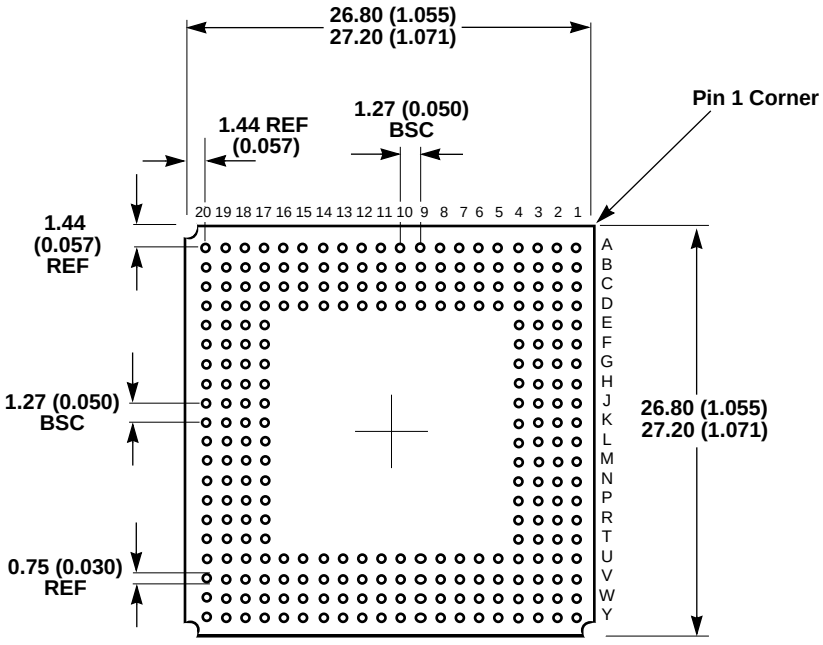
1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

14.2 256-Pin PBGA (Plastic Ball Grid Array) Package Outline Drawing



Top View

Side View



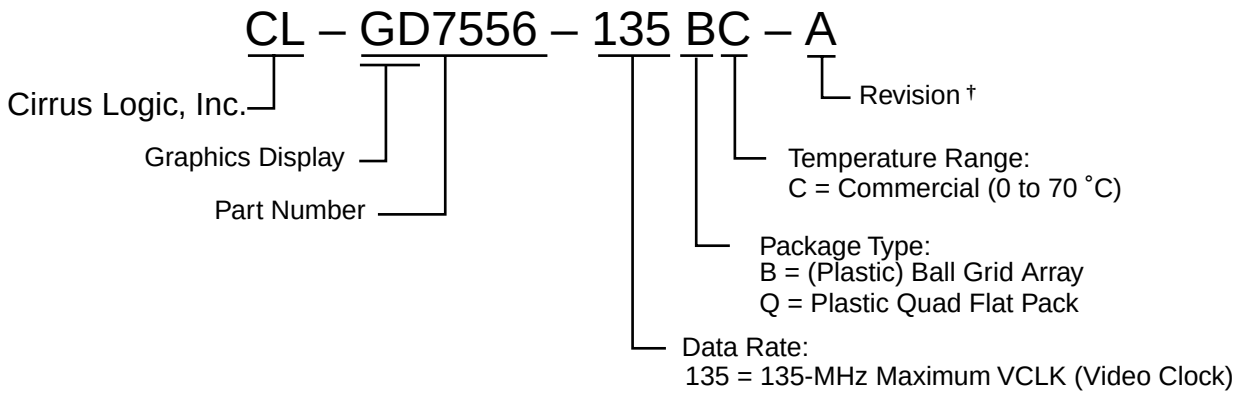
Bottom View

NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.

2) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

15. ORDERING INFORMATION EXAMPLE



† Contact Cirrus Logic for up-to-date information on revisions.

Notes

Appendix A

MEMORY CONFIGURATIONS

A.1 Introduction

The CL-GD7556 supports scalable 64-bit-wide display-memory configurations, from 1 to 2 Mbytes, using the following types of DRAMs.

- Dual-CAS# symmetric EDO (extended data-out) DRAMs
- Dual-WE# symmetric EDO DRAMs
- Dual-WE# asymmetric EDO DRAMs

A.2 Configuration and Control Register

A number of CL-GD7556 Extension registers are used to select the type of memory configuration and the required interface timing for the selected memory. Extension register SRF is shown here for reference.

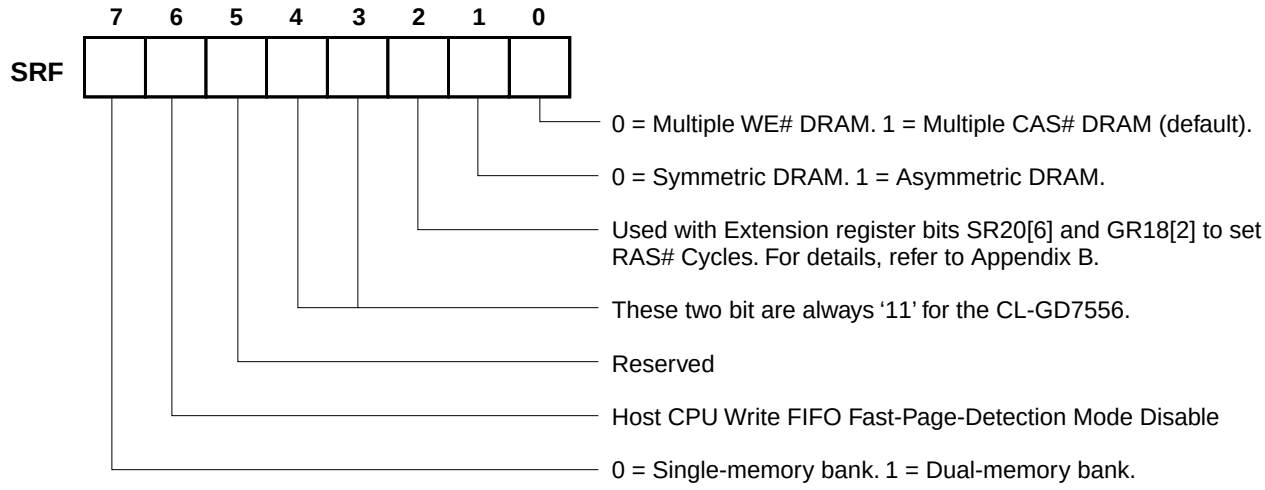


Figure A-1. Display-Memory Control Register

A.3 Possible Memory Configurations

Table A-1 shows the possible memory configurations that the CL-GD7556 supports. Because the memory bus width is always 64 bits, the CL-GD7556 can support 1 or 2 MBytes of display memory, without compromising performance. Some signals of the CL-GD7556 change functions according to the DRAM organization that is used. For optimum performance, choose multiple-CAS# configurations over multiple-WE# configurations

A number of CL-GD7556 Extension registers (such as Extension register SRF in Section 12.6) are used to select the type of memory configuration and the required interface timing for the selected memory.

Table A-1. CL-GD7556 Memory Configurations[a]

Total Display Memory Size	Memory Bus Width	DRAMs		Connection Table to Use
		Number	Type	
1 Mbyte	64 bits	2	128 Kbytes × 32	–
1 Mbyte	64 bits	4	128 Kbytes × 16	A-3
2 Mbytes[b]	64 bits	4	256 Kbytes × 16	A-2 and A-4

[a] Larger configurations with 128 Kbyte × 32 DRAMs and 128 Kbytes × 16 DRAMs are possible, but are not practical.

[b] For this configuration, Extension register SRF[7] must be cleared to 0.

A.4 Control Signals for Various Memory Configurations

The following tables indicate how the CL-GD7556 and the DRAMs must be connected.

Table A-2. 2-Mbyte Display Memory: Four 256K × 16 Dual-CAS# Symmetric DRAMs

DRAM Pins Connected to CL-GD7556 Pins	CL-GD7556 Pins Connected to the DRAM Pins			
	To DRAM #0	To DRAM #1	To DRAM #2	To DRAM #3
UCAS#	CAS1#/WE1#	CAS3#/WE3#	CAS5#/WE5#	CAS7#/WE7#
LCAS#	CAS0#/WE0#	CAS2#/WE2#	CAS4#/WE4#	CAS6#/WE6#
OE#	OE#	OE#	OE#	OE#
RAS#[a]	RAS0#	RAS0#	RAS0#	RAS0#
WE#	CAS#/WE#	CAS#/WE#	CAS#/WE#	CAS#/WE#
ADDR[8:0][a]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA[15:0]	MD[15:0]	MD[31:16]	MD[47:32]	MD[63:48]
Bit planes stored in each DRAM	3,2	1,0	3,2	1,0

[a] In this configuration, the RAS1# and MA9 pins are not used.

Table A-3. 1-Mbyte Display Memory: Four 128K × 16 Dual-CAS#, 512-Column, 256-Row DRAMs

DRAM Pins Connected to CL-GD7556 Pins	CL-GD7556 Pins Connected to the DRAM Pins			
	To DRAM #0	To DRAM #1	To DRAM #2	To DRAM #3
UCAS#	CAS1#/WE1#	CAS3#/WE3#	CAS5#/WE5#	CAS7#/WE7#
LCAS#	CAS0#/WE0#	CAS2#/WE2#	CAS4#/WE4#	CAS6#/WE6#
OE#	OE#	OE#	OE#	OE#
RAS#[a]	RAS0#	RAS0#	RAS0#	RAS0#
WE#	CAS#/WE#	CAS#/WE#	CAS#/WE#	CAS#/WE#
ADDR[8:0][a]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA[15:0]	MD[15:0]	MD[31:16]	MD[47:32]	MD[63:48]
Bit planes stored in each DRAM	3,2	1,0	3,2	1,0

[a] In this configuration, the RAS1# and MA9 pins are not used.

Table A-4. 2-Mbyte Display Memory: Four 256K × 16 Dual-WE#, Asymmetric DRAMs

DRAM Pins Connected to CL-GD7556 Pins	CL-GD7556 Pins Connected to the DRAM Pins			
	To DRAM #0	To DRAM #1	To DRAM #2	To DRAM #3
WEH#	CAS1#/WE1#	CAS3#/WE3#	CAS5#/WE5#	CAS7#/WE7#
WEL#	CAS0#/WE0#	CAS2#/WE2#	CAS4#/WE4#	CAS6#/WE6#
OE#	OE#	OE#	OE#	OE#
RAS#[a]	RAS0#	RAS0#	RAS0#	RAS0#
CAS#	CAS#/WE#	CAS#/WE#	CAS#/WE#	CAS#/WE#
ADDR[9]	MA9	MA9	MA9	MA9
ADDR[8:0	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA[15:0]	MD[15:0]	MD[31:16]	MD[47:32]	MD[63:48]
Bit planes stored in each DRAM	3,2	1,0	3,2	1,0

[a] In this configuration, the RAS1# pin is not used.

Appendix B

CLOCK OPTIONS

B.1 Introduction

The dual-frequency synthesizer in the CL-GD7556 generates all the clocks needed for the memory timing (for example, RAS# and CAS#), as well as the video clock timing. To derive these internal clock signals, an external reference clock must be provided to the OSC input of the CL-GD7556. For all calculations in this document, the external reference clock used is 14.318 MHz ± 0.01% with a duty cycle of 50 ± 10%.

B.2 MCLK (Memory Clock)

MCLK (the memory clock) is used to generate all memory timing signals (for example, RAS# and CAS#).

B.2.1 MCLK Default Frequency

The CL-GD7556 memory clock has a default frequency of 42.955 MHz. For the equation in the next section, this frequency is equivalent to 18h (24 decimal). For information regarding CL-GD7556 configuration, refer to Appendix G.

B.2.2 MCLK Programming

For higher performance, the CL-GD7556 has a programmable memory clock. The desired MCLK frequency is programmed directly into Extension register SR1F[5:0], by using the equation below. The MCLK frequency that is selected at system reset (that is, 18h) is valid until SR1F is written.

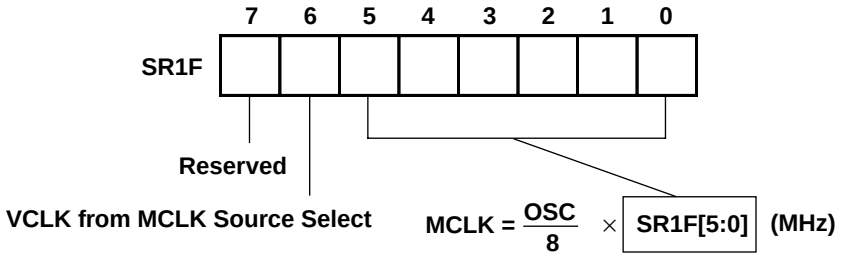


Figure B-1. Programmable Memory Clock

Examples of valid MCLK frequencies are shown in Table B-1:

Table B-1. Examples of Valid MCLK Frequencies

Extension Register SR1F[5:0] (decimal and hex)	[Reference Frequency ÷ 8] =	Desired MCLK Frequency (MHz)
21 (15h)	14.318 ÷ 8 = 1.79	37.585
23 (17h)		41.165
24 (18h, the default value at reset)		**42.955**
25 (19h)		44.744
26 (1Ah)		46.534
28 (1Ch)		50.114
31 (1Fh)		55.5
33 (21h)		59.1
37 (25h)		66.2
40 (28h)		71.6
42 (2Ah)		75.2
45 (2Dh)		80.5

B.2.3 MCLK Cycles and Selection of RAS# Cycle Length and Duty Cycle

The RAS# length and duty cycle are determined as a function of MCLK cycles as shown in the following table:

SR20[6]	GR18[2]	SRF[2]	RAS# Cycle Length	RAS# Duty Cycle
0	0	0	7 MCLKs	4 MCLKs low and 3 MCLKs high
0	0	1	6 MCLKs	3.5 MCLKs low and 2.5 MCLKs high
0	1	0	8 MCLKs	5 MCLKs low and 3 MCLKs high
1	1	0	9 MCLKs	5 MCLKs low and 4 MCLKs high

B.3 VCLK (Video Clock)

The VCLK (video clock) is the fundamental graphics/video timing clock in the system. The CRT monitor timing signals HSYNC and VSYNC, as well as the flat panel clocks, are derived from VCLK.

B.3.1 VCLK Default Source

As indicated in Table B-2, the VCLK source is determined by a number of factors. For a default VCLK, either one of four VCLKs, or MCLK, or MCLK/2 (that is, one-half the frequency of MCLK), can be used.

Table B-2. VCLK Sources and Frequencies

Extension Registers		External/General Registers		Video Clock (Defaults)	
SR1F[6]	**SR1E[0]**	**MISC[3]**	**MISC[2]**	**Source**	**Frequency (MHz)**
0	X	0	0	VCLK0	25.180
0	X	0	1	VCLK1	28.325
0	X	1	0	VCLK2	41.165
0	X	1	1	VCLK3	36.082
1	0	X	X	MCLK	42.955
1	1	X	X	MCLK/2	21.477

B.3.2 VCLK Programming

As indicated in Table B-3, the VCLK sources can be programmed with two registers each.

Table B-3. Internal VCLK Sources

Video Clock Source	Default Frequency (MHz)	Numerator			Denominator			Post-scalar
		Extension Register	Decimal	Hex	Extension Register	Decimal	Hex	
VCLK0	25.180	SRB[6:0]	102	66h	SR1B[5:1]	29	1Dh	1
VCLK1	28.325	SRC[6:0]	91	5Bh	SR1C[5:1]	23	17h	1
VCLK2	41.165	SRD[6:0]	69	45h	SR1D[5:1]	24	18h	0
VCLK3	36.082	SRE[6:0]	126	7Eh	SR1E[5:1]	25	19h	1

As shown in the equation in Figure B-2, a VCLK frequency is determined by a 7-bit numerator (N), a 5-bit denominator (D), and a 1-bit post-scalar (P).

Typically, there are a large number of combined numerator/denominator values that can program a common frequency. The choice among these combinations is made empirically. Better results can be obtained if the post-scalar is programmed to '1'.

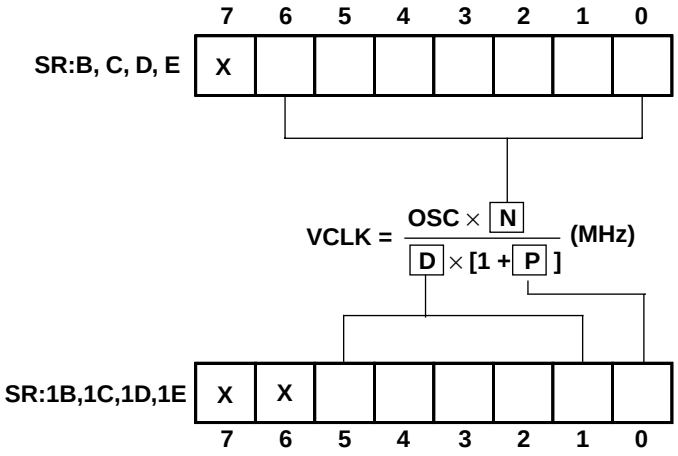


Figure B-2. Programmable Video Clock

B.4 Using MCLK as VCLK

Some graphics display modes require that MCLK and VCLK be programmed to frequencies within ≈1% of each other (or to frequencies that are nearly multiples of each other). However, in this case, MCLK and VCLK can interfere with each other. This interference can show up as 'jitter' on the display screen.

The solution is to shut down the VCLK oscillator and use MCLK (or MCLK ÷ 2) as VCLK. The Extension register settings shown in Table B-4 select MCLK (or MCLK ÷ 2) as the VCLK source.

Table B-4. Memory Clock Used as Video Clock

Graphics Display Mode	MCLK Frequency	VCLK Frequency	VCLK Source	VCLK Source Select		
				Extension Register SR1F[5:0]	Extension Register SR1F[6]	Extension Register SR1E[0]
58h at 72 Hz	50.1 MHz	50 MHz	VCLK = MCLK	1Ch	1	0
5Ch at 72 Hz	50.1 MHz	50 MHz	VCLK = MCLK	1Ch	1	0
64h at 60 Hz	50.1 MHz	25 MHz	VCLK = (MCLK ÷ 2)	1Ch	1	1
66h at 60 Hz	50.1 MHz	25 MHz	VCLK = (MCLK ÷ 2)	1Ch	1	1

Appendix C

POWER MANAGEMENT

C.1 Introduction

The CL-GD7556 has two flat panel power-management modes, Standby and Suspend. The CL-GD7556 also manages CRT monitor power consumption through DPMS (display power management signaling) support.

C.2 Intelligent Power Management

The CL-GD7556 provides several intelligent power-management features to enable the power-saving modes. For power-management VGA BIOS calls discussed in this section, refer to the Cirrus Logic "CL-GD7556 VGA BIOS External Function Specification" in the *CL-GD7556 Software Reference Manual*. Table C-1 lists dedicated CL-GD7556 pins that facilitate power management.

Table C-1. Dedicated Pins for Power Management

Pin Name	PQFP Pin No.	Pin Type	Pin Function Description	Pin Use
ACTI	63	I	Activity sense function. When the ACTI input pin is connected to another input pin, the ACTI pin can be used to sense various types of activity in order to initiate an action. A keyboard interrupt, for example, can be used to reset the internal Standby mode timer.	To use ACTI , set Extension register bit CR8D[6] to 1. Then, any low-to-high activity on the ACTI pin resets the internal Standby mode timer. When the CL-GD7556 is already in Standby mode, this activity restarts the CRT monitor clock, enables the DAC, and starts the flat panel power-up sequence.
AD[31:0]	26–35, 37–42, 67–76, 78–81, 83–84	I	Address/data pins from PCI bus. These address pins are used to reset the Standby mode timer.	When the CL-GD7556 is already in Standby mode, an access of VGA memory restarts the CRT monitor clock, enables the DAC, and starts the flat panel power-up sequence. The internal Standby mode timer is reset if any of the following occur: (1) Extension register bit CR8D[5] = 1 and there is a valid VGA memory accesses. (2) There is activity on the V-Port. (3) The Hardware Cursor registers are updated.

Table C-1. Dedicated Pins for Power Management *(cont.)*

Pin Name	PQFP Pin No.	Pin Type	Pin Function Description	Pin Use
CLK32K / SUSPST#	57	I or O	Functions for this pin include: (1) CLK32K, the 32-kHz clock input function (2) SUSPST#, the Suspend mode status output function	When Extension register CR8D[4] is: • 0 (the default), a 32-kHz refresh clock source is expected on this pin during Suspend mode. • 1, the Suspend mode status can be read on this pin, and the 32-kHz refresh clock is derived by dividing down the OSC input frequency.
CLK32K	57	I	(1) 32-kHz clock input function: This pin function is used to provide memory refresh during Suspend mode. **NOTE:** This clock must be present and stable before the CL-GD7556 is placed into Suspend mode.	When Extension register bit CR8D[4] is 0 and the CL-GD7556 is in Suspend mode: (1) The OSC input pin is disabled. (2) A 32-kHz real-time clock source must be connected to the CLK32K pin. (3) The status of the 32-kHz clock input is available on CR8A[6] as follows: 0 = No clock 1 = Active 32-kHz clock
SUSPST#	57	O	(2) Suspend mode status output function: This pin function indicates the status of Suspend mode.	When Extension register bit CR8D[4] is 1, then the pin function SUSPST# is active low whenever the CL-GD7556 is in either hardware-controlled or software-controlled Suspend mode. (1) Hardware-controlled Suspend mode is controlled by the SUSPI pin. (2) Software-controlled Suspend mode is controlled by Extension register bit CR80[2].
FPDECTL	124	O	Flat Panel Display Enable Control: This output pin is used for those flat panels that require an external display enable that is sequenced during power sequencing.	This pin is sequenced high or low automatically by the CL-GD7556 in three ways: (1) As part of normal flat panel power-up/down sequence. (2) When switching between a CRT monitor and a flat panel (3) When entering or exiting Suspend or Standby modes. The time delay between this pin and the other flat panel power and control pins is set with Extension register bits CR8C[7:6,1:0].

Table C-1. Dedicated Pins for Power Management *(cont.)*

Pin Name	PQFP Pin No.	Pin Type	Pin Function Description	Pin Use
FPVCC	125	O	Flat panel VCC: This pin is part of the flat panel power sequencing, which occurs any time the flat panel is turned on or off. This pin can be controlled with a software override bit.	To use this pin: (1) Connect the pin to the flat panel VCC control circuit. (2) This pin is sequenced high or low automatically by the CL-GD7556 in three ways: (a) As part of normal power-up/down sequence (b) When switching between a CRT monitor and a flat panel (c) When entering or exiting Suspend or Standby modes **CAUTION:** The following action is *not* recommended, as flat panel damage can result. This information is included only for reference. (3) To override normal internal controls, set Extension register CR8B[5] to 1, and toggle CR8B[4] to set FPVCC low (0) or high (1).
FPVEE	123	O	Flat panel VEE: This pin is part of the flat panel power sequencing, which occurs any time the flat panel is turned on or off. This pin can be controlled with a software override bit.	To use this pin: (1) Connect the pin to the flat panel VEE (contrast) control circuit. (2) This pin is sequenced high or low automatically by the CL-GD7556 in three ways: (a) As part of normal power-up/down sequence (b) When switching between a CRT monitor and a flat panel (c) When entering or exiting Suspend or Standby modes **CAUTION:** The following action is *not* recommended, as flat panel damage can result. This information is included only for reference. (3) To override normal internal controls, set Extension register CR8B[7] to 1, and toggle CR8B[6] to set FPVEE low (0) or high (1).

Table C-1. Dedicated Pins for Power Management *(cont.)*

Pin Name	PQFP Pin No.	Pin Type	Pin Function Description	Pin Use
SUSPI	56	I	Suspend mode input control function. (1) Hardware control Initiating Suspend mode through hardware is the most efficient power-saving mode. When the SUSPI pin is driven active: (a) The hardware-controlled Suspend mode is initiated. (b) The CRT monitor is turned off. (c) The flat panel power-down sequence is started. (d) The CL-GD7556 PCI host bus is disabled. Consequently, attempts by the CPU to access the CL-GD7556 are ignored. (2) Software control The Suspend mode can be initiated with software commands, whenever hardware-controlled Suspend mode is not active. In this mode the clocks and the PCI host bus are still active, and so the CR80[2] bit can be reset to terminate the software-controlled Suspend mode.	(1) Use the SUSPI pin for hardware-controlled Suspend mode as follows: (a) Set Extension register bit CR8D[2] to 1 to enable the SUSPI pin. (b) When the input needs to be: [1] Active-high, clear CR8D[3] to 0. [2] Active-low, set CR8D[3] to 1. (c) Connect SUSPI to an external source. (d) Depending on the setting of CR8D[3], either an active high or an active low signal on this input initiates the hardware-controlled Suspend sequence. (e) Returning this pin to its inactive level terminates the Suspend mode and starts the power-up sequence. (2) For software-controlled Suspend mode: (a) Activate software-controlled Suspend mode by setting Extension register bit CR80[2] to 1. (b) Terminate software-controlled Suspend mode by setting CR80[2] to 0.
SUSPST#	(See CLK32K / SUSPST#)			

C.2.1 CRT-Only Power Mode

During the CRT-only operation, the flat panel drive signals are all inactive, and the flat panel power-off sequence occurs automatically.

C.2.2 Normal Power Mode

In normal power mode, either the flat panel system, the CRT monitor, or both are being used. During normal power mode, the following occurs:

- The active display screen(s) receive power.
- Full-screen refresh is in effect.
- The host CPU has access to the following:
  - — Display memory
  - — RAMDAC
  - — I/O registers
- Refresh is provided to display memory.

C.2.3 Standby Mode

When the system is not being actively used, the CL-GD7556 can be set to automatically enter Standby mode by using the Standby mode timer. During Standby mode, the display screen goes blank, but application programs that are already launched continue to run normally. To restore the flat panel and/or the CRT monitor display screens, the CL-GD7556 can be programmed to terminate the Standby mode such as by pressing a key.

When the system enters Standby mode, the CRT monitor is turned off by disabling the RAMDAC output, and the flat panel is turned off using the power-down sequence. As a result, since there is no screen refresh, normal clock rates can be replaced by slower clock rates, further reducing power consumption. When the system is in Standby mode, the following occur:

- The flat panel power-down sequence occurs automatically when Standby mode is entered, and the flat panel power-up sequence occurs automatically when Standby mode is exited.
- The VCLK oscillator is stopped.
- No clock is provided to the CRT controller.
- The RAMDAC is in the low power mode.
- Display memory refresh occurs at a slower refresh rate.
- The host CPU can access and modify all registers, the display memory, and palette DAC. Depending on the status of Extension register CR8D[5], this activity can terminate the Standby mode.

C.2.3.1 Standby Mode: Initiating and Entering

The CL-GD7556 provides two methods for initiating and entering Standby mode. The software-controlled method is initiated by setting Extension register CR80[3] to 1. The hardware-controlled method is initiated by using the Standby mode timer. Both methods for initiating the Standby mode offer the features itemized above. One or more methods can be used simultaneously to initiate and/or maintain Standby mode. Standby mode is entered as follows:

1. To use software to enter the Standby mode, set CR80[3] to 1.
2. To use hardware to enter the Standby mode, as shown in Table C-2, set the timer delay with Extension register CR8B[3:0]. If the programmed timer delay is reached before the timer is reset, the Standby mode power-down sequence is started. The Standby mode timer can be reset before it times out in one of the following ways:
   a. To use activity on the ACTI input to reset the timer, set Extension register CR8D[6] to 1.
   b. To use any VGA memory access to reset the timer, set Extension register CR8D[5] to 1. If there is any activity on the V-Port or in the Extension registers for the hardware cursor, the Standby mode timer resets.

Table C-2. Standby Timer Delay Settings

CR8B[3:0] Standby Timer Control Bits				Hex Code	Actual Seconds Programmed for Delay Time (Seconds)	Approximate Corresponding Delay Time (Minutes)
[3]	[2]	[1]	[0]			
0	0	0	0	0h	Disabled	Disabled
0	0	0	1	1h	32	0.5
0	1	0	1	5h	288	4.8
0	1	1	1	7h	416	6.9
1	0	1	0	Ah	608	10.1
1	1	1	1	Fh	928	15.5

C.2.3.2 Standby Mode: Timer Reset by ACTI Function

When Extension register CR8D[6] is set to 1, it enables the ACTI input function on pin 63. When the ACTI input is enabled, a low-to-high transition on this pin is used to reset the internal Standby timer. For example, this pin can be connected to the keyboard interrupt from the system logic to periodically reset the timer.

C.2.3.3 Standby Mode: Status

The status of Standby mode can be obtained by checking Extension register CR8A[4]. When CR8A[4] = 1, the CL-GD7556 is in Standby mode.

C.2.3.4 Standby Mode: Terminating and Exiting

The flat panel power-up sequence occurs automatically when Standby mode is terminated and exited (that is, when any of the conditions for initiating Standby mode are removed as described below).

- Terminate software-controlled Standby mode by clearing CR80[3] to 0.
- Terminate hardware-controlled Standby mode by resetting the Standby mode timer, using either the ACTI pin or a VGA memory access.
  - — To use activity on the ACTI input to reset the timer, set CR8D[6] to 1.
  - — To use any VGA memory access to reset the timer, set CR8D[5] to 1.

When there is a request to terminate the Standby mode while a power-up or power-down sequence is in progress, the power-up/down sequence is allowed to complete before the new request is initiated.

C.2.4 Suspend Mode

The CL-GD7556 Suspend mode is used to save power when the system is not being actively used for a long period of time. The Suspend mode can be initiated either with a hardware input or through software.

C.2.4.1 Suspend Mode: Hardware-Controlled

Hardware-controlled Suspend mode, which provides the most efficient means of power saving, is initiated by using the SUSPI pin. When the system enters hardware-controlled Suspend mode, the following occur:

- The flat panel power-down sequence occurs automatically when Suspend mode is entered, and the flat panel power-up sequence occurs automatically when Suspend mode is exited.
- The VCLK and MCLK oscillators automatically shut off when the Suspend sequence occurs.
- No host CPU access is allowed to the CL-GD7556.
- Although display memory cannot be accessed by the host CPU during Suspend mode, the contents are preserved. (This action is useful when a system remains inactive for a relatively long time.)
- Register data contents are retained so that the environment can be rebuilt when Suspend mode terminates.

Unless DRAMs are self-refresh, the CL-GD7556 internal refresh clock for display memory is set to 32 kHz. In this mode, the input pads are shut off and the bus interface does not receive power. Except for the dedicated SUSPI input pin, all input pins are de-activated. Also, except for the SUSPST# output pin (which reflects the state of the Suspend mode), all output pins are forced low, further reducing power consumption. Additional power is saved by denying host CPU access to display memory. Also, if selected, a slower 32-kHz clock refreshes the display memory by performing CAS#-before-RAS# refresh. This slow clock input, which is recommended for maximum power savings, comes from one of two sources:

- By setting Extension register CR8D[4] to 1, a 32-kHz clock output results from dividing the 14.318-MHz clock by 432.
- By clearing Extension register CR8D[4] to 0, the CL-GD7556 is set up for an external 32-kHz clock input. This input must be provided through the CLK32K input, and the 14.318-MHz input is disabled to save power.

The display memory refresh rate must be set by programming CR8D[1:0] as shown in Table C-3.

Table C-3. Suspend Mode Display Memory Refresh Selection

CR8D		Suspend Mode Display Memory Refresh Type
[1]	[0]	
0	0	Refresh cycle is 8 ms, CAS#-before-RAS# (Default)
0	1	Refresh cycle is 64 ms, CAS#-before-RAS#
1	0	Self-refresh. CAS# and RAS# are driven low
1	1	No refresh. All clock inputs are disabled, and display memory outputs are high-impedance. (This setting is only for test purposes.)

C.2.4.2 Suspend Mode: Software-Controlled

Software-controlled Suspend mode is initiated by setting Extension register CR80[2] to 1.

NOTE: In contrast to the hardware-controlled Suspend mode, software-controlled Suspend mode allows the host CPU to access all internal registers, which requires an active clock and I/O capability, and therefore more power. As a result, this mode is not recommended.

C.2.4.3 Suspend Mode: Initiating and Entering

Hardware-controlled Suspend mode is recommended, in order to minimize power consumption. To enable hardware-controlled Suspend mode, set Extension register CR8D[2] to 1 . When SUSPI input is driven active (high or low, depending on CR8D[3]), the Suspend mode is initiated. The polarity of the SUSPI input is controlled by CR8D[3]:

- When Extension register CR8D[3] = 0, SUSPI is active high
- When Extension register CR8D[3] = 1, SUSPI becomes SUSPI# (that is, active low)

Software-controlled Suspend mode is entered by setting CR80[2] to 1. In this mode, host CPU access to registers is still active, so that CR80[2] can be reset to terminate the Suspend mode.

C.2.4.4 Suspend Mode: Sequence

The typical Suspend mode sequence is as follows:

1. The system receives a request to suspend.
2. The system interrupts the application. The interrupt routine calls the VGA BIOS Suspend routine. The VGA BIOS Suspend routine waits until all host CPU cycles already in the CPU write buffer are executed.

   A host CPU read verifies that the host CPU write buffer is empty. When the host CPU read is done, the host CPU write buffer is empty. If a BitBLT operation is in progress, it suspends automatically at the first memory refresh cycle. After resuming, the BitBLT operation continues from the point of operation that it was suspended.

   The Suspend mode can be initiated while the host CPU write FIFO contains host CPU write cycles waiting to be executed. However, the Suspend mode must not be initiated while the RDY# signal is high and waiting for the completion of a cycle. To prohibit this action from occurring, the Suspend routine executes and then waits for the completion of a host CPU read, but only if there are no BitBLT operations in progress. If a BitBLT operation is in progress, the Suspend routine skips to the next step in the Suspend sequence without waiting for the RDY# pin to turn off.
3. Set the SUSPI pin high. Using OEMSI (the OEM BIOS customizing utility provided by Cirrus Logic in the BIOS Development kit), the VGA BIOS must be customized for the I/O location of the SUSPI pin control. [Note that the SUSPI pin is to be controlled by a spare I/O port (that is, a 1-bit output port) on the motherboard.]
4. The SUSPST# output is set low.
5. At the end of the first memory refresh cycles (1, 3, or 5 CAS#-before-RAS# refreshes):
   a. The display memory control is switched to 32-kHz refresh cycles. No other memory cycle types can execute.
   b. Pad control is forced to Suspend mode and host CPU inputs are disabled.
6. After the SUSPI pin is set high and after the interval programmed by Extension register CR8C, the CL-GD7556 executes flat panel power-down sequencing. This sequencing requires approximately 150 ms to complete.
7. The CL-GD7556 stops VCLK and MCLK.
8. If DRAMs are self-refresh and Extension register CR8D[1:0] is set to ‘10’, the 32-kHz clock can now be stopped and the system can be powered down.

C.2.4.5 Suspend Mode: Status

Suspend mode status can be obtained by checking the SUSPST# output pin. SUSPST#, a multifunction pin, is active when Extension register CR8D[4] = 1. When the CL-GD7556 is in Suspend mode, SUSPST# is set low from the time the clocks are stopped until 32 µs after the clocks are restarted.

C.2.4.6 Suspend Mode: Terminating and Exiting

The Suspend mode must be terminated/exited in the same manner in which it was entered.

- When the SUSPI input pin is driven inactive (low or high, depending on CR8D[3]), Suspend mode is terminated.
- In software, Suspend mode is terminated by setting CR80[2] to 0.

When Suspend mode is terminated, the system returns to the same operational state it was in before Suspend mode was entered. The typical Resume sequence is as follows:

1. The system starts the 32-kHz clock.
2. The Resume VGA BIOS call is executed, which sets SUSPI low. SUSPST# remains low.
3. The clock synthesizers start after 60 µs. To ensure a stable signal before the next step in the sequence is executed, allow 64 ms to elapse.
4. The host CPU pins are returned to their operational state after the last slow-refresh cycle is done or after the self-refresh end sequence is completed. Memory control is then passed onto the memory clock. Using the memory clock is the standard method for driving the display memory.
5. After the interval programmed by Extension register CR8C, the flat panel VDD is on and all I/O registers are restored.
6. The flat panel pads are enabled after another interval programmed by Extension register CR8C.
7. After another interval programmed by Extension register CR8C, the flat panel backlight and bias are enabled and the system is fully resumed.

C.3 Techniques for Reducing Power Consumption

C.3.1 Power Reduction in Suspend Mode

In a CMOS device such as the CL-GD7556, power is consumed whenever inputs cross CMOS thresholds. Since the host CPU address/data buses are inputs to the CL-GD7556, the following alternatives are available to reduce power when the system is in Suspend mode.

- Use the hardware-controlled Suspend mode instead of software-controlled Suspend mode. In hardware-controlled Suspend mode, the host CPU access to the CL-GD7556 is disabled. Software-controlled Suspend mode requires the clocks and host CPU bus to be active and therefore dissipates more power.
- Hold the buses quiescent (that is, program them either to 0 or 1 instead of letting them float). As a result, inputs do not cross CMOS thresholds and power is not consumed.
- If the host CPU processor allows, shut down the host CPU I/O ports and stop the host CPU clock that is connected to the CL-GD7556 CLK pin.
- A 32-kHz oscillator input can be supplied to the CLK32K input pin 57 (U3), in which case the 14.318-MHz clock pin 54 (T2) must be turned off.
- To reduce the power used by the display-memory interface, use low-power CMOS DRAM(s). When CMOS DRAMs are not being accessed, they do not draw significant current and are effectively powered-down. Self-refresh DRAMs can be used to further reduce power consumption.

C.3.2 Complete Power-Down of the Graphics Controller

The CL-GD7556 can support system implementations where the VGA subsystem is powered off, providing maximum power savings. The critical task for the CL-GD7556 is to properly execute flat panel power-down sequencing before shutting off power. Software tasks are the most critical because the VGA controller register states and the contents of display memory must be saved to a system-specified location and then properly restored upon power-up to the graphics subsystem.

The CL-GD7556 VGA BIOS has Save/Restore functions for the contents of the standard VGA registers and the Extension registers. Cirrus Logic also has sample code for programs that save the contents of display memory. Both the VGA BIOS and the Save/Restore code are necessary to support the Save/Restore function. Cirrus Logic can provide source code that demonstrates Save/Restore functionality for both display memory and registers, allowing the system designer to ensure proper operation of this implementation.

C.4 Green Computing (Power Saving for CRT Monitor)

The CL-GD7556 features comprehensive PC power-management functions that support compliance with the United States Environmental Protection Agency's Energy Star Computer Program.

C.4.1 Display Power Management Signaling (DPMS)

The greatest power savings can be obtained by putting the CRT monitor into a low-power mode, which requires that the CRT monitor respond to DPMS (Display Power Management Signaling).

The VESA (Video Electronics Standards Association) DPMS Proposal defines four levels of display power. Through Extension register bits GRE[2:1], the CL-GD7556 can support each of these four levels. The CL-GD7556 DPMS modes can operate independently of the flat panel power modes that the CL-GD7556 supports.

The only time the CL-GD7556 power management mode is directly tied to the DPMS register setting of GRE[2:1] is in timer-initiated Standby mode. Because this mode is a hardware-controlled timer-driven mode, there is no opportunity for the VGA BIOS to program any of the CL-GD7556 registers. As a result, when the CL-GD7556 is in the timer-initiated Standby mode, the CRT monitor is internally forced into the DPMS Standby mode (that is, the CRT monitor VSYNC signal is automatically provided with a 62.5 Hz clock and HSYNC is inactive) and the CL-GD7556 disregards any value in GRE[2:1].

Table C-4 shows the CL-GD7556 Extension register GRE[2:1] values, the resultant DPMS states, the required compliance for the DPMS states, and the activity that takes place in various DPMS states.

Table C-4. CL-GD7556 DPMS Register Programming

Extension Register GRE		DPMS State	DPMS Compliance	Activity in Various DPMS States			
[2]	[1]			VSYNC Activity	HSYNC Activity	DAC Power State	Recovery Time for CRT Monitor
0	0	ON = Full operation	Mandatory	Active	Active	On	N/A
0	1	STANDBY= Operating state of minimal power reduction	Optional	62.5 Hz	Inactive	Off	Short
1	0	SUSPEND= Significant reduction of power consumption	Mandatory	Inactive	32 kHz	Off	Long
1	1	OFF= Lowest level of power consumption	Mandatory	Inactive	Inactive	Off	System-dependent

NOTES:

1) If the CL-GD7556 is in hardware-controlled Standby mode, then the DPMS state is also Standby mode.

2) If the CL-GD7556 is in hardware-controlled Suspend mode, then the DPMS state is also Suspend mode.

C.4.2 CRT Monitor Static HSYNC and VSYNC Signals

HSYNC is inactive if Extension register GRE[1] is programmed to a '1', and the polarity sense is as programmed into MISC[6]. VSYNC is inactive if GRE[2] is programmed to a '1', and the sense is as programmed into MISC[7].

If either GRE[1] or GRE[2] is programmed to a '1', the DAC is powered down. This action satisfies the requirement in the VESA proposal which states that the "...host system sets the video image information to the blank level prior to the host transmitting the Standby/Suspend/Off signal to the display". This action significantly reduces the power used by the CL-GD7556.

C.4.3 Optimizing Use of DPMS and Controller Power Management Modes

When the CL-GD7556 is in CRT-only mode and the CRT monitor is in DPMS Standby or Suspend mode, power consumption can be minimized by having the VGA BIOS reduce the video clock and the memory clock frequencies. Similarly, to ensure there is no power to the CRT monitor, the VGA BIOS must set DPMS to 'Off' when the CL-GD7556 is in flat panel-only mode.

Prior to initiating the CL-GD7556 Suspend mode, the VGA BIOS can program GRE[2:1] to any of the DPMS power-save states (that is, Standby, Suspend, or Off). The 32-kHz input that the CL-GD7556 uses for display memory refresh while in the Suspend mode can also be used as the synchronization pulse required, when DPMS Standby or Suspend mode is requested. This action allows a system designer the flexibility to select the CRT monitor recovery time desired when resuming from the CL-GD7556 Suspend state. Even in the case of hardware-initiated Suspend mode, it is assumed that some time period is allocated for system housekeeping before Suspend mode is actually initiated, which allows DPMS programming to occur.

C.5 VESA VBE/PM BIOS Functions

The CL-GD7556 is fully compliant with the VESA display power management VGA BIOS extensions, VBE/PM Version 1.0. The following sections describe these calls.

C.5.1 Report VBE/PM Capabilities

Input:
- AH = 4Fh VESA Extension
- AL = 10h VBE/PM Services
- BL = 00h Report VBE/PM Capabilities
- ES:DI Null pointer, which must be 0000:0000h. Reserved for future use

Output:
- AX = Status
- BH = Power-saving state supported by the CL-GD7556. (Refer to Note 1.)
  - 0 = Power-saving state is not supported.
  - 1 = Power-saving state is supported.
    - 00h Power is on
    - 01h Standby mode
    - 02h Suspend mode
    - 04h Power is off
    - 08h Reduced on. Intended for flat panels. (Refer to Note 2.)

NOTES:

1) In some instances, an attached display device cannot support all power states that can be controlled by the CL-GD7556. It is the responsibility of the power-management program to implement the power-saving states that are offered by the CL-GD7556. When the CL-GD7556 has a means of determining which power-saving state is implemented in the attached display device, the function previously discussed reports the power-saving states that are supported by both the CL-GD7556 and the display device.
2) The option 'REDUCED ON' is not defined in VBE/PM Version 1.0 and is not implemented.

C.5.2 Set Display Device Power State

Input:
- AH = 4Fh VESA Extension
- AL = 10h VBE/PM Services
- BL = 01h Set Display Device Power State
- BH = Display device power state currently requested by the CL-GD7556
  - 00h Power is on
  - 01h Standby mode
  - 02h Suspend mode
  - 04h Power is off
  - 08h Reduced on. Intended for flat panels.

Output:
- AX = Status: If the requested display device power state is not available, this function returns AX = 014Fh, indicating that the function is supported, but that the call failed. In this case, the BH register and Display Device Power State are left unchanged.
- BH = Unchanged

C.5.3 Get Display Power State

Input:	AH = 4Fh	VESA Extension
	AL = 10h	VBE/PM Services
	BL = 02h	Get Display Device Power State
Output:	AX =	Status: If this function is not supported by the CL-GD7556 hardware, AX = 014Fh must be returned in the status.
	BH =	Display Device Power state currently requested by the CL-GD7556
		00h Power is on
		01h Standby mode
		02h Suspend mode
		04h Power is off
		08h Reduced on. Intended for flat panels.

Appendix D

SIGNATURE GENERATOR

D.1 Introduction

To automatically test the CL-GD7556 video-output logic at full speed, the CL-GD7556 has SG (signature generator) logic. With this feature, it is possible to capture a unique 16-bit signature for any given setup of a graphics display mode and display memory data.

When there is an error in the display memory interface, control logic, or pixel-data manipulation, a different signature is produced that can be compared to a known good signature value obtained from the same image. This comparison allows a test technician to quickly and accurately test a display screen without having to visually inspect the display screen for errors. This method is used extensively in the Cirrus Logic Manufacturing Test.

D.2 Signature Generator Test

To run the SG, bits must be written in Extension register SR18 (the Signature Generator Control register) to initialize and arm the SG. A status bit, SR18[0], reflects that the SG is running. When the Status bit changes state to 'not running', the signature may be read from Extension registers SR19 and SR1A.

NOTE: The signature is a function of the displayed pixels, not the display data. If the display screen includes blinking attributes or a blinking cursor, then the signature is different for those frames in which the pixel is blinked off, compared to those frames in which the pixel is blinked on.

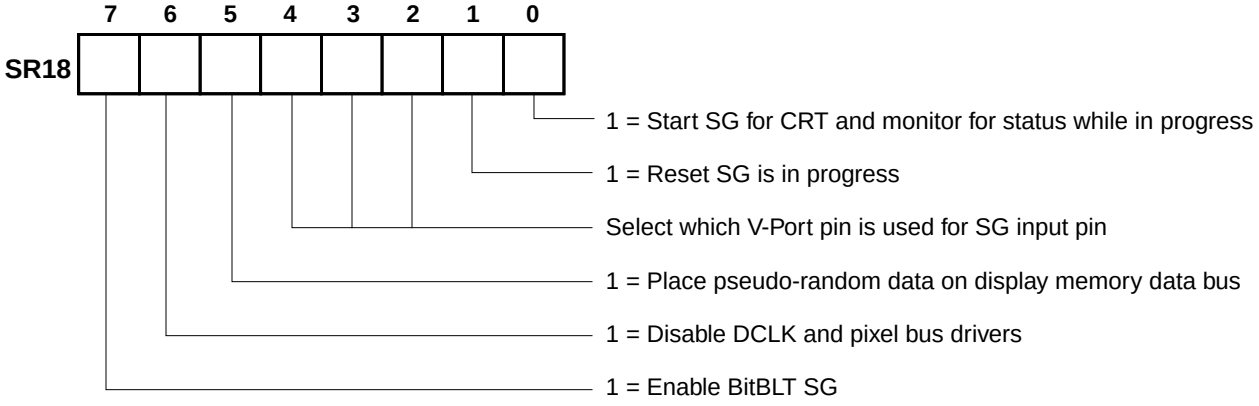


Figure D-1. Signature Generator Control Register

D.3 Signature Generator Control Register Definition

The Signature Generator Control register definitions are as follows:

Table D-1. SR18 Signature Generator Control Register Definitions

SR18 Bit	SR18 Bit Function
SR18[7]	BitBLT Signature Generator Control. 0 = Disable BitBLT Signature Generator 1 = Enable BitBLT Signature Generator
SR18[6]	This bit does not affect the Signature Generator.
SR18[5]	Signature Generator Display Memory Data Enable. 0 = Normal operation 1 = Pseudo-random data placed on the display memory data bus
SR18[4:2]	Signature Generator Input from the V-Port Bus. These bits select one of the 8 VPY inputs to use as the SG input pin: ‘111’ = VPY7 ‘110’ = VPY6 ‘101’ = VPY5 ‘100’ = VPY4 ‘011’ = VPY3 ‘010’ = VPY2 ‘001’ = VPY1 ‘000’ = VPY0
SR18[1]	Signature Generator Reset. 0 = Allow the Signature Generator to operate under the control of SR18[0] 1 = Reset the Signature Generator operation in progress
SR18[0]	Signature Generator Enable / Status. 1 = Signature Generator operation starts generating signature on next VSYNC (write) 0 = Signature Generator operation is finished and signature data is ready (read) **NOTE:** SR18[0] must be set to 1 to start the SG. SR18[0] is cleared to 0 when the SG is done.

The SG low-byte and high-byte results are read from Extension registers SR19 and SR1A, respectively.

- SR19[7:0]: These bits are the low byte of the 16-bit SG result from one frame of signature data.
- SR1A[7:0]: These bits are the high byte of the 16-bit SG result from one frame of signature data.

D.4 Signature Generator Sample Code

The following 'C' sample code describes how a programmer captures eight signatures for any given display screen. This sample assumes that the display screen is already being displayed and that in text display modes, no blinking attributes are being displayed.

```
signature_capture ()           /* Capture eight signatures for any given mode */
 {
 unsigned int result,i,SR19,SR1A;
 int SIG [8];
 union REGS in;

 in.x.ax = 0x0100;             /* Shut off the cursor, if in text display mode */
 in.x.cx = 0x2000;
 int86x (0x10,&in,&out,&seg);
 outp (0x3c4,6);               /* Unlock Extension registers */

 for (i = 0;i <= 7; i++) {     /* Cycle through all pixel data bits */
    outp (0x3c4,0x18);                    /* Arm SG and set for pixel data bit */
    outp (0x3c5, (2 | (i<<2)));           /* Reset */
    outp (0x3c5, (i << 2));               /* Select the data bit */
    outp (0x3c4,0x18);
    outp (0x3c5, (1 | (i << 2)));         /* and start the SG */
    result = inp (0x3c5);                 /* Pre-read SG status */
    while ((result & 0x01) != 0) {        /* Wait until signature is done */
        outp (0x3c4,0x18);
        result = inp (0x3c5);             /* Read the status */
    }
    outp (0x3c4,0x19);                    /* Get signature low byte */
    SR19 = inp (0x3c5);
    outp (0x3c4,0x1A);                    /* Get signature high byte */
    SR1A = inp (0x3c5);
    SIG [i] = (SR1A << 8) + SR19;
 }                                        /* End of for */
 }
```

Notes

Appendix E

PIN-SCAN TESTING

E.1 Introduction

Pin-scan testing automatically verifies if CL-GD7556 pins have been properly soldered to a circuit board. This test detects pins that either are not connected to the board or are shorted to a neighboring pin or trace. When using the CL-GD7556 Pin-Scan Test mode, a circuit board tester is required. The frequency of the tester must be lower than 100 kHz.

Pin-Scan Test Advantages

The advantages of pin-scan testing are:

- Simple test patterns can verify full-board connectivity.
- During the test, the pins are automatically connected sequentially in a single chain around the CL-GD7556 so that the value on each output pin depends on the values applied to all input pins, rather than on the internal state of the CL-GD7556.
- The pin-scan logic is strictly combinatorial so that no clock pulses are required.

E.2 Pin-Scan Test Performance

The pin-scan test is performed as follows:

1. To enter the Pin-Scan Test mode, 60-kΩ pull-up resistors are needed on both the MD33/TMPU pin 218 (B12) and MD27/SCANPU pin 238 (B7).
2. As shown in Figure E-1, drive RST# low at least 20 ns while TWR# pin 119 is low. Then, drive RST# high to keep Extension register bit SR22[0] equal to '1'.
3. Drive all the input pins to '0'.
4. Verify that the values on the output pins match the predicted values shown in the fifth column of Table E-1.
5. On subsequent test cycles, individually drive each input pin to a '1', and verify that all the affected output pins change to the predicted values shown in the fourth column of Table E-1. In the table, pin numbers are listed according to the pin-scan order, with MD18 pin 3 (C1) as the first input and OE# pin 255 (A1) as the last output.

   NOTE: Pin names in Table E-1 are given for both of the CL-GD7556 packages: the PQFP (Plastic Quad Flat Pack) and the PBGA (Plastic Ball Grid Array).

6. To exit the Pin-Scan Test mode, drive RST# from low to high while TWR# is high, as shown in Figure E-1.

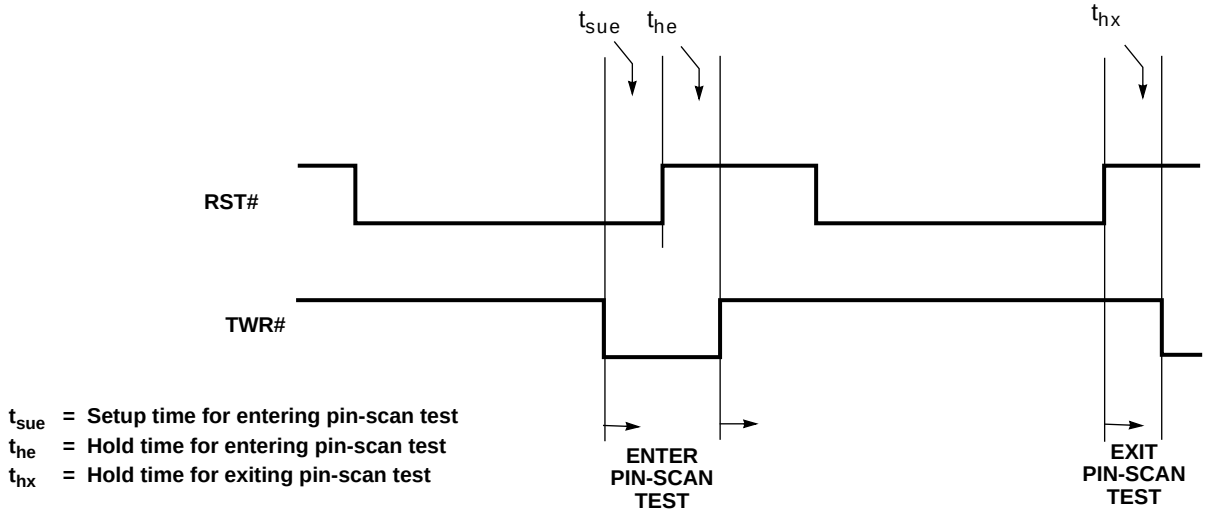


Figure E-1. Entering and Exiting the Pin-Scan Test Mode

E.3 Pin-Scan Test: Pins Not Tested

Pins that are not tested in the pin-scan test are in the list that follows:

- All power pins
- All ground pins
- RST# pin
- TWR# pin
- RED, GREEN, and BLUE pins
- IREF and VREF pins

E.4 Pin-Scan Test Results

During the test, when the value applied to an input pin is changed but:

- *None* of the affected output pins change to the correct logic level in response, then the input pin is either shorted or not soldered correctly.
- *One (or some)* of the affected output pins do not change to the correct logic level in response, then the output pin is either shorted or not soldered correctly.

Table E-1. Pin-Scan Order

PQFP Pin No.	PBGA Ball No.	CL-GD7556 Pin Names	In/ Out	If all inputs = '0', predicted value of this pin is:	If one input = '1', predicted value of this pin is:
3	C1	MD18 / ROMA10	In	0	1
4	C2	MD17 / ROMA9	In	0	1
5	C3	MD16 / ROMA8	In	0	1
6	D3	MD15 / ROMA7	In	0	1
7	D1	MD14 / ROMA6	In	0	1
9	E3	MD13 / ROMA5	In	0	1
10	E2	MD12 / ROMA4	In	0	1
11	E1	MD11 / ROMA3	In	0	1
12	E4	MD10 / ROMA2	In	0	1
13	F3	MD9 / ROMA1	In	0	1
14	F2	MD8 / ROMA0	In	0	1
15	F1	CAS1# / WE1#	In	0	1
16	F4	CAS0# / WE0#	In	0	1
17	G3	MD7 / ROMD7	In	0	1
18	G2	MD6 / ROMD6	In	0	1
19	G1	MD5 / ROMD5	In	0	1
20	G4	MD4 / ROMD4	In	0	1
21	H3	MD3 / ROMD3	In	0	1
22	H2	MD2 / ROMD2	In	0	1
23	H1	MD1 / ROMD1	In	0	1
24	H4	MD0 / ROMD0	In	0	1
26	J2	AD31	In	0	1
27	J1	AD30	In	0	1
28	J4	AD29	In	0	1
29	K3	AD28	In	0	1
30	K2	AD27	In	0	1
31	K1	AD26	In	0	1
32	K4	AD25	In	0	1
33	L3	AD24	In	0	1
34	L2	AD25	In	0	1
35	L1	AD22	In	0	1

Table E-1. Pin-Scan Order *(cont.)*

PQFP Pin No.	PBGA Ball No.	CL-GD7556 Pin Names	In/ Out	If all inputs = '0', predicted value of this pin is:	If one input = '1', predicted value of this pin is:
37	M3	AD21	In	0	1
38	M2	AD20	In	0	1
39	M1	AD19	In	0	1
40	M4	AD18	In	0	1
41	N3	AD17	In	0	1
42	N2	AD16	In	0	1
43	N1	INTR#	Out	1	0
45	P3	STOP#	In	0	1
46	P2	PAR	In	0	1
47	P1	DEVSEL#	Out	1	0
48	P4	TRDY#	Out	0	1
50	R2	CLK	In	0	1
51	R1	IRDY#	In	0	1
52	R4	FRAME#	In	0	1
53	T3	IDSEL	In	0	1
54	T2	OSC / XVCLK	In	0	1
56	T4	SUSPI	In	0	1
57	U3	CLK32K / SUSPT#	In	0	1
58	U2	C/BE3#	In	0	1
59	U1	C/BE2#	In	0	1
60	U4	C/BE1#	In	0	1
61	V2	C/BE0#	In	0	1
63	Y1	ACTI	In	0	1
67	Y3	AD15	In	0	1
68	W3	AD14	In	0	1
69	V3	AD13	In	0	1
70	V4	AD12	In	0	1
71	Y4	AD11	In	0	1
72	W4	AD10	In	0	1
73	V5	AD9	In	0	1
74	W5	AD8	In	0	1

Table E-1. Pin-Scan Order *(cont.)*

PQFP Pin No.	PBGA Ball No.	CL-GD7556 Pin Names	In/ Out	If all inputs = '0', predicted value of this pin is:	If one input = '1', predicted value of this pin is:
75	Y5	AD7	In	0	1
76	U5	AD6	In	0	1
78	W6	AD5	In	0	1
79	Y6	AD4	In	0	1
80	U6	AD3	In	0	1
81	V7	AD2	In	0	1
83	Y7	AD1	In	0	1
84	U7	AD0	In	0	1
86	W8	VPC0	In	0	1
87	Y8	VPC1	In	0	1
88	U8	VPC2	In	0	1
89	V8	VPC3	In	0	1
90	W9	VPC4	In	0	1
91	Y9	VPC5	In	0	1
92	U9	VPC6	In	0	1
93	V10	VPC7	In	0	1
94	W10	VPY0	In	0	1
95	Y10	VPY1	In	0	1
96	U10	VPY2	In	0	1
97	V11	VPY3	In	0	1
98	W11	DDCC / VCLKO	In	0	1
100	U11	VPY4	In	0	1
101	V12	VPY5	In	0	1
102	W12	VPY6	In	0	1
103	Y12	VPY7	In	0	1
104	U12	DDCD	In	0	1
106	W13	HREFI	In	0	1
108	U13	VACTI	In	0	1
110	W14	VSI	In	0	1
111	Y14	VPCLKI	In	0	1
112	U14	HSYNC	In	0	1

Table E-1. Pin-Scan Order *(cont.)*

PQFP Pin No.	PBGA Ball No.	CL-GD7556 Pin Names	In/ Out	If all inputs = '0', predicted value of this pin is:	If one input = '1', predicted value of this pin is:
114	W15	VSYNC	In	0	1
118	W16	CSYNC	Out	0	1
123	Y17	FPVEE / BIAS	Out	0	1
124	U17	FPDECTL	In	0	1
125	W18	FPVCC	In	0	1
127	Y20	PROG0 / TV-ON	Out	0	1
129	W20	PROG2 / NTSC/PAL	Out	1	0
131	V20	FP18	Out	0	1
132	V19	FP19	Out	1	0
133	V18	FP20	Out	0	1
135	U20	FP21	Out	1	0
136	U19	FP22	Out	0	1
137	T18	FP23	Out	1	0
138	T19	FP24	Out	0	1
139	T20	FP25	Out	1	0
140	T17	FP26	Out	0	1
141	R18	FP27	Out	1	0
143	R20	FP28	Out	0	1
144	R17	FP29	Out	1	0
145	P18	FP30	Out	0	1
146	P19	FP31	Out	1	0
147	P20	FP32	Out	0	1
148	P17	FP33	Out	1	0
149	N18	FP34	Out	0	1
150	N19	FP35	Out	1	0
152	N17	FPDE	Out	0	1
153	M18	LLCLK	In	0	1
155	M20	FPVDCLK	In	0	1
156	M17	LFS	In	0	1
157	L18	FP0	Out	1	0
158	L19	FP1	Out	0	1

Table E-1. Pin-Scan Order *(cont.)*

PQFP Pin No.	PBGA Ball No.	CL-GD7556 Pin Names	In/ Out	If all inputs = '0', predicted value of this pin is:	If one input = '1', predicted value of this pin is:
159	L20	FP2	Out	1	0
160	L17	FP3	Out	0	1
161	K18	FP4	Out	1	0
162	K19	FP5	Out	0	1
163	K20	FP6	Out	1	0
164	K17	FP7	Out	0	1
166	J19	FP8	Out	1	0
167	J20	FP9	Out	0	1
168	J17	FP10	Out	1	0
169	H18	FP11	Out	0	1
170	H19	FP12	Out	1	0
172	H17	FP13	Out	0	1
173	G18	FP14	Out	1	0
174	G19	FP15	Out	0	1
175	G20	FP16	Out	1	0
176	G17	FP17	Out	0	1
178	F19	MD63	In	0	1
179	F20	MD62	In	0	1
180	F17	MD61	In	0	1
181	E18	MD60	In	0	1
182	E19	MD59	In	0	1
183	E20	MD58	In	0	1
184	E17	MD57	In	0	1
185	D18	MD56	In	0	1
186	D19	MD55	In	0	1
187	D20	MD54	In	0	1
188	D17	CAS7# / WE7#	In	0	1
189	C19	CAS6# / WE6#	In	0	1
193	A19	MA9	Out	0	1
194	B19	RAS1#	Out	1	0
195	A18	MD53	In	0	1

Table E-1. Pin-Scan Order *(cont.)*

PQFP Pin No.	PBGA Ball No.	CL-GD7556 Pin Names	In/ Out	If all inputs = '0', predicted value of this pin is:	If one input = '1', predicted value of this pin is:
196	B18	MD52	In	0	1
197	C18	MD51	In	0	1
198	C17	MD50	In	0	1
199	A17	MD49	In	0	1
201	C16	MD48	In	0	1
202	B16	MD47	In	0	1
203	A16	MD46	In	0	1
204	D16	MD45	In	0	1
205	C15	MD44	In	0	1
206	B15	MD43	In	0	1
207	A15	CAS5# / WE5#	In	0	1
208	D15	CAS4# / WE4#	In	0	1
209	C14	MD42	In	0	1
210	B14	MD41	In	0	1
211	A14	MD40 / RIOPU	In	0	1
212	D14	MD39	In	0	1
213	C13	MD38	In	0	1
214	B13	MD37	In	0	1
215	A13	MD36	In	0	1
216	D13	MD35	In	0	1
217	C12	MD34 / MMIOPU	In	0	1
218	B12	MD33 / TMPU	In	0	1
219	A12	MD32	In	0	1
221	C11	MA8	Out	1	0
222	B11	MA7	Out	0	1
223	A11	MA6	Out	1	0
224	D11	MA5	Out	0	1
225	C10	MA4	Out	1	0
226	B10	CAS# / WE#	In	0	1
228	D10	RAS0#	Out	0	1
229	C9	MA3	Out	1	0

Table E-1. Pin-Scan Order *(cont.)*

PQFP Pin No.	PBGA Ball No.	CL-GD7556 Pin Names	In/ Out	If all inputs = '0', predicted value of this pin is:	If one input = '1', predicted value of this pin is:
230	B9	MA2	Out	0	1
231	A9	MA1	Out	1	0
232	D9	MA0	Out	0	1
234	B8	MD31 / BIOSPU	In	0	1
235	A8	MD30 / ROM32KPU	In	0	1
236	D8	MD29 / XCLKPU	In	0	1
237	C7	MD28 / INTPU	In	0	1
238	B7	MD27 / SCANPU	In	0	1
240	D7	MD26	In	0	1
241	C6	MD25 / SW2PU	In	0	1
242	B6	MD24 / SW1PU	In	0	1
243	A6	CAS3# / WE3#	In	0	1
244	D6	CAS2# / WE2#	In	0	1
245	C5	MD23 / ROMA15	In	0	1
246	B5	MD22 / ROMA14	In	0	1
247	A5	MD21 / ROMA13	In	0	1
248	D5	MD20 / ROMA12	In	0	1
249	C4	MD19 / ROMA11	In	0	1
251	A4	MCLK / XMCLK / SW0	In	0	1
253	B3	EROM#	Out	0	1
255	A1	OE#	Out	1	0

Appendix F

EXTENDED DISPLAY MODE PROGRAMMING

F.1 Introduction

The CL-GD7556 is capable of supporting a wide range of Extended VGA and Super VGA high-resolution display modes on both flat panels and CRT monitors, including the following:

- 1280 × 1024 CRT monitors: up to 256 colors (non-interlaced)
- 1024 × 768 flat panels and CRT monitors: up to 64K colors
- 800 × 600 flat panels and CRT monitors: up to 16M colors
- 640 × 480 flat panels and CRT monitors: up to 16M colors

In this appendix, the Extended VGA display modes are described in terms of:

- Display memory organizations (Section F.2)
- Display memory addressing and mapping techniques for extended display modes (Section F.3)
- Programming examples that demonstrate how to implement some of these features (Section F.4)

For information on all the extended display modes supported by the CL-GD7556, refer to Chapter 4.

F.2 Display Memory Organization for Planar and Packed-Pixel Display Modes

Table F-1 compares the display memory organization of the planar and packed-pixel display modes.

Table F-1. Comparison of Planar and Packed-Pixel Display Modes

Item of Comparison	Type of Display Mode	
	Planar Display Mode	**Packed-Pixel Display Mode**
The setting for CL-GD7556 Extension register SR7[0]	Extension register SR7[0] = 0	Extension register SR7[0] = 1
Number of colors displayed	Only up to 16 colors can be displayed at one time.	256, 32K, 64K, or 16M colors can be displayed at one time. (The availability of the number of colors depends on the resolution of the display screen and the total amount of display memory.)
Bits per pixel	Only 4 bits per pixel.	8, 16, or 24 bits per pixel. As determined by the setting of the HDR (the Hidden DAC Extension register), the number of bits per pixel for a display mode is set to either 8, 16, or 24 bits per pixel.
Placement of pixel data in display memory	Four display memory planes are used. Each pixel is dispersed across the four display memory bit planes.	Only one display memory plane is used. All pixel data are in this same display memory plane.
Address generation	Address bits are read across the four display memory bit planes.	The CL-GD7556 memory controller handles all address generation. To the host CPU, the display memory appears as follows: • When display memory is in a segmented mode, the display memory appears sequential, with 64 Kbytes of linearly addressable display memory. • When display memory is in a linear addressing mode, the display memory appears to be from 1 to 2 Mbytes of linearly addressable display memory.
Page address mapping	Only display mode resolutions above 1024 × 768 require page address mapping.	All display mode resolutions require page address mapping.

F.2.1 Planar Display Mode: 16-Color

The CL-GD7556 planar display mode is a standard IBM VGA display mode that displays only 16 colors on the screen at one time. This display mode is enabled when Sequencer register bit SR4[2] is set to 1 and bit SR4[3] is cleared to 0. This display mode requires 4 bits per pixel and represents a pixel by dispersing bits of information across 4 display memory planes, with 1 bit per plane. The display memory is organized as bytes, with 8 pixels per byte.

The display memory planes are overlaid in the host CPU memory address space so that each plane occupies the same host CPU address. For read/write operations, the host CPU can access any of these planes independently by programming the Sequencer register bits SR2[7:0].

Figure F-1 shows how the planar mode display memory is organized in four planes. The figure depicts how color information for each pixel is stored in corresponding bits across the four planes. In addition, the figure depicts how bank 0 and bank 1 (used in paging) are aligned across each plane.

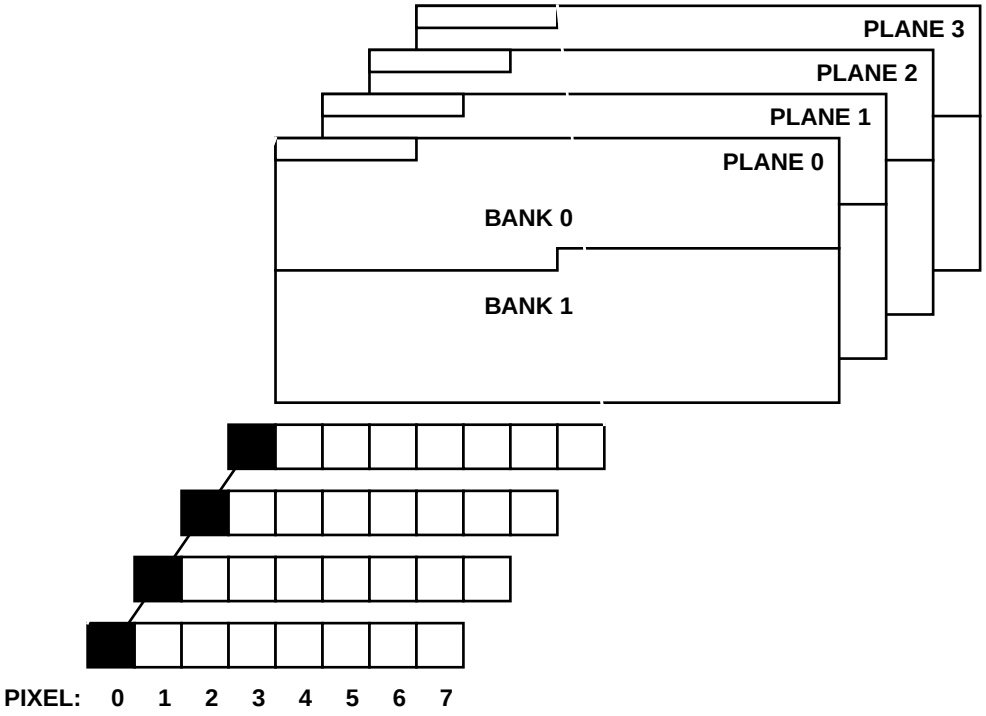


Figure F-1. Memory Organization for Planar Display Mode (16 Colors)

The standard IBM VGA supports 256 Kbytes of display memory. In the planar display mode, the 256 Kbytes of display memory are divided into four display memory planes, with 64 Kbytes per plane. Normally, the 64-Kbyte segment of each plane is mapped in A0000h to AFFFFh, and the host CPU can easily address each plane.

However, a problem arises when a display mode requires more than 64 Kbytes of addressable display memory per plane. For example, when a planar display mode is used for display screens that have a screen format of 1024 × 768, the planar display mode requires 98,304 bytes, which is an additional 32,768 bytes of addressable display memory per plane. The problem of having more than 64 Kbytes of addressable display memory is solved by using the extended display memory addressing techniques discussed in Section F.3.

F.2.2 Packed-Pixel Display Mode: 256 Colors

This display mode is enabled when Extension register bit SR7[0] is set to 1. (When Sequencer register bit SR4[3] is set to 1, this display mode becomes Chain-4 mode.) The following figure shows how 8-bit-per-pixel (packed-pixel mode) bytes are stored in terms of the physical plane organization.

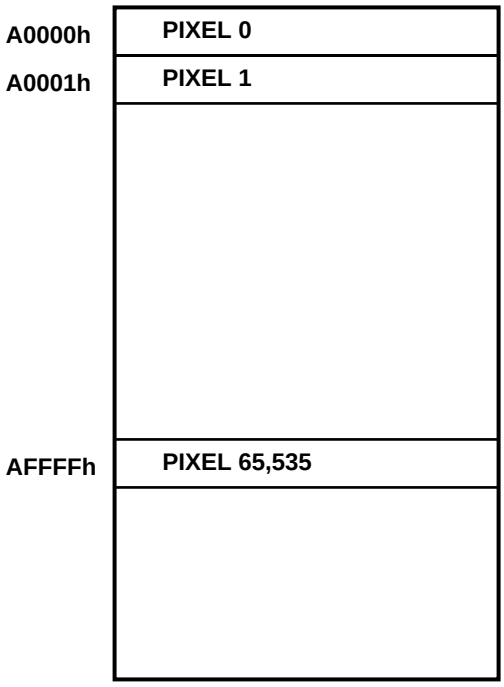


Figure F-2. 256-Color Packed-Pixel Mode

The CL-GD7556 on-chip memory controller makes this organization completely transparent. Hence, to the host CPU, addressing is sequential. For example:

- At segment A0000h, pixel 0 resides at offset 0.
- At segment A0001h, pixel 1 resides at offset 1.

  •
  •
  •

- At segment AFFFh, pixel 65,535 resides at offset 65,535.

To address display memory that is beyond the 64-Kbyte segment boundary, the CL-GD7556 supports a display memory paging technique that allows up to 2 Mbytes of display memory to be paged into the host CPU address range.

When mapping display memory for linear addresses (as discussed in Section F.3.1), display memory paging is not required.

F.2.3 Packed-Pixel Display Mode: Direct Color (32K and 64K Colors)

The CL-GD7556 supports Direct-Color packed-pixel display modes that are capable of displaying up to either 32,768 (32K) colors or 65,536 (64K) colors simultaneously, at screen resolutions of up to 1024 × 768. Color information used to display these colors simultaneously is:

- 15 bits per pixel for 32K colors
- 16 bits per pixel for 64K colors

To enable Direct-Color display modes, Extension register bit SR7[0] is set to 1, and then the CL-GD7556 graphics color palette (CLUT) set to Direct-Color display modes by programming Extension register HDR to '80h'.

Figure F-3 shows how 15-bit pixel data (for 32K colors) is stored relative to the physical plane organization. The RGB color information is stored in RGB 5-5-5 format (5 bits each for red, green, and blue). Two bytes per pixel are used for storing the color information. The most-significant bit (bit 15) is ignored.

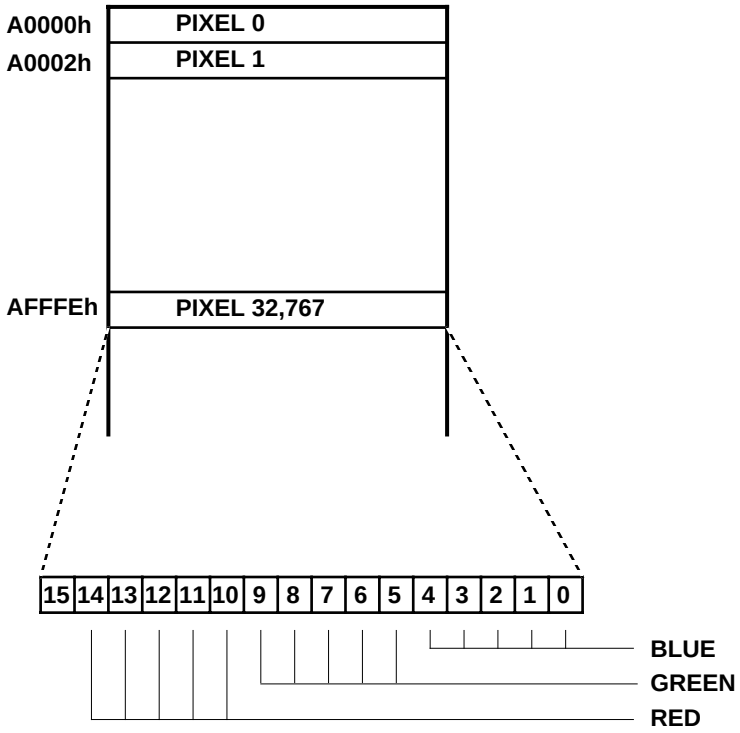


Figure F-3. 32,768 Color (15-Bit) Packed-Pixel Display Mode

Figure F-4 shows how 16-bit pixel data (for 64K colors) is stored in terms of the physical plane organization. The RGB color information is stored in RGB 6-6-6 format (5 bits of red, 6 bits of green, and 5 bits of blue). Two bytes per pixel are used for storing the color information.

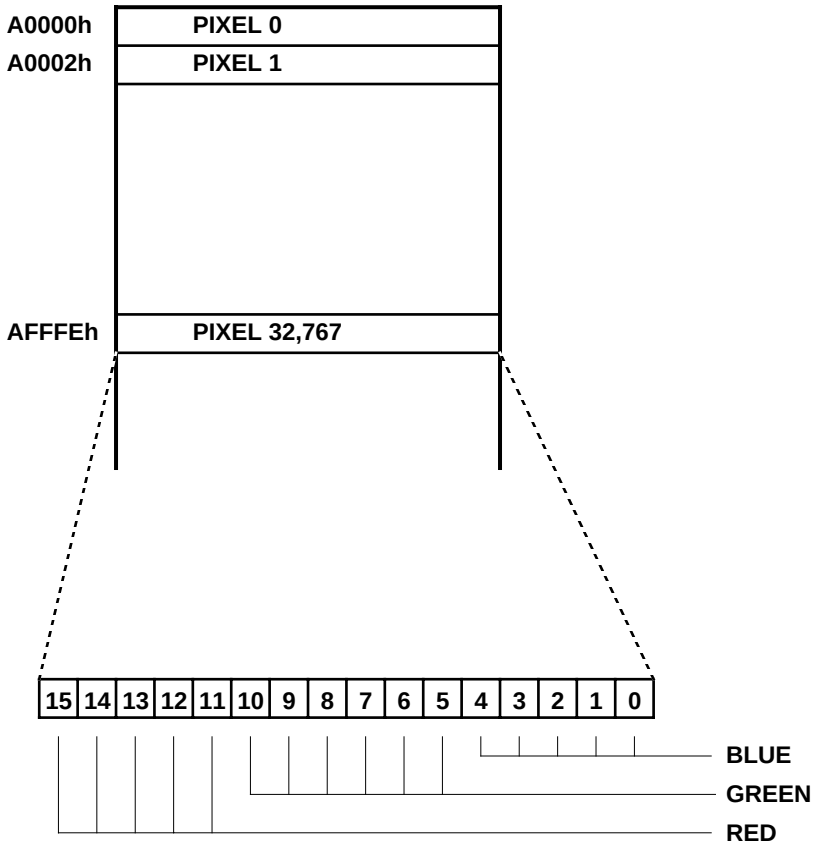


Figure F-4. 65,536 Color (16-Bit) Packed-Pixel Display Mode

As in the 256-Color Packed-Pixel Display mode (refer to Section F.2.2), the CL-GD7556 on-chip memory controller makes this organization of the physical plane completely transparent. As a result, addressing is sequential to the host CPU. For example:

- At segment A0000h, pixel 0 resides at offset 0 and offset 1.
- At segment A0001h, pixel 1 resides at offset 2 and offset 3.

  •
  •
  •

- At segment AFFFE, pixel 32,767 resides at offset 65,534 and offset 65,535.

To address display memory that is beyond the 64-Kbyte segment boundary, the CL-GD7556 supports a display memory paging technique that allows up to 2 Mbytes of display memory to be paged into the host CPU address range.

F.2.4 Packed-Pixel Display Mode: True Color, 24-Bit (16M Colors)

The CL-GD7556 supports True-Color packed-pixel display modes that are capable of displaying 16M colors simultaneously at screen resolutions of up to 800 × 600. To display 16M colors in TARGA™-compatible mode, 24 bits per pixel of RGB color information (8 bits each for red, green, and blue) are used.

To enable the Mixed-Color mode, Extension register SR7[0] is set to '1', and the CL-GD7556 graphics color palette (CLUT) is set to a True-Color format by programming Extension register HDR to 'C5h'.

Figure F-5 shows how 24-bit pixel data is stored in terms of the physical plane organization. Three bytes per pixel are used for storing the color information.

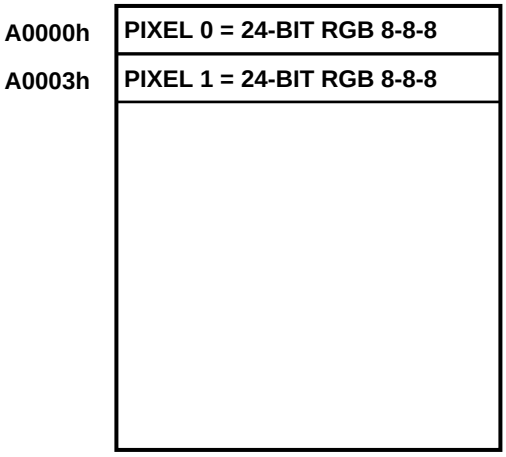


Figure F-5. 24-Bit True-Color Packed-Pixel Display Mode

The CL-GD7556 on-chip memory controller makes this organization of the physical plane completely transparent. As a result, to the host CPU, the byte addressing is sequential. For example:

- At segment A0000h, pixel 0 resides at offset 0 to offset 2 as follows:
  - — Blue color information at offset 0
  - — Green color information at offset 1
  - — Red color information at offset 2
- At segment A0003h, pixel 1 resides at offset 3 to offset 5 as follows:
  - — Blue color information at offset 3
  - — Green color information at offset 4
  - — Red color information at offset 5
- At segment AFFFDh, pixel 21,845 resides at offset 65,533 to offset 65,535 and so forth.

To address display memory beyond the 64-Kbyte-segment boundary, the CL-GD7556 supports a display memory paging scheme that allows up to 2 Mbytes of display memory to be paged into the host CPU address range.

F.3 Display Memory Mapping for Extended Display Modes

The CL-GD7556 addresses 1 or 2 Mbytes of display memory. However, in the DOS environment, at A0000h–BFFFFh, only 128 Kbytes of address space are reserved for display memory. As a result, if the CL-GD7556 has to share this memory space with MDA, Hercules®, or CGA controllers, it is left with only a single 64-Kbyte segment from A0000h to AFFFFh.

To extend the address space for the display memory, the CL-GD7556 supports the display memory mapping techniques shown in Table F-2.

Table F-2. Display Memory Mapping Techniques

Display Memory Mapping Technique	Reference	Description of Display Memory Mapping Technique
Linear	Section F.3.1	Allows display memory to be mapped to a continuous 1- or 2-Mbyte region above the standard 1-Mbyte DOS address space.
Single-Page	Section F.3.2	Allows one 64-Kbyte segment of display memory to be mapped into the host CPU address space.
Dual-Page	Section F.3.3	Allows two 32-Kbyte segments of display memory to be mapped into the host CPU address space.

F.3.1 Display Memory Mapping for Linear Addresses

Linear address mapping allows display memory to be mapped to either a continuous 1- or 2-Mbyte region above the standard 1-Mbyte DOS address space. This action allows application programs to access the display memory as a linearly addressed string of up to 2 Mbytes, rather than being constrained to using a standard 64-Kbyte segment from A0000h to AFFFFh.

When the CL-GD7556 is in linear addressing mode, it provides a 16-Mbyte address space. The 16-Mbyte space can be set up as four 4-Mbyte byte-swapping apertures for the Power PC, which requires linear addressing. The bottom of this space is used for display memory access, and the top 256 bytes of each 4-Mbyte aperture can be used for memory-mapped I/O.

To use the CL-GD7556 in the linear addressing mode, the software drivers that are used must be written so as to ensure compatibility with the operating system. In addition, the following conditions must be true:

- External/General register bits PCI10[31:24] and the most-significant address bits on the PCI address bus (that is, AD[31:24]) must match.
- Extension register bits SR7[7:4] must not equal ‘0000’.

For Windows drivers, the base address of the linear space is retrieved from External/General register PCI10, using a PCI System BIOS INT 1A call. The setting of the SYSTEM.INI is not used.

F.3.2 Display Memory Mapping for a Single-Page Address

Single-page address mapping is used to extend the host CPU address space for display memory. As shown in Figure F-6 below, and as described in this section, single-page address mapping allows the following actions:

- Any 64-Kbyte segment (or 'page') of display memory can be mapped into address range A0000h–AFFFFh of the host CPU address.
- The Start Page Address can begin:
  - — At any 4-Kbyte boundary of 1-Mbyte display memory
  - — At any 16-Kbyte boundary of 2-Mbyte display memory

After the 64-Kbyte segment of display memory is mapped into the host CPU address range, it can be accessed by the host CPU for read and write operations.

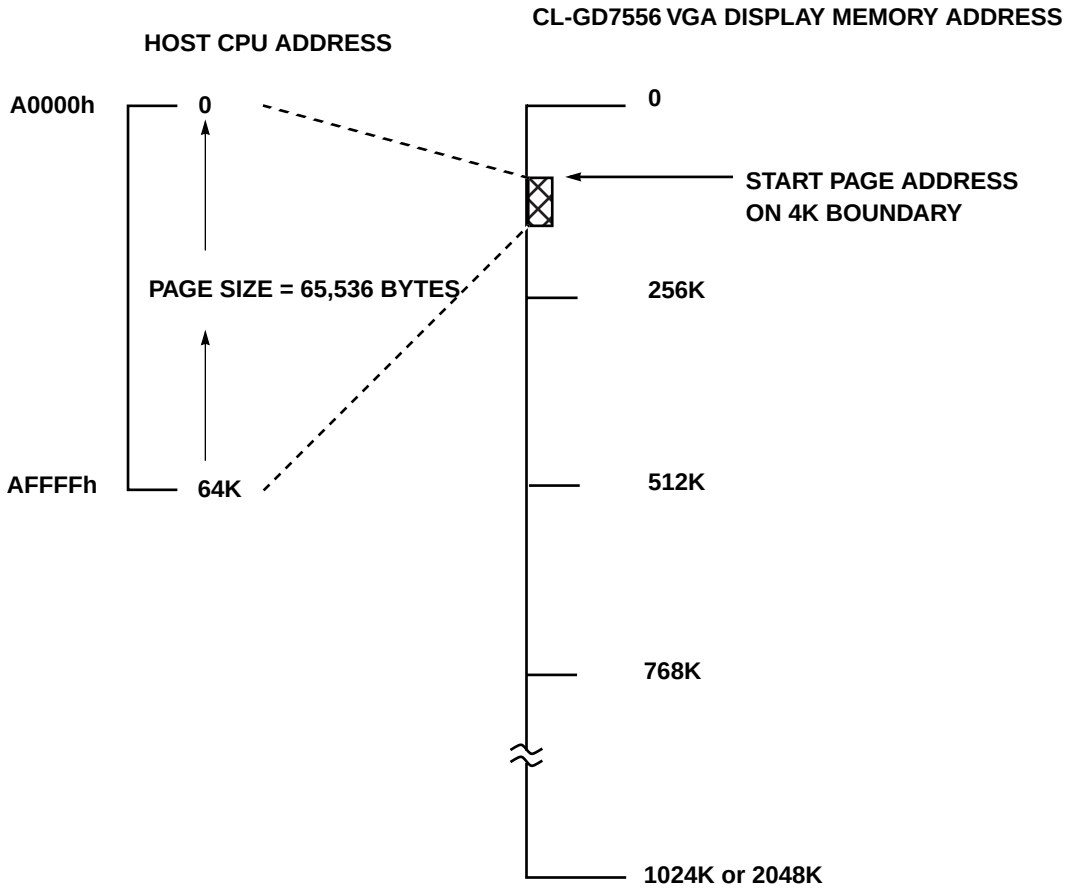


Figure F-6. Single-Page Address Mapping Technique

To select a 64-Kbyte segment of display memory and map it into the host CPU address range, perform the following actions:

- To always select only one 64-Kbyte segment of display memory (and never two 32-Kbyte segments), select Display Memory Offset 0 by programming Extension register bit GRB[0] to a 0.
- For display memory that has a granularity of:
  - — 4-Kbytes, set Extension register GRB[5] to 0.
  - — 16-Kbytes, set Extension register GRB[5] to 1.
- To select the desired Display Memory Offset 0 address, program Extension register bits GR9[7:0]. The value that is programmed into these register bits is then added to host CPU address bits to provide the address for mapping the display memory as shown in Figure F-7 and Figure F-8.

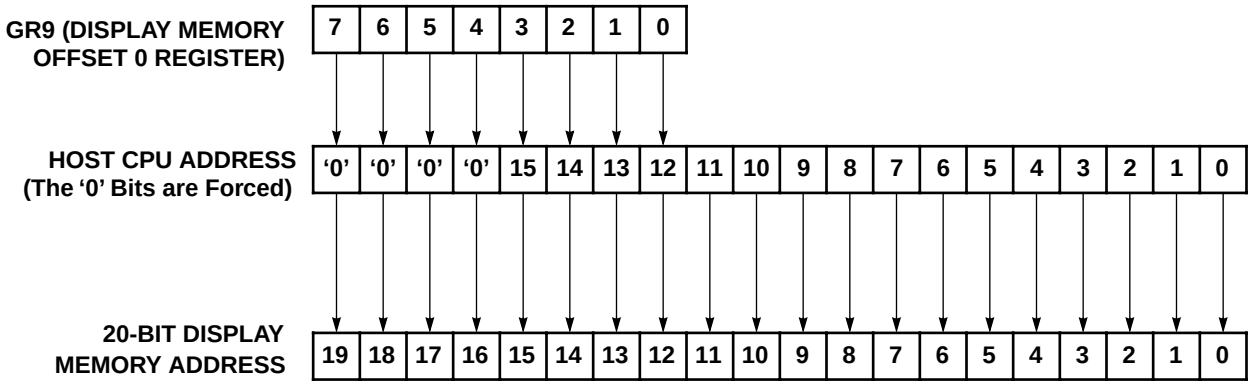


Figure F-7. Single-Page-Mode Remapping Adder Alignment with 4-Kbyte Granularity

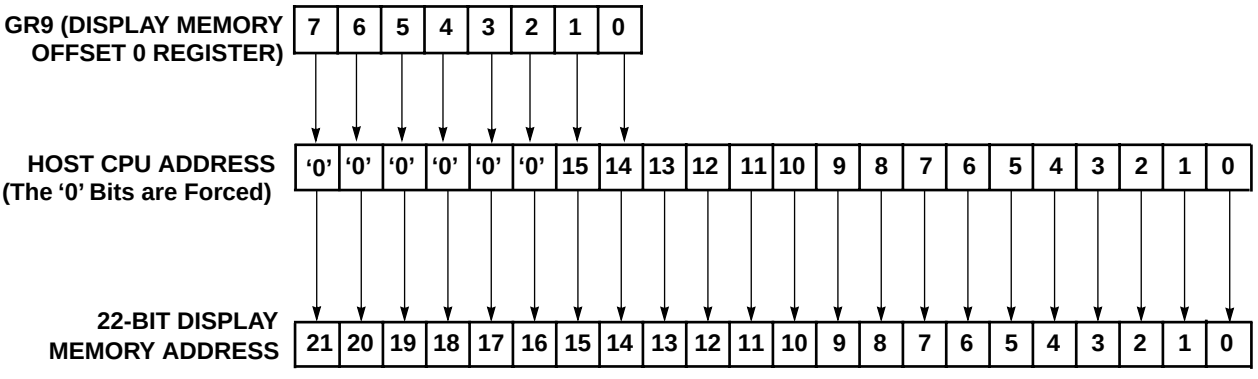


Figure F-8. Single-Page-Mode Remapping Adder Alignment with 16-Kbyte Granularity

F.3.3 Display Memory Mapping for a Dual-Page Address

Dual-page address mapping is used for read-modify-write operations on large blocks of data. As shown in Figure F-9, and as described in this section, dual-page address mapping allows the following actions:

- Two 32-Kbyte segments (or 'pages') of display memory can be mapped into host CPU address ranges A0000h–A7FFFh and A8000h–AFFFFh.
- The 32-Kbyte segments can be either separate or overlapping.
- The Start Page Address can begin at any 4-Kbyte boundary for 1 Mbyte of display memory.
- The Start Page Address can begin at any 16-Kbyte boundary for 2 Mbytes of display memory.

After the two 32-Kbyte segments of display memory are mapped into the host CPU address range, they can be accessed by the host CPU for read and write operations. This action allows for block transfers of data bits, by using repeated 'move string' DMA (direct-memory access) instructions.

NOTE: The advantages of dual-page addressing are largely superseded by the BitBLT engine.

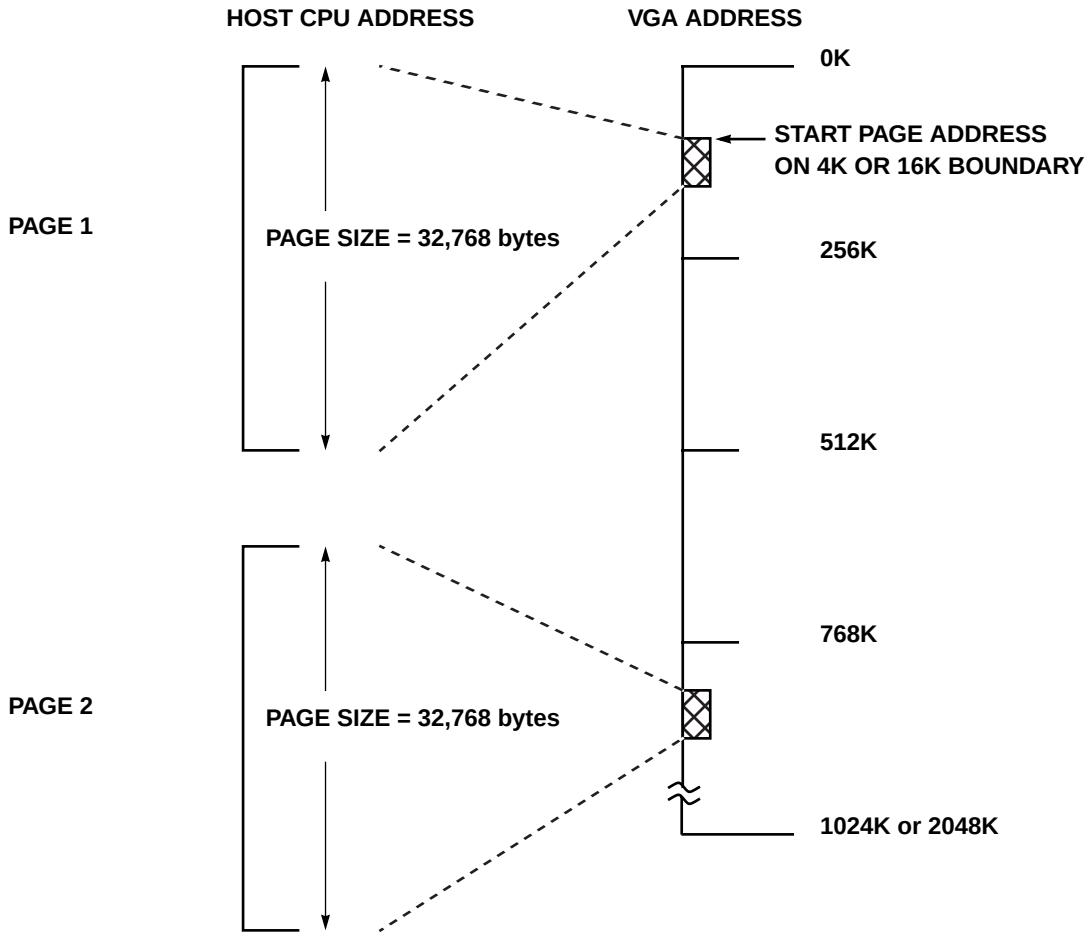


Figure F-9. Dual-Page Address Mapping Scheme

To select any two separate or overlapping 32-Kbyte segments of display memory and then map them into the host CPU address range, perform the following actions:

- Set Extension register GRB[0] to 1 to select dual-page mode addressing.
- Host CPU Address bit AD15 selects which of the two Display Memory Offset registers (GR9 and GRA) is used to calculate the resulting value of the display memory address. Set AD15 to:
  - — 0 to select GR9 for Display Memory Offset 0
  - — 1 to select GRA for Display Memory Offset 1
- Program the Start Page Addresses as follows:
  - — To determine the start address of page 1, program Extension register GR9[7:0].
  - — To determine the start address of page 2, program Extension register GRA[7:0].

NOTES:

1) The Start Page Address can begin at any 4-Kbyte boundary for display modes that fit into 1 Mbyte of display memory.

2) The Start Page Address can begin at any 16-Kbyte boundary for display modes that fit into 1 or 2 Mbytes of display memory.

For two 32-Kbyte pages that use 4-Kbyte granularity Figure F-10 shows how, for both Display Memory Offset 0 and 1, the offset register bits and the host CPU address bits are added to obtain a resulting display memory address of 1 Mbyte of display memory.

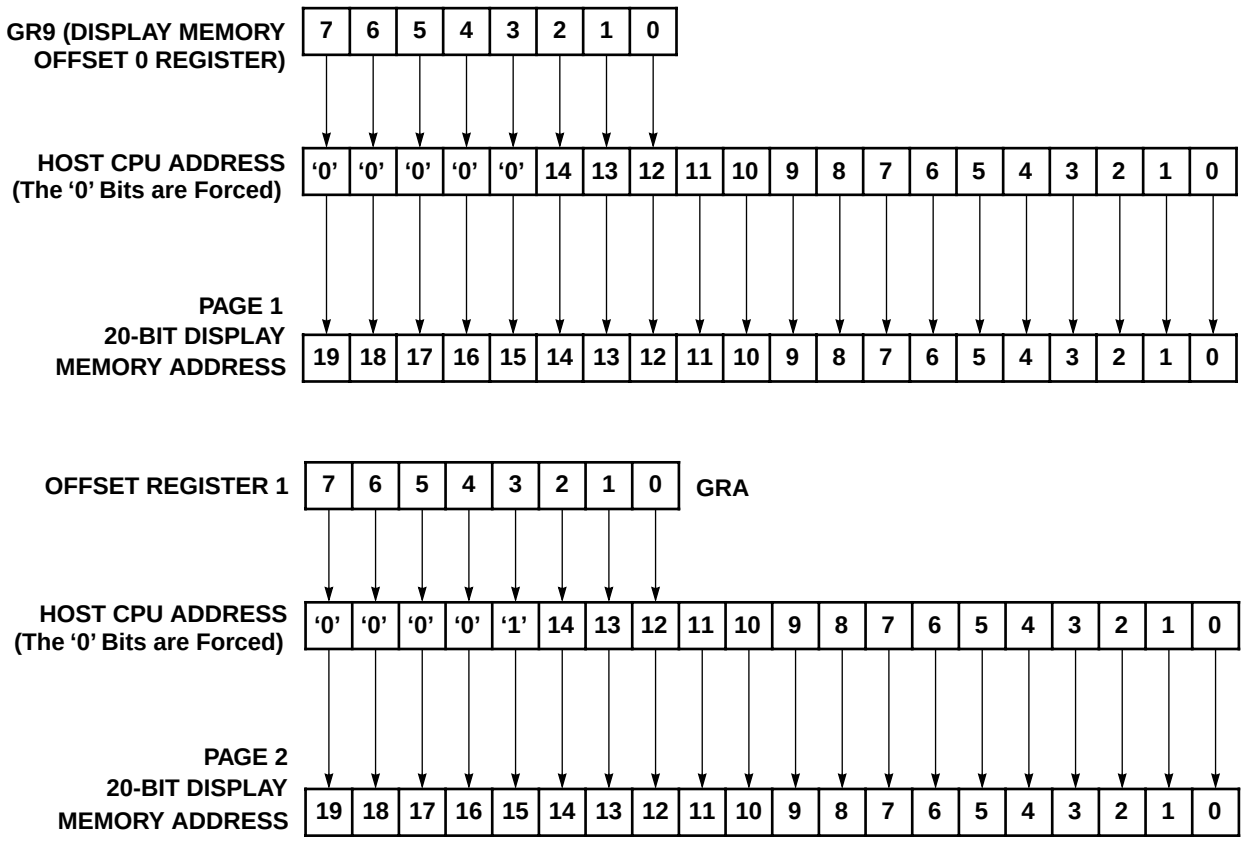


Figure F-10. Dual-Page-Mode Remapping Adder Alignment with 4-Kbyte Granularity

For two 32-Kbyte pages that use 16-Kbyte granularity Figure F-11 shows how the Display Memory Offset 0 and 1 register bits and the host CPU address bits (AD[21:0]) are added to obtain a resulting display memory address of 1 or 2 Mbytes of display memory.

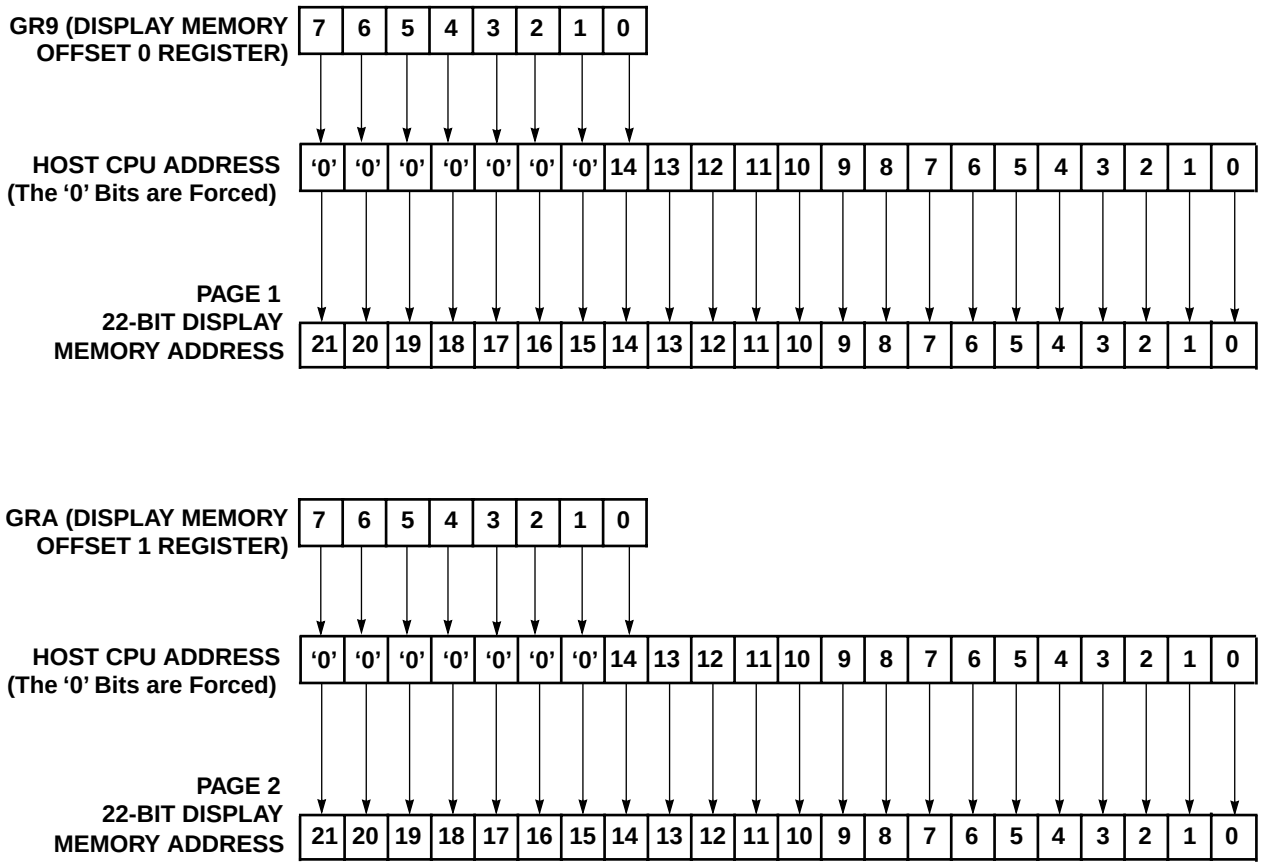


Figure F-11. Dual-Page-Mode Remapping Adder Alignment with 16-Kbyte Granularity

Table F-3 lists the CL-GD7556 Extension registers that control the host CPU base address and display memory mapping functions:

Table F-3. Extension Registers for Host CPU Base Address and Display Memory Mapping

Extension Register	Port	Index	Register Bit(s)	Value of Bit(s)	Function of Bit(s)
SR7: Extended Sequencer Mode	3C4	07	SR7[7:4]	15...0	Select display memory segment (that is, any value that is not '0000')
GR9: Display Memory Offset 0 Register	3CF	09	GR9[7:0]	255...0	Access up to 2 Mbytes of display memory, with up to 16-Kbyte granularity.
GRA: Display Memory Offset 1 Register	3CF	0A	GRA[7:0]	255...0	Access up to 2 Mbytes of display memory, with up to 16-Kbyte granularity.
GRB: Graphics Controller Mode Extensions	3CF	0B	GRB[0]	'0'	Map single-page display memory
				'1'	Map dual-page display memory
			GRB[5]	'0'	Set Display Memory Offset register granularity to 4 Kbytes
				'1'	Set Display Memory Offset register granularity to 16 Kbytes

F.4 VGA Programming Examples

This section provides the CL-GD7556 software programming examples.

F.4.1 Unlocking the CL-GD7556 Extension Registers

To identify a CL-GD7556 Low-Voltage 64-Bit Video and Graphics LCD/CRT Controller as the controller that is being used, call the extended VGA BIOS inquiry function by using the interrupt INT 10h. However, if an extended VGA BIOS is not available, then to identify a CL-GD7556 controller:

- Program Extension register SR6 (Unlock All Extension Registers) to enable CL-GD7556 Extension registers.
- Read Extension register CR27 (the Device ID and Manufacturing Revision ID register).

The following code shows the steps to enable access to CL-GD7556 Extension registers:

```
; Function:
; Enable Extension registers

; Calling Protocol:
;     Enable_extensions

Enable_extensions macro
      mov      dx,3C4h    ; Load Extension register SR6 I/O port
      mov      al,06h     ; Load SR6 index
      mov      ah,12h     ; Load SR6 with xxx1x010 to enable Extension registers
      out      dx,ax      ; Write index and data
Enable_extensions endm
```

The following code shows the steps to disable access to CL-GD7556 Extension registers:

```
; Function:
; Disable Extension registers

; Calling Protocol:
;     Disable_extensions

Disable_extensions macro
      mov      dx,3C4h    ; Load Extension register SR6 I/O port
      mov      al,06h     ; Load SR6 index
      mov      ah,00h     ; Load SR6 with 00 to disable Extension registers
      out      dx,ax      ; Write index and data
Disable_extensions endm
```

F.4.2 Identifying a CL-GD7556 VGA Controller

Extension register CR27 (the Device Identification register) is used to identify a CL-GD7556 VGA controller. The following sample code listing shows how to program Extension register CR27 to read the CL-GD7556 device ID.

```
; Function:
; Identify Cirrus Logic CL-GD7556 Low-Voltage 64-Bit Video and Graphics LCD/CRT
Controller

; Input:
; None

; Output:
; al = 00h ID failed
; al = 4Ch CL-GD7556 device ID

; Calling Protocol:
; Id_CL-GD7556()

_Id_CL-GD7556 proc far
      mov      dx,3C4h    ; Load Extension register SR6 I/O port
      mov      al,06      ; Load SR6 index
      out      dx,al      ; Write index and data register
      inc      dx         ; Increment index register
      in       al,dx      ; Read data register
      cmp      al,12h     ; Compare SR6 read-back value. Are registers locked?
      mov      al,00h     ; If registers locked, return ID failed.
      jne      chk27      ; No. Check to see if this is a CL-GD7556
exit: ret                 ; Return in al the device ID value, or ID failed
chk27:mov      dx,3D4h    ; Load Extension register CR27 I/O port return
      mov      al,27h     ; Load CR27 index
      out      dx,al      ; Write index and data register
      inc      dl         ; Increment dl
      in       al,dx      ; Read device ID
      and      al,FCh     ; Clear bits 0 and 1
      cmp      al,40h     ; Check for CL-GD7556 ID
      je       exit       ; Yes (the device is a CL-GD7556)
      xor      al,al      ; No  (the device is not a CL-GD7556)
      jmp      exit
_Id_CL-GD7556 endp
```

F.4.3 Initializing the CL-GD7556 Extended Display Mode By Using an INT 10h Call

The following code listing is used to initialize a desired extended display mode by calling the Cirrus Logic VGA BIOS set display mode function. (This example is for the CL-GD7556.)

```
; Function:
; Set up extended display mode supported by CL-GD7556 VGA BIOS

; Calling Protocol:
;     al = Desired CL-GD7556 display mode number
;     Return
;     al = Current display mode

Set_Video_Mode proc near
      mov      ah,0       ; Load VGA BIOS set display mode function 0
      int      10h        ; Call VGA BIOS interrupt 10 hex,
                          ; al = display mode number
      mov      ah,0Fh     ; VGA BIOS load current display mode number
      int      10h        ;
      ret                 ; Return current display mode number in al
Set_Video_Mode endp
```

F.4.4 Programming Memory Mapping Registers

F.4.4.1 Display Memory Mapping for a Single-Page Address

The following code listing shows how to program Extension register GRB (the Graphics Controller Mode Extensions register) to set up single-page mapping.

```
; Function:
; Set up Single-Page Mapping

; Calling Protocol:
;     Set_Single_Page

Set_Single_Page proc near ; Set up Extension register GRB for single page
      mov      dx,3CEh    ; Load GRB I/O port
      mov      al,0Bh     ; Load GRB index
      out      dx,al      ; Write index register
      inc      dx         ; Increment dx to read data port
      in       al,dx      ; Read data
      and      al,FEh     ; Apply mask to set GRB[0] = 0
      out      dx,al      ; Write GRB I/O port with new data
      ret
Set_Single_Page           endp
```

F.4.4.2 Display Memory Mapping for a Single-Page Address with 64-Kbyte Segment

The following code listing shows how to program Extension register GR9 (Display Memory Offset 0 register) to map a desired 64-Kbyte page of display memory into the host CPU address.

```
; Function:
; Load Extension register GR9 with new start address of a 64-Kbyte segment

; Input:
; bl = 0..255 page number for start address of desired 64-Kbyte segment

; Calling Protocol:
;     Select_Single_Page

Select_Single_Page macro
      mov      dx,3CEh    ; Load Extension register GR9 I/O port
      mov      al,09h     ; Load GR9 index
      mov      ah,bl      ; Get page number for mapping
      out      dx,ax      ; Program selected page
Select_Single_Page endm
```

F.4.4.3 Display Memory Remapping for a Dual-Page Address

The following code listing shows how to program Extension register GRB (the Graphics Controller Mode Extensions register) to set up dual-page remapping.

```
; Function:
; Set up Dual-Page Remapping

; Calling Protocol:
;     Set_Dual_Page

Set_Dual_Page proc far    ; Set up Extension register GRB for dual page
      mov      dx,3CEh    ; Load GRB I/O port
      mov      al,0Bh     ; Load GRB index
      out      dx,al      ; Write index register
      inc      dx         ; Increment dx to read data port
      in       al,dx      ; Read data
      or       al,01h     ; Data = enable 32K page size, dual page
      out      dx,al      ; Write GRB I/O port with new data
      ret
Set_Dual_Page  endp
```

F.4.4.4 Display Memory Remapping for a Dual-Page Address with 32-Kbyte Segment

The following code listing shows how to program Extension registers GR9 (Display Memory Offset 0 register) and GRA (Display Memory Offset 1 register) to set up dual-page remapping with 32-Kbyte segments.

```
; Function:
; Load Extension registers GR9 and GRA with new start address of 32-Kbyte
; segments

; Input:
; bl = 0..255 page number for 32-Kbyte segment mapped to A0000h-A7FFFh
; bh = 0..255 page number for 32-Kbyte segment mapped to A8000h-AFFFFh

; Calling Protocol:
;     Select_Dual_Pages

Select_Dual_Pages macro
      mov      dx,3CEh    ; Load Extension register GR9 I/O port
      mov      al,09h     ; Load GR9 index
      mov      ah,bl      ; Get page number for A0000h-A7FFFh mapping
      out      dx,ax      ; Program selected page
      mov      al,0Ah     ; Load GRA index
      mov      ah,Bh      ; Get page number for A8000h-AFFFFh mapping
      out      dx,ax      ; Program selected page
Select_Dual_Pages endm
```

Notes

Appendix G

HARDWARE CONFIGURATION NOTES

G.1 Introduction

The CL-GD7556 memory data pins MD[40:24] are multipurpose pins used to initialize the CL-GD7556 for operation. External pull-up resistors are connected to these memory data pins, which are read during the low-to-high transition of the system reset pulse. The resulting low or high status of the inputs is stored in Extension registers SR22 and SR24. If an external pull-up resistor:

- *Is not connected* to a memory data pin, the pin is read as low because of the CL-GD7556 internal pull-down resistor.
- *Is connected* to a memory data pin, the pin is read as high.

The hardware configuration data can be latched into Extension registers SR22 and SR24 by programming a 0-1-0 transition on Extension register bit SR24[3]. This action can be used when the system reset pulse is not long enough to read the hardware configuration data.

NOTE: Some of the software-programmable register bits that are used to select the desired function of some multifunction pins are covered in the Cirrus Logic 'motherboard' application notes in the *CL-GD7556 Application Book*.

G.2 Configuration Summary

The CL-GD7556 memory data pins listed in Table G-1 have an internal pull-down resistor. If no pull-up resistor is attached, the default is a '0'. If a '1' is to be loaded into the latch associated with a given MD line, an external pull-up resistor must be added.

The following table provides an overview of the configuration bits. The last column describes the CL-GD7556 pin functions, when a pull-up resistor is or is not connected to the CL-GD7556 MD line. For more configuration details, refer to Section 2.8.

Table G-1. Configuration Bits

CL-GD7556 PQFP Pin (Memory Data Bit)		Pull-Up Resistor Connection to MD Pin?	Resulting Function of CL-GD7556 Pin
PQFP Pin Number	PQFP Pin Name		
211 (A14)[a]	MD40 / RIOPU	Connected	The PCI I/O Offset Effect is enabled.
		Not Connected	The PCI I/O Offset Effect (that is, relocatable I/O) is disabled.
217 (C12)[a]	MD34 / MMIOPU	Connected	Memory-mapping of standard VGA registers is enabled.
		Not Connected	Memory-mapping of standard VGA registers is disabled.
218 (B12)[a]	MD33 / TMPU	Connected	Test mode is enabled for pin-scan and factory testing.
		Not Connected	The Test mode is disabled.
219 (A12)[a]	MD32/PCI-CMOS	Connected	The PCI-bus interface is set for CMOS thresholds.
		Not Connected	The PCI-bus interface is set for TTL thresholds, except for the CLK pin.
234 (B8)[a]	MD31 / BIOSPU	Connected	On-chip PCI VGA BIOS is supported.
		Not Connected	On-chip PCI VGA BIOS is not supported.
235 (A8)[a]	MD30 / ROM32KPU	Connected	Support is enabled for a 32-Kbyte VGA BIOS. (This setting is not recommended, since the CL-GD7556 VGA BIOS requires a minimum of 48 Kbytes.)
		Not Connected	The default 64-Kbyte EPROM VGA BIOS is selected.
236 (D8)[a]	MD29 / XCLKPU	Connected	External clock inputs are configured for the SWO / MCLK / XMCLK and OSC / XVCLK pins. This configuration is for factory testing only.
		Not Connected	Internal clock inputs are configured for the CL-GD7556.
237 (C7)[a]	MD28 / INTPU	Connected	The INTR# (Interrupt Request) pin function is disabled. In this case, the INTR# pin must not be connected.
		Not Connected	The INTR# pin function is enabled.
238 (B7)[a]	MD27 / SCANPU	Connected	Pin-scan testing is enabled. (See Appendix E for more information.)
		Not Connected	Pin-scan testing is disabled.
241 (C6)[a]	MD25 / SW2PU[b]	Connected	Extension register bit SR24[2] is set to 1.
		Not Connected	Extension register bit SR24[2] is set to 0.
242 (B6)[a]	MD24 / SW1PU[b]	Connected	Extension register bit SR24[1] is set to 1.
		Not Connected	Extension register bit SR24[1] is set to 0.

[a] The numbers in (##) are the PGA pad numbers.

[b] This pin is used by the VGA BIOS.

Appendix H

MEMORY-MAPPED I/O

H.1 Introduction

The CL-GD7556 allows memory-mapped I/O accesses to occur to the BitBLT-control registers. (That is, application programs can access the BitBLT-control registers as memory locations.) When multiple registers must be changed at once, the memory-mapped I/O method of accessing the BitBLT-control registers can occur up to four times faster than using register I/O.

During a memory-mapped I/O access, the register address is implied in the address rather than being transferred as part of the data (that is, in the index field). As a result, the data transfer rate is doubled. Furthermore, because doubleword transfers are allowed, the data transfer rate is doubled again.

H.2 Memory-Mapped I/O Method of Accessing BitBLT-Control Registers

The memory-mapped I/O function is enabled when Extension register SR17[2] = 1. When enabled, the registers listed in Table H-1 are addressable as a 256-byte block of memory. The CL-GD7556 memory-mapped I/O accessing supports both the Segmented and Linear addressing modes.

H.2.1 Segmented Addressing

Segmented addressing is enabled under the following conditions:

- Graphics Controller register bits GR6[3:2] are set to ‘01’.
- Extension register bits SR7[7:4] are set to ‘0000’.
- Extension register bit SR17[6] is set to ‘0’.

In this case:

- The window into display memory is 64 Kbytes (A000:0h to AFFF:Fh).
- A block of 256 bytes of memory address space is reserved beginning at B800:0h. (Address bits A[14:8] are a ‘don’t care’, and so the block is actually aliased at every 256-byte boundary.) This block can be accessed using byte, word, or doubleword cycles.

H.2.2 Linear Addressing

Linear addressing (discussed in more detail in Section 3.3.1), is enabled under the following conditions:

- Extension register bit SR17[6] is set to ‘1’
- Extension register bits SR7[7:4] are set to a non- zero value.
- Graphics Controller register bits GR6[3:2] are a ‘don’t care’.

For linear addressing, the memory address space is located only at the highest 256 bytes of a 4-Mbyte linear address space starting at 3FFF00h.

Table H-1 indicates the registers that are accessible when memory-mapped I/O is used. Except for GR31, which is a read/write register, all registers in Table H-1 are write-only.

Table H-1. Registers Accessed Using Memory-Mapped I/O

Offset (hex)	Graphics Controller Register	Extension Register	Register Description
00	GR0		Background Color Byte 0
01		GR10	Background Color Byte 1
02		GR12	Reserved
03		GR14	Reserved
04	GR1		Foreground Color Byte 0
05		GR11	Foreground Color Byte 1
06		GR13	Foreground Color Byte 2
07		GR15	Reserved
08		GR20	BitBLT Width Byte 0
09		GR21	BitBLT Width Byte 1
0A		GR22	BitBLT Height Byte 0
0B		GR23	BitBLT Height Byte 1
0C		GR24	BitBLT Destination Pitch Byte 0
0D		GR25	BitBLT Destination Pitch Byte 1
0E		GR26	BitBLT Source Pitch Byte 0
0F		GR27	BitBLT Source Pitch Byte 1
10		GR28	BitBLT Destination Start Address Byte 0
11		GR29	BitBLT Destination Start Address Byte 1
12		GR2A	BitBLT Destination Start Address Byte 2
13		GR2B	Reserved
14		GR2C	BitBLT Source Start Address Byte 0
15		GR2D	BitBLT Source Start Address Byte 1
16		GR2E	BitBLT Source Start Address Byte 2
17		GR2F	BitBLT Destination Write Mask
18		GR30	BitBLT Mode
19		–	Reserved
1A		GR32	BitBLT Raster Operation (ROP)
1B		GR33	BitBLT Mode Extension Register
1C–3F		–	Reserved
40		GR31	BitBLT Start/Status (Read/Write)
41-FF		–	Reserved

Appendix I

COLOR AND BRIGHTNESS ADJUSTMENT

I.1 Introduction

To produce a system that faithfully reproduces data (color, hue, saturation, intensity) on a computer screen, there are two main items of concern. The first item is to properly compensate for the inherent physical properties of the hardware. The second item is to provide a mechanism to deal with data streams that have been previously altered for a specific, and different, environment.

I.2 Gamma Correction Properties of CRT Monitors

For display devices, there is a nonlinear relationship between light intensity (that is, the amount of brightness and color contrast that appears on a display screen) and the applied video signal. For **CRT monitors**, this nonlinear relationship (referred to as gamma) can be expressed by the following equation, in which gamma (γ) is the exponent of the gamma-curve power-transfer function:

$$\text{Light Intensity} = (\text{Video Signal, in mV})^{\gamma}$$

To correct for gamma (that is, to compensate for the nonlinear relationship of a display device), a signal that is the inverse of the curve caused by the gamma can be applied to the recording or capturing of the source video data. The typical pre-corrected gamma curve equation is:

$$\text{Pre-corrected Light Intensity} = (\text{Video Signal, in mV})^{1/\gamma}$$

A conventional CRT monitor has the following power-law response to voltage: the intensity reproduced at the face of the display screen is approximately equal to the applied voltage, raised to the 2.5 power. This law is illustrated by the CRT monitor 'Gamma' curve shown in Figure I-1. (The gamma of a properly adjusted conventional CRT monitor varies anywhere between approximately 2.35 to 2.55. Most CRT monitors have a gamma value that is very close to the theoretical value of 2.5.)

Gamma correction can be thought of as the process of compensating for the nonlinearity of gamma in order to achieve correct reproduction of intensity on the face of the CRT monitor display screen. To compensate for this nonlinearity, an inverse power transfer function of 1/2.5 (that is, 1/gamma) is applied to the intensity, as illustrated by the '1/Gamma' curve of Figure I-1. As a result of the applied inverse power transfer function, as shown in Figure I-1, a linear response is obtained for the intensity of the applied voltage as illustrated by the 'Linear' curve.

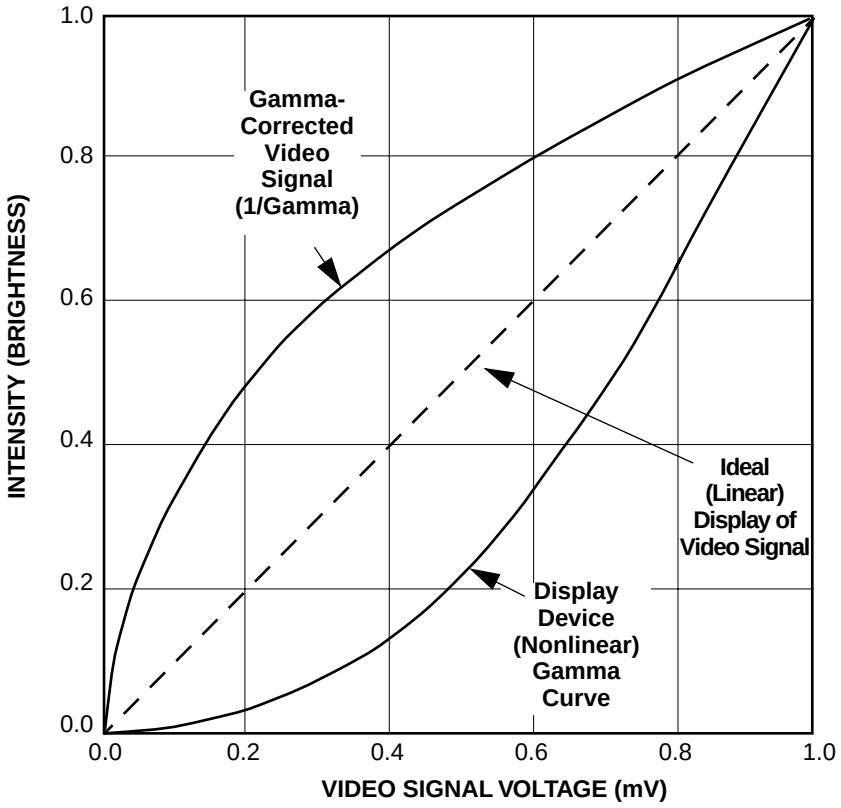


Figure I-1. CRT Monitor Gamma Curve

Typically, the largest source of variation in the nonlinearity of a CRT monitor is caused by the black level or brightness adjustment of the CRT monitor. The brightness control of a display device must first be adjusted so that black elements in the picture are reproduced correctly, before any effort is made to determine or set gamma.

The nonlinearity function of the CRT monitor is dictated by the electrostatic interaction between the cathode and the grid that controls the current of the electron beam of an electron gun. (That is, the nonlinearity function has nothing to do with the phosphor of the CRT monitor.)

I.3 Gamma Adjustment for Properties of Video Recording Media

Television and motion pictures are typically viewed in a dim environment, while computers are typically viewed in a brightly lit environment. When an image is coded according to a video standard such as NTSC/PAL, the coding implicitly assumes the image is to be viewed in a dim environment. However, if an image created for a dim environment is transmitted to a viewer in a bright environment, the image can have excessive contrast. The same video image, when viewed in a bright environment, can therefore appear dark on a computer CRT monitor and bright on a flat panel.

The assumption of a dim environment is built into the coding used by video and film cameras since typically videos and films are viewed in a dim environment. As a result, a video camera is manufactured to work with two assumptions:

- A typical CRT monitor has a 2.5 gamma.
- When an image is recorded by a video camera, the video camera under-corrects for the 2.5 gamma by using an exponent of approximately 1/2.2 instead of 1/2.5.

As shown in Figure I-2, this assumption that a video camera under-corrects for gamma can be overcome by applying an additional power transfer function that has an exponent between 1.1 and 1.2.

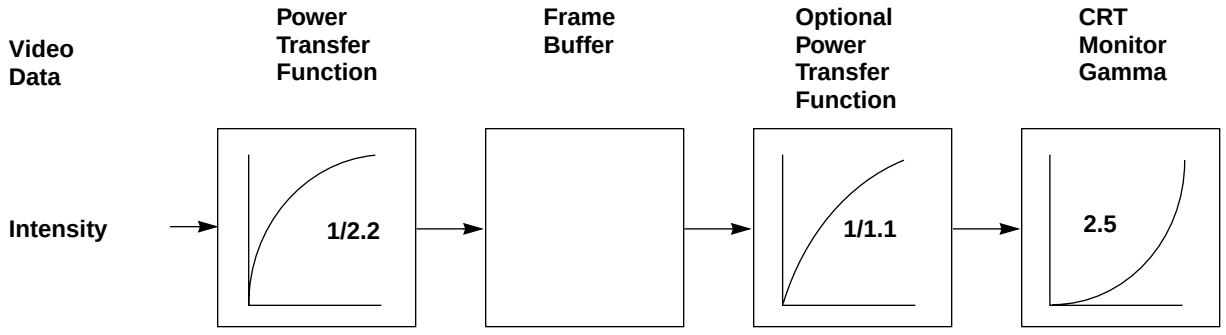


Figure I-2. How Gamma Adjustment Is Handled in Displaying Video Data

Ambient lighting is rarely taken into account in the exchange of computer images. For example, in the JPEG and MPEG standards, there is no mention of a power transfer function, but typically it is implied that the type of coding used is nonlinear (that is, video-like). Therefore, unacceptable results are obtained when JPEG or MPEG images are applied as linear data. In computer graphics standards such as PHIGS (Progammer's Hierarchical Interactive Graphic System) and CGM (Computer Graphics Metafile), there is also no mention of power transfer function. However, typically it is implied that the type of coding used is linear (that is, coding this is not video-like). As a result, without gamma correction and/or adjustment, these lighting discrepancies make it difficult to exchange and view image data between systems.

I.4 Gamma Correction for Properties of Computer Graphics Data

For computers, in general the software systems for drawing graphics on a display screen perform calculations for lighting, shading, depth cueing, and anti-aliasing by using intensity values that approximate the physical mixing of light. As shown in Figure I-3, intensity values stored in the frame buffer are corrected for gamma by hardware CLUTs (color look-up tables) on the fly as they are sent to the display screen. The power transfer function of the CRT monitor acts on the gamma-corrected signal voltages to reproduce the correct intensity values at the face of the display screen. Software systems usually provide a default gamma value and some method to change it.

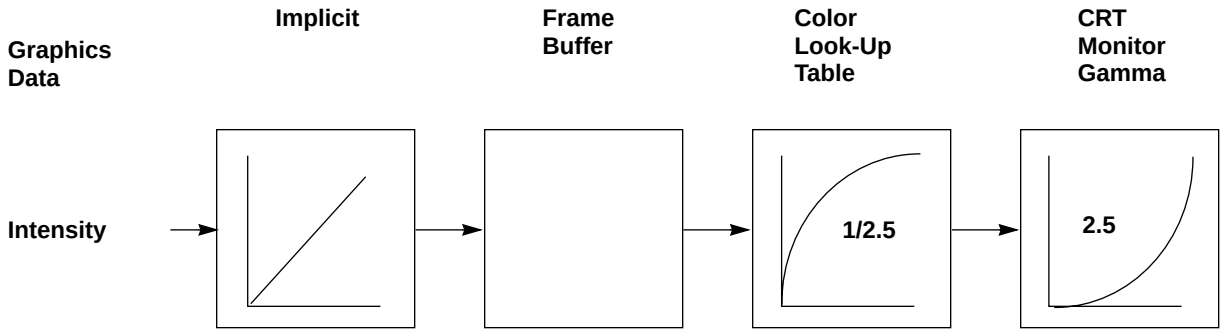


Figure I-3. How Gamma Correction is Handled in Displaying Graphics Data

The availability of a CLUT after the frame buffer on the way out to the display makes it possible for software to perform tricks, such as inverting all of the look-up table entries to flash (that is momentarily change the color that appears on the entire display screen without changing any of the frame buffer data that is being sent to the display screen).

I.5 Gamma Correction Recommendation from Microsoft

Microsoft recommends gamma correction. For example, in the *Hardware Design Guide for MicroSoft Windows® 95*, published by Microsoft Press, it states the following: "Any 24-bit and higher displays should support down loadable *random access memory digital-to-analog converter* (RAMDAC) entries to perform gamma correction in hardware". (Italics indicate emphasis added by Microsoft.)

I.6 Color and Brightness Properties of Flat Panels

Flat panels do exhibit a non-linear response to input color and brightness data. However, the variables are not as predictable as they are on CRT monitors. The color/brightness response of flat panels vary:

- By flat panel spatial resolution. For example, not all flat panels with spatial resolutions of 640 x 480, 800 x 600, or 1024 x 768 have the same color/brightness response curve.
- By flat panel types. For example, TFT and dual-scan STN panels do not have the same color/brightness response curve.
- By flat panel manufacturer. For example, there is no published documentation on color/brightness response curves from flat panel manufacturers.

The gamma curves for a CRT monitor and color/brightness response curves for flat panel differ greatly. Therefore, it is almost impossible to develop a common correction factor that would apply equally to both display types being driven be a single LCD/CRT controller. To alleviate this problem, the CL-GD7556 has included hardware resources that can be programmed for:

- Standard gamma correction factors for CRT monitors
- Common color/brightness variations between flat panels (as part of OEM manufacturing process)
- Independent control of color intensity and contrast for red, green, and blue colors on the display (by end user)
- Independent control of color intensity and contrast for all three colors in a Video Window (by end user)
- Brightness control of the graphics/background of the display (by end user)
- Brightness control of the Video Window (by end user)

I.7 CRT Monitor Gamma Correction Support by the CL-GD7556

The CL-GD7556 provides two mechanisms for gamma correction/adjustment:

- One CLUT for both High-Color graphics images (that is, 16-bit/pixel images) and True-Color graphics images (that is, 24-bit/pixel images), discussed in Section I.7.1
- Another separate and independent CLUT for video images, discussed in Section I.7.2

I.7.1 Gamma Correction/Adjustment for Graphics Images

For graphics images, as shown in Figure I-4, the CLUT consists of three separate and independent color tables, consisting of 256 eight-bit internal RAM registers for the individual primary red, green, and blue colors.

The CLUT is used for the gamma correction of the individual primary red, green, and blue colors as an image is sent to the 24-bit True-Color DAC. This CLUT is accessed by using External/General registers 3C7–3C9.

Gamma correction is available only in High-Color and True-Color modes. When there is a change from one display mode to another display mode, the VGA BIOS loads a linear default value for the gamma correction CLUT to the High-Color and True-Color modes. It is then up to the application program to modify these default values as necessary. There is independent control of the individual primary red, green, and blue colors for a particular pixel in the 15-, 16-, and 24-bit/pixel display modes.

- In 15- and 16-bit/pixel display modes, the 5 bits for red, 5/6 bits for green, and 5 bits for blue are processed to form 8 bits each. Then they all independently select from the 256 entries in each of their respective color tables.
- In 24-bit/pixel modes, the 8 bits for red, 8 bits for green, and 8 bits for blue all independently select from the 256 entries in each of their respective color tables.

In comparison, as shown in Figure I-5, for 8-bit/pixel display modes, the exact same CLUT reverts to the standard VGA compatible CLUT. The 8-bits/pixel data is used to index into one of 256 entries in the CLUT. This index is then used to select all three red, green, and blue values at one time, as they are not accessed independently.

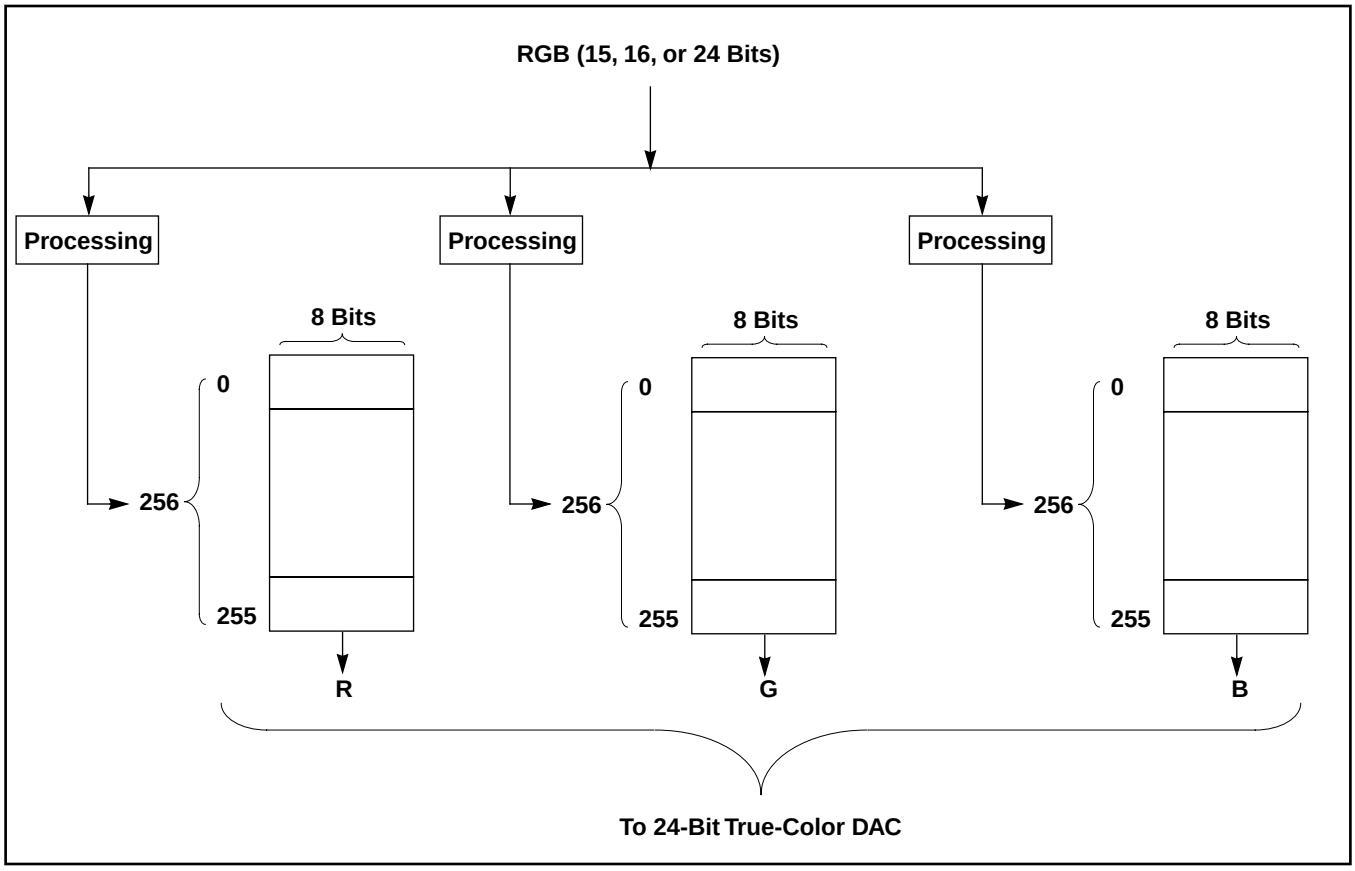


Figure I-4. Graphics Gamma Correction CLUT

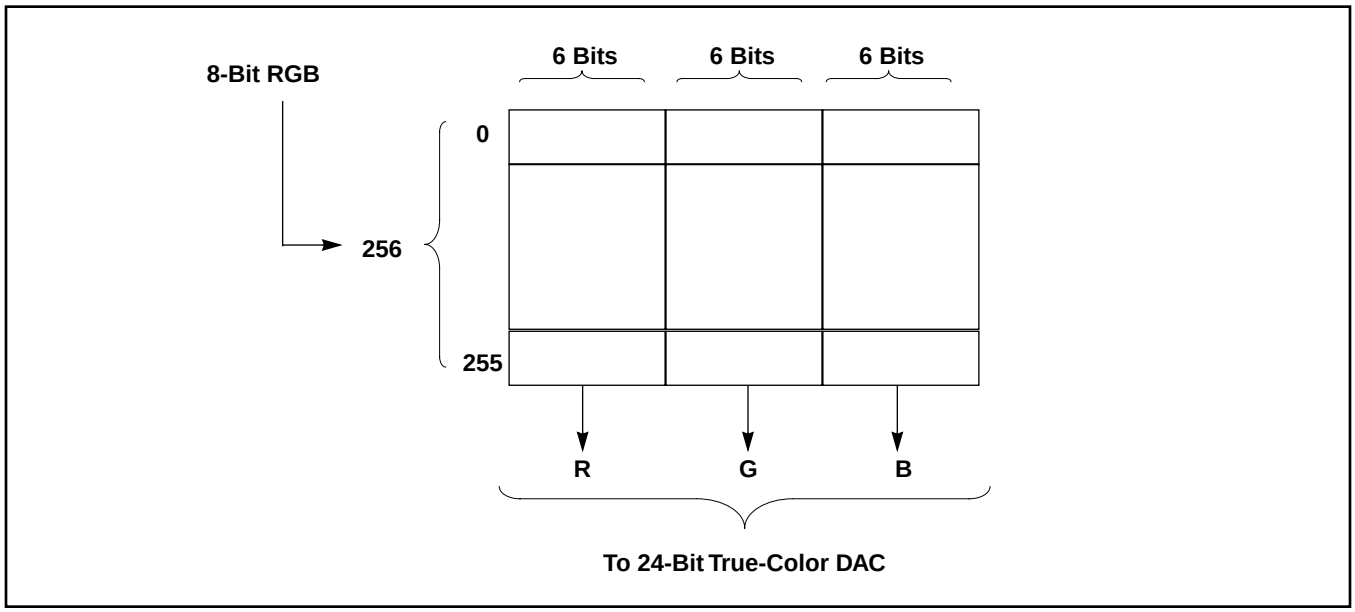


Figure I-5. Graphics 8-Bit/Pixel CLUT

Therefore, the one CLUT can be used for non-gamma corrected standard VGA 8-bit/pixel modes, as well as gamma corrected 15-/16-bit/pixel (High-Color) and 24-bit/pixel (True-Color) modes.

For 15-, 16-, and 24-bit/pixel display modes, the CL-GD7556 also has the ability to bypass this gamma correction CLUT and go directly to the 24-bit True-Color DAC. This bypass is done when Extension register GRE[7] is set to 1. During this bypass mode, the CLUT is not active and has no influence on the colors being displayed.

I.7.2 Gamma Correction/Adjustment for Video Images

The CL-GD7556 has an alternate path for handling video data. As shown in Figure I-6, the CLUT consists of three separate and independent color tables, consisting of 256 eight-bit internal RAM registers for the individual primary red, green, and blue colors. The CLUT is used for gamma adjustment of the video image as it is being sent to the 24-bit True-Color DAC. This CLUT is accessed by using External/General registers 3C7–3C9 after Extension register bit CR3F[4] has been set to 1.

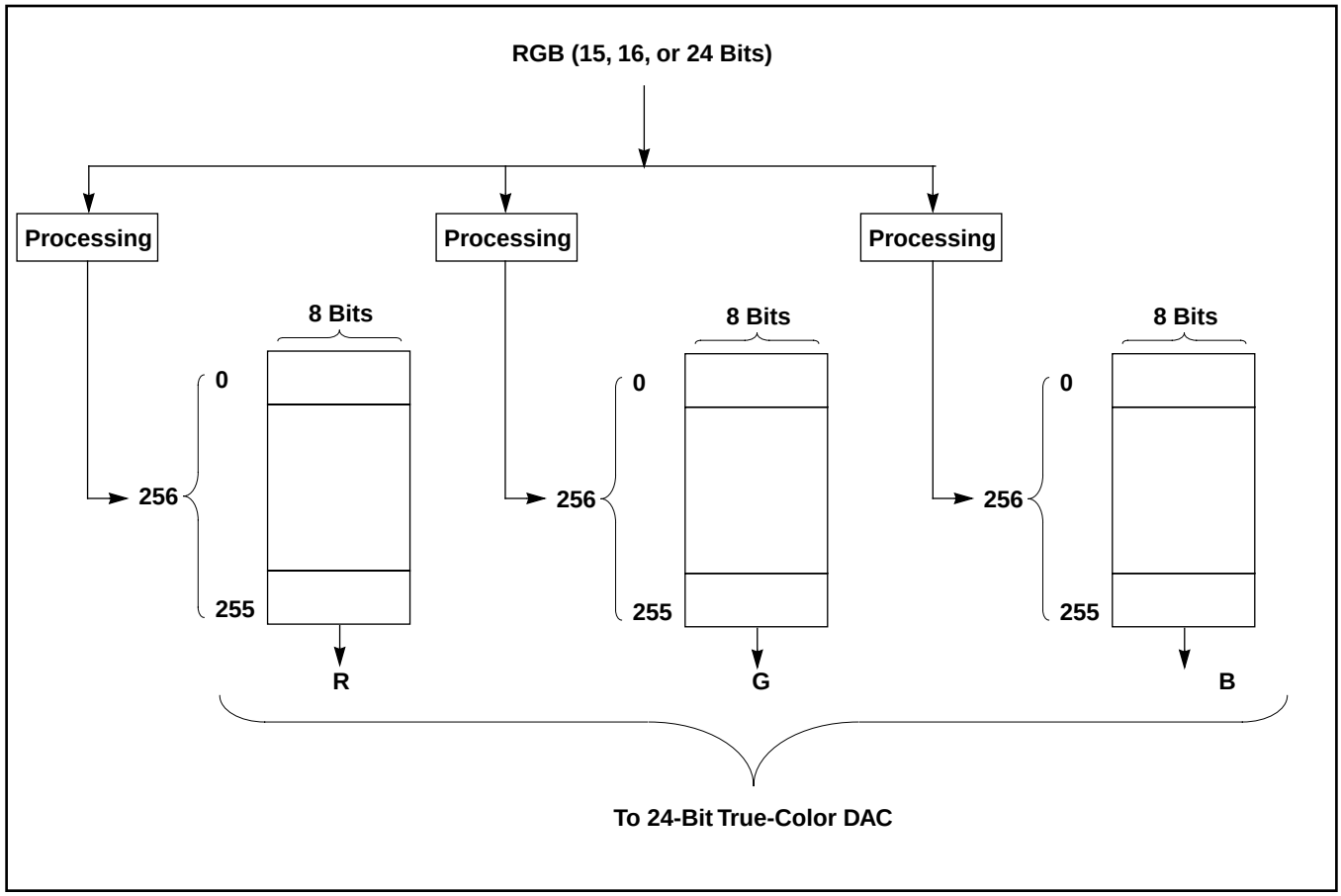


Figure I-6. Video Window Color-Adjustment CLUT

The under-corrected gamma code of the video image is removed and then the color-adjusted values in the video CLUT are applied on the fly as it is being displayed. This color adjustment mechanism is enabled when Extension register bit CR36[6] is set to 1.

When the gamma code is removed from the video image, the output dynamic voltage swing is decreased. In order to compensate for this, Extension register CR35 is programmed to increase the dynamic output voltage of the video image. This in turn adjusts the brightness of the video image for better quality viewing. This brightness register affects only the video image and does not affect the surrounding graphics image. This brightness register can also be used when gamma removal is not applied to the video image.

The two color correction/adjustment mechanisms for both graphics and video are shown in Figure I-7.

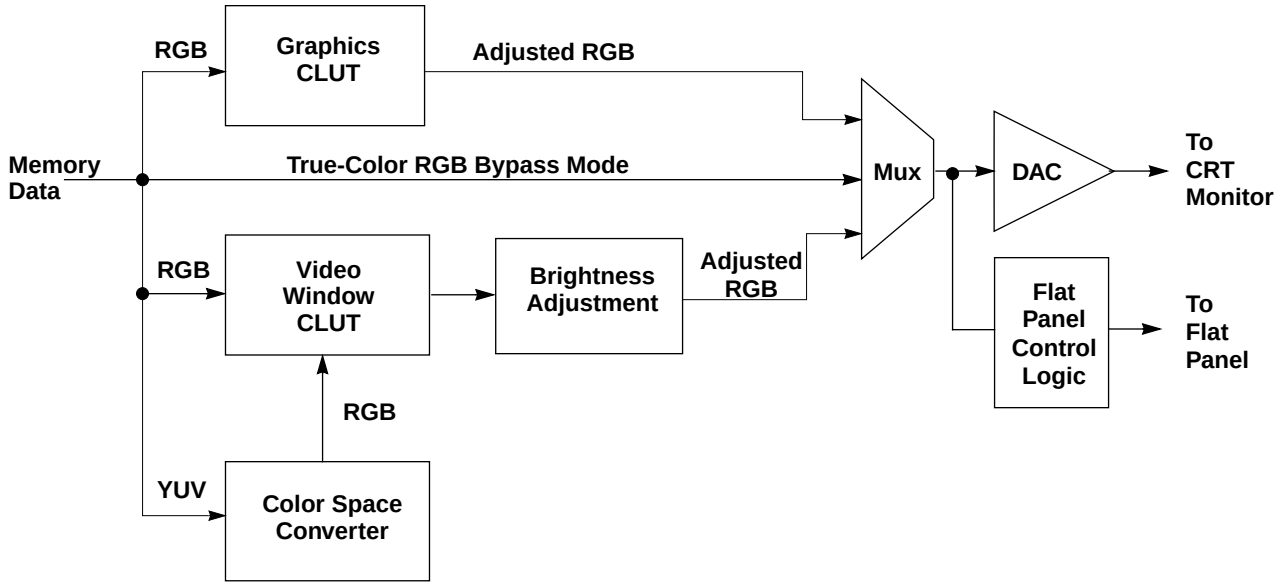


Figure I-7. Gamma Correction/Adjustment Block Diagram

I.8 Color and Brightness Control Utility

Cirrus Logic provides a 'Color Balance' utility that allows the OEM manufacturer or the end user to adjust the colors and brightness of both the graphics/background and the Video Window. These controls provide full-screen graphics and video windows that have consistently high-quality color, regardless of the type of display device being used (either CRT monitor or flat panel). Color adjustment is made by the OEM or end user with the 'Color Balance' utility to map the desired colors into both of the CLUTs. (See the *CL-GD7556 Software Reference Manual* for details).

In addition to color adjustment, the CL-GD7556 provides brightness and contrast (or luminance) adjustments for the Video Window. Extension register CR35[7:0] is programmed with a 2's compliment number that either increases or decreases the luminance value of each pixel. The 'Color Balance' utility uses this register to adjust the video display for the end user.

Notes

Appendix J

BALL-GRID-ARRAY CONTACT DEFINITIONS

Table J-1 identifies the contact positions for the CL-GD7556 PBGA package. The following definitions apply to Table J-1:

- Numbers in the 'PBGA Contact Position' column refer to a Plastic Ball-Grid-Array package.
- Numbers in the 'PQFP Pin. No.' column refer to a Plastic Quad Flat Package.
- Pins are identified with the following abbreviations and symbols:
  - I — Input function
  - O — Output function
  - I/O — A bidirectional function that is an input or output depending on the mode
  - I or O — Either an input or output, depending on the pin function selected
  - OD — An open-drain output that is electrically equivalent to open-collector
  - TS — A tristate function that is configured as either an input, output, or high-impedance
  - S-TS — A sustained-tristate output goes from an active to an inactive state and then to high-impedance
  - # — Active-low function
- Pin names ending with 'PU' have pull-up options. For information on the pull-up options, refer to section 2.8.

Table J-1. PBGA Contact Definitions

PBGA Contact Position	PQFP Pin No.	Pin Type	Pin Name
A1	255	O	OE#
A2	256	GND	VSS13
A3	254	—	No connect
A4	251	I/O	SW0 / MCLK / XMCLK
A5	247	I/O	MD21 / ROMA13
A6	243	O	WE3# / CAS3#
A7	239	Pwr	CVDD3
A8	235	I/O	MD30 / ROM32KPU
A9	231	O	MA1
A10	227	Pwr	MVDD2
A11	223	O	MA6
A12	219	I/O	MD32 / CMOSPU
A13	215	I/O	MD36
A14	211	I/O	MD40 / RIOPU
A15	207	O	WE5# / CAS5#
A16	203	I/O	MD46
A17	199	I/O	MD49
A18	195	I/O	MD53
A19	193	O	MA9
A20	191	—	No connect
B1	1	—	No connect
B2	2	—	No connect
B3	253	O	EROM#
B4	250	Pwr	MAVDD
B5	246	I/O	MD22 / ROMA14
B6	242	I/O	MD24 / SW1PU
B7	238	I/O	MD27 / SCANPU
B8	234	I/O	MD31 / BIOSPU
B9	230	O	MA2
B10	226	O	CAS# / WE#
B11	222	O	MA7
B12	218	I/O	MD33 / TMPU
B13	214	I/O	MD37
B14	210	I/O	MD41
B15	206	I/O	MD43
B16	202	I/O	MD47
B17	200	Pwr	MVDD3
B18	196	I/O	MD52
B19	194	O	RAS1#
B20	192	GND	VSS10
C1	3	I/O	MD18 / ROMA10
C2	4	I/O	MD17 / ROMA9
C3	5	I/O	MD16 / ROMA8

Table J-1. PBGA Contact Definitions *(cont.)*

PBGA Contact Position	PQFP Pin No.	Pin Type	Pin Name
C4	249	I/O	MD19 / ROMA11
C5	245	I/O	MD23 / ROMA15
C6	241	I/O	MD25 / SW2PU
C7	237	I/O	MD28 / INTPU
C8	233	GND	VSS12
C9	229	O	MA3
C10	225	O	MA4
C11	221	O	MA8
C12	217	I/O	MD34 / MMIOPU
C13	213	I/O	MD38
C14	209	I/O	MD42
C15	205	I/O	MD44
C16	201	I/O	MD48
C17	198	I/O	MD50
C18	197	I/O	MD51
C19	189	O	WE6# / CAS6#
C20	190	—	No connect
D1	7	I/O	MD14 / ROMA6
D2	8	Pwr	MVDD1
D3	6	I/O	MD15 / ROMA7
D4	252	GND	MAVSS
D5	248	I/O	MD20 / ROMA12
D6	244	O	WE2# / CAS2#
D7	240	I/O	MD26
D8	236	I/O	MD29 / XCLKPU
D9	232	O	MA0
D10	228	O	RAS0#
D11	224	O	MA5
D12	220	GND	VSS11
D13	216	I/O	MD35
D14	212	I/O	MD39
D15	208	O	WE4# / CAS4#
D16	204	I/O	MD45
D17	188	O	WE7# / CAS7#
D18	185	I/O	MD56
D19	186	I/O	MD55
D20	187	I/O	MD54
E1	11	I/O	MD11 / ROMA3
E2	10	I/O	MD12 / ROMA4
E3	9	I/O	MD13 / ROMA5
E4	12	I/O	MD10 / ROMA2
E17	184	I/O	MD57
E18	181	I/O	MD60

Table J-1. PBGA Contact Definitions *(cont.)*

PBGA Contact Position	PQFP Pin No.	Pin Type	Pin Name
E19	182	I/O	MD59
E20	183	I/O	MD58
F1	15	O	WE1# / CAS1#
F2	14	I/O	MD8 / ROMA0
F3	13	I/O	MD9 / ROMA1
F4	16	O	WE0# / CAS0#
F17	180	I/O	MD61
F18	177	GND	VSS9
F19	178	I/O	MD63
F20	179	I/O	MD62
G1	19	I/O	MD5 / ROMD5
G2	18	I/O	MD6 / ROMD6
G3	17	I/O	MD7 / ROMD7
G4	20	I/O	MD4 / ROMD4
G17	176	O	FP17
G18	173	O	FP14
G19	174	O	FP15
G20	175	O	FP16
H1	23	I/O	MD1 / ROMD1
H2	22	I/O	MD2 / ROMD2
H3	21	I/O	MD3 / ROMD3
H4	24	I/O	MD0 / ROMD0
H17	172	O	FP13
H18	169	O	FP11
H19	170	O	FP12
H20	171	GND	VSS8
J1	27	I/O	AD30
J2	26	I/O	AD31
J3	25	GND	VSS1
J4	28	I/O	AD29
J17	168	O	FP10
J18	165	Pwr	FPVDD1
J19	166	O	FP8
J20	167	O	FP9
K1	31	I/O	AD26
K2	30	I/O	AD27
K3	29	I/O	AD28
K4	32	I/O	AD25
K17	164	O	FP7
K18	161	O	FP4
K19	162	O	FP5
K20	163	O	FP6
L1	35	I/O	AD22

Table J-1. PBGA Contact Definitions *(cont.)*

PBGA Contact Position	PQFP Pin No.	Pin Type	Pin Name
L2	34	I/O	AD23
L3	33	I/O	AD24
L4	36	Pwr	BVDD2
L17	160	O	FP3
L18	157	O	FP0
L19	158	O	FP1
L20	159	O	FP2
M1	39	I/O	AD19
M2	38	I/O	AD20
M3	37	I/O	AD21
M4	40	I/O	AD18
M17	156	O	LFS
M18	153	O	LLCLK
M19	154	GND	VSS7
M20	155	O	FPVDCLK
N1	43	TS	INTR#
N2	42	I/O	AD16
N3	41	I/O	AD17
N4	44	Pwr	CVDD1
N17	152	O	FPDE
N18	149	O	FP34
N19	150	O	FP35
N20	151	Pwr	FPVDD2
P1	47	TS	DEVSEL#
P2	46	I/O	PAR
P3	45	TS	STOP#
P4	48	TS	TRDY#
P17	148	O	FP33
P18	145	O	FP30
P19	146	O	FP31
P20	147	O	FP32
R1	51	I	IRDY#
R2	50	I	CLK
R3	49	GND	VSS2
R4	52	I	FRAME#
R17	144	O	FP29
R18	141	O	FP27
R19	142	GND	DACVSS2
R20	143	O	FP28
T1	55	I	RST#
T2	54	I	OSC / XVCLK
T3	53	I	IDSEL
T4	56	I	SUSPI

Table J-1. PBGA Contact Definitions *(cont.)*

PBGA Contact Position	PQFP Pin No.	Pin Type	Pin Name
T17	140	O	FP26
T18	137	O	FP23
T19	138	O	FP24
T20	139	O	FP25
U1	59	I/O	C/BE2#
U2	58	I/O	C/BE3#
U3	57	I/O	CLK32K / SUSPST#
U4	60	I/O	C/BE1#
U5	76	I/O	AD6
U6	80	I/O	AD3
U7	84	I/O	AD0
U8	88	I	VPC2
U9	92	I	VPC6
U10	96	I	VPY2
U11	100	I	VPY4
U12	104	I	DDCD
U13	108	I	VACTI
U14	112	TS	HSYNC
U15	116	Ref	IREF
U16	120	O	BLUE
U17	124	O	FPDECTL
U18	134	Pwr	DACVDD2
U19	136	O	FP22
U20	135	O	FP21
V1	62	—	No connect
V2	61	I/O	C/BE0#
V3	69	I/O	AD13
V4	70	I/O	AD12
V5	73	I/O	AD9
V6	77	Pwr	BVDD1
V7	81	I/O	AD2
V8	85	GND	VSS4
V9	89	I	VPC3
V10	93	I	VPC7
V11	97	I	VPY3
V12	101	I	VPY5
V13	105	Pwr	VAVDD
V14	109	Pwr	DACVDD1
V15	113	GND	DACVSS1
V16	117	Pwr	CRTVDD
V17	121	O	GREEN
V18	133	O	FP20
V19	132	O	FP19

Table J-1. PBGA Contact Definitions *(cont.)*

PBGA Contact Position	PQFP Pin No.	Pin Type	Pin Name
V20	131	O	FP18
W1	64	GND	VSS3
W2	66	—	No connect
W3	68	I/O	AD14
W4	72	I/O	AD10
W5	74	I/O	AD8
W6	78	I/O	AD5
W7	82	Pwr	CVDD2
W8	86	I	VPC0
W9	90	I	VPC4
W10	94	I	VPY0
W11	98	OD	VCLK0 / DDCC
W12	102	I	VPY6
W13	106	I	HREFI
W14	110	I	VSI
W15	114	TS	VSYNC
W16	118	—	No connect
W17	122	O	RED
W18	125	O	FPVCC
W19	130	—	No connect
W20	129	O	PROG2
Y1	63	I	ACTI
Y2	65	—	No connect
Y3	67	I/O	AD15
Y4	71	I/O	AD11
Y5	75	I/O	AD7
Y6	79	I/O	AD4
Y7	83	I/O	AD1
Y8	87	I	VPC1
Y9	91	I	VPC5
Y10	95	I	VPY1
Y11	99	GND	VSS5
Y12	103	I	VPY7
Y13	107	GND	VAVSS
Y14	111	I	VPCLKI
Y15	115	Ref	VREF
Y16	119	O/I	PROG1 / TWR#
Y17	123	O	FPVEE
Y18	126	—	No connect
Y19	128	GND	VSS6
Y20	127	O	PROG0

GLOSSARY

This section contains definitions of terms used in this manual.

--Numbers--

3-colors-and-transparent mode: See the entry **"three-colors-and-transparent mode"**.

4-color-mode: See the entry **"three-colors-and-transparent mode"**.

16M: 2^{24} or 16,777,216

32K: 2^{15} or 32,768

64K: 2^{16} or 65,536

256/256K: A way of notating: first, the amount of data going into a CLUT RAM (2^8 bits, or 256 bits), and second, the amount of data coming out of the CLUT RAM (2^{18} bits, or 256K bits). In a system, this indicates that 256 colors can be selected from a palette of 256K possibilities. The palette is usually pre-programmed to account for user preferences or gamma correction.

256K: 2^{18} or 262,144

--A--

AccuPak™: A 8-bit color space format output option (that is, a method of compressing video from 16 bits to 8 bits) that is used by software decoders such as the CL-PX4072. AccuPak is proprietary to Cirrus Logic.

active matrix: A type of display device that provides for fast response to changes in the data being displayed. Active matrix display devices have a thin-film transistor at the site of each pixel, that is, for each pixel that appears on a display screen. This term is often used with, or in place of, the acronym 'TFT'.

add-in daughterboard: A circuit board that plugs into a computer motherboard to provide additional functionality. It often connects to an external device, such as a CRT monitor or storage subsystem.

address: A label identifying a memory or register location where information is stored.

addressing: Accessing information at a given location or using a specific technique.

anti-aliasing: A process that uses an algorithm to smooth the transition between adjacent pixels, thereby reducing the stair-step effect that otherwise results when decompression/expansion takes place.

aperture: A logical partition (that is, a 'logical' view) of display memory that is allocated for a specific function.

application program interface: An interface that allows applications to make calls to a library of program functions.

artifact: A flaw that appears in a display image as a result of a physical disruption of the display image. Examples of artifacts include unwanted flicker, noise, spotting, contouring, or other pattern motion.

aspect ratio: The ratio of the width of a display screen to the height of a display screen. The aspect ratio, along with the number of scanlines that make up the image on the display screen, determines what sample rate must be used to digitize a video signal.

attribute controller: The IBM historical term for a display device controller. The standard attribute controller, now just a block within a display device controller, formats the display image for the display screen. It controls for such attributes as the color selection for the display screen, text blinking, underlining, and alternate font selection.

audio-video interleaved: A type of multimedia file that interleaves first, a frame of audio data followed by a frame of video data; and second, a second frame of audio data followed by a second frame of video data; and so forth.

--B--

back porch: The area of a display device waveform that is between (1) the end of the active signal and (2) the leading (that is, rising) edge of the horizontal sync signal.

ball grid array: A layout scheme for a semiconductor package that has multiple rows and columns of ball-like pads on the bottom of the package. The pads are used to solder the package to a circuit board. Similar to a pin-grid-array, but without the pins.

banding: A display image artifact in which the image has distinct blocks (or 'bands') of colors instead of a smooth transition of coloring.

bandwidth: The maximum rate of usage of a resource for a particular operation. Also, the range of frequencies within which performance, with respect to some characteristic, falls within specified limits. With respect to the throughput of data, bandwidth is usually measured in quantities of data bits per second.

big-endian/little-endian: Two types of byte-order sequence for the four contiguous bytes of data that make up a doubleword. The big-endian sequence is used by Motorola CPUs. The little-endian sequence is used by DEC computers Intel CPUs.

- Big-endian sequence: byte 4 (bits 31–24), byte 3 (bits 23–16), byte 2 (bits 15–8), and byte 1 (bits 7–0)
- Little-endian sequence: byte 2 (bits 15–8), byte 1 (bits 7–0), byte 4 (bits 31–24), and byte 3 (bits 23–16)

BIOS: A 'basic input/output system' is a collection of subprograms that control the transfer of characters between a microprocessor and other devices. (See also the entries **"BIOS ROM**,**" "ROM BIOS"**, **"System BIOS"**, and **"VGA BIOS"**.)

BIOS ROM: Usually an EPROM chip that holds a BIOS code.

BIOS-level compatibility: With regard to a VGA subsystem, refers to the minimum level of compatibility necessary for a VGA BIOS to accommodate the majority of standard IBM VGA applications.

bit map: A rectangular array of display memory locations, each of which is associated with a pixel on a display device. The contents of each location determines the color of the pixel. Frequently, there are more locations in the bit map than appear on the display screen, allowing images to be maintained for later presentation.

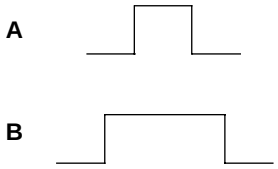
BitBLAST: A bit block accelerated setup transfer operation in which the BitBLT control registers are duplicated, and a status bit is provided. Application programs can monitor this status bit to determine when to program the parameters for a new BitBLT operation. This programming is done before the current BitBLT completes execution, in a second set of registers that are transparent to the software.

BitBLT: (bit-block transfer) A type of graphics drawing routine that transfers a rectangular block of bit-mapped data from a source location to a destination area. That is, a BitBLT moves data from either (1) one area of display memory to another area of display memory or (2) from system memory to display memory. The CL-GD7556 has hardware to help speed BitBLT operations.

BitBLT engine: The hardware logic block that performs BitBLT routines.

blanking: On a CRT monitor, the beam that causes light to appear on the CRT monitor display screen is said to undergo blanking (that is, made so that it does not appear) during the non-active parts of each scanline and during each horizontal and vertical retrace.

bracket: Refers to a signal that, in comparison to another signal, has a leading edge that precedes the leading edge of the other signal and that has a trailing edge that follows the trailing edge of the other signal. In the figure that follows, signal B brackets signal A.



brightness: The amount of light that appears on a display screen. Brightness is also called ‘intensity’.

brightness adjustment: A technique for adjusting the brightness of a video signal that appears on a display device. Also, a technique that is used to compensate for the loss of dynamic output voltage swing for a video signal that has undergone gamma removal.

buffer: An interim register or register stack that provides a means of speeding the transfer of data. The buffer stores and releases data faster than some other device (such as a hard disk drive) can normally handle the data transfer.

bus master: The device that takes control of the current bus transaction, in a system in which control of data transfers on the bus is shared between the host CPU and associated peripheral devices. The bus master receives and grants requests for service from other devices that are connected to the bus.

byte: A group of eight bits, addressed as a unit.

byte swapping: Converting bytes of data from one type of order to another type of order. For example, with byte swapping, a byte that has a little-endian order could be made to change to a big-endian order.

--C--

capture: See the entry **"video capture"**.

CCIR 601: The recommendation developed by the CCIR (International Radio Consultive Committee) to digitize color video signals.

CGA controller: The first color display device controller available for IBM-compatible computers. The CGA has a low resolution and color depth. While the CGA is generally considered obsolete, the display modes originally designed for the CGA are included in the VGA standard to which the CL-GD7556 adheres.

chain 4: A type of packed-pixel mode in which four display memory maps are 'chained' together into one large bit plane. A byte is therefore read from bit planes 0, 1, 2, and 3. In chain-4 addressing, consecutive pixels are stored at every fourth byte address in display memory. (See also the entry **"packed pixel"**.)

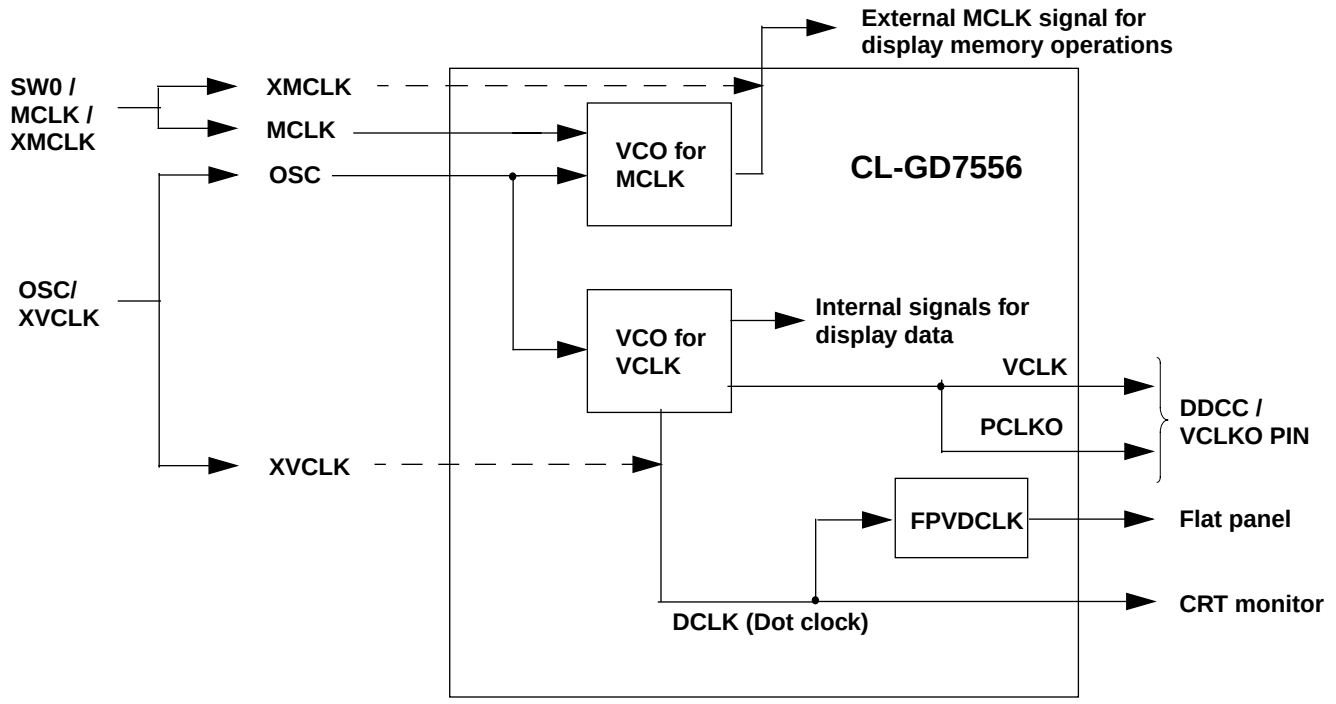
character cell: In text display mode, an area of the display screen that displays one character. For VGA text display modes, character cells are either 8, 9, 12, or 16 pixels wide and either 8, 14, or 16 pixels high.

character clock: A clock that is generated by dividing the VCLK by either 8 or 9. The CRT monitor timing signals (HSYNC, VSYNC) are derived by dividing the character clock.

chroma key: A method of combining two sources of data so that one display image area is replaced with another display image area. This method specifies an YUV color space or a range of colors, which are used to indicate what area cannot be copied from display memory and which therefore is not visible on a destination area. This method allows another display image to replace the blanked-out area. (See also the entry **"transparent BitBLT"**.)

chrominance: The color component of a 2-channel video signal. (See also the entry **"luminance"**.)

clock: The diagram below shows some of the clock signals for the CL-GD7556. For more information, refer to the pin description chapter, Chapter 2, and see the entries **"dot clock", "MCLK"**, **"SCLK"**, and **"VCLK"**, and **"video clock"**.



CLUT RAM: The CLUT RAM is also known as the 'color palette RAM'. For the CL-GD7556, there are two on-chip random-access memory areas that are used for a color look-up table that is up to 24 bits wide and 256 deep. The graphics CLUT provides color data for the normal display modes. The Video-Window CLUT provides color data for the video window, when it is enabled.

codec: A coder/decoder mechanism for coding and decoding data.

color depth: The number of colors that can appear simultaneously on a display screen. (Also called 'color resolution' or 'bit depth'.)

- For a flat panel, color depth refers to the upper physical limit of a flat panel display screen for displaying simultaneous shades of colors.
- For a display mode, color depth refers to the number of colors that the display mode allows to appear simultaneously on a display screen. The number is determined by the number of bits associated with each pixel in display memory. If *n* bits per pixel are used, 2^n colors can appear simultaneously on a display screen.

color expansion: The automatic conversion of a monochrome bit map (which typically defines a character, icon, or pattern) into foreground and background color values. When a source bit has a value of 0, the bit is converted into a background color value. When a source bit has a value of 1, the bit is converted into a foreground color value.

color intensity: The brightness with which a color appears on a display screen, as determined by the CLUT setting for that color.

color key: The CL-GD7555 has the capability of overlaying computer-generated graphics, on a pixel-by-pixel basis, with external video. The method of determining whether to overlay a pixel involves comparing a color key with a specific RGB color space. When the graphics data match the color key, the graphics data are replaced with the external video.

color keying: The process of using either a specific red, green, or blue color or a color space format to 'key' (that is, define) an area of data that is to be manipulated or changed.

color look-up table: An on-chip CL-GD7556 table that translates color information from the display memory into color information for a display device.

color mode: A type of display mode that uses 2, 4, 8, or more bits per pixel.

color palette: See the entry **"palette"**.

color planes: In planar modes, refers to four independent planes of display memory, with each plane dedicated to controlling one color component (red, green, blue) and intensity.

color space format: The mathematical representation for a color. Examples of color space formats include the RGB, YIQ, and YUV color space formats.

comparator: A hardware unit that is used to perform an arithmetic or logical comparison between two fields that are typically the same width. Arithmetic comparisons include "equal", "greater than", and "less than". Logical comparisons generally use matching techniques to establish an identity.

compression: A process that uses algorithms to reduce the amount of data that is to be stored or sent so that the data requires a lesser amount of memory or a smaller bandwidth of memory.

contouring: A display image artifact, in which the image develops curving lines that appear as in a geographical contour map. Contouring results when there are not enough bits available to represent the display image.

contrast: Refers to the ratio between the maximum luminance and the minimum luminance. To calculate a meaningful ratio, all ambient and display mode parameters must be defined, as well as the type of display device. Ambient light, contrasting colors (that is black vs. white, or one color vs. another color) and viewing angle can greatly affect the contrast ratio.

controller: A hardware unit that performs all the control functions required for the flow of data through one or more interfaces to other parts of a system.

crosstalk: Undesired energy that appears in one signal path as a result of cross coupling with other signal paths.

CRT monitor: The type of display device, currently used with most desktop personal computers, that uses a cathode ray tube to display data.

--D--

DAC: A device that converts digital signals to continuous analog signals. An example of a DAC is the palette DAC. (See also the entry **"palette DAC"**.)

data compression: A reduction in the number of bits of digital information that is needed to convey some given amount of information.

decoder, MPEG: A device that splits an MPEG data stream into its component parts of YUV video, audio, and timing information. An MPEG decoder decompresses data that has been previously compressed with an encoder.

decoder, video: A NTSC/PAL/SECAM device for converting video data to the YUV color space format.

depth cueing: A type of shading that makes possible a 3D effect.

desktop replacement: A term that refers to a notebook computer that, because of its advanced computing and display capabilities, replaces or even surpasses the use of a desktop computer.

destination pitch: The scanline-to-scanline byte address offset of the areas involved in a BitBLT.

digital-to-analog converter: In a VGA subsystem, a hardware unit that converts the digital levels of 6 or 8 bits per primary red, green, or blue color to analog levels suitable for an analog interface.

Direct Color: A type of packed-pixel, color, extended VGA display mode that results in color data going directly to the DAC (that is, the data does not go through the CLUT before going to the display screen). The two types of Direct Color modes are the High Color and True Color modes.

direct connection: A type of connection in which one unit of hardware is connected to another unit of hardware without requiring any external logic.

Display Control Interface: An Intel/Microsoft specification for a mechanism that eliminates some of the layers involved in using the Windows Graphics Device Interface so that video decompression and playback is more efficient.

display data: Data that appears on a display device. Display data can be either graphics data or video data. (See also the entries **"graphics"** and **"video"**.)

Display Data Channel: A VESA protocol proposal for a serial interface between a computer display and the host CPU system.

display device: A unit for showing the visual representation of data (such as a PC CRT monitor, a notebook computer flat panel, or a television screen).

display device controller: A hardware unit that performs all the control functions required for the flow of data between these elements of a computer: host CPU, display memory, and a display device. Examples of display device controllers include the CGA and EGA controllers (which are mostly obsolete) and the VGA and SVGA controllers.

display image: The visual material that appears on a display screen.

display memory: The area in computer memory where the information used to update the display screen is kept. For standard IBM compatibility, the range of addresses for display memory is A000:0h through BFFF:Fh.

display mode: A way of presenting data on a display screen. For IBM compatibility, there have been defined a number of standard VGA display modes, including both graphics display modes (also known as 'all-points-addressable modes') and text display modes (also known as 'alphanumeric display modes'). In addition to the standard VGA display modes, third-party vendors have introduced many extended VGA display modes.

Display Power Management Specification: A VESA proposal to standardize on a common definition and methodology in which display device controllers send to display devices a signal that enables the display device to enter various power management states.

display screen: The face of a display device, on which visual material is shown.

display screen refresh: The process of continuously redrawing images on the display screen of a display device. An image drawn on a display device remains visible only for as long as the persistence of a display screen illuminating element. (For example, for a CRT monitor, the persistence of the phosphor is only a few milliseconds). Different types of display devices use different display screen refresh rates, but to avoid visible screen flickering, for a flat panel the refresh rate is typically between 60 and 80 Hz. A common refresh rate is 75 Hz. In general, the higher the refresh rate, the more stable the display screen image appears to be.

display time: The period during which data appears on a display screen.

dithering: The technique of modulating a signal spatially within a frame to increase the number of shades of color. This technique is effective over large areas but fails if an area is too small. This technique creates the appearance of more colors at the expense of resolution. Also called 'spatial dithering'.

dithering engine: A hardware logic block that uses an algorithm to obtain color resolutions beyond the inherent capability of a flat panel. In contrast to the frame rate control technique, which uses multiple frame rates to achieve color resolutions, the dithering engine technique uses a group of pixels in one frame to achieve color resolutions.

dithering matrix: The number of bits for each primary red, green, and blue color.

dot clock: The internal signal that operates at the pixel rate. The dot clock is sometimes called the 'pixel clock' or 'VCLK'. For a block diagram that relates some of the CL-GD7556 clock signals, see the entry **"clock"**.

double buffering: The process of using two frame buffers so that while the data in the first buffer appears on a display screen, the data in the second buffer is being operated on. After the operation completes on the data in the second buffer, the data in the second buffer appears on the display screen, and the data in the first buffer is then operated on, and so forth.

doubleword: A doubleword is 32 bits (that is, 4 bytes).

downscaling: See the entry **"scaling"**.

DRAM: A memory technology that uses a single transistor/single capacitor cell for each memory location within a random-access matrix. DRAM technology is characterized by high density, low power, and low cost. DRAMs must be dynamically refreshed continuously to avoid loss of data.

driver: A software module that interfaces a particular display device to an application program to allow the display device to operate at a higher resolution than allowed by a standard VGA display mode.

dual-page mapping: A mode for mapping two 32-Kbyte segments of display memory into the host CPU address range. This type of mapping uses both Display Memory Offset registers 0 and 1 (that is, Extension registers GR9 and GRA) to relocate the start page address on either 4-Kbyte or 16-Kbyte boundaries. Dual-page mapping, which allows for the block transfer of data by the host CPU, is superseded by BitBLT engine technology.

DYUV: A Cirrus Logic proprietary algorithm for compressing YUV data for the V-Port™ and video windows.

--E--

echo: The return of a sufficient portion of a transmitted signal so as to be recognizable due to reflection. An echo check is a type of readback error-control technique in which the original message that was sent is also returned to verify that the message was received correctly.

edge-sharpening technology: A mechanism for eliminating the fuzzy edges (that is, edges that are ragged or unclear) that often occur when interpolation is used for upscaling. This technology senses when the edges need to be sharpened and automatically substitutes replication for interpolation.

EGA controller: The second color display device controller available for IBM-compatible computers. While the EGA is generally considered obsolete, the display modes originally designed for the EGA are included in the VGA standard to which the CL-GD7556 adheres.

emulation: Simulation of unavailable hardware by available hardware and software. Emulations improve the usefulness of a product by making it compatible with other products. EGA is capable of emulating MDA and sometimes CGA and Hercules. VGA is capable of emulating EGA, CGA, and MDA.

encoder: A device for changing the format of data to make it easier to send or easier to display.

enhanced write mode: An Extended Write mode that has had an additional layer of programming added for new options.

EPROM: An erasable, programmable read-only nonvolatile memory storage device. An EPROM that can be written once (per erasure cycle) and read many times. It can be erased by using an ultraviolet light, and it is programmed with a special programming device. An EPROM can be used to hold the VGA BIOS. (See also the entry **"VGA BIOS"**.)

extended-data out: A DRAM technology that is characterized by multiple short page-mode CAS# cycle times relative to the corresponding RAS# cycle times. The paged CAS# cycles are contiguous, in that between data reads, the CAS# cycles do not go to an inactive state.

external decoder: An off-chip decoder. (Refer to the entry **"decoder"**.) An example of an external decoder is the CL-PX4072.

--F--

falling edge: See the entry **"leading edge"**.

fast-page mode: A read or write mode of DRAMs that is characterized by a decrease in cycle time of about 2–3 times and a corresponding increase in performance. The data accessed in fast-page mode cycles must be adjacent in memory.

FasText™ Mode: An automated paged-memory font access for display modes. FasText mode is a user-selectable option that configures the font memory so that page-memory accesses are used instead of random-memory accesses to fetch the font data during display time.

Feature Connector: A VGA subsystem expansion connector that can be used to accept or drive video signals to or from the VGA subsystem. The Feature Connector, also called the VESA Pass-Through Connector, is used in applications involving video overlay. This feature is not supported in the CL-GD7556.

field: In reference to a register, a field is a group of data, such as bits in one or more registers, that can be treated as a single unit. In reference to a CRT monitor, a field contains a number of scanlines for a display screen, and two fields make up an entire frame.

FIFO: A first-in first-out memory system that can temporarily hold data so that the device that is sending the data can send it faster than the device that is receiving the data can accept it. The sending and receiving devices typically operate asynchronously.

flash: A momentary change of the color that appears on the entire display screen and that occurs without changing the data that is being sent to the display screen. This effect is often used in game application programs.

flat panel: The display device associated with notebook computers. Most flat panels use liquid crystal display technology.

flicker: A type of artifact that occurs when the refresh rate for the display screen is too low. Flicker appears on a display screen as quick on-off flashes of light intensity.

four-color-mode: See the entry **"three-colors-and-transparent mode"**.

frame: A single momentary image of display data.

frame buffer: The memory that is used to hold the frame of data for the image that appears on a display screen.

frame data rate: A measure of video speed, that is, the number of frames per second that the source of video data needs to repaint the display screen with a new frame of data. For example, for a computer using video data from the NTSC system, the display screen is repainted once every 30th of a second, for a frame data rate of 30 frames per second. If a frame data rate is too fast, artifacts can appear on a display screen. If a frame data rate is too slow, video can appear to have excessive jerking. Also called the 'frame rate'.

frame rate conversion: The process of converting one frame data rate to another frame data rate.

frame rate modulation: An algorithm that create shades of color on color dual-scan STN flat panels. The algorithm modulates the 'on' and 'off' times of individual pixels in the flat panel over multiple frames, such that the eye integrates the super-imposed pixels as perceptible color shades.

free running: A clock signal that is active at all times.

frequency synthesizer: An electronic circuit that can generate a number of stable frequencies from a fixed reference frequency.

full-motion video: Video data that appears on a display screen as smooth and natural, without excessive jerking.

full-screen: The full height and width of a display screen. The term 'full-screen' is often used in reference to the area on the display screen that is active.

--G--

gamma: The numerical value of the exponent of the output intensity power transfer function of a display device. Also, refers to the fact that the response of a display device system is non-linear in nature. (See also the entries **"brightness adjustment"**, **"gamma adjustment"**, **"gamma correction"**, and **"gamma removal"**.)

gamma/color adjustment: For a video image, a technique that uses a separate and independent CLUT to modify the RAM response between the voltage applied to the output intensity power transfer function and the intensity of the display device.

gamma correction: For a graphics image, a technique that uses a separate and independent CLUT RAM to compensate for the differences in the output intensity power transfer functions of the voltage applied to the output and the intensity power transfer function of the display device.

gamma removal: For a display device, a technique for linearizing the output intensity power transfer function by removing the gamma effect.

graphics: Refers to the type of display data (both textual and graphical data) that appears on a computer display screen as a result of computer application programs. This type of data, which is also called 'surrounding graphics', is in contrast to video data. (See also the entry **"video"**.)

graphics controller: Within a display device controller, a section of circuitry that can provide a hardware assist for drawing algorithms by performing logical functions on display memory data that is being sent to the display screen.

graphics data: See the entry **"graphics"**.

graphics display mode: A display mode in which all pixels on the display screen can be controlled independently to draw graphics objects (as opposed to text display mode, in which only a pre-defined set of characters can be displayed).

graphics memory: The on-screen memory area for storing data for standard and extended VGA display modes.

graphics window: The part of the display screen upon which graphics data is displayed. Unless video data is displayed within a video window, the graphics window takes up the entire display screen. (See also the entry **"video window"**.)

green PC: A personal computer that has been designed for minimum power consumption.

--H--

hardware occlusion: The process of accomplishing occlusion through hardware, that is, by using either the chroma key or color key replacement techniques. (See also the entry **"occlusion"**.)

HDR: The Hidden DAC register, which is 'hidden' because it shares its I/O address with External/General register 3C6.

High Color: A type of Direct Color packed-pixel mode in which each pixel is represented by either 15 bits (that is, 5 bits each of red, green, and blue color information for 32K simultaneously displayed colors) or 16 bits (that is, 5 bits each of red and blue and 6 bits of green color information for 64K simultaneously displayed colors).

horizontal sync pulse: A system timing signal that defines the length of an individual scanline. Each scanline begins and ends with a horizontal sync pulse.

host CPU: The master central processing unit in a computer system. Typically a 80386, 80486, or Pentium® microprocessor in an IBM compatible PC (personal computer).

hot spot: A single x, y coordinate on a display screen. The hot spot, which is used to define the position of all hardware icons, is positioned at a resolution of one pixel.

hue: The dominant wavelength of color as subjectively perceived by the human eye.

hyper-page mode: Used interchangeable with the term 'extended-data out'. See the entry **"extended-data out"**.

--I--

intensity: In reference to illumination, the measure of the flow of power that is radiated from, or incident on, a surface. In reference to display device controllers, the level of brightness that appear on a display screen.

interlaced: A graphics system in which the even scanlines for a display device occur in one vertical cycle, and the odd scanlines occur in another vertical cycle. As a result, pixels in the even scanlines are refreshed during one vertical scan, and the pixels in the odd scanlines are refreshed during another vertical scan.

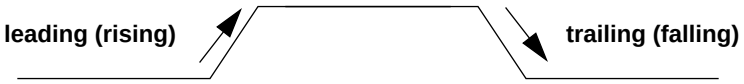
interpolation: A mathematical way to supply missing information by averaging the information that is already available and extracting the missing data from it.

--J--

JPEG: An algorithm for the non-destructive compression of still pictures in order to reduce the amount of memory required to store an image.

--L--

leading edge: An active-high signal can have the states shown: leading (rising) edge or trailing (falling).



An active-low signal can have the states shown: leading (falling) or trailing (rising).

linear addressing: A means of using multiple memory banks for mapping more than the standard 64 Kbytes reserved for display memory into one contiguous CPU memory address space (instead of using only the A0000:0h–BFFFF:Fh region of host CPU memory address space).

liquid crystal display: A type of flat panel technology that uses segments of a liquid crystal solution between glass plates. An electric field at the plates causes the solution to change its light-reflecting properties selectively.

little-endian: See the entry **"big-endian"**.

live video: Multiple frames of video data that appear one after another, giving the appearance of motion, (as opposed to a single frame of video data that appears as only one still image).

luminance: The black-and-white (that is, brightness) component of a 2-channel video signal. The luminance of a color is the color wavelength (also known as 'spectral radiance') and its conversion to luminance values. The luminance component is often called the 'Y' component. (See also the entry **"chrominance"**.)

--M--

mapping: The process of defining display memory addresses so that data used by a particular display mode can be stored at a certain location.

masking: The process of preventing a register bit from being changed.

MCLK: The CL-GD7556 clock that is used to clock a display memory subsystem.

MDA controller: The original display device controller marketed by IBM for monochrome personal computers. The MDA has no bit-mapped graphics capability.

memory mapping: A technique for giving a display memory location a working address that is different from its true address.

Mixed Color: A type of color mode that uses bit 15 to select between one of two packed-pixel modes: either (1) a 256-color packed-pixel mode that is based on the palette RAM or (2) a particular Direct Color packed-pixel mode – a 15-bit High Color mode that bypasses the palette on a pixel-by-pixel basis.

monitor: See the entry **"CRT monitor"**.

monochrome bit map: A bit map that has 1 bit per pixel and that typically defines either a character or a monochrome icon or pattern.

monochrome mode: A type of display mode that uses one bit per pixel. Typically, when a bit is 'on', that part of a display screen represented by the bit appears white, and when a bit is 'off', that part of a display screen represented by the bit appears black.

motherboard: The large printed circuit board in a personal computer into which add-in daughterboards can be plugged. It contains the host CPU, core memory, and I/O controller. It can also contain a number of other peripheral controllers.

MPEG: An algorithm for non-destructive compression of motion video data in order to reduce the amount of memory required to store an image.

multimedia: A system that uses various media, such as graphics, audio, video, text, and still pictures in an interactive way.

MVA: The proprietary Cirrus Logic architecture that enables the CL-GD7556 to incorporate a wide range of cost-effective multimedia video capabilities. These capabilities include full-screen, high-quality accelerated playback of audio-video interleaved video clips, a hardware MPEG decoder, realtime preview and capture of live video, and live video playback.

--N--

native mode: For a given flat panel, refers to a display mode that is in the original resolution of a display device. As a result, there is no expansion of the image on the display screen, and the entire display screen is in use. (For example, a flat panel with a resolution of 800 x 600 that is set for a display mode that also has a resolution of 800 x 600 is said to be in the native mode.)

non-interlaced: A graphics system in which all the scanlines for a display device occur sequentially, one after another. As a result, every pixel is refreshed during every vertical scan.

NTSC: A 525-scanline, 60-Hz color encoding scheme used for television. NTSC is used in North America and Japan, as well as some other areas. The NTSC is an extension of RS-170, and it is often spoken of as a timing standard.

--O--

occlusion: The superimposition of one type of data so that it appears to be over (or overlapping) another type of data. For example, video data can be superimposed over graphics data. In this case, the video data is said to 'occlude' the graphics data. Also, within a video window, graphics data can be superimposed over video data. In this case, the graphics data is said to 'occlude' the video data. (See also the entries **"chroma key"** and **"color key"**.)

OEMSI: The Cirrus Logic OEMSI Utility, which is used to customize the Cirrus Logic VGA BIOS for specific requirements. By using the OEMSI Utility, an OEM can change a wide variety of Cirrus Logic VGA BIOS defaults and features without having to access the Cirrus Logic VGA BIOS source code.

off screen: Refers to the area of display memory that remains, after the on-screen memory is subtracted. For the CL-GD7556, off-screen memory consists of that memory reserved for the hardware cursor/hardware icons, the half-frame accelerator, and the video windows, as well as 64-Kbytes reserved for the CL-GD7556.

on screen: Refers to the area in display memory that stores the data (such as ASCII text, graphics bit maps, and MVA data) that appears on the display screen.

on-the-fly: For data that is sent from display memory to the display screen, refers to changes made to the data at nearly the same time that the data is being displayed.

overlay: The direct superimposition of one type of data (typically video data) onto another type of data (typically graphics data). The overlay function uses the Feature Connector, which is not supported in the CL-GD7556.

overscan (noun): The border around a display screen (that is, the portion on all four sides of a display device that is between active video signals and blanking signals).

overscan (verb): To scan the border area of a display screen.

--P--

packed-pixel: A mode for segmenting the display memory for storing the color information on a pixel. With the packed-pixel mode, there is only one display memory plane, as if it were one large bit map. This plane is segmented into pixels that hold all the color data for each pixel (that is, one, two, or three bytes). There are two types of packed-pixel modes: **"true packed-pixel"** and **"chain 4"**. (See the entries for these terms.) Another mode for segmenting the display memory for storing the color information on a pixel is the planar mode. (See the contrasting entry, **"planar mode"**.)

PAL: A 625-scanline, 50-Hz color television encoding scheme used for television. PAL is used in Europe (except France), as well as some other places.

palette: A color look-up table that contains the range of colors that are available on a display device screen, but not necessarily simultaneously. For the standard VGA subsystem, the range is either 16 or 256 simultaneous colors out of 256K. For the CL-GD7555, the palette is extended to 32K, 64K, or 16M simultaneous colors on the screen. The palette uses a CLUT RAM that is used for converting data that is associated with a pixel in display memory to a specific color.

palette DAC: For a display device controller, three 8-bit DACs, each with its own associated color look-up table. The palette DAC converts digital video data to the analog R,G,B data required to drive a CRT monitor. (See also the entry **"DAC"**.)

panning: Causing the appearance of horizontal movement on a display screen. Used for viewing 'off-screen' data in a virtual-window application. (See also the entry "scrolling".)

pattern fill: The process of filling an area on a display screen with a repeating pattern.

PC Card: A PCMCIA (Personal Computer Memory Card International Association) standard for a peripheral device, about the size of a credit card, that is inserted into a computer to perform various functions. PC Cards were formerly called PCMCIA cards.

PCI: An Intel standard for a 32-bit host CPU bus that allows bus mastering.

PCI bridge: A circuit, consisting of a PCI host CPU chip and a core-logic chip, that uses the PCI bus to interface between the PCI host CPU chip and the CL-GD7556.

PCI bus: A 32-bit Intel host CPU bus that allows bus mastering.

PCI bus retry: An attempt by the CL-GD7556 to gain access to the PCI bus, after having been previously denied access by the PCI bus.

PCLK: A clock output supplied by an external video decoder to clock video data into the CL-GD7556.

PCLKO: A dot clock that is not divided by 2. The PCLKO clock appears on a CL-GD7556 output pin and is used in testing.

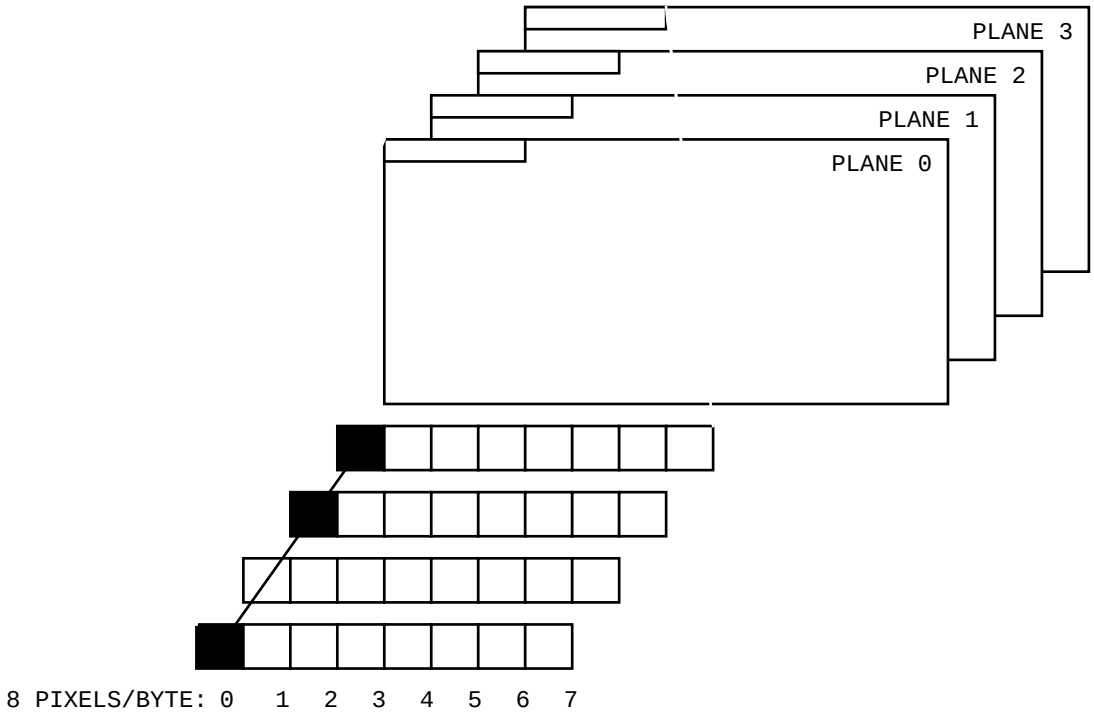
pitch: The scanline-to-scanline byte address offset.

pixel: The smallest addressable graphic on a display screen. In RGB systems, the color of a pixel is defined by some red intensity, some green intensity, and some blue intensity.

pixel clock: See the entry **"dot clock"**.

pixel data: The digital data that contains the color information for each pixel that appears on a display screen. Pixel data includes two types of data: 'video data' (which appears in a video window on the display screen) and 'graphics data' (which appears in the surrounding graphics of the display screen).

planar mode: A mode for segmenting the display memory for storing the color information on a pixel. With the planar mode, the pixel color information is stored in four bits across the four display memory planes. Another mode for segmenting the display memory for storing the color information on a pixel is the packed-pixel mode. (See the contrasting entry, **"packed pixel"**.)



power transfer function: A function that shows the relationship between (1) a range of applied video signals, expressed in millivolts, and (2) the intensity response of a CRT monitor or a flat panel, expressed in foot-Lamberts.

PowerPC: A personal computer manufactured by Apple®, which uses the host CPU chip co-manufactured by Motorola® and IBM. The PowerPC architecture uses the big-endian byte-order sequence.

pre-compression: A process, similar to compression, that reduces the amount of memory required for storing video data. Pre-compression is used when video data must go through the host CPU or other bus master, instead of through a mechanism such as the CL-GD7556 V-Port.

primary RGB: The red, green, and blue bits that are present for a display image before dithering takes place.

--Q--

quadword: A quadword is 64 bits (that is, 8 bytes).

--R--

RAM: A random-access read/write semiconductor memory device that can read or write to any memory location on subsequent access. Its write access time is approximately the same as its read access time. 'RAM' includes devices such as SRAMs (Static RAMs) and DRAMs (Dynamic RAMs).

raster operation: A BitBLT operation that combines source bytes with destination bytes, using various logic operations. Also called 'ROP'. (See also the entry **"BitBLT"**.)

readback: A type of check in which the information that was sent to an output device is also returned to the source and compared with the original information to ensure accuracy.

real time: Refers to the processing of data by a computer system in connection with another process that is outside the computer, according to the time requirements imposed by the outside process. 'Realtime capture', for example, is the process of capturing and digitizing video at a rate of 30 frames per second.

refresh: See the entry **"display screen refresh"**.

reset state: One of two conditions (that is, 'on' which equals a 1, or 'off' which equals a 0) that a CL-GD7556 standard VGA or Extension VGA register bit can be in during the period after the CL-GD7556 is powered on and before the VGA BIOS parameters are loaded.

resolution: The basic measurement of how much information is on a display screen (that is, how many pixels per square inch can be displayed). Resolution is typically specified in terms of columns of pixels by rows of pixels (that is, as pixels per scanline and scanlines per frame). For example, for standard VGA display mode number 13h, the resolution is 320 columns of pixels by 200 rows of pixels. (Also called 'spatial resolution' or 'size'.)

response time: The rate at which pixels on a display screen turn on and off.

rising edge: See the entry **"leading edge"**.

RGB: The type of color space format that uses three color signals (red, green, and blue) with a color display device. Both digital and analog RGB interfaces exist. In contrast to the RGB interface is the type of interface that uses only a single signal with a monochrome display device.

ROM: A read-only memory device that is written only once. ROM chips are typically used to contain low-level programs that do not change, such as the VGA BIOS. (See also the entry **"EPROM"**.)

ROM BIOS: A program, such as the VGA BIOS, that resides in a ROM or EPROM chip. (See also the entry **"VGA BIOS"**.)

--S--

saturation: The amount of color that is present, that is, the degree to which the hue of a color is undiluted by its complementary color to form white.

scaling: The process of changing the effective resolution of a video data that appears on a display device, so that the resulting display image appears either larger or smaller than the original image.

- Upscaling is the process of increasing the display image size by creating extra data from an incoming video stream through either interpolating or replicating video data before placing it into display memory.
- Downscaling is the process of decreasing the display image size by either decimating or interpolating out data from an incoming video stream before the video data is placed into display memory.

scaling engine: A hardware logic block that accomplishes the scaling process.

scanline: For CRT monitors, refers to an individual sweep of an electron beam across the face of the display screen, which makes an image appear on the display screen. For flat panels, refers to the sweep that is caused by a row driver, that is, by the matrix addressing of successive pixel elements using row-by-column addressing.

screen refresh: See the entry **"display screen refresh"**.

scrolling: Causing the appearance of vertical movement on a display screen. Used for viewing 'off-screen' data in a virtual-window application. (See also the entry "panning".)

SECAM: A 625-scanline, 50-Hz color television encoding scheme, similar to the PAL color television encoding scheme. SECAM is used primarily in France and parts of the former Union of Soviet Socialist Republics. With the SECAM scheme, the chrominance signals undergo frequency modulation.

setup latency: The time it takes to set up (that is, load) data. For example, the time it takes registers to be loaded with values for a BitBLT is referred to as the setup latency.

shading: The technique of modulating a signal over time by using multiple frames to increase the number of shades of color.

shift clock: A clock input that serially shifts internal data.

SimulSCAN: A Cirrus Logic proprietary process that allows for simultaneous displays to appear on both a CRT monitor and a flat panel.

simultaneous colors: The number of colors in a display system that can be displayed on the display screen at one time. This number is limited by the circuitry of the display device controller that is used in a system and is often much smaller than the number of colors the display device can actually support. The number of simultaneous colors that a display device controller supports is normally determined by the number of color planes, or bits per pixel, that it uses. For example, a display device controller with eight bits per pixel supports 256 simultaneous colors.

single-page mapping: Refers to always using Display Memory Offset Register 0 (GR9) as the entry into display memory. This mode is chosen when GRB[0] is programmed to a '0'.

source pitch: A scanline-to-scanline byte address offset. (For more information, refer to Extension register GR27).

spatial dithering: See the entry **"dithering"**.

spatial resolution: See the entry **"resolution"**.

standard: In Cirrus Logic Portable Graphics documentation, a term that is used interchangeably with the term 'VGA'. (See the entry **"VGA"**.) 'Standard' is also applied to the term 'standard' television set, that is, the type of television for home use.

status: When a bit is used as a status bit, it is tested to check for the presence of an internal interrupt condition.

still-image viewer: A DOS-based application program that allows the viewing of images that do not move (in contrast to images such as video, which are in motion).

STN: A type of flat panel display device that adds a chiral additive (that is, a molecular twisting agent) to the panel's liquid crystal material to achieve its optical effect.

submarining: The temporary disappearance of the mouse pointer as it moves across a display screen.

Super VGA: See the entry **"SVGA controller"**.

surrounding graphics: See the entry **"graphics"**.

SVGA controller: An SVGA (or "Super VGA") display device controller that extends the capabilities of the features provided by the original IBM VGA display device controllers. The SVGA controllers support display modes that have a maximum resolution of up to 1280 x 1024 and a maximum color depth of up to 16M simultaneous colors.

S-VHS: An high-resolution format for video recording and playback. Also refers to the enhanced video tape deck that provides better resolution and less noise than the original VHS video tape deck.

switchless configuration: The process of using the VGA BIOS, instead of using hardware switches, to configure the CL-GD7556.

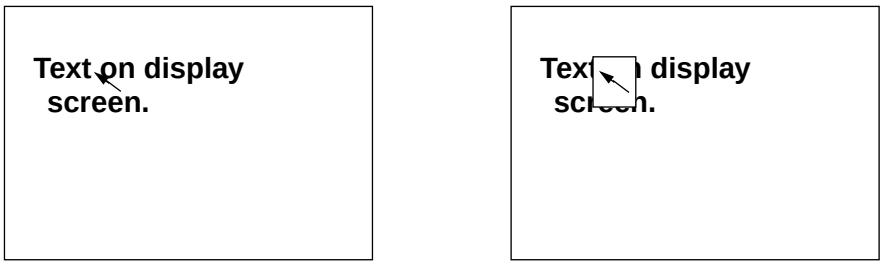
system BIOS: Firmware routines (typically residing in ROM) that, upon system reset or power-up, initialize and load into system memory all the system resources, including the operating system, configuration information, interrupt vectors, and the CL-GD7556 VGA BIOS. The system BIOS queries the system resources, configures the interrupt vector tables for the available system resources, and loads the configuration information. In addition, the system BIOS loads the VGA BIOS, other expansion BIOSs, and the resident portions of open systems that need moved to system RAM. (See also the entry **"VGA BIOS"**.)

--T--

text display mode: A display mode in which only a pre-defined set of characters can be displayed (as opposed to graphics display modes, in which all pixels on the display screen can be controlled independently to draw graphics objects).

TFT: A type of flat panel display device that provides for high speeds by placing one or more thin-film transistors at the site of each pixel. This term is often used with, or in place of the term 'active-matrix'.

three-colors-and-transparent mode: A hardware icon display mode, in which three of the four icon pseudo-colors that make up the icon pattern can use only three colors out of 256K pre-programmed colors of the icon palette. The fourth icon pseudo-color is not replaced by a color in the icon palette, but rather it allows graphics or video data to be displayed. As a result of this programming, the icon can be an irregular shape moving on the graphics or video background. (By contrast, in the four-color mode, the icon is always represented as a non-transparent rectangle.)



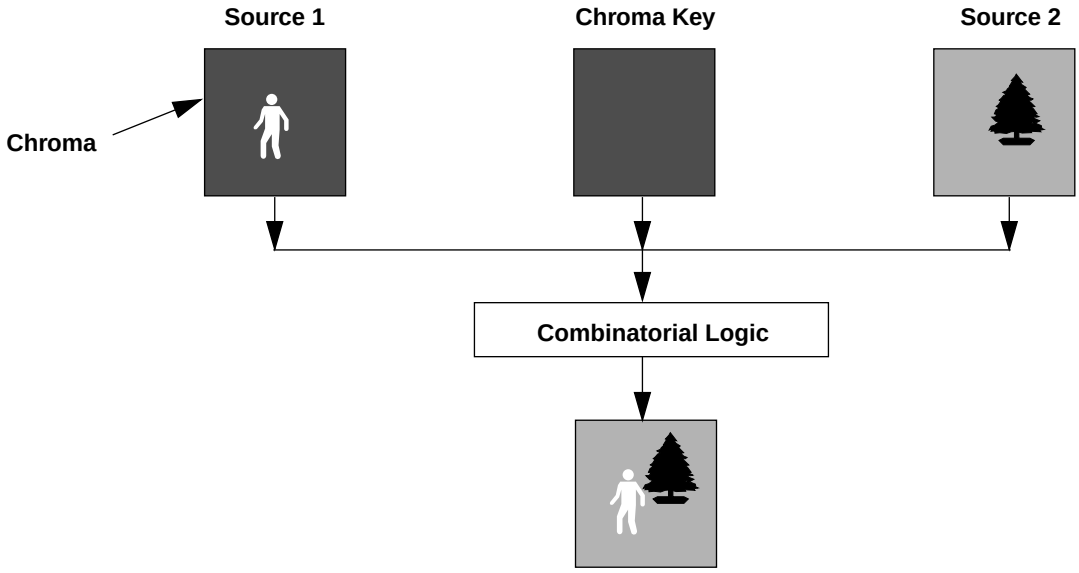
Three-colors-and-transparent mode **Four-color-mode**

trailing edge: See the entry **"leading edge"**.

transparent BitBLT: A type of BitBLT that uses chroma keying (a type of masking) to combine two sources of data. In the figure that follows, where the chroma key is:

- Not detected in source 1, data is taken from source 1.
- Detected in source 1, data is taken from source 2.

(See also the entry **"BitBLT"**.)



True Color: A type of Direct Color packed-pixel mode that uses at least three color components, such as RGB or YCrCb. Industry-wide, the term 'True Color' refers to the use of 24 bits per pixel (or 32 bits per pixel, with 8 bits used in masking) to produce 256 shades each of red, green, and blue for photo-realistic image quality. (When referring to 'True Color' in terms of the CL-GD7556, 24 bits per pixel are used to provide 16M simultaneously displayed colors.)

true packed-pixel: A type of packed-pixel mode in which consecutive pixels are stored at consecutive display memory addresses. This type of addressing is in contrast with chain-4 addressing, which is a type of packed-pixel mode in which consecutive pixels are stored at every fourth byte address in display memory.

TV: An NTSC, PAL, or SECAM display device (that is, a standard home television set).

TV decoder: A device for decoding television broadcast video data that has been previously encoded for transmission. An example of a TV decoder is the CL-PX4072.

TV in a window: The display of a video signal (either from a TV tuner or a VCR) within a video window.

--U--

universal retry: The automatic assertion of a retry for any memory write attempts to a video aperture.

upscaling: See the entry **"scaling"**.

--V--

VCLK: The internal CL-GD7556 clock signal for display data signals. Depending on CL-GD7556 register settings, the VCLK can be either the same frequency as the MCLK signal or it can be some subdivision of the frequency of the MCLK signal. Although historically the VCLK was also called the video clock, it must not be confused with the video clock that is used to clock video data for a video window. (See also the entry **"video clock"**.) For a block diagram that relates some of the CL-GD7556 clock signals, see the entry **"clock"**.

vertical retrace: The time interval immediately following the completion of a complete frame (or field for an interlaced display). The electron beam returns to the top of the display screen in preparation for the next frame or field during this period.

vertical sync pulse: A system timing signal that defines the length of a complete frame (or field for an interlaced display) that is composed of the individual scanlines. Each field begins and ends with a vertical sync pulse.

VESA®: The 'Video Electronics Standards Association', a consortium of vendors of CRT monitors, graphics/video chips, and graphics/video software. This consortium sets hardware and software standards for PC-compatible display devices and software interfaces. VESA efforts include VBE (VESA BIOS extension) and SVGA CRT monitor timing. Cirrus Logic is an active participant on many VESA committees.

VGA: A standard display device controller that was introduced by IBM. The VGA controllers support display modes that have a maximum resolution of up to 720 x 400 and a maximum color depth of up to 256/256K simultaneous colors. Other display device controllers, such as the CGA and EGA, have architectures that are a subset of that of the VGA display device controller. The SVGA has an architecture that is a superset of that of the VGA display device controller.

VGA architecture: Refers to the display device controller standard that was introduced by IBM. The standard VGA registers make up the core of the VGA architecture. (See also the entry **"VGA registers"**.)

VGA BIOS: ROM-based CL-GD7556 firmware routines that, upon system reset or power-up, interact with the system BIOS to control the VGA subsystem. Also called 'ROM BIOS'.

VGA controller: A display device controller that was introduced by IBM in 1987. The VGA controller allows for display modes that have a maximum resolution of 640 x 480 and a maximum color depth of up to 256 simultaneous colors. Third-party chip vendors, including Cirrus Logic, have enhanced or extended the original VGA standard so that display modes have a maximum resolution of up to 1280 x 1024 and a maximum color depth of up to 16M simultaneous colors. (See also the entry **"SVGA controller"**.)

VGA display mode: A way of presenting data on a display screen that is compatible with the IBM standard display modes, that is, hex display modes 0–13h.

VGA memory: See the entry **"graphics memory"**.

VGA registers: In a display device controller, the storage units that contain data relating to either the configuration of a display device or the display mode of the display device (as opposed to the display memory, which contains the data for the image that appears on the display screen). The VGA registers can be divided into six groups: the five standard VGA registers for CRT monitors (the External/General, Sequencer, CRT Controller, Graphics Controller, and Attribute Controller registers) and the VGA Extension registers, which include registers for both CRT monitors and flat panels. The VGA registers are accessed by a number of addressing schemes, each involving an index or address register and a data register.

VGA subsytem: The CL-GD7556 VGA subsystem of a computer system includes the following functions: host CPU bus interface, graphics controller and other standard VGA registers, display memory interface, display device interface, VSYNC and HSYNC clock generators, VGA BIOS, display power management system, V-Port, on-chip CLUT RAMDAC, and GUI acceleration logic.

VHS: A medium-resolution format for video recording and playback.

video: The type of display data that appears either on a television set display screen or in a video window on a computer display screen. Video data originates from signals from either a broadcast station or recording media such as a VCR. Video signals (which include such information as intensity, color, synchronization, and blanking), require special processing to display on a flat panel display device. Video data is in contrast to graphics data. (See also the entry **"graphics"**.)

video acceleration: Using hardware circuitry to perform functions with graphics or video data, which otherwise would have to be done in software by the host CPU. Examples of functions that use video acceleration include scanline or pixel interpolation or replication, color space conversion, and BitBLTs.

video capture: The process of converting analog video frames to a digital format and storing the video data frame by frame, for future processing. This process is also called 'digitization'.

video clock: The clock (VPCLKI) that is used to clock video data into the CL-GD7556. The video clock is not the same as the VCLK. (See the entry **"VCLK"**.) For a block diagram that relates some of the CL-GD7556 clock signals, see the entry **"clock"**.

video data: See the entry **"video"**.

video data input source: A hardware unit that operates on files stored on mass storage devices (such as a CD-ROM or hard disk drive) that are connected to the bus. Examples of video input sources include: NTSC/PAL TV decoders, MPEG decoders (and MPEG-1 files), and DCI-compatible files.

video pipeline: Refers to all the hardware and software elements that are involved in delivering video data from its input source and processing it for its appearance on a display screen.

video playback: The display of video data, stored on a CD-ROM or hard disk drive, on either a CRT monitor or a flat panel display screen, or both.

Video Port Manager: The software element of the V-Port. The Video Port Manager runs under Windows and manages the transfer of video data from an external decoder through the V-Port-to-Memory interface, directly into display memory for display on the display device.

video preview: The process of watching video data frame by frame before doing a video capture.

video signal: Either a signal that originates from a television broadcast station or from recording media (such as a VCR). Video signals were originally intended to be displayed on a standard television set, but can now also be displayed on computer CRT monitor or a flat panel display screen.

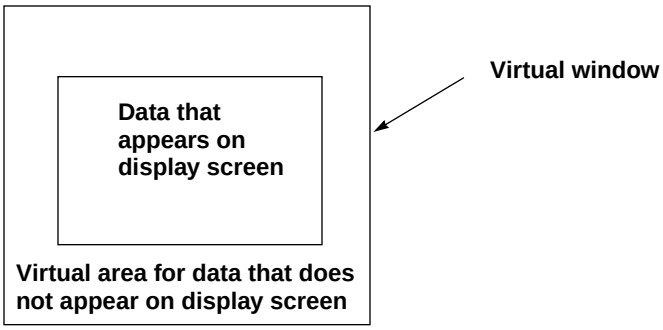
video source: The origin of video data.

video stream: Multiple frames of images, that is, the progression of video data from its input to its display on a display device. A video stream appears on a display screen one after another in a moment-by-moment manner, giving the appearance of motion.

video window: An area of a computer display screen that has been allocated for an overlay image. The video window can be positioned anywhere on a display screen. Contrast this term with the entry **"graphics window"**.

virtual display: A flat panel display screen that has the capability of being panned and scrolled.

virtual window: A window that is set up in display memory, with some of the data in the virtual window appearing on the display screen and some of the data stored off the display screen in a 'virtual area'.



voltage-controlled oscillator: A type of oscillator that changes its frequency depending on the voltage that it receives on one of its control pins.

V-Port™: A standardized bus interface for transferring video data to a computer display. It consists of a hardware element (V-Port to Memory) and a software element (the Video Port Manager). The V-Port takes video data directly from an external decoder and transfers the video data into the display memory.

V-Port to Memory: The hardware element of the V-Port. The V-Port to Memory is the interface between an external decoder and the CL-GD7556.

--W--

wait state: One or more time intervals (typically in units of clock periods that are in tens of nanoseconds) that are inserted when a host CPU is reading from or writing to a memory or peripheral device that cannot respond fast enough. When wait states are inserted, the host CPU does nothing but pause and wait for the slower device. This pause, while detrimental on the system throughput, is unavoidable. However, the number of wait states can be reduced by using asynchronous data transfer techniques such as host CPU bus caches or write FIFOs.

Winmark: A pixel-per-second unit of measure devised for use with Ziff-Davis programs, which assess the hardware and software performance of a computer system or subsystem.

word: The amount of display memory that a given computer can access in a single cycle. For standard IBM compatibility a word is 16 bits (that is, 2 bytes).

write buffer: The buffer that is logically positioned between the host CPU interface and the display memory.

--X--

XGA: A flat panel that has a resolution of 1024 x 768.

--Y--

YCrCb: A color space format defined in CCIR601. The ‘Y’ stands for the black-and-white (also called the ‘luminance’) component of the color space. ‘Cr’ and ‘Cb’ are respective scaled versions of ‘U’ and ‘V’, the color (also called ‘chrominance’) components in the YUV color space.

YUV: A color space format generally associated with broadcast television. The ‘Y’ stands for the black-and-white (also called ‘luminance’) component of the color space. The ‘U’ and ‘V’ stand for the color (also called ‘chrominance’) components of the color space.

YUV color space converter: A method of digitizing analog video data into digital data for a flat panel.

--Z--

ZV-Port specification: A specification for a standard that eliminates the need to send video and audio data through the host CPU or the system bus. Instead, the data stream is sent from the PC card socket adapter directly to the display device controller and the frame buffer (that is, display memory).

BIT INDEX

This Bit Index indexes the register bits in Chapter 7 to Chapter 12.

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