
# *CL-GD755X*
# *Application Book*

*March, 1997*
*Revision 2.0*
*Stock # 367555 - 002*

## Notice

This document describes a potential application of Cirrus Logic integrated circuits. No warranty is given for the suitability of the circuitry or program code described herein for any purpose other than demonstrating functional operation. Cirrus Logic believes this information is accurate and reliable. However, it is subject to change without notice. No responsibility is assumed by Cirrus Logic for the use of this information, nor for infringements of patents or other rights of third parties. This document implies no license under patents or copyrights.

CIRRUS LOGIC®

# CL-GD755X
## Application Book

**Revision 2.0**
**March 1997**

## CL-GD7555 Application Notes:

| | | Revision Summary |
|---|---|---|
| 7555-AN-1 | A PCI Bus XGA/SVGA Solution.<br>(GDB7555-C-DM1-1 PCI Bus Demonstration Board)<br>April 1996, Version 1.0 | No change from App Book Rev 1.0 |
| 7555-AN-3 | Analog Voltage Filtering Requirements<br>for the CL-GD7555 LCD/CRT Controller<br>July 1996, Version 1.0 | No change from App Book Rev 1.0 |
| 7555-AN-4 | A Programmable Core-Voltage Solution<br>for the CL-GD7555 LCD/CRT Controller<br>June 1996, Version 1.0 | No change from App Book Rev 1.0 |
| 7555-AN-7 | State Information on Pad Control Signals<br>for the CL-GD7555 LCD/CRT Controller<br>June 1996, Version 1.0 | No change from App Book Rev 1.0 |
| 7555-AN-9 | Designing for DDC Level 2B<br>with the CL-GD7555 LCD/CRT Controller<br>June 1996, Version 1.0 | No change from App Book Rev 1.0 |
| 7555-AN-10 | V-Port Implementation<br>for the CL-GD7555 LCD/CRT Controller<br>March 1997, Version 1.0 | NEW |
| 7555-AN-11 | Layout Guidelines<br>for the CL-GD7555 LCD/CRT Controller<br>July 1996, Version 1.0 | No change from App Book Rev 1.0 |
| 7555-AN-13 | Using the Chrontel CH7001 VGA-to-NTSC/PAL Encoder<br>with the CL-GD7555 LCD/CRT Controller<br>July 1996, Version 1.0 | No change from App Book Rev 1.0 |
| 7555-AN-14 | Requirements for OSC Signal during Suspend/Resume<br>of the CL-GD7555 LCD/CRT Controller<br>February 1997, Version 1.0 | NEW |
| 7555-AN-15 | Design Requirements for Power Sequencing<br>for the CL-GD7555 LCD/CRT Controller (Revision CD)<br>March 1997, Version 1.0 | NEW |

## CL-GD7556 Application Notes:

| | | Revision Summary |
|---|---|---|
| 7556-AN-1 | Design Requirements for Board Upgrade<br>from the CL-GD7555 LCD/CRT Controller<br>to the CL-GD7556-AB LCD/CRT Controller<br>March 1997, Version 1.1 | NEW |

**Revision 2.0**
**March 1997**

## Application Alerts:

| | | |
|---|---|---|
| 7555-AA-1 | Using the CL-GD7555 PCI Bus Demonstration Board with an Off-the-Shelf Motherboard<br>June 1996, Version 1.0 | No change from App Book Rev 1.0 |
| 7555-AA-2 | Using Extended-Data-Out DRAMs with the CL-GD7555 LCD/CRT Controller<br>June 1996, Version 1.0 | No change from App Book Rev 1.0 |
| 7555-AA-3 | Changes to Support for DRAM Configurations and Display Modes for the CL-GD7555 LCD/CRT Controller<br>June 1996, Version 1.0 | No change from App Book Rev 1.0 |
| 7555-AA-4 | Programming the LCD Power-Sequencing Time Delay for the CL-GD7555 LCD/CRT Controller<br>March 1997, Version 1.0 | NEW |

## Errata:

| | | |
|---|---|---|
| 7555-ERR-1 | CL-GD7555-CF Errata<br>March 1997, Version 1.00, Rev. 1.00 | NEW |
| 7556-ERR-1 | CL-GD7555-AB Errata<br>March 1997, Version 1.01, Rev. 1.01 | NEW |
| 7556-ERR-1 | CL-GD7555-AC Errata<br>March 1997, Version 1.01, Rev. 1.01 | NEW |

## Panel Interface Guide:

| | | |
|---|---|---|
| 7555-PIG-1 | LCD Panel Interface Connections<br>June 1996 | UPDATE |

## Schematics

NEW

CIRRUS LOGIC®

# CL-GD7555

*Advance Application Note — 7555-AN-1, v1.0*

# A PCI Bus XGA/SVGA Solution

***using the CL-GD7555 XGA/SVGA LCD/CRT Controller with the GDB7555-C-DM1-1 PCI Bus Demonstration Board***

**Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application note documents a sample PCI Bus Demonstration Board that uses the CL-GD7555 XGA/SVGA LCD/CRT controller.

**Applicability**

This document contains CL-GD7555 connectivity data that can be applied to user applications.

This document applies to the following products:

_✔_CL-GD7555

**Related Documents**

– *CL-GD7555 Reference Manuals*



***Version 1.0*** ***April 2, 1996***

# Table of Contents

# 1. Introduction

This application note describes how to configure and operate the Cirrus Logic GDB7555-C-DM1-1 PCI-Bus Demonstration Board (referred to in this document as the 'Demonstration Board').

The Demonstration Board is a sample Video Graphics Adapter board using the CL-GD7555 single-chip XGA/SVGA LCD/CRT controller. Use this Demonstration Board to do the following:

- Evaluate the CL-GD7555 controller in a functional environment
- Design a PCI Bus system that uses the CL-GD7555 XGA/SVGA LCD/CRT Controller
- Evaluate the CL-GD7555 power-down features
- Evaluate the CL-GD7555 V-Port capability and MotionVideo™ Acceleration capability
- Use the CL-GD7555 with a 1024 x 768 TFT 2-pixel-per-clock LCD panel

For more information, refer to the following:

- The appendix, which includes schematics for the Demonstration Board
- The *CL-GD7555 Hardware Reference Manual*
- The *CL-GD7555 Software Reference Manual*

## 2. Demonstration Board Configuration Components

Figure 2–1 shows the locations of all components used to configure the Demonstration Board. Tables in this section list all significant configuration components, the selection options, and the default settings.

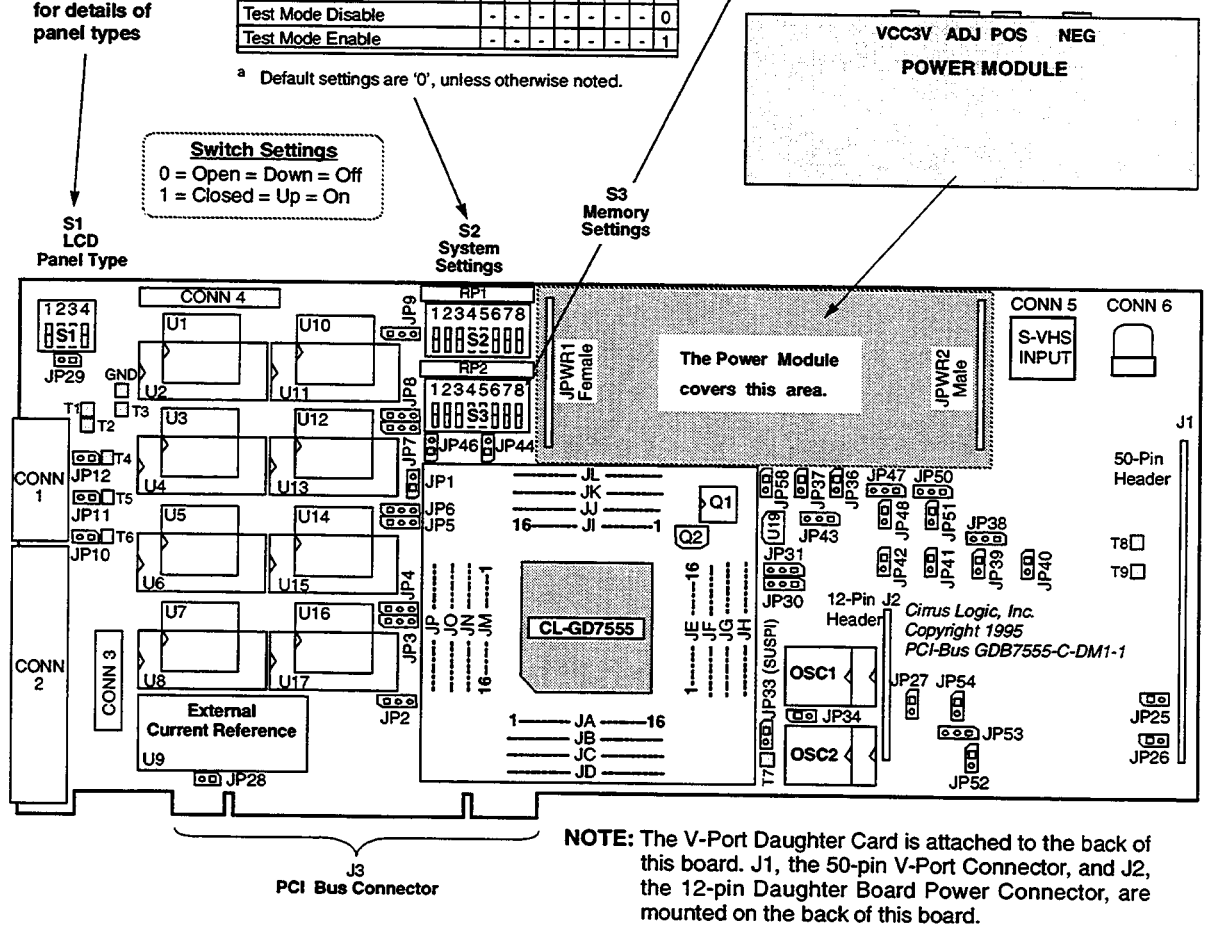
| S1 Settings | SW# | | |
|---|---|---|---|
| LCD Panel Type | 1 | 2 | 3 |
| 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 2 | 0 | 1 | 0 |
| 3 | 1 | 1 | 0 |
| 4 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 |
| 7 | 1 | 1 | 1 |

See Table 4 for details of panel types

| S2 Settings[a] | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| *Not Used* | x | - | - | - | - | - | - | - |
| Pin-scan Test Disable | - | 0 | - | - | - | - | - | - |
| Pin-scan Test Enable | - | 1 | - | - | - | - | - | - |
| Intr. Req. connected to IREQ# | - | - | 0 | - | - | - | - | - |
| Intr. Req. not connected | - | - | 1 | - | - | - | - | - |
| Internal Clock | - | - | - | 0 | - | - | - | - |
| External Clock | - | - | - | 1 | - | - | - | - |
| 64K BIOS | - | - | - | - | 0 | - | - | - |
| 32K BIOS | - | - | - | - | 1 | - | - | - |
| BIOS Support Disable | - | - | - | - | - | 0 | - | - |
| BIOS Support Enable (default) | - | - | - | - | - | 1 | - | - |
| *Not Used* | - | - | - | - | - | - | x | - |
| Test Mode Disable | - | - | - | - | - | - | - | 0 |
| Test Mode Enable | - | - | - | - | - | - | - | 1 |

[a] Default settings are '0', unless otherwise noted.

| S3 Settings | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|---|
| Memory Mapped I/O for Non-x86 CPU | Disabled | 0 | - | - | - | - | - | - | - |
| | Enabled | 1 | - | - | - | - | - | - | - |
| *Not Used* | | - | x | x | x | x | x | x | - |
| Relocatable PCI I/O | Disabled | - | - | - | - | - | - | - | 0 |
| | Enabled | - | - | - | - | - | - | - | 1 |




**NOTE:** The V-Port Daughter Card is attached to the back of this board. J1, the 50-pin V-Port Connector, and J2, the 12-pin Daughter Board Power Connector, are mounted on the back of this board.

**Figure 2–1. The GDB7555-C-DM1-1 PCI-Bus XGA/SVGA Demonstration Board**

## 2.1 Modification/Rework Instructions for GDB7555-C-DM1-1 Demonstration Board

The following changes to the GDB7555-C-DM1-1 Demonstration Board or the schematics are required for proper operation. These changes should not be necessary on future revisions of the board.

1) Some Demonstration Boards come with FB4 - FB7 mounted and some not mounted. The Demonstration Boards without FB4 - FB7 mounted have wires shorted instead.

2) For DDC2B Support, the following must be modified:
   a) Place a wire on T3 to CRTVDD.
   b) Add a 6.8K pull-up resistor to U18 (CL-GD7555) pin 104 (DDCD) or test point JH. The 6.8K pull-up resistor must be pulled up to CRTVDD.

3) There are a few silk screen errors on the Demonstration Board :
   a) For Panel Type Switches - Table S1:

| | | | |
|---|---|---|---|
| Change: | 0 = CLOSED | to: | 0 = OPEN = OFF |
| | 1 = OPEN | | 1 = CLOSED = ON |
| | X = DON'T CARE | | X = DON'T CARE |

   b) For Table S2 and S3:

| | | | |
|---|---|---|---|
| Change: | 0 = CLOSED | to: | 0 = OPEN = OFF |
| | 1 = OPEN | | 1 = CLOSED = ON |
| | X = DON'T CARE | | X = DON'T CARE |

   c) For Table S2:

| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|---|
| Change: | | | | | | | | | |
| | Video Port Enable | 0 | X | X | X | X | X | X | X |
| | Video Port Disable | 1 | X | X | X | X | X | X | X |
| To : | Reserved – Not Used | 0 | X | X | X | X | X | X | X |
| | | 1 | X | X | X | X | X | X | X |

   d) For Table S3:

| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|---|
| Change: | | | | | | | | | |
| | Memory Mapped I/O – Disabled | 0 | X | X | X | X | X | X | X |
| | Memory Mapped I/O – Enabled | 1 | X | X | X | X | X | X | X |
| | PCI Board Vendor ID | X | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | X |
| To: | Memory Mapped I/O for Non-x86 CPU – Disabled | 0 | X | X | X | X | X | X | X |
| | Memory Mapped I/O for Non-x86 CPU – Enabled | 1 | X | X | X | X | X | X | X |
| | Reserved – Not Used | X | X | X | X | X | X | X | X |

4) Capacitor C15 (1uF) for the Internal Current Reference is currently tied to JP31 pin 3 and DACVSS. It should be reconnected to JP31 pin 3 and DACVDD1 (test point JE pin 12).

## 2.2 Test Points

### 2.2.1 Miscellaneous Test Points

A number of test points, T1 through T9, are located on the board to assist in testing various input and output signals. The specific functions of these test points are shown in Table 1.

**Table 1. Miscellaneous Test Point Functions**

| Test Point No. | Function Available On The Test Point |
|---|---|
| T1 | Connected to HSYNC |
| T2 | Connected to VSYNC |
| T3 | *Not Used* |
| T4 | Connected to Blue DAC Output |
| T5 | Connected to Green DAC Output |
| T6 | Connected to Red DAC Output |
| T7 | Connected to Suspend Input Pin |
| T8 | V-Port connector pin 25 |
| T9 | V-Port connector pin 29 |

### 2.2.2 CL-GD7555 Test Points

Test points JA through JP, are in rows parallel to the edges of the CL-GD7555. These test points are connected to CL-GD7555 input and output pins to assist in evaluation and testing. For CL-GD7555 pin connection mapping to the test points refer to Table 2. For signal identification refer to the schematic sheets in Appendix A.

**Table 2. Test point to Pin Mapping**

| | JA | JB | JC | JD |
|---|---|---|---|---|
| 1 | | | MD18 | MD17 |
| 2 | MD16 | MD15 | MD14 | MVDD |
| 3 | MD13 | MD12 | MD11 | MD10 |
| 4 | MD9 | MD8 | CAS#1 | CAS#0 |
| 5 | MD7 | MD6 | MD5 | MD4 |
| 6 | MD3 | MD2 | MD1 | MD0 |
| 7 | GND | AD31 | AD30 | AD29 |
| 8 | AD28 | AD27 | AD26 | AD25 |
| 9 | AD24 | AD23 | AD22 | BVDD |
| 10 | AD21 | AD20 | AD19 | AD18 |
| 11 | AD17 | AD16 | INTR# | CVDD |
| 12 | STOP# | PAR | DEVSEL# | TRDY# |
| 13 | GND | CLK | IRDY# | FRAME# |
| 14 | IDSEL | OSC | RESET# | SUSPI |
| 15 | CLK32K | C/BE#3 | C/BE#2 | C/BE#1 |
| 16 | C/BE#0 | | ACTI | GND |

| | JE | JF | JG | JH |
|---|---|---|---|---|
| 1 | | | AD15 | AD14 |
| 2 | AD13 | AD12 | AD11 | AD10 |
| 3 | AD9 | AD8 | AD7 | AD6 |
| 4 | BVDD | AD5 | AD4 | AD3 |
| 5 | AD2 | CVDD | AD1 | AD0 |
| 6 | GND | VPC0 | VPC1 | VPC2 |
| 7 | VPC3 | VPC4 | VPC5 | VPC6 |
| 8 | VPC7 | VPY0 | VPY1 | VPY2 |
| 9 | VPY3 | DDCC | GND | VPY4 |
| 10 | VPY5 | VPY6 | VPY7 | DDCD |
| 11 | VAVDD | HREFI | VAVSS | VACTI |
| 12 | DACVDD | VSI | VPCLKI | HSYNC |
| 13 | DACVSS | VSYNC | VREF | IREF |
| 14 | CRTVDD | | PROG1 | BLUE |
| 15 | GREEN | RED | FPVEE | FPDECTL |
| 16 | FPVCC | | PROG0 | GND |

| | JI | JJ | JK | JL |
|---|---|---|---|---|
| 1 | PROG2 | | FP18 | FP19 |
| 2 | FP20 | DACVDD | FP21 | FP22 |
| 3 | FP23 | FP24 | FP25 | FP26 |
| 4 | FP27 | DACVSS | FP28 | FP29 |
| 5 | FP30 | FP31 | FP32 | FP33 |
| 6 | FP34 | FP35 | FPVDD | FPDE |
| 7 | LLCLK | GND | FPVDCLK | LFS |
| 8 | FP0 | FP1 | FP2 | FP3 |
| 9 | FP4 | FP5 | FP6 | FP7 |
| 10 | FPVDD | FP8 | FP9 | FP10 |
| 11 | FP11 | FP12 | GND | FP13 |
| 12 | FP14 | FP15 | FP16 | FP17 |
| 13 | GND | MD63 | MD62 | MD61 |
| 14 | MD60 | MD59 | MD58 | MD57 |
| 15 | MD56 | MD55 | MD54 | CAS#7 |
| 16 | CAS#6 | | | GND |

| | JM | JN | JO | JP |
|---|---|---|---|---|
| 1 | MA9 | RAS1# | MD53 | MD52 |
| 2 | MD51 | MD50 | MD49 | MVDD |
| 3 | MD48 | MD47 | MD46 | MD45 |
| 4 | MD44 | MD43 | CAS#5 | CAS#4 |
| 5 | MD42 | MD41 | MD40 | MD39 |
| 6 | MD38 | MD37 | MD36 | MD35 |
| 7 | MD34 | MD33 | MD32 | GND |
| 8 | MA8 | MA7 | MA6 | MA5 |
| 9 | MA4 | WE# | MVDD | RAS0# |
| 10 | MA3 | MA2 | MA1 | MA0 |
| 11 | GND | MD31 | MD30 | MD29 |
| 12 | MD28 | MD27 | CVDD | MD26 |
| 13 | MD25 | MD24 | CAS#3 | CAS#2 |
| 14 | MD23 | MD22 | MD21 | MD20 |
| 15 | MD19 | MAVDD | SW0 | MAVSS |
| 16 | EPROM# | | OE# | GND |

## 2.3 Connectors

The following are the main Demonstration Board connectors:

### 2.3.1 PCI Bus Connector

J3 is the board-edge connector to connect the Demonstration Board to the PCI bus.

### 2.3.2 CRT Connector

CONN 1 is a 15-pin DIN connector to connect a CRT monitor to the Demonstration Board.

### 2.3.3 LCD Connector 1

CONN 2 is a 44-pin connector to connect the primary LCD panel signals to the Demonstration Board.

### 2.3.4 LCD Connector 2

CONN 3 is a 16-pin connector to connect the extended TFT panel signals to the Demonstration Board.

### 2.3.5 NTSC Connector

CONN 4 is configured as a 24-pin NTSC connector, but it is not supported at this time.

### 2.3.6 Video Connections

CONN 5 is an S-Video connector to connect external video signals to the Demonstration Board.

CONN 6 is an RCA jack to connect composite-video signals to the Demonstration Board.

### 2.3.7 Power Module Connection

Headers JPWR1 and JPWR2 connect the Power Module to the Demonstration Board.

### 2.3.8 V-Port Daughter Board Connector

J1, on the back of the board, is a 50-pin connector to connect the optional V-Port daughterboard to the Demonstration Board.

### 2.3.9 V-Port Daughter Board Power Connection

J2, on the back of the board, is a 12-pin connector to supply power to the optional V-Port daughter card.

## 2.4 Configuration Jumpers and Header Blocks

This section lists by function the jumpers and header blocks. In some cases, headers are used as connectors. Table 3 describes the settings for the JP jumper and header blocks in this section.

### 2.4.1 Voltage Level and Power-Management Configuration

The jumper and header blocks listed here are for selecting voltage levels and connections for the Demonstration Board. In all cases, the default voltage level for an interface is 5 V. The Demonstration Board is shipped with 5-V DRAM. Voltages can be mixed in any combination.

- JP38: Selects either 3.3 or 5 V for CVDD, DACVDD, MAVDD and VAVDD.
- JP43: Selects either 3.3 or 5 V for MVDD and Display Memory.
- JP47: Selects either 3.3 or 5 V for FPVDD and panel power VDD.
- JP50: Selects either 3.3 or 5 V for CRTVDD, the voltage for the CRT.
- JP53: Selects either 3.3 or 5 V for BVDD and OSC VDD.

The following jumper block provides power to the V-Port.

- JP27: When connected, this jumper provides 5 V power to the V-Port.

The following jumper block allows configuring for power-management modes.

- JP33: Enable/Disable the hardware-initiated Suspend mode.

### 2.4.2 Jumper Blocks for Display Memory Size and Type

The jumper blocks listed below are for selecting the type of display memory that is used. The Demonstration Board is shipped with 2M bytes of dual-CAS# 5-V DRAM. The board can accommodate either SOJ or TSOP packages. An additional 2M bytes can be added, but JP1 must also be added to enable RAS1#.

- JP1: Select either 2M DRAM support (the default) or 4M DRAM support.
- JP2–JP9: Select either dual-CAS# or dual-WE# DRAMs. The default is dual-CAS# DRAMs, which Cirrus Logic ships on the Demonstration Board.

**Table 3. Settings for the PCI Bus Demonstration Board Jumper and Header Blocks**

| Jumper / Header Block No. | Jumper / Header Block Functions | If 3-Position Block: Function of *Jumpers on 1-2*<br>If 2-Position Block: Function of *No Jumper* | If 3-Position Block: Function of *Jumpers on 2-3*<br>If 2-Position Block: Function of *Jumper On* |
|---|---|---|---|
| JP1 | 4M byte Display Memory Select. | The default display-memory configuration is 2 Mbytes. | This jumper enables the control signals for the full 4 Mbytes of display memory, when the extra 2 Mbytes of memory is installed. |
| JP2 - JP9 | Display Memory CAS#/WE# type select. | Select dual-CAS# DRAMs (Board default) – (these pins are shorted on the board, and so no jumper is needed.) | Select dual -WE# DRAM memory. Also, the traces between jumper positions 1 and 2 must be cut under these jumper blocks. |
| JP10 - JP12 | CRT R,G,B Impedance | No termination resistors on the R,G,B connections. | 150-ohm load termination resistor on each R,G,B connection. (these pins are shorted on the board, and so no jumpers are needed.) |
| JP25 | VACTI Connection to V-Port J1 | VACTI not connected to V-Port. See JP26 for alternate connection. | VACTI connected to V-Port J1 pin 41. (Board default)<br>**NOTE:**<br>If the video source does not supply a video capture enable signal on J1 pin 41, HREFI can be used as an enable signal by placing a jumper on J29 to connect the signal inputs. |
| JP26 | VACTI Connected to HREFI | VACTI and HREFI are not tied together, but HREFI is hardwired to V-Port J1 pin 49. | VACTI and HREFI are tied together. Both are connected to V-Port J1 pins 41 and 49. (Board default) |
| JP27 | 5 V Power to V-Port | V-Port is not powered. | 5 V is connected to the V-Port. (these pins are shorted on the board, and so no jumper is needed.) |
| JP28 | PCI Interrupt | PCI Interrupt not connected. (Board default) | PCI Interrupt connected. |
| JP29 | SW0 Line connection | SW0 pin not connected to switch S1. The SW0 pin can be used for external MCLK, but the trace between these pins must be cut. | SW0 pin connected to switch S1. (these pins are shorted on the board, and so no jumper is needed.) |
| JP30 - JP31 | IREF Circuit Selection | External IREF circuit connected. Both jumpers are on 1-2. | Internal IREF circuit connected. Both jumpers are on 2-3. (Board default) |
| JP33 | Initiate Hardware Suspend (when CR8D[2] is '1', Suspend enabled) | When CR8D[3] is '0' (SUSPI pin is active high), removing the jumper initiates Suspend mode. | When CR8D[3] is '1' (SUSPI pin is active low), adding the jumper initiates Suspend mode. |
| JP34 | 14 MHz Clock Source | No clock source connected. | 14 MHz clock source connected. |
| JP36 | 5 V Total Current | | Measure total current drawn by CL-GD7555 from 5 V supply. |

**Table 3. Settings for the PCI Bus Demonstration Board Jumper and Header Blocks** *(cont.)*

| Jumper / Header Block No. | Jumper / Header Block Functions | If 3-Position Block: Function of *Jumpers on 1-2*<br>If 2-Position Block: Function of *No Jumper* | If 3-Position Block: Function of *Jumpers on 2-3*<br>If 2-Position Block: Function of *Jumper On* |
|---|---|---|---|
| JP37 | 3.3 V Total Current | | Measure total current drawn by CL-GD7555 from 3.3 V supply. |
| JP38 | Select 5 V or 3.3 V for CVDD,DACVDD,MAVDD and VAVDD | Connect 3.3 V supply to CVDD, DACVDD, MAVDD and VAVDD. | Connect 5.0 V supply to CVDD, DACVDD, MAVDD and VAVDD. (Board default) |
| JP39 | CVDD Total Current | | Measure total current drawn by CVDD. |
| JP40 | MAVDD Total Current | | Measure total current drawn by MAVDD. |
| JP41 | VAVDD Total Current | | Measure total current drawn by VAVDD. |
| JP42 | DACVDD Total Current | | Measure total current drawn by DACVDD. |
| JP43 | Select 5 V or 3.3 V for MVDD and Display Memory | Connect 3.3 V supply to MVDD and Display Memory. | Connect 5.0 V supply to MVDD and Display Memory. (Board default) |
| JP44 | MVDD Total Current | | Measure total current drawn by MAVDD. |
| JP46 | Display-Memory Total Current | | Measure total current drawn by Display Memory. |
| JP47 | Select 5 V or 3.3 V for FPVDD and Panel Power Supply VDD<br>**WARNING:**<br>To prevent damage to the flat panel, before connecting it, properly set the flat panel voltages. | Connect 3.3 V supply to FPVDD and Panel Power Supply VDD. | Connect 5.0 V supply to FPVDD and Panel Power Supply VDD. (Board default) |
| JP48 | FPVDD Total Current | | Measure total current drawn by FPVDD. |
| JP50 | Select 5 V or 3.3 V for CRTVDD | Connect 3.3 V supply to CRTVDD. | Connect 5.0 V supply to CRTVDD. (Board default) |
| JP51 | CRTVDD Total Current | | Measure total current drawn by CRTVDD. |
| JP52 | VIO Total Current | | Measure total current drawn VIO. |
| JP53 | Select either VIO or 3.3 V for BVDD and OSC VDD | Connect 3.3-V supply to BVDD and OSC VDD. | Connect VIO supply to BVDD and OSC VDD. (Board default) |

**Table 3. Settings for the PCI Bus Demonstration Board Jumper and Header Blocks** *(cont.)*

| Jumper / Header Block No. | Jumper / Header Block Functions | If 3-Position Block: Function of *Jumpers on 1-2*<br>If 2-Position Block: Function of *No Jumper* | If 3-Position Block: Function of *Jumpers on 2-3*<br>If 2-Position Block: Function of *Jumper On* |
|---|---|---|---|
| JP54 | BVDD Total Current | | Measure total current drawn by BVDD. |
| JP58 | Voltage Switching VDD Selection | Voltage Switching is not connected. (Board default) | Voltage Switching is connected. |

## 2.5 Selecting the LCD Panel Type Configuration – S1 Switch Settings

S1 is an 4-position DIP switch block for selecting the type of flat panel that the controller supports. Switches positions 1, 2 and 3 are connected to the SW[0:2] pins of the CL-GD7555, and their settings are read and stored by the chip during Reset. The Cirrus Logic BIOS reads these stored bits to determine the proper configuration for the CL-GD7555.

- The switch positions are defined: '0' is open and '1' is closed. A '1' connects a pullup resistor to the appropriate SW/MD pin for SW1 and SW2.
- The settings for switch S1, position 4 is a 'don't care'.
- Other LCDs can be supported by using the Cirrus Logic OEMSI Utility (a BIOS customization utility) to change the BIOS default parameters. To obtain parameters for other panels call the Cirrus Logic Bulletin Board Service at USA (510) 440-9080.

### Table 4. Settings for Switch Block S1

| Panel Type | Code for Panel Supported | Panel Description (All Panels Are Color) | Panel Screen Format | Switch Position Setting | | |
|---|---|---|---|---|---|---|
| | | | | 1 | 2 | 3 |
| 0 | *Reserved* | – | – | 0 | 0 | 0 |
| 1 | C256KSS-36 | Single-scan active-matrix TFT<br>18-bit or 12-bit, 2-pixels-per-clock panels.<br>These panels use both CONN2 and CONN3 (the extended TFT connector). | 1024 × 768 | 1 | 0 | 0 |
| 2 | C8DD-16 | Dual-scan passive STN<br>16-bit | 640 × 480 | 0 | 1 | 0 |
| 3 | C256KSS-18 (default)<br>C4KSS-12<br>C512SS-9 | Single-scan active-matrix TFT<br>24-bit, 18-bit, 12-bit, or 9-bit | 640 × 480 | 1 | 1 | 0 |
| 4 | *Reserved* | – | – | 0 | 0 | 1 |
| 5 | *Reserved* | – | – | 0 | 0 | 1 |
| 6 | C8DD-16 | Dual-scan passive STN<br>16-bit | 800 × 600 | 0 | 1 | 1 |

## 2.6 Connecting and Using the Power Module

This section explains how to connect and adjust the Power Module.

Use the jumper settings described in Table 3 to choose whether the Power Module supplies 3.3 or 5 VDC to the CL-GD7555 and to an LCD panel. If LCD voltage supply outputs need adjustment, use the procedures described in Section 2.8.2 through Section 2.8.4.

### 2.6.1 Connecting the Power Module

The Demonstration Board ships with the Power Module attached to it. However, if the Power Module has been removed, connect it to the Demonstration Board as follows:

1. Set the voltage jumper blocks listed in Table 3 as required.
2. Position the Power Module male connector over the female header block JP15, position the female connector over the male header block JP23, and press the Module into place. (For orientation, refer to Figure 2–1)

### 2.6.2 Power Module 3.3-V Adjustment Procedure

If the Demonstration Board jumpers are set for 3.3-V operation, you may adjust the Power Module's 3.3-V Core Voltage output as follows:

1. Monitor the Core Voltage on test points JD pin 11, JF pin 5, or JO pin 12.
2. To set the Core Voltage, use the Core Voltage Adjust potentiometer (VCC3V). Figure 2–3 shows the location of the potentiometer.

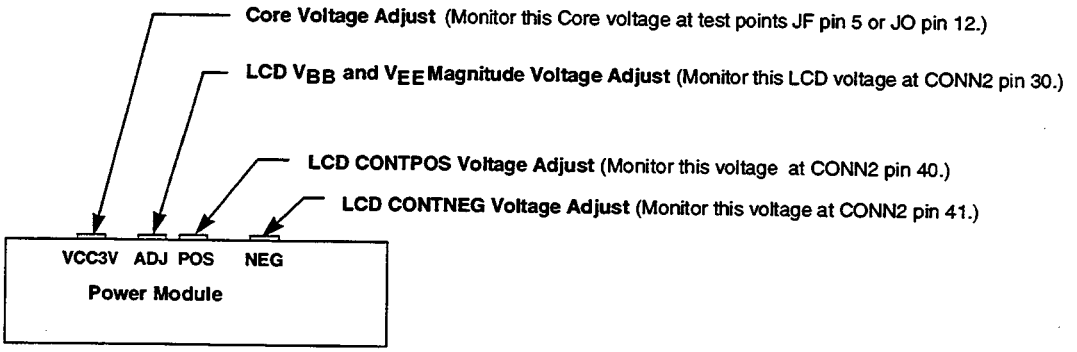



**Figure 2–2. Power Module Adjustment Controls**

### 2.6.3 Power Module LCD Voltage Adjustment Procedure

To adjust the Power Module so that it delivers the manufacturer's recommended LCD voltage supply:

1. Identify the correct voltage required by the LCD panel. Refer to the manufacturer's data sheets or the Cirrus Logic 'Panel Interface Guide' for this information.
2. With the power off, disconnect the LCD panel before proceeding.
3. Turn the system on and use the *CLMODE* utility to initiate an LCD panel power-up sequence.
4. While measuring the voltage at connector CONN2 pin 30, adjust the "ADJ" potentiometer until the LCD voltage is the correct value.

### 2.6.4 Power Module CONTPOS Voltage Adjustment Procedure

To adjust the CONTPOS output of the Power Module:

1. With the system power off, disconnect the LCD panel.
2. Turn the system on and use the *CLMODE* utility to initiate an LCD power-up sequence.
3. While measuring CONTPOS at connector CONN2 pin 40, adjust the "POS" potentiometer to produce the required output.

### 2.6.5 Power Module CONTNEG Voltage Adjustment Procedure

To adjust the CONTNEG output of the Power Module:

1. With the system power off, disconnect the LCD panel.
2. Turn the system on and use the *CLMODE* utility to initiate an LCD power-up sequence.
3. While measuring CONTNEG at connector CONN2 pin 41, adjust the "NEG" potentiometer to produce the required output.

## 2.7 LCD Panel Interface Connections

The LCD panels are connected to the Demonstration Board through connectors CONN2 and CONN3. The mapping of the panel input and output signals is given in the shown in Table 5. The FP pin names in the Demonstration Board schematics are different than those specified in early versions of the Hardware Reference Manual.

**Table 5. CL-GD7555 Demonstration Board Interface Pins to LCD Flat Panels**

| LCD Flat Panel Type with Corresponding Pin Connections | | | | | | | | CL-GD7555 | Demonstration Board | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TFT LCD Types | | | | | | STN LCD Types | | | | | |
| TFT with 1-Pixel/Clock | | | | TFT with 2-Pixels/Clock[a] | | Color | | Pin No. | Pin Name | CONN 2Pin No. | CONN3 Pin No. |
| 24-Bit | 18-Bit | 12-Bit | 9-Bit | 18-Bit | 12-Bit | 16-Bit | 8-Bit | | | | |
| R7 | R5 | R3 | R2 | $R_A5$ | $R_A3$ | SUD3 | — | 176 | FP17 | 13 | |
| R6 | R4 | R2 | R1 | $R_A4$ | $R_A2$ | SUD2 | — | 175 | FP16 | 14 | |
| R5 | R3 | R1 | R0 | $R_A3$ | $R_A1$ | SUD1 | — | 174 | FP15 | 15 | |
| R4 | R2 | R0 | — | $R_A2$ | $R_A0$ | SUD0 | — | 173 | FP14 | 16 | |
| R3 | R1 | — | — | $R_A1$ | — | SUD7 | — | 172 | FP13 | 9 | |
| R2 | R0 | — | — | $R_A0$ | — | SUD6 | — | 170 | FP12 | 10 | |
| R1 | — | — | — | — | — | — | — | 146 | FP31 | 33 | |
| R0 | — | — | — | — | — | — | — | 145 | FP30 | 43 | |
| G7 | G5 | G3 | G2 | $G_A5$ | $G_A3$ | SLD7 | SUD3 | 169 | FP11 | 8 | |
| G6 | G4 | G2 | G1 | $G_A4$ | $G_A2$ | SLD6 | SUD2 | 168 | FP10 | 7 | |
| G5 | G3 | G1 | G0 | $G_A3$ | $G_A1$ | SLD5 | SUD1 | 167 | FP9 | 6 | |
| G4 | G2 | G0 | — | $G_A2$ | $G_A0$ | SLD4 | SUD0 | 166 | FP8 | 5 | |
| G3 | G1 | — | — | $G_A1$ | — | SUD5 | — | 164 | FP7 | 11 | |
| G2 | G0 | — | — | $G_A0$ | — | SUD4 | — | 163 | FP6 | 12 | |
| G1 | — | — | — | | — | — | — | 139 | FP25 | 42 | |
| G0 | — | — | — | | — | — | — | 138 | FP24 | 44 | |
| B7 | B5 | B3 | B2 | $B_A5$ | $B_A3$ | SLD3 | SLD3 | 162 | FP5 | 4 | |
| B6 | B4 | B2 | B1 | $B_A4$ | $B_A2$ | SLD2 | SLD2 | 161 | FP4 | 3 | |
| B5 | B3 | B1 | B0 | $B_A3$ | $B_A1$ | SLD1 | SLD1 | 160 | FP3 | 2 | |
| B4 | B2 | B0 | — | $B_A2$ | $B_A0$ | SLD0 | SLD0 | 159 | FP2 | 1 | |
| B3 | B1 | — | — | $B_A1$ | — | — | — | 158 | FP1 | 23 | |
| B2 | B0 | — | — | $B_A0$ | — | — | — | 157 | FP0 | 39 | |
| B1 | — | — | — | — | — | — | — | 132 | FP19 | 29 | |
| B0 | — | — | — | — | — | — | — | 131 | FP18 | 20 | |
| FPVDCLK | | | | FPVDCLK | | SCLK | | 155 | | 18 | |
| LLCLK | | | | — | | LP | | 153 | | 35 | |
| LFS | | | | LFS | | FLM | | 156 | | 22 | |
| DE | | | | DE | | — | | 152 | | 26 | |
| FPVEE | | | | FPVEE | | FPVEE | | 123 | | 37 | |
| FPVCC | | | | FPVCC | | FPVCC | | 125 | | 38 | |
| (Optional) | | | | (Optional) | | (Optional) | | 124 | | | |

a. See Table continued on following page for $R_B$, $G_B$ and $B_B$ pin locations.

**Table 5. CL-GD7555 Demonstration Board Interface Pins to LCD Flat Panels** *(cont.)*

| LCD Flat Panel Type with Corresponding Pin Connections | | | | | | | | CL-GD7555 | Demonstration Board | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TFT LCD Types | | | | | | STN LCD Types | | | | | |
| TFT with 1-Pixel/Clock | | | | TFT with 2-Pixels/Clock[a] | | Color | | Pin No. | Pin Name | CONN 2Pin No. | CONN3 Pin No. |
| 24-Bit | 18-Bit | 12-Bit | 9-Bit | 18-Bit | 12-Bit | 16-Bit | 8-Bit | | | | |
| See Previous Page | | | | $R_{B5}$ | $R_{B3}$ | See Previous Page | | 150 | FP35 | | 14 |
| | | | | $R_{B4}$ | $R_{B2}$ | | | 149 | FP34 | | 13 |
| | | | | $R_{B3}$ | $R_{B1}$ | | | 148 | FP33 | | 12 |
| | | | | $R_{B2}$ | $R_{B0}$ | | | 147 | FP32 | | 11 |
| | | | | $R_{B1}$ | — | | | 146 | FP31 | 33 | |
| | | | | $R_{B0}$ | — | | | 145 | FP30 | 43 | |
| | | | | $G_{B5}$ | $G_{B3}$ | | | 144 | FP29 | | 10 |
| | | | | $G_{B4}$ | $G_{B2}$ | | | 143 | FP28 | | 9 |
| | | | | $G_{B3}$ | $G_{B1}$ | | | 141 | FP27 | | 7 |
| | | | | $G_{B2}$ | $G_{B0}$ | | | 140 | FP26 | | 6 |
| | | | | $G_{B1}$ | — | | | 139 | FP25 | 42 | |
| | | | | $G_{B0}$ | — | | | 138 | FP24 | 44 | |
| | | | | $B_{B5}$ | $B_{B3}$ | | | 137 | FP23 | | 5 |
| | | | | $B_{B4}$ | $B_{B2}$ | | | 136 | FP22 | | 4 |
| | | | | $B_{B3}$ | $B_{B1}$ | | | 135 | FP21 | | 3 |
| | | | | $B_{B2}$ | $B_{B0}$ | | | 133 | FP20 | | 2 |
| | | | | $B_{B1}$ | — | | | 132 | FP19 | 29 | |
| | | | | $B_{B0}$ | — | | | 131 | FP18 | 20 | |

a. See Table on previous page for $R_A$, $G_A$ & $B_A$ pin locations.

# 3. Connecting and Operating the Demonstration Board

Use the following checklist when installing, connecting to, and operating the Demonstration Board.

## 3.1 Checklist

____ 1. Verify the Demonstration Board is labeled "GDB7555-C-DM1-1 ".

____ 2. If desired, to set the CL-GD7555 registers for Standby mode and Suspend mode, refer to the Cirrus Logic *OEMSI User's Manual* and the *CL-GD7555 Hardware Reference Manual*.

____ 3. Verify the Demonstration Board connectors and jumper settings. (Refer to Section 2.3 through Section 2.4.)

**WARNING:**

The Demonstration Board voltage jumpers must be properly set *before* you apply power, or damage may result to the Demonstration Board or the LCD panel.

____ 4. Verify the switch settings for switch blocks S1, S2 and S3. (Refer to Section 2.5)

____ 5. If the Power Module is not already installed on the Demonstration Board, install it. (Refer to Section 2.6)

▼ **WARNING:** At Step 6 **DO NOT** connect the LCD panel and its connector to the Demonstration Board, or the LCD panel may be damaged. Connect the panel only after Step 10.

____ 6. Connect a CRT to CONN1, the CRT DB15 connector on the Demonstration Board. (When a CRT is connected, the system starts up (boots) to the CRT, even if an LCD is connected. Otherwise, when a CRT is not used, and only an LCD is used, the system boots to the LCD.)

____ 7. Turn on the system.

____ 8. Ensure that the Core Voltage is correct (3.3 V or 5 V). Measure the Core Voltage level from the Power Module.

____ 9. Ensure that the voltage level is correct for the LCD panel you will use. Refer to the manufacturer's data sheets or the Cirrus Logic "Panel Interface Guide" in the *CL-GD7555 Application Book* for the correct value for the panel, and then set the ADJ voltage potentiometer on the Power Module as needed.

____ 10. Use the Cirrus Logic utility *CLMODE*, which is provided on a diskette that comes with the Demonstration Board kit, to set the system to SimulSCAN mode and to check the power-sequencing voltage.
a. If the power sequence matches that in Figure 4–1, go to the next step.
b. Otherwise, if the power sequence does not match Figure 4–1, call Cirrus Logic.

____ 11. Use *CLMODE* to set the system to the CRT-only mode.

____ 12. To connect the LCD panel, do the following:
a. For panel connection information, refer to the "Panel Interface Guide" in the *CL-GD7555 Application Book.*
b. Connect the LCD panel to the 44-pin male connector supplied with the Demonstration Board kit. When TFT 2-pixels-per-clock panels are used, the 16-pin TFT-panel extension connector must also be connected. See Section 2.7 for details.
c. Attach the LCD panel connector(s) to CONN2, the 44-pin female connector (and CONN3 the 16-pin extension connector) on the Demonstration Board.

____ 13. Use *CLMODE* to select either SimulSCAN (for CRT and LCD) or LCD-only mode.

____ 14. If desired, to control various Demonstration Board features, use the Cirrus Logic utility *PCLREGS*, which is provided on diskette.

## 3.2 Directions for Installing Windows 3.1 Drivers

1) Change Windows 3.1 display driver to 'VGA.drv'.
2) Install standard VGA display adapter.
3) Install CL-GD7555 Windows 3.1 disk.
4) Run 'Setup' from Program Manager within Windows 3.1.
5) Follow instructions in setup program.

## 3.3 Directions for Installing Windows '95 Drivers

1) Install CL-GD7555 Windows '95 disk.
2) Run 'Setup' from within Windows.
3) Follow instructions in setup program. Copy all files from disk, even if they are older files than those currently installed on the disk.
4) After installing all the files, Windows '95 will ask you to restart.
5) Restart Windows and the correct driver should be loaded.
6) Now you are ready to run Windows '95 with the CL-GD7555.

# 4. Power Up-Power Down Sequence for LCD

This section discusses the CL-GD7555 power-up and power-down sequences for the LCD. Figure 4–1 shows these sequences:

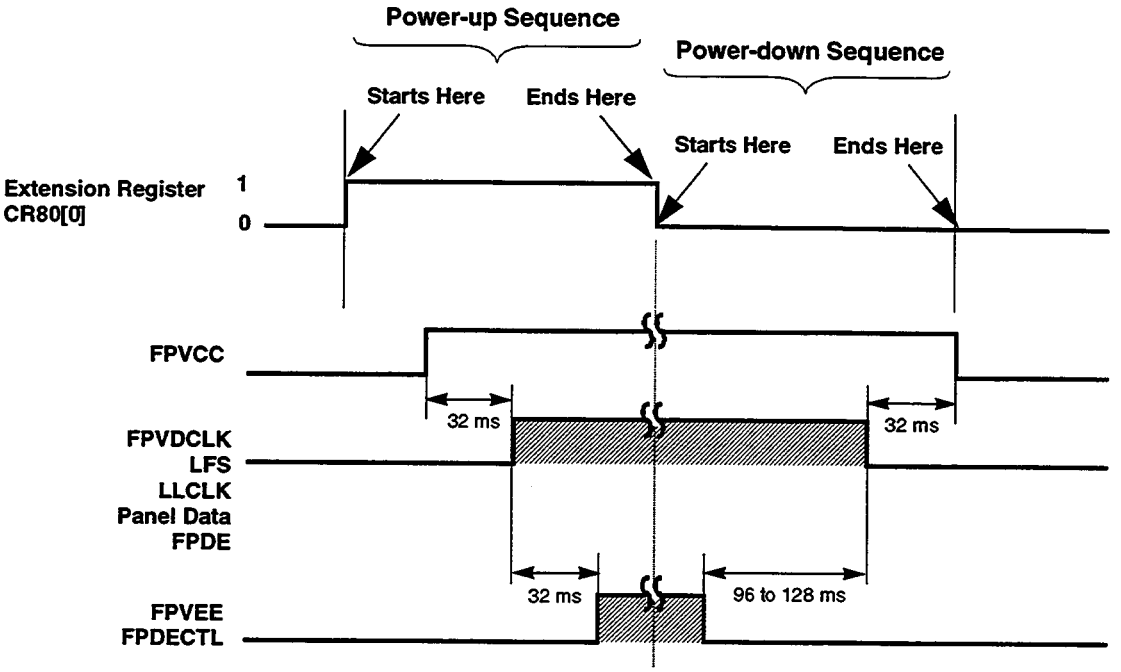



**Figure 4–1. Normal Power-Up/Power-Down Sequence**

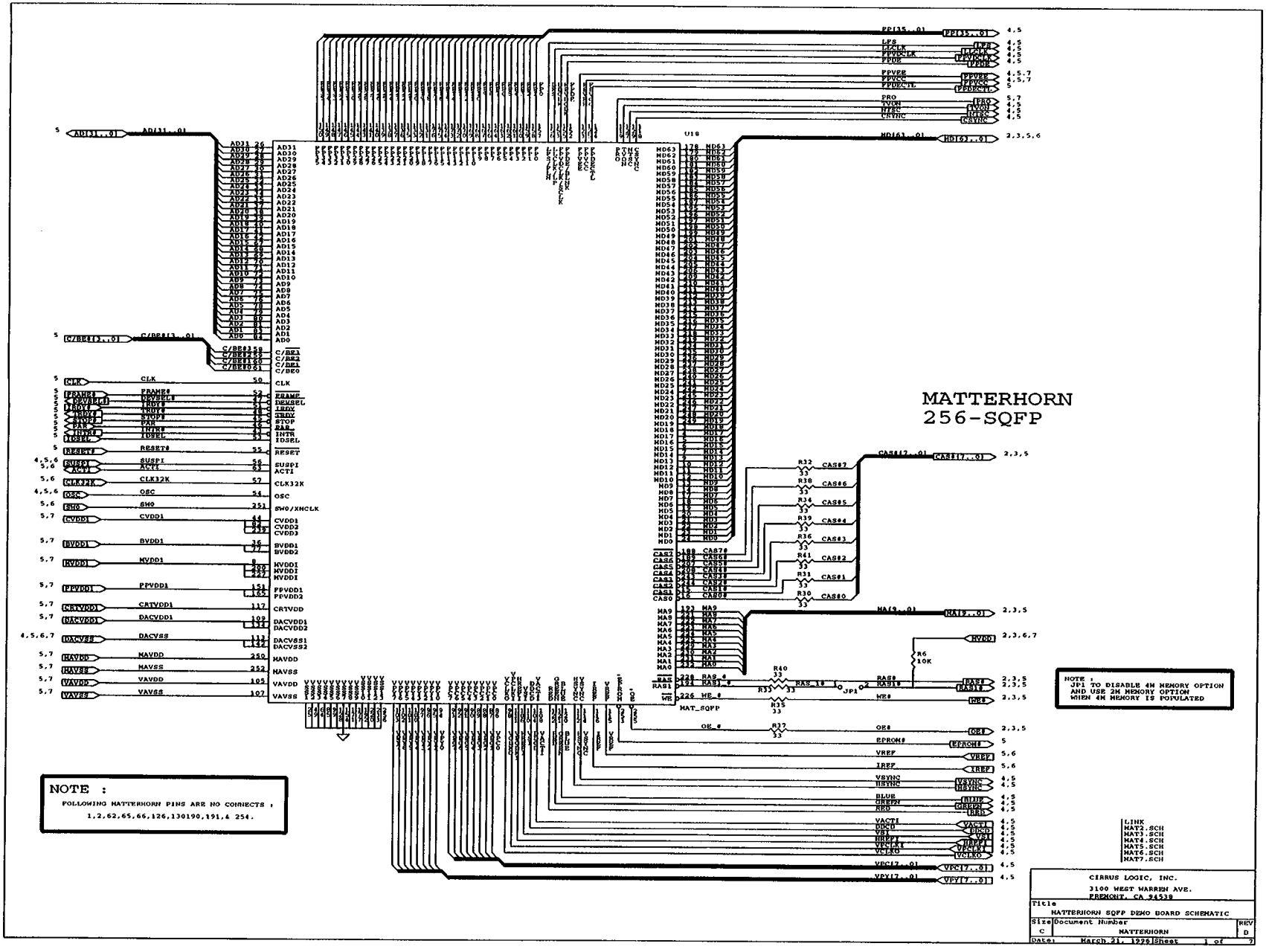
▼ WARNING: FPVCC and FPVEE are used to control the switching of appropriate voltages to the LCD. They must not be used to drive the LCD directly, or damage may occur to the LCD.

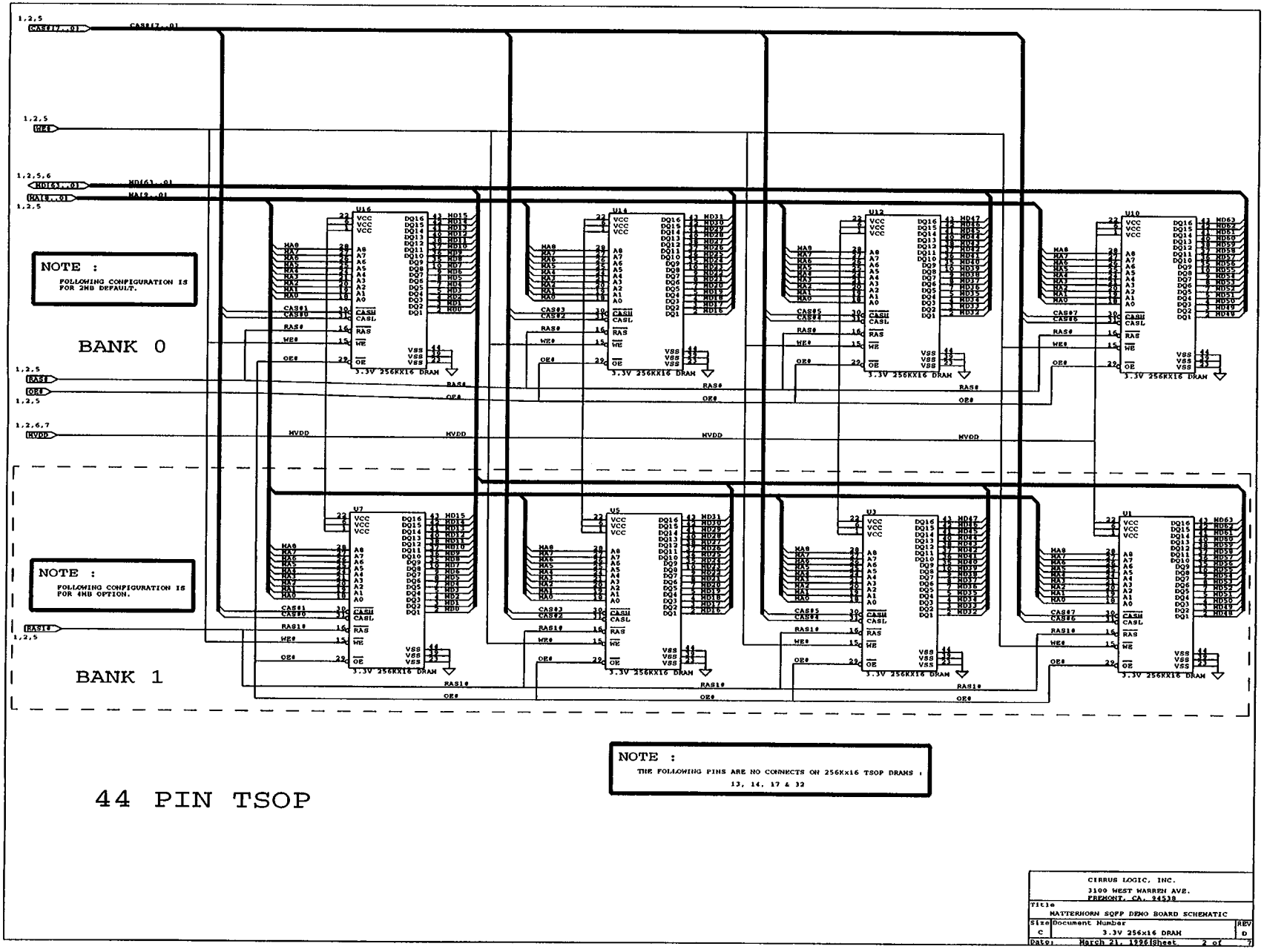
NOTES:

1) The LCD power-up sequence begins when any of the following occur:
   (a) When the LCD is powered on with Extension register CR80[0] transition from 0-to-1.
   (b) When Standby or Suspend modes are terminated, and the LCD was active prior to entering the Standby or Suspend mode
   (c) When switching from a CRT-only to LCD-only.
2) The LCD power-down sequence begins when any of the following occur:
   (a) When the LCD is powered off with Extension register CR80[0] transition from 1-to-0.
   (b) When Standby or Suspend modes are entered, and the LCD was active prior to entering the Standby or Suspend mode
   (c) When switching from LCD-only to a CRT-only.
3) For connections to specific LCDs, refer to Table 6 on page 18 and the 'Panel Interface Guide' in the *CL-GD7555 Applications Book.*
4) Use the Power Module to provide power for LCD operation. Specifically, the Power Module uses:
   (a) FPVCC to switch the LCD VCC supply voltage
   (b) FPVEE to switch the BIAS and CONTRAST supply voltages
   (c) FPDECTL to switch the LCD backlight supply voltage

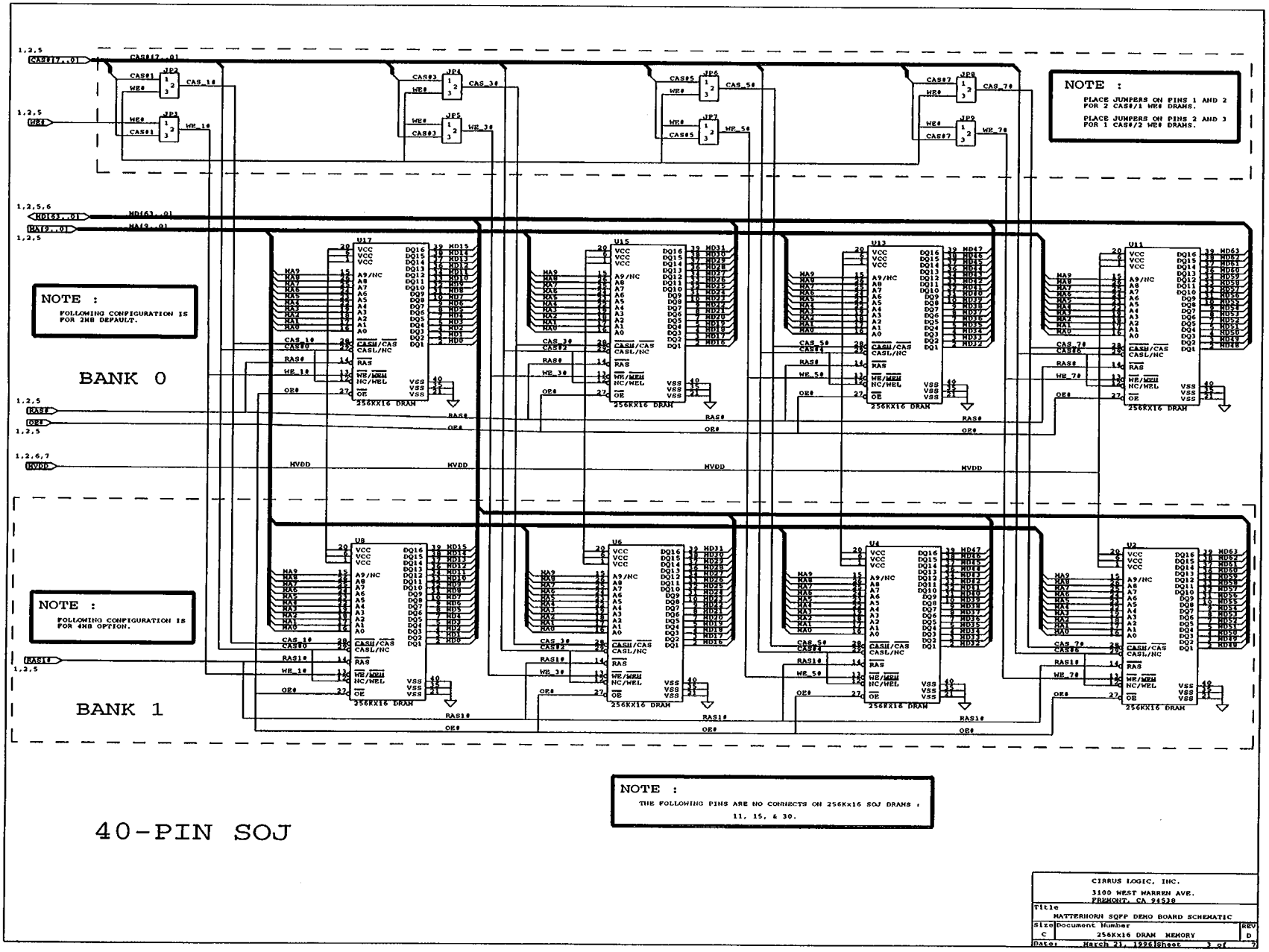
# Appendix A

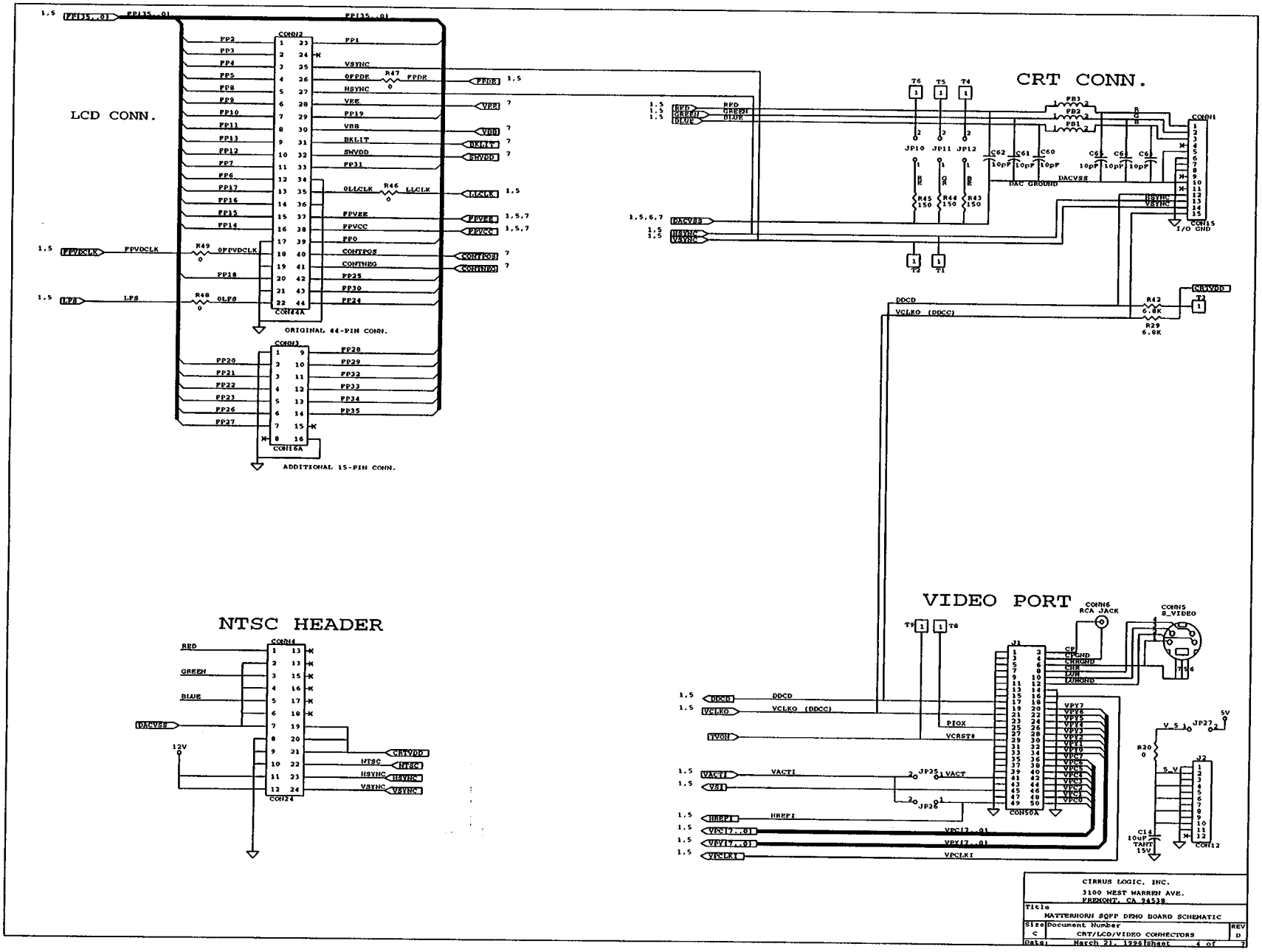
## *GDB7555-C-DM1-1 Demonstration Board Schematics*

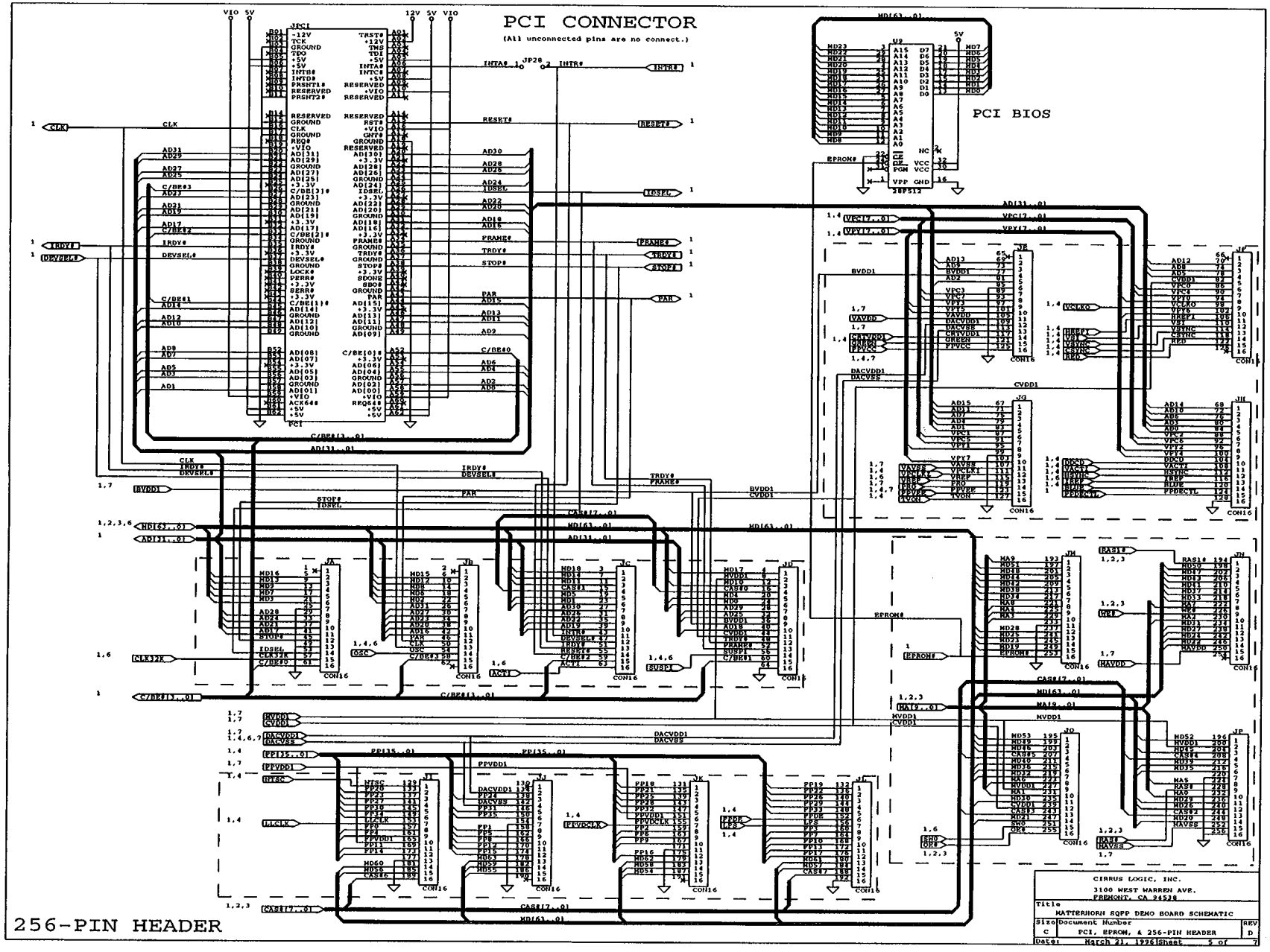

MATTERHORN
256-SQFP
NOTE :
POLLOWING MATTERHORN PINS ARE NO CONNECTS :
1,2,62,65,66,126,130190,191,& 254.
NOTE :
JP1 TO DISABLE 4M MEMORY OPTION
AND USE 2M MEMORY OPTION
WHEN 4M MEMORY IS POPULATED
LINK
MAT2.SCH
MAT3.SCH
MAT4.SCH
MAT5.SCH
MAT6.SCH
MAT7.SCH
CIRRUS LOGIC, INC.
3100 WEST WARREN AVE.
FREMONT, CA 94538
Title
MATTERHORN SQFP DEMO BOARD SCHEMATIC
Size C
Document Number
MATTERHORN
REV D
Date: March 21, 1996 Sheet 1 of 7



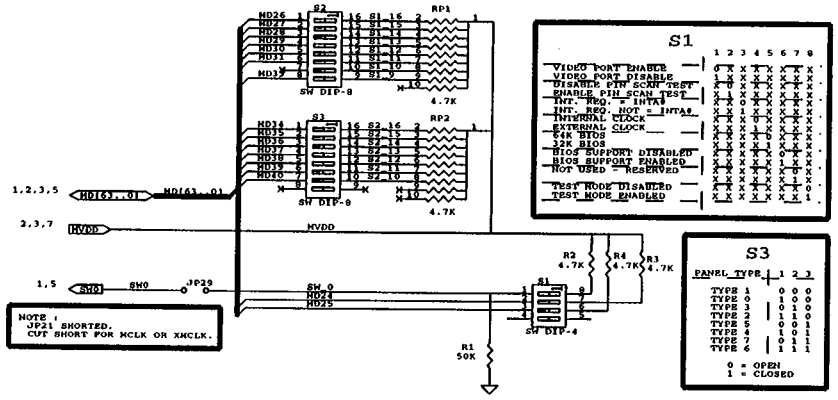

| | | |
|---|---|---|
| CIRRUS LOGIC, INC. 3100 WEST WARREN AVE. FREMONT, CA. 94538 | | |
| Title: MATTERHORN SOFP DEMO BOARD SCHEMATIC | | |
| Size: C | Document Number: 3.3V 256x16 DRAM | REV: D |
| Date: March 21, 1996 | Sheet 2 of 7 | |


NOTE :
PLACE JUMPERS ON PINS 1 AND 2 FOR 2 CAS#/1 WE# DRAMS.
PLACE JUMPERS ON PINS 2 AND 3 FOR 1 CAS#/2 WE# DRAMS.
NOTE :
FOLLOWING CONFIGURATION IS FOR 2MB DEFAULT.
BANK 0
NOTE :
FOLLOWING CONFIGURATION IS FOR 4MB OPTION.
BANK 1
256Kx16 DRAM
NOTE :
THE FOLLOWING PINS ARE NO CONNECTS ON 256Kx16 SOJ DRAMS : 11, 15, & 30.
40-PIN SOJ
CIRRUS LOGIC, INC.
3100 WEST WARREN AVE.
FREMONT, CA 94538
Title
MATTERHORN SQFP DEMO BOARD SCHEMATIC
Size C
Document Number
256Kx16 DRAM MEMORY
REV D
Date: March 21, 1996 Sheet 3 of 7


LCD CONN.
CRT CONN.
VIDEO PORT
NTSC HEADER
ORIGINAL 44-PIN CONN.
ADDITIONAL 15-PIN CONN.
CIRRUS LOGIC, INC.
3100 WEST WARREN AVE.
FREMONT, CA 94538
Title
HATTERHORN SOFP DEMO BOARD SCHEMATIC
Size C
Document Number
CRT/LCD/VIDEO CONNECTORS
REV D
Date: March 21, 1995 Sheet 4 of 7

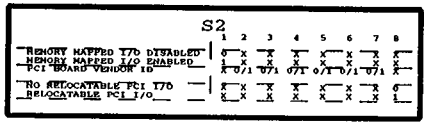

PCI CONNECTOR
(All unconnected pins are no connect.)
PCI BIOS
256-PIN HEADER
CIRRUS LOGIC, INC.
3100 WEST WARREN AVE.
FREMONT, CA 94538
Title
MATTERHORN SQFP DEMO BOARD SCHEMATIC
Size C
Document Number
PCI, EPROM, & 256-PIN HEADER
REV D
Date: March 21, 1996 Sheet 5 of 7

# CONFIGURATION SWITCHES







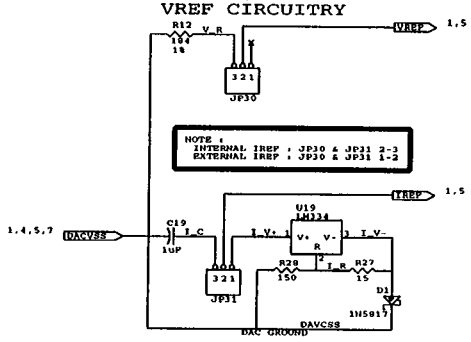



0 = OPEN
1 = CLOSE
X = DON'T CARE

ALL SWITCHES OPEN = DEFAULT CASE
NORMAL PCI CYCLE, FEATURE CONNECTOR SET FOR VIDEO PORT, INTERNAL CLOCK, NO BIOS SUPPORT, 256-PIN PACKAGE, NO TEST CONFIGURATIONS.

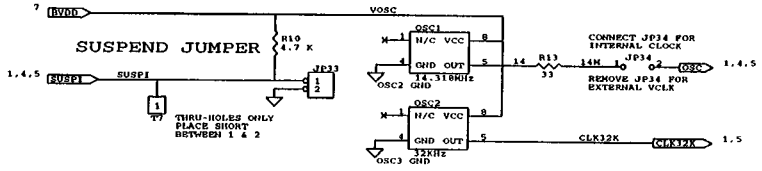



## VREF CIRCUITRY

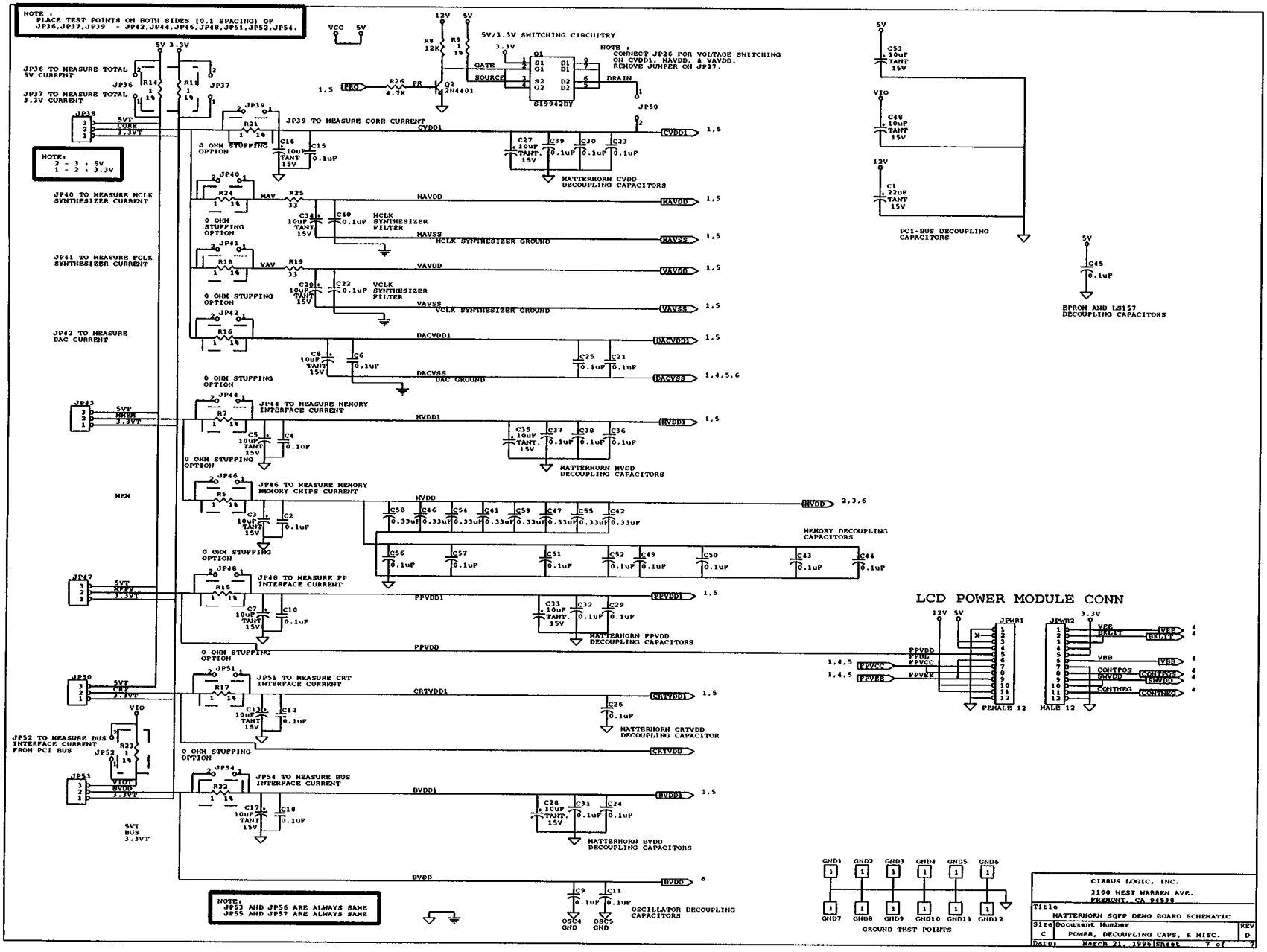



## IREF CIRCUITRY

# CLOCKS




| | | |
|---|---|---|
| CIRRUS LOGIC, INC. 3100 WEST WARREN AVE. FREMONT, CA 94538 | | |
| Title: MATTERHORN SQFP DEMO BOARD SCHEMATIC | | |
| Size: C | Document Number: CONFIG. SWITCHES, IREF, VREF, & MISC | REV: D |
| Date: March 21, 1996 | Sheet 6 of 7 | |


NOTE : PLACE TEST POINTS ON BOTH SIDES (0.1 SPACING) OF JP36,JP37,JP39 - JP42,JP44,JP46,JP48,JP51,JP52,JP54.
JP36 TO MEASURE TOTAL 5V CURRENT
JP37 TO MEASURE TOTAL 3.3V CURRENT
JP39 TO MEASURE CORE CURRENT
JP40 TO MEASURE MCLK SYNTHESIZER CURRENT
JP41 TO MEASURE FCLK SYNTHESIZER CURRENT
JP42 TO MEASURE DAC CURRENT
JP44 TO MEASURE MEMORY INTERFACE CURRENT
JP46 TO MEASURE MEMORY MEMORY CHIPS CURRENT
JP48 TO MEASURE PP INTERFACE CURRENT
JP51 TO MEASURE CRT INTERFACE CURRENT
JP52 TO MEASURE BUS INTERFACE CURRENT FROM PCI BUS
JP54 TO MEASURE BUS INTERFACE CURRENT
0 OHM STUFFING OPTION
NOTE: 2 - 3 : 5V 1 - 2 : 3.3V
5V/3.3V SWITCHING CIRCUITRY
NOTE : CONNECT JP26 FOR VOLTAGE SWITCHING ON CVDD1, MAVDD, & VAVDD. REMOVE JUMPER ON JP27.
SI9942DY
2N4401
CVDD1
MAVDD
MAVSS
VAVDD
VAVSS
DACVDD1
DACVSS
HVDD1
HVDD
PPVDD1
PPVDD
CRTVDD1
CRTVDD
BVDD1
BVDD
MATTERHORN CVDD DECOUPLING CAPACITORS
NCLK SYNTHESIZER FILTER
NCLK SYNTHESIZER GROUND
VCLK SYNTHESIZER FILTER
VCLK SYNTHESIZER GROUND
DAC GROUND
MATTERHORN HVDD DECOUPLING CAPACITORS
MEMORY DECOUPLING CAPACITORS
MATTERHORN PPVDD DECOUPLING CAPACITORS
MATTERHORN CRTVDD DECOUPLING CAPACITOR
MATTERHORN BVDD DECOUPLING CAPACITORS
OSCILLATOR DECOUPLING CAPACITORS
PCI-BUS DECOUPLING CAPACITORS
EPROM AND LS157 DECOUPLING CAPACITORS
LCD POWER MODULE CONN
JPWR1
JPWR2
FEMALE 12
MALE 12
NOTE: JP53 AND JP56 ARE ALWAYS SAME JP55 AND JP57 ARE ALWAYS SAME
GROUND TEST POINTS
CIRRUS LOGIC, INC.
3100 WEST WARREN AVE.
FREMONT, CA 94539
Title
MATTERHORN SQFP DEMO BOARD SCHEMATIC
Size C
Document Number
POWER, DECOUPLING CAPS, & MISC.
REV D
Date: March 21, 1996 Sheet 7 of 7

# Analog Voltage Filtering Requirements

***for the CL-GD7555 LCD/CRT Controller***

**Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application note presents information on optimizing the connections for the CL-GD7555 LCD/CRT controller, using appropriate filters.

**Applicability**

This document applies to the following products:

✔ CL-GD7555

**Related Documents**

– *CL-GD7555 Reference Manuals*

## 1. Purpose

For optimal operation, circuit designs using the CL-GD7555 controllers must provide a well-filtered VDD source to MCLK (the memory clock pin) and VCLK (the video clock pin).

## 2. Recommended Analog Voltage Filter Circuits

Figure 1 shows required components for an analog voltage filter circuit for the memory clock, and Figure 2 shows required components for an analog voltage filter circuit for the video clock.

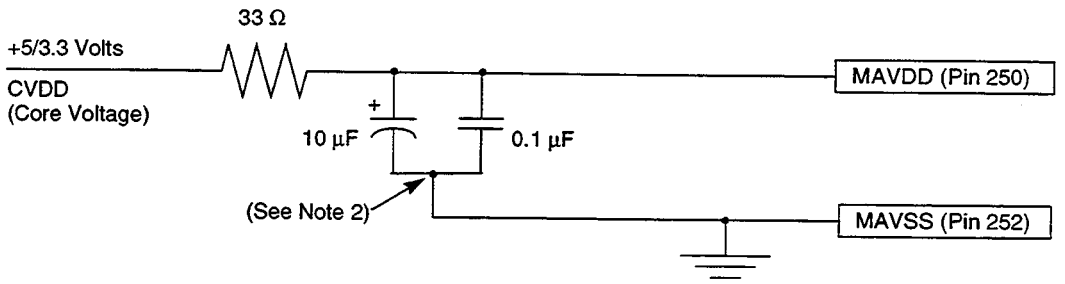



**Figure 1. Recommended Schematic for Analog Voltage Filter for Memory Clock**

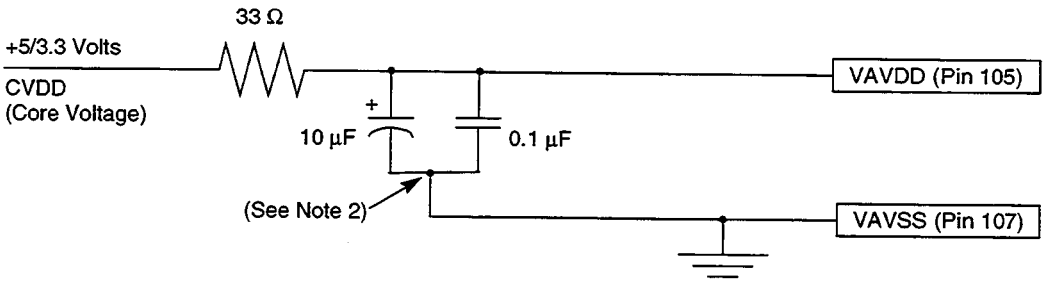



**Figure 2. Recommended Schematic for Analog Voltage Filter for Video Clock**

**NOTES:**

1) MAVDD (the supply voltage to the CL-GD7555 memory clock) and VAVDD (the supply voltage to the CL-GD7555 video clock) must be connected through the filter circuits shown.
2) The negative side of the capacitors must be connected together and to analog ground at one point.
3) The filter components must be located as close to the pins of the CL-GD7555 as possible.

CIRRUS LOGIC®

# CL-GD7555

*Advance Application Note — 7555-AN-4, v1.0*

# A Programmable Core-Voltage Solution

***for the CL-GD7555 LCD/CRT Controller***

**Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application note presents information on programming the CL-GD7555 LCD/CRT controller to a voltage of either 3.3 or 5 V.

**Applicability**

This document contains CL-GD7555 connectivity data that can be applied to user applications.

This document applies to the following products:

✔ CL-GD7555

**Related Documents**

– *CL-GD7555 Reference Manuals*



***Version 1.0***

***June 19, 1996***

# 1. Introduction

The CL-GD7555 supports dynamic selective switching of the Core VDD between 3.3 and 5 V. This capability allows a designer to support display modes that are possible only when the CL-GD7555 core operates at 5 V. However, for best power consumption the system can operate at 3.3 V. Since programming of the core voltage depends on the requirements of the display mode setting, the higher voltage must be used only when absolutely necessary to support a specific display mode.

This application note describes a two-part method for optimizing both performance and power consumption for the CL-GD7555. The method uses the following:

- A circuit which includes the Siliconix Si9942DY chip
- One of the three available CL-GD7555 programmable output pins, PROG[2:0], pins 129, 119, and 127 respectively, which can be programmed by Extension register bits SR2F[7:5] to select a core VDD of either 3.3 or 5 V

# 2. Background

The MCLK (Memory Clock) setting for the CL-GD7555 can be changed, depending on which factor is more desirable: maximizing CL-GD7555 performance or minimizing CL-GD7555 power consumption.

**NOTE:** Both the core VDD and analog VDD to the CL-GD7555 must always be set to the same level.

## 2.1 Operation with 5 V: MCLK of 80 MHz

To run the MCLK at 80 MHz, both the core VDD and analog VDD must always be set for 5 V. The MCLK must run at 80 MHz to maximize performance for the following display modes:

- CRT-only display modes:
  - 68h when horizontal frequency is 68.677 kHz
  - 6Dh when horizontal frequency is 64 kHz
  - 74h when horizontal frequency is 68.677 kHz
  - 79h when horizontal frequency is either 48.3 or 56 kHz
- Flat panel-only or SimulSCAN display mode 79h

## 2.2 Operation with 3.3 V: MCLK of 66 MHz

For those display modes that are less limited by bandwidth, a 66-MHz MCLK is sufficient to achieve very good performance. In this case, active power can be minimized by setting the core VDD and analog VDD to 3.3 V.

# 3. Circuit Description

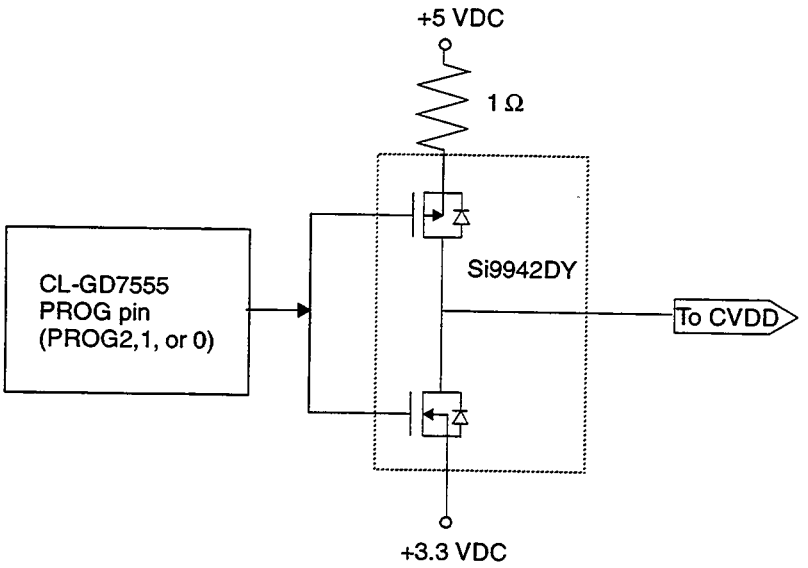
The circuit includes a Siliconix Si9942DY dual-enhancement-mode N-channel and P-channel MOSFET (metal-oxide semiconductor field-effect transistor). This part was chosen for two reasons.

- First, it is packaged in a small, 8-pin, surface-mount-technology package.
- Second, its maximum drain current rating at 25° C is 3 A. This rating is more than enough to supply the core VDD, which typically draws less than 300 mA during 5-V operation.

## 3.1 Circuit Theory of Operation

As shown in Figure 1, the Si9942DY part works as follows.

- If a low signal is applied to both gate inputs of the Si9942DY, the N-Channel device is turned off, and the P-Channel device is turned on, thereby supplying 5 V to CVDD.
- If a high signal is applied to both gate inputs of the Si9942DY, the N-Channel device is turned on, and the P-Channel device is turned off, thereby supplying 3.3 V to CVDD.




Program a PROG*n* pin to:
Low for the Si9942DY circuit to output a 5-V CVDD.
High for the Si9942DY circuit to output a 3.3-V CVDD.

**Figure 1. Diagram of Si9942DY**

## 3.2 Circuit Design

When both gates of the circuit design shown in Figure 1 are conducting (which happens when the programmable output from PROG*n* is switching states), the circuit current must be limited. To limit the circuit current, a 1-Ω resistor is placed in series with the 5-V supply. When the Si9942DY is operating at 5 V, the voltage dropped across this 1-Ω resistor does not affect the operation of the Si9942DY.

When MCLK is switched to 80 MHz (that is, 12.5 ns), the DRAM used must be able to handle a 2-MCLK page-cycle time and 9-MCLK random-cycle time.

To ensure a steady power supply going to the chip, a 10-µF capacitor must be placed on the output. (Refer to Figure 2 in Section 3.4.)

## 3.3 Programming the Circuit

As shown in the table below, to program the core voltage value for the circuit shown in Figure 1, use one of the Extension register bits SR2F[7:5], each of which controls the logic state of a selected PROG*n* pin.

**Table 1. Programming for CVDD Voltage Level**

| For a CVDD of: | Program one of the bits in SR2F[7:5] to: |
|---|---|
| 3.3 V | 1 |
| 5 V | 0 |

- For the following display modes, the CL-GD7555 can be optimized for performance by programming Extension register SR2F[7:5] to a zero, which sets a selected PROG*n* pin to a low and delivers 5 V to the core VDD.
  - CRT-only display modes:
    - 68h when horizontal frequency is 68.677 kHz
    - 6Dh when horizontal frequency is 64 kHz
    - 74h when horizontal frequency is 68.677 kHz
    - 79h when horizontal frequency is either 48.3 or 56 kHz
  - Flat panel-only or SimulSCAN display mode 79h
- For most display modes, the CL-GD7555 can be optimized for power consumption by programming Extension register SR2F[7:5] to a one, which sets the selected PROG*n* pin to a high and delivers 3.3 V to the core VDD.

## 3.4 Sample Circuit

As shown in the circuit in Figure 2, the 2N4401 is connected to the gate inputs of the Si9942DY. When the selected PROG*n* pin output is:

- Low (that is, zero volts), the gate inputs of the Si9942DY go to 12 V.
- High, the 2N4401 turns on. Consequently, the output of the 2N4401 goes low, and the gate inputs of the Si9942DY go to zero volts.

The circuit switches from 5 to 3.3 V in approximately 500 µsec. The circuit switches from 3.3 to 5 V in approximately 100 µsec. The switching time is limited largely by:

- The 10-µF bypass capacitors connected to the Core VDD pins.
- The value of the resistor connected to the collector of the bipolar transistor.

**NOTE:** To decrease the switching time, a smaller value resistor can be used, but at the expense of increased power consumption when the transistor is on.

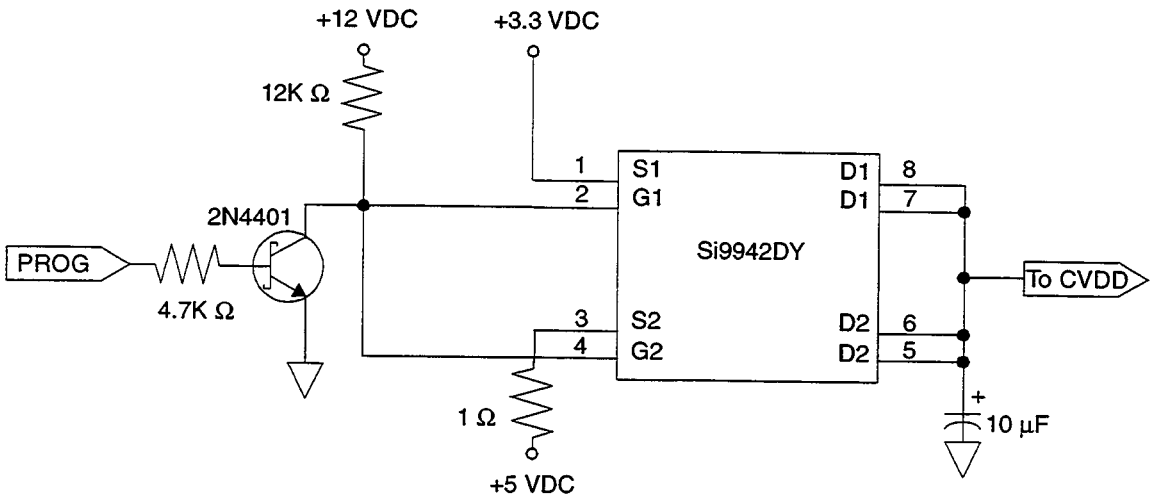



**Figure 2. Sample Circuit Schematic**

# State Information on Pad Control Signals

***for the CL-GD7555 LCD/CRT Controller***

**Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application note presents state information on the pad control signals of the Cirrus Logic CL-GD7555 LCD/CRT controller.

**Applicability**

This document applies to the following products:

✔ CL-GD7555

**Related Documents**

– *CL-GD7555 Reference Manuals*

# 1. Introduction

This application note documents each CL-GD7555 pad control signal under each of the following four conditions:

- The flat panel is in Standby mode, under software control.
- The flat panel is in Suspend mode, under hardware control.
- The flat panel is in Suspend mode, under software control.
- The flat panel is in Reset Operation.

# 2. Pad Control Signals and States

**IMPORTANT:** Some of the previous documentation for the CL-GD7555 incorrectly listed the names and numbers for the FP[35:0] pin functions. In Table 2-1, Column 1 lists the previous pin name, Column 2 lists the corrected pin name, Column 3 lists the PQFP pin number, and Column 4 lists the PBGA ball position.

**Table 2-1. Corrected Pin Names**

| Previous Pin Name | Corrected Pin Name | PQFP Pin Number | PBGA Ball Position |
|---|---|---|---|
| FP35 | FP17 | 176 | G17 |
| FP34 | FP16 | 175 | G20 |
| FP33 | FP15 | 174 | G19 |
| FP32 | FP14 | 173 | G18 |
| FP31 | FP13 | 172 | H17 |
| FP30 | FP12 | 170 | H19 |
| FP29 | FP11 | 169 | H18 |
| FP28 | FP10 | 168 | J17 |
| FP27 | FP9 | 167 | J20 |
| FP26 | FP8 | 166 | J19 |
| FP25 | FP7 | 164 | K17 |
| FP24 | FP6 | 163 | K20 |
| FP23 | FP5 | 162 | K19 |
| FP22 | FP4 | 161 | K18 |
| FP21 | FP3 | 160 | L17 |
| FP20 | FP2 | 159 | L20 |
| FP19 | FP1 | 158 | L19 |
| FP18 | FP0 | 157 | L18 |
| FP17 | FP35 | 150 | N19 |
| FP16 | FP34 | 149 | N18 |
| FP15 | FP33 | 148 | P17 |
| FP14 | FP32 | 147 | P20 |
| FP13 | FP31 | 146 | P19 |
| FP12 | FP30 | 145 | P18 |
| FP11 | FP29 | 144 | R17 |
| FP10 | FP28 | 143 | R20 |
| FP9 | FP27 | 141 | R18 |
| FP8 | FP26 | 140 | T17 |
| FP7 | FP25 | 139 | T20 |
| FP6 | FP24 | 138 | T19 |
| FP5 | FP23 | 137 | T18 |
| FP4 | FP22 | 136 | U19 |
| FP3 | FP21 | 135 | U20 |
| FP2 | FP20 | 133 | V18 |
| FP1 | FP19 | 132 | V19 |
| FP0 | FP18 | 131 | V20 |

For Table 2–2, which follows, note the following.

- Pins are listed by number and ball position.
- Some pins have more than one name, to indicate that the pin has more than one function.
- Pins names (and functions) that apply only to specific CL-GD7555 products are indicated.
- The following symbols and abbreviations are used to describe pin functions under the specified conditions. (Pin functions are described in the CL-GD7555 Reference Manuals.)

| | |
|---|---|
| # | Pin function is active-low. |
| A | Pin function is active. |
| H | High. There are 5 volts on the pin. |
| I | Pin functions as an input. |
| I(A) | Pin functions as an active input. |
| I/O | Pin functions as both an input and an output. (The pin function is bidirectional.) |
| I or O | Pin functions as an input or an output, depending on the mode or configuration used. |
| L | Low. There are 0 volts on the pin. |
| NA | Not applicable. |
| Note 1 | When self-refresh DRAMs are used, all CAS# and RAS# output pins are low (L) during both hardware- and software-controlled Suspend modes. |
| Note 2 | An external pull-up resistor is needed for this option. |
| Note 3 | When Extension register bit CR51[3] = 0, the V-Port is disabled and V-Port inputs are a 'don't care'.<br>When Extension register bit CR51[3] = 1, the V-Port is enabled. (Before this bit is set to 1, Extension register bits CR50[2:0] must be set to '001'.) |
| O | Pin functions as an output. |
| O-OD | Pin functions as an output, and the output is open-drain. |
| O-TS | Pin functions as an output, and the output is tristate.<br>The output state depends on the voltage level on the pin. When the pin receives:<br>• A voltage of 0 V, it functions as a low.<br>• A voltage of 5 V, it functions as a high.<br>• A voltage of more than 5 V, it functions as a high-impedance. |
| SR | Pin function is slow refresh.<br>With slow refresh, only the display memory DRAM is being refreshed.<br>Also, CAS# and RAS# pads output CAS#-before-RAS# refresh cycles once every 30 µsec. |
| S-TS | Pin functions as a sustained tristate.<br>As defined by the PCI bus specification, a sustained tristate pin is:<br><br>An active-low tristate signal that is driven by one and only one agent at a time.<br>• The agent that drives a S-TS pin low must drive it high for at least one clock before letting it float.<br>• A new agent cannot start driving a S-TS signal any sooner than one clock after the previous agent tristates it.<br>• A pull-up is required to sustain the inactive state until another agent drives it, and the pull-up must be provided by the central resource. |
| X | Inputs to the pin are a 'don't care', as the pin signal is forced to a logical high internally. |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 1 | B1 | No connect | No Connection. (Standby and Suspend mode states do not apply.) | | | | NA |
| 2 | B2 | No connect | No Connection. (Standby and Suspend mode states do not apply.) | | | | NA |
| 3 | C1 | MD18 | I/O | A | I(A) | I(A) | I |
| | | ROMA10 | O | NA | NA | NA | NA |
| 4 | C2 | MD17 | I/O | A | I(A) | I(A) | I |
| | | ROMA9 | O | NA | NA | NA | NA |
| 5 | C3 | MD16 | I/O | A | I(A) | I(A) | I |
| | | ROMA8 | O | NA | NA | NA | NA |
| 6 | D3 | MD15 | I/O | A | I(A) | I(A) | I |
| | | ROMA7 | O | NA | NA | NA | NA |
| 7 | D1 | MD14 | I/O | A | I(A) | I(A) | I |
| | | ROMA6 | O | NA | NA | NA | NA |
| 8 | D2 | MVDD1 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 9 | E3 | MD13 | I/O | A | I(A) | I(A) | I |
| | | ROMA5 | O | NA | NA | NA | NA |
| 10 | E2 | MD12 | I/O | A | I(A) | I(A) | I |
| | | ROMA4 | O | NA | NA | NA | NA |
| 11 | E1 | MD11 | I/O | A | I(A) | I(A) | I |
| | | ROMA3 | O | NA | NA | NA | NA |
| 12 | E4 | MD10 | I/O | A | I(A) | I(A) | I |
| | | ROMA2 | O | NA | NA | NA | NA |
| 13 | F3 | MD9 | I/O | A | I(A) | I(A) | I |
| | | ROMA1 | O | NA | NA | NA | NA |
| 14 | F2 | MD8 | I/O | A | I(A) | I(A) | I |
| | | ROMA0 | O | NA | NA | NA | NA |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 15 | F1 | WE1# | O | A | H | H | H |
| | | CAS1# (See note 1 on page 5.) | O | A | SR | SR | H |
| 16 | F4 | WE0# | O | A | H | H | H |
| | | CAS0# (See note 1 on page 5.) | O | A | SR | SR | H |
| 17 | G3 | MD7 | I/O | A | I(A) | I(A) | I |
| | | ROMD7 | I | NA | NA | NA | NA |
| 18 | G2 | MD6 | I/O | A | I(A) | I(A) | I |
| | | ROMD5 | I | NA | NA | NA | NA |
| 19 | G1 | MD5 | I/O | A | I(A) | I(A) | I |
| | | ROMD5 | I | NA | NA | NA | NA |
| 20 | G4 | MD4 | I/O | A | I(A) | I(A) | I |
| | | ROMD4 | I | NA | NA | NA | NA |
| 21 | H3 | MD3 | I/O | A | I(A) | I(A) | I |
| | | ROMD3 | I | NA | NA | NA | NA |
| 22 | H2 | MD2 | I/O | A | I(A) | I(A) | I |
| | | ROMD2 | I | NA | NA | NA | NA |
| 23 | H1 | MD1 | I/O | A | I(A) | I(A) | I |
| | | ROMD1 | I | NA | NA | NA | NA |
| 24 | H4 | MD0 | I/O | A | I(A) | I(A) | I |
| | | ROMD0 | I | NA | NA | NA | NA |
| 25 | J3 | VSS1 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 26 | J2 | AD31 | I/O | A | I | A | I |
| 27 | J1 | AD30 | I/O | A | I | A | I |
| 28 | J4 | AD29 | I/O | A | I | A | I |
| 29 | K3 | AD28 | I/O | A | I | A | I |
| 30 | K2 | AD27 | I/O | A | I | A | I |
| 31 | K1 | AD26 | I/O | A | I | A | I |
| 32 | K4 | AD25 | I/O | A | I | A | I |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 33 | L3 | AD24 | I/O | A | I | A | I |
| 34 | L2 | AD23 | I/O | A | I | A | I |
| 35 | L1 | AD22 | I/O | A | I | A | I |
| 36 | L4 | BVDD2 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 37 | M3 | AD21 | I/O | A | I | A | I |
| 38 | M2 | AD20 | I/O | A | I | A | I |
| 39 | M1 | AD19 | I/O | A | I | A | I |
| 40 | M4 | AD18 | I/O | A | I | A | I |
| 41 | N3 | AD17 | I/O | A | I | A | I |
| 42 | N2 | AD16 | I/O | A | I | A | I |
| 43 | N1 | INTR# | O-TS | A | TS | A | TS |
| 44 | N4 | CVDD1 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 45 | P3 | STOP# | S-TS | A | TS | A | TS |
| 46 | P2 | PAR | I/O | A | TS | A | NA |
| 47 | P1 | DEVESEL# | S-TS | A | TS | A | TS |
| 48 | P4 | TRDY# | S-TS | A | TS | A | TS |
| 49 | R3 | VSS2 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 50 | R2 | CLK | I | A | X | A | I |
| 51 | R1 | IRDY# | I | A | X | A | I |
| 52 | R4 | FRAME# | I | A | X | A | I |
| 53 | T3 | IDSEL | I | A | X | A | I |
| 54 | T2 | OSC (See note 2 on page 5.) | I | A | For Suspend mode, pad is 'don't care' if external 32-kHz clock is used. | | I |
| | | XVCLK | I | A | For Suspend mode, pad is 'don't care' if external 32-kHz clock is used. | | NA |
| 55 | T1 | RST# | I | A | A | A | I |
| 56 | T4 | SUSPI | I | A | A | A | NA |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 57 | U3 | CLK32K | I | A | A | A | A |
| | | SUSPT# | O | A | A | A | NA |
| 58 | U2 | C/BE3# | I | A | X | A | I |
| 59 | U1 | C/BE2# | I | A | X | A | I |
| 60 | U4 | C/BE1# | I | A | X | A | I |
| 61 | V2 | C/BE0# | I | A | X | A | I |
| 62 | V1 | No connect | No Connection. (Standby and Suspend mode states do not apply.) | | | | NA |
| 63 | Y1 | ACT1 | I | A | X | X | I |
| 64 | W1 | VSS3 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 65 | Y2 | No connect | No Connection. (Standby and Suspend mode states do not apply.) | | | | NA |
| 66 | W2 | No connect | No Connection. (Standby and Suspend mode states do not apply.) | | | | NA |
| 67 | Y3 | AD15 | I/O | A | I | A | I |
| 68 | W3 | AD14 | I/O | A | I | A | I |
| 69 | V3 | AD13 | I/O | A | I | A | I |
| 70 | V4 | AD12 | I/O | A | I | A | I |
| 71 | Y4 | AD11 | I/O | A | I | A | I |
| 72 | W4 | AD10 | I/O | A | I | A | I |
| 73 | V5 | AD9 | I/O | A | I | A | I |
| 74 | W5 | AD8 | I/O | A | I | A | I |
| 75 | Y5 | AD7 | I/O | A | I | A | I |
| 76 | U5 | AD6 | I/O | A | I | A | I |
| 77 | V6 | BVDD1 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 78 | W6 | AD5 | I/O | A | I | A | I |
| 79 | Y6 | AD4 | I/O | A | I | A | I |
| 80 | U6 | AD3 | I/O | A | I | A | I |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 81 | V7 | AD2 | I/O | A | I | A | I |
| 82 | W7 | CVDD2 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 83 | Y7 | AD1 | I/O | A | I | A | I |
| 84 | U7 | AD0 | I/O | A | I | A | I |
| 85 | V8 | VSS4 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 86 | W8 | VPC0 (See note 3 on page 5.) | I | A | X | X | X |
| 87 | Y8 | VPC1 (See note 3 on page 5.) | I | A | X | X | X |
| 88 | U8 | VPC2 (See note 3 on page 5.) | I | A | X | X | X |
| 89 | V9 | VPC3 (See note 3 on page 5.) | I | A | X | X | X |
| 90 | W9 | VPC4 (See note 3 on page 5.) | I | A | X | X | X |
| 91 | Y9 | VPC5 (See note 3 on page 5.) | I | A | X | X | X |
| 92 | U9 | VPC6 (See note 3 on page 5.) | I | A | X | X | X |
| 93 | V10 | VPC7 (See note 3 on page 5.) | I | A | X | X | X |
| 94 | W10 | VPY0 (See note 3 on page 5.) | I | A | X | X | X |
| 95 | Y10 | VPY1 (See note 3 on page 5.) | I | A | X | X | X |
| 96 | U10 | VPY2 (See note 3 on page 5.) | I | A | X | X | X |
| 97 | V11 | VPY3 (See note 3 on page 5.) | I | A | X | X | X |
| 98 | W11 | DDCC | O-OD | A | H | H | X |
| | | VCLK0 | O-OD | A | H | H | X |
| 99 | Y11 | VSS5 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 100 | U11 | VPY4 (See note 3 on page 5.) | I | A | X | X | X |
| 101 | V12 | VPY5 (See note 3 on page 5.) | I | A | X | X | X |
| 102 | W12 | VPY6 (See note 3 on page 5.) | I | A | X | X | X |
| 103 | Y12 | VPY7 (See note 3 on page 5.) | I | A | X | X | X |
| 104 | U12 | DDCD | O-OD | A | H | H | X |
| 105 | V13 | VAVDD | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 106 | W13 | HREFI (See note 3 on page 5.) | I | A | X | X | X |
| 107 | Y13 | VAVSS | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 108 | U13 | VACTI (See note 3 on page 5.) | I | A | X | X | X |
| 109 | V14 | DACVDD1 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 110 | W14 | VSI (See note 3 on page 5.) | I | A | X | X | X |
| 111 | Y14 | VPCLKI (See note 3 on page 5.) | I | A | X | X | X |
| 112 | U14 | HSYNC | O | When External/General register MISC[6] is:<br>• 0, HSYNC is active low.<br>• 1, HSYNC is active high. | | | L |
| 113 | V15 | DACVSS1 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 114 | W15 | VSYNC | O | When External/General register MISC[7] is:<br>• 0, VSYNC is active low.<br>• 1, VSYNC is active high. | | | L |
| 115 | Y15 | VREF | Analog pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 116 | U15 | IREF | Analog pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 117 | V16 | CRTVDD | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 118 | W16 | No connect | No Connection. (Standby and Suspend mode states do not apply.) | | | | NA |
| 119 | Y16 | PROG1 | O | When Extension register bit SR2F[6] is:<br>• 0, the voltage level on this pin is high.<br>• 1, the voltage level on this pin is low. | | | L |
| | | TWR# | I | A | A | A | NA |
| 120 | U16 | BLUE | Analog pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 121 | V17 | GREEN | Analog pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 122 | W17 | RED | Analog pin. (Standby and Suspend mode states do not apply.) | | | | NA |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 123 | Y17 | FPVEE | O | L | L | L | L |
| 124 | U17 | FPDECTL | O | L | L | L | L |
| 125 | W18 | FPVCC | O | L | L | L | L |
| 126 | Y18 | No connect | No Connection. (Standby and Suspend mode states do not apply.) | | | | NA |
| 127 | Y20 | PROG0 | O | When Extension register bit SR2F[6] is:<br>• 0, the voltage level on this pin is high.<br>• 1, the voltage level on this pin is low. | | | L |
| 128 | Y19 | VSS6 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 129 | W20 | PROG2 | O | When Extension register bit SR2F[6] is:<br>• 0, the voltage level on this pin is high.<br>• 1, the voltage level on this pin is low. | | | L |
| 130 | W19 | No connect | No Connection. (Standby and Suspend mode states do not apply.) | | | | NA |
| 131 | V20 | FP18 | O | L | L | L | L |
| 132 | V19 | FP19 | O | L | L | L | L |
| 133 | V18 | FP20 | O | L | L | L | L |
| 134 | U18 | DACVDD2 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 135 | U20 | FP21 | O | L | L | L | L |
| 136 | U19 | FP22 | O | L | L | L | L |
| 137 | T18 | FP23 | O | L | L | L | L |
| 138 | T19 | FP24 | O | L | L | L | L |
| 139 | T20 | FP25 | O | L | L | L | L |
| 140 | T17 | FP26 | O | L | L | L | L |
| 141 | R18 | FP27 | O | L | L | L | L |
| 142 | R19 | DACVSS2 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 143 | R20 | FP28 | O | L | L | L | L |
| 144 | R17 | FP29 | O | L | L | L | L |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 145 | P18 | FP30 | O | L | L | L | L |
| 146 | P19 | FP31 | O | L | L | L | L |
| 147 | P20 | FP32 | O | L | L | L | L |
| 148 | P17 | FP33 | O | L | L | L | L |
| 149 | N18 | FP34 | O | L | L | L | L |
| 150 | N19 | FP35 | O | L | L | L | L |
| 151 | N20 | FPVDD2 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 152 | N17 | FPDE | O | L | L | L | L |
| 153 | M18 | LLCLK | O | L | L | L | L |
| 154 | M19 | VSS7 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 155 | M20 | FPVDCLK | O | L | L | L | L |
| 156 | M17 | LFS | O | L | L | L | L |
| 157 | L18 | FP0 | O | L | L | L | L |
| 158 | L19 | FP1 | O | L | L | L | L |
| 159 | L20 | FP2 | O | L | L | L | L |
| 160 | L17 | FP3 | O | L | L | L | L |
| 161 | K18 | FP4 | O | L | L | L | L |
| 162 | K19 | FP5 | O | L | L | L | L |
| 163 | K20 | FP6 | O | L | L | L | L |
| 164 | K17 | FP7 | O | L | L | L | L |
| 165 | J18 | FPVDD1 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 166 | J19 | FP8 | O | L | L | L | L |
| 167 | J20 | FP9 | O | L | L | L | L |
| 168 | J17 | FP10 | O | L | L | L | L |
| 169 | H18 | FP11 | O | L | L | L | L |
| 170 | H19 | FP12 | O | L | L | L | L |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 171 | H20 | VSS8 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 172 | H17 | FP13 | O | L | L | L | L |
| 173 | G18 | FP14 | O | L | L | L | L |
| 174 | G19 | FP15 | O | L | L | L | L |
| 175 | G20 | FP16 | O | L | L | L | L |
| 176 | G17 | FP17 | O | L | L | L | L |
| 177 | F18 | VSS9 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 178 | F19 | MD63 | I/O | A | I(A) | I(A) | I |
| 179 | F20 | MD62 | I/O | A | I(A) | I(A) | I |
| 180 | F17 | MD61 | I/O | A | I(A) | I(A) | I |
| 181 | E18 | MD60 | I/O | A | I(A) | I(A) | I |
| 182 | E19 | MD59 | I/O | A | I(A) | I(A) | I |
| 183 | E20 | MD58 | I/O | A | I(A) | I(A) | I |
| 184 | E17 | MD57 | I/O | A | I(A) | I(A) | I |
| 185 | D18 | MD56 | I/O | A | I(A) | I(A) | I |
| 186 | D19 | MD55 | I/O | A | I(A) | I(A) | I |
| 187 | D20 | MD54 | I/O | A | I(A) | I(A) | I |
| 188 | D17 | WE7# | O | A | H | H | H |
| | | CAS7# (See note 1 on page 5.) | O | A | SR | SR | H |
| 189 | C19 | WE6# | O | A | H | H | H |
| | | CAS6# (See note 1 on page 5.) | O | A | SR | SR | H |
| 190 | C20 | No connect | No Connection. (Standby and Suspend mode states do not apply.) | | | | NA |
| 191 | A20 | No connect | No Connection. (Standby and Suspend mode states do not apply.) | | | | NA |
| 192 | B20 | VSS10 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 193 | A19 | MA9 | O | A | L or H | L or H | L |
| 194 | B19 | RAS1# (See note 1 on page 5.) | O | A | SR | SR | H |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 195 | A18 | MD53 | I/O | A | I(A) | I(A) | I |
| 196 | B18 | MD52 | I/O | A | I(A) | I(A) | I |
| 197 | C18 | MD51 | I/O | A | I(A) | I(A) | I |
| 198 | C17 | MD50 | I/O | A | I(A) | I(A) | I |
| 199 | A17 | MD49 | I/O | A | I(A) | I(A) | I |
| 200 | B17 | MVDD3 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 201 | C16 | MD48 | I/O | A | I(A) | I(A) | I |
| 202 | B16 | MD47 | I/O | A | I(A) | I(A) | I |
| 203 | A16 | MD46 | I/O | A | I(A) | I(A) | I |
| 204 | D16 | MD45 | I/O | A | I(A) | I(A) | I |
| 205 | C15 | MD44 | I/O | A | I(A) | I(A) | I |
| 206 | B15 | MD43 | I/O | A | I(A) | I(A) | I |
| 207 | A15 | WE5# | O | A | H | H | H |
| | | CAS5# (See note 1 on page 5.) | O | A | SR | SR | H |
| 208 | D15 | WE4# | O | A | H | H | H |
| | | CAS4# (See note 1 on page 5.) | O | A | SR | SR | H |
| 209 | C14 | MD42 | I/O | A | I(A) | I(A) | I |
| 210 | B14 | MD41 | I/O | A | I(A) | I(A) | I |
| 211 | A14 | MD40 | I/O | A | I(A) | I(A) | NA |
| | | RIOPU | I | NA | NA | NA | CD |
| 212 | D14 | MD39 | I/O | A | I(A) | I(A) | I |
| 213 | C13 | MD38 | I/O | A | I(A) | I(A) | I |
| 214 | B13 | MD37 | I/O | A | I(A) | I(A) | I |
| 215 | A13 | MD36 | I/O | A | I(A) | I(A) | I |
| 216 | D13 | MD35 | I/O | A | I(A) | I(A) | I |
| 217 | C12 | MD34 | I/O | A | I(A) | I(A) | NA |
| | | MMIOPU | I | NA | NA | NA | CD |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 218 | B12 | MD33 | I/O | A | I(A) | I(A) | NA |
| | | TMPU | I | NA | NA | NA | CD |
| 219 | A12 | MD32 | I/O | A | I(A) | I(A) | I |
| 220 | D12 | VSS11 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 221 | C11 | MA8 | O | A | L or H | L or H | L |
| 222 | B11 | MA7 | O | A | L or H | L or H | L |
| 223 | A11 | MA6 | O | A | L or H | L or H | L |
| 224 | D11 | MA5 | O | A | L or H | L or H | L |
| 225 | C10 | MA4 | O | A | L or H | L or H | L |
| 226 | B10 | CAS# (See note 1 on page 5.) | O | A | SR | SR | H |
| | | WE# | O | A | H | H | H |
| 227 | A10 | MVDD2 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 228 | D10 | RAS0# (See note 1 on page 5.) | O | A | SR | SR | H |
| 229 | C9 | MA3 | O | A | L or H | L or H | L |
| 230 | B9 | MA2 | O | A | L or H | L or H | L |
| 231 | A9 | MA1 | O | A | L or H | L or H | L |
| 232 | D9 | MA0 | O | A | L or H | L or H | L |
| 233 | C8 | VSS12 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 234 | B8 | MD31 | I/O | A | I(A) | I(A) | NA |
| | | BIOSPU | I | NA | NA | NA | CD |
| 235 | A8 | MD30 | I/O | A | I(A) | I(A) | NA |
| | | ROM32KPU | I | NA | NA | NA | CD |
| 236 | D8 | MD29 | I/O | A | I(A) | I(A) | NA |
| | | XCLKPU | I | NA | NA | NA | CD |
| 237 | C7 | MD28 | I/O | TS | I(A) | I(A) | NA |
| | | INTPU | I | NA | NA | NA | CD |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 238 | B7 | MD27 | I/O | A | I(A) | I(A) | NA |
| | | SCANPU | I | NA | NA | NA | CD |
| 239 | A7 | CVDD3 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |
| 240 | D7 | MD26 | I/O | A | I(A) | I(A) | I |
| 241 | C6 | MD25 | I/O | A | I(A) | I(A) | NA |
| | | SW2PU | Pull-up resistor. (Standby and Suspend mode states do not apply.) | | | | CD |
| 242 | B6 | MD24 | I/O | A | I(A) | I(A) | NA |
| | | SW1PU | Pull-up resistor. (Standby and Suspend mode states do not apply.) | | | | CD |
| 243 | A6 | WE3# | O | A | H | H | H |
| | | CAS3# (See note 1 on page 5.) | O | A | SR | SR | H |
| 244 | D6 | WE2# | O | A | H | H | H |
| | | CAS2# (See note 1 on page 5.) | O | A | SR | SR | H |
| 245 | C5 | MD23 | I/O | A | I(A) | I(A) | I |
| | | ROMA15 | O | NA | NA | NA | NA |
| 246 | B5 | MD22 | I/O | A | I(A) | I(A) | I |
| | | ROMA14 | O | NA | NA | NA | NA |
| 247 | A5 | MD21 | I/O | A | I(A) | I(A) | I |
| | | ROMA13 | O | NA | NA | NA | NA |
| 248 | D5 | MD20 | I/O | A | I(A) | I(A) | I |
| | | ROMA12 | O | NA | NA | NA | NA |
| 249 | C4 | MD19 | I/O | A | I(A) | I(A) | I |
| | | ROMA11 | O | NA | NA | NA | NA |
| 250 | B4 | MAVDD | Power/ground pin (Standby and Suspend mode states do not apply.) | | | | NA |
| 251 | A4 | MCLK | I/O | A | TS | H | NA |
| | | XMCLK | I | A | A | A | NA |
| | | SWO | I | A | A | A | NA |

**Table 2–2. CL-GD7555 Pad Control Signals, under Corresponding Mode Conditions**

| Plastic Quad Flat Pack Pin No. / Plastic Ball Grid Array Ball Position / Pin Name / Pin Function | | | | Standby Modes | Suspend Mode | | State of Pin During Reset Operation |
|---|---|---|---|---|---|---|---|
| PQFP Pin No. | PBGA Ball Position | Pin Name | In/ Out | Software-Controlled | Hardware-Controlled | Software-Controlled | |
| 252 | D4 | MAVSS | Power/ground pin (Standby and Suspend mode states do not apply.) | | | | NA |
| 253 | B3 | EPROM# | O | NA | NA | NA | NA |
| 254 | A3 | No connect | No connection. (Standby and Suspend mode states do not apply.) | | | | NA |
| 255 | A1 | OE# | O | A | H | H | H |
| 256 | A2 | VSS13 | Power/ground pin. (Standby and Suspend mode states do not apply.) | | | | NA |

CIRRUS LOGIC®

# CL-GD7555

*Advance Application Note — 7555-AN-9, v1.0*

# Designing with Display Data Channel DDC2B

***for the CL-GD7555 LCD/CRT Controller***

**Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application note presents information on designing with Display Data Channel DDC2, (level 2B) for the PCI bus that is used with the CL-GD7555 LCD/CRT controller.

**Applicability**

This document applies to the following products:

✔ CL-GD7555

**Related Documents**

– *CL-GD7555 Reference Manuals*



***Version 1.0***

***June 19, 1996***

# 1. Introduction

This application note discusses how Cirrus Logic recommends that its CL-GD7555 chips be configured to support the VESA (Video Electronics Standards Association) DDC2B (Display Data Channel, level 2B) specification. This specification defines a serial communication channel between a computer display device and a host CPU system. Based on the $I^2C$ protocol, the DDC2B channel uses two signals: one is for a clock signal and the other is for data.

The DDC2B channel can be used to carry both configuration information for optimum use of the display device and additional control information for the display device. This same DDC2B serial communication channel can be used to program video decoder devices such as the CL-PX4072 NTSC/PAL decoder.

# 2. DDC2B Board Designs

This section discusses how to design a board to support DDC2B. The CL-GD7555 pins that are used to carry signals for DDC2B are DDCC pin (pin 98) and DDCD pin (pin 104). When Extension register bit SR23[4] is programmed to 0:

- The DDCC pin either drives a clock signal to pin 15 of the 15-pin VGA connector, or it receives a clock signal from pin 15.
- The DDCD pin drives a data signal to pin 12 of the VGA connector, or it receives a data signal from pin 12.

## 2.1 Board Design 1: Supporting DDC2B Only

Both the DDCC and DDCD pins are open-drain outputs and require a pull-up resistor to support DDC2B. On the Cirrus Logic PCI Bus Demonstration Board, each pin is pulled up to the CRTVDD power pin with a 6.8-kΩ resistor.

Extension register SR8 is used to control and monitor the status of these two pins as shown in Table 1.

**Table 1. Extension Register SR8 Bits Used for DDC2B Support**

| Extension Register SR8 Bits | Usage |
|---|---|
| 7 | DDCD status |
| 2 | DDCC status |
| 1 | DDCD output control |
| 0 | DDCC output control |

## 2.2 Board Design 2: Supporting DDC2B and Video Decoders with I²C Interface

In addition to supporting DDC2B, the DDCC pins and DDCD pins can be used to program video decoder devices that support the I²C interface.

For example, the DCC Level 2B logic can be used to relay commands from the host CPU to I²C devices, such as the Cirrus Logic CL-PX4072 multi-standard NTSC/PAL TV decoder.

However, some CRT monitors do not implement DDC2B correctly. When those CRT monitors are connected, the serial communication from the CL-GD7555 to the video decoder device can have interference. To avoid such interference, use an analog multiplexer to isolate the channel between the CL-GD7555 and the video decoder device from the channel between the CL-GD7555 and the CRT monitor.

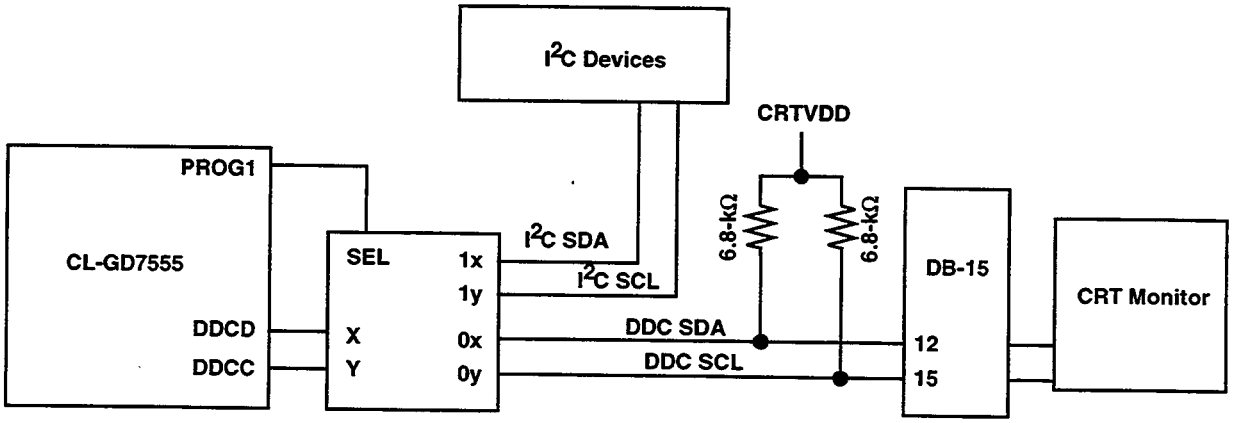



**Figure 1. Implementing DDC2B to Avoid Interference Between Channels**

# 3. BIOS Support

The CL-GD7555 VGA BIOS supports the DDC2B specification. Two extended function calls are supported: One is to inquire the capability of the monitor and the other to read the Extended Display Identification (EDID). Refer to "The CL-GD VGA BIOS External Function Specification" for more detail.

# V-Port™ Implementation

***for the CL-GD7555 LCD/CRT Controller***

**Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application note presents information on video control and data connections to the CL-GD7555 LCD/CRT controller.

**Applicability**

This document is intended to be used in conjunction with applicable CL-GD7555 documentation to aid the system designer.

This document applies to the following products:

✔ CL-GD7555

**Related Documents**

– *CL-GD7555 Reference Manuals*

# Table of Contents

# 1. Introduction

This application note details the operation of the V-Port feature of the Cirrus Logic CL-GD7555 controller. The V-Port is a subset of the ZV-Port standard, in that V-Port handles only video data (and not audio data), while the ZV-Port standard handles both video and audio.

**NOTE:** Since May, 1995, ZV-Port standardization is endorsed by the PCMCIA (Personal Computer Memory Card Industry Association) and its Japanese counterpart, JEIDA (Japanese Electronics Industry Development Association).

This application note describes several implementations of the V-Port including:

- A direct connection of the CL-GD7555 V-Port to an on-board video decoder that provides either live or playback video from a video source. (Refer to Section 3.3.)
- A CL-GD7555 motherboard implementation that is compatible with the ZV-Port standard and that uses the CL-GD7555 V-Port with the Cirrus Logic CL-GD6729 Host Adapter chip. In this implementation, the V-Port is connected to the PC Card bus between the CL-GD6729 and the PC Card socket. (Refer to Section 4.1.)
- A combination of the above connections, in which the V-Port is connected to both an on-board video source as well as to a PC Card bus. (Refer to Section 4.2.)

# 2. V-Port Requirements

This section outlines requirements for using the CL-GD7555 V-Port feature.

## 2.1 Requirement 1: 16-bits/pixel Video Data Color Space Format

The incoming video data to the CL-GD7555 V-Port must be in one of the following 16-bits/pixel color space formats:

- 4:2:2 YUV, equivalent to 16M-color RGB quality
- RGB 5-5-5, displaying 32K colors

## 2.2 Requirement 2: HREFI Pin Connection

The CL-GD7555 VACTI signal is a signal that indicates that video data are valid. However, the ZV-Port standard does not specify the CL-GD7555 VACTI signal. As a result, when the CL-GD7555 is used on a motherboard that is to be ZV-Port compatible, the CL-GD7555 HREFI pin and VACTI pin must be connected.

To use the downscaling feature of the CL-GD7555 V-Port, HREFI and VACTI must be the same polarity, which is active high.

## 2.3 Requirement 3: Use of 5-V CRTVDD

Power to the CL-GD7555 V-Port pads are supplied from FPVDD[2:1] (Flat Panel VDD) and BVDD[2:1] (Bus VDD). To set FPVDD and BVDD to either 3.3 V or 5 V, regardless of the voltage of the incoming video data signal, CRTVDD must be set to 5 V.

When the power supply to the V-Port is set to 3.3 V, and the incoming video signal is 5 V, damage to the V-Port pads can occur. By setting CRTVDD to 5 V, the CL-GD7555 V-Port pads become 5-V tolerant, even when either FPVDD[2:1], or BVDD[2:1], or both are 3.3 V.

# 3. V-Port Operation

During the V-Port operation, video data are transferred directly from the V-Port to the MotionVideo Memory area in the display memory for storage. Video data coming in through the V-Port can be accepted at the video source rate, which is approximately 13.5 MHz. The data are then either stored directly in the display memory or stored in a compressed form in the display memory. As a result, the data can be simultaneously read out of the display memory and displayed at the VCLK display clock rate, with real-time decompression (as required). This decoupling of the video storage and video playback clock rates allows more flexible design options.

The V-Port allows a total video/graphics solution that can be quite cost-effective since it eliminates the need for an external video windowing controller and an external video frame buffer. Instead, video data can be directly fed into either an 8-bit or a 16-bit V-Port from an external video source. In addition, the V-Port can be configured to interface with various external devices in various modes, as described in the sections that follow.

Examples of V-Port video data input sources include the following, both of which provide 16-bit data in a color space format:

- An MPEG decoder
- An NTSC/PAL decoder

The V-Port data path contains:

- A YUV-to-RGB converter that, at display time, converts data that is compatible with the CCIR 601 YUV specification to the RGB 8-8-8 format.
- An optional color space format converter that, at display time, converts data that is in a format compatible with the CCIR 601 YUV specification to AccuPak, a proprietary 2x compressed format from Cirrus Logic. After converting the data, the CL-GD7548 stores the data in display memory, then sends the data to the MotionVideo Data path, and at display time decompresses the AccuPak-format data for subsequent display.

## 3.1 V-Port Width

The 16-bit-wide V-Port interface was designed to use minimal external logic when interfacing to other NTSC/PAL decoders or MPEG decoders. The CL-GD7555 V-Port can accept data in several different formats (such as interlaced, non-interlaced, and so forth).

## 3.2 V-Port Signal Definitions

This section describes the V-Port signal definitions, which are compatible with the proposed ZV-Port standard interface. The ZV-Port has the following signals:

### *V-Port™ Video Data Input: Signal Definitions*

- VPCLKI (V-Port clock input)
  - — This signal is used to clock valid pixel data into the CL-GD7555. The data transfer rate varies according to the type of data format that is used by the external video decoder.
  - — One VPCLKI is generated for each 16-bit pixel, whether the video data is scaled or not, during both display time and non-display time. VPCLKI is active during the entire vertical refresh interval.
  - — VPCLKI is free-running at up to 20.25 MHz. The trailing edge of VPCLKI is used to clock the data into the CL-GD7555. The VACTI input, which comes from an external decoder such as the CL-PX4072, is forced high when data is available on the V-Port data bus. This VACTI input indicates that data being transferred through the V-Port is valid.
- VSI (vertical sync input)
  - — The CL-GD7555 V-Port vertical control circuitry has programmable registers that use the trailing edge of the VSI signal as a reference for the start offset. (The start offset is a signal that delays the start of the signal delineating the width for a video window.)
  - — The 9-bit field in Extension register bits CR57[7:0] and CR58[5] controls the number of scanlines to be captured.
- HREFI (horizontal reference input)
  - — Horizontally, no programming is required for the CL-GD7555, as each falling edge of VPCLKI corresponds to valid data for one pixel.
- VACTI (video active input)
  - — VACTI enables valid data from the CL-PX4072.
  - — VACTI goes high when pixel data is valid on the Y and UV lines and goes low when the data is invalid.
  - — VACTI allows the VPCLKI signal to be free running. When the CL-GD7555 is configured for a 16-bit-wide V-Port, the leading edge of VACTI is synchronized with the trailing edge of VPCLKI to capture valid data.
  - — When the CL-GD7555 is configured for a V-Port that is 8 bits wide and double-edge clocking is selected, only 8 bits of data are used. In this case, VACTI must bracket both VPCLKI edges. The CL-PX4072 can use the VACTI and VPCLKI signals to scale down the data from the video source.
- VPY[7:0] (luminance data)
  - — These signals are 8 bits of luminance data from the external video controller.
  - — When the CL-GD7555 is configured for a V-Port that is 8 bits wide and double-edge clocking is selected, both luminance and chrominance data are routed to these pins, and VPC is not used.
- VPC[7:0] (chrominance data)
  - — These signals are 8 bits of chrominance data from the external video controller.
  - — There is a 9-bit programmable delay to skip 'n' number of HREFI pulses, before the internal V-Port Vertical Display Enable signal is asserted.

## 3.3 V-Port Implementation

In implementing the V-Port, communication between the CL-GD7555 and an external decoder device is based upon a synchronous data flow, in that the external decoder device drives all the V-Port interfaces, including the VPCLKI.

The V-Port can be implemented in one of two different V-Port modes, depending on how data are latched relative to the clock edge as follows:

- V-Port Mode 1: Data are latched on the VPCLKI falling edge
- V-Port Mode 2: Data are latched on the VPCLKI rising edge

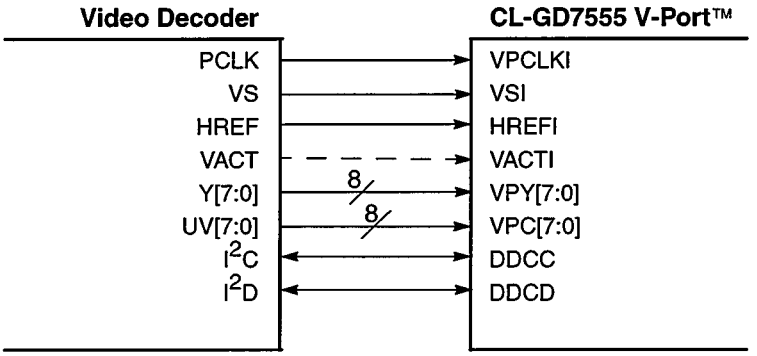
In either V-Port mode 1 or 2, the CL-GD7555 can support both interlaced and non-interlaced video data streams. This flexibility allows the CL-GD7555 to directly interface with various TV/MPEG decoder chips.

The CL-GD7555 also has a serial interface consisting of two pins: a clock pin and a data pin, both of which are open-drain and which support serial programming interfaces to the TV/MPEG decoder chips.

### 3.3.1 V-Port Mode 1: Data Latched on VPCLKI Falling Edge

In V-Port-to-Memory Mode 1, video data are latched on the VPCLKI trailing edge (that is, the falling edge). An example of an implementation of this mode is the interface to the CL-PX4072, as shown in Figure 1. Full implementation of the V-Port-to-Memory Mode 1 interface requires the following 20 active pins:

- VPCLKI (V-Port clock input signal). With this mode, the high-to-low transition of VPCLKI latches the data bits.
- VSI (vertical sync input signal)
- HREFI (horizontal reference input signal)
- VACTI (video active signal, used to indicate the transfer of active video data)
- 16 data bits (8 data bits of Y-luminance on VPY[7:0] and 8 data bits of UV-chrominance on VPC[7:0])




**NOTE:** The DDCC and DDCD pins are not required for the V-Port. However, when the CL-GD7555 is used in certain motherboard implementations, the DDCC and DDCD pins output signals are used to program a NTSC/PAL TV decoder (such as the CL-PX4072 or the Philips® SAA7110).

**Figure 1. V-Port™-to-Memory Mode 1 Interface Signals**

The CL-PX4072 provides only interlaced video data streams that support the following analog video data standards: NTSC, PAL, SECAM, and S-VHS.

### 3.3.2 V-Port Mode 2: Data Latched on VPCLKI Rising Edge

In V-Port-to-Memory Mode 2, video data are latched on the VPCLKI leading edge (that is, the rising edge). In contrast to V-Port-to-Memory Mode 1, V-Port-to-Memory Mode 2 does not require the additional VACTI signal in the interface. Full implementation of the V-Port-to-Memory Mode 2 interface requires only the following 19 active pins:

- VPCLKI (V-Port clock input signal). With this mode, the low-to-high transition of VPCLKI latches the data bits.
- VSI (vertical sync input signal)
- HREFI (horizontal reference input signal)
- 16 data bits (8 data bits for luminance and 8 data bits for chrominance)

In V-Port-to-Memory Mode 2, the CL-GD7555 can support both interlaced and non-interlaced video data streams.

- The interlaced video data stream supports a direct connection with decoder chips, such as the Philips® SAA7110 or the CL-PX4072.
- The non-interlaced video data stream supports a direct connection with MPEG decoder chips, such as the C-CUBE CL-480. In this type of operation, the relationship of the VSI signal to the HREFI signal is 'non-interlaced' and the frame buffer addresses for the video data are generated sequentially.

### 3.3.3 V-Port Pinouts

Table 1 gives the CL-GD7555 pins required to implement a 16-bit V-Port.

**Table 1. Pinout for 16-Bit V-Port**

| CL-GD7555 Pin Number | CL-GD7555 Pin Description |
|---|---|
| 106 | HREFI - Horizontal Reference Input |
| 110 | VSI - Vertical Sync Input |
| 108 | VACTI - Video Data Active Input |
| 111 | VPCLKI - Video Port Clock Input |
| 93:86 | VPC[7:0] - Video Port Pixel Data (Used for UV[7:0]) |
| 103:100 | VPY[7:4], VPY[3:0] - Video Port Pixel Data (Used for Y[7:0]) |
| 98 | DDCC - Display Data Channel Clock |
| 104 | DDCD - Display Data Channel Data |

To configure the CL-GD7555 for the V-Port operation:

- Extension register CR50 must be programmed to configure the V-Port for the various V-Port modes of operations. (The data latch at either the falling edge or the rising edge of the VPCLKI, interlaced or non-interlaced.)
- Extension register bit CR51[3] (the V-Port Enable bit) must be set to 1 to start the V-Port operation.

**NOTES:**

1) To support the serial programming interface to an external decoder chip, a pull-up resistor of about 1 kΩ must be connected to DDCC and DDCD pins (pins 98 and 104).
2) If the V-Port feature is not used in a motherboard design, the V-Port pins above can be left open or floating except for DDCC/DDCD pins. It is generally recommended, however, that the unused input pins be either pulled up or pulled down.

## 3.4 V-Port Timing Diagrams

For timing diagrams of the V-Port interface, refer to the CL-GD7555 Hardware Reference Manual.

## 4. PC Card Multimedia Implementation Using V-Port

The V-Port can be used in conjunction with a Host Adapter PC Card Controller to implement a V-Port on a system. V-Port data consists of both audio and video information that is generated by circuitry on a PC Card. The data are transmitted to subsystems within the host system through some of the PC Card bus address lines that are given in Table 2.

**Table 2. Pinouts for the PC Card V-Port Mode**

| CL-GD7555 | | PC Card | | |
|---|---|---|---|---|
| **CL-GD7555 Relevant Pin Names** | **CL-GD7555 Pin Number** | **PC Card Pin Name** | **PC Card Pin Number** | **PC Card Multimedia Mode Signal Definition** |
| VPCLKI | 111 | IOIS16 | 33 | Pixel Clock |
| HREFI | 106 | A10 | 8 | Horizontal Sync |
| VSI | 110 | A11 | 10 | Vertical Sync |
| VPY[0] | 94 | A9 | 11 | Y0 |
| VPY[1] | 95 | A17 | 46 | Y1 |
| VPY[2] | 96 | A8 | 12 | Y2 |
| VPY[3] | 97 | A18 | 47 | Y3 |
| VPY[4] | 100 | A13 | 13 | Y4 |
| VPY[5] | 101 | A19 | 48 | Y5 |
| VPY[6] | 102 | A14 | 14 | Y6 |
| VPY[7] | 103 | A20 | 49 | Y7 |
| VPC[0] | 86 | A21 | 50 | UV0 |
| VPC[1] | 87 | A22 | 53 | UV1 |
| VPC[2] | 88 | A16 | 19 | UV2 |
| VPC[3] | 89 | A23 | 54 | UV3 |
| VPC[4] | 90 | A15 | 20 | UV4 |
| VPC[5] | 91 | A24 | 55 | UV5 |
| VPC[6] | 92 | A12 | 21 | UV6 |
| VPC[7] | 93 | A25 | 56 | UV7 |
| – | – | A7 | 22 | SCLK |
| – | – | A6 | 23 | MCLK |
| – | – | INPACK | 60 | LRCLK |
| – | – | SPKR | 62 | SDATA |
| – | – | A[3:0] | 26–29 | Address |
| – | – | A[5:4] | 24–25 | Reserved |

**NOTE:** In the PC Card Multimedia mode, only digital video and audio signals are processed.

There are the two implementation modes of the V-Port, the Bypass mode and the Pass-through mode. This application note addresses only the video part of the V-Port Bypass mode.

## 4.1 ByPass Mode (Video Only)

In combination with the CL-GD7555 V-Port, a video data decoder device can be implemented on a 68-pin PC Card. The pins of the Host Adapter PC Card Controller are mostly address pins. These address pins are used for transmitting video data that is tristated in a ZV-Port mode of operation in order to avoid signal contention. As a result, instead of video data having to go through a host CPU bus, the PC Card feeds the video data directly into the V-Port.

When a video decoder card is inserted into a PC Card slot, it is initialized the same way as the PC Card standard specifies. After the host system Card Services software recognizes and notes the ZV-Port feature of the inserted PC Card, the Card Services software allows a client application program to configure the PC Card using the Card Services API (applications programming interface).

In the sample implementation shown in Figure 2, the CL-GD6729 enters into a multimedia mode by tristating address pins A[25:4] of the PC Card bus when the CL-GD6729 Multimedia Mode bit (that is, bit 0 of I/O port address 0x3E0, Index 16) is set. (During the normal PC Card operation, address pins A[25:4] are outputs from a host CPU adapter.) The tristating action by the CL-GD6729 avoids the contention between address signals and video signals and allows the A[25:4] signal lines to carry video data and video capture timing control signals directly to the CL-GD7555 V-Port.

When the PC Card Multimedia Mode is used, the ZV-Port pins must be connected to the CL-GD7555 V-Port and the audio subsystem as shown in Table 2. When the V-Port is disabled or powered down, this connection between the CL-GD7555 and PC Card bus does not interfere with the normal (or non-multimedia) PC Card Bus operations. If needed, a bus switch or a buffer that is turned off during normal PC Card Bus operation can reduce the loading of the PC Card Bus to provide enough drive current capability.

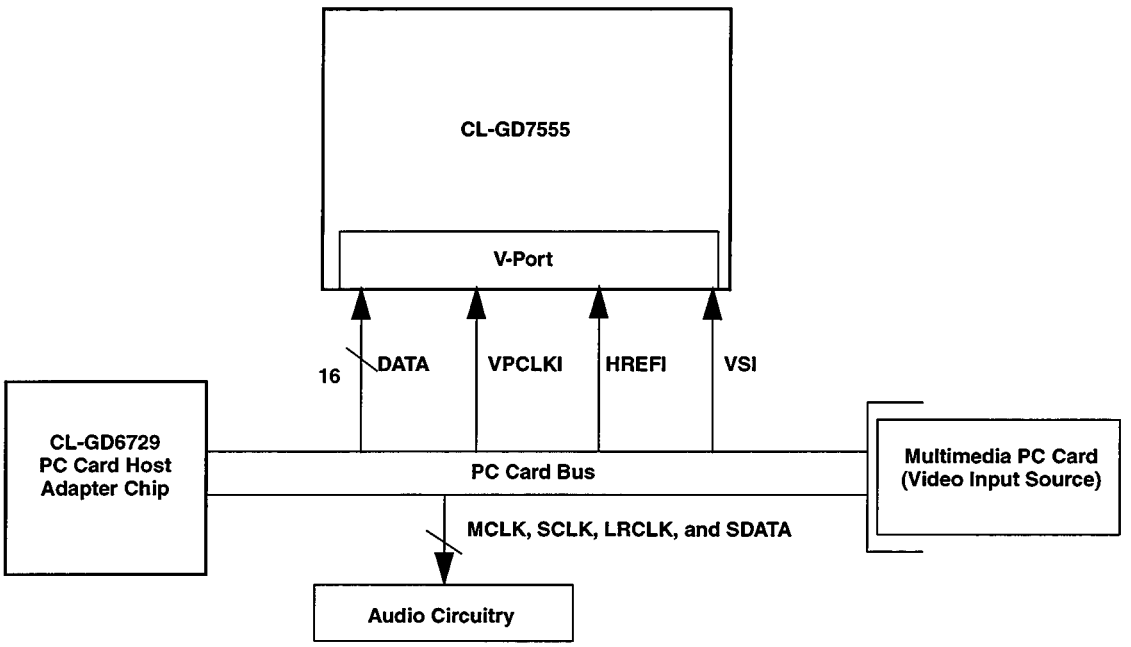



**Figure 2. Video Data Path for PC Card Multimedia Implementation (Bypass Mode)**

## 4.2 Using More than One PC Card that Is Compliant with the ZV-Port Standard

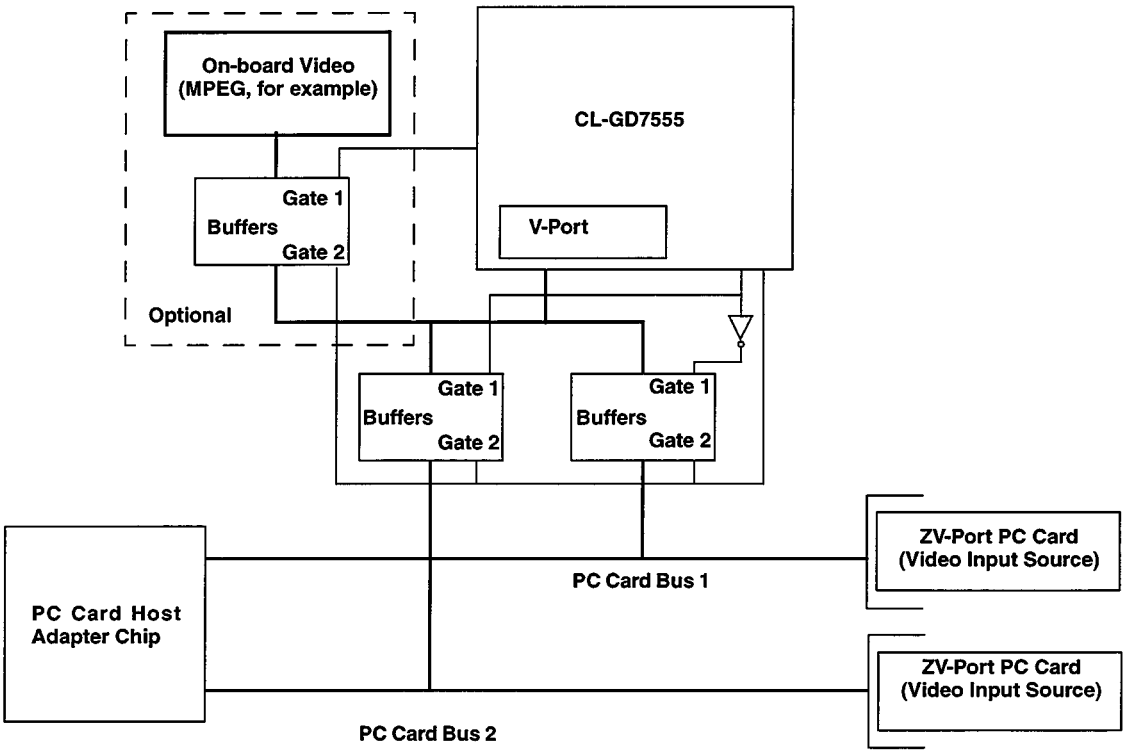
More than one PC Card that is compliant with the ZV-Port standard can be inserted into PC Card sockets simultaneously. To allow this insertion of multiple ZV-Port PC Cards, individual PC Card buses must be isolated from each other by the use of buffers or a multiplexer in the system. Figure 3 shows a block diagram of a full implementation of the ZV-Port.

The control signals to the external buffers in Figure 3 can come from multiple sources as follows:

- CL-GD7555 I/O pins: The PROG[2:0] (pins 129, 119, 127) can be used for the control signals to the external buffers if they are not already being used to implement the dynamic core VDD switching function.
- Motherboard I/O pins: Any available general-purpose I/O pins on the motherboard can also be used for the control signals to the external buffers.

**NOTE:** If video signals from one video source stop while that video source is feeding video data to the CL-GD7555 V-Port, switching to the other video source does not occur because the VSI stops toggling at that point.

As mentioned earlier, there are video decoder chips that use a serial clock and serial data to program the internal registers. These serial signals, however, are not in the ZV-Port standard. Those PC Cards that are compliant with the ZV-Port standard and that have a video decoder chip with this serial interface must have a serial controller that converts the parallel data sent over the PC Card bus to serial data.




**This block diagram shows an implementation in which either PC Card slot can be used. (Audio inputs are not shown.)**

**Figure 3. Full ZV-Port Implementation**

# Layout Guidelines

***for the CL-GD7555 LCD/CRT Controller***

**Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application note presents layout information for the CL-GD7555 LCD/CRT controllers.

**Applicability**

This document is intended to be used in conjunction with applicable CL-GD7555 documentation to aid the system designer.

This document applies to the following products:

✔ CL-GD7555

**Related Documents**

- *CL-GD7555 Hardware Reference Manual*
- *CL-GD7555 Demonstration Board Application Notes*

# Table of Contents

# 1. Introduction

This application note presents layout information for using CL-GD7555 in system designs. The plastic ball-grid array (PBGA) CL-GD7555 package has the following:

- 256 solder ball-type pads around the periphery of the CL-GD7555 (for electrical connection to the mother-board and other system components)
- 16 thermal solder ball pads in the center of the CL-GD7555 (for heat dissipation)

CL-GD7555: View of Bottom (Solder Side)

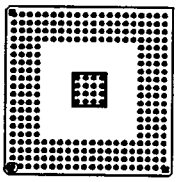


**Figure 1. CL-GD7555 Plastic Ball-Grid Array**

For more information, refer to:

- The CL-GD7555 Reference Manuals
- Schematics in the CL-GD7555 Demonstration Board application notes

## 2. Layout Guidelines for Maximum Thermal Performance

The CL-GD7555 package is rated to dissipate 2.5 W, based on simulations with PCBs (printed circuit boards) that do not have thermal vias. By carefully designing the PCB layout for the motherboard that uses the CL-GD7555, the system can allow for even greater heat dissipation for the CL-GD7555, so that greater than 2.5 W can be dissipated.

When the CL-GD7555 PBGA package is used with a motherboard, the motherboard footprint for the CL-GD7555 must also have:

- 256 solder ball-type landing pads that match the location of 256 pads around the periphery of the CL-GD7555
- 16 thermal solder ball landing pads that match the location of the 16 pads in the center of the CL-GD7555

For maximum heat dissipation for the CL-GD7555 when it is used on a motherboard PCB, refer to Figure 2 and incorporate the following design actions for the CL-GD7555 footprint:

1) ***Place bare copper on both the solder side and the component side of the motherboard PCB.*** It is recommended that on both the solder side and the component side of the motherboard PCB, the following is laid down: an area of bare copper (or equivalent material) that spans an 8-ball by 8-ball area that connects to the solid-filled thermal vias on the motherboard PCB.

2) ***Add an 8 x 8 grid of solid-filled thermal vias.*** To maximize the heat dissipation for the CL-GD7555, on the motherboard PCB, it is recommended that the center of the footprint for the PBGA package have an 8 x 8 grid of solid-copper-filled thermal vias. This 8 x 8 array:

   **a)** Must include connections to the following:

   — The motherboard PCB internal ground plane

   — The copper area on both the solder side and component side of the motherboard PCB

   **b)** Consists of solid-copper-filled thermal vias, with a diameter that is not less than 0.356 mm (0.014 inches).

   **NOTE:** Although the current package for the CL-GD7555 has only a 4 x 4 array of solid-filled thermal vias, using a design that supports up to an 8 x 8 array allows more flexibility in terms of using other PBGA package configurations.

3) ***Maximize the CL-GD7555 connections to ground and power planes.*** To maximize thermal conductance of the CL-GD7555 to both the ground plane and the power plane of the motherboard PCB, the following are recommended:

   **a)** The CL-GD7555 ground and power ball pads must be connected to their respective motherboard PCB planes through solid-filled vias.

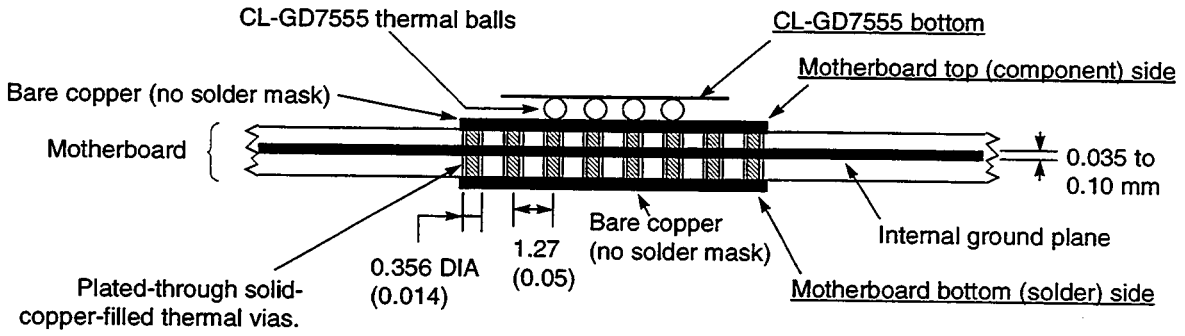
   — Copper filled vias are recommended.

   — The diameter of the solid-filled vias must be no less than 0.356 mm (0.014 inches).

   **b)** The CL-GD7555 thermal ball pads must be placed directly on top of solid-filled vias that tie directly to the motherboard PCB ground plane.

4) ***Optimize the ground plane thickness.*** All CL-GD7555 thermal vias (including both those with and without a thermal solder ball pad) are to be connected to the ground plane of the motherboard PCB. For maximum heat dissipation, it is recommended that the motherboard PCB ground plane be between 0.035 mm to 0.10 mm thick.

**Motherboard PCB: Side View of Footprint for Center of CL-GD7555**




**Motherboard PCB: Top View of Footprint for CL-GD7555**

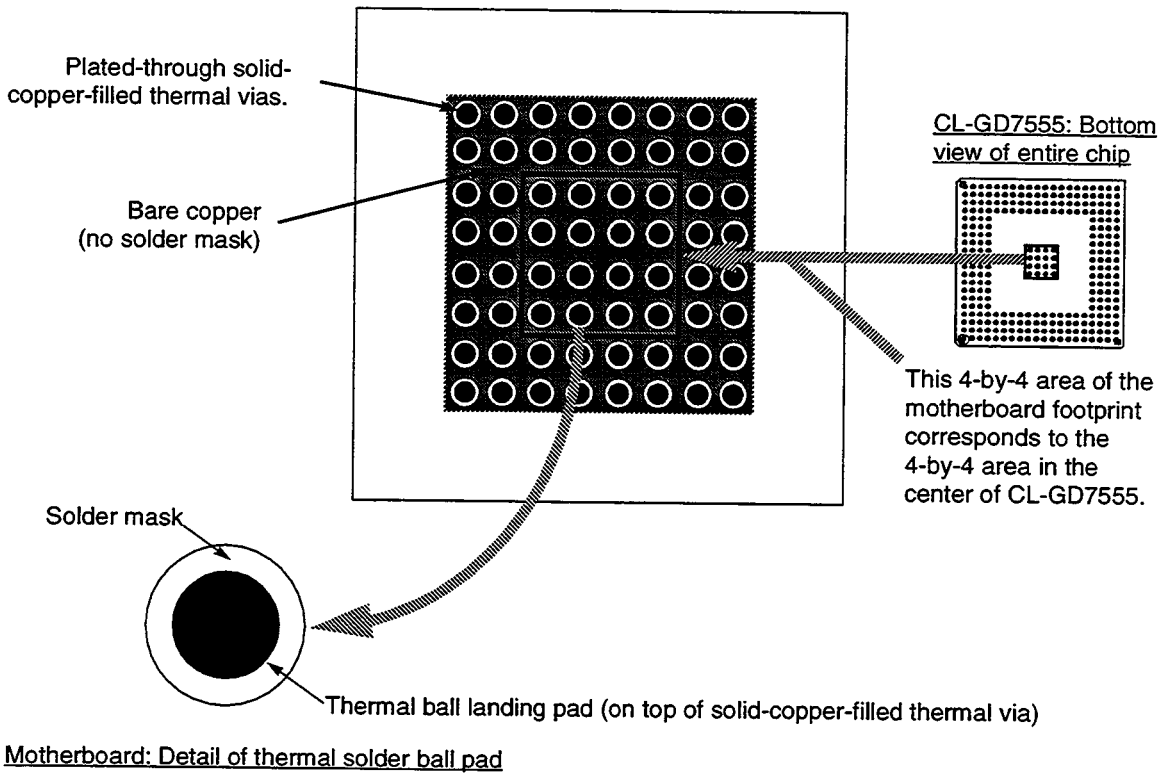



**Figure 2. Side, Top, and Detail Views of the CL-GD7555 Footprint**

## 3. Layout Guidelines for the Power and Ground Planes

Cirrus Logic recommends the use of multi-layer boards for its components, especially for designing high-performance systems. As system frequencies continue to increase, it becomes less likely that one can obtain acceptable results unless two of the layers are reserved: one layer must be dedicated exclusively as a power plane for distribution of power, and one layer must be dedicated exclusively as a ground plane.

As discussed in Section 2.1 and Section 2.2, in laying out the power and ground planes, cuts are made in the planes. As there is a certain amount of art involved in the exact positioning and size of these cuts, some experimentation may be required to obtain satisfactory results.

Cuts in the power plane must take place in the same position as cuts that are made in the ground plane. Isolated ground and power planes must not overlay a noisy digital power or ground plane. If such an overlay occurs, the result can simulate a capacitor, composed of the overlay conductors and separated by the relatively thin dielectric between the two pieces of epoxy that make up a four-layer board. Consequently, noisy buses (such as a data bus or an address bus) must not be allowed to cross any isolated area.

**IMPORTANT:** Designers with prior experience using discrete RAMDACs and clock sources may have found that the guidelines given here have not been necessary, especially for systems running at relatively low frequencies. However, because the CL-GD7555 operates at such high frequencies, the guidelines and precautions given here are necessary.

## 3.1 Layout Guidelines for the Power Plane

When laying out a board that uses the CL-GD7555, one plane on the board must be dedicated to power.

### 3.1.1 Power Plane: Isolating the Core VDD, VCLK VDD, and MCLK VDD Pins

The core VDD (CVDD), VCLK synthesizer VDD (VAVDD), and MCLK synthesizer VDD (MAVDD) power rails are distributed to the CL-GD7555 from the VCC on the board. To isolate CVDD, VAVDD, and MAVDD both from each other and from VCC, refer to Figure 1 and the schematics in the CL-GD7555 Demonstration Board application notes. Make cuts in the power plane and add in-line resistors, using the following guidelines.

- Isolate noise on the VCC rail and provide additional latch-up protection by placing a resistance of 1/2-Ω in series between the board VCC rail and the CL-GD7555 CVDD pins. (The 1/2-Ω series resistance results from two 1-Ω resistors in parallel with each other.) The 1/2-Ω resistance is needed to make up an RC filter for this isolation circuit.
- Isolate the VAVDD part of the power plane with 33-Ω series resistors that serve as RC filter components.
- Isolate the MAVDD part of the power plane with 33-Ω series resistors that serve as RC filter components.

### 3.1.2 Power Plane: Traces for DRAM VDD, Flat Panel VDD, Bus VDD, and CRT VDD Pins

The DRAM VDD (MVDD), the flat panel VDD (FPVDD), Bus VDD (BVDD), and CRT VDD (CRTVDD) pins provide power to those pads that interface to signals from the rest of the system. Traces for the MVDD, FPVDD, BVDD, and CRTVDD pins, which connect a +3.3-V or +5.0-V power supply to signals from the rest of the system, must be as thick and as short as possible.

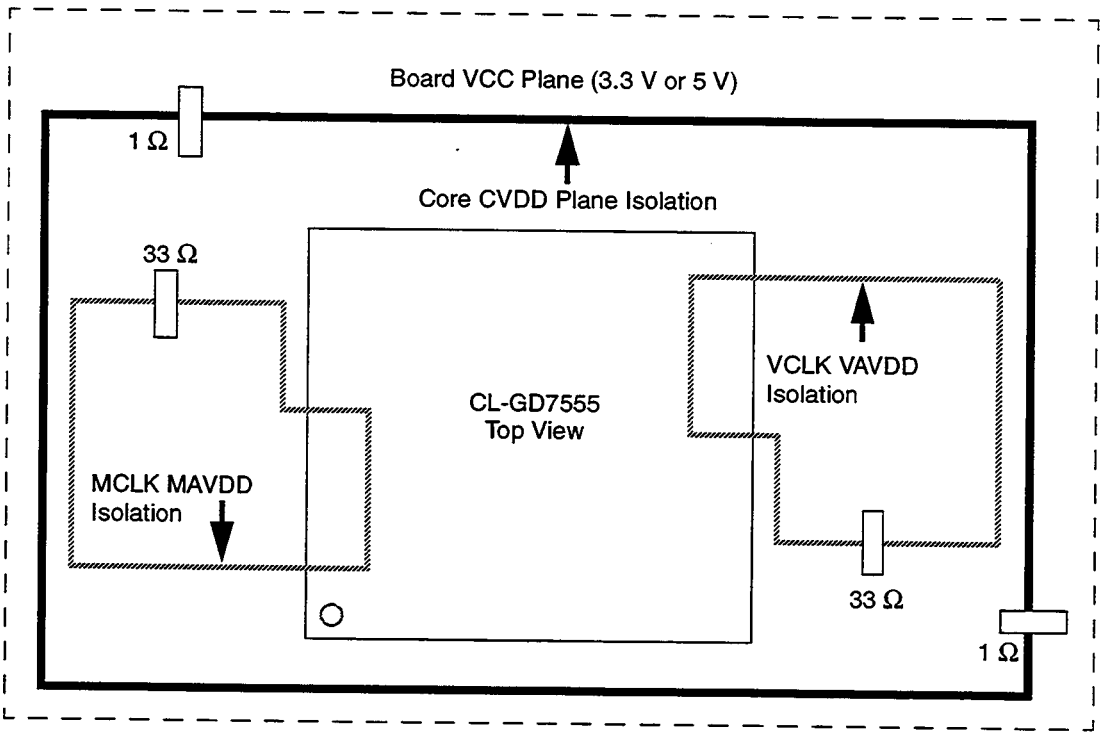



**Figure 1. Example: Isolating the Power Plane for PQFP**

### 3.1.3 Power Plane: Decoupling Capacitors

The CL-GD7555 operates at high frequencies. (In some cases, such as the 60-Hz mode for a 1280 x 1024 resolution, the VCLK operates at 108 MHz.) As a result, adequate power decoupling is absolutely crucial to a successful layout design.

Each CL-GD7555 power pin must have a 0.1-µF decoupling capacitor returned to the local ground.

- These capacitors must be placed as close to the respective power pins as possible.
- In addition, these capacitors must have excellent high-frequency characteristics. (Cirrus Logic has found the surface-mount ceramic-chip capacitors perform adequately.)

For the MAVDD and VAVDD power pins, the high-frequency decoupling capacitors:

- Must be as close to the power pin as possible
- Must be connected to the appropriate isolated-power-grid area
- Must be returned to the appropriate local ground

The board design must include bulk bypassing capacitors, such as tantalum capacitors. The high-frequency characteristics of bypass capacitors are not as critical as that of the decoupling capacitors.

## 3.2 Layout Guidelines for the Ground Plane

When laying out a board that uses the CL-GD7555, one plane on the board must be dedicated to ground. The ground plane must have cuts that suppress currents between the various areas but do not completely isolate the currents. For a typical design, refer to Figure 2 and the schematics in the CL-GD7555 Demonstration Board application notes. Make cuts in the ground plane, using the following guideline:

- Ground plane cuts must not interfere in any way with return currents between the CL-GD7555 and the DRAM array, as any ground differential between the CL-GD7555 and DRAM directly subtracts from noise margins.

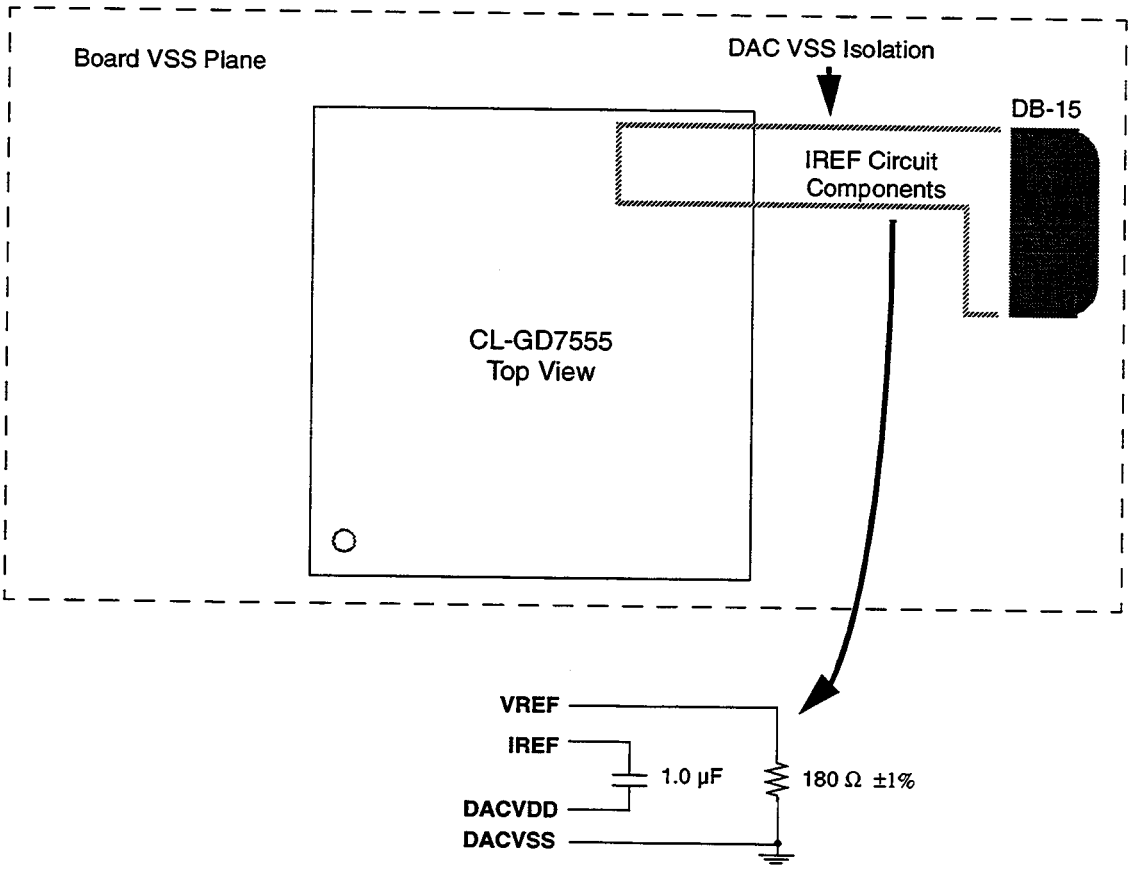



**Figure 2. Example: Isolating the Ground Plane**

## 4. Layout Guidelines for IREF Circuitry

The current reference (IREF) to the DAC is generated with an on-chip constant current source. Use the following guidelines for the IREF circuit.

- As shown in Figure 2, IREF circuit components must be returned to the DAC / IREF section of the ground plane.
- In some layouts, to suppress noise it may be necessary to place a capacitor of approximately 0.1 µF between IREF and the DAC VDD (DACVDD). The layout must make provisions for such a capacitor, in case it becomes necessary to add it. (During system evaluation, the decision can be made as to whether or not to use the capacitor. If it appears necessary to add the capacitor, its exact value can be determined at that time.)

## 5. Layout Guidelines for RGB Lines

Traces for RGB lines are likely to be fairly long. Rise and fall times on the RGB lines are from 2 to 4 ns, causing them to behave as transmission lines. As a result, the characteristic impedance must be controlled so that it is close to the nominal monitor termination value of 75 Ω. To control the impedance, as shown in the schematics in CL-GD7555 Demonstration Board application notes, there must be π-LC filters on each of the RGB lines.

In selecting component values, the trade-off is between the quality of the display image appearing on the CRT monitor display screen and acceptable emissions. Obtaining a crisp display image on the display screen requires that rise and fall times on the RGB lines be as fast as possible. However, for acceptable emissions results, it is necessary that rise and fall times on the lines be relatively slow. As pixel rates increase, the margin between these two conflicting requirements decreases. Use the following guidelines for the RGB lines.

- The following component values represent our present recommendation:
  - — Each of the recommended capacitors must have a value of 10 pF.
  - — Each of the recommended inductors must be a ferrite bead, with 10- to 20-Ω impedance at 100 MHz.
- The π-LC filter components must be placed as close to the VGA DB-15 CRT monitor connector as possible.
- For each of the RGB lines, a 150-Ω resistor to the DAC VSS (DACVSS) is specified. These resistors must be placed as close to the CL-GD7555 as possible.

## 6. Layout Guidelines for the DRAM Array

The display memory DRAMs typically operate as fast as or even faster than the system memory DRAMs. Consequently, the layout of this array must be given as much consideration as that of the system memory. The following general guidelines apply.

- The DRAMs must be placed close to the CL-GD7555. In addition, they must be organized so that each individual device is close to the respective MD pins on the CL-GD7555.
- In designs using four DRAMs, make provisions for damping resistors on the control and address lines in order to minimize noise in the array. Position the damping resistors at the CL-GD7555 end of the lines.
- The control lines for the DRAMs must be treated as fast, heavily loaded lines. The control lines require traces that are relatively wide, typically from 8 to 10 mils. Furthermore, the traces for the control lines must be adequately spaced. Ideally, place the traces 25 mils from the center of one line to the center of another line. Whenever possible, avoid long parallel runs for traces for control lines.

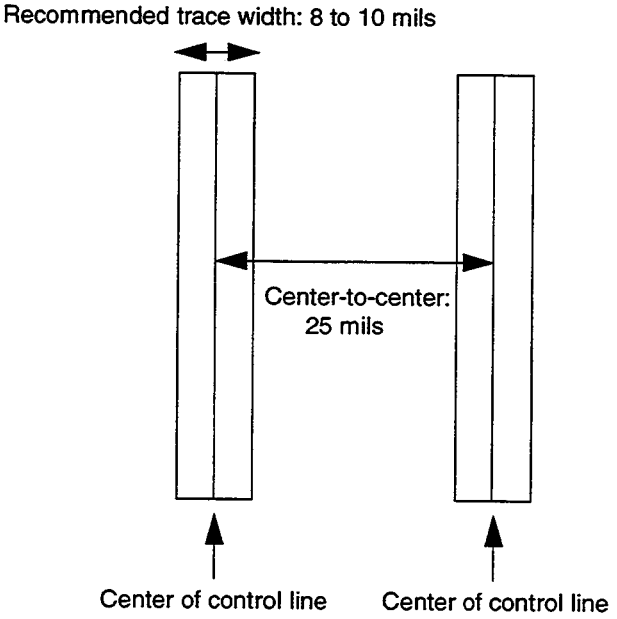



**Figure 3. Traces for DRAM Control Lines**

# Using the Chrontel CH7001 VGA-to-NTSC/PAL Encoder

***with the CL-GD7555 LCD/CRT Controller***

**Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application note presents information on using the Chrontel CH7001 NTSC/PAL Encoder Demonstration Board with the CL-GD7555 LCD/CRT controller.

**Applicability**

This document applies to the following products:

_✔_ CL-GD7555

**Related Materials**

- *Chrontel Application Note AN-11: PC Board Layout Considerations*
- *Chrontel Application Note AN-19: Tuning Clock Outputs*
- *Chrontel CH7001 Data Sheet and Technical Bulletins*
- *Cirrus Logic CL-GD7555 Reference Manuals*
- *Cirrus Logic VGA BIOS Diskette*
- *Cirrus Logic VGA BIOS External Function Specifications*

# Table of Contents

## 1. Introduction

This application note documents how to use the Chrontel CH7001 VGA-to-NTSC/PAL encoder Demonstration Board with the CL-GD7555 LCD/CRT Super VGA Controller. Refer to the Chrontel documentation, listed on the front of this application note, to use the Chrontel Demonstration Board in a circuit design to do the following:

- Select either a NTSC or PAL display device
- Adjust the horizontal or vertical position of the NTSC or PAL display device
- Select a mode for reducing flicker on the NTSC or PAL display device

## 2. Block Diagram of the CH7001-to-CL-GD7555 Interface

Figure 1 is a block diagram of how the Chrontel CH7001 Demonstration Board interfaces to the CL-GD7555.

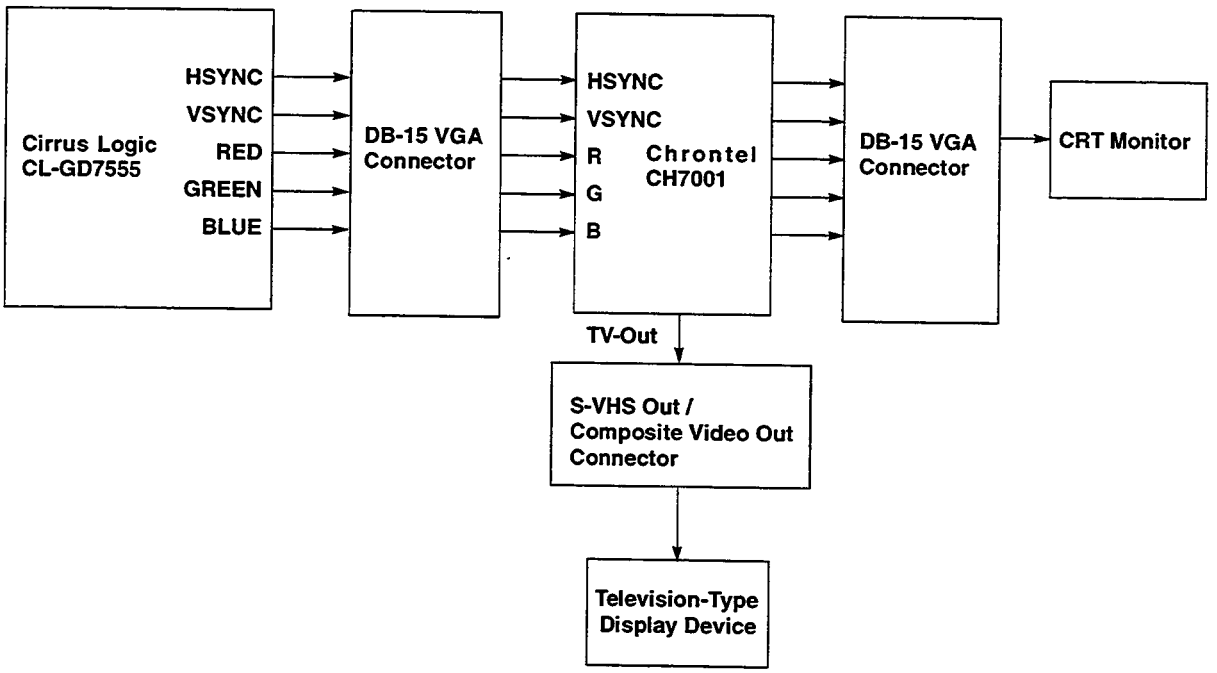



**Figure 1. Block Diagram of Chrontel CH7001 - Cirrus Logic CL-GD7555 Connection**

## 3. Chrontel Demonstration Board Components

Figure 2 shows the location of components used to interface the Chrontel board with the CL-GD7555.

**NOTE:** To power the Chrontel Demonstration Board up or down, on the switch block, use Switch 8, the PD* (power down) switch.

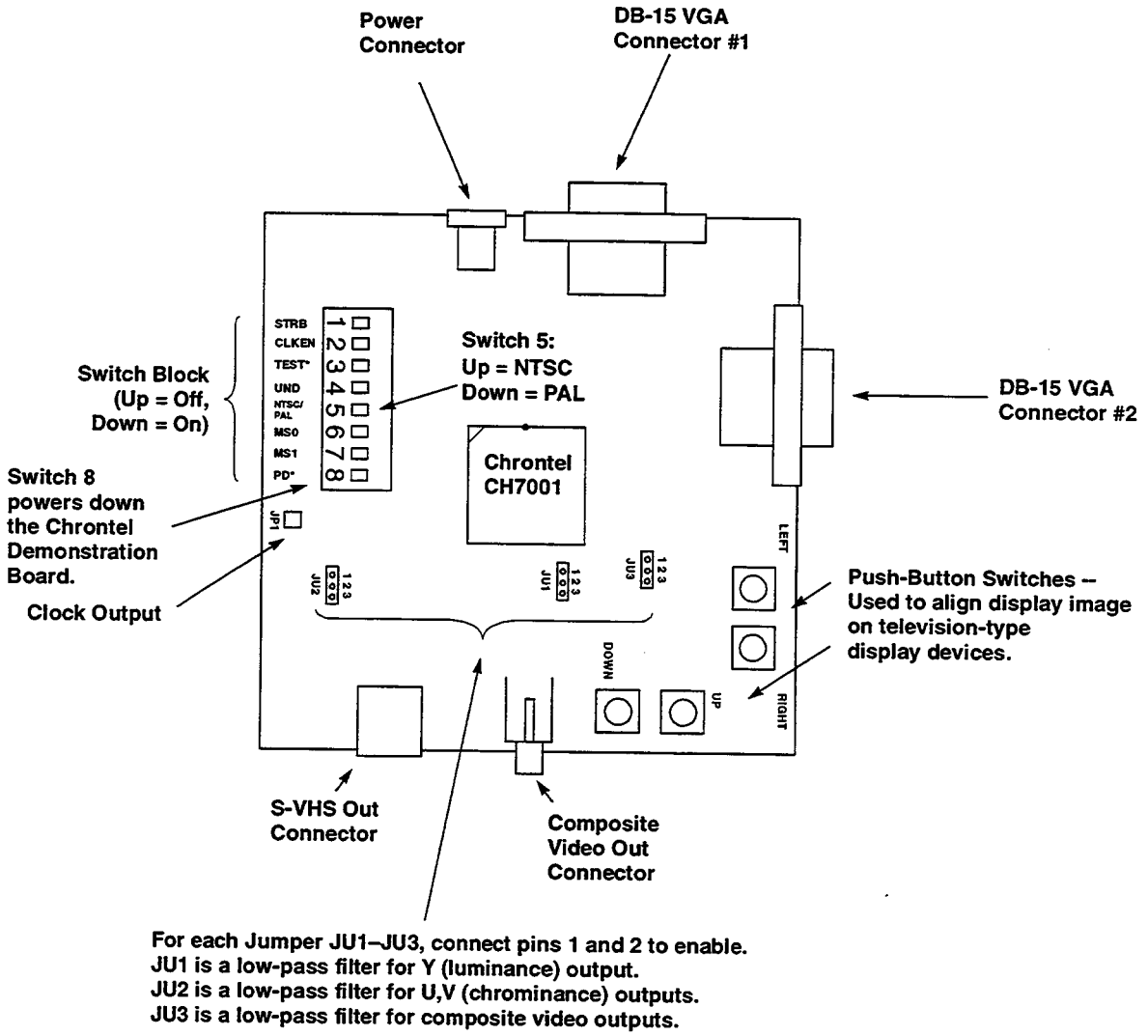



**Figure 2. Location of Chrontel CH7001 Demonstration Board Components**

# 4. Programming Notes for the Chrontel Demonstration Board

This section documents how to use the Chrontel Demonstration Board with the CL-GD7555. As discusssed in Section 5, to customize the Cirrus Logic VGA BIOS for specific requirements, use the Cirrus Logic OEMSI Utility.

## 4.1 Display Devices that Can Be Used

### 4.1.1 Display Devices that Can Be Used with the CL-GD7555

Using the Cirrus Logic CL-GD7555 in a system design allows a display image to appear on one or more display devices. With the CL-GD7555, the range of display device configurations includes the following:

1) Flat panel only
2) CRT monitor only
3) SimulSCAN, in which an image appears on both a flat panel and a CRT monitor (but *not* a TV-type display device)

### 4.1.2 Display Devices that Can Be Used with Both the CL-GD7555 and the CH7001

Using *both* the Cirrus Logic CL-GD7555 and the Chrontel CH7001 in a system design extends the range of display device configurations on which a display image can appear to include the following:

1) Flat panel only
2) CRT monitor only
3) SimulSCAN, in which an image appears on both a flat panel and a CRT monitor (but *not* a TV-type display device)
4) NTSC TV-type display device only
5) PAL TV-type display device only
6) Both a TV-type display device and a CRT monitor

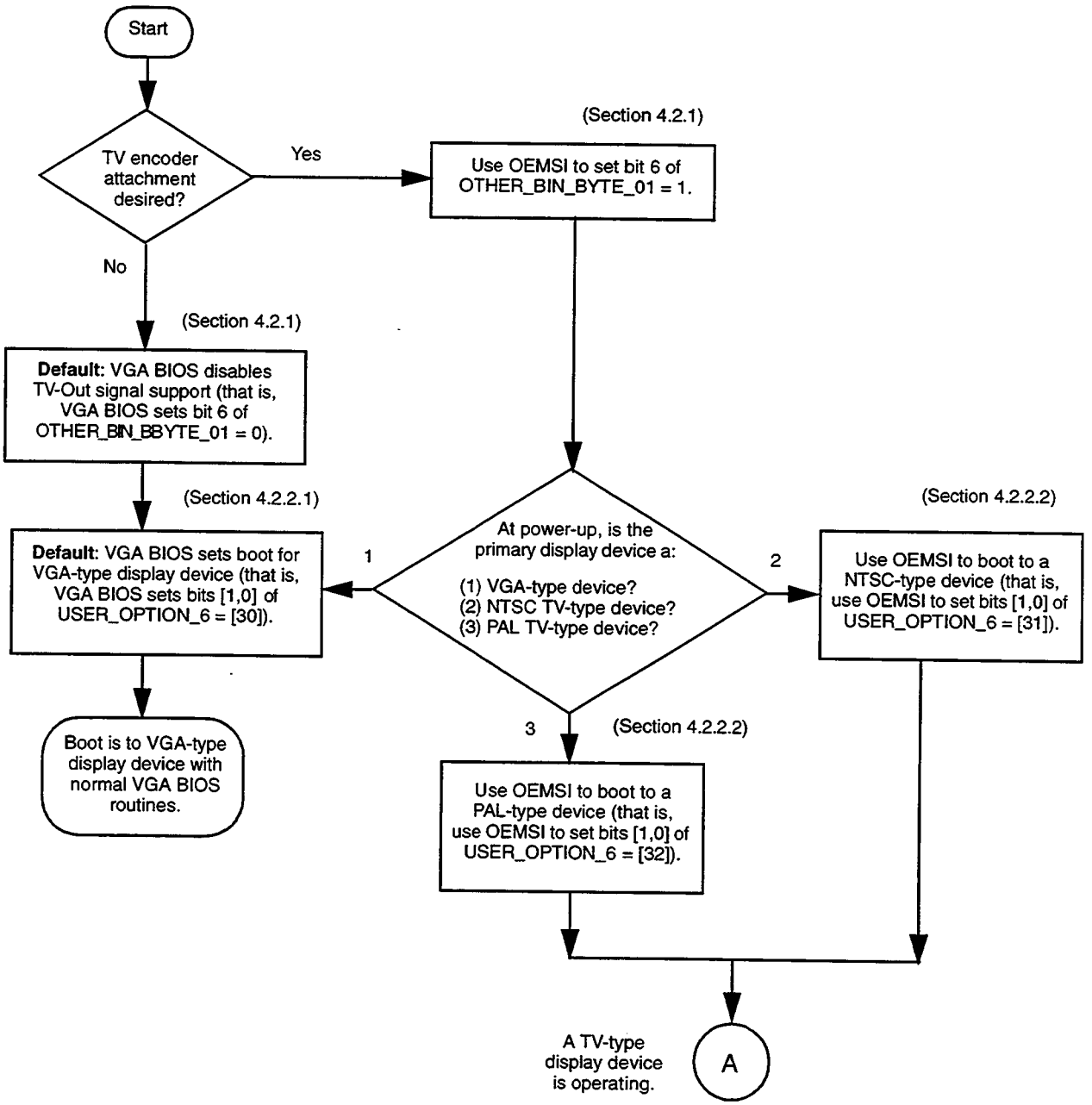
### 4.1.3 Information on Display Device Configurations

For information on enabling these display device configurations – flat panel only, CRT monitor only, or the SimulSCAN operation – refer to the *CL-GD7555 Hardware Reference Manual*, Extension register bits CR80[1:0].

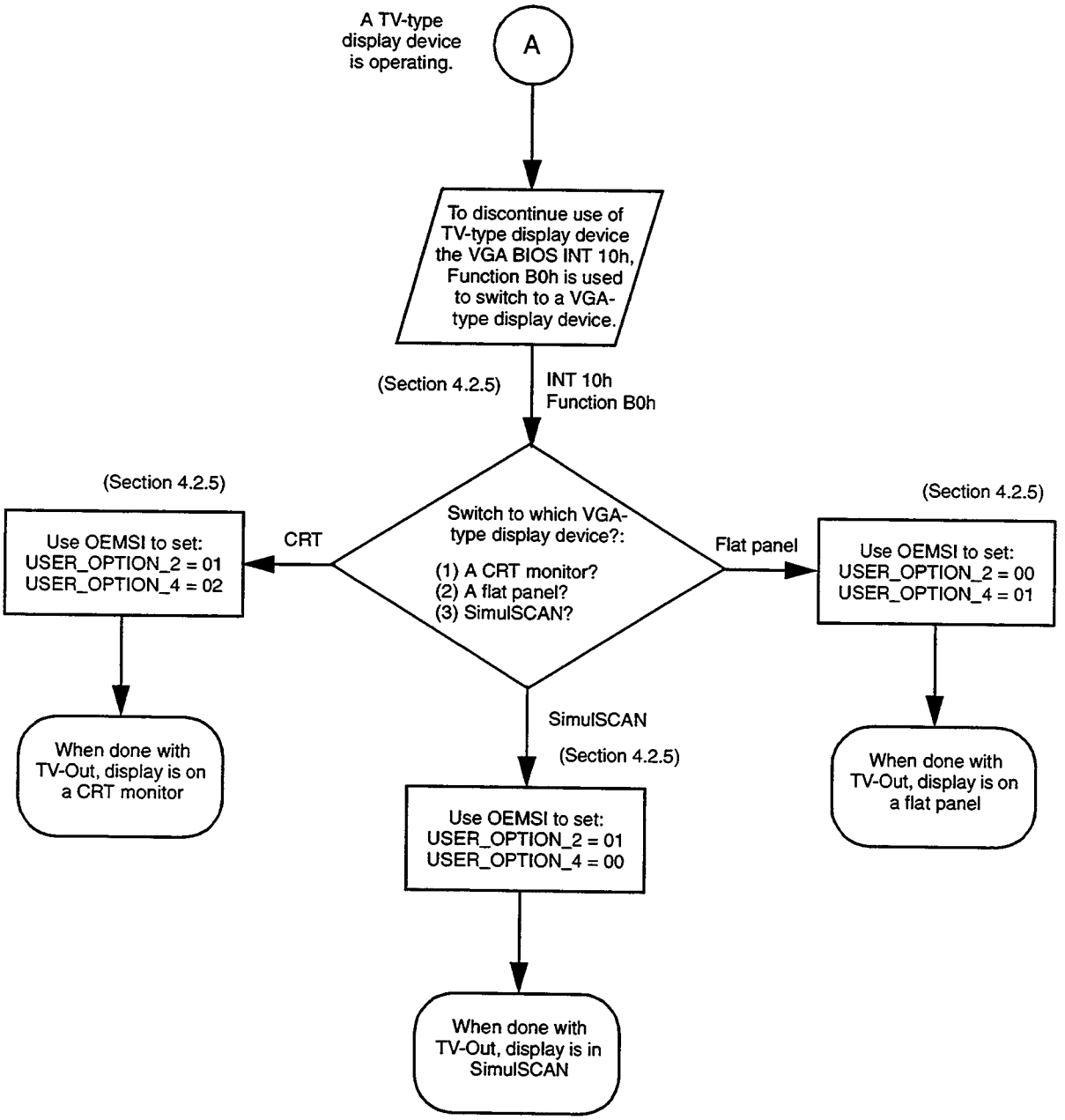
## 4.2 Enabling TV-Type Display Device(s)

As shown in the flowchart that follows, the OEMSI Utility is needed for custom changes to the Cirrus Logic VGA BIOS default. (Section 5 gives an example of how to make the changes, step by step.)

**Flowchart 1. Programming the Chrontel Demonstration Board**



**Flowchart 1 (cont.). Programming the Chrontel Demonstration Boar**



### 4.2.1 Enabling Support of a TV-Out Signal

By default, the Cirrus Logic VGA BIOS assumes that no TV encoder is attached to the CL-GD7555 (that is, support for TV-out signals is disabled). As a result, for those systems that are configured with a TV encoder such as the Chrontel CH7001, to enable support for TV-out signals, as discussed in Section 5, use the OEMSI Utility to set bit 6 of `OTHER_BIN_BYTE_01` to 1.

VGA BIOS default disables TV-out support by programming bit 6 of `OTHER_BBIN_BYTE_01` to 0:

```
OTHER_BIN_BYTE_01 = [0000-0000]
```

To enable TV-out support, use OEMSI to program bit 6 of `OTHER_BIN_BYTE_01` to 1:

```
OTHER_BIN_BYTE_01 = [0100-0000]
```

**IMPORTANT:** Other bits within `OTHER_BIN_BYTE_01` disable or enable other programming functions.

### 4.2.2 Enabling a Boot Display Device

#### 4.2.2.1 Default Boot Display Device

By default, at POST the Cirrus Logic VGA BIOS disables a TV-type display device (and enables a VGA-type display device) by programming `USER_OPTION_6` to [30]:

```
USER_OPTION_6 = [30]
```

#### 4.2.2.2 Enabling a Boot to a TV-Type Display Device

To select either an NTSC or a PAL display device as the boot device, as discussed in Section 5, use the OEMSI Utility to set bits [1:0] within `USER_OPTION_6`.

1) For the Cirrus Logic VGA BIOS to enable support of a NTSC-type display device, use OEMSI to program `USER_OPTION_6` as follows:

```
USER_OPTION_6 = [31]
```

2) For the Cirrus Logic VGA BIOS to enable support of a PAL-type display device, use OEMSI to program `USER_OPTION_6` as follows:

```
USER_OPTION_6 = [32]
```

### 4.2.3 Default Display Device When TV-Out Signal Is Disabled

If either an NTSC or a PAL display device are selected as the boot display device, and if in addition the TV-Out signal becomes disabled (refer to Section 4.2.1), then the possible display device options include the following:

1) By default, the Cirrus Logic VGA BIOS enables the CRT-only option by programming the following:

```
USER_OPTION_2 = [01]
USER_OPTION_4 = [02]
```

2) For the Cirrus Logic VGA BIOS to enable the panel-only option, as discussed in Section 5, use the OEMSI Utilty to program the following:

```
USER_OPTION_2 = [00]
USER_OPTION_4 = [02]
```

3) For the Cirrus Logic VGA BIOS to enable the SimulSCAN option, as discussed in Section 5, use the OEMSI Utility to program the following:

```
USER_OPTION_2 = [01]
USER_OPTION_4 = [00]
```

### 4.2.4 Enabling a Boot to a Display Mode Other than Display Mode 3h

By default, the Cirrus Logic VGA BIOS boots to display mode 3h. To select an alternative display mode as the boot display mode, use external signaling mode INT 15h function calls.

### 4.2.5 Selecting a TV-Type Display Device or Switching Back to a VGA-Type Display Device

Before selecting a TV-type display device, ensure that the current display mode that is being used by the CL-GD7555 is also one that is supported by a TV-type display device. If the display mode currently being used is not one that is supported by a TV-type display device, switching to a television display mode from the following does not work:

- Panel-only display mode
- CRT-only display mode
- SimulSCAN operation (that is, operating both a flat panel and a CRT monitor)

The following display modes are supported by TV-type display devices:

- All standard VGA display modes (that is, display modes 0h–13h and display modes Dh–Fh)
- Extended VGA display modes 5Eh, 5Fh, 64h, 66h, and 71h

Use the Cirrus Logic VGA BIOS function B0h (that is, the Set/Get TV Output function) to set the desired TV-type display device to an NTSC or PAL display device or to switch back to a VGA-type display device.

| | | | | |
|---|---|---|---|---|
| **Input:** | AH | = | 12h | |
| | BL | = | B0h | |
| | AL | = | Bits 3:0 | Display Device Output Type<br>(0h = VGA Output Type – no TV Out.)<br>(1h = NTSC Output Type)<br>(2h = PAL Output Type)<br>(3h:Eh = Reserved)<br>(Fh = Request status of TV Out type) |
| | | | Bits 7:4 | Reserved |
| **Output:** | AL | = | Bits 3:0 | Display Device Output Type<br>(0h = VGA Output Type – no TV Out)<br>(1h = NTSC Output Type)<br>(2h = PAL Output Type)<br>(3h:Fh = Reserved) |
| | | | Bits 7:4 | Reserved |
| | BH | = | Bit 0 | '0' = TV Output type functionality is disabled.<br>'1' = TV Output type functionality is supported. |
| | | | Bit 7:1 | Reserved |

After the Cirrus Logic VGA BIOS is set for a TV-type output, on the Chrontel Demonstration Board set Switch Block Switch 5 to either up for an NTSC output, or set it to down for a PAL output. (Refer to Figure 2.)

#### 4.2.5.1 Selecting a TV-Type Display Device

When using the CL-GD7555 to select a TV-type display device, prior to enabling a TV-type output, if the version of the CL-GD7555:

- *Is not* version CD or greater, the flat panel must be unplugged before it can be safely powered down.

  ▼ Warning: Unless the flat panel is unplugged, damage can occur to the flat panel.

- *Is* version CD or greater, the flat panel is safely powered down.

#### 4.2.5.2 Switching from a TV-Type Display Device to a VGA-Type Display Device

When using the CL-GD7555 to switch from a TV-type display device to a VGA-type display device :

- Previously, if the VGA subsystem booted as a TV-type display device, the result is one of two possibilities:
  - — By VGA BIOS default, the result is a switch to a CRT monitor only.
  - — By using OEMSI (see the flowchart), an alternate result is a switch to either a panel only or to SimulSCAN
- Otherwise, the switch is to the type of display device that was active prior to enabling the TV output.

## 4.3 Changing the Timing for TV-Out Signals

If the Cirrus Logic VGA BIOS `USER_OPTION_6` is not set to [30] (that is, it is set to either [31] or [32]), the VGA BIOS automatically enables the registers that are used for TV-out signals.

To customize the default NTSC and PAL TV-out timing signals, as discussed in Section 5, within the OEMSI Utility, search for the TV heading. Upon finding the TV heading, as appropriate, change either TV table entry 1 or TV table entry 2.

- For NTSC timing registers (that is, for a display screen refresh rate of 60 Hz), use:

  ```
  TV table entry 1
  ```

- For PAL timing registers (that is, for a display screen refresh rate of 50 Hz), use:

  ```
  TV table entry 2
  ```

## 4.4 Adjusting the Overscan Border

To adjust the overscan border with the Chrontel Demonstration Board, use the push-button switches labelled "UP", "DOWN", "LEFT", and "RIGHT". (Refer to Figure 2.)

## 5. Steps for Using the Chrontel CH7001 Demonstration Board

This section documents how to use the Cirrus Logic OEMSI Utility to change the Cirrus Logic VGA BIOS for use with the Chrontel Demonstration Board.

1. Obtain the Cirrus Logic VGA BIOS diskette, which contains the following files:
   - MAKERAM.EXE
   - OEMSI.EXE
   - OEMDATA.TXT
   - VGA.BIN
   - VGA.COM
   - VGA.SYS
2. Refer to Figure 1 and Figure 2 and make the following connections:
   a. Use the Chrontel Demonstration Board power connector to connect it to a power supply.
   b. Use a DB-15 connector cable to connect one of the two Chrontel Demonstration Board DB-15 connectors to the CL-GD7555 Demonstration Board.
   c. Use another DB-15 connector cable to connect the other one of the two Chrontel Demonstration Board DB-15 connectors to a CRT monitor for a PC.
   d. Connect the Chrontel Demonstration Board to a television-type display device. Use either the Chrontel Demonstration Board's S-VHS Out connector or the Compositve Video Out connector, or both.
3. Turn on the PC and its CRT monitor, and insert the Cirrus Logic VGA BIOS diskette in a floppy disk drive (for example, the a: drive).
4. At the DOS c: prompt, make a directory to hold the contents of the VGA BIOS diskette.

   ```
   c:>md yourdir
   ```

5. Copy the contents of the VGA BIOS (VGA.BIN) and the OEMSI Utility (OEMSI.EXE) to your directory.

   ```
   c:>yourdir>copy a:\VGA.BIN .

   c:>yourdir>copy a:\OEMSI.EXE .
   ```

6. Within your directory, copy the VGA.BIN file to a file name of your choosing.

   ```
   c:>yourdir>copy VGA.BIN CHOICE1.BIN
   ```

7. Use the OEMSI Utility on the new binary file you just created (in the example above, `CHOICE1.BIN`) to create and export an OEMSI data file (for example, `DATAFIL.1`).

   ```
   c:>yourdir>oemsi -b DATAFIL.1 CHOICE1.BIN
   ```

   When this command successfully completes, the following message appears:

   ```
   DATAFIL.1 successfully exported.
   ```

8. Refer to Flowchart 1 and as necessary, edit the OEMSI data file (in this example, `datafil.1`).
   a. For example, if a TV encoder attachment (such as the Chrontel Demonstration Board) is desired, edit the OEMSI data file as follows.

      ```
      c:>yourdir>edit datafil.1
      ```

   b. When you press the Return key, the OEMSI data file appears. To enable a TV encoder attachment, use the down arrow key to move the cursor to `OTHER_BIN_BYTE_01` = [0000-0000]
   c. Use the keyboard to change bit 6 from a 0 to a 1.
   d. When the change is done, exit the OEMSI data file by pressing the ALT and X keys, and save the change by indicating the "YES" choice.
9. After making this change to the OEMSI data file, use the OEMSI Utility to import the changed version of the OEMSI data file into the VGA BIOS file.

   ```
   c:>yourdir>oemsi -i datafil.1 choice1.bin
   ```

   When this command successfully completes, the following message appears:

   ```
   choice1.bin has been successfully imported.
   ```

10. Repeat the previous two steps for any other edits.
11. At this point, the new VGA BIOS is ready for operation with the Chrontel CH7001 Demonstration Board.
12. To use the Chrontel Demonstration Board, refer to the Chrontel documentation cited on the cover of this document.

# Requirements for the OSC Signal during Suspend/Resume Operations

***of the CL-GD7555 LCD/CRT Controller***

**Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application note presents requirements for the CL-GD7555 OSC signal during suspend/resume operations.

**Applicability**

This document applies to the following products:

✔ CL-GD7555

**Related Materials**

– *Cirrus Logic CL-GD7555 Reference Manuals*

# 1. Introduction

This application note documents the OSC signal requirements during the suspend/resume operations of the CL-GD7555 LCD/CRT Super VGA Controller.

# 2. Requirements for OSC Signal during Suspend Operations

During the CL-GD7555 suspend operation, the requirements for the OSC signal are as follows:

## 2.1 OSC Requirements when Extension Register Bit CR8D[4] Is 1

When Extension register bit CR8D[4] is 1:

- The CL-GD7555 CLK32K / SUSPST# pin is configured for SUSPST#. In this case, a clock signal does not need to be present on the CLK32K / SUSPST# pin.
- A 14.318-MHz clock signal must be continuously present on the CL-GD7555 OSC input pin. This clock signal must be present on the OSC pin when the suspend operation begins and during the suspend operation.

## 2.2 OSC Requirements when Extension Register Bit CR8D[4] Is 0

When Extension register bit CR8D[4] is 0:

- The CL-GD7555 CLK32K / SUSPST# pin is configured for CLK32K. In this case, a 32.768-kHz clock signal must be continuously present on the CLK32K / SUSPST# pin.
- This bit setting allows the 14.318-MHz clock signal on the OSC input pin to be stopped for the duration of the suspend operation, if desired.

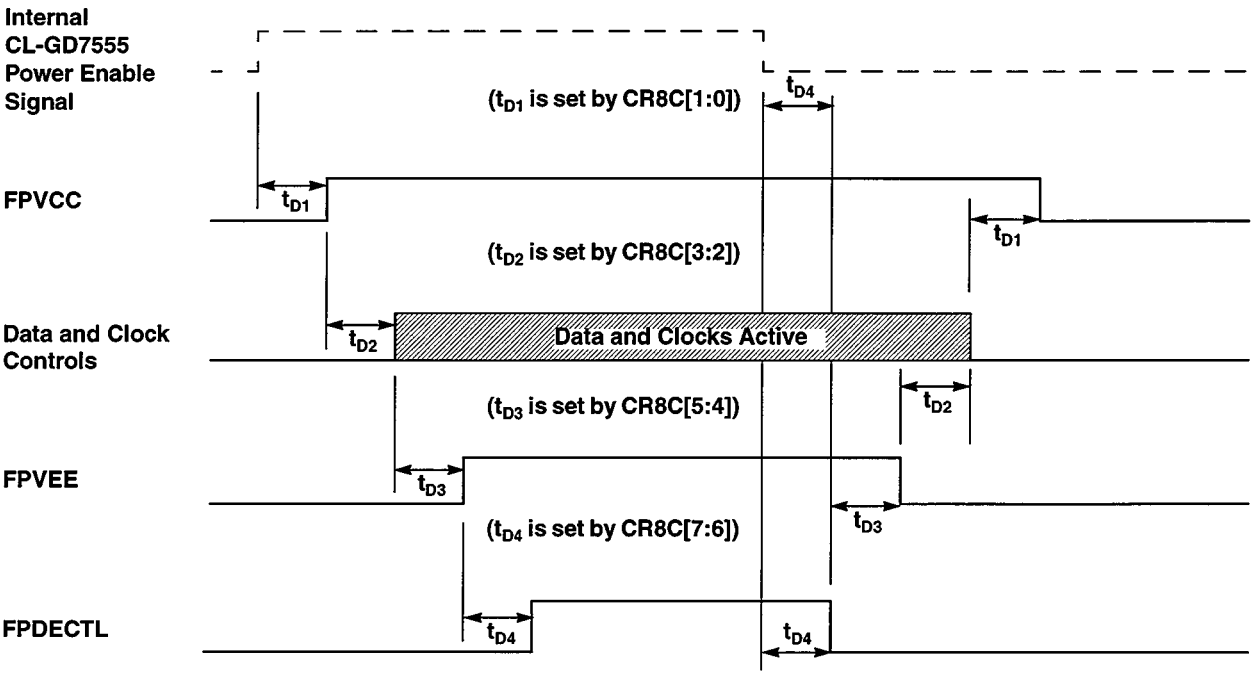
For either a software-controlled suspend operation or a hardware-controlled suspend operation (that is, when CR80[2] is 1 or the SUSPI input signal is asserted), to initiate the suspend operation, software is not allowed to poll for a confirmation of a suspend operation. As a result, after either CR80[2] is 1 or SUSPI is asserted, the clock signal to the OSC pin must be maintained for a minimum safe delay time, after which time the OSC signal can be inactivated if desired.

## 12.128 CR8C: Programmable Power Sequencing Register *(cont.)*

**Bit** **Description**

| Bit Setting for Specified Delay | Amount of Delay Between Beginning of Specified Signals | |
|---|---|---|
| CR8C[7:6] = $t_{D4}$ | In Units of Time | In Units of Periods of the CLK32K Pin |
| CR8C[5:4] = $t_{D3}$ | | |
| CR8C[3:2] = $t_{D2}$ | | |
| CR8C[1:0] = $t_{D1}$ | | |
| '00' | ~ 32 ms | 1024 periods (Cirrus Logic VGA BIOS default) |
| '01' | ~ 4 ms | 128 periods |
| '10' | ~ 64 µs | 2 periods |
| '11' | ~ 256 ms | 4096 periods |

**NOTE:** For each of the $t_{D1}$, $t_{D2}$, $t_{D3}$, and $t_{D4}$ parameters, the Cirrus Logic VGA BIOS default values are ~32 msec.




**Flat Panel Power-Up and Power-Down Delay Settings**

## 3. Requirements for OSC Signal during Resume Operations

After the CL-GD7555 has been in a suspend operation and resume operations are beginning, the requirements for the CL-GD7555 OSC signal are as follows:

1. The 14.318-MHz clock signal on the OSC pin must be re-activated no later than when the SUSPI signal is de-asserted.
2. After SUSPI is de-asserted, wait 10 msec before accessing either the CL-GD7555 VGA External/General palette registers at 3C6–3C9 or the display memory frame buffer. This 10-msec delay ensures that the VCLK and MCLK signals that are derived from OSC have stabilized.

   **NOTE:** When SUSPI is de-asserted, the internal CL-GD7555 clock synthesizers remain in suspend mode for as many as 3 CLK32K / SUSPST# periods before activating and then stabilizing.

# Design Requirements for Power Sequencing

***for the CL-GD7555 LCD/CRT Controller (Revision CD)***

**Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application note presents power sequencing requirements for Revision CD of the CL-GD7555 controller.

**Applicability**

This document applies to the following products:

_✔_ CL-GD7555

**Related Materials**

– *Cirrus Logic CL-GD7555 Reference Manuals*

# 1. Introduction

This application note documents design requirements for power sequencing for the CL-GD7555 Revision CD LCD/CRT Super VGA Controller when it is used in a 3.3-/5-V mixed-voltage configuration.

# 2. CRTVDD Design Requirements

The CL-GD7555 can be used in a mixed-voltage configuration that is capable of using either 3.3 or 5 V. In such a configuration, the CL-GD7555 Revision CD CRTVDD power supply pin must be connected to +5 V, in order to impart 5-V tolerance to the I/O pad ring (which prevents possible latch-up conditions).

As a result, the CL-GD7555 has the following design requirements:

- When the CL-GD7555 is used in a mixed-voltage configuration:
  - — The CRTVDD pin must be connected to +5 V.
  - — The CRTVDD pin must activate at the same time as or no later than other VDD supply pins.
- The 3.3-V power supply must be subordinate to the 5-V power supply.

## 2.1 CRTVDD Connection Requirements

The CL-GD7555 has the following connection requirements:

- When the CL-GD7555 is used in a mixed-voltage configuration that is capable of using either 3.3 or 5 V, the CRTVDD power supply pin must always be connected to +5 V in order to bias the n-well regions of the I/O pads.
- At all times, the CRTVDD pin must receive the highest supply voltage applied to the CL-GD7555, even during the moments of system power-up and power-down.
- If any of the following VDD power supply groups – BVDD, FPVDD, or MVDD – are used in a 3.3-V configuration, to ensure the proper functioning of the CL-GD7555 Demonstration Board, refer to Figure 1 and Figure 2 and make the following adjustments to the Power Supply Module that is used with the Demonstration Board.

  1. On the solder side of the Power Supply Module, solder in place a wire that connects to the trace shown the pin of the voltage regulator that is closest to C7.

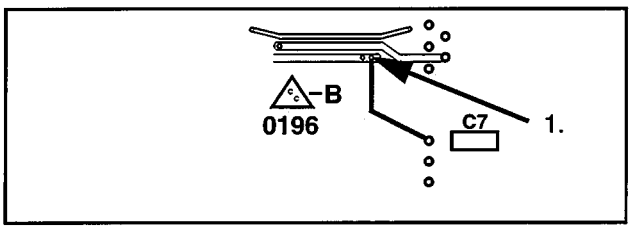



**Figure 1. CL-GD7555 Power Supply Module for Demonstration Board (Solder Side)**

2. On the component side of the Power Supply Module, remove the inductor L1.

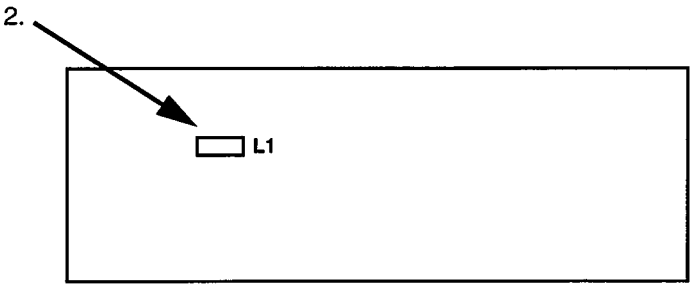



**Figure 2. CL-GD7555 Power Supply Module for Demonstration Board (Component Side)**

## 2.2 CRTVDD Activation Time

Because the CL-GD7555 CRTVDD 5-V power supply pin is used to bias the n-well regions of the I/O pads, the CRTVDD pin must be activated at either the same time as, or at no later time than, the other VDD power supply pins, listed below.

- BVDD1,2
- FPVDD1,2
- MVDD1,2,3

**NOTE:** The CRTVDD relationship with the CVDD[3:1], MAVDD, and VAVDD pins does not matter, since the CRTVDD pin is not used to bias the n-wells in those parts of the CL-GD7555.

## 3. Power Supply Design Requirements

Because the CL-GD7555 CRTVDD 5-V power supply pin is used to bias the n-well regions of the I/O pads, when the CL-GD7555 is used in a mixed-voltage configuration that is capable of using either 3.3 or 5 V, the CL-GD7555 power supply must be designed as follows.

- The 3.3-V power supply must be subordinate to the 5-V power supply so that it does not activate before the 5-V power supply.
- The 3.3-V power supply must never – that is, neither at power-up, nor power-down – be momentarily more than a diode-drop higher voltage than the 5-V power supply.

**NOTE:** On the CL-GD7555 Demonstration Board, the +3.3-V supply (that is, the "ADJ" potentiometer) is derived from the +12-V rail.

In Figure 3, the 'problem area' shows a condition that was measured on the CL-GD7555 Demonstration Board and which must be avoided. (This particular figure demonstrates a problem that is caused by the 5-V power supply activating too slowly.)

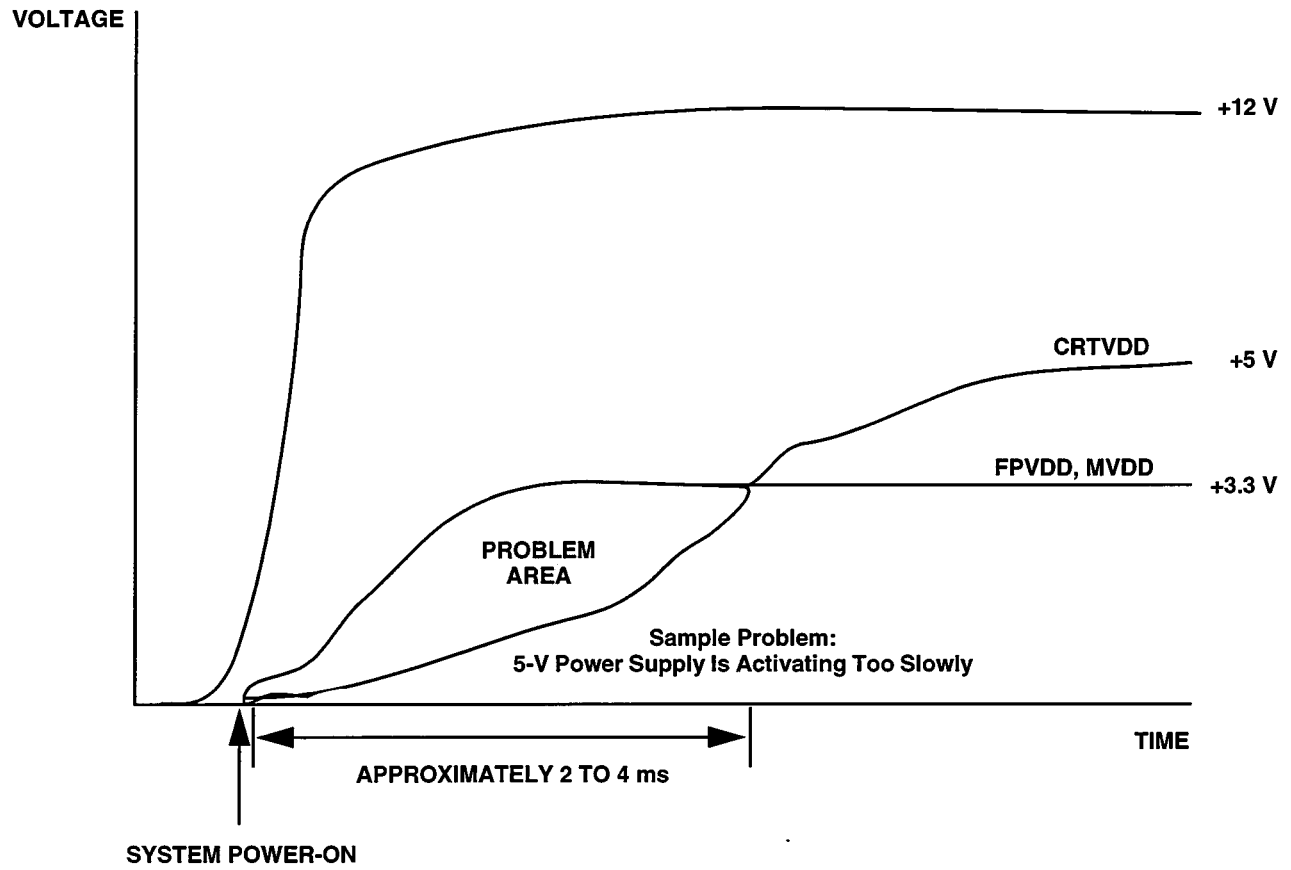



**Figure 3. CL-GD7555 Power-Up**
**('Problem Area' Demonstrates a Condition that Is To Be Avoided)**

# Design Requirements for Board Upgrade

***from the CL-GD7555 LCD/CRT Controller to the CL-GD7556-AB LCD/CRT Controller***

**Graphics Company – Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application note presents design changes to be made when upgrading a board from the CL-GD7555 controller to the CL-GD7556 controller.

**Applicability**

This document applies to the following products:

✔ CL-GD7555
✔ CL-GD7556

**Related Materials**

– *Cirrus Logic CL-GD7555 and CL-GD7556 Reference Manuals*

# Revision Pages:

| Version | Change Made From Previous Version to Current Version: | Page |
|---|---|---|
| Version 1.1 | • In section 1, add a third subsection heading, section 1.3, and move the bullet that starts "No internal pull-up..." from section 1.2 to section 1.3. | 3 |
| | • In section 2, change the second bullet so that instead of reading only "4.7 kΩ", it now reads "4.7 kΩ to 6.8 kΩ". | 3 |
| | • The previous section 4 is now section 5.<br>The previous section 5 is now section 4. | 5 |
| | • In the currection section 5 (which starts with the text "No Internal..."), change "Revision AB" to "Revision AC". | 5 |

# 1. Introduction

This application note documents design changes that are required when upgrading a board design from one that uses a CL-GD7555 LCD/CRT Super VGA Controller to a board that uses the CL-GD7556 Revision AB.

The CL-GD7556 pinout and register set are supersets of those for the CL-GD7555. On a board that uses only 3.3-V, the CL-GD7556 achieves the same 5-V graphics/video performance of the CL-GD7555. In addition, the CL-GD7556 also has the following features:

- Resolution of up to 1280 x 1024, at 75-Hz vertical refresh rate
- Support for 1024 x 768 dual-scan STN panels
- On-chip design of TV-Out to external analog TV encoder

## 1.1 Issues When Upgrading from CL-GD7555 to the CL-GD7556 Revision AB Only

The following issue applies only when upgrading from the CL-GD7555 to the CL-GD7556 Revision AB:

- External pull-down resistors for hardware configuration (Section 2)

## 1.2 Issues When Upgrading from CL-GD7555 to the CL-GD7556 Revision AB and Subsequent Revisions

The following issues apply when upgrading from the CL-GD7555 to the CL-GD7556 Revision AB and all subsequent revisions:

- Proper supply voltage to the VDD pins (Section 3)
- Support for the on-chip TV-Out design (Section 4)

## 1.3 Issues When Upgrading from CL-GD7555 to the CL-GD7556 Revision AC and Subsequent Revisions

The following issues apply when upgrading from the CL-GD7555 to the CL-GD7556 Revision AC and all subsequent revisions:

- No internal pull-up resistor on the PCI reset RST# signal (Section 5)

# 2. External Hardware Configuration Pull-Down Resistors (Revision AB Only)

The CL-GD7556 has twelve hardware configuration pins (such as the BIOSPU, MMIOPU, and so forth). Each of these twelve pins must be connected to either a pull-up resistor or a pull-down resistor, depending on how the pin is used. (For more information, in the *CL-GD7556 Hardware Reference Manual*, refer to Chapter 2, "Pin Descriptions".)

If the resistor to be used is a:

- *Pull-up*, the resistance must be in the range of from 10 kΩ to 20 kΩ.
- *Pull-down*, the resistance must be in the range of 4.7 kΩ to 6.8 kΩ.

**NOTE:** The requirement for pull-down resistors applies to the CL-GD7556 Revision AB silicon only. For the next CL-GD7556 revision and for all subsequent revisions, only pull-up resistors are to be required.

# 3. Proper Supply Voltage to the VDD Pins (Revision AB and Subsequent Revisions)

## 3.1 VDD Issue 1: CL-GD7556 VDD Pins Are Used in +3.3-Volt-Only Environment

On the CL-GD7556, all of the VDD pins (that is, the core VDD, the analog VDDs, and the peripheral VDDs) must be set to +3.3 V. The core VDD and the peripheral VDDs (that is, the CRT VDD, the memory VDD, the flat panel VDD, and the bus VDD) are all connected inside the CL-GD7556. As a result, the voltage applied to those VDD pins must be the same.

Although the CL-GD7556 works only in a 3.3-V environment, all of the CL-GD7556 input pads are 5-V tolerant. Most of the existing designs based on the CL-GD7556 set the CRT VDD to 5 V either because other CL-GD7555 VDDs are set to 5 V or because the CL-GD7555 V-Port pads must be 5-V tolerant even when all the other VDDs are 3.3 V.

▼ **For those designs that use a CL-GD7555 and that supply 5 V to any of the CL-GD7555 VDD pins, the CL-GD7556 is not a drop-in replacement.**

## 3.2 VDD Issue 2: CL-GD7556 VDD Pins Are +5-V Tolerant

As previously stated, all input pads of the CL-GD7556 are +5-V tolerant. As a result, the following input signals to the CL-GD7556 can be +5 V *as long as* the VDD pins of the CL-GD7556 are set to +3.3 V (+/- 0.15 V).

- PCI bus input signals
- Display memory input signals [that is, from EDO (extended-data out) DRAM]
- V-Port input signals

The output signals from the CL-GD7556 are always rail to rail. Either +5-V EDO DRAM, or a +5-V flat panel LCD, or both can be used as long as the following conditions are met:

- If +5-V EDO DRAM is used:
  - — The output signals from the CL-GD7556 to the EDO DRAM must meet the specifications for input threshold voltage and timing parameters of the EDO DRAM.
  - — The memory VDD of the CL-GD7556 must be set to +3.3 V (+/- 0.15 V).
- If a +5-V flat panel LCD is used:
  - — The output signals from the CL-GD7556 to the LCD flat panel must meet the specifications for input threshold voltage and timing parameters of LCD flat panel
  - — The flat panel VDD of the CL-GD7556 must be set to +3.3 V (+/- 0.15 V).

**NOTE:** Use of either series resistors or filter circuitry affects both the rise/fall time and the voltage level of the CL-GD7556 output signals.

### 3.3 VDD Issue 3: Threshold Level of the CL-GD7556 PCI and V-Port Input Pins

As with the CL-GD7555, the threshold level of the CL-GD7556 PCI input pads are programmed to either a 3.3-V CMOS level or a 5-V TTL level. For the CL-GD7556:

- *PCI input pins*, except for the PCI clock signal, the threshold level for the PCI bus inputs is set by either a hardware configuration pin (that is, pin 219) or an Extension register bit (that is, SR20[7]). The PCI clock is always set to the 3.3-V CMOS level.
- *V-Port input pins*, the input threshold level is set by Extension register bit SR20[4].

When the input threshold level is set to the 3.3-V CMOS level, the $V_{ih}$ (minimum) and the $V_{il}$ (maximum) are set as follows:

- $V_{ih}$ (minimum) = 0.7 × (Core VDD)
- $V_{il}$ (maximum) = 0.3 × (Core VDD)

Example:

The Core VDD is 3.3 V. As a result,

- $V_{ih}$ (minimum) = 0.7 × (Core VDD) = 0.7 × 3.3 V = approximately +2.3 V
- $V_{il}$ (maximum) = 0.3 × (Core VDD) = 0.3 × 3.3 V = approximately +1.0 V

## 4. On-Chip TV-Out Support (Revision AB and All Subsequent Revisions)

The CL-GD7556 has on-chip TV-Out circuitry that outputs RGB/CSYNC signals to an external analog TV encoder. The circuitry is the same as that of the CL-GD7548. For board design guidelines for TV-Out support, refer to the CL-GD7548 application notes.

## 5. No Internal Pull-up Resistor on the PCI Reset Signal (Revision AC and All Subsequent Revisions)

From the next revision of the CL-GD7556 silicon, the internal pull-up resistor on the PCI reset signal (that is, RST#) is to be removed. As a result, when using all subsequent revisions of the CL-GD7556, the board designer must ensure that this signal is always driven high during normal operation.

# CL-GD7555 Application Alert: Using the CL-GD7555 PCI Bus Demonstration Board with an Off-the-Shelf Motherboard

***Procedural Requirements***

**Portable Graphics**
**Cirrus Logic, Inc.**

**Scope**

This application alert presents information not found in previous documentation for the CL-GD7555 LCD/CRT controller.

**Applicability**

This document is intended to be used in conjunction with applicable CL-GD7555 documentation to aid the system designer.

This document applies to the following products:

✔ CL-GD7555

**Related Documents**

– *CL-GD7555 Reference Manuals*

## 1. Introduction

This application alert identifies a problem that certain off-the-shelf motherboards have when they are used with the CL-GD7555 Demonstration Board (referred to in this document as the 'Demonstration Board'). Although the motherboards discussed in this alert work in a desktop environment, they fail with the Demonstration Board because of the new environment that the Demonstration Board presents.

## 2. Statement of Issue

In order to support a variety of panels and to support extensive new features, the CL-GD7555 requires 48 Kbytes of system BIOS instead of the 32 Kbytes of system BIOS required by most previous Super VGA graphics controllers. Consequently, some motherboards fail when they are used with the Demonstration Board. As of the publication date of this document, Cirrus Logic is cooperating with system BIOS providers to resolve these issues.

## 3. Motherboards that Can Be Used with the Demonstration Board

The following off-the-shelf motherboards can be used with the Demonstration Board:

| Manufacturer | Comments |
|---|---|
| American Megatrends (AMI)<br>6145-F Northbelt Parkway<br>Norcross, GA 30071<br>(770) 263-8181 | Motherboards with a core system BIOS dating from July 15, 1995 (Revision 623). |
| Award Software<br>777 Middlefield Road<br>Mountain View, CA 94043<br>(415) 968-4433 | Motherboards manufactured since December 1, 1995. |

# 4. Solutions for Operating a Demonstration Board with a Non-Compliant Motherboard

Cirrus Logic presents the following guidelines as a temporary solution for operating the Demonstration Board with those motherboards that do not comply with the PCI specification for the system BIOS.

1. Ensure that there is an executable panel RAM BIOS on the hard disk.
2. Ensure that the first statement in the AUTOEXEC.BAT file is the executable RAM BIOS command and there is a path to this statement.
3. Use a 32-Kbyte CRT-only BIOS to boot the system. If the system:
   a. Executes the panel RAM BIOS and boots the system, it can then enter either DOS, Windows 3.11, or Windows 95.
   b. Fails to execute the panel RAM BIOS (that is, the system does not boot), go to the next step.
4. Determine if the system can boot without a PCI VGA BIOS on the Demonstration Board.
   a. If the system *cannot boot* without a PCI VGA BIOS on the Demonstration Board, you must contact the appropriate system BIOS vendor to obtain the correct PCI system BIOS.
   b. If the system *can boot* without a PCI VGA BIOS on the Demonstration Board, go to the next step.
5. If the system can boot without a PCI VGA BIOS on the Demonstration Board, determine if the Demonstration Board PCI Slot is disabled. If the PCI slot:
   a. *Is not disabled*:
      (1) Ensure that there is an executable panel RAM BIOS on the hard disk.
      (2) Ensure that the first statement in the AUTOEXEC.BAT file is the executable panel RAM BIOS command and there is a path to this statement.
      (3) Boot the system, after which it can enter either DOS, Windows 3.11, or Windows 95.
   b. *Is disabled*:
      (1) Obtain a PCI slot-enabling program from the PCI system BIOS vendor.
      (2) Install this program on the hard disk.
      (3) Ensure that the first statement in the AUTOEXEC.BAT file is the executable slot-enabling program and there is a path to this statement.
      (4) Ensure that the second statement in the AUTOEXEC.BAT file is the executable panel RAM BIOS command and there is a path to this statement.
      (5) Boot the system, after which it can enter either DOS, Windows 3.11, or Windows 95.

# CL-GD7555 Application Alert: Using Extended-Data-Out DRAMs

***with the CL-GD7555 LCD/CRT Controller***

**Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application alert presents information on using Extended-Data-Out DRAMs (also known as Hyper-Page-Mode DRAMs) with the CL-GD7555 LCD/CRT controller.

**Applicability**

This document is intended to be used in conjunction with applicable CL-GD7555 documentation to aid the system designer.

This document applies to the following products:

_✔_ CL-GD7555

**Related Documents**

– *CL-GD7555 Reference Manuals*

## 1. Introduction

This application alert discusses the type of display memory that can be used with the CL-GD7555 LCD/CRT controller.

## 2. Extended-Data-Out DRAMs

The CL-GD7555 supports only EDO (Extended-Data-Out) multiple-CAS# DRAMs (also known as Hyper-Page-Mode DRAMs) and not fast-page-mode DRAMs. As a result, Extension register bit GR18[2] must always be set to 1.

The EDO DRAMs can be either a 3.3- or 5.0-V type, since the CL-GD7555 display memory interface can run at either 3.3 or 5.0 V, depending on the voltage level for the display memory interface. The EDO DRAM types preserve read data until the start of either the next display memory CAS# (column-address strobe) or RAS# (row-address strobe), whichever signal comes first.

EDO DRAMs are supported by the CL-GD7555 at the following specified maximum MCLK frequencies at the appropriate core VDD voltage levels:

- MCLK up to 66 MHz for a core VDD of 3.3 V (± 0.15 V)
- MCLK up to 80 MHz for a core VDD of 5 V (± 0.25 V)

Consequently, for a cycle time of two MCLKs per page, the page cycle is:

- A maximum of 30-ns/page cycle at a core VDD of 3.3 V
- A maximum of 25-ns/page cycle at a core VDD of 5 V

## 3. Timing

To optimize the timing for the best performance of the EDO DRAMs that are used with the CL-GD7555:

- Refer to Chapter 4 of the *CL-GD7555 Hardware Reference Manual* for the appropriate table that summarizes the timing requirements for the display memory bus interface for a particular system configuration.
- Check the timing and compare it to the manufacturer's specifications for display memory that is to be used.

# CL-GD7555 Application Alert: Changes to Support for DRAM Configurations and Display Modes

***for the CL-GD7555 LCD/CRT Controller***

**Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application alert documents the changes that have been made to the DRAM configurations and display modes supported by the CL-GD7555 LCD/CRT controller.

**Applicability**

This document is intended to be used in conjunction with applicable CL-GD7555 documentation to aid the system designer.

This document applies to the following products:

✔ CL-GD7555 (all revisions)

**Related Documents**

– *CL-GD7555 Reference Manuals*

## 1. Introduction

This application alert discusses changes that have been made to: (1) the type of DRAM configurations that are supported for the display memory used with the CL-GD7555 and (2) the display modes that the CL-GD7555 supports.

## 2. DRAM Configurations

The CL-GD7555 supports both 1- and 2-Mbyte DRAM configurations for the display memory used with the CL-GD7555. Cirrus Logic does not support a 4-Mbyte DRAM configuration for display memory.

## 3. Display Modes

The attached pages document changes made to Chapter 4 of the *CL-GD7555 Hardware Reference Manual* since the publication of Version 1.1.

**Table 4-2. Cirrus Logic Extended VGA CRT-Only Display Modes** *(cont.)*

| Extended VGA Display Mode No. (hex) | VESA Display Mode No. (hex) | Color Depth (bits per pixel) | Characters × Rows | Character Cell (pixels) | Resolution (pixels) | Horizontal Freq. (kHz) | Vertical Freq. (Hz) | VCLK (MHz) | MCLK Minimum (MHz) | Required CVDD Voltage (Volts) |
|---|---|---|---|---|---|---|---|---|---|---|
| 66 | 110 | 32K‡ | – | – | 640 × 480 | 31.5 | 60 | 25 | 50 | 3.3 |
| | | | | | | 37.9 | 72 | 31.5 | 50 | 3.3 |
| | | | | | | 37.5 | 75 | 31.5 | 50 | 3.3 |
| | | | | | | 43.269 | 85 | 36 | 50 | 3.3 |
| 67 | 113 | 32K‡ | 128 x 48 | 8 × 16 | 800 × 600 | 35.2 | 56 | 36 | 50 | 3.3 |
| | | | | | | 37.8 | 60 | 40 | 50 | 3.3 |
| | | | | | | 48.1 | 72 | 50 | 50 | 3.3 |
| | | | | | | 47 | 75 | 49.5 | 50 | 3.3 |
| | | | | | | 53.674 | 85 | 56.25 | 50 | 3.3 |
| 68[a] | 116 | 32K‡ | 128 x 48 | 8 × 16 | 1024 × 768 | 35.5 | 43i | 44.9 | 50 | 3.3 |
| | | | | | | 48.2 | 60 | 65 | 50 | 3.3 |
| | | | | | | 56 | 70 | 75 | 60 | 3.3 |
| | | | | | | 60 | 75 | 78.7 | 60 | 3.3 |
| | | | | | | 68.677 | 85 | 94.5 | 80 | 5.0 |
| ~~69[b]~~ | ~~119~~ | ~~32K‡~~ | ~~160 x 64~~ | ~~8 x 16~~ | ~~1280 x 1024~~ | ~~48~~ | ~~43i~~ | ~~75~~ | ~~50~~ | ~~3.3~~ |
| 6C[a] | 106 | 16/256K | 160 × 64 | 8 × 16 | 1280 × 1024 | 48 | 43i | 75 | 50 | 3.3 |
| 6D[a] | 107 | 256/256K | 160 × 64 | 8 × 16 | 1280 × 1024 | 48 | 43i | 75 | 50 | 3.3 |
| | | | | | | 64 | 60 | 108 | 80 | 5.0 |
| 71 | 112 | 16M | 80 × 30 | 8 × 16 | 640 × 480 | 31.5 | 60 | 25 | 50 | 3.3 |
| | | | | | | 37.9 | 72 | 31.5 | 50 | 3.3 |
| | | | | | | 37.5 | 75 | 31.5 | 50 | 3.3 |
| | | | | | | 43.269 | 85 | 36 | 50 | 3.3 |
| 74[a] | 117 | 64K | 128 × 48 | 8 × 16 | 1024 × 768 | 35.5 | 43i | 44.9 | 50 | 3.3 |
| | | | | | | 48.3 | 60 | 65 | 50 | 3.3 |
| | | | | | | 56 | 70 | 75 | 60 | 3.3 |
| | | | | | | 60 | 75 | 78.7 | 60 | 3.3 |
| | | | | | | 68.677 | 85 | 94.5 | 80 | 5.0 |
| ~~75[b]~~ | ~~11A~~ | ~~64K~~ | ~~160 x 64~~ | ~~8 x 16~~ | ~~1280 x 1024~~ | ~~48~~ | ~~43i~~ | ~~75~~ | ~~60~~ | ~~3.3~~ |

**Table 4-2. Cirrus Logic Extended VGA CRT-Only Display Modes** *(cont.)*

| Extended VGA Display Mode No. (hex) | VESA Display Mode No. (hex) | Color Depth (bits per pixel) | Characters × Rows | Character Cell (pixels) | Resolution (pixels) | Horizontal Freq. (kHz) | Vertical Freq. (Hz) | VCLK (MHz) | MCLK Minimum (MHz) | Required CVDD Voltage (Volts) |
|---|---|---|---|---|---|---|---|---|---|---|
| 78[a] | 115 | 16M | 100 x 37 | 8 × 16 | 800 × 600 | 35.2 | 56 | 36 | 50 | 3.3 |
| | | | | | | 37.8 | 60 | 40 | 50 | 3.3 |
| | | | | | | 48.1 | 72 | 50 | 60 | 3.3 |
| | | | | | | 47 | 75 | 49.5 | 60 | 3.3 |
| | | | | | | 53.674 | 85 | 56.25 | 66 | 3.3 |
| ~~79[b]~~ | ~~118~~ | ~~16M~~ | ~~128 x 48~~ | ~~8 x 16~~ | ~~1024 x 768~~ | ~~35.5~~ | ~~43i~~ | ~~44.9~~ | ~~60~~ | ~~3.3~~ |
| | | | | | | ~~48.3~~ | ~~60~~ | ~~65~~ | ~~80~~ | ~~5.0~~ |
| | | | | | | ~~56~~ | ~~70~~ | ~~75~~ | ~~80~~ | ~~5.0~~ |

[a] A minimum of 2 Mbytes of display memory are required to support all of the capabilities of this display mode.

[b] ~~A minimum of 4 Mbytes of display memory are required to support all of the capabilities of this display mode.~~

### 4.2.2 Flat Panel-Only and SimulSCAN 800 x 600 (SVGA) Display Modes

For 800 x 600 flat panels, the Cirrus Logic VGA BIOS supports flat panel-only and SimulSCAN operations with the standard VGA display modes listed in Section 4.1 and the extended VGA display modes in Table 4-4.

- Within the table, the 'MCLK Minimum' column gives the recommended memory clock frequency at which the CL-GD7555 can run without adverse effects to functionality. Better benchmarks can be achieved with an MCLK frequency higher than the frequency specified.
- DSTN flat panels require display memory for frame accelerator functionality.
- On 800 x 600 flat panels, when expansion to 800 x 600 is disabled, display modes with resolutions less than 800 x 600 are displayed at a 640 x 480 resolution.
- For SimulSCAN operation with a CRT monitor and an 800 x 600 flat panel:
  - — Both the CRT monitor and the flat panel must be configured at a minimum to support the resolution of a given display mode during SimulSCAN operation.
  - — For the 800 x 600 flat panels, all resolutions use 800 x 600 timing. As a result, even if an 800 x 600 flat panel displays a 640 x 480 display mode, the SimulSCAN operation is not allowed when using a CRT monitor that is configured to a maximum resolution of 640 x 480.

**Table 4-4. Flat Panel-Only and SimulSCAN™ Display Modes for 800 x 600 Flat Panels**

| Extended VGA Display Mode No. (hex) | VESA Display Mode No. (hex) | Color Depth (bits per pixel) | Characters × Rows | Character Cell (pixels) | Resolution (pixels) | Expand from 640 × 480 to 800 × 600? | Type of Flat Panel | VCLK (MHz) | MCLK Minimum (MHz) | Required CVDD Voltage (Volts) |
|---|---|---|---|---|---|---|---|---|---|---|
| 58, 6A[a] | 102 | 16/256K | 100 × 37 | 8 × 16 | 800 × 600 | – | DSTN | 40 | 60 | 3.3 |
| | | | | | | | TFT | 40 | 50 | 3.3 |
| 5C | 103 | 256/256K | 100 × 37 | 8 × 16 | 800 × 600 | – | DSTN | 40 | 60 | 3.3 |
| | | | | | | | TFT | 40 | 50 | 3.3 |
| 5E | 100 | 256/256K | 80 × 25 | 8 × 16 | 640 × 400 | Yes | DSTN | 40 | 60 | 3.3 |
| | | | | | | | TFT | 40 | 50 | 3.3 |
| 5F | 101 | 256/256K | 80 × 30 | 8 × 16 | 640 × 480 | Yes | DSTN | 40 | 60 | 3.3 |
| | | | | | | | TFT | 40 | 50 | 3.3 |
| 64 | 111 | 64K | 80 × 30 | 8 × 16 | 640 × 480 | Yes | DSTN | 40 | 60 | 3.3 |
| | | | | | | | TFT | 40 | 50 | 3.3 |
| 65 | 114 | 64K | 100 × 37 | 8 × 16 | 800 × 600 | – | DSTN | 40 | 60 | 3.3 |
| | | | | | | | TFT | 40 | 50 | 3.3 |
| 66 | 110 | 32K[b] | 80 × 30 | 8 × 16 | 640 × 480 | Yes | DSTN | 40 | 60 | 3.3 |
| | | | | | | | TFT | 40 | 50 | 3.3 |
| 67 | 113 | 32K[b] | 100 × 37 | 8 × 16 | 800 × 600 | – | DSTN | 40 | 60 | 3.3 |
| | | | | | | | TFT | 40 | 50 | 3.3 |
| 71 | 112 | 16M | 80 × 30 | 8 × 16 | 640 × 480 | Yes | DSTN | 40 | 66 | 3.3 |
| | | | | | | | TFT | 40 | 50 | 3.3 |
| 78[c] | 115 | 16M | 100 × 37 | 8 × 16 | 800 × 600 | – | DSTN | 40 | 66 | 3.3 |
| | | | | | | | TFT | 40 | 50 | 3.3 |

[a] Graphics display mode 6Ah must be used, rather than graphics display mode 58h, for application programs to retain compatibility with other VGA BIOS products.

[b] This display mode is 32K direct-color packed-pixel.

[c] A minimum of 2 Mbytes of display memory are required to support all the capabilities of this display mode.

### 4.2.3 Flat Panel-Only and SimulSCAN 1024 x 768 (XGA) Display Modes

For 1024 x 768 flat panels, the Cirrus Logic VGA BIOS supports flat panel-only and SimulSCAN operations with the standard VGA display modes listed in Section 4-1 and the extended VGA display modes in Table 4-5.

- Within the table, the 'MCLK Minimum' column gives the recommended memory clock frequency at which the CL-GD7555 can run without adverse effects to functionality. Better benchmarks can be achieved with an MCLK frequency higher than the frequency specified.
- Graphics display mode 6Ah must be used, rather than graphics display mode 58h, for application programs to retain compatibility with other VGA BIOS products.
- For SimulSCAN operation with 1024 x 768 panels, both the CRT monitor and the flat panel must be configured at a minimum to support the resolution of a given display mode during SimulSCAN operation.

**Table 4-5. Flat Panel-Only and SimulSCAN Display Modes for 1024 x 768 Flat Panels**

| Extended VGA Display Mode Number (hex) | VESA Display Mode Number (hex) | Color Depth (bits per pixel) | Characters × Rows | Character Cell (pixels) | Resolution (pixels) | Expand from 640 × 480 to 800 × 600? | Type of Flat Panel | VCLK (MHz) | MCLK Minimum (MHz) | Required CVDD Voltage (Volts) |
|---|---|---|---|---|---|---|---|---|---|---|
| 58, 6A[a] | 102 | 16/256K | 100 × 37 | 8 × 16 | 800 × 600 | – | TFT | 65 | 50 | 3.3 |
| 5C | 103 | 256/256K | 100 × 37 | 8 × 16 | 800 × 600 | – | TFT | 65 | 50 | 3.3 |
| 5D | 104 | 16/256K | 128 × 48 | 8 × 16 | 1024 × 768 | – | TFT | 65 | 50 | 3.3 |
| 5E | 100 | 256/256K | 80 × 25 | 8 × 16 | 640 × 400 | Yes | TFT | 65 | 50 | 3.3 |
| 5F | 101 | 256/256K | 80 × 30 | 8 × 16 | 640 × 480 | Yes | TFT | 65 | 50 | 3.3 |
| 60 | 105 | 256/256K | 128 × 48 | 8 × 16 | 1024 × 768 | – | TFT | 65 | 50 | 3.3 |
| 64 | 111 | 64K | 80 × 30 | 8 × 16 | 640 × 480 | Yes | TFT | 65 | 50 | 3.3 |
| 65 | 114 | 64K | 100 × 37 | 8 × 16 | 800 × 600 | – | TFT | 65 | 50 | 3.3 |
| 66 | 110 | 32K[b] | 80 × 30 | 8 × 16 | 640 × 480 | Yes | TFT | 65 | 50 | 3.3 |
| 67 | 113 | 32K[b] | 100 × 37 | 8 × 16 | 800 × 600 | – | TFT | 65 | 50 | 3.3 |
| 68 | 116 | 32K[b] | 128 × 48 | 8 × 16 | 1024 × 768 | – | TFT | 65 | 50 | 3.3 |
| 71 | 112 | 16M | 80 × 30 | 8 × 16 | 640 × 480 | Yes | TFT | 65 | 50 | 3.3 |
| 74 | 117 | 64K | 128 × 48 | 8 × 16 | 1024 × 768 | – | TFT | 65 | 50 | 3.3 |
| 78[c] | 115 | 16M | 100 × 37 | 8 × 16 | 800 × 600 | – | TFT | 65 | 50 | 3.3 |
| ~~79~~ | ~~118~~ | ~~16M~~ | ~~128 × 48~~ | ~~8 × 16~~ | ~~1024 × 768~~ | – | ~~TFT~~ | ~~65~~ | ~~80~~ | ~~5.0~~ |

[a] Graphics display mode 6Ah must be used, rather than graphics display mode 58h, for application programs to retain compatibility with other VGA BIOS products.

[b] This display mode is 32K direct-color packed-pixel.

[c] A minimum of 2 Mbytes of display memory are required to support all the capabilities of this display mode.

# Programming the LCD Power-Sequencing Time Delay

***for the CL-GD7555 LCD/CRT Controller***

**Graphics Company - Portable Graphics Group**
**Cirrus Logic, Inc.**

**Scope**

This application alert presents information not found in previous documentation for the CL-GD7555 LCD/CRT controller.

**Applicability**

This document is intended to be used in conjunction with applicable CL-GD7555 documentation to aid the system designer.

This document applies to the following products:

✔ CL-GD7555

**Related Documents**

– *CL-GD7555 Reference Manuals*

## 1. Introduction

This application alert identifies a restriction that applies to programming the CL-GD7555 LCD power-sequencing time delays.

## 2. Statement of Issue

Currently, the CL-GD7555 meets various panel power-sequencing requirements as follows. By setting Extension register CR8C to different values, corresponding LCD power-sequencing delays result. (Refer to Figure 1 and Table 1.) The Cirrus Logic VGA BIOS sets the default power-sequencing time delays to 32 ms between all signals (that is, CR8C[7:0] = 00h).

However, there is one restriction in programming the timing delays. All the delay settings between the different power sequencing signals must be set to the same value. For example, all the different time delays ($t_{D1}$, $t_{D2}$, $t_{D3}$, $t_{D4}$) must all be programmed to either 32 ms, 4 ms, 1 ms, or 256 ms. The time delays cannot be simultaneously set to different values.

## 3. Solution

Beginning with CL-GD7556 and all future products, all the different time delays ($t_{D1}$, $t_{D2}$, $t_{D3}$, $t_{D4}$) are to be individually programmable independent of each other to further increase design flexibility.

| *CR8C | | Settings for Extension Register CR8C | Delay Between Beginning of Specified Signals |
|---|---|---|---|
| [7] | [6] | | |
| [5] | [4] | | |
| [3] | [2] | | |
| [1] | [0] | | |
| 0 | 0 | CR8C[7:0]=00h | 32 ms |
| 0 | 1 | CR8C[7:0]=55h | 4 ms |
| 1 | 0 | CR8C[7:0]=AAh | 1 ms |
| 1 | 1 | CR8C[7:0]=FFh | 256 ms |

**Table 1. Register CR8C**

**Note: *CR8C[7:6], CR8C[5:4], CR8C[3:2], and CR8C[1:0] must all be set to same values.**

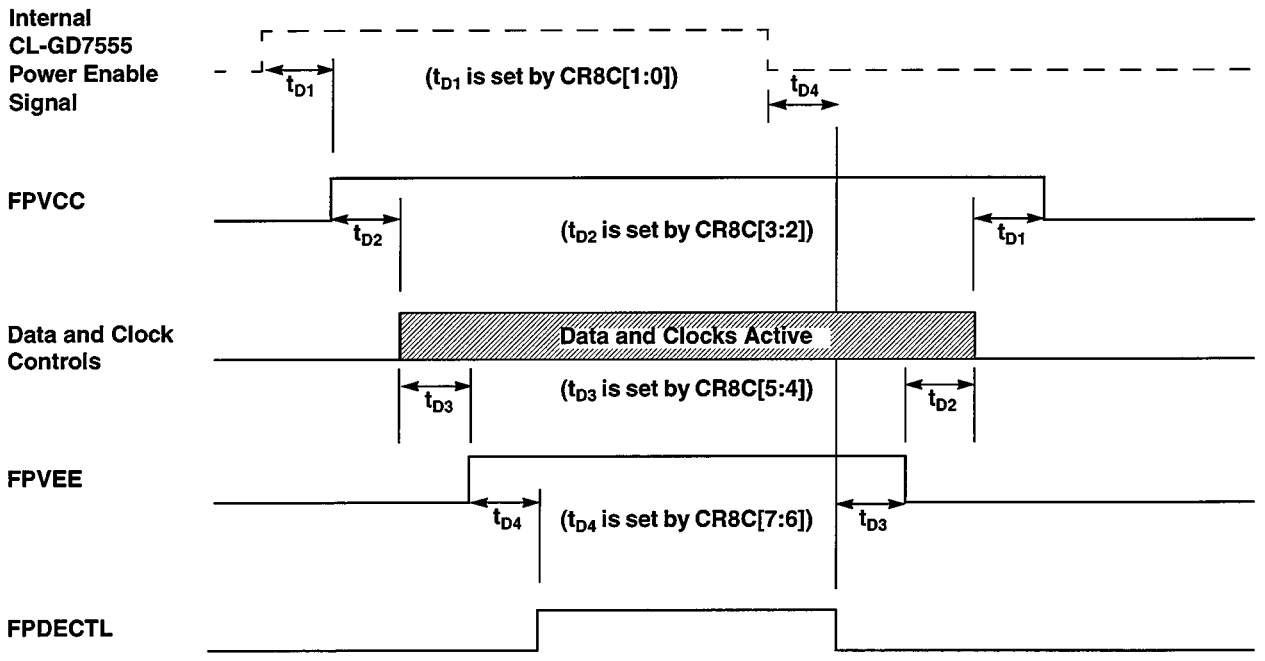



**Figure 1. Flat Panel Power-Up and Power-Down Delay Settings**

# Errata Note

***for the CL-GD7555-CF LCD/CRT Controller***

**Portable Graphics Group**
**Graphics Company**
**Cirrus Logic, Inc.**

***CIRRUS LOGIC CONFIDENTIAL!***

**Scope and Applicability**

This note presents errata for the Cirrus Logic CL-GD7555-CF LCD/CRT controller. This document contains information that is of a confidential nature and is not to be reproduced, copied, or redistributed in any manner.

**Related Documents**

– *CL-GD7555 Reference Manuals*

| | |
|---|---|
| Product described: | CL-GD7555-CF |
| Errata revision:: | 1.00 |
| Supersedes : | None |
| Date: | January 10, 1997 |
| Page count: | 4 |

The following is the list of known deviations of the CL-GD7555-CF from its design specification, as of the date of the publication of this document.

# 1. Video Window Issues

## 1.1 Video Window Artifacts in 1024 x 768 Display Modes

Issue: When the following are true:

- CVDD is +3.00 V
- The temperature of the chip case is 90° C
- The VCLK frequency is at 65 MHz

Then: Artifacts such as flashing lines or repeating video data appear inside the video window.

Remedy: To secure the operational margin, in a 1024 × 768 non-interlaced display mode, reduce the VCLK to 62 MHz. As a result, the vertical refresh rate is set to 59 Hz.

**NOTE:** The operating voltages of the CL-GD7555 are as follows:

- For 3.3-V operation: +3.3 V ± 0.15V
- For +5.0-V operation: +5.0V ± 0.25V

## 1.2 Video Window Noise Caused by Vertical Interpolation Failure

Issue: When the CVDD is less than 3.6 V and VCLK frequency is 65 MHz, vertical interpolation fails, which causes noise (that is, horizontal lines) within a video window.

Remedy: When the CVDD is +3.3 V ± 0.15V and the VCLK frequency is higher than 52 MHz, vertical interpolation is disabled by the Cirrus Logic video driver.

# 2. PCI Clock Rate Reduction Issues

Issue: When the PCI clock frequency is set to less than 30% of MCLK frequency, then a host CPU write to display memory can cause a system to lock up, even when Extension register bit SR23[5] is set to 1. (This lockup also occurs on the CL-GD7555 revision CE.)

Remedy: Before reducing the PCI clock frequency, Extension register bit SRF[6] must first be set to 1.

# Errata Note

***for the CL-GD7556-AB LCD/CRT Controller***

**Portable Graphics Group**
**Graphics Company**
**Cirrus Logic, Inc.**

***CIRRUS LOGIC CONFIDENTIAL!***

**Scope and Applicability**

This note presents errata for the Cirrus Logic CL-GD7556-AB LCD/CRT controller. This document contains information that is of a confidential nature and is not to be reproduced, copied, or redistributed in any manner.

**Related Documents**

– *CL-GD7556 Reference Manuals*

| | |
|---|---|
| Product described: | CL-GD7556-AB |
| Errata revision: | 1.01 |
| Supersedes : | None |
| Date: | March 3, 1997 |
| Page count: | 4 |

The following is the list of known deviations of the CL-GD7556-AB from its design specification, as of the date of the publication of this document.

# 1. Hardware Configuration Issues

## 1.1 Issue 1: Both Pull-Down and Pull-Up Resistors Must Be Used for Hardware Configuration

Issue: To configure the CL-GD7556-AB hardware configuration pins (including the panel type switch pins), as necessary connect the configuration pins to either pull-down resistors ranging from 4.7K to 6.8K Ω or pull-up resistors ranging from 10K to 20K Ω. (The pull-up resistors in the input pads necessitate the use of the pull-down resistors.) When:

- A pull-down resistor is connected, the configuration pin reads 0.
- A pull-up resistor is connected, the configuration pin reads 1.

Remedy: As required for a particular configuration of the CL-GD7556-AB, connect a pull-down or a pull-up resistor to each appropriate CL-GD7556-AB hardware configuration pin.

In the next revision of the CL-GD7556 silicon, the pull-up resistors in the CL-GD7556 inputs pads are to be removed. With this fix, only pull-up resistors need be connected as required.

## 1.2 Issue 2: Errors in Interpretting the PCI Demonstration Board Hardware Configuration Table

Issue: Because of the pull-up resistors that already exist in the inputs pads of the CL-GD7556-AB chip, these Cirrus Logic PCI Demonstration Boards have been reworked:

- GDB 7555X-E-DM1-1
- GDB 7555X-A-DM2-1

The rework to the Demonstration Boards has resulted in errors in interpretting the hardware configuration table that appears on the back of the Demonstration Boards.

Remedy: When using the CL-GD7556-AB with the PCI Demonstration Board, interpret the hardware configuration table as follows:

- 1 = Open (or OFF)
- 0 = Closed (or ON)

In the next revision of the CL-GD7556 silicon, the pull-up resistors in the CL-GD7556 inputs pads are to be removed.

**NOTE:** When the CL-GD7556 silicon is fixed, the Demonstration Boards must have the above-mentioned rework removed. Furthermore, the interpretation of the hardware configuration table is to revert to the original interpretation (that is, 1 = Closed and 0 = Open).

## 2. High Suspend-Mode Current

Issue: The suspend-mode current is approximately 15 mA. The cause of this high suspend-mode current is the pull-ups in the input pads described above.

Remedy: In the next revision of the CL-GD7556 silicon, the pull-up resistors in the CL-GD7556 inputs pads are to be removed. With this fix, the suspend current decreases to approximately 500 uA.

## 3. V-Port Memory Write Error

Issue: Vertical lines appear inside the video window when both the following are true:

- MCLK is approximately 80 MHz.
- Video data are fed from the V-Port to the video window.

These unwanted vertical lines are caused by memory write errors in the V-Port operation.

Remedy: To eliminate the vertical lines when using the CL-GD7556-AB silicon, MCLK must be decreased to approximately 75 MHz. In the next revision of the CL-GD7556 silicon, this issue is to be fixed.

## 4. Improper Vertical Timing Control for On-Chip TV-Out

Issue: An unstable image on a TV-type display device occurs as a result of both the vertical blanking control and the vertical synchronization control not being properly implemented in the CL-GD7556 on-chip TV-Out circuitry.

Remedy: None at the present. The impact of this artifact is minimal. In the next revision of the CL-GD7556 silicon, this issue is to be fixed.

## 5. ESD Fails on Two Pins

Issue: The electro-static discharge test fails on the these two pins: the RESET# pin (pin 55) and the VREF pin (pin 115). These pins fail as follows:

- ESD test fails at 50 V in the machine model. (The specification is 200 V.)
- ESD test fails at 1.5 V in the human body model. (The specification is 2000 V.)

Remedy: None at the present. In the next revision of the CL-GD7556 silicon, this issue is to be fixed.

## 6. PCI Clock Rate Reduction Issues

Issue: When the PCI clock frequency is set to less than 30% of MCLK frequency, then a host CPU write to display memory can cause a system to lock up, even when Extension register bit SR23[5] is set to 1. (This lockup also occurs on CL-GD7555 revision CE and CF.)

Remedy: Before reducing the PCI clock frequency, Extension register bit SRF[6] must first be set to 1.

# Errata Note

***for the CL-GD7556-AC LCD/CRT Controller***

**Portable Graphics Group**
**Graphics Company**
**Cirrus Logic, Inc.**

***CIRRUS LOGIC CONFIDENTIAL!***

**Scope and Applicability**

This note presents errata for the Cirrus Logic CL-GD7556-AC LCD/CRT controller. This document contains information that is of a confidential nature and is not to be reproduced, copied, or redistributed in any manner.

**Related Documents**

– *CL-GD7556 Reference Manuals*

| | |
|---|---|
| Product described: | CL-GD7556-AC |
| Errata revision: | 1.01 |
| Supersedes : | 1.0.0 (Errata Note CL-GD7556-AB) |
| Date: | March 3, 1997 |
| Page count: | 4 |

The following is the list of known deviations of the CL-GD7556-AC from its design specification, as of the date of the publication of this document.

## 1. Relatively High Suspend-Mode Current

Issue: The suspend-mode power consumption is approximately 6 mW. This value is about:

- 20% more than that of the CL-GD7555-CF at 5 V
- 2.5 times that of the CL-GD7555-CF at 3.3 V

Remedy: None at the present.

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P Pin #'s | CL-GD755x Pin #'s | CL-GD755x Pin Name | CL-GD755x Description | FPD LHD 102T-10 640 x 480 C16MSS-24 | Hitachi LMG 5278 XUFC 640 x 480 M2DD-8 | Hitachi LMG 9600 ZWCC 800 x 600 C8DD-16 | Hitachi LMG 9720 XUFC 640 x 480 C8DD-8 | Hitachi LMG 9721 XUFC 640 x 480 C8DD-16 |
|---|---|---|---|---|---|---|---|---|
| 1 | 159 | FP2 | Data | B4 (Pin 31) | LD0 (p12) | LD0 (CN2-pin 16) | LD0 (CN1-pin 12) | LD0 (CN1-pin 12) |
| 2 | 160 | FP3 | Data | B5 (Pin 30) | LD1 (p13) | LD1 (CN2-pin 17) | LD1 (CN1-pin 13) | LD1 (CN1-pin 13) |
| 3 | 161 | FP4 | Data | B6 (Pin 29) | LD2 (p14) | LD2 (CN2-pin 18) | LD2 (CN1-pin 14) | LD2 (CN1-pin 14) |
| 4 | 162 | FP5 | Data | B7 (Pin 28) | LD3 (p15) | LD3 (CN2-pin 19) | LD3 (CN1-pin 15) | LD3 (CN1-pin 15) |
| 5 | 166 | FP8 | Data | G4 (Pin 21) | UD0 (p8) | LD4 (CN2-pin 20) | UD0 (CN1-pin 8) | LD4 (CN2-pin 6) |
| 6 | 167 | FP9 | Data | G5 (Pin 20) | UD1 (p9) | LD5 (CN2-pin 21) | UD1 (CN1-pin 9) | LD5 (CN2-pin 7) |
| 7 | 168 | FP10 | Data | G6 (Pin 19) | UD2 (p10) | LD6 (CN2-pin 22) | UD2 (CN1-pin 10) | LD6 (CN2-pin 8) |
| 8 | 169 | FP11 | Data | G7 (Pin 28) | UD3 (p11) | LD7 (CN2-pin 23) | UD3 (CN1-pin 11) | LD7 (CN2-pin 9) |
| 9 | 172 | FP13 | Data | R3 (Pin 13) | | UD7 (CN1-pin 15) | | UD7 (CN2-pin 4) |
| 10 | 170 | FP12 | Data | R2 (Pin 14) | | UD6 (CN1-pin 14) | | UD6 (CN2-pin 3) |
| 11 | 164 | FP7 | Data | G3 (Pin 23) | | UD5 (CN1-pin 13) | | UD5 (CN2-pin 2) |
| 12 | 163 | FP6 | Data | G2 (Pin 24) | | UD4 (CN1-pin 12) | | UD4 (CN2-pin 1) |
| 13 | 176 | FP17 | Data | R7 (Pin 8) | | UD3 (CN1-pin 11) | | UD3 (CN1-pin 11) |
| 14 | 175 | FP16 | Data | R6 (Pin 9) | | UD2 (CN1-pin 10) | | UD2 (CN1-pin 10) |
| 15 | 174 | FP15 | Data | R5 (Pin 10) | | UD1 (CN1-pin 9) | | UD1 (CN1-pin 9) |
| 16 | 173 | FP14 | Data | R4 (Pin 11) | | UD0 (CN1-pin 8) | | UD0 (CN1-pin 8) |
| 18 | 155 | FPVDCLK | Shift Clock | CLK (Pin 2) | CP (pin 3) | CL2 (CN1-pin 6) | CL2 (CN1-pin 3) | CL2 (CN1-pin 3) |
| 20 | 131 | FP18 | Data | G1 (Pin 25) | | | | |
| 22 | 156 | LFS | Frame Clock | FLM (Pin 4) | FRAME (pin 1) | FLM (CN1-pin 1) | FLM (CN1-pin 1) | FLM (CN1-pin 1) |
| 23 | 158 | FP1 | Data | B3 (Pin 33) | | | | |
| 24 | | | *Spare* | B0 (Pin 36) | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | |
| 26 | 152 | FPDE | Display Enable | ENAB (Pin 43) | | | | |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | |
| 28 | - | VEE | Switched NEG | | | | | |
| 29 | 132 | FP19 | Data | G0 (Pin 26) | | | | |
| 30 | - | VBB | Switched POS | | | | | |
| 31 | - | VBKLT | Backlight (+12) | Backlight | Backlight | Backlight | Backlight | Backlight |
| 32 | - | SWVDD | Switched Logic | +5V (P 38, 39, 40), 8/4 (P 46), ENABL/LPN (P 48) | VDD (pin 5) | VDD (CN2 -pin 24) | VDD (CN1-pin 5) | VDD (CN1-pin 5) |
| 33 | 146 | FP31 | Data | | | | | |
| 35 | 153 | LLCLK | Line clock | LP (Pin 4) | LOAD (pin 2) | CL1 (CN1-pin 4) | CL1 (CN1-pin 2) | CL1 (CN1-pin 2) |
| 37 | 123 | FPVEE | VEE Enable | DE (Pin 50) | DISP.OFF* (pin 4) | DISP.OFF (CN1-Pin 3) | DISP.OFF (CN1-Pin 4) | DISP.OFF (CN1-Pin 4) |
| 38 | 125 | FPVCC | VCC Enable | | | | | |
| 39 | 157 | FP0 | Data | B2 (Pin 34) | | | | |
| 40 | - | CONTPOS | Switched + Contrast | | | VLCD (CN2-pins 27,28,29) | VEE (CN1-pin 7) | VEE (CN1-pin 7) |
| 41 | - | CONTNEG | Switched - Contrast | | VEE (pin 7) | | | |
| 42 | 139 | FP25 | Data | R0 (Pin 16) | | | | |
| 43 | 145 | FP30 | Data | B1 (Pin 35) | | | | |
| 44 | 138 | FP24 | Data | R1 (Pin 15) | | | | |
| 17,19,21,34,36 | - | Ground | | GND (Pins 1, 3, 5, 7, 12, 17, 22, 27, 37) | VSS (pin 6) | VSS (CN1-pin 5, 7) | VSS (CN1-pin 6) | VSS (CN1-pin 6) |
| (16 Pin) 1 & 16 | - | Ground | | GND (P 41, 42, 44, 45, 47, 51) | | VSS (CN2-pins 25 & 26) | | VSS (CN2-pins 5 & 10) |
| 2 | 133 | FP20 | Data 133 | | | | | |
| 3 | 135 | FP21 | Data 135 | | | | | |
| 4 | 136 | FP22 | Data 136 | | | | | |
| 5 | 137 | FP23 | Data 137 | | | | | |
| 6 | 140 | FP26 | Data 140 | | | | | |
| 7 | 141 | FP27 | Data 141 | | | | | |
| 9 | 143 | FP28 | Data 143 | | | | | |
| 10 | 144 | FP29 | Data 144 | | | | | |
| 11 | 147 | FP32 | Data 147 | | | | | |
| 12 | 148 | FP33 | Data 148 | | | | | |
| 13 | 149 | FP34 | Data 149 | | | | | |
| 14 | 150 | FP35 | Data 150 | | | | | |
| 8 | - | Unused | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | N/A | "-22 VDC" | "+ 31 VDC" | "+ 31 VDC" | "+ 31 VDC" |
| Notes ? | | | | NO | NO | NO | NO | NO |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P | CL-GD755x | | | Hitachi | Hitachi | Hitachi | Hitachi |
|---|---|---|---|---|---|---|---|
| | | | | LMG 9821 XUCC-2 | LMG 9900 ZWCC | TX 24D55 VC1CAA | TM 26D50 VC2AA |
| | | | | 640 x 480 | 800 x 600 | 640 x 480 | 640 x 480 |
| Pin #'s | Pin #'s | Pin Name | Description | C8DD-16 | C8DD-16 | C512SS-9 | C512SS-9 |
| 1 | 159 | FP2 | Data | LD0 (CN2-pin 2) | DL0 (pin 11) | B0 (pin 13) | |
| 2 | 160 | FP3 | Data | LD1 (CN2-pin 3) | DL1 (pin 13) | B1 (pin 12) | B1 (pin 12) |
| 3 | 161 | FP4 | Data | LD2 (CN2-pin 4) | DL2 (pin 17) | B2 (pin 11) | B2 (pin 11) |
| 4 | 162 | FP5 | Data | LD3 (CN2-pin 5) | DL3 (pin 19) | B3 (pin 10) | B3 (pin 10) |
| 5 | 166 | FP8 | Data | LD4 (CN2-pin 6) | DL4 (pin 1) | G0 (pin 9) | |
| 6 | 167 | FP9 | Data | LD5 (CN2-pin 7) | DL5 (pin 3) | G1 (pin 8) | G1 (pin 8) |
| 7 | 168 | FP10 | Data | LD6 (CN2-pin 8) | DL6 (pin 5) | G2 (pin 7) | G2 (pin 7) |
| 8 | 169 | FP11 | Data | LD7 (CN2-pin 9) | DL7 (pin 7) | G3 (pin 6) | G3 (pin 6) |
| 9 | 172 | FP13 | Data | UD7 (CN1-pin 15) | DU7 (pin 31) | | |
| 10 | 170 | FP12 | Data | UD6 (CN1-pin 14) | DU6 (pin 29) | | |
| 11 | 164 | FP7 | Data | UD5 (CN1-pin 13) | DU5 (pin 25) | | |
| 12 | 163 | FP6 | Data | UD4 (CN1-pin 12) | DU4 (pin 23) | | |
| 13 | 176 | FP17 | Data | UD3 (CN1-pin 11) | DU3 (pin 22) | R3 (pin 2) | R3 (pin 2) |
| 14 | 175 | FP16 | Data | UD2 (CN1-pin 10) | DU2 (pin 24) | R2 (pin 3) | R2 (pin 3) |
| 15 | 174 | FP15 | Data | UD1 (CN1-pin 9) | DU1 (pin 26) | R1 (pin 4) | R1 (pin 4) |
| 16 | 173 | FP14 | Data | UD0 (CN1-pin 8) | DU0 (pin 28) | R0 (pin 5) | |
| 18 | 155 | FPVDCLK | Shift Clock | CL2 (CN1-pin 3) | XCK(pin 10) | DCLK (pin 15) | DCLK (pin 21) |
| 20 | 131 | FP18 | Data | | | | |
| 22 | 156 | LFS | Frame Clock | FLM (CN1-pin 1) | YD (pin 4) | VSYNC (pin 25) | VSYNC (pin 17) |
| 23 | 158 | FP1 | Data | | | | |
| 24 | | | *Spare* | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | |
| 26 | 152 | FPDE | Display Enable | | | DTMG (pin 23) | DTMG (pin 15) |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | |
| 28 | - | VEE | Switched NEG | | | | |
| 29 | 132 | FP19 | Data | | | | |
| 30 | - | VBB | Switched POS | | | | |
| 31 | - | VBKLT | Backlight (+12) | Backlight | Backlight | Backlight | Backlight |
| 32 | - | SWVDD | Switched Logic | VDD (CN1-pin 5) | VDD (pin 14 &16) | VDD (p 17 & 18),BLC (p 27),CCNT (p 26) | VDD (pin 23,24) BLC (pin 28) |
| 33 | 146 | FP31 | Data | | | | |
| 35 | 153 | LLCLK | Line clock | CL1 (CN1-pin 2) | LP (pin 6) | HSYNC (Pin 24) | HSYNC (pin 19) |
| 37 | 123 | FPVEE | VEE Enable | DISP.OFF (CN1-Pin 4) | DISP (pin 18) | | |
| 38 | 125 | FPVCC | VCC Enable | | | | |
| 39 | 157 | FP0 | Data | | | | |
| 40 | - | CONTPOS | Switched + Contrast | VEE (CN1-pin 7) | VCON (pin 12) aprox. ***2 VDC*** | | |
| 41 | - | CONTNEG | Switched - Contrast | | | VEE (pin 20 & 21) | Vee (pin 26,27) |
| 42 | 139 | FP25 | Data | | | | |
| 43 | 145 | FP30 | Data | | | | |
| 44 | 138 | FP24 | Data | | | | |
| 17,19,21,34,36 | - | Ground | | VSS (CN1-pin 6) | VSS (pins 2, 8, 9, 15, 21, 27, 30 ) | VSS (1,14,16,19, & 22) | D0TE(pin 29), HREV(pin 14) |
| (16 Pin) 1 & 16 | - | Ground | | VSS (CN2-pins 1 & 10) | | | VSS (pins 1,16,18,20,22,25) |
| 2 | 133 | FP20 | Data 133 | | | | |
| 3 | 135 | FP21 | Data 135 | | | | |
| 4 | 136 | FP22 | Data 136 | | | | |
| 5 | 137 | FP23 | Data 137 | | | | |
| 6 | 140 | FP26 | Data 140 | | | | |
| 7 | 141 | FP27 | Data 141 | | | | |
| 9 | 143 | FP28 | Data 143 | | | | |
| 10 | 144 | FP29 | Data 144 | | | | |
| 11 | 147 | FP32 | Data 147 | | | | |
| 12 | 148 | FP33 | Data 148 | | | | |
| 13 | 149 | FP34 | Data 149 | | | | |
| 14 | 150 | FP35 | Data 150 | | | | |
| 8 | - | Unused | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | "+ 31 VDC" | -2.0 VDC ***(Use 10M and 1M resistor on VCON)*** | "-24 VDC" | "-24 VDC" |
| Notes ? | | | | NO | **PVDD = 3.3 or 5 VDC** | NO | NO |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P Pin #'s | CL-GD755x Pin #'s | Pin Name | Description | Hitachi TX 26D60 VC1CAA 640 x 480 C256KSS-18 | Hitachi TX 26D80 VC1CAA 800 x 600 C256KSS-18 | Hitachi TX 30D01 VC1CAA 800 x 600 C256KSS-18 | IBM F 8534 800 x 600 C256KSS-18 |
|---|---|---|---|---|---|---|---|
| 1 | 159 | FP2 | Data | B2 (pin 22) | B2 (pin 31) | B2 (pin 31) | +BLUE2 (pin 6) |
| 2 | 160 | FP3 | Data | B3 (pin 23) | B3 (pin 33) | B3 (pin 33) | +BLUE3 (pin 4) |
| 3 | 161 | FP4 | Data | B4 (pin 24) | B4 (pin 34) | B4 (pin 34) | +BLUE4 (pin 3) |
| 4 | 162 | FP5 | Data | B5 (pin 25) | B5 (pin 35) | B5 (pin 35) | +BLUE5 (pin 2) |
| 5 | 166 | FP8 | Data | G2 (pin 15) | G2 (pin 21) | G2 (pin 21) | +GREEN2 (pin 14) |
| 6 | 167 | FP9 | Data | G3 (pin 16) | G3 (pin 23) | G3 (pin 23) | +GREEN3 (pin 12) |
| 7 | 168 | FP10 | Data | G4 (pin 17) | G4 (pin 24) | G4 (pin 24) | +GREEN4 (pin 11) |
| 8 | 169 | FP11 | Data | G5 (pin 18) | G5 (pin 25) | G5 (pin 25) | +GREEN5 (pin 10) |
| 9 | 172 | FP13 | Data | R1 (pin 7) | R1 (pin10) | R1 (pin10) | +RED1 (pin23) |
| 10 | 170 | FP12 | Data | R0 (pin 6) | R0 (pin 9) | R0 (pin 9) | +RED0 (pin 24) |
| 11 | 164 | FP7 | Data | G1 (pin 14) | G1 (pin 20) | G1 (pin 20) | +GREEN1 (pin 15) |
| 12 | 163 | FP6 | Data | G0 (pin 13) | G0 (pin 19) | G0 (pin 19) | +GREEN0 (pin 16) |
| 13 | 176 | FP17 | Data | R5 (pin 11) | R5 (pin 15) | R5 (pin 15) | +RED5 (pin 18) |
| 14 | 175 | FP16 | Data | R4 (pin 10) | R4 (pin 14) | R4 (pin 14) | +RED4 (pin 19) |
| 15 | 174 | FP15 | Data | R3 (pin 9) | R3 (pin 13) | R3 (pin 13) | +RED3 (pin 20) |
| 16 | 173 | FP14 | Data | R2 (pin 8) | R2 (pin 11) | R2 (pin 11) | +RED2 (pin 22) |
| 18 | 155 | FPVDCLK | Shift Clock | DCLK (pin 2) | DCLK (pin 2) | DCLK (pin 2) | -DTCLK (pin 26) |
| 20 | 131 | FP18 | Data | | | | |
| 22 | 156 | LFS | Frame Clock | VSYNC (pin 4) | VSYNC (pin 5) | VSYNC (pin 5) | VSYNC (pin 27) |
| 23 | 158 | FP1 | Data | B1 (pin 21) | B1 (pin 30) | B1 (pin 30) | +BLUE1 (pin 7) |
| 24 | | | *Spare* | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | |
| 26 | 152 | FPDE | Display Enable | DTMG (pin 27) | DTMG (pin 37) | DTMG (pin 37) | +DSPTMG (pin 28) |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | |
| 28 | - | VEE | Switched NEG | | | | |
| 29 | 132 | FP19 | Data | | | | |
| 30 | - | VBB | Switched POS | | | | |
| 31 | - | VBKLT | Backlight (+12) | Backlight | Backlight | Backlight | Backlight |
| 32 | - | SWVDD | Switched Logic | VDD (pin 28, 29, & 30) | VDD (pins 39, & 40) | VDD (pins 39, & 40) **3.3VDC** | VDD (pins 29, & 30) **5.0 Volts** |
| 33 | 146 | FP31 | Data | | | | |
| 35 | 153 | LLCLK | Line clock | HSYNC (Pin 3) | HSYNC (Pin 4) | HSYNC (Pin 4) | HSYNC (Pin 26) |
| 37 | 123 | FPVEE | VEE Enable | | | | |
| 38 | 125 | FPVCC | VCC Enable | | | | |
| 39 | 157 | FP0 | Data | B0 (pin 20) | B0 (pin 29) | B0 (pin 29) | +BLUE0 (pin 8) |
| 40 | - | CONTPOS | Switched + Contrast | | | | |
| 41 | - | CONTNEG | Switched - Contrast | | | | |
| 42 | 139 | FP25 | Data | | | | |
| 43 | 145 | FP30 | Data | | | | |
| 44 | 138 | FP24 | Data | | | | |
| 17,19,21,34,36 | - | Ground | | VSS (1, 5, 12, 19, & 26) | VSS (pins 1, 3, 6, 7, 8, 12, 15, 16, 17) | VSS (pins 1, 3, 6, 7, 8, 12, 15, 16, 17) | GND (pins 1, 5, 9, 13, 17, 21, 25) |
| (16 Pin) 1 & 16 | - | Ground | | | VSS (pins 18, 22, 26, 27, 28, 32, 36) | VSS (pins 18, 22, 26, 27, 28, 32, 36) | GND (pins 31, 23, 35, 37) |
| 2 | 133 | FP20 | Data 133 | | | | |
| 3 | 135 | FP21 | Data 135 | | | | |
| 4 | 136 | FP22 | Data 136 | | | | |
| 5 | 137 | FP23 | Data 137 | | | | |
| 6 | 140 | FP26 | Data 140 | | | | |
| 7 | 141 | FP27 | Data 141 | | | | |
| 9 | 143 | FP28 | Data 143 | | | | |
| 10 | 144 | FP29 | Data 144 | | | | |
| 11 | 147 | FP32 | Data 147 | | | | |
| 12 | 148 | FP33 | Data 148 | | | | |
| 13 | 149 | FP34 | Data 149 | | | | |
| 14 | 150 | FP35 | Data 150 | | | | |
| 8 | - | Unused | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | "+5 VDC" | "+5 VDC" | "+3.3 VDC" | "+5.0 AND +3.3 VDC" |
| Notes ? | | | | NO | NO | **PVDD = 3.3 Volts** | **V33 (Pins 33, 34) = 3.3 Volts** |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P | CL-GD755x | | | Kyocera | Kyocera | Matsushita | Mitsubishi | National / Panasonic |
|---|---|---|---|---|---|---|---|---|
| | | | | KCL 6448 HSTT-X1 | KCS 8060 BSTT | ED-M-1227 | AA 95 VA3D | EDM GPZ 3KCF |
| | | | | 640 x 480 | 800 x 600 | 640 x 480 | 640 x 480 | 640 x 480 |
| Pin #'s | Pin #'s | Pin Name | Description | C8DD-16 | C8DD-16 | M2DD-8 | C512SS-9 | C8DD-16 |
| 1 | 159 | FP2 | Data | LD0 (pin 16) | LD0 (CN2 - pin 1) | D0L (p12) | | DL0 (pin 11) |
| 2 | 160 | FP3 | Data | LD1 (pin 17) | LD1 (CN2 - pin 2) | D1L (p13) | B1 (DA10) | DL1 (pin 13) |
| 3 | 161 | FP4 | Data | LD2 (pin 18) | LD2 (CN2 - pin 3 | D2L (p14) | B2 (DA11) | DL2 (pin 17) |
| 4 | 162 | FP5 | Data | LD3 (pin 19) | LD3 (CN2 - pin 4) | D3L (p15) | B3 (DA12) | DL3 (pin 19) |
| 5 | 166 | FP8 | Data | LD4 (pin 20) | LD4 (CN2 - pin 5) | D0U (p8) | | DL4 (pin 1) |
| 6 | 167 | FP9 | Data | LD5 (pin 21) | LD5 (CN2 - pin 6) | D1U (p9) | G1 (DA6) | DL5 (pin 3) |
| 7 | 168 | FP10 | Data | LD6 (pin 22) | LD6 (CN2 - pin 7) | D2U (p 10) | G2 (DA7) | DL6 (pin 5) |
| 8 | 169 | FP11 | Data | LD7 (pin 23) | LD7 (CN2 - pin 8) | D3U (p11) | G3 (DA8) | DL7 (pin 7) |
| 9 | 172 | FP13 | Data | HD7 (pin 15) | HD7 (CN1- pin 15) | | | DU7 (pin 31) |
| 10 | 170 | FP12 | Data | HD6 (pin 14) | HD6 (CN1- pin 14) | | | DU6 (pin 29) |
| 11 | 164 | FP7 | Data | HD5 (pin 13) | HD5 (CN1- pin 13) | | | DU5 (pin 25) |
| 12 | 163 | FP6 | Data | HD4 (pin 12) | HD4 (CN1- pin 12) | | | DU4 (pin 23) |
| 13 | 176 | FP17 | Data | HD3 (pin 11) | HD3 (CN1- pin 11) | | R3 (DA4) | DU3 (pin 22) |
| 14 | 175 | FP16 | Data | HD2 (pin 10) | HD2 (CN1- pin 10) | | R2 (DA3) | DU2 (pin 24) |
| 15 | 174 | FP15 | Data | HD1 (pin 9) | HD1 (CN1- pin 9) | | R1 (DA2) | DU1 (pin 26) |
| 16 | 173 | FP14 | Data | HD0 (pin 8) | HD0 (CN1- pin 8) | | | DU0 (pin 28) |
| 18 | 155 | FPVDCLK | Shift Clock | CP (Pin 6) | CP (Cn1- Pin 6) | CPX (p 3) | DCLK (sp2) | CP (pin 10) |
| 20 | 131 | FP18 | Data | | | | | |
| 22 | 156 | LFS | Frame Clock | FRM (Pin 1) | FRM (CN1 - Pin 1) | FRM (p1) | VD (SP7) | FRM (pin 4) |
| 23 | 158 | FP1 | Data | DF (Pin 2) | DF (CN1 - Pin 2) | | | |
| 24 | | | *Spare* | | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | |
| 26 | 152 | FPDE | Display Enable | | | | DENA (SP6) | |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | |
| 28 | - | VEE | Switched NEG | | | | | |
| 29 | 132 | FP19 | Data | | | | | |
| 30 | - | VBB | Switched POS | VEE (Pins 27 & 28) | VEE (CN2 - Pins 12 & 13) | | | |
| 31 | - | VBKLT | Backlight (+12) | Backlight | Backlight | Backlight | Backlight | Backlight |
| 32 | - | SWVDD | Switched Logic | VDD (pin 24), BS (Pin 26) | VDD (CN2 - pin 9) | VDD (p 4) | VDD1 (SP8,9) | VDD (pin 14 &16) |
| 33 | 146 | FP31 | Data | | | | | |
| 35 | 153 | LLCLK | Line clock | LOAD (pin 4) | LOAD (CN1 - pin 4) | LOAD (pin 2) | HD (SP4) | LOAD (pin 6) |
| 37 | 123 | FPVEE | VEE Enable | DISP (pin 3) | DISP (CN1 - pin 3) | | | DISPON (pin 18) |
| 38 | 125 | FPVCC | VCC Enable | | | | | |
| 39 | 157 | FP0 | Data | | | | | |
| 40 | - | CONTPOS | Switched + Contrast | VCONT (Pin 29) | VCONT (CN2 - Pin 14) | | | VCON (pin 12) ***2 VDC*** |
| 41 | - | CONTNEG | Switched - Contrast | | | VLCD (P 6) | | |
| 42 | 139 | FP25 | Data | | | | | |
| 43 | 145 | FP30 | Data | | | | | |
| 44 | 138 | FP24 | Data | | | | | |
| 17,19,21,34,36 | - | Ground | | VSS (pin 5, 7, & 25 ) | VSS (pin CN1 - Pins 5 & 7) | GND (p 5 & 7) | VSS (SP1, 3, 5, 10) | VSS (pins 2, 8, 9, 15, 21, 27, 30 ) |
| (16 Pin) 1 & 16 | - | Ground | | | VSS (pin CN2 - Pin 10) | | VSS (DA1,5,9,13,14,15) | |
| 2 | 133 | FP20 | Data 133 | | | | | |
| 3 | 135 | FP21 | Data 135 | | | | | |
| 4 | 136 | FP22 | Data 136 | | | | | |
| 5 | 137 | FP23 | Data 137 | | | | | |
| 6 | 140 | FP26 | Data 140 | | | | | |
| 7 | 141 | FP27 | Data 141 | | | | | |
| 9 | 143 | FP28 | Data 143 | | | | | |
| 10 | 144 | FP29 | Data 144 | | | | | |
| 11 | 147 | FP32 | Data 147 | | | | | |
| 12 | 148 | FP33 | Data 148 | | | | | |
| 13 | 149 | FP34 | Data 149 | | | | | |
| 14 | 150 | FP35 | Data 150 | | | | | |
| 8 | - | Unused | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | "+ 28 VDC" | "+ 37 VDC" | "-25 VDC" | "+5 VDC" | ***+2.0 VDC*** |
| Notes ? | | | | NO | NO | NO | NO | Use 10M and 1M resistor on VCON |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P | CL-GD755x | | | NEC | NEC | NEC | GENERIC | Optrex |
|---|---|---|---|---|---|---|---|---|
| | | | | NL 6448 AC20-02 (03) | NL 6448 AC30-03 (06, 10) | NL 8060 AC24-01 | | DMF-50081-NF |
| | | | | 640 x 480 | 640 x 480 | 800 x 600 | 1024 x 768 | 640 x 480 |
| Pin #'s | Pin #'s | Pin Name | Description | C4KSS-12 | C4KSS-12 | C4KSS-12 | C256KSS-(2x18)36 | M2SS-4 |
| 1 | 159 | FP2 | Data | B0 (pin 16) | B0 (pin 17) | B0 (pin 17) | BA2 | |
| 2 | 160 | FP3 | Data | B1 (pin 17) | B1 (pin 18) | B1 (pin 18) | BA3 | |
| 3 | 161 | FP4 | Data | B2 (pin 18) | B2 (pin 19) | B2 (pin 19) | BA4 | |
| 4 | 162 | FP5 | Data | B3 (pin 19) | B3 (pin 20) | B3 (pin 20) | BA5 | |
| 5 | 166 | FP8 | Data | G0 (pin 12) | G0 (pin 12) | G0 (pin 12) | GA2 | DU0 (pin 9) |
| 6 | 167 | FP9 | Data | G1 (pin 13) | G1 (pin 13) | G1 (pin 13) | GA3 | DU1 (pin 10) |
| 7 | 168 | FP10 | Data | G2 (pin 14) | G2 (pin 14) | G2 (pin 14) | GA4 | DU2 (pin 11) |
| 8 | 169 | FP11 | Data | G3 (pin 15) | G3 (pin 15) | G3 (pin 15) | GA5 | DU3 (pin 12) |
| 9 | 172 | FP13 | Data | | | | RA1 | |
| 10 | 170 | FP12 | Data | | | | RA0 | |
| 11 | 164 | FP7 | Data | | | | GA1 | |
| 12 | 163 | FP6 | Data | | | | GA0 | |
| 13 | 176 | FP17 | Data | R3 (pin 10) | R3 (pin 10) | R3 (pin 10) | RA5 | |
| 14 | 175 | FP16 | Data | R2 (pin 9) | R2 (pin 9) | R2 (pin 9) | RA4 | |
| 15 | 174 | FP15 | Data | R1 (pin 8) | R1 (pin 8) | R1 (pin 8) | RA3 | |
| 16 | 173 | FP14 | Data | R0 (pin 7) | R0 (pin 7) | R0 (pin 7) | RA2 | |
| 18 | 155 | FPVDCLK | Shift Clock | CLK (Pin 1) | CLK (Pin 1) | CLK (Pin 1) | CLK | CP (pin 3) |
| 20 | 131 | FP18 | Data | | | | BB0 | |
| 22 | 156 | LFS | Frame Clock | VSYNC (pin 5) | VSYNC (pin 5) | VSYNC (pin 5) | VSYNC | FLM (pin 1) |
| 23 | 158 | FP1 | Data | | | | BA1 | |
| 24 | | | *Spare* | | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | |
| 26 | 152 | FPDE | Display Enable | DE (Pin 25) | DE (Pin 31) | DE (Pin 31) | DE | |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | |
| 28 | - | VEE | Switched NEG | | | | | VEE (pin 8) |
| 29 | 132 | FP19 | Data | | | | BB1 | |
| 30 | - | VBB | Switched POS | | | | | |
| 31 | - | VBKLT | Backlight (+12) | | VDD (pins 26, 27) | VDD (pins 26, 27) | VDD | Backlight |
| 32 | - | SWVDD | Switched Logic | VCC (pin 24), MODE (pin 26) | VCC (P 22,23,25), MODE (P 32) | VCC (Pins 23,25), MODE (P 32) | VCC | VCC (pin 6) |
| 33 | 146 | FP31 | Data | | | | RB1 | |
| 35 | 153 | LLCLK | Line clock | HSYNC (pin 4) | HSYNC (pin 4) | HSYNC (pin 4) | HSYNC | LP (pin 2) |
| 37 | 123 | FPVEE | VEE Enable | BLOFFO (Pin 22) | BLOFFO (Pin 22) | BLOFFO (Pin 22) | | DISP_OFF (pin 13) |
| 38 | 125 | FPVCC | VCC Enable | | VCCONNO (Pin 33) | VCCONNO (Pin 33) | | |
| 39 | 157 | FP0 | Data | | | | BA0 | |
| 40 | - | CONTPOS | Switched + Contrast | | | | | |
| 41 | - | CONTNEG | Switched - Contrast | | | | | VADJ (pin 5) |
| 42 | 139 | FP25 | Data | | | | GB1 | |
| 43 | 145 | FP30 | Data | | | | RB0 | |
| 44 | 138 | FP24 | Data | | | | GB0 | |
| 17,19,21,34,36 | - | Ground | | GND (pins 2,3,6,11,20,23,28,29) | GND (pins 2,3,6,11,16,21) | GND (pins 2,3,6,11,16,21) | All GND Pins (see panel spec.) | VSS (pin 7) |
| (16 Pin) 1 & 16 | - | Ground | | ACA (Pin 21) | GND (pins 24,29,30,34) | GND (pins 24,29,30,34) | | |
| 2 | 133 | FP20 | Data 133 | | | | GB4 | |
| 3 | 135 | FP21 | Data 135 | | | | BB2 | |
| 4 | 136 | FP22 | Data 136 | | | | GB5 | |
| 5 | 137 | FP23 | Data 137 | | | | BB3 | |
| 6 | 140 | FP26 | Data 140 | | | | RB2 | |
| 7 | 141 | FP27 | Data 141 | | | | BB4 | |
| 9 | 143 | FP28 | Data 143 | | | | RB3 | |
| 10 | 144 | FP29 | Data 144 | | | | BB5 | |
| 11 | 147 | FP32 | Data 147 | | | | RB4 | |
| 12 | 148 | FP33 | Data 148 | | | | GB2 | |
| 13 | 149 | FP34 | Data 149 | | | | RB5 | |
| 14 | 150 | FP35 | Data 150 | | | | GB3 | |
| 8 | - | Unused | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | N/A | N/A | N/A | N/A | "-25 VDC" |
| Notes ? | | | | NO | NO | NO | See App Note 754x-AN-8 | NO |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P | CL-GD755x | | | Optrex | Optrex | Samsung | Samsung | Samsung | Samsung |
|---|---|---|---|---|---|---|---|---|---|
| | | | | DMF-50383-NF | DMF-50414-NCU-FW | LT 094 V1-X0S (X1S) | LT 094 V3-X0S | LT 104 S1 | LT 104 V3 |
| | | | | 640 x 480 | 640 x 480 | 640 x 480 | 640 x 480 | 800 x 600 | 640 x 480 |
| Pin #'s | Pin #'s | Pin Name | Description | M2DD-8 | C8DD-16 bit | C512SS-9 | C4KSS-12 | C256KSS-18 | C256KSS-18 |
| 1 | 159 | FP2 | Data | DL0 (pin 12) | DL0 (pin 17) | | B0 (pin 19) | B2 (pin 31) | B2 (Pin 22) |
| 2 | 160 | FP3 | Data | DL1 (pin 13) | DL1 (pin 18) | B0 (CN1-Pin 13) | B1 (pin 20) | B3 (pin 33) | B3 (Pin 23) |
| 3 | 161 | FP4 | Data | DL2 (pin 14) | DL2 (pin 19) | B1 (CN1-Pin 14) | B2 (pin 21) | B4 (pin 34) | B4 (Pin 24) |
| 4 | 162 | FP5 | Data | DL3 (pin 15) | DL3 (pin 20) | B2 (CN1-Pin 15) | B3 (pin 22) | B5 (pin 35) | B5 (Pin 25) |
| 5 | 166 | FP8 | Data | DU0 (pin 8) | DL4 (pin 21) | | G0 (pin 14) | G2 (pin 21) | G2 (Pin 15) |
| 6 | 167 | FP9 | Data | DU1 (pin 9) | DL5 (pin 22) | G0 (CN1-Pin 9) | G1 (pin 15) | G3 (pin 23) | G3 (Pin 16) |
| 7 | 168 | FP10 | Data | DU2 (pin 10) | DL6 (pin 23) | G1 (CN1-Pin 10) | G2 (pin 16) | G4 (pin 24) | G4 (Pin 17) |
| 8 | 169 | FP11 | Data | DU3 (pin 11) | DL7 (pin 24) | G2 (CN1-Pin 11) | G3 (pin 17) | G5 (pin 25) | G5 (Pin 18) |
| 9 | 172 | FP13 | Data | | DU7 (pin 15) | | | R1 (pin10) | R1 (Pin 7) |
| 10 | 170 | FP12 | Data | | DU6 (pin 14) | | | R0 (pin 9) | R0 (Pin 6) |
| 11 | 164 | FP7 | Data | | DU5 (pin 13) | | | G1 (pin 20) | G1 (Pin 14) |
| 12 | 163 | FP6 | Data | | DU4 (pin 12) | | | G0 (pin 19) | G0 (Pin 13) |
| 13 | 176 | FP17 | Data | | DU3 (pin 11) | R2 (CN1-Pin 7) | R3 (pin 12) | R5 (pin 15) | R5 (Pin 11) |
| 14 | 175 | FP16 | Data | | DU2 (pin 10) | R1 (CN1-Pin 6) | R2 (pin 11) | R4 (pin 14) | R4 (Pin 10) |
| 15 | 174 | FP15 | Data | | DU1 (pin 9) | R0 (CN1-Pin 5) | R1 (pin 10) | R3 (pin 13) | R3 (Pin 9) |
| 16 | 173 | FP14 | Data | | DU0 (pin 8) | | R0 (pin 9) | R2 (pin 11) | R2 (Pin 8) |
| 18 | 155 | FPVDCLK | Shift Clock | CP (pin 3) | CP(pin 3) | CLOCK (CN1-Pin 1) | CLK (Pin 1) | DCLK (pin 2) | DCLK (Pin 2) |
| 20 | 131 | FP18 | Data | | | | | | |
| 22 | 156 | LFS | Frame Clock | FLM (pin 1) | FLM (pin 1) | VSYNC (CN1-Pin 4) | VSYNC (pin 5) | VSYNC (pin 5) | VSYNC (pin 4) |
| 23 | 158 | FP1 | Data | | | | | B1 (pin 30) | B1 (Pin 21) |
| 24 | | | *Spare* | | | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | | |
| 26 | 152 | FPDE | Display Enable | | | DE(CN1-Pin 3) | DE(Pin 7) | DE[DTMG] (pin 37) | DE (Pin 27) |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | | |
| 28 | - | VEE | Switched NEG | | | | | | |
| 29 | 132 | FP19 | Data | | | | | | |
| 30 | - | VBB | Switched POS | | | | | | |
| 31 | - | VBKLT | Backlight (+12) | Backlight | Backlight | Backlight | Backlight | Backlight | Backlight |
| 32 | - | SWVDD | Switched Logic | VDD (pin 5) | VCC (pin 5) | Vcc (CN2-P2) VBB (CN2-P1) | Vcc (P 24) VDD (P 25) | VDD (pins 39, & 40) | VDD (Pins 28, 29 & 30) |
| 33 | 146 | FP31 | Data | | | | | | |
| 35 | 153 | LLCLK | Line clock | LP (pin 2) | LP (pin 2) | HSYNC (CN2-Pin 6) | HSYNC (pin 3) | HSYNC (Pin 4) | HSYNC (pin 3) |
| 37 | 123 | FPVEE | VEE Enable | DISP_OFF (pin 4) | DISP_OFF (pin 4) | | | | |
| 38 | 125 | FPVCC | VCC Enable | | | | | | |
| 39 | 157 | FP0 | Data | | | | | B0 (pin 29) | B0 (Pin 20) |
| 40 | - | CONTPOS | Switched + Contrast | | VHH (pin 7) | | | | |
| 41 | - | CONTNEG | Switched - Contrast | VEE (pin 7) | | | | | |
| 42 | 139 | FP25 | Data | | | | | | |
| 43 | 145 | FP30 | Data | | | | | | |
| 44 | 138 | FP24 | Data | | | | | | |
| 17,19,21,34,36 | - | Ground | | VSS (pin 6) | VSS (pin 6,16 & 25) | GND (CN1-Pins 2, 8, 12) | GND (Pins 2,4,6,8,13) | VSS (pins 1, 3, 6, 7, 8, 12, 15, 16, 17) | GND (Pins 1, 5, 12) |
| (16 Pin) 1 & 16 | - | Ground | | | | GND (CN2-Pins 3, 4) | GND (Pins 18, 23, 29) | VSS (pins 18, 22, 26, 27, 28, 32, 36) | GND (Pins 19, 26) |
| 2 | 133 | FP20 | Data 133 | | | | | | |
| 3 | 135 | FP21 | Data 135 | | | | | | |
| 4 | 136 | FP22 | Data 136 | | | | | | |
| 5 | 137 | FP23 | Data 137 | | | | | | |
| 6 | 140 | FP26 | Data 140 | | | | | | |
| 7 | 141 | FP27 | Data 141 | | | | | | |
| 9 | 143 | FP28 | Data 143 | | | | | | |
| 10 | 144 | FP29 | Data 144 | | | | | | |
| 11 | 147 | FP32 | Data 147 | | | | | | |
| 12 | 148 | FP33 | Data 148 | | | | | | |
| 13 | 149 | FP34 | Data 149 | | | | | | |
| 14 | 150 | FP35 | Data 150 | | | | | | |
| 8 | - | Unused | | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | "-25 VDC" | "+ 26 VDC" | +5VDC | +5VDC | "+5 VDC" | +5VDC |
| Notes ? | | | | NO | NO | NO | NO | NO | NO |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P | CL-GD755x | | | Sanyo AL 0603 ADP 640X480 |
|---|---|---|---|---|
| Pin #'s | Pin #'s | Pin Name | Description | C4KSS-12 |
| 1 | 159 | FP2 | Data | B0 (Pin 16) |
| 2 | 160 | FP3 | Data | B1 (Pin 17) |
| 3 | 161 | FP4 | Data | B2 (Pin 18) |
| 4 | 162 | FP5 | Data | B3 (Pin 19) |
| 5 | 166 | FP8 | Data | G0 (Pin 12) |
| 6 | 167 | FP9 | Data | G1 (Pin 13) |
| 7 | 168 | FP10 | Data | G2 (Pin 14) |
| 8 | 169 | FP11 | Data | G3 (Pin 15) |
| 9 | 172 | FP13 | Data | |
| 10 | 170 | FP12 | Data | |
| 11 | 164 | FP7 | Data | |
| 12 | 163 | FP6 | Data | |
| 13 | 176 | FP17 | Data | R3 (Pin 10) |
| 14 | 175 | FP16 | Data | R2 (Pin 9 ) |
| 15 | 174 | FP15 | Data | R1 (Pin 8 ) |
| 16 | 173 | FP14 | Data | R0 (Pin 7 ) |
| 18 | 155 | FPVDCLK | Shift Clock | CK (Pin 1 ) |
| 20 | 131 | FP18 | Data | |
| 22 | 156 | LFS | Frame Clock | VSYNC (Pin 5) |
| 23 | 158 | FP1 | Data | |
| 24 | | | *Spare* | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | |
| 26 | 152 | FPDE | Display Enable | |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | |
| 28 | - | VEE | Switched NEG | |
| 29 | 132 | FP19 | Data | |
| 30 | - | VBB | Switched POS | |
| 31 | - | VBKLT | Backlight (+12) | Backlight |
| 32 | - | SWVDD | Switched Logic | VCC (Pin 22 & 24) |
| 33 | 146 | FP31 | Data | |
| 35 | 153 | LLCLK | Line clock | HSYNC (Pin 4) |
| 37 | 123 | FPVEE | VEE Enable | |
| 38 | 125 | FPVCC | VCC Enable | |
| 39 | 157 | FP0 | Data | |
| 40 | - | CONTPOS | Switched + Contrast | |
| 41 | - | CONTNEG | Switched - Contrast | |
| 42 | 139 | FP25 | Data | |
| 43 | 145 | FP30 | Data | |
| 44 | 138 | FP24 | Data | |
| 17,19,21,34,36 | - | Ground | | GND (Pin s2,3,6,11,20) |
| (16 Pin) 1 & 16 | - | Ground | | GND (Pin s 21, 23,28,29) |
| 2 | 133 | FP20 | Data 133 | |
| 3 | 135 | FP21 | Data 135 | |
| 4 | 136 | FP22 | Data 136 | |
| 5 | 137 | FP23 | Data 137 | |
| 6 | 140 | FP26 | Data 140 | |
| 7 | 141 | FP27 | Data 141 | |
| 9 | 143 | FP28 | Data 143 | |
| 10 | 144 | FP29 | Data 144 | |
| 11 | 147 | FP32 | Data 147 | |
| 12 | 148 | FP33 | Data 148 | |
| 13 | 149 | FP34 | Data 149 | |
| 14 | 150 | FP35 | Data 150 | |
| 8 | - | Unused | | |
| Required Voltage (See Demo Board App Notes) | | | | +5VDC |
| Notes ? | | | | Yes |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P | CL-GD755x | | | Sanyo | | Sanyo | | Sanyo | Sanyo | Sanyo | Sanyo |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Interface | Panel Part #s | Interface | Panel Part #s | LCM-5275-61(2) NAK | LCM-5314-22 NAK | LCM-5321-22 NAK | LCM-5331-22 NTK |
| | | | | 640 x 480 | | 640 x 480 | | 640 x 480 | 640 x 480 | 640 x 480 | 640 x 480 |
| Pin #'s | Pin #'s | Pin Name | Description | M2SS-4 | | M2DD-8 | | M2DD-8 | C8SS-16 | C8SS-16 | C8DD-16 |
| 1 | 159 | FP2 | Data | | LCM-5522-xxxx | LD0 (pin 12) | LCM-5505-xxxx | LD0 (pin 10) | LD0 (pin 17) | LD0 (pin 17) | LD0 (pin 15) |
| 2 | 160 | FP3 | Data | | LCM-5540-xxxx | LD1 (pin 13) | LCM-5515-xxxx | LD1 (pin 11) | LD1 (pin 18) | LD1 (pin 18) | LD1 (pin 14) |
| 3 | 161 | FP4 | Data | | LM-DK55-xxxx | LD2 (pin 14) | LCM-5541-xxxx | LD2 (pin 12) | LD2 (pin 19) | LD2 (pin 19) | LD2 (pin 13) |
| 4 | 162 | FP5 | Data | | | LD3 (pin 15) | LCM-5571-xxxx | LD3 (pin 13) | LD3 (pin 20) | LD3 (pin 20) | LD3 (pin 12) |
| 5 | 166 | FP8 | Data | D0 (pin 8) | | UD0 (pin 8) | LM-GA55-xxxx | UD0 (pin 6) | LD4 (pin 21) | LD4 (pin 21) | LD4 (pin 11) |
| 6 | 167 | FP9 | Data | D1 (pin 9) | | UD1 (pin 9) | LM-KE55-xxxx | UD1 (pin 7) | LD5 (pin 22) | LD5 (pin 22) | LD5 (pin 10) |
| 7 | 168 | FP10 | Data | D2 (pin 10) | | UD2 (pin 10) | | UD2 (pin 8) | LD6 (pin 23) | LD6 (pin 23) | LD6 (pin 9) |
| 8 | 169 | FP11 | Data | D3 (pin 11) | | UD3 (pin 11) | | UD3 (pin 9) | LD7 (pin 24) | LD7 (pin 24) | LD7 (pin 8) |
| 9 | 172 | FP13 | Data | | | | | | UD7 (pin 16) | UD7 (pin 16) | UD7 (pin 16) |
| 10 | 170 | FP12 | Data | | | | | | UD6 (pin 15) | UD6 (pin 15) | UD6 (pin 17) |
| 11 | 164 | FP7 | Data | | | | | | UD5 (pin 14) | UD5 (pin 14) | UD5 (pin 18) |
| 12 | 163 | FP6 | Data | | | | | | UD4 (pin 13) | UD4 (pin 13) | UD4 (pin 19) |
| 13 | 176 | FP17 | Data | | | | | | UD3 (pin 12) | UD3 (pin 12) | UD3 (pin 20) |
| 14 | 175 | FP16 | Data | | | | | | UD2 (pin 11) | UD2 (pin 11) | UD2 (pin 21) |
| 15 | 174 | FP15 | Data | | | | | | UD1 (pin 10) | UD1 (pin 10) | UD1 (pin 22) |
| 16 | 173 | FP14 | Data | | | | | | UD0 (pin 9) | UD0 (pin 9) | UD0 (pin 23) |
| 18 | 155 | FPVDCLK | Shift Clock | CL2 (pin 6) | | CL2 (pin 3) | | CL2 (pin 4) | CL2 (pin 6) | CL2 (pin 6) | CL2 (pin 25) |
| 20 | 131 | FP18 | Data | | | | | | | | |
| 22 | 156 | LFS | Frame Clock | FLM (pin 1) | | FLM (pin 1) | | FLM (pin 1) | FLM (pin 1) | FLM (pin 1) | FLM (pin 30) |
| 23 | 158 | FP1 | Data | M (pin 2) | | | | M (pin 2) | M (pin 2) | M (pin 2) | M (pin 29) |
| 24 | | | *Spare* | | | | | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | | | | |
| 26 | 152 | FPDE | Display Enable | | | | | | | | |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | | | | |
| 28 | - | VEE | Switched NEG | | | VEE (pin 7) | | | | | |
| 29 | 132 | FP19 | Data | | | | | | | | |
| 30 | - | VBB | Switched POS | VEE (pin 14) | | | | Vee (pin 16) | Vee (pins 28 & 29) | Vee (pins 29 & 30) | Vee (pins 3 & 4) |
| 31 | - | VBKLT | Backlight (+12) | Backlight | | Backlight | | Backlight | Backlight | 5pin (2) | Backlight |
| 32 | - | SWVDD | Switched Logic | V DD (pin 12) | | VDD ( Pin 5) | | VDD (Pin 14) | Vdd (pin 25) | Vdd (25) | Vdd (pin 7) |
| 33 | 146 | FP31 | Data | | | | | | | | |
| 35 | 153 | LLCLK | Line clock | CL1 (pin 4) | | CL1 (pin 2) | | CL1 (p3) | CL1 (pin 4) | CL1 (pin 4) | CL1 (pin 27) |
| 37 | 123 | FPVEE | VEE Enable | DISP.OFF (pin 3) | | DISP.OFF (Pin 4) | | DISP.OFF* (Pin 5) | | DISP(3) | DISP (pin 28) |
| 38 | 125 | FPVCC | VCC Enable | | | | | | | | |
| 39 | 157 | FP0 | Data | | | | | | | | |
| 40 | - | CONTPOS | Switched + Contrast | VO (pin 15) | | | | VO (pin 17) | VO (Pin 30) | VO (P 31) | VO (pin 2) |
| 41 | - | CONTNEG | Switched - Contrast | | | VEE (pin 7) | | | | | |
| 42 | 139 | FP25 | Data | | | | | | | | |
| 43 | 145 | FP30 | Data | | | | | | | | |
| 44 | 138 | FP24 | Data | | | | | | | | |
| 17,19,21,34,36 | - | Ground | | VSS (pin 5, 7, & 13) | | VSS (pin 6) | | Vss (pin 15) | Vss (pins 3,8) | Vss (pins 5,8,26,27) | Vss (pins 5, 6, 24, 26) |
| (16 Pin) 1 & 16 | - | Ground | | | | | | | Vss (pins 26,27) | 5pin (1) | |
| 2 | 133 | FP20 | Data 133 | | | | | | | | |
| 3 | 135 | FP21 | Data 135 | | | | | | | | |
| 4 | 136 | FP22 | Data 136 | | | | | | | | |
| 5 | 137 | FP23 | Data 137 | | | | | | | | |
| 6 | 140 | FP26 | Data 140 | | | | | | | | |
| 7 | 141 | FP27 | Data 141 | | | | | | | | |
| 9 | 143 | FP28 | Data 143 | | | | | | | | |
| 10 | 144 | FP29 | Data 144 | | | | | | | | |
| 11 | 147 | FP32 | Data 147 | | | | | | | | |
| 12 | 148 | FP33 | Data 148 | | | | | | | | |
| 13 | 149 | FP34 | Data 149 | | | | | | | | |
| 14 | 150 | FP35 | Data 150 | | | | | | | | |
| 8 | - | Unused | | | | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | "+38 VDC" | | "-24 VDC" | | "35 VDC" | "+37 VDC" | "+38 VDC" | +30 VDC" |
| Notes ? | | | | NO | | NO | | NO | NO | NO | NO |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P Pin #'s | CL-GD755x Pin #'s | CL-GD755x Pin Name | CL-GD755x Description | Sanyo LCM-5474-24 640 x 480 M2DD-8 | Sanyo LCM-5484-24 640 x 480 M2DD-8 | Sanyo LCM-CC 53-22 NEK 640 x 480 C8DD-16 | Sanyo LCM-CD 53-22 NTK 640 x 480 C8DD-16 | Sanyo LM-BE 53-22 NTK 640 x 480 C8SS-16 | Sanyo LM-BG 53-22 NAK 640 x 480 C8SS-16 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 159 | FP2 | Data | LD0 (pin 12) | LD0 (pin 12) | LD0 (pin 15) | LD0 (pin 16) | LD0 (pin 16) | LD0 (pin 16) |
| 2 | 160 | FP3 | Data | LD1 (pin 13) | LD1 (pin 13) | LD1 (pin 14) | LD1 (pin 17) | LD1 (pin 17) | LD1 (pin 17) |
| 3 | 161 | FP4 | Data | LD2 (pin 14) | LD2 (pin 14) | LD2 (pin 13) | LD2 (pin 18) | LD2 (pin 18) | LD2 (pin 18) |
| 4 | 162 | FP5 | Data | LD3 (pin 15) | LD3 (pin 15) | LD3 (pin 12) | LD3 (pin 19) | LD3 (pin 19) | LD3 (pin 19) |
| 5 | 166 | FP8 | Data | UD0 (pin 1) | UD0 (pin 1) | LD4 (pin 11) | LD4 (pin 20) | LD4 (pin 20) | LD4 (pin 20) |
| 6 | 167 | FP9 | Data | UD1 (pin 2) | UD1 (pin 2) | LD5 (pin 10) | LD5 (pin 21) | LD5 (pin 21) | LD5 (pin 21) |
| 7 | 168 | FP10 | Data | UD2 (pin 3) | UD2 (pin 3) | LD6 (pin 9) | LD6 (pin 22) | LD6 (pin 22) | LD6 (pin 22) |
| 8 | 169 | FP11 | Data | UD3 (pin 4) | UD3 (pin 4) | LD7 (pin 8) | LD7 (pin 23) | LD7 (pin 23) | LD7 (pin 23) |
| 9 | 172 | FP13 | Data | | | UD7 (pin 16) | UD7 (pin 15) | UD7 (pin 15) | UD7 (pin 15) |
| 10 | 170 | FP12 | Data | | | UD6 (pin 17) | UD6 (pin 14) | UD6 (pin 14) | UD6 (pin 14) |
| 11 | 164 | FP7 | Data | | | UD5 (pin 18) | UD5 (pin 13) | UD5 (pin 13) | UD5 (pin 13) |
| 12 | 163 | FP6 | Data | | | UD4 (pin 19) | UD4 (pin 12) | UD4 (pin 12) | UD4 (pin 12) |
| 13 | 176 | FP17 | Data | | | UD3 (pin 20) | UD3 (pin 11) | UD3 (pin 11) | UD3 (pin 11) |
| 14 | 175 | FP16 | Data | | | UD2 (pin 21) | UD2 (pin 10) | UD2 (pin 10) | UD2 (pin 10) |
| 15 | 174 | FP15 | Data | | | UD1 (pin 22) | UD1 (pin 9) | UD1 (pin 9) | UD1 (pin 9) |
| 16 | 173 | FP14 | Data | | | UD0 (pin 23) | UD0 (pin 8) | UD0 (pin 8) | UD0 (pin 8) |
| 18 | 155 | FPVDCLK | Shift Clock | CL2 (pin 11) | CL2 (pin 11) | CL2 (pin 25) | CL2 (pin 6) | CL2 (pin 6) | CL2 (pin 6) |
| 20 | 131 | FP18 | Data | | | | | | |
| 22 | 156 | LFS | Frame Clock | FLM (pin 6) | FLM (pin 6) | FLM (pin 30) | FLM (pin 1) | FLM (pin 1) | FLM (pin 1) |
| 23 | 158 | FP1 | Data | M (pin 7) | M (pin 7) | M (pin 29) | M (pin 2) | M (pin 2) | M (pin 2) |
| 24 | | | *Spare* | | | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | | |
| 26 | 152 | FPDE | Display Enable | | | | | | |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | | |
| 28 | - | VEE | Switched NEG | VEE (LCD(B) pin 3,4) | | | | | |
| 29 | 132 | FP19 | Data | | | | | | |
| 30 | - | VBB | Switched POS | | | Vee (pins 2, 3 & 4) | | VEE (pins 27, 28 & 29) | Vee (pins 27 & 28) |
| 31 | - | VBKLT | Backlight (+12) | Backlight | Backlight | Backlight | Backlight | Backlight | Backlight |
| 32 | - | SWVDD | Switched Logic | VDD (LCD(B) Pin 1) | VDD (LCD(B) Pin 1) | Vdd (pin 7) | Vdd (pin 24, 27, 28) | VDD (Pin 24) | Vdd (pin 24) |
| 33 | 146 | FP31 | Data | | | | | | |
| 35 | 153 | LLCLK | Line clock | CL1 (p9) | CL1 (p9) | CL1 (pin 27) | CL1 (pin 4) | CL1 (pin 4) | CL1 (pin 4) |
| 37 | 123 | FPVEE | VEE Enable | DISP.OFF (Pin 5) | DISP.OFF (Pin 5) | DISP (pin 28) | DISP_OFF (pin 3) | DISP_OFF (Pin 3) | DISP_OFF (pin 3) |
| 38 | 125 | FPVCC | VCC Enable | | | | | | |
| 39 | 157 | FP0 | Data | | | | | | |
| 40 | - | CONTPOS | Switched + Contrast | | | | VCON (P 29) (2.8 VDC MAX) | | VO (Pin 29) |
| 41 | - | CONTNEG | Switched - Contrast | VO (LCD(B) pin 5) | VEE (LCD(B) pin 3,4) | | | | |
| 42 | 139 | FP25 | Data | | | | | | |
| 43 | 145 | FP30 | Data | | | | | | |
| 44 | 138 | FP24 | Data | | | | | | |
| 17,19,21,34,36 | - | Ground | | VSS (8,10) | (B2), 8,10 | Vss (pins 5, 6, 24, 26) | Vss (pins 5, 7, 25, 26) | Vss (pins 5,7,25,26) | Vss (pins 5, 7, 25 & 26) |
| (16 Pin) 1 & 16 | - | Ground | | LCD(B) pin 2 | | | | | |
| 2 | 133 | FP20 | Data 133 | | | | | | |
| 3 | 135 | FP21 | Data 135 | | | | | | |
| 4 | 136 | FP22 | Data 136 | | | | | | |
| 5 | 137 | FP23 | Data 137 | | | | | | |
| 6 | 140 | FP26 | Data 140 | | | | | | |
| 7 | 141 | FP27 | Data 141 | | | | | | |
| 9 | 143 | FP28 | Data 143 | | | | | | |
| 10 | 144 | FP29 | Data 144 | | | | | | |
| 11 | 147 | FP32 | Data 147 | | | | | | |
| 12 | 148 | FP33 | Data 148 | | | | | | |
| 13 | 149 | FP34 | Data 149 | | | | | | |
| 14 | 150 | FP35 | Data 150 | | | | | | |
| 8 | - | Unused | | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | "-24 VDC" | "-24 VDC" | +30 VDC | *+2.8 VDC* | "+38 VDC" | +38 VDC |
| Notes ? | | | | NO | NO | NO | Use 10M and 1M resistor on VCON | NO | NO |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P | CL-GD755x | | | Sanyo | Sanyo | Sanyo | Sanyo | Sanyo | Sanyo | Sanyo |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | LM-CA 53-22 NAZ | LM-CA 53-22 NSK | LM-CA 53-22 NSZ | LM-CA 53-22 NTK | LM-CC 53-22 NEK | LM-CC 53-22 NTK | LM-CC 53-22 NTS |
| | | | | 640 x 480 | 640 x 480 | 640 x 480 | 640 x 480 | 640 x 480 | 640 x 480 | 640 x 480 |
| Pin #'s | Pin #'s | Pin Name | Description | C8DD-16 | C8SS-16 | C8DD-16 | C8DD-16 | C8DD-16 | C8DD-16 | C8DD-16 |
| 1 | 159 | FP2 | Data | UD0 (CN1-pin 8) | LD0 (pin 15) | LD0 (pin 16) | LD0 (pin 15) | LD0 (pin 15) | LD0 (pin 16) | LD0 (pin 16) |
| 2 | 160 | FP3 | Data | UD1 (CN1-pin 9) | LD1 (pin 14) | LD1 (pin 17) | LD1 (pin 14) | LD1 (pin 14) | LD1 (pin 17) | LD1 (pin 17) |
| 3 | 161 | FP4 | Data | UD2 (CN1-pin 10) | LD2 (pin 13) | LD2 (pin 18) | LD2 (pin 13) | LD2 (pin 13) | LD2 (pin 18) | LD2 (pin 18) |
| 4 | 162 | FP5 | Data | UD3 (CN1-pin 11) | LD3 (pin 12) | LD3 (pin 19) | LD3 (pin 12) | LD3 (pin 12) | LD3 (pin 19) | LD3 (pin 19) |
| 5 | 166 | FP8 | Data | UD4 (CN1-pin 12) | LD4 (pin 11) | LD4 (pin 20) | LD4 (pin 11) | LD4 (pin 11) | LD4 (pin 20) | LD4 (pin 20) |
| 6 | 167 | FP9 | Data | UD5 (CN1-pin 13) | LD5 (pin 10) | LD5 (pin 21) | LD5 (pin 10) | LD5 (pin 10) | LD5 (pin 21) | LD5 (pin 21) |
| 7 | 168 | FP10 | Data | UD6 (CN1-pin 14) | LD6 (pin 9) | LD6 (pin 22) | LD6 (pin 9) | LD6 (pin 9) | LD6 (pin 22) | LD6 (pin 22) |
| 8 | 169 | FP11 | Data | UD7 (CN1-pin 15) | LD7 (pin 8) | LD7 (pin 23) | LD7 (pin 8) | LD7 (pin 8) | LD7 (pin 23) | LD7 (pin 23) |
| 9 | 172 | FP13 | Data | LD7 (CN2-pin 23) | UD7 (pin 16) | UD7 (pin 15) | UD7 (pin 16) | UD7 (pin 16) | UD7 (pin 15) | UD7 (pin 15) |
| 10 | 170 | FP12 | Data | LD6 (CN2-pin 22) | UD6 (pin 17) | UD6 (pin 14) | UD6 (pin 17) | UD6 (pin 17) | UD6 (pin 14) | UD6 (pin 14) |
| 11 | 164 | FP7 | Data | LD5 (CN2-pin 21) | UD5 (pin 18) | UD5 (pin 13) | UD5 (pin 18) | UD5 (pin 18) | UD5 (pin 13) | UD5 (pin 13) |
| 12 | 163 | FP6 | Data | LD4 (CN2-pin 20) | UD4 (pin 19) | UD4 (pin 12) | UD4 (pin 19) | UD4 (pin 19) | UD4 (pin 12) | UD4 (pin 12) |
| 13 | 176 | FP17 | Data | LD3 (CN2-pin 19) | UD3 (pin 20) | UD3 (pin 11) | UD3 (pin 20) | UD3 (pin 20) | UD3 (pin 11) | UD3 (pin 11) |
| 14 | 175 | FP16 | Data | LD2 (CN2-pin 18) | UD2 (pin 21) | UD2 (pin 10) | UD2 (pin 21) | UD2 (pin 21) | UD2 (pin 10) | UD2 (pin 10) |
| 15 | 174 | FP15 | Data | LD1 (CN2-pin 17) | UD1 (pin 22) | UD1 (pin 9) | UD1 (pin 22) | UD1 (pin 22) | UD1 (pin 9) | UD1 (pin 9) |
| 16 | 173 | FP14 | Data | LD0 (CN2-pin 16) | UD0 (pin 23) | UD0 (pin 8) | UD0 (pin 23) | UD0 (pin 23) | UD0 (pin 8) | UD0 (pin 8) |
| 18 | 155 | FPVDCLK | Shift Clock | CL2 (CN1-pin 6) | CL2 (pin 25) | CL2 (pin 6) | CL2 (pin 25) | CL2 (pin 25) | CL2 (pin 6) | CL2 (pin 6) |
| 20 | 131 | FP18 | Data | | | | | | | |
| 22 | 156 | LFS | Frame Clock | FLM (CN1-pin 1) | FLM (pin 30) | FLM (pin 1) | FLM (pin 30) | FLM (pin 30) | FLM (pin 1) | FLM (pin 1) |
| 23 | 158 | FP1 | Data | M (CN1-pin 2) | M (pin 29) | M (pin 2) | M (pin 29) | M (pin 29) | M (pin 2) | M (pin 2) |
| 24 | | | *Spare* | | | | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | | | |
| 26 | 152 | FPDE | Display Enable | | | | | | | |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | | | |
| 28 | - | VEE | Switched NEG | | | | | | | |
| 29 | 132 | FP19 | Data | | | | | | | |
| 30 | - | VBB | Switched POS | Vee (CN2-pins 27 & 28) | Vee (pins 3 & 4) | Vee (pins 27 & 28) | Vee (pins 3 & 4) | Vee (pins 2, 3, 4) | Vee (pins 27, 28, 29) | Vee (pins 27, 28, 29) |
| 31 | - | VBKLT | Backlight (+12) | Backlight | Backlight | Backlight | Backlight | Backlight | Backlight | Backlight |
| 32 | - | SWVDD | Switched Logic | Vdd (CN2-pin 24) | Vdd (pin 7) | Vdd (pin 24) | Vdd (pin 7) | Vdd (pin 7) | Vdd (pin 24) | Vdd (pin 24) |
| 33 | 146 | FP31 | Data | | | | | | | |
| 35 | 153 | LLCLK | Line clock | CL1 (CN1-pin 4) | CL1 (pin 27) | CL1 (pin 4) | CL1 (pin 27) | CL1 (pin 27) | CL1 (pin 4) | CL1 (pin 4) |
| 37 | 123 | FPVEE | VEE Enable | DISP (CN1-pin 3) | DISP_OFF (pin 28) | DISP_OFF (pin 3) | DISP_OFF (pin 28) | DISP_OFF (pin 28) | DISP_OFF (pin 3) | DISP_OFF (pin 3) |
| 38 | 125 | FPVCC | VCC Enable | | | | | | | |
| 39 | 157 | FP0 | Data | | | | | | | |
| 40 | - | CONTPOS | Switched + Contrast | VO (CN2-pin 29) | VO (pin 2) | VO (pin 29) | VO (pin 2) | | | |
| 41 | - | CONTNEG | Switched - Contrast | | | | | | | |
| 42 | 139 | FP25 | Data | | | | | | | |
| 43 | 145 | FP30 | Data | | | | | | | |
| 44 | 138 | FP24 | Data | | | | | | | |
| 17,19,21,34,36 | - | Ground | | Vss (CN1- pins 5,7) | Vss (pins 5, 6, 24, 26) | Vss (pins 5, 7, 25, 26) | Vss (p 5, 6, 24, 26) | Vss (p 5, 6, 24, 26) | Vss (p 5, 7, 25, 26) | Vss (p 5, 7, 25, 26) |
| (16 Pin) 1 & 16 | - | Ground | | Vss (CN2- pins 25 & 26) | | | | | | |
| 2 | 133 | FP20 | Data 133 | | | | | | | |
| 3 | 135 | FP21 | Data 135 | | | | | | | |
| 4 | 136 | FP22 | Data 136 | | | | | | | |
| 5 | 137 | FP23 | Data 137 | | | | | | | |
| 6 | 140 | FP26 | Data 140 | | | | | | | |
| 7 | 141 | FP27 | Data 141 | | | | | | | |
| 9 | 143 | FP28 | Data 143 | | | | | | | |
| 10 | 144 | FP29 | Data 144 | | | | | | | |
| 11 | 147 | FP32 | Data 147 | | | | | | | |
| 12 | 148 | FP33 | Data 148 | | | | | | | |
| 13 | 149 | FP34 | Data 149 | | | | | | | |
| 14 | 150 | FP35 | Data 150 | | | | | | | |
| 8 | - | Unused | | | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | "+30 VDC" | +30 VDC | +30 VDC | +30 VDC | +30 VDC | +30 VDC | +30 VDC |
| Notes ? | | | | NO | NO | NO | NO | NO | NO | NO |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P | CL-GD755x | | | Sanyo | Sanyo | Sanyo | Sanyo | Seiko | Seiko |
|---|---|---|---|---|---|---|---|---|---|
| | | | | LM-CD 53-22 NEK | LM-CD 53-22 NTK | LM-CK 53-22 NAK | LM-FK 53-22 NTK | G 642 G | GZ 10000 A000 |
| | | | | 640 x 480 | 640 x 480 | 640 x 480 | 800 x 600 | 640 x 480 | 640 x 480 |
| Pin #'s | Pin #'s | Pin Name | Description | C8DD-16 | C8DD-16 | C8SS-16 | C8DD-16 | M2DD-8 | C8SS-16 |
| 1 | 159 | FP2 | Data | DL0 (pin 11) | LD0 (pin 16) | LD0 (pin 15) | LD0 (pin 16) | LD0 (pin 15) | UD0 (pin 7) |
| 2 | 160 | FP3 | Data | DL1 (pin 13) | LD1 (pin 17) | LD1 (pin 14) | LD1 (pin 17) | LD1 (pin 16) | UD1 (pin 9) |
| 3 | 161 | FP4 | Data | DL2 (pin 17) | LD2 (pin 18) | LD2 (pin 13) | LD2 (pin 18) | LD2 (pin 17) | UD2 (pin 11) |
| 4 | 162 | FP5 | Data | DL3 (pin 19) | LD3 (pin 19) | LD3 (pin 12) | LD3 (pin 19) | LD3 (pin 18) | UD3 (pin 13) |
| 5 | 166 | FP8 | Data | DL4 (pin 1) | LD4 (pin 20) | LD4 (pin 11) | LD4 (pin 20) | UD0 (pin 11) | UD4 (pin 15) |
| 6 | 167 | FP9 | Data | DL5 (pin 3) | LD5 (pin 21) | LD5 (pin 10) | LD5 (pin 21) | UD1 (pin 12) | UD5 (pin 17) |
| 7 | 168 | FP10 | Data | DL6 (pin 5) | LD6 (pin 22) | LD6 (pin 9) | LD6 (pin 22) | UD2 (pin 13) | UD6 (pin 19) |
| 8 | 169 | FP11 | Data | DL7 (pin 7) | LD7 (pin 23) | LD7 (pin 8) | LD7 (pin 23) | UD3 (pin 14) | UD7 (pin 21) |
| 9 | 172 | FP13 | Data | DU7 (pin 31) | UD7 (pin 15) | UD7 (pin 16) | UD7 (pin 15) | | LD0 (pin 8) |
| 10 | 170 | FP12 | Data | DU6 (pin 29) | UD6 (pin 14) | UD6 (pin 17) | UD6 (pin 14) | | LD1 (pin 10) |
| 11 | 164 | FP7 | Data | DU5 (pin 25) | UD5 (pin 13) | UD5 (pin 18) | UD5 (pin 13) | | LD2 (pin 12) |
| 12 | 163 | FP6 | Data | DU4 (pin 23) | UD4 (pin 12) | UD4 (pin 19) | UD4 (pin 12) | | LD3 (pin 14) |
| 13 | 176 | FP17 | Data | DU3 (pin 22) | UD3 (pin 11) | UD3 (pin 20) | UD3 (pin 11) | | LD4 (pin 16) |
| 14 | 175 | FP16 | Data | DU2 (pin 24) | UD2 (pin 10) | UD2 (pin 21) | UD2 (pin 10) | | LD5 (pin 18) |
| 15 | 174 | FP15 | Data | DU1 (pin 26) | UD1 (pin 9) | UD1 (pin 22) | UD1 (pin 9) | | LD6 (pin 20) |
| 16 | 173 | FP14 | Data | DU0 (pin 28) | UD0 (pin 8) | UD0 (pin 23) | UD0 (pin 8) | | LD7 (pin 22) |
| 18 | 155 | FPVDCLK | Shift Clock | XCK (pin 10) | CL2 (pin 6) | CL2 (pin 25) | CL2 (pin 6) | XSCL (Pin 9) | XSCLU, XSCLL (Pins 24,26 |
| 20 | 131 | FP18 | Data | | | | | | |
| 22 | 156 | LFS | Frame Clock | YD (pin 4) | FLM (pin 1) | FLM (pin 30) | FLM (pin 1) | DIN (Pin 8) | DIN (Pin 28) |
| 23 | 158 | FP1 | Data | | M (pin 2) | M (pin 29) | M (pin 2) | FR (Pin 5) | FR (pin 30) |
| 24 | | | *Spare* | | | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | | |
| 26 | 152 | FPDE | Display Enable | | | | | | |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | | |
| 28 | - | VEE | Switched NEG | | | | | | |
| 29 | 132 | FP19 | Data | | | | | | |
| 30 | - | VBB | Switched POS | | | Vee (pins 3 & 4) | | | VLCD (Pins 1 & 2) |
| 31 | - | VBKLT | Backlight (+12) | Backlight | Backlight | Backlight | Backlight | CN2-1 | Backlight Circuit |
| 32 | - | SWVDD | Switched Logic | Vdd (pins 14 & 16) | Vdd (pins 24, 27, 28) | Vdd (7) | Vdd (pin 24) | VDD (Pin 1) | VDD (pins 33,34) |
| 33 | 146 | FP31 | Data | | | | | | |
| 35 | 153 | LLCLK | Line clock | LP (pin 6) | CL1 (pin 4) | CL1 (pin 27) | CL1 (pin 4) | LP (Pin 4) | LP (Pin 32) |
| 37 | 123 | FPVEE | VEE Enable | DISP (pin 18) | DISP_OFF (pin 3) | DISP (28) | DISP_OFF (pin 3) | | |
| 38 | 125 | FPVCC | VCC Enable | | | | | | |
| 39 | 157 | FP0 | Data | | | | | | |
| 40 | - | CONTPOS | Switched + Contrast | Vcon (pin 12) ***2 VDC*** | Vcon (pin 29) ***2 VDC*** | VO (pin 2) | VEE (Pins 27, 28, & 29) | | |
| 41 | - | CONTNEG | Switched - Contrast | | | | | VLCD (Pin 3) | |
| 42 | 139 | FP25 | Data | | | | | | |
| 43 | 145 | FP30 | Data | | | | | | |
| 44 | 138 | FP24 | Data | | | | | | |
| 17,19,21,34,36 | - | Ground | | GND (p 2, 8, 9, 15) | Vss (p 5, 7, 25, 26) | Vss (pins 5,6,24,26) | Vss (pins 5, 7, 25, 26) | BL BOARD, 2 | VSS (Pins 5,6,23,25) |
| (16 Pin) 1 & 16 | - | Ground | | GND (p 21, 27, 30) | | | | | VSS (Pins 27,29,31) |
| 2 | 133 | FP20 | Data 133 | | | | | | |
| 3 | 135 | FP21 | Data 135 | | | | | | |
| 4 | 136 | FP22 | Data 136 | | | | | | |
| 5 | 137 | FP23 | Data 137 | | | | | | |
| 6 | 140 | FP26 | Data 140 | | | | | | |
| 7 | 141 | FP27 | Data 141 | | | | | | |
| 9 | 143 | FP28 | Data 143 | | | | | | |
| 10 | 144 | FP29 | Data 144 | | | | | | |
| 11 | 147 | FP32 | Data 147 | | | | | | |
| 12 | 148 | FP33 | Data 148 | | | | | | |
| 13 | 149 | FP34 | Data 149 | | | | | | |
| 14 | 150 | FP35 | Data 150 | | | | | | |
| 8 | - | Unused | | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | ***+2.0 VDC*** | ***+2.0 VDC*** | "+38 VDC" | "+30 VDC" | "-24 VDC" | "+40 VDC" |
| Notes ? | | | | Use 10M and 1M resistor on VCON | Use 10M and 1M resistor on VCON | NO | NO | NO | NO |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P Pin #'s | CL-GD755x Pin #'s | CL-GD755x Pin Name | CL-GD755x Description | Sharp LM 32008 F 320 x 240 M2SS-4 | Sharp LM 32010 P 320 x 240 M2SS-4 | Sharp LM 64048 Z 640 x 480 M2DD-8 | Sharp LM 64C031 640 x 480 C8SSID-8 | Sharp LM 64C08 P 640 x 480 C8DD-16 | Sharp LM 64C15 P / LM 64C35 P 640 x 480 C8DD-16 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 159 | FP2 | Data | | | DL0 (p11) | D7 (pin 17) | DL0 (pin 17) | DL0 (pin 11) |
| 2 | 160 | FP3 | Data | | | DL1 (p12) | D6 (pin 16) | DL1 (pin 18) | DL1 (pin 13) |
| 3 | 161 | FP4 | Data | | | DL2 (p13) | D5 (pin 15) | DL2 (pin 19) | DL2 (pin 17) |
| 4 | 162 | FP5 | Data | | | DL3 (p14) | D4 (pin 14) | DL3 (pin 20) | DL3 (pin 19) |
| 5 | 166 | FP8 | Data | D0 (pin 7) | D0 (pin 7) | DU0 (p7) | D3 (pin 13) | DL4 (pin 21) | DL4 (pin 1) |
| 6 | 167 | FP9 | Data | D1 (pin 8) | D1 (pin 8) | DU1 (p8) | D2 (pin 12) | DL5 (pin 22) | DL5 (pin 3) |
| 7 | 168 | FP10 | Data | D2 (pin 9) | D2 (pin 9) | DU2 (p9) | D1 (pin 11) | DL6 (pin 23) | DL6 (pin 5) |
| 8 | 169 | FP11 | Data | D3 (pin 10) | D3 (pin 10) | DU3 (p10) | D0 (pin 10) | DL7 (pin 24) | DL7 (pin 7) |
| 9 | 172 | FP13 | Data | | | | | DU7 (pin 15) | DU7 (pin 31) |
| 10 | 170 | FP12 | Data | | | | | DU6 (pin 14) | DU6 (pin 29) |
| 11 | 164 | FP7 | Data | | | | | DU5 (pin 13) | DU5 (pin 25) |
| 12 | 163 | FP6 | Data | | | | | DU4 (pin 12) | DU4 (pin 23) |
| 13 | 176 | FP17 | Data | | | | | DU3 (pin 11) | DU3 (pin 22) |
| 14 | 175 | FP16 | Data | | | | | DU2 (pin 10) | DU2 (pin 24) |
| 15 | 174 | FP15 | Data | | | | | DU1 (pin 9) | DU1 (pin 26) |
| 16 | 173 | FP14 | Data | | | | | DU0 (pin 8) | DU0 (pin 28) |
| 18 | 155 | FPVDCLK | Shift Clock | CP2 (pin 3) | CP2 (pin 3) | CP2 (p3) | XCLKL(pin 3) | XCK(pin 3) | XCK(pin 10) |
| 20 | 131 | FP18 | Data | | | | | | |
| 22 | 156 | LFS | Frame Clock | S (pin 1) | S (pin 1) | S (p1) | YD (pin 1) | YD (pin 1) | YD (pin 4) |
| 23 | 158 | FP1 | Data | | | | | | |
| 24 | | | *Spare* | | | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | | |
| 26 | 152 | FPDE | Display Enable | | | | XCLKU(pin 4) | | |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | | |
| 28 | - | VEE | Switched NEG | | | | | | |
| 29 | 132 | FP19 | Data | | | | | | |
| 30 | - | VBB | Switched POS | | | | | | |
| 31 | - | VBKLT | Backlight (+12) | | | | | | |
| 32 | - | SWVDD | Switched Logic | | Backlight | Backlight | Backlight | Backlight | Backlight |
| 33 | 146 | FP31 | Data | V DD (pin 4) | V DD (pin 4) | VDD (p4) | VDD (pin6) | VDD (pin 5) | VDD (pin 14 &16) |
| 35 | 153 | LLCLK | Line clock | | | | | | |
| 37 | 123 | FPVEE | VEE Enable | CP1 (pin 2) | CP1 (pin 2) | CP1 (p2) | LP (pin 2) | LP (pin 2) | LP (pin 6) |
| 38 | 125 | FPVCC | VCC Enable | | | | | DISP (pin 4) | DISP (pin 18) |
| 39 | 157 | FP0 | Data | | | | | | |
| 40 | - | CONTPOS | Switched + Contrast | | | | VEE (pin 8) | VEE (pin 7) | VCOM (pin 12) ***2 VDC*** |
| 41 | - | CONTNEG | Switched - Contrast | VEE (pin 6) | VEE (pin 6) | VEE (p6) | | | |
| 42 | 139 | FP25 | Data | | | | | | |
| 43 | 145 | FP30 | Data | | | | | | |
| 44 | 138 | FP24 | Data | | | | | | |
| 17,19,21,34,36 | - | Ground | | VSS (pin 5) | VSS (pin 5) | VSS (p5) | VSS (pin 7,9,18) | VSS (pin 6,16 & 25) | VSS (pins 2, 8, 9, 15, 21, 27, 30 ) |
| (16 Pin) 1 & 16 | - | Ground | | | | | | | |
| 2 | 133 | FP20 | Data 133 | | | | | | |
| 3 | 135 | FP21 | Data 135 | | | | | | |
| 4 | 136 | FP22 | Data 136 | | | | | | |
| 5 | 137 | FP23 | Data 137 | | | | | | |
| 6 | 140 | FP26 | Data 140 | | | | | | |
| 7 | 141 | FP27 | Data 141 | | | | | | |
| 9 | 143 | FP28 | Data 143 | | | | | | |
| 10 | 144 | FP29 | Data 144 | | | | | | |
| 11 | 147 | FP32 | Data 147 | | | | | | |
| 12 | 148 | FP33 | Data 148 | | | | | | |
| 13 | 149 | FP34 | Data 149 | | | | | | |
| 14 | 150 | FP35 | Data 150 | | | | | | |
| 8 | - | Unused | | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | "-18 VDC" | "-18 VDC" | -21 VDC | "+ 36 VDC" | "+ 26 VDC" | ***+2.0 VDC*** |
| Notes ? | | | | NO | NO | NO | NO | NO | Use 10M and 1M resistor on VCON |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P | CL-GD755x | | | Sharp | Sharp | Sharp | Sharp | Sharp |
|---|---|---|---|---|---|---|---|---|
| | | | | LM 64P80 | LM 80C03 P | LQ 10D 011 | LQ 10D 131 | LQ 10D 311 |
| | | | | 640 x 480 | 800 x 600 | 640 x 480 | 640 x 480 | 640 x 480 |
| Pin #'s | Pin #'s | Pin Name | Description | M2DD-8 | C8DD-16 | C512SS-9 | C4KSS-12 | C256KSS-18 |
| 1 | 159 | FP2 | Data | DL0 (p12) | DL0 (pin 11) | | B0 (pin 23) | B2 (CN3-p11) |
| 2 | 160 | FP3 | Data | DL1 (p13) | DL1 (pin 13) | BBIT 0 (pin 11) | B1 (pin 25) | B3 (CN1-p13) |
| 3 | 161 | FP4 | Data | DL2 (p14) | DL2 (pin 17) | BBIT 1 (pin 12) | B2 (pin 29) | B4 (CN1-p14) |
| 4 | 162 | FP5 | Data | DL3 (p15) | DL3 (pin 19) | BBIT 2 (pin 13) | B3 (pin 31) | B5 (CN1-p15) |
| 5 | 166 | FP8 | Data | DU0 (p8) | DL4 (pin 1) | | G0 (pin 11) | G2 (CN3-p7) |
| 6 | 167 | FP9 | Data | DU1 (p9) | DL5 (pin 3) | GBIT 0 (pin 7) | G1 (pin 13) | G3 (CN1-p9) |
| 7 | 168 | FP10 | Data | DU2 (p10) | DL6 (pin 5) | GBIT 1 (pin 8) | G2 (pin 17) | G4 (CN1-p10) |
| 8 | 169 | FP11 | Data | DU3 (p11) | DL7 (pin 7) | GBIT 2 (pin 9) | G3 (pin 19) | G5 (CN1-p 11) |
| 9 | 172 | FP13 | Data | | DU7 (pin 31) | | | R1 (CN3-p 2) |
| 10 | 170 | FP12 | Data | | DU6 (pin 29) | | | R0 (CN3-p1) |
| 11 | 164 | FP7 | Data | | DU5 (pin 25) | | | G1 (CN3-p6) |
| 12 | 163 | FP6 | Data | | DU4 (pin 23) | | | G0 (CN3-p 5) |
| 13 | 176 | FP17 | Data | | DU3 (pin 22) | RBIT 2 (pin 5) | R3 (pin 7) | R5 (CN1-P7) |
| 14 | 175 | FP16 | Data | | DU2 (pin 24) | RBIT 1 (pin 4) | R2 (pin 5) | R4 (CN1-P6) |
| 15 | 174 | FP15 | Data | | DU1 (pin 26) | RBIT 0 (pin 3) | R1 (pin 3) | R3 (CN1-P5) |
| 16 | 173 | FP14 | Data | | DU0 (pin 28) | | R0 (pin 1) | R2 (CN3-p3) |
| 18 | 155 | FPVDCLK | Shift Clock | CP2 (p3) | XCK(pin 10) | CK (pin 1) | CK (pin 10) | CK (CN1-p1) |
| 20 | 131 | FP18 | Data | | | | | |
| 22 | 156 | LFS | Frame Clock | S (p1) | YD (pin 4) | VSYNC (pin 17) | VSYNC (pin 4) | VSYNC (CN1-p4) |
| 23 | 158 | FP1 | Data | | | | | B1 (CN3-p10) |
| 24 | | | *Spare* | | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | |
| 26 | 152 | FPDE | Display Enable | | | | ENAB (pin 28) | ENAB (CN2-P5) |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | |
| 28 | - | VEE | Switched NEG | | | | | |
| 29 | 132 | FP19 | Data | | | | | |
| 30 | - | VBB | Switched POS | | | | | |
| 31 | - | VBKLT | Backlight (+12) | Backlight | Backlight | VDD (pin 20) & Backlight | Backlight | Backlight |
| 32 | - | SWVDD | Switched Logic | VDD (p5) | VDD (pin 14 &16) | VCC (pin 18) | VCC (Pin 22 & 24) | VCC (CN2-P1 & 2) |
| 33 | 146 | FP31 | Data | | | | | |
| 35 | 153 | LLCLK | Line clock | CP1 (p2) | LP (pin 6) | HSYNC (pin 15) | HSYNC (pin 6) | HSYNC (CN1-p3) |
| 37 | 123 | FPVEE | VEE Enable | DISP(p4) | DISP (pin 18) | | | |
| 38 | 125 | FPVCC | VCC Enable | | | | | |
| 39 | 157 | FP0 | Data | | | | | B0 (CN3-p9) |
| 40 | - | CONTPOS | Switched + Contrast | | VCON (pin 12) ***2 VDC*** | | | |
| 41 | - | CONTNEG | Switched - Contrast | VEE (p7) | | | | |
| 42 | 139 | FP25 | Data | | | | | |
| 43 | 145 | FP30 | Data | | | | | |
| 44 | 138 | FP24 | Data | | | | | |
| 17,19,21,34,36 | - | Ground | | VSS (p6) | VSS (pins 2, 8, 9, 15, 21, 27, 30 ) | GND (pins 2,6,10) | GND (pins 2, 8, 9, 12, 15) | GND (CN1-P2,8,12) |
| (16 Pin) 1 & 16 | - | Ground | | | | GND (pins 14,16,19,) | GND (pins 20, 21, 27, 30) | GND (CN2-P3 & 4, CN3-P4 & 8) |
| 2 | 133 | FP20 | Data 133 | | | | | |
| 3 | 135 | FP21 | Data 135 | | | | | |
| 4 | 136 | FP22 | Data 136 | | | | | |
| 5 | 137 | FP23 | Data 137 | | | | | |
| 6 | 140 | FP26 | Data 140 | | | | | |
| 7 | 141 | FP27 | Data 141 | | | | | |
| 9 | 143 | FP28 | Data 143 | | | | | |
| 10 | 144 | FP29 | Data 144 | | | | | |
| 11 | 147 | FP32 | Data 147 | | | | | |
| 12 | 148 | FP33 | Data 148 | | | | | |
| 13 | 149 | FP34 | Data 149 | | | | | |
| 14 | 150 | FP35 | Data 150 | | | | | |
| 8 | - | Unused | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | -21 VDC | ***+2.0 VDC*** | "+ 12 VDC" | "+5 VDC" | "+ 12 VDC" |
| Notes ? | | | | NO | Use 10M and 1M resistor on VCON | NO | NO | NO |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P | CL-GD755x | | | Sharp | Sharp | Sharp | Sharp | Sharp |
|---|---|---|---|---|---|---|---|---|
| | | | | LQ 10D 321 / 331 | LQ 10D 344 | LQ 10D S01 / LQ 11D S01 | LQ 9D 011 | LQ 9D 151/161 |
| | | | | 640 x 480 | 640 x 480 | 800 x 600 | 640 x 480 | 640 x 480 |
| Pin #'s | Pin #'s | Pin Name | Description | C256KSS-18 | C256KSS-18 | C256KSS-18 | C512SS-9 | C4KSS-12 |
| 1 | 159 | FP2 | Data | B2 (Pin 22) | B2 (Pin 22) | B2 (Pin 28) | | B0 (pin 23) |
| 2 | 160 | FP3 | Data | B3 (Pin 23) | B3 (Pin 23) | B3 (Pin 29) | B0 (CN1-p13) | B1 (pin 25) |
| 3 | 161 | FP4 | Data | B4 (Pin 24) | B4 (Pin 24) | B4 (Pin 30) | B1 (CN1-p14) | B2 (pin 29) |
| 4 | 162 | FP5 | Data | B5 (Pin 25) | B5 (Pin 25) | B5 (Pin 31) | B2 (CN1-p15) | B3 (pin 31) |
| 5 | 166 | FP8 | Data | G2 (Pin 15) | G2 (Pin 15) | G2 (Pin 19) | | G0 (pin 11) |
| 6 | 167 | FP9 | Data | G3 (Pin 16) | G3 (Pin 16) | G3 (Pin 20) | G0 (CN1-p 9) | G1 (pin 13) |
| 7 | 168 | FP10 | Data | G4 (Pin 17) | G4 (Pin 17) | G4 (Pin 21) | G1 (CN1-p10) | G2 (pin 17) |
| 8 | 169 | FP11 | Data | G5 (Pin 18) | G5 (Pin 18) | G5 (Pin 22) | G2 (CN1-p11) | G3 (pin 19) |
| 9 | 172 | FP13 | Data | R1 (Pin 7) | R1 (Pin 7) | R1 (Pin 9) | | |
| 10 | 170 | FP12 | Data | R0 (Pin 6) | R0 (Pin 6) | R0 (Pin 8) | | |
| 11 | 164 | FP7 | Data | G1 (Pin 14) | G1 (Pin 14) | G1 (Pin 18) | | |
| 12 | 163 | FP6 | Data | G0 (Pin 13) | G0 (Pin 13) | G0 (Pin 17) | | |
| 13 | 176 | FP17 | Data | R5 (Pin 11) | R5 (Pin 11) | R5 (Pin 13) | R2 (CN1-p7) | R3 (pin 7) |
| 14 | 175 | FP16 | Data | R4 (Pin 10) | R4 (Pin 10) | R4 (Pin 12) | R1 (CN1-p 6) | R2 (pin 5) |
| 15 | 174 | FP15 | Data | R3 (Pin 9) | R3 (Pin 9) | R3 (Pin 11) | R0 (CN1-p5) | R1 (pin 3) |
| 16 | 173 | FP14 | Data | R2 (Pin 8) | R2 (Pin 8) | R2 (Pin 10) | | R0 (pin 1) |
| 18 | 155 | FPVDCLK | Shift Clock | CK (Pin 2) | CK (Pin 2) | CK (Pin 2) | CK (CN1-p1) | CK (pin 10) |
| 20 | 131 | FP18 | Data | | | | | |
| 22 | 156 | LFS | Frame Clock | VSYNC (Pin 4) | VSYNC (Pin 4) | VSYNC (Pin 6) | VSYNC (CN1-p4) | VSYNC (pin 4) |
| 23 | 158 | FP1 | Data | B1 (Pin 21) | B1 (Pin 21) | B1 (Pin 27) | | |
| 24 | | | *Spare* | | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | |
| 26 | 152 | FPDE | Display Enable | ENAB (Pin 27) | ENAB (Pin 27) | ENAB (Pin 35) | ENAB (CN2-P5) | ENAB (pin 28) |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | |
| 28 | - | VEE | Switched NEG | | | | | |
| 29 | 132 | FP19 | Data | | | | | |
| 30 | - | VBB | Switched POS | | | | | |
| 31 | - | VBKLT | Backlight (+12) | Backlight | Backlight | Backlight | Backlight | Backlight |
| 32 | - | SWVDD | Switched Logic | VCC (Pins 28 & 29 ) | VCC (Pins 28 & 29 ) | VCC (Pins 36 & 37) | VCC (CN2-P1 & 2) | VCC (Pin 22 & 24) |
| 33 | 146 | FP31 | Data | | | | | |
| 35 | 153 | LLCLK | Line clock | HSYNC (Pin 3) | HSYNC (Pin 3) | HSYNC (Pin 5) | HSYNC (CN1-p3) | HSYNC (pin 6) |
| 37 | 123 | FPVEE | VEE Enable | | | | | |
| 38 | 125 | FPVCC | VCC Enable | | | | | |
| 39 | 157 | FP0 | Data | B0 (Pin 20) | B0 (Pin 20) | B0 (Pin 26) | | |
| 40 | - | CONTPOS | Switched + Contrast | | | | | |
| 41 | - | CONTNEG | Switched - Contrast | | | | | |
| 42 | 139 | FP25 | Data | | | | | |
| 43 | 145 | FP30 | Data | | | | | |
| 44 | 138 | FP24 | Data | | | | | |
| 17,19,21,34,36 | - | Ground | | GND (Pin 1, 5, 12, 19, 26) | GND (Pin 1, 5, 12, 19, 26) | GND (Pins 1,3,4,14,15,16,23,24) | GND (CN1-P2,8,12) | GND (pins 2, 8, 9, 12, 15) |
| (16 Pin) 1 & 16 | - | Ground | | | R/L, U/D (30 & 31) | GND (Pin 25, 32, 33, 34, 40, 41) | GND (CN2-P3, 4) | GND (pins 20, 21, 27, 30) |
| 2 | 133 | FP20 | Data 133 | | | | | |
| 3 | 135 | FP21 | Data 135 | | | | | |
| 4 | 136 | FP22 | Data 136 | | | | | |
| 5 | 137 | FP23 | Data 137 | | | | | |
| 6 | 140 | FP26 | Data 140 | | | | | |
| 7 | 141 | FP27 | Data 141 | | | | | |
| 9 | 143 | FP28 | Data 143 | | | | | |
| 10 | 144 | FP29 | Data 144 | | | | | |
| 11 | 147 | FP32 | Data 147 | | | | | |
| 12 | 148 | FP33 | Data 148 | | | | | |
| 13 | 149 | FP34 | Data 149 | | | | | |
| 14 | 150 | FP35 | Data 150 | | | | | |
| 8 | - | Unused | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | "+5 VDC" | "+5 VDC" | "+5 VDC" | "+5 VDC" | "+3.3 VDC" |
| Notes ? | | | | NO | NO | NO | NO | PVDD = 3.3 Volts |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P | CL-GD755x | | | Toshiba | Toshiba | Toshiba | Toshiba | Toshiba | Toshiba |
|---|---|---|---|---|---|---|---|---|---|
| | | | | LTM-08 C015 /09 C016 /08 C015 | LTM-09 C020 | LTM-09 C020 K | LTM-10 C025 | LTM-10 C035 | TLX-806 2S-C3X |
| | | | | 640 x 480 | 640 x 480 | 640 x 480 | 640 x 480 | 800 x 600 | 640 x 480 |
| Pin #'s | Pin #'s | Pin Name | Description | C512SS-9 | C512SS-9 | C512SS-9 | C256KSS-18 | C256KSS-18 | C8DD-16 |
| 1 | 159 | FP2 | Data | | | | B2 (Pin 24) | B2 (Pin 24) | LD0 (IF2-pin 2) |
| 2 | 160 | FP3 | Data | B0 (CN2-p1) | B0 (Pin 4) | B0 (Pin 15) | B3 (Pin 26) | B3 (Pin 26) | LD1 (IF2-pin 3) |
| 3 | 161 | FP4 | Data | B1 (CN2-p3) | B1 (Pin 5) | B1 (Pin 13) | B4 (Pin 27) | B4 (Pin 27) | LD2 (IF2-pin 4) |
| 4 | 162 | FP5 | Data | B2 (CN2-p5) | B2 (Pin 7) | B2 (Pin 5) | B5 (Pin 28) | B5 (Pin 28) | LD3 (IF2-pin 5) |
| 5 | 166 | FP8 | Data | | | | G2 (Pin 14) | G2 (Pin 14) | LD4 (IF2-pin 6) |
| 6 | 167 | FP9 | Data | G0 (CN1-p 9) | G0 (Pin 10) | G0 (Pin 21) | G3 (Pin 16) | G3 (Pin 16) | LD5 (IF2-pin 7) |
| 7 | 168 | FP10 | Data | G1 (CN1-p11) | G1 (Pin 12) | G1 (Pin 19) | G4 (Pin 17) | G4 (Pin 17) | LD6 (IF2-pin 8) |
| 8 | 169 | FP11 | Data | G2 (CN1-p13) | G2 (Pin 13) | G2 (Pin 17) | G5 (Pin 18) | G5 (Pin 18) | LD7 (IF2-pin 9) |
| 9 | 172 | FP13 | Data | | | | R1 (Pin 5) | R1 (Pin 5) | UD7 (IF1-pin 15) |
| 10 | 170 | FP12 | Data | | | | R0 (Pin 4) | R0 (Pin 4) | UD6 (IF1-pin 14) |
| 11 | 164 | FP7 | Data | | | | G1 (Pin 13) | G1 (Pin 13) | UD5 (IF1-pin 13) |
| 12 | 163 | FP6 | Data | | | | G0 (Pin 12) | G0 (Pin 12) | UD4 (IF1-pin 12) |
| 13 | 176 | FP17 | Data | R2 (CN1-p7) | R2 (Pin 22) | R2 (Pin 7) | R5 (Pin 10) | R5 (Pin 10) | UD3 (IF1-pin 11) |
| 14 | 175 | FP16 | Data | R1 (CN1-p 5) | R1 (Pin 21) | R1 (Pin 9) | R4 (Pin 9) | R4 (Pin 9) | UD2 (IF1-pin 10) |
| 15 | 174 | FP15 | Data | R0 (CN1-p3) | R0 (Pin 20) | R0 (Pin 11) | R3 (Pin 8) | R3 (Pin 8) | UD1 (IF1-pin 9) |
| 16 | 173 | FP14 | Data | | | | R2 (Pin 6) | R2 (Pin 6) | UD0 (IF1-pin 8) |
| 18 | 155 | FPVDCLK | Shift Clock | NCLK (CN1-p1) | CK (Pin 25) | NCLK (Pin 3) | NCLK (Pin 2) | NCLK (Pin 2) | SCP (IF1-pin 3) |
| 20 | 131 | FP18 | Data | | | | | | FP (IF1-pin 1) |
| 22 | 156 | LFS | Frame Clock | | | | | | |
| 23 | 158 | FP1 | Data | | | | B1 (Pin 23) | B1 (Pin 23) | |
| 24 | | | *Spare* | | | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | | |
| 26 | 152 | FPDE | Display Enable | | | | ENAB (Pin 20) | ENAB (Pin 20) | |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | | |
| 28 | - | VEE | Switched NEG | | | | | | |
| 29 | 132 | FP19 | Data | | | | | | |
| 30 | - | VBB | Switched POS | | | | | | |
| 31 | - | VBKLT | Backlight (+12) | Backlight | Backlight | Backlight | Backlight | Backlight | Backlight |
| 32 | - | SWVDD | Switched Logic | VDD (CN2-P9 & 10) | VDD (Pins 14, 15, & 16) | VDD (Pins 1 & 24) | VDD (Pin 30 & 31) | VDD (Pin 30 & 31) | VDD (IF1-pin 5) |
| 33 | 146 | FP31 | Data | ENAB (CN2-P7) | ENAB (Pin 23) | ENAB (Pin 23) | | | |
| 35 | 153 | LLCLK | Line clock | | | | | | LP (IF1-pin 2) |
| 37 | 123 | FPVEE | VEE Enable | | | | | | DISP (IF1-pin 4) |
| 38 | 125 | FPVCC | VCC Enable | | | | | | |
| 39 | 157 | FP0 | Data | | | | B0 (Pin 22) | B0 (Pin 22) | |
| 40 | - | CONTPOS | Switched + Contrast | | | | | | VEE (IF1-pin 7) |
| 41 | - | CONTNEG | Switched - Contrast | | | | | | |
| 42 | 139 | FP25 | Data | | | | | | |
| 43 | 145 | FP30 | Data | | | | | | |
| 44 | 138 | FP24 | Data | | | | | | |
| 17,19,21,34,36 | - | Ground | | GND (CN1-P2,4,6,8,10,12,14) | GND (Pins 1, 6, 11, 19, 24, 29) | GND (Pins 2, 4, 6, 8, 10, 12) | GND (Pin 1, 3, 7, 11, 15) | GND (Pin 1, 3, 7, 11, 15) | VSS (IF1-pin 6) |
| (16 Pin) 1 & 16 | - | Ground | | GND (CN2-P4,4,6,8) | | GND (Pins 14, 16, 18, 20, 22) | GND (Pin 19, 21, 25, 29) | GND (Pin 19, 21, 25, 29) | VSS (IF2-pins 1 & 10) |
| 2 | 133 | FP20 | Data 133 | | | | | | |
| 3 | 135 | FP21 | Data 135 | | | | | | |
| 4 | 136 | FP22 | Data 136 | | | | | | |
| 5 | 137 | FP23 | Data 137 | | | | | | |
| 6 | 140 | FP26 | Data 140 | | | | | | |
| 7 | 141 | FP27 | Data 141 | | | | | | |
| 9 | 143 | FP28 | Data 143 | | | | | | |
| 10 | 144 | FP29 | Data 144 | | | | | | |
| 11 | 147 | FP32 | Data 147 | | | | | | |
| 12 | 148 | FP33 | Data 148 | | | | | | |
| 13 | 149 | FP34 | Data 149 | | | | | | |
| 14 | 150 | FP35 | Data 150 | | | | | | |
| 8 | - | Unused | | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | "+5 VDC" | "+5 VDC" | "+5 VDC" | "+5 VDC" | "+5 VDC" | "+ 25 VDC" |
| Notes ? | | | | NO | NO | NO | NO | NO | NO |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P | CL-GD755x | | | Toshiba | Toshiba | Toshiba | Toshiba | Toshiba | Toshiba |
|---|---|---|---|---|---|---|---|---|---|
| | | | | TLX-807 2S-C3X | TLX-810 2S-C3X | TLX-812 2S-C3X | TLX-813 2S-C3X | TLX-813 4S-C3X | TLX-813 7S-C3X |
| | | | | 640 x 480 | 640 x 480 | 640 x 480 | 640 x 480 | 640 x 480 | 640 x 480 |
| Pin #'s | Pin #'s | Pin Name | Description | C8SSID-8 | C8DD-16 | C8DD-16 | C8DD-16 | C8DD-16 | C8DD-16 |
| 1 | 159 | FP2 | Data | D7 (CN1 - pin 2) | LD0 (CN2-pin 2) | LD0 (CN2-pin 2) | LD0 (pin 13) | LD0 (IF2-pin 2) | LD0 (pin 11) |
| 2 | 160 | FP3 | Data | D6 (CN1 - pin 3) | LD1 (CN2-pin 3) | LD1 (CN2-pin 3) | LD1 (pin 15) | LD1 (IF2-pin 3) | LD1 (pin 13) |
| 3 | 161 | FP4 | Data | D5 (CN1 - pin 4) | LD2 (CN2-pin 4) | LD2 (CN2-pin 4) | LD2 (pin 16) | LD2 (IF2-pin 4) | LD2 (pin 17) |
| 4 | 162 | FP5 | Data | D4 (CN1 - pin 5) | LD3 (CN2-pin 5) | LD3 (CN2-pin 5) | LD3 (pin 17) | LD3 (IF2-pin 5) | LD3 (pin 19) |
| 5 | 166 | FP8 | Data | D3 (CN1 - pin 6) | LD4 (CN2-pin 6) | LD4 (CN2-pin 6) | LD4 (pin 19) | LD4 (IF2-pin 6) | LD4 (pin 1) |
| 6 | 167 | FP9 | Data | D2 (CN1 - pin 7) | LD5 (CN2-pin 7) | LD5 (CN2-pin 7) | LD5 (pin 20) | LD5 (IF2-pin 7) | LD5 (pin 3) |
| 7 | 168 | FP10 | Data | D1 (CN1 - pin 8) | LD6 (CN2-pin 8) | LD6 (CN2-pin 8) | LD6 (pin 21) | LD6 (IF2-pin 8) | LD6 (pin 5) |
| 8 | 169 | FP11 | Data | D0 (CN1 - pin 9) | LD7 (CN2-pin 9) | LD7 (CN2-pin 9) | LD7 (pin 23) | LD7 (IF2-pin 9) | LD7 (pin 7) |
| 9 | 172 | FP13 | Data | | UD7 (CN1-pin 15) | UD7 (CN1-pin 15) | UD7 (pin 12) | UD7 (IF1-pin 15) | UD7 (pin 31) |
| 10 | 170 | FP12 | Data | | UD6 (CN1-pin 14) | UD6 (CN1-pin 14) | UD6 (pin 11) | UD6 (IF1-pin 14) | UD6 (pin 29) |
| 11 | 164 | FP7 | Data | | UD5 (CN1-pin 13) | UD5 (CN1-pin 13) | UD5 (pin 9) | UD5 (IF1-pin 13) | UD5 (pin 25) |
| 12 | 163 | FP6 | Data | | UD4 (CN1-pin 12) | UD4 (CN1-pin 12) | UD4 (pin 8) | UD4 (IF1-pin 12) | UD4 (pin 23) |
| 13 | 176 | FP17 | Data | | UD3 (CN1-pin 11) | UD3 (CN1-pin 11) | UD3 (pin 7) | UD3 (IF1-pin 11) | UD3 (pin 22) |
| 14 | 175 | FP16 | Data | | UD2 (CN1-pin 10) | UD2 (CN1-pin 10) | UD2 (pin 5) | UD2 (IF1-pin 10) | UD2 (pin 24) |
| 15 | 174 | FP15 | Data | | UD1 (CN1-pin 9) | UD1 (CN1-pin 9) | UD1 (pin 4) | UD1 (IF1-pin 9) | UD1 (pin 26) |
| 16 | 173 | FP14 | Data | | UD0 (CN1-pin 8) | UD0 (CN1-pin 8) | UD0 (pin 3) | UD0 (IF1-pin 8) | UD0 (pin 28) |
| 18 | 155 | FPVDCLK | Shift Clock | XCKL (CN2 - pin 3) | SCP (CN1-pin 3) | SCP (CN1-pin 3) | SCP(pin 27) | SCP (IF1-pin 3) | SCP(pin 10) |
| 20 | 131 | FP18 | Data | | | | | | |
| 22 | 156 | LFS | Frame Clock | FP (CN2 - pin 1) | FP (CN1-pin 1) | FP (CN1-pin 1) | FP (pin 24) | FP (IF1-pin 1) | FP (pin 4) |
| 23 | 158 | FP1 | Data | | | | | | |
| 24 | | | *Spare* | | | | | | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | | | | | | |
| 26 | 152 | FPDE | Display Enable | XCKU (CN2 - pin 8) | | | | | |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | | | | | | |
| 28 | - | VEE | Switched NEG | | | | | | |
| 29 | 132 | FP19 | Data | | | | | | |
| 30 | - | VBB | Switched POS | | | | | | |
| 31 | - | VBKLT | Backlight (+12) | Backlight | Backlight | Backlight | Backlight | Backlight | Backlight |
| 32 | - | SWVDD | Switched Logic | VDD (CN2 - pins 5, 7) | VDD (CN1-pin 5) | VDD (CN1-pin 5) | VDD (pin 1) | VDD (IF1-pin 5) | VDD (pin 14 &16) |
| 33 | 146 | FP31 | Data | | | | | | |
| 35 | 153 | LLCLK | Line clock | LP (CN2 - pin 2) | LP (CN1-pin 2) | LP (CN1-pin 2) | LP (pin 25) | LP (IF1-pin 2) | LP (pin 6) |
| 37 | 123 | FPVEE | VEE Enable | | DISP (CN1-pin 4) | DISP (CN1-pin 4) | DISP (pin 28) | DISP (IF1-pin 4) | DISP (pin 18) |
| 38 | 125 | FPVCC | VCC Enable | | | | | | |
| 39 | 157 | FP0 | Data | | | | | | |
| 40 | - | CONTPOS | Switched + Contrast | | VEE (CN1-pin 7) | VEE (CN1-pin 7) | VEE (pin 30) | VCONT (I/F 1 Pin 6) ***2 VDC*** | VCONT (pin 12) ***2 VDC*** |
| 41 | - | CONTNEG | Switched - Contrast | | | | | | |
| 42 | 139 | FP25 | Data | | | | | | |
| 43 | 145 | FP30 | Data | | | | | | |
| 44 | 138 | FP24 | Data | | | | | | |
| 17,19,21,34,36 | - | Ground | | GND (CN1 - pins 1, 10) | VSS (CN1-pin 6) | VSS (CN1-pin 6) | VSS (pins 2, 6, 10, 14) | VSS (IF2-pins 1 & 10) | VSS (pins 2, 8, 9, 15) |
| (16 Pin) 1 & 16 | - | Ground | | GND (CN2 - pins 4, 6) | VSS (CN2-pins 1 & 10) | VSS (CN2-pins 1 & 10) | VSS (pins 18, 22, 26, 29) | | VSS (pins 21, 27, 30 ) |
| 2 | 133 | FP20 | Data 133 | | | | | | |
| 3 | 135 | FP21 | Data 135 | | | | | | |
| 4 | 136 | FP22 | Data 136 | | | | | | |
| 5 | 137 | FP23 | Data 137 | | | | | | |
| 6 | 140 | FP26 | Data 140 | | | | | | |
| 7 | 141 | FP27 | Data 141 | | | | | | |
| 9 | 143 | FP28 | Data 143 | | | | | | |
| 10 | 144 | FP29 | Data 144 | | | | | | |
| 11 | 147 | FP32 | Data 147 | | | | | | |
| 12 | 148 | FP33 | Data 148 | | | | | | |
| 13 | 149 | FP34 | Data 149 | | | | | | |
| 14 | 150 | FP35 | Data 150 | | | | | | |
| 8 | - | Unused | | | | | | | |
| Required Voltage (See Demo Board App Notes) | | | | + 5 VDC | "+ 25 VDC" | "+ 5 VDC" | "+ 25 VDC" | ***+2.0 VDC*** | ***+2.0 VDC*** |
| Notes ? | | | | NO | NO | NO | NO | Use 10M and 1M resistor on VCONT | Use 10M and 1M resistor on VCONT |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

# CL-GD7555 Panel Interface Connection Table



| DB-44 Maxon # MDH-BA-44P Pin #'s | CL-GD755x Pin #'s | CL-GD755x Pin Name | CL-GD755x Description | Toshiba TLX-814 2S-C3X 800 x 600 C6DD-16 |
|---|---|---|---|---|
| 1 | 159 | FP2 | Data | LD0 (pin 13) |
| 2 | 160 | FP3 | Data | LD1 (pin 15) |
| 3 | 161 | FP4 | Data | LD2 (pin 16) |
| 4 | 162 | FP5 | Data | LD3 (pin 17) |
| 5 | 166 | FP8 | Data | LD4 (pin 19) |
| 6 | 167 | FP9 | Data | LD5 (pin 20) |
| 7 | 168 | FP10 | Data | LD6 (pin 21) |
| 8 | 169 | FP11 | Data | LD7 (pin 23) |
| 9 | 172 | FP13 | Data | UD7 (pin 12) |
| 10 | 170 | FP12 | Data | UD6 (pin 11) |
| 11 | 164 | FP7 | Data | UD5 (pin 9) |
| 12 | 163 | FP6 | Data | UD4 (pin 8) |
| 13 | 176 | FP17 | Data | UD3 (pin 7) |
| 14 | 175 | FP16 | Data | UD2 (pin 5) |
| 15 | 174 | FP15 | Data | UD1 (pin 4) |
| 16 | 173 | FP14 | Data | UD0 (pin 3) |
| 18 | 155 | FPVDCLK | Shift Clock | SCP(pin 27) |
| 20 | 131 | FP18 | Data | |
| 22 | 156 | LFS | Frame Clock | FP (pin 24) |
| 23 | 158 | FP1 | Data | |
| 24 | | | *Spare* | |
| 25 | 114 | *VSYNC* | *CRT VSYNC* | |
| 26 | 152 | FPDE | Display Enable | |
| 27 | 112 | *HSYNC* | *CRT HSYNC* | |
| 28 | - | VEE | Switched NEG | |
| 29 | 132 | FP19 | Data | |
| 30 | - | VBB | Switched POS | |
| 31 | - | VBKLT | Backlight (+12) | Backlight |
| 32 | - | SWVDD | Switched Logic | VDD (pin 1) |
| 33 | 146 | FP31 | Data | FR (Pin 26) |
| 35 | 153 | LLCLK | Line clock | LP (pin 25) |
| 37 | 123 | FPVEE | VEE Enable | DISP (pin 28) |
| 38 | 125 | FPVCC | VCC Enable | |
| 39 | 157 | FP0 | Data | |
| 40 | - | CONTPOS | Switched + Contrast | VCONT (pin 30) ***2 VDC*** |
| 41 | - | CONTNEG | Switched - Contrast | |
| 42 | 139 | FP25 | Data | |
| 43 | 145 | FP30 | Data | |
| 44 | 138 | FP24 | Data | |
| 17,19,21,34,36 | - | Ground | | VSS (pins 2, 6, 10, 14) |
| (16 Pin) 1 & 16 | - | Ground | | VSS (pins 18, 22, & 29) |
| 2 | 133 | FP20 | Data 133 | |
| 3 | 135 | FP21 | Data 135 | |
| 4 | 136 | FP22 | Data 136 | |
| 5 | 137 | FP23 | Data 137 | |
| 6 | 140 | FP26 | Data 140 | |
| 7 | 141 | FP27 | Data 141 | |
| 9 | 143 | FP28 | Data 143 | |
| 10 | 144 | FP29 | Data 144 | |
| 11 | 147 | FP32 | Data 147 | |
| 12 | 148 | FP33 | Data 148 | |
| 13 | 149 | FP34 | Data 149 | |
| 14 | 150 | FP35 | Data 150 | |
| 8 | - | Unused | | |
| Required Voltage (See Demo Board App Notes) | | | | ***+2.0 VDC*** |
| Notes ? | | | | Use 10M and 1M resistor on VCONT |



**Caution: When making connections, reference the CL-GD7555X pin *numbers* (and not pin *names*).**

## Direct Sales Offices

### *Domestic*

**N. CALIFORNIA**
Fremont
TEL: 510/623-8300
FAX: 510/252-6020

**S. CALIFORNIA**
Westlake Village
TEL: 805/371-5860
FAX: 805/371-5861

**NORTHWESTERN AREA**
Portland, OR
TEL: 503/620-5547
FAX: 503/620-5665

**SOUTH CENTRAL AREA**
Austin, TX
TEL: 512/255-0080
FAX: 512/255-0733

Irving, TX
TEL: 972/252-6698
FAX: 972/252-5681

Houston, TX
TEL: 281/257-2525
FAX: 281/257-2555

**NORTHEASTERN AREA**
Andover, MA
TEL: 978/794-9992
FAX: 978/794-9998

**SOUTHEASTERN AREA**
Raleigh, NC
TEL: 919/859-5210
FAX: 919/859-5334

Boca Raton, FL
TEL: 561/241-2364
FAX: 561/241-7990

### *International*

**CHINA**
Beijing
TEL: 86/10-6428-0783
FAX: 86/10-6428-0786

**FRANCE**
Paris
TEL: 33/1-48-12-2812
FAX: 33/1-48-12-2810

**GERMANY**
Herrsching
TEL: 49/81-52-92460
FAX: 49/81-52-924699

**HONG KONG**
Tsimshatsui
TEL: 852/2376-0801
FAX: 852/2375-1202

**ITALY**
Milan
TEL: 39/2-3360-5458
FAX: 39/2-3360-5426

**JAPAN**
Tokyo
TEL: 81/3-3340-9111
FAX: 81/3-3340-9120

**KOREA**
Seoul
TEL: 82/2-565-8561
FAX: 82/2-565-8565

**SINGAPORE**
TEL: 65/743-4111
FAX: 65/742-4111

**TAIWAN**
Taipei
TEL: 886/2-2718-4533
FAX: 886/2-2718-4526

**UNITED KINGDOM**
London, England
TEL: 44/1727-872424
FAX: 44/1727-875919

## High-Value Systems in Silicon

Cirrus Logic is a premier supplier of system-level integrated circuits that demand high-performance mixed-signal processing. Our company's software-rich 'systems in silicon' add high value to major brands worldwide. We apply our system expertise to enable high-volume applications in data storage, networking, and multimedia for both computing and consumer electronics markets as well as ultra-high-precision data acquisition applications for industrial automation and instrumentation markets.

Cirrus Logic's manufacturing strategy ensures maximum product quality and availability, as well as access to world-class processing technologies through joint ventures with IBM® and Lucent Technologies®.

Contact one of our systems and applications specialists to see how your company can benefit from the high value Cirrus Logic adds to its customers' products.



**Cirrus Logic, Inc.**
3100 West Warren Ave., Fremont, CA 94538
TEL: 510/623-8300 FAX: 510/252-6020

***Publications Ordering:*** 800/359-6414 (USA) or 510/249-4200
***Worldwide Web:*** http://www.cirrus.com
367555-001