Acumos VGA Video Controller
AVGA1

OVERVIEW

The AVGA1 Video Controller realizes the most highly integrated, single-chip VGA video system available today. Incorporating a built-in Video DAC, Clock Synthesizer, and all System Bus and Feature Connector interface support, the AVGA1 is foremost in cost-sensitive, space-limited applications. With the addition of only two 256K x 4 DRAMs, plus passive components, the VGA video system is complete.

FEATURES

- Full **IBM® VGA** compatibility in a 128-pin Plastic Quad Flat Pack (PQFP) package
- Built-in **VIDEO DAC**. *The video outputs connect directly to an IBM® PS/2™ or compatible analog display. No external color look-up table or display interface support is required.*
- Built-in **CLOCK SYNTHESIZER**, *generating all timing from the 14 MHz clock supplied by the System Bus interface. No additional external oscillators are required.*
- Selectable internally generated memory timing clock of 37.5 MHz for 80ns DRAM or 44.7 MHz for high-performance 70ns DRAMs.
- Built-in **MONITOR TYPE DETECTION** circuit.
- Connects *directly* to the **MICRO CHANNEL™** or **PC/XT/AT** System Bus, and **VIDEO FEATURE CONNECTOR**, *and requires no additional interface support logic or buffers*
- Video circuit complete with the addition of passive components and two 256K x 4 DRAMs
- Supports **16-bit Video Memory** read/write cycles *in all video modes*
- ***Waitless Write*** cycles to Video Memory maximize access by the System Processor, by combining a **MEMORY WRITE DATA FIFO** and **ZERO WAIT STATE** (AT Bus) request capability.
- Dual-ported memory access control, rapidly prefetching video memory data into a **DISPLAY DATA FIFO** while allowing the System Processor optimum access time to the display buffer
- Supports **16-bit I/O** read/write cycles to I/O ports, *for enhanced performance.*
- Supports **8- or 16-bit BIOS ROM** implementations
- **ZERO WAIT STATE** (AT Bus) request capability for BIOS ROM Memory access cycles.
- 132-column Alphanumeric Mode, *using an internally generated 41 MHz dot clock*
- 800 x 600 x 16 color Graphics Mode, *using an internally generated 36 MHz dot clock*

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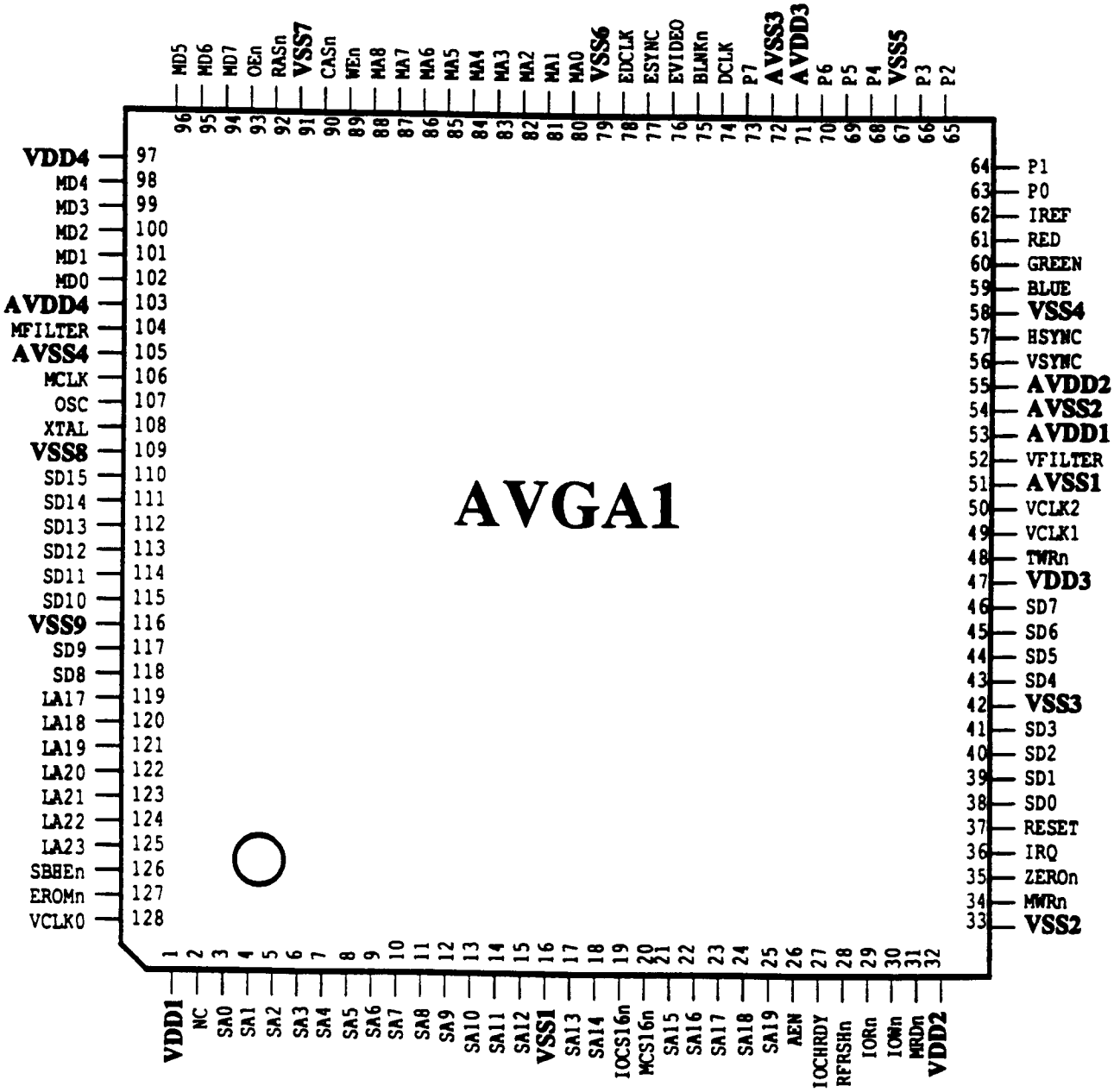


AVGA1 Pin-Out

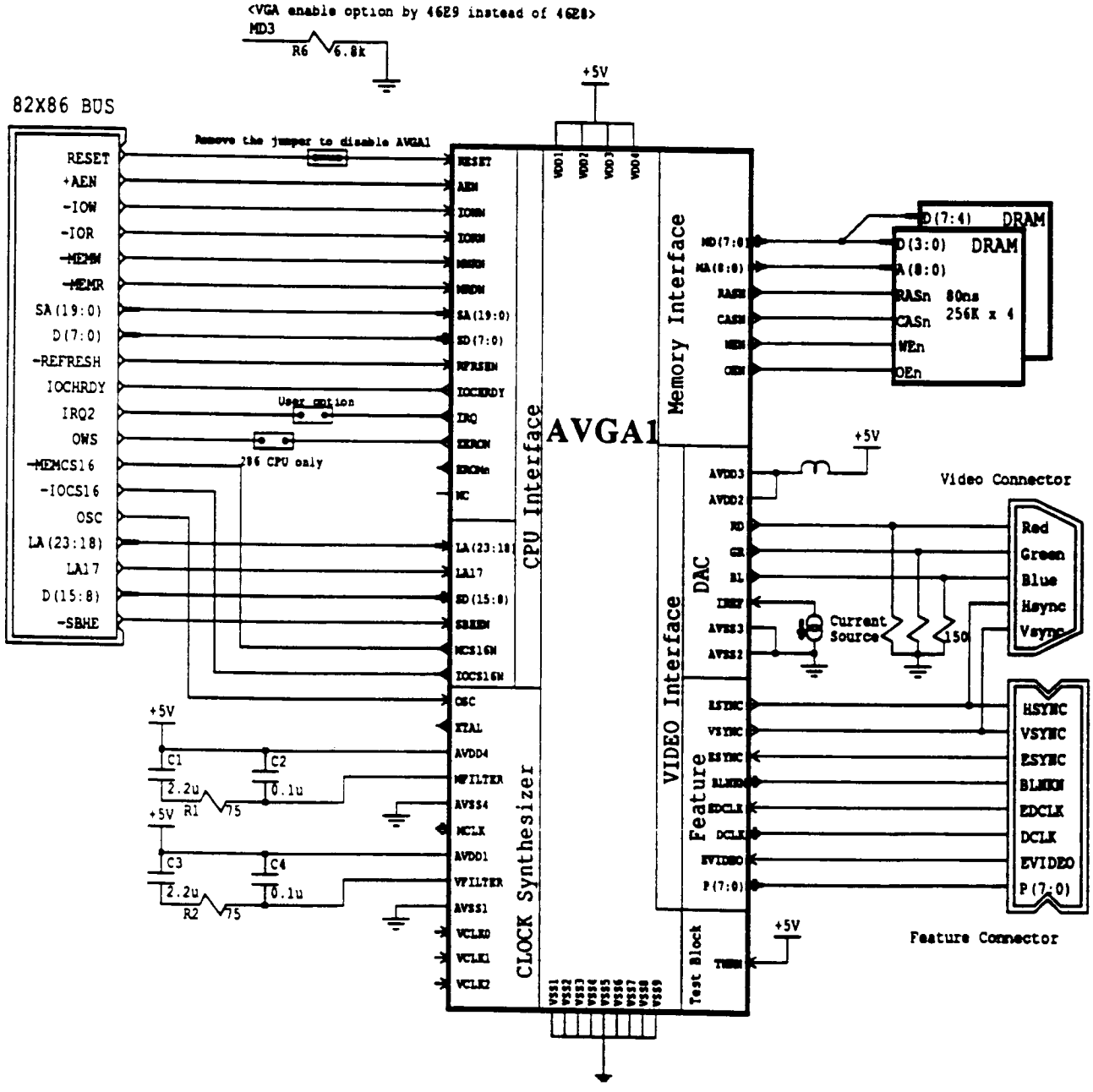


FIGURE 1 **AT Mother-board Implementation**

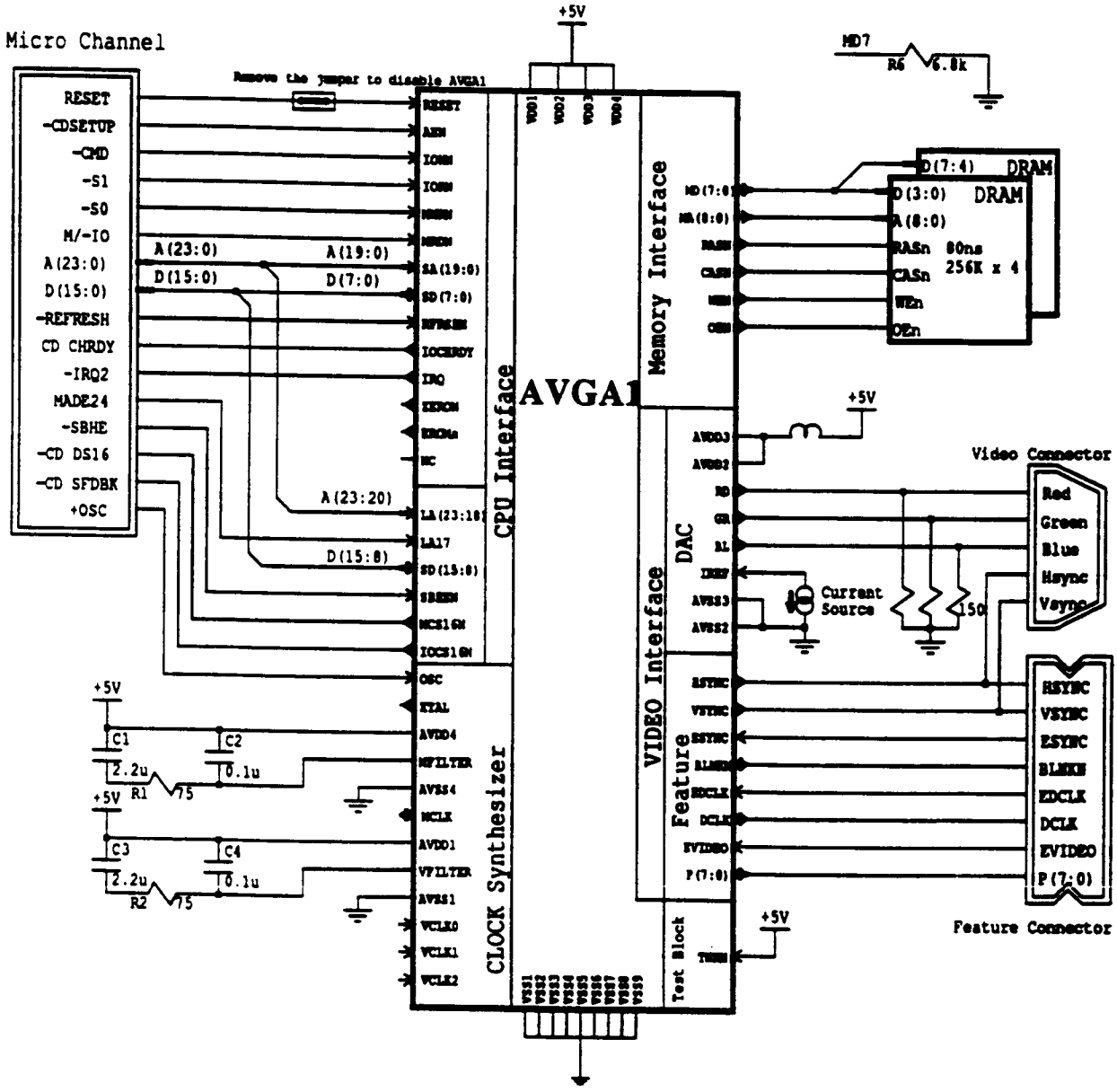


FIGURE 2 **MCA Implementation**

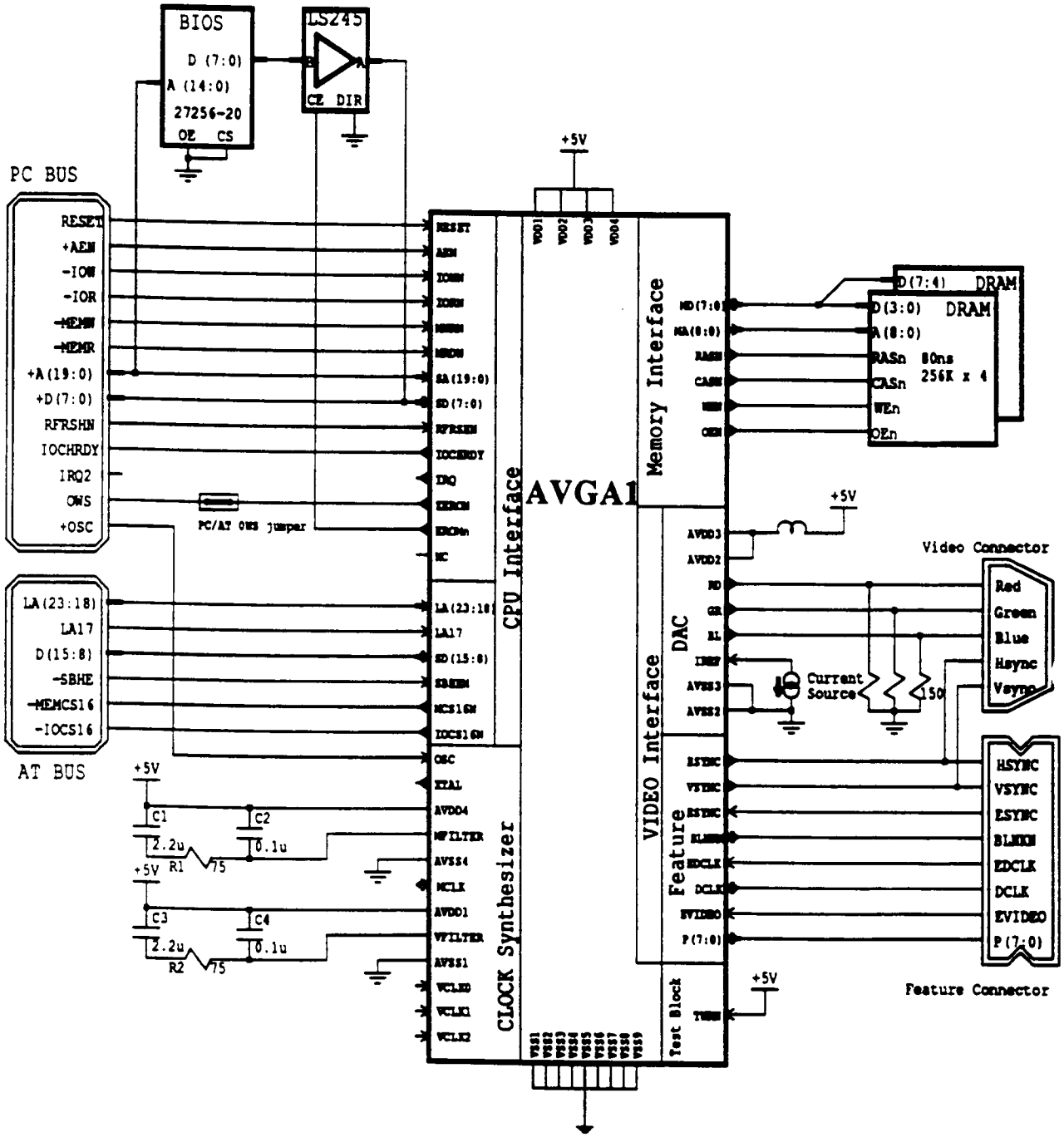


FIGURE 3 **PC/AT add-in 8 bit BIOS**

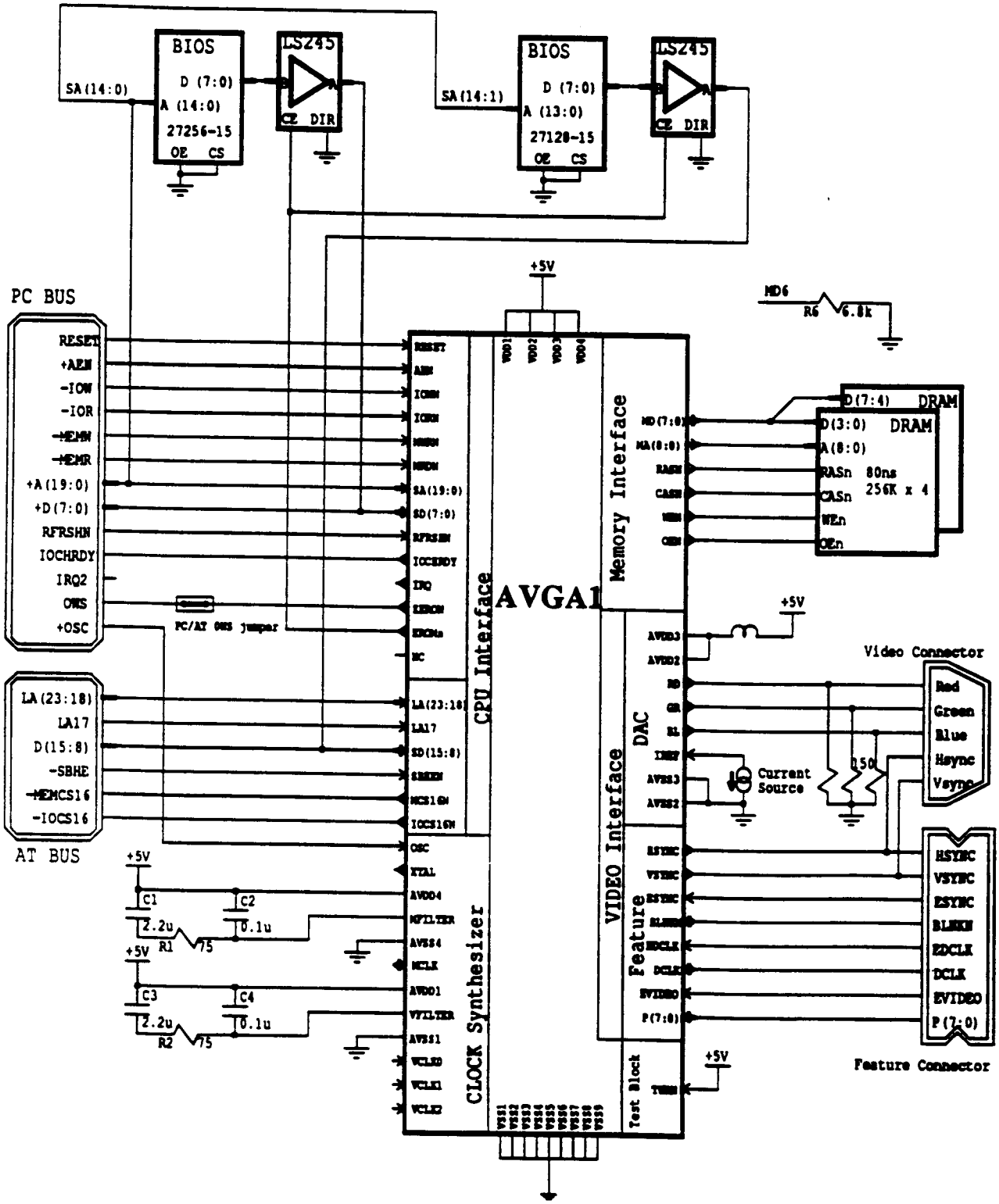


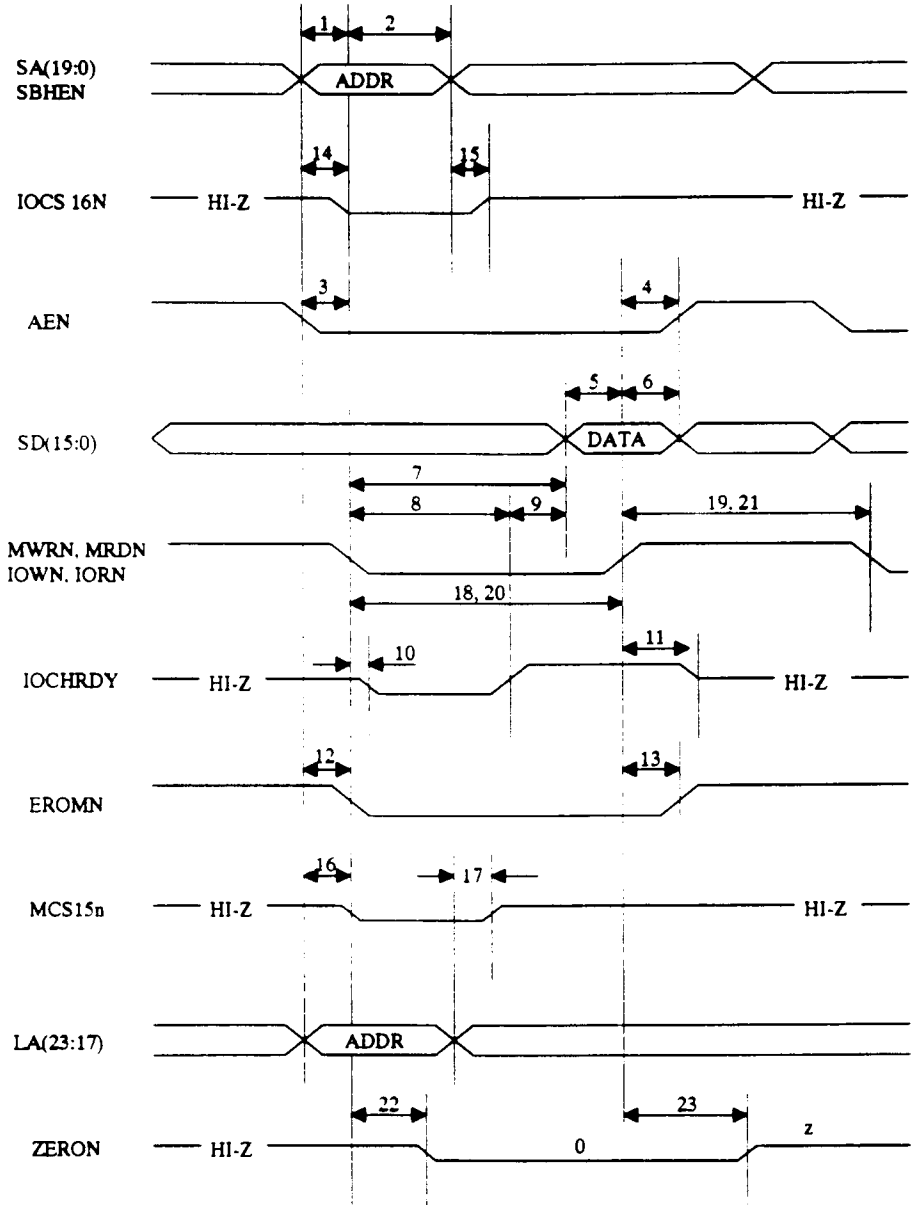
FIGURE 4 **PC/AT add-in 16 bit BIOS**

ABSOLUTE MAXIMUM RATINGS	
Supply voltage, VDD	7V
Voltage, from any pin to VSS	-0.5 to +7V
Operating free-air temperature range	0° C to 70° C
Storage temperature range	-65° C to 150° C
Power Dissipation	2 Watt

D.C. CHARACTERISTICS

(0° C to 70° C)

PARAMETER		MIN	NOM	MAX	UNIT
VDD	Supply voltage	4.75	5.00	5.25	V
IDD	Power supply current			260	mA
VIH	High-level input voltage	2.0		VDD + 0.5	V
VIL	Low-level input voltage	-0.5		0.8	V
IIH	High-level input current (VIL=VDD)			10	uA
IIL	Low-level input current (VDD=5.25V; VIL=-0.5V)			-0.05	mA
VOH	High-level output voltage	2.4		VDD	V
VOL	Low-level output voltage	VSS		0.4	V
IOH, IOL	High-level, low-level output current			See PIN DESCRIPTIONS	
IOZ	Output Leakage Current (VOH=VDD; VOL=VSS)			± 10	uA
VREF	DAC Output Level Comparator Voltage Reference (internal)	320	337	354	mV



AT Mode Bus Interface Timing

A.C. TIMING CHARACTERISTICS
AT Mode Bus Interface

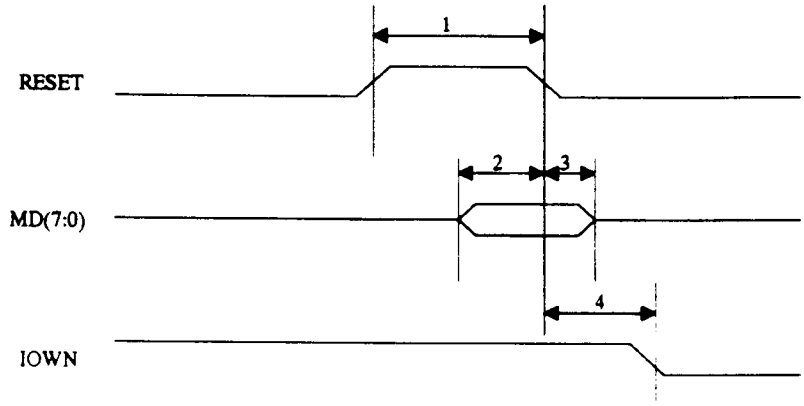
Parameter	Minimum	Maximum
1a. sa(19:0) setup to mrdn, mwrn low	20ns	---
1b. sa(19:0) setup to iorn, iown low	15ns	---
1c. sbhen setup to mrdn, mwrn, iorn, iown	5ns	---
2a. sa(19:0) hold from to mrdn, mwrn low	15ns	---
2b. sa(19:0) hold from iorn, iown low	18ns	---
2c. sbhen hold from mrdn, mwrn, iorn, iown	5ns	---
3. aen setup to iorn/iown low	16ns	---
4. aen hold from iorn/iown high	5ns	---
5. sd(15:0) write data setup to iown high	5ns	---
6a. sd(15:0) read data hold from iorn high	---	28ns
6b. sd(15:0) read data hold from mrdn high	---	20ns
6c. sd(15:0) write data hold from iown high	15ns	---
6d. sd(15:0) write data hold after mwrn high	10ns	---
7a. sd(15:0) read data valid from iorn low	---	60ns (240pf load)
7b. sd(15:0) write data valid after mwrn low		3t
8. iochrdy high from mwrn/mrdn low	8.7ns	
9. Memory read data valid from iochrdy high	---	15ns (240pf load)
10. iochrdy low from mwrn/mrdn low	9ns	39ns (240pf load)
11. iochrdy tristate from mwrn/mrdn high	4ns	12ns (240pf load)
12. eromn low from valid a(23:15)	---	42ns (20pf load)
13. eromn hold from mrdn high	---	20ns (20pf load)
14. sa(19:0) valid to iocs16 low	---	60ns (240pf load)
15. iocs16 hold from sa(19:0)	---	23ns (240pf load)
16. La(23:17) valid to memcs16 low	---	70ns (240pf load)
17. memcs16 hold from La(23:17)	---	17ns (240pf load)
18. iown low	90ns	
19. iown high	80ns	

AT Mode Bus Interface (continued)		
Parameter	**Minimum**	**Maximum**
20. mwrn low	3t	
21. mwrn high	3t	
22a. mrdn low to zeron low (BIOS rom access)	5.6ns	21.6ns
22b. mrdn low to zeron low (vid. mem access)	6t + 20ns	100t
22c. mwrn low to zeron low (iochrdy high)	5.7ns	21.8ns
23a. mrdn high to zeron tristate (BIOS rom access)	4.5ns	17.6ns
23b. mrdn high to zeron tristate (vid. mem access)	5.0ns	19ns

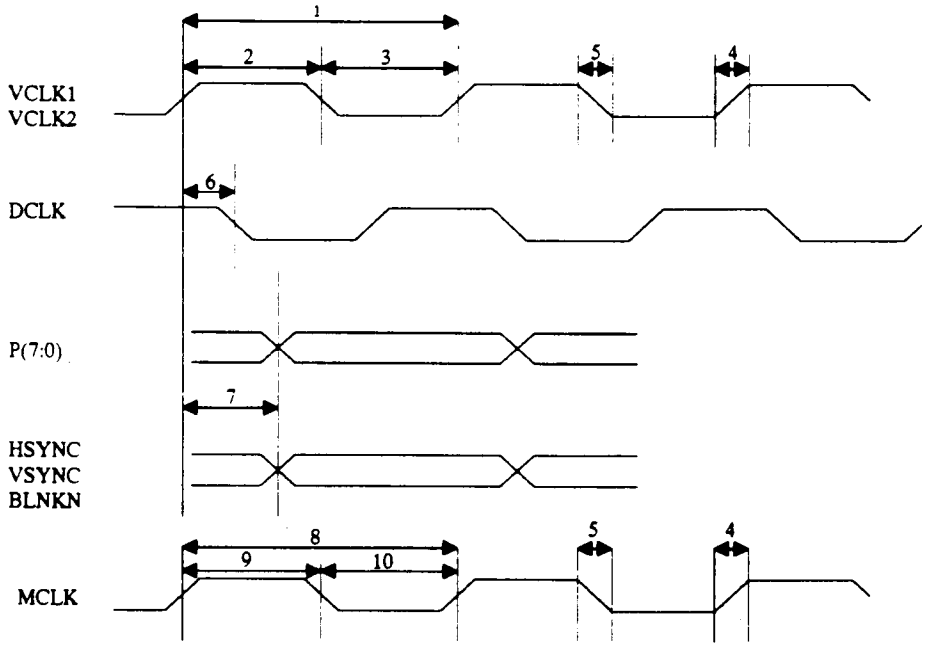
Note: t=MCLK period (26.6ns or 22.3ns)

Clock Timing		
Parameter	**Minimum**	**Maximum**
1. VCLK1,VCLK2 period	24ns	---
2. VCLK1, VCLK2 high	9ns	---
3. VCLK1, VCLK2 low	9ns	---
4. Clock Rise time	---	3ns
5. Clock Fall time	---	3ns
6. VCLK to DCLK delay	9.3ns	36ns (50pf load)
7a. VCLK to Hsync, Vsync or Blnkn delay	9.8ns	36ns (150pf load)
7b. VCLK to P(7:0) delay	8.5ns	37ns (50pf load)
8. MCLK period	22ns	---
9. MCLK High	10ns	---
10. MCLK Low	10ns	---

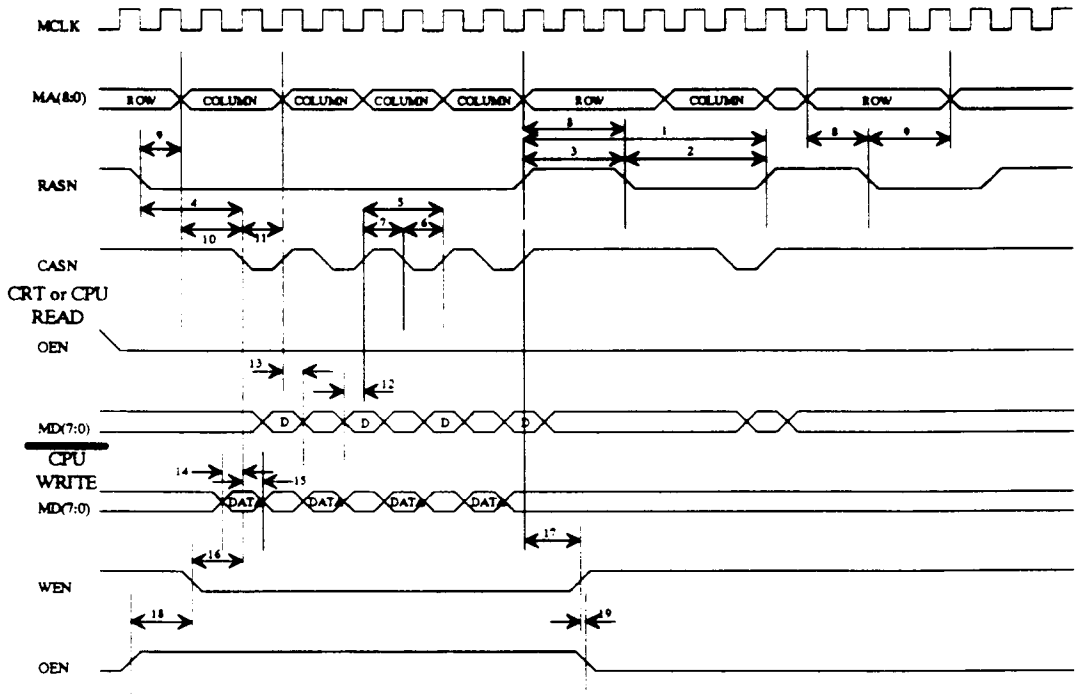
Note: Timing reference is for VCLK1 or VCLK2 used as inputs for external video clocks.



Reset Timing



Clock Timing


MCLK
MA(8:0)
ROW
COLUMN
RASN
CASN
CRT or CPU READ
OEN
MD(7:0)
CPU WRITE
DAT
WEN

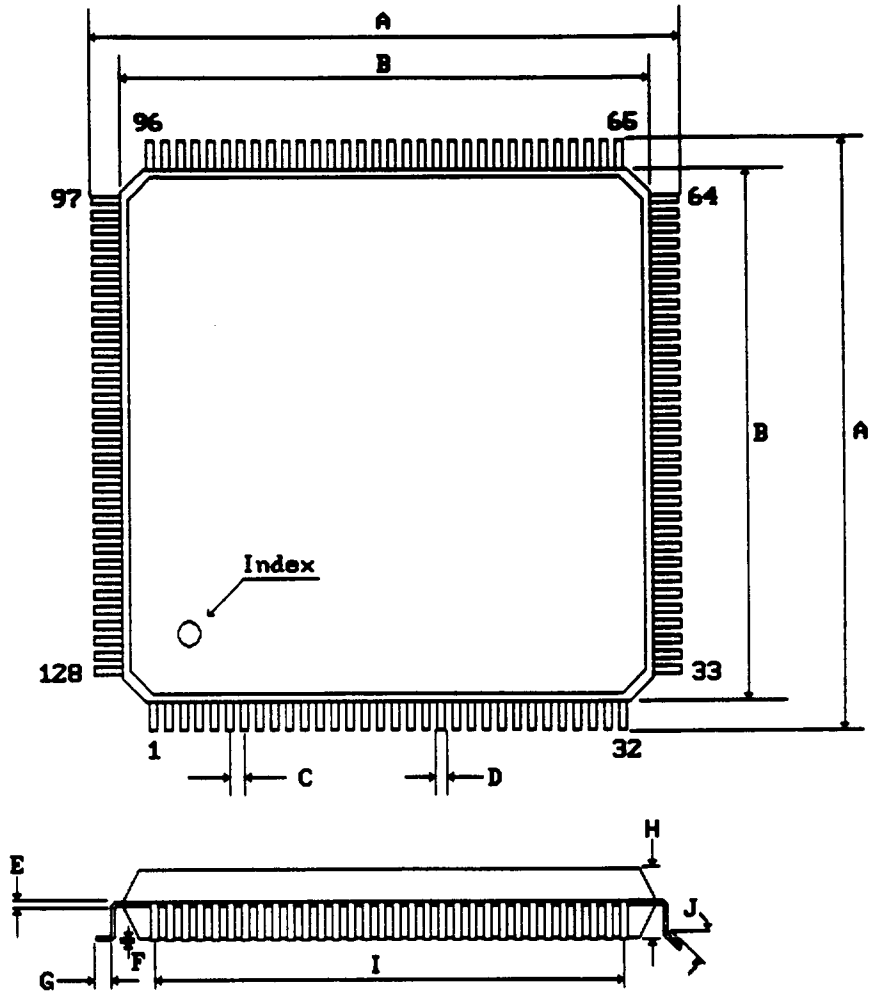
DRAM Timing

DRAM Timing		
Parameter	**Minimum**	**Maximum**
1. RASN cycle time	6t	6t
2. RASN pulse width low	3.5t - 13.2ns	
3. RASN high time (precharge)	2.5t + 4ns	
4. RASN low to CASN low	2.5t - 8.4ns	2.5t - 2.9ns
5. CASN cycle time	2t	2t
6. CASN pulse width low	1t	1t
7. CASN high time (precharge)	1t	1t
8. Row address setup to RASN low	1.5t	1.5t
9. Row address hold time to RASN low	1t	1t
10. Column address setup to CASN low	1t	1.5t - 8.9ns
11. Column address hold to CASN low	1t + 1ns	1t + 6.2ns
12. Read Data valid before CASN high	0ns	---
13. Read Data hold after CASN high	10ns	---
14. Write Data setup to CASN low	1t	2t
15. Write Data hold after CASN low	1t	1t
16. WE0N low setup CASN low	2t	2t
17. WE0N low hold after CASN high	1t	1t
18. OEN high before WE0N low	1t	1t
19. OEN low after WE0N high	1ns	4ns

Notes: All outputs have 20pf loading

Reset Timing		
Parameter	**Minimum**	**Maximum**
1. minimum reset width	12t	---
2. set-up time between mdi and reset	10ns	---
3. hold time between mdi and reset	20ns	---
4. Reset low to first iown	12t	---

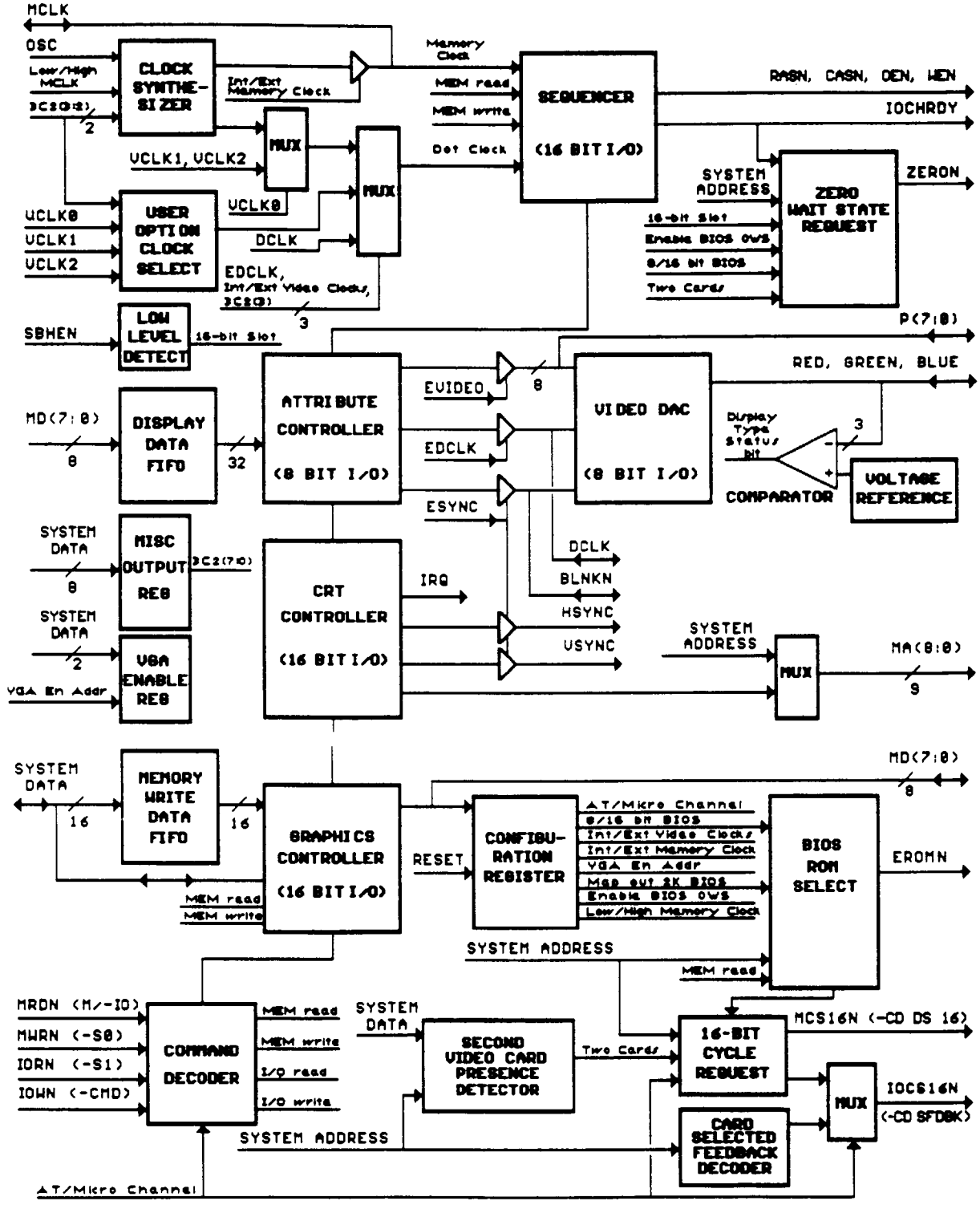
PACKAGE OUTLINE - 128 PIN PQFP (PLASTIC QUAD FLAT PACK)



SYMBOL	in.	mm.
A	1.239 ± 0.027	31.47 ± 0.69
B	1.102 ± 0.004	28.00 ± 0.10
C	0.031 ± 0.004	0.80 ± 0.10
D	0.013 ± 0.005	0.33 ± 0.13
E	0.006 ± 0.002	0.15 ± 0.05

SYMBOL	in.	mm.
F	0.009 ± 0.005	0.23 ± 0.13
G	0.027 ± 0.010	0.69 ± 0.25
H	0.134 ± 0.006	3.40 ± 0.15
I	0.976 ± 0.004	24.80 ± 0.10
J	0° - 12°	

BLOCK DIAGRAM



PIN DESCRIPTIONS

SYSTEM BUS INTERFACE								
PIN NAME	**PIN NO.**	**PIN TYPE (TTL)** √ = Pin has internal pullup (250 KΩ ± 50%)		**OUTPUT CURRENT (mA MIN)**		**LOAD (pf MAX)**	**SIGNAL INTERFACE**	
				IOH (VOH= 2.4V)	**IOL** (VOL= 0.4V)		**AT BUS**	**MICRO CHANNEL**
RESET	37	IN	√				RESET DRV	CHRESET
LA(23:20)	125-122	IN	√				LA(23:20)	A(23:20)
LA(19:18)	121,120	IN	√				LA(19:18)	*not used*
LA(17)	119	IN	√				LA(17)	MADE24
SA(19:0)	25-21, 18,17, 15-3	IN					SA(19:0)	A(19:0)
SD(15:8)	110-115, 117,118	IN/OUT	√	-3 (-15 mA @ 2.0V)	12 (24 mA @ 0.5V)	240	SD(15:8)	D(15:8)
SD(7:0)	46-43, 41-38	IN/OUT		-3 (-15 mA @ 2.0V)	12 (24 mA @ 0.5V)	240	SD(7:0)	D(7:0)
SBHEN	126	IN	√				SBHE	-SBHE
RFRSHN	28	IN					-REFRESH	-REFRESH
AEN	26	IN					AEN	-CD SETUP(n)
MWRN	34	IN					-SMEMW	-S0
MRDN	31	IN					-SMEMR	M/-IO
IOWN	30	IN					-SIOW	-CMD
IORN	29	IN					-SIOR	-S1
IOCHRDY	27	OUT		-3	12 (24 mA @ 0.5V)	200	IOCHRDY	CD CHRDY(n)
IOCS16N	19	OUT		-3	20 (24 mA @ 0.5V)	200	-IO CS16	-CD SFDBK(n)
MCS16N	20	OUT		-3	20 (24 mA @ 0.5V)	200	-MEM CS16	-CD DS 16(n)
IRQ	36	OUT		-3	12 (24 mA @ 0.5V)	200	IRQ	-IRQ
ZERON	35	OUT Open Collector			20 (24 mA @ 0.5V)	200	0WS	*not used*
NC	2	*RESERVED*					*This pin should remain unconnected.*	

SYSTEM BUS INTERFACE PIN DESCRIPTIONS

AEN (26)

PC/AT BUS: Address Enable. When this input signal is high during a bus cycle, the System's DMA Controller has control of the System's Address, Data, and Control lines. If this pin is high during an I/O or Memory transfer cycle to a valid AVGA1 address, the AVGA1 responds to Memory cycles only; if low, the AVGA1 responds to both I/O and Memory cycles.

Micro Channel: -Card Setup. When this signal is driven low, the AVGA1 is placed in Setup Mode and maps in the POS (Programmable Option Select) Register 2 at I/O address 102H.
The AVGA1 then responds only to I/O read/write accesses to port 102; it does not respond to Video Memory access.

This signal may be supplied to the AVGA1 either latched or unlatched, because the signal is latched internally while input -CMD (pin IOWN) is low. For a motherboard-based VGA design, this signal would ordinarily be supplied from bit 5 of the System Board Enable/Setup Register at I/O address 094H.

IOCHRDY (27)

PC/AT BUS: I/O Channel Ready. This output, by going low, requests that Video Memory access cycles be lengthened until it is driven high. This tri-state output floats whenever the AVGA1 is not participating in a Video Memory access cycle. This pin remains tri-stated off during Video BIOS ROM accesses and all I/O cycles.

In Memory read cycles, the leading edge of the active low input MRDN always causes this output to go low. This output is clocked high when the AVGA1 has completed the memory data transfer. The output remains high until MRDN going inactive causes it to float.

In Memory write cycles, the AVGA1 can drive this pin high immediately, by the leading edge of active low input MWRN. The reason is that the AVGA1's MEMORY WRITE DATA FIFO stores the data being written, releases the Processor by driving this pin high, then performs the write cycle later. If the FIFO is not ready for more data at the start of a Memory write cycle, then this pin is driven low by the leading edge of MWRN.

Micro Channel: Channel Ready. This output, by going low, requests that Video Memory access cycles be lengthened until it is driven high. This pin is not tri-state, and remains high when the AVGA1 is not responding to a memory cycle. This pin remains high during Video BIOS ROM accesses and all I/O cycles.

In Memory read cycles, a valid Address decode and valid Status always causes this output to go low. This output is clocked high when the AVGA1 has completed the memory access. The Address decode is generated from Micro Channel signals A(23:0), MADE24, -REFRESH, and M/-IO; the Status is a decode of -S0 and -S1.

In Memory write cycles, this pin can be driven high immediately by a valid Address decode and Status (see the PC/AT description of this pin).

SYSTEM BUS INTERFACE PIN DESCRIPTIONS (cont.)

IOCS16N (19)

AT BUS: -I/O 16 bit Chip Select. This open-collector output pin signals the System Processor that the present cycle is a 16-bit I/O cycle. The signal is generated from an address decode of inputs SA(15:0) and AEN, for the following I/O ports:

3C4,3C5	(SEQUENCER)
3CE,3CF	(GRAPHICS CONTROLLER)
3B4/3D4,3B5/3D5	(CRT CONTROLLER)
3BA/3DA	(INPUT STATUS REGISTER 1)

Micro Channel: -Card Selected Feedback. This pin is driven low by a valid Address decode whenever the System Processor addresses I/O ports or Memory segments where the AVGA1 is mapped in. The Address decode is generated from Micro Channel signals A(23:0), MADE24, -REFRESH, and M/-IO. The memory segment addressing range includes the Video BIOS ROM only if it is 16 bits, indicated by setting Configuration Register bit CF(6)=0; if CF(6)=1, then this pin remains high while accessing the BIOS ROM. Accessing I/O ports 102H or 3C3H does not cause this pin to go low, although the AVGA1 contains these registers.

This pin remains high while the AVGA1 is in Setup Mode (see pin AEN), regardless of the address.

IORN (29)

PC/AT BUS: -I/O Read. This active low input causes the AVGA1 to drive I/O port data onto the System Data Bus during an I/O read bus cycle.

Micro Channel: -Status Bit 1. This input, and two other inputs -Status Bit 0 (MWRN) and M/-IO (MRDN), are fully decoded and latched by -CMD (pin IOWN) low. The resulting latched decode determines the type of channel cycle, as given in the following table:

M/-IO	-S0	-S1	Cycle Type
0	0	1	I/O write
0	1	0	I/O read
1	0	1	Memory write
1	1	0	Memory read
X	0	0	none
X	1	1	none

IOWN (30)

PC/AT BUS: -I/O Write. This active low input causes the AVGA1 to transfer data from the System Data Bus into a register during an I/O write bus cycle. Data is written to a register by the trailing edge of this signal.

Micro Channel: -Command. This active low input signal is used to latch the System Address and Status into transparent latches. The latched Address and Status decode is gated with this signal to provide timing control during read/write bus cycles. During read cycles, the AVGA1 drives valid data onto the System Data Bus before the trailing edge of this signal. During write cycles, data written to Video Memory is expected to be valid throughout the interval when this input is low; data is written to I/O ports by the trailing edge of this signal.

SYSTEM BUS INTERFACE PIN DESCRIPTIONS (cont.)

IRQ (36)

PC/AT BUS: Interrupt Request. A low to high transition on this output indicates that the AVGA1's CRT Display timing has reached the end of the active display frame, at the start of the bottom screen border. This signal is ordinarily unused in PC/AT-based VGA add-in boards. Connecting this pin to one of the System's IRQ lines through a jumper block is recommended, to allow its possible use.

This pin is a tri-state buffer, enabled by CRTC Register 11H bit 5=0.

Micro Channel: -Interrupt Request. A high impedance to low transition on this open collector output indicates that the AVGA1's CRT Display timing has reached the end of the active display frame, at the start of the bottom screen border. This pin is not driven high. Transitions on this output are enabled only if CRTC Register 11H bit 5=0 and POS Register 2 (102H) bit 0=1.

LA(17) (119)

AT BUS: Latchable Address 17. The combined decode of this input signal with inputs LA(23:18) is used to generate a request for a 16-bit Video Memory cycle. Requests for 16-bit Memory access to the Video BIOS ROM are generated from the combined decode of LA(23:18), this pin, and SA(16:15).

Micro Channel: Memory Address Enable 24. This input signal is latched by a low -CMD (IOWN) signal and must be high during a Memory cycle in order for the AVGA1 to participate in the cycle.

LA(19:18) (121,120)

AT BUS: Latchable Addresses 19 & 18. The combined decode of these input signals with inputs LA(23:20) and LA(17) is used to generate a request for a 16-bit Video Memory cycle. Requests for 16-bit Memory access to the Video BIOS ROM are generated from the combined decode of LA(23:20), these pins, LA(17), and SA(16:15).

Micro Channel: Not used. These inputs have internal pullup resistors and may be left to float.

LA(23:20) (125-122)

AT BUS: Latchable Addresses 23-20. The combined decode of these input signals with inputs LA(19:17) is used to generate a request for a 16-bit Video Memory cycle. Requests for 16-bit Memory access to the Video BIOS ROM are generated from the combined decode of these pins, LA(19:17), and SA(16:15).

Micro Channel: Address Bits 23-20. These address inputs are latched by a low -CMD (IOWN) signal and must all be zero during a Memory cycle in order for the AVGA1 to participate in the cycle.

SYSTEM BUS INTERFACE PIN DESCRIPTIONS (cont.)

MCS16N (20)

AT BUS: -MEM 16 Chip Select. This open-collector output requests the System Processor to make the present cycle a 16-bit Memory cycle. This signal is generated either from an address decode of inputs LA(23:17) during Video Memory access, or from an address decode of LA(23:17) and SA(16:15) during BIOS ROM access. In both cases, other conditions qualify the 16-bit requests. Video memory 16-bit cycles are enabled by the AVGA1 if no other Video Controller is detected in the System, in order to prevent requesting 16-bit cycles while the other Video Controller's memory is accessed. BIOS ROM 16-bit Memory cycles are enabled only if Configuration Register bit CF(6)=0 (BIOS ROM is 16 bits).

Although delays introduced into the latched System Addresses SA(16:15) by the System commonly make these signals unreliable for generating 16-bit memory requests, the AVGA1 incorporates an especially high speed signal path design from these inputs to the MCS16N output buffer, to achieve reliability.

Micro Channel: -Card Data Size 16. This totem pole output requests the System Processor to make the present Memory or I/O cycle a 16-bit cycle.

This signal is generated from the combined decode of unlatched Micro Channel signals MADE24, -REFRESH, M/-IO, and inputs A(23:0) which define the addressing range: A(23:15) for Video Memory, and A(23:11) for the BIOS ROM. This output is also driven low while accessing the same 16-bit I/O ports listed previously in the description of pin IOCS16N's function in the AT BUS. The signal is generated from the combined decode of unlatched M/-IO and A(15:1).

MRDN (31)

PC/AT BUS: -Memory Read. This active low input causes the AVGA1 to drive Video Memory data onto the System Data Bus during a Video Memory read cycle. The signal should be connected to the AT BUS signal -SMEMR, active during memory read cycles within the lower 1 Mb of System Address space.

This input signal also strobes the output EROMN, which controls external bus buffer(s) driving BIOS ROM data onto the System Data Bus.

Micro Channel: Memory/-Input Output. This input, and two other inputs -Status Bit 0 (MWRN) and -Status Bit 1 (IORN), are fully decoded and latched by the leading edge of -CMD (IOWN). The resulting latched decode determines the type of channel cycle, as shown in the table under the description of pin IORN.

MWRN (34)

PC/AT BUS: -Memory Write. This active low input causes the AVGA1 to write data from the System Data Bus into Video Memory. The signal should be connected to the AT BUS signal -SMEMW, active during memory write cycles within the lower 1 Mb of System Address space.

Micro Channel: -Status Bit 0. This input, and two other inputs -Status Bit 1 (IORN) and M/-IO (MRDN), are fully decoded and latched by the leading edge of -CMD (IOWN). The resulting latched decode determines the type of channel cycle, as shown in the table under the description of pin IORN.

SYSTEM BUS INTERFACE PIN DESCRIPTIONS (cont.)

RESET (37)

This active high input initializes the AVGA1. The high to low transition of this input loads the Configuration Register CF(7:0) with data present on the MD(7:0) pins, determined by internal pullup resistors and external, optional pulldowns.

The RESET pin is equipped with an internal pullup resistor, so that the AVGA1 may be completely disabled by disconnecting this pin from the reset signal supplied to it, for example, through a removable jumper block. This is useful if the AVGA1 has been installed in a motherboard, but it is later desirable to install an upgrade which would occupy the same Memory and I/O Address space.

RFRSHN (28)

PC/AT BUS: -Refresh. This input signal must be high during a Video Memory read cycle in order for the AVGA1 to participate in the cycle.

Micro Channel: -Refresh. This input signal is latched by a low -CMD (IOWN) signal and must be high during a Video Memory cycle in order for the AVGA1 to participate in the cycle.

SA(19:0) (25-21,18,17,15-3)

System Address Bits SA(19:0). These address inputs are decoded to select Memory and I/O during read/write access cycles. Video Memory is selected by decoding SA(19:15), and the BIOS ROM by decoding SA(19:11). All I/O ports are selected by decoding SA(15:0) except POS Register 2, which is selected by decoding SA(2:0).

In Micro Channel operation, these address inputs are transferred into transparent latches by a low IOWN (-CMD) signal and therefore may change state while IOWN is low. In PC/AT BUS operation, however, these address inputs are not latched and must remain valid during the data access cycle.

Inputs SA(12:2) and input TWRN also provide access to eight, 8-bit Test Registers used for chip manufacturing test (see the description of pin TWRN).

SBHEN (126)

-System Byte High Enable. This active low input enables data to be transferred across System Data Bus pins SD(15:8). This input and pin SA(0) are decoded to distinguish between low byte and high byte data transfers. This input should be connected to the AT BUS or Micro Channel signal -SBHE. The signal is internally latched in Micro Channel operation, by input IOWN (-CMD) low.

This pin has an internal pullup resistor which ensures that this input is forced inactive if an AVGA1 is installed in an 8-bit card slot. The AVGA1 traps any high to low level transition of this input after RESET has been asserted, to determine whether it is installed in a 16-bit card slot and properly control output ZERON.

SYSTEM BUS INTERFACE PIN DESCRIPTIONS (cont.)

SD(15:8) (110-115,117,118)

System Data Bus bits 15-8. These bidirect pins transfer I/O and Video Memory data during 16-bit bus cycles. During 16-bit read cycles, input signal SBHEN=0 (internally latched in Micro Channel operation) enables these output buffers. These pins have internal pullup resistors, in order to reduce internal power whenever these inputs are allowed to float, as in an 8-bit System.

SD(7:0) (46-43,41-38)

System Data Bus bits 7-0. These bidirect pins transfer data during all I/O and Video Memory accesses. During read operations, all output buffers are enabled except in the special case of reading (Micro Channel operation only) the VGA Enable Register at I/O address 3C3H. Only bit 0 of this register is driven onto SD(0) by the AVGA1.

ZERON (35)

AT BUS: Zero Wait State. This open collector output pin is driven low to signal the System Processor that it can complete the present bus cycle without inserting any additional wait states. This output is recommended for use in 80286-based systems.

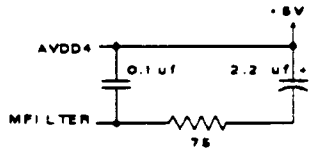
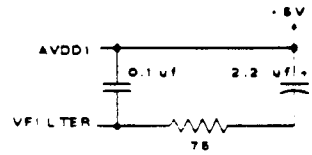
The AVGA1 drives this pin low in order to shorten Video Memory read/write cycles or BIOS ROM read cycles; this output remains inactive during I/O access cycles. ZERON is driven active during all Video Memory access cycles, but it can go active during BIOS ROM read cycles only if Configuration Register bit CF(1) has been cleared to 0.

In Video Memory read/write cycles, ZERON is driven low by output IOCHRDY being driven high, signalling the Processor that data transfer is complete and that no additional wait states are required. During some write cycles, in which the AVGA1 stores data temporarily in the MEMORY WRITE DATA FIFO, ZERON is driven low almost immediately by input MWRN going low, because IOCHRDY remains high. ZERON goes low while accessing any odd-addressed byte of Video Memory, and also while reading any even-addressed byte only if no second installed card has been detected and the AVGA1 is installed in a 16-bit card slot (refer to the description of input SBHEN).

During a BIOS ROM read cycle, ZERON is driven low by input MRDN being driven low. It remains low until MRDN is driven high. ZERON goes low while reading any odd-addressed byte of the BIOS ROM, and also while reading any even-addressed byte only if Configuration Register bit CF(6)=0 and the AVGA1 is installed in a 16-bit card slot (refer to the description of input SBHEN). Use of ZERON typically results in reduction of BIOS ROM read cycles from 3 to 2 processor clock cycles (one Send-Status [T_s] and one Command [T_c] cycle).

Micro Channel: This output is disabled and remains high impedance.

CLOCK SYNTHESIZER				
PIN NAME	**PIN NO.**	**PIN TYPE**	**SPECIFICATIONS**	**DESCRIPTION**
OSC	107	TTL IN	Frequency: 14.31818 MHz ± 0.01% Duty cycle: 50 ± 10 %	Reference clock input of the CLOCK SYNTHESIZER. This input is driven normally by the clock signal OSC, supplied by both the AT BUS and the MICRO CHANNEL System Bus Interfaces. Alternatively, this input can be driven by a 14.31818 MHz CRYSTAL, connected across this pin and the XTAL pin. The CLOCK SYNTHESIZER multiplies the frequency of this input signal in order to generate Memory Timing Clock (MCLK) frequencies, and the internal Video Dot Clock (VCLK), (see "Video Dot Clock Selection" on page 60): Clock Multiplier Freq. (MHz) MCLK 84/32 37.585 MCLK 100/32 44.744 VCLK 56/32 25.057 VCLK 63/32 28.189 VCLK 92/32 41.164 VCLK 80/32 35.795 The CLOCK SYNTHESIZER can be configured so that either MCLK or VCLK, or both, may be supplied by external oscillators. If Configuration Register bit CF(4)=0, then MCLK is external; if CF(5)=0, then VCLK is supplied by up to four external oscillators. The frequency of the 37.5 MHz MCLK has been optimized for use with 80 ns. DRAMs; the 44.7 MHz MCLK can be used with 70 ns. DRAMs, for higher system performance.
XTAL *(Use is optional)*	108	ANALOG OUT	Frequency: 14.31818 MHz ± 0.01% Duty cycle: 50 ± 10 %	Crystal The input clock of the CLOCK SYNTHESIZER can be supplied by a 14.31818 MHz CRYSTAL, connected across this pin and the OSC pin.

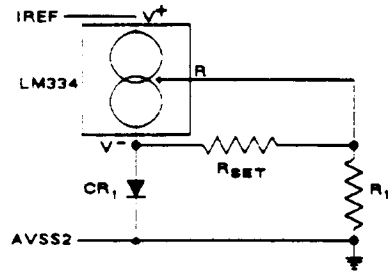
CLOCK SYNTHESIZER (continued)				
PIN NAME	**PIN NO.**	**PIN TYPE**	**SPECIFICATIONS**	**DESCRIPTION**
MFILTER	104	ANALOG IN/OUT		MCLK VCO phase comparator filter. The VCO which generates the Memory Timing Clock (MCLK) requires a filter network to be connected between this pin and the AVDD4 pin, as shown on the left.
VFILTER	52	ANALOG IN/OUT		VCLK VCO phase comparator filter. The VCO which generates the Video Clock (VCLK) requires a filter network to be connected between this pin and the AVDD1 pin, as shown on the left.
MCLK	106	TTL IN/OUT	Config. Frequency CF(0)=1 37.585 MHz ± 0.01% CF(0)=0 44.744 MHz ± 0.01% Duty cycle: 50 ± 10 % I_{OH} = -12 mA min (V_{OH}=2.4V) I_{OL} = 12 mA min (V_{OL}=0.4V) Load = 10 pf max	Memory Timing Clock. Normally, the CLOCK SYNTHESIZER generates the internal Memory Timing Clock, and this pin functions as a test output for monitoring the internal MCLK. The frequency of MCLK is determined by Configuration Register bit CF(0), as shown on the left. The CLOCK SYNTHESIZER's MCLK VCO can be disabled, however, by setting Configuration Register bit CF(4)=0, so that MCLK may be supplied by an external, TTL-level clock source.

VIDEO INTERFACE							
PIN NAME	PIN NO.	PIN TYPE √ = Pin has internal pullup (250 KΩ ± 50%)		OUTPUT CURRENT (mA MIN) I_{OH} @ 2.4V (V_{OH} MIN)	 I_{OL} @ 0.4V (V_{OL} MAX)	LOAD (pf MAX)	DESCRIPTION
VSYNC	56	TTL OUT TRISTATE		-12	12 (20 mA @V_{OL} = 0.5V)	50	Vertical Sync This signal is the vertical sync pulse driving the CRT display and also supplied externally to the FEATURE CONNECTOR. The input pin ESYNC controls this output. If ESYNC is driven low, then this output floats.
HSYNC	57	TTL OUT TRISTATE		-12	12 (20 mA @V_{OL} = 0.5V)	50	Horizontal Sync This signal is the horizontal sync pulse driving the CRT display and also supplied externally to the FEATURE CONNECTOR. The input pin ESYNC controls this output. If ESYNC is driven low, then this output floats.
BLNKN	75	TTL IN/OUT		-12	12	50	Blanking The signal on this bidirect pin is fed back into the BLANK input of the Video DAC. When low, this signal causes the output pins RED, GREEN, and BLUE to be 0 V. This pin is connected externally to the FEATURE CONNECTOR. The input pin ESYNC controls the output buffer of this bidirect pin. If ESYNC is driven low, then this pin becomes an input, and the Video DAC's BLANK input can be driven externally by the FEATURE CONNECTOR. If ESYNC is high, then this pin is driven internally.

VIDEO INTERFACE (continued)							
PIN NAME	PIN NO.	PIN TYPE	√ = Pin has internal pullup (250 KΩ ± 50%)	OUTPUT CURRENT (mA MIN) IOH @ 2.4V (VOH MIN)	OUTPUT CURRENT (mA MIN) IOL @ 0.4V (VOL MAX)	LOAD (pf MAX)	DESCRIPTION
ESYNC	77	TTL IN	√				Enable Sync This pin controls the output buffers of pins VSYNC, HSYNC, and BLNKN; driving this pin low disables (floats) the outputs.
P(7:0)	73, 70-68, 66-63	TTL IN/OUT		-12	12	50	Pixel Data The signals on these bidirect pins are fed back into the PIXEL ADDRESS inputs of the Video DAC. These pins are connected externally to the FEATURE CONNECTOR. The input pin EVIDEO controls the output buffers of these bidirect pins. If EVIDEO is driven low, then these pins become inputs, and the Video DAC's PIXEL ADDRESS inputs can be driven externally by the FEATURE CONNECTOR. If EVIDEO is high, then these pins are driven internally by the AVGA1.
DCLK	74	TTL IN/OUT		-12	12	50	DAC Clock The signal on this bidirect pin is fed back into the PIXEL CLOCK input of the Video DAC, and it can also be selected as the source for the internal Video Dot Clock. This pin is connected externally to the FEATURE CONNECTOR. The rising edge of this signal latches the values of P(7:0) and the BLNKN signal into the Video DAC. It is typically the same frequency as the internal Video Dot Clock. The input pin EDCLK controls the output buffer of this bidirect pin. If EDCLK is driven low, then this pin becomes an input, and the Video DAC's PIXEL CLOCK input can be driven externally by the FEATURE CONNECTOR. If EDCLK is high, then this pin is driven internally by the AVGA1.

VIDEO INTERFACE (continued)							
PIN NAME	PIN NO.	PIN TYPE	√ = Pin has internal pullup (250 KΩ ± 50%)	OUTPUT CURRENT (mA MIN) IOH @ 2.4V (VOH MIN)	OUTPUT CURRENT (mA MIN) IOL @ 0.4V (VOL MAX)	LOAD (pf MAX)	DESCRIPTION
EVIDEO	76	TTL IN	√				Enable Video This pin controls the output buffers of pins P(7:0); EVIDEO=0 floats the outputs.
EDCLK	78	TTL IN	√				Enable DAC Clock This pin controls the output buffer of pin DCLK; EDCLK=0 floats the output. This pin also controls selection of the Video Dot Clock, as described in "Video Dot Clock Selection" on page 60.
VCLK0, VCLK1, VCLK2 *(Use is optional)*	128, 49,50	TTL IN	√				Optional Video Clocks 0,1,2 These inputs can be selected as the source of the Video Dot Clock, if Configuration Register bit CF(5)=0 [External Video Clocks]. Inputs VCLK1 and VCLK2 can be selected if Configuration bit CF(5)=1 [Internal Video Clocks] and if VCLK0=0. For details of clock selection, refer to "Video Dot Clock Selection" on page 60.

VIDEO INTERFACE (continued)					
PIN NAME	**PIN NO.**	**PIN TYPE**	**SPECIFICATIONS**	**LOAD** (pf MAX)	**DESCRIPTION**
RED, GREEN, BLUE	61-59	ANALOG IN/OUT	Full-scale output: 0.70V ± 7% (Termination: 50Ω to VSS)		Red, Green, & Blue Video Outputs These pins are the outputs of three 6-bit DACs. Each DAC consists of 63 summed current sources. A 6-bit register value applied to the DAC input determines the number of current sources to be summed. The full-scale output current (IF) sourced by each pin is related to the DAC Reference Current (IREF pin) as follows: $I_F = (63/30) \times I_{REF}$ To maintain IBM® VGA compatibility, each pin should be terminated to ground through a precision resistor, 150Ω ± 2%. Additional termination to ground through a 75Ω ± 2% resistor should produce a loaded output level of 0.7 V ±7%. Therefore, the full-scale output current is nominally 14 mA.

VIDEO INTERFACE (continued)					
PIN NAME	**PIN NO.**	**PIN TYPE**	**SPECIFICATIONS**	**LOAD** (pf MAX)	**DESCRIPTION**
IREF	62	ANALOG IN	-3.0 mA ≤ IREF ≤ -10.0 mA (@ VDD = 5.25 V)		DAC Reference Current The current drawn from VDD through this pin determines the full-scale output current of each DAC. (See pins RED, GREEN, & BLUE). This pin should be connected to a constant current source. An example of a current source based on the LM334, used in zero temperature coefficient mode, is given below. The nominal IREF is 6.67 mA, which produces a full-scale output current on RED, GREEN, & BLUE of 14 mA.  R_{SET} = 20Ω ± 1% R_1 = 200Ω ± 5% CR_1 = 1N4148 or equivalent Notes: R_{SET} determines IREF; R_1 and CR_1 provide temperature compensation. The voltage (V_{SET}) across R_{SET} varies according to temperature (T): V_{SET} (mV) = 59 + 0.2T, 0° ≤ T ≤ 70° C The current I_{SET} through resistor R_{SET} determines the output current: IREF ≈ $2I_{SET}$

DYNAMIC RAM INTERFACE							
PIN NAME	**PIN NO.**	**PIN TYPE (TTL)** √ = Pin has internal pullup (250 KΩ ± 50%)		**OUTPUT CURRENT (mA MIN)** I_{OH} (V_{OH} = 2.4 V)	**OUTPUT CURRENT (mA MIN)** I_{OL} (V_{OL} = 0.4 V)	**LOAD (pf MAX)**	**DESCRIPTION** All outputs are generated synchronously from MCLK (Memory Timing Clock) timing. The output buffers can be turned off (high impedance), to facilitate board-level testing of the DRAMs (see the pin description of input TWRN).
RASN	92	OUT		-12	12	35	Row Address Strobe The falling edge of this active low output coincides with output of a valid DRAM Row Address on pins MA(8:0).
CASN	90	OUT		-12	12	35	Column Address Strobe The falling edge of this active low output coincides with output of a valid DRAM Column Address on pins MA(8:0). The rising edge latches data from the DRAM, on pins MD(7:0), into the AVGA1. CAS-before-RAS refresh is not supported.
OEN	93	OUT		-12	12	35	Output Enable Data from the DRAM is input to the AVGA1 through pins MD(7:0) while this signal and CASN are low.

DYNAMIC RAM INTERFACE (continued)							
PIN NAME	PIN NO.	PIN TYPE (TTL) √ = Pin has internal pullup (250 KΩ ± 50%)		OUTPUT CURRENT (mA MIN)		LOAD (pf MAX)	DESCRIPTION
				I_{OH} (V_{OH} = 2.4 V)	I_{OL} (V_{OL} = 0.4 V)		
WEN	89	OUT		-12	12	35	Write Enable Data is written to the DRAM through pins MD(7:0) by the falling edge of either this signal or CASN (Late/Early Writes).
MA(8:0)	88-80	OUT		-12	12	35	Memory Address (8:0) These pins output addresses originating from the CRT Controller or System Address Bus. A burst of either three or five RAS-only DRAM refresh cycles, having consecutive refresh addresses, are output at the end of each horizontal scan interval.
MD(7:0)	94-96, 98-102	IN/OUT	√	-12	12	35	Memory Data (7:0) The System Processor reads and writes Video display data through these bidirect pins; the CRT Controller sequentially reads data through them. The outputs float when input RESET is high. Also, these pins are inputs to the AVGA1 Configuration Register, which is loaded by the falling edge of RESET. Internal pullups provide a default value of FFH to be loaded. Configuration Register bits CF(7:0) are loaded from the correspondingly indexed pins MD(7:0).

BIOS ROM SUPPORT						
PIN NAME	PIN NO.	PIN TYPE (TTL)	OUTPUT CURRENT (mA MIN)		LOAD (pf MAX)	DESCRIPTION
			I_{OH} (V_{OH} = 2.4V)	I_{OL} (V_{OL} = 0.4V)		
EROMN	127	OUT	-12	12	35	Enable ROM

This totem pole output controls the active low output enable inputs of up to two external 8-bit bus buffers, which drive BIOS ROM data onto the System Data Bus. This output is driven high by bringing the input RESET high.

This output can go active only if the System Processor is performing a Memory read cycle within the 32Kb segment from System Address C0000 through C7FFF. To maintain IBM® VGA compatibility, the 2Kb range from C6000 through C67FF is excluded from the address decode only if Configuration Register bit CF(2)=1, and the output remains inactive; otherwise, if bit CF(2)=0, then this output goes active while also addressing the 2Kb range. In PC/XT/AT operation, the address is decoded from SA(19:11); in Micro Channel operation, LA(23:20), SA(19:11), and LA(17) (MADE24) are decoded.

The output is strobed to go low by an active Memory read command asserted at an input pin. In PC/XT/AT operation, the strobing input signal is MRDN low; in Micro Channel operation, IOWN (-CMD) low.

TEST				
PIN NAME	**PIN NO.**	**PIN TYPE (TTL)**	√ = Pin has internal pullup (250 KΩ ± 50%)	**DESCRIPTION**
TWRN	48	IN	√	Test Latch Load Enable *This pin is used primarily for chip testing and must be driven high or allowed to float for normal operation of the chip.* It can be used, however, in board-level testing, to disable (float) most of the AVGA1 outputs and drive them by a board tester. This pin provides an active-low, load enable pulse to eight, 8-bit transparent latches which supply internal chip test mode functions. These latches are designated TEST REGISTERS TR0(7:0) through TR7(7:0). The address *j* of each latch TR*j*(7:0) is decoded from input pins SA(12:10), and the test data byte (7:0) written to the latch is obtained from input pins SA(9:2). All latch data bits are active high. All latches are cleared to 0 asynchronously by driving the RESET pin high, or allowing it to float. Loading a test register consists of placing its address and test data onto pins SA(12:2), then bringing TWRN low. The test data is transferred to the latch outputs while TWRN remains low and remains latched after TWRN is returned high. While TWRN is low, the latch remains transparent; its outputs will follow any transitions on SA(9:2). In order to disable the output buffers, set Test Register bit TR0(5)=1 by setting pins SA(12:2) = 020H and TWRN=0. To re-enable the output buffers, clear TR0(5) to 0, either by writing 0 to the register or by driving RESET high. Setting TR0(5)=1 causes only the following outputs to be disabled (floating): CASN MD(7:0) IOCHRDY OEN IOCS16N RASN IRQ SD(15:0) MA(8:0) WEN MCS16N ZERON

POWER			
PIN NAME	**PIN NO.**	**SUPPLY**	**CIRCUIT SECTION**
VDD1-VDD4	1,32,47,97	+5V	LOGIC
VSS1-VSS9	16,33,42,58,67,79,91,109,116	GND	LOGIC
AVDD2,AVDD3	55,71	+5V	VIDEO DAC
AVSS2, AVSS3	54,72	GND	VIDEO DAC
AVDD1	53	+5V	VCLK VCO
AVSS1	51	GND	VCLK VCO
AVDD4	103	+5V	MCLK VCO
AVSS4	105	GND	MCLK VCO

AVGA1 REGISTERS

All of the registers summarized in the following table are contained in the AVGA1.

NAME	I/O ADDRESS	R/W Read, Write, Only	NOTES
AVGA1 Configuration Register	---	WO	Bits CF(7:0) written by RESET low, from MD(7:0)
AVGA1 Test Registers	---	WO	Registers TR0(7:0)-TR7(7:0) written by TWRN low
Input Status Register 0	3C2	RO	
Miscellaneous Output Register	3C2	W	
	3CC	R	
Input Status Register 1	3BA/3DA	RO	
Feature Control Register	3BA/3DA	W	
	3CA	R	
VGA Enable Register	3C3	RW	Micro Channel only [CF(7)=0]
	46E8	WO	PC/XT/AT Bus only [CF(7)=1 and CF(3)=1]
	46E9	WO	PC/XT/AT Bus only [CF(7)=1 and CF(3)=0]
POS Register 2	102	RW	
Sequencer	3C4	RW	Index
	3C5	RW	Data registers 00 - 04
Graphics Controller	3CE	RW	Index
	3CF	RW	Data registers 00 - 08
CRT Controller	3B4/3D4	RW	Index
	3B5/3D5	RW	Data registers 00 - 18H
Attribute Controller	3C0	RW	Index
	3C0	W	Data registers 00 - 14H
	3C1	RO	
Video DAC	3C6	RW	Pixel Mask Register
	3C7	WO	Pixel Address Register (read mode)
		RO	DAC State Register
	3C8	RW	Pixel Address Register (write mode)
	3C9	RW	Pixel Data Registers 00 - FF

AVGA1 CONFIGURATION REGISTER CF(7:0)

This 8-bit register configures the AVGA1 into various modes of operation. Software cannot access this register. Data present on the Memory Data Bus MD(7:0) is loaded into this register by power-on reset. Data on the MD bus is supplied at reset by both internal pullup resistors (nominally 250K) and optional, external pulldown resistors (nominally 6.8K); therefore, if no pulldown resistors are installed, power-on reset loads this register with data FF.

CF(7) AT/Microchannel
- 0: Microchannel System Bus Interface
- 1: PC/XT/AT System Bus Interface

CF(6) 8-bit/16-bit Video BIOS ROM
- 0: 16-bit BIOS ROM
- 1: 8-bit BIOS ROM

CF(5) Internal/External Video Clocks
- 0: External video clocks; Clock Synthesizer VCLK VCO disabled.
- 1: Internal video clocks; Clock Synthesizer VCLK VCO enabled.

CF(4) Internal/External Memory Clock
- 0: External clock; the MCLK pin is configured as an input; Clock Synthesizer MCLK VCO disabled.
- 1: Internal clock; the MCLK pin is an output; Clock Synthesizer MCLK VCO enabled.

CF(3) Select VGA Enable Register Address

This bit changes the I/O port address of the VGA Enable Register, normally mapped into port 46E8, only if the AVGA1 is configured for AT BUS operation by setting CF(7)=1. Intended for use in hardware implementations having the AVGA1 installed in a System's motherboard, this bit allows disabling the AVGA1 through port 46E9 instead. Therefore, any other VGA Video Adapter, enabled by port 46E8, can be installed in a card slot of the same System without conflict with the AVGA1.

If bit CF(7)=0 (Microchannel), then this bit has no effect.
- 0: VGA Enable Register is mapped into 46E9.
- 1: VGA Enable Register is mapped into 46E8.

CF(2) Map Out 2K BIOS ROM Addresses
- 0: Include all 32K addresses, C0000 through C7FFF, in the memory address decode for output pin EROMN to go active when reading the BIOS ROM.
- 1: Ignore 2K addresses, C6000 through C67FF, from the memory address decode; output pin EROMN remains high for these addresses.

CF(1) Enable BIOS ROM Zero Wait
- 0: Enable output ZERON to be driven active when accessing the BIOS ROM, through output EROMN active.
- 1: Output ZERON remains high impedance when accessing the BIOS ROM.

CF(0) Low/High Memory Timing Clock (MCLK) Select
- 0: Clock Synthesizer MCLK frequency = 44.744 MHz; 70 ns. DRAMs
- 1: Clock Synthesizer MCLK frequency = 37.585 MHz; 80 ns. DRAMs

GENERAL REGISTERS

This section describes the following registers:

Register	Port address	
Miscellaneous Output Register	Write:	3C2H
	Read:	3CCH
Feature Control Register	Write:	3xAH
	Read:	3CAH
Input Status Register 0	Read:	3C2H
Input Status Register 1	Read:	3xAH

x denotes a digit that depends upon the current emulation mode. Use:
B for monochrome emulation modes
D for color emulation modes.
Note: The Input Status registers are read-only.

Miscellaneous Output Register

An 8-bit read/write register: port address for read is hex 3CC; for write, hex 3C2. A hardware reset resets all bits to zero.

Miscellaneous Output Register	
7	Vertical sync polarity (see Note)
6	Horizontal sync polarity (see Note)
5	0dd/even page
4	(reserved)
3	Clock select, bit 1
2	Clock select, bit 0
1	Enable RAM
0	I/O address select

Bit 7 Vertical sync polarity—
0 selects "vertical retrace".
1 selects "-vertical retrace".
(See Note above.)

Bit 6 Horizontal sync polarity—
0 selects "horizontal retrace".
1 selects "-horizontal retrace".

Note: Bits 7 and 6. sync polarity, are used to define the vertical size (in lines) of the monitor:

Bits 7,6	Vertical Size
0 0	(reserved)
0 1	400 lines
1 0	350 lines
1 1	480 lines(See Note above.)

Bit 5 **Odd/even page** Selects between two 64K pages of memory when in the odd/even modes.

0 selects the low page of memory.
1 selects the high page of memory.

Bits 3 and 2 Clock select

Bits 3,2	
0 0	25.1744 MHz clock
0 1	28.3212 MHz clock
1 0	41.164 MHz clock
1 1	35.795 MHz clock

Bit 1 **Enable RAM**—
0 disables processor access to video RAM.
1 enables processor access to video RAM.

Bit 0 **I/O address select**—Maps the video I/O addresses for emulation of either the Monochrome Display and Parallel Printer Adapter or the Color Graphics Adapter:

0 sets addresses for monochrome emulation.
1 sets addresses for color graphics emulation.

Feature Control Register
An 8-bit read/write register: port address for read is hex 3CA; for write, hex 3BA (monochrome emulation) or hex 3DA (color graphics emulation).

Feature Control Register	
7, 6, 5, 4	(reserved)
3	Vertical sync select
2, 1, 0	(reserved)

Bit 3 of this register selects one of two options for the "vertical sync" output. Bit 3 should always be set to 0 to enable normal vertical sync output to the monitor; when bit 3 = 1, the "vertical sync" output is the logical OR of "vertical sync" and "vertical display enable".

Input Status Register 0
An 8-bit read-only register at port address hex 3C2.

Input Status Register 0	
7, 6, 5	(reserved)
4	Switch Sense
3, 2, 1, 0	(reserved)

Bit 4 is the AND output of the DAC monitor sense comparators. These comparators are set for a reference voltage of 0.3V. This bit is a 1 if the R&G&B analog outputs are all less than 0.3V.

Input Status Register 1

An 8-bit read-only register at port address hex 3BA (monochrome emulation) or hex 3DA (color graphics emulation).

Input Status Register 1	
7, 6, 5, 4	(reserved)
3	Vertical retrace
2, 1	(reserved)
0	Display enable not

Bit 3 **Vertical retrace**—The value of bit 3 reflects the state of the "vertical retrace" pulse (0 for inactive, 1 for active).

Bit 0 **Display enable not**—The value of bit 0 reflects the state of the "vertical retrace" and "horizontal retrace" pulses (0 when both are inactive).

SEQUENCER REGISTERS

This section describes the following registers:

Register	Port address
Address Register	3C4H
Reset Register	3C5H (index 0)
Clocking Mode Register	3C5H (index 1)
Map Mask Register	3C5H (index 2)
Character Map Select Register	3C5H (index 3)
Memory Mode Register	3C5H (index 4)

Sequencer Address Register

An 8-bit read/write register at port address hex 3C4.

Sequencer Address Register	
7 6, 5, 4, 3	(reserved)
2	Index, bit 2
1	Index, bit 1
0	Index, bit 0

The three low-order bits of this register contain the index value that identifies one of the sequencer registers at address hex 3C5.

Reset Register

An 8-bit read/write register at index 0

Reset Register	
7, 6, 5, 4, 3, 2	(reserved)
1	Synchronous reset
0	Asynchronous reset

For normal operation, bits 1 and 0 must both be set to 1. Setting either bit to 0 initiates a clear and halt in the sequencer. (This arrangement is required for compatibility with the Enhanced Graphics Adapter.)

Clocking Mode Register

An 8-bit read/write register at index 1

Clocking Mode Register	
7, 6	(reserved)
5	Screen off
4	Shift 4
3	Dot clock
2	Shift load
1	(reserved)
0	8/9 Dot clocks

Bit 5 **Screen off**—Setting bit 5 to 1 blanks the screen and disables the picture-generating logic. This bit can be used for rapid screen updates; disabling the picture logic allows the video processor uninterrupted access to memory.

Bit 4 **Shift 4**
0 loads the video serializers at every cycle of the character clock.
1 loads the video serializers at every fourth cycle of the character clock.

Bit 3 **Dot clock–**
0 selects master clock input to the dot clock .
1 divides the master clock by two to drive the dot clock.

Divide-by-two stretches all timing periods and, for example, is used for 320 PEL and 360 PEL horizontal modes to provide 40 columns of characters.

Bit 2 **Shift load**—The value of this bit is significant only when bit 4 = 0. If that is true:
0 loads the video serializers at every cycle of the character clock.
1 loads the video serializers once for every two cycles of the character clock. (This mode allows 16 bits to be fetched.)

Bit 0 **8/9 dot clocks-**
0 selects nine dots per character cycle.
1 selects eight dots per character clock cycle.

Modes 0+, 1+, 2+, 3+, 7, and 7+ use nine-dot characters; other modes use the ninth dot for background color.

Map Mask Register
An 8-bit read/write register at index 2

Map Mask Register	
7, 6, 5, 4	(reserved)
3	Memory map 3
2	Memory map 2
1	Memory map 1
0	Memory map 0

The four low-order bits of this register control processor write access to the four memory maps:

0 disables write access.
1 enables write access.

With this register set to hex 0F, the processor can complete a 32-bit write operation in one memory cycle. This substantially reduces the overhead on the processor during display update cycles in graphics modes. Data scrolling operations are also enhanced by setting this register to a value of hex 0F and writing the display buffer address with the data stored in the processor data latches.

Note: When odd/even modes are selected, maps 0 and 1 and maps 2 and 3 should have the same map mask value.

Character Map Select Register
An 8-bit read/write register at index 3

The contents of this register are used when the AVGA1 has been programmed to use bit 3 of the character attribute to select a character set in video RAM.

Notes:
1. The Sequencer Memory Mode register bit 1 must be a logical 1 to enable this function; otherwise; the first 8K of map 2 is always selected. Eight character sets can be supported by 256K memory.
2. Any change made to the contents of this register takes effect at the start of the next character line on the display.
3. An asynchronous reset clears this register to logical 0. This should be done only when the sequencer is reset.

Character Map Select Register	
7, 6	(reserved)
5	Character map select, high bit, A
4	Character map select, high bit, B
3, 2	Character map select, A
1, 0	Character map select, B

Bits 5,3,2 Character map select A–A 3-bit pointer to the character set that is to be used when attribute bit 3 = 1. See table on the next page.

Bits 4,1,0 Character map select B-A 3-bit pointer to the character set that is to be used when attribute bit 3 = 0. See table below.

Bits 5,3,2 or 4, 1, 0	Selected Map	Address Offset Into Map
000	0	0K
001	1	16K
010	2	32K
011	3	48K
100	4	8K
101	5	24K
110	6	40K
111	7	56K

Memory Mode Register
An 8-bit read/write register at index 4

Memory Mode Register	
7, 6, 5, 4	(reserved)
3	Chain 4
2	Odd/even
1	Extended memory
0	(reserved)

Bit 3 **Chain 4**

0 enables the processor to access data sequentially in the bit map identified by the Map Mask register. 1 causes the two low-order bits of the address (A1 and A0) to select the map that is accessed

A1	A0	Map
0	0	0
0	1	1
1	0	2
1	1	3

Note: Bit 3, with A1 and A0, controls the map selected in the controller during processor reads. This bit also controls the double word addressing in the CRTC. This bit used with A1 and A0 controls the map selected by the graphics section of the adapter during processor reads.

Bit 2 **Odd/even**

0 directs even processor addresses to access maps 0 and 2, and odd addresses to maps 1 and 3
1 causes the processor addresses to access data sequentially within a bit map.

Bit 1 **Extended memory**

This bit should always be set to 1 to indicate that the total memory installed on the adapter card is 256K and to enable access to the extended memory through address bits 14 and 15.

CRT CONTROLLER (CRTC) REGISTERS

This section describes the following registers:

Register	Port address
CRTC Address Register	3x4H (no index)
Horizontal Total Register	3x5H (index 00H)
Horizontal Display End Register	3x5H (index 01H)
Start Horizontal Blank Register	3x5H (index 02H)
End Horizontal Blank Register	3x5H (index 03H)
Start Horizontal Retrace Register	3x5H (index 04H)
End Horizontal Retrace Register	3x5H (index 05H)
Vertical Total Register	3x5H (index 06H)
Overflow Register	3x5H (index 07H)
Preset Row Scan Register	3x5H (index 08H)
Maximum Scan Line Register	3x5H (index 09H)
Cursor Start Register	3x5H (index 0AH)
Cursor End Register	3x5H (index 0BH)
Start Address High Register	3x5H (index 0CH)
Start Address Low Register	3x5H (index 0DH)
Cursor Location High Register	3x5H (index 0EH)
Cursor Location Low Register	3x5H (index 0FH)
Vertical Retrace Start Register	3x5H (index 10H)
Vertical Retrace End Register	3x5H (index 11H)
Vertical Display End Register	3x5H (index 12H)
Offset Register	3x5H (index 13H)
Underline Location Register	3x5H (index 14H)
Start Vertical Blank Register	3x5H (index 15H)
End Vertical Blank Register	3x5H (index 16H)
CRTC Mode Control Register	3x5H (index 17H)
Line Compare Register	3x5H (index 18H)

x denotes a digit that depends upon the current emulation mode. Use: B for monochrome emulation modes D for color graphics emulation modes.

Index values are loaded into the CRTC Address Register.

CRTC Address Register

An 8-bit read/write register at port address hex 3B4 for monochrome emulation or hex 3D4 for color graphics emulation.

CRTC Address Register	
7, 6	(reserved)
5	(reserved, must be 0)
4	Index bit 4
3	Index bit 3
2	Index bit 2
1	Index bit 1
0	Index bit 0

The value in this register is used as the index that identifies one of the CRTC registers at address hex 3B5 (monochrome emulation) or 3D5 (color graphics emulation).

Horizontal Total Register
An 8-bit read/write register at index hex 00

This register controls the period of the "horizontal retrace" pulse; that is, the time it takes to scan a horizontal line and retrace to the start of the next line. The value set in this register is the value of:

(number of character clock cycles in one horizontal scan and retrace cycle) minus 5.

Horizontal Display Enable End Register
An 8-bit read/write register at index hex 01

This register controls the length of horizontal display enable. The value set into the register is one less than the number of character positions displayed per horizontal scan line.

Start Horizontal Blanking Register
An 8-bit read/write register at index hex 02

This register contains the horizontal character count that triggers the start of the horizontal blanking pulse.

End Horizontal Blanking Register
An 8-bit read/write register at index hex 03

End Horizontal Blanking Register	
7	Reserved (must be 1)
6, 5	Display enable skew control
4	End blanking, bit 4
3	End blanking, bit 3
2	End blanking, bit 2
1	End blanking, bit 1
0	End blanking, bit 0

Bits 6 & 5 Display enable skew control—These bits control the amount of display enable skew in terms of character clock cycles:

Bits 6, 5	
0 0	Zero character clock skew
0 1	One character clock skew
1 0	Two character clock skew
1 1	Three character clock skew

The skew time is, typically, one cycle of the character clock. This allows time for the CRTC to access the display buffer and process the character code and attributes, and ensures that the video output is in synchronization with the "horizontal retrace" and "vertical retrace" signals. This is normally set to 00.

Bits 4 - 0 **End horizontal blanking**—The five low-order bits of the horizontal character count that triggers the end of the "horizontal blanking" pulse. Bit 5 of the count is accessed in the End Horizontal Retrace Pulse register at index 5.

The algorithm that determines this 6-bit value is: r = V + W

where V is the value of the Start Retrace register, W is the required width of the blanking pulse in character clock cycles, and r is the 6-bit result.

Start Horizontal Retrace Pulse Register
An 8-bit read/write register at index hex 04
This register specifies the horizontal character count that triggers the start of the "horizontal retrace" pulse.

End Horizontal Retrace Pulse Register
An 8-bit read/write register at index hex 05

End Horizontal Retrace Pulse Register	
7	End Horizontal Blanking, bit 5
6, 5	Horizontal retrace delay
4	End horizontal retrace, bit 4
3	End horizontal retrace, bit 3
2	End horizontal retrace, bit 2
1	End horizontal retrace. bit 1
0	End horizontal retrace, bit 0

Bit 7 **End horizontal blanking**—The high-order bit of the character count that triggers the end of the "horizontal blanking" pulse. The low-order bits are accessed in the End Horizontal Blanking register.

Bits 6 and 5 **Horizontal retrace delay**—These bits control the skew of the "horizontal retrace" pulse. Binary 00 gives no horizontal retrace delay. For some modes, it is necessary to provide a "horizontal retrace" pulse that takes up the entire blanking interval. Some internal timings are generated by the falling edge of the "horizontal retrace" pulse. To guarantee that the signals are latched properly, the retrace pulse is started before the end of "display enable", and then skewed several character clock cycles to provide the proper screen centering.

Bits 4 - 0 **End horizontal retrace** - The horizontal character count that triggers the end of the "horizontal retrace" pulse. The algorithm that determines this 5-bit value is:

$$r = V + W$$

where V is the value of the Start Retrace register, W is the required width of the retrace pulse in character clock cycles, and r is the 5-bit result.

Vertical Total Register
An 8-bit read/write register at index hex 06

This register contains the eight low-order bits of a 10-bit register that controls the period of the "vertical retrace" pulse; that is the time it takes to scan a full screen and return to the starting point. Bits 9 and 8, the high-order bits, of this register are addressed in the CRTC Overflow register.

The value set in this register is the time, in character clock cycles, for: vertical retrace plus two less than the number of horizontal scan lines on the screen.

CRTC Overflow Register
An 8-bit read/write register at index hex 07

This register contains the high-order overflow bits for CRTC registers that require more than 8 bits:

CRTC Overflow Register	
7	Vertical Retrace Start register, bit 9
6	Vertical Display Enable End register, bit 9
5	Vertical Total register, bit 9
4	Line Compare Register, bit 8
3	Start Vertical Blanking register, bit 8
2	Vertical Retrace Start register, bit 8
1	Vertical Display Enable End register, bit 8
0	Vertical Total register, bit 8

Preset Row Scan Register
An 8-bit read/write register at index hex 08

Preset Row Scan Register	
7	(reserved)
6	Byte panning, bit 1
5	Byte panning, bit 0
4	Preset row scan, bit 4
3	Preset row scan, bit 3
2	Preset row scan, bit 2
1	Preset row scan, bit 1
0	Preset row scan, bit 0

Bits 6 and 5 Byte panning bits - These bits extend the capability for PEL panning by up to three characters (24 or 27 PELs). For details, see "Horizontal PEL Panning Register."

Bits 4 - 0 Preset row scan (PEL scrolling - These bits contain the starting row scan count for use after a vertical retrace. The row scan counter is incremented by the "horizontal retrace" pulse; when the maximum count is reached, the row scan is cleared to zeros.

Maximum Scan Line Register
An 8-bit read/write register at index hex 09

Maximum Scan Line Register	
7	200 to 400 line conversion
6	Line Compare register, bit 9
5	Start Vertical Blanking register, bit 9
4	Maximum scan line, bit 4
3	Maximum scan line, bit 3
2	Maximum scan line, bit 2
1	Maximum scan line. bit 1
0	Maximum scan line, bit 0

Bit 7 **200-to-400 line conversion**—When this bit is set to 1, clock pulses to the row scan counter are divided by 2. This allows 200 line modes to be displayed as 400 lines.

Bits 6 and 5 Overflow bits for the named registers.

Bits 4 - 0 Maximum scan line - Identifies the number of scan lines per character row. The 5-bit value is one less than the actual number.

Cursor Start Register
An 8-bit read/write register at index hex 0A

Cursor Start Register	
7, 6	(reserved)
5	Cursor on/off
4	Starting scan row, bit 4
3	Starting scan row, bit 3
2	Starting scan row, bit 2
1	Starting scan row, bit 1
0	Starting scan row, bit 0

Bit 5 Cursor On/Off—
0 turns on the cursor.
1 turns off the cursor.

Bits 4 - 0 **Starting scan row** - Identifies the starting scan row for the cursor on a character line. The 5-bit value is one less than the actual number.

Cursor End Register
An 8-bit read/write register at index hex 0B

Cursor End Register	
7	(reserved)
6, 5	Cursor skew
4	Ending scan row, bit 4
3	Ending scan row, bit 3
2	Ending scan row, bit 2
1	Ending scan row, bit 1
0	Ending scan row, bit 0

Bits 6 and 5 **Cursor skew** - These bits control the skew of the cursor signal:

Bits 6, 5	
0 0	Zero character clock skew
0 1	One character clock skew
1 0	Two character clock skew
1 1	Three character clock skew

Bits 4 - 0 **Ending scan row**—Identifies the ending scan row for the cursor on a character line.

Start Address High Register
An 8-bit read/write register at index hex 0C

This register contains the 8 high-order bits of the start location in the display buffer.

Start Address Low Register
An 8-bit read/write register at index hex 0D

This register contains the 8 low-order bits of the start location in the display buffer.

Cursor Location High Register
An 8-bit read/write register at index hex 0E

This register contains the 8 high-order bits of the cursor location in the display buffer.

Cursor Location Low Register
An 8-bit read/write register at index hex 0F

This register contains the 8 low-order bits of the cursor location in the display buffer.

Vertical Retrace Start Register
An 8-bit read/write register at index hex 10

This register contains the eight low-order bits of 10-bit scan line count that triggers the start of the "vertical retrace" pulse. The two high order bits are accessed via the CRTC Overflow Register.

Vertical Retrace End Register
An 8-bit read/write register at index hex 11

Vertical Retrace End Register	
7	Protect registers 0 through 7
6	Select 5 refresh cycles
5, 4	(reserved)
3	Vertical retrace end, bit 3
2	Vertical retrace end, bit 2
1	Vertical retrace end, bit 1
0	Vertical retrace end, bit 0

Bit 7 **Protect registers** When bit 7 is set to 1, writing is disabled for the CRTC registers at indexes 0 through 7. Note that you can still write to bit 4, the line compare bit, in the CRTC Overflow register.

Bit 6 **Select 5 refresh cycles** -
0 selects three DRAM refresh cycles per horizontal line.
1 selects five DRAM refresh cycles.

Three cycles are normally used for analog monitors.

Bits 3 - 0 **Vertical retrace end** -The horizontal scan count that triggers the end of the "vertical retrace" pulse. The algorithm used to calculate this 4-bit value is:

r = V + W

where V is the value of the Start Vertical Retrace register, W is the width of the "vertical retrace" pulse in horizontal scan units, and r is the 4-bit result.

Vertical Display Enable End Register
An 8-bit read/write register at index hex 12

This register contains the eight low-order bits of the 10-bit count that triggers the end of the "vertical display enable" pulse. The two high-order bits are accessed via the CRTC Overflow Register.

The value in the 10-bit count is one less than the total number of horizontal scan lines in the video area of the screen.

Offset Register
An 8-bit read/write register at index hex 13

This register contains the logical line width of the screen and determines the offset, in the display buffer, from the start of one character row to the start of next row. The method of clocking the CRTC determines whether this address is a word or double-word address.

Underline Location Register
An 8-bit read/write register at index hex 14

Underline Location Register	
7	(reserved)
6	Double-word mode
5	Count by 4
4	Horizontal scan row, bit 4
3	Horizontal scan row, bit 3
2	Horizontal scan row, bit 2
1	Horizontal scan row, bit 1
0	Horizontal scan row, bit 0

Bit 6 **Double word mode**
0 allows bit 6 of the CRTC Mode Control register to control the addressing mode.
1 forces double-word addresses.

Bit 5 **Count by 4** - Bit 5 is set to 1 when double-word addresses are being used; this divides by 4 the character clock input to the memory address counter.

Bits 4 - 0 **Horizontal scan row**—These bits specify the horizontal scan in the character row that should be used for underlining. The 5-bit value is one less than the actual number.

Start Vertical Blanking Register
An 8-bit read/write register at index hex 15

This register contains the eight low-order bits of the horizontal scan line count that triggers the start of the "vertical blanking" pulse. The two high-order bits are accessed via other CRTC registers: bit 9 is in the Maximum Scan Line register; bit 8 is in the CRTC Overflow register.

The value in the 10-bit count is one less than the total number of horizontal scan lines in the video area of the screen.

End Vertical Blanking Register
An 8-bit read/write register at index hex 16

End Vertical Blanking Register	
7	(reserved)
6	End vertical blanking, bit 6
5	End vertical blanking, bit 5
4	End vertical blanking, bit 4
3	End vertical blanking, bit 3
2	End vertical blanking, bit 2
1	End vertical blanking, bit 1
0	End vertical blanking, bit 0

Bits 6 through 0 of this register contain the horizontal scan line count, that triggers the end of the "vertical blanking" pulse. The algorithm that determines this 7-bit value is:

$$r = V + W$$

where V is the value of the Start Vertical Blanking register, W is the width of the blanking pulse in character clock units, and r is the 7-bit result.

Mode Control Register
An 8-bit read/write register at index hex 17

Mode Control Register	
7	Hardware reset
6	Word/byte mode
5	Address wrap
4	(reserved)
3	Count by 2
2	Horizontal retrace select
1	Select row scan counter
0	CMS 0

Bit 7 Hardware reset–
0 disables the horizontal and vertical retrace outputs.
1 enables the horizontal and vertical retrace outputs.

Bit 6 Word/Byte mode
0 sets the memory address mode to word.
1 sets the memory address mode to byte.

If bit 6 of the Underline Location register is set to 1, the address mode is forced to double-word irrespective of the value assigned to bit 6 of the Mode Control register.

Bit 5 **Address wrap** - This bit should be set to 1. In word mode, this bit controls the output from the memory address counter to the address bus; bit 5 = 1 enables the full 256K of memory on the adapter.

Bit 3 **Count-by-2** -
0 allows each cycle of the character clock to increment the memory address counter (byte-mode increments of the buffer address) 1 divides-by-2 the clock input to the address counter (word-mode increments of the buffer address).

Bit 2 **Horizontal retrace select**–
0 allows each "horizontal retrace" pulse to increment the vertical timing counter.
1 divides-by-2 the "horizontal retrace" input to the vertical timing counter (making it possible to count up to 2048 horizontal lines).

Bit 1 **Select row scan counter**–
0 selects bit 1 of the row scan counter for output as memory address 14.
1 selects the MA 14 counter bit for output as memory address 14.

Bit 0 **Compatibility mode support** -
0 substitutes bit 0 of the row scan address for memory address bit 13 during active display time (see Note).
1 enables memory address bit 13.

Note: The CRTC used on the Color Graphics Adapter is a 6845; this can address a maximum of 128 horizontal scan lines. To obtain 640x200 resolution, the CRTC is programmed for 100 horizontal scan lines with two row scan addresses per character row. Row scan address bit 0 is the most significant address bit to the display buffer. Successive scan lines of the display image are displaced in memory by 8K bytes. This allows bit compatibility with the 6845 and CGA APA modes of operation.

Line Compare Register
An 8-bit read/write register at index hex 18
This register contains the eight low-order bits of the compare value that is used to disable scrolling on a portion of the screen. When the vertical counter reaches this value, the internal start of line counter is cleared.

The two high-order bits are accessed in the CRTC Overflow register.

GRAPHICS CONTROLLER REGISTERS

This section describes the following registers:

Register	Port address
Graphics Address Register	3CEH
Set/Reset Register	3CFH (index 0)
Enable Set/Reset Register	3CFH (index 1)
Color Compare Register	3CFH (index 2)
Data Rotate Register	3CFH (index 3)
Read Map Select Register	3CFH (index 4)
Mode Register	3CFH (index 5)
Miscellaneous Register	3CFH (index 6)
Color Don't Care Register	3CFH (index 7)
Bit Mask Register	3CFH (index 8)

Index values are loaded into the Graphics Address Register.

Graphics Address Register

An 8-bit read/write register at port address hex 3CE.

Graphics Address Register	
7, 6, 5	(reserved)
4	(reserved, must be 0)
3	Index bit 3
2	Index bit 2
1	Index bit 1
0	Index bit 0

The value in this register is used as the index that identifies one of the graphics registers at address hex 3CF.

Set/Reset Register

An 8-bit read/write register at index 0

Set/Reset Register	
7, 6, 5, 4	(reserved)
3	Set/reset, bit plane 3
2	Set/reset, bit plane 2
1	Set/reset, bit plane 1
0	Set/reset, bit plane 0

The four low-order bits of this register are written to the bit planes when the processor does a memory write with write mode 0 selected and set/reset mode enabled.

Set/reset can be enabled on a plane-by-plane basis with separate commands to the enable Set/Reset register. The Bit Mask register allows selected bits in each plane to remain unaffected, provided the memory write was preceded by a processor memory read at the same address.

This register is also the data source for write mode 3. In this mode, bits are masked in each plane by the logical AND of the rotated processor data and the Bit Mask register.

Enable Set/Reset Register
An 8-bit read/write register at index 1

Enable Set/Reset Register	
7, 6, 5, 4	(reserved)
3	Enable set/reset, bit plane 3
2	Enable set/reset. bit plane 2
1	Enable set/reset, bit plane 1
0	Enable set/reset, bit plane 0

The four low-order bits of this register enable the set/reset function in write mode 0; they do nothing in write modes 1, 2, and 3. When set/reset is enabled for a bit plane a write operation writes from the set/reset register to the plane. When disabled, processor data is written to the plane.

Color Compare Register
An 8-bit read/write register at index 2

Color Compare Register	
7, 6, 5, 4	(reserved)
3	Color compare, bit plane 3
2	Color compare, bit plane 2
1	Color compare, bit plane 1
0	Color compare, bit plane 0

The 4 low-order bits of this register contain the compare value that video data is compared with during processor reads. The data returned from the comparison will be a logical 1 in each bit position where the four bit planes equal the compare value.

Notes:
1. Bit planes with Color Don't Care set return a logical 1 to a color compare.
2. Color compare data has no significant meaning in mode hex 13.
3. This register has no effect when Read Mode 0 is selected.

Data Rotate Register
An 8-bit read/write register at index 3

Data Rotate Register	
7, 6, 5	(reserved)
4, 3	Function select
2	Rotate count 2
1	Rotate count 1
0	Rotate count 0

Bits 4 and 3 Function select—These bits determine how the data latches in the processor affects video data that is being written into memory:

Bits 4,3

0 0	Video data unmodified
0 1	Video data ANDed with latched data
1 0	Video data ORed with latched data
1 1	Video data XORed with latched data

Data may be any of the choices selected by the Graphics Mode register except processor latches, which may not be modified. If rotated data is selected, the rotation applies before the logical function.

Bits 2 - 0 Rotate count - This value shows the number of positions that processor data must be right-rotated on memory write operations. Rotate is valid only in write modes 0 and 3; in mode 3, the processor data is rotated before performing the logical AND with the Bit Mask register.

Read Map Select Register
An 8-bit read/write register at index 4

Read Map Select Register	
7, 6, 5, 4, 3, 2	(reserved)
1	Map Select 1
0	Map Select 0

The two low-order bits of this register contain the number (0 through 3) of the bit plane from which the processor is to read data.

Notes:
1. This register has no effect on Color Compare register read mode 1.
2. In odd/even modes the value may be binary 00 or 01 for chained bit planes 0 and 1.
3. This register has no effect in mode hex 13 where all bit planes are chained to form one plane.

Mode Register
An 8-bit read/write register at index 5

Mode Register	
7	(reserved)
6, 5	Shift register control
4	Odd/even
3	Read mode
2	(reserved)
1, 0	Write mode

Bits 6 and 5 Shift register control -

Bits 6,5

0 0	Video map data is loaded directly into the Shift registers.
0 1	Even numbered bits from each map are loaded into even color-bit-plane shift registers (C0 and C2). Odd numbered bits from each map are loaded into the odd color-bit-plane shift registers (C1 and C3). This is used for modes 4 and 5.

1 0 The four most-significant bits of each map are loaded into the shift registers followed by the four remaining bits, so that the high-order data is shifted out first. Data is processed through the shift registers in map sequence; 0 first. 3 last. This is used in mode hex 13.

1 1 (reserved).

Bit 4 Odd/even—In normal use, this bit is the inverse of bit 2 of the Sequencer Memory Mode register. When set to 1, odd/even addressing mode is selected.

Bit 3 Read mode—

0 Causes processor reads to access the bit plane selected by the Read Map Select register.

1 Causes processor reads to access the results of the comparison of the four bit planes and the Color Compare register.

Bits 1 and 0 Write mode—

Bits 1,0

0 0 Write mode 0 - Each bit plane is written with the processor data rotated right by the number of counts in the Rotate register, unless set/reset is enabled for the plane. Planes for which set/reset is enabled are written with 8 bits of the value contained in the Set/Reset register for that plane (SIR). The bit mask allows for selected bits to remain unaffected.

0 1 Write mode 1 - Each bit plane is written with the contents of the processor latches. These latches are loaded by a processor read operation.

1 0 Write mode 2 - Bit plane n (0 through 3) is filled with 8 bits of the value of data bit n (On).

1 1 Write mode 3 - Each plane is written with 8 bits of the value contained in the Set/Reset register for that plane (the Enable Set/Reset Register has no effect). Rotated data is ANDed with the Bit Mask register data to form an 8-bit value that performs the same function as the Bit Mask register in write modes 00 and 10 (see also Bit Mask Register).

Note: The logic function specified by the Function Select bits (Data Rotate register bits D4 and 3) is applied to data being written to memory inmodes 0, 2 and 3.

Any operation using the bit mask requires a read of the target location prior to writing the target.

Miscellaneous Register

An 8-bit read/write register at index 6

Miscellaneous Register	
7, 6, 5, 4	(reserved)
3, 2	Memory map
1	Chain odd maps to even
0	Graphics mode

Bits 3 and 2 Memory map These bits control the mapping of the display buffer into the processor address space:

Bits 3,2	
0 0	Hex A0000 for 128K bytes
0 1	Hex A0000 for 64K bytes
1 0	Hex B0000 for 32K bytes
1 1	Hex B8000 for 32K bytes

Bit 1 **Chain odd maps to even** - When set to 1, this bit directs processor address bit 0 to be replaced by a higher bit, and odd/even maps to be selected with odd/even values of the address bit.

Bit 0 **Graphics mode**
0 selects alphanumeric mode (display data bypasses the graphics section of the adapter and is latched in by the attribute section). 1 selects graphics mode (color data is serialized in the shift registers before it is passed to the attribute section).

Color Don't Care Register
An 8-bit read/write register at index 7

Color Don't Care Register	
7, 6, 5, 4	(reserved)
3	Bit plane 3
2	Bit plane 2
1	Bit plane 1
0	Bit plane 0

The four low-order bits of this register control whether or not a specific bit plane is examined in a color compare operation:

0 disables color comparison.
1 enables color comparison.

When a plane is disabled, the compare result for that plane is forced to an equal compare.

Bit Mask Register
An 8-bit read/write register at index 8

This register provides a bit mask for write operations in write modes 0, 1, and 2. Bits in the mask that are set to 0 disable writes to those positions and preserve the stored value; bits set to 1 allow writes to those bit positions. The bit mask applies to all bit planes simultaneously.

Note that the bit mask applies only when the write location is the location used in the most recent read operation.

ATTRIBUTE CONTROLLER REGISTERS

This section describes the following registers:

Register	Output port address (Note 1)
Attribute Address Register	3C0H (Note 2)
Palette Registers	3C0H (indexes 00H to 0FH)
Mode Control Register	3C0H (index 10H)
Overscan Color Register	3C0H (index 11H)
Color Plane Enable Register	3C0H (index 12H)
Horizontal PEL Panning Register	3C0H (index 13H)
Color Select Register	3C0H (index 14H)

Notes:

1. Attribute controller registers are read from input port 3C1H and written to output port 3C0H.
2. After initialization, Out commands toggle between writing to the Attribute Address register and to the indexed register. See "Attribute Address Register."

Attribute Address Register

An 8-bit read/write register: read from input port hex 3C1H; written to at output port hex 3C0H.

The five low-order bits of this register are used as the index to the other registers on the same port. Out commands to this port are directed alternately to the Attribute Address register and the indexed register.

To initialize the output port: issue an I/O read instruction to the controller at address hex 3BA (monochrome emulation) or hex 3DA (color graphics emulation). This will direct the next Out command to the address register.

Attribute Address Register	
7, 6	(reserved)
5	Palette address source
4	Index bit 4
3	Index bit 3
2	Index bit 2
1	Index bit 1
0	Index bit 0

Bit 5 Palette address source
0 allows the processor to load the Color Palette.
1 allows the memory data to access the Color Palette.

Note: After loading the Color Palette, set bit 5 to 1.

Bits 4 - 0 Index bits The index value that identifies one of the other registers on the attribute controller input/output ports.

Palette Registers
A group of read/write registers at indexes hex 00 through 0F in the Attribute Controller: input port address hex 3C1; output port address hex 3C0. (See "Attribute Address Register.")

Palette Registers	
7, 6	(reserved)
5	Color bit 5
4	Color bit 4
3	Color bit 3
2	Color bit 2
1	Color bit 1
0	Color bit 0

The six low-order bits in these registers map the text attribute or graphic color input value to a display color on the screen. This internal palette is used to contribute to the 8-bit color output of the VGA and allows 16 colors to be displayed simultaneously in text and planar graphics modes. In mode 13, where 256 colors can be displayed simultaneously, these registers remain in use to index into the DAC color table and should not be modified from the default settings.

Mode Control Register
An 8-bit read/write register at index hex 10 in the Attribute Controller.

Mode Control Register	
7	Internal palette size select
6	PEL clock select
5	PEL panning compatibility
4	(reserved)
3	Select background intensity or enable blink
2	Enable line graphics character code
1	Display type
0	Graphics/alphanumeric mode

Bit 7 Internal palette size select—
0 selects the Palette registers as the source for color bits C4 and C5.
1 selects the Color Select register, bits 0 and 1, as the source for color bits C4 and C5

Bit 6 PEL clock select—This bit controls the clocking of PELS at the output of the attribute section of the adapter:

0 allows the PEL data to change at each cycle of the dot clock.
1 allows the PEL data to change only at every other clock cycle.

This is intended for use with Graphics register 5, bits 5 and 6, and allows the attribute palette to create eight bits of color data, for 256 color graphics mode.

Bit 5 PEL panning compatibility–
0 prevents a line compare effecting the output of the PEL Panning register or the byte pan bits of the CRTC.
1 allows a successful line compare in the CRTC to force the output of the PEL Panning register to 0 until the start of the "vertical sync" pulse.

This bit allows a selected portion of a screen to be panned left.

Bit 3 Select background intensity or enable blink–
0 allows bit 7 of the character attributes to control background intensity.
1 allows bit 7 of the character attributes to control blink.

This bit must be set to logical 1 to enable blink in graphics modes.

Bit 2 Enable line graphics character code
0 sets the ninth dot to the background value.
1 enables the special line graphics character codes for monochrome emulation and sets the ninth dot to the same value as the eighth dot.

For character fonts that do not utilize the line graphics character codes hex C0 through hex DF, bit 2 of this register should be set to 0. If this bit is set to 1, unwanted video information is displayed on the screen.

Bit 1 Select display type -
Controls the interpretation of character attributes:

0 selects color display.
1 selects monochrome display.

Bit 0 Graphics/alphanumeric mode–
0 selects alphanumeric mode.
1 selects graphics mode.

Overscan Color Register
An 8-bit read/write register at index hex 11 in the Attribute Controller.

The value in this register determines the color of the border (overscan) area provided in 80-column modes. Overscan borders are not supported in 40-column modes.

Color Plane Enable Register
An 8-bit read/write register at index hex 12 in the Attribute Controller.

Color Plane Enable Register	
7, 6, 5, 4	(reserved)
3	Enable color from bit plane 3
2	Enable color from bit plane 2
1	Enable color from bit plane 1
0	Enable color from bit plane 0

The four low-order bits of this register control whether or not the data read from a specific bit plane is used for video output:

0 disables the bit plane output.
1 enables the bit plane output.

Horizontal PEL Panning Register
An 8-bit read/write register at index hex 13 in the Attribute Controller.

Horizontal PEL Panning Register	
7, 6, 5, 4	(reserved)
3	Panning bit 3
2	Panning bit 2
1	Panning bit 1
0	Panning bit 0

The four low-order bits of this register control PEL panning.

PEL panning is available in A/N and APA modes. In monochrome emulation mode and modes 0+, 1+, 2+, and 3+, the image can be shifted a maximum of eight PELS. In all other A/N and APA modes, the image can be shifted a maximum of seven PELS.

The amount of left-shift for each value is shown below.

Value	Modes 0+, 1+, 2+, 3+, 7, and 7+	Mode 13H	Other Modes
0	1	0	0
1	2	-	1
2	3	1	2
3	4	-	3
4	5	2	4
5	6	-	5
6	7	3	6
7	8	-	7
8	0	-	-

Color Select Register
An 8-bit read/write register at index hex 14 in the Attribute Controller.

Color Select Register	
7, 6, 5, 4	(reserved)
3	Color bit C7
2	Color bit C6
1	Color bit C5
0	Color bit C4

Bits 3 and 2 C7 and C6 - These two bits are used in conjunction with the six bits of the Attribute Palette registers to create the eight bits of color data that are used to address the DAC color LUT.

Bits 1 and 0 C5 and C4 - When bit 7 of the Attribute Mode Control register is set to 1, these two bits supply the values for color output bits C5 and C4. (When bit 7 of the Attribute Mode Control register is set to 0, bits 5 and 4 of the internal palette are used for color bits C5 and C4.)

Video Dot Clock Selection

The dot clock is selected by a combination of Configuration Bit CF(5), Miscellaneous Output Register (I/O port 3C2) bits 3 & 2, and inputs EDCLK and VCLK0, as shown in the following three tables:

INTERNAL VIDEO CLOCK MODE CF(5)=1				
VCLK0	**EDCLK**	**3C2(3)**	**3C2(2)**	**Dot Clock Selected**
X	X	0	0	25.057 MHz
X	X	0	1	28.189 MHz
1	1	1	0	41.164 MHz
1	1	1	1	35.795 MHz
X	0	1	X	DCLK input

EXTERNAL VIDEO CLOCK MODE CF(5)=0				
VCLK0	**EDCLK**	**3C2(3)**	**3C2(2)**	**Dot Clock Selected**
X	X	0	0	VCLK0 input
X	X	0	1	VCLK1 input
X	1	1	X	VCLK2 input
X	0	1	X	DCLK input

HALF INTERNAL VIDEO CLOCK MODE CF(5)=1				
VCLK0	**EDCLK**	**3C2(3)**	**3C2(2)**	**Dot Clock Selected**
X	X	0	0	25.057 MHz
X	X	0	1	28.189 MHz
0	1	1	0	VCLK1 input
0	1	1	1	VCLK2 input
X	0	1	X	DCLK input

132-Column Alphanumeric Mode

This extended video mode is selected if the CRT Controller Horizontal Total register (index 0) is programmed with any value ≥ 80H. The Video Dot Clock is 41.164 MHz, selected by programming Miscellaneous Output Register bit 3=1 and bit 2=0. The Sequencer is programmed for 8-dot character intervals, with a non-divided dot clock.

The Character Map(s) should be loaded *while* this mode is selected, because the memory organization of the Character Maps differs from the normal VGA case. Loading the Character Maps, however, needs no special address translation incorporated into programming, because the AVGA1 remaps Video memory automatically when this mode is selected. The Character Maps should be loaded by unchained (sequential) addressing, the AVGA1 having been mapped into System Address segment A0000 for 64Kb locations, with the Sequencer Map Mask Register programmed to enable writing to Plane 2. Subsequently, the AVGA1 should be programmed for Chain 2 addressing, with Planes 0 & 1 enabled, as is normally the case in an Alphanumeric mode.

This mode does not support displaying two different character maps on the screen at the same time, as determined by character attribute bit 3 in the normal VGA operation. However, one of eight Character Maps can be selected for the entire screen display, by programming the Sequencer Character Map Select Register (3C5, index 03) bits 2:0 with a Character Map number. The Character Map number represents one 8Kb segment of the total available 64Kb of Character Maps in this mode. Each Character Map number corresponds to an 8Kb offset from the initial System Address segment where the Maps are loaded initially: Map 0 is loaded into A0000-A1FFF, Map 1 into A2000-A3FFF, etc. Note the functional change of the Character Map Select register bits 2:0 when this mode is selected; the remaining bits 5:3 are not used.

The AVGA1 uses both Plane 2 and Plane 3 physical DRAM pages for Character Map storage in this mode, although the Character Maps appear to be loaded into Plane 2 only. The AVGA1 remaps character generator dot patterns of all lower 128 character codes into Plane 2, and all the upper 128 into Plane 3. Only half of each 64Kb physical Plane is therefore used, providing a total of eight, 8Kb Character Maps.

The only significant difference in the AVGA1 register programming in this mode, compared to an 80-column 8-dot Alpha mode, is in the CRT Controller. The following CRT Controller parameters are recommended in this mode:

Data	Register
9FH	Horizontal Total (index 0)
83H	Horiz Display Enable End (index 1)
84H	Start Horizontal Blanking (index 2)
82H	End Horizontal Blanking (index 3)
8AH	Start Horizontal Retrace (index 4)
9EH	End Horizontal Retrace (index 5)
42H	Offset (index 13H)

This mode is disabled whenever the CRTC Horizontal Total Register is programmed with a value ≤ 7FH.

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AVGA1

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