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1 SiS530/SiS5595 OVERVIEW

SiS530 Host, PCI, 3D A.G.P. Video/Graphics & Memory Controller
SiS5595 PCI SYSTEM I/O

The P5 A.G.P./VGA chipset, SiS530/5595, provides a high performance/cost index Desktop/Mobile solution for the Intel Pentium P54C/P55C, AMD K5/K6/K6-II, Cyrix M1/M2 and other compatible Pentium CPU with 3D A.G.P. VGA system.

The Host, PCI, 3D A.G.P. Video/Graphics & Memory Controller, SiS530 integrates the Host-to-PCI bridge, the PCI interface, the L2 cache controller, the DRAM controller, the high performance hardware 2D/3D VGA controller, and the PCI IDE controller.

The Host interface supports Synchronous/Asynchronous Host/DRAM clocking configuration to eminently improve the system performance and DRAM compatibility issues.

The L2 cache controller can support up to 2 MB P.B. SRAM, and the DRAM controller can support SDRAM memory up to 1.5 GBytes with three double-sided SDRAM DIMMs configuration. The cacheable DRAM sizes support up to 256 MBytes.

The built-in fast PCI IDE controller supports the ATA PIO/DMA, and the Ultra DMA33/66 function that support the data transfer rate up to 66 MB/s. It provides the separate data path for two IDE channels that can eminently improve the performance under the multi-tasking environment.

The A.G.P. internal interface is supported for integrated H/W 3D VGA controller. The integrated VGA controller is a high performance and targeted at 3D graphics application. In addition, the integrated 3D Video/Graphics controller adopts the 64bits 100MHz host bus interface high technology to improve the performance eminently. To cost-effective the PC system, the share system memory architecture will be adopted and it can flexibly using the 2MB, 4MB and 8MB frame buffer size from programming the system BIOS. To enhance the system performance, SiS530 also supports the local frame buffer solution and memory sizes can support up to 8MB with SDRAM and SGRAM.

In addition to provide the standard interface for CRT monitors, it also provides the Digital Flat Panel Port (DFP) for a standard interface between a personal computer and a digital flat panel monitor. This port allows a host computer to connect directly to an external flat panel monitor without the need for analog-to-digital conversion found in most flat panel monitors today. As for DVD solution, the integrated 3D VGA controller also support DVD H/W accelerator to improve the DVD playback performance.

The SiS5595 PCI system I/O integrates the PCI-to-ISA bridge with the DDMA, PC/PCI DMA and Serial IRQ capability, the ACPI/Legacy PMU, the Data Acquisition Interface, the Universal Serial Bus host/hub interface, and the ISA bus interface which contains the ISA bus controller, the DMA controllers, the interrupt controllers, the Timers and the Real Time Clock (RTC). It also integrates the Keyboard Controller and PS/2 mouse interface that can support keyboard power on function for users to power on system by entering the hot key or password from keyboard. The built-in USB controller, which is fully compliant to OHCI (Open Host Controller Interface), provides two USB ports capable of running full/low speed USB devices. The Data Acquisition Interface offers the ability of monitoring and reporting the environmental condition of the PC. It could monitor 5 positive analog voltage inputs, 2 Fan speed inputs, and one temperature input.

In addition, SiS5595 also supports ACPI function to meet ***Advanced Configuration and Power Interface*** (ACPI) 1.0 specification for Windows 98 environment, it can support power-management timer, Power button, Real-time clock alarm wake up, more sleeping state, ACPI LED for sleeping and working state, LAN wake up, Modem Ring In wake up, and OnNow initiative function.

The following will show the system block diagram.

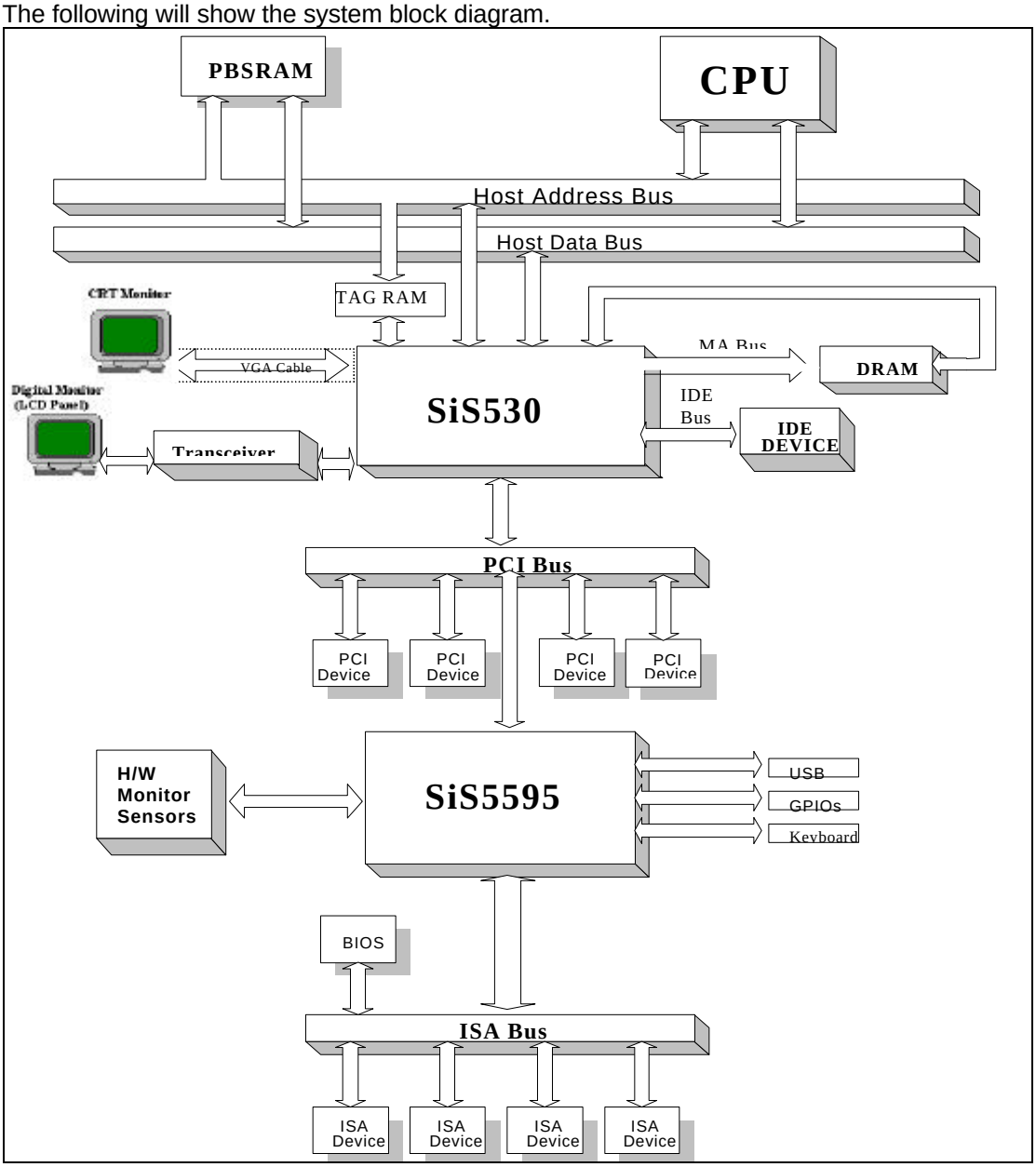


Figure 1.1-1 SiS530/SiS5595 System Block Diagram

2 FEATURES

2.1 SiS530 HOST, PCI, 3D A.G.P. VIDEO/GRAPHICS & MEMORY CONTROLLER

- **Supports Intel/AMD/Cyrix/IDT Pentium CPU Host Bus at 66/75/83/95/100 MHz and 2.5/3.3V Bus Interface**
  - Supports the Pipelined Address of Pentium compatible CPU
  - Supports the Linear Address Mode of Cyrix CPU
  - 100/100, 95/95, 83/83, 75/75 and 66/66 MHz Synchronous Host/DRAM clocking configuration
  - 100/75, 95/75, 83/66, 66/100 and 66/83 MHz Asynchronous Host/DRAM clocking configuration
  - Supports Host Bus operation for integrated 3D VGA Controller
- **Meets PC99 Requirements**
- **Supports PCI Revision 2.2 Specification**
- **Integrated Super AGP VGA for Hardware 2D/3D Video/Graphics Accelerators**
  - Supports tightly coupled 64 bits 100MHz host interface to VGA to speed up GUI performance and the video playback frame rate
  - Built-in programmable 24-bit true-color RAMDAC up to 230 MHz pixel clock
  - Built-in reference voltage generator and monitor sense circuit
  - Supports loadable RAMDAC for gamma correction in high color and true color modes
  - Built-in dual-clock generator
  - Supports Multiple Adapters and Multiple Monitors
  - Built-in PCI multimedia interface
  - Flexible design for shared frame buffer or local frame buffer architecture
  - Shared System Memory Area 2MB, 4MB and 8MB
  - Supports SDRAM and SGRAM local frame buffer and memory size up to 8 MB
  - Supports Digital Flat Panel Port for Digital Monitor (LCD Panel)
  - Supports DVD H/W Accelerator
- **Integrated Second Level (L2) Cache Controller**
  - Write Back Cache Mode
  - Direct Mapped Cache Organization
  - Supports Pipelined Burst SRAM
  - Supports 256K/512K/1M/2M Bytes Cache Sizes
  - Cache Hit Read/Write Cycle of 3-1-1-1
  - Cache Back-to-Back Read Cycle of 3-1-1-1-1-1-1-1
  - Supports Single Read Allocation for L2 Cache
  - Supports Concurrency of CPU to L2 cache and Integrated A.G.P. VGA master to DRAM accesses
- **Integrated DRAM Controller**
  - Supports up to 3 double sided DIMMs (6 rows memory)
  - Supports 8Mbytes to 1.5 GBytes of main memory
  - Supports Cacheable DRAM Sizes up to 256 MBytes
  - Supports 1M/2M/4M/8M/16M/32M x N for 2-bank or 4-bank SDRAM

- Supports 3.3V DRAM
- Supports Concurrent Write Back
- Supports CAS before RAS Refresh, Self Refresh
- Supports Relocation of System Management Memory
- Programmable CS#, DQM#, SRAS#, SCAS#, RAMWE# and MA Driving Current
- Option to Disable Local Memory in Non-cacheable Regions
- Entries GART cache to Minimize the Number of Memory Bus Cycles Required for Accessing Graphical Texture Memory
- Programmable Counters to Ensure Guaranteed Minimum Access Time for Integrated A.G.P. VGA, CPU, and PCI accesses
- Two Programmable Non-cacheable Regions
- Supports X-1-1-1/X-2-2-2 Burst Write Cycles
- Fully Configurable for the Characteristic of Shadow RAM (640 KBytes to 1 MBytes)
- Shadow RAM in Increments of 16 KBytes Built-in 8 Way Associative/16
- Supports SDRAM 7/8-1-1-1 Burst Read Cycles

■ **Provides High Performance PCI Arbiter**

- Supports up to 4 PCI Masters
- Supports Rotating Priority Mechanism
- Hidden Arbitration Scheme Minimizes Arbitration Overhead
- Supports Concurrency between CPU to Memory and PCI to PCI
- Supports Concurrency between CPU to 33Mhz PCI Access and 33Mhz PCI to integrated A.G.P. VGA Access
- Programmable Timers Ensure Guaranteed Minimum Access Time for PCI Bus Masters, and CPU

■ **PCI Bus Interface**

- Supports 32-bit PCI local bus standard Revision 2.2 compliant
- Integrated write-once subsystem vendor ID configuration register
- Supports zero wait-state memory mapped I/O burst write
- Integrated 2 stages PCI post-write buffer to enhance frame buffer write performance
- Integrated 256 bits read cache to enhance frame buffer read performance
- Supports full 16-bit re-locatable VGA I/O address decoding

■ **Integrated Host-to-PCI Bridge**

- Supports Asynchronous PCI Clock
- Translates the CPU Cycles into the PCI Bus Cycles
- Zero Wait State Burst Cycles
- Supports Pipelined Process in CPU-to-PCI Access
- Maximum PCI Burst Transfer from 256 Bytes to 4 Kbytes
- Supports Memory Remapping Function for PCI master accessing Graphical Window

■ **Integrated A.G.P. Compliant Target/66Mhz Host-to-PCI Bridge**

- Supports Graphic Window Size from 4MBytes to 256MBytes
- Supports Pipelined Process in CPU-to-Integrated 3D A.G.P. VGA Access
- Supports 8 Way, 16 Entries Page Table Cache for GART to enhance Integrated A.G.P. VGA Controller Read/Write Performance

- Supports PCI-to-PCI bridge function for memory write from 33Mhz PCI bus to Integrated A.G.P. VGA

- **Integrated Posted Write Buffers and Read Prefetch Buffers to Increase System Performance**
  - CPU-to-Memory Posted Write Buffer (CTMFF) with 12QW Deep, Always Sustains 0 Wait Performance on CPU-to-Memory
  - CPU-to-Memory Read Buffer with 4 QW Deep
  - CPU-to-PCI Posted Write Buffer with 2 QW Deep
  - PCI-to-Memory Posted Write Buffer with 8 QW Deep, Always Streams 0 Wait Performance on PCI-to/from-Memory Access
  - PCI-to-Memory Read Prefetch Buffer with 8 QW Deep
  - CPU-to-VGA Posted Write Buffer with 4 QW Deep
- **Fast PCI IDE Master/Slave Controller**
  - Bus Master Programming Interface for Windows 98 Compliant Controller
  - Plug and Play Compatible
  - Supports Scatter and Gather
  - Supports Dual Mode Operation - Native Mode and Compatibility Mode
  - Supports IDE PIO Timing Mode 0, 1, 2 ,3 and 4
  - Supports Multiword DMA Mode 0, 1, 2
  - Supports Ultra DMA 33/66
  - Two Separate IDE Bus
  - Two 16 DW FIFO for PCI Burst Transfers.
- **Supports NAND Tree for Ball Connectivity Testing**
- **576-Balls BGA Package**
- **3.3V Core with mixed 2.5V, 3.3V and 5V I/O CMOS Technology**

2.1.1. INTEGRATED HIGH PERFORMANCE & HIGH QUALITY 3D GRAPHICS/VIDEO ACCELERATORS

High Performance & High Quality 3D Accelerator

- Integrated a high performance 3D engine
- Integrated 32-bit floating point format VLIW triangle setup engine
- Integrated 16kbit texture cache
- Supports Super-AGP for texture fetch
- Peak polygon rate: 800K polygon/sec @ 50 pixel/polygon with Gouraud shaded, point-sampled, linear and bilinear texture mapping
- Peak fill rate: 40M pixel/sec
- Integrated a high quality 3D engine
- Supports solid, flat, and Gouraud shading
- Supports high quality dithering
- Supports Z-test, Alpha-test, and scissors clipping test
- Supports line pattern, and ROP
- Supports Z-buffer and Alpha buffer
- Supports per-pixel texture perspective correction
- Supports point-sampled, linear, bi-linear, and tri-linear texture filtering
- Supports MIP structure texture
- Supports rectangle structure texture
- Supports 1/2/4 BPP palletize texture
- Supports 1/2/4/8 BPP luminance texture
- Supports 4/8 BPP mix mode texture format
- Supports 8/16/24/32 BPP RGB/ARGB texture format
- Supports video texture in all supported texture formats
- The supported video formats are RGB555, RGB565, and YUV422 formats
- Supports texture transparency, blending, wrapping, mirror, and clamping
- Supports fogging, Alpha blending, and primitive transparency

High Performance 2D Accelerator

- Integrated 42 double-words hardware command queue
- Supports Turbo Queue (Software Command Queue in off-screen memory) architecture to achieve extra-high performance
- Integrated Direct Draw Accelerator
- Integrated 1T 64-bit BITBLT graphics engine with the following functions:

– 256 raster operations

- Rectangle fill
- Color expansion
- Enhanced Color expansion
- Multiple Scan-line
- Poly-Line-drawing with styled pattern
- Integrated 8x8 pattern registers
- Integrated 8x8 mask registers
- Rectangle Clipping
- Transparent BitBlt
- Trapezoid Fill

- Supports memory-mapped, zero wait-state, burst engine write
- Supports burst frame buffer read/write for SDRAM
- Integrated 64x64x2 bit-mapped hardware cursor
- Maximum 8M Bytes frame buffer with linear addressing
- Integrated 4 stages engine write-buffer and 9x64 bits read-buffer to minimize engine wait-state
- Integrated 64x32 CRT FIFOs to support super high resolution graphics modes and reduce CPU wait-state

Video Accelerator

- Supports single frame buffer architecture
- Supports YUV-to-RGB color space conversion
- Supports bi-linear video interpolation with integer increments of 1/64
- Supports graphics and video overlay function
- Independent graphics and video formats
- 16 color-key and/or chroma-key operation
- 3-bit graphics and video blending
- Supports current scan line of refresh read-back
- Supports tearing free double buffer swapping
- Supports RGB555, RGB565, YUV422, and YUV420 video format
- Integrated two 96x64 video playback line buffers
- Supports DCI Drivers
- Supports Direct Draw Drivers

DVD H/W Accelerator

- Supports Color Space Conversion
- Supports Video Scaling
- Supports YUV12 Format

Display Memory Interface

Supports Local Frame Buffer:

- Supports SDRAM and SGRAM timing
- Supports 32/64 bits LVTTL memory data bus interface
- Supports Block-Write function for SGRAM
- Supports 2MB, 4MB, and 8MB memory configuration
- Supports 1Mx16, 1Mx32, 256Kx32, 512Kx32 SDRAM/SGRAM types up to 100 MHz

Supports Shared Frame Buffer:

- Supports SDRAM timing
- Supports 64 bits memory data bus interface
- Supports programmable 2MB, 4MB, and 8MB memory configuration

High Integration

- Integrated programmable 24-bit true-color RAMDAC up to 230 MHz pixel clock
- Integrated reference voltage generator and monitor sense circuit
- Supports loadable RAMDAC for gamma correction in high color and true color modes
- Integrated dual-clock generator
- Integrated PLL loop filter
- Integrated two 96x64 video line buffers for MPEG video playback
- Integrated PCI multimedia interface

Resolution, Color & Frame Rate

- Supports 230 MHz pixel clock
- Supports super high resolution graphics modes
- 640x480 4/8/16/32 bpp @85Hz NI
- 800x600 8/16/32 bpp @ 85Hz NI
- 1024x768 8/16/32 bpp @ 85Hz NI
- 1280x1024 8/16/32 bpp @ 85 Hz NI (32-bpp mode for local frame buffer only)
- 1600x1200 8/16 bpp @256 colors 85Hz NI (16-bpp mode for local frame buffer only)
- Supports virtual screen up to 2048x2048
- Supports 80/132 columns text modes

Digital Flat Panel Port

- Supports low-cost TMDS and LVDS interface
- Supports TFT-24bit, TFT-18bit, TFT-12bit LCD Monitor
- Supports DDC2B (VESA DDC 3.0) for display configuration and detection
- VESA DPMS support for display power management

- Compliant with VESA EDID 2.0 Standard
- Supports Hot Plugging function defined by VESA Plug and Display (P&D) 1.0 Standard
- Supports up to 1024x768@75Hz (VESA standard CRT timings)
- Supports 85MHz pixel clock for 1280x1024 flat panel display by using the reduced refresh rate timing

Power Management

- Supports VESA Display Power Management Signaling (DPMS) compliant VGA monitor for power management
- Supports direct I/O command to force graphics controller into standby/suspend/off state
- Power down internal SRAM in direct color mode

Multimedia Application

- Supports DDC1 and DDC2B specifications
- Supports RAMDAC snoop for multimedia applications

Miscellaneous

- Supports Signature Analysis for automatic test

2.2. FUNCTIONAL BLOCK DIAGRAM

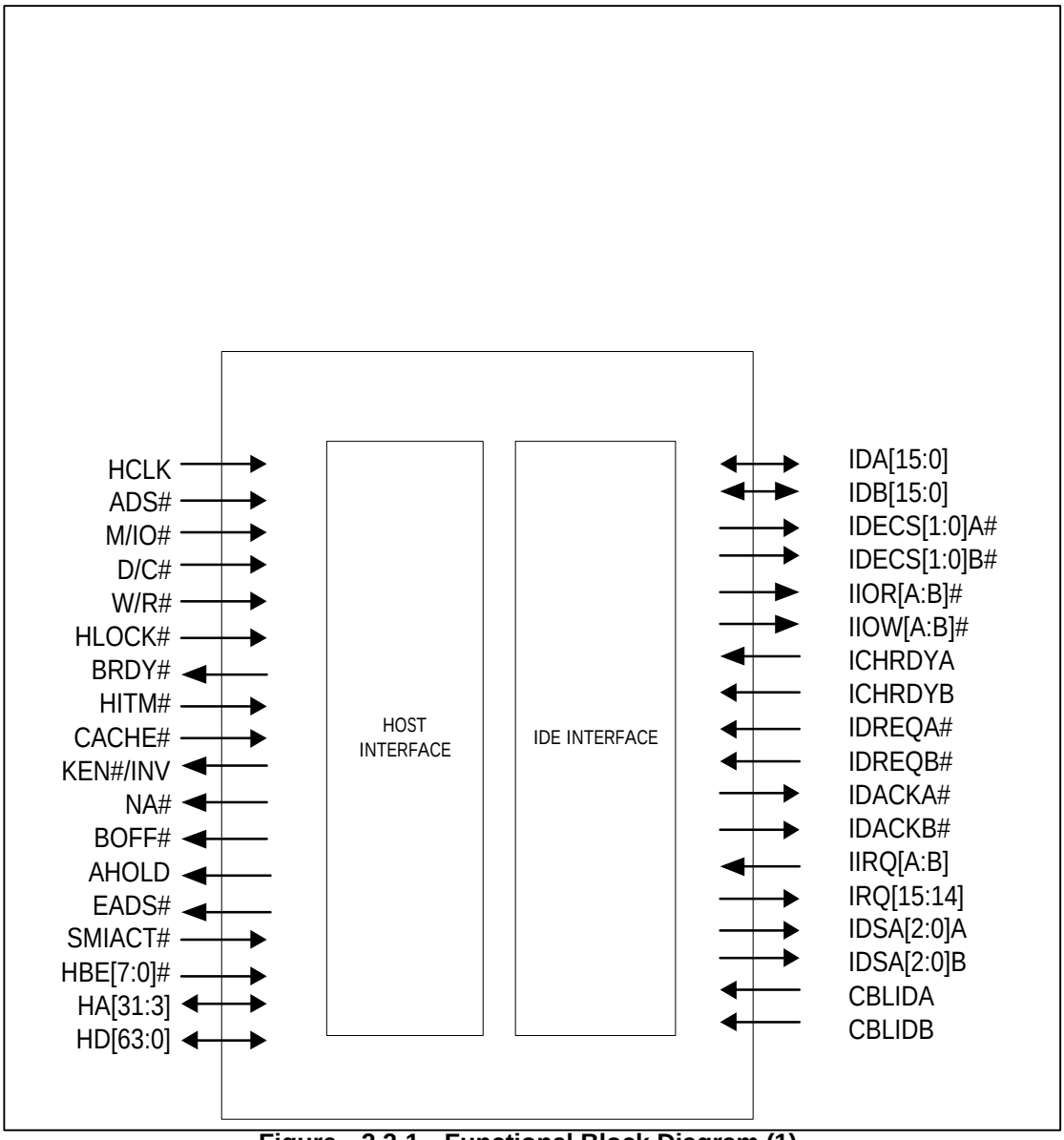


Figure 2.2-1 Functional Block Diagram (1)

~To be continued

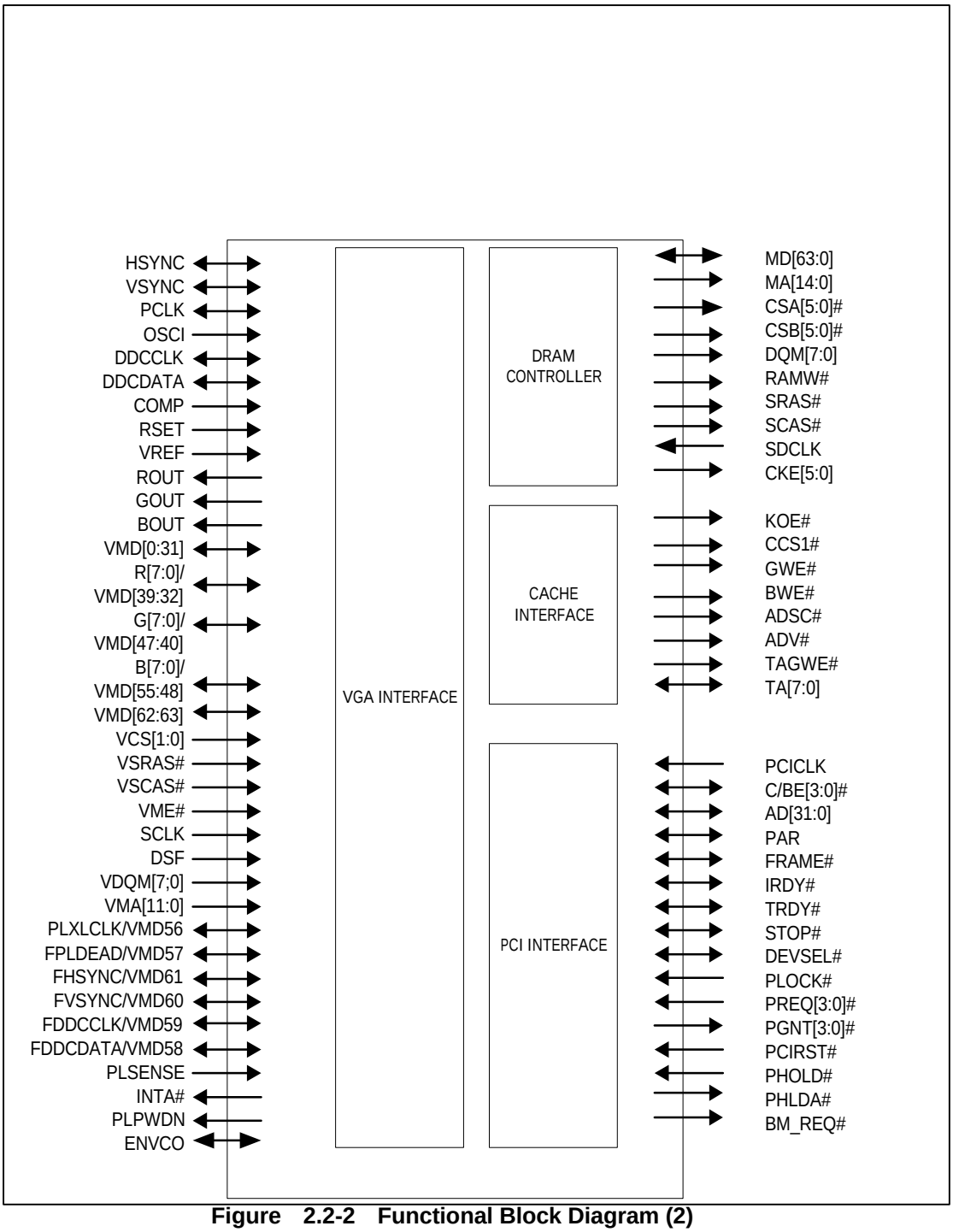


Figure 2.2-2 Functional Block Diagram (2)

3 PIN ASSIGNMENT

3.1. SiS530 PIN ASSIGNMENT (TOP VIEW-LEFT SIDE)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A			AVDD1	AVDD 2/3	BOUT	ROUT	AVSS4	MD29	MD59	MD24	MD22	MD19	MD49	CKE2	CKE4	A
B		ENVCO	DDCCLK	AVSS 2/3	AVDD4	GOUT	RSET	MD62	MD27	MD57	MD55	MD52	MD17	CKE1	DQM3	B
C	VMD63	PLPWD N	DDCDATA	VSYNC	NC	NC	VREF	MD30	MD28	MD25	MD23	MD20	MD18	CKE0	DQM7	C
D	PL-DCLK	VMD60	VMD62	HSYNC	NC	NC	NC	MD31	MD60	MD26	MD54	MD21	MD51	MD16	DQM2	D
E	VCS1#	VMD56	VMD57	VMD59	OSCI	AVSS1	COMP	MD63	MD61	MD58	MD56	MD53	MD48	CKE5	NC	E
F	VMD55	VDQM4	VDQM6	VDQM7	PLSENS E								MD50	CKE3	NC	F
G	VMD50	VMD51	VMD52	VMD54	VMD61											G
H	VMD44	VMD46	VMD47	VMD48	VMD58											H
J	VMD40	VMD42	VMD43	VMD53	VDQM5											J
K	VMD35	VMD36	VMD38	VMD39	VMD49						OVDD 3	DVDD	OVDD 3	DVDD	OVDD3	K
L	SCLK	VMD32	VMD34	VMD41	VMD45					OVDD 3						L
M	VMA8	VMA9	VMA10	DSF	VMD37					DVDD		VSS	VSS	VSS	VSS	M
N	VMA3	VMA4	VMA6	VMA7	VMA11	VMD33				OVDD 3		VSS	VSS	VSS	VSS	N
P	VSRAS#	VCS0#	VMA0	VMA2	VMA1	VMA5				DVDD		VSS	VSS	VSS	VSS	P
R	VMD29	VMD30	VWE#	VSCAS#	NC	NC				OVDD 3		VSS	VSS	VSS	VSS	R
T	VMD28	VMD27	VMD26	VMD25	VMD31	VDQM3				DVDD		VSS	VSS	VSS	VSS	T
U	VMD24	VDQM2	VDQM0	VMD23	VDQM1	VMD21				OVDD 3		VSS	VSS	VSS	VSS	U
V	VMD22	VMD20	VMD19	VMD18	VMD17					DVDD		VSS	VSS	VSS	VSS	V
W	VMD16	VMD15	VMD14	VMD13	VMD9					OVDD 3						W
Y	VMD12	VMD11	VMD10	VMD8	VMD5					OVDD 3	OVDD 3	DVDD	OVDD 3	DVDD	OVDD3	Y
AA	VMD7	VMD6	VMD4	VMD1	PHOLD#											AA
AB	VMD3	VMD2	VMD0	INTA#	PREQ2#											AB
AC	PHLDA#	BMREQ#	PCIRST#	PREQ3#	PGNT3#											AC
AD	PREQ0#	PREQ1#	PGNT0#	PGNT1#	AD28								IDA12	IIOWA	NC	AD
AE	PGNT2#	AD31	AD30	AD29	5VDD	AD20	AD16	TRDY#	PAR	AD4	AD0	IDA10	IDA14	IIRQA	NC	AE
AF	AD27	AD26	AD25	AD24	AD17	DEVSEL #	AD15	AD11	AD9	AD3	IDA8	IDA9	IDA3	IDA0	ICHRDY A	AF
AG	AVDD	PCICLK	AVSS	AD21	C/BE2#	PLOCK#	AD14	AD10	AD7	AD2	IRQ15	IDA5	IDA2	IDA15	IDACKA #	AG
AH		C/BE3#	AD23	AD19	FRAME#	STOP#	AD13	AD8	AD6	AD1	IDA7	IDA4	IDA13	IDRE QA	IDSAA1	AH
AJ			AD22	AD18	IRDY#	C/BE1#	AD12	C/BE0#	AD5	IRQ14	IDA6	IDA11	IDA1	IIORA	IDSAA0	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

3.2. SiS530 PIN ASSIGNMENT (TOP VIEW-RIGHT SIDE)

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	AVDD	SDCLK	MA14	MA8	MA4	CSA0#	CSA4#	DQM0	MD14	MD12	MD9	MD40			A
B	CSB0#	CSB4#	MA12	MA7	MA3	CSA1#	CSA5#	DQM4	MD46	MD11	MD41	MD39	MD6		B
C	CSB1#	CSB5#	MA11	MA6	MA2	CSA3#	SRAS#	WE#	MD13	MD43	MD8	MD38	MD5	MD37	C
D	CSB2#	TEST#	MA10	MA5	MA0	DQM5	DQM1	MD15	MD45	MD10	MD36	MD3	MD35	MD34	D
E	DQM6	AVSS	MA9	MA1	CSA2#	SCAS#	MD47	MD44	MD42	MD7	MD1	MD33	MD32	TAGWE#	E
F	CSB3#	MA13								MD4	TA7	TA6	TA5	TA3	F
G										MD2	TA2	TA1	CCS1#	GWE#	G
H										MD0	BWE#	ADSC#	KOE#	HA30	H
J										TA4	TA0	HA4	HA29	HA3	J
K	DVDD	OVDD3	DVDD	OVDD3	OVDD3					ADV#	HA28	HA22	HA26	HA21	K
L					OVDD3					HA6	HA24	HA27	HA25	HA7	L
M	VSS	VSS	VSS		DVDD					HA23	HA8	HA5	HA11	HA9	M
N	VSS	VSS	VSS		OVDD2				HA31	HA10	HA12	HA15	HA14	HA16	N
P	VSS	VSS	VSS		DVDD				HA13	HA17	HA18	HA19	HA20	HBE7#	P
R	VSS	VSS	VSS		OVDD2				NC	NC	HBE2#	HBE4#	HBE5#	HBE6#	R
T	VSS	VSS	VSS		DVDD				HBE1#	HBE3#	ADS#	EADS#	W/R#	HBE0#	T
U	VSS	VSS	VSS		OVDD2				NA#	HITM#	AHOLD	BRDY#	BOFF#	HLOCK#	U
V	VSS	VSS	VSS		DVDD					M/IO#	SMIACT#	CACHE#	KEN#/INV	D/C#	V
W					OVDD2					HD6	HD1	HD3	HD2	HD0	W
Y	DVDD	OVDD2	DVDD	OVDD2	OVDD2					HD10	HD8	HD7	HD5	HD4	Y
AA										HD17	HD13	HD12	HD11	HD9	AA
AB										HD23	HD16	HD18	HD15	HD14	AB
AC										HD29	HD19	HD21	HD20	HD22	AC
AD	IDB8	IDB13								HD35	HD28	HD25	HD26	HD24	AD
AE	CBLIDA	IDB10	IDB15	CBLIDB	HD62	HD51	HD43	HD45	HD42	AVSS	HD33	HD31	HD30	HD27	AE
AF	IDB7	IDB4	IDB2	ICHRDYB	IDACKB#	HD58	HD63	HD57	HD53	HD48	HD44	HD37	HD34	HD32	AF
AG	IDECSA1#	IDB5	IDB12	IDB0	IIORB	IDSAB0	IDECSB1#	HD59	HD54	HD49	HD41	HD40	HD39	HD36	AG
AH	IDECSA0#	IDB9	IDB3	IDB14	IIOWB	IDSAB1	IDECSB0#	HD60	HD55	HD50	HD47	HD46	HD38		AH
AJ	IDSAA2	IDB6	IDB11	IDB1	IDREQB	IIRQB	IDSAB2	HD61	HD56	HD52	HCLK	AVDD			AJ
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

3.3. SiS530 ALPHABETICAL PIN LIST

SIGNAL NAME	SiS530 BALL NO
5VDD	AE5
AD0	AE11
AD1	AH10
AD2	AG10
AD3	AF10
AD4	AE10
AD5	AJ9
AD6	AH9
AD7	AG9
AD8	AH8
AD9	AF9
AD10	AG8
AD11	AF8
AD12	AJ7
AD13	AH7
AD14	AG7
AD15	AF7
AD16	AE7
AD17	AF5
AD18	AJ4
AD19	AH4
AD20	AE6
AD21	AG4
AD22	AJ3
AD23	AH3
AD24	AF4
AD25	AF3
AD26	AF2
AD27	AF1
AD28	AD5

SIGNAL NAME	SiS530 BALL NO
AD29	AE4
AD30	AE3
AD31	AE2
ADS#	T26
ADSC#	H27
ADV#	K25
AHOLD	U26
AVDD	AG1
AVDD	A16
AVDD	AJ27
AVDD1	A3
AVDD2/3	A4
AVDD4	B5
AVSS	AG3
AVSS	E16
AVSS	E17
AVSS	AE25
AVSS1	E6
AVSS2/3	B4
AVSS4	A7
BMREQ#	AC2
BOFF#	U28
BOUT	A5
BRDY#	U27
BWE#	H26
C/BE0#	AJ8
C/BE1#	AJ6
C/BE2#	AG5
C/BE3#	AH2
CACHE#	V27

SIGNAL NAME	SiS530 BALL NO
CBLIDA	AE16
CBLIDB	AE19
CCS1#	G28
CKE0	C14
CKE1	B14
CKE2	A14
CKE3	F14
CKE4	A15
CKE5	E14
COMP	E7
CSA0#	A21
CSA1#	B21
CSA2#	E20
CSA3#	C21
CSA4#	A22
CSA5#	B22
CSB0#	B16
CSB1#	C16
CSB2#	D16
CSB3#	F16
CSB4#	B17
CSB5#	C17
D/C#	V29
DDCCLK	B3
DDCDATA	C3
DEVSEL#	AF6
DQM0	A23
DQM1	D22
DQM2	D15
DQM3	B15

SIGNAL NAME	SiS530 BALL NO
DQM4	B23
DQM5	D21
DQM6	E16
DQM7	C15
DSF	M4
DVDD	M10
DVDD	P10
DVDD	T10
DVDD	V10
DVDD	K12
DVDD	Y12
DVDD	Y13
DVDD	K14
DVDD	Y14
DVDD	K18
DVDD	Y18
DVDD	M20
DVDD	P20
DVDD	T20
DVDD	V20
EADS#	T27
ENVCO	B2
FRAME#	AH5
GOUT	B6
GWE#	G29
HA3	J29
HA4	J27
HA5	M27
HA6	L25
HA7	L29
HA8	M26

SIGNAL NAME	SiS530 BALL NO
HA9	M29
HA10	N25
HA11	M28
HA12	N26
HA13	P24
HA14	N28
HA15	N27
HA16	N29
HA17	P25
HA18	P26
HA19	P27
HA20	P28
HA21	K29
HA22	K27
HA23	M25
HA24	L26
HA25	L28
HA26	K28
HA27	L27
HA28	K26
HA29	J28
HA30	H29
HA31	N24
HBE0#	T29
HBE1#	T24
HBE2#	R26
HBE3#	T25
HBE4#	R27
HBE5#	R28
HBE6#	R29
HBE7#	P29

SIGNAL NAME	SiS530 BALL NO
HCLK	AJ26
HD0	W29
HD1	W26
HD2	W28
HD3	W27
HD4	Y29
HD5	Y28
HD6	W25
HD7	Y27
HD8	Y26
HD9	AA29
HD10	Y25
HD11	AA28
HD12	AA27
HD13	AA26
HD14	AB29
HD15	AB28
HD16	AB26
HD17	AA25
HD18	AB27
HD19	AC26
HD20	AC28
HD21	AC27
HD22	AC29
HD23	AB25
HD24	AD29
HD25	AD27
HD26	AD28
HD27	AE29
HD28	AD26
HD29	AC25

SIGNAL NAME	SiS530 BALL NO	SIGNAL NAME	SiS530 BALL NO	SIGNAL NAME	SiS530 BALL NO
HD30	AE28	HD61	AJ23	IDB5	AG17
HD31	AE27	HD62	AE20	IDB6	AJ17
HD32	AF29	HD63	AF22	IDB7	AF16
HD33	AE26	HITM#	U25	IDB8	AD16
HD34	AF28	HLOCK#	U29	IDB9	AH17
HD35	AD25	HSYNC	D4	IDB10	AE17
HD36	AG29	ICHRDYA	AF15	IDB11	AJ18
HD37	AF27	ICHRDYB	AF19	IDB12	AG18
HD38	AH28	IDA0	AF14	IDB13	AD17
HD39	AG28	IDA1	AJ13	IDB14	AH19
HD40	AG27	IDA2	AG13	IDB15	AE18
HD41	AG26	IDA3	AF13	IDECSA0#	AH16
HD42	AE24	IDA4	AH12	IDECSA1#	AG16
HD43	AE22	IDA5	AG12	IDECSB0#	AH22
HD44	AF26	IDA6	AJ11	IDECSB1#	AG22
HD45	AE23	IDA7	AH11	IDSAA0	AJ15
HD46	AH27	IDA8	AF11	IDSAA1	AH15
HD47	AH26	IDA9	AF12	IDSAA2	AJ16
HD48	AF25	IDA10	AE12	IDSAB0	AG21
HD49	AG25	IDA11	AJ12	IDSAB1	AH21
HD50	AH25	IDA12	AD13	IDSAB2	AJ22
HD51	AE21	IDA13	AH13	IIORA	AJ14
HD52	AJ25	IDA14	AE13	IIORB	AG20
HD53	AF24	IDA15	AG14	IIOWA	AD14
HD54	AG24	IDACKA#	AG15	IIOWB	AH20
HD55	AH24	IDACKB#	AF20	IIRQA	AE14
HD56	AJ24	IDB0	AG19	IIRQB	AJ21
HD57	AF23	IDB1	AJ19	INTA#	AB4
HD58	AF21	IDB2	AF18	IRDY#	AJ5
HD59	AG23	IDB3	AH18	IREQA	AH14
HD60	AH23	IDB4	AF17	IREQB	AJ20

SIGNAL NAME	SiS530 BALL NO
IRQ14	AJ10
IRQ15	AG11
KEN#/INV	V28
KOE#	H28
M/IO#	V25
MA0	D20
MA1	E19
MA2	C20
MA3	B20
MA4	A20
MA5	D19
MA6	C19
MA7	B19
MA8	A19
MA9	E18
MA10	D18
MA11	C18
MA12	B18
MA13	F17
MA14	A18
MD0	H25
MD1	E26
MD2	G25
MD3	D27
MD4	F25
MD5	C28
MD6	B28
MD7	E25
MD8	C26
MD9	A26
MD10	D25

SIGNAL NAME	SiS53 BALL NO
MD11	B25
MD12	A25
MD13	C24
MD14	A24
MD15	D23
MD16	D14
MD17	B13
MD18	C13
MD19	A12
MD20	C12
MD21	D12
MD22	A11
MD23	C11
MD24	A10
MD25	C10
MD26	D10
MD27	B9
MD28	C9
MD29	A8
MD30	C8
MD31	D8
MD32	E28
MD33	E27
MD34	D29
MD35	D28
MD36	D26
MD37	C29
MD38	C27
MD39	B27
MD40	A27
MD41	B26

SIGNAL NAME	SiS530 BALL NO
MD42	E24
MD43	C25
MD44	E23
MD45	D24
MD46	B24
MD47	E22
MD48	E13
MD49	A13
MD50	F13
MD51	D13
MD52	B12
MD53	E12
MD54	D11
MD55	B11
MD56	E11
MD57	B10
MD58	E10
MD59	A9
MD60	D9
MD61	E9
MD62	B8
MD63	E8
NA#	U24
NC	C5
NC	D5
NC	R5
NC	C6
NC	D6
NC	R6
NC	D7
NC	E15

SIGNAL NAME	SIS530 BALL NO
NC	F15
NC	AD15
NC	AE15
NC	R24
NC	R25
OSCI	E5
OVDD2	Y16
OVDD2	Y17
OVDD2	Y19
OVDD2	N20
OVDD2	R20
OVDD2	U20
OVDD2	W20
OVDD2	Y20
OVDD3	L10
OVDD3	N10
OVDD3	R10
OVDD3	U10
OVDD3	W10
OVDD3	Y10
OVDD3	K11
OVDD3	Y11
OVDD3	K13
OVDD3	K15
OVDD3	Y15
OVDD3	K16
OVDD3	K17
OVDD3	K19
OVDD3	K20
OVDD3	L20
PAR	AE9

SIGNAL NAME	SIS530 BALL NO
PCICLK	AG2
PCIRST#	AC3
PGNT0#	AD3
PGNT1#	AD4
PGNT2#	AE1
PGNT3#	AC5
PHLDA#	AC1
PHOLD#	AA5
PL-DCLK	D1
PLOCK	AG6
PLPWDN	C2
PLSENSE	F5
PREQ0#	AD1
PREQ1#	AD2
PREQ2#	AB5
PREQ3#	AC4
ROUT	A6
RSET	B7
SCAS#	E21
SCLK	L1
SDCLK	A17
SMIACT#	V26
SRAS#	C22
STOP#	AH6
TA0	J26
TA1	G27
TA2	G26
TA3	F29
TA4	J25
TA5	F28
TA6	F27

SIGNAL NAME	SIS530 BALL NO
TA7	F26
TAGWE#	E29
TEST#	D17
TRDY#	AE8
VCS0#	P2
VCS1#	E1
VDQM0	U3
VDQM1	U5
VDQM2	U2
VDQM3	T6
VDQM4	F2
VDQM5	J5
VDQM6	F3
VDQM7	F4
VMA0	P3
VMA1	P5
VMA2	P4
VMA3	N1
VMA4	N2
VMA5	P6
VMA6	N3
VMA7	N4
VMA8	M1
VMA9	M2
VMA10	M3
VMA11	N5
VMD0	AB3
VMD1	AA4
VMD2	AB2
VMD3	AB1
VMD4	AA3

SIGNAL NAME	SiS530 BALL NO
VMD5	Y5
VMD6	AA2
VMD7	AA1
VMD8	Y4
VMD9	W5
VMD10	Y3
VMD11	Y2
VMD12	Y1
VMD13	W4
VMD14	W3
VMD15	W2
VMD16	W1
VMD17	V5
VMD18	V4
VMD19	V3
VMD20	V2
VMD21	U6
VMD22	V1
VMD23	U4
VMD24	U1
VMD25	T4
VMD26	T3
VMD27	T2
VMD28	T1
VMD29	R1
VMD30	R2
VMD31	T5
VMD32	L2
VMD33	N6
VMD34	L3
VMD35	K1

SIGNAL NAME	SiS530 BALL NO
VMD36	K2
VMD37	M5
VMD38	K3
VMD39	K4
VMD40	J1
VMD41	L4
VMD42	J2
VMD43	J3
VMD44	H1
VMD45	L5
VMD46	H2
VMD47	H3
VMD48	H4
VMD49	K5
VMD50	G1
VMD51	G2
VMD52	G3
VMD53	J4
VMD54	G4
VMD55	F1
VMD56	E2
VMD57	E3
VMD58	H5
VMD59	E4
VMD60	D2
VMD61	G5
VMD62	D3
VMD63	C1
VREF	C7
VSCAS#	R4
VSRAS#	P1

SIGNAL NAME	SiS530 BALL NO
VSS	M12
VSS	N12
VSS	P12
VSS	R12
VSS	T12
VSS	U12
VSS	V12
VSS	M13
VSS	N13
VSS	P13
VSS	R13
VSS	T13
VSS	U13
VSS	V13
VSS	M14
VSS	N14
VSS	P14
VSS	R14
VSS	T14
VSS	U14
VSS	V14
VSS	M15
VSS	N15
VSS	P15
VSS	R15
VSS	T15
VSS	U15
VSS	V15

SIGNAL NAME	SiS530 BALL NO
VSS	M16
VSS	N16
VSS	P16
VSS	R16
VSS	T16
VSS	U16
VSS	V16
VSS	M17
VSS	N17
VSS	P17
VSS	R17
VSS	T17
VSS	U17

SIGNAL NAME	SiS530 BALL NO
VSS	V17
VSS	M18
VSS	N18
VSS	P18
VSS	R18
VSS	T18
VSS	U18
VSS	V18
VSYNC	C4
VWE#	R3
W/R#	T28
WE#	C23

3.4. SiS530 MULTIPLEX PIN LIST

SiS530 BALL NO	SIGNAL NAME	SIGNAL NAME
L2	VMD32	R0
N6	VMD33	R1
L3	VMD34	R2
K1	VMD35	R3
K2	VMD36	R4
M5	VMD37	R5
K3	VMD38	R6
K4	VMD39	R7
J1	VMD40	G0
L4	VMD41	G1
J2	VMD42	G2
J3	VMD43	G3
H1	VMD44	G4
L5	VMD45	G5
H2	VMD46	G6

SiS530 BALL NO	SIGNAL NAME	SIGNAL NAME
H3	VMD47	G7
H4	VMD48	B0
K5	VMD49	B1
G1	VMD50	B2
G2	VMD51	B3
G3	VMD52	B4
J4	VMD53	B5
G4	VMD54	B6
F1	VMD55	B7
E2	VMD56	PLXLCLK
E3	VMD57	FPLDEDA
H5	VMD58	FDDCDAT
E4	VMD59	FDDCCLK
D2	VMD60	PLVSYNC
G5	VMD61	PLHSYNC

4 SIGNAL DESCRIPTION

4.1. HOST INTERFACE SIGNALS

NAME	TYPE ATTR	DESCRIPTION
HCLK	I	**Host Clock :** Primary clock input to drive the part.
ADS#	I	**Address Status :** Address Status is driven by the CPU to indicate the start of a CPU bus cycle.
M/IO#	I	**Memory I/O Command Indicator :** Memory I/O definition is an input to indicate an I/O cycle when low, or a memory cycle when high.
D/C#	I	**Data/Code Command Indicator :** Data/Code is used to indicate whether the current cycle is a data or code access.
W/R#	I	**Write/Read Command Indicator :** Write/Read from the CPU indicates whether the current cycle is a write or read access.
BRDY#	O	**Burst Ready :** Burst Ready indicates that data presented is valid during a burst cycle.
CACHE#	I	**Cacheable Indicator :** The Cache pin indicates an L1 internally cacheable read cycle or a burst write-back cycle. If this pin is driven inactive during a read cycle, the CPU will not cache the returned data, regardless of the state of the KEN# pin.
KEN#/ INV	O	**Cache Enable/Invalidate :** This function as both the KEN# signal during CPU read cycles, and the INV signal during L1 snoop cycles. During CPU cycles, KEN#/INV is normally low. KEN#/INV will be driven high during the 1st BRDY# or NA# assertion of a non-L1-cacheable CPU read. KEN#/INV is driven high (low) during the EADS# assertion of a PCI master DRAM write (read) snoop cycle.
NA#	O	**Next Address :** The SiS Chip always asserts NA# no matter the burst, or pipelined burst SRAMs are used. This signal is connected to CPU and indicates to CPU that it is ready to process a second cycle.
BOFF#	O	**Back Off :** The SiS Chip asserts BOFF# to stop the current CPU cycle.
AHOLD	O	**Address Hold :** The SiS Chip asserts AHOLD when a PCI master is performing a cycle to DRAM. AHOLD is held for the duration of PCI burst transfer. The SiS Chip negates AHOLD when the completion of PCI to DRAM read or write cycles complete and during PCI peer transfers.

HLOCK#	I	**Host Lock :** When CPU asserts HLOCK# to indicate the current bus cycle is locked.
EADS#	O	**External Address Strobe :** The EADS# is driven to indicate that a valid external address has been driven to the CPU address pins to be used for an inquire cycle.
HITM#	I	**Hit Modified :** Hit Modified indicates the snoop cycle hits a modified line in the L1 cache of the CPU.
SMIACT#	I	**System Management Interrupt Active :** The SMIACT# pin is used as the SMI acknowledgement input from the CPU to indicate that the SMI# is being acknowledged and the processor is operating in System Management Mode (SMM).
HBE[7:0]#	I	**Host Byte Enables :** CPU Byte Enables indicate which byte lanes on the CPU data bus carry valid data during the current bus cycle. HBE7# indicates that the most significant byte of the data bus is valid while HBE0# indicates that the least significant byte of the data bus is valid.
HA[31:3]	I/O	**Host Address Bus :** The Host Address is driven by the CPU during CPU bus cycles. The SiS Chip forwards it to either the DRAM or the PCI bus depending on the address range. The address bus is driven by the SiS Chip during bus master cycles or Flushing L2 cycle.
HD[63:0]	I/O	**Host Data Bus :** The Host data is driven by the CPU during CPU write cycle. The Host data is driven by L2 in three conditions. One is the CPU reads cycle and it hits the L2 cache. Another is the flushing L2 cycle. When CPU reading data from DRAM, the Host data is driven by SiS530. The other is the CPU reads cycle but the data does not exist in L2 cache, and it needs to perform a write-back cycle before a burst line fill.

4.2. L2 CACHE INTERFACE SIGNALS

NAME	TYPE ATTR	DESCRIPTION
KOE#	O	**Cache Output Enable :** Cache Output Enable for pipelined burst SRAM to enable data read.

CCS1#	O	**Cache Chip Select :** A L2 cache consisting of burst SRAMs will power up, if necessary, and perform an access if this signal is asserted when ADSC# is asserted. A L2 cache consisting of burst SRAMs will power down if this signal is negated when ADSC# is asserted. When CCS1# is negated a L2 cache consisting of burst SRAMs ignores ADS#. If CCS1# is asserts when ADS# is asserted a L2 cache consisting burst SRAMs will power up, if necessary, and perform an access.
GWE#	O	**Global-Write Enable :** GWE# asserted causes a QWORD to be written into the L2 cache. It is used for L2 cache line fills.
BWE#	O	**Byte-Write Enable :** When GWE#=1, the assertion of BWE# causes the byte lanes that are enabled via the HBE[7:0]# signals to be written into the L2 cache, if they are powered up.
ADSC#	O	**Cache Address Strobe :** Cache address strobe is for pipelined burst SRAM to load L2 cache address register from the SRAM address pins.
ADV#	O	**Cache Address Advance :** Cache address advance is for pipelined burst SRAM to advance to the next data into the cache line.
TAGWE#	O	**TAG RAM Write Enable Output :** When asserted, new state and/or new TAG address are written into the external tag RAM.
TA[7:0]	I/O	**TAG RAM Data Bus Lines :** The voltage level must be the same as DRAM voltage level.

4.3. DRAM INTERFACE SIGNALS

NAME	TYPE ATTR	DESCRIPTION
MA[14:0]	O	**Memory Address Lines 14-0:** Memory address 14-0 are the row and column addresses for DRAM.
MD[63:0]	I/O	**Memory Data Bus :** When write, it is driven by SiS530. When read, it is driven by DRAM modules.
CSA[5:0]#	O	**Chip Select (SDRAM) :** These pins activate the SDRAM and accept any command when CS# signal is low.
CSB[5:0]#	O	**Chip Select (SDRAM) :** These pins activate the SDRAM and accept any command when CS# signal is low. Two copies are provided for loading purposes.

DQM[7:0]	O	**Input / Output Data Mask (SDRAM) :** SDRAM output enables during a read cycle and a byte mask during a write cycle.
RAMW#	O	**Memory Write :** RAM Write is an active low output signal to enable local DRAM writes.
SRAS#	O	**SDRAM Row Address Strobe :** SDRAM latch row address on the positive edge of the clock with SRAS# low. This pin is driven to low by SiS530 when row access or pre-charge.
SCAS#	O	**SDRAM Column Address Strobe :** SDRAM latches column address on the positive edge of the clock with SCAS# low. This pin is driven to low by SiS530 when column access.
SDCLK	I	**SDRAM Clock :** This signal provides the source clock to SiS530 for asynchronous DRAM clock scheme.
CKE[5:0]	O	**SDRAM Clock Enable :** While in ACPI S2 or S3 state, SiS530 can put the SDRAM in the self refresh mode by CKE signal. During power down mode, CKE[5:0] signals will be floated and the CKE[5:0] must remain low by SiS5595 CKES# signal via 74LVT245.

4.4. PCI INTERFACE SIGNALS

NAME	TYPE ATTR	DESCRIPTION
PCICLK	I	**PCI Clock :** The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS Chip. It runs at the same frequency and skew of the PCI local bus.
C/BE[3:0]#	I/O	**PCI Bus Command and Byte Enables :** PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS Chip is a PCI bus master and inputs when it is a PCI slave.

AD[31:0]	I/O	**PCI Address /Data Bus :** In address phase: 1.When the SiS Chip is a PCI bus master, AD[31:0] are output signals. 2.When the SiS Chip is a PCI target, AD[31:0] are input signals. In data phase: 1.When the SiS Chip is a target of a memory read/write cycle, AD[31:0] are floating. 2.When the SiS Chip is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
PAR	I/O	**Parity :** Parity is an even parity generated across AD[31:0] and C/BE[3:0]#.
FRAME#	I/O	**Frame :** FRAME# is an output when the SiS Chip is a PCI bus master. The SiS Chip drives FRAME# to indicate the beginning and duration of an access. When the SiS Chip is a PCI slave device, FRAME# is an input signal.
IRDY#	I/O	**Initiator Ready :** IRDY# is an output when the SiS Chip is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS Chip is a PCI slave, IRDY# is an input pin.
TRDY#	I/O	**Target Ready :** TRDY# is an output when the SiS Chip is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS Chip is a PCI master, it is an input pin.
STOP#	I/O	**Stop :** STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnect, retry, and target-abort sequences on the PCI bus.

DEVSEL#	I/O	**Device Select :** As a PCI target, SiS Chip asserts DEVSEL# by doing positive or subtractive decoding. SiS Chip positively asserts DEVSEL# when the DRAM address is being accessed by a PCI master, PCI configuration registers or embedded controllers' registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M memory space are responded subtractively. The DEVESEL# is an input pin when SiS Chip is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
PLOCK#	I	**PCI Lock :** PCI Lock indicates an exclusive bus operation that may require multiple transactions to complete. When PLOCK# is sampled asserted at the beginning of a PCI cycle, the SiS Chip considers itself a locked resource and remains in the locked state until PLOCK# is sampled negated on a new PCI cycle.
PREQ[3:0]#	I	**PCI Bus Request :** PCI Bus Request is used to indicate to the PCI bus arbiter that an agent requires the use of PCI bus.
PGNT[3:0]#	O	**PCI Bus Grant :** PCI Bus Grant indicates to an agent that an access to the PCI bus has been granted.
BM_REQ#/	O	**Bus Master Request :** It can be used to carry the following two information: 1) A.G.P. activity event to reload the system standby timer in the SiS5595, and 2)A.G.P./PCI/IDE bus master request event to exit from ACPI/C3 state. Upon power up, the clock after FRAME# is sampled asserted is defined as the slot containing the Bus master request event, the next clock containing the A.G.P. activity event, ...etc.
PCIRST#	I	**PCI Bus Reset :** The PCIRST# is used to reset the device on PCI bus. PCIRST# is driven low when PWRGD is sampled low and driven inactive about 1ms after PWRGD is sampled high.
PHOLD#	I	**Bus Hold :** PHOLD# is used to request the use of the PCI bus. PHOLD# is asserted on behalf of the ISA master, DMA devices, or USB devices. PHOLD# is eventually connected to the PCI system arbiter (normally located in SiS530).
PHLDA#	O	**Bus Hold Acknowledge :** The PCI system arbiter asserts this signal to acknowledge grant of the PCI bus access to the SiS5595.

4.5. IDE INTERFACE SIGNALS

NAME	TYPE ATTR	DESCRIPTION
IDA[15:0]	I/O	**IDE Channel_0 Data Bus :**
IDB[15:0]	I/O	**IDE Channel_1 Data Bus :**
IDECS[1:0]A#	O	**IDE Channel 0 Chip Select signals :**
IDECS[1:0]B#	O	**IDE Channel 1 Chip Select signals :**
IIOR[A:B]#	O	**IDE Channel 0/1 I/O Read Cycle Command :**
IIOW[A:B]#	O	**IDE Channel 0/1 I/O Write Cycle Command :**
ICHRDYA ICHRDYB	I	**IDE Channel 0/1 I/O Channel Ready Signal :**
IDREQA# IDREQB#	I	**IDE Channel 0/1 DMA Request Signals :**
IDACKA# IDACKB#	O	**IDE Channel 0/1 DMA Acknowledge Signals :**
IIRQ[A:B]	I	**IDE Channel 0/1 Interrupt Request Signals :** These are the synchronous interrupt request inputs from IDE device.
IRQ[15:14]	O	**IDE Channel 1/0 Interrupt Request Signals :** These are the synchronous interrupt request output to the SiS5595 internal 8259 controller.
IDSA[2:0]A	O	**IDE Channel 0 Address [2:0] :**
IDSA[2:0]B	O	**IDE Channel 1 Address [2:0] :**
CBLIDA CBLIDB	I	**IDE Channel 0/1 Cable Detection :** These signals will carry the Ultra DMA 66 information to IDE controller.

4.6. VGA INTERFACE SIGNALS

NAME	TYPE ATTR	DESCRIPTION
HSYNC	I/O	**Horizontal Sync :**
VSYNC	I/O	**Vertical Sync :**
OSCI	I	**Oscillator Clock Input :** This signal is provided the 14 MHz frequency to integrated VGA controller.
DDCCLK	I/O	**Display Data Channel Clock Line :**
DDCDATA	I/O	**Display Data Channel Data Line :**
COMP	A.I	**Compensation Pin :** Bypass this pin with an external 0.1 uF capacitor to AVDD.
RSET	A.I	**Reference Resistor :** An external resistor is connected between the RSET pin and AGND to control the magnitude of the full-scale current.

VREF	A.I	**Voltage Reference :** If an external voltage is used, it must supply this input with a 1.235V reference.
ROUT	A.O	**Analog Red Video Signal Output :**
GOUT	A.O	**Analog Green Video Signal Output :**
BOUT	A.O	**Analog Blue Video Signal Output :**
VMD[0:31]	I/O	**VGA Memory Data 0~31 :**
R[7:0]/VMD[39:32]	O, I/O	**Digital Red Video Signal Output /VGA Memory Data 39~32 :**
G[7:0]/VMD[47:40]	O, I/O	**Digital Green Video Signal Output/VGA Memory Data 47~40 :**
B[7:0]/VMD[55:48]	O, I/O	**Digital Blue Video Signal Output /VGA Memory Data 55~48:**
VMD[62:63]	I/O	**VGA Memory Data 62~63 :**
VCS[1:0]#	O	**VGA Memory Chip Select 1~0 :**
VSRAS#	O	**VGA Memory Row Address Strobe :**
VSCAS#	O	**VGA Memory Column Address Strobe :**
VME#	O	**VGA Memory Write Enable :**
SCLK	O	**VGA Memory Clock :**
DSF	O	**Special Functional Input Flag :**
VDQM[7:0]	O	**VGA Memory Pin Mask/Output Enable :**
VMA[11:0]	O	**VGA Memory Address 11~0 :**
PLXLCLK/VMD56	O, I/O	**Panel Link external Latch Clock/VGA Memory Data 56 :**
FPLDEAD/VMD57	O, I/O	**Flat Panel Data Enable/VGA Memory Data 57 :** This signal qualifies the active data period. FPLDEAD signal is always required by the transmitter and must be high during active display time and low during blank time. If the digital flat panel is not used, this signal can use as VGA memory data line.
FHSYNC/VMD61	O, I/O	**Flat Panel Horizontal Sync/VGA Memory Data 61 :**
FVSYNC/VMD60	O, I/O	**Flat Panel Vertical Sync/VGA Memory Data 60 :**
FDDCCLK/VMD59	I/O, I/O	**Panel Data Channel Clock Line/VGA Memory Data 59 :**
FDDCDATA/VMD58	I/O, I/O	**Panel Data Channel Data Line/VGA Memory Data 58 :**
PLSENSE	I	**Panel Sense :** This signal will sense the P&P Monitor is present or not.
PLPWDN	O	**Power Down :** A high level indicates normal operation and a low level indicates power down mode.
INTA#	O	**Panel Link Interrupt :**
PL-DCLK	O	**Panel Link Data Clock :**
ENVCO	I/O	**Enable MCLK Clock Generator :** A high level indicates enable the internal clock generator and a low level indicates disable the internal clock generator.

NOTE: A. I: Analog Input; A. O: Analog Output

4.7. POWER SIGNALS

NAME	TYPE ATTR	DESCRIPTION
DVDD	PWR	**+3.3V DC Power Source :**
OVDD3	PWR	**+3.3V DC Power Source :**
OVDD2	PWR	**+3.3V/2.5V DC Power Source:**
VSS	PWR	**Ground signals :**
AVDD4	PWR	**Analog Power Source for integrated VGA :**
AVSS4	PWR	**Analog Ground Source for integrated VGA :**
AVDD2/3	PWR	**Analog Power Source for integrated VGA :**
AVSS2/3	PWR	**Analog Ground Source for integrated VGA :**
AVDD1	PWR	**Analog Power Source for integrated VGA :**
AVSS1	PWR	**Analog Ground Source for integrated VGA :**
AVDD	PWR	**Analog Power Source :**
AVSS	PWR	**Analog Ground Source :**
5VDD	PWR	**5V DC Power Source :**

4.8. MISC. SIGNALS

NAME	TYPE ATTR	DESCRIPTION
NC		**Not Connect :**
TEST#	I	**Test Mode Select for NAND Tree function :** The high level indicates that this function will be disabled. The low level indicates that this function will be enabled and all of NAND tree pins will enter into the Tri-State.

5. FUNCTIONAL DESCRIPTION

5.1. HOST INTERFACE

SiS530 is designed to support Socket7 CPU and integrated 3D VGA controller.

SiS530 supports the pipelined addressing mode of the CPU by issuing the next address signal, NA#. NA# is asserted except single read DRAM cycles & burst write cycles.

SiS530 supports the CPU L1 write-back (WB) or write-through (WT) cache policies and the L2 WB cache policies. The L1 cache is snooped by the assertion of EADS# when the CPU is put in the HOLD state.

SiS530 issues AHOLD to the CPU in response to the assertion of PCI master requests. Once the AHOLD is asserted, SiS530 does not immediately assert PGNT[3:0]# until both the CPU to PCI posted write buffer and the memory write buffer are empty.

5.1.1. HOST INTERFACE DECODING RULES

The destination of CPU initiated cycle is decoded by the host interface. Memory cycles may be forwarded to DRAM controller, VGA DRAM controller or PCI bus. I/O cycles are either forwarded to host VGA bus or PCI bus.

5.1.1.1. MEMORY CYCLE

SiS530 determines whether a memory cycle' s destination is system DRAM or not by checking DRAM bank/status registers, shadowing related registers, Graphics Window base address registers, Graphics Window size registers. For memory cycles which are not targeting system DRAM, the host interface further checks memory space enable register, memory base address register and memory limit address register, prefetchable memory base address register and prefetchable memory limit address register in the virtual PCI-to-PCI bridge to see if the destination is residing in host VGA bus or not. If the address locates within these ranges, the host interface signals host VGA Interface to forward the cycle to host VGA. Otherwise, the cycle would be forwarded to PCI bus by PCI Interface.

The only exception for the above rule is mapping standard video frame buffer area (A0000h~BFFFFh). The mapping of this range is totally controlled by VGA enable bit of the PCI-to-PCI bridge control register residing in the virtual bridge (device 2).

5.1.1.2. I/O CYCLE

I/O cycles are either forwarded to host VGA or PCI bus. Basically, SiS530 determines whether an I/O cycle is destining host VGA bus or not by checking I/O base address register and I/O limit address register in the virtual PCI-to-PCI bridge. If the address locates within the range, the host interface signals host VGA Interface to forward the cycle to VGA controller. Otherwise, the cycle would be forwarded to PCI bus by PCI Interface.

The I/O address decoding is also affected by the bridge control register and bridge command register of the virtual PCI-to-PCI bridge (device 2). When VGA enable bit of the bridge control register is set to 1, all I/O accesses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh are forwarded to host VGA bus. When the bit is set to 0, I/O accesses with the address ranges are forwarded to PCI bus.

I/O address decoding for the addresses of A[9:0] = 3C6h, 3C8h and 3C9h is also affected by the VGA palette snoop enable bit of the bridge command register and the palette write cycle forwarding control register. When the palette write cycle forwarding control register is set to 1, I/O writes with these addresses are forwarding to one interface only (either host VGA or PCI Interface), and it is totally controlled by VGA enable bit. When the value of palette write cycle forwarding control register is 0, these I/O write cycles are always forwarding to PCI Interface and may optionally be forwarded to host VGA Interface, which is controlled by VGA palette snoop enable and VGA enable.

Host interface must take care of returning BRDY# for palette write when the cycle is forwarded both to PCI and Host VGA bus. Host interface must wait until both PCI and Host VGA device have finished the operation before returning BRDY# to CPU.

ISA enable bit of the bridge control register also affects I/O address decoding. When the ISA enable bit is 1, CPU initiated I/O cycles addressing the last 768 bytes in each 1Kbyte block will be forwarded to the PCI bus even the address is within the address range defined by the virtual bridge' s I/O base and I/O limit registers.

I/O addresses CF9h (reset control register) and CF8h (configuration address register, only accepts double word access) are always forwarded to PCI bus. The decoding of I/O addresses in the range CFCh~CFFh (configuration data register) depends on the bus number defined configuration address register. If the bus number is equal to or greater than the secondary bus number register and is smaller or equal to the subordinate bus number register in the virtual PCI-to-PCI bridge, the cycle will be forwarded to host VGA bus. Otherwise, the cycle will be forwarded to PCI bus.

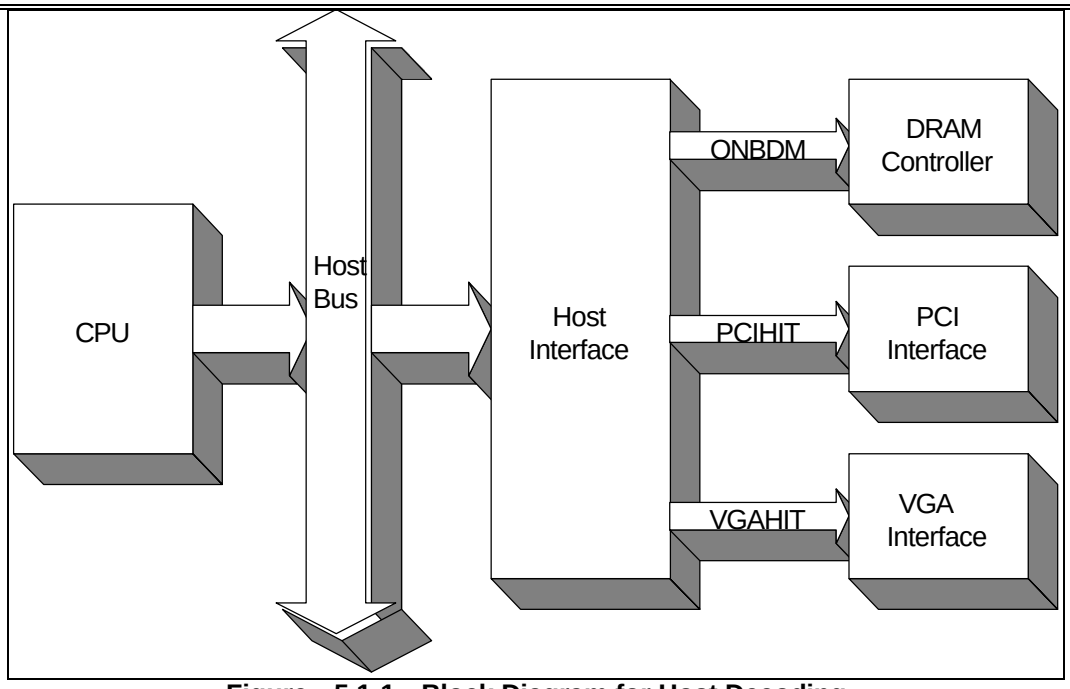


Figure 5.1-1 Block Diagram for Host Decoding

5.1.1.3. OTHER CYCLES

Interrupt acknowledge cycles are always forwarded to PCI bus (PCI Interface intercepts the first cycle and forward the second cycle to PCI bus). The Write Back special cycle is handled by the host interface itself when the write back enable bit is set to 1 and L2 flushing mechanism control is set to 0. Otherwise, the Write Back special cycle will be passed to PCI Interface (PCI Interface does nothing except for return BRDY# to CPU).

5.1.1.4. HOST BUS ARBITRATION

SiS530 may require the usage of host bus for some reasons. After L2 flushing command is accepted, host bus must be owned by SiS530 to flush modified lines in L2 cache into system DRAM. When a PCI master is accessing system memory, host bus must also be owned by SiS530 to snoop about CPU and to access L2 cache. Host bus arbitration must be done among CPU, PCI Interface and host VGA Interface. When SiS530 determined that itself needed the host bus, it asserts AHOLD or BOFF# to seize the host bus from the Pentium processor. If SiS530 requires only the host address bus, it asserts AHOLD. If SiS530 wants to seize the host data bus, it also asserts BOFF# in addition to the assertion of AHOLD.

PCI Interface and host VGA Interface asserts HOLD to Host Bus Arbiter in the Host Interface. After HLDA is returned, the respective block has totally control the host bus. It can snoop about the CPU cache and access L2 cache/DRAM. After HLDA is returned to PCI Interface or host VGA Interface. PCI Interface or host VGA Interface can own the host bus as long as it keeps HOLD asserted. Arbiter in PCI Interface or host VGA Interface will determine how long the HOLD should be lasted.

5.2. CACHE CONTROLLER

The built-in L2 Cache Controller uses a direct-mapped scheme, which can be configured as either in the write through or write back mode. Notice that the L2 Write-through mode is only supported during the cache sizing period. SiS530 supports 256K/512K/1M/2M Bytes pipelined burst SRAM and the function of auto-sizing cache size.

SiS530 supports 8bits TAG address lines. There are 7 bits of TAG RAM are used for TAG address and another one bit is used as dirty bit, when the write back mode is performed.

Table 5.2-1 Supported Size of L2 Cache shows the cache sizes that are supported by the SiS530, with the corresponding TAG RAM sizes, and cacheable memory sizes of TAG-7bits.

Table 5.2-2 SRAM TAG Address Mapping Table shows the TAG address mapping.

Table 5.2-1 Supported Size of L2 Cache

CACHE SIZE	TAG RAM	CACHEABLE SIZE
256K	8Kx8	32M
512K	16Kx8	64M
1M	32Kx8	128M
2M	64Kx8	256M

Note: To improve the performance, the TAG RAM must be adopted 3.3V component

Table 5.2-2 SRAM TAG Address Mapping Table

TAG-7BITS	256K	512K	1M	2M
TA7	Dirty bit	dirty bit	dirty bit	dirty bit
TA6	24	24	24	24
TA5	23	23	23	23
TA4	22	22	22	22
TA3	21	21	21	21
TA2	20	20	20	27
TA1	19	19	26	26
TA0	18	25	25	25

There are two mechanisms to trigger the flushing L2 operation, which are decided by L2 flushing mechanism control register. When triggered by write back special cycle, SiS530 only supports flushing all function. When triggered by configuration write register A0h, SiS530 also supports the flushing 4K function.

During the flushing operation, SiS530 will assert AHOLD to hold the CPU and drive the address to host address bus. If this cache line is dirty, SiS530 will read the data from L2 cache and write into system DRAM. In the same time, SiS530 cleans the dirty bit and sets this cache line to be invalid. If this cache line is not dirty, SiS530 will do nothing except setting this cache line to be invalid. After, these operation, it starts next address' s scanning.

5.3. DRAM CONTROLLER

The SiS530 can support up to 1.5 GBytes of DRAM and each bank could be single or double sided 64-bit Synchronous DRAM (SDRAM). The SiS530 supports industry standard DIMM modules. Six CS# lines permit up to six rows (3 double sided banks) of DRAM, and 512 MBytes maximum memory size per bank is acceptable.

The installed SDRAM type can be 1M, 2M, 4M, 8M, 16M, 32M byte deep by n (n = 4, 8, 16,or 32) bit wide. The SiS530 DRAM Controller operates synchronous/asynchronous clock to the CPU clock that performing best performance and DRAM compatible issue.

5.3.1. DRAM CONFIGURATION

SiS530 supports three banks (double sided DRAM) of DRAM each 64-bit wide. The three banks may be configured in three banks of SDRAM DIMM. Access to the banks are not interleaved and need not to be populated starting from row 0 or in consecutive sequence.

In the share frame buffer mode of the integrated 3D VGA controller, the display memory must be populated on Bank0 (using CS0# signal).

The basic configurations are shown as the following:

5.3.2. SDRAM CONFIGURATION (2 DIMM/3 DIMM):

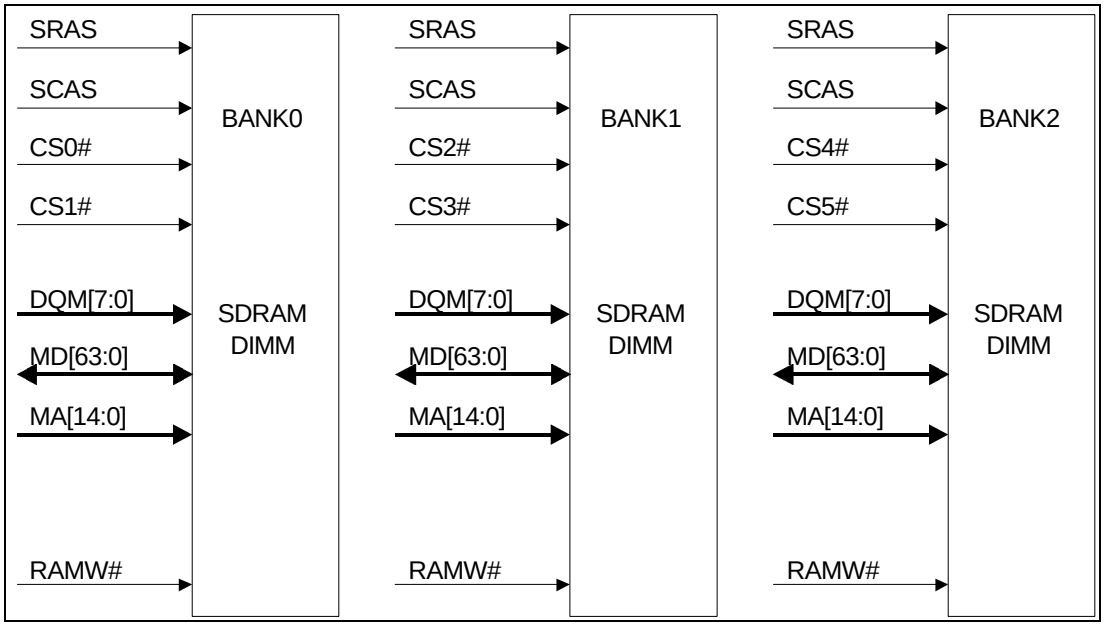


Figure 5.3-1 SDRAM Configuration

Note: In shared memory frame buffer mode, the integrated 3D VGA controller access the display memory by the Bank 0.

5.3.3. DRAM SCRAMBLE TABLE

The DRAM scramble table contains information for memory address mapping. These tables provide the translation between CPU host address (HA) and memory Row and Column address (MA).

There are several memory address mappings: MA mapping for 2Bank and 4Bank mapping for SDRAM that SiS530 supports:

MA mapping table for SDRAM

Table 5.3-1 MA mapping table for 2 Banks Device SDRAM Type (1)

Type	1M (1x11x8)		2M (1x11x9)		4M (1x11x10)	
Address	Row	Column	Row	Column	Row	Column
MA0	15	3	15	3	15	3
MA1	16	4	16	4	16	4
MA2	17	5	17	5	17	5
MA3	18	6	18	6	18	6
MA4	19	7	19	7	19	7
MA5	20	8	20	8	20	8
MA6	21	9	21	9	21	9
MA7	22	10	22	10	22	10
MA8	12	NA	23	11	23	11
MA9	13	NA	13	NA	24	12
MA10	14	NA	14	NA	14	NA
MA11	11	11	12	12	13	13
MA12	NA	NA	NA	NA	NA	NA
MA13	NA	NA	NA	NA	NA	NA
MA14	NA	NA	NA	NA	NA	NA

Table 5.3-2 MA mapping table for 2 Banks Device SDRAM Type (2)

Type	4M (1x13x8)		8M (1x13x9)		16M (1x13x10)	
Address	Row	Column	Row	Column	Row	Column
MA0	15	3	15	3	15	3
MA1	16	4	16	4	16	4
MA2	17	5	17	5	17	5
MA3	18	6	18	6	18	6
MA4	19	7	19	7	19	7
MA5	20	8	20	8	20	8
MA6	21	9	21	9	21	9
MA7	22	10	22	10	22	10
MA8	12	NA	23	11	23	11
MA9	13	NA	13	NA	24	12
MA10	14	NA	14	NA	14	NA
MA11	11	11	12	12	13	13
MA12	NA	NA	NA	NA	NA	NA
MA13	23	NA	24	NA	25	NA
MA14	24	NA	25	NA	26	NA

Table 5.3-3 MA mapping table for 4 Banks Device SDRAM Type (1)

Type	2M (2x11x8))		4M (2x12x8)		8M (2x12x9)		16M (2x12x10)	
Address	Row	Column	Row	Column	Row	Column	Row	Column
MA0	15	3	15	3	15	3	15	3
MA1	16	4	16	4	16	4	16	4
MA2	17	5	17	5	17	5	17	5
MA3	18	6	18	6	18	6	18	6
MA4	19	7	19	7	19	7	19	7
MA5	20	8	20	8	20	8	20	8
MA6	21	9	21	9	21	9	21	9
MA7	22	10	22	10	22	10	22	10
MA8	23	NA	23	NA	23	11	23	11
MA9	13	NA	13	NA	24	NA	24	12
MA10	14	NA	14	NA	14	NA	25	NA
MA11	11	11	11	11	12	12	13	13
MA12	12	12	12	12	13	13	14	14
MA13	NA	NA	24	NA	25	NA	26	NA
MA14	NA	NA	NA	NA	NA	NA	NA	NA

Table 5.3-4 MA mapping table for 4 Banks Device SDRAM Type (2)

Type	8M (2x13x8)		16M (2x13x9)		32M (2x13x10)	
Address	Row	Column	Row	Column	Row	Column
MA0	15	3	15	3	15	3
MA1	16	4	16	4	16	4
MA2	17	5	17	5	17	5
MA3	18	6	18	6	18	6
MA4	19	7	19	7	19	7
MA5	20	8	20	8	20	8
MA6	21	9	21	9	21	9
MA7	22	10	22	10	22	10
MA8	23	NA	23	11	23	11
MA9	13	NA	24	NA	24	12
MA10	14	NA	14	NA	25	NA
MA11	11	11	12	12	13	13
MA12	12	12	13	13	14	14
MA13	24	NA	25	NA	26	NA
MA14	25	NA	26	NA	27	NA

5.3.4. CPU TO DRAM POSTED WRITE FIFO

There is a built-in CPU to Memory posted write buffer with 8 QWord deep (CTMFF). All write accesses from CPU to DRAM will be buffered. For the CPU read miss / Line fill cycles, the write-back data from the second level cache will be buffered first, and right after the data had been written into the FIFO, CPU can perform the read operation by the memory controller starting to read data from DRAM. The buffered data then is written to DRAM. With this concurrent write back policy, many wait states are eliminated. If there comes a bunch of continuous DRAM write cycles, some ones will be pending if the CTMFF is full.

5.3.5. ARBITER

The arbiter is the interface between the DRAM interface and the masters that can access DRAM. In addition to pass or translate the information from outside to DRAM controller, arbiter is also responsible for which master has higher priority to access DRAM. The arbiter treats different DRAM access request as DRAM master, and that makes 9 masters which are trying to access DRAM by sending their requests to the arbiter. After one of them gets the grant from the arbiter, it owns DRAM bus and begins to do memory data transaction.

The masters are: Refresh High request, CPU read request, PCI masters, Posted write FIFO write request, AGP high read request, AGP high write request, AGP low read request, AGP low write request and Refresh Low request. The order of these masters shown above also stands for their priority to access memory.

5.3.6. REFRESH CYCLE

Refresh functionality is provided. There are up to twelve deep refresh queues 56h B[5:4] with two levels of refresh priority. SiS530 generates a new refresh request every 15.6 us which is programmable by register 56h B[3:2], and the request will be served only when there is no other DRAM operation in progress or pending. If the request does not get service, it will be pushed into the refresh queue. When the queue is full, a high priority refresh request asserts and takes priority over all other DRAM requests.

5.4. PCI BRIDGE

The PCI bridge of SiS530 consists of three parts: PCI arbiter, PCI master bridge and PCI target bridge. The PCI arbiter controls the assignment of PCI bus ownership among all PCI masters. The PCI master bridge forwards the transactions from host bus. The PCI target bridge claims PCI cycles toward system memory as required by PCI master devices. SiS530 is operated at asynchronous PCI clock with CPU clock.

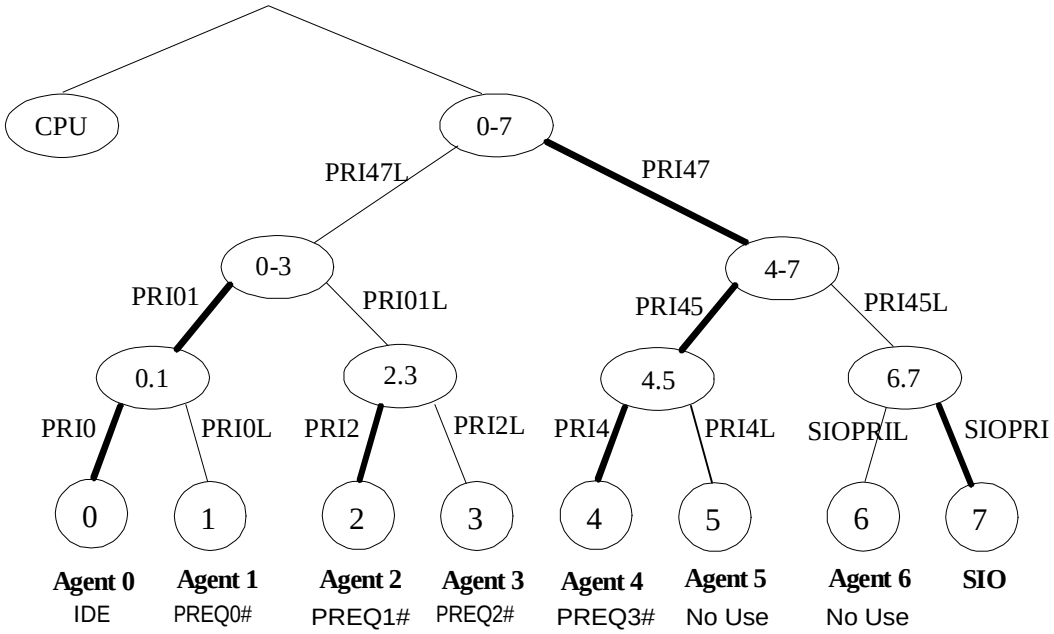
5.4.1. PCI ARBITER

The main function of PCI arbiter takes charge of the PCI bus ownership assignment. This PCI arbiter supports at most 4 external PCI masters using standard PCI PREQ#/PGNT# mechanism, 1 IDE DMA using internal request/grant mechanism and 1 PCI master using PHOLD#/PHLDA# mechanism. The master that uses PHOLD#/PHLDA mechanism is not pre-emptive. That means the master can own the bus as long as it wishes after it gains the control of PCI bus. The master that use PHOLD#/PHLDA# mechanism to access PCI bus is typically SiS5595 chip.

Arbitration Algorithm

PCI Masters (Agent 0~6, SIO) Requests

Figure 5.4-1 Arbitration Tree shows the arbitration tree in arbiter design. Whenever a PCI cycle occurs, priority status will be changed. The initial priority for master 0-7 to own PCI bus is 4 -> 0 -> SIO -> 2 -> 5 -> 1 -> 6 -> 3 -> 4...



NOTE: 1. "SIO" means the System I/O for PCI to ISA bridge (SiS5595).
2. The arbiter will treat PHOLD# as Agent SIO.
3. SiS recommended used the PREQ0~2# for PCI slot if the board is only designed 3 PCI slots.

Figure 5.4-1 Arbitration Tree

CPU Request

To avoid CPU being constantly held for a long time while PCI masters continuously deliver requests to the arbiter, SiS530 implemented a timer-based algorithm to reserve PCI bandwidth for CPU. Three timers, PCI Grant Timer (PGT)/ Master Latency Timer (MLT)/ CPU Idle Timer (CIT), are included in the host bridge for this purpose.

Whenever any PCI device owns the PCI bus other than host bridge, PCI grant timer (PGT) starts to count. After the timer is expired, the host bridge asserts its request signal to ask for gaining the control of PCI bus. Since the host bridge has the highest priority, PCI arbiter grants the bus to the host bridge as soon as possible after it receives the request from the host bridge.

Once the host bridge gets a chance to start a transaction on PCI bus, its master latency timer (MLT) begins to count. After MLT is expired, the host bridge deasserts its request signal to inform the arbiter that the host bridge no more needs the PCI bus. If there is any other PCI device that requests for the bus, arbiter grants the bus to the device and CPU is held again.

If there is no request from any PCI devices, the arbiter parks the bus on the host bridge. The ratio MLT/PGT approximately guarantees the minimum PCI bandwidth allocated to host bridge when CPU and PCI masters are contending for system resources, but it does not constrain CPU's highest utilization of PCI bus because of our bus parking policy.

To prevent the host bridge from capturing PCI bus too long while CPU actually has nothing to do at all, the third timer, CPU Idle Timer (CIT) is included in our design. CIT starts to count when the host bridge get a chance to start a transaction on PCI bus, but is reloaded with its initial value whenever the host bus leaves idle state. CIT actually keeps track on how long the CPU is in idle state. After CIT is expired, the host bridge deasserts its request signal just in the same manner as the case of MLT's expiration.

PGT is a 16-bit timer. MLT and CIT are both 8-bit timers. All of the initial values of the three timers are programmable and can be tuned according to the nature of the application. Although CIT & MLT are both 8-bit timers, the initial value of CIT is typically programmed much smaller than MLT.

Arbitration Parking

When no agent is currently using or requesting the bus, the arbiter will grant the bus ownership to the arbitration controller of SiS530.

PCI Peer-to-peer Access Concurrent with CPU to L2/DRAM Access

Although the PCI arbiter holds CPU in response to master requests, the PCI arbiter will release the CPU hold as soon as possible after it detects the cycle initiated by the master is not targeting system memory.

With this feature, a transaction initiated by a PCI master targeting a PCI target would not hold CPU. The CPU can still access L2 cache, system memory and PCI post-write buffers when PCI peer-to-peer activities are undergoing. With the enlarged 8 Dword deep PCI post-write buffers, it takes longer for CPU to halt while PCI peer-to-peer accesses are taking place.

5.4.2. PCI MASTER BRIDGE

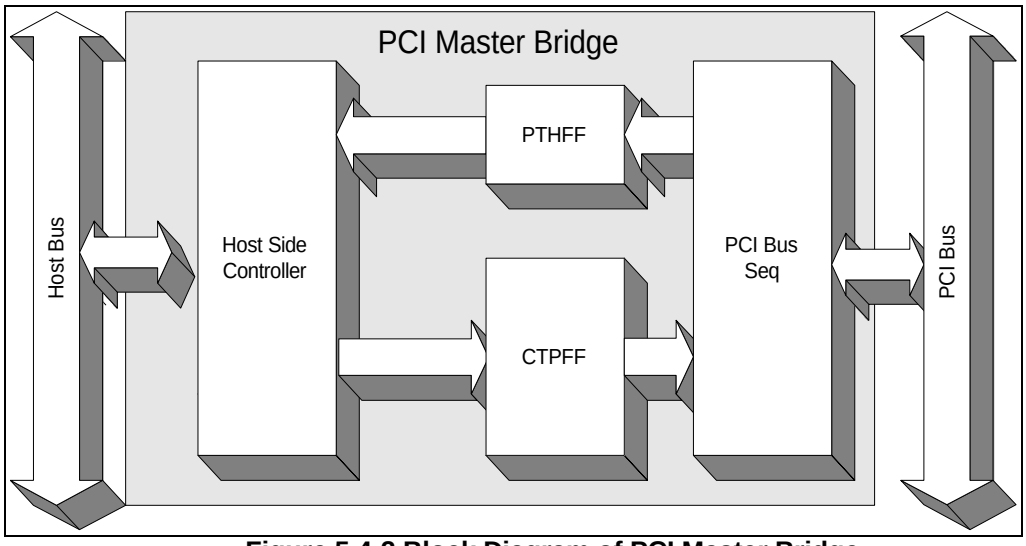


Figure 5.4-2 Block Diagram of PCI Master Bridge

The PCI master bridge forwards CPU cycles to the 33Mhz PCI bus. In the case of a 64-bit CPU request, the bridge takes the duty of read assembly and write disassembly control, A post-write buffer is implemented to improve the performance of CPU to PCI memory write and CPU to IDE data post write. Any non-posted write cycles forwarded to the PCI bus will be suspended until the post-write buffer is empty. For memory write cycles toward PCI or I/O write cycles towards IDE data port, the address and data from host bus are pushed into the post write buffer if it is not full. The push rate for a double word is 3 CPU clocks. The pushed data are, at later time, written to the PCI bus. If the addresses of consecutive written data are in double word incremental sequence and they are targeting memory space, they will be transferred to the PCI bus in a burst manner.

The bridge provides a mechanism for converting standard I/O cycles on the CPU bus to configuration cycles on the PCI bus. Configuration Mechanism#1 in PCI Specification is used to do the cycle conversion.

The bridge is response for updating SiS530 internal configuration register. Care has to be done when updating GART base address register and Graphics Window size register since these two registers affect the mapping of system memory. The bridge will postpone the update of these two registers until all previously issued system memory write accesses are all retired from the DRAM post-write buffer.

The bridge always intercepts the first interrupt acknowledge cycle from CPU bus, and forwards the second interrupted acknowledge cycle onto the PCI bus.

PCI master bridge asserts BOFF# to CPU when its read cycle is retried by any PCI target. However, PCI master bridge would not assert BOFF# for retried memory write

cycles or I/O write cycles. PCI master bridge will re-initiate the retried cycles again and again until they are successfully transferred on PCI bus. The main reason for not asserting BOFF# to CPU for retried I/O write cycles is to secure correct palette snoop operation on host VGA bus. If PCI master bridge asserts BOFF# to CPU for a retried palette write cycle, the cycle will be forwarded both to PCI bus and host VGA bus, and this will result in incorrect palette updating behavior on host VGA bus. The PCI arbiter parks the PCI bus to PCI master bridge when there are no requests from master. Typically, the bridge issues PCI cycles through bus parking mechanism. However PCI master bridge may also issue bus request to PCI arbiter when the CPU is held too long or when the PCI bus is occupied by PCI masters for a period of time. Three counters: PGT, MLT and CIT are included in PCI master bridge for managing bridge' s bus request. Please reference PCI arbiter section for more information about the arbitration mechanism.

Since the system reset circuitry is moved to South Bridge (SiS5595) other than North Bridge (SiS530) itself. To have the correct response on CPU initiated special cycles, the PCI master bridge is responsible for transferring these cycles to South Bridge (SiS5595) by way of PCI bus. For all special cycles, the PCI master bridge translates them into PCI Special Cycles with embedded information on AD bus following the encoding rule in Table 5.4-1 Special Bus Cycle Encoding Rule.

Table 5.4-1 Special Bus Cycle Encoding Rule

SPECIAL BUS CYCLE	AD[31:0]
Shutdown	00000000h
Flush (INVD, WBINVD instr.)	00000001h
Halt	00000002h
Write Back (WBINVD instr.)	00000003h
Flush Acknowledge (FLUSH# assertion)	00000004h
Branch Trace Message	00000005h
Stop Grant	00000012h

5.4.3.PCI TARGET BRIDGE

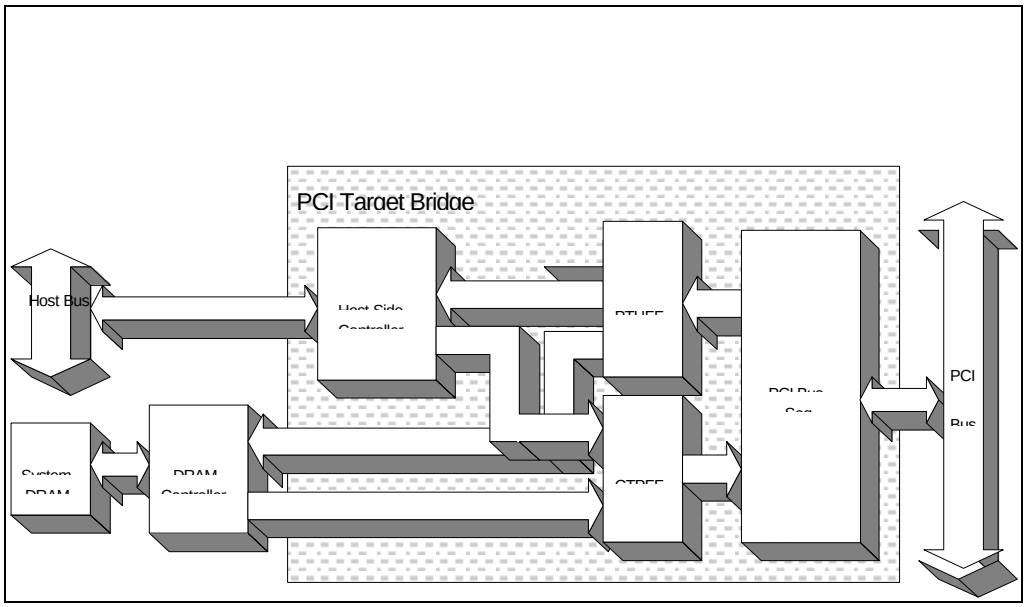


Figure 5.4-3 Block Diagram of PCI Target Bridge

While in the PCI Master write cycles, post-write is always performed. And function of Write Merge with CPU-to-DRAM post-write buffer is incorporated to eliminate the penalty of snooping write-back. On the other hand, prefetch is enabled for master read cycles by default, and such function could be disabled optionally. And, Direct-Read from CPU-to-DRAM post-write buffer is implemented to eliminate the overhead of snooping write-back also.

The post-write and prefetch buffers are both 8QW deep FIFO.

5.4.3.1. TARGET INITIATED TERMINATION

In general, SiS530 is capable to complete all the requests to access main memory from PCI masters until master terminates the transaction actively. Sometimes, as SiS530 is unable to respond or is unable to burst, it will initiate to terminate bus transactions and STOP# will be issued by doing Retry or Disconnect.

5.4.3.2. TARGET RETRY

SiS530 may operate Target Retry for one of two reasons:

1. Whenever a PCI master tries to access main memory and SiS530 is locked previously by another agent, Target Retry will be signaled.
2. Once SiS530 can not meet the requirement of target initial latency, Target Retry is used and no data is transferred.

5.4.3.3. DISCONNECT WITH DATA

In some situations, such as the burst crosses a resource boundary or a resource conflict, SiS530 might be temporarily unable to continue bursting, and, therefore, SiS530 concludes an active termination.

SiS530 supports PCI burst transfers, the bursting length can be 256 bytes, 512 bytes, 1K bytes, 2K bytes, or 4K bytes. A burst will be terminated by doing Disconnect if the transfer goes across the programmed bursting length. In this way, at most 128 cache lines of data can be uninterruptedly transferred no matter what the status they are in L1 and L2. One reason for the constraint is that page miss may occur only once at the beginning of the entire bursting transaction since the maximum bursting length is always within the page size in any of the used DRAM.

5.4.3.4. DISCONNECT WITHOUT DATA

If Target Subsequent Latency timer expires, it causes SiS530 to assert STOP# by doing Disconnect operation.

5.4.3.5. DATA FLOW

The major two data paths are PCI->PTHFF->DRAM and DRAM->CTPFF->PCI for PCI master write DRAM cycles and read DRAM cycles, respectively. For cache system, if an inquiry cycle hits Pipeline Burst SRAM, SiS530 would read from L2 directly, but write DRAM and L2 simultaneously.

Based on snooping result, there is additional data path that SiS530 should perform.

Table 5.4-2 Data Flow Based on Snooping Result

PCI Master Read Memory Cycle			
Result of Snoop			
Status of L1	Status of L2	Data Flow	Operation
	Miss or None	DRAM -> CTPFF -> PCI	Read DRAM
Miss or Unmodified	Hit and Not Dirty	DRAM -> CTPFF -> PCI	Read DRAM
	Hit and Dirty	L2 -> CTPFF -> PCI	Read L2
	Miss or None	L1 -> CTMFF & CTPFF	Direct Read
		CTPFF -> PCI	
Hit Modified	Hit, Dirty or Not	L1 -> L2 & CTPFF	Direct Read
		CTPFF -> PCI	

PCI Master Write Memory Cycle			
Result of Snoop			
Status of L1	Status of L2	Data Flow	PSL Operation
	Miss or None	PCI -> PTHFF -> DRAM	Write DRAM
Miss or Unmodified	Hit, Dirty or Not	PCI -> PTHFF -> L2&DRAM	Write DRAM&L2

	Miss or None	L1 -> CTMFF	
		PTHFF & CTMFF -> DRAM	Write Merge
Hit Modified	Hit, Dirty or Not	L1 -> L2	
		PCI -> PTHFF -> L2&DRAM	Write DRAM&L2

Note: CTPFF means CPU-to-PCI Posted Write Buffer
CTMFF means CPU-to-Memory Posted Write Buffer
PTMFF means PCI-to-Memory Posted Write Buffer

5.4.3.6. PCI MASTER READ/WRITE DRAM CYCLE

If inquiry cycle hits neither L1 nor L2, SiS530 could perform prefetching/retiring operation and inquiry cycles simultaneously.

5.4.3.7. PCI MASTER WRITE L2 AND DRAM CYCLES

For the purpose of writing L2, PCI Target Bridge must drive the HBE[7:0]# and HD[63:0] bus. Then, BOFF# is asserted to force CPU floats the host bus. And to retain the correct address on HA, the improved snoop function is temporally suspended.

5.5. POWER MANAGEMENT SUPPORT

To support power management feature of SiS5595, SiS530 reports all PCI masters' activities and optionally reports activities on internal A.G.P. bus to SiS5595 via the pin BMREQ#. The information contained by BMREQ# can be classified into two categories. The first category is CPU operation and the second category is PCI master operation. Each category occupies different time slot. If BMREQ# is reporting CPU operation in clock T1, then BMREQ# will report master operation in clock T2 and vice versa. Configuration Register 69h of host bridge is used to define what kinds of operations should be reported.
SiS530 may also trap ACPI I/O port accesses to support ACPI S3 and S2 states and to disable system arbiter. Configuration register 6Ah is used to define the ACPI I/O space base address and SiS530 uses this register to trap the ACPI I/O port accesses.

5.6. IDE CONTROLLER

SiS530 supports a full function PCI IDE controller capable of PIO, DMA and Ultra DMA 33/66 mode operation. It can be supported by programming the internal registers to support PIO Mode 0 ~ 4, Single/Multi-Word DMA Mode 0 ~ 2 and Ultra DMA Mode 0 ~ 4 timing.

The IDE Controller block diagram is shown as below:

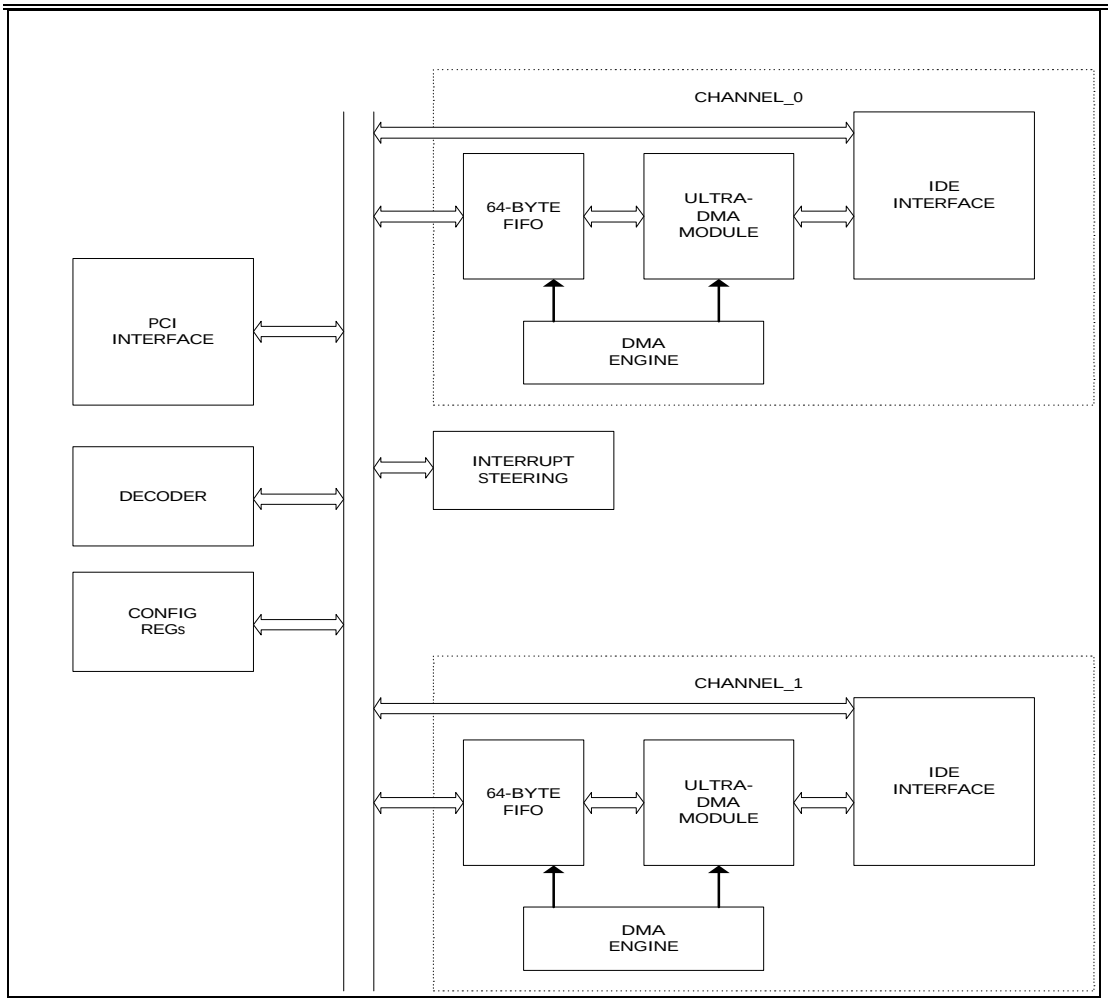


Figure 5.6-1 Block Diagram for IDE Controller

There are two 64-byte FIFO associated with two IDE channels. The data can be popped into FIFO by the unit of word or double-word. All accesses to the IDE data port will go through FIFO, no matter prefetch/post write is enabled or not. Accesses to the command or control port will bypass FIFO. This mechanism allows the host to access command or control ports when FIFO is not empty. The FIFO has an option to be 32-byte in depth(from Register 52h bit 0 in PCI IDE configuration space), which is for backward compatibility only and is suggested not to be used. SiS Chip provides the 64-byte FIFO mainly to support Ultra-DMA. Because the Ultra-DMA can be operated at twice the speed of traditional DMA in mode 0-2, a small FIFO may easily become bottleneck and degrade system performance.

The host may need to access command or control ports when PIO mode or DMA mode data transfer is undergoing. The IDE controller provides a mechanism to complete the command/control port access without disrupting the operation of FIFO.

In PIO mode, when doing post write, the command/control port access is held-off until the FIFO is flushed to IDE. When doing prefetch, the command/control access is held-

off until the FIFO is full. Before the command/control port access is actually carried out, the host will keep waiting on PCI bus.

In DMA mode, the command/control access will go through a higher priority than the DMA data transfer cycles. When the command/control access cycle is first seen on the PCI bus, the controller will retry the cycle so that PCI bus will not be used by the host while it is only waiting. At the same time, the controller will suspend the DMA data transfer cycles by completing the current cycle successfully, then de-asserts IDACK# to inform IDE device to stop the DMA data transfer. The IDE device may or may not de-assert its IDREQ at this moment. On the other hand, the host should keep retrying the command/control cycle on PCI bus. Eventually the cycle will be accepted and carried out when DMA data transfer is stopped. After the command/control cycle is completed, the controller resumes DMA data transfer cycles as soon as the IDE device asserts IDREQ.

Both primary and secondary channels may be programmed as Native mode or Compatibility mode via the Class Code Field in the controller's Configuration Space register.

In Compatibility mode, the interrupt requests for channel 0 and channel 1 are re-routed to IRQ 14 and IRQ 15 of the built-in Interrupt Controller.

Following table illustrates the accessing methods to the I/O ports in compatibility mode:

Primary Channel:

Table 5.6-1 Accessing Method to I/O Ports for Primary Channel

			READ		WRITE	
PORT	***ICSA1#***	***ICSA0#***	***IIORA#***	***IIORB#***	***IIOWA#***	***IIOWB#***
1F0	1	0	0	1	0	1
1F1	1	0	0	1	0	1
1F2	1	0	0	1	0	1
1F3	1	0	0	1	0	1
1F4	1	0	0	1	0	1
1F5	1	0	0	1	0	1
1F6	1	0	0	1	0	1
1F7	1	0	0	1	0	1
3F6	0	1	0	1	0	1

Secondary Channel:

Table 5.6-2 Accessing Method to I/O Ports for Secondary Channel

			READ		WRITE	
PORT	***ICSB1#***	***ICSB0#***	***IIORA#***	***IIORB#***	***IIOWA#***	***IIOWB#***
170	1	0	1	0	1	0
171	1	0	1	0	1	0
172	1	0	1	0	1	0
173	1	0	1	0	1	0
174	1	0	1	0	1	0

175	1	0	1	0	1	0
176	1	0	1	0	1	0
177	1	0	1	0	1	0
376	0	1	1	0	1	0

In Native mode, the interrupt requests of both channels (channel 0 and channel 1) share the same PCI interrupt pin. The interrupt pin may be re-routed to any one of eleven ISA compatible interrupts (IRQ[15:14], IRQ[12:9], and IRQ[7:3]) via programming Register 61h bits [3:0] in SiS5595 PCI to ISA bridge Configure space.

Meanwhile, accessing of the I/O ports are via the addresses programmed in Base Address Registers 10h~13h, 14h~17h, 18h~1Bh and 1Ch~1Fh in PCI IDE configuration space.

While serving as a bus master device, the IDE controller may transfer data between IDE devices and main memory directly. By performing the DMA transfer, IDE offloads the CPU and improves system performance. Bus master DMA programming is according to the information specification "Programming Interface for Bus Master IDE Controller".

The integrated IDE controller contains PCI configuration header and registers to meet PCI 2.2 specification. The integrated PCI IDE controller supports PCI type 0 configuration cycles of configuration mechanism #1.

Proper cycle timing is generated to meet PCI Bus speed and different modes of IDE drive. All cycle timing can be controlled by software programming from Register 40h to Register 49h in PCI IDE configuration space.

As a slave device, IDE decodes and interprets PCI cycles and generate signals to start and terminate IDE cycles. This block responds only to cycles that belong to IDE I/O address space. It supports both 16-bit and 32-bit I/O data transfer at address 1F0/170. All other IDE registers read or write operations are 8-bit only.

PIO mode operation

The IDE controller is capable of doing prefetch or post write in PIO mode. The count(in bytes) of prefetch length for each channel can be programmed in Prefetch Count Registers 4Ch~4Dh and 4Eh~4Fh in PCI IDE Configuration space. Normally, the count will be programmed as 512(2^9), which is the size of a single sector. The prefetch and post write functions can be enabled or disabled independently through control bits in Register 4Bh of PCI IDE configuration space. When prefetch is enabled, the controller will start prefetching when the first read data port command is received. It will keep prefetching until the FIFO is full or when prefetch count is reached. Whenever the FIFO becomes non-empty again, the prefetch will automatically resume until the prefetch count is reached.

When post write is enabled, the host can write data to FIFO in word- or Dword-increment. The IDE controller will automatically start IDE write cycles as long as FIFO is non-empty. When the fast post write function is enabled, the write IDE data port command on PCI bus will last for 3 PCI clocks only. When disabled, the PCI command will be 5 PCI clocks.

DMA mode operation

There is a DMA engine associated with each channel. The DMA engine can be invoked by writing the start-bit in Bus Master command register. The DMA engine will first request for PCI bus to read the descriptor from memory, load the address pointer and byte-count. For IDE read operation, the controller will start prefetching data into FIFO at this moment. When FIFO is half-full (or 62.5/25/12.5% full, programmable), the DMA engine will request for PCI bus to flush the data in FIFO to memory. If the prefetch count is reached while the FIFO is not yet half-full, the DMA engine will also request for PCI bus to flush the FIFO. For write operation, after descriptor is read, the DMA engine will again request for PCI bus to read data from memory to FIFO. At the same time, when the FIFO becomes non-empty, the controller will automatically start IDE write cycles to flush data in FIFO to IDE device. When data in FIFO is less than eight bytes, the DMA engine will again request for PCI bus to re-fill the FIFO.

Normally, the byte-count loaded in IDE controller will be equal to IDE transfer size programmed to IDE devices. If the two values were programmed differently, the IDE controller and the software that driving IDE should work together to prevent system from failure.

When the DMA engine is writing IDE

If the byte-count was programmed to be greater than the IDE transfer size, the IDE device will de-assert IDREQ signal when the transfer size is reached and issues interrupt to IDE controller. The IDE controller will pass transparently the interrupt to host. When the host clears the start-bit in response to the interrupt, the IDE controller will simply discard the remaining data in FIFO. When the host reads the status bit, it will see the interrupt bit set and active bit also set. This will be interpreted as a normal ending. If the byte-count was programmed to be less than the IDE transfer size, the controller will exhaust its data in FIFO while IDREQ signal is still asserting. The host should time-out because it does not receive any interrupt. When the host reads the status register, it will see the interrupt bit not set and the active bit set.

When the DMA engine is reading IDE

If the byte-count was programmed to be greater than the IDE transfer size, the IDE device will de-assert IDREQ signal when the transfer size is reached and issue interrupt to IDE controller. The IDE controller should mask the interrupt, request for PCI bus to flush all the data in FIFO to memory. After the FIFO is empty, the controller will unmask the interrupt to inform host that all data is visible in memory. The host, after receiving the interrupt, will read the status register and see the interrupt bit set and active bit also set. This will be interpreted as a normal ending.

If the byte count was programmed to be less than the IDE transfer size, the IDE controller will stop prefetching when its byte-count has reached while IDREQ signal is still asserted by device. The controller may or may not flush its data in FIFO to memory, depending on whether the FIFO has reached its request level or not. The host will eventually be time-out because it does not receive any interrupt. When the host reads the status register, it will see the interrupt bit not set and the active bit set. The remaining data in FIFO will be discarded when the host clears the start-bit.

Ultra-DMA33/66 Operation

Ultra DMA is a fast data transfer protocol used on IDE bus. By utilizing both the rising edge and the falling edge of the data strobe signal to latch data from DD[15:0], the data transfer rate is effectively doubled than that of the traditional multi-word DMA while the highest fundamental frequency on the cable is the same. In view of the faster transfer rate on IDE bus may easily fill the FIFO up when reading IDE device, in such condition the IDE bus will be idle and result in system performance degradation, SiS Chip lengthens the internal FIFO for each channel (channel 0/channel 1) to 16-Dword to improve system performance. When the FIFO is half-full (or 3/4-full, programmable), the DMA engine should request for PCI bus by asserting an internal request signal to system arbiter. The system arbiter, based on an algorithm described in the previous sections, shall grant the PCI bus to DMA engine by asserting an internal grant signal to it. Ideally, the FIFO should never be full during data-in operation so that the burst data transfers on IDE will not be suspended. When the IDE controller is transferring data from system memory to IDE, the DMA engine will initiate PCI burst cycles to read data from memory into FIFO until FIFO is full. The FIFO will decrease at the rate of the selected Ultra DMA mode as the IDE controller doing data-out operation. In the best situation, the FIFO should not be empty during data-out operation otherwise the burst data transfer on IDE will be suspended.

The Ultra-DMA mode can be enabled on a per-device basis and all three timing modes(0-2) are supported by programming the corresponding configuration registers. For Ultra-DMA operations, the following signal lines shall change to their new definition when IDACK# is asserted. These signals will revert back to their old definitions right after IDACK# is de-asserted.

The following table shows the signal line difference between old definition and new definition (Ultra DMA).

Table 5.6-3 Table for Different Command Definition

Old Definition	New Definition
IIOW#	STOP#
IIOR#	HDMARDY# --- data in operation HSTROBE --- data out operation
ICHRDY#	DSTROBE --- data in operation DDMARDY# --- data out operation

5.7. INTEGRATED HIGH PERFORMANCE 3D VGA CONTROLLER

5.7.1 HIGHLIGHT FUNCTION BLOCK

Basically the 2D graphics engine of integrated 3D VGA controller is a 64-bit BitBlt graphics engine. The integrated 3D VGA controller supports single-cycle read/write and block-write function of SGRAM in local frame buffer.

For enhanced 256-color graphics mode, the engine supports the following functions:

- 256 raster operations
- Rectangle fill
- Color/Font expansion
- Enhanced Color expansion
- Line-drawing with styled pattern
- Built-in 8x16 pattern registers
- Built-in 8x8 mask registers
- Rectangle Clipping
- Transparent BitBlt
- Direct Draw

For 32K or 64K high-color graphics mode, the engine supports the following functions:

- 256 raster operations
- Rectangle fill
- Color/Font expansion
- Enhanced Color expansion
- Line-drawing with styled pattern
- Built-in 8x16 pattern registers
- Built-in 8x8 mask registers
- Rectangle Clipping
- Transparent BitBltDirect Draw

For 16M-color graphics mode, due to different graphics process methods, the engine supports the following functions:

- Source/Destination BitBlt
- Pattern/Destination BitBlt
- Color/Font Expansion

Targeting on Direct3D acceleration, the integrated VGA controller achieves extremely high fill and polygon rate in high quality with high balanced pipeline 3D architecture. The major key technologies that guarantee a high 3D performance are the integrated Turbo Queue, Setup Engine, Texture Cache, and Pipeline Render Engine.

5.7.2 TECHNICAL DESCRIPTION

2D Graphics Engine

It is an enhanced 1T 64-bit BitBlt Graphics Engine.

For enhanced 256-color graphics mode, the engine supports the following functions:

- 256 raster operations
- Rectangle fill
- Color/Font expansion
- Enhanced Color expansion
- Line-drawing with styled pattern
- Built-in 8x16 pattern registers
- Built-in 8x8 mask registers
- Rectangle Clipping
- Transparent BitBlt
- Direct Draw

For 256/32K/64K/16M-color graphics mode, the engine supports the following functions:

- 256 raster operations
- Rectangle fill
- Color expansion
- Enhanced Color expansion
- Line-drawing with styled pattern
- Built-in 8x8 mask registers
- Built-in 8x16 pattern registers
- Rectangle Clipping
- Transparent BitBlt

Descriptions of the graphics engine functions are summarized as follows:

BIT BLOCK TRANSFER (BITBLT)

BitBlt moves a block of data from one location (source) to another location (destination). It is a ternary operation. The operands could be the source data, the destination data, and the brush pattern. There are three different kinds of BitBlt: from the host memory to the display memory, from the display memory to the host memory, and from one location of the display memory to another location of the display memory.

In the first two cases, the operation simply uses the "move string instruction" (REP MOVS) to move the source data to the destination to accomplish the BitBlt operation. It is called "CPU-driven BitBlt".

In the case of moving from the display memory to the display memory, integrated Graphics Controller could gain the advantage of its advanced engine design to solve the problems of memory overlapping during the block transfers. The only effort is to program the adequate parameters.

BITBLT WITH MASK

When the BitBlt operation deals with the hatched brush pattern, the programmer just needs to set the monochrome mask into Mask Registers, then the engine would handle the complicated process.

COLOR EXPANSION

The color/font expansion is used to expand a monochrome data (one bit per pixel) into a second color format which is n-bit per pixel during a moving operation. The foreground color and background color is addressed respectively from I/O address 8224h to 8227h and from I/O address 8228h to 822Bh. The font patterns are stored in the pattern registers (I/O address 8300h to 847Fh) or in the off-screen memory which is called Enhanced Color Expansion. These pattern registers store the monochrome bitmap. The BitBlt engine can expand 3072 pixels at a time. Thus the font-drawing and monochrome bitmap expansion can be easily accomplished.

ENHANCED COLOR EXPANSION

If the size of a monochrome bitmap is larger than 3072 pixels, there is not enough space in pattern registers to store this bitmap. In this case, the bitmap should be stored in the off-screen display memory instead of the pattern registers. The operation is called Enhanced Color Expansion.

The format written into the off-screen memory of the Enhanced Color Expansion operation is m x n

LINE DRAWING

The Bresenham's Line Algorithm is a well popular algorithm in graphics, which is used to draw a line. The drawing line could be either a solid line or a dashed line. To draw a solid line, we must use one solid foreground color. To draw a dashed line, we'll use two colors specified by the foreground and background color registers. There are several registers involved to control the starting location, pixel count and line style, etc.

RECTANGLE FILL

A rectangle area fill is a function to fill a specified rectangle area by using either a solid color (rectangle fill) or a pattern (pattern fill).

Rectangle Fill is simply to fill the destination rectangle with a solid color. The solid color is specified into the pattern foreground color register. Pattern Fill repeats a source pattern into a destination rectangle. Therefore the pattern registers must be specified.

RASTER OPERATIONS (RASTER OPS OR ROPS)

Raster Ops would perform some logical or arithmetic operations on the graphics data. There are 256 raster ops defined by Microsoft. Each raster op code is a Boolean operation with three operands: the source, the selected pattern, and the destination.

DIRECT DRAW

The Windows 95 Game SDK enables the creation of world class computer games. Direct Draw is a component of that SDK that allows direct manipulation of video display memory. To enhance the performance of games, SiS530 provides some Direct Draw functions.

Since the former engine functions can just support part of Direct Draw capabilities, transparent BitBlt functions are added into the graphics accelerator to meet the other Direct Draw functions. They are color key range comparison, alpha blending, and Direct Draw raster operation. The register format for transparent BitBlt is different from those of the engine's functions listed above.

When transparent BitBlt is enabled, the source and destination data are sent to the color key range comparators to determine whether they are between the high and low color key values. If they are in the color key range, the Direct Draw raster operation (D_Rop) will determine whether the source data after alpha blending or the original destination will be written back to memory.

5.7.2.1. TURBO QUEUE IN 2D GRAPHICS ENGINE

In the integrated 3D VGA controller, the graphics engine performs the acceleration functions as stated in the previous section via the acceleration commands stored in the command queue. The command queue is a FIFO (First In First Out) and ring structure, i.e., if an acceleration command is filled in the last stage of the command queue, then the following acceleration command would be filled in the first stage of the command queue.

Once this command queue is congested, the CPU's request will be pending until the command queue has free space to accept more acceleration commands. This would downgrade the graphics system performance severely. Thus the length of command queue will dominate the performance of the graphics engine.

To lengthen the command queue as long as required, the integrated 3D VGA controller provides two different kinds of command queue. The first one is built in the integrated VGA controller, which is called Hardware Command Queue. The other one is built in the off-screen display memory, which is called Turbo Queue and patent owned by SiS. The architecture diagram of the integrated 3D VGA controller command queue is as follows.

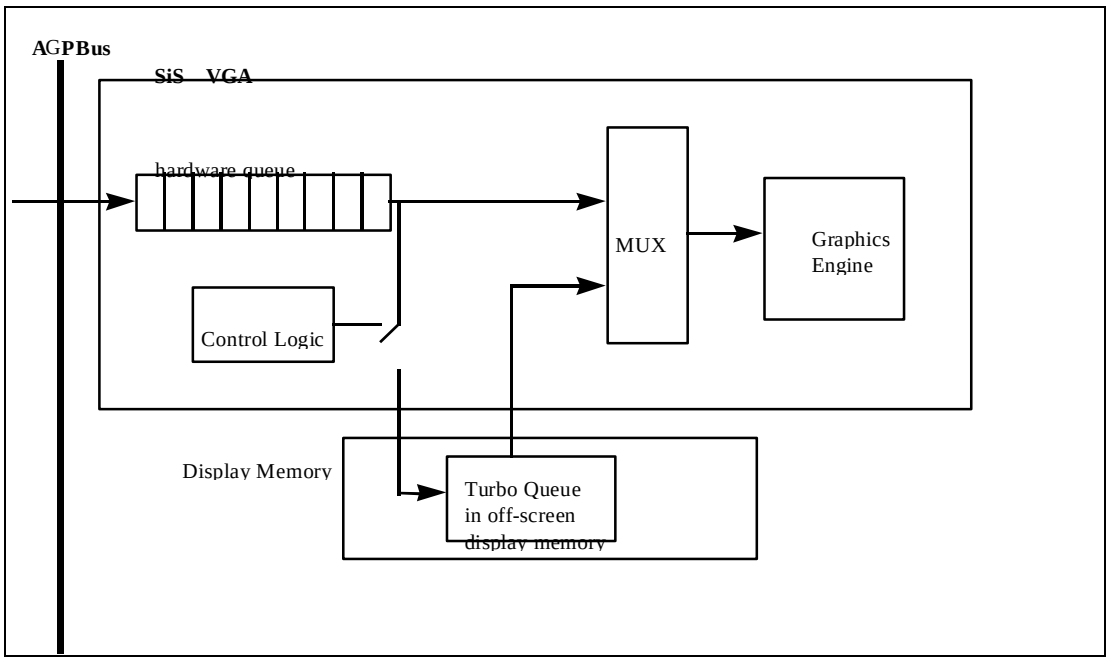


Figure 5.7-1 The Hardware Command Queue

Figure 5.7-1 The Hardware Command Queue is a 42 double-words queue. And there are 62K Bytes off-screen memory space reserved for the Turbo Queue. Since the average length of an engine command is 8 double-words (which is called 1 stage), therefore the integrated 3D VGA controller command queue could be regarded as infinity stages with Turbo Queue and could get rid of the CPU waiting issue to get extra high performance.

When the hardware command queue is going to be full, the head commands would be moved to the Turbo Queue and left hardware queue space for new commands. The command queue architecture makes the transmission of the integrated 3D VGA controller commands most efficient.

The Turbo Queue is also a FIFO and ring structure as stated before. The Turbo Queue base address is generally set to the last 64K Bytes segment on off-screen. To program the extended register SR2C (Turbo Queue Base Address Register) could allocate the Turbo Queue into the off-screen region of the display memory automatically.

5.7.2.2. 3D ACCELERATION

TURBO QUEUE IN 3D ACCELERATOR

The major technologies for the high performance and high quality 3D rendering in the integrated 3D VGA controller are:

- Turbo Queue
- Setup Engine
- Texture Cache
- Pipeline Rendering Engine

Using the Turbo Queue architecture (SiS patent pending) will speedup the rendering for 3D engine. The Turbo Queue length is virtually infinite, therefore 3D driver can issue commands without waiting. To save the high cost for building a long enough hardware command queue, the integrated 3D VGA controller allocates a portion of the off-screen memory as the command queue buffer. Once The integrated 3D VGA controller detects the status of the internal hardware command queue nearly full, some of the commands in the hardware queue will be temporally swapped to the off-screen area. When 2D or 3D engine finishes previous command, these off-screen commands will be read back first as the next command for execution.

In the integrated 3D VGA controller architecture, 2D and 3D engines share the same hardware queue and off-screen command queue but only one engine is active at a time. In this way, we can guarantee a correct execution sequence.

SETUP ENGINE

Setup Engine is one of the most critical parts in the new generation 3D design. It calculates and prepares all of the parameters for primitive drawing. All these computations need more than hundreds of addition, subtraction, multiplication, and division. If we do this setup calculation by host CPU, the sequential coding and processing forms a bottleneck for 3D rendering.

To off-load this computation time from host CPU and to do it in parallel, the integrated 3D VGA controller integrates a VLIW-like 32-bit floating point Setup Engine. It can finish all of the setup computations for a triangle within 60 memory clocks. This should be 10 times faster than the computing power from Pentium-200 CPU. Moreover, Setup Engine also supports line and point setup calculations with much less memory clocks than triangle setup required. This Setup Engine, specially designed to fit all the data formats in Microsoft Direct3D API, can accept vertex values directly in floating point format.

Once Setup Engine finishes the setup computations for a triangle, it transfers all these parameters to Render Engine within one memory clock. While Rendering Engine is busying drawing a triangle, Setup Engine can calculate the parameters needed for the next one.

RENDERING ENGINE

Rendering Engine is a pipeline structure engine in the integrated 3D controller. This engine is formed by Shading Engine, Texture Engine, and Post Engine.

The output of Shading Engine is a series of pixel color which represents the shade of a primitive. Texture Engine is responsible for attaching the texture color on a pixel. Then, Post Engine will do some operations such as fogging, alpha blending, dithering, and ROP for this pixel.

In order to support high quality texture mapping, the integrated 3D VGA controller supports point-sampled, linear, bi-linear, and tri-linear texture filtering. With an integrated high-capacity texture cache, the integrated 3D VGA controller can render texture pixels in the same fill rate no matter point-sampled, linear, or bi-linear texture filtering method is in use. For tri-linear texture mapping, half fill rate is achieved. But better video quality is expected rendering in tri-linear texture mapping mode.

TEXTURE CACHE

Texture Cache is one of the critical part of high performance 3D design. Most of the 3D chips have not built-in texture cache and need to fetch each texture pixel again and again during the rendering process. If the texture is in use for several times, there is no reason to fetch texture from memory again and again. Built-in texture cache could significantly improve texture mapping performance.

With built-in texture cache, each time when a texture miss happens, a segment of texture will be read from texture buffer and stored in a internal texture cache line. Replacement policy is based on LRU (Least Recently Used) algorithm to optimize the texture cache hit rate. Under Direct3D benchmark, more than 90% hit rate has been measured. The texture buffer can locate in off-screen area or system memory. If you need very large texture buffer size, the location in system memory is suggested.

CONCLUSION

The introduction of the integrated 3D VGA controller means the beginning of the new generation of 3D accelerator and the end of low-end, unbalanced 3D solutions. To achieve a high performance in 3D rendering, several strategies have to be used. Turbo Queue, Setup Engine, Rendering Engine, and Texture Cache will become the uncompromising choice in high performance 3D architecture.

5.7.2.3. DISPLAY MEMORY ARCHITECTURE

There are two display memory architecture, local frame buffer and shared frame buffer, presented in the integrated 3D VGA controller.

LOCAL FRAME BUFFER MODE:

In 1-bank (single side, 32 bits data bus) configuration,

- SCLK would be active.
- VCS0# would be active.
- Only DQM[0:3] would be active.
- VWE# would be active.
- VSRAS# and VSCAS# would be active.
- Only VMD[0:31] would be active.

- VMA[0:11] would be connected to all bank.

In 2-bank (single side, 64 bits data bus) configuration,

- SCLK would be active.
- VCS0# would be active.
- VDQM[0:7] would be active.
- VWE# would be active.
- VSRAS# and VSCAS# would be active.
- VMD[0:63] would be active.
- VMA[0:11] would be connected to all bank.

In 4-bank (double size, 64 bits data bus) configuration,

- SCLK would be active.
- VCS0#, VCS1# would be active.
- VDQM[0:7] would be active.
- VWE# would be active.
- VSRAS# and VSCAS# would be active.
- VMD[0:63] would be active.
- VMA[0:11] would be connected to all bank.

SHARED FRAME BUFFER MODE:

Only in bank-0 configuration

- SDCLK[0:3] would be active.
- CS0# would be active.
- DQM[0:7] would be active.
- WE# would be active.
- SRAS# and SCAS# would be active.
- MD[0:63] would be active.
- MA[0:14] would be connected to all bank

5.7.2.4 INTERNAL DUAL-CLOCK SYNTHESIZER

The integrated 3D VGA controller has built-in a dual-clock synthesizer to generate the MCLK and VCLK. This clock synthesizer could generate several variable frequencies, thus it could provide the flexibility for selecting the working frequency.

The following block diagram is for clock synthesizer.

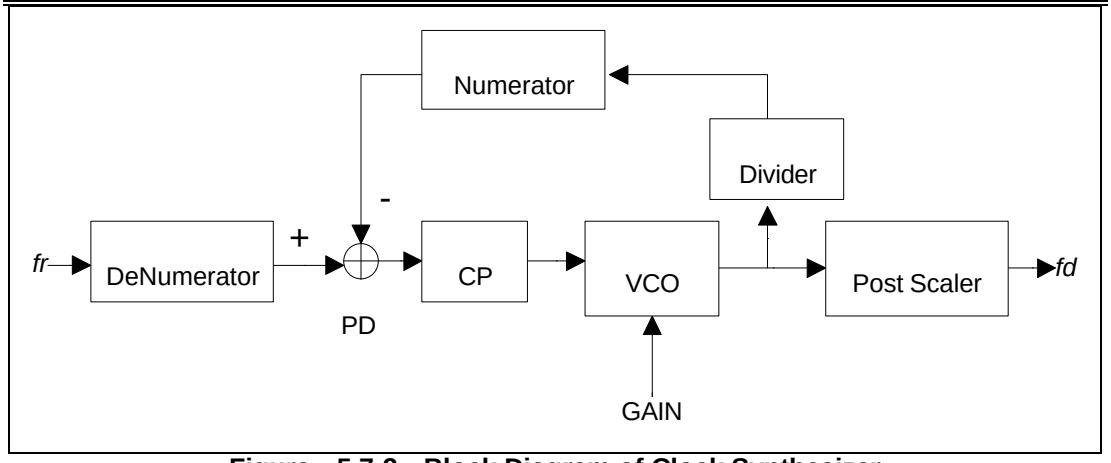


Figure 5.7-2 Block Diagram of Clock Synthesizer

where PD is phase detection,
CP is charge pump,
VCO is voltage controlled oscillator,
fr is reference frequency, and
fd is desired frequency.

The operation of clock synthesizer is described as follow:

When the synthesizer outputs the steady frequency, it means that

fd=fr*((Numerator+1))/(DeNumerator+1))*(Divider/Post Scalar)

With this formula, we could select adequate values for Numerator, DeNumerator, Divider, and Post Scalar to obtain the desired frequency.

The planned Video Clocks (VCLK) are as follow: (units: MHz)

Table 5.7-2 Table of Planned Video Clock

25.175	28.322	40.000	50.000	77.000
36.000	44.889	135.000	120.000	80.000
31.500	110.000	65.000	75.000	94.500
162.00	175.500			

Other video clocks would be added to the scheme after verified OK.
The planned Memory Clocks (MCLK) are from 40 MHz to 100 MHz with resolution 2 MHz and used by local frame buffer.

5.7.2.5. POWER MANAGEMENT

To satisfy the power saving for Green PC, the integrated 3D VGA controller supports the control protocol of DPMS (Display Power Management Signaling) proposed by VESA Monitor Committee. This protocol can reduce the VGA Monitors' power consumption.

The integrated 3D VGA controller has built-in two timers for stand-by and suspend modes that can be programmed from 2 minutes to 30 minutes (2 min./increase) with the extended registers.

The integrated 3D VGA controller also supports forcing the video subsystem into stand-by, suspend, or off modes with the extended registers.

Power saving is done by blocking HSYNC and/or VSYNC signals to the VGA monitor. The sources of activation are from the monitoring of keyboard, hardware cursor, and/or video memory read/write. The overview of the signal blocking requirements are as follows:

Table 5.7-3 Table of Power Management State

POWER MANAGEMENT STATE	HORIZONTAL SYNC	VERTICAL SYNC	VIDEO DISPLAY
ON	Pulses	Pulses	Yes
Stand-By	No Pulses	Pulses	No
Suspend	Pulses	No Pulses	No
OFF	No Pulses	No Pulses	No

Resolutions Supported

Table 5.7-4 Table of Resolutions Supported

Resolution	2M Byte DRAM	4M Byte DRAM	8M Byte DRAM
640x480x8	√	√	√
640x480x16	√	√	√
640x480x24	√	√	√
800x600x4	√	√	√
800x600x8	√	√	√
800x600x16	√	√	√
800x600x24	X	√	√
1024x768x4	√	√	√
1024x768x8	√	√	√
1024x768x16	X	√	√
1024x768x24	X	X	√
1280x1024x4	√	√	√
1280x1024x8	X	√	√
1280x1024x16	X	X	√
1600x1200x4	√	√	√
1600x1200x8	X	√	√

Except these real resolution modes, the integrated 3D VGA controller is also built-in virtual screen mode which could support up to 2048x2048 resolution.

5.7.2.6 VIDEO ACCELERATOR

VIDEO PASSWORD/IDENTIFICATION REGISTER

A video registers protection is implemented in the index 80h of CRT index register 3D4. To disable the protection, the software must first match the protection key value of 86h. If not match, read/write to any of the video associated registers are denied.

VIDEO PLAY BACK

The integrated 3D VGA controller video accelerator only could work in PCI multimedia mode.

In PCI multimedia mode, the integrated 3D VGA controller supports PCI multimedia design guide Rev. 1.0 spec to meet future potential trend.

MULTI-FORMAT VIDEO FRAME BUFFER

The video frame buffer of the integrated 3D VGA controller is shared with graphics frame buffer and is a multi-format frame buffer. It could accept 16-bpp YUV422, RGB555, and RGB565 color format and 12-bpp YUV420 (plane mode).

The decompression CODEC, hardware or software, could fill the valid decompressed video frame data into the off-screen video frame buffer through the PCI local bus.

The other PCI motion video card or CPU can transfer the video data through PCI local bus directly into video frame buffer.

Then the integrated 3D VGA controller would overlay the video on the screen.

YUV420 PLANE MODE

The integrated 3D VGA controller supports YUV420 plane mode. The data rate of YUV420 is 12-bpp which is smaller than 16-bpp of YUV422. So that the data bandwidth can be reduced and improve the video playback performance. The YUV420 mode need three start addresses for Y, U and V plane, and two offsets for Y and U, V plane.

VIDEO PLAYBACK LINE BUFFERS

When CRT refresh the screen, the video data must be overlaid with graphics data. Therefore the video data would first be read out from off-screen video frame buffer into the video playback line buffers for further handling.

The video playback line buffers serve as buffers between display memory and the playback mechanisms, are provided to fit the limitation of the display memory during video playback operation.

COLOR SPACE CONVERSION & COLOR FORMAT CONVERSION

If the data read from the video frame buffer is in YUV422, the real time YUV-to-RGB converter will be turned on. The video data would be converted to RGB888 format for successive processing. The YUV422 are converted to follow the CCIR601-2 standard.

If the data read from the video frame buffer is in RGB format, the YUV-to-RGB converter would be bypassed. All the RGB565 and RGB555 format are supported and then would be converted to RGB888 format.

HORIZONTAL INTERPOLATION DDA

The DDA (Digital Differential Accumulator) using the following mathematical calculation with 2-tap, N-phase and scaling up factor UFACT (from J points scaling up to J * UFACT points):

Destination[i] = (1 - Weight") * Source[j] + Weight" * Source[j+1]
j = TRUNC(i / UFACT)
Weight" = TRUNC(i / UFACT) - j

However since the *Weight" is not an integer, the multiplication is hard to implement and therefore the following Weight is used for calculation.

Weight = TRUNC(Weight" * N) / N

The integrated 3D VGA controller built-in an X-interpolation DDA mechanism to get better video stretching quality. The interpolation accuracy of DDA mechanism is 2-tap and 8-phase.

VERTICAL INTERPOLATION DDA

The integrated 3D VGA controller built-in a Y-interpolation DDA mechanism and two line buffers mechanism to get better video stretching quality. The interpolation accuracy of DDA mechanism is 2-tap and 8-phase.

VIDEO PLAYBACK HORIZONTAL ZOOMING

The playback video data can be horizontal zoom-in in 64/n factor (n = 1 ~ 64) and zoom-out in about m/16 factor (m = 1 ~ 16). The zooming factor (HPFACT) is controlled by 4-bit integer part and 6-bit fraction part. The horizontal video size will be zoomed to 1/HPFACT. If HPFACT<1, it will perform horizontal up scaling. If HPFACT>1, it will perform horizontal down scaling.

VIDEO PLAYBACK VERTICAL ZOOMING

The playback video data can be vertical zoom-in in 64/n factor (n = 1 ~ 64) and zoom-out in arbitrary factor. The zooming factor (VPFACT) is controlled by 6-bit fraction part. The video size will be zoomed to 1/VPFACT. Since the VPFACT is always less than 1, therefore you can only perform vertical up scaling by this factor. The vertical down scaling can be done by multiplying the Video Frame Buffer Offset with an integer I. Then the vertical video size will be zoomed to 1/(I*VPFACT).

COLOR KEYING

A control signal is generated by comparing the 24 bits graphics data to the 24 bits color key low value and 24 bits color key high value. The bit number is dependent on color depth used. If the graphics data value is between the two color key values (all of the three RGB parts), the color key is detected. This comparison mechanism can be disable by setting the video window size to zero, i.e. X-start=0, X-end=0, Y-start=0, and Y-end=0.

GRAPHICS & VIDEO OVERLAY

The overlay of the graphics data and the video data is performed by color keying and chroma keying method. The overlay operation is set by Key Overlay Operation Mode Register. The operation is defined below:

Table 5.7-5 Table of Graphics and Video Overlay Operation Mode

Operation Mode	Operation
0000	always select graphics data

0011	select blended data when color key, otherwise select graphics data
1111	always select Video data

VIDEO WINDOW CONTROL REGISTERS

The video window area is defined by six registers that specify a rectangular region by X-start, X-end, Y-start, and Y-end (X: Horizontal, Y: Vertical). Please refer to " 7.9.2".
The location of the video window is referenced to the VGA sync signals.
The size of the video window is defined in VGA pixels and lines.

VIDEO PANNING

The displayed video image could be panned around the captured video image by setting the video display starting address, i.e., you may selectively display any part of the captured video image. The video display starting address is equal to the video frame buffer starting address adding the panning offset.

OVERLAY MEMORY DATA

The display memory is configured to two areas: one is the graphics area (which is the actual screen display area) storing graphics pixel data, and the other is the video area (which is also called off-screen area) storing the video pixel data.

In the graphics area, the corresponding video window area is reserved with the color key value. During the CRT scan period, a comparison of graphics data with color key data is performed. Once a match meets, the CRT output path would be switched from graphics path to video path to display the video data.

VIDEO PLAYBACK CONTRAST ENHANCEMENT AND BRIGHTNESS CONTROL

To achieve higher video quality, the integrated 3D VGA controller built-in the Contrast Enhancement and Brightness Control mechanism.

For Contrast Enhancement, first, the mean value is calculated by some pixels and some frames. The number of sampled pixels and frames is programmable by registers. Contrast Enhancement mechanism then increases the difference between the video data and mean value. The increasing rate is programmed by gain. The value of gain is frame 1.0 to 1.4375.

The Brightness of video data can be controlled. The Brightness is a 2's complement value from -128 to 127. This value is then added with the video data to increase or decrease the brightness of video.

5.7.2.7 SIGNATURE ANALYSIS

The signature analysis is provided to automatically test the graphics data which is the input of the DAC. This technique is based on the concept of cyclic redundancy checking (CRC) and is realized in hardware using linear feedback shift registers (LFSRs). It is composed of a 16-bit signature generator register which is called multiple-input signature register (MISR, shown in the following figure) and is used to ensure a unique signature of different patterns.

For a given test image, the signature analysis could get a right unique signature number. If an error occurs in the controller or the data manipulation, it would result in a different wrong

signature number as compared to the pre-calculated signature value. Thus a test technician could sort the good or bad chips more quickly and accurately and requires no visual inspection of the screen for errors in the mass product environment. This could save significant testing time. If the display screen includes blinking attributes or a blinking cursor, then the signature will be different when blink-off and blink-on for those frames. Assume all error patterns are equally likely, then the probability of failing to detect an error by the MISR is approximately 0.000015.

To match the inputs of MISR, the 24-bit graphics data (i.e. the input of the DAC of the RAMDAC) would be first converted into 16-bit data. The corresponding transfer function of the MISR of the following figure is

$$p(x) = 1 + c_1 \cdot x + c_2 \cdot x^2 + c_3 \cdot x^3 + ... + c_{16} \cdot x^{16}$$

where $c_1, c_2, c_3, ..., c_{16}$ can be either 0 or 1. The integrated 3D VGA controllersets the parameters of the signature register as

$$p(x) = 1 + x + x^7 + x^{10} + x^{16}$$

Once the software enables the signature analySiS function, The integrated 3D VGA controller could test itself intelligently and automatically. This function could also be disabled by the extended control register for power saving purposes.

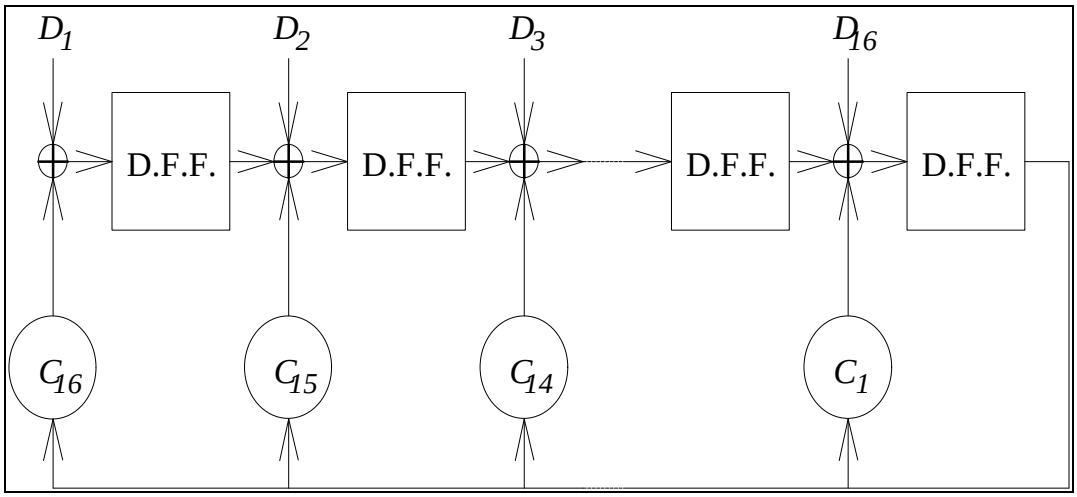


Figure 5.7-3 Multi-Input Signature Register (MISR)

5.7.2.8. SOFTWARE SUPPORT

To fully utilize and support the integrated 3D VGA controller hardware features, SiS has developed a high-performance VESA extension compliant BIOS.

Extended graphics and text modes are supported by software application drivers which developed by SiS. The following applications are currently supported:

- 3D Studio Version 3.0
- AutoCAD/386 Release 11, 12, 13
- Auto Shade/386 Version 2.0

- Microsoft Windows 3.1 & 3.11
- Microsoft Windows 95/98
- Microsoft Windows NT Version 4.0 and 5.0
- OS/2 Presentation Manager 3.0 and 4.0

Video operation is supported by software application which drivers developed by SiS. The following applications are currently supported:

- DCI driver
- Direct Draw driver

3D operations are supported by software application drivers developed by SiS. The following applications are currently supported:

- Microsoft Direct3D
- OpenGL in Windows NT4.0/5.0
- OpenGL in Windows 98
- Renderware for Windows 95/98

COMPATIBILITY

The integrated 3D VGA controller is fully compatible with all standard IBM VGA modes and EGA, CGA, MDA, and Hercules modes.

5.8. BALL CONNECTIVITY TESTING

SiS Chip will provide a NAND chain Test Mode by TEST# signal is pull low. In order to ensure the connections of balls to tracks of main board, SiS Chip provides a simple way to do connective measurements. Basically, an additional 2-input-NAND gate is added into the I/O buffer cells. And, one of inputs of NAND gate is connected to input pin of I/O buffer as test input port in test mode. To monitor the test result at test output port, the output of the NAND gate is connected to the other input of the next NAND gate. Such that, the test result could be propagated and it forms a NAND tree, as depicted in Figure 5.8-1. To adapt to the scheme, all output buffers of SiS Chip are changed to bi-direction buffers to accept test signals.

5.8.1 TEST SCHEME

There are six NAND tree chains are provided by SiS Chip. Each NAND tree chain has several test-input pins and one output pin.

The following description is an example on 4-test-input pins to explain a NAND tree chain test scheme.

First of all, logic LOW is driven into TESTIN1 pin from track on main board. If logic HIGH could be observed at TESTOUT pin, it means that the connection of TESTIN1 pin to track is good, as shown in Figure 5.8-2. To test TESTIN2 pin, TESTIN2 pin should be driven LOW also. And, TESTIN1 pin should be kept at logic HIGH, such that the test result could be passed to TESTOUT pin and so on. Although SiS Chip operates at 3.3V, all input buffers of SiS Chip are 5V-input tolerance. Hence, all test signal could go up to 5V.

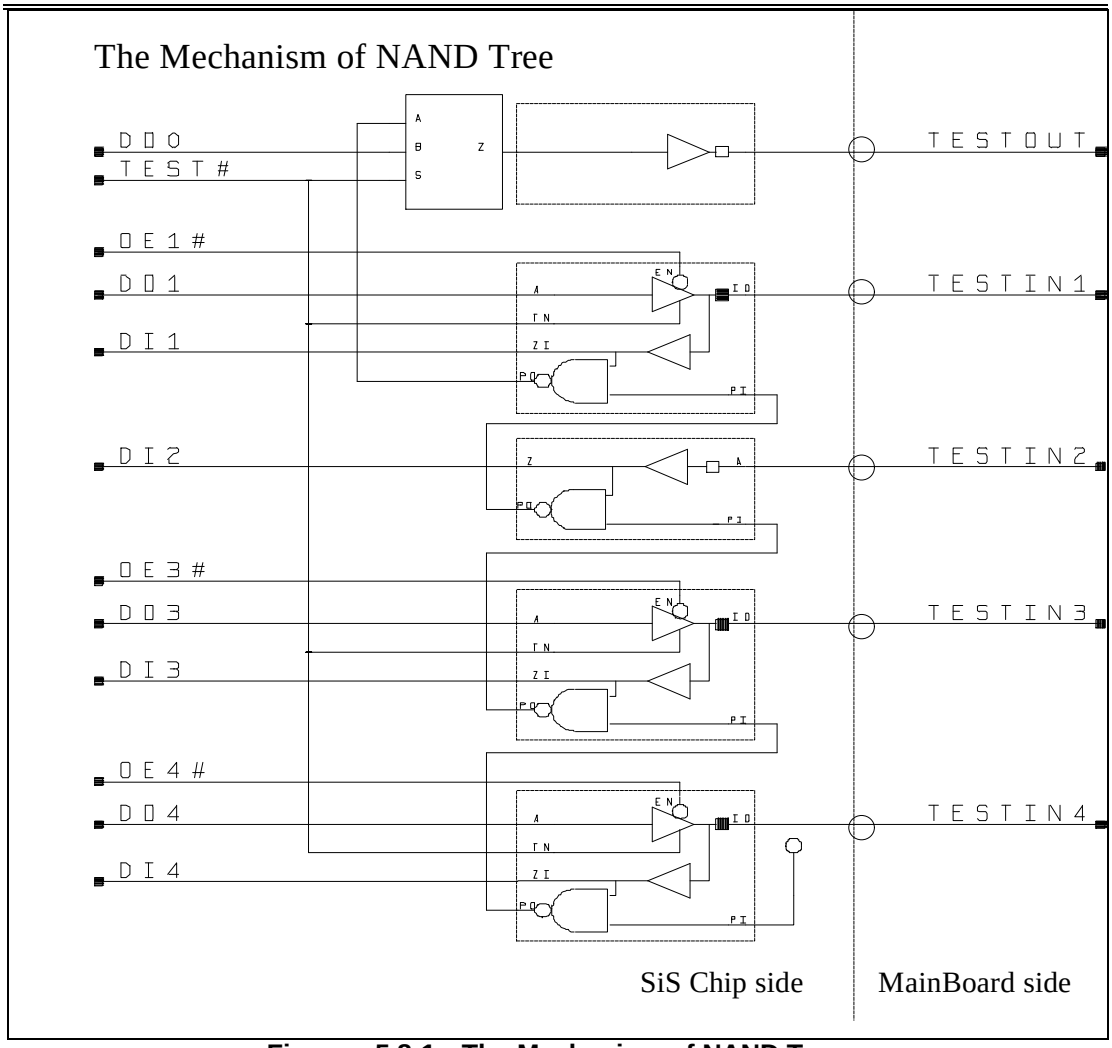


Figure 5.8-1 The Mechanism of NAND Tree

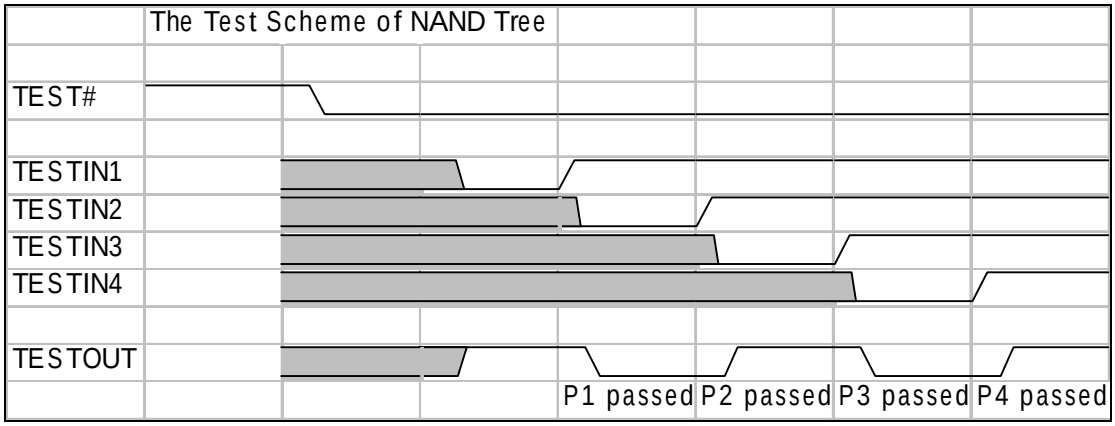


Figure 5.8-2 The Test Scheme of NAND Tree

5.8.2. MEASUREMENTS

During test process, this scheme requires all test inputs to be driven simultaneously. To decrease the amount of test probes, SiS Chip divides pins into 6 branches. Meanwhile, some noise sensitive signals or analogue signals, i.e. RTC, and power signals, are excluded. The final number of test-input probes is limited to 78 and these six NAND trees are listed on next page.

Table 5.8-1 NAND Tree List for SiS530

TEST VECTORS	TEST INPUT BALL NAME LIST	TEST OUTPUT BALL NAME
NT1[1:72] (NAND Tree 1)	OSCI, VSYNC, HSYNC, DDCCLK, DDCDAT, ENVCO, PLSENSE, PLPWDN, VMD63, VMD62, VMD61, VMD60, DCLK, VMD59, VMD58, VMD57, VMD56, VCS#1, VDQM7, VDQM6, VDQM5, VDQM4, VMD55, VMD54, VMD53, VMD52, VMD51, VMD50, VMD49, VMD48, VMD47, VMD46, VMD45, VMD44, VMD43, VMD42, VMD41, VMD40, VMD39, VMD38, VMD37, VMD36, VMD35, VMD34, VMD33, VMD32, SCLK, DSF, VMA11, VMA10, VMA9, VMA8, VMA7, VMA6, MA5, VMA4, VMA3, VMA2, VMA1, VMA0, VCS#0, VSRAS#, VSCAS#, VWE#, VMD31, VMD30, VMD29, VMD28, VMD27, VMD26, VMD25, VMD24	PGNT0#
NT2[1:76] (NAND Tree 2)	VDQM3, VDQM2, VDQM1, VDQM0, VMD23, VMD22, VMD21, VMD20, VMD19, VMD18, VMD17, VMD16, VMD15, VMD14, VMD13, VMD12, VMD11, VMD10, VMD9, VMD8, VMD7, VMD6, VMD5, VMD4, VMD3, VMD2, VMD1, VMD0, INTA#, PREQ#3, PREQ#0, PREQ#1, PREQ#2, AD31, AD30, AD29, AD28, AD27, AD26, AD25, AD24, CBE#3, AD23, AD22, AD21, AD20, AD19, AD18, AD17, AD16, CBE#2, FRAME#, IRDY#, TRDY#, DEVSEL#, PLOCK#,	PGNT1#

	STOP#, PAR, CBE#1, AD15, AD14, AD13, AD12, AD11, AD10, AD9, AD8, CBE#0, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0	
NT3[1:61] (NAND Tree 3)	IRQ14, IRQ15, IDA7, PCICLK, IDA8, PCIRST#, PHOLD, IDA6, IDA9, IDA5, IDA10, IDA4, IDA11, IDA3, IDA12, IDA2, IDA13, IDA1, IDA14, IDA0, IDA15, IADRQ, IAIOWC#, IAIORC#, IACHRDY, IADACK, IAIRQ, IADSA1, IADSA0, IADSA2, IACBLID, IACS#0, IACS#1, IDB7, IDB8, IDB6, IDB9, IDB5, IDB10, IDB4, IDB11, IDB3, IDB12, IDB2, IDB13, IDB1, IDB14, IDB0, IDB15, IBDRQ, IBIOWC#, IBIORC#, IBCHRDY, IBDACK, IBIRQ, IBDSA1, IBDSA0, IBDSA2, IBCBLID, IBCS#0, IBCS#1	PGNT2#
NT4[1:79] (NAND Tree 4)	HD63, HD62, HD61, HD60, HD59, HD58, HD57, HD56, HD55, HD54, HD53, HD51, HD52, HD50, HD49, HD48, HD47, HD43, HD41, HD45, HD44, HD46, HD40, HD42, HD38, HD39, HD36, HD37, HD34, HD35, HD32, HD33, HD31, HD29, HD30, HD27, HD28, HD25, HD26, HD23, HD24, HD19, HD21, HD20, HD22, HD17, HD16, HD18, HD15, HD13, HD14, HD12, HD11, HD10, HD9, HD8, HD7, HD6, HD5, HD4, HD3, HD1, HD2, HD0, SMIACT#, M/IO#, HCLK, CACHE#, KEN#, D/C#, AHOLD, BRDY#, NA#, BOFF#, HLOCK#, ADS#, HITM#, EADS#, W/R	PGNT3#
NT5[1:84] (NAND Tree 5)	HBE#0, HBE#1, HBE#2, HBE#3, HBE#4, HBE#5, HBE#6, HBE#7, HA20, HA19, HA18, HA17, HA16, HA14, HA15, HA13, HA12, HA9, HA11, HA10, HA5, HA8, HA7, HA31, HA25, HA23, HA27, HA21, HA26, HA24, HA22, HA28, HA3, HA29, HA4, HA6, HA30, KOE#, ADSC#, ADSV#,	PHLDA

	BWE#, GWE#, CS1#, TA0, TA1, TA2, TA3, TA4, TA5, TA6, TA7, TAGWE#, MD32, MD0, MD33, MD1, MD34, MD2, MD35, MD3, MD36, MD4, MD37, MD5, MD38, MD6, MD39, MD7, MD40, MD8, MD41, MD9, MD42, MD10, MD43, MD11, MD44, MD12, MD45, MD13, MD46, MD14, MD47, MD15	
NT6[1:77] (NAND Tree 6)	SCAS#, RAMW#, DQM4, DQM0, DQM5, DQM1, SRAS#, CS#A5, CS#A4, CS#A3, CS#A2, CS#A1, CS#A0, MA0, MA1, MA2, MA3, MA4, MA5, MA6, MA7, MA8, MA9, MA10, MA11, MA12, MA13, MA14, SDCLK, CS#B5, CS#B4, CS#B3, CS#B2, CS#B1, CS#B0, DQM6, DQM2, DQM7, DQM3, CKE5, CKE4, CKE3, CKE2, CKE1, CKE0, MD48, MD16, MD49, MD17, MD50, MD18, MD51, MD19, MD52, MD20, MD53, MD21, MD54, MD22, MD55, MD23, MD56, MD24, MD57, MD25, MD58, MD26, MD59, MD27, MD60, MD28, MD61, MD29, MD62, MD30, MD63, MD31	BM_REQ#

6. HARDWARE TRAPPING DESCRIPTION

There are some pins are used for trapping purpose to identify the hardware configurations at the power-up stage. These pins will be recognized as "1" if pull-up resistors are used; and will be recognized as "0" if pull-down resistors are used. The following table is a summary of all the Hardware Trap pins in SiS Chip.

SYMBOL	DESCRIPTION
MD62	**Control for Integrated VGA Controller** Pull-up: Disable Pull-down: Enable
MD61	**Decoding behavior for integrated VGA Host bus interface** Pull-up: Slow Decode Pull-down: Fast Decode
MD59	**Interrupt signal (INT#A) Control for Digital Flat Panel** Pull-up: Disable Pull-down: Enable
MD48	**Shared Frame Buffer/Local Frame Buffer Selection** Pull-up: Shared Frame Buffer Architecture Pull-down:Local Frame Buffer Architecture
MD47	**Internal PLL Circuits for PCI clock to optimize timing control** Pull-up: Disable Pull-down: Enable
MD46	**Internal PLL circuit for SDRAM clock to optimize timing control** Pull-up: Disable Pull-down: Enable
MD45	**Internal PLL Circuits for CPU clock to optimize timing control** Pull-up: Disable Pull-down: Enable
MD[43:40]	**Internal HDWCLK Clock Delay Control**

	Please refer to Note 2.
MD[39:36]	**Internal MCLK Delay Control for shared frame buffer mode** Please refer to Note 3
ENVCO	**Testing Mode Control for MCLK Clock Generator** Pull-up: Normal Mode Pull-down: Test Mode
VMD63, VMD62, VMD61	**Internal SCLK Control for local frame buffer mode** Please refer to Note 4
MD53, MD52, MD49, MD44	**Testing Mode Control** Pull-up: Test Mode Pull-down: Normal Mode
MD58	**Digital Flat Panel interface Control** Pull-up: Enable Pull-down: Disable

Note:

1. There are pull-down resistors on MD and VMD lines.
2. This field controls the phase of HDWCLK that ahead of CPUCLK.

In order to guarantee HD which is driven from SiS530 onto to host bus has enough setup time margin to CPU, HDWCLK is introduced to let SiS530 internal HD driving circuits refer to, and HDWCLK is programmable to be ahead of CPU clock.

MD[43:40]	Descriptions	MD[43:40]	Descriptions
1111	-2.0ns	0111	+2.0ns
1110	-1.5ns	0110	+2.5ns
1101	-1.0ns	0101	+3.0ns
1100	-0.5ns	0100	+3.5ns
1011	+0.0ns	0011	+4.0ns
1010	***+0.5ns***	0010	+4.5ns
1001	+1.0ns	0001	+5.0ns
1000	+1.5ns	0000	+5.5ns

3. This field controls the phase of MCLK that ahead of SDCLK for using shared frame buffer.

MCLK setting is used for VGA memory controller, it functions as SDWCLK for core logic.

MD[39:36]	Descriptions	MD[39:36]	Descriptions
1111	+6.5ns	0111	+2.5ns
1110	+6.0ns	0110	+2.0ns
1101	+5.5ns	0101	+1.5ns
1100	+5.0ns	0100	+1.0ns
1011	+4.5ns	0011	+0.5ns

1010	***+4.0ns***	0010	+0.0ns
1001	+3.5ns	0001	-0.5ns
1000	+3.0ns	0000	-1ns

4. For using Local Frame Buffer solution:

VMD62	VMD63	VMD61	SCLK	FRAME BUFFER TYPE
0	0	0	83MHz	SDRAM
0	1	0	90MHz	SDRAM
1	0	0	100MHz	SDRAM
1	1	0	110MHz	SDRAM
0	0	1	83MHz	SGRAM
0	1	1	90MHz	SGRAM
1	0	1	100MHz	SGRAM
1	1	1	110MHz	SGRAM

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7. CORE LOGIC CONFIGURATION REGISTER

7.1. HOST-TO-PCI BRIDGE CONFIGURATION SPACE

7.1.1. HOST-TO-PCI BRIDGE CONFIGURATION SPACE HEADER

DEVICE	IDSEL	FUNCTION NUMBER
Host to PCI bridge	AD11	0000b

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
00-01h	Vendor ID	1039h	RO
02-03h	Device ID	0530h	RO
04-05h	PCI Command Register	0005h	RO,R/W
06-07h	PCI Status Register	0210h	RO WC
08h	Revision ID	02h	RO
09h	Programming Interface	00h	RO
0Ah	Sub-Class Code	00h	RO
0Bh	Base Class Code	06h	RO
0Ch	Cache Line Size	00h	RO
0Dh	Master Latency timer	FFh	R/W
0Eh	Header Type	80h	RO
0Fh	BIST	00h	RO
10-13h	Graphic Window Base Address	00000000h	RO R/W
14-33h	Reserved	00h	
34h	Capability Pointer	C0h	RO

7.1.2. HOST/L2 CACHE/DRAM

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
50h	NA# Control	00h	R/W
51h	L2 Cache Control Register	00h	R/W
52h	L2 Cache/DRAM Function Control	00h	R/W
53~54h	Reserved	0000h	R/W
55h	DRAM Bank open/close Control	00h	R/W
56h	Refresh Control	00h	R/W
57h	Reserved	00h	R/W
58h	DRAM Control	50h	R/W

59~5Bh	Reserved	000000h	R/W
5Ch	DRAM Initialization Command	00h	R/W
5Dh	DRAM Control	00h	R/W
5Eh	DRAM Control	00h	R/W
5Fh	Reserved	00h	R/W
60~62h	DRAM Types of Bank 0/1/2	0000h	R/W
63h	DRAM Status Register	00h	R/W

7.1.3. CURRENT DRIVING

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
64h	DRAM Signals Driving Current Control	00h	R/W
65h	PCI Signals Driving Current Control	00h	R/W

7.1.4. POWER MANAGEMENT

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
68h	SMRAM Access Control	00h	R/W
69h	System Event Monitor Control for Power Management	00h	R/W
6A~6Bh	ACPI I/O Base Address Register	0000h	R/W
6Ch	DRAM Self-Refresh Control for Power Management	00h	R/W

7.1.5. SHADOW RAM & NON-CACHEABLE AREA

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
70~75h	Shadow RAM Register	00h	R/W
76h	BIOS Shadow Attribute	00h	R/W
77h	Non-cacheable Area Characteristics	00h	R/W
78~79h	Allocation of Non-cacheable area I	0000h	R/W
7A~7Bh	Allocation of Non-cacheable area II	0000h	R/W

7.1.6. HOST BRIDGE & PCI ARBITER

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
80h	Target Bridge to DRAM Characteristics	00h	R/W
81h	PCI Target Bridge Characteristics	00h	R/W
82h	PCI Target Bridge Bus Characteristics	00h	R/W
83h	CPU to PCI Characteristics	00h	R/W
84~85h	PCI Grant Timer	FFFFh	R/W
86h	CPU Idle Timer for PCI	FFh	R/W

87h	CPU to PCI Characteristics and Arbitration option	00h	R/W
88~89h	PCI Discard Timer	0000h	R/W

7.1.7. CLOCK CONTROL

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
8Ah	TAGWE# Signal Control	5Ah	R/W
8Bh	Reserved	00h	R/W
8Ch	SDRCLK/SDWCLK Control	2Ah	R/W
8Dh	Reserved	00h	R/W

7.1.8. DISPLAY STATUS

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
8Eh	Integrated VGA Enable & Monochrome Device Adapter Existence Register	00h	R/W

7.1.9. GART AND PAGE TABLE CACHE

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
90~93h	GART Base Address for Re-mapping	00000000h	R/W
94h	Graphic Window Control	00h	R/W
95~96h	Reserved	0	R/W
97h	Page Table Cache Control	00h	R/W
98h	Page Table Cache Invalidation Control	00h	R/W

7.1.10. DRAM PRIORITY TIMER

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
A0~A1h	CPU/PCI-GUI Privilege Timer	0000h	R/W
A2h	CPU/PCI-GUI Privilege Timer Control	00h	R/W
A3h	VGA Grant Timer	00h	R/W

7.1.11. A.G.P. AND HOST BRIDGE

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
C0~C3h	A.G.P. Capability Identify Register	00200002h	RO
C4~C7h	A.G.P. Status Register	1F000203h	RO
C8~CBh	A.G.P. Command Register	00000000h	R/W

7.2. DEVICE 2 (VIRTUAL PCI-TO-PCI BRIDGE)

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
00-01h	Vendor ID	1039h	RO
02-03h	Device ID	0001h	RO
04-05h	PCI Command Register	0000h	RO R/W
06-07h	PCI Status Register	0000h	RO
08h	Revision ID	00h	RO
09h	Programming Interface	00h	RO
0Ah	Sub-Class Code	04h	RO
0Bh	Base Class Code	06h	RO
0Ch	Cache Line Size	00h	RO
0Dh	Master Latency timer	00h	RO
0Eh	Header Type	01h	RO
0Fh	BIST	00h	RO
19h	Secondary Bus Number	00h	R/W
1Ah	Subordinate Bus Number	00h	R/W
1Ch	I/O Base	F0h	R/W RO
1Dh	I/O Limit	00h	R/W RO
1Eh	Secondary PCI-PCI Status	0000h	WC RO
20~21h	Non-prefetchable Memory Base Address	FFF0h	R/W RO
22~23h	Non-prefetchable Memory Limit Address	0000h	R/W RO
24~25h	Prefetchable Memory Base Address	FFF0h	R/W RO
26~27h	Prefetchable Memory Limit Address	0000h	R/W RO
28~3Dh	Reserved	0000h	RO
3Eh	PCI to PCI Bridge Control	0000h	RW RO

7.3. PCI IDE DEVICE

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUE	ACCESS TYPE
00-01h	Vendor ID	1039h	RO
02-03h	Device ID	5513h	RO
04-05h	PCI Command Register	0000h	RO R/W
06-07h	PCI Status Register	0000h	RO
08h	Revision ID	D0h	RO

09h	Programming Interface	00h	RO
0Ah	Sub-Class Code	01h	RO
0Bh	Base Class Code	01h	RO
0Ch	Cache Line Size	00h	RO
0Dh	Master Latency timer	00h	RO
0Eh	Header Type	80h	RO
0Fh	BIST	00h	RO
10h~13h	Primary Channel Command Block Base Address Register	00000000h	R/W
14h~17h	Primary Channel Control Block Base Address Register	00000000h	R/W
18h~1Bh	Secondary Channel Command Block Base Address Register	00000000h	R/W
1Ch~1Fh	Secondary Channel Control Block Base Address Register	00000000h	R/W
20h~23h	Bus Master IDE Control Register Base Address	00000000h	R/W
24h~2Bh	Reserved		
2Ch~2Dh	Subsystem Vendor ID	0000h	R/W
2Eh~2Fh	Subsystem ID	0000h	R/W
30h~33h	Expansion ROM Base Address	00000000h	R/W
40h	IDE Primary Channel/Master Drive Data Recovery Time	00h	R/W
41h	IDE Primary Channel/Master Drive Data Active Time	00h	R/W
42h	IDE Primary Channel/Slave Drive Data Recovery Time	00h	R/W
43h	IDE Primary Channel/Slave Drive Data Active Time	00h	R/W
44h	IDE Secondary Channel/Master Drive Data Recovery Time	00h	R/W
45h	IDE Secondary Channel/Master Drive Data Active Time	00h	R/W
46h	IDE Secondary Channel/Slave Drive Data Recovery Time	00h	R/W
47h	IDE Secondary Channel/Slave Drive Data Active Time	00h	R/W
48h	IDE Status Register	00h	R/W
49h	Reserved		
4Ah	IDE General Control Register 0	00h	R/W
4Bh	IDE General Control Register 1	00h	R/W
4Ch~4Dh	Prefetch Count of Primary Channel	FFFFh	R/W
4Eh~4Fh	Prefetch Count of Secondary Channel	FFFFh	R/W

50h~51h	IDE minimum accessed time register	0000h	R/W
52h	IDE Miscellaneous Control Register	00h	R/W

7.4. REGISTER DESCRIPTIONS

7.4.1. HOST BRIDGE REGISTERS (FUNCTION 0)

7.4.1.1. HOST-TO-PCI BRIDGE CONFIGURATION SPACE HEADER

Register 00h Vendor ID

Default Value: 1039h
Access: Read Only
The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Vendor Identification Number**

Register 02h Device ID

Default Value: 0530h
Access: Read Only
The device identifier is allocated as 0530h by Silicon Integrated Systems Corp.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Device Identification Number**

Register 04h Command

Default Value: 0005h
Access: Read/Write, Read Only
The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.

BIT	ACCESS	DESCRIPTION
15:3	RO	**Reserved**
2	RO	**Bus Master** This bit is read-only and the default value is 1. That means the bus master function of the host bridge can not be disabled.
1	R/W	**Memory Space** The bit controls the response to memory space accesses. When the bit is disabled, the host bridge neglect all accesses from PCI masters. 0: Disable 1: Enable

0	RO	**I/O Space** Default value is 1. The host bridge only respond to the addresses 0CF8h and 0CF9h in I/O space, and the I/O transaction must be generated by the host bridge itself.

Register 06h Status

Default Value: 0210h
Access: Read Only, Write Clear

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

BIT	ACCESS	DESCRIPTION
15:14	RO	**Reserved**
13	WC	**Received Master Abort** This bit is set by SiS530 whenever it terminates a transaction with master abort. This bit is cleared by writing a 1 to it.
12	WC	**Received Target Abort** This bit is set by SiS530 whenever it terminates a transaction with target abort. This bit is cleared by writing a 1 to it.
11	RO	**Reserved**
10:9	RO	**DEVSEL# Timing DEVT** The two bits define the timing to assert DEVSEL#. SiS530 always asserts DEVSEL# within two clocks after the assertion of FRAME#. Default value is DEVT=01.
8:5	RO	**Reserved**
4	RO	**CAP_LIST Bit** The default value is 1 to indicate the configuration space of SiS530 implements new capability mechanism.
3:0	RO	**Reserved**

Register 08h Revision ID

Default Value: 02h
Access: Read Only

The Revision ID is 02h for SiS530 A2 stepping.

BIT	ACCESS	Description
7:0	RO	**Revision Identification Number**

Register 09h Programming Interface

Default Value: 00h
Access: Read Only

The default value is 00h since no specific register-level programming interface is provided.

BIT	ACCESS	DESCRIPTION

7:0	RO	**Programming Interface**

Register 0Ah Sub Class Code

Default Value: 00h
Access: Read Only
The Sub Class Code is 00h for host bridge.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Sub Class Code**

Register 0Bh Base Class Code

Default Value: 06h
Access: Read Only
The value of 06h in this field identifies a bridge device.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Base Class Code**

Register 0Ch Cache Line Size

Default Value: 00h
Access: Read Only
The value of this register is always 00h since the host bridge would not generate the Memory Write and Invalidate command.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Cache Line Size**

Register 0Dh Master Latency Timer (MLT)

Default Value: FFh
Access: Read/Write
The MLT is used in conjunction with PGT(Register 84h) and CIT(Register 86h) to provide a fair and efficient system arbitration mechanism. The value of MLT guarantees the minimum system bandwidth for CPU when both CPU and PCI masters are all craving for system resources(system memory or PCI bus).

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Initial Value for Master Latency Timer** Power-on default value is FFh but it is recommended to set its value to 20h. Unit: PCI clock

Register 0Eh Header Type

Default Value: 80h
Access: Read Only
The value of 80h implies that SiS530 is a multiple function device.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Header Type**

Register 0Fh BIST

Default Value: 00h
Access: Read Only
The value is 00h since SiS530 do not support Build-in Self Test.

BIT	ACCESS	DESCRIPTION
7:0	RO	**BIST**

Register 10h Graphic Window Base Address (GWBA)

Default Value: 00000000h
Access: Read/Write, Read Only
The register defines the starting address of the graphic window for integrated 3D VGA controller. Accessibility and effectiveness of this register is controlled by the Graphic Window Control Register(Register 94h).

BIT	ACCESS	DESCRIPTION
31:22	R/W RO	**Define A[31:22] of Graphic window base address** The accessibility of this bits[31:22] are controlled by graphic window size(Bits[6:4], Register 94h).
21:0	RO	**Reserved and read as zeroes.**

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Size
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	4M
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	8M
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	16M
R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	32M
R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	0	64M
R/W	R/W	R/W	R/W	R/W	0	0	0	0	0	128M
R/W	R/W	R/W	R/W	0	0	0	0	0	0	256M

Register 34h Capability Pointer (CAPPTR)

Default Value: C0h
Access: Read Only
The value of C0h indicates that the A.G.P. bus standard register block is started from Register C0h.

BIT	ACCESS	Description
7:0	RO	**Capability Pointer** Pointer to the Start of A.G.P. bus standard register block.

7.4.1.2. HOST/L2 CACHE/DRAM CONTROL REGISTER

Register 50h NA Control

Default Value: 00h
Access: Read/Write
The register controls when and how the SiS530 assert NA# to CPU for allowing address/data pipelining on the host bus.

BIT	ACCESS	DESCRIPTION

7	R/W	**NA# assert Control** When this bit is disabled, SiS530 would not assert NA# under any circumstance. When this bit is enabled, SiS530 asserts NA# for all burst read cycles and I/O cycles. However, I/O address 0CF8h and 0CFCh are the only exceptions and SiS530 would not asserts NA# for these I/O cycles. Bits[6:4] control how and when SiS530 asserts NA# if this bit is enabled. 0: Disable 1: Enable
6	R/W	**Memory Single Write Cycle NA#** When this bit is enabled, SiS530 asserts NA# for all memory single write cycles regardless of the destination of the cycles. When this bit is disabled, SiS530 would not respond NA# to CPU for all single memory write cycles. 0: Disable 1: Enable
5	R/W	**NA# Timing for L2 Cache-hit Burst Cycle** This bit controls when SiS530 asserts NA# for L2 cache-hit burst cycles. When this bit is "0", SiS530 asserts NA# and the 1st BRDY# for the burst read cycle exactly at the same time. When this bit is "1", SiS530 asserts NA# one clock after the 1st BRDY# is returned to CPU. It is recommended to set this bit to "1" if there are two banks of PB SRAM in the system. 0: Normal 1: Delay 1 CPU clock
4	R/W	**I/O Cycle NA#** When this bit is enabled, SiS530 asserts NA# for all I/O cycles. When this bit is disabled, SiS530 would not respond NA# to CPU for all I/O cycles. 0: Disable 1: Enable
3:0	R/W	**Reserved**

Register 51h L2 Cache Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**L2 Cache Enable** When no L2 exists, this bit should be programmed to "0". 0: Disable 1: Enable

6	R/W	**BRDY# Timing for L2 Cache-hit Cycle** When this bit is set to 0, SiS530 asserts BRDY# at 3T after sampling ADS# if it is cache-hit cycle. When this bit is set to 1, SiS530 asserts BRDY# at 4T, delay 1T, after sampling ADS# when cache-hit cycles. It is recommended to set this bit to "1" when it is needed another one clock for TAG RAM output and decoding. 0: Normal 1: Delay 1 CPU clock
5:4	R/W	**L2 Cache Size** The register specifies the L2 cache size of the system. **Bits[5:4]** — **Size** 00 — 256K 01 — 512K 10 — 1M 11 — 2M
3	R/W	**L2 Cache WT/WB Policy** The register specifies the coherence policy for L2 cache and system DRAM. This bit must set to 0 when BIOS is sizing the L2 cache. This bit can be set to "1" to support L2 cache in write back mode once L2 cache sizing mode is finished. 0: Write Through Mode 1: Write Back Mode
2	R/W	**L2 Cache Burst Addressing Mode** This bit specifies the addressing mode of CPU burst cycles. The linear mode is used for Cyrix CPU. 0: Toggle Mode 1: Linear Mode
1	R/W	**Reserved**
0	R/W	**L2 Cache Sizing Mode** SiS530 enters its L2 cache sizing mode when this bit is set to 1. In the sizing mode, TAG addresses are neglected and all accesses to system memory are treated as L2 cache hit cycles. This bit should be set to 0 after the L2 cache sizing procedure has finished. 0: Disable 1: Enable

Register 52h L2 Cache/DRAM Function Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION

7	R/W	**DRAM Read Lead-off Time Delay Control for Synchronous Mode** 0: Normal 1: Slower 1 CPU clock
6	R/W	**Single Read Allocation (L2 Update) Control** When this bit is enabled, any memory single read cycle will cause the corresponding memory line to be updated to L2 cache. 0: Disable 1: Enable
5	R/W	**Graphic Window Address Decoding Timing** This bit controls the decoding time for page table cache when accessing Graphic Window by CPU/integrated 3D VGA controller. 0: 1 DRAM clock 1: 2 DRAM clocks
4	R/W	**Asynchronous/Synchronous Mode between CPU/DRAM Clock** This bit can only be set to "1" when the frequency of CPU clock and the frequency of DRAM clock are the same and the skew between these two clocks should be zero. 0: Asynchronous Mode 1: Synchronous Mode
3:0	R/W	**Reserved**

Register 53~54h Reserved

Register 55h DRAM Bank Open/Close Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Implemented DRAM Bank Open/Close Control** **Bits[7:6]** — **Delay** 00 — 1 DRAM clock 01 — 2 DRAM clocks 10 — 3 DRAM clocks 11 — 5 DRAM clocks
5:4	R/W	**Reserved**
3	R/W	**Reserved bit for Write DRAM Cycles** 0: Disable 1: Enable
2	R/W	**Reserved bit for Data Read DRAM Cycles** 0: Disable 1: Enable
1	R/W	**Reserved bit for Code Read DRAM Cycles** 0: Disable 1: Enable

0	R/W	**Reserved bit for Graphics Windows Range Access** 0: Disable 1: Enable

Register 56h Refresh Control

Default Value: 00h
Access: Read/Write
This register controls the characteristics of DRAM refresh operation.

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Refresh command to Refresh/Active Command Delay** **Bits[7:6]** — **Description** 00 — 9 DRAM clocks 01 — 8 DRAM clocks 10 — 7 DRAM clocks 11 — 6 DRAM clocks
5:4	R/W	**Refresh Queue Depth** Bits[5:4] controls the depth of refresh queue. To minimize the performance penalty caused by refresh cycles, the concept of refresh queue is introduced. Refresh request is arbitrated with other DRAM request. If a refresh request does not get served, it enters the refresh queue. The priority of refresh request is promoted to highest when the refresh queue is full. **Bits[5:4]** — **Depth** 00 — 0 01 — 4 10 — 8 11 — 12
3:2	R/W	**Refresh Rate Control** **Bits[3:2]** — **Rate** 00 — 15.6 us 01 — 7.8 us 10 — 3.9 us 11 — Reserved
1	R/W	**DRAM Refresh Enable** 0: Disable 1: Enable
0	R/W	**DRAM Refresh Test Mode** For internal test only, please program this bit with 0. 0: Normal Mode 1: Test Mode

Register 57h Reserved

Register 58h DRAM Control

Default Value: 50h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**RAS Precharge time** **Bits[7:6]** — **Description** 00 — 2 DRAM clocks 01 — 3 DRAM clocks (default) 10 — 4 DRAM clocks 11 — 5 DRAM clocks
5:4	R/W	**RAS to CAS Delay** **Bits[5:4]** — **Description** 00 — 2 DRAM clocks 01 — 3 DRAM clocks (default) 10 — 4 DRAM clocks 11 — 5 DRAM clocks
3:0	R/W	**Reserved**

Register 59~5Bh Reserved

Register 5Ch DRAM Initialization Command

Default Value: 00h

Access: Read/Write

This register controls DRAM initialization process. Writing this register may cause SiS530 to issue initialization command to DRAM directly.

BIT	ACCESS	DESCRIPTION
7	R/W	**Precharge Command** Write 1 to this bit causes SiS530 to issue precharge command to DRAM. This bit is automatically cleared after the precharge command completed.
6	R/W	**Mode Register Set Command** Write 1 to this bit causes SiS530 to issue mode setting command to DRAM. This bit is automatically cleared after the command completed.
5	R/W	**DRAM Refresh Command** Write 1 to this bit causes SiS530 to issue refresh command to DRAM. This bit is automatically cleared after the command completed.
4	R/W	**DRAM Initialization Mode Selection** This bit controls whether the command specified in Bits[7:5] of this register should be issued to one row only or to all rows. If the value of this bit is 0, the DRAM Status Register(Register 63h) controls which row the command should be issued to. 0: One Row 1: All Rows

3	R/W	**DRAM NOP Command** Write 1 to this bit causes SiS530 to issue NOP command to DRAM. This bit is automatically cleared after the command completed.
2:0	R/W	**Reserved**

Register 5Dh DRAM Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	Description
7:5	R/W	**Reserved**
4	R/W	**DRAM Write Retire Rate** 0: X-2-2-2 1: X-1-1-1
3	R/W	**CAS# Latency** 0: 2 DRAM clocks 1: 3 DRAM clocks
2:0	R/W	**Reserved**

Register 5Eh DRAM Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Reserved**
6	R/W	**DRAM Optimal RAS Precharge Time Control** When the value of this bit is 1, SiS530 checks whether the consecutive cycles toward DRAM are destining to the same row or not to optimize the RAS precharge time. If the cycles are destining to the same row, the minimum RAS# precharge time for DRAM must be met before issuing a row active command. However, if they are destining to the different row, the RAS precharge time is met automatically. So, row active command can be issued immediately. When this function is disabled, SiS530 does not use the information about the destinations of consecutive cycles to optimize RAS precharge time. There is no timing difference RAS regardless whether the cycles are destining to same or different row. 0: Disable 1: Enable
5:0	R/W	**Reserved**

Register 5Fh Reserved

Register 60/61/62h DRAM Types of Bank 0/1/2

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Reserved**
5	R/W	**Double/Single Sided DRAM** 0: Single Sided 1: Double Sided
4	R/W	**Reserved**
3:0	R/W	**DRAM Type Selection** **Bit [3:0] DRAM Type** / **Bit [3:0] DRAM Type** 0000: 1x11x8(1M) / 1000: 1x11x10 (4M) 0001: 1x13x8 (4M) / 1001: 1x13x10 (16M) 0010: 2x12x8 (4M) / 1010: 2x12x10 (16M) 0011: 2x13x8(8M) / 1011: 2x13x10(32M) 0100: 1x11x9 (2M) / 1100: 2x11x8 (2M) 0101: 1x13x9 (8M) / Others: Reserved 0110: 2x12x9 (8M) 0111: 2x13x9(16M)

Register 63h DRAM Status Register

Default Value: 00h

Access: Read/Write

This register is used to specify which DRAM banks are plugged with DRAM.

BIT	ACCESS	DESCRIPTION
7	R/W	**Reserved**
6	R/W	**Share Memory Architecture Control** 0: Disable (Local Frame Buffer) 1: Enable (Share Frame Buffer) System BIOS must read the status bit of VGA register that depended on the H/W trapping on MD48 then to set this bit for shared frame buffer or local frame buffer.
5:4	R/W	**Share Memory Size** **Bit[5:4] Share Memory Size** 00 Reserved 01 2M 10 4M 11 8M
3	R/W	**Reserved**
2	R/W	**DRAM Status for Bank2** 0: Absent 1: Installed

1	R/W	**DRAM Status for Bank1** 0: Absent 1: Installed
0	R/W	**DRAM Status for Bank0** 0: Absent 1: Installed

7.4.1.3. CURRENT DRIVING CONTROL REGISTER

Register 64h DRAM Signals Driving Current Control

Default Value: 00h
Access: Read/Write
This 8-bit register controls the buffer strengths of DRAM related signals.

BIT	ACCESS	DESCRIPTION
7	R/W	**CS[5:0]# Current Rating** 0: Weak 1: Strong
6	R/W	**DQM[7:0] Current Rating** 0: Weak 1: Strong
5	R/W	**MA[14:0] Current Rating** 0: Weak 1: Strong
4	R/W	**RAMW# Current Rating** 0: Weak 1: Strong
3	R/W	**SRAS#/SCAS# Current Rating** 0: Weak 1: Strong
2	R/W	**CKE[5:0]# Current Rating** 0: Weak 1: Strong
1	R/W	**MD[63:0] Current Rating** 0: Weak 1: Strong
0	R/W	**Reserved**

Register 65h PCI Signals Driving Current Control

Default Value: 00h
Access: Read/Write
This 8-bit register controls the buffer strengths of the signals located on PCI bus.

BIT	ACCESS	DESCRIPTION
7:2	R/W	**Reserved**

1	R/W	**AD[31:0] Current Rating** This bit controls the buffer strength of AD[31:0] on PCI bus. 0: 4mA 1: 8mA
0	R/W	**PCI Control Signal Current Rating** This bit specifies the current rating of FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, C/BE[3:0]# and PGNT[3:0]#. 0: 4mA 1: 8mA

7.4.1.4. POWER MANAGEMENT CONTROL REGISTER

Register 68h SMRAM Access Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**SMRAM Area Re-mapping Control** This field controls how the address on the host bus is mapped to the system memory address when the SMRAM access control bit is enabled or CPU is in the system management mode. **Bits[7:6]** **Host Address** **System Memory Address** 00 E0000h~E7FFFh E0000h~E7FFFh 01 E0000h~E7FFFh A0000h~A7FFFh 10 E0000h~E7FFFh B0000h~B7FFFh 11 A0000h~AFFFFh A0000h~AFFFFh
5	R/W	**Reserved**
4	R/W	**SMRAM Access Control** When the bit is enabled, SMRAM area can be used even when SMIACT# is not asserted. If the bit is disabled, SMRAM area can only be accessed during the SMI handler. 0: Disable 1: Enable
3:0	R/W	**Reserved**

Register 69h System Event Monitor Control for Power Management

Default Value: 00h
Access: Read/Write

This register controls what kinds of events on internal host VGA bus should be reported to the SiS5595 through the pin BM_REQ# for power management matter.

BIT	ACCESS	DESCRIPTION

7	R/W	**Monitoring internal host VGA bus I/O Access** When this bit is enabled, any I/O access from CPU to internal host VGA bus will be reported to the SiS5595 via BM_REQ# if the address of the cycle is within the range of base address register. 0: Disable 1: Enable
6	R/W	**Monitoring internal host VGA bus Non-prefetchable Memory Access** When this bit is enabled, any memory access from CPU to internal host VGA bus non-prefetchable memory area will be reported to SiS5595 via BM_REQ#. 0: Disable 1: Enable
5	R/W	**Monitoring internal host VGA bus Prefetchable Memory Access** When this bit is enabled, any memory access from CPU to internal host VGA bus prefetchable memory area will be reported to SiS5595 via BM_REQ#. 0: Disable 1: Enable
4	R/W	**Monitoring VGA Compatible I/O Access toward internal host VGA bus** When this bit is enabled, any VGA compatible I/O access (3B0h ~ 3BBh, 3C0 ~ 3DFh) toward internal host VGA bus will be reported to SiS5595 via BM_REQ#. 0: Disable 1: Enable
3	R/W	**Monitoring VGA Compatible Memory Access toward internal host VGA bus** When this bit is enabled, any VGA compatible memory access (A0000h ~ BFFFFh) toward internal host VGA bus will be reported to SiS5595 via BM_REQ#. 0: Disable 1: Enable
2	R/W	**Monitoring A.G.P. Bus Master Activity** When this bit is enabled, internal A.G.P. bus master activity will be reported to SiS5595 via BM_REQ#. 0: Disable 1: Enable
1:0	R/W	**Reserved**

Register 6Ah~6Bh ACPI I/O Space Base Address Register

Default Value: 00000000h

Access: Read/Write

The register specifies the ACPI I/O space base address, and SiS530 may monitor ACPI I/O accesses if the validity bit of this register is set to 1.

BIT	ACCESS	DESCRIPTION
15:5	R/W	**A[15:5] for ACPI I/O Space Base Address** This register provides A[15:5] for the start address of the ACPI I/O space.
4:1	R/W	**Reserved**
0	R/W	**Validity** If this bit is set to 1, the base address contained in Bit[15:5] is valid. Otherwise the base address defined in Bit[15:5] is ignored. 0: Invalid 1: Valid

Register 6Ch DRAM Self-Refresh Control for Power Management

Default Value: 00h
Access: Read/Write
This register controls in what degree that SiS530 support ACPI function and also controls the behavior of CKE.

BIT	ACCESS	DESCRIPTION
7	R/W	**ACPI S3 State Support** 0: Disable 1: Enable
6	R/W	**ACPI S2 State Support** 0: Disable 1: Enable
5	R/W	**CKE Output Enable Control** When this bit is enabled, SiS530 drives CKE. When this bit is disable, SiS530 floats its CKE output. 0: Disable 1: Enable
4	R/W	**CKE Selection** When the value of this bit is 1, SiS530 always drives CKE to low provided CKE Output Enable Control bit is enabled. When the value of this bit is 0, SiS530 drives CKE to low only when it entered self-refresh mode (S2 or S3 state and stop grant cycle issued). 0: Normal Mode 1: Force Low
3:0	R/W	Reserved

7.4.1.5. SHADOW RAM & NON-CACHEABLE AREA CONTROL REGISTER

Register 70h to register 76h define the attribute of the Shadow RAM from 640 KBytes to 1 MBytes. All of the registers 70h to 75h are defined as below, and each register defines the corresponding memory segment's attribute which are listed in the following table.

REGISTER	DEFINED RANGE	REGISTER	DEFINED RANGE
Register 70h bits 7:5	0C0000h-0C3FFFh	Register 73h bits 7:5	0D8000h-0DBFFFh

Register 70h bits 3:1	0C4000h-0C7FFFh	Register 73h bits 3:1	0DC000h-0DFFFFh
Register 71h bits 7:5	0C8000h-0CBFFFh	Register 74h bits 7:5	0E0000h-0E3FFFh
Register 71h bits 3:1	0CC000h-0CFFFFh	Register 74h bits 3:1	0E4000h-0E7FFFh
Register 72h bits 7:5	0D0000h-0D3FFFh	Register 75h bits 7:5	0E8000h-0EBFFFh
Register 72h bits 3:1	0D4000h-0D7FFFh	Register 75h bits 3:1	0EC000h-0EFFFFh

Register 70/ 71/ 72/ 73/ 74/ 75h Shadow RAM Registers

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Read enable**
6	R/W	**L1/L2 cacheable**
5	R/W	**Write enable**
4	R/W	**Reserved**
3	R/W	**Read enable**
2	R/W	**L1/L2 cacheable**
1	R/W	**Write enable**
0	R/W	**Reserved**

Register 76h Attribute of Shadow RAM for BIOS Area

Default Value: 00h
Access: Read/Write

The 8-bit register controls the access of shadow RAM on BIOS area (F0000h~FFFFFh). When a bit is enabled, the type of the access defined by the bit is allowed.

BIT	ACCESS	DESCRIPTION
7	R/W	**Read Control** When this bit is enabled, any read access for BIOS shadow RAM area is forwarded to system memory. 0: Disable 1: Enable
6	R/W	**Cacheable Control** This bit controls the cacheability for BIOS shadow RAM area 0: Disable 1: Enable
5	R/W	**Write Control** When this bit is enabled, any write access for BIOS shadow RAM area is forwarded to system memory. 0: Disable 1: Enable
4	R/W	**Reserved**

3	R/W	**Shadow RAM enable for PCI access** When this bit is enabled, accesses from PCI masters toward shadow RAM area is allowed. 0: Disable 1: Enable
2:0	R/W	**Reserved**

Register 77h Characteristics of Non-cacheable Area

Default Value: 00h
Access: Read/Write
This register controls the characteristics of the non-cacheable areas defined in Register78h and Register 7Ah.

BIT	ACCESS	DESCRIPTION
7:4	R/W	**Reserved**
3	R/W	**Location of Non-cacheable Area I** This bit specifies whether the non-cacheable area I is located on system memory or PCI bus. 0: System Memory 1: PCI Bus.
2	R/W	**Non-cacheable Area I Enable Control** This bit controls whether the address and size specified on Register 78h are valid or not. When this bit is enable, the range defined by Register 78h is non-cacheable. 0: Disable 1: Enable
1	R/W	**Location of Non-cacheable Area II** This bit specifies whether the non-cacheable area II is located on system memory or PCI bus. 0: System Memory 1: PCI Bus.
0	R/W	**Non-cacheable Area II Enable Control** This bit controls whether the address and size specified on Register 7Ah are valid or not. When this bit is enable, the range defined by Register 7Ah is non-cacheable. 0: Disable 1: Enable

Register 78h~79h Allocation of Non-Cacheable Area I

Default Value: 0000h
Access: Read/Write
This register defines the size and the base address of the first non-cacheable area.

BIT	ACCESS	DESCRIPTION

15:13	R/W	**Size of Non-cacheable Area I** **Bits[15:13]** — **Size** 000 — 64KB 001 — 128KB 010 — 256KB 011 — 512KB 100 — 1MB 101 — 2MB 110 — 4MB 111 — 8MB
12:0	R/W	**Base Address of Non-cacheable Area I** This field specifies A[28:16] for the base address of the non-cacheable area I. The upper 3 bits of the base address are always regarded as zeros.

Register 7Ah~7Bh Allocation of Non-cacheable Area II

Default Value: 0000h
Access: Read/Write
This register defines the size and the base address of the second non-cacheable area.

BIT	ACCESS	DESCRIPTION
15:13	R/W	**Size of Non-cacheable Area II** **Bits[15:13]** — **Size** 000 — 64KB 001 — 128KB 010 — 256KB 011 — 512KB 100 — 1MB 101 — 2MB 110 — 4MB 111 — 8MB
12:0	R/W	**Base Address of Non-cacheable Area II** This field specifies A[28:16] for the base address of the non-cacheable area II. The upper 3 bits of the base address are always regarded as zeros.

7.4.1.6. PCI BRIDGE AND PCI ARBITER CONTROL REGISTER

Register 80h Target Bridge to DRAM Characteristics

Default Value: 00h
Access: Read/Write
The 8-bit register controls the characteristics of PCI-to-DRAM bridge.

BIT	ACCESS	DESCRIPTION

7:5	R/W	**Address Boundary Alignment for PCI Bursting** This field controls the alignment of address boundaries. For SiS530, a master-generated PCI burst cycle can never across any address boundary defined by this field. If a cycle is trying to across an address boundary for a memory burst transaction, SiS530 will terminate this transaction with disconnect immediately. **Bits[7:5]** — **Boundary Alignment** 000 — 256 Bytes 001 — 512 Bytes 010 — 1 KBytes 011 — 2 Kbytes 100 — 4 KBytes Others — Reserved
4:0	R/W	**Reserved**

Register 81h PCI Target Bridge Characteristics

Default Value: 00h
Access: Read/Write
This register controls the characteristics for PCI target bridge.

BIT	ACCESS	DESCRIPTION
7	R/W	**Improved Snoop Function Control for Write cycle** This bit controls whether or not the PCI target bridge does improve snoop function for write cycles. 0: Disable 1: Enable
6	R/W	**Improved Snoop Function Control for Read Cycle** This bit controls whether or not the PCI target bridge does improves snoop function for read cycles. 0: Disable 1: Enable
5	R/W	**Reserved**
4	R/W	**DRAM Request Control** This bit controls when to issue the DRAM request for accessing memory. 0: After hold CPU 1: After PCI command is received
3	R/W	**Timing of Writing L2** 0: 2-2-2.. 1: 3-3-3..
2:0	R/W	**Reserved**

Register 82h PCI Target Bridge Bus Characteristics

Default Value: 00h
Access: Read/Write

This register controls the characteristics for 33Mhz PCI target bridge.

BIT	ACCESS	DESCRIPTION
7	R/W	**PCI Peer Concurrency** When this bit is enabled, CPU to L2/DRAM accesses are allowed to perform concurrently with PCI-to-PCI accesses. 0: Disable 1: Enable
6	R/W	**Prefetch Buffer Control** When this bit is set to 1, SiS530 asserts its first TRDY# for a transaction after it prefetched 1quadword of data from system memory. Otherwise, SiS530 asserts its first TRDY# after 2 quadwords are prefetched. 0: Assert TRDY# after prefetching 2 Qws 1: Assert TRDY# after prefetching 1 Qws
5	R/W	**Reserved**
4	R/W	**Memory Read Command Prefetch Control** This bit controls whether or not SiS530 prefetch data for memory read command. Please note that Memory Read Multiple and Memory Read Line commands always do prefetch. The semantic of this bit is different to others. The value of 0 means enable for this bit. 0: Enable 1: Disable
3:2	R/W	**Initial Latency Control** This field controls the target initial latency of the PCI target bridge. If SiS530 is unable to assert TRDY# for a transaction within the target initial latency defined by this field, SiS530 asserts STOP# to retry this cycle. 00: Disable 01: 16 PCI Clocks 10: 24 PCI Clocks 11: 32 PCI Clocks
1	R/W	**Subsequent Latency Control** When this bit is enabled, SiS530 terminates a transaction with STOP# if it fails to assert TRDY# for the subsequent block within 8 clocks. 0: Disable 1: Enable
0	R/W	**Address Decoding Time Extension Control** This bit controls the decoding time for deciding whether the PCI transaction is destining to the system memory or not. 0: 1 CPU Clocks 1: 2 CPU Clocks

Register 83h CPU to PCI Characteristics

Default Value: 00h

Access: Read/Write

This register controls miscellaneous functions supported by the CPU-to-PCI bridge of SiS530. The setting of this register may affect PCI performance in various degree.

BIT	ACCESS	DESCRIPTION
7:2	R/W	**Reserved**
1	R/W	**Memory Burst Control** This bit controls whether or not the host bridge generates memory burst cycles. 0: Disable 1: Enable
0	R/W	**Memory Post Write Control** When this bit is enable, all CPU to PCI memory write cycles are posted. 0: Disable 1: Enable

Register 84h PCI Grant Timer

Default Value: FFFFh

Access: Read/Write

The timer is used to prevent PCI masters from seizing the PCI bus too long. When the timer expired, PCI arbiter forces the master that is currently occupying PCI bus to relinquish PCI bus by removing its grant.

BIT	ACCESS	DESCRIPTION
15:0	R/W	**PCI Grant Timer** The setting of this register should consider the overall system configuration and the value of MLT(Register 1Dh). For a system that has many PCI master devices, the value should be higher. For a system with fewer master devices, the value should be smaller. Typical value of this timer is 60h if MLT is set to 20h. Unit: PCI clock

Register 86h CPU Idle Timer for PCI

Default Value: FFh

Access: Read/Write

The timer is used to prevent CPU from idling too long while outstanding PCI requests cannot be served.

BIT	ACCESS	DESCRIPTION
7:0	R/W	**CPU Idle Timer** Recommended value for this timer is 03h. Unit: PCI clock

Register 87h CPU to PCI Characteristics and Arbitration Option

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION

7	R/W	**Reserved**
6	R/W	**CPU Involved Arbitration on PCI** PGT(Register 84h), CIT(Register 86h) and MLT(Register 0Dh) can only take effect when this bit is enable. When this bit is enable, SiS530 does not block CPU from operation longer than the period defined by PGT to serve PCI masters, and minimum access time for CPU is guaranteed by MLT. 0: Disable 1: Enable
5	R/W	**Reserved**
4	R/W	**PCI Grant Timer Testing Mode** For internal usage only, please program this bit with 0. 0: Disable 1: Enable
3	R/W	**64-bit Access Retry Behavior Control** When the value of this bit is 0 and the second half non-post PCI cycle(or the second data phase) of a 64-bit access is retried by a PCI target, SiS530 tries to issue the second half cycle again and again until it completes successfully on PCI bus. When this bit is set to 1, retry for any non-post cycle issued by the host bridge results in the assertion of BOFF#. It is recommended to set this bit to 0. 0: Continue Retry 1: Back-Off CPU
2	R/W	**Lock Control** When this bit is enabled, a 64-bit memory read cycle from CPU toward 33Mhz PCI bus is converted into locked PCI memory read cycles. 0: Disable 1: Enable
1:0	R/W	**Reserved**

Register 88h CPU Discard Timer

Default Value: 0000h
Access: Read/Write

The timer is used to keep PCI hold when PCI read is retried due to the CPU-to-PCI post write FIFO is not empty.

BIT	ACCESS	DESCRIPTION
15:0	R/W	**Initial Value of CPU Discard Timer**

7.4.1.7. CLOCK CONTROL REGISTER

Register 8Ah TAGWE# Signal Control Register

Default Value: 5Ah
Access: Read/Write

In order to issue NA# for memory single write, SiS530 generates TAGWE# signal a little ahead of normal CPU clock. Besides, SiS530 also provide a set of register to adjust the pulse width of signal TAGWE#.

BIT	ACCESS	DESCRIPTION
7:4	R/W	**TAGWE Pulse Width** **Bit[7:4] Descriptions Bit[7:4] Descriptions** 1111 T/2+8.0ns 0111 T/2+4.0ns 1110 T/2+7.5ns 0110 T/2+3.5ns 1101 T/2+7.0ns ***0101*** ***T/2+3.0ns*** 1100 T/2+6.5ns 0100 T/2+2.5ns 1011 T/2+6.0ns 0011 T/2+2.0ns 1010 T/2+5.5ns 0010 T/2+1.5ns 1001 T/2+5.0ns 0001 T/2+1.0ns 1000 T/2+4.5ns 0000 T/2+0.5ns Where T is CPU clock.
3:0	R/W	**TAGWCLK Control** This field controls the phase of TAGWCLK that ahead of CPUCLK. **Bit[3:0] Descriptions Bit[3:0] Descriptions** 1111 -2.0ns 0111 +2.0ns 1110 -1.5ns 0110 +2.5ns 1101 -1.0ns 0101 +3.0ns 1100 -0.5ns 0100 +3.5ns 1011 +0.0ns 0011 +4.0ns ***1010*** ***+0.5ns*** 0010 +4.5ns 1001 +1.0ns 0001 +5.0ns 1000 +1.5ns 0000 +5.5ns

Register 8Bh Reserved

Register 8Ch SDRCLK/SDWCLK Control Register

Default Value: 1Ah

Access: Read/Write

In order to improve the setup time of MD for read/write DRAM, SiS530 introduces two internal clocks, SDRCLK and SDWCLK, that have some phase difference from SDCLK, which is the clock that applies to SDRAM. Adjusting these two clocks lets the target have more setup time budget. However, it decreases the hold time.

BIT	ACCESS	DESCRIPTION

7:4	R/W	**SDRCLK Control** This field controls the phase of SDRCLK that behind after SDCLK. **Bit[7:4]** **Descriptions** **Bit[7:4]** **Descriptions** 1111 +6.0ns 0111 +2.0ns 1110 +5.5ns 0110 +1.5ns 1101 +5.0ns 0101 +1.0s 1100 +4.5ns 0100 +0.5ns 1011 +4.0ns 0011 +0.0ns 1010 +3.5ns 0010 **-0.5ns** 1001 +3.0ns 0001 - 1.0ns 1000 +2.5ns 0000 - 1.5ns
3:0	R/W	**SDWCLK Control** This field controls the phase of SDWCLK that ahead of SDCLK. **Bit[3:0]** **Descriptions** **Bit[3:0]** **Descriptions** 1111 -2.5ns 0111 +1.5ns 1110 -2.0ns 0110 +2.0ns 1101 -1.5ns 0101 +2.5ns 1100 -2.0ns 0100 +3.0ns 1011 -0.5ns 0011 +3.5ns ***1010*** ***+0.0ns*** 0010 +4.0ns 1001 +0.5ns 0001 +4.5ns 1000 +1.0ns 0000 +5.0ns

Register 8Dh Reserved

7.4.1.8. DISPLAY STATUS REGISTER

Register 8Eh Integrated VGA Enable & Monochrome Device Adapter (MDA) Existence Register

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:1	R/W	**Reserved**
0	R/W	**Monochrome Device Adapter (MDA) Existence Register** 0: Not exist 1: Exist

7.4.1.9. GART AND PAGE TABLE CACHE CONTROL REGISTER

Register 90h GART Base Address

Default Value: 00000000h
Access: Read/Write

This register specifies the starting address of the Graphics Address Re-mapping Table. The Re-mapping table is resided in system memory and it translates graphic address into the system memory address.

BIT	ACCESS	DESCRIPTION
31:12	R/W	**A[31:12] for GART Base Address** This register provides the starting address of the Graphics Address Re-mapping Table which is always located in system memory. Please note that although there is no register that directly specifies the size of GART, the size of GART can still be known via graphic window size(Bits[6:4] of Register 94h) (Please note that the address provided via GART Base is 4KB aligned)
11:0	R/W	**Reserved**

Register 94h Graphic Window Control

Default Value: 00h

Access: Read/Write

This register specified the size of the graphic window and indicates that whether the Graphic Window Base Address Register and Re-mapping GART Base Address Register contain valid information or not.

BIT	ACCESS	DESCRIPTION
7	R/W	**Reserved**
6:4	R/W	**Graphic Window Size** This field defines the size of the graphic window. The accessibility of GWBA register (Register 10h) is also controlled by this field. **Bits[6:4]** — **Size** 000 — 4Mbyte 001 — 8Mbyte 010 — 16Mbyte 011 — 32Mbyte 100 — 64Mbyte 101 — 128Mbyte 110 — 256Mbyte 111 — Reserved
3:2	R/W	**Reserved**
1	R/W	**Graphic Window Base Address Validity** The value of "1¡ for this bit indicates that the Graphic Window Base Address specified in GWBA Register(Register 10h) is valid. Otherwise, the address specified in GWBA Register is invalid. 0: Invalid 1: Valid
0	R/W	**GART Base Address Validity** The value of "1¡ for this bit indicates that the GART Base Address specified in Register 90h is valid. Otherwise, the address specified in Register 90h is invalid. 0: Invalid 1: Valid

Register 97h Page Table Cache Control

Default Value: 00h
Access: Read/Write

Page Table Cache is used to speedup the address translation process from graphic address to system memory address. It stores recently used GART entries in the core logic to prevent traffics toward system memory during address translation process. This register controls the characteristic of the page table cache and the address translation mechanism.

BIT	ACCESS	DESCRIPTION
7:3	R/W	**Reserved**
2	R/W	**Page Table Cache Invalidation Control** This bit controls in what mean that SiS530 avoids to use stalled page table cache. When the value of this bit is 0, SiS530 automatically detects write accesses toward all GART entries and it invalidates the entire page table cache immediately once it observed such an event. When the value of this bit is 1, aids from software must be provided to prevent SiS530 from using stalled page table cache entries. Mini-port driver must write Page Table Cache Invalidation Control Register(Register 98h Bit1) when new re-mapping information is updated to GART. 0: Detect writing GART entry 1: Write Configuration Register 98h Bit1
1	R/W	**Reserved**
0	R/W	**Page Table Cache Enable** When this bit is enabled, page table cache will be used for accelerating the address translation process. When this bit is disable, no GART entries are cached into the page table cache and any address translation is done after getting the GART entry by a memory read. 0: Disable 1: Enable

Register 98h Page Table Cache Invalidation Control

Default Value: 00h
Access: Read/Write

The register controls the invalidation of page table cache.

BIT	ACCESS	DESCRIPTION
7:2	R/W	**Reserved**
1	R/W	**Invalidate Whole Page Table Cache** Invalidate whole page table cache entries when write 1 to this bit. This bit is cleared after the invalidation process completed.
0	R/W	**Reserved**

7.4.1.10. DRAM PRIORITY TIMER CONTROL REGISTER

Register A0h CPU/PCI-GUI Privilege Timer

Default Value: 0000h
Access: Read/Write

SiS530 maintains the privilege of DRAM usage between CPU/PCI and GUI. When both CPU/PCI and GUI are craving for the resource of system memory, this set of timers provides the adjustment of DRAM bandwidth between these two agents. The operation of the set of timers is explained below.

If GUI data transfer has higher privilege over CPU/PCI, GUI high privilege timer decreases every clock when GUI access toward system memory is undergoing. If CPU/PCI privilege is higher than GUI, CPU/PCI high privilege timer decreases every clock when CPU/PCI accesses system memory. The privilege relationship between CPU/PCI and GUI is exchanged after the timer expired. CPU/PCI accesses do not affect any one of these two timers if CPU/PCI does not have higher privilege than GUI. In the same way, GUI low priority accesses do not affect timers if GUI device does not have higher privilege than CPU/PCI.

BIT	ACCESS	DESCRIPTION
15:8	R/W	**Initial Value for GUI High Privilege Timer** The timer controls how long GUI data transfer has higher privilege over CPU/PCI for DRAM accesses. Unit: DRAM clock * 4
7:0	R/W	**Initial Value for CPU/PCI High Privilege Timer** The timer controls how long the CPU/PCI has higher privilege over GUI data transfer for DRAM accesses. Unit: DRAM clock * 4

Register A2h CPU/PCI-GUI Privilege Timer Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**CPU/PCI-GUI Privilege Timer Control** **Bits[7:6]** — **Privilege** 00 — CPU/PCI high privilege 01 — GUI high privilege 1x — Enable CPU/PCI-GUI Privilege Timer
5:0	R/W	**Reserved**

Register A3h VGA Grant Timer

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:1	R/W	**Initial Value of VGA Grant Timer** The timer controls how long VGA grant hold once it get the DRAM bus. Unit: DRAM clock * 8
0	R/W	**Reserved**

7.4.1.11. A.G.P. AND HOST BRIDGE CONTROL REGISTERS

Register C0h A.G.P. Capability Identify Register (ACAPID)

Default Value: 00200002h
Access: Read Only

BIT	ACCESS	DESCRIPTION
31:24	RO	**Reserved**
23:20	RO	**A.G.P revision Major** Default value is 0010b to indicate that SiS530 conforms to the major revision 2 of internal A.G.P. bus interface specification.
19:16	RO	**A.G.P revision Minor** Default value is 0000b to indicate that SiS530 conforms to the minor revision 0 of internal A.G.P. interface specification.
15:8	RO	**Next Capability** Default value is 00h to indicate the final item.
7:0	RO	**A.G.P. Capability ID** Default value is 02h to indicate the list item as pertaining to A.G.P. registers.

Register C4h A.G.P. Status Register

Default Value: 1F000203h
Access: Read Only

BIT	ACCESS	DESCRIPTION
31:24	RO	**RQ Field** The RQ field contains the maximum number of A.G.P. command requests SiS530 can manage. Default value is 1Fh to indicate that the maximum number of A.G.P. command requests SiS530 can manage is 32.
23:10	RO	**Reserved**
9	RO	**SBA** Default value is 1 to indicate that SiS530 supports side band addressing.
8:2	RO	**Reserved**
1:0	RO	**Data Rate** The RATE field indicates the data transfer rates supported by this devices. Default value is 11b to indicate SiS530 support both 1X and 2X mode.

Register C8h A.G.P. Command Register

Default Value: 00000000h
Access: Read Write

BIT	ACCESS	DESCRIPTION
31:10	R/W	**Reserved**
9	R/W	**SBA_ENABLE** When set, the side band address mechanism is enabled.

8	R/W	**A.G.P._ENABLE** Setting the bit allows the target to accept A.G.P. operations. When cleared, the target ignores incoming A.G.P. operations. Please note that the target must be enabled before the master.
7:2	R/W	**Reserved**
1:0	R/W	**Data Rate** One (and only one) bit in the DATA_RATE field must be set to indicate the desired data transfer rate. <Bit0: 1X, Bit1: 2X>. The same bit must be set on both master and target. The DATA_RATE field applies to AD and SBA buses. **Bits[1:0]** — **Data Rate** 00 — Reserved 01 — 1X mode 10 — 2X mode 11 — Reserved

7.4.2. VIRTUAL PCI-TO-PCI BRIDGE REGISTERS (DEVICE 2)

Register 00h Vendor ID

Default Value: 1039h
Access: Read Only
The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Vendor Identification Number**

Register 02h Device ID

Default Value: 0001h
Access: Read Only
The device identifier is allocated as 0001h by Silicon Integrated Systems Corp.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Device Identification Number**

Register 04h Command

Default Value: 00h
Access: Read/Write, Read Only
The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.

BIT	ACCESS	DESCRIPTION
15:6	RO	**Reserved**
5	R/W	**VGA Palette Snoop Enable** Controls the behavior in the case of CPU access destining to VGA compatible address. The bit affects the destinations of I/O writes issued by the CPU with address 3C6h, 3C8h, 3C9h. 0: Disable 1: Enable

4:2	RO	**Reserved**
1	R/W	**Memory Space Enable** Controls the forwarding of memory accesses from CPU to internal A.G.P. bus When the bit is disabled, the bridge would not forward any memory accesses to internal A.G.P. bus. When the bit is enabled, the bridge forwards CPU memory cycles toward internal A.G.P. bus according to standard PCI-to-PCI bridge forwarding rule. 0: Disable 1: Enable
0	R/W	**I/O Space Enable** Controls the forwarding of I/O accesses from CPU to internal A.G.P. bus When the bit is disabled, the bridge would not forward any I/O accesses to internal A.G.P. bus. When the bit is enabled, the bridge forwards CPU I/O cycles toward internal A.G.P. bus according to standard PCI-to-PCI bridge forwarding rule. 0: Disable 1: Enable

Register 06h Status

Default Value: 00h
Access: Read Only
This register is reserved since the status information of the primary bus is stored in the status register of Device 0.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Reserved**

Register 08h Revision ID

Default Value: 00h
Access: Read Only
The Revision ID is 00h for our first Revision.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Revision Identification Number**

Register 09h Programming Interface

Default Value: 00h
Access: Read Only
The default value is 00h since no specific register-level programming interface is provided.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Programming Interface**

Register 0Ah Sub Class Code

Default Value: 04h
Access: Read Only
The Sub Class Code is 04h for PCI-to-PCI bridge.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Sub Class Code**

Register 0Bh Base Class Code

Default Value: 06h
Access: Read Only
The value of 06h in this field identifies a bridge device.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Base Class Code**

Register 0Ch Cache Line Size

Default Value: 00h
Access: Read Only
The value of this register is always 00h since the host bridge would not generate the Memory Write and Invalidate command.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Cache Line Size**

Register 0Dh Master Latency Timer (MLT)

Default Value: 00h
Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Master Latency Timer**

Register 0Eh Header Type

Default Value: 01h
Access: Read Only
The value of 01h identifies PCI-to-PCI bridge header is being used.

BIT	ACCESS	DESCRIPTION
7:0	RO	**Header Type**

Register 0Fh BIST

Default Value: 00h
Access: Read Only
The value is 00h since we do not support Build-in Self Test.

BIT	ACCESS	DESCRIPTION
7:0	RO	**BIST**

Register 19h Secondary Bus Number (SBUSN)

Default Value: 00h
Access: Read/Write
This register identifies the bus number assigned to the second bus side of the virtual PCI-to-PCI Bridge. This field is programmed by the PCI configuration software to allow mapping of configuration cycles to A.G.P. bus.

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Secondary Bus Number**

Register 1Ah Subordinate Bus Number (SUBUSN)

Default Value: 00h
Access: Read/Write
This register is used to record the number of the highest numbered PCI bus that is behind A.G.P. bus.

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Subordinate Bus Number**

Register 1Bh Secondary Master Latency Timer (SMLT)

Default Value: 00h
Access: Read/Write, Read Only
This register adheres to the definition of the Latency Timer in the PCI Local Bus Specification but applies only to A.G.P. interface.

BIT	ACCESS	DESCRIPTION
7:3	R/W	**Secondary Master Latency Timer** Default value is 00h. Unit: 8 * A.G.P clock
2:0	RO	**Reserved**

Register 1Ch I/O Base

Default Value: F0h
Access: Read/Write, Read Only
The I/O Base register defines the bottom address of an address range that is used by SiS530 to determine when to forward I/O transactions from CPU to host VGA bus.

BIT	ACCESS	DESCRIPTION
7:4	R/W	**I/O Address Base A[15:12]** Bits[7:4] control the CPU to internal host VGA bus I/O access. SiS530 forwards I/O cycle initiated by CPU to internal host VGA bus if the address of the cycle meets the following requirement. I/O_BASE ≤ address ≤ I/O_LIMIT
3:0	RO	**Reserved**

Register 1Dh I/O Limit

Default Value: 00h
Access: Read/Write, Read Only
The I/O Limit register defines the top address of an address range that is used by SiS530 to determine when to forward I/O transactions from CPU to internal host VGA bus.

BIT	ACCESS	DESCRIPTION

7:4	R/W	**I/O Address Limit A[15:12]** Bits[7:4] control the CPU to internal VGA controller I/O access. SiS530 forwards I/O cycle initiated by CPU to host VGA bus if the address of the cycle meets the following requirement. I/O_BASE ≤ address ≤ I/O_LIMIT
3:0	RO	**Reserved**

Register 1Eh Secondary PCI-PCI Status (SSTS)

Default Value: 0000h

Access: Read/Write, Read Only

The Secondary Status register is similar in function and bit definition to the Status register of device 0 function 0 of SiS530.

BIT	ACCESS	DESCRIPTION
15:14	RO	**Reserved**
13	WC	**Receiver Master Abort** When SiS530 terminates a cycle on host VGA bus with master abort, this bit is set to 1. This bit can be cleared by writing a 1 to it.
12:0	RO	**Reserved**

Register 20h Non-prefetchable Memory Base Address (MBASE)

Default Value: FFF0h

Access: Read/Write, Read Only

The register defines the bottom address of a non-prefetchable memory address range that is used by SiS530 to determine when to forward memory transactions from CPU to host VGA bus.

BIT	ACCESS	DESCRIPTION
15:4	R/W	**Memory Address Base A[31:20].** Bits[15:4] control the CPU to internal VGA controller memory access. SiS530 forwards I/O cycle initiated by CPU to host VGA bus if the address of the cycle meets the following requirement. MBASE ≤ address ≤ MLIMIT
3:0	RO	**Reserved**

Register 22h Non-prefetchable Memory Limit Address (MLIMIT)

Default Value: 0000h

Access: Read/Write, Read Only

The register defines the top address of a non-prefetchable memory address range that is used by SiS530 to determine when to forward memory transactions from CPU to host VGA bus

BIT	ACCESS	DESCRIPTION
15:4	R/W	**Memory Address Limit A[31:20].** Bits[15:4] control the CPU to integrated VGA controller memory access. SiS530 forwards I/O cycle initiated by CPU to host VGA bus if the address of the cycle meets the following requirement. MBASE ≤ address ≤ MLIMIT

3:0	RO	**Reserved**

Register 24h Prefetchable Memory Base Address (PMBASE)

Default Value: FFF0h

Access: Read/Write, Read Only

The register defines the bottom address of a prefetchable memory address range that is used by SiS530 to determine when to forward memory transactions from CPU to host VGA

BIT	ACCESS	DESCRIPTION
15:4	R/W	**Memory Address Base A[31:20].** Bits[15:4] control the CPU to integrated VGA controller memory access. SiS530 forwards I/O cycle initiated by CPU to host VGA bus if the address of the cycle meets the following requirement. PMBASE ≤ address ≤ PMLIMIT
3:0	RO	**Reserved**

Register 26h Prefetchable Memory Limit Address (PMLIMIT)

Default Value: 0000h

Access: Read/Write, Read Only

The register defines the top address of a prefetchable memory address range that is used by SiS530 to determine when to forward memory transactions from CPU to host VGA bus.

BIT	ACCESS	DESCRIPTION
15:4	R/W	**Memory Address Limit A[31:20].** Bits[15:4] control the CPU to integrated VGA controller memory access. SiS530 forwards I/O cycle initiated by CPU to host VGA bus if the address of the cycle meets the following requirement. PMBASE ≤ address ≤ PMLIMIT
3:0	RO	**Reserved**

Register 3Eh PCI to PCI Bridge Control (BCTRL)

Default Value: 0000h

Access: Read/Write, Read Only

The Bridge Control register provides control extensions to the Command register.

BIT	ACCESS	DESCRIPTION
15:4	RO	**Reserved.**
3	R/W	**VGA Enable** The bit controls the response by bridge to VGA compatible memory and I/O address. VGA compatible memory and I/O address will be forwarded to host VGA bus when this bit is set to "1". 0 : Disable 1 : Enable

2	R/W	**ISA Enable** When this bit is enabled, IO transactions addressing the last 768 bytes in each 1KB block will be forwarded to primary PCI bus even if the address are within the range defined by the IOBASE and IOLIMIT. 0 : Disable 1 : Enable
1:0	RO	**Reserved**

7.4.3. PCI IDE CONFIGURATION SPACE REGISTER

DEVICE	IDSEL	FUNCTION NUMBER
IDE	AD11	0001b

Register 00h Vendor ID

Default Value: 1039h
Access: Read Only
The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Vendor Identification Number**

Register 02h Device ID

Default Value: 5513h
Access: Read Only
The device identifier is allocated as 5513h by Silicon Integrated Systems Corp.

BIT	ACCESS	DESCRIPTION
15:0	RO	**Device Identification Number**

Register 04h Command

Default Value: 0000h
Access: Read/Write, Read Only
The Command register provides coarse control over a device ability to generate and respond to PCI cycles.

BIT	ACCESS	DESCRIPTION
15:3	RO	**Reserved**
2	R/W	**Bus Master** When set, the Bus master function is enabled. It is disabled by default.
1	R/W	**Memory Space** The bit controls the response to memory space accesses. This bit should be programmed as "0".

0	R/W	**I/O Space** When enabled, the built-in IDE will respond to any access of the IDE legacy ports in the compatibility mode, or to any access of the IDE relocatable ports in the native mode. Also, any access to the PCI bus master IDE registers are allowed. This bit is zero (disabled) on reset.

Register 06h Status

Default Value: 0000h
Access: Read/Write, Read Only, Write Clear

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

BIT	ACCESS	DESCRIPTION
15:14	RO	**Reserved** These bits are hardware to zero.
13	WC	**Master Abort Asserted** This bit is set when a PCI bus master IDE transaction is terminated by master abort. While this bit is set, IDE will issue an interrupt request. This bit can be cleared by writing a 1 to it.
12	WC	**Received Target Abort** The bit is set whenever PCI bus master IDE transaction is terminated with target abort.
11	RO	**Signaled Target Abort** The bit will be asserted when IDE terminates a transaction with target abort.
10:9	RO	**DEVSEL# Timing DEVT** These two bits define the timing of asserting DEVSEL#. The built-in IDE always asserts DEVSEL# in fast timing, and thus the two bits are hardwired to 0 per PCI Spec.
8	R/W	**Reserved, Read as "0".**
7:0	RO	**Reserved** Default value is 00h

Register 08h Revision ID

Default Value: D0h
Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Revision Identification Number**

Register 09h Programming Interface

Default Value: 00h
Access: Read Only

The default value is 00h since no specific register-level programming interface is provided.

BIT	ACCESS	DESCRIPTION
7	RO	**Master IDE Device** This bit is hardwired to one to indicate that the built-in IDE is capable of supporting bus master function.
6:4	RO	**Reserved**
3	RO	**Secondary IDE Programmable Indicator** When the bit is programmed as "1", it means that the primary channel can be programmed to operate in compatible or native mode. When the bit is programmed as "0", the mode is fixed and is determined by the value of bit 2. This bit should be programmed as "1" during the BIOS boot up procedures.
2	RO	**Secondary IDE Operating Mode** This bit defines the mode that the secondary IDE channel is operating in. Zero corresponds to 'compatibility' while one means native mode. By default, this bit is 0 and is programmable.
1	RO	**Primary IDE Programmable Indicator** When the bit is programmed as "1", it means that the primary channel can be programmed to operate in compatible or native mode. When the bit is programmed as "0", the mode is fixed and is determined by the value of bit 0. This bit should be programmed as "1" during the BIOS boot up procedures.
0	RO	**Primary IDE Operating Mode** This bit defines the mode that the primary IDE channel is operating in. Zero corresponds to 'compatibility' while one means native mode. By default, this bit is 0 and is programmable.

Register 0Ah Sub Class Code

Default Value: 01h
Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Sub Class Code**

Register 0Bh Base Class Code

Default Value: 01h
Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Base Class Code**

Register 0Ch Cache Line Size

Default Value: 00h
Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Cache Line Size**

Register 0Dh Latency Timer

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Initial Value for Latency Timer** The default value is 0. Unit: PCI clock

Register 0Eh Header Type

Default Value: 80h
Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Header Type**

Register 0Fh BIST

Default Value: 00h
Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**BIST**

Register 10h~13h Primary Channel Command Block Base Address Register

Register 14h~17h Primary Channel Control Block Base Address Register

Register 18h~1Bh Secondary Channel Command Block Base Address Register

Register 1Ch~1Fh Secondary Channel Control Block Base Address Register

In the native mode, above four registers define the IDE base address for each of the two IDE devices in both the primary and secondary channels respectively. In the compatible mode, the four registers can still be programmed and read out, but it does not affect the IDE address decoding.

Register 20h~23h Bus Master IDE Control Register Base Address

Offset Register	REGISTER ACCESS
00H	**Bus Master IDE Command Register (Primary)**
01H	**Reserved**
02H	**Bus Master IDE Status Register(Primary)**
03H	**Reserved**
04-07H	**Bus Master IDE PRD (*) Table Pointer (Primary)**
08H	**Bus Master IDE Command Register (Secondary)**
09H	**Reserved**
0AH	**Bus Master IDE Status Register (Secondary)**
0BH	**Reserved**
0C-0FH	**Bus Master IDE PRD (*) Table Pointer (Secondary)**

*PRD: Physical Region Descriptor

Register 24h~2Bh Reserved

Default Value: 00h
Access: Read Only

Register 2C~2Dh Subsystem Vendor ID

Default Value: 0000h
Access: Read/Write
This register can be written once and is used to identify vendor of the subsystem.

Register 2Eh~2Fh Subsystem ID

Default Value: 0000h
Access: Read/Write
This register can be written once and is used to identify subsystem ID.

Register 30h~33h Expansion ROM Base Address

Default Value: 00000000h
Access: Read/Write

Register 34h~3Fh Reserved

Register 40h IDE Primary Channel/Master Drive Data Recovery Time Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Test mode for internal use only** 0: Normal mode 1: Test mode This test mode for recovery and active timer counter.
6	R/W	**Test mode for internal use only** 0: Normal mode 1: Test mode This test mode for prefetch byte counter.
5:4	R/W	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 41h IDE Primary Channel/Master Drive Data Active Time Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable
6:4	R/W	**Ultra DMA 33/66 cycle time Select** 000: Reserved 001: Cycle time of 2 CLK clocks for data out 010: Cycle time of 3 CLK clocks for data out 011: Cycle time of 4 CLK clocks for data out 100: Cycle time of 5 CLK clocks for data out 101: Cycle time of 6 CLK clocks for data out 110: Cycle time of 7 CLK clocks for data out 111: Cycle time of 8 CLK clocks for data out Note : 2 CLK = 1 PCICLK
3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 42h IDE Primary Channel/Slave Drive Data Recovery Time Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 43h IDE Primary Channel/Slave Drive Data Active Time Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable

6:4	R/W	**Ultra DMA 33/66 cycle time Select** 000: Reserved 001: Cycle time of 2 CLK clocks for data out 010: Cycle time of 3 CLK clocks for data out 011: Cycle time of 4 CLK clocks for data out 100: Cycle time of 5 CLK clocks for data out 101: Cycle time of 6 CLK clocks for data out 110: Cycle time of 7 CLK clocks for data out 111: Cycle time of 8 CLK clocks for data out Note : 2 CLK = 1 PCICLK
3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 44h IDE Secondary Channel/Master Drive Data Recovery Time Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 45h IDE Secondary Channel/Master Drive Data Active Time Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable

6:4	R/W	**Ultra DMA 33/66 cycle time Select** 000: Reserved 001: Cycle time of 2 CLK clocks for data out 010: Cycle time of 3 CLK clocks for data out 011: Cycle time of 4 CLK clocks for data out 100: Cycle time of 5 CLK clocks for data out 101: Cycle time of 6 CLK clocks for data out 110: Cycle time of 7 CLK clocks for data out 111: Cycle time of 8 CLK clocks for data out Note : 2 CLK = 1 PCICLK
3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 46h IDE Secondary Channel/Slave Drive Data Recovery Time Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved**
3:0	R/W	**Recovery Time** 0000: 12 PCICLK 0001: 1 PCICLK 0010: 2 PCICLK 0011: 3 PCICLK 0100: 4 PCICLK 0101: 5 PCICLK 0110: 6 PCICLK 0111: 7 PCICLK 1000: 8 PCICLK 1001: 9 PCICLK 1010: 10 PCICLK 1011: 11 PCICLK 1100: 13 PCICLK 1101: 14 PCICLK 1110: 15 PCICLK 1111: 15 PCICLK

Register 47h IDE Secondary Channel/Slave Drive Data Active Time Control

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Ultra DMA Mode Control** 0: Disable 1: Enable

6:4	R/W	**Ultra DMA 33/66 cycle time Select** 000: Reserved 001: Cycle time of 2 CLK clocks for data out 010: Cycle time of 3 CLK clocks for data out 011: Cycle time of 4 CLK clocks for data out 100: Cycle time of 5 CLK clocks for data out 101: Cycle time of 6 CLK clocks for data out 110: Cycle time of 7 CLK clocks for data out 111: Cycle time of 8 CLK clocks for data out Note : 2 CLK = 1 PCICLK
3	RO	**Reserved**
2:0	R/W	**Data Active Time Control** 000: 8 PCICLK 001: 1 PCICLK 010: 2 PCICLK 011: 3 PCICLK 100: 4 PCICLK 101: 5 PCICLK 110: 6 PCICLK 111: 12 PCICLK

Register 48h IDE Status Register

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	RO	**Reserved**
5	RO	**Channel 1 Cable Type Status (via CBLIDB signal)** 0: 80 pins cable type 1: 40 pins cable type
4	RO	**Channel 0 Cable Type Status (via CBLIDA signal)** 0: 80 pins cable type 1: 40 pins cable type
3:2	R/W	**PCI Read Request Threshold Setting** 00: PCI Request asserted when FIFO is 62.5% full during prefetch cycles. 01: PCI Request asserted when FIFO is 50.0% full during prefetch cycles. 10: PCI Request asserted when FIFO is 25.0% full during prefetch cycles. 11: PCI Request asserted when FIFO is 12.5% full during prefetch cycles.

1:0	R/W	**PCI Write Request Threshold Setting** 00: PCI Request asserted when FIFO is 12.5% full during prefetch cycles. 01: PCI Request asserted when FIFO is 25.0% full during prefetch cycles. 10: PCI Request asserted when FIFO is 50.0% full during prefetch cycles. 11: PCI Request asserted when FIFO is 62.5% full during prefetch cycles.

Register 49h Reserved

Register 4Ah IDE General Control Register 0

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Bus Master generates PCI burst cycles Control** 0: Disable 1: Enable
6	R/W	**Test Mode for internal use only** 0: Test Mode 1: Normal Mode
5	R/W	**Fast post-write control** 0: Disabled 1: Enabled (Recommended)
4	R/W	**Test Mode for internal use only** 0: Normal Mode 1: Test Mode When this bit is set 1, the IRQ of HD drive would pass direct to 8259. On the others hand, IDE would gate IRQ until IDE FIFO is empty under abnormal operation.
3	R/W	**Reserved**
2	R/W	**IDE Channel 1 Enable Bit** 0: Disabled 1: Enabled
1	R/W	**IDE Channel 0 Enable Bit** 0: Disabled 1: Enabled
0	R/W	**Reserved**

Register 4Bh IDE General Control register 1

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Enable Postwrite of the Slave Drive in Channel 1** 0: Disabled 1: Enabled
6	R/W	**Enable Postwrite of the Master Drive in Channel 1** 0: Disabled 1: Enabled
5	R/W	**Enable Postwrite of the Slave Drive in Channel 0** 0: Disabled 1: Enabled
4	R/W	**Enable Postwrite of the Master Drive in Channel 0** 0: Disabled 1: Enabled
3	R/W	**Enable Prefetch of the Slave Drive in Channel 1** 0: Disabled 1: Enabled
2	R/W	**Enable Prefetch of the Master Drive in Channel 1** 0: Disabled 1: Enabled
1	R/W	**Enable Prefetch of the Slave Drive in Channel 0** 0: Disabled 1: Enabled
0	R/W	**Enable Prefetch of the Master Drive in Channel 0** 0: Disabled 1: Enabled

(Following two 16-bit wide registers define the prefetching length of each IDE channel respectively.)

Register 4Ch~4Dh Prefetch Count of Primary Channel

Default Value: FFFFh
Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:0	R/W	**Prefetch Count of Primary Channel** The Count (in bytes) of IDE prefetch. The maximum value can be programmed is 512. (Default value is 512)

Register 4Eh~4Fh Prefetch Count of Secondary Channel

Default Value: FFFFh
Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:0	R/W	**Prefetch Count of Secondary Channel** The Count (in bytes) of IDE prefetch. The maximum value can be programmed is 512. (Default value is 512)

Register 50h~51h Reserved

Default Value: 0000h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:0	R/W	**Reserved**

Register 52h IDE Miscellaneous Control Register

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:5	RO	**Reserved**
4	R/W	**IDE I/O Buffer Driving Strength Control** 0: 4mA 1: 8mA
3	R/W	**Reserved**
2	R/W	**Control of IDE Programmable Indicator (Reg. 09 bit 1 and 3)** 0: IDE register 09 bit 1 and 3 would be read as "1¡ ¨ 1: IDE register 09 bit 1 and 3 would be programmable
1	R/W	**Test Mode for internal use only** 0 : Normal Mode 1 : Test Mode If this bit is set 1, IDE would reset IDE FIFO pointer when 8 bit command is forward to HDs driver. This bit would work on the condition that the transferring byte count of OS is not equal to the byte count received by HDs driver.
0	R/W	**Reserved**

7.4.3.1. OFFSET REGISTERS FOR PCI BUS MASTER IDE CONTROL REGISTERS

The PCI Bus master IDE Registers use 16 bytes of I/O Space. These registers can be accessed through I/O R/W to the address defined in the Bus Master IDE control register Base Address in the PCI IDE Configuration space. The base address is also defined in Register 20h~23h of PCI IDE configuration space.

Register 00h Bus Master Primary IDE Command Register

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved. Return 0 on reads.**
6:5	R/W	**Read or Write Control** This bit defines the R/W control of the bus master transfer. When set to zero, PCI bus master reads are conducted. When set to one, PCI bus master writes are conducted.
2:1	RO	**Reserved**

0	R/W	**Start/Stop Bus Master** The SiS Chip built-in IDE Controller enables its bus master operation whenever it detects this bit changing from a zero to a one. The operation can be halted by writing a zero to this bit.

Register 01h Reserved

Register 02h Bus Master Primary IDE Status Register

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	RO	**Simplex Only** This bit is hardwired to zero to indicate that both bus master channels can be operated at a time.
6	R/W	**Drive 1 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 1 for this channel is capable of DMA transfers.
5	R/W	**Drive 0 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 0 for this channel is capable of DMA transfers.
4:3	RO	**Reserved. Return 0 on reads**
2	R/W	**Interrupt** The bit is set by the rising edge of the IDE interrupt line to indicate that all data transferred from the drive is visible in the system memory. Writing a '1' to this bit can reset it.
1	RO	**Error** This bit is set when the IDE controller encounters an error during data transferring to/from memory.
0	R/W	**Bus Master IDE Device Active** This bit is set when the start bit in the command register is set. It can be cleared when the last transfer of a region is performed, or the start bit is reset.

Register 03h Reserved

Register 04h~07h Bus Master Primary IDE PRD Table Pointer Register

This 32-bit register contains address pointing to the starting address of the PRD table.
Default Value: 00000000h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:2	R/W	**Base Address of the PRD Table**
1:0	R/W	**Reserved**

*PRD: Physical Region Descriptor

Register 08h Bus Master Secondary IDE Command Register

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:4	RO	**Reserved. Return 0 on reads.**
3	R/W	**Read or Write Control.** This bit defines the R/W control of the bus master transfer. When set to "0", PCI bus master reads are conducted. When set to "1", PCI bus master writes are conducted.
2:1	RO	**Reserved**
0	R/W	**Start/Stop Bus Master** The SiS chip built-in IDE Controller enables its bus master operation whenever it detects this bit changing from a zero to a one. The operation can be halted by writing a zero to this bit.

Register 09h Reserved

Register 0Ah Bus Master Secondary IDE Status Register

Default Value: 00h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	RO	**Simplex Only** This bit is hardwired to zero to indicate that both bus master channels can be operated at a time.
6	R/W	**Drive 1 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 1 for this channel is capable of DMA transfers.
5	R/W	**Drive 0 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 0 for this channel is capable of DMA transfers**.**
4:3	RO	**Reserved. Return 0 on reads**
2	R/W	**Interrupt** The bit is set by the rising edge of the IDE interrupt line to indicate that all data transferred from the drive is visible in the system memory. Writing a '1' to this bit can reset it.
1	RO	**Error** This bit is set when the IDE controller encounters an error during data transferring to/from memory.
0	R/W	**Bus Master IDE Device Active** This bit is set when the start bit in the command register is set. It can be cleared when the last transfer of a region is performed, or the start bit is reset.

Register 0Bh Reserved

Register 0Ch~0Fh Bus Master Secondary IDE PRD Table Pointer Register

This 32-bit register contains address pointing to the starting address of the PRD table.
Default Value: 00000000h
Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:2	R/W	**Base Address of the PRD Table**
1:0	R/W	**Reserved**

*PRD: Physical Region Descriptor

8. INTEGRATED 3D VGA CONTROLLER REGISTERS

8.1. GENERAL REGISTERS

MISCELLANEOUS OUTPUT REGISTER

Register Type: Read/Write
Read Port: 3CC
Write Port: 3C2
Default: 00h

D7 Vertical Sync Polarity
- 0: Select 'positive vertical sync'
- 1: Select 'negative vertical sync'

D6 Horizontal Sync Polarity
- 0: Select 'positive horizontal sync'
- 1: Select 'negative horizontal sync'

Table 8.1-1 Sync Polarity vs. Vertical Screen Resolution

D7	D6	EGA	VGA
0	0	200 Lines	Invalid
0	1	350 Lines	400 Lines
1	0	Invalid	350 Lines
1	1	Invalid	480 Lines

D5 Odd/Even Page
- 0: Select low page of memory
- 1: Select high page of memory

D4 Reserved

D[3:2] Clock Select

Table 8.1-2 Table for Video Clock Selection

D3	D2	DCLK
0	0	25.175 MHz
0	1	28.322 MHz
1	0	Don't Care
1	1	For internal clock generator.

D1 Display RAM Enable
- 0: Disable processor access to video RAM
- 1: Enable processor access to video RAM

D0 I/O Address Select
- 0: Sets addresses for monochrome emulation
- 1: Sets addresses for color graphics emulation

FEATURE CONTROL REGISTER

Register Type: Read/Write
Read Port: 3CA
Write Port: 3BA/3DA

Default: 00h
D[7:4] Reserved (0)
D3 Vertical Sync Select
0: Normal Vertical Sync output to monitor
1: [Vertical Sync OR Vertical Display Enable] output to monitor
D[2:0] Reserved (0)

INPUT STATUS REGISTER 0

Register Type: Read only
Read Port: 3C2
Default: 00h
D7 Vertical Retrace Interrupt Pending
0: Cleared
1: Pending
D[6:5] Reserved
D4 Switch Sense
D[3:0] Reserved

INPUT STATUS REGISTER 1

Register Type: Read only
Read Port: 3BA/3DA
Default: 00h
D[7:6] Reserved
D[5:4] Diagnostic

Table 8.1-3 Table for Video Read-back Through Diagnostic Bit (I)

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
D5	**D4**	**D5**	**D4**
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table 8.1-4 Table for Video Read-back Through Diagnostic Bit (II)

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
D5	**D4**	**D5**	**D4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D3 Vertical Trace
0: Inactive
1: Active
D[2:1] Reserved
D0 Display Enable Not
0: Display period
1: Retrace period

VGA ENABLE REGISTER
Register Type: Read/Write
Read/Write Port: 3C3 or 46E8
Default: 00h
D0 VGA Enable (for 3C3 only)
0: Disable
1: Enable
D3 VGA Enable (for 46E8 only)
0: Disable
1: Enable

SEGMENT SELECTION REGISTER 0
Register Type: Read/Write
Read/Write Port: 3CD
Default: 00h
If D3 of SRB (Dual Segment Mode Enable bit) sets to 1, then
D7 Reserved
D[6:0] Segment Selection Write Bit[6:0]
If D3 of SRB (Dual Segment Mode Enable bit) sets to 0, then
D[7:4] Segment Selection Write Bit[3:0]
D[3:0] Segment Selection Read Bit[3:0]

SEGMENT SELECTION REGISTER 1
Register Type: Read/Write
Read/Write Port: 3CB
Default: 00h
If D3 of SRB (Dual Segment Mode Enable bit) sets to 1, then
D7 Reserved
D[6:0] Segment Selection Read Bit[6:0]
If D3 of SRB (Dual Segment Mode Enable bit) sets to 0, then
D[7:0] Reserved

8.2. CRT CONTROLLER REGISTERS

CRT CONTROLLER INDEX REGISTER
Register Type: Read/Write
Read/Write Port: 3B4/3D4
Default: 00h
D[7:0] CRT Controller Index
- 00h ~ 18h for standard VGA
- 19h ~ 26h for SiS extended CRT registers
- 80h ~ BFh for SiS extended video registers

Table 8.2- 1 Table of CRT Controller Registers

INDEX (3B4/3D4)	CRT CONTROLLER REGISTERS (3B5/3D5)
00h	Horizontal Total
01h	Horizontal Display Enable End
02h	Horizontal Blank Start
03h	Horizontal Blank End
04h	Horizontal Retrace Start

05h	Horizontal Retrace End
06h	Vertical Total
07h	Overflow Register
08h	Preset Row Scan
09h	Max Scan Line/Text Character Height
0Ah	Text Cursor Start
0Bh	Text Cursor End
0Ch	Screen Start Address High
0Dh	Screen Start Address Low
0Eh	Text Cursor Location High
0Fh	Text Cursor Location Low
10h	Vertical Retrace Start
11h	Vertical Retrace End
12h	Vertical Display Enable End
13h	Screen Offset
14h	Underline Location
15h	Vertical Blank Start
16h	Vertical Blank End
17h	Mode Control
18h	Line Compare
19h	Extended Signature Read-Back Register 0
1Ah	Extended Signature Read-Back Register 1
1Bh	CRT horizontal counter read-back
1Ch	CRT vertical counter read back
1Dh	CRT overflow counter read back
1Eh	Extended Signature Read-Back Register 2
22h	Graphics Data Latch Read-back Register
24h	Attribute Controller Toggle Read-back Register
26h	Attribute Controller Index Read-back Register

CR0: HORIZONTAL TOTAL
Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 00h
Default: 00h
D[7:0] Horizontal Total Bit[7:0]

CR1: HORIZONTAL DISPLAY ENABLE END
Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 01h
Default: 00h
D[7:0] Horizontal Display Enable End Bit[7:0]

CR2: HORIZONTAL BLANK START
Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 02h
Default: 00h
D[7:0] Horizontal Blank Start Bit[7:0]

CR3: HORIZONTAL BLANK END

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 03h
Default: 00h

D7	Reserved
D[6:5]	Display Skew Control Bit[1:0] 00: No skew 01: Skew 1 character 10: Skew 2 characters 11: Skew 3 characters
D[4:0]	Horizontal Blank End Bit[4:0]

CR4: HORIZONTAL RETRACE START

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 04h
Default: 00h

D[7:0]	Horizontal Retrace Start Bit[7:0]

CR5: HORIZONTAL RETRACE END

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 05h
Default: 00h

D7	Horizontal Blank End Bit[5]
D[6:5]	Horizontal Retrace Delay Bit[1:0] 00: Skew 0 character clock 01: Skew 1 character clock 10: Skew 2 character clocks 11: Skew 3 character clocks
D[4:0]	Horizontal Retrace End Bit[4:0]

CR6: VERTICAL TOTAL

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 06h
Default: 00h

D[7:0]	Vertical Total Bit[7:0]

CR7: OVERFLOW REGISTER

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 07h
Default: 00h

D7	Vertical Retrace Start Bit[9]
D6	Vertical Display Enable End Bit[9]
D5	Vertical Total Bit[9]
D4	Line Compare Bit[8]
D3	Vertical Blank Start Bit[8]
D2	Vertical Retrace Start Bit[8]
D1	Vertical Display Enable End Bit[8]
D0	Vertical Total Bit[8]

CR8: PRESET ROW SCAN

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 08h
Default: 00h

D7	Reserved
D[6:5]	Byte Panning Control Bit[1:0]
D[4:0]	Preset Row Scan Bit[4:0]

CR9: MAXIMUM SCAN LINE/TEXT CHARACTER HEIGHT

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 09h
Default: 00h

D7	Double Scan
	0: Disable
	1: Enable 400 lines display
D6	Line Compare Bit[9]
D5	Vertical Blank Start Bit[9]
D[4:0]	Character Cell Height Bit[4:0]

CRA: TEXT CURSOR START

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Ah
Default: 00h

D[7:6]	Reserved
D5	Text Cursor Off
	0: Text Cursor On
	1: Text Cursor Off
D[4:0]	Text Cursor Start Bit[4:0]

CRB: TEXT CURSOR END

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Bh
Default: 00h

D7	Reserved
D[6:5]	Text Cursor Skew
	00: No skew
	01: Skew one character clock
	10: Skew two character clocks
	11: Skew three character clocks
D[4:0]	Text Cursor End Bit[4:0]

CRC: SCREEN START ADDRESS HIGH

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Ch
Default: 00h

D[7:0]	Screen Start Address Bit[15:8]

CRD: SCREEN START ADDRESS LOW

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Dh

Default: 00h
D[7:0] Screen Start Address Bit[7:0]

CRE: TEXT CURSOR LOCATION HIGH
Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Eh
Default: 00h
D[7:0] Text Cursor Location Bit[15:8]

CRF: TEXT CURSOR LOCATION LOW
Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Fh
Default: 00h
D[7:0] Text Cursor Location Bit[7:0]

CR10: VERTICAL RETRACE START
Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 10h
Default: 00h
D[7:0] Vertical Retrace Start Bit[7:0]

CR11: VERTICAL RETRACE END
Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 11h
Default: 00h
D7 Write Protect for CR0 to CR7
0: Disable Write Protect
1: Enable Write Protect
D6 Alternate Refresh Rate
0: Selects three refresh cycles per scanline
1: Selects five refresh cycles per scanline
D5 Vertical Interrupt Enable
0: Enable
1: Disable
D4 Vertical Interrupt Clear
0: Clear
1: Not Clear
D[3:0] Vertical Retrace End Bit[3:0]

CR12: VERTICAL DISPLAY ENABLE END
Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 12h
Default: 00h
D[7:0] Vertical Display Enable End Bit[7:0]

CR13: SCREEN OFFSET
Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 13h
Default: 00h
D[7:0] Screen Offset Bit[7:0]

CR14: UNDERLINE LOCATION REGISTER

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 14h
Default: 00h

D7	Reserved
D6	Double-word Mode Enable 0: Disable 1: Enable
D5	Count by 4 0: Disable 1: Enable
D[4:0]	Underline Location Bit[4:0]

CR15: VERTICAL BLANK START

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 15h
Default: 00h

D[7:0]	Vertical Blank Start Bit[7:0]

CR16: VERTICAL BLANK END

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 16h
Default: 00h

D[7:0]	Vertical Blank End Bit[7:0]

CR17: MODE CONTROL REGISTER

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 17h
Default: 00h

D7	Hardware Reset 0: Disable horizontal and vertical retrace outputs 1: Enable horizontal and vertical retrace outputs
D6	Word/Byte Address Mode 0: Set the memory address mode to word 1: Set the memory address mode to byte
D5	Address Wrap 0: Disable the full 256K of memory 1: Enable the full 256K of memory
D4	Reserved
D3	Count by Two 0: Byte refresh 1: Word refresh
D2	Horizontal Retrace Select 0: Normal 1: Double Scan
D1	RA1 replace MA14 0: Enable 1: Disable
D0	RA0 replace MA13 0: Enable 1: Disable

CR18: LINE COMPARE REGISTER
Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 18h
Default: 00h
D[7:0] Line Compare Bit[7:0]

CR19: EXTENDED SIGNATURE READ-BACK REGISTER 0
Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 19h
Default: xxh
D[7:0] Signature read-back bit[7:0]

CR1A: EXTENDED SIGNATURE READ-BACK REGISTER 1
Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Ah
Default: xxh
D[7:0] Signature read-back bit[15:8]

CR1B: CRT HORIZONTAL COUNTER READ BACK
Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Bh
Default: xxh
D[7:0] CRT horizontal counter bit[7:0]

CR1C: CRT VERTICAL COUNTER READ BACK
Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Ch
Default: xxh
D[7:0] CRT vertical counter bit[7:0]

CR1D: CRT OVERFLOW COUNTER READ BACK
Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Dh
Default: xxh
D7 Reserved
D6 MCLK Synthesizer Locking
D5 MCLK Synthesizer Locking
D4 CRT horizontal counter bit 8
D3 Reserved
D[2:0] CRT vertical counter bit[10:8]

NOTE: The horizontal and vertical counter value will be latched when read register CR20. So the three registers value should be read after read CR20.

CR1E: EXTENDED SIGNATURE READ-BACK REGISTER 2
Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Eh
Default: xxh
D[7:0] Signature read-back bit[23:16]

CR20: CRT COUNTER TRIGGER PORT
Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 20h
Default: xxh
D[7:0] Reserved

CR22: GRAPHICS DATA LATCH READ-BACK REGISTER
Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 22h
Default: xxh
D[7:0] Graphics Data Latch bit[7:0]

CR24: ATTRIBUTE CONTROLLER TOGGLE READ-BACK REGISTER
Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 24h
Default: xxh
D7 Attribute Controller Toggle
D[6:0] Reserved

CR26: ATTRIBUTE CONTROLLER INDEX READ-BACK REGISTER
Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 26h
Default: xxh
D[7:6] Reserved
D5 Video Enable
D[4:0] Attribute Controller Index bit[4:0]

8.3. SEQUENCER REGISTERS

8.3.1. SEQUENCER INDEX REGISTER
Register Type: Read/Write
Read/Write Port: 3C4
Default: 00h
D[7:6] Reserved
D[5:0] Sequencer Index Bit[5:0]

Table 8.3-1 Table of Sequencer Registers

INDEX (3C4)	SEQUENCER REGISTER (3C5)
00	Reset Register
01	Clock Mode
02	Color Plane Write Enable
03	Character Generator Select
04	Memory Mode

SR0: RESET REGISTER
Register Type: Read/Write
Read/Write Port: 3C5, Index 00h
Default: 00h
D[7:2] Reserved
D1 Synchronous reset

0: Reset
1: Normal

D0 Asynchronous reset
0: Reset
1: Normal

SR1: CLOCK MODE REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 01h
Default: 00h

D[7:6] Reserved

D5 Screen Off
0: Display On
1: Display Off

D4 Shifter Load 32 enable
0: Disable
1: Data shifter loaded every 4th Character Clock

D3 Dot Clock Divide by 2 enable
0: Disable
1: Video Clock is divided by 2 to generate Dot Clock

D2 Shifter Load 16 (while D4=0)
0: Disable
1: Data shifter loaded every 2nd Character Clock

D1 Reserved

D0 8/9 Dot Clock
0: Dot Clock is divided by 9 to generate Character Clock
1: Dot Clock is divided by 8 to generate Character Clock

SR2: COLOR PLANE WRITE ENABLE REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 02h
Default: 00h

D[7:4] Reserved

D3 Plane 3 write enable
0: Disable
1: Enable

D2 Plane 2 write enable
0: Disable
1: Enable

D1 Plane 1 write enable
0: Disable
1: Enable

D0 Plane 0 write enable
0: Disable
1: Enable

SR3: CHARACTER GENERATOR SELECT REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 03h
Default: 00h

D[7:6] Reserved

D5 Character generator table B select Bit[2]
D4 Character generator table A select Bit[2]
D[3:2] Character generator table B select Bit[1:0]
D[1:0] Character generator table A select Bit[1:0]

Table 8.3-2 Table of Selecting Active Character Generator

D5	D3	D2	USED WHEN TEXT ATTRIBUTE BIT 3 IS 1
D4	D1	D0	USED WHEN TEXT ATTRIBUTE BIT 3 IS 0
0	0	0	Character Table 1
0	0	1	Character Table 2
0	1	0	Character Table 3
0	1	1	Character Table 4
1	0	0	Character Table 5 (VGA only)
1	0	1	Character Table 6 (VGA only)
1	1	0	Character Table 7 (VGA only)
1	1	1	Character Table 8 (VGA only)

SR4: MEMORY MODE REGISTER
Register Type: Read/Write
Read/Write Port: 3C5, Index 04h
Default: 00h
D[7:4] Reserved
D3 Chain-4 Mode enable
0: Disable
1: Enable
D2 Odd/Even Mode enable
0: Enable
1: Disable
D1 Extended Memory
0: Select 64K
1: Select 256K
D0 Reserved

8.4. GRAPHICS CONTROLLER REGISTER

Graphics Controller Index Register
Register Type: Read/Write
Read/Write Port: 3CE
Default: 00h
D[7:4] Reserved
D[3:0] Graphics Controller Index Bit[3:0]

Table 8.4- 1 Table of Graphics Controller Registers

INDEX (3CE)	GRAPHICS CONTROLLER REGISTER (3CF)
00	Set/Reset Register
01	Set/Reset Enable Register
02	Color Compare Register
03	Data Rotate & Function Select
04	Read Plane Select Register

05	Mode Register
06	Miscellaneous Register
07	Color Don't Care Register
08	Bit Mask Register

GR0: SET/RESET REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 00h
Default: 00h
D[7:4] Reserved
D3 Set/Reset Map for plane 3
D2 Set/Reset Map for plane 2
D1 Set/Reset Map for plane 1
D0 Set/Reset Map for plane 0

GR1: SET/RESET ENABLE REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 01h
Default: 00h
D[7:4] Reserved
D3 Enable Set/Reset for plane 3
0: Disable
1: Enable
D2 Enable Set/Reset for plane 2
0: Disable
1: Enable
D1 Enable Set/Reset for plane 1
0: Disable
1: Enable
D0 Enable Set/Reset for plane 0
0: Disable
1: Enable

GR2: COLOR COMPARE REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 02h
Default: 00h
D[7:4] Reserved
D3 Color Compare Map for plane 3
D2 Color Compare Map for plane 2
D1 Color Compare Map for plane 1
D0 Color Compare Map for plane 0

GR3: DATA ROTATE/FUNCTION SELECT REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 03h
Default: 00h
D[7:5] Reserved
D[4:3] Function Select

Table 8.4- 2 Table of Function Select

D4	D3	FUNCTION
0	0	write data unmodified
0	1	write data AND processor latches
1	0	write data OR processor latches
1	1	write data XOR processor latches

D[2:0] Rotate Count

Table 8.4- 3 Table of Rotate Count

D2	D1	D0	RIGHT ROTATION
0	0	0	none
0	0	1	1 bits
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

GR4: READ PLANE SELECT REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 04h
Default: 00h
D[7:2] Reserved
D[1:0] Read Plane Select bit 1, 0
00: Plane 0
01: Plane 1
10: Plane 2
11: Plane 3

GR5: MODE REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 05h
Default: 00h
D7 Reserved
D6 256-color Mode
0: Disable
1: Enable
D5 Shift Register Mode
0: Configure shift register to be EGA compatible
1: Configure shift register to be CGA compatible
D4 Odd/Even Addressing Mode enable
0: Disable
1: Enable
D3 Read Mode
0: Map Select Read
1: Color Compare Read
D2 Reserved

D[1:0] Write mode

Table 8.4- 4 Table for Write Mode

D1	D0	MODE SELECTED
0	0	Write Mode 0: Direct processor write (Data Rotate, Set/Reset may apply).
0	1	Write Mode 1: Use content of latches as write data.
1	0	Write Mode 2: Color Plane n(0-3) is filled with the value of bit m in the processor write data.
1	1	Write Mode 3: Color Plane n(0-3) is filled with 8 bits of the color value contained in the Set/Reset Register for that plane. The Enable Set/Reset Register is not effective. Processor data will be AND with Bit Mask Register content to form new bit mask pattern. (data rotate may apply).

GR6: MISCELLANEOUS REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 06h
Default: 00h
D[7:4] Reserved
D[3:2] Memory Address Select

Table 8.4- 5 Table of Memory Address Select

D3	D2	ADDRESS RANGE
0	0	A0000 to BFFFF
0	1	A0000 to AFFFF
1	0	B0000 to B7FFF
1	1	B8000 to BFFFF

D1 Chain Odd And Even Maps
0: Disable
1: Enable
D0 Graphics Mode Enable
0: Select alphanumeric mode
1: Select graphics mode

GR7: COLOR DON'T CARE REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 07h
Default: 00h
D[7:4] Reserved
D3 Plane 3 Don't Care
0: Disable color comparison
1: Enable color comparison
D2 Plane 2 Don't Care
0: Disable color comparison
1: Enable color comparison
D1 Plane 1 Don't Care
0: Disable color comparison

1: Enable color comparison

D0 Plane 0 Don't Care
0: Disable color comparison
1: Enable color comparison

GR8: BIT MASK REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 08h
Default: 00h
D[7:0] Bit Mask Enable Bit[7:0]

8.5. ATTRIBUTE CONTROLLER AND VIDEO DAC REGISTERS

ATTRIBUTE CONTROLLER INDEX REGISTER

Register Type: Read/Write
Read Port: 3C0
Write Port: 3C0
Default: 00h
D[7:6] Reserved
D5 Palette Address Source
0: From CPU
1: From CRT
D[4:0] Attribute Controller Index Bit[4:0] (00h-14h)

Table 8.5-1 Table of Attribute Controller Registers

INDEX (3C0)	ATTRIBUTE CONTROLLER REGISTER (3C0)
00h	Color Palette Register 0
01h	Color Palette Register 1
02h	Color Palette Register 2
03h	Color Palette Register 3
04h	Color Palette Register 4
05h	Color Palette Register 5
06h	Color Palette Register 6
07h	Color Palette Register 7
08h	Color Palette Register 8
09h	Color Palette Register 9
0Ah	Color Palette Register 10
0Bh	Color Palette Register 11
0Ch	Color Palette Register 12
0Dh	Color Palette Register 13
0Eh	Color Palette Register 14
0Fh	Color Palette Register 15
10h	Mode Control Register
11h	Screen Border Color
12h	Color Plane Enable Register
13h	Pixel Panning Register
14h	Color Select Register (VGA)

AR0~ARF: PALETTE REGISTERS

Register Type: Read/Write
Read Port: 3C1, Index 00h ~ 0Fh
Write Port: 3C0, Index 00h ~ 0Fh
Default: 00h
D[7:6] Reserved
D[5:0] Palette Entries

AR10: MODE CONTROL REGISTER

Register Type: Read/Write
Read Port: 3C1, Index 10h
Write Port: 3C0, Index 10h
Default: 00h
D7 P4, P5 Source Select
0: AR0-F Bit[5:4] are used as the source for the Lookup Table Address Bit[5:4]
1: AR14 Bit[1:0] are used as the source for the Lookup Table Address Bit[5:4]
D6 Pixel Double Clock Select
0: The pixels are clocked at every clock cycle
1: The pixels are clocked at every other clock cycle
D5 PEL Panning Compatibility with Line Compare
0: Disable
1: Enable
D4 Reserved
D3 Background Intensity or Blink enable (while the Character Attribute D7=1)
0: Background Intensity attribute enable
1: Background Blink attribute enable
D2 Line Graphics enable
0: The ninth bit of nine-bit-wide character cell will be the same as the background.
1: The ninth bit of nine-bit-wide character cell will be made be the same as the eighth bit for character codes in the range C0h through DFh.
D1 Display Type
0: The contents of the Attribute byte are treated as color attribute.
1: The contents of the Attribute byte are treated as MDA-compatible attribute.
D0 Graphics/Text Mode
0: The Attribute Controller will function in text mode.
1: The Attribute Controller will function in graphics mode.

AR11: SCREEN BORDER COLOR

Register Type: Read/Write
Read Port: 3C1, Index 11h
Write Port: 3C0, Index 11h
Default: 00h
D[7:6] Reserved
D[5:0] Palette Entry

AR12: COLOR PLANE ENABLE REGISTER

Register Type: Read/Write

Read Port: 3C1, Index 12h
Write Port: 3C0, Index 12h
Default: 00h
D[7:6] Reserved
D[5:4] Display Status MUX Bit[1:0]
These bits select two of the eight bits color outputs to be available in the status register. The output color combinations available on the status bits are as follows:

Table 8.5-2 Table for Video Read-back Through Diagnostic Bit (I)

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
D5	D4	D5	D4
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table 8.5-3 Table for Video Read-back Through Diagnostic Bit (II)

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
D5	D4	D5	D4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D[3:0] Enable Color Plane Bit[3:0]

AR13: PIXEL PANNING REGISTER
Register Type: Read/Write
Read Port: 3C1, Index 13h
Write Port: 3C0, Index 13h
Default: 00h
D[7:4] Reserved
D[3:0] Pixel Pan Bit[3:0]
This field specifies the number of pixels the display data will be shifted to the left. This field is interpreted as indicated in the following table:

Table 8.5-4 Table of Pixel Panning

D3	D2	D1	D0	MONOCHROME TEXT	VGA MODE 13	ALL OTHERS
0	0	0	0	8	0	0
0	0	0	1	0	Invalid	1
0	0	1	0	1	1	2
0	0	1	1	2	Invalid	3
0	1	0	0	3	2	4
0	1	0	1	4	Invalid	5
0	1	1	0	5	3	6
0	1	1	1	6	Invalid	7

1	0	0	0	7	Invalid	Invalid
1	0	0	1	Invalid	Invalid	Invalid
1	0	1	0	Invalid	Invalid	Invalid
1	0	1	1	Invalid	Invalid	Invalid
1	1	0	0	Invalid	Invalid	Invalid
1	1	0	1	Invalid	Invalid	Invalid
1	1	1	0	Invalid	Invalid	Invalid
1	1	1	1	Invalid	Invalid	Invalid

AR14: COLOR SELECT REGISTER

Register Type: Read/Write
Read Port: 3C1, Index 14h
Write Port: 3C0, Index 14h
Default: 00h
D[7:4] Reserved
D[3:2] Color Bit[7:6]
These two bits are concatenated with the six bits from the Palette Register to form the address into the LUT and to drive P[7:6].
D[1:0] Color Bit[5:4]
If AR10 D7 is programmed to a '1', these two bits replace the corresponding two bits from the Palette Register to form the address into the LUT and to drive P[5:4]. If AR10 D7 is programmed to a '0', these two bits are ignored.

8.6 COLOR REGISTERS

8.6.1. DAC STATUS REGISTER

Register Type: Read Only
Read Port: 3C7
Default: 00h
D[7:2] Reserved
D[1:0] DAC State Bit[1:0]
00: Write Operation in progress
11: Read Operation in progress
others: Reserved

DAC INDEX REGISTER (READ MODE)

Register Type: Write Only
Write Port: 3C7
Default: 00h
D[7:0] DAC Index Bit[7:0]

DAC INDEX REGISTER (WRITE MODE)

Register Type: Read/Write
Read/Write Port: 3C8
Default: 00h
D[7:0] DAC Index Bit[7:0]

DAC DATA REGISTER

Register Type: Read/Write
Read/Write Port: 3C9

Default: 00h
When SR7 D2 = 1,
D[7:6] Reserved
D[5:0] DAC Data [5:0]
Before writing to this register, 3C8h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue values for the DAC entry are written. After the third value is written, the values are transferred to the LUT and the DAC index is incremented in case new values for the next DAC index are to be written.
Before reading from this register, 3C7h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue value for the DAC entry may be read from this DAC index. After the third value is read, the DAC index is incremented in case the value for the next DAC index to be read.
When SR7 D2 = 0,
D[7:0] DAC Data [7:0]
When SR7 D2 = 0, the 24-bit LUT is enabled. This LUT can translate the R, G, B values into new R, G, B values independently. This LUT can be used for performing GAMMA correction function. The programming procedure is same as standard LUT when SR7 D2 = 1.

PEL MASK REGISTER
Register Type: Read/Write
Read/Write Port: 3C6
Default: 00h
D[7:0] Pixel Mask Bit[7:0]
This field is the Pixel Mask for the palette DAC. If a bit in this field is programmed to a '0', the corresponding bit in the pixel data will be ignored in looking up an entry in the LUT.

8.7. EXTENDED REGISTERS

8.7.1. EXTENDED INDEX REGISTER

Register Type: Read/Write
Read/Write Port: 3C4
Default: 00h
D[7:6] Reserved
D[5:0] Extended Register Index Bit[5:0] (05h ~ 37h)

Table 8.7-1 Table of Extended Registers

INDEX (3C4)	EXTENDED ENHANCED REGISTER (3C5)
05h	Extended Password/Identification Register
06h	Extended Graphics Mode Control Register
07h	Extended Misc. Control Register 0
08h	Extended CRT/CPU Threshold Control Register 0
09h	Extended CRT/CPU Threshold Control Register 1
0Ah	Extended CRT Overflow Register
0Bh	Extended Misc. Control Register 1
0Ch	Extended Misc. Control Register 2
0Dh	Extended Configuration Status 0

0Eh	Extended Configuration Status 1
0Fh	Extended Scratch Register 0
10h	Extended Scratch Register 1
11h	Extended DDC and Power Control Register
12h	Extended Horizontal Overflow Register
13h	Extended Clock Generator Register
13h	Extended 25Mhz Video Clock Register 2
13h	Extended 28Mhz Video Clock Register 2
14h	Extended Hardware Cursor Color 0 Red Register
15h	Extended Hardware Cursor Color 0 Green Register
16h	Extended Hardware Cursor Color 0 Blue Register
17h	Extended Hardware Cursor Color 1 Red Register
18h	Extended Hardware Cursor Color 1 Green Register
19h	Extended Hardware Cursor Color 1 Blue Register
1Ah	Extended Hardware Cursor Horizontal Start Register 0
1Bh	Extended Hardware Cursor Horizontal Start Register 1
1Ch	Extended Hardware Cursor Horizontal Preset Register
1Dh	Extended Hardware Cursor Vertical Start Register 0
1Eh	Extended Hardware Cursor Vertical Start Register 1
1Fh	Extended Hardware Cursor Vertical Preset Register
20h	Extended Linear Addressing Base Address Register 0
21h	Extended Linear Addressing Base Address Register 1
22h	Extended Standby/Suspend Timer Register
23h	Extended Misc. Control Register 3
24h	Extended Reserved Register
25h	Extended Scratch Register 2
26h	Extended Graphics Engine Register 0
27h	Extended Graphics Engine Register 1
28h	Extended Internal Memory Clock Register 0
29h	Extended Internal Memory Clock Register 1
2Ah	Extended Internal Video Clock Register 0
2Ah	Extended 25Mhz Video Clock Register 0
2Ah	Extended 28Mhz Video Clock Register 0
2Bh	Extended Internal Video Clock Register 1
2Bh	Extended 25Mhz Video Clock Register 1
2Bh	Extended 28Mhz Video Clock Register 1
2Ch	Extended Turbo Queue Base Address
2Dh	Extended Memory Start Control Register
2Eh	Extended Reserved Register
2Fh	Extended DRAM Frame Buffer Size Register
30h	Extended Fast Page Flip Starting Address Low Register
31h	Extended Fast Page Flip Starting Address Middle Register
32h	Extended Fast Page Flip Starting Address High Register
33h	Extended Misc. Control Register 4
34h	Extended Misc. Control Register 5
35h	Extended Misc. Control Register 6
36h	Extended Scratch Register 3
37h	Extended Scratch Register 4

38h	Extended Misc. Control Register 7
39h	Extended Misc. Control Register 8
3Ah	Extended MPEG Turbo Queue Base Address
3Bh	Extended Clock Generator Control Register
3Ch	Extended Misc. Control Register 9
3Dh	Extended Misc. Control Register 10
3Eh	Extended Misc. Control Register 11
3Fh	Extended Misc. Control Register 12

SR5: EXTENDED PASSWORD/IDENTIFICATION REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 05h
Default: 00h

D[7:0] Password/Identification Bit[7:0]
If 86h is written into this register, then A1h will be read from this register, and unlock all the extension registers.
If the value other than 86h is written into this register, then 21h will be read from this register, and lock all the extension registers.

SR6: EXTENDED GRAPHICS MODE CONTROL REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 06h
Default: 00h

D7 Graphics mode linear addressing enable
0: Disable
1: Enable

D6 Graphics mode hardware cursor display enable
0: Disable
1: Enable

D5 Graphics mode interlaced enable
0: Disable
1: Enable

D4 True-Color graphics mode enable
0: Disable
1: Enable

D3 64K-Color graphics mode enable
0: Disable
1: Enable

D2 32K-Color graphics mode enable
0: Disable
1: Enable

D1 Enhanced graphics mode enable
0: Disable
1: Enable

D0 Enhanced text mode enable
0: Disable
1: Enable

SR7: EXTENDED MISC. CONTROL REGISTER 0

Register Type: Read/Write

Read/Write Port: 3C5, Index 07h
Default: 00h

D7 Merge video line buffer into CRT FIFO
0: Disable
1: Enable
The size of CRT FIFO can be set to 256x64 bit when merged with video line buffer only when video playback is disabled.

D6 Reserved

D5 Internal RAMDAC power saving mode
0: Power saving mode
1: High power mode

D4 Extended video clock frequency divided by 2
0: Disable
1: Enable

D3 Enable multi-line pre-fetch function
0: Enable
1: Disable

D2 24-bit color palette enable for direct color mode
0: Enable
1: Disable

D1 High Speed DAC operation bit [0]
(Please refer to SR3F, D[7])
This bit should be set when DCLK frequency is greater than 135MHz

D0 External DAC reference voltage input
0: Internal DAC reference voltage
1: External DAC reference voltage
To achieve more accurate reference voltage. The reference voltage of DAC can be input from external.

SR8: EXTENDED CRT/CPU THRESHOLD CONTROL REGISTER 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 08h
Default: 00h
D[7:4] CRT/CPU Arbitration Threshold Low Bit[3:0]
D[3:0] CRT/Engine Threshold High Bit[3:0]

SR9: EXTENDED CRT/CPU THRESHOLD CONTROL REGISTER 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 09h
Default: 00h
D7 Select 32-bpp format true color mode
D[6:4] ASCII/Attribute Threshold Bit[2:0]
D[3:0] CRT/CPU Threshold High Bit[3:0]

SRA: EXTENDED CRT OVERFLOW REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Ah
Default: 00h
D[7:4] Extended Screen Offset Bit[11:8]
D3 Extended Vertical Retrace Start Bit[10]
D2 Extended Vertical Blank Start Bit[10]

D1	Extended Vertical Display Enable End Bit[10]
D0	Extended Vertical Total Bit[10]

SRB: EXTENDED MISC. CONTROL REGISTER 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Bh
Default: 00h

D7	True-Color Graphics mode RGB Sequence Selection 0: Red, Green, and Blue in byte order 1: Blue, Green, and Red in byte order
D[6:5]	Memory-mapped I/O Space Selection Bit[1:0] 00: Disable 01: Select Axxxxh as Memory-mapped I/O Space 10: Select Bxxxxh as Memory-mapped I/O Space 11: Select PCI config register 14h as Memory-mapped I/O space
D4	True-Color frame rate modulation enable 0: Disable 1: Enable
D3	Dual segment register mode enable 0: Disable 1: Enable
D2	I/O gating enable while write-buffer is not empty 0: Disable 1: Enable
D1	16-color packed pixel enable 0: Disable 1: Enable
D0	CPU-driven BITBLT operation enable 0: Disable 1: Enable

SRC: EXTENDED MISC. CONTROL REGISTER 2

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Ch
Default: 00h

D7	Graphics mode 32-bit memory access enable 0: Disable 1: Enable
D6	Text mode 16-bit memory access enable 0: Disable 1: Enable
D5	Read-ahead cache operation enable 0: Disable 1: Enable
D3	Test mode enable 0: Disable 1: Enable
D[4, 2:1]	Memory Configuration Bit[2:0] 000: 1MByte/1 bank 001: 2MByte/2 banks 010: 4MByte/2 banks or 4 banks

011: Reserved
100: Reserved
101: 2MByte/1 banks
110: 4MByte/1 banks
111: 8MByte/2 banks

D0 Synchronous reset timing generator enable
0: Disable
1: Enable

SRD: EXTENDED CONFIGURATION STATUS 0

Register Type: Read Only
Read Port: 3C5, Index 0Dh
Default: 00h

D7 Leading MCLK bit[0] Status
This bit will present the status of trapping of MD36.
Please refer to H/W trapping section for more details.

D6 Internal Clock Generator Status
0: Select external clock generator
1: Select internal clock generator
This bit will present the status of trapping of ENVCO.

D5 Memory clock select bit[1] on local frame buffer.
This bit will present the status of trapping of VMD62.

D4 Internal AGP bus Status
0: Disable internal AGP Bus
1: Enable internal AGP bus
This bit will present the status of trapping of MD52.

D3 Memory clock select bit[0] on local frame buffer.
This bit will present the status of trapping of VMD63.

D2 Leading MCLK bit[3] Status
This bit will present the status of trapping of MD39.
Please refer to H/W trapping section for more details.

D1 Video Subsystem Control Status
This bit will present the status of trapping of MD49.
When this bit is present 0 that means this function is controlled by BIOS.

D0 Shared Frame buffer/Local Frame buffer Status
0: Local Frame Buffer Mode
1: Shared Frame Buffer Mode
This bit will present the status of trapping of MD48.

SRE: EXTENDED CONFIGURATION STATUS 1

Register Type: Read Only
Read Port: 3C5, Index 0Eh
Default: 00h

D7 Select SGRAM/SDRAM type on local frame buffer.
0: SDRAM
1: SGRAM
This bit will present the status of trapping of VMD61.

D6 Integrated VGA Controller Status
0: Disable
1: Enable

This bit will present the status of trapping of MD62.

D5 Host bus Decoding Mode Status
0: Slow
1: Fast
This bit will present the status of trapping of MD61.

D4 Reserved

D3 Support INT#A for Digital Flat Panel Interface Status
0: Disable
1: Enable
This bit will present the status of trapping of MD59.

D2 Reserved for MD58 status

D1 Leading MCLK bit[2] Status
This bit will present the status of trapping of MD38.
Please refer to H/W trapping section for more details.

D0 Leading MCLK bit[1] Status
This bit will present the status of trapping of MD37.
Please refer to H/W trapping section for more details.

SRF: EXTENDED SCRATCH REGISTER 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Fh
Default: 00h
D[7:0] Reserved for video BIOS

SR10: EXTENDED SCRATCH REGISTER 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 10h
Default: 00h
D[7:0] Reserved for video BIOS

SR11: EXTENDED DDC AND POWER CONTROL REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 11h
Default: 00h

D7 Force VGA into suspend mode
0: Disable
1: Enable

D6 Force VGA into standby mode
0: Disable
1: Enable

D5 Enable video memory access as activation source
0: Disable
1: Enable

D4 Enable keyboard and hardware cursor as system activation source
0: Disable
1: Enable

D3 Enable ACPI Power Management
0: Disable
1: Enable

D2 Reserved

D1 DDC DATA Programming

While writing this bit,
0: Output '0' logic into DDC Data Signal.
1: Output '1' logic into DDC Data Signal.
While reading this bit,
0: Get '0' logic from DDC Data Signal .
1: Get '1' logic from DDC Data Signal .

D0 DDC CLK Programming
While writing this bit,
0: Output '0' logic into DDC Clock Signal.
1: Output '1' logic into DDC Clock Signal.
While reading this bit,
0: Get '0' logic from DDC Clock Signal .
1: Get '1' logic from DDC Clock Signal .

SR12: EXTENDED HORIZONTAL OVERFLOW REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 12h
Default: 00h

D[7:5] Horizontal Retrace Skew
000 : no delay
001 : delay 1 DCLK
010 : delay 2 DCLK
011 : delay 3 DCLK
100 : delay 4 DCLK
101 : delay 5 DCLK
110 : delay 6 DCLK
111 : delay 7 DCLK

D4 Extended Horizontal Blank End Bit[6]
D3 Extended Horizontal Retrace Start Bit[8]
D2 Extended Horizontal Blank Start Bit[8]
D1 Extended Horizontal Display Enable End Bit[8]
D0 Extended Horizontal Total Bit[8]

SR13: EXTENDED CLOCK GENERATOR REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 13h
Default: 00h
D7 MCLK Post-scale Bit[2]
D6 Internal VCLK Post-Scale Bit[2]
D[5:0] Reserved

SR13-1: EXTENDED 25MHZ VIDEO CLOCK REGISTER 2

Register Type: Read/Write
Read/Write Port: 3C5, Index 13h
Default: 00h
D7 Reserved
D6 25Mhz VCLK Post-Scale Bit[2]
D[5:0] Reserved

SR13-2: EXTENDED 28MHZ VIDEO CLOCK REGISTER 2

Register Type: Read/Write

Read/Write Port: 3C5, Index 13h
Default: 00h
D7 Reserved
D6 28Mhz VCLK Post-Scale Bit[2]
D[5:0] Reserved

SR14: EXTENDED HARDWARE CURSOR COLOR 0 RED REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 14h
Default: 00h
D[7:6] Reserved
D[5:0] Hardware Cursor Color 0 Red Bit[5:0]

SR15: EXTENDED HARDWARE CURSOR COLOR 0 GREEN REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 15h
Default: 00h
D[7:6] Reserved
D[5:0] Hardware Cursor Color 0 Green Bit[5:0]

SR16: EXTENDED HARDWARE CURSOR COLOR 0 BLUE REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 16h
Default: 00h
D[7:6] Reserved
D[5:0] Hardware Cursor Color 0 Blue Bit[5:0]

SR17: EXTENDED HARDWARE CURSOR COLOR 1 RED REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 17h
Default: 00h
D[7:6] Reserved
D[5:0] Hardware Cursor Color 1 Red Bit[5:0]

SR18: EXTENDED HARDWARE CURSOR COLOR 1 GREEN REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 18h
Default: 00h
D[7:6] Reserved
D[5:0] Hardware Cursor Color 1 Green Bit[5:0]

SR19: EXTENDED HARDWARE CURSOR COLOR 1 BLUE REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 19h
Default: 00h
D[7:6] Reserved
D[5:0] Hardware Cursor Color 1 Blue Bit[5:0]

SR1A: EXTENDED HARDWARE CURSOR HORIZONTAL START REGISTER 0

Register Type: Read/Write

Read/Write Port: 3C5, Index 1Ah
Default: 00h
D[7:0] Hardware Cursor Horizontal Start Bit[7:0]

SR1B: EXTENDED HARDWARE CURSOR HORIZONTAL START REGISTER 1
Register Type: Read/Write
Read/Write Port: 3C5, Index 1Bh
Default: 00h
D7 Enable hardware cursor using memory-mapped I/O
0: Disable
1: Enable
D[6:4] Reserved
D[3:0] Hardware Cursor Horizontal Start Bit[11:8]

SR1C: EXTENDED HARDWARE CURSOR HORIZONTAL PRESET REGISTER
Register Type: Read/Write
Read/Write Port: 3C5, Index 1Ch
Default: 00h
D[7:6] Reserved
D[5:0] Hardware Cursor Horizontal Preset Bit[5:0]

SR1D: EXTENDED HARDWARE CURSOR VERTICAL START REGISTER 0
Register Type: Read/Write
Read/Write Port: 3C5, Index 1Dh
Default: 00h
D[7:0] Hardware Cursor Vertical Start Bit[7:0]

SR1E: EXTENDED HARDWARE CURSOR VERTICAL START REGISTER 1
Register Type: Read/Write
Read/Write Port: 3C5, Index 1Eh
Default: 00h
D[7:4] Hardware Cursor Pattern Select Bit[3:0]
D3 Hardware Cursor Side Pattern Enable
0: Disable
1: Enable
D[2:0] Hardware Cursor Vertical Start Bit[10:8]

SR1F: EXTENDED HARDWARE CURSOR VERTICAL PRESET REGISTER
Register Type: Read/Write
Read/Write Port: 3C5, Index 1Fh
Default: 00h
D[7:6] Reserved
D[5:0] Hardware Cursor Vertical Preset Bit[5:0]

SR20: EXTENDED LINEAR ADDRESSING BASE ADDRESS REGISTER 0
Register Type: Read/Write
Read/Write Port: 3C5, Index 20h
Default: 00h
D[7:0] Linear Addressing Base Address Bit[26:19]

SR21: EXTENDED LINEAR ADDRESSING BASE ADDRESS REGISTER 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 21h
Default: 00h

D[7:5] Linear Addressing Space Aperture Bit[2:0]
- 000: 512 Kbyte
- 001: 1 Mbyte
- 010: 2 Mbyte
- 011: 4 Mbyte
- 100: 8 Mbyte
- Others: Reserved

D[4:0] Linear Addressing Base Address Bit[31:27]

SR22: EXTENDED STANDBY/SUSPEND TIMER REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 22h
Default: 00h

D[7:4] Suspend Timer Bit[3:0]
The resolution for Suspend Timer is 2 minutes.

D[3:0] Standby Timer Bit[3:0]
The resolution for Standby Timer is 2 minutes.

SR23: EXTENDED MISC. CONTROL REGISTER 3

Register Type: Read/Write
Read/Write Port: 3C5, Index 23h
Default: 00h

D7 Reserved

D6 CRC Generator Enable
- 0: Disable
- 1: Enable

D5 Reserved

D4 Bypass SRAM
- 0: Disable
- 1: Enable

D3 Video Compatible Hardware Cursor Visibility Enable
- 0: Disable
- 1: Enable

D[2:0] DRAM Control Signal Delay Compensation Bit[1:0]
- 000: Delay 4 ns
- 001: Delay 5 ns
- 010: Delay 6 ns
- 011: Delay 7 ns
- 100: Delay 8 ns
- 101: Delay 9 ns
- 110: Delay 10 ns
- 111: Delay 11 ns

SR24: EXTENDED RESERVED REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 24h
Default: 00h

D[7:0] Reserved

SR25: EXTENDED SCRATCH REGISTER 2

Register Type: Read/Write
Read/Write Port: 3C5, Index 25h
Default: 00h
D[7:0] Reserved for VGA BIOS

SR26: EXTENDED GRAPHICS ENGINE REGISTER 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 26h
Default: 00h
D7 Reserved
D6 Power-down Internal RAMDAC
0: Disable
1: Enable
D[5] Reserved
D[4] Continuous Memory Data Access
D[3:1] Reserved
D[0] Extended Screen Start Address Brt [20]

SR27: EXTENDED GRAPHICS ENGINE REGISTER 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 27h
Default: 00h
D7 Turbo Queue Engine enable
0: Disable
1: Enable
D6 Graphics Engine Register Programming enable
0: Disable
1: Enable
D[5:4] Logical Screen Width and Byte-Per-Pixel Select Bit[1:0]
00 1024, 256 colors or 512, 32k/64k colors
01 2048, 256 colors or 1024, 32k/64k colors
10 4096, 256 colors or 2048, 32k/64k colors
11 invalid
D[3:0] Extended Screen Start Address Bit[19:16]

SR28: EXTENDED INTERNAL MEMORY CLOCK REGISTER 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 28h
Default: 00h
D[7] MCLK Divider
0: Do not divide
1: Divide by 2
D[6:0] MCLK Numerator Bit[6:0]
[0000000:1111111] = [1:128]

NOTE: For the operation of internal memory clock generation, please refer to " the section of Internal Dual-Clock Synthesizer".

SR29: EXTENDED INTERNAL MEMORY CLOCK REGISTER 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 29h
Default: 00h

D7 MCLK VCO Gain
0: Gain for low frequency operation
1: Gain for high frequency operation

D[6:5] MCLK Post-Scale Bit[1:0]
When SR13 D7=0
00: Do not scale
01: Scaled by 2
10: Scaled by 3
11: Scaled by 4
When SR13 D7=1
00: Reserved
01: Reserved
10: Scaled by 6
11: Scaled by 8

D[4:0] MCLK DeNumerator Bit[4:0]
[00000:11111] = [1:32]

NOTE: For the operation of internal memory clock generation, please refer to "the section of Internal Dual-Clock Synthesizer".

SR2A: EXTENDED INTERNAL VIDEO CLOCK REGISTER 0

Register Type: Read/Write
Read/Write Port: 3C5h,Index 2Ah
Default: 00h

D[7] Internal VCLK Divider
0: Do not divide
1: Divide by 2

D[6:0] Internal VCLK Numerator Bit[6:0]
[0000000:1111111] = [1:128]

NOTE: For the operation of internal video clock generation, please refer to "the section of Internal Dual-Clock Synthesizer ".

SR2A-1: EXTENDED 25MHZ VIDEO CLOCK REGISTER 0

Register Type: Read/Write
Read/Write Port: 3C5h,Index 2Ah
Default: 00h

D[7] 25Mhz VCLK Divider
0: Do not divide
1: Divide by 2

D[6:0] 25Mhz VCLK Numerator Bit[6:0]
[0000000:1111111] = [1:128]

SR2A-2: EXTENDED 28MHZ VIDEO CLOCK REGISTER 0

Register Type: Read/Write
Read/Write Port: 3C5h,Index 2Ah
Default: 00h

D[7] 28Mhz VCLK Divider
0: Do not divide

1: Divide by 2

D[6:0] 28Mhz VCLK Numerator Bit[6:0]
[0000000:1111111] = [1:128]

SR2B: EXTENDED INTERNAL VIDEO CLOCK REGISTER 1

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Bh
Default: 00h

D7 Internal VCLK VCO Gain
0: Gain for low frequency operation
1: Gain for high frequency operation

D[6:5] Internal VCLK Post-Scale Bit[1:0]
When SR13 D6 = 0
00: Do not scale
01: Scaled by 2
10: Scaled by 3
11: Scaled by 4
When SR13 D6 = 1
00: Reserved
01: Reserved
10: Scaled by 6
11: Scaled by 8

D[4:0] Internal VCLK DeNumerator Bit[4:0]
[00000:11111] = [1:32]

NOTE: For the operation of internal video clock generation, please refer to "the section of Internal Dual-Clock Synthesizer".

SR2B-1: EXTENDED 25MHZ VIDEO CLOCK REGISTER 1

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Bh
Default: 00h

D7 25MHz VCLK VCO Gain
0: Gain for low frequency operation
1: Gain for high frequency operation

D[6:5] 25MHz VCLK Post-Scale Bit[1:0]
When SR13-1 D6 = 0
00: Do not scale
01: Scaled by 2
10: Scaled by 3
11: Scaled by 4
When SR13-1 D6 = 1
00: Reserved
01: Reserved
10: Scaled by 6
11: Scaled by 8

D[4:0] 25MHz VCLK DeNumerator Bit[4:0]
[00000:11111] = [1:32]

SR2B-2: EXTENDED 28MHZ VIDEO CLOCK REGISTER 1

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Bh

Default: 00h
D7 28MHz VCLK VCO Gain
0: Gain for low frequency operation
1: Gain for high frequency operation
D[6:5] 28MHz VCLK Post-Scale Bit[1:0]
When SR13-2 D6= 0,
00: Do not scale
01: Scaled by 2
10: Scaled by 3
11: Scaled by 4
When SR13B D6= 1
00: Reserved
01: Reserved
10: Scaled by 6
11: Scaled by 8
D[4:0] 28MHz VCLK DeNumerator Bit[4:0]
[00000:11111] = [1:32]

SR2C: EXTENDED TURBO QUEUE BASE ADDRESS

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Ch
Default: 00h
D7 Turbo Queue Base Address Bit[7]
D[6:0] Turbo Queue Base Address Bit[6:0]

SR2D: EXTENDED MEMORY START CONTROL REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 2Dh
Default: 00h
D[7:4] Reserved
D[3:0] Page Size Select
0000: 2 KB at 32-bit mode, 4 KB at 64-bit mode
0001: 4 KB at 32-bit mode, 8 KB at 64-bit mode
0010: 8 KB at 32-bit mode, 16 KB at 64-bit mode
0011: 16 KB at 32-bit mode, 32 KB at 64-bit mode
0100: 1 KB at 32-bit mode, 2 KB at 64-bit mode
Others: Reserved

SR2E: EXTENDED RESERVED REGISTER

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Eh
Default: 00h
D[7:4] DRAM scramble table Bit[3:0] on shared frame buffer mode.
D[3:0] Reserved

SR2F: EXTENDED DRAM FRAME BUFFER SIZE REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 2Fh
Default: 00h
D[7:6] Reserved

D5	Enable Fast Change Mode Timing 0: Disable 1: Enable
D4	Enable Fast Page Flip 0: Disable 1: Enable
D[3:2]	Reserved
D[1:0]	Shared Frame Buffer Size 00: Reserved 01: 2 MB 10: 4 MB 11: 8MB

SR30: EXTENDED FAST PAGE FLIP STARTING ADDRESS LOW REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 30h
Default: 00h

D[7:0]	Fast page flip starting address bit[7:0]

SR31: EXTEND FAST PAGE FLIP STARTING ADDRESS MIDDLE REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 31h
Default: 00h

D[7:0]	Fast page flip start address bit[15:8]

SR32: EXTENDED FAST PAGE FLIP STARTING ADDRESS HIGH REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 32h
Default: 00h

D[7:5]	Reserved
D[4]	Fast page flip start address bit[2:0]
D[3:0]	Fast page flip start address bit[19:16]

Note: The fast page flip starting address is latched when SR32 is written. So the registers, SR30 and SR31, should be programmed before SR32. These registers are enabled by setting SR2F D4.

SR33: EXTENDED MISC. CONTROL REGISTER 4

Register Type: Read/Write
Read/Write Port: 3C5, Index 33h
Default: 00h

D7	Reserved
D6	Select external 14MHz(OSCI) as MCLK (Shared Frame Buffer Mode Only) 0: Disable 1: Enable
D5	Relocated VGA I/O port addresses decoding disable 0: Disable 1: Enable The standard VGA register I/O port address can be relocated to address defined by PCI Config Register 18h. This bit disable the relocated address decoding.
D4	Standard VGA I/O port addresses decoding enable

0: Enable
1: Disable
The standard VGA register I/O port address decoding can be disabled by this bit.

D3 Reserved

D2 Select SGRAM Latency
0: Latency = 3T
1: Latency = 2T

D1 Enable SGRAM Mode Write timing
0: Disable
1: Enable
This bit must be set before accessing SGRAM. It must clear to 0 before setting to 1 to generate a new Mode Write cycle.

D0 Enable SGRAM timing
0: Disable
1: Enable

SR34: EXTENDED MISC. CONTROL REGISTER 5

Register Type: Read/Write
Read/Write Port: 3C5, Index 34h
Default: 00h

D7 DRAM controller one cycle write enable
0: Disable
1: Enable

D6 DRAM controller one cycle read enable
0: Enable
1: Disable

D[5:3] Reserved

D2 Enable MD output PAD low Driving
0: Disable
1: Enable

D1 Enable CRT Low request on UMA mode.

D0 Enable Hardware Command Queue threshold low
0: Disable
1: Enable

SR35: EXTENDED MISC. CONTROL REGISTER 6

Register Type: Read/Write
Read/Write Port: 3C5, Index 35h
Default: 00h

D7 Reserved

D6 Enable MA output PAD low Driving
0: Disable
1: Enable

D5 SGRAM burst timing enable
0: Enable
1: Disable

D4 Enable Host Bus burst write zero-wait
0: Disable
1: Enable

D[3:2] DRAM DQM LOW period width compensation bit[1:0]

00: Add 0ns
01: Add 2ns
10: Add 4ns
11: Add 6ns

SR36: EXTENDED SCRATCH REGISTER 3

Register Type: Read/Write
Read/Write Port: 3C5, Index 36h
Default: 00h

D[7:0]	Reserved for VGA BIOS

SR37: EXTENDED SCRATCH REGISTER 4

Register Type: Read/Write
Read/Write Port: 3C5, Index 37h
Default: 00h

D[7:0]	Reserved for VGA BIOS

SR38: EXTENDED MISC. CONTROL REGISTER 7

Register Type: Read/Write
Read/Write Port: 3C5, Index 38h
Default: 00h

D[7:4]	Hardware Cursor Location Hardware Cursor Starting Address Bit[21:18]
D3	PCI read cache time-out function enable 0: Enable 1: Disable
D2	Disable Line compare 0: Enable 1: Disable
D[1:0]	Video Clock Register Selection Bit[1:0] 00: Select Internal Video Clock Registers SR13, SR2A, SR2B 01: Select 25MHz Video Clock Registers SR13, SR2A-1, SR2B-1 10: Select 28MHz Video Clock Registers SR13, SR2A-2, SR2B-2 11: Reserved

There are three video clock registers Internal Video Clock Registers, 25Mhz Video Clock Registers, 28Mhz Video Clock Registers. All three registers use the same index of 3C5, index 13h, 2Ah and 2Bh. The selection is programmed by Video Clock Register Selection Bit[1:0]. The VCLK frequency is generated from Internal Video Clock Registers when Miscellaneous Output Register (write port 3C2) Bit[3:2]=11. The VCLK frequency is generated from 25Mhz Video Clock Registers when Miscellaneous Output Register (write port 3C2) bit[3:2]=00. The VCLK frequency is generated from 28Mhz Video Clock Registers when Miscellaneous Output Register (write port 3C2) bit[3:2]=01.

39: EXTENDED MISC. CONTROL REGISTER 8

Register Type: Read/Write
Read/Write Port: 3C5, Index 39h
Default: 00h
D[7:3] Reserved
D2 3D Accelerator Control
0: Disable
1: Enable
D[1:0] Reserved

SR3A: RESERVED

SR3B: EXTENDED CLOCK GENERATOR CONTROL REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 3Bh
Default: 00h
D[7:6] Video clock generator damping control bit[1:0]
D[5:4] Reserved
D[3:2] Memory clock generator damping control bit[1:0]
D[1:0] Reserved

SR3C: EXTENDED MISC. CONTROL REGISTER 9

Register Type: Read/Write
Read/Write Port: 3C5, Index 3Ch
Default: 00h
D7 Enable DRAM control signal output PAD low Driving
0: Disable
1: Enable
D6 Enable SCLK output PAD high Driving.
0: Disable
1: Enable
D[5:0] Reserved

SR3D: EXTENDED MISC. CONTROL REGISTER 10

Register Type: Read/Write
Read/Write Port: 3C5, Index 3Dh
Default: 00h
D7 Enable 2D/3D software queue 62K bytes
0: software queue 30K bytes
1: software queue 62K bytes
D6 DRAM Handshaking signal delay bit 2 (Shared Frame Buffer Mode only)
D5 Reserved
D[4:3] DRAM Handshaking signal delay bit [1:0] (Shared Frame Buffer Mode only)
D2 Disable standard display memory (A0000~BFFFF) access
0: Enable
1: Disable
D1 Enable CRT end of line detection
0: Disable
1: Enable
D0 Enable 3D pre-setup engine

0: Disable
1: Enable

SR3E: EXTENDED MISC. CONTROL REGISTER11

Register Type: Read/Write
Read/Write Port: 3C5, Index 3Eh
Default: 00h

D7 Enable DCLK off
0: Disable
1: Enable

D[6:5] AGP Control signal delay compensation Bit [1:0]
00: delay 0 ns
01: delay 1 ns
10: delay 2 ns
11: delay 3 ns

D4 Select type of 16Mb (512k*32) when using SGRAM
0: Select SGRAM of 8Mb (256k*32)
1: Select SGRAM of 16Mb (512k*32)

D3 Enable DRAM controller stick to texture-read request
0: Disable
1: Enable

D2 Hardware cursor starting address bit[22]

D1 Enable block write function when using SGRAM
0: Disable
1: Enable

D0 Enable high speed DCLK
0: Disable
1: Enable

SR3F: EXTENDED MISC. CONTROL REGISTER12

Register Type: Read/Write
Read/Write Port: 3C5, Index 3Fh
Default: 00h

D[7] High speed DAC operation bit[1] (Please refer to SR7, D[1])

D[6:5] Enable CRT 32/64/256-stage threshold full control bit[1:0]
00: using CRT 32-stage threshold full
01: using CRT 64-stage threshold full
10: using CRT 63-stage threshold full
11: using CRT256-stage threshold full

D4 CRT/CPU Threshold High Bit[4]

D3 CRT/Engine Threshold High Bit[4]

D2 CRT/CPU Arbitration Threshold Low Bit[4]

D1 Enable Flat Panel Data/Control Out PAD low driving
0: Disable
1: Enable

D0 Reserved

The integrated graphics controller supports a powerful graphics engine to enhance the performance. The functions of the graphics engine in the integrated VGA controller include BitBlt, BitBlt with mask, Color/Font Expansion, Enhanced Color/Font Expansion, Line Drawing, and Direct Draw.

Since the register formats for the line drawing and Direct Draw are different from those of the other general engine functions, we would like to describe these three register formats separately in the following paragraphs:
-Register format for general engine functions
-Register format for line drawing
-Register format for direct draw

8.8. 2D GRAPHICS ENGINE REGISTERS

8.8.1. REGISTER FORMAT FOR GENERAL ENGINE FUNCTIONS

The integrated graphics controller supports a powerful graphics engine to enhance the performance. The functions of the graphics engine in it include BitBlt, Color Expansion, Enhanced Color Expansion, Line Drawing, Transparent BitBlt, Multiple Scan-line and Trapezoid Fill.

Since the register formats for the line drawing, transparent BitBlt, multiple scan-line and trapezoid fill are different from those of the other general engine functions, we would like to describe these five register formats separately in the following paragraphs:
Register Format for General Engine Functions

The following table shows the register format for the general Graphics Engine functions. The general Graphics Engine functions are BitBlt, Color Expansion and Enhanced Color Expansion.

Table8.8-1 Table of General Engine Register

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O Address
Source Base Address				8200h
Reserved		Source Pitch		8204h
Source X		Source Y		8208h
Destination X		Destination Y		820Ch
Destination Base Address				8210h
Destination Height		Destination Pitch		8214h
Rectangular Height		Rectangular Width		8218h
Pattern FG (Foreground) Color				821Ch
Pattern BG (Background) Color				8220h
Source FG (Foreground) Color				8224h
Source BG (Background) Color				8228h
Mask3	Mask2	Mask1	Mask0	822Ch
Mask7	Mask6	Mask5	Mask4	8230h
Top Clipping		Left Clipping		8234h
Bottom Clipping		Right Clipping		8238h
Command				823Ch
Command Queue Status				8240h
Pattern 3	Pattern 2	Pattern 1	Pattern 0	8300h
Pattern 7	Pattern 6	Pattern 5	Pattern 4	8304h
Pattern 11	Pattern 10	Pattern 9	Pattern 8	8308h
Pattern 15	Pattern 14	Pattern 13	Pattern 12	830Ch
Pattern 19	Pattern 18	Pattern 17	Pattern 16	8310h
Pattern 23	Pattern 22	Pattern 21	Pattern 20	8314h

Pattern 27	Pattern 26	Pattern 25	Pattern 24	8318h
Pattern 31	Pattern 30	Pattern 29	Pattern 28	831Ch
Pattern 35	Pattern 34	Pattern 33	Pattern 32	8320h
Pattern 39	Pattern 38	Pattern 37	Pattern 36	8324h
Pattern 43	Pattern 42	Pattern 41	Pattern 40	8328h
Pattern 47	Pattern 46	Pattern 45	Pattern 44	832Ch
Pattern 51	Pattern 50	Pattern 49	Pattern 48	8330h
Pattern 55	Pattern 54	Pattern 53	Pattern 52	8334h
Pattern 59	Pattern 58	Pattern 57	Pattern 56	8338h
Pattern 63	Pattern 62	Pattern 61	Pattern 60	833Ch
Pattern 67	Pattern 66	Pattern 65	Pattern 64	8340h
Pattern 71	Pattern 70	Pattern 69	Pattern 68	8344h
Pattern 75	Pattern 74	Pattern 73	Pattern 72	8348h
Pattern 79	Pattern 78	Pattern 77	Pattern 76	834Ch
Pattern 83	Pattern 82	Pattern 81	Pattern 80	8350h
Pattern 87	Pattern 86	Pattern 85	Pattern 84	8354h
Pattern 91	Pattern 90	Pattern 89	Pattern 88	8358h
Pattern 95	Pattern 94	Pattern 93	Pattern 92	835Ch
Pattern 99	Pattern 98	Pattern 97	Pattern 96	8360h
Pattern 103	Pattern 102	Pattern 101	Pattern 100	8364h
Pattern 107	Pattern 106	Pattern 105	Pattern 104	8368h
Pattern 111	Pattern 110	Pattern 109	Pattern 108	836Ch
Pattern 115	Pattern 114	Pattern 113	Pattern 112	8370h
Pattern 119	Pattern 118	Pattern 117	Pattern 116	8374h
Pattern 123	Pattern 122	Pattern 121	Pattern 120	8378h
Pattern 127	Pattern 126	Pattern 125	Pattern 124	837Ch
Pattern 131	Pattern 130	Pattern 129	Pattern 128	8380h
Pattern 135	Pattern 134	Pattern 133	Pattern 132	8384h
Pattern 139	Pattern 138	Pattern 137	Pattern 136	8388h
Pattern 143	Pattern 142	Pattern 141	Pattern 140	838Ch
Pattern 147	Pattern 146	Pattern 145	Pattern 144	8390h
Pattern 151	Pattern 150	Pattern 149	Pattern 148	8394h
Pattern 155	Pattern 154	Pattern 153	Pattern 152	8398h
Pattern 159	Pattern 158	Pattern 157	Pattern 156	839Ch
Pattern 163	Pattern 162	Pattern 161	Pattern 160	83A0h
Pattern 167	Pattern 166	Pattern 165	Pattern 164	83A4h
Pattern 171	Pattern 170	Pattern 169	Pattern 168	83A8h
Pattern 175	Pattern 174	Pattern 173	Pattern 172	83ACh
Pattern 179	Pattern 178	Pattern 177	Pattern 176	83B0h
Pattern 183	Pattern 182	Pattern 181	Pattern 180	83B4h
Pattern 187	Pattern 186	Pattern 185	Pattern 184	83B8h
Pattern 191	Pattern 190	Pattern 189	Pattern 188	83BCh
Pattern 195	Pattern 194	Pattern 193	Pattern 192	83C0h
Pattern 199	Pattern 198	Pattern 197	Pattern 196	83C4h
Pattern 203	Pattern 202	Pattern 201	Pattern 200	83C8h
Pattern 207	Pattern 206	Pattern 205	Pattern 204	83CCh
Pattern 211	Pattern 210	Pattern 209	Pattern 208	83D0h
Pattern 215	Pattern 214	Pattern 213	Pattern 212	83D4h

Pattern 219	Pattern 218	Pattern 217	Pattern 216	83D8h
Pattern 223	Pattern 222	Pattern 221	Pattern 220	83DCh
Pattern 227	Pattern 226	Pattern 225	Pattern 224	83E0h
Pattern 231	Pattern 230	Pattern 229	Pattern 228	83E4h
Pattern 235	Pattern 234	Pattern 233	Pattern 232	83E8h
Pattern 239	Pattern 238	Pattern 237	Pattern 236	83ECh
Pattern 243	Pattern 242	Pattern 241	Pattern 240	83F0h
Pattern 247	Pattern 246	Pattern 245	Pattern 244	83F4h
Pattern 251	Pattern 250	Pattern 249	Pattern 248	83F8h
Pattern 255	Pattern 254	Pattern 253	Pattern 252	83FCh

Source Base Address

Register Type: Read/Write
Read/Write Port: 8200h~8203h

D[31:23] Reserved
D[22:0] Base Linear Address of Source Bitmap in Byte
Limit: Source Bitmap Addressing Range is from 0 to 8M,
Quad-Word Boundary in BitBlt,
Byte Boundary in Enhanced Color Expansion.

Source Pitch

Register Type: Read/Write
Read/Write Port: 8204h~8205h

D[15:13] Reserved
D[12:0] Row Pitch of Source Bitmap in Byte.
Limit: Double Word Boundary in BitBlt,
Byte Boundary in Color Expansion and Enhanced Color Expansion.

Rectangle Source Y

Register Type: Read/Write
Read/Write Port: 8208h~8209h

D[15:12] Reserved
D[11:0] Started Y Coordinate of Source Bitmap in Pixel

Rectangle Source X

Register Type: Read/Write
Read/Write Port: 820Ah~820Bh

D[15:12] Reserved
D[11:0] Started X Coordinate of Source Bitmap in Pixel

Rectangle Destination Y

Register Type: Read/Write
Read/Write Port: 820Ch~820Dh

D[15:12] Reserved
D[11:0] Started Y Coordinate of Destination Bitmap in Pixel

Rectangle Destination X

Register Type: Read/Write
Read/Write Port: 820Eh~820Fh

D[15:12]	Reserved
D[11:0]	Started X Coordinate of Destination Bitmap in Pixel

Destination Base Address

Register Type: Read/Write
Read/Write Port: 8210h~8213h

D[31:23]	Reserved
D[22:0]	Base Linear Address of Destination Bitmap in Byte Limit: Destination Bitmap Addressing Range is from 0 to 8M, Quad-Word Boundary.

Destination Pitch

Register Type: Read/Write
Read/Write Port: 8214h~8215h

D[15:13]	Reserved
D[12:0]	Row Pitch of Destination Bitmap in Byte Limit: Double Word Boundary.

Destination Height

Register Type: Read/Write
Read/Write Port: 8216h~8217h

D[15:13]	Reserved
D[12:0]	Device Height of Destination Bitmap in Pixel

Rectangular Width

Register Type: Read/Write
Read/Write Port: 8218h~8219h

D[15:13]	Reserved
D[12:0]	Destination Rectangular Drawing Width of Bitmap in Pixel

Rectangular Height

Register Type: Read/Write
Read/Write Port: 821Ah~821Bh

D[15:13]	Reserved
D[12:0]	Destination Rectangular Drawing Height of Bitmap in Pixel

Pattern Foreground Color

Register Type: Read/Write
Read/Write Port: 821Ch~821Fh

D[31:0]	Foreground Color Register of Pattern

Pattern Background Color

Register Type: Read/Write
Read/Write Port: 8220h~8223h

D[31:0] Background Color Register of Pattern

Source Foreground Color

Register Type: Read/Write
Read/Write Port: 8224h~8227h

D[31:0] Foreground Color Register of Source

Source Background Color

Register Type: Read/Write
Read/Write Port: 8228h~822Bh

D[31:0] Background Color Register of Source

Mono Mask Register

Register Type: Read/Write
Read/Write Port: 822Ch~8233h

D[63:0] Monochrome Mask Register of Pattern

Left Clipping

Register Type: Read/Write
Read/Write Port: 8234h~8235h

D[15:0] Left Bound of Rectangular Clipping in Pixel
Limit: In the 2's complement format.

Top Clipping

Register Type: Read/Write
Read/Write Port: 8236h~8237h

D[15:0] Top Bound of Rectangular Clipping in Pixel
Limit: In the 2's complement format.

Right Clipping

Register Type: Read/Write
Read/Write Port: 8238h~8239h

D[15:0] Right Bound of Rectangular Clipping in Pixel
Limit: In the 2's complement format.

Bottom Clipping

Register Type: Read/Write
Read/Write Port: 823Ah~823Bh

D[15:0] Bottom Bound of Rectangular Clipping in Pixel
Limit: In the 2's complement format.

Command Register

Register Type: Read/Write
Read/Write Port: 823Ch~823Fh

D[31:27] Reserved
D26 Rectangular Clipping Merge Control

0: Merge clipping bound with screen bound
1: Do not merge clipping bound with screen bound

D[25:24] Reserved

D[23:21] Enhanced Color Expansion Pixel Preset
Limit: Preset must "000" in color expansion command

D20 Transparent Control
0: Opaque
1: Transparent

D19 Reserved

D18 Rectangular Clipping Control
0: Disable rectangular clipping logic
1: Enable rectangular clipping logic

D17 Y direction control
0: Y counter decrease
1: Y counter increase

D16 X direction control
0: X counter decrease
1: X counter increase

D[15:8] 256 Raster Operations

D[7:6] Pattern select bit 1-0
00: Pattern is from pattern foreground color register
01: Pattern is from pattern register
10: Pattern is from monochrome mask register
11: Reserved

D[5:4] Source select
00: Source is from video memory
01: Source is from CPU-driven BitBlt buffer
10: Reserved
11: Reserved

D[3:0] Command type select Bit[3:0]
0000: BitBlt
0001:Color Expansion
0010:Enhanced Color Expansion
0011:Multiple Scanline
0100:Line Draw
0101:Trapezoid Fill
0110:Transparent BitBlt
Others: Reserved

Command Queue Status

Register Type: Read
Read/Write Port: 8240h~8243h

D31 2D graphics engine is idle
0: 2D graphics engine is busy
1: 2D graphics engine is idle

D30 3D engine is idle
0: 3D engine is busy
1: 3D engine is idle

D29 Command queue is empty
0: Command queue is not empty

1: Command queue is empty
D[28:24] Current CPU-driven BitBlt buffer stages Bit[4:0]
D23 Status of enhanced color expansion command
0: Command is not in queue
1: Command is in queue
D[22:13] reserved
D[12:0] Available queue length Bit[12:0]

Pattern Register n

Register Type: Read/Write
Read/Write Port: 8300h~833Fh for 256-color
8300h~837Fh for high-color
8300h~83FFh for true-color

D[7: 0] For BitBlt and Enhanced Color Expansion function, these registers store the 8x8 color pattern bitmap.
For Color Expansion function, the registers from 8300h to 847Fh store the monochrome bitmap, thus it can expand 3072 pixels at one command.

8.8.2. REGISTER FORMAT FOR LINE DRAWING

The register format for Line-Drawing is shown in the following table.

Table 8.8-2 Table of Line-Drawing Registers

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O Address
Y0		X0		8208h
Y1		X1		820Ch
Destination Base Address				8210h
Destination Height		Destination Pitch		8214h
Style Period		Line Count		8218h
FG (Foreground) Color				821Ch
BG (Background) Color				8220h
Line Style 0				822Ch
Line Style 1				8230h
Top Clipping		Left Clipping		8234h
Bottom Clipping		Right Clipping		8238h
Command				823Ch
Command Queue Status				8240h
Y2		X2		8300h
...		...		...
Y97		X97		847Ch

X0

Register Type: Read/Write
Read/Write Port: 8208h~8209h

D[15:0] The X-start Coordinate of the First Line
Limit: For normal resolution mode it is in the 12.0 format,
for high resolution mode it is in the 12.4 format.

Y0

Register Type: Read/Write
Read/Write Port: 820Ah~820Bh

D[15:0] The Y-start Coordinate of the First Line
Limit: For normal resolution mode it is in the 12.0 format, for high resolution mode it is in the 12.4 format.

X1

Register Type: Read/Write
Read/Write Port: 820Ch~820Dh

D[15:0] The X-end Coordinate of the First Line and X-start Coordinate of the Second Line
Limit: For normal resolution mode it is in the 12.0 format, for high resolution mode it is in the 12.4 format.

Y1

Register Type: Read/Write
Read/Write Port: 820Eh~820Fh

D[15:0] The Y-end Coordinate of the First Line and Y-start Coordinate of the Second Line
Limit: For normal resolution mode it is in the 12.0 format, for high resolution mode it is in the 12.4 format.

Destination Base Address

Register Type: Read/Write
Read/Write Port: 8210h~8213h

D[31:23] Reserved
D[22:0] Base Linear Address of Destination Bitmap in Byte
Limit: Destination Bitmap Addressing Range is from 0 to 8M, Quad-Word Boundary.

Destination Pitch

Register Type: Read/Write
Read/Write Port: 8214h~8215h

D[15:13] Reserved
D[12:0] Row Pitch of Destination Bitmap in Byte
Limit: Double Word Boundary

Destination Height

Register Type: Read/Write
Read/Write Port: 8216h~8217h

D[15:13] Reserved
D[12:0] Device Height of Destination Bitmap in Pixel

Line Count

Register Type: Read/Write
Read/Write Port: 8218h~8219h

D[15:7]	Reserved
D[6:0]	Total Line Count Limit: The range is from 1 to 97.

Style Period

Register Type: Read/Write
Read/Write Port: 821Ah~821Bh

D[15:6]	Reserved
D[5:0]	Period of the Line Style in Pixel Limit: A value of 0 equals 1 pixel.

Foreground Color

Register Type: Read/Write
Read/Write Port: 821Ch~821Fh

D[31:0]	Foreground Color of the Line Style

Background Color

Register Type: Read/Write
Read/Write Port: 8220h~8223h

D[31:0]	Background Color of the Line Style

Line Style

Register Type: Read/Write
Read/Write Port: 822Ch~8233h

D[63:0]	Pattern of the Line Style

Left Clipping

Register Type: Read/Write
Read/Write Port: 8234h~8235h

D[15:0]	Left Bound of Rectangular Clipping in Pixel Limit: In the 2's complement format.

Top Clipping

Register Type: Read/Write
Read/Write Port: 8236h~8237h

D[15:0]	Top Bound of Rectangular Clipping in Pixel Limit: In the 2's complement format.

Right Clipping

Register Type: Read/Write
Read/Write Port: 8238h~8239h

D[15:0]	Right Bound of Rectangular Clipping in Pixel Limit: In the 2's complement format.

Bottom Clipping

Register Type: Read/Write
Read/Write Port: 823Ah~823Bh

D[15:0]	Bottom Bound of Rectangular Clipping in Pixel Limit: In the 2's complement format.

Command Register

Register Type: Read/Write
Read/Write Port: 823Ch~823Fh

D[31:27]	Reserved
D26	Rectangular Clipping Merge Control 0: Merge clipping bound with screen bound 1: Do not merge clipping bound with screen bound
D[25:24]	Reserved
D23	Line Style Control 0: Disable line style 1: Enable line style
D22	Style counter reset control 0: Style counter will be reset 1: Style counter will not be reset
D21	Line drawing last pixel control 0: Last pixel will be drawn 1: Last pixel will not be drawn
D20	Transparent Control 0: Opaque 1: Transparent
D19	Line Resolution Control 0: Disable high resolution line drawing 1: Enable high resolution line drawing
D18	Rectangular Clipping Control 0: Disable rectangular clipping logic 1: Enable rectangular clipping logic
D[17:16]	Reserved
D[15:8]	256 Raster Operations
D[7:4]	Reserved
D[3:0]	Command type select Bit[3:0] 0000:BitBlt 0001:Color Expansion 0010:Enhanced Color Expansion 0011:Multiple Scanline 0100:Line Draw 0101:Trapezoid Fill 0110:Transparent BitBlt Others: Reserved

Command Queue Status

Register Type: Read
Read/Write Port: 8240h~8243h

D31	2D graphics engine is idle 0: 2D graphics engine is busy 1: 2D graphics engine is idle
D30	3D engine is idle

0: 3D engine is busy
1: 3D engine is idle

D29 Command queue is empty
0: Command queue is not empty
1: Command queue is empty

D[28:24] Current CPU-driven BitBlt buffer stages Bit[4:0]

D23 Status of enhanced color expansion command
0: Command is not in queue
1: Command is in queue

D[22:13] Reserved

D[12:0] Available queue length Bit[12:0]

Points

Register Type: Read/Write
Read/Write Port: 8300h~847Fh

D[31:16] The Y coordinate of the *N*-th point
D[15:0] The X coordinate of the *N*-th point

8.8.3. REGISTER FORMAT FOR TRANSPARENT BITBLT

The register format for Transparent BitBlt is shown in the following table.

Table 8.8-3 Table of Transparent Bitblt Registers

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O Address
Source Base Address				8200h
Reserved		Source Pitch		8204h
Source X		Source Y		8208h
Destination X		Destination Y		820Ch
Destination Base Address				8210h
Destination Height		Destination Pitch		8214h
Rectangular Height		Rectangular Width		8218h
High Value of Destination Color Key				821Ch
Low Value of Destination Color Key				8220h
High Value of Source Color Key				8224h
Low Value of Source Color Key				8228h
Top Clipping		Left Clipping		8234h
Bottom Clipping		Right Clipping		8238h
Command				823Ch
Command Queue Status				8240h

Source Base Address

Register Type: Read/Write
Read/Write Port: 8200h~8203h

D[31:23] Reserved
D[22:0] Base Linear Address of Source Bitmap in Byte
Limit: Source Bitmap Addressing Range is from 0 to 8M,
Quad-Word Boundary.

Source Pitch

Register Type: Read/Write
Read/Write Port: 8204h~8205h

D[15:13] Reserved
D[12:0] Row Pitch of Source Bitmap in Byte
Limit: Double Word Boundary.

Rectangle Source Y

Register Type: Read/Write
Read/Write Port: 8208h~8209h

D[15:12] Reserved
D[11:0] Started Y Coordinate of Source Bitmap in Pixel

Rectangle Source X

Register Type: Read/Write
Read/Write Port: 820Ah~820Bh

D[15:12] Reserved
D[11:0] Started X Coordinate of Source Bitmap in Pixel

Rectangle Destination Y

Register Type: Read/Write
Read/Write Port: 820Ch~820Dh

D[15:12] Reserved
D[11:0] Started Y Coordinate of Destination Bitmap in Pixel

Rectangle Destination X

Register Type: Read/Write
Read/Write Port: 820Eh~820Fh

D[15:12] Reserved
D[11:0] Started X Coordinate of Destination Bitmap in Pixel

Destination Base Address

Register Type: Read/Write
Read/Write Port: 8210h~8213h

D[31:0] Base Linear Address of Destination Bitmap in Byte
Limit: Destination Bitmap Addressing Range is from 0 to 8M,
Quad-Word Boundary.

Destination Pitch

Register Type: Read/Write
Read/Write Port: 8214h~8215h

D[15:13] Reserved
D[12:0] Row Pitch of Destination Bitmap in Byte
Limit: Double Word Boundary.

Destination Height

Register Type: Read/Write

Read/Write Port: 8216h~8217h

D[15:13] Reserved
D[12:0] Device Height of Destination Bitmap in Pixel

Rectangular Width

Register Type: Read/Write
Read/Write Port: 8218h~8219h

D[15:13] Reserved
D[12:0] Destination Rectangular Drawing Width of Bitmap in Pixel

Rectangular Height

Register Type: Read/Write
Read/Write Port: 821Ah~821Bh

D[15:13] Reserved
D[12:0] Destination Rectangular Drawing Height of Bitmap in Pixel

High Value of Destination Color Key

Register Type: Read/Write
Read/Write Port: 821Ch~821Fh

D[31:0] High Value of Destination Color Key

Low Value of Destination Color Key

Register Type: Read/Write
Read/Write Port: 8220h~8223h

D[31:0] Low Value of Destination Color Key

High Value of Source Color Key

Register Type: Read/Write
Read/Write Port: 8224h~8227h

D[31:0] High Value of Source Color Key

Low Value of Source Color Key

Register Type: Read/Write
Read/Write Port: 8228h~822Bh

D[31:0] Low Value of Source Color Key

Left Clipping

Register Type: Read/Write
Read/Write Port: 8234h~8235h

D[15:0] Left Bound of Rectangular Clipping in Pixel
Limit: In the 2's complement format.

Top Clipping

Register Type: Read/Write
Read/Write Port: 8236h~8237h

D[15:0] Top Bound of Rectangular Clipping in Pixel

Limit: In the 2's complement format.

Right Clipping

Register Type: Read/Write
Read/Write Port: 8238h~8239h

D[15:0] Right Bound of Rectangular Clipping in Pixel
Limit: In the 2's complement format.

Bottom Clipping

Register Type: Read/Write
Read/Write Port: 823Ah~823Bh

D[15:0] Bottom Bound of Rectangular Clipping in Pixel
Limit: In the 2's complement format.

Command Register

Register Type: Read/Write
Read/Write Port: 823Ch~823Fh

D[31:27] Reserved
D26 Rectangular Clipping Merge Control
0: Merge clipping bound with screen bound
1: Do not merge clipping bound with screen bound
D[25:19] Reserved
D18 Rectangular Clipping Control
0: Disable rectangular clipping logic
1: Enable rectangular clipping logic
D17 Y direction control
0: Y counter decrease
1: Y counter increase
D16 X direction control
0: X counter decrease
1: X counter increase
D[15:12] Reserved
D[11:8] Raster Operation Bit[3:0]
D[7:6] Reserved
D[5:4] Source select
00: Source is from video memory
01: Source is from CPU-driven BitBlt buffer
10: Reserved
11: Reserved
D[3:0] Command type select Bit[3:0]
0000: BitBlt
0001: Color Expansion
0010: Enhanced Color Expansion
0011: Multiple Scanline
0100: Line Draw
0101: Trapezoid Fill
0110: Transparent BitBlt
Others: Reserved

Command Queue Status

Register Type: Read
Read/Write Port: 8240h~8243h

D31 2D graphics engine is idle
0: 2D graphics engine is busy
1: 2D graphics engine is idle
D30 3D engine is idle
0: 3D engine is busy
1: 3D engine is idle
D29 Command queue is empty
0: Command queue is not empty
1: Command queue is empty
D[28:24] Current CPU-driven BitBlt buffer stages Bit[4:0]
D23 Status of enhanced color expansion command
0: Command is not in queue
1: Command is in queue
D[22:13] reserved
D[12:0] Available queue length Bit[12:0]

8.8.4 REGISTER FORMAT FOR MULTIPLE SCAN-LINE

The register format for Multiple Scan-line is shown in the following table.

Table 8.8-4 Table of Multiple Scan-line Registers

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O Address
Y Start		Scan-Line Count		8208h
X0 End		X0 Start		820Ch
Destination Base Address				8210h
Destination Height		Destination Pitch		8214h
Pattern FG (Foreground) Color				821Ch
Pattern BG (Background) Color				8220h
Mask3	Mask2	Mask1	Mask0	822Ch
Mask7	Mask6	Mask5	Mask4	8230h
Top Clipping		Left Clipping		8234h
Bottom Clipping		Right Clipping		8238h
Command				823Ch
Command Queue Status				8240h
X1 End		X1 Start		8244h
Pattern 3	Pattern 2	Pattern 1	Pattern 0	8300h
....	....	....	....	....
Pattern 63	Pattern 62	Pattern 61	Pattern 60	833Ch
X2 End		X2 Start		8340h
....		....		....
X81 End		X81 Start		847Ch

Scan-Line Count

Register Type: Read/Write
Read/Write Port: 8208h~8209h

D[15:7] Reserved

D[6:0]	Total Scan-Line Count Limit: The range is from 1 to 82 for 256-color, 1 to 66 for high-color, 1 to 34 for true-color.

Y Start

Register Type: Read/Write
Read/Write Port: 820Ah~820Bh

D[15:12]	Reserved
D[11:0]	The Y-start Coordinate of the First Scan-Line

X0 Start

Register Type: Read/Write
Read/Write Port: 820Ch~820Dh

D[15:12]	Reserved
D[11:0]	The X-start Coordinate of the First Scan-Line

X0 End

Register Type: Read/Write
Read/Write Port: 820Eh~820Fh

D[15:12]	Reserved
D[11:0]	The X-end Coordinate of the First Scan-Line

Destination Base Address

Register Type: Read/Write
Read/Write Port: 8210h~8213h

D[31:0]	Base Linear Address of Destination Bitmap in Byte Limit: Destination Bitmap Addressing Range is from 0 to 8M, Quad-Word Boundary

Destination Pitch

Register Type: Read/Write
Read/Write Port: 8214h~8215h

D[15:13]	Reserved
D[12:0]	Row Pitch of Destination Bitmap in Byte Limit: Double Word Boundary

Destination Height

Register Type: Read/Write
Read/Write Port: 8216h~8217h

D[15:13]	Reserved
D[12:0]	Device Height of Destination Bitmap in Pixel

Pattern Foreground Color

Register Type: Read/Write
Read/Write Port: 821Ch~821Fh

D[31:0]	Foreground Color Register of Pattern

Pattern Background Color

Register Type: Read/Write
Read/Write Port: 8220h~8223h

D[31:0]	Background Color Register of Pattern

Mono Mask Register

Register Type: Read/Write
Read/Write Port: 822Ch~8233h

D[63:0]	Monochrome Mask Register of Pattern

Left Clipping

Register Type: Read/Write
Read/Write Port: 8234h~8235h

D[15:0]	Left Bound of Rectangular Clipping in Pixel Limit: In the 2's complement format.

Top Clipping

Register Type: Read/Write
Read/Write Port: 8236h~8237h

D[15:0]	Top Bound of Rectangular Clipping in Pixel Limit: In the 2's complement format.

Right Clipping

Register Type: Read/Write
Read/Write Port: 8238h~8239h

D[15:0]	Right Bound of Rectangular Clipping in Pixel Limit: In the 2's complement format.

Bottom Clipping

Register Type: Read/Write
Read/Write Port: 823Ah~823Bh

D[15:0]	Bottom Bound of Rectangular Clipping in Pixel Limit: In the 2's complement format.

Command Register

Register Type: Read/Write
Read/Write Port: 823Ch~823Fh

D[31:27]	Reserved
D26	Rectangular Clipping Merge Control 0: Merge clipping bound with screen bound 1: Do not merge clipping bound with screen bound
D[25:22]	Reserved
D21	Scan-line last pixel control 0: Last pixel will be drawn 1: Last pixel will not be drawn
D20	Transparent Control 0: Opaque

	1: Transparent
D19	Reserved
D18	Rectangular Clipping Control 0: Disable rectangular clipping logic 1: Enable rectangular clipping logic
D[17:16]	Scan-line direction select bit 1-0 00: Draw scanlines upward 01: Draw scanlines at a specified vertical position 10: Draw scanlines downward 11: Reserved
D[15:8]	256 Raster Operations
D[7:6]	Pattern select bit 1-0 00: Pattern is from pattern foreground color register 01: Pattern is from pattern register 10: Pattern is from monochrome mask register 11: Reserved
D[5:4]	Reserved
D[3:0]	Command type select Bit[3:0] 0000:BitBlt 0001:Color Expansion 0010:Enhanced Color Expansion 0011:Multiple Scanline 0100:Line Draw 0101:Trapezoid Fill 0110:Transparent BitBlt Others: Reserved

Command Queue Status

Register Type: Read
Read/Write Port: 8240h~8243h

D31	2D graphics engine is idle 0: 2D graphics engine is busy 1: 2D graphics engine is idle
D30	3D engine is idle 0: 3D engine is busy 1: 3D engine is idle
D29	Command queue is empty 0: Command queue is not empty 1: Command queue is empty
D[28:24]	Current CPU-driven BitBlt buffer stages Bit[4:0]
D23	Status of enhanced color expansion command 0: Command is not in queue 1: Command is in queue
D[22:13]	Reserved
D[12:0]	Available queue length Bit[12:0]

X1 Start

Register Type: Read/Write
Read/Write Port: 8244h~8245h

D[15:12]	Reserved

D[11:0] The X-start Coordinate of the Second Scan-Line

X1 End

Register Type: Read/Write
Read/Write Port: 8246h~8247h

D[15:12] Reserved
D[11:0] The X-end Coordinate of the Second Scan-Line

Pattern Register n

Register Type: Read/Write
Read/Write Port: 8300h~833Fh for 256-color
8300h~837Fh for high-color
8300h~83FFh for true-color

D[7:0] For 256-color, high-color and true-color mode, these registers store the 8x8 color pattern bitmap.

Points

Register Type: Read/Write
Read/Write Port: 8340h~847Fh for 256-color
8380h~847Fh for high-color
8400h~847Fh for true-color

D[31:28] Reserved
D[27:16] The X-end coordinate of the N-th Scan-line
D[15:12] Reserved
D[11:0] The X-start coordinate of the N-th Scan-line

8.8.5 REGISTER FORMAT FOR TRAPEZOID FILL

The register format for Trapezoid Fill is shown in the following table.

Table 8.8-5 Table of Trapezoid Fill Registers

D[31:24]	D[23:16]	D[15:08]	D[07:00]	I/O Address
Y Start		Trapezoid Height		8208h
Right Edge X Start		Left Edge X Start		820Ch
Destination Base Address				8210h
Destination Height		Destination Pitch		8214h
Pattern FG (Foreground) Color				821Ch
Pattern BG (Background) Color				8220h
Mask3	Mask2	Mask1	Mask0	822Ch
Mask7	Mask6	Mask5	Mask4	8230h
Top Clipping		Left Clipping		8234h
Bottom Clipping		Right Clipping		8238h
Command				823Ch
Command Queue Status				8240h
Left Edge Delta Y		Left Edge Delta X		8244h
Right Edge Delta Y		Right Edge Delta X		8248h
Left Edge Error Term				824Ch
Right Edge Error Term				8250h

Trapezoid Height

Register Type: Read/Write
Read/Write Port: 8208h~8209h

D[15:12]	Reserved
D[11:0]	Height of the trapezoid in pixel

Y Start

Register Type: Read/Write
Read/Write Port: 820Ah~820Bh

D[15:12]	Reserved
D[11:0]	The Y-start Coordinate

Left Edge X Start

Register Type: Read/Write
Read/Write Port: 820Ch~820Dh

D[15:12]	Reserved
D[11:0]	The X-start Coordinate of Left Edge

Right Edge X Start

Register Type: Read/Write
Read/Write Port: 820Eh~820Fh

D[15:12]	Reserved
D[11:0]	The X-start Coordinate of Right Edge

Destination Base Address

Register Type: Read/Write
Read/Write Port: 8210h~8213h

D[31:0]	Base Linear Address of Destination Bitmap in Byte Limit: Destination Bitmap Addressing Range is from 0 to 8M, Quad-Word Boundary

Destination Pitch

Register Type: Read/Write
Read/Write Port: 8214h~8215h

D[15:13]	Reserved
D[12:0]	Row Pitch of Destination Bitmap in Byte Limit: Double Word Boundary

Destination Height

Register Type: Read/Write
Read/Write Port: 8216h~8217h

D[15:13]	Reserved
D[12:0]	Device Height of Destination Bitmap in Pixel

Pattern Foreground Color

Register Type: Read/Write
Read/Write Port: 821Ch~821Fh

D[31:0] Foreground Color Register of Pattern

Pattern Background Color

Register Type: Read/Write
Read/Write Port: 8220h~8223h

D[31:0] Background Color Register of Pattern

Mono Mask Register

Register Type: Read/Write
Read/Write Port: 822Ch~8233h

D[63:0] Monochrome Mask Register of Pattern

Left Clipping

Register Type: Read/Write
Read/Write Port: 8234h~8235h

D[15:0] Left Bound of Rectangular Clipping in Pixel
Limit: In the 2's complement format.

Top Clipping

Register Type: Read/Write
Read/Write Port: 8236h~8237h

D[15:0] Top Bound of Rectangular Clipping in Pixel
Limit: In the 2's complement format.

Right Clipping

Register Type: Read/Write
Read/Write Port: 8238h~8239h

D[15:0] Right Bound of Rectangular Clipping in Pixel
Limit: In the 2's complement format.

Bottom Clipping

Register Type: Read/Write
Read/Write Port: 823Ah~823Bh

D[15:0] Bottom Bound of Rectangular Clipping in Pixel
Limit: In the 2's complement format.

Command Register

Register Type: Read/Write
Read/Write Port: 823Ch~823Fh

D[31:27] Reserved
D26 Rectangular Clipping Merge Control
0: Merge clipping bound with screen bound
1: Do not merge clipping bound with screen bound
D25 Reserved
D24 Right edge major axial selection
0: Y-axial is major
1: X-axial is major

D23	Left edge major axial selection 0: Y-axial is major 1: X-axial is major
D22	Right edge Y direction control 0: Y counter decrease 1: Y counter increase
D21	Right edge X direction control 0: X counter decrease 1: X counter increase
D20	Transparent Control 0: Opaque 1: Transparent
D19	Line Resolution Control 0: Disable high resolution mode 1: Enable high resolution mode
D18	Rectangular Clipping Control 0: Disable rectangular clipping logic 1: Enable rectangular clipping logic
D17	Left edge Y direction control 0: Y counter decrease 1: Y counter increase
D16	Left edge X direction control 0: X counter decrease 1: X counter increase
D[15:8]	256 Raster Operations
D[7:6]	Pattern select bit 1-0 00: Pattern is from pattern foreground color register 01: Pattern is from pattern register 10: Pattern is from monochrome mask register 11: Reserved
D[5:4]	Reserved
D[3:0]	Command type select Bit[3:0] 0000:BitBlt 0001:Color Expansion 0010:Enhanced Color Expansion 0011:Multiple Scanline 0100:Line Draw 0101:Trapezoid Fill 0110:Transparent BitBlt Others:Reserved

Command Queue Status

Register Type: Read
Read/Write Port: 8240h~8243h

D31	2D graphics engine is idle 0: 2D graphics engine is busy 1: 2D graphics engine is idle
D30	3D engine is idle 0: 3D engine is busy 1: 3D engine is idle

D29	Command queue is empty 0: Command queue is not empty 1: Command queue is empty
D[28:24]	Current CPU-driven BitBlt buffer stages Bit[4:0]
D23	Status of enhanced color expansion command 0: Command is not in queue 1: Command is in queue
D[22:13]	Reserved
D[12:0]	Available queue length Bit[12:0]

Left Edge Delta X

Register Type: Read/Write
Read/Write Port: 8244h~8245h

D[15:0]	Delta X of Left edge Limit: For normal resolution mode it is in the 12.0 format, For high resolution mode it is in the 12.4 format.

Left Edge Delta Y

Register Type: Read/Write
Read/Write Port: 8246h~8247h

D[15:0]	Delta Y of Left edge Limit: For normal resolution mode it is in the 12.0 format, for high resolution mode it is in the 12.4 format.

Right Edge Delta X

Register Type: Read/Write
Read/Write Port: 8248h~8249h

D[15:0]	Delta X of Right edge Limit: For normal resolution mode it is in the 12.0 format, for high resolution mode it is in the 12.4 format.

Right Edge Delta Y

Register Type: Read/Write
Read/Write Port: 824Ah~824Bh

D[15:0]	Delta Y of Right edge Limit: For normal resolution mode it is in the 12.0 format, for high resolution mode it is in the 12.4 format.

Left Edge Error Term

Register Type: Read/Write
Read/Write Port: 824Ch~824Fh

D[31:22]	Reserved
D[21:0]	Initial Error Term of Left edge Limit: In the 2's complement format.

RIGHT EDGE ERROR TERM

Register Type: Read/Write
Read/Write Port: 8250h~8253h

D[31:22]	Reserved
D[21:0]	Initial Error Term of Right edge Limit: In the 2's complement format.

PATTERN REGISTER N

Register Type:	Read/Write
Read/Write Port:	8300h~833Fh for 256-color 8300h~837Fh for high-color 8300h~83FFh for true-color
D[7:0]	For 256-color, high-color and true-color mode, these registers store the 8x8 color pattern bitmap.

8.9. VIDEO ACCELERATOR REGISTERS

Table 8.9- 1 Table of Video Accelerator Registers

INDEX(3D4)	VIDEO ACCELERATOR REGISTER (3D5)
80h	Password/Identification Register
81h	Video Window Horizontal Display Start Low Register
82h	Video Window Horizontal Display End Low Register
83h	Video Window Horizontal Display Overflow Register
84h	Video Window Vertical Display Start Low Register
85h	Video Window Vertical Display End Low Register
86h	Video Window Vertical Display Overflow Register
87h	Reserved
88h	Reserved
89h	Video Frame Buffer Overflow Register
8Ah	Video Display Frame Buffer Starting Address Low Register
8Bh	Video Display Frame Buffer Starting Address Middle Register
8Ch	Video Frame Buffer Offset Low Register
8Dh	Reserved
8Eh	Video Frame Buffer Offset Address High Register
8Fh	Reserved
90h	Reserved
91h	Reserved
92h	Horizontal Up Scaling Factor and Horizontal Interpolation Accuracy Factor Register
93h	Vertical Up Scaling Factor Register
94h	Horizontal Scaling Factor Integer Register
95h	Video Overlay Color Key Blue Low Value Register
96h	Video Overlay Color Key Green Low Value Register
97h	Video Overlay Color Key Red Low Value Register
98h	Video Control Misc. Register 0
99h	Reserved
9Ah	Video Chroma Key B/Y Low Value Register
9Bh	Video Chroma Key G/U Low Value Register
9Ch	Video Chroma Key R/V Low Value Register
9Dh	Video Control Misc. Register 3
9Eh	Video Playback Threshold Low Value Register

9Fh	Video Playback Threshold High Value Register
A0h	Line Buffer Size Register
A1h	Video Overlay Color Key Blue High Value Register
A2h	Video Overlay Color Key Green High Value Register
A3h	Video Overlay Color Key Red High Value Register
A4h	Video Chroma Key B/Y High Value Register
A5h	Video Chroma Key G/U High Value Register
A6h	Video Chroma Key R/V High Value Register
A7h	Reserved
A8h	Reserved
A9h	Key Overlay Operation Mode Register
AAh~B2h	Reserved
B3h	Contrast Enhancement Mean Value Sampling Rate Factor Register
B4h	Brightness Register
B5h	Contrast Enhancement Control Register
B6h	Video Misc. Control Register 3
B7h	Video U Plane Starting Address Low Register
B8h	Video U Plane Starting Address Middle Register
B9h	Video UV Plane Starting Address High Register
BAh	Video V Plane Starting Address Low Register
BBh	Video V Plane Starting Address Middle Register
BCh	Video UV Plane Offset Register
BDh	Video UV Plane Offset High Register
BEh	Video Misc. Control Register 4
E0h	Index Register of TV OUT Registers
E1h	Data Register of TV OUT Registers

PASSWORD/IDENTIFICATION REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 80h
Default: 00h
D[7:0] Password/identification Bit[7:0]
Description:
If 86h is written to this register, A1h will be read from this register and all the video extension registers would be unlocked to allow desired change.
If any value other than 86h is written to this register, 21h will be read from this register and all the video extension registers would be locked to prevent unauthorized change.

VIDEO WINDOW HORIZONTAL DISPLAY START LOW REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 81h
Default: 00h
D[7:0] Video window horizontal display start Bit[7:0]
Description:
The Video Window Horizontal Display Start Bit[10:0] form the left boundary of the video window. The Bit[10:8] is located in the Video Window Horizontal Display Overflow Register (Index 83h). The boundary is in unit of pixel.

VIDEO WINDOW HORIZONTAL DISPLAY END LOW REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 82h
Default: 00h
D[7:0] Video window horizontal display end Bit[7:0]
Description:
The Video Window Horizontal Display End Bit[10:0] form the right boundary of the video window. The Bits[10:8] is located in the Video Window Horizontal Display Overflow Register (Index 83h). The boundary is in unit of pixel.

VIDEO WINDOW HORIZONTAL DISPLAY OVERFLOW REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 83h
Default: 00h
D7 Reserved
D[6:4] Video window horizontal display end Bit[10:8]
D3 Reserved
D[2:0] Video window horizontal display start Bit[10:8]

VIDEO WINDOW VERTICAL DISPLAY START LOW REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 84h
Default: 00h
D[7:0] Video window vertical display start Bit[7:0]
Description:
The Video Window Vertical Display Start Bit[10:0] form the top boundary of the video window. The Bit[10:8] is located in the Video Window Vertical Display Overflow Register (Index 86h). The boundary is in unit of line.

VIDEO WINDOW VERTICAL DISPLAY END LOW REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 85h
Default: 00h
D[7:0] Video window vertical display end Bit[7:0]
Description:
The Video Window Vertical Display End Bit[10:0] form the bottom boundary of the video window. The Bit[10:8] is located in the Video Window Vertical Display Overflow Register (Index 86h). The boundary is in unit of line.

VIDEO WINDOW VERTICAL DISPLAY OVERFLOW REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 86h
Default: 00h
D7 Reserved
D[6:4] Video window horizontal display end Bit[10:8]
D3 Reserved
D[2:0] Video window horizontal display start Bit[10:8]

VIDEO FRAME BUFFER OVERFLOW REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 89h

Default: 00h
D[7:3] Video display frame buffer starting address Bit[20:16]
D[2:0] Reserved

VIDEO DISPLAY FRAME BUFFER STARTING ADDRESS LOW REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index 8Ah
Default: 00h
D[7:0] Video display frame buffer starting address Bit[7:0]
Description:
The Video Display Frame Buffer Starting Address Bit[19:0] form the video display starting address in unit of double-word. The Bit[15:8] are located in the Video Display Frame Buffer Starting Address Middle Register (Index 8Bh). The Bits[19:16] are located in the Video Frame Buffer Overflow Register (Index 89h).
This address could be different from the video capture frame buffer starting address to perform the video display panning function.

VIDEO DISPLAY FRAME BUFFER STARTING ADDRESS MIDDLE REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index 8Bh
Default: 00h
D[7:0] Video display frame buffer starting address Bit[15:8]

VIDEO FRAME BUFFER OFFSET LOW REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index 8Ch
Default: 00h
D[7:0] Video frame buffer offset Bit[7:0]
Description:
The Video Frame Buffer Offset Bit[11:0] form the offset of the video frame buffer. The Bit[11:8] are located in the Video Frame Buffer Offset High Register (Index 8Eh).
The offset defines the size of the scan line of the video data captured in the video frame buffer in unit of double word. It should slightly larger than the actual size of captured video image to avoid the data over stored to next scan line buffer.

VIDEO FRAME BUFFER OFFSET ADDRESS HIGH REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index 8Eh
Default: 00h
D[7:4] Reserved
D[3:0] Video frame buffer offset Bit[11:8]

HORIZONTAL UP SCALING FACTOR AND HORIZONTAL INTERPOLATION ACCURACY FACTOR REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index 92h
Default: 00h
D[7:6] Horizontal up-scaling interpolation accuracy factor
00: replication
01: 2-phase
10: 4-phase

11: 8-phase
D[5:0] Horizontal up scaling factor Bit[5:0]

Description:
This field contains the video playback horizontal up scaling factor fraction (HSFF). It is combined with the horizontal scaling factor integer (HSFI) register (Index 94h) to form horizontal scaling. The horizontal size will be scaled to 1/(HSFI+(HSFF/64)). The HSFI should be zero for up-scaling. The HSFI should not be zero for down-scaling.
The Up-scaling interpolation accuracy factor can modify the up-scaling interpolation DDA accuracy phases.

VERTICAL UP SCALING FACTOR REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index 93h
Default: 00h
D[7:6] Video frame buffer data format selection Bit[1:0]
For YUV format,
00: UYVY 4:2:2
01: VYUY 4:2:2
10: YUYV 4:2:2
11: YVYU 4:2:2
For RGB format,
00: RGB 5:5:5
01: RGB 5:6:5
D[5:0] Vertical up scaling factor Bit[5:0]
Description:
This field contains the video playback vertical up scaling factor (VUSF). The vertical size will be scaled to 64/VUSF. If VUSF=0, the vertical size will not be scaled.

HORIZONTAL SCALING FACTOR INTEGER REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index 94h
Default: 00h
D[7:4] Reserved
D[3:0] Horizontal Scaling Factor Integer Bit[3:0]

VIDEO OVERLAY COLOR KEY BLUE LOW VALUE REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index 95h
Default: 00h
D[7:0] Blue Key Bit[7:0]
Description:
This register contains the blue video overlay color key low value.
In 8-bit color mode, it is used as the color key low value.
In 16-bit color mode, it is used as the low byte of color key low value.
In 24-bit color mode, it is used as the blue byte of the color key low value.
If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

VIDEO OVERLAY COLOR GREEN LOW VALUE REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 96h
Default: 00h
D[7:0] Green Key Bit[7:0]
Description:
This register contains the green video overlay color key low value.
In 8-bit color mode, it is invalid.
In 16-bit color mode, it is used as the high byte of color key low value.
In 24-bit color mode, it is used as the green byte of the color key low value.
If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

VIDEO OVERLAY COLOR RED LOW VALUE REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 97h
Default: 00h
D[7:0] Red Key Bit[7:0]
Description:
This register contains the red video overlay color key low value.
In 8-bit color mode, it is invalid.
In 16-bit color mode, it is invalid.
In 24-bit color mode, it is used as the red byte of the color key low value.
If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

VIDEO CONTROL MISC. REGISTER 0

Register Type: Read/Write
Read/Write Port: 3D5, Index 98h
Default: 00h
D7 Reserved
D6 Video format selection
0: Select RGB format
1: Select YUV format
This bit is used with the video frame buffer data format selection field of register CR92 to select the correct video data format.
D5 Reserved
D4 Video only display mode
0: Disable video only display mode
1: Enable video only display mode
The graphics display can be disable by setting this bit. This can reduce the DRAM bandwidth especially on the full screen video playback mode.
D[3:2] Reserved
D1 Enable video playback
0: Disable video playback
1: Enable video playback
This bit could enable the video playback. When the data of the video frame buffer is fetched by the system, the bandwidth of DRAM maybe not enough.

The video playback can be disabled to gain the bandwidth but the video will not be played back.

D0 Reserved

VIDEO CONTROL MISC. REGISTER 1

Register Type: Read/Write
Read/Write Port: 3D5, Index 99h
Default: 00h
D[7:0] Reserved

VIDEO CHROMA KEY B/Y LOW VALUE REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Ah
Default: 00h
D[7:0] Video Chroma B/Y Key Low Bit[7:0]
Description:
This register contains the blue or Y video overlay chroma key low value.
In RGB chroma key mode, it is used as the blue byte of the chroma key low value.
In YUV chroma key mode, it is used as the Y of the chroma key low value.
If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

VIDEO CHROMA KEY G/U LOW VALUE REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Bh
Default: 00h
D[7:0] Video Chroma G/U Key Low Bit[7:0]
Description:
This register contains the green or U video overlay chroma key low value.
In RGB chroma key mode, it is used as the green byte of the chroma key low value.
In YUV chroma key mode, it is used as the U of the chroma key low value.
If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

VIDEO CHROMA KEY R/V LOW VALUE REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Ch
Default: 00h
D[7:0] Video Chroma R/V Key Low Value Bit[7:0]
Description:
This register contains the red or V video overlay chroma key low value.
In RGB chroma key mode, it is used as the red byte of the chroma key low value.
In YUV chroma key mode, it is used as the V of the chroma key low value.
If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

VIDEO CONTROL MISC. REGISTER 2

Register Type: Read/Write

Read/Write Port: 3D5, Index 9Dh
Default: 00h
D[7:3] Reserved
D2 Chroma Key Format selection
0: RGB format
1: YUV format
D1 UV format select for video playback
0: CCIR 601 format
1: 2's complement format
D0 Reserved

VIDEO PLAYBACK THRESHOLD LOW VALUE REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index 9Eh
Default: 00h
D7 Reserved
D[6:0] Video playback threshold low Bit[6:0]
Description:
This register contains the video line buffer threshold low.
The threshold low defines the video line buffer lower boundary which indicates the line buffer is not enough and the video data should be read from the DRAM.

VIDEO PLAYBACK THRESHOLD HIGH VALUE REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index 9Fh
Default: 00h
D7 Reserved
D[6:0] Video playback threshold high Bit[6:0]
Description:
This register contains the video line buffer threshold high.
The threshold high defines the video line buffer upper boundary which indicates the data in the video line buffer is enough.
These two thresholds (video playback threshold low and threshold high) should be modified to obtain the maximum performance by compromising with the CRT threshold, video capture threshold, and DRAM refresh rate, etc.

LINE BUFFER SIZE REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index A0h
Default: 00h
D[7:0] Line Buffer Size Bit[7:0]
Description:
This register should be set to the line buffer size used by playback. The size is in unit of quad-word.

VIDEO OVERLAY COLOR KEY BLUE HIGH VALUE REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index A1h
Default: 00h
D[7:0] Blue Key High Value Bit[7:0]
Description:

This register contains the blue video overlay color key high value.
In 8-bit color mode, it is used as the color key high value.
In 16-bit color mode, it is used as the low byte of color key high value.
In 24-bit color mode, it is used as the blue byte of the color key high value.
If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

VIDEO OVERLAY COLOR KEY GREEN HIGH VALUE REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index A2h
Default: 00h
D[7:0] Green Key High Value Bit[7:0]
Description:
This register contains the green video overlay color key high value.
In 8-bit color mode, it is invalid.
In 16-bit color mode, it is used as the high byte of color key high value.
In 24-bit color mode, it is used as the green byte of the color key high value.
If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

VIDEO OVERLAY COLOR KEY RED HIGH VALUE REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index A3h
Default: 00h
D[7:0] Red Key High Value Bit[7:0]
Description:
This register contains the red video overlay color key high value.
In 8-bit color mode, it is invalid.
In 16-bit color mode, it is invalid.
In 24-bit color mode, it is used as the red byte of the color key high value.
If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

VIDEO CHROMA KEY B/Y HIGH VALUE REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index A4h
Default: 00h
D[7:0] Video Chroma B/Y Key High Value Bit[7:0]
Description:
This register contains the blue or Y video overlay chroma key high value.
In RGB chroma key mode, it is used as the blue byte of the chroma key high value.
In YUV chroma key mode, it is used as the Y of the chroma key high value.
If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced by graphics data in the way defined by key operation mode.

VIDEO CHROMA KEY G/U HIGH VALUE REGISTER
Register Type: Read/Write

Read/Write Port: 3D5, Index A5h
Default: 00h
D[7:0] Video Chroma G/U Key High Value Bit[7:0]
Description:
This register contains the green or U video overlay chroma key high value.
In RGB chroma key mode, it is used as the green byte of the chroma key high value.
In YUV chroma key mode, it is used as the U of the chroma key high value.
If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced by graphics data in the way defined by key operation mode.

VIDEO CHROMA KEY R/V HIGH VALUE REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index A6h
Default: 00h
D[7:0] Video Chroma R/V Key High Value Bit[7:0]
Description:
This register contains the red or V video overlay chroma key high value.
In RGB chroma key mode, it is used as the red byte of the chroma key high value.
In YUV chroma key mode, it is used as the V of the chroma key high value.
If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

KEY OVERLAY OPERATION MODE REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index A9h
Default: 00h
D[7:4] Reserved
D[3:0] Key Overlay Operation Mode Bit[3:0]
Description:
There are two keys for graphics data and video data overlay, which are color key and chroma key. The key overlay operation mode indicates the way the overlay would be performed.

Table 8.9- 2 Table of Key Overlay Operation Mode

OPERATION MODE	OPERATION
0000	Always select graphics data.
0001	Select blended data when color key and chroma key. Otherwise select graphics data.
0010	Select blended data when color key and not chroma key. Otherwise select graphics data.
0011	Select blended data when color key. Otherwise select graphics data.
0100	Select blended data when not color key and chroma key. Otherwise select graphics data.
0101	Select blended data when chroma key. Otherwise select graphics data.
0110	Select blended data when color key xor chroma key. Otherwise select graphics data.
0111	Select blended data when color key or chroma key.

	Otherwise select graphics data.
1000	Select blended data when not color key and not chroma key. Otherwise select graphics data.
1001	Select blended data when color key xnor chroma key. Otherwise select graphics data.
1010	Select blended data when not chroma key. Otherwise select graphics data.
1011	Select blended data when color key or not chroma key. Otherwise select graphics data.
1100	Select blended data when not chroma key. Otherwise select graphics data.
1101	Select blended data when not color key or chroma key. Otherwise select graphics data.
1110	Select blended data when not color key or not chroma key. Otherwise select graphics data.
1111	Always select blended data.

CONTRAST ENHANCEMENT MEAN VALUE SAMPLING RATE FACTOR REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index B3h
Default: 00h
D[7:0] Contrast Enhancement Mean Value Sampling Rate Factor Bits[7:0]
Description:
The contrast enhancement needs mean value for each frame. This mean value is calculated by sampling some pixels from one video frame. The sampling rate = Contrast Enhancement Mean Value Sampling Rate Factor / 1024.

Brightness
Register Type: Read/Write
Read/Write Port: 3D5, Index B4h
Default: 00h
D[7:0] Brightness Bit[7:0]
Description:
The Brightness is an 8-bit 2's complement number from -128 to +127. This value is added with the video data to control the brightness.

CONTRAST ENHANCEMENT CONTROL REGISTER

Register Type: Read/Write
Read/Write Port: 3D5, Index B5h
Default: 00h
D[2:0] Contrast Gain Bit[2:0]
000: 1.0
001: 1.0625
010: 1.125
011: 1.1875
100: 1.25
101: 1.3125
110: 1.375
111: 1.4375
D[5:3] Contrast Mean Frame Samples Bit[2:0]
000: 2 frames

001: 4 frames
010: Reserved
011: 8 frames
100: Reserved
101: Reserved
110: Reserved
111: 16 frames

D[7:6] Contrast Mean Pixel Samples Bit[1:0]
00: 2048 pixels
01: 4096 pixels
10: 8192 pixels
11: 16384 pixels

VIDEO CONTROL MISC. REGISTER 3
Register Type: Read/Write
Read/Write Port: 3D5, Index B6h
Default: 00h
D[7:3] Reserved
D2 Enable YUV 420 mode
0: Disable
1: Enable
D[1:0] Reserved

VIDEO U PLANE STARTING ADDRESS LOW REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index B7h
Default: 00h
D[7:0] Video U Plane Starting Address Low Bit[7:0]

VIDEO U PLANE STARTING ADDRESS MIDDLE REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index B8h
Default: 00h
D[7:0] Video U Plane Starting Address Middle Bit[15:8]

VIDEO UV PLANE STARTING ADDRESS HIGH REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index B9h
Default: 00h
D[7:4] Video V Plane Starting Address High Bit[19:16]
D[3:0] Video U Plane Starting Address High Bit[19:16]

VIDEO V PLANE STARTING ADDRESS LOW REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index BAh
Default: 00h
D[7:0] Video V Plane Starting Address Low Bit[7:0]

VIDEO V PLANE STARTING ADDRESS LOW REGISTER
Register Type: Read/Write

Read/Write Port: 3D5, Index BBh
Default: 00h
D[7:0] Video V Plane Starting Address Middle Bit[15:8]

VIDEO UV PLANE OFFSET REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index BCh
Default: 00h
D[7:0] Video UV Plane Offset Bit[7:0]

VIDEO UV PLANE OFFSET HIGH REGISTER
Register Type: Read/Write
Read/Write Port: 3D5, Index BDh
Default: 00h
D[7:4] Reserved
D[3:0] Video UV Plane Offset Bit[11:8]

VIDEO CONTROL MISC. REGISTER 4
Register Type: Read/Write
Read/Write Port: 3D5, Index BEh
Default: 00h
D[7:5] Reserved
D4 Line Buffer Merge Control
0: Disable
0: Enable
D3 Reserved
D2 Video V Plane Starting Address High Bit20
D1 Video U Plane Starting Address High Bit20
D0 Reserved

8.10. PCI CONFIGURATION REGISTERS

CONFIGURATION REGISTER 00H
Register Type: Read
Read Port: 0000h
Default: 63061039h
D[31:16] Device ID
The Device ID of integrated 3D VGA is 6306h
D[15:0] Vendor ID
Integrated Vendor ID is 1039h

CONFIGURATION REGISTER 04H
Register Type: Read/Write
Read Port: 0004h
Default: 02200004h
D[31:27] Reserved
D[26:25] DEVSEL* timing (= 01, Read Only)
00: fast
01: medium (fixed at this value)
10: slow

D[24:22]	Reserved
D21	66 MHz Capable 0: Support 33MHz 1: Support 66 MHz (fixed at this value)
D[20:13]	Reserved
D12	Capabilities List 0: does not implement a list of capabilities 1: implements a list of capabilities
D[11:06]	Reserved
D5	VGA Palette Snoop 0: Disable 1: Enable
D4	Reserved
D3	Bus Master 0: Device is not a bus master 1: Device is a bus master (fixed at this value)
D1	Memory Space 0: Disable 1: Enable
D0	I/O Space 0: Disable 1: Enable

CONFIGURATION REGISTER 08H

Register Type:	Read
Read Port:	0008h
Default:	030000AXh
D[31:8]	Class Code (= 030000h)
D[7:0]	Revision ID (= Axh, for Rev. Ax)

CONFIGURATION REGISTER 10H

Register Type:	Read/Write
Read Port:	0010h
Default:	00000008h
D[31:0]	32-bit memory base register for 4MB linear frame buffer

CONFIGURATION REGISTER 14H

Register Type:	Read/Write
Read Port:	0014h
Default:	00000000h
D[31:0]	32-bit memory base register for 64KB memory mapped I/O

CONFIGURATION REGISTER 18H

Register Type:	Read/Write
Read Port:	0018h
Default:	00000001h
D[31:0]	Reserved

CONFIGURATION REGISTER 2CH

Register Type:	Read/Write Once Only
Read Port:	002Ch

Default: 00000000h
D[31:16] Subsystem ID
D[15:0] Subsystem Vendor ID

CONFIGURATION REGISTER 30H
Register Type: Read/Write
Read Port: 0030h
Default: 000C0000h
D[31:11] Expansion ROM Base Address
D[10:1] Reserved
D0 ROM Enable Bit
0: Disable
1: Enable

CONFIGURATION REGISTER 3CH
Register Type: Read/Write
Read Port: 003Ch
Default: 00000100h
If D3 of SRE is 1, then
D[15:8] Interrupt Pin (= 01h, Read Only)
D[7:0] Interrupt Line (= 00h)
If D3 of SRE is 0, then
D[15:8] Interrupt Pin (= 00h, Read Only)
D[7:0] Interrupt Line (= 00h)

8.11. AGP CONFIGURATION REGISTERS

Note: All the registers described in this section can be accessed only when AGP is enable.

CONFIGURATION REGISTER 34H
Register Type: Read Only
Read Port: 0034h
Default: 00000050h
D[7:0] Capabilities list offset pointer (Read Only)

CONFIGURATION REGISTER 50H
Register Type: Read Only
Read Port: 0050h
Default: 00105C02h
D[23:20] Major revision number
D[19:16] Minor revision number
D[15:8] Pointer to next item
D[7:0] Cap_ID: value 02h identifies the list item as pertaining to AGP register.

CONFIGURATION REGISTER 54H
Register Type: Read Only
Read Port: 0054h
Default: 01000003h
D[31:24] Maximum number of AGP command requests

D[23:10]	Reserved
D9	Side band addressing support 0: Not support 1: Support
D[8:2]	Reserved
D1	2X mode support 0: Not support 1: Support
D0	1X mode support 0: Not support 1: Support

CONFIGURATION REGISTER 58H

Register Type:	Read/Write
Read Port:	0058h
Default:	00000000h
D[31:24]	Maximum number of AGP requests can be enqueued
D[23:10]	Reserved
D9	Sideband address control 0: sideband address mode disable 1: sideband address mode enable
D8	AGP device control 0: AGP disable 1: AGP enable
D[7:2]	Reserved
D1	AGP 2X mode control 0: 2X mode disable 1: 2X mode enable
D0	AGP 1X mode control 0: 1X mode disable 1: 1X mode enable

CONFIGURATION REGISTER 5CH

Register Type:	Read
Read Port:	005Ch
Default:	00000000h
D[15:8]	NULL: 00h indicates final item in the capability list
D[7:0]	Reserved

8.12. DIGITAL FLAT PANEL INTERFACE REGISTERS

PANEL LINK HORIZONTAL RETRACE START

Register Type: Read/Write
Read/Write Port: 3D5, index C0h

D[7:0]	PLHRS[7:0] Panel link horizontal retrace start.

PANEL LINK HORIZONTAL RETRACE END/SKEW

Register Type: Read/Write
Read/Write Port: 3D5, index C1h

D[7:5] PLHSKEW[2:0]
Panel Link horizontal retrace skew: 0~7 DCLK.
D[4:0] PLHRE[4:0]
Panel Link horizontal retrace end.

PANEL LINK HORIZONTAL DISPLAY START
Register Type: Read/Write
Read/Write Port: 3D5, index C2h
D[7:0] PLHDES[7:0]
Panel Link horizontal display enable start.

PANEL LINK HORIZONTAL DISPLAY END
Register Type: Read/Write
Read/Write Port: 3D5, index C3h
D[7:0] PLHDEE[7:0]
Panel Link horizontal display enable end.

PANEL LINK VERTICAL RETRACE START
Register Type: Read/Write
Read/Write Port: 3D5, index C4h
D[7:0] PLVRS[7:0]
Panel Link vertical retrace start.

PANEL LINK VERTICAL RETRACE END/MISC.
Register Type: Read/Write
Read/Write Port: 3D5, index C5h
D[7] PLVSPLTY
0: Vertical Sync high active
1: Vertical Sync low active
D[6] PLHSPLTY
0: Horizontal Sync high active
1: Horizontal Sync low active
D[5:4] PLMODE[1:0]
00: 12-bit RGB to LVDS/TMDS transmitter.
10: 18-bit RGB to LVDS/TMDS transmitter.
11: 24-bit RGB to LVDS/TMDS transmitter.
D[3:0] PLVRE[3:0]
Panel Link vertical retrace end.

PANEL LINK VERTICAL RETRACE START
Register Type: Read/Write
Read/Write Port: 3D5, index C6h
D[7] ENPLINK
0: Disable Panel Link
1: Enable Panel Link
D[6] ENTESTP32K
0: Normal operation.
1: Test mode: Enable counter test
D[5:3] PLVRS[10:8]
High bits of vertical retrace start.
D[2:0] PLDESKEW[2:0]

Display enable skew: 1~7 DCLK.

PANEL LINK VERTICAL DISPLAY ENABLE START: LOW BITS
Register Type: Read/Write
Read/Write Port: 3D5, index C7h
D[7:0]: PLVDES[7:0]
Panel Link vertical display enable start.

PANEL LINK VERTICAL DISPLAY ENABLE END: LOW BITS
Register Type: Read/Write
Read/Write Port: 3D5, index C8h
D[7:0]: PLVDEE[7:0]
Panel Link vertically display enable end.

PANEL LINK INTERRUPT CONTROL SIGNAL AND HIGH BITS OF VERTICAL DISPLAY CONTROL REGISTERS
Register Type: Read/Write
Read/Write Port: 3D5, index C9h
D[7] PLINTCLR
0: Normal
1: Clear Panel Link interrupt request.
D[6] ENPLINT
0: Disable Panel Link interrupt.
1: Enable Panel Link interrupt.
D[5:3] PLVDEE[10:8]
High bits of Panel Link display enable end.
D[2:0] PLVDES[10:8]
High bits of Panel Link display enable start.

PANEL LINK INTERRUPT READ BACK BITS
Register Type: Read
Read Port: 3D5, index CAh
D[7] DE only mode
0: Sync and DE mode
1: DE only mode
D[6] EnPLCKHDRV
0: Panel Link clock output low driving.
1: Panel Link clock output high driving.
D[5:4] PLCLKDLY[1:0]
00: no delay Panel Link clock output
01: delay Panel Link clock output 1 ns
10: delay Panel Link clock output 2 ns
11: delay Panel Link clock output 3 ns
D[3] DIVPLCLK
0: Panel Link clock output frequency is equivalent to DCLK.
1: Panel Link clock output frequency is DCLK divided by 2
D[2] INVPLCLK
0: Panel Link clock output phase is the same as DCLK

1: Panel Link clock output phase is inverse of DCLK

D[1] PLSWITCH
- 0: Disable Panel Link output pad
- 1: Enable Panel Link output pad.

D[0] EnHWINT
- 0: Disable hardware interrupt: INTA#
- 1: Enable hardware interrupt: INTA#

PANEL LINK INTERRUPT READ BACK AND DDC DATA/CLOCK

Register Type: Read/write

Read/write Port: 3D5, index CBh

D[7:6] reserved

D[5] write Flat Panel DDC clock output : FDDCCLK
- 0: pull high DDC clock output
- 1: pull low DDC clock output

D[4] write Flat Panel DDC data output : FDDCDATA
- 0: pull high DDC data output
- 1: pull low DDC data output

D[3] read Flat Panel DDC clock input: FDDCCLK
- 0: Flat Panel DDC clock input low
- 1: Flat Panel DDC clock input high

D[2] read Flat Panel DDC data input: FDDCDATA
- 0: Flat Panel DDC data input low
- 1: Flat Panel DDC data input high

D[1] PLINTRTP: Flat Panel interrupt read-back bit
- 0: No interrupt
- 1: Panel Link Interrupt

D[0] PLATTCH: Flat Panel Plugging Status read back bit
- 0: No Flat Panel plugged
- 1: Flat Panel Plugged

8.13. LEGEND OF 3D REGISTERS

8.13.1. LEGEND OF 3D REGISTERS

Table 8.13- 1 Legend of 3D Registers

NOTATION	DEFINITION
(number)	The number of bits
(f)	Floating point representation
(i)	Integer representation
(s12)	Sign Magnitude Representation with 12 integer bits
A	Alpha component
A8	Alpha component, 8 bits integer representation
$Addr_{number}$	Address buss
Apix	Alpha component of a pixel
Atex	Alpha component of a texel
B	Blue color component
Cout	Output color

Cpix	Pixel color
Cr	Color stored in the color register CR
F	Fog factor
G	Green color component
Ltex	Luminance of a texel
M	Mix mode factor
R	Red color component
SB	Specular blue color component
SG	Specular green color component
SR	Specular red color component
TSARGBa	The register which stores the color component ARGB of vertex a
TSARGBb	The register which stores the color component ARGB of vertex b
TSARGBc	The register which stores the color component ARGB of vertex c
TSFSa	The register which stores the fog factor and specular color components of vertex a
TSFSb	The register which stores the fog factor and specular color components of vertex b
TSFSc	The register which stores the fog factor and specular color components of vertex c
TSUa	The register which stores the U coordinate of vertex a
TSUb	The register which stores the U coordinate of vertex b
TSUc	The register which stores the U coordinate of vertex c
TSVa	The register which stores the V coordinate of vertex a
TSVb	The register which stores the V coordinate of vertex b
TSVc	The register which stores the V coordinate of vertex c
TSWa	The register which stores the W perspective correction factor of vertex a
TSWb	The register which stores the W perspective correction factor of vertex b
TSWc	The register which stores the W perspective correction factor of vertex c
TSXa	The register which stores the X coordinate of vertex a
TSXb	The register which stores the X coordinate of vertex b
TSXc	The register which stores the X coordinate of vertex c
TSYa	The register which stores the Y coordinate of vertex a
TSYb	The register which stores the Y coordinate of vertex b
TSYc	The register which stores the Y coordinate of vertex c
TSZa	The register which stores the Z coordinate of vertex a
TSZb	The register which stores the Z coordinate of vertex b
TSZc	The register which stores the Z coordinate of vertex c
U	The X coordinate in a Texture
V	The Y coordinate in a Texture
W	Perspective correction factor
X	X coordinate
Y	Y coordinate
Z	Z coordinate
Z16	Z value, 16 bits representation

8.13.2. 3D REGISTERS SUMMARY

Table 8.13- 2 Vertex Parameter Registers

	NAME	I/O ADDRESS	TRIANGLE DRAWING	LINE DRAWING	POINT DRAWING
1	TSFSa	8803h-8800h	√	√	√
2	TSZa	8807h-8804h	√	√	√
3	TSXa	880Bh-8808h	√	√	√
4	TSYa	880Fh-880Ch	√	√	√
5	TSARGBa	8813h-8810h	√	√	√
6	TSUa	8817h-8814h	√	√	√
7	TSVa	881Bh-8818h	√	√	√
8	TSWa	881Fh-881Ch	√	√	
9	TSFSb	8823h-8820h	√	√	
10	TSZb	8827h-8824h	√	√	
11	TSXb	882Bh-8828h	√	√	
12	TSYb	882Fh-882Ch	√	√	
13	TSARGBb	8833h-8830h	√	√	
14	TSUb	8837h-8834h	√	√	
15	TSVb	883Bh-8838h	√	√	
16	TSWb	883Fh-883Ch	√	√	
17	TSFSc	8843h-8840h	√		
18	TSZc	8847h-8844h	√		
19	TSXc	884Bh-8848h	√		
20	TSYc	884Fh-884Ch	√		
21	TSARGBc	8853h-8850h	√		
22	TSUc	8857h-8854h	√		
23	TSVc	885Bh-8858h	√		
24	TSWc	885Fh-885Ch	√		
25	Reserved	89F7h-8860h	√		

Table 8.13- 3 Primitive Setting Registers

89FBh ~	D[31:24]	Reserved	
89F8h	D[23:21]	Reserved	
	D[20:18]	TSHMD	Shading Mode
	D[17:16]	TTFROM	Point, Start, or Top Vertex Come From
	D[15:14]	TMFROM	Middle Vertex Come From
	D[13:12]	TBFROM	End or Bottom Vertex Come From
	D[11:8]	TSETFIRE	Set 3D Engine Fire Position
	D[7]	TDRAWDIR	Drawing Direction
	D[6:3]	Reserved	
	D[2:0]	TDRAW	Drawing Primitive Command

Table 8.13- 4 Engine Fire & Status Registers

89FFh ~	D[31:0]	TFIRE	Write for 3D Engine Fire

89FCh	D[31:0]	TSTATUS	Read for 3D Engine Status

Table 8.13- 5 Enable Setting Registers

8A03h ~	D[31:24]	Reserved	
8A00h	D[23:22]	Reserved	
	D[21]	TenZW	Z Write Enable
	D[20]	TenZT	Z Test Enable
	D[19]	Reserved	
	D[18]	TenAW	Alpha Write Enable
	D[17]	TenAT	Alpha Test Enable
	D[16]	TenABUF	Alpha Buffer Enable
	D[15]	TenMips	
	D[14]	Reserved	
	D[13]	Reserved	
	D[12]	TenLPT	Line Pattern Enable
	D[11]	Reserved	
	D[10]	TenTXMP	Texture Mapping Enable
	D[9]	TenTXPP	Texture Perspective Enable
	D[8]	TenTXTR	Texture Transparency Enable
	D[7]	TenCACHE	Enable Texture Cache
	D[6]	Reserved	
	D[5]	Reserved	
	D[4]	TenSPEC	Specular Enable
	D[3]	TenFOG	Fog Enable
	D[2]	TenBLEND	Blending Enable
	D[1]	TenTRSP	Transparency Enable
	D[0]	TenDITH	Dither Enable

Table 8.13- 6 Z Setting Registers

8A07h ~	D[31:24]	Reserved	
8A04h	D[23:22]	Reserved	
	D[21:20]	TZBUFFM	Z-Buffer Data Format
	D[19]	Reserved	
	D[18:16]	TZTMD	Z-Test Mode
	D[15:14]	Reserved	
	D[13:0]	TZPIT	Z-Buffer Pitch
8A0Bh ~ 8A08h	D[31:0]	TZBAS	Z-Buffer Base Address

Table 8.13- 7 Alpha Setting Registers

8A0Fh ~	D[31:30]	Reserved	
8A0Ch	D[29:28]	TABUFFM	Alpha Buffer Data Format
	D[27]	Reserved	
	D[26:24]	TATMD	Alpha Test Mode
	D[23:16]	TAREF	Alpha Reference Value
	D[15:12]	Reserved	
	D[11:0]	TAPIT	Alpha Buffer Pitch

8A13h ~ 8A10h	D[31:0]	TABAS	Alpha Buffer Base Address

Table 8.13- 8 Destination Setting Registers

8A17h ~	D[31:28]	Reserved	
8A14h	D[27:24]	TROP	Raster Operation
	D[23]	Reserved	
	D[22:16]	TDSTCFM	Destination Color Format
	D[15:14]	Reserved	
	D[13:0]	TDSTPIT	Destination Color Surface Pitch
8A1Bh ~ 8A18h	D[31:0]	TDSTBAS	Destination Color Surface Base Address

Table 8.13- 9 Line Setting Registers

8A1Fh ~ 8A1Ch	D[31:0]	TLPT	Line Pattern and Repeat Factor

Table 8.13- 10 Fog Setting Registers

8A23h ~	D[31:25]	Reserved	
8A20h	D[24]	TFOGMD	Fog Mode
	D[23:0]	TFOGC	Fog Color Register

Table 8.13- 11 Miscellaneous Setting Registers

8A27h ~	D[31:24]	Reserved	
8A24h	D[23:0]	TTRSL	Transparency Color Range Low Value
8A2Bh ~	D[31:28]	TBLDST	Destination Blending Mode
8A28h	D[27:24]	TBLSRC	Source Blending Mode
	D[23:0]	TTRSH	Transparency Color Range High Value
8A2Fh ~ 8A2C	D[31:0]	Reserved	
8A33h ~	D[31:26]	Reserved	
8A30h	D[25:0]	TCLTB	Clipping Value for Top & Bottom
8A37h ~	D[31:26]	Reserved	
8A34h	D[25:0]	TCLLR	Clipping Value for Left & Right

Table 8.13- 12 Texture Setting Registers

8A3Bh ~	D[31:24]	TTXFM	Texel Format
8A38h	D[23:16]	TTXMPMD	Texture Mapping Mode
	D[15]	UVPOLAR	Set Sign or Un-sign Format of U,V
	D[14:12]	TTXBLMKB	Texture Blending Mask Bit Setting
	D[11:8]	TTXLV	Texture Level
	D[7:6]	Reserved	
	D[5]	TTXINSY	Texture Memory Located in System Memory
	D[4]	TTXCHCL	Clear Texture Cache
	D[3]	TTXFLMAX	Texture Magnified Filter Mode

	D[2:0]	TTXFLMIN	Texture Restrictional Filter Mode
8A3Fh ~	D[31:26]	TTXBLCMD	Texture Blending Color Mode Setting
8A3Ch	D[25:24]	TTXBLAMD	Texture Blending Alpha Mode Setting
	D[23:0]	TTXTRSL	Texture Transparency Color Range Low Value
8A43h ~	D[31:24]	Reserved	
8A40h	D[23:0]	TTXTRSH	Texture Transparency Color Range High Value
8A47h ~ 8A44h	D[31:0]	TTX0BAS	Texture Level 0 Base Address
8A4Bh ~ 8A48h	D[31:0]	TTX1BAS	Texture Level 1 Base Address
8A4Fh ~ 8A4Ch	D[31:0]	TTX2BAS	Texture Level 2 Base Address
8A53h ~ 8A50h	D[31:0]	TTX3BAS	Texture Level 3 Base Address
8A57h ~ 8A54h	D[31:0]	TTX4BAS	Texture Level 4 Base Address
8A5Bh ~ 8A58h	D[31:0]	TTX5BAS	Texture Level 5 Base Address
8A5Fh ~ 8A5Ch	D[31:0]	TTX6BAS	Texture Level 6 Base Address
8A63h ~ 8A60h	D[31:0]	TTX7BAS	Texture Level 7 Base Address
8A67h ~ 8A64h	D[31:0]	TTX8BAS	Texture Level 8 Base Address
8A6Bh ~ 8A68h	D[31:0]	TTX9BAS	Texture Level 9 Base Address
8A6Fh ~	D[31:27]	Reserved	
8A6Ch	D[26:16]	TTX0PCTL	Texture Level 0 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX1PCTL	Texture Level 1 Pitch
8A73h ~	D[31:27]	Reserved	
8A70h	D[26:16]	TTX2PCTL	Texture Level 2 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX3PCTL	Texture Level 3 Pitch
8A77h ~	D[31:27]	Reserved	
8A74h	D[26:16]	TTX4PCTL	Texture Level 4 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX5PCTL	Texture Level 5 Pitch
8A7Bh ~	D[31:27]	Reserved	
8A78h	D[26:16]	TTX6PCTL	Texture Level 6 Pitch
	D[15:11]	Reserved	
	D[10:0]	TTX7PCTL	Texture Level 7 Pitch
8A7Fh ~	D[31:27]	Reserved	
8A7Ch	D[26:16]	TTX8PCTL	Texture Level 8 Pitch

	D[15:11]	Reserved	
	D[10:0]	TTX9PCTL	Texture Level 9 Pitch
8A83h ~	D[31:28]	TTXW	Width of Texture Level 0
8A80h	D[27:24]	TTXH	Height of Texture Level 0
	D[23:19]	Reserved	
	D[18:10]	TTXMIPBS	Texture MIPMAP Bias
	D[9:0]	TTXLVINSY	Texture Level # in System Memory
8A87h ~	D[31:0]	Reserved	
8A84h			
8A8Bh ~	D[31:0]	Reserved	
8A88h			
8A8Fh ~	D[31:0]	Reserved	
8A8Ch	D[23:0]	TTXCR	Texture Color Register for Luminance
8A93h ~ 8A90h	D[31:0]	TTXCTB	Texture Border Color Register
8AD3h ~ 8A94h	D[31:0] x 16	TTXIDX15 ~ TTXIDX0	Texture Index Palette Register 0 ~ Texture Index Palette Register 15

Index Format
Index4: Use TTXIDX15 - TTXIDX0
Index2: Use TTXIDX3 - TTXIDX0
Index1: Use TTXIDX1 - TTXIDX0

Table 8.13- 13 Reserved Registers

8AFEh ~ 8AD4h		Reserved	

Table 8.13- 14 End of Primitive Setting Register

8AFFh	D[7:0]	TEND	End of Primitive List

8.13.3. VERTEX PARAMETER REGISTERS

Fog & Specular Color Components of Vertex a
Register Type: Read/Write
Read/Write Port: 8803h ~ 8800h
Default: xx xx xx xxh
D[31:24] TSFSa (i) ➡➡ fog factor of vertex a
D[23:16] TSSRa (i) ➡➡ specular red color of vertex a
D[15:8] TSSGa (i) ➡➡ specular green color of vertex a
D[7:0] TSSBa (i) ➡➡ specular blue color of vertex a

Z Coordinate of Vertex a
Register Type: Read/Write
Read/Write Port: 8807h ~ 8804h
Default: xx xx xx xxh
D[31:0] TSZa (f) ➡➡ Z of vertex a

X Coordinate of Vertex a
Register Type: Read/Write
Read/Write Port: 880Bh ~ 8808h
Default: xx xx xx xxh
D[31:0] TSXa (f) ➡➡ X of vertex a

Y Coordinate of Vertex a
Register Type: Read/Write
Read/Write Port: 880Fh ~ 880Ch
Default: xx xx xx xxh
D[31:0] TSYa (f) ➡➡ Y of vertex a

Color Component ARGB of Vertex a
Register Type: Read/Write
Read/Write Port: 8813h ~ 8810h
Default: xx xx xx xxh
D[31:24] TSAa (i) ➡➡ A of vertex a
D[23:16] TSRa (i) ➡➡ R of vertex a
D[15:8] TSGa (i) ➡➡ G of vertex a
D[7:0] TSBa (i) ➡➡ B of vertex a

X Coordinate in a Texture of Vertex a
Register Type: Read/Write
Read/Write Port: 8817h ~ 8814h
Default: xx xx xx xxh
D[31:0] TSUa (f) ➡➡ U of vertex a

Y Coordinate in a Texture of Vertex a
Register Type: Read/Write
Read/Write Port: 881Bh ~ 8818h
Default: xx xx xx xxh
D[31:0] TSVa (f) ➡➡ V of vertex a

Perspective Correction Factor in a Texture of Vertex a
Register Type: Read/Write
Read/Write Port: 881Fh ~ 881Ch
Default: xx xx xx xxh
D[31:0] TSWa (f) ➡➡ W of vertex a

Fog & Specular Color Components of Vertex b
Register Type: Read/Write
Read/Write Port: 8823h ~ 8820h
Default: xx xx xx xxh
D[31:24] TSFSb (i) ➡➡ fog factor of vertex b
D[23:16] TSSRb (i) ➡➡ specular red color of vertex b
D[15:8] TSSGb (i) ➡➡ specular green color of vertex b
D[7:0] TSSBb (i) ➡➡ specular blue color of vertex b

Z Coordinate of Vertex b
Register Type: Read/Write

Read/Write Port: 8827h ~ 8824h
Default: xx xx xx xxh
D[31:0] TSZb (f) ➡➡ Z of vertex b

X Coordinate of Vertex b
Register Type: Read/Write
Read/Write Port: 882Bh ~ 8828h
Default: xx xx xx xxh
D[31:0] TSXb (f) ➡➡ X of vertex b

Y Coordinate of Vertex b
Register Type: Read/Write
Read/Write Port: 882Fh ~ 882Ch
Default: xx xx xx xxh
D[31:0] TSYb (f) ➡➡ Y of vertex b

Color Component ARGB of Vertex b
Register Type: Read/Write
Read/Write Port: 8833h ~ 8830h
Default: xx xx xx xxh
D[31:24] TSAb (i) ➡➡ A of vertex b
D[23:16] TSRb (i) ➡➡ R of vertex b
D[15:8] TSGb (i) ➡➡ G of vertex b
D[7:0] TSBb (i) ➡➡ B of vertex b

X Coordinate in a Texture of Vertex b
Register Type: Read/Write
Read/Write Port: 8837h ~ 8834h
Default: xx xx xx xxh
D[31:0] TSUb (f) ➡➡ U of vertex b

Y Coordinate in a Texture of Vertex c
Register Type: Read/Write
Read/Write Port: 883Bh ~ 8838h
Default: xx xx xx xxh
D[31:0] TSVb (f) ➡➡ V of vertex b

Perspective Correction Factor in a Texture of Vertex b
Register Type: Read/Write
Read/Write Port: 883Fh ~ 883Ch
Default: xx xx xx xxh
D[31:0] TSWb (f) ➡➡ W of vertex b

Fog & Specular Color Components of Vertex c
Register Type: Read/Write
Read/Write Port: 8843h ~ 8840h
Default: xx xx xx xxh
D[31:24] TSFSc (i) ➡➡ fog factor of vertex c
D[23:16] TSSRc (i) ➡➡ specular red color of vertex c
D[15:8] TSSGc (i) ➡➡ specular green color of vertex c

D[7:0] TSSBc (i) ➡➡ specular blue color of vertex c

Z Coordinate of Vertex c
Register Type: Read/Write
Read/Write Port: 8847h ~ 8844h
Default: xx xx xx xxh
D[31:0] TSZc (f) ➡➡ Z of vertex c

X Coordinate of Vertex c
Register Type: Read/Write
Read/Write Port: 884Bh ~ 8848h
Default: xx xx xx xxh
D[31:0] TSXc (f) ➡➡ X of vertex c

Y Coordinate of Vertex c
Register Type: Read/Write
Read/Write Port: 884Fh ~ 884Ch
Default: xx xx xx xxh
D[31:0] TSYc (f) ➡➡ Y of vertex c

Color Component ARGB of Vertex c
Register Type: Read/Write
Read/Write Port: 8853h ~ 8850h
Default: xx xx xx xxh
D[31:24] TSAc (i) ➡➡ A of vertex c
D[23:16] TSRc (i) ➡➡ R of vertex c
D[15:8] TSGc (i) ➡➡ G of vertex c
D[7:0] TSBc (i) ➡➡ B of vertex c

X Coordinate in a Texture of Vertex c
Register Type: Read/Write
Read/Write Port: 8857h ~ 8854h
Default: xx xx xx xxh
D[31:0] TSUc (f) ➡➡ U of vertex c

Y Coordinate in a Texture of Vertex c
Register Type: Read/Write
Read/Write Port: 885Bh ~ 8858h
Default: xx xx xx xxh
D[31:0] TSVc (f) ➡➡ V of vertex c

Perspective Correction Factor in a Texture of Vertex c
Register Type: Read/Write
Read/Write Port: 885Fh ~ 885Ch
Default: xx xx xx xxh
D[31:0] TSWc (f) ➡➡ W of vertex c

Reserved Registers
Register Type: Read/Write
Read/Write Port: 89F7h ~ 8860h

Default: xx xx xx xxh
D[31:0] Reserved

8.13.4. PRIMITIVE SETTING REGISTERS

Register Type: Read/Write
Read/Write Port: 89FBh ~ 89F8h
Default: xx xx xx xxh
D[31:21] Reserved
D[20:18] TSHMD ➡➡ Shading Mode

For triangle shading,

000: Reserved
001: FLAT_SHADING via top vertex
010: FLAT_SHADING via middle vertex
011: FLAT_SHADING via bottom vertex
100: SMOOTH_SHADING via GOURAUD_SHADING
111 ~ 101: Reserved

For line shading,

000: Reserved
001: FLAT_SHADING via start vertex
010: Reserved
011: FLAT_SHADING via end vertex
100: SMOOTH_SHADING via GOURAUD_SHADING
111 ~ 101: Reserved

D[17:16] TTFROM ➡➡ top vertex come from

For triangle,

00: top vertex come from vertex a
01: top vertex come from vertex b
10: top vertex come from vertex c
11: reserved

For line,

00: start vertex come from vertex a
01: start vertex come from vertex b
10: start vertex come from vertex c
11: reserved

For point,

00: vertex come from vertex a
01: vertex come from vertex b
10: vertex come from vertex c
11: reserved

D[15:14] TMFROM ➡➡ middle vertex come from

For triangle,

00: middle vertex come from vertex a
01: middle vertex come from vertex b
10: middle vertex come from vertex c

11: reserved

D[13:12] TBFROM ➡➡ bottom vertex come from

For triangle,

00: bottom vertex come from vertex a
01: bottom vertex come from vertex b
10: bottom vertex come from vertex c
11: reserved

For line,

00: end vertex come from vertex a
01: end vertex come from vertex b
10: end vertex come from vertex c
11: reserved

D[11:8] TSETFIRE ➡➡ Set 3D Engine Fire Position
0000: 3D Engine fired right after the write of TFIRE
0001: 3D Engine fired right after the write of TSARGBa
0010: 3D Engine fired right after the write of TSWa
0011: 3D Engine fired right after the write of TSARGBb
0100: 3D Engine fired right after the write of TSWb
0101: 3D Engine fired right after the write of TSARGBc
0110: 3D Engine fired right after the write of TSWc
0111: 3D Engine fired right after the write of TSVc
1000-1111: Reserved

D7 TDRAWDIR ➡➡ Drawing Direction

For triangle drawing,

0: left to right
1: right to left

For line drawing,

0: horizontal
1: vertical

D[6:3] Reserved

D[2:0] TDRAW ➡➡ Drawing Primitive Command
000: Draw a Point
001: Draw a Line
010: Draw a Triangle
011-111: Reserved

8.13.5. ENGINE FIRE & STATUS REGISTER

Register Type: Read/Write
Read/Write Port: 89FFh ~ 89FCh
Default: xx xx xx xxh

For write operation,

D[31:0] TFIRE ➡➡ Write to Fire 3D Engine

For read operation,

D[31:0] TSTATUS ➡➡ Read for 3D Engine Status as follow:

D[27:16]	Available 3D Queue Length 3D Queue Length = D[27:16] * 8 Bytes
D[15:2]	Reserved
D1	T3IDLEQE ➡➡ 3D Engine Idle & 3D Queue Empty 0: 3D Engine Busy or 3D Queue not Empty 1: 3D Engine Idle and 3D Queue Empty
D0	T3IDLE ➡➡ 3D Engine Idle 0: 3D Engine Busy 1: 3D Engine Idle

8.13.6. ENABLE SETTING REGISTER

Register Type: Read/Write
Read/Write Port: 8A03h ~ 8A00h
Default: all 00h

D[31:22]	Reserved
D21	TenZW ➡➡ Z Write Enable 0: Z Write Disable 1: Z Write Enable
D20	TenZT ➡➡ Z Test Enable 0: Z Test Disable 1: Z Test Enable
D19	Reserved
D18	TenAW ➡➡ Alpha Write Enable 0: Alpha Write Disable 1: Alpha Write Enable
D17	TenAT ➡➡ Alpha Test Enable 0: Alpha Test Disable 1: Alpha Test Enable
D16	TenABUF ➡➡ Alpha Buffer Enable 0: Alpha Buffer Disable 1: Alpha Buffer Enable
D15	Reserved
D[14:13]	TenSTIP, TenSTIPA ➡➡ Stipple Enable, Stipple Alpha Enable 0x: Stipple Disable 10: Stipple Enable, Stipple Alpha Disable 11: Stipple Enable, Stipple Alpha Enable
D12	TenLPT ➡➡ Line Pattern Enable 0: Line Pattern Disable 1: Line Pattern Enable
D11	TenPRSET ➡➡ Primitive Setup Enable 0: Primitive Setup Disable 1: Primitive Setup Enable
D10	TenTXMP ➡➡ Texture Mapping Enable 0: Texture Mapping Disable 1: Texture Mapping Enable
D9	TenTXPP ➡➡ Texture Perspective Correction Enable 0: Texture Perspective Correction Disable 1: Texture Perspective Correction Enable
D8	TenTXTR ➡➡ Texture Transparency Enable 0: Texture Transparency Disable

1: Texture Transparency Enable

D7 TenCACHE ➡➡ Enable Texture Cache
0: Texture Cache Disable
1: Texture Cache Enable

D6 Reserved

D5 TenLCH ➡➡ Enable Large Cache Size
0: Small Cache Size
1: Large Cache Size

D4 TenSPEC ➡➡ Specular Enable
0: Specular Disable
1: Specular Enable

D3 TenFOG ➡➡ Fog Enable
0: Fog Disable
1: Fog Enable

D2 TenBLEND ➡➡ Blending Enable
0: Blending Disable
1: Blending Enable

D1 TenTRSP ➡➡ Transparency Enable
0: Transparency Disable
1: Transparency Enable

D0 TenDITH ➡➡ Dither Enable
0: Dither Disable
1: Dither Enable

8.13.7. Z SETTING REGISTERS

Z Setting Register 1

Register Type: Read/Write
Read/Write Port: 8A07h ~ 8A04h
Default: xx xx xx xxh

D[31:24] Reserved

D[23:22] Reserved

D[21:20] TZBUFFM ➡➡ Z Buffer Format
00: Z8
01: Z16
1x: Reserved

D19 Reserved

D[18:16] TZTMD ➡➡ Z Test Mode
000: Z test never pass
001: Pass if Znew < Zdst
010: Pass if Znew = Zdst
011: Pass if Znew ≤ Zdst
100: Pass if Znew > Zdst
101: Pass if Znew ≠ Zdst
110: Pass if Znew ≥ Zdst
111: Z test always pass

D[15:14] Reserved

D[13:0] TZPIT ➡➡ Z Buffer Pitch
Addr13 ~ Addr0

Z Setting Register 2

Register Type: Read/Write
Read/Write Port: 8A0Bh ~ 8A08h
Default: xx xx xx xxh
D[31:0] TZBAS ➡➡ Z Buffer Base Address
If Z Buffer is located in system memory,
D[31:0] Addr31 ~ Addr0
If Z Buffer is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

8.13.8. ALPHA SETTING REGISTERS

Alpha Setting Register 1

Register Type: Read/Write
Read/Write Port: 8A0Fh ~ 8A0Ch
Default: xx xx xx xxh
D[31:30] Reserved
D[29:28] TABUFFM ➡➡ Alpha Buffer Color Format
00 ~ 10: Reserved
11: A8 (alpha component, 8-bit integer representation)
D27 Reserved
D[26:24] TATMD ➡➡ Alpha Test Mode
000: Alpha test never pass
001: Pass if Anew < Aref
010: Pass if Anew = Aref
011: Pass if Anew ≤ Aref
100: Pass if Anew > Aref
101: Pass if Anew ≠ Aref
110: Pass if Anew ≥ Aref
111: Alpha test always pass
D[23:16] TAREF ➡➡ Alpha Reference Value
A8 format (alpha component, 8-bit integer representation)
D[15:12] Reserved
D[11:0] TAPIT ➡➡ Alpha Buffer Pitch
Addr11 ~ Addr0

Alpha Setting Register 2

Register Type: Read/Write
Read/Write Port: 8A13h ~ 8A10h
Default: xx xx xx xxh
D[31:0] TABAS ➡➡ Alpha Buffer Base Address
If Alpha Buffer is located in system memory,
D[31:0] Addr31 ~ Addr0
If Alpha Buffer is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

8.13.9. DESTINATION SETTING REGISTERS

Destination Setting Register 1

Register Type: Read/Write
Read/Write Port: 8A17h ~ 8A14h
Default: xx xx xx xxh
D[31:28] Reserved
D[27:24] TROP ➡➡ Raster Operation

Table 8.13- 15 Raster Operation

0000: BLACK	0
0001: NOT_MERGE_PEN	DPon
0010: MASK_NOT_PEN	DPna
0011: NOT_COPY_PEN	Pn
0100: MASK_PEN_NOT	PDna
0101: NOT	Dn
0110: XOR_PEN	DPx
0111: NOT_MASK_PEN	DPan
1000: MASK_PEN	DPa
1001: NOT_XOR_PEN	DPxn
1010: NOP	D
1011: MERGE_NOT_PEN	DPno
1100: COPY_PEN	P
1101: MERGE_PEN_NOT	PDno
1110: MERGE_PEN	DPo
1111: WHITE	1

D23 Reserved
D[22:16] TDSTCFM ➡➡ Destination Color Format
D22 0: RGB ordering in RGB format
1: BGR ordering in RGB format
D[21:20] 00: Index format or RGB_8bpp format
01: RGB_16bpp format
10: RGB_24bpp format
11: RGB_32bpp format
If *D[22:20] = 001 (RGB_16bpp format),*
D[19:16]

Table 8.13- 16 RGB_16bpp Format

0000: RGB555,	xRRR RRGG GGGB BBBB
0001: RGB565,	RRRR RGGG GGGB BBBB
0010: ARGB1555,	ARRR RRGG GGGB BBBB
0011: ARGB4444,	AAAA RRRR GGGG BBBB

If D[22:20] = 011 (RGB_32bpp format),
D[19:16]

Table 8.13-17 RGB_32bpp Format

0000: ARGB1888	Axxx xxxx RRRR RRRR GGGG GGGG BBBB BBBB
0001: ARGB2888	AAxx xxxx RRRR RRRR GGGG GGGG BBBB BBBB
0010: ARGB4888	AAAA xxxx RRRR RRRR GGGG GGGG

	BBBB BBBB
0011: ARGB8888	AAAA AAAA RRRR RRRR GGGG GGGG BBBB BBBB
0100: RGB0888	xxxx xxxx RRRR RRRR GGGG GGGG BBBB BBBB
Others: Reserved	

If D[22:20] = 101 (RGB_16bpp format),
D[19:16]

Table 8.13- 18 RGB_16bpp Format

0000: BGR555	XBBB BBGG GGGR RRRR
0001: BGR565	BBBB BGGG GGGR RRRR
0010: ABGR1555	ABBB BBGG GGGR RRRR
0011: ABGR4444	AAAA BBBB GGGG RRRR

If D[22:20] = 111 (RGB_32bpp format),
D[19:16]

Table 8.13- 19 RGB_32bpp Format

0000: ABGR1888	Axxx xxxx BBBB BBBB GGGG GGGG RRRR RRRR
0001: ABGR2888	AAxx xxxx BBBB BBBB GGGG GGGG RRRR RRRR
0010: ABGR4888	AAAA xxxx BBBB BBBB GGGG GGGG RRRR RRRR
0011: ABGR8888	AAAA AAAA BBBB BBBB GGGG GGGG RRRR RRRR
0100: BGR0888	xxxx xxxx BBBB BBBB GGGG GGGG RRRR RRRR
Others: Reserved	

D[15:14] Reserved
D[13:0] TDSTPIT ➡➡ Destination Pitch
Addr13 ~ Addr0

Destination Setting Register 2
Register Type: Read/Write
Read/Write Port: 8A1Bh ~ 8A18h
Default: xx xx xx xxh
D[31:0] TDSTBAS ➡➡ Destination Base Address
If Destination Surface is located in system memory,
D[31:0] Addr31 ~ Addr0
If Destination Surface is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Line Setting Register
Register Type: Read/Write
Read/Write Port: 8A1Fh ~ 8A1Ch

Default: xx xx xx xxh
D[31:16] TLPT ➡➡ Line pattern
D[15:0] TLPTNRP (i) ➡➡ Repeat factor of Line Pattern

Fog Setting Register
Register Type: Read/Write
Read/Write Port: 8A23h ~ 8A20h
Default: xx xx xx xxh
D[31:25] Reserved
D24 TFOGMD ➡➡ Fog Mode
0: Constant Fog Mode
1: Normal Fog Mode
D[23:16] TGFR (i) ➡➡ Fog Color R
D[15:8] TGFG (i) ➡➡ Fog Color G
D[7:0] TGFB (i) ➡➡ Fog Color B

8.13.10. MISCELLANEOUS SETTING REGISTERS

Miscellaneous Setting Register 1
Register Type: Read/Write
Read/Write Port: 8A27h ~ 8A24h
Default: xx xx xx xxh
D[31:27] Reserved
D[23:16] TTRSLR (i) ➡➡ R of Transparency Color Low Range
D[15:8] TTRSLG (i) ➡➡ G of Transparency Color Low Range
D[7:0] TTRSLB (i) ➡➡ B of Transparency Color Low Range

Miscellaneous Setting Register 2
Register Type: Read/Write
Read/Write Port: 8A2Bh ~ 8A28h
Default: xx xx xx xxh
D[31:28] TBLDST ➡➡ Destination Blending Mode
0000: BLEND_ZERO
Blend factor is (0, 0, 0, 0) for (A,R,G,B)
0001: BLEND_ONE
Blend factor is (1, 1, 1, 1) for (A,R,G,B)
0010: BLEND_SRC_COLOR
Blend factor is [R(s),G(s),B(s),A(s)]
0011: BLEND_INV_SRC_COLOR
Blend factor is [1-R(s),1-G(s),1-B(s),1-A(s)]
0100: BLEND_SRC_ALPHA
Blend factor is [A(s),A(s),A(s),A(s)]
0101: BLEND_INV_SRC_ALPHA
Blend factor is [1-A(s),1-A(s),1-A(s), 1-A(s)]
0110: BLEND_DST_ALPHA
Blend factor is [A(d),A(d),A(d),A(d)]
0111: BLEND_INV_DST_ALPHA
Blend factor is [1-A(d),1-A(d),1-A(d)]
Others: Reserved
D[27:24] TBLSRC ➡➡ Source Blending Mode
0000: BLEND_ZERO

Blend factor is (0, 0, 0, 0)
0001: BLEND_ONE
Blend factor is (1, 1, 1, 1)
0010-0011: Reserved
0100: BLEND_SRC_ALPHA
Blend factor is [A(s), A(s), A(s), A(s)]
0101: BLEND_INV_SRC_ALPHA
Blend factor is [1-A(s), 1-A(s), 1-A(s), 1-A(s)]
0110: BLEND_DST_ALPHA
Blend factor is [A(d), A(d), A(d), A(d)]
0111: BLEND_INV_DST_ALPHA
Blend factor is [1-A(d), 1-A(d), 1-A(d)]
1000: BLEND_DST_COLOR
Blend factor is [R(d), G(d), B(d), A(d)]
1001: BLEND_INV_DST_COLOR
Blend factor is [1-R(d), 1-G(d), 1-B(d), 1-A(d)]
1010: BLEND_SRC_ALPHA_SAT
Blend factor is (f, f, f, 1); f = min[A(s), 1-A(d)]
1011: BLEND_BOTH_SRC_ALPHA
Source blend factor is [A(s), A(s), A(s), A(s)]
Destination blend factor is [1-A(s), 1-A(s), 1-A(s), 1-A(s)]
1100: BLEND_BOTH_INV_SRC_ALPHA
Source blend factor is [1-A(s), 1-A(s), 1-A(s), 1-A(s)]
Destination blend factor is [A(s), A(s), A(s), A(s)]
Others: Reserved

D[23:16] TTRSHR (i) ➡➡ R of Transparency Color High Range
D[15:8] TTRSHG (i) ➡➡ G of Transparency Color High Range
D[7:0] TTRSHB (i) ➡➡ B of Transparency Color High Range

Miscellaneous Setting Register 3

Register Type: Read/Write
Read/Write Port: 8A2Fh ~ 8A2Ch
Default: xx xx xx xxh
D[31:0] Reserved

Miscellaneous Setting Register 4

Register Type: Read/Write
Read/Write Port: 8A33h ~ 8A30h
Default: xx xx xx xxh
D[31:26] Reserved
D[25:13] TCLTOP (s12) ➡➡ Top Clipping Value
D[12:0] TCLBOT (s12) ➡➡ Bottom Clipping Value

Miscellaneous Setting Register 5

Register Type: Read/Write
Read/Write Port: 8A37h ~ 8A34h
Default: xx xx xx xxh
D[31:26] Reserved
D[25:13] TCLLEFT (s12) ➡➡ Left Clipping Value
D[12:0] TCLRGT (s12) ➡➡ Right Clipping Value

8.13.11. TEXTURE SETTING REGISTERS

Texture Setting Register 1

Register Type: Read/Write
Read/Write Port: 8A3Bh ~ 8A38h
Default: xxh, xxh, x0000000b, 00h

D[31:24] TTXFM ➡➡ Texel Format

D31 RGB ordering
0: RGB ordering in RGB format
1: BGR ordering in RGB format

D[30:28] Format
000: Palette Index format
001: Mix format
010: YUV format
011: Luminance format
100: RGB_8bpp or BGR_8bpp format
101: RGB_16bpp or BGR_8bpp format
110: RGB_24bpp or BGR_24bpp format
111: RGB_32bpp or BGR_32bpp format
(Color ordering is shown from MSB to LSB)

For D[31:28] = 0000 (RGB ordering & palette index format),

D[27:24] 0000: Index1
Use TTXIDX0, 1
0001: Index2
Use TTXIDX0, 1, 2, 3
0010: Index4
Use TTXIDX0-15

For D[31:28] = 0001 (RGB ordering & mix format),

D[27:24] 0000: M4
MMMM
0110: AM44
AAAA MMMM

For D[31:28] = 0010 (RGB ordering & YUV format),

D[27:24] 0000: YUV422
$Y_1Y_1Y_1Y_1\ Y_1Y_1Y_1Y_1$ CuCuCuCu CuCuCuCu $Y_0Y_0Y_0Y_0\ Y_0Y_0Y_0Y_0$ CvCvCvCv CvCvCvCv
0001: YVU422
$Y_1Y_1Y_1Y_1\ Y_1Y_1Y_1Y_1$ CvCvCvCv CvCvCvCv $Y_0Y_0Y_0Y_0\ Y_0Y_0Y_0Y_0$ CuCuCuCu CuCuCuCu
0010: UVY422
CuCuCuCu CuCuCuCu $Y_1Y_1Y_1Y_1\ Y_1Y_1Y_1Y_1$ CvCvCvCvCvCvCvCv $Y_0Y_0Y_0Y_0Y_0\ Y_0Y_0Y_0$
0011: VUY422
CvCvCvCv CvCvCvCv $Y_1Y_1Y_1Y_1\ Y_1Y_1Y_1Y_1$ CuCuCuCuCuCuCuCu $Y_0Y_0Y_0Y_0Y_0Y_0Y_0Y_0$

For D[31:28] = 0011 (RGB ordering & luminance format),

D[27:24] 0000: L1
L
0001: L2
LL
0010: L4

LLLL
0011: L8
LLLL LLLL
0101: AL22
AALL
1000: AL44
AAAA LLLL
1100: AL88
AA AAAA LLLL LLLL
Others: Reserved

For D[31:28] = 0100 (ARGB 8bpp format),

D[27:24] 0000: RGB332
RRRG GGBB
0001: RGB233
RRGG GBBB
0010: RGB232
xRRG GGBB
0011: ARGB1232
ARRG GGBB
Others: Reserved

For D[31:28] = 0101 (ARGB 16bpp format),

D[27:24] 0000: RGB555
xRRR RRGG GGGB BBBB
0001: RGB565
RRRR RGGG GGGB BBBB
0010: ARGB1555
ARRR RRGG GGGB BBBB
0011: ARGB4444
AAAA RRRR GGGG BBBB
0111: ARGB8332
AAAA AAAA RRRG GGBB
1011: ARGB8233
AAAA AAAA RRGG GBBB
1111: ARGB8232
AAAA AAAA xRRG GGBB
Others: Reserved

For D[31:28] = 0110 (ARGB 24bpp format),

D[27:24] 0011: ARGB8565
AAAA AAAA RRRR RGGG GGGB BBBB
0111: ARGB8555
AAAA AAAA xRRR RRGG GGGB BBBB
1000: RGB888
RRRR RRRR GGGG GGGG BBBB BBBB
Others: Reserved

For D[31:28] = 0111 (ARGB 32bpp format),

D[27:24] 0011: ARGB8888
AAAA AAAA RRRR RRRR GGGG GGGG BBBB BBBB
0100: ARGB0888
xxxx xxxx RRRR RRRR GGGG GGGG BBBB BBBB
Others: Reserved

For D[31:28] = 1100 (ABGR 8bpp format),

D[27:24] 0000: BGR332
BBBG GGRR
0001: BGR233
BBGG GRRR
0010: BGR232
xBBG GGRR
0011: ABGR1232
ABBG GGRR
Others: Reserved

For D[31:28] = 1101 (ABGR 16bpp format),

D[27:24] 0000: BGR555
xBBB BBGG GGGR RRRR
0001: BGR565
BBBB BGGG GGGR RRRR
0010: ABGR1555
ABBB BBGG GGGR RRRR
0011: ABGR4444
AAAA BBBB GGGG RRRR
0111: ABGR8332
AAAA AAAA BBBG GGRR
1011: ABGR8233
AAAA AAAA BBGG GRRR
1111: ABGR8232
AAAA AAAA xBBG GGRR
Others: Reserved

For D[31:28] = 1110 (ABGR 24bpp format),

D[27:24] 0011: ABGR8565
AAAA AAAA BBBB BGGG GGGR RRRR
0111: ABGR8555
AAAA AAAA xRRR RRGG GGGB RRRR
1000: BGR888
BBBB BBBB GGGG GGGG RRRR RRRR
Others: Reserved

For D[31:28] = 1111 (ABGR 32bpp format),

D[27:24] 0011: ABGR8888
AAAA AAAA BBBB BBBB GGGG GGGG RRRR RRRR
0100: ABGR0888
xxxx xxxx BBBB BBBB GGGG GGGG RRRR RRRR
Others: Reserved

D[23:16] TTXMPMD ➡➡ Texture Mapping Mode
(Priority: wrap > mirror > clamp)
xx xxxx00: Wrap Disable
xx xx00xx: Mirror Disable
xx 00xxxx: Clamp Disable
xx xxxxx1: Wrap along U axis
xx xxxx1x: Wrap along V axis
xx xxx1x0: Mirror along U axis
xx xx1x0x: Mirror along V axis
xx x1x0x0: Clamp along U axis
xx 1x0x0x: Clamp along V axis
x0 xxxxxx: Do not use Border Color (CTB) for smoothing

x1 xxxxxx: Use CTB for smoothing
0x xxxxxx: Do not use CTB if out of texture area
1x xxxxxx: Use CTB if out of texture area

D15 UVPOLAR ➡➡ Set Sign or Un-sign Format of Cu, Cv
0: Cu and Cv are un-sign representation
1: Cu and Cv are Sign magnitude representation

D[14:2] TTXBLMKB ➡➡ Texture Blending Mask Bit Setting
000: Bit n = Bit 0 of Atex
001: Bit n = Bit 1 of Atex
010: Bit n = Bit 2 of Atex
011: Bit n = Bit 3 of Atex
100: Bit n = Bit 4 of Atex
101: Bit n = Bit 5 of Atex
110: Bit n = Bit 6 of Atex
111: Bit n = Bit 7 of Atex

D[11:8] TTXLV ➡➡ Texture Level
0000: Single Texture Structure
1001 ~ 0001: MIP structure
This number must small than or equal to
max {TTXW, TTXH}.
1111 ~ 1010: Reserved

D[7:6] Reserved

D5 TTXINSY ➡➡ Texture Memory Located in System Memory
0: Texture Memory is located in local frame buffer
1: Texture Memory is located in system memory

D4 TTXCHCL ➡➡ Clear Texture Cache
0: Let Texture Cache Work Normally
1: Clear Data in Texture Cache

D3 TTXFLMAX ➡➡ Texture filter mode when a texture is magnified
0: Nearest
1: Linear

D[2:0] TTXFLMIN ➡➡ Texture filter mode when a texture is restricted
000: NEAREST
001: LINEAR
010: NEAREST_MIP_NEAREST
011: NEAREST_MIP_LINEAR
100: LINEAR_MIP_NEAREST
101: LINEAR_MIP_LINEAR
11x: Reserved

Texture Setting Register 2

Register Type: Read/Write
Read/Write Port: 8A3Fh ~ 8A3Ch
Default: xx xx xx xxh

D[31:26] TTXBLCMD ➡➡ Texture Blending Color Mode Setting

For ARGB format,

00 0000: Cout = Ctex
00 0001: Cout = Cpix
00 0010: Cout = Cpix Ctex
00 0011: Cout = Cpix Ctex

00 0100: Cout = (1 - Atex) Cpix + Atex Ctex
00 0101: Reserved
00 0110: Cout = (1 - Apix) Ctex + Apix Cpix
00 0111: Cout = (1 - Apix) Ctex + Apix Cpix
00 1000: Cout = Ctex, if Bit n of Atex = 1,
Cout = Cpix, if Bit n of Atex = 0
00 1001: Cout = Ctex , if Bit n of Atex = 1,
Cout = Cpix, if Bit n of Atex = 0
00 101x: Reserved
00 1100: Cout = Cpix Ctex, if Bit n of Atex = 1,
Cout = Cpix , if Bit n of Atex = 0
00 1101: Cout = Cpix Ctex, if Bit n of Atex = 1,
Cout = Cpix, if Bit n of Atex = 0
00 1110: Cout = Cpix Ctex, if Bit n of Atex = 1,
Cout = Cpix, if Bit n of Atex = 0
0 1111: Reserved
01 xxxx: Reserved
1x xxxx: Reserved

For RGB format,

00 0000: Cout = Ctex
00 0001: Cout = Cpix
00 0010: Cout = Cpix Ctex
00 0011: Cout = Cpix Ctex
00 0100: Cout = Ctex
00 0101: Reserved
00 0110: Cout = Cpix
00 0111: Cout = Cpix
00 1000: Cout = Ctex
00 1001: Cout = Cpix
00 101x: Reserved
00 1100: Cout = Cpix Ctex
00 1101: Cout = Cpix
00 1110: Cout = Cpix Ctex
00 1111: Reserved
01 xxxx: Reserved
1x xxxx: Reserved

For AL format,

00 0000: Cout = Ltex Cr
00 0001: Cout = Cpix
00 0010: Cout = Ltex Cpix
00 0011: Cout = Ltex Cr Cpix
00 0100: Cout = (1 - Ltex) Cpix + Ltex Cr
00 0101: Reserved
00 0110: Cout = (1- Apix) Cr + Apix Cpix
00 0111: Cout = (1- Apix) Ltex Cr + Apix Cpix
00 1000: Cout = Ltex Cr, if Bit n of Atex = 1
Cout = Cpix, if Bit n of Atex = 0
00 1001: Cout = Ltex Cr, if Bit n of Atex = 1
Cout = Cpix, if Bit n of Atex = 0

00 101x: Reserved
00 1100: Cout = Ltex Cpix, if Bit n of Atex = 1
Cout = Cpix, if Bit n of Atex = 0
00 1101: Cout = Ltex Cpix, if Bit n of Atex = 1
Cout = Cpix, if Bit n of Atex = 0
00 1110: Cout = Ltex Cr Cpix, if Bit n of Atex = 1
Cout = Cpix, if Bit n of Atex = 0
00 1111: Reserved
01 xxxx: Reserved
1x xxxx: Reserved

For L format,

00 0000: Cout = Ltex Cr
00 0001: Cout = Cpix
00 0010: Cout = Ltex Cpix
00 0011: Cout = Ltex Cr Cpix
00 0100: Cout = Ltex Cr
00 0101: Reserved
00 0110: Cout = Cpix
00 0111: Cout = Cpix
00 1000: Cout = Ltex Cr
00 1001: Cout = Cpix
00 101x: Reserved
00 1100: Cout = Ltex Cpix
00 1101: Cout = Cpix
00 1110: Cout = Ltex Cr Cpix
00 1111: Reserved
01 xxxx: Reserved
1x xxxx: Reserved

D[25:24] TTXBLAMD ➡➡ Texture Blending Alpha Mode Setting
00: Aout = Atex, for ARGB, AL texture format
Aout = Apix, for RGB, L texture format
01: Aout = Apix
10: Aout = Apix Atex, for ARGB, AL texture format
Aout = Apix, for RGB, L texture format
11: Reserved
D[23:16] TTXTRSLR (i) ➡➡ R of Texture Transparency Color Low Range
D[15:8] TTXTRSLG (i) ➡➡ G of Texture Transparency Color Low Range
D[7:0] TTXTRSLB (i) ➡➡ B of Texture Transparency Color Low Range

Texture Setting Register 3

Register Type: Read/Write
Read/Write Port: 8A43h ~ 8A40h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXTRSHR (i) ➡➡ R of Texture Transparency Color High Range
D[15:8] TTXTRSHG (i) ➡➡ G of Texture Transparency Color High Range
D[7:0] TTXTRSHB (i) ➡➡ B of Texture Transparency Color High Range

Texture Level 0 Base Address

Register Type: Read/Write

Read/Write Port: 8A47h ~ 8A44h
Default: xx xx xx xxh
D[31:0] TTX0BAS ➡➡ Texture Level 0 Base Address
If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0
If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 1 Base Address
Register Type: Read/Write
Read/Write Port: 8A4Bh ~ 8A48h
Default: xx xx xx xxh
D[31:0] TTX1BAS ➡➡ Texture Level 1 Base Address
If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0
If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 2 Base Address
Register Type: Read/Write
Read/Write Port: 8A4Fh ~ 8A4Ch
Default: xx xx xx xxh
D[31:0] TTX2BAS ➡➡ Texture Level 2 Base Address
If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0
If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 3 Base Address
Register Type: Read/Write
Read/Write Port: 8A53h ~ 8A50h
Default: xx xx xx xxh
D[31:0] TTX3BAS ➡➡ Texture Level 3 Base Address
If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0
If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 4 Base Address
Register Type: Read/Write
Read/Write Port: 8A57h ~ 8A54h
Default: xx xx xx xxh
D[31:0] TTX4BAS ➡➡ Texture Level 4 Base Address
If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0
If Texture Memory is located in local frame buffer,
D[31:23] Reserved

D[22:0] Addr22 ~ Addr0

Texture Level 5 Base Address
Register Type: Read/Write
Read/Write Port: 8A5Bh ~ 8A58h
Default: xx xx xx xxh
D[31:0] TTX5BAS ➡➡ Texture Level 5 Base Address
If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0
If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 6 Base Address
Register Type: Read/Write
Read/Write Port: 8A5Fh ~ 8A5Ch
Default: xx xx xx xxh
D[31:0] TTX6BAS ➡➡ Texture Level 6 Base Address
If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0
If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 7 Base Address
Register Type: Read/Write
Read/Write Port: 8A63h ~ 8A60h
Default: xx xx xx xxh
D[31:0] TTX7BAS ➡➡ Texture Level 7 Base Address
If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0
If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 8 Base Address
Register Type: Read/Write
Read/Write Port: 8A67h ~ 8A64h
Default: xx xx xx xxh
D[31:0] TTX8BAS ➡➡ Texture Level 8 Base Address
If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0
If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 9 Base Address
Register Type: Read/Write
Read/Write Port: 8A6Bh ~ 8A68h
Default: xx xx xx xxh
D[31:0] TTX9BAS ➡➡ Texture Level 9 Base Address

If Texture Memory is located in system memory,
D[31:0] Addr31 ~ Addr0
If Texture Memory is located in local frame buffer,
D[31:23] Reserved
D[22:0] Addr22 ~ Addr0

Texture Level 0 & 1 Pitch Control
Register Type: Read/Write
Read/Write Port: 8A6Fh ~ 8A6Ch
Default: xx xx xx xxh
D[31:27] Reserved
D[26:16] TTX0PCTL ➡➡ Texture Level 0 Pitch Control
Addr10 ~ Addr0
D[15:11] Reserved
D[10:0] TTX1PCTL ➡➡ Texture Level 1 Pitch Control
Addr10 ~ Addr0

Texture Level 2 & 3 Pitch Control
Register Type: Read/Write
Read/Write Port: 8A73h ~ 8A70h
Default: xx xx xx xxh
D[31:27] Reserved
D[26:16] TTX2PCTL ➡➡ Texture Level 2 Pitch Control
Addr10 ~ Addr0
D[15:11] Reserved
D[10:0] TTX3PCTL ➡➡ Texture Level 3 Pitch Control
Addr10 ~ Addr0

Texture Level 4 & 5 Pitch Control
Register Type: Read/Write
Read/Write Port: 8A77h ~ 8A74h
Default: xx xx xx xxh
D[31:27] Reserved
D[26:16] TTX4PCTL ➡➡ Texture Level 4 Pitch Control
Addr10 ~ Addr0
D[15:11] Reserved
D[10:0] TTX5PCTL ➡➡ Texture Level 5 Pitch Control
Addr10 ~ Addr0

Texture Level 2 & 3 Pitch Control
Register Type: Read/Write
Read/Write Port: 8A7Bh ~ 8A78h
Default: xx xx xx xxh
D[31:27] Reserved
D[26:16] TTX6PCTL ➡➡ Texture Level 6 Pitch Control
Addr10 ~ Addr0
D[15:11] Reserved
D[10:0] TTX7PCTL ➡➡ Texture Level 7 Pitch Control
Addr10 ~ Addr0

Texture Level 8 & 9 Pitch Control

Register Type: Read/Write
Read/Write Port: 8A7Fh ~ 8A7Ch
Default: xx xx xx xxh
D[31:27] Reserved
D[26:16] TTX8PCTL ➡➡ Texture Level 8 Pitch Control
Addr10 ~ Addr0
D[15:11] Reserved
D[10:0] TTX9PCTL ➡➡ Texture Level 9 Pitch Control
Addr10 ~ Addr0

Texture Setting Register 4

Register Type: Read/Write
Read/Write Port: 8A83h ~ 8A80h
Default: xx xx xx xxh
D[31:28] TTXW ➡➡ Texture Width
0000: Texture Width = 2^0 = 1
0001: Texture Width = 2^1 = 2
0010: Texture Width = 2^2 = 4
0011: Texture Width = 2^3 = 8
0100: Texture Width = 2^4 = 16
0101: Texture Width = 2^5 = 32
0110: Texture Width = 2^6 = 64
0111: Texture Width = 2^7 = 128
1000: Texture Width = 2^8 = 256
1001: Texture Width = 2^9 = 512
1010 ~ 1111: Reserved
D[27:24] TTXH ➡➡ Texture Height
0000: Texture Height = 2^0 = 1
0001: Texture Height = 2^1 = 2
0010: Texture Height = 2^2 = 4
0011: Texture Height = 2^3 = 8
0100: Texture Height = 2^4 = 16
0101: Texture Height = 2^5 = 32
0110: Texture Height = 2^6 = 64
0111: Texture Height = 2^7 = 128
1000: Texture Height = 2^8 = 256
1001: Texture Height = 2^9 = 512
1010-1111: Reserved
D[23:16] TXCBR (i) ➡➡ R of Texture Color Base Register for Mix Mode
D[15:8] TXCBG (i) ➡➡ G of Texture Color Base Register for Mix Mode
D[7:0] TXCBB (i) ➡➡ B of Texture Color Base Register for Mix Mode

Texture Color Register 0 for Mix Mode

Register Type: Read/Write
Read/Write Port: 8A87h ~ 8A84h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXC0R (i) ➡➡ R of Texture Color Register 0
D[15:8] TTXC0G (i) ➡➡ G of Texture Color Register 0
D[7:0] TTXC0B (i) ➡➡ B of Texture Color Register 0

Texture Color Register 1 for Mix Mode
Register Type: Read/Write
Read/Write Port: 8A8Bh ~ 8A88h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXC1R (i) ➡➡ R of Texture Color Register 1
D[15:8] TTXC1G (i) ➡➡ G of Texture Color Register 1
D[7:0] TTXC1B (i) ➡➡ B of Texture Color Register 1

Texture Color Register for Luminance
Register Type: Read/Write
Read/Write Port: 8A8Fh ~ 8A8Ch
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXCRR (i) ➡➡ R of Luminance
D[15:8] TTXCRG (i) ➡➡ G of Luminance
D[7:0] TTXCRB (i) ➡➡ B of Luminance

Texture Border Color Register
Register Type: Read/Write
Read/Write Port: 8A93h ~ 8A90h
Default: xx xx xx xxh
D[31:24] TXCTBA (i) ➡➡ A of Texture Border
D[23:16] TXCTBR (i) ➡➡ R of Texture Border
D[15:8] TXCTBG (i) ➡➡ G of Texture Border
D[7:0] TXCTBB (i) ➡➡ B of Texture Border

Texture Index Palette Register 0
Register Type: Read/Write
Read/Write Port: 8A97h ~ 8A94h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX0B (i) ➡➡ B of Index 0
D[15:8] TTXIDX0G (i) ➡➡ G of Index 0
D[7:0] TTXIDX0R (i) ➡➡ R of Index 0

Texture Index Palette Register 1
Register Type: Read/Write
Read/Write Port: 8A9Bh ~ 8A98h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX1B (i) ➡➡ B of Index 1
D[15:8] TTXIDX1G (i) ➡➡ G of Index 1
D[7:0] TTXIDX1R (i) ➡➡ R of Index 1

Texture Index Palette Register 2
Register Type: Read/Write
Read/Write Port: 8A9Fh ~ 8A9Ch
Default: xx xx xx xxh
D[31:24] Reserved

D[23:16] TTXIDX2B (i) ➡➡ B of Index 2
D[15:8] TTXIDX2G (i) ➡➡ G of Index 2
D[7:0] TTXIDX2R (i) ➡➡ R of Index 2

Texture Index Palette Register 3
Register Type: Read/Write
Read/Write Port: 8AA3h ~ 8AA0h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX3B (i) ➡➡ B of Index 3
D[15:8] TTXIDX3G (i) ➡➡ G of Index 3
D[7:0] TTXIDX3R (i) ➡➡ R of Index 3

Texture Index Palette Register 4
Register Type: Read/Write
Read/Write Port: 8AA7h ~ 8AA4h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX4B (i) ➡➡ B of Index 4
D[15:8] TTXIDX4G (i) ➡➡ G of Index 4
D[7:0] TTXIDX4R (i) ➡➡ R of Index 4

Texture Index Palette Register 5
Register Type: Read/Write
Read/Write Port: 8AABh ~ 8AA8h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX5B (i) ➡➡ B of Index 5
D[15:8] TTXIDX5G (i) ➡➡ G of Index 5
D[7:0] TTXIDX5R (i) ➡➡ R of Index 5

Texture Index Palette Register 6
Register Type: Read/Write
Read/Write Port: 8AAFh ~ 8AACh
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX6B (i) ➡➡ B of Index 6
D[15:8] TTXIDX6G (i) ➡➡ G of Index 6
D[7:0] TTXIDX6R (i) ➡➡ R of Index 6

Texture Index Palette Register 7
Register Type: Read/Write
Read/Write Port: 8AB3h ~ 8AB0h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX7B (i) ➡➡ B of Index 7
D[15:8] TTXIDX7G (i) ➡➡ G of Index 7
D[7:0] TTXIDX7R (i) ➡➡ R of Index 7

Texture Index Palette Register 8
Register Type: Read/Write

Read/Write Port: 8AB7h ~ 8AB4h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX8B (i) ➡➡ B of Index 8
D[15:8] TTXIDX8G (i) ➡➡ G of Index 8
D[7:0] TTXIDX8R (i) ➡➡ R of Index 8

Texture Index Palette Register 9
Register Type: Read/Write
Read/Write Port: 8ABBh ~ 8AB8h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX9B (i) ➡➡ B of Index 9
D[15:8] TTXIDX9G (i) ➡➡ G of Index 9
D[7:0] TTXIDX9R (i) ➡➡ R of Index 9

Texture Index Palette Register 10
Register Type: Read/Write
Read/Write Port: 8ABFh ~ 8ABCh
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX10B (i) ➡➡ B of Index 10
D[15:8] TTXIDX10G (i) ➡➡ G of Index 10
D[7:0] TTXIDX10R (i) ➡➡ R of Index 10

Texture Index Palette Register 11
Register Type: Read/Write
Read/Write Port: 8AC3h ~ 8AC0h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX11B (i) ➡➡ B of Index 11
D[15:8] TTXIDX11G (i) ➡➡ G of Index 11
D[7:0] TTXIDX11R (i) ➡➡ R of Index 11

Texture Index Palette Register 12
Register Type: Read/Write
Read/Write Port: 8AC7h ~ 8AC4h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX12B (i) ➡➡ B of Index 12
D[15:8] TTXIDX12G (i) ➡➡ G of Index 12
D[7:0] TTXIDX12R (i) ➡➡ R of Index 12

Texture Index Palette Register 13
Register Type: Read/Write
Read/Write Port: 8ACBh ~ 8AC8h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX13B (i) ➡➡ B of Index 13
D[15:8] TTXIDX13G (i) ➡➡ G of Index 13
D[7:0] TTXIDX13R (i) ➡➡ R of Index 13

Texture Index Palette Register 14
Register Type: Read/Write
Read/Write Port: 8ACFh ~ 8ACCh
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX14B (i) ➡➡ B of Index 14
D[15:8] TTXIDX14G (i) ➡➡ G of Index 14
D[7:0] TTXIDX14R (i) ➡➡ R of Index 14

Texture Index Palette Register 15
Register Type: Read/Write
Read/Write Port: 8AD3h ~ 8AD0h
Default: xx xx xx xxh
D[31:24] Reserved
D[23:16] TTXIDX15B (i) ➡➡ B of Index 15
D[15:8] TTXIDX15G (i) ➡➡ G of Index 15
D[7:0] TTXIDX15R (i) ➡➡ R of Index 15

Reserved Registers
Register Type: Read/Write
Read/Write Port: 8AFEh ~ 8AD4h
Default: xx xx xx xxh
D[31:0] Reserved

8.13.12. END OF PRIMITIVE SETTING REGISTER

Register Type: Read/Write
Read/Write Port: 8AFFh
Default: xxh
D[7:0] TEND ➡➡ End of Primitive List
This is a dummy register. The data stored in this register is no meaning.

8.13.13. STIPPLE PATTERN REGISTERS

Stipple Pattern 0 Register
Register Type: Read/Write
Read/Write Port: 8B03h ~ 8B00h
Default: xx xx xx xxh
D[31:0] T0STIP ➡➡ Stipple Pattern 0
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 1 Register
Register Type: Read/Write
Read/Write Port: 8B07h ~ 8B04h
Default: xx xx xx xxh
D[31:0] T1STIP ➡➡ Stipple Pattern 1
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 2 Register
Register Type: Read/Write
Read/Write Port: 8B0Bh ~ 8B08h
Default: xx xx xx xxh
D[31:0] T2STIP ➡➡ Stipple Pattern 2
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 3 Register
Register Type: Read/Write
Read/Write Port: 8B0Fh ~ 8B0Ch
Default: xx xx xx xxh
D[31:0] T3STIP ➡➡ Stipple Pattern 3
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 4 Register
Register Type: Read/Write
Read/Write Port: 8B13h ~ 8B10h
Default: xx xx xx xxh
D[31:0] T4STIP ➡➡ Stipple Pattern 4
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 5 Register
Register Type: Read/Write
Read/Write Port: 8B17h ~ 8B14h
Default: xx xx xx xxh
D[31:0] T5STIP ➡➡ Stipple Pattern 5
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 6 Register
Register Type: Read/Write
Read/Write Port: 8B1Bh ~ 8B18h
Default: xx xx xx xxh
D[31:0] T6STIP ➡➡ Stipple Pattern 6
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 7 Register
Register Type: Read/Write
Read/Write Port: 8B1Fh ~ 8B1Ch
Default: xx xx xx xxh
D[31:0] T7STIP ➡➡ Stipple Pattern 7
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 8 Register
Register Type: Read/Write

Read/Write Port: 8B23h ~ 8B20h
Default: xx xx xx xxh
D[31:0] T8STIP ➡➡ Stipple Pattern 8
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 9 Register
Register Type: Read/Write
Read/Write Port: 8B27h ~ 8B24h
Default: xx xx xx xxh
D[31:0] T9STIP ➡➡ Stipple Pattern 2
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 10 Register
Register Type: Read/Write
Read/Write Port: 8B2Bh ~ 8B28h
Default: xx xx xx xxh
D[31:0] T10STIP ➡➡ Stipple Pattern 10
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 11 Register
Register Type: Read/Write
Read/Write Port: 8B2Fh ~ 8B2Ch
Default: xx xx xx xxh
D[31:0] T11STIP ➡➡ Stipple Pattern 11
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 12 Register
Register Type: Read/Write
Read/Write Port: 8B33h ~ 8B30h
Default: xx xx xx xxh
D[31:0] T12STIP ➡➡ Stipple Pattern 12
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 13 Register
Register Type: Read/Write
Read/Write Port: 8B37h ~ 8B34h
Default: xx xx xx xxh
D[31:0] T13STIP ➡➡ Stipple Pattern 13
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 14 Register
Register Type: Read/Write
Read/Write Port: 8B3Bh ~ 8B38h
Default: xx xx xx xxh

D[31:0] T14STIP ➡➡ Stipple Pattern 14
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 15 Register
Register Type: Read/Write
Read/Write Port: 8B3Fh ~ 8B3Ch
Default: xx xx xx xxh
D[31:0] T15STIP ➡➡ Stipple Pattern 15
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 16 Register
Register Type: Read/Write
Read/Write Port: 8B43h ~ 8B40h
Default: xx xx xx xxh
D[31:0] T16STIP ➡➡ Stipple Pattern 16
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 17 Register
Register Type: Read/Write
Read/Write Port: 8B47h ~ 8B44h
Default: xx xx xx xxh
D[31:0] T17STIP ➡➡ Stipple Pattern 17
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 18 Register
Register Type: Read/Write
Read/Write Port: 8B4Bh ~ 8B48h
Default: xx xx xx xxh
D[31:0] T18STIP ➡➡ Stipple Pattern 18
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 19 Register
Register Type: Read/Write
Read/Write Port: 8B4Fh ~ 8B4Ch
Default: xx xx xx xxh
D[31:0] T19STIP ➡➡ Stipple Pattern 19
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 20 Register
Register Type: Read/Write
Read/Write Port: 8B53h ~ 8B50h
Default: xx xx xx xxh
D[31:0] T20STIP ➡➡ Stipple Pattern 20
0: The pixel should not be written.

1: The pixel should be written.

Stipple Pattern 21 Register
Register Type: Read/Write
Read/Write Port: 8B57h ~ 8B54h
Default: xx xx xx xxh
D[31:0] T21STIP ➡➡ Stipple Pattern 21
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 22 Register
Register Type: Read/Write
Read/Write Port: 8B5Bh ~ 8B58h
Default: xx xx xx xxh
D[31:0] T22STIP ➡➡ Stipple Pattern 22
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 23 Register
Register Type: Read/Write
Read/Write Port: 8B5Fh ~ 8B5Ch
Default: xx xx xx xxh
D[31:0] T23STIP ➡➡ Stipple Pattern 23
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 24 Register
Register Type: Read/Write
Read/Write Port: 8B63h ~ 8B60h
Default: xx xx xx xxh
D[31:0] T24STIP ➡➡ Stipple Pattern 24
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 25 Register
Register Type: Read/Write
Read/Write Port: 8B67h ~ 8B64h
Default: xx xx xx xxh
D[31:0] T25STIP ➡➡ Stipple Pattern 25
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 26 Register
Register Type: Read/Write
Read/Write Port: 8B6Bh ~ 8B68h
Default: xx xx xx xxh
D[31:0] T26STIP ➡➡ Stipple Pattern 26
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 27 Register
Register Type: Read/Write
Read/Write Port: 8B6Fh ~ 8B6Ch
Default: xx xx xx xxh
D[31:0] T27STIP ➡➡ Stipple Pattern 27
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 28 Register
Register Type: Read/Write
Read/Write Port: 8B73h ~ 8B70h
Default: xx xx xx xxh
D[31:0] T28STIP ➡➡ Stipple Pattern28
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 29 Register
Register Type: Read/Write
Read/Write Port: 8B77h ~ 8B74h
Default: xx xx xx xxh
D[31:0] T29STIP ➡➡ Stipple Pattern 29
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 30 Register
Register Type: Read/Write
Read/Write Port: 8B7Bh ~ 8B78h
Default: xx xx xx xxh
D[31:0] T30STIP ➡➡ Stipple Pattern 30
0: The pixel should not be written.
1: The pixel should be written.

Stipple Pattern 31 Register
Register Type: Read/Write
Read/Write Port: 8B7Fh ~ 8B7Ch
Default: xx xx xx xxh
D[31:0] T31STIP ➡➡ Stipple Pattern 31
0: The pixel should not be written.
1: The pixel should be written.

9. ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS

Table 9.1- 1 Absolute Maximum Ratings

PARAMETER	MIN.	MAX.	UNIT
Ambient operation temperature	0	70	^0C
Storage temperature	-40	125	^0C
Input voltage	-0.3	V_{DD}+0.3	V
Output voltage	-0.5	3.3	V

NOTE:
Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

9.2 DC CHARACTERISTICS

T_A = 0 - 70 ^{0}C, V_{DD} = 3.3 V ± 5 %, V_{DD} 5= 5 V ± 5 %,GND = 0 V

Table 9.2- 1 DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
V_{IL}	Input low voltage	-0.5	0.8	V	
V_{IH}	Input high voltage	2.2	V_{DD}+0.3	V	
V_{OL}	Output low voltage	-	0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH} = -1.0 mA
I_{IL}	Input leakage current	-	± 10	uA	
I_{OZ}	tristate leakage current	-	± 20	uA	0.45 < V_{OUT} < V_{DD}

9.3 DC CHARACTERISTICS FOR DAC (ANALOG OUTPUT CHARACTERISTICS)

Table 9.3- 1 DC Characteristics for DAC

DESCRIPTION	MIN	TYPICAL	MAX	UNIT
Black Level	-	0	-	V
White Level	-	660	-	mV
ILE	-1.0	-	+1.0	LSB
DLE	-0.5	-	+0.5	LSB
1 LSB	-	2.625	-	mV
Iref	-	8.40	-	mA

9.4 AC CHARACTERISTICS FOR DAC (ANALOG OUTPUT CHARACTERISTICS)

Table 9.4- 1 AC Characteristics for DAC

DESCRIPTION	PARAMETER	CONDITION	TYPICAL	MAX.	UNIT
Settling Time	Tsett	R=37.5 ohm C1=30 pF	-	6	ns

9.5 AC CHARACTERISTICS FOR INTEGRATED 3D VGA CONTROLLER

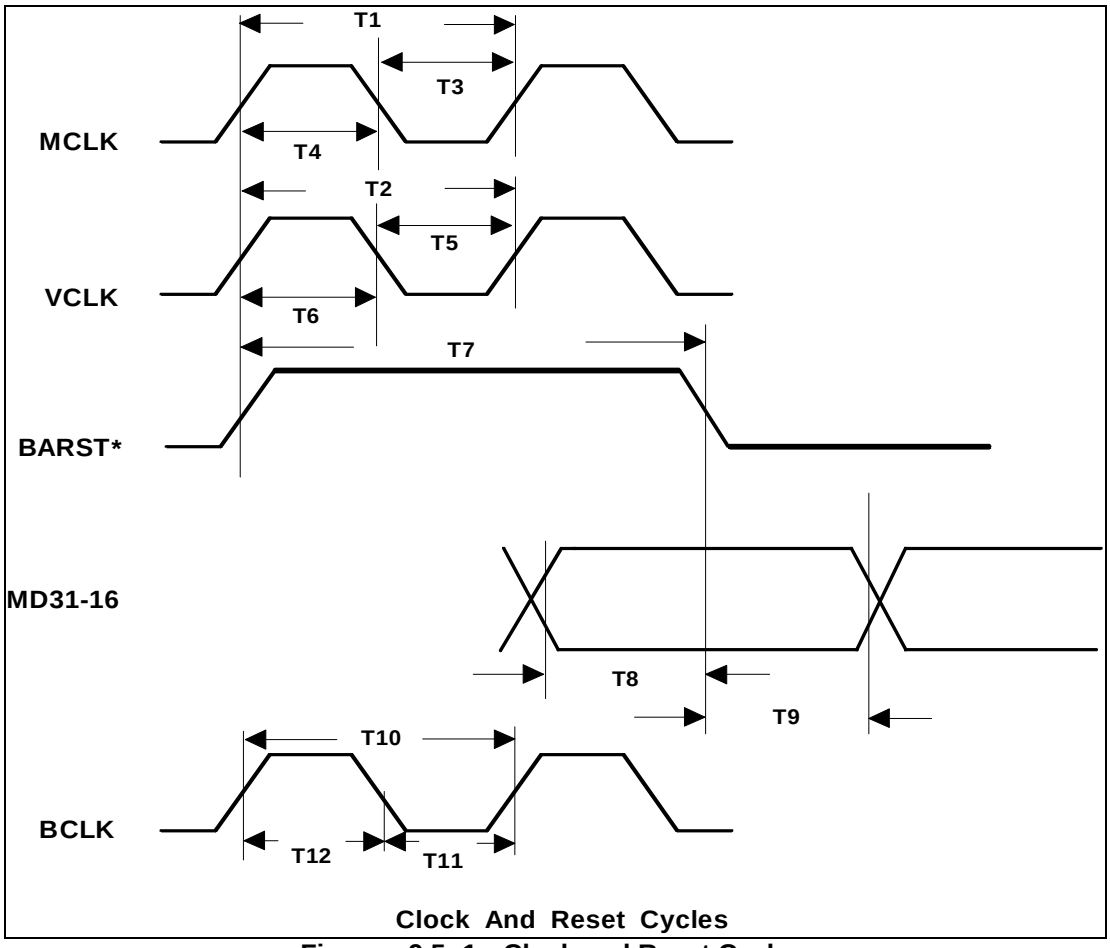


Figure 9.5- 1 Clock and Reset Cycles

Table 9.5- 1 Clock and Reset Timing Table

SYMBOL	PARAMETER	MIN	MAX
T_1	MCLK Period	10	
T_2	VCLK Period	5.5	
T_3	MCLK Low Time	4	
T_4	MCLK High Time	4	

T_5	VCLK Low Time	2.2	
T_6	VCLK High Time	2.2	
T_7	Reset High Time	400	
T_8	System Configuration Data Setup Time	20	
T_9	System Configuration Data Hold Time	20	
T_{10}	BCLK Period (33MHz / 66MHz)	30 /15	∞ / 30
T_{11}	BCLK High Time (33MHz /66MHz)	11 / 6	
T_{12}	BCLK Low Time (33MHz /66MHz)	11 / 6	

(Units: ns)

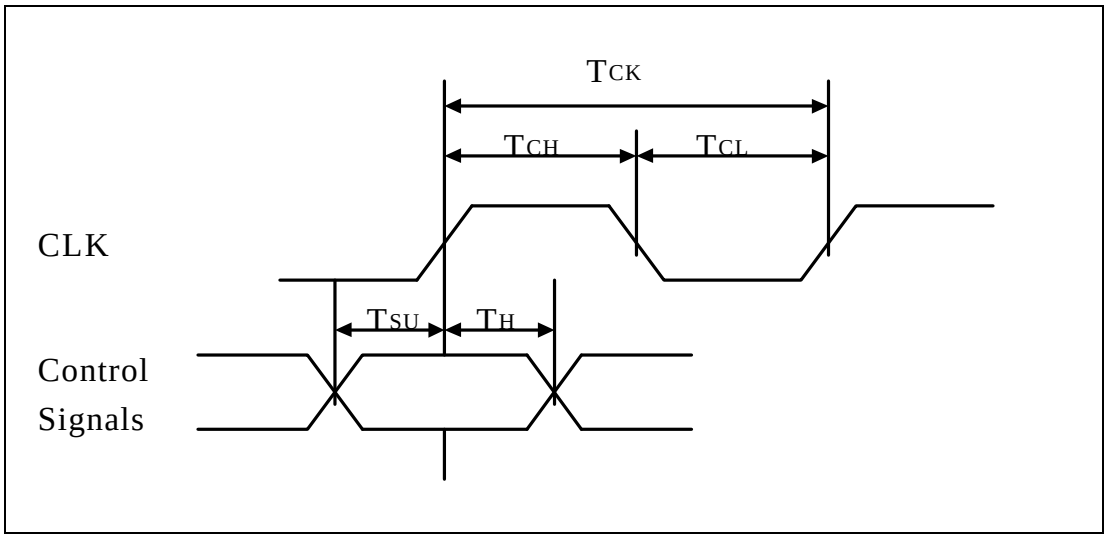


Figure 9.5- 2 SDRAM/SGRAM input/output Timing

Table 9.5- 2 SDRAM/SGRAM Timing Table

SYMBOL	PARAMETER		MIN	MAX.	UNITS
T_{CK}	Clock Cycle Time	latency=3	12 (83.3 MHz)		ns
		latency=2	18 (55 MHz)		ns
T_{CH}	CLK high level width		4		ns
T_{CL}	CLK low level width		4		ns
T_{SU}	Setup Timing		3.5		ns
T_H	Hold Timing		1.5		ns

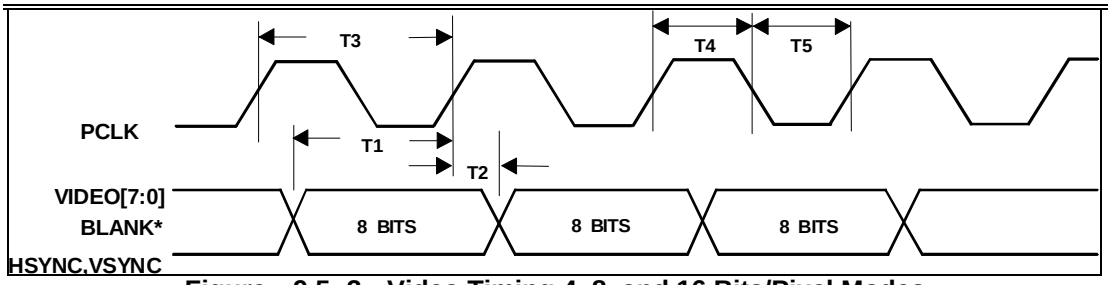


Figure 9.5- 3 Video Timing 4, 8, and 16 Bits/Pixel Modes

Table 9.5-3 16 BPP Video AC Timing Table

SYMBOL	PARAMETER	MIN.	MAX.	NOTES
T_1	VIDEO[7:0], BLANK*, SYNC Setup Time	10	-	
T_2	VIDEO[7:0], BLANK*, SYNC Hold Time	2	-	
T_3	PCLK Period	20	-	
T_4	PCLK High Time	7	-	
T_5	PCLK Low Time	7	-	

(Units: ns)

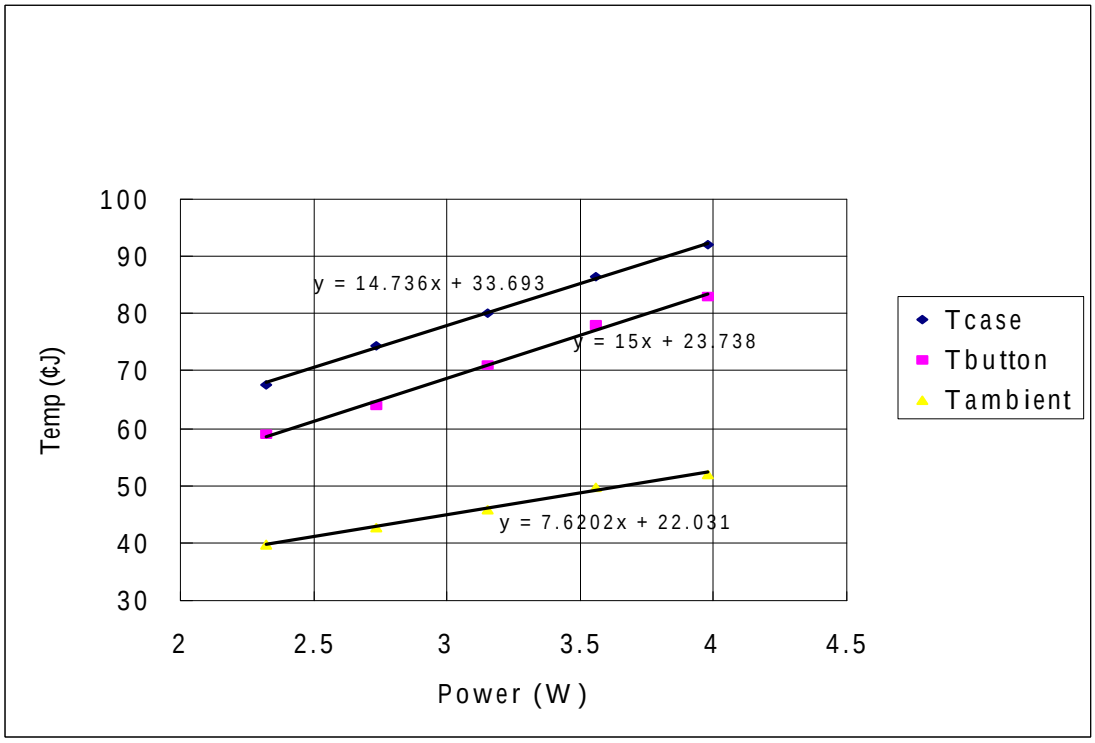
10. THERMAL ANALYSIS

10.1 CHIP THERMAL ANALYSIS WITHOUT HEAT SINK

Room Temperature: 25.3¢ J
Result:

Power (W)	2.325	2.737	3.152	3.5595	3.98
Tcase (¢)	67.7	74.3	80.1	86.4	92.1
Tbutton (¢)	59	64	71	78	83
Tambient (¢)	39.8	42.7	45.9	49.8	52

Note: Tcase: Temperature at the molding compound surface.
Tbutton: Temperature at the back side of PCB where thermal balls are directly attend.
Tambient: Temperature at PCB near the side of the BGA package.

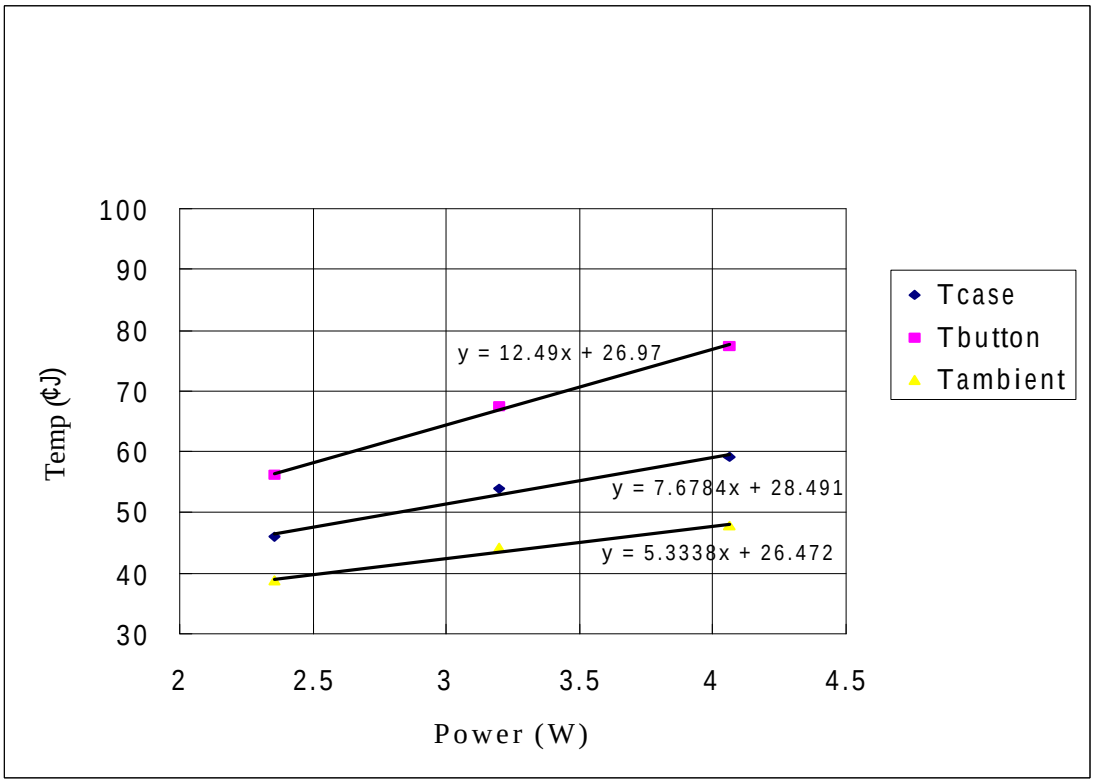


Test Condition:
CPU 100MHz, SDRAM 100MHz, VGA 100MHz, PCI 33.3MHz.
OS: Window 95.
Resolution: 1024*768 16bit High Color, Refresh Rate: 75Hz.
Run one 2D program(Speedy)+ six 3D samples(Direct 3DRM example).
Sample Time: at least 30 mins.
Result: 82.3¢ J

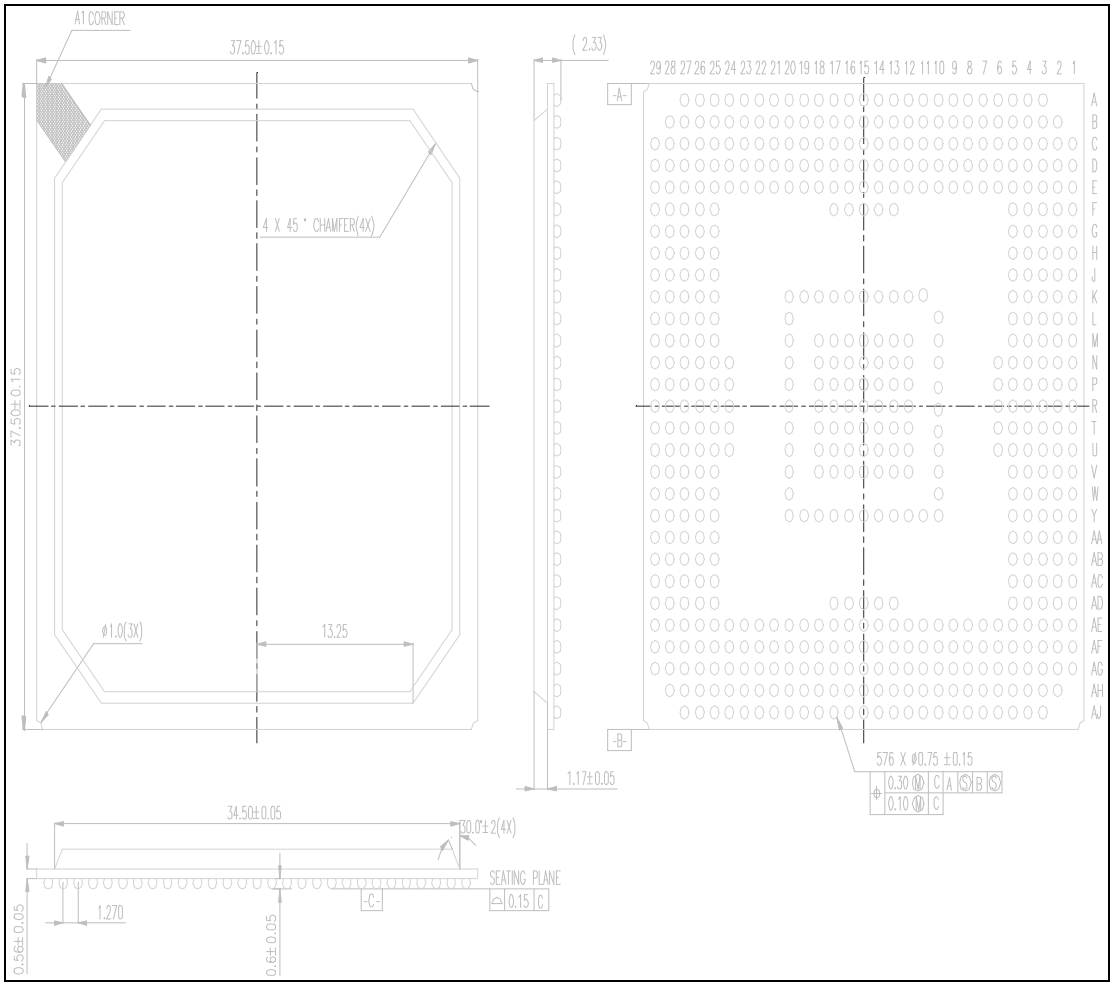
10.2 CHIP THERMAL ANALYSIS WITH HEAT SINK

Room Temperature : 25.3¢ J
Result :

Power (W)	2.325	2.737	3.152	3.5595	3.98
Tcase (¢)	56.7	62.3	65.4	72.1	76.9
Tbutton (¢)	45.4	49.2	54.3	56.7	59.8
Tambient (¢)	38.2	41.4	43.4	46.4	48.2



11. MECHANICAL DIMENSION



12. TOPSIDE MARK IDENTIFICATION

Topside Mark	(Description)
	Logo
530	Part No.
©ΘSiS'98	Internal Control No.
□□□□□□□	Internal Control No.
□□□□□□ xx	Internal Control No. & Rev.

13. COPYRIGHT NOTICE

Pentium PCI / AGP 3D VGA Chipset

SiS530

Preliminary

Rev. 1.0

NOV. 10, 1998