AMD RS690 Databook

Technical Reference Manual
Rev. 3.04

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Please note that in this databook, references to "DVI" and "HDMI" may refer to: (1) the function of the integrated DVI/HDMI interface described in details in section 2.2.1 and 3.7, as well as in other sections; or (2) the capability of the TMDS interface, multiplexed on the PCI-E external graphics interface, to enable DVI or HDMI through passive enabling circuitries. Any statement in this databook on any DVI or HDMI-related functionality must be understood to apply to (1), (2), or both, according to the immediate context of the reference.

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Chapter 1
Overview

1.1 Introducing the RS690

The RS690 is a seventh generation Integrated Graphics Processor (IGP) that integrates a DirectX® 9.0 compliant 2D/3D graphics core and a system controller in a single chip. It supports the AMD Athlon™ 64, Athlon 64 FX, Athlon 64 X2, AMD and Sempron processors, including AM2 socket CPUs. All CPUs are supported on both high performance and value platforms.

The RS690 integrates an ATI Radeon™ X700-based graphics engine, dual display, a TV encoder, an integrated DVI/HDMI interface, an integrated TMDS controller, and Northbridge functionality in a single BGA package. This high level of integration and scalability enables manufacturers to offer enthusiast level capabilities and performance while minimizing board space and system cost.

The RS690 is pin-compatible with AMD's RS485, allowing existing RS485 platforms to easily migrate to the RS690. Comparing with the RS485, the RS690 provides additional features with reduced overall system power.

Robust and Flexible Core Logic Features

The RS690 combines graphics and system logic functions in a single chip using a 21mm-body FCBGA package, reducing overall solution area. For optimal system and graphics performance, the RS690 supports a high speed HyperTransport™ interface to the AMD processor, running at a data rate of up to 2GT/s and supporting the new generation of AM2 socket processors. The RS690 is ideally suited to 64-bit operating systems, and supports platform configurations with greater than 4GB of system memory. The rich PCI Express® expansion capabilities of RS690, including support for PCI Express external graphics and up to four other PCI Express peripherals (or five, when using only 8 lanes for external graphics), are complemented by the advanced I/O features of AMD's SB600 Southbridge.

Best for Windows Vista™

The RS690 delivers the best Windows Vista™ experience of any integrated graphics and core logic product for the AMD platform. It incorporates an ATI Radeon™ X700-based graphics core, which provides the 3D rendering power needed to generate the Windows Vista desktop even under the most demanding circumstances. In addition, dedicated hardware acceleration is provided for key new Windows Vista features such as ClearType®. This ATI Radeon X700-based graphics technology also enables great 3D application performance through SmartShader™ HD, SmoothVision™ HD, and 3Dc™ technologies.

Leading Multimedia Capabilities

The RS690 incorporates the innovative ATI Avivo™* display architecture, providing users with visual quality which is second to none. Advanced scaling and color correction capabilities, along with increased precision through the entire display pipeline, ensure an optimal image on CRT monitors, LCD panels, and any other display devices. A new TV encoder, based on designs used in ATI's Xilleon™ products, provides unequalled quality, and fully integrated DVI/HDMI and HDCP support allows compatibility with even the most modern high definition televisions without the additional cost of external components.

***Note:** ATI Avivo™ is a technology platform that includes a broad set of capabilities offered by certain ATI Radeon products. Full enablement of some ATI Avivo™ capabilities may require complementary products.

Low Power Consumption and Industry Leading Power Management

The RS690 is manufactured using a power efficient 80nm technology, and it supports a whole range of industry standards and all new proprietary power management features. It provides comprehensive support for the ACPI specification and AMD power management features such as AMD PowerNow!™. The RS690 family also includes variants with support for dedicated local display cache memory, which further reduces system power consumption.

Software Compatibility

The graphics driver for the RS690 is fully compatible with all other ATI Radeon class graphics controllers from AMD. A single driver can support multiple graphics configurations across AMD's product lines, including the ATI Radeon family and the AMD chipset family. In addition, this driver compatibility allows the RS690 to benefit immediately from AMD's software optimization and from the advanced Windows® XP and Windows Vista support available in the ATI Radeon family drivers.

1.2 RS690C

The RS690C is a special variant of the RS690 that supports neither a DVI/HDMI interface nor a TMDS interface that enables DVI/HDMI. Beyond the difference, all other information in this document applies to both the RS690 and RS690C, unless otherwise specified.

1.3 RS690 Features

1.3.1 CPU HyperTransport™ Interface

- Supports the mobile and desktop Athlon 64/Athlon 64 FX/Athlon X2/AMD Sempron processors, including AM2 socket CPUs.
- Supports 200, 400, 600, 800, and 1000MHz HyperTransport (HT) interface speeds.
- Supports LDTSTP interface, CPU throttling, and stutter mode.

1.3.2 ATI HyperMemory™ Technology

- Supports ATI HyperMemory™* technology.

*** Note:** The amount of HyperMemory available includes both dedicated and shared memory and is determined by various factors. For details, please refer to the product advisory numbered PA_IGPGenC5, available on AMD's OEM Resource Center or from you AMD CSS representative.

1.3.3 PCI Express® Interface

- Compliant with the PCI Express (PCI-E) 1.1a Specification.
- Highly flexible PCI-E implementation to suit a variety of platform needs.
- Supports a x16 graphics interface.
- A single-port, x16 graphics interface, configurable to any of the following modes of support:
  - An external graphics device utilizing all 16 lanes.
  - A TMDS interface, enabling DVI/HDMI (see *section 1.3.9, "DVI/HDMI (Not applicable to the RS690C)"* below for details).
  - A single x1, x2, x4, or x8 general purpose PCI-E link.
- A four-port, x4 PCI Express general purpose interface, configurable to one of the following modes of support:
  - Four x1 links.
  - Two x2 links.
  - One x2 and two x1 links.
  - One x4 link.

1.3.4 A-Link Express II Interface

- One x4 A-Link Express II interface (PCI Express 1.1 compliant) for connection to an AMD Southbridge, providing more bandwidth than the older A-Link Express interface.

1.3.5 2D Acceleration Features

- Highly-optimized 128-bit engine, capable of processing multiple pixels per clock.
- Hardware acceleration of Bitblt, Line Draw, Polygon / Rectangle Fill, Bit Masking, Monochrome Expansion, Panning/Scrolling, Scissoring, and full ROP support (including ROP3).
- Optimized handling of fonts and text using AMD proprietary techniques.
- Hardware acceleration for ClearType font rendering.
- Game acceleration including support for Microsoft's DirectDraw®: Double Buffering, Virtual Sprites, Transparent Blit, and Masked Blit.
- Supports a maximum resolution of 2048x1536 @ 32bpp for a maximum pixel clock speed of 400MHz (driver-limited).
- Acceleration in 1/8/15/16/32 bpp modes:
  - ClearType mode for 1bpp
  - Pseudocolor mode for 8bpp
  - ARGB1555 and RGB565 modes for 16bpp
  - ARGB8888 mode for 32bpp
- Significant increase in the High-End Graphics WinBench® score due to capability for C18 color expansion.
- Setup of 2D polygons and lines.
- Support for GDI extensions in Windows XP and Windows Vista: Alpha BLT, Transparent BLT, Gradient Fill.
- Hardware cursor (up to 64x64x32bpp), with alpha channel for direct support of Windows XP and Windows Vista alpha cursor.

1.3.6 3D Acceleration Features

- Multi-texturing via one texture blending unit per pixel pipes, allowing up to 512 texel reads per pixel in a single pass.
- 3D texture support, including projective 3D textures.
- Comprehensive support for bump mapping: emboss, dot-product, and environment bump maps.
- Improved precision in anisotropic filtering and bilinear filtering.
- Supports a maximum resolution of 2048x1536 @ 32bpp for a maximum pixel clock speed of 400MHz (driver-limited).
- Complete 3D primitive support: points, lines, triangles, lists, strips and quadrilaterals and BLTs with Z compare.
- Improved texture compositing.
- Hidden surface removal using 16, 24, or 32-bit Z-buffering (maximum Z-buffer depth is 24 bits when stencil buffer enabled) and Early Z hardware.
- 8-bit stencil buffer.
- Bilinear and trilinear texture filtering.
- Full support of Direct3D texture lighting.
- Dithering support in 16bpp for near 24bpp quality in less memory.
- Extensive 3D mode support.
- Anti-aliasing using multi-sampling algorithm with support for 2, 4, and 6 samples.
- Optimized for full performance in true color triple buffered 32bpp acceleration modes.
- New generation rendering engine provides top 3D performance.
- Support for OpenGL format for Indirect Vertices in Vertex Walker.
- Full DirectX 9.0 support (Vertex Shader version 2.0 and Pixel Shader version 2.0):
  - Full precision floating point pixel pipeline.

- Support for up to 4 MRTs (Multiple-Render-Targets).
- Support for writing all texture formats from render pipe in floating points (including cube mapes and 3D textures).
- Support for up to 512bpp formats (4 color case).
- Advanced setup engine, capable of processing 1 polygon (lit and textured) per cycle.

1.3.7 Motion Video Acceleration Features

- Enhanced MPEG-2 hardware decode acceleration (SD contents only), including support for:
  - Integrated general purpose iDCT engine for MPEG2 and DV decode acceleration.
  - Integrated MPEG motion compensation engine for decode acceleration.
  - Parallel operation of the iDCT and MC and high processing rates with minimal software overhead.
- Supports Microsoft DirectX Video Acceleration (DirectX VA) 2.0 (for SD contents only).
- Provides dramatically reduced CPU utilization without incurring the cost of a full MPEG-2 decoder.
- MPEG-4 simple profile support.
- Supports top quality DVD with low CPU usage.
- Hardware-based adaptive de-interlacing filter and scaler provide high quality full-screen and full-speed video playback. Minimizes the aliasing artifacts along edges usually caused by a conventional deinterlacer/scaler.

1.3.8 Multiple Display Features

General

- [Not applicable to the RS690C] Dual independent displays. Possible configurations include:
  - CRT and DVI/HDMI
  - TV (component, composite, or S-Video) and DVI/HDMI
  - DVI and DVI*
  - DVI and HDMI*

  * **Note:** The options require implementation of the TMDS interface that is multiplexed on the PCI-E external graphics interface; see *section 1.3.9, "DVI/HDMI (Not applicable to the RS690C)," on page 1-5*.
- [Not applicable to the RS690C] Resolution, refresh rates, and display data can be completely independent for the two display paths.
- Each display controller supports true 30bpp throughout the display pipeline.
- Each display path supports VGA and accelerated modes, video overlay, hardware cursor, hardware icon, and palette gamma correction.
- Supports both interlaced and non-interlaced displays.
- Support for display modes up to 2880 pixels/line per display.
- Full ratiometric expansion ability is supported for source desktop modes up to 1920 pixels/line.
- HD TV support (with underscan) for display modes of 1920 or less pixels/line.
- SD TV support (with underscan) for display modes of 1024 or less pixels/line.
- Maximum DAC frequency of 400MHz.
- Supports 8, 16, 32 & 64-bpp depths for the main graphics layer:
  - For 32-bpp depth, supports xRGB 8:8:8:8, xRGB 2:10:10:10, sCrYCb 8:8:8:8, and xCrYCb 2:10:10:10 data formats.
  - For 64-bpp depth, supports xRGB 16:16:16:16 data format.
- Independent gamma, color conversion and correction controls for main graphics layer.

- Supports display resolutions beyond 2560x1600.
- Support for DDC1 and DDC2B+ for plug and play monitors.
- 8-bit alpha blending of graphics and video overlay.
- Hardware cursor up to 64x64 pixels in 2bpp, full color AND/XOR mix, and full color 8-bit alpha blend.
- Hardware icon up to 128x128 pixels in 2bpp, with two colors, transparent, and inverse transparent. AND/XOR mixing. Supports 2x2 icon magnification.
- Virtual desktop support.
- Support for flat panel displays via VGA, DVI (not applicable to the RS690C), or HDMI (not applicable to the RS690C).
- [Not applicable to the RS690C] Integrated HD Audio Controller for HDMI audio data.
- Support for stereoscopic monitors.

TV Out

- An integrated TV encoder from AMD's Xilleon products, with an on-chip DAC (shared with the CRT analog output) (**Note:** Simultaneous output for TV and CRT is **not** supported).
- 10-bit DAC with 10-tap filter producing scaled, flicker removed, artifact suppressed display on a PAL or NTSC TV with composite, S-Video, component, and RGB output.
- With the proper BIOS implementation, supports different TV standards including NTSC, NTSC-J, PAL-M, PAL-CN, PAL-B, PAL-G, PAL-D, PAL-H, PAL-I, PAL-K, and PAL-N.
- Supports Macrovision 7.1 copy protection standard (required by DVD players).
- Supports a maximum resolution of 1024x768.
- Supports the following formats of YPbPr component output: 480i, 480p, 576i, 576p, 720p, and 1080i.
- Internal adaptive flicker filtering available on both display paths for interlaced TV outputs.
- Supports fully-programmable 2D, adaptive comb filter for composite output.
- TV-out power management support.
- Line 21 Closed Caption and Extended Data Service support for encoding in Vertical Blanking Interval (VBI) of TV signal.
- CGMS copy management support in VBI through Line-20 and/or Extended Data Service (Line-21 Field 2) for NTSC, and through Wide Screen Signaling data (WSS) for PAL.

SURROUNDVIEW

- RS690's SURROUNDVIEW™ feature allows support for up to three independent monitors for systems equipped with an additional ATI discrete graphics card (requires special BIOS and display driver support).

1.3.9 DVI/HDMI (Not applicable to the RS690C)

- Integrated DVI or HDMI interface: single-link support only for HDMI‡, 30-bit dual-link support for DVI.
- Also supports a TMDS interface, enabling DVI or HDMI*, which is multiplexed on the PCI-E external graphics interface (only available if no external graphics card, or only a x8 one, is attached to the PCI-E external graphics interface).‡
- 1650 Mbps/channel† with 165MHz† pixel clock rate per link.
- Supports industry standard EVA-861B video modes including 480p, 720p, and 1080i. For a full list of currently supported modes, contact your AMD CSS representative.
- HDMI basic audio support at 32, 44.1, and 48 kHz. Supports two-channel uncompressed audio and multi-channel audio compressed to two channels like 5.1 AC3 and DTS. HD Audio device compatible with Microsoft's HD audio drivers.
- HDCP support on data stream for single-link transmission, with on-chip key storage (available only on **either one** of the integrated DVI/HDMI interface **or** the TMDS interface (multiplexed on the PCI-E graphics lanes) at any time).**

Notes: * CEC is not supported.

† To be qualified.

** HDCP content protection is only available to licensed buyers of the technology and can only be enabled when connected to an HDCP-capable receiver.

‡ The TMDS interface multiplexed on the PCI-E graphics lanes cannot enable HDMI when the integrated DVI/HDMI interface is supporting HDMI, and vice versa.

1.3.10 Power Management Features

- Fully supports ACPI states S1, S3, S4, and S5.
- The chip power management support logic supports four device power states defined for the OnNow Architecture—On, Standby, Suspend, and Off. Each power state can be achieved by software control bits.
- Hardware controlled intelligent clock gating enables clocks only to active functional blocks, and is completely transparent to software.
- Support for AMD Cool'n'Quiet™ technology via FID/VID change.
- Support for AMD PowerNow!™ technology.
- Clocks to every major functional block are controlled by a unique dynamic clock switching technique that is completely transparent to the software. By turning off the clock to the block that is idle or not used at that point, the power consumption is significantly reduced during normal operation.
- Support dynamic lane reduction for the PCI-E interfaces, adjusting lane width according to required bandwidth.

1.3.11 PC Design Guide Compliance

The RS690 complies with all relevant Windows Logo Program (WLP) requirements from Microsoft for WHQL certification.

1.3.12 Test Capability Features

The RS690 has a variety of test modes and capabilities that provide a very high fault coverage and low DPM (Defect Per Million) ratio:

- Full scan implementation on the digital core logic through ATPG (Automatic Test Pattern Generation) vectors.
- Dedicated test logic for the on-chip custom memory macros to provide complete coverage on these modules.
- A JTAG test mode to allow board level testing of neighboring devices.
- An EXOR tree test mode on all the digital I/O's to allow for proper soldering verification at the board level.
- A VOH/VOL test mode on all digital I/O’s to allow for proper verification of output high and output low values at the board level.
- Improved access to the analog modules to allow full evaluation and characterization.
- Improved IDDQ mode support to allow chip evaluation through current leakage measurements.

These test modes can be accessed through the settings on the instruction register of the JTAG circuitry.

1.3.13 Packaging

- Single chip solution in 80nm, 1.2V low power CMOS technology.
- 465-FCBGA package, 21mmx21mm.

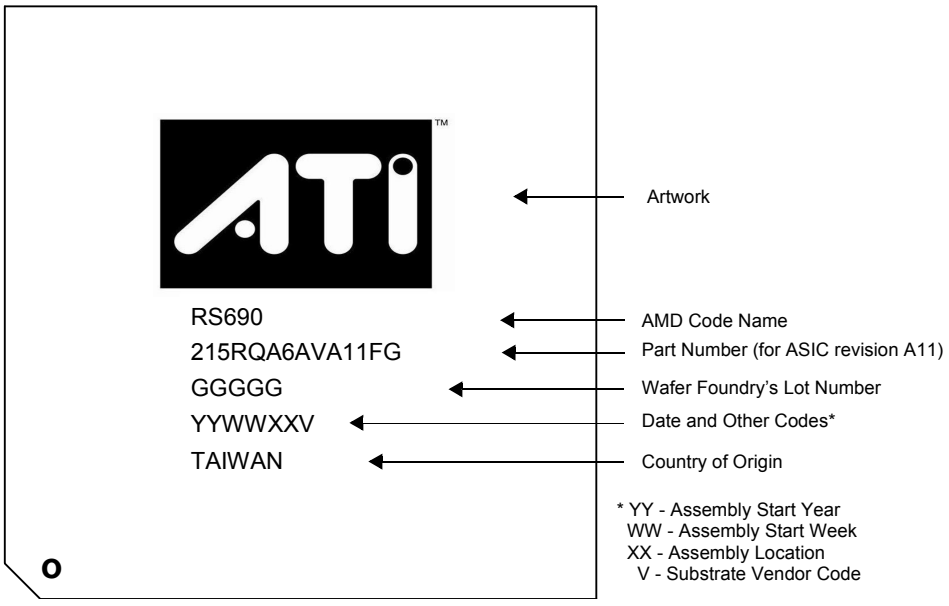
1.4 Software Features

- Supports Microsoft Windows XP and Windows Vista operating systems.
- BIOS ability to read EDID 1.1, 1.2, and 1.3.
- Ability to selectively enable and disable several devices including CRT, LCD, TV, and DFP.
- Register-compatible with VGA standards, BIOS-compatible with VESA VBE2.0.

- Supports corporate manageability requirements such as DMI.
- ACPI support.
- Full Write Combining support for maximum performance of the CPU.
- Full-featured, yet simple Windows utilities:
  - Calibration utility for WYSIWYG color
  - Independent brightness control of desktop and overlay
  - End user diagnostics
- Drivers meet Microsoft's rigorous WHQL criteria and are suitable for systems with the "Designed for Windows" logos.
- Comprehensive OS and API support.
- Hot-key support (Windows ACPI 1.0b or AMD Event Handler Utility where appropriate).
- Extensive power management support.
- Rotation mode support in software.
- Dual CRTC, simultaneous view, extended desktop support (Windows XP and Windows Vista)
- DirectX 9.0 support.
- Switchable overlay support.
- H.264 playback support.

1.5 Branding Diagrams

1.5.1 Branding Diagrams for ASIC Revision A11



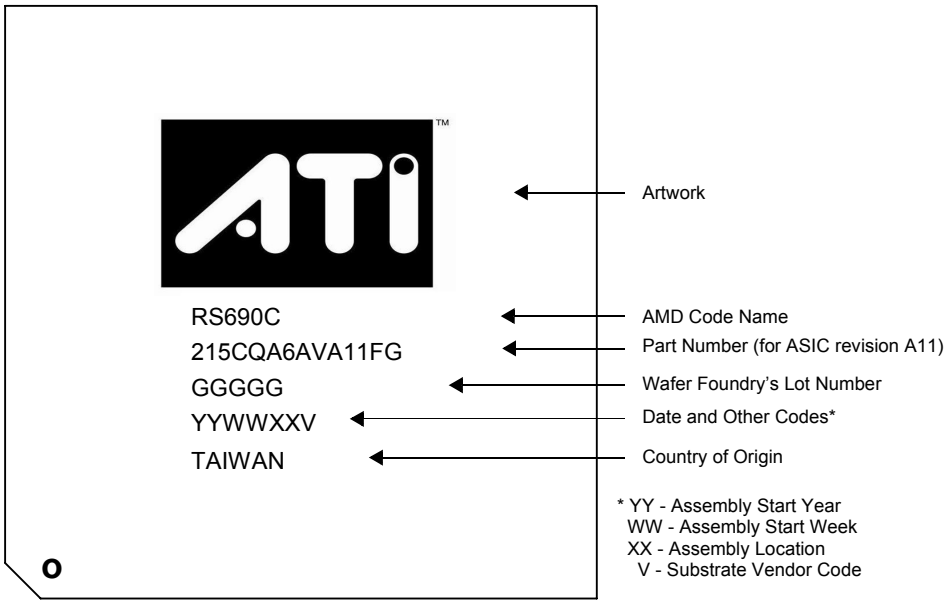
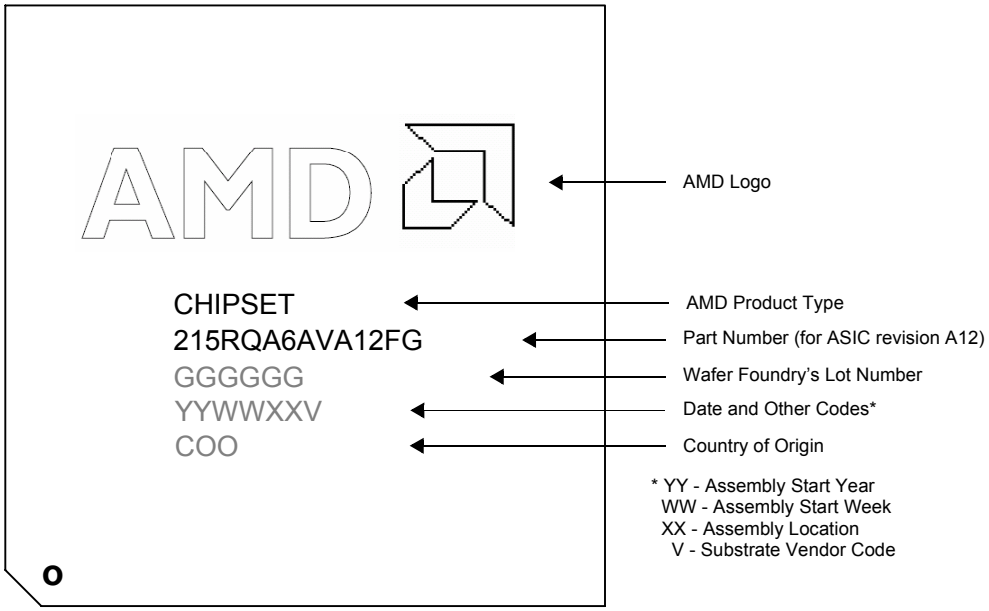


Figure 1-1 RS690-variant Branding Diagrams for ASIC Revision A11

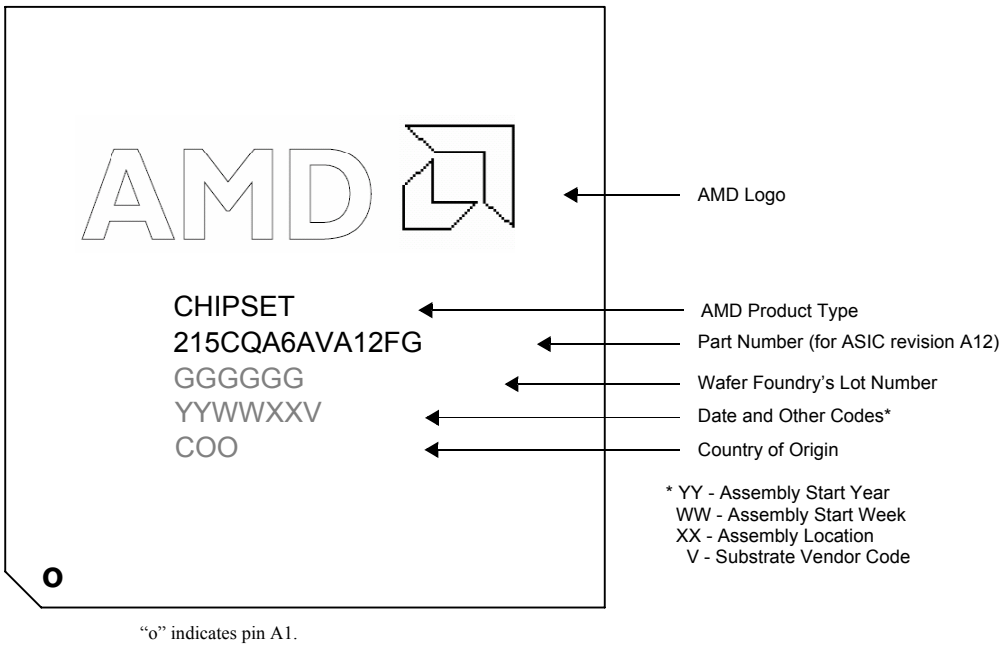
1.5.2 Branding Diagrams for ASIC Revision A12 and After

Note: The branding diagrams below do not necessarily contain the latest ASCI revision numbers for the IGPs. Unless specified otherwise, no information in this databook is specific to the ASIC revision numbers given in the diagrams.



"o" indicates pin A1.

Figure 1-2 RS690 Branding Diagram for ASIC Revision A12 and After



"o" indicates pin A1.

Figure 1-3 RS690C Branding Diagram for ASIC Revision A12 and After

1.6 Part Number Legend

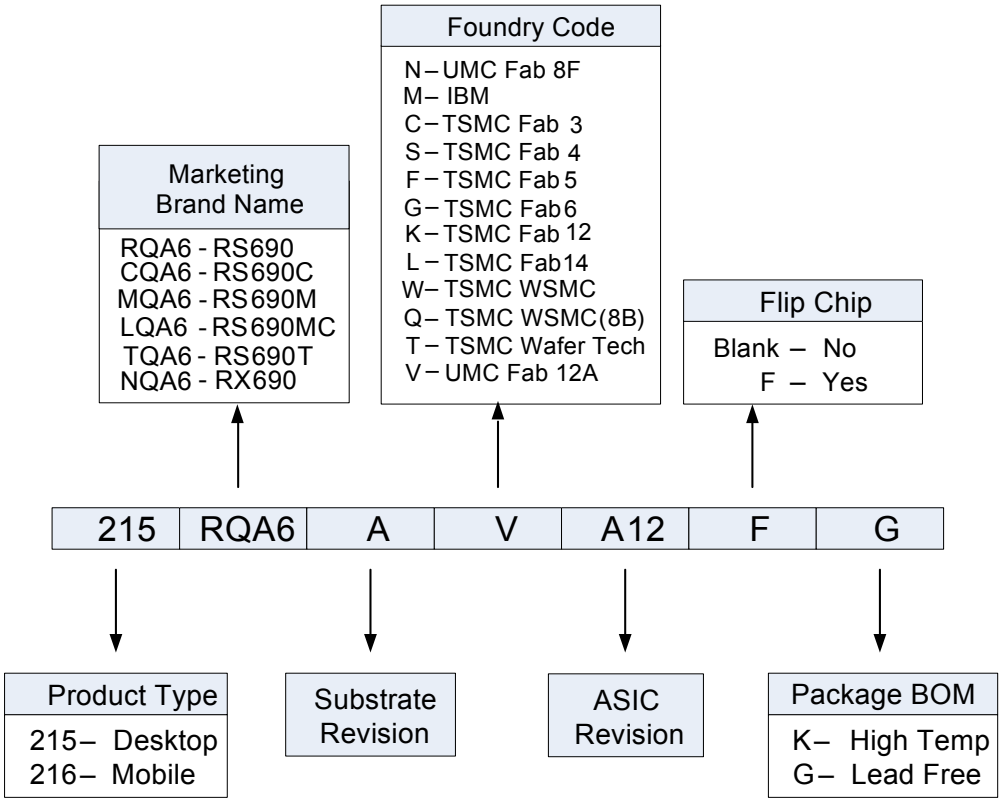


Figure 1-4 The RS690-Family ASIC Part Number Legend

Table 1-1 RS690-Family ASIC Part Numbers

Code Name	Part Number
RS690	215RQA6AVA12FG
RS690C	215CQA6AVA12FG
RS690M	216MQA6AVA12FG
RS690MC	216LQA6AVA12FG
RS690T	216TQA6AVA12FG
RX690	215NQA6AVA12FG

1.7 Conventions and Notations

The following conventions are used throughout this manual.

1.7.1 Pin Names

Pins are identified by their pin names or ball references. Multiplexed pins assume alternate "functional names" when they perform their alternate functions, and these "functional names" are given in *Chapter 3, "Pin Descriptions and Strap Options."*

All active-low signals are identified by the suffix '#' in their names (e.g., LDTSTOP#).

1.7.2 Pin Types

The pins are assigned different codes according to their operational characteristics. These codes are listed in *Table 1-2*.

Table 1-2 Pin Type Codes

Code	Pin Type
I	Digital Input
O	Digital Output
OD	Open Drain
I/O	Bi-Directional Digital Input or Output
M	Multifunctional
Pwr	Power
Gnd	Ground
A-O	Analog Output
A-I	Analog Input
A-I/O	Analog Bi-Directional Input/Output
A-Pwr	Analog Power
A-Gnd	Analog Ground
Other	Pin types not included in any of the categories above

1.7.3 Numeric Representation

Hexadecimal numbers are appended with "h" (Intel assembly-style notation) whenever there is a risk of ambiguity. Other numbers are in decimal.

Pins of identical functions but different trailing integers (e.g., "CPU_D0, CPU_D1,... CPU_D7") are referred to collectively by specifying their integers in square brackets and with colons (i.e., "CPU_D[7:0]"). A similar short-hand notation is used to indicate bit occupation in a register. For example, NB_COMMAND[15:10] refers to the bit positions 10 through 15 of the NB_COMMAND register.

1.7.4 Register Field

A field of a register is referred to by the format of [Register Name].[Register.Field]. For example, "NB_MC_CNTL.DISABLE_BYPASS" is the "DISABLE_BYPASS" field of the register "NB_MC_CNTL."

1.7.5 Hyperlinks

Phrases or sentences in *blue italic font* are hyperlinks to other parts of the manual. Users of the PDF version of this manual can click on the links to go directly to the referenced sections, tables, or figures.

1.7.6 Acronyms and Abbreviations

The following is a list of the acronyms and abbreviations used in this manual.

Table 1-3 Acronyms and Abbreviations

Acronym	Full Expression
ACPI	Advanced Configuration and Power Interface
A-Link-E II	A-Link Express II interface between the IGP and the Southbridge.
BGA	Ball Grid Array
BIOS	Basic Input Output System. Initialization code stored in a ROM or Flash RAM used to start up a system or expansion card.
BIST	Built In Self Test.
BLT	Blit
bpp	bits per pixel
CEC	Consumer Electronic Control
CPIS	Common Panel Interface Specification
CRT	Cathode Ray Tube
CSP	Chip Scale Package
DAC	Digital to Analog Converter
DBI	Dynamic Bus Inversion
DDC	Display Data Channel. A VESA standard for communicating between a computer system and attached display devices.
DDR	Double Data Rate
DFP	Digital Flat Panel. Monitor connection standard from VESA.
DPM	Defects per Million
DTV	Digital TV
DVD	Digital Video Disc
DVI	Digital Video Interface. Monitor connection standard from the DDWG (Digital Display Work Group).
DVS	Digital Video Stream
EPROM	Erasable Programmable Read Only Memory
FIFO	First In, First Out
FPDI	Flat Panel Display Interface
GDI	Graphics Device Interface
GND	Ground
GPIO	General Purpose Input/Output
GTL+	Gunning Transceiver Logic
HDCP	High-Bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
HDTV	High Definition TV. The 1920x1080 and the 1280x720 modes defined by ATSC.
HPD	Hot Plug Detect
iDCT	inverse Discrete Cosine Transform
IDDQ	Direct Drain Quiescent Current
IGP	Integrated Graphics Processor. A single device that integrates a graphics processor and a system controller.

Table 1-3 Acronyms and Abbreviations (Continued)

Acronym	Full Expression
JTAG	Joint Test Access Group. An IEEE standard.
MB	Mega Byte
MPEG	Motion Pictures Experts Group. Refers to compressed video image streams in either MPEG-1 or MPEG-2 formats.
NTSC	National Television Standards Committee. The standard definition TV system used in North America and other areas.
PAL	Phase Alternate Line. The standard definition TV system used in Europe and other areas.
PCI	Peripheral Component Interface
PCI-E	PCI Express
PCMCIA	Personal Computer Memory Card International Association. It is also the name of a standard for PC peripherals promoted by the Association.
PLL	Phase Locked Loop
POST	Power On Self Test
PD	Pull-down Resistor
PU	Pull-up Resistor
ROP	Raster Operation
SDRAM	Synchronous Dynamic RAM
TMDS	Transition Minimized Differential Signaling
UMA	Unified Memory Architecture
UV	Chrominance (also CrCb). Corresponds to the color of a pixel.
UXGA	Ultra Extended Graphics Array
VBI	Vertical Blank Interval
VESA	Video Electronics Standards Association
VGA	Video Graphics Adapter
VRM	Voltage Regulation Module

Chapter 2
Functional Descriptions

This chapter describes the functional operation of the major interfaces of the RS690 system logic chip. *Figure 2-1, "RS690 Internal Block Diagram,"* illustrates the RS690 internal blocks and interfaces.

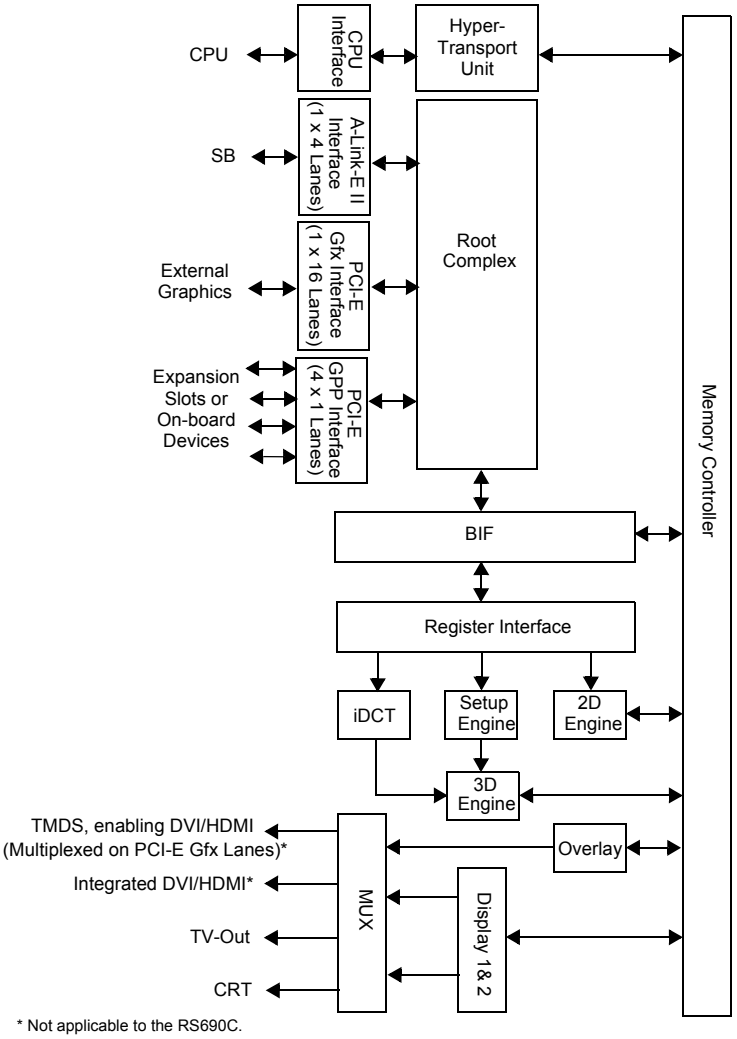


Figure 2-1 RS690 Internal Block Diagram

2.1 Host Interface

The RS690 is optimized to interface with the Athlon 64/Athlon 64 FX/Athlon X2/AMD Sempron processors, including AM2 socket CPUs. This section presents an overview of the HyperTransport interface. For a detailed description of the interface, please refer to the HyperTransport I/O Link Specification from the HyperTransport Consortium. *Figure 2-2, "Host Interface Block Diagram,"* illustrates the basic blocks of the host bus interface of the RS690.

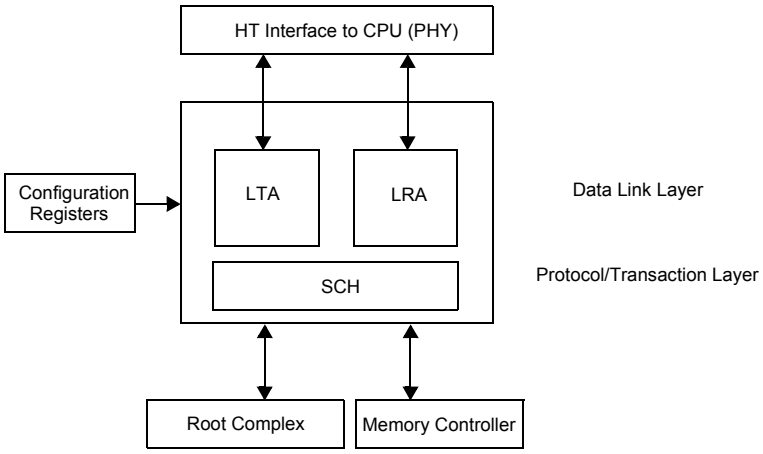


Figure 2-2 Host Interface Block Diagram

The HyperTransport (HT) Interface, formerly known as the LDT (Lightning Data Transport) interface, is a high speed, packet-based link implemented on two unidirectional buses. It is a point-to-point interface where data can flow both upstream and downstream at the same time. The commands, addresses, and data travel in packets on the HyperTransport link. Lengths of packets are in multiples of four bytes. The HT link consists of three parts: the physical layer (PHY), the data link layer, and the protocol/transaction layer. The PHY is the physical interface between the RS690 and the CPU. The data link layer includes the initialization and configuration sequences, periodic redundancy checks, connect/disconnect sequences, and information packet flow controls. The protocol layer is responsible for maintaining strict ordering rules defined by the HT protocol.

The RS690 HyperTransport bus interface consists of 17 unidirectional differential data/control pairs and two differential clock pairs in each of the upstream and downstream direction. On power up, the HT link is 8 bits wide and runs at a default speed of 200MT/s. After negotiation, carried out by the HW and SW together, the link width can be brought up to 16 bits and the interface can run up to 2GT/s. The interface is illustrated in *Figure 2-3, "RS690 Host Bus Interface Signals," on page 2-3.* The signal name and direction for each signal is shown with respect to the processor. Please note that the signal names may be different from those used in the pin listing of the RS690. Detailed descriptions of the signals are given in *section 3.3, "CPU HyperTransport Interface,' on page 3-5*.

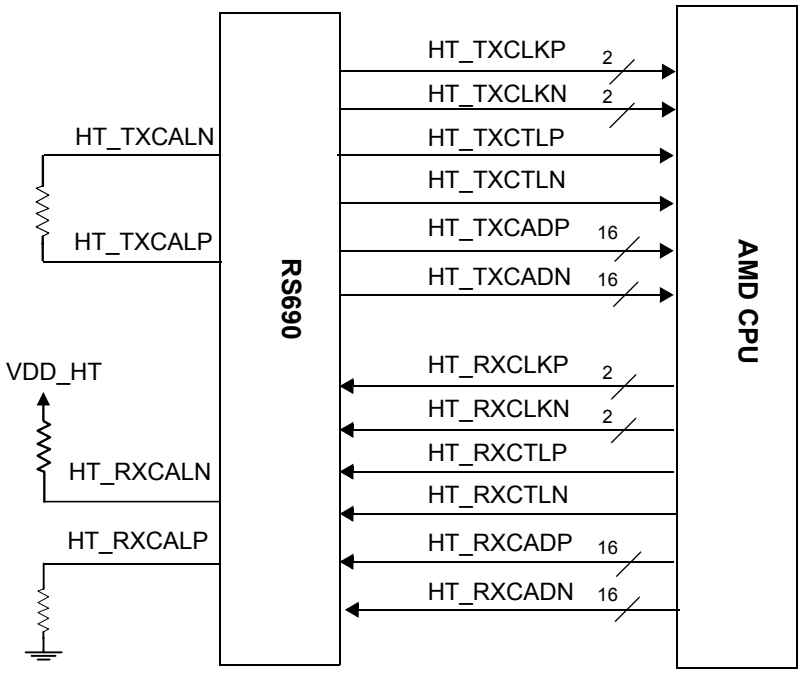


Figure 2-3 RS690 Host Bus Interface Signals

2.2 DVI/HDMI (Not Applicable to the RS690C)

2.2.1 DVI/HDMI Data Transmission Order and Signal Mapping

The RS690 contains an integrated DVI/HDMI interface and a TMDS interface (multiplexed on the PCI-E graphics lanes), both supporting clock frequencies of up to 165 MHz for each signal link. *Figure 2-4* below shows the transmission ordering of the signals on both interfaces in single-link mode.

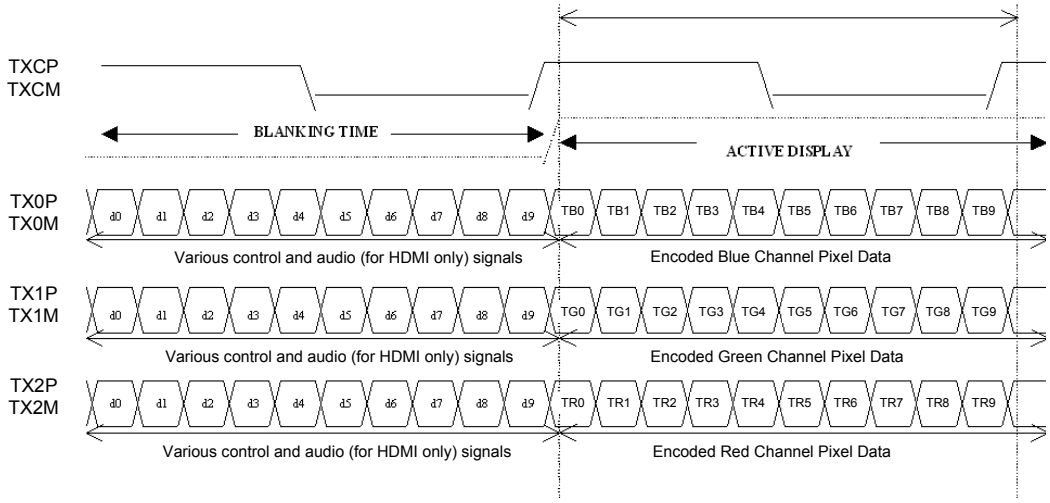


Figure 2-4 Data Transmission Ordering for the Integrated DVI/HDMI and TMDS Interfaces

For dual-link mode, which is for DVI only, the same transmission order applies to data channels on the second link, with the first link transmitting data for even pixels and the second link for odd pixels. See *Table 2-2, "Dual-Link Signal Mapping for DVI," on page 2-6* for details.

The signal mapping for the transmission is shown in *Table 2-1, "Single-Link Signal Mapping for DVI/HDMI," on page 2-5*, and *Table 2-2, "Dual-Link Signal Mapping for DVI," on page 2-6*.

Table 2-1 Single-Link Signal Mapping for DVI/HDMI

DVI/HDMI Functional Name	Data Phase	Signal
TX0M/P	Phase 1	B0
	Phase 2	B1
	Phase 3	B2
	Phase 4	B3
	Phase 5	B4
	Phase 6	B5
	Phase 7	B6
	Phase 8	B7
	Phase 9	B8
	Phase 10	B9
TX1M/P	Phase 1	G0
	Phase 2	G1
	Phase 3	G2
	Phase 4	G3
	Phase 5	G4
	Phase 6	G5
	Phase 7	G6
	Phase 8	G7
	Phase 9	G8
	Phase 10	G9
TX2M/P	Phase 1	R0
	Phase 2	R1
	Phase 3	R2
	Phase 4	R3
	Phase 5	R4
	Phase 6	R5
	Phase 7	R6
	Phase 8	R7
	Phase 9	R8
	Phase 10	R9

Note: H/VSYNC are transmitted on TX0M/P(Blue) channel during blank.

Table 2-2 Dual-Link Signal Mapping for DVI

Link 1			Link 2		
DVI Functional Name	**Data Phase**	**Signal**	**DVI Functional Name**	**Data Phase**	**Signal**
TX0M/P	Phase 1	EVEN_B0	TX3M/P	Phase 1	ODD_B0
	Phase 2	EVEN_B1		Phase 2	ODD_B1
	Phase 3	EVEN_B2		Phase 3	ODD_B2
	Phase 4	EVEN_B3		Phase 4	ODD_B3
	Phase 5	EVEN_B4		Phase 5	ODD_B4
	Phase 6	EVEN_B5		Phase 6	ODD_B5
	Phase 7	EVEN_B6		Phase 7	ODD_B6
	Phase 8	EVEN_B7		Phase 8	ODD_B7
	Phase 9	EVEN_B8		Phase 9	ODD_B8
	Phase 10	EVEN_B9		Phase 10	ODD_B9
TX1M/P	Phase 1	EVEN_G0	TX4M/P	Phase 1	ODD_G0
	Phase 2	EVEN_G1		Phase 2	ODD_G1
	Phase 3	EVEN_G2		Phase 3	ODD_G2
	Phase 4	EVEN_G3		Phase 4	ODD_G3
	Phase 5	EVEN_G4		Phase 5	ODD_G4
	Phase 6	EVEN_G5		Phase 6	ODD_G5
	Phase 7	EVEN_G6		Phase 7	ODD_G6
	Phase 8	EVEN_G7		Phase 8	ODD_G7
	Phase 9	EVEN_G8		Phase 9	ODD_G8
	Phase 10	EVEN_G9		Phase 10	ODD_G9
TX2M/P	Phase 1	EVEN_R0	TX5M/P	Phase 1	ODD_R0
	Phase 2	EVEN_R1		Phase 2	ODD_R1
	Phase 3	EVEN_R2		Phase 3	ODD_R2
	Phase 4	EVEN_R3		Phase 4	ODD_R3
	Phase 5	EVEN_R4		Phase 5	ODD_R4
	Phase 6	EVEN_R5		Phase 6	ODD_R5
	Phase 7	EVEN_R6		Phase 7	ODD_R6
	Phase 8	EVEN_R7		Phase 8	ODD_R7
	Phase 9	EVEN_R8		Phase 9	ODD_R8
	Phase 10	EVEN_R9		Phase 10	ODD_R9

Notes:
- H/VSYNC are transmitted on TX0M/P(Blue) channel during blank.
- For DVI dual-link mode, the first active data pixel is defined as pixel#0 (an even pixel), as opposed to the DVI specifications.

2.2.2 Support for HDMI Packet Types

Table 2-3 Support for HDMI Packet Type

Packet Value	Packet Type	Supported or Not	Source	Comment
0x00	Null	Yes	Inserted by hardware if no packets in horizontal active on line 2 (can be disabled by software).	Sent when required to meet maximum time between data island specification.
0x01	Audio Clock Regeneration	Yes	Inserted by hardware or video driver. Contents from register bits or combination of register bits and hardware control. Inserted in horizontal blank.	—
0x02	Audio Sample	Yes	Audio samples come from HD audio DMA. Channel status from HD audio and video registers. Inserted in horizontal blank whenever audio FIFO contains data.	—
0x03	General Control	No	Sending and contents controlled by video driver. Inserted (on even frames only in interlaced mode) when requested by software or whenever AVMUTE status changes. Inserted in horizontal active on line selected by software.	—
0x04	ACP Packet	Yes*	—	Audio content protection information.
0x05	ISRC1 Packet	Yes	Controlled by video driver. Inserted in horizontal active on line selected by software.	For transmitting UPC or ISRC codes.
0x06	ISRC2 Packet	Yes	Software controlled. Inserted in horizontal active on line selected by software.	Implement if ISRC1 is used.
0x07	Reserved	N/A	N/A	N/A
InfoFrame Packet Type				
HDMI ID	**EIA-861B ID**			
0x80	0x00	Vendor-Specific	Yes*	—	—
0x81	0x01	AVI	Yes	Controlled by video driver. Inserted in horizontal active on line selected by software.	For colorimetry, repetition count, video format, picture formatting.
0x82	0x02	Source Product Descriptor	Yes*	—	—
0x83	0x03	Audio	Yes	Inserted in horizontal active on line selected by software. Contents from registers written by video and HD audio drivers. Sent only when HD audio enables audio (video driver can also disable).	For channel counts, sampling frequency, etc.
0x84	0x04	MPEG Source	Yes	Software controlled. Inserted in horizontal active on line selected by software.	For bit rate, field repeat, frame type

*** Note:** These packet types are supported using generic packet types. A maximum of two of them can be supported simultaneously.

2.3 VGA DAC Characteristics

Table 2-4 VGA DAC Characteristics

Parameter	Min	Typ	Max	Notes
Resolution	10 bits	-	-	1
Maximum PS/2 setting Output Voltage	-	0.7V	-	1, 10
Maximum PS/2 setting Output Current	-	18.7mA	-	1, 10
Full Scale Error	+8% / -3%	-	+10%	2, 3
DAC to DAC Correlation	-2%	-	+2%	1, 4
Differential Linearity	-2 LSB	-	+2 LSB	1, 5
Integral Linearity	-2 LSB	-	+2 LSB	1, 5
Rise Time (10% to 90%)	0.58ns	-	1.7ns	1, 6
Full Scale Settling Time	-	TBA	-	1, 7, 8
Glitch Energy	-	TBA	-	1, 8
Monotonicity	-	-	-	9

Notes:
1 Tested over the operating temperature range at nominal supply voltage, with an Iref of -1.50mA (Iref is the level of the current flowing out of the RSET resistor).
2 Tested over the operating temperature range at reduced supply voltage, with an Iref of -1.50mA (Iref is the level of the current flowing out of the RSET resistor).
3 Full scale error from the value predicted by the design equations.
4 About the mid-point of the distribution of the three DACs measured at full scale deflection.
5 Linearity measured from the best fit line through the DAC characteristics. Monotonicity guaranteed.
6 Load = 37.5Ω + 20pF with Iref = -1.50 mA (Iref is the current flowing out of the RSET resistor).
7 Measured from the end of the overshoot to the point where the amplitude of the video ringing is down to +/-5% of the final steady state value.
8 This parameter is sampled, not 100% tested.
9 Monotonicity is guaranteed.
10 Levels are 7.8% higher with setup pedestal enabled.

2.4 External Clock Chip

On the RS690 platform, an external clock chip provides the reference clock to the CPU (for generating the CPU internal clocks) and a reference clock to the RS690 (for generating the HyperTransport, PCI Express, and A-Link Express II clocks). For more information about supported clock chips, please consult your AMD CSS representative.

Chapter 3
Pin Descriptions and Strap Options

This chapter gives the pin descriptions and the strap options for the RS690. To jump to a topic of interest, use the following list of hyperlinked cross references:

3.1 Pin Assignment

The figures below only represent the relative ball positions. For the actual physical layout of the balls, please refer to *Figure 5-3, "RS690 Ball Arrangement," on page 5- 7*.

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSSA	I2C_CLK	STRP_DATA	VDD_CORE	DACHSYNC	DACSDA	VDD_CORE	DFT_GPIO5	VDD_CORE	PLLVDD18	PLLVDD12	LVDDR18D	TXOUT_L1N
B	VDDA_12	BMREQ#	DDC_DATA	I2C_DATA	ALLOW_LDTSTOP	DACSCL	VSS	DFT_GPIO4	VDD_CORE	PLLVSS	OSCIN	LVDDR18D	TXOUT_L1P
C	VDDA_12	TVCLKIN	TESTMODE	VSS	LDTSTOP#	DACVSYNC	DFT_GPIO3	DFT_GPIO2	VDD_CORE	SYSRESET#	POWERGOOD	LVDDR33	LVDDR33
D	VDDA_12	VDDA_12	VDDA_12	VSS		DFT_GPIO0	DFT_GPIO1		VDD_CORE		VDDR3	LVSSR	
E	GFX_CLKN	VDDA_12	VDDA_12			VDDA_12	VDD_PLL		VSS		VDDR3	GPIO3	
F	VSSA	GFX_CLKP	VSSA	VDDA_12			VDD_PLL		VSS_PLL		VSS	GPIO4	
G	SB_CLKP	SB_CLKN	VSSA	GFX_RX0N	GFX_RX0P	VSSA	VDDA_12		VSS_PLL		VSS	GPIO2	
H	VSSA	GFX_TX0N	VSSA								VDD_CORE	VSS	
J	GFX_TX0P	VSSA	VSSA	GFX_RX2P	GFX_RX2N	VSSA	GFX_RX1N	GFX_RX1P			VDD_CORE	VSS	
K	GFX_TX1N	GFX_TX1P	GFX_TX2P										
L	GFX_TX3P	GFX_TX3N	GFX_TX2N	GFX_RX4P	GFX_RX4N	VSSA	GFX_RX3N	GFX_RX3P	VDDA_12		VDD_CORE	VSS	VDD_CORE
M	VDDA_12_PKG	VSSA	VSSA	GFX_RX6P	GFX_RX6N	VSSA	GFX_RX5N	GFX_RX5P	VDDA_12		VSS	VDD_CORE	VSS
N	GFX_TX4N	GFX_TX4P	VSSA								VDD_CORE	VSS	VDD_CORE
P	GFX_TX5N	GFX_TX5P	GFX_TX6P	GFX_RX8P	GFX_RX8N	VSSA	GFX_RX7N	GFX_RX7P	VSSA		VSS	VDD_CORE	VSS
R	GFX_TX7P	GFX_TX7N	GFX_TX6N	GFX_RX9P	GFX_RX9N	VSSA	GFX_RX10P	GFX_RX10N	VSSA		VDD_CORE	VSS	VDD_CORE
T	VSSA	GFX_TX8P	VSSA										
U	GFX_TX8N	VSSA	VSSA	GFX_RX11P	GFX_RX11N	VSSA	VDDA_12				VDD_CORE	VDD_CORE	
V	GFX_TX9N	GFX_TX9P	GFX_TX10P						GFX_RX14P		VSSA	VSSA	
W	GFX_TX11P	GFX_TX11N	GFX_TX10N	GFX_RX12P	GFX_RX12N	VSSA	VDDA_12		GFX_RX14N		SB_RX2P	SB_RX2N	
Y	VSSA	GFX_TX12P	VSSA	GFX_RX13P	GFX_RX13N		GPP_RX2P		VSSA		VSSA	VSSA	
AA	GFX_TX12N	GFX_TX13P	VSSA				GPP_RX2N		GPP_RX3N		SB_RX3P	SB_RX1N	
AB	GFX_TX14P	GFX_TX13N	VDDA_12	VDDA_12		GFX_RX15N	GFX_RX15P		GPP_RX3P		SB_RX3N	SB_RX1P	
AC	GFX_TX14N	VSSA	VDDA_12	VSSA	VSSA	VSSA	VSSA	SB_TX1P	VSSA	VSSA	VDDA_12_PKG	VDDR	DEBUG2
AD	VSSA	VDDA_12	VSSA	GPP_TX2P	GPP_TX3P	GPP_TX3N	SB_TX3P	SB_TX2P	SB_TX1N	SB_TX0N	PCE_CALRP	VDDR	DEBUG0
AE	VDDA_12	VDDA_12	GFX_TX15P	GFX_TX15N	GPP_TX2N	VSSA	SB_TX3N	SB_TX2N	SB_TX0P	VSSA	PCE_CALRN	VDDR	DEBUG1
	1	2	3	4	5	6	7	8	9	10	11	12	13

CPU Interface
A-Link Express II interface
Clock Interface
CRT and TV Interface
External graphics Interface
Integrated DVI/HDMI Interface
General Purpose External Device Interface
Power Management Interface
Powers
Grounds
Others

Figure 3-1 RS690 Pin Assignment (Left)

14	15	16	17	18	19	20	21	22	23	24	25	
LVSSR	TXOUT_U0P	LVSSR	TXOUT_U2N	TXOUT_U3P	VDD_CORE	AVDDDI	AVDDQ	AVSSQ	VSS	HT_RXCALP	VSS	A
TXOUT_L0P	TXOUT_L0N	TXOUT_U0N	TXOUT_U2P	TXOUT_U3N	VDD_CORE	AVSSDI	RSET	AVDD	HTREFCLK	HTPVDD	HTPVSS	B
TMDS_HPD	LVSSR	LVSSR	TXOUT_U1P	TXOUT_U1N	LVSSR	Y	C	AVDD	HTTSTCLK	HT_RXCALN	HT_TXCALP	C
LPVDD	TXCLK_LN		TXOUT_L3P		COMP	VDD_CORE		VDD_HT_PKG	VSS	HT_TXCALN	VSS	D
LPVSS	TXCLK_LP		TXOUT_L3N		RED				HT_TXCAD1P	HT_TXCAD0P	HT_TXCAD0N	E
LVSSR	LVSSR		VSS		GREEN		HT_TXCAD8P	HT_TXCAD8N	HT_TXCAD1N	HT_TXCAD2N	HT_TXCAD2P	F
TXOUT_L2N	TXCLK_UN		AVSSN		BLUE	VDD_CORE	HT_TXCAD10N	HT_TXCAD10P	VSS	VSS	HT_TXCAD3P	G
TXOUT_L2P	TXCLK_UP		AVSSN						VSS	HT_TXCAD3N	VSS	H
VDD_18	VDD_18				VDD_CORE	HT_TXCAD9P	HT_TXCAD9N	VSS	HT_TXCAD4P	HT_TXCLK0P	HT_TXCLK0N	J
									HT_TXCAD4N	HT_TXCAD5N	HT_TXCAD5P	K
VSS	VDD_CORE		VDD_CORE	HT_TXCAD11P	HT_TXCAD11N	VSS	HT_TXCLK1P	HT_TXCLK1N	VSS	VSS	HT_TXCAD6P	L
VDD_CORE	VSS		VSS	HT_TXCAD12P	HT_TXCAD12N	VSS	HT_TXCAD13N	HT_TXCAD13P	VSS	HT_TXCAD6N	VSS	M
VSS	VDD_CORE								HT_TXCTLP	HT_TXCAD7P	HT_TXCAD7N	N
VDD_CORE	VSS		VDD_CORE	HT_TXCAD14P	HT_TXCAD14N	VSS	HT_TXCAD15P	HT_TXCAD15N	HT_TXCTLN	HT_RXCTLP	HT_RXCTLN	P
VSS	VDD_CORE		VSS	HT_RXCAD15N	HT_RXCAD15P	VSS	HT_RXCAD14P	HT_RXCAD14N	VSS	VSS	HT_RXCAD7N	R
									VSS	HT_RXCAD7P	VSS	T
VDD_CORE	VDD_CORE			HT_RXCAD12P	HT_RXCAD12N	VSS	HT_RXCAD13N	HT_RXCAD13P	HT_RXCAD5N	HT_RXCAD6N	HT_RXCAD6P	U
VSSA	VSSA								HT_RXCAD5P	HT_RXCAD4P	HT_RXCAD4N	V
SB_RX0P	SB_RX0N		VDD_HT		HT_RXCAD11P	HT_RXCAD11N	HT_RXCLK1P	HT_RXCLK1N	VSS	VSS	HT_RXCLK0N	W
VSSA	VSSA		VDD_HT		HT_RXCAD8N			VSS	VSS	HT_RXCLK0P	VSS	Y
NC	THERMALDIODE_P		VDD_HT		HT_RXCAD8P	HT_RXCAD9N			HT_RXCAD2N	HT_RXCAD3N	HT_RXCAD3P	AA
NC	THERMALDIODE_N		VDD_HT		VDD_HT	HT_RXCAD9P		HT_RXCAD10N	HT_RXCAD2P	HT_RXCAD1P	HT_RXCAD1N	AB
VSS	VSS	VSS	DEBUG9	VDD_HT	VDD_HT	VDD_HT	HT_RXCAD10P	VSS	VSS	HT_RXCAD0P	HT_RXCAD0N	AC
GPP_TX0P	GPP_TX0N	GPP_RX0P	DEBUG13	DEBUG10	GPP_TX1P	GPP_RX1P	VDD_HT	VDD_HT	VDD_HT	VDD_HT	VSS	AD
VSS	DEBUG6	GPP_RX0N	DEBUG14	VSS	GPP_TX1N	GPP_RX1N	DEBUG15	VSS	VDD_HT	VDD_HT	VDD_HT	AE
14	15	16	17	18	19	20	21	22	23	24	25	

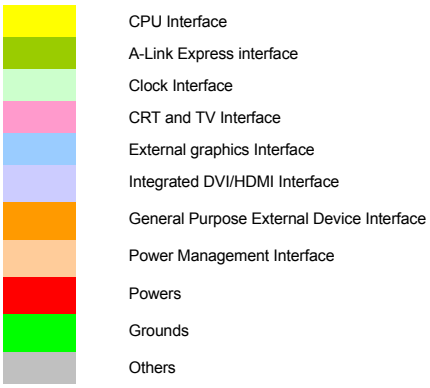


Figure 3-2 RS690 Pin Assignment (Right)

3.2 Interface Block Diagram

The figure below shows the different interfaces on the RS690. Interface names in blue are hyperlinks to the corresponding sections in this chapter.

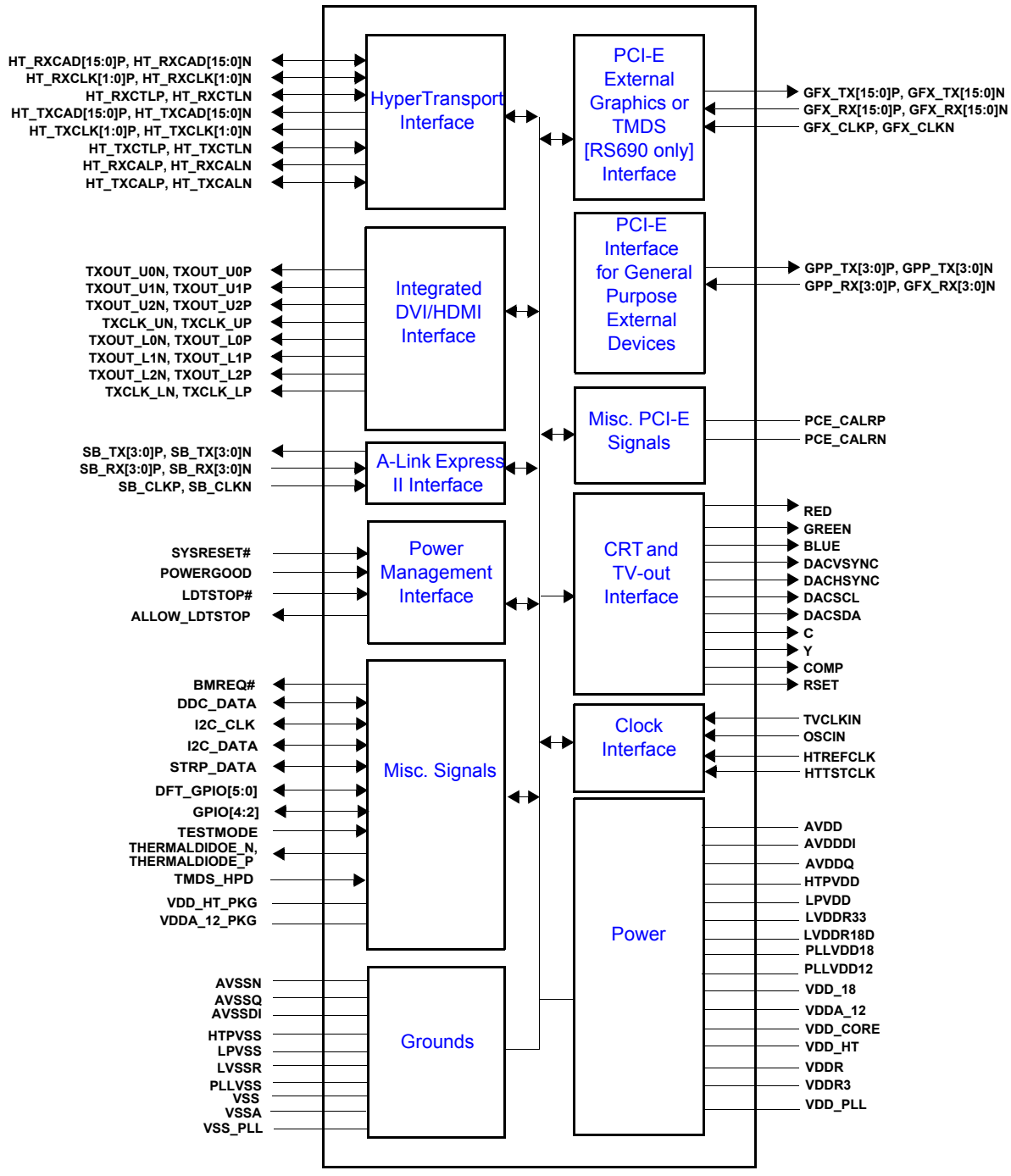


Figure 3-3 RS690 Interface Block Diagram

3.3 CPU HyperTransport Interface

Table 3-1 CPU HyperTransport Interface

Pin Name	Type	Power Domain	Ground Domain	Functional Description
HT_RXCAD[15:0]P, HT_RXCAD[15:0]N	I	VDDHT	VSS	Receiver Command, Address, and Data Differential Pairs
HT_RXCLK[1:0]P, HT_RXCLK[1:0]N	I	VDDHT	VSS	Receiver Clock Signal Differential Pair. Forwarded clock signal. Each byte of RXCAD uses a different clock signal. Data is transferred on each clock edge.
HT_RXCTLP, HT_RXCTLN	I	VDDHT	VSS	Receiver Control Differential Pair. For distinguishing control packets from data packets.
HT_TXCAD[15:0]P, HT_TXCAD[15:0]N	O	VDDHT	VSS	Transmitter Command, Address, and Data Differential Pairs
HT_TXCLK[1:0]P, HT_TXCLK[1:0]N	O	VDDHT	VSS	Transmitter Clock Signal Differential Pair. Each byte of TXCAD uses a different clock signal. Data is transferred on each clock edge.
HT_TXCTLP, HT_TXCTLN	O	VDDHT	VSS	Transmitter Control Differential Pair. Forwarded clock signal. For distinguishing control packets from data packets.
HT_RXCALN	Other	VDDHT	VSS	Receiver Calibration Resistor to VDD_HT power rail.
HT_RXCALP	Other	VDDHT	VSS	Receiver Calibration Resistor to Ground
HT_TXCALP	Other	VDDHT	VSS	Transmitter Calibration Resistor to HTTX_CALN
HT_TXCALN	Other	VDDHT	VSS	Transmitter Calibration Resistor to HTTX_CALP

3.4 PCI Express® Interfaces

3.4.1 1 x 16 Lane Interface for External Graphics

Table 3-2 1 x 16 Lane PCI Express Interface for External Graphics

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
GFX_TX[15:0]P, GFX_TX[15:0]N	O	VDD_PCIE	VSS_PCIE	50Ω between complements	Transmit Data Differential Pairs. Connect to external connector for an external graphics card on the motherboard (if implemented).
GFX_RX[15:0]P, GFX_RX[15:0]N	I	VDD_PCIE	VSS_PCIE	50Ω between complements	Receive Data Differential Pairs. Connect to external connector for an external graphics card on the motherboard (if implemented).
GFX_REFCLKP, GFX_REFCLKN	I	VDD_PCIE	VSS_PCIE	50Ω between complements	Clock Differential Pairs. Connect to external clock generator when an external graphics card is implemented.

3.4.2 A-Link Express II to Southbridge

Table 3-3 1 x 4 Lane A-Link Express II Interface for Southbridge

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
SB_TX[3:0]P, SB_TX[3:0]N	O	VDD_PCIE	VSS_PCIE	50Ω between complements	Transmit Data Differential Pairs. Connect to the corresponding Receive Data Differential pairs on the Southbridge.
SB_RX[3:0]P, SB_RX[3:0]N	I	VDD_PCIE	VSS_PCIE	50Ω between complements	Receive Data Differential Pairs. Connect to the corresponding Transmit Data Differential pairs on the Southbridge.
SB_CLKP, SB_CLKN	I	VDD_PCIE	VSS_PCIE	50Ω between complements	Clock Differential Pair. Connect to an external clock generator on the motherboard.

3.4.3 4 x 1 Lane Interface for General Purpose External Devices

Table 3-4 4 x 1 Lane PCI Express® Interface for General Purpose External Devices

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
GPP_TX[3:0]P, GPP_TX[3:0]N	O	VDD_PCIE	VSS_PCIE	50Ω between complements	Transmit Data Differential Pairs. Connect to external connectors on the motherboard for add-in card or ExpressCard support.
GPP_RX[3:0]P, GPP_RX[3:0]N	I	VDD_PCIE	VSS_PCIE	50Ω between complements	Receive Data Differential Pairs. Connect to external connectors on the motherboard for add-in card or ExpressCard support.

3.4.4 Miscellaneous PCI Express® Signals

Table 3-5 PCI Express® Interface for Miscellaneous PCI Express® Signals

Pin Name	Type	Power Domain	Ground Domain	Functional Description
PCE_CALRN	Other	VDD_PCIE	VSS_PCIE	RX Impedance Calibration. Connect to VDD_PCIE on the motherboard with an external resistor of an appropriate value.
PCE_CALRP	Other	VDD_PCIE	VSS_PCIE	TX Impedance Calibration. Connect to GND on the motherboard with an external resistor of an appropriate value.

3.5 Clock Interface

Table 3-6 Clock Interface

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
TVCLKIN	I	VDDR3	VSS	–	Input pin for reference clock for external TV-out support (3.3V signaling).
HTREFCLK	I	HTPVDD	HTPVSS	-	HyperTransport 66MHz reference clock from external clock source
HTTSTCLK	I	HTPVDD	HTPVSS	-	HyperTransport Bus Test Clock. Drives test clock in test mode. Connect to ground in functional mode.
GFX_REFCLKP, GFX_REFCLKN	I	VDDPCIE	VSSAPCIE	50Ω between complements	Clock Differential Pairs for external graphics. Connect to external clock generator when an external graphics card is implemented.
SB_CLKP, SB_CLKN	I	VDDPCIE	VSSAPCIE	50Ω between complements	Clock Differential Pair for the Southbridge and general purpose PCI Express® (PCI-E) devices. Connect to an external clock generator on the motherboard.
OSCIN	I	VDDR3	VSS	Disabled	14.3181818MHz Reference clock input from the External Clock chip (3.3 volt signaling).

3.6 CRT and TV Interface

Table 3-7 CRT and TV Interface

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
RED	A-O	AVDD	AVSSN	–	Red for CRT monitor output, or Pr for component video TV output
GREEN	A-O	AVDD	AVSSN	–	Green for CRT monitor output, or Y for component video TV output
BLUE	A-O	AVDD	AVSSN	–	Blue for CRT monitor output, or Pb for component video TV output
Y	A-O	AVDD	AVSSN	–	SVID luminance output for TV out, or Y for component video TV output
C	A-O	AVDD	AVSSN	–	SVID chrominance output for TV out, or Pr for component video TV output
COMP	A-O	AVDD	AVSSN	–	Composite video TV output, or Pb for component video TV output

Table 3-7 CRT and TV Interface (Continued)

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
DACHSYNC	A-O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Display Horizontal Sync
DACVSYNC	A-O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Display Vertical Sync
RSET	Other	N/A	AVSSQ	–	DAC internal reference to set full scale DAC current through 1% resistor to AVSS
DACSDA	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	I^2C Data for display (to video monitor)
DACSCL	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	I^2C Clock for display (to video monitor)

3.7 Integrated DVI/HDMI Interface

Note: The RS690C does not contain an integrated DVI/HDMI interface. The following pins should be treated as reserved for the RS690C.

Table 3-8 Integrated DVI/HDMI Interface

Pin Name	DVI/HDMI Functional Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
TXOUT_L0N	TX0M	O	LVDDR33 LVDDR18D	VSSLT	None	DVI/HDMI data channel 0 (-)
TXOUT_L0P	TX0P	O	LVDDR33 LVDDR18D	VSSLT	None	DVI/HDMI data channel 0 (+)
TXOUT_L1N	TX1M	O	LVDDR33 LVDDR18D	VSSLT	None	DVI/HDMI data channel 1 (-)
TXOUT_L1P	TX1P	O	LVDDR33 LVDDR18D	VSSLT	None	DVI/HDMI data channel 1 (+)
TXOUT_L2N	TX2M	O	LVDDR33 LVDDR18D	VSSLT	None	DVI/HDMI data channel 2 (-)
TXOUT_L2P	TX2P	O	LVDDR33 LVDDR18D	VSSLT	None	DVI/HDMI data channel 2 (+)
TXOUT_L3N	TX3M	O	LVDDR33 LVDDR18D	VSSLT	None	DVI data channel 3 (-). The channel is only used in DVI dual-link mode and is not used for HDMI support.
TXOUT_L3P	TX3P	O	LVDDR33 LVDDR18D	VSSLT	None	DVI data channel 3 (+). The channel is only used in DVI dual-link mode and is not used for HDMI support.
TXOUT_U0N	TX4M	O	LVDDR33 LVDDR18D	VSSLT	None	DVI data channel 4 (-). The channel is only used in DVI dual-link mode and is not used for HDMI support.
TXOUT_U0P	TX4P	O	LVDDR33 LVDDR18D	VSSLT	None	DVI data channel 4 (+) The channel is only used in DVI dual-link mode and is not used for HDMI support.
TXOUT_U1N	TX5M	O	LVDDR33 LVDDR18D	VSSLT	None	DVI data channel 5 (-). The channel is only used in DVI dual-link mode and is not used for HDMI support.
TXOUT_U1P	TX5P	O	LVDDR33 LVDDR18D	VSSLT	None	DVI data channel 5 (+). The channel is only used in DVI dual-link mode and is not used for HDMI support.

Table 3-8 Integrated DVI/HDMI Interface (Continued)

Pin Name	DVI/HDMI Functional Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
TXOUT_U2N	–	O	LVDDR33 LVDDR18D	VSSLT	None	Unused
TXOUT_U2P	–	O	LVDDR33 LVDDR18D	VSSLT	None	Unused
TXOUT_U3N	–	O	LVDDR33 LVDDR18D	VSSLT	None	Unused
TXOUT_U3P	–	O	LVDDR33 LVDDR18D	VSSLT	None	Unused
TXCLK_LN	TXCM	O	LVDDR33 LVDDR18D	VSSLT	None	DVI/HDMI clock channel (-)
TXCLK_LP	TXCP	O	LVDDR33 LVDDR18D	VSSLT	None	DVI/HDMI clock channel (+)
TXCLK_UN	–	O	LVDDR33 LVDDR18D	VSSLT	None	Unused
TXCLK_UP	–	O	LVDDR33 LVDDR18D	VSSLT	None	Unused

3.8 TMDS Interface Multiplexed on the PCI Express® Graphics Lanes (Not Applicable to the RS690C)

The RS690 supports a dual-link TMDS interface, enabling DVI/HDMI, which is multiplexed on the PCI-E external graphics lanes. The TMDS interface is available only if no external graphics card, or only a x8 one, is attached to the PCI-E graphics interface.

HDMI is enabled only through the single-link mode. The interface cannot enable HDMI when the integrated DVI/HDMI interface is supporting HDMI, and vice versa. *Table 3-9, "TMDS Interface Multiplexed on the PCI Express® Graphics Interface,"* shows the multiplexing relationships between the PCI-E external graphics signals and the TMDS signals.

Table 3-9 TMDS Interface Multiplexed on the PCI Express® Graphics Interface

Pin Name	Ball Reference	TMDS Function
GFX_TX0P	J1	TX2P - 1st Link Red+
GFX_TX0N	H2	TX2M - 1st Link Red-
GFX_TX1P	K2	TX1P - 1st Link Green+
GFX_TX1N	K1	TX1M - 1st Link Green-
GFX_TX2P	K3	TX0P - 1st Link Blue+
GFX_TX2N	L3	TX0M- 1st Link Blue -
GFX_TX3P	L1	TXCP - Clock+
GFX_TX3N	L2	TXCM - Clock-
GFX_TX4P	N2	TX5P- 2nd Link Red+
GFX_TX4N	N1	TX5M - 2nd Link Red-
GFX_TX5P	P2	TX4P- 2nd Link Green+
GFX_TX5N	P1	TX4M - 2nd Link Green-
GFX_TX6P	P3	TX3P - 2nd Link Blue+
GFX_TX6N	R3	TX3M - 2nd Link Blue-

3.9 Power Management Pins

Table 3-10 Power Management Pins

Pin Name	Type	Power Domain	Ground Domain	Functional Description
LDTSTOP#	I	VDDR3	VSS	HyperTransport Stop. Input from the Southbridge to enable and disable the HyperTransport link during system state transitions. For systems requiring power management. Single-ended.
ALLOW_LDTSTOP	OD	VDDR3	VSS	Output going to the Southbridge to allow LDTSTOP assertions: 1 = LDTSTOP# can be asserted 0 = LDTSTOP# has to be de-asserted
SYSRESET#	I	VDDR3	VSS	Global Hardware Reset. This signal comes from the Southbridge.
POWERGOOD	I	VDDR3	VSS	Input from the motherboard signifying that the power to the RS690 is up and ready. Signal high means all power planes are valid. It is not observed internally until it has been high for more than 6 consecutive REFCLK cycles. The rising edge of this signal is deglitched. The nominal input high voltage is 3.3V.

3.10 Miscellaneous Pins

Table 3-11 Miscellaneous Pins

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
BMREQ#	O	VDDR3	VSS	–	This output signal to the Southbridge indicates that there is a DMA request from a PCI Express Bus device. The signal is not used on the RS690 platforms and should be left unconnected.
DEBUG[15:13, 10:9, 6, 2:0]	I/O	VDDR	VSS	–	Debug port signals. See *section 3.13, "Debug Port Signals," on page 3- 11* for details.
DFT_GPIO[5:0]	I/O	VDD_18	VSS	–	GPIO for DFT purpose.
GPIO[4:2]	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	General Purpose I/O. These pins can also be used as outputs to the voltage regulator for pulse-width modulation of various voltages on the motherboard. If not used for pulse-width-modulation, GPIO3 can also be used as a "hot plug" panel detection input pin that monitors if the voltage is greater than 2.0V on the hot-plugging line from a digital display.
I2C_CLK	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	I^2C interface clock signal. Can also be used simultaneously as DDC interface clock . It can also be used as GPIO.
I2C_DATA	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	I^2C interface data signal. It can also be used as GPIO.
DDC_DATA	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Pin for additional DDC data channel for displays. It makes use of I2C_CLK to create an I^2C interface. Can also be used as GPIO.
NC	–	–	–	–	No connect. These pins should be left unconnected to anything.
STRP_DATA	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	I2C interface data signal for external EEPROM based strap loading. Can also be used as GPIO, or as output to the voltage regulator for pulse-width modulation of RS690's core voltage.
TESTMODE	I	VDDR3	VSS	–	When high, puts the RS690 in test mode and disables the RS690 from operating normally.
THERMALDIODE_P, THERMALDIODE_N	A-O	–	–	–	Diode connections to external SMBus microcontroller for monitoring IC thermal characteristics.
TMDS_HPD	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	TMDS Hot Plug Detect. It monitors the hot-plug line for panel detection. It is a 3.3V CMOS compatible input. When not used for hot plug detection, it can also be used as output to the voltage regulator for pulse-width modulation of various voltages on the motherboard.

Table 3-11 Miscellaneous Pins (Continued)

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
VDD_HT_PKG	Other	VDD_HT	VSS	–	The pin is for connecting a calibration resistor to the VDD_HT power plane. The VDD_HT_PKG pin is connected to the VDD_HT power pins via package routing, so that a calibration resistor for the VDD_HT power plane can be connected to the RS690 through the VDD_HT_PKG pin, and the VDD_HT power plane does not have to be extended physically for the purpose.
VDDA_12_PKG	Other	VDDA_12	VSS	–	The pins are for connecting calibration resistors to the VDDA_12 power plane. VDDA_12_PKG pins are connected to the VDDA_12 power pins via package routing, so that the calibration resistors for the VDDA_12 power plane can be connected to the RS690 through the VDDA_12_PKG pins, and the VDDA_12 power plane does not have to be extended physically for the purpose.

3.11 Power Pins

Table 3-12 Power Pins

Pin Name	Voltage	Pin Count	Ball Reference	Comments
AVDD	2.5V or 3.3V	2	B22, C22	Dedicated power for the DAC. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection, which can affect display quality. Adequate decoupling should be provided between this pin and AVSS.
AVDDQ	1.8V	1	A21	DAC Bandgap Reference Voltage
AVDDDI	1.8V	1	A20	Dedicated digital power for the DAC
VDD_CORE	1.2V	32	A19, A4, A7, A9, B19, B9, C9, D20, D9, G20, H11, J11, J19, L11, L13, L15, L17, M12, M14, N11, N13, N15, P12, P14, P17, R11, R13, R15, U11, U12, U14, U15	Core power
VDD_18	1.8V	2	J14, J15	Core transform power for GPIOs and power for DFT_GPIOs
VDDA_12	1.2 V	20	AB3, AB4, AC3, AD2, AE1, AE2, B1, C1, D1, D2, D3, E2, E3, E6, F4, G7, L9, M9, U7, W7	PCI-E interface main I/O power
VDDR	1.8	3	AC12, AD12, AE12	IO power for debug interface (1.8V)
VDD_HT	1.2V	15	AA17, AB17, AB19, AC18, AC19, AC20, AD21, AD22, AD23, AD24, AE23, AE24, AE25, W17, Y17	I/O power for HyperTransport interface
VDDR3	3.3V	2	D11, E11	I/O power for the following I/O pads: POWERGOOD, SYSRESET#
VDD_PLL	1.2V	2	E7, F7	PCI-E interface PLL power
LPVDD	1.8V	1	D14	Power for integrated DVI/HDMI PLL macro.
LVDDR18D	1.8V	2	A12, B12	1.8V integrated DVI/HDMI Digital Power
LVDDR33	3.3V	2	C12, C13	3.3V integrated DVI/HDMI Analog Power
PLLVDD18	1.8V	1	A10	1.8V power for system PLLs
PLLVDD12	1.2V	1	A11	1.2V power for system PLLs
HTPVDD	1.8V	1	B24	Power for HyperTransport interface PLL
Total Power Pin Count		88		

3.12 Ground Pins

Table 3-13 Ground Pins

Pin Name	Pin Count	Ball Reference	Comments
AVSSN	2	G17, H17	Dedicated analog ground for the DAC
AVSSQ	1	A22	Dedicated ground for the Band Gap Reference. Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection, which can affect display quality. Adequate decoupling should be provided between this pin and AVDD.
AVSSDI	1	B20	Dedicated digital ground for the DAC (1.8V)
LPVSS	1	E14	PLL macro ground pin
LVSSR	8	A14, A16, C15, C16, C19, D12, F14, F15	ground pin
VSS	59	A23, A25, AC14, AC15, AC16, AC22, AC23, AD25, AE14, AE18, AE22, B7, C4, D23, D25, D4, E9, F11, F17, G11, G23, G24, H12, H23, H25, J12, J22, L12, L14, L20, L23, L24, M11, M13, M15, M17, M20, M23, M25, N12, N14, P11, P13, P15, P20, R12, R14, R17, R20, R23, R24, T23, T25, U20, W23, W24, Y22, Y23, Y25	Common ground
VSSA	48	A1, AA3, AC10, AC2, AC4, AC5, AC6, AC7, AC9, AD1, AD3, AE10, AE6, F1, F3, G3, G6, H1, H3, J2, J3, J6, L6, M2, M3, M6, N3, P6, P9, R6, R9, T1, T3, U2, U3, U6, V11, V12, V14, V15, W6, Y1, Y11, Y12, Y14, Y15, Y3, Y9	PCI Express interface ground
VSS_PLL	2	F9. G9	Ground pin for PCI-E interface PLL
PLLVSS	1	B10	Ground pin for graphics core PLL
HTPVSS	1	B25	Ground pin for HyperTransport interface PLL
Total Ground Pin Count	124		

3.13 Debug Port Signals

In order to fully support debugging of customer platforms, it is **mandatory** that customer designs allow access to the signals listed in *Table 3-14, "RS690 Debug Port Signals"* below. Signals in the table should be brought out to test points on the motherboard.

Table 3-14 RS690 Debug Port Signals

Pin Name	Ball Ref	Debug Port Name
DEBUG0	AD13	Debug0
DEBUG1	AE13	Debug1
DEBUG2	AC13	Debug2
DEBUG6	AE15	Debug6
DEBUG9	AC17	Debug9
DEBUG10	AD18	Debug10
DEBUG13	AD17	Debug13
DEBUG14	AE17	Debug14

Table 3-14 RS690 Debug Port Signals

Pin Name	Ball Ref	Debug Port Name
DEBUG15	AE21	Debug15
DFT_GPIO2	C8	Debug [programmable*]
DFT_GPIO3	C7	Debug [programmable*]
DFT_GPIO4	B8	Debug [programmable*]
DFT_GPIO5	A8	Debug [programmable*]

***Note:** The port is programmable into any of Debug0 to Debug15.

3.14 Strapping Options

The RS690 provides strapping options to define specific operating parameters. The strap values are latched into internal registers after the assertion of the POWERGOOD signal to the RS690. *Table 3-15, "Strap Definitions for the RS690,"* shows the definitions of all the strap functions. These straps are set by one of the following four methods:

- Allowing the internal pull-up resistors to set all strap values to "1" automatically.
- Attaching pull-down resistors to specific strap pins listed in *Table 3-15* to set their values to "0".
- Downloading the strap values from an I^2C serial EEPROM (for debug purpose only; contact your AMD CSS representative for details).
- Setting through an external debug port, if implemented (contact your AMD CSS representative for details).

All of the straps below are defined active low. They are pulled up internally by default, so that no external pull-ups are required to select "1"s for those straps. To select "0"s, the strap pins must be pulled down to VSS through resistors. During reset, the strap pins are undriven, allowing either an internal pull-up to pull a pin to "1" or an external pull-down to pull a pin to "0." The values on the strap pins are then latched into the device and used as operational parameters. However, for debug purposes, those latched values may be overridden through an external debug strap port or by a bit-stream downloaded from a serial EEPROM.

Table 3-15 Strap Definitions for the RS690

Strap Function	Strap Pin	Description
RESERVED	DFT_GPIO5	This is a reserved strap and no strap resistor should be connected to it.
GPPSB_LINK_CONFIG	DFT_GPIO[4:2]	Southbridge and General Purpose Link Configuration. See *Table 3-16* below for details.
LOAD_ROM_STRAPS#	DFT_GPIO1	Selects loading of strap values from EEPROM 0: I^2C master can load strap values from EEPROM if connected, or use default values if not connected **1: Use default values (Default)**
RESERVED	DFT_GPIO0	This is a reserved strap and no strap resistor should be connected to it.

Table 3-16 Strap Definition for GPPSB_LINK_CONFIG

Strap Pin Value			Link Width					Configuration
DFT_GPIO4	DFT_GPIO3	DFT_GPIO2	SB	GPP1	GPP2	GPP3	GPP4	
1	**1**	**1**	**Use register field STRAP_BIF_LINK_CONFIG_GPPSB of register StrapsOutputMux_7 (NBMISCIND: 0x67 bit[7:4]) to define link configuration (Default).**					-
1	1	0	4	0	0	0	0	A
1	0	1	4	4	0	0	0	B
1	0	0	4	2	2	0	0	C
0	1	1	4	2	1	1	0	D
0	1	0	4	1	1	1	1	E
Others			**Use register field STRAP_BIF_LINK_CONFIG_GPPSB of register StrapsOutputMux_7 (NBMISCIND: 0x67 bit[7:4]) to define link configuration.**					-

Note: The three strap pins are internally pulled up so that if left unconnected on the motherboard, the RS690 will use register field **STRAP_BIF_LINK_CONFIG_GPPSB of register StrapsOutputMux_7 (NBMISCIND: 0x67 bit[7:4])** to define the link configuration. The power on default value of this register corresponds to Configuration E. If the pin straps are used, the GPPSB configuration will then be determined according to this table and cannot be changed after the system has been powered up.

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Chapter 4
Timing Specifications

4.1 CPU HyperTransport Bus Timing

For HyperTransport bus timing information, please refer to CPU specifications.

4.2 HyperTransport Reference Clock Timing Parameters

Table 4-1 HTREFCLK Pad (66.66MHz) Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Comment
TIP	REFCLK Period	–	15	–	ns	Time intervals measured at 50% VDDCK threshold point
FIP	REFCLK Frequency	–	66.66	–	MHz	FIP is the reciprocal of TIP.
TIH	REFCLK High Time	2	–	–	ns	–
TIL	REFCLK Low Time	2	–	–	ns	–
TIR	REFCLK Rise Time	–	–	1.5	ns	–
TIF	REFCLK Fall Time	–	–	1.5	ns	–
TIJCC	REFCLK Cycle-to-Cycle Jitter Requirement	–	–	300	ps	–
TIJLT	REFCLK Long Term Jitter Requirement (1µs after scope trigger)	–	–	1	ns	–

4.3 PCI Express® Differential Clock AC Specifications

Table 4-2 PCI Express® Differential Clock (GFX_CLK, SB_CLK) AC Characteristics

Parameter	Minimum	Maximum	Unit
Absolute Minimum Differential Clock Period	9.872	–	ns
Rise Time	175	700	ps
Fall time	175	700	ps
Rise/Fall Matching	–	20	%
Cycle-to-Cycle Jitter	–	125	ps
Duty Cycle	45	55	%

4.4 OSCIN Timing

Table 4-3 Timing Requirements for the OSCIN Pad

Symbol	Parameter	Min	Typical	Max	Unit	Note
TIP	REFCLK Period	0.037	–	1.1	µs	1
FIP	REFCLK Frequency	0.9	–	27	MHz	2
TIR	REFCLK Rise Time	–	–	1.5	ns	
TIF	REFCLK Fall Time	–	–	1.5	ns	

Table 4-3 Timing Requirements for the OSCIN Pad (Continued)

Symbol	Parameter	Min	Typical	Max	Unit	Note
TIJCC	REFCLK Cycle-to-Cycle Jitter Requirement	–	–	300	ps	
FRQD	Frequency Tolerance	–	30	–	ppm	3

Notes:
1 Time intervals measured at 50% threshold point.
2 FIP is the reciprocal of TIP.
3 FRQD is the tolerance of the frequency input for proper generation of the expected PLL frequencies.

4.5 Power Rail Power Up Sequence

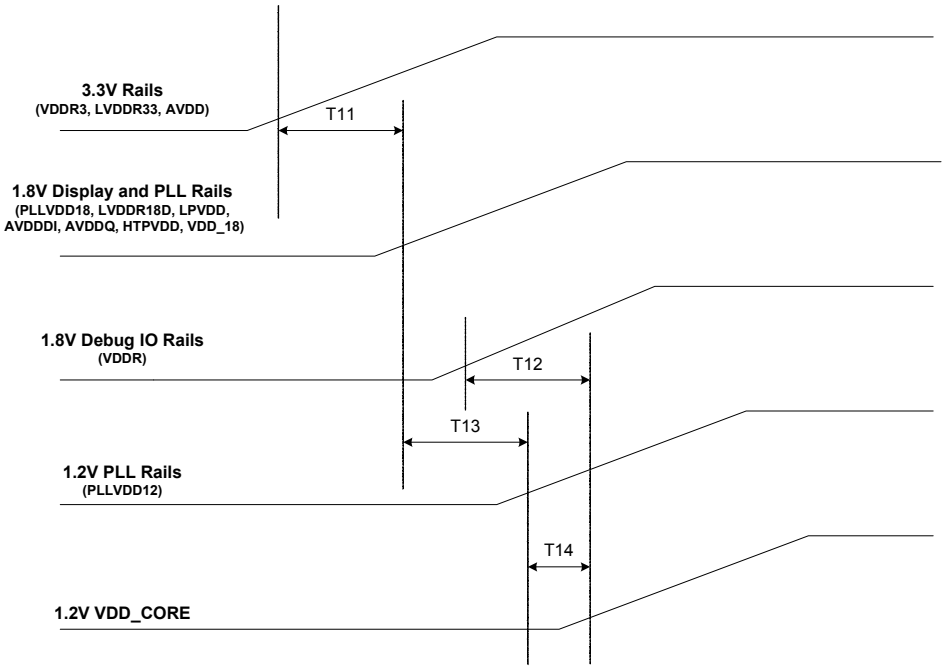

Figure 4-1 Power Rail Power Up Sequence for the RS690

Table 4-4 RS690 Power Rail Power Up Sequence Requirements

Symbol	Parameter	Voltage Difference During Ramping	
		Minimum (V)	Maximum (V)
T11	3.3V rails ramp high relative to 1.8V display and PLL rails	0	2.1
T12	1.8V debug IO rail ramps high relative to VDD_CORE (1.2V)	0	No restrictions
T13	1.8V display and PLL rails ramp high relative to 1.2V PLL rails	0	No restrictions
T14	1.2V PLL rails ramp high relative to VDD_CORE (1.2V)	0	No restrictions

Notes:
1. Power rails in the same group may require separate power sources. Please refer to the *RS690/RS485-series IGP Motherboard Design Guide* for details.
2. There are no specific requirements for the following 1.2V rails: VDD_HT, VDDA_12, and VDD_PLL.
3. For power down, the rails should either be turned off simultaneously or in the reversed order of the above power up sequence. Variations in speeds of decay due to different capacitor discharge rates can be safely ignored.

Figure 4-1 above only shows the power up sequence for the power rails that the RS690 connects to. For a power up sequence for the whole RS690 platform, please refer to the *RS690/RS485-Series IGP Motherboard Design Guide*.

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Chapter 5
Electrical Characteristics and Physical Data

5.1 Electrical Characteristics

5.1.1 Maximum and Minimum Ratings

Table 5-1 Maximum and Minimum Ratings

Pin	Minimum	Typical	Maximum	Unit	Comments
VDD_CORE		1.2	1.26	V	ASIC core power
VDD_18	1.71	1.8	1.89	V	Core transform power for GPIOs and power for DFT_GPIOs
VDD_HT	1.14	1.2	1.26	V	I/O power for HyperTransport™ interface
VDDR3	3.135	3.3	3.465	V	3.3 Volt I/O power
VDDA_12	1.14	1.2	1.26	V	PCI Express Interface main I/O power
AVDDDI	1.71	1.8	1.89	V	Digital power for DAC
AVDDQ	1.71	1.8	1.89	V	Band gap reference voltage for DAC
AVDD	3.135	3.3	3.465	V	I/O power for DAC
LPVDD	1.71	1.8	1.89	V	Power forintegrated DVI/HDMI PLL macro
LVDDR18D	1.71	1.8	1.89	V	1.8V power
LVDDR33	3.135	3.3	3.465	V	3.3V power
PLVDD12	1.14	1.2	1.26	V	1.2V power for system PLLs
PLVDD18	1.71	1.8	1.89	V	1.8V power for system PLLs
HTPVDD	1.71	1.8	1.89	V	Power for HyperTransport interface PLL

Note: Numbers in this table are to be qualified.

5.1.2 DC Characteristics

Table 5-2 DC Characteristics for 3.3V TTL Signals

Pins	Symbol	Description	Minimum	Maximum	Unit
ALLOW_LDTSTOP† BMREQ#† DACVSYNC DACSCL*†, DACSDA DACHSYNC† DDC_DATA GPIO[4:2] LDTSTOP#‡ OSCIN‡ I2C_DATA, I2C_CLK* POWERGOOD‡ STRP_DATA SYSRESET#‡ TESTMODE‡ TMDS_HPD‡ SUS_STAT#‡	VILdc	DC voltage at PAD pin that will produce a stable low at the Y pin of macro	–	0.6	V
	VIHdc	DC voltage at PAD pin that will produce a stable high at the Y pin of macro	1.4	–	V
	VOL	Output low voltage	–	0.35	V
	VOH	Output high voltage	2.6	–	V
	IOL	Output low current at V=0.1V	2.3*	–	mA
	IOH	Output high current at V=VDDR-0.1V	2.2*	–	mA

Notes:
‡ Input pins. Output parameters in the table do not apply.
† Output pins. Input parameters in the table do not apply.
* DACSCL and I2C_CLK have different values for IOL and IOH:
DACSCL: IOL=14mA, IOH=5.8mA
I2C_CLK: IOL=9.5mA, IOH=3.2mA
Other numbers in this tables are applicable to the two signals.

Table 5-3 DC Characteristics for 1.8V TTL Signals

Pins	Symbol	Description	Minimum	Maximum	Unit
DFT_GPIO[5:0]†	VILdc	DC voltage at PAD pin that will produce a stable low at the Y pin of macro	–	0.69*	V
	VIHdc	DC voltage at PAD pin that will produce a stable high at the Y pin of macro	0.81*	–	V
	VOL	Output low voltage	–	0.59	V
	VOH	Output high voltage	1.16	–	V
	IOL	Output low current at V=0.1V	1.52	–	mA
	IOH	Output high current at V=VDDR-0.1V	1.79	–	mA

* **Note:** Measured with edge rate of 1μs at PAD pin.

Table 5-4 DC Characteristics for the HTREFCLK Pad (66.66MHz)

Symbol	Description	Minimum	Typical	Maximum	Comments
VIL	Input Low Voltage	–	0V	0.2V	–
VIH	Input High Voltage	1.4V	1.8V	–	–
VIMAX	Maximum Input Voltage	–	–	2.1V	–

Table 5-5 DC Characteristics for the OSCIN Pad (14.3181818MHz)

Symbol	Description	Minimum	Typical	Maximum	Comments
VIL	Input Low Voltage	–	0V	0.6V	–
VIH	Input High Voltage	2.5V	2.6V	–	–
VIMAX	Maximum Input Voltage	–	–	3.3V	–

Table 5-6 DC Characteristics for the Integrated DVI/HDMI (Not Applicable to the RS690C)

Symbol	Parameter	Min	Typical	Max	Unit	Note
VCM	Common-mode Voltage on Signal Pair	-0.5	–	4.0	V	
VH	Single-ended High Level Output Voltage	AVCC - 10	–	AVCC + 10	mV	1
VL	Single-ended Low Level Output Voltage	AVCC - 600	–	AVCC - 400	mV	1
VSW	Single-ended Output Swing	400	–	600	mV	
VOS	Differential Output Overshoot (Ringing)	–	–	15%*2VSW	–	
VUS	Differential Output Undershoot (Ringing)	–	–	25%*2VSW	–	
IDDLP	Average Supply Current at LPVDD	–	20.0	–	mA	2
IDDLV	Average Supply Current at LVDDR18 and LVDDR33	–	100.0	–	mA	2
IPDLP	Power Down Current at LPVDD	–	10.0	–	μA	3
IPDLV	Power Down Current at LVDDR18 and LVDDR33	–	10.0	–	μA	3

Notes:
1 AVCC stands for the termination supply voltage of the receiver, which is 3.3V +/- 5%.
2 Measured under typical conditions, at minimum differential clock frequency and maximum DVI/HDMI PLL VOC frequency.
3 Measured under typical conditions, based on typical leakage values.
4 Figure 5-1 below illustrates some of the DC Characteristics of the DVI/HDMI interface.

Table 5-7 DC Characteristics for the TMDS Interface Multiplexed on the PCI Express® Gfx Lanes

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Note
VCM	Common-mode Voltage on Signal Pair	-0.5	–	4.0	V	
VH	Single-ended High Level Output Voltage	AVCC - 10	–	AVCC + 10	mV	1
VL	Single-ended Low Level Output Voltage	AVCC - 600	–	AVCC - 400	mV	1
VSW	Single-ended Output Swing	400	–	600	mV	
VOS	Differential Output Overshoot (Ringing)	–	–	15%*2VSW	–	
VUS	Differential Output Undershoot (Ringing)	–	–	25%*2VSW	–	

Notes:
1 AVCC stands for the termination supply voltage of the receiver, which is 3.3V +/- 5%.
2 Figure 5-1 below illustrates some of the DC characteristics of the TMDS interface.

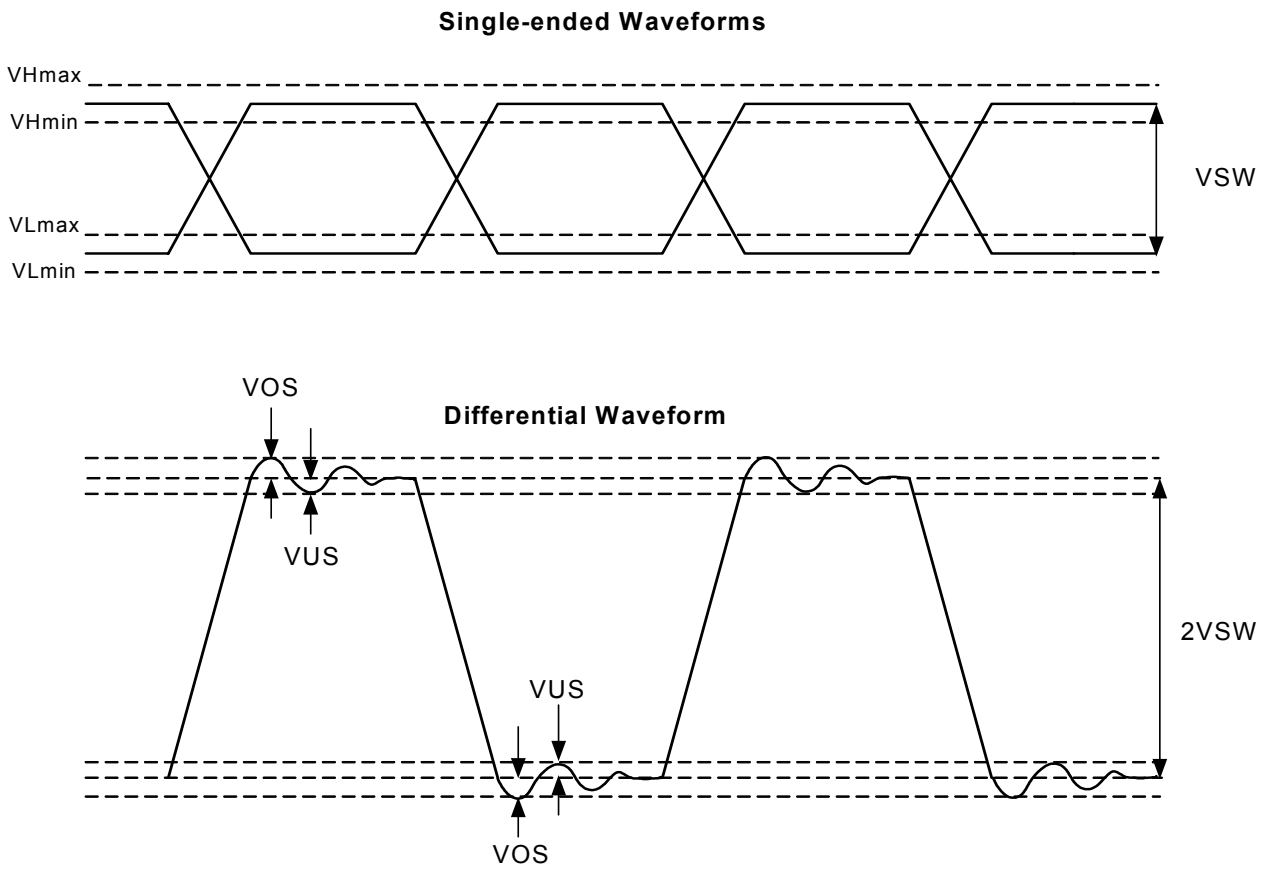

Figure 5-1 DC Characteristics of the Integrated DVI/HDMI and the TMDS Interface

5.2 RS690 Thermal Characteristics

This section describes some key thermal parameters of the RS690. For a detailed discussion on these parameters and other thermal design descriptions including package level thermal data and analysis, please consult the *Thermal Design and Analysis Guidelines for the RS690 Product Family*.

5.2.1 RS690 Thermal Limits

Table 5-8 RS690 Thermal Limits

Parameter	Minimum	Nominal	Maximum	Unit	Note
Operating Case Temperature	0	—	95	°C	1
Absolute Rated Junction Temperature	—	—	125	°C	2
Storage Temperature	-40	—	60	°C	

Table 5-8 RS690 Thermal Limits (Continued)

Parameter	Minimum	Nominal	Maximum	Unit	Note
Ambient Temperature	0	—	45	°C	4
Thermal Design Power	—	8	—	W	5

Notes:
1 - The maximum operating case temperature is the die top-center temperature measured via a thermocouple based on the methodology given in the document *Thermal Design and Analysis Guidelines for the RS690 Product Family* (Chapter 10). This is the temperature at which the functionality of the chip is qualified.
2 - The maximum absolute rated junction temperature is the junction temperature at which the device can operate without causing damage to the ASIC.
3 - The ambient temperature is defined as the temperature of the local intake air at the inlet to the thermal management device. The maximum ambient temperature is dependent on the heat sink design, and the value given here is based on AMD's own heat sink solution for the RS690. Refer to Chapter 7 in *Thermal Design and Analysis Guidelines for the RS690 Product Family* for heatsink and thermal design guidelines. Refer to Chapter 5 for details of ambient conditions.
4 The Thermal Design Power (TDP) is defined as the worst-case power dissipation while running currently available applications at nominal voltages and at the maximum operating temperature. The TDP is intended only as a design reference. It is not an absolute maximum power under all conditions. The value shown here is a preliminary estimate only.

5.2.2 Thermal Diode Characteristics

The RS690 has an on-die thermal diode, with its positive and negative terminals connected to the THERMALDIODE_P and THERMALDIODE_N pins respectively. Combined with a thermal sensor circuit, the diode temperature, and hence the ASIC temperature, can be derived from a differential voltage reading (ΔV). The equation relating T to ΔV is given below:

$$\Delta V = \frac{\eta \times K \times T \times \ln(N)}{q}$$

where:

ΔV = Difference of two base-to-emitter voltage readings, one using current = I and the other using current = N x I

N = Ratio of the two thermal diode currents (=10 when using an ADI thermal sensor, e.g. ADM 1020, 1030)

η = Ideality factor of the diode

K = Boltzman's Constant

T = Temperature in Kelvin

q = Electron charge

The series resistance of the thermal diode (R_T) must be taken into account as it introduces an error in the reading (for every 1.0 W, approximately 0.8°C is added to the reading). The sensor circuit should be calibrated to offset the R_T induced, plus any other known fixed error. Measured values of diode ideality factor and series resistance for the diode circuit are defined in the *Thermal Design and Analysis Guidelines for the RS690 Product Family*.

5.3 Package Information

5.3.1 Physical Dimensions

Figure 5-2 and *Table 5-9* describe the physical dimensions of the RS690 package. *Figure 5-3* shows the detailed ball arrangement for the RS690.

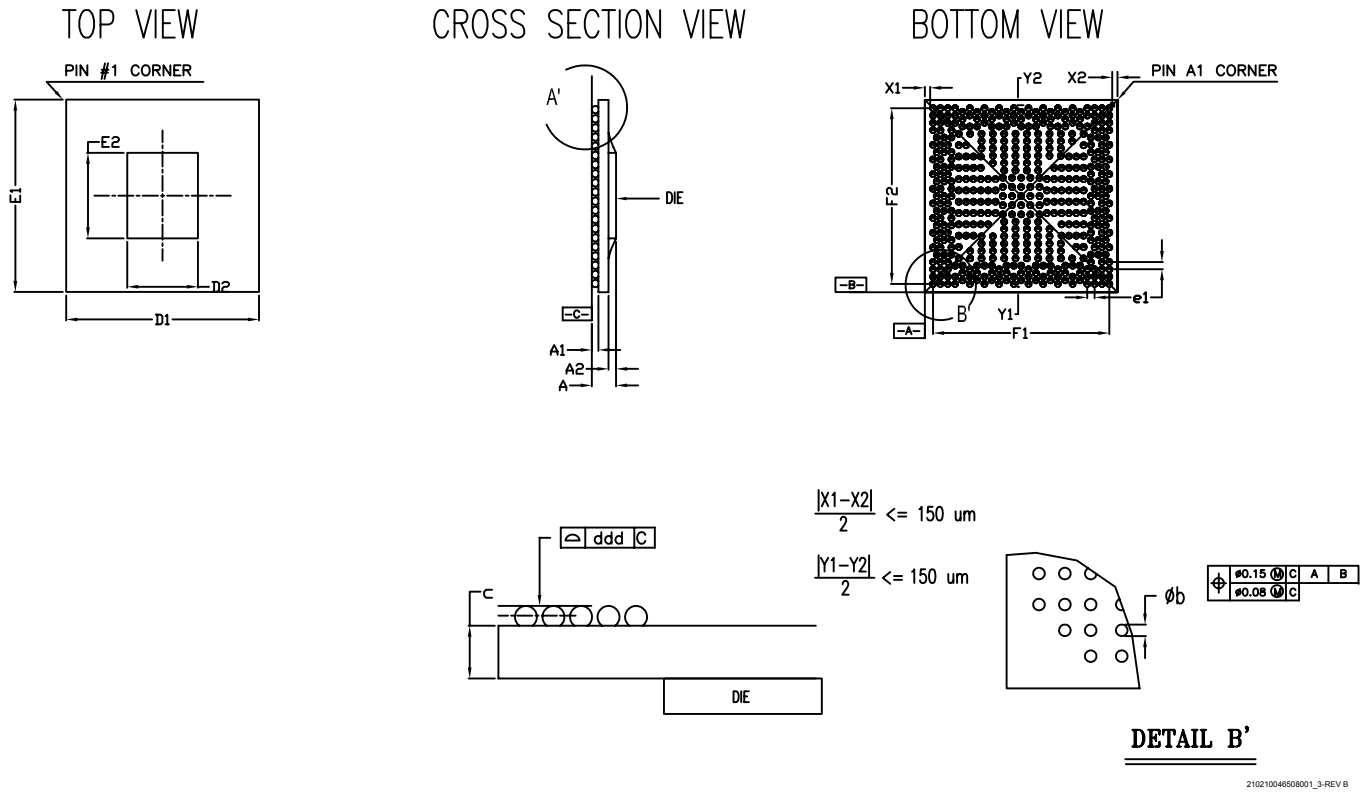

Figure 5-2 RS690 Package Outline

Table 5-9 RS690 465-Pin FCBGA Package Physical Dimensions

Ref.	Minimum(mm)	Typical(mm)	Maximum(mm)
c	0.96	1.06	1.16
A	2.18	2.33	2.48
A1	0.30	0.40	0.50
A2	0.84	0.87	0.90
ϕb	0.40	0.50	0.60
D1	20.80	21.00	21.20
D2	-	7.33	-
E1	20.80	21.00	21.20
E2	-	6.93	-
F1	-	19.20	-
F2	-	19.20	-
e1	-	0.80*	-
ddd	-	-	0.15

*** Note**: Only minimum pitch shown.

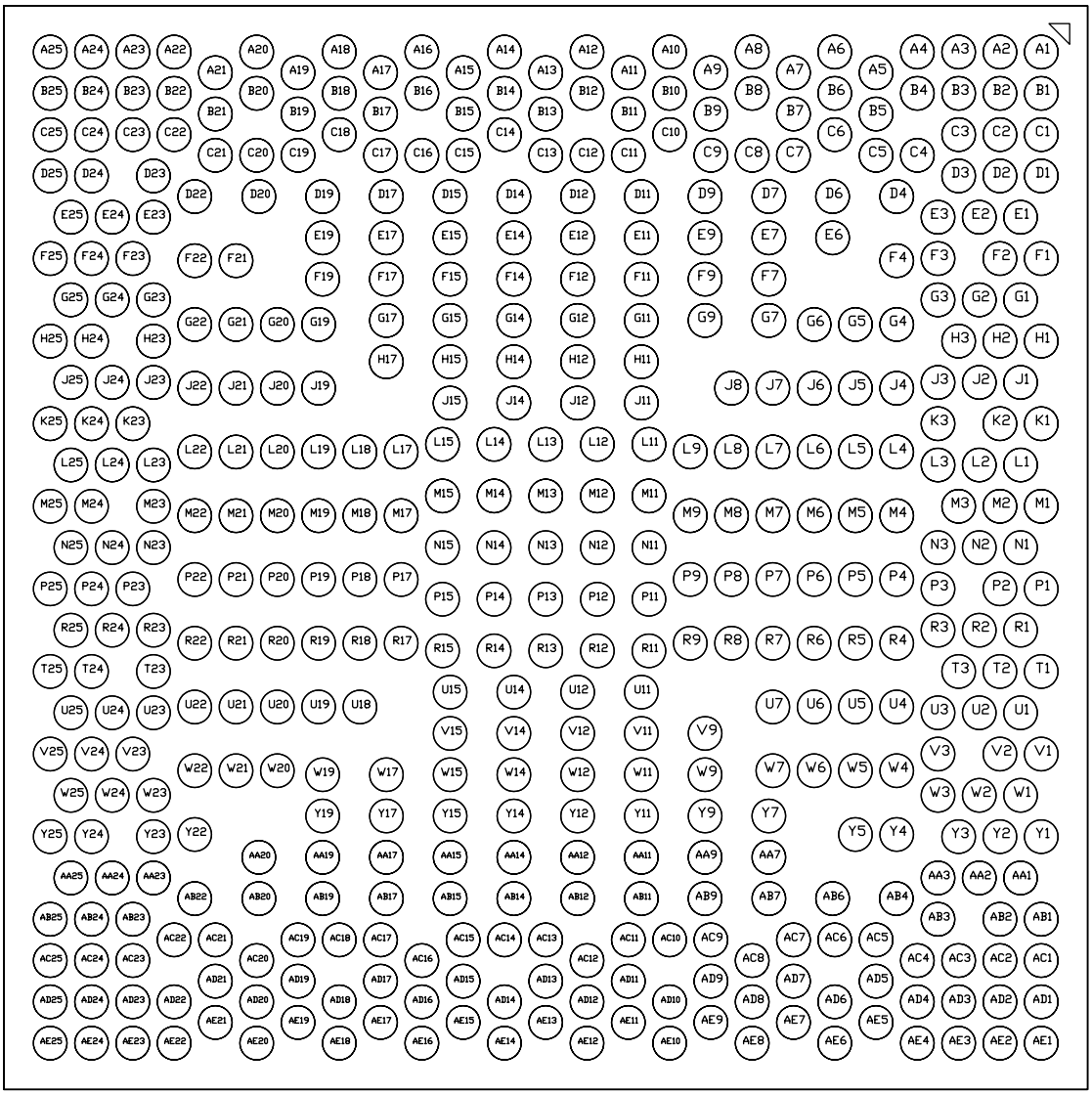

Figure 5-3 RS690 Ball Arrangement

5.3.2 Pressure Specification

To avoid damages to the ASIC (die or solder ball joint cracks) caused by improper mechanical assembly of the cooling device, follow the recommendations below:

- It is recommended that the maximum pressure which is evenly applied across the contact area between the thermal management device and the die does not exceed 40 PSI. Note that a contact pressure of 30-40 PSI is adequate to secure the thermal management device and achieve the lowest thermal contact resistance with a temperature drop across the thermal interface material of no more than 3°C. Also, the surface flatness of the metal spreader should be 0.001 inch/1 inch.
- Pre-test the assembly fixture with a strain gauge to make sure that the flexing of the final assembled board and the pressure applying around the ASIC package will not exceed 600 micron strain under any circumstances.
- Ensure that any distortion (bow or twist) of the board after SMT and cooling device assembly is within industry guidelines (IPC/EIA J-STD-001). For measurement method, refer to the industry approved technique described in the manual IPC-TM-650, section 2.4.22.

5.3.3 Board Solder Reflow Process Recommendations

5.3.3.1 Stencil Opening Size for Solderball Pads on PCB

It is recommended that the stencil aperture for solderballs be kept at the same size as the land pads' except for the nine pads at each corner of the ASIC package, for which a maximum size of 400µm is recommended (see *Figure 5-4* below). This recommendation is based on AMD's sample land pattern design for the RS690, which is available from your AMD CSS representative.

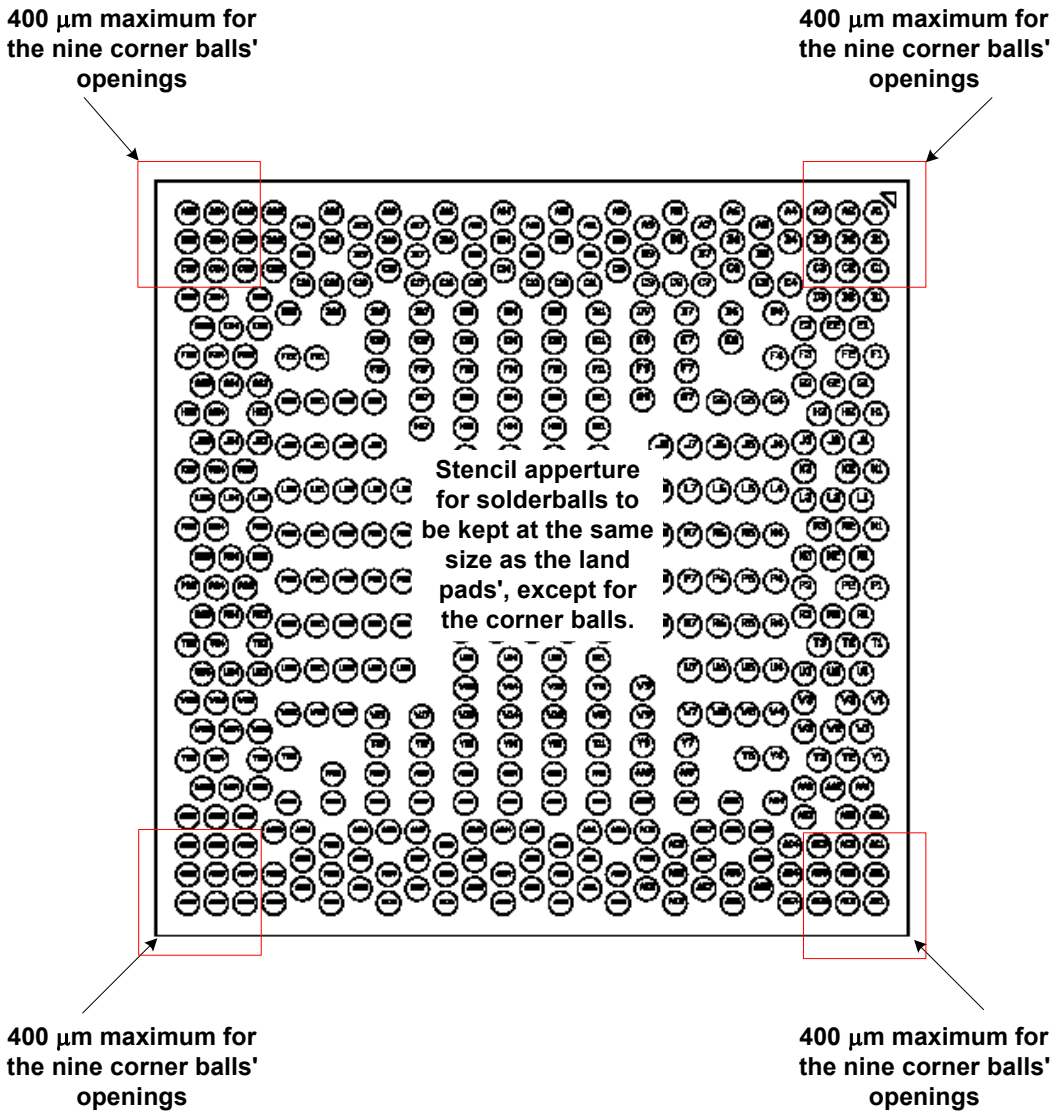

Figure 5-4 Stencil Opening Recommendations

5.3.3.2 Reflow Profile

A reference reflow profile is given below. Please note the following when using RoHS/lead-free solder (SAC105/305/405 Tin-Silver-Cu):

- The final reflow temperature profile will depend on the type of solder paste and chemistry of flux used in the SMT process. Modifications to the reference reflow profile may be required in order to accommodate the requirements of the other components in the application.
- An oven with 10 heating zones or above is recommended.

- To ensure that the reflow profile meets the target specification on both sides of the board, a different profile and oven recipe for the first and second reflow may be required.
- Mechanical stiffening can be used to minimize board warpage during reflow.
- It is suggested to decrease temperature cooling rate to minimize board warpage.
- This reflow profile applies only to RoHS/lead-free (high temperature) soldering process and it should not be used for Eutectic solder packages. Damage may result if this condition is violated.
- Maximum 3 reflows are allowed on the same part.

Table 5-10 Recommended Board Solder Reflow Profile - RoHS/Lead-Free Solder

Profiling Stage	Temperature	Process Range
Overall Preheat	Room temp to 220°C	2 mins to 4 mins
Soaking Time	130°C to 170°C	Typical 60 – 80 seconds
Liquidus	220°C	Typical 60 – 80 seconds
Ramp Rate	Ramp up and Cooling	<2°C / second
Peak	Max. 245°C	235°C +/-5°C
Temperature at peak within 5°C	240°C to 245°C	10 – 30 seconds

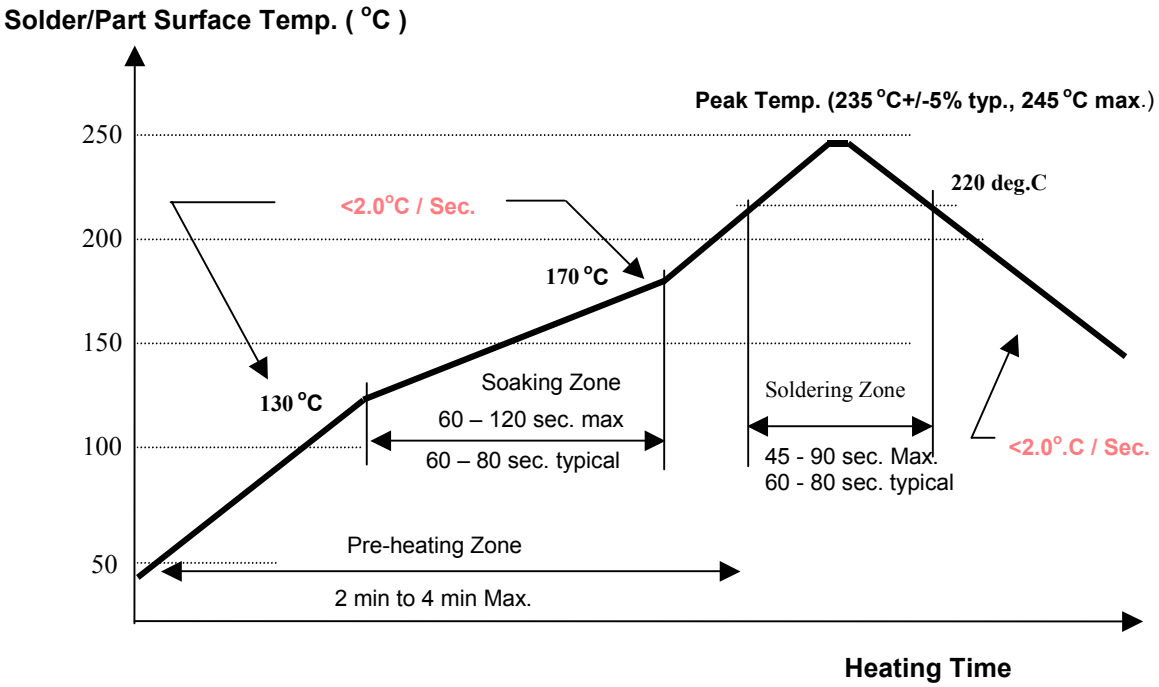

Figure 5-5 RoHS/Lead-Free Solder (SAC305/405 Tin-Silver-Copper) Reflow Profile

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Chapter 6
Power Management and ACPI

6.1 ACPI Power Management Implementation

This chapter describes the support for ACPI power management provided by the RS690. The RS690 supports ACPI Revision 1.0b. The hardware, system BIOS, video BIOS, and drivers of the RS690 have all the logic required for meeting the power management specifications of PC2001, OnNow, and the Windows Logo Program and Device Requirements version 2.1. *Table 6-1, "ACPI States Supported by the RS690,"* describes the ACPI states supported by the RS690. *Table 6-2, "ACPI Signal Definitions,"* describes the signals used in the ACPI power management scheme of the RS690.

Table 6-1 ACPI States Supported by the RS690

ACPI State	Description
Graphics States:	
D0	Full on, display active.
D1	Display Off. RS690 power on. Configuration registers, state, and main memory contents retained.
D3 Hot	Similar to D1, with additional power saving and the graphics PLLs shut off.
D3 Cold	RS690 power off.
Processor States:	
S0/C0: Working State	Working State. The processor is executing instructions.
S0/C1: Halt	CPU Halt state. No instructions are executed. This state has the lowest latency on resume and contributes minimum power savings.
S0/C2: Stop Grant Caches Snoopable	Stop Grant or Cache Snoopable CPU state. This state offers more power savings but has a higher latency on resume than the C1 state.
S0/C3: Stop Grant Caches Not Snoopable	Stop Grant or Cache not Snoopable Sleep state. The CPU's caches maintain state but ignore any snoops. This state offers more power savings but has a higher latency on resume than the C1 and C2 states.
System States:	
S1: Standby Powered On Suspend	System is in Standby mode. This state has low wakeup latency on resume. OEM support of this state is optional.
S3: Standby Suspend to RAM	System is off but context is saved to RAM. OEM support of this state is optional. System memory is put into self-refresh.
S4: Hibernate Suspend to Disk	System is off but context is saved to disk. When the system transitions to the working state, the OS is resumed without a system re-boot.
S5: Soft Off	System is off. OS re-boots when the system transitions to the working state.
G3: Mechanical Off	Occurs when system power (AC or battery) is not present or is unable to keep the system in one of the other states.

Note: Also supported are additional processor power states that are not part of the ACPI specification, e.g. C1E (C1 Enhanced) and C3 pop-up. Please refer to the *SB600 Databook* and the *RS690 Register Programming Requirements* for more information.

Table 6-2 ACPI Signal Definitions

Signal Name	Description	Source
ALLOW_LDTSTOP	Output to the Southbridge to allow LDTSTOP# assertion.	Northbridge
LDTSTOP#	HyperTransport™ Technology Stop: Enables and disables links during system state transitions.	Southbridge
POWERON#	Power on	Power switch
RESET#	Global Reset	Southbridge

6.2 Power Management for the Graphics Controller

The RS690 supports power management for the embedded graphics device as specified by the PCI Bus Power Management Interface Specification version 1.0, according to which the integrated graphics core of the RS690 qualifies as a device embedding a single function in the power management system.

6.2.1 PCI Function Power States

There are up to four power states defined for each PCI function associated with each PCI device in the system. These power states are D0, D1, D2 and D3. D0 (on) consumes the most power while D3 (off) consumes the least. D1 and D2 enable levels of power savings in between those of D0 and D3. The concepts of these power states are universal for all functions in the system. When transitioned to a given power management state, the intended functional behavior is dependent upon the type (or class) of the function.

6.2.2 PCI Power Management Interface

The four basic power management operations are:

- Capabilities Reporting
- Power Status Reporting
- Setting Power State
- System Wakeup

All four of these capabilities are required for each power management function with the exception of wakeup event generation.

This section describes the format of the registers in the PCI Configuration Space that are used by these power management operations. The Status and Capabilities Pointer (CAP_PTR) fields have been highlighted to indicate where the PCI Power Management features appear in the standard Configuration Space Header.

Table 6-3 Standard PCI Configuration Space Header Type 0

RegisterFields(32bits)				Offset
MSB		LSB		
Device ID		Vendor ID		00h (LSB)
Status (with Bit 4 set to 1)		Command		04h
Class Code		Revision ID		08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
Base Address Registers				10h
				14h
				18h
				1Ch
				20h
				24h
CardBus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			CAP_PTR	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch

6.2.3 Capabilities List Data Structure in PCI Configuration Space

The Capabilities bit in the PCI Status register (offset = 06h) indicates whether or not the subject function implements a linked list of extended capabilities. Specifically, if bit 4 is set, the CAP_PTR register is implemented to give offset to the first item in the Capabilities link list.

Table 6-4 PCI Status Register

Bits	Default Value	Read/ Write	Description
15:05	--	--	Refer to *PCI Local Bus Specification*, *Revision 2.2*
04	1b	Read Only	This bit indicates whether this function implements a list of extended capabilities such as PCI power management. When set, this bit indicates the presence of Capabilities. A value of 0 implies that this function does not implement Capabilities.
03:00	0h	Read Only	Reserved

The location of the Capabilities Pointer (CAP_PTR) depends on the PCI header type. See *PCI specification Revision 2.2* for specification of CAP_PTR offsets.

Table 6-5 Capabilities Pointer (CAP_PTR)

Bits	Default Value	Read/ Write	Description
07:00	50h	Read Only	The CAP_PTR provides an offset in the PCI Configuration Space of the function to access the location of the first item in the Capabilities linked list. The CAP_PTR offset is DWORD aligned, so that the two least significant bits are always zeros.

The graphics core implements extended capabilities of the AGP and Power Management. It needs to provide the standardized register interface. The first entry in the chain of descriptors has to be the PMI descriptor, as this functionality will be supported even if the RS690 operates as a PCI device. The Capabilities Identifier for Power Management is 01h.

6.2.4 Register Block Definition

This section describes the PCI Power Management Interface registers. These registers are implemented inside the Host Interface (HI) as part of the configuration space of the device (RS690).

Table 6-6 Power Management Register Block

Register Fields	Offset
Capabilities ID	00h
Next Item Pointer	01h
Power Management Capabilities (PMC)	02h
Power Management Control/Status Register (PMCSR)	04h
Reserved	06h

The first 16 bits (Capabilities ID [offset = 0] and Next Item Pointer [offset = 1]) are used for the linked list infrastructure. The next 32 bits (PMC [offset = 2] and PMCSR registers [offset = 4]) are required for compliance with this specification.

As with all PCI configuration registers, these registers may be accessed as bytes, 16-bit words, or 32-bit DWORDs. All of the write operations to the reserved registers must be treated as no-ops. This implies that the access must be completed normally on the bus and the data should be discarded. Read accesses to the reserved or the unimplemented registers must be completed normally and a data value of 0000h should be returned.

Table 6-7 Power Management Control/Status Register (PMCSR)

Field Name	Bits	Default (Reset)	Description	
Power State	1:0	00b	This field describes the power state of the graphics core.	
			States	Function
			00 = D0	Normal operation, no power savings enabled
			01 = D1	Sleeping state 1: Display is off Host access to DRAM is allowed
			10 = D2	Sleeping state 2 Display is off. All engines are off. Graphics core does not respond to host accesses to the frame buffer.
			11 = D3	Everything, except Host Interface, is turned off.
Power State	15:2	00h	These Read Only bits will return the clock status of each clock tree, generated inside the clock block.	

The offset for each register is listed as an offset from the beginning of the linked list item that is determined either from the CAP_PTR (if Power Management is the first item in the list) or the NEXT_ITEM_PTR of the previous item in the list.

6.2.5 Capability Identifier: Cap_ID (Offset = 0)

The Capability Identifier, when read by system software as 01h, indicates that the data structure currently being pointed to is the PCI Power Management data structure. Each function of a PCI device may have only one item in its capability list with Cap_ID set to 01h.

Table 6-8 Capability Identifier (Cap_ID)

Bits	Default Value	Read/ Write	Description
7:0	01h	Read Only	This field, when set to 01h, identifies the linked list item as being the PCI Power Management registers

Figure 6-1, 'Linked List for Capabilities," shows the implementation of the capabilities list. The CAP_PTR gives the location of the first item in the list. PCI Power Management registers have been stated as example in this list (although the capabilities can be in any order).

- The first byte of each entry is required to be the ID of that capability. The PCI Power Management capability has an ID of 01h.
- The next byte is a pointer giving an absolute offset in the functions PCI Configuration Space to the next item in the list and must be DWORD aligned.
- If there are no more entries in the list, the NEXT_ITEM_PTR must be set to 0 to indicate an end of the linked list. Each capability can then have registers following the NEXT_ITEM_PTR.

The definition of these registers (including layout, size, and bit definitions) is specific to each capability. The PCI Power Management Register Block is defined in *Figure 6-1, 'Linked List for Capabilities,"* below.

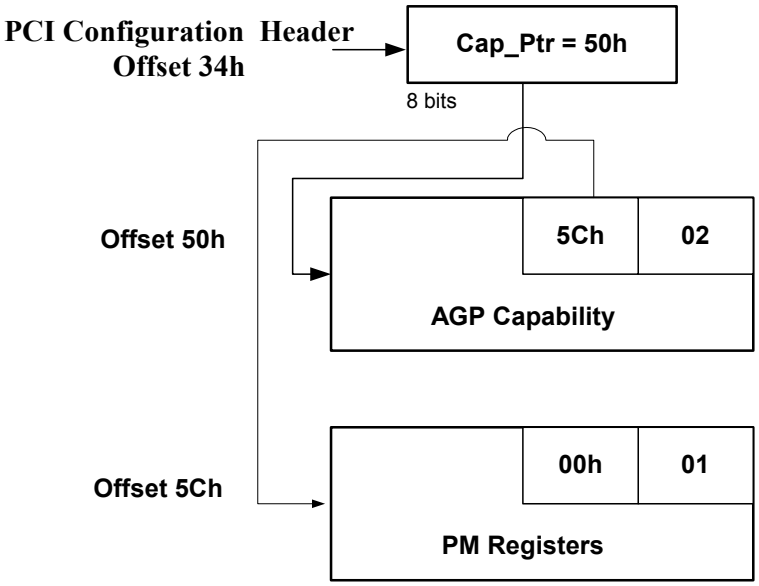

Figure 6-1 Linked List for Capabilities

6.2.6 Next Item Pointer

The Next Item Pointer register describes the location of the next item in the capability list of the function. The value given is an offset in the PCI Configuration Space of that function. This register must be set to 00h if the function does not implement any other capabilities defined by the PCI Specifications for inclusion in the capabilities list, or if power management is the last item in the list.

Table 6-9 Next Item Pointer (NEXT_ITEM_PTR)

Bits	Default Value	Read/ Write	Description
7:0	80h	Read Only	This field provides an offset in the PCI Configuration Space of the function pointing to the location of next item in the capability list of the function. For Power Management of the RS690, this pointer is set to 80h and it points to the next capability pointer of the MSI structure.

6.2.7 PMC - Power Management Capabilities (Offset = 2)

The Power Management Capabilities register is a 16-bit Read Only register that provides information on the capabilities of the function related to power management. The information in this register is generally static and is known at design time.

Table 6-10 Power Management Capabilities – PMC

Bits	Default Value	Read/ Write	Description
15:11	00111b	Read Only	This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) XXXX1b - PME# can be asserted from D0. bit(12) XXX1Xb - PME# can be asserted from D1. bit(13) XX1XXb - PME# can be asserted from D2. bit(14) X0XXXb - PME# cannot be asserted from D3hot. bit(15) 0XXXXb - PME# cannot be asserted from D3cold.
10	1b	Read Only	RS690 supports D2.

Table 6-10 Power Management Capabilities – PMC (Continued)

Bits	Default Value	Read/ Write	Description
9	1b	Read Only	RS690 supports D1.
8:6	000b	Read Only	Reserved
5	1b	Read Only	The Device Specific Initialization bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. The RS690 requires device specific initialization after Reset; this field must therefore return a value 1 to the system.
4	0b	Read Only	Reserved
3	0b	Read Only	Reserved
2:0	001b	Read Only	A value of 001b indicates that this function complies with Revision 1.0 of the PCI Power Management Interface Specification.

Chapter 7
Testability

7.1 Test Capability Features

The RS690 has integrated test modes and capabilities. These test features cover both the ASIC and board level testing. The ASIC tests provide a very high fault coverage and low DPM (Defect Per Million) ratio of the part. The board level tests modes can be used for motherboard manufacturing and debug purposes. The following are the test modes of the RS690:

- Full scan implementation on the digital core logic that provides about 99% fault coverage through ATPG (Automatic Test Pattern Generation Vectors).
- Dedicated test logic for the on-chip custom memory macros to provide complete coverage on these modules.
- Improved access to the analog modules and PLLs in the RS690 to allow full evaluation and characterization of these modules.
- A JTAG test mode (which is not entirely compliant to the IEEE 1149.1 standard) to allow board level testing of neighboring devices.
- An XOR TREE test mode on all the digital I/Os to allow for proper soldering verification at the board level.
- A VOH/VOL test mode on all digital I/Os to allow for proper verification of output high and output low voltages at the board level.

These test modes can be accessed through the settings on the instruction register of the JTAG circuitry.

7.2 Test Interface

Table 7-1 Pins on the Test Interface

Pin Name	Ball number	Type	Description
TESTMODE	C3	I	IEEE 1149.1 test port reset
DDC_DATA	B3	I	TMS: Test Mode Select (IEEE 1149.1 test mode select)
I2C_DATA	B4	I	TDI: Test Mode Data In (IEEE 1149.1 data in)
I2C_CLK	A2	I	TCLK: Test Mode Clock (IEEE 1149.1 clock)
TMDS_HPD	C14	O	TDO: Test Mode Data Out (IEEE 1149.1 data out)
POWERGOOD	C11	I	I/O Reset
OSCIN	B11	I	I/O Test Clock

7.3 XOR Tree

7.3.1 Brief Description of an XOR Tree

An example of a generic XOR tree is shown in the *Figure 7-1* below.

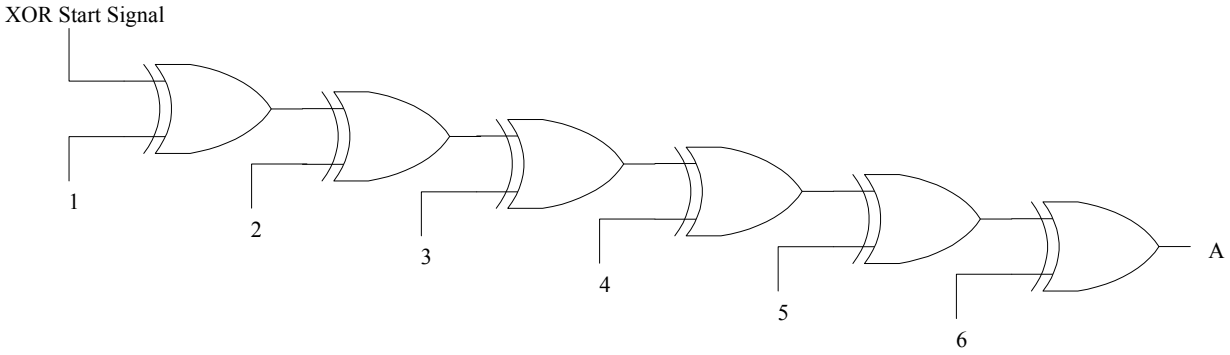

Figure 7-1 An Example of a Generic XOR Tree

Pin A is assigned to the output direction, and pins 1 through 6 are assigned to the input direction. It can be seen that after all pins 1 to 6 are assigned to logic 0 or 1, a logic change in any one of these pins will toggle the output pin A.

The following is the truth table for the XOR tree shown in *Figure 7-1* The XOR start signal is assumed to be logic 1.

Table 7-2 Example of an XOR Tree

Test Vector number	Input Pin 1	Input Pin 2	Input Pin 3	Input Pin 4	Input Pin 5	Input Pin 6	Output Pin A
1	0	0	0	0	0	0	1
2	1	0	0	0	0	0	0
3	1	1	0	0	0	0	1
4	1	1	1	0	0	0	0
5	1	1	1	1	0	0	1
6	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1

7.3.2 Description of the XOR Tree for the RS690

The XOR start signal is applied at the TDI pin of the JTAG circuitry and the output of the XOR tree is obtained at the TDO pin. Refer to *Section 7.3.4* for the list of the signals included on the XOR tree. There is no specific connection order to the signals on the tree. A toggle of any of these balls in the XOR tree will cause the output to toggle.

7.3.3 XOR Tree Activation

The RS690 chip enters the XOR tree test mode by means of the JTAG. First, the 8-bit instruction register of the JTAG is loaded with the XOR instruction (“00001000”). This instruction assigns the input direction to all the pins except pin TDO, which is assigned the output direction to serve as the output of the XOR tree. After loading, the JTAG is taken to the Run-Test state for completion of the XOR tree initialization.

Note: 10MHz clock frequency is recommended for the XOR TREE test mode.

7.3.4 XOR Chain for the RS690

When the XOR tree is activated, any pin on the XOR tree must be either pulled down or pulled up to the I/O voltage of the pin. Only pins that are **not** on the XOR tree can be left floating.

When differential signal pairs are listed as single entries on the XOR tree, opposite input values should be applied to the two signals in each pair (e.g., for entry no. 13 on the tree, when “1” is applied to HT_RXCAD15P, “0” should be applied to HT_RXCAD15N).

Table 7-3 RS690 XOR Tree

No.	Pin Name	Ball Ref.
1	GPIO2	G12
2	GPIO4	F12
3	GPIO3	E12
4	DACVSYNC	C6
5	DACHSYNC	A5
6	DACSCL	B6
7	DFT_GPIO0	D6
8	DFT_GPIO1	D7
9	DFT_GPIO2	C8
10	DFT_GPIO3	C7
11	DFT_GPIO4	B8
12	DFT_GPIO5	A8
13	HT_RXCAD15N/P	R18/R19
14	HT_RXCAD14N/P	R22/R21
15	HT_RXCAD13N/P	U21/U22
16	HT_RXCAD12N/P	U19/U18
17	HT_RXCAD11N/P	W20/W19
18	HT_RXCAD10N/P	AB22/AC21
19	HT_RXCAD9N/P	AA20/AB20
20	HT_RXCAD8N/P	Y19/AA19
21	HT_RXCAD7N/P	R25/T24
22	HT_RXCAD6N/P	U24/U25
23	HT_RXCAD5N/P	U23/V23
24	HT_RXCAD4N/P	V25/V24
25	HT_RXCAD3N/P	AA24/AA25
26	HT_RXCAD2N/P	AA23/AB23
27	HT_RXCAD1N/P	AB25/AB24
28	HT_RXCAD0N/P	AC25/AC24
29	HT_RXCTLN/P	P25/P24
30	HT_RXCLK1N/P	W22/W21
31	HT_RXCLK0N/P	W25/Y24
32	GPP_RX3N/P	AA9/AB9
33	GPP_RX2N/P	AA7/Y7
34	GPP_RX1N/P	AE20/AD20
35	GPP_RX0N/P	AE16/AD16
36	SB_RX3N/P	AB11/AA11
37	SB_RX2N/P	W12/W11
38	SB_RX1N/P	AA12/AB12
39	SB_RX0N/P	W15/W14
40	GFX_RX15N/P	AB6/AB7
41	GFX_RX14N/P	W9/V9
42	GFX_RX13N/P	Y5/Y4
43	GFX_RX12N/P	W5/W4
44	GFX_RX11N/P	U5/U4
45	GFX_RX10N/P	R8/R7
46	GFX_RX9N/P	R5/R4
47	GFX_RX8N/P	P5/P4
48	GFX_RX7N/P	P7/P8
49	GFX_RX6N/P	M5/M4
50	GFX_RX5N/P	M7/M8
51	GFX_RX4N/P	L5/L4
52	GFX_RX3N/P	L7/L8
53	GFX_RX2N/P	J5/J4
54	GFX_RX1N/P	J7/J8
55	GFX_RX0N/P	G4/G5
56	NC/NC	AD17/AE17
57	NC	AE21
58	NC	AD18
59	NC	AC17
60	NC	AE15
61	NC	AC13
62	NC	AE13
63	NC	AD13

7.4 VOH/VOL Test

7.4.1 Brief Description of a VOH/VOL Tree

The VOH/VOL logic gives signal output on I/Os when test patterns are applied through the TEST_ODD and TEST_EVEN inputs. Sample of a generic VOH/VOL tree is shown in the *Figure 7-2* below.

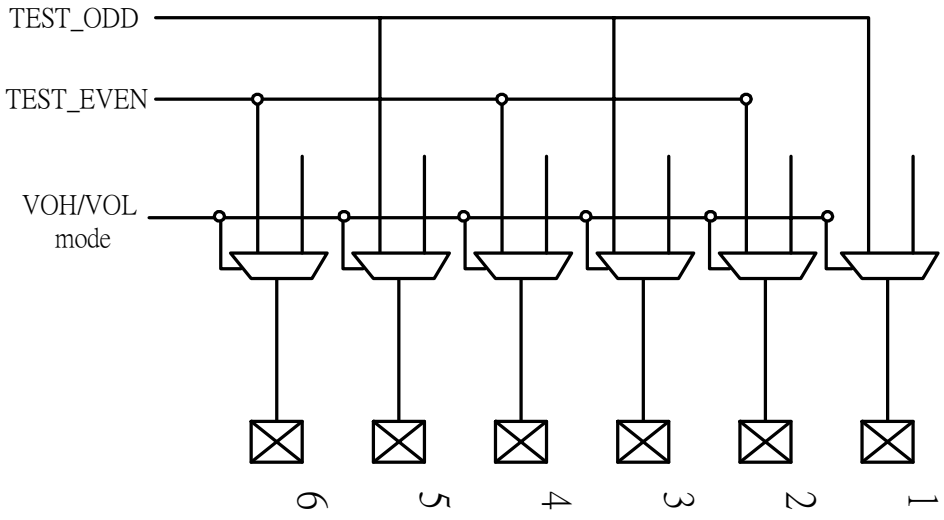

Figure 7-2 Sample of a Generic VOH/VOL Tree

The following is the truth table for the above VOH/VOL tree.

Table 7-4 Truth Table for the VOH/VOL Tree Outputs

Test Vector Number	TEST_ODD Input	TEST_EVEN Input	Output Pin 1	Output Pin 2	Output Pin 3	Output Pin 4	Output Pin 5	Output Pin 6
1	0	0	0	0	0	0	0	0
2	0	1	0	1	0	1	0	1
3	1	0	1	0	1	0	1	0
4	1	1	1	1	1	1	1	1

Refer to *Table 7.4.3, "VOH/VOL Pin List," on page 7-5* for the list of pins that are on the VOH/VOL tree.

7.4.2 VOH/VOL Tree Activation

To activate the VOH/VOL tree and run a VOH/VOL test, perform the sequence below:

1. Supply a clock at any speed (same or faster than test pattern data rate) to the OSCIN pin as the I/O test clock source.
2. Set POWERGOOD to 0.
3. Set TESTMODE to 1.
4. Set DACSDA to 0.

5. Load JTAG instruction register with the instruction 0110 0011.

6. Load JTAG instruction register with the instruction 0010 0111.

7. Set POWERGOOD to 1.

8. Load JTAG instruction register with the instruction 1001 1001.

9. Run test by loading JTAG data register with data 0000 0000 0000 00xy, where bit x is the input value for TEST_ODD and bit y that for TEST_EVEN (see Table 7-4 above).

10. To end test, load JTAG instruction register with the instruction 0101 1101.

7.4.3 VOH/VOL Pin List

Table 7-5 below shows the RS690 VOH/VOL tree. There is no specific order of connection. Under the Control column, an "ODD" or "EVEN" indicates that the logical output of the pin is same as the "TEST_ODD" or "TEST_EVEN" input respectively.

When a differential pair appear in the table as a single entry, the output of the positive ("P") pin is indicated in the Control column (see last paragraph for explanations), and the output of the negative pin ("N") will be of the opposite value. E.g., for entry no. 1 on the tree, when TEST_EVEN is 1, HT_TXCAD15P will give a value of 1 and HT_TXCAD15N will give a value of 0.

Table 7-5 RS690 VOH/VOL Tree

No.	Pin Name	Ball Ref.	Control
1	HT_TXCAD15P/N	P21/P22	EVEN
2	HT_TXCAD14P/N	P18/P19	ODD
3	HT_TXCAD13P/N	M22/M21	EVEN
4	HT_TXCAD12P/N	M18/M19	ODD
5	HT_TXCAD11P/N	L18/L19	EVEN
6	HT_TXCAD10P/N	G22/G21	ODD
7	HT_TXCAD9P/N	J20/J21	EVEN
8	HT_TXCAD8P/N	F21/F22	ODD
9	HT_TXCTLP/N	N23/P23	EVEN
10	HT_TXCAD7P/N	N24/N25	ODD
11	HT_TXCAD6P/N	L25/M24	EVEN
12	HT_TXCAD5P/N	K25/K24	ODD
13	HT_TXCAD4P/N	J23/K23	EVEN
14	HT_TXCAD3P/N	G25/H24	ODD
15	HT_TXCAD2P/N	F25/F24	EVEN
16	HT_TXCAD1P/N	E23/F23	ODD
17	HT_TXCAD0P/N	E24/E25	EVEN
18	DACSCL	B6	ODD
19	DACVSYNC	C6	EVEN
20	DACHSYNC	A5	ODD
21	GPIO2	G12	EVEN
22	GPIO4	F12	ODD
23	GPIO3	E12	EVEN
24	DFT_GPIO5	A8	ODD
25	DFT_GPIO4	B8	EVEN
26	DFT_GPIO3	C7	ODD
27	DFT_GPIO2	C8	EVEN
28	DFT_GPIO1	D7	ODD
29	DFT_GPIO0	D6	EVEN
30	SB_TX3P/N	AD7/AE7	ODD
31	SB_TX2P/N	AD8/AE8	EVEN
32	SB_TX1P/N	AC8/AD9	ODD
33	SB_TX0P/N	AE9/AD10	EVEN
34	GPP_TX3P/N	AD5/AD6	ODD
35	GPP_TX2P/N	AD4/AE5	EVEN
36	GPP_TX1P/N	AD19/AE19	ODD
37	GPP_TX0P/N	AD14/AD15	EVEN
38	GFX_TX15P/N	AE3/AE4	ODD
39	GFX_TX14P/N	AB1/AC1	EVEN
40	GFX_TX13P/N	AA2/AB2	ODD

No.	Pin Name	Ball Ref.	Control
41	GFX_TX12P/N	Y2/AA1	EVEN
42	GFX_TX11P/N	W1/W2	ODD
43	GFX_TX10P/N	V3/W3	EVEN
44	GFX_TX9P/N	V2/V1	ODD
45	GFX_TX8P/N	T2/U1	EVEN
46	GFX_TX7P/N	R1/R2	ODD
47	GFX_TX6P/N	P3/R3	EVEN
48	GFX_TX5P/N	P2/P1	ODD
49	GFX_TX4P/N	N2/N1	EVEN
50	GFX_TX3P/N	L1/L2	ODD
51	GFX_TX2P/N	K3/L3	EVEN
52	GFX_TX1P/N	K2/K1	ODD
53	GFX_TX0P/N	J1/H2	EVEN
54	NC	AE17	EVEN
55	NC	AD17	ODD
56	NC	AE21	EVEN
57	NC	AD18	ODD
58	NC	AC17	EVEN
59	NC	AE15	ODD
60	NC	AC13	ODD
61	NC	AE13	ODD
62	NC	AD13	ODD

Appendix A
Pin Listings

This appendix contains pin listings for the RS690 sorted in different ways. To go to the listing of interest, use the linked cross-references below:

"RS690 Pin List Sorted by Ball Reference" on page A-2

"RS690 Pin List Sorted by Pin Name" on page A-6

A.1 RS690 Pin List Sorted by Ball Reference

Table A-1 RS690 Pin List Sorted by Ball Reference

Ball Ref.	Pin Name
A1	VSSA
A10	PLLVDD18
A11	PLLVDD12
A12	LVDDR18D
A13	TXOUT_L1N
A14	LVSSR
A15	TXOUT_U0P
A16	LVSSR
A17	TXOUT_U2N
A18	TXOUT_U3P
A19	VDD_CORE
A2	I2C_CLK
A20	AVDDDI
A21	AVDDQ
A22	AVSSQ
A23	VSS
A24	HT_RXCALP
A25	VSS
A3	STRP_DATA
A4	VDD_CORE
A5	DACHSYNC
A6	DACSDA
A7	VDD_CORE
A8	DFT_GPIO5
A9	VDD_CORE
AA1	GFX_TX12N
AA11	SB_RX3P
AA12	SB_RX1N
AA14	NC
AA15	THERMALDIODE_P
AA17	VDD_HT
AA19	HT_RXCAD8P
AA2	GFX_TX13P
AA20	HT_RXCAD9N
AA23	HT_RXCAD2N
AA24	HT_RXCAD3N
AA25	HT_RXCAD3P
AA3	VSSA
AA7	GPP_RX2N
AA9	GPP_RX3N
AB1	GFX_TX14P
AB11	SB_RX3N
AB12	SB_RX1P
AB14	NC

Ball Ref.	Pin Name
AB15	THERMALDIODE_N
AB17	VDD_HT
AB19	VDD_HT
AB2	GFX_TX13N
AB20	HT_RXCAD9P
AB22	HT_RXCAD10N
AB23	HT_RXCAD2P
AB24	HT_RXCAD1P
AB25	HT_RXCAD1N
AB3	VDDA_12
AB4	VDDA_12
AB6	GFX_RX15N
AB7	GFX_RX15P
AB9	GPP_RX3P
AC1	GFX_TX14N
AC10	VSSA
AC11	VDDA_12_PKG
AC12	VDDR
AC13	DEBUG2
AC14	VSS
AC15	VSS
AC16	VSS
AC17	DEBUG9
AC18	VDD_HT
AC19	VDD_HT
AC2	VSSA
AC20	VDD_HT
AC21	HT_RXCAD10P
AC22	VSS
AC23	VSS
AC24	HT_RXCAD0P
AC25	HT_RXCAD0N
AC3	VDDA_12
AC4	VSSA
AC5	VSSA
AC6	VSSA
AC7	VSSA
AC8	SB_TX1P
AC9	VSSA
AD1	VSSA
AD10	SB_TX0N
AD11	PCE_CALRP
AD12	VDDR
AD13	DEBUG0

Ball Ref.	Pin Name
AD14	GPP_TX0P
AD15	GPP_TX0N
AD16	GPP_RX0P
AD17	DEBUG13
AD18	DEBUG10
AD19	GPP_TX1P
AD2	VDDA_12
AD20	GPP_RX1P
AD21	VDD_HT
AD22	VDD_HT
AD23	VDD_HT
AD24	VDD_HT
AD25	VSS
AD3	VSSA
AD4	GPP_TX2P
AD5	GPP_TX3P
AD6	GPP_TX3N
AD7	SB_TX3P
AD8	SB_TX2P
AD9	SB_TX1N
AE1	VDDA_12
AE10	VSSA
AE11	PCE_CALRN
AE12	VDDR
AE13	DEBUG1
AE14	VSS
AE15	DEBUG6
AE16	GPP_RX0N
AE17	DEBUG14
AE18	VSS
AE19	GPP_TX1N
AE2	VDDA_12
AE20	GPP_RX1N
AE21	DEBUG15
AE22	VSS
AE23	VDD_HT
AE24	VDD_HT
AE25	VDD_HT
AE3	GFX_TX15P
AE4	GFX_TX15N
AE5	GPP_TX2N
AE6	VSSA
AE7	SB_TX3N
AE8	SB_TX2N

Ball Ref.	Pin Name
AE9	SB_TX0P
B1	VDDA_12
B10	PLLVSS
B11	OSCIN
B12	LVDDR18D
B13	TXOUT_L1P
B14	TXOUT_L0P
B15	TXOUT_L0N
B16	TXOUT_U0N
B17	TXOUT_U2P
B18	TXOUT_U3N
B19	VDD_CORE
B2	BMREQ#
B20	AVSSDI
B21	RSET
B22	AVDD
B23	HTREFCLK
B24	HTPVDD
B25	HTPVSS
B3	DDC_DATA
B4	I2C_DATA
B5	ALLOW_LDTSTOP
B6	DACSCL
B7	VSS
B8	DFT_GPIO4
B9	VDD_CORE
C1	VDDA_12
C10	SYSRESET#
C11	POWERGOOD
C12	LVDDR33
C13	LVDDR33
C14	TMDS_HPD
C15	LVSSR
C16	LVSSR
C17	TXOUT_U1P
C18	TXOUT_U1N
C19	LVSSR
C2	TVCLKIN
C20	Y
C21	C
C22	AVDD
C23	HTTSTCLK
C24	HT_RXCALN
C25	HT_TXCALP
C3	TESTMODE
C4	VSS

Ball Ref.	Pin Name
C5	LDTSTOP#
C6	DACVSYNC
C7	DFT_GPIO3
C8	DFT_GPIO2
C9	VDD_CORE
D1	VDDA_12
D11	VDDR3
D12	LVSSR
D14	LPVDD
D15	TXCLK_LN
D17	TXOUT_L3P
D19	COMP
D2	VDDA_12
D20	VDD_CORE
D22	VDD_HT_PKG
D23	VSS
D24	HT_TXCALN
D25	VSS
D3	VDDA_12
D4	VSS
D6	DFT_GPIO0
D7	DFT_GPIO1
D9	VDD_CORE
E1	GFX_CLKN
E11	VDDR3
E12	GPIO3
E14	LPVSS
E15	TXCLK_LP
E17	TXOUT_L3N
E19	RED
E2	VDDA_12
E23	HT_TXCAD1P
E24	HT_TXCAD0P
E25	HT_TXCAD0N
E3	VDDA_12
E6	VDDA_12
E7	VDD_PLL
E9	VSS
F1	VSSA
F11	VSS
F12	GPIO4
F14	LVSSR
F15	LVSSR
F17	VSS
F19	GREEN
F2	GFX_CLKP

Ball Ref.	Pin Name
F21	HT_TXCAD8P
F22	HT_TXCAD8N
F23	HT_TXCAD1N
F24	HT_TXCAD2N
F25	HT_TXCAD2P
F3	VSSA
F4	VDDA_12
F7	VDD_PLL
F9	VSS_PLL
G1	SB_CLKP
G11	VSS
G12	GPIO2
G14	TXOUT_L2N
G15	TXCLK_UN
G17	AVSSN
G19	BLUE
G2	SB_CLKN
G20	VDD_CORE
G21	HT_TXCAD10N
G22	HT_TXCAD10P
G23	VSS
G24	VSS
G25	HT_TXCAD3P
G3	VSSA
G4	GFX_RX0N
G5	GFX_RX0P
G6	VSSA
G7	VDDA_12
G9	VSS_PLL
H1	VSSA
H11	VDD_CORE
H12	VSS
H14	TXOUT_L2P
H15	TXCLK_UP
H17	AVSSN
H2	GFX_TX0N
H23	VSS
H24	HT_TXCAD3N
H25	VSS
H3	VSSA
J1	GFX_TX0P
J11	VDD_CORE
J12	VSS
J14	VDD_18
J15	VDD_18
J19	VDD_CORE

Ball Ref.	Pin Name
J2	VSSA
J20	HT_TXCAD9P
J21	HT_TXCAD9N
J22	VSS
J23	HT_TXCAD4P
J24	HT_TXCLK0P
J25	HT_TXCLK0N
J3	VSSA
J4	GFX_RX2P
J5	GFX_RX2N
J6	VSSA
J7	GFX_RX1N
J8	GFX_RX1P
K1	GFX_TX1N
K2	GFX_TX1P
K23	HT_TXCAD4N
K24	HT_TXCAD5N
K25	HT_TXCAD5P
K3	GFX_TX2P
L1	GFX_TX3P
L11	VDD_CORE
L12	VSS
L13	VDD_CORE
L14	VSS
L15	VDD_CORE
L17	VDD_CORE
L18	HT_TXCAD11P
L19	HT_TXCAD11N
L2	GFX_TX3N
L20	VSS
L21	HT_TXCLK1P
L22	HT_TXCLK1N
L23	VSS
L24	VSS
L25	HT_TXCAD6P
L3	GFX_TX2N
L4	GFX_RX4P
L5	GFX_RX4N
L6	VSSA
L7	GFX_RX3N
L8	GFX_RX3P
L9	VDDA_12
M1	VDDA_12_PKG
M11	VSS
M12	VDD_CORE
M13	VSS
M14	VDD_CORE

Ball Ref.	Pin Name
M15	VSS
M17	VSS
M18	HT_TXCAD12P
M19	HT_TXCAD12N
M2	VSSA
M20	VSS
M21	HT_TXCAD13N
M22	HT_TXCAD13P
M23	VSS
M24	HT_TXCAD6N
M25	VSS
M3	VSSA
M4	GFX_RX6P
M5	GFX_RX6N
M6	VSSA
M7	GFX_RX5N
M8	GFX_RX5P
M9	VDDA_12
N1	GFX_TX4N
N11	VDD_CORE
N12	VSS
N13	VDD_CORE
N14	VSS
N15	VDD_CORE
N2	GFX_TX4P
N23	HT_TXCTLP
N24	HT_TXCAD7P
N25	HT_TXCAD7N
N3	VSSA
P1	GFX_TX5N
P11	VSS
P12	VDD_CORE
P13	VSS
P14	VDD_CORE
P15	VSS
P17	VDD_CORE
P18	HT_TXCAD14P
P19	HT_TXCAD14N
P2	GFX_TX5P
P20	VSS
P21	HT_TXCAD15P
P22	HT_TXCAD15N
P23	HT_TXCTLN
P24	HT_RXCTLP
P25	HT_RXCTLN
P3	GFX_TX6P
P4	GFX_RX8P

Ball Ref.	Pin Name
P5	GFX_RX8N
P6	VSSA
P7	GFX_RX7N
P8	GFX_RX7P
P9	VSSA
R1	GFX_TX7P
R11	VDD_CORE
R12	VSS
R13	VDD_CORE
R14	VSS
R15	VDD_CORE
R17	VSS
R18	HT_RXCAD15N
R19	HT_RXCAD15P
R2	GFX_TX7N
R20	VSS
R21	HT_RXCAD14P
R22	HT_RXCAD14N
R23	VSS
R24	VSS
R25	HT_RXCAD7N
R3	GFX_TX6N
R4	GFX_RX9P
R5	GFX_RX9N
R6	VSSA
R7	GFX_RX10P
R8	GFX_RX10N
R9	VSSA
T1	VSSA
T2	GFX_TX8P
T23	VSS
T24	HT_RXCAD7P
T25	VSS
T3	VSSA
U1	GFX_TX8N
U11	VDD_CORE
U12	VDD_CORE
U14	VDD_CORE
U15	VDD_CORE
U18	HT_RXCAD12P
U19	HT_RXCAD12N
U2	VSSA
U20	VSS
U21	HT_RXCAD13N
U22	HT_RXCAD13P
U23	HT_RXCAD5N
U24	HT_RXCAD6N

Ball Ref.	Pin Name
U25	HT_RXCAD6P
U3	VSSA
U4	GFX_RX11P
U5	GFX_RX11N
U6	VSSA
U7	VDDA_12
V1	GFX_TX9N
V11	VSSA
V12	VSSA
V14	VSSA
V15	VSSA
V2	GFX_TX9P
V23	HT_RXCAD5P
V24	HT_RXCAD4P
V25	HT_RXCAD4N
V3	GFX_TX10P
V9	GFX_RX14P
W1	GFX_TX11P
W11	SB_RX2P
W12	SB_RX2N
W14	SB_RX0P
W15	SB_RX0N
W17	VDD_HT
W19	HT_RXCAD11P
W2	GFX_TX11N
W20	HT_RXCAD11N
W21	HT_RXCLK1P
W22	HT_RXCLK1N
W23	VSS
W24	VSS
W25	HT_RXCLK0N
W3	GFX_TX10N
W4	GFX_RX12P
W5	GFX_RX12N
W6	VSSA
W7	VDDA_12
W9	GFX_RX14N
Y1	VSSA
Y11	VSSA
Y12	VSSA
Y14	VSSA
Y15	VSSA
Y17	VDD_HT
Y19	HT_RXCAD8N
Y2	GFX_TX12P
Y22	VSS
Y23	VSS
Y24	HT_RXCLK0P
Y25	VSS
Y3	VSSA
Y4	GFX_RX13P
Y5	GFX_RX13N
Y7	GPP_RX2P
Y9	VSSA

A.2 RS690 Pin List Sorted by Pin Name

Table A-2 RS690 Pin List Sorted by Pin Name

Pin Name	Ball Ref.
ALLOW_LDTSTOP	B5
AVDD	B22
AVDD	C22
AVDDDI	A20
AVDDQ	A21
AVSSDI	B20
AVSSN	G17
AVSSN	H17
AVSSQ	A22
BLUE	G19
BMREQ#	B2
C	C21
COMP	D19
DACHSYNC	A5
DACSCL	B6
DACSDA	A6
DACVSYNC	C6
DDC_DATA	B3
DEBUG0	AD13
DEBUG1	AE13
DEBUG10	AD18
DEBUG13	AD17
DEBUG14	AE17
DEBUG15	AE21
DEBUG2	AC13
DEBUG6	AE15
DEBUG9	AC17
DFT_GPIO0	D6
DFT_GPIO1	D7
DFT_GPIO2	C8
DFT_GPIO3	C7
DFT_GPIO4	B8
DFT_GPIO5	A8
GFX_CLKN	E1
GFX_CLKP	F2
GFX_RX0N	G4
GFX_RX0P	G5
GFX_RX10N	R8
GFX_RX10P	R7
GFX_RX11N	U5
GFX_RX11P	U4
GFX_RX12N	W5
GFX_RX12P	W4
GFX_RX13N	Y5
GFX_RX13P	Y4
GFX_RX14N	W9
GFX_RX14P	V9
GFX_RX15N	AB6
GFX_RX15P	AB7
GFX_RX1N	J7
GFX_RX1P	J8
GFX_RX2N	J5
GFX_RX2P	J4
GFX_RX3N	L7
GFX_RX3P	L8
GFX_RX4N	L5
GFX_RX4P	L4
GFX_RX5N	M7
GFX_RX5P	M8
GFX_RX6N	M5
GFX_RX6P	M4
GFX_RX7N	P7
GFX_RX7P	P8
GFX_RX8N	P5
GFX_RX8P	P4
GFX_RX9N	R5
GFX_RX9P	R4
GFX_TX0N	H2
GFX_TX0P	J1
GFX_TX10N	W3
GFX_TX10P	V3
GFX_TX11N	W2
GFX_TX11P	W1
GFX_TX12N	AA1
GFX_TX12P	Y2
GFX_TX13N	AB2
GFX_TX13P	AA2
GFX_TX14N	AC1
GFX_TX14P	AB1
GFX_TX15N	AE4
GFX_TX15P	AE3
GFX_TX1N	K1
GFX_TX1P	K2
GFX_TX2N	L3
GFX_TX2P	K3
GFX_TX3N	L2
GFX_TX3P	L1
GFX_TX4N	N1
GFX_TX4P	N2
GFX_TX5N	P1
GFX_TX5P	P2
GFX_TX6N	R3
GFX_TX6P	P3
GFX_TX7N	R2
GFX_TX7P	R1
GFX_TX8N	U1
GFX_TX8P	T2
GFX_TX9N	V1
GFX_TX9P	V2
GPIO2	G12
GPIO3	E12
GPIO4	F12
GPP_RX0N	AE16
GPP_RX0P	AD16
GPP_RX1N	AE20
GPP_RX1P	AD20
GPP_RX2N	AA7
GPP_RX2P	Y7
GPP_RX3N	AA9
GPP_RX3P	AB9
GPP_TX0N	AD15
GPP_TX0P	AD14
GPP_TX1N	AE19
GPP_TX1P	AD19
GPP_TX2N	AE5
GPP_TX2P	AD4
GPP_TX3N	AD6
GPP_TX3P	AD5
GREEN	F19
HT_RXCAD0N	AC25
HT_RXCAD0P	AC24
HT_RXCAD10N	AB22
HT_RXCAD10P	AC21
HT_RXCAD11N	W20
HT_RXCAD11P	W19
HT_RXCAD12N	U19
HT_RXCAD12P	U18
HT_RXCAD13N	U21
HT_RXCAD13P	U22
HT_RXCAD14N	R22
HT_RXCAD14P	R21
HT_RXCAD15N	R18

Pin Name	Ball Ref.
HT_RXCAD15P	R19
HT_RXCAD1N	AB25
HT_RXCAD1P	AB24
HT_RXCAD2N	AA23
HT_RXCAD2P	AB23
HT_RXCAD3N	AA24
HT_RXCAD3P	AA25
HT_RXCAD4N	V25
HT_RXCAD4P	V24
HT_RXCAD5N	U23
HT_RXCAD5P	V23
HT_RXCAD6N	U24
HT_RXCAD6P	U25
HT_RXCAD7N	R25
HT_RXCAD7P	T24
HT_RXCAD8N	Y19
HT_RXCAD8P	AA19
HT_RXCAD9N	AA20
HT_RXCAD9P	AB20
HT_RXCALN	C24
HT_RXCALP	A24
HT_RXCLK0N	W25
HT_RXCLK0P	Y24
HT_RXCLK1N	W22
HT_RXCLK1P	W21
HT_RXCTLN	P25
HT_RXCTLP	P24
HT_TXCAD0N	E25
HT_TXCAD0P	E24
HT_TXCAD10N	G21
HT_TXCAD10P	G22
HT_TXCAD11N	L19
HT_TXCAD11P	L18
HT_TXCAD12N	M19
HT_TXCAD12P	M18
HT_TXCAD13N	M21
HT_TXCAD13P	M22
HT_TXCAD14N	P19
HT_TXCAD14P	P18
HT_TXCAD15N	P22
HT_TXCAD15P	P21
HT_TXCAD1N	F23
HT_TXCAD1P	E23
HT_TXCAD2N	F24
HT_TXCAD2P	F25
HT_TXCAD3N	H24

Pin Name	Ball Ref.
HT_TXCAD3P	G25
HT_TXCAD4N	K23
HT_TXCAD4P	J23
HT_TXCAD5N	K24
HT_TXCAD5P	K25
HT_TXCAD6N	M24
HT_TXCAD6P	L25
HT_TXCAD7N	N25
HT_TXCAD7P	N24
HT_TXCAD8N	F22
HT_TXCAD8P	F21
HT_TXCAD9N	J21
HT_TXCAD9P	J20
HT_TXCALN	D24
HT_TXCALP	C25
HT_TXCLK0N	J25
HT_TXCLK0P	J24
HT_TXCLK1N	L22
HT_TXCLK1P	L21
HT_TXCTLN	P23
HT_TXCTLP	N23
HTPVDD	B24
HTPVSS	B25
HTREFCLK	B23
HTTSTCLK	C23
I2C_CLK	A2
I2C_DATA	B4
LDTSTOP#	C5
LPVDD	D14
LPVSS	E14
LVDDR18D	A12
LVDDR18D	B12
LVDDR33	C12
LVDDR33	C13
LVSSR	A14
LVSSR	A16
LVSSR	C15
LVSSR	C16
LVSSR	C19
LVSSR	D12
LVSSR	F14
LVSSR	F15
NC	AA14
NC	AB14
OSCIN	B11
PCE_CALRN	AE11

Pin Name	Ball Ref.
PCE_CALRP	AD11
PLLVDD12	A11
PLLVDD18	A10
PLLVSS	B10
POWERGOOD	C11
RED	E19
RSET	B21
SB_CLKN	G2
SB_CLKP	G1
SB_RX0N	W15
SB_RX0P	W14
SB_RX1N	AA12
SB_RX1P	AB12
SB_RX2N	W12
SB_RX2P	W11
SB_RX3N	AB11
SB_RX3P	AA11
SB_TX0N	AD10
SB_TX0P	AE9
SB_TX1N	AD9
SB_TX1P	AC8
SB_TX2N	AE8
SB_TX2P	AD8
SB_TX3N	AE7
SB_TX3P	AD7
STRP_DATA	A3
SYSRESET#	C10
TESTMODE	C3
THERMALDIODE_N	AB15
THERMALDIODE_P	AA15
TMDS_HPD	C14
TVCLKIN	C2
TXCLK_LN	D15
TXCLK_LP	E15
TXCLK_UN	G15
TXCLK_UP	H15
TXOUT_L0N	B15
TXOUT_L0P	B14
TXOUT_L1N	A13
TXOUT_L1P	B13
TXOUT_L2N	G14
TXOUT_L2P	H14
TXOUT_L3N	E17
TXOUT_L3P	D17
TXOUT_U0N	B16
TXOUT_U0P	A15

Pin Name	Ball Ref.
TXOUT_U1N	C18
TXOUT_U1P	C17
TXOUT_U2N	A17
TXOUT_U2P	B17
TXOUT_U3N	B18
TXOUT_U3P	A18
VDD_18	J14
VDD_18	J15
VDD_CORE	A19
VDD_CORE	A4
VDD_CORE	A7
VDD_CORE	A9
VDD_CORE	B19
VDD_CORE	B9
VDD_CORE	C9
VDD_CORE	D20
VDD_CORE	D9
VDD_CORE	G20
VDD_CORE	H11
VDD_CORE	J11
VDD_CORE	J19
VDD_CORE	L11
VDD_CORE	L13
VDD_CORE	L15
VDD_CORE	L17
VDD_CORE	M12
VDD_CORE	M14
VDD_CORE	N11
VDD_CORE	N13
VDD_CORE	N15
VDD_CORE	P12
VDD_CORE	P14
VDD_CORE	P17
VDD_CORE	R11
VDD_CORE	R13
VDD_CORE	R15
VDD_CORE	U11
VDD_CORE	U12
VDD_CORE	U14
VDD_CORE	U15
VDD_HT	AA17
VDD_HT	AB17
VDD_HT	AB19
VDD_HT	AC18
VDD_HT	AC19
VDD_HT	AC20
VDD_HT	AD21

Pin Name	Ball Ref.
VDD_HT	AD22
VDD_HT	AD23
VDD_HT	AD24
VDD_HT	AE23
VDD_HT	AE24
VDD_HT	AE25
VDD_HT	W17
VDD_HT	Y17
VDD_HT_PKG	D22
VDD_PLL	E7
VDD_PLL	F7
VDDA_12	AB3
VDDA_12	AB4
VDDA_12	AC3
VDDA_12	AD2
VDDA_12	AE1
VDDA_12	AE2
VDDA_12	B1
VDDA_12	C1
VDDA_12	D1
VDDA_12	D2
VDDA_12	D3
VDDA_12	E2
VDDA_12	E3
VDDA_12	E6
VDDA_12	F4
VDDA_12	G7
VDDA_12	L9
VDDA_12	M9
VDDA_12	U7
VDDA_12	W7
VDDA_12_PKG	AC11
VDDA_12_PKG	M1
VDDR	AC12
VDDR	AD12
VDDR	AE12
VDDR3	D11
VDDR3	E11
VSS	A23
VSS	A25
VSS	AC14
VSS	AC15
VSS	AC16
VSS	AC22
VSS	AC23
VSS	AD25
VSS	AE14

Pin Name	Ball Ref.
VSS	AE18
VSS	AE22
VSS	B7
VSS	C4
VSS	D23
VSS	D25
VSS	D4
VSS	E9
VSS	F11
VSS	F17
VSS	G11
VSS	G23
VSS	G24
VSS	H12
VSS	H23
VSS	H25
VSS	J12
VSS	J22
VSS	L12
VSS	L14
VSS	L20
VSS	L23
VSS	L24
VSS	M11
VSS	M13
VSS	M15
VSS	M17
VSS	M20
VSS	M23
VSS	M25
VSS	N12
VSS	N14
VSS	P11
VSS	P13
VSS	P15
VSS	P20
VSS	R12
VSS	R14
VSS	R17
VSS	R20
VSS	R23
VSS	R24
VSS	T23
VSS	T25
VSS	U20
VSS	W23
VSS	W24

Pin Name	Ball Ref.
VSS	Y22
VSS	Y23
VSS	Y25
VSS_PLL	F9
VSS_PLL	G9
VSSA	A1
VSSA	AA3
VSSA	AC10
VSSA	AC2
VSSA	AC4
VSSA	AC5
VSSA	AC6
VSSA	AC7
VSSA	AC9
VSSA	AD1
VSSA	AD3
VSSA	AE10
VSSA	AE6
VSSA	F1

Pin Name	Ball Ref.
VSSA	F3
VSSA	G3
VSSA	G6
VSSA	H1
VSSA	H3
VSSA	J2
VSSA	J3
VSSA	J6
VSSA	L6
VSSA	M2
VSSA	M3
VSSA	M6
VSSA	N3
VSSA	P6
VSSA	P9
VSSA	R6
VSSA	R9
VSSA	T1
VSSA	T3

Pin Name	Ball Ref.
VSSA	U2
VSSA	U3
VSSA	U6
VSSA	V11
VSSA	V12
VSSA	V14
VSSA	V15
VSSA	W6
VSSA	Y1
VSSA	Y11
VSSA	Y12
VSSA	Y14
VSSA	Y15
VSSA	Y3
VSSA	Y9
Y	C20

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Appendix B
Revision History

Rev. 0.2 (May 2006)

- Preliminary release (Rev. 0.1 has not been released publicly).

Rev0.3 (Aug 2006)

- Added references to the RS690C.
- Added legal disclaimers concerning DVI and HDMI references in this book.
- Changed the ways in which the integrated DVI/HDMI and the TMDS interface (multiplexed on the PCI-E graphics lanes) are being referred to.
- Updated Section 1.3.9, “DVI/HDMI (Not applicable to the RS690C)”: Clarified limitation of HDCP support.
- Updated Section 1.6, “Branding Diagram”: Added branding diagrams.
- Updated Section 2.2, “DVI/HDMI (Not Applicable to the RS690C)”: Corrected data ordering of DVI/HDMI; the section now applies to both the integrate DVI/HDMI interface and the TMDS interface (multiplexed on the PCI-E graphics lanes).
- Updated Table 3-10, “Power Management Pins”: Corrected nominal voltage of POWERGOOD to 3.3V.
- Updated Table 3-19, “TMDS Interface Multiplexed on the PCI-E Graphics Interface”: Corrected mapping relationships between and PCI-E and TMDS signals.
- Updated Section 3.10, “Miscellaneous Pins”: Added description for pulse-width modulation function of the following pins: STRP_DATA, GPIO[4:2], and TMDS_HPD; added description for DDC_DATA; corrected I/O type for GPIOs.
- Updated Table 3-15, “Strap Definitions for the RS690”: Added descriptions for two Reserved straps.
- Added Section 4.1, “CPU HyperTransport Bus Timing”: Referred designers to AMD specifications.
- Updated Section 4.4, “OSCIN Timing”: Removed high and low time requirements.
- Updated Section 4.5, “Power Rail Power Up Sequence”: Added power rail power up sequence.
- Added Table 5-6, “DC Characteristics for the Integrated DVI/HDMI (Not Applicable to the RS690C).”
- Added Table 5-7, “DC Characteristics for the TMDS Interface Multiplexed on the PCI Express® Gfx Lanes.”
- Updated Section 5.2, “RS690 Thermal Characteristics.”
- Updated Section 5.3.3.1, “Stencil Opening Size for Solderball Pads on PCB”: Changed stencil opening recommendations.

Rev 0.4 (Aug 2006)

- Revised Table 3-23, “Power Pins”: Corrected ball references for VDD_PLL pins; corrected voltage level for LVDDR33.

Rev 0.5 (Sep 2006)

- Revised Section 1.3.6, “3D Acceleration Features”: Corrected maximum resolution supported to 2048x1536@32bpp for a maximum pixel clock speed of 400MHz. .
- Revised Section 1.3.9, “DVI/HDMI (Not applicable to the RS690C)”: Updated HDMI basic audio support statement.
- Updated Table 3-10, “Power Management Pins”: Corrected I/O type for ALLOW_LDTSTOP to “OD.”
- Updated Table 3-11, “Miscellaneous Pins”: Corrected I/O type for TMDS_HPD to “I/O.”
- Revised Section 4.5, “Power Rail Power Up Sequence”: Removed 1.2V PCI-E and HT rails from the sequence.

Rev 0.6 (Oct 2006)

- Updated Table 5-4, “DC Characteristics for the HTREFCLK Pad (66.66MHz)”: Revised VIH minimum to 1.4V.

Rev 3.00 (Jan 2007)

- Raised revision number to 3.00, following the AMD scheme.
- Revised H.264 support statement and moved it to Section 1.3.
- Added Section 1.3.2, “ATI HyperMemory™ Technology.”
- Updated Section 1.3.8, “Multiple Display Features”: Corrected TV modes supported.
- Added Section 1.5.2, “Branding Diagrams for ASIC Revision A12 and After.”
- Updated Section 2.2, “DVI/HDMI (Not Applicable to the RS690C)”: Reorganized the section into two subsections.
- Updated Table 5-2, “DC Characteristics for 3.3V TTL Signals”: Corrected IOL and IOH values for DACSCL and I2C_CLK.
- Updated Section 5.3.2, “Pressure Specification”: Revised statement on the maximum pressure to be applied for securing the thermal management device.
- Updated Table 3-23, “Power Pins” and Table 5-1, “Maximum and Minimum Ratings”: Clarified description for VDD_18, which also powers the DFT_GPIOs.

Rev 3.01 (Feb 2007)

- Updated Section 1.3.9, “DVI/HDMI (Not applicable to the RS690C)”: Qualified that HDCP support is for single-link transmission only; revised audio support statement.
- Updated Table 3-2, “1 x 16 Lane PCI Express Interface for External Graphics”: Corrected pin type of GFX_REFCLKP/N to input only.
- Updated Table 3-3, “1 x 4 Lane A-Link Express II Interface for Southbridge”: Corrected pin type of SB_CLKP/N to input only.
- Updated Table 3-11, “Miscellaneous Pins”: Updated description for BMREQ#.
- Updated Table 5-8, “RS690 Thermal Limits”: Revised Operating Case Temperature to 0°C minimum and 95°C maximum.

Rev 3.02 (April 2007)

- Added legal note on Macrovision in Section 1.3.8, “Multiple Display Features.”
- Added Table 5-3, “DC Characteristics for 1.8V TTL Signals.”

Rev 3.03 (April 2007)

- Updated legal notes on Macrovision and moved them to the legal notice page at the beginning of the book.

Rev 3.04 (Sep 2007)

- Updated branding diagrams for ASIC revision A12 (Section 1.5.2, “Branding Diagrams for ASIC Revision A12 and After”).
- Added support for DirectX VA 2.0 (SD contents only) (Section 1.3.7, “Motion Video Acceleration Features”).
- Updated the solder reflow profile (Section 5.3.3.2, “Reflow Profile”).
- Corrected A13 to TXOUT_L1N in Table A-1, “RS690 Pin List Sorted by Ball Reference.”