AMD 780G Family
Register Reference Guide

For RS780, RS780C, RS780D, RS780E,
RS780M, RS780MC, and RX781

Technical Reference Manual
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AMD

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Chapter 1
Introduction

1.1 About This Manual

This document is intended for BIOS engineers designing BIOSes for systems based on AMD's RS780 chipset. It describes the register reference information needed to ensure the proper functioning of the RS780 ASIC. Use this document in conjunction with the related *AMD RS780 Register Programming Requirements Guide*, and the *AMD RS780 BIOS Developer's Guide*.

Unless indicated otherwise, the programming information in this document applies to the following RS780 ASIC variants:

- RS780 (AMD 780G)
- • RS780C (AMD 780V)
- • RS780D (AMD 790GX)
- • RS780E (AMD 780E)
- • RS780M (AMD M780G)
- • RS780MC (AMD M780V)
- • RX781 (AMD M770) (Note: Registers that contain GPUF0MMReg do not apply to the RX781)

Chapter 1 outlines the notations and conventions used throughout this manual.

Chapter 2 provides detailed descriptions of the registers.

Appendix A provides several cross-referenced lists of the registers (sorted by register name and address).

Changes and additions from the previous release of this document are highlighted in red. Refer to *Appendix B: Revision History* at the end of this manual for a detailed revision history.

1.2 Nomenclature and Conventions

1.2.1 Numeric Representations

- Hexadecimal numbers are appended with "h" whenever there is a risk of ambiguity. Other numbers are assumed to be in decimal.
- Registers (or fields) of identical function are sometimes indicated by a single expression in which the part of the signal name that differs is enclosed in [ ] brackets. For example, the eight Host Data registers — HOST_DATA0 through to HOST_DATA7 — are represented by the single expression HOST_DATA[7:0].
- Series of numbers appearing in similar addresses are sometimes enclosed in [ ] brackets. For example, PCIE_HDR_LOGO exists for PCI-E device 2 to 8, and the registers' addresses are expressed collectively as pcieConfig [2:8]\:0x11C.

1.2.2 Register Description

All registers in this document are described with the format of the sample table below. All offsets are in hexadecimal notation, while programmed bits are in either binomial or hexadecimal notation.

Table 1-1 Register Description Table Notation—Example

DST_HEIGHT_WIDTH_8 - W - 32 bits - [MMReg:0x158C]			
Field Name	**Bits**	**Default**	**Description**
DST_WIDTH *(mirror bits 7:0 of DST_WIDTH:DST_WIDTH)*	23:16	0x0	Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete
DST_HEIGHT *(mirror bits 7:0 of DST_HEIGHT:DST_HEIGHT)*	31:24	0x0	Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT
[W] (Reserved) 15: 0 DST_WIDTH 23: 16 Destination width: range 0 to 256 (ZERO extent)			

Register Information	Example
Register name	DST_HEIGHT_WIDTH_8
Read / Write capability R = Readable W = Writable RW = Readable and Writable	W
Register size	32 bits
Register address(es)*	MMReg:0x158C
Field name	DST_WIDTH
Field position/size	23:16
Field default value	0x0
Field description	Destination....complete
Field mirror information	*(mirror bits 7:0 of DST_WIDTH:DST_WIDTH)*
Brief register description	[W] (Reserved) 15: 0 DST_WIDTH 23: 16 Destination width: range 0 to 256 (ZERO extent)
*** Note:** There maybe more than one address; the convention used is as follows: **[aperName:offset]** - single mapping, to one aperture/decode and one offset **[aperName1, aperName2, …, aperNameN:offset]** - multiple mappings to different apertures/decodes but same offset **[aperName:startOffset-endOffset]** - mapped to an offset range in the same aperture/decode	

Warning: Do not attempt to modify the values of registers or bit fields that are marked as "Reserved." Doing so may cause the system to behave in unexpected ways.

Chapter 2
Register Descriptions

2.1 Northbridge Configuration Registers

PCI Bus 0 - Device 0 Registers

NB_VENDOR_ID - R - 16 bits - nbconfig:0x0			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID	15:0	0x1022	Vendor Identifier This 16-bit field identifies the manufacturer of the device: Advanced Micro Devices, Inc.

NB_DEVICE_ID - R - 16 bits - nbconfig:0x2			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x9600	Device Identifier This 16-bit field is assigned by the device manufacturer and identifies the type of device. The current northbridge Device ID assignment is 0x5956. The host bridge alternate device ID is 0x5957 or 0x5958 (selected by the e-fuse configuration bit).

NB_COMMAND - RW - 16 bits - nbconfig:0x4			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN (R)	0	0x0	I/O Access Enable This bit is always 0 because the RS780 does not respond to I/O cycles on the PCI Bus. 0=Disable 1=Enable
MEM_ACCESS_EN	1	0x0	Memory Access Enable Controls weather PCI memory accesses to system memory are accepted 0=Disable 1=Enable
BUS_MASTER_EN (R)	2	0x1	Bus Master Enable This bit is always set, indicating that the RS780 is allowed to act as a bus master on the PCI Bus. 0=Disable 1=Enable
SPECIAL_CYCLE_EN (R)	3	0x0	Special Cycle This bit is always 0 because the RS780 ignores PCI special cycles. 0=Disable 1=Enable

MEM_WRITE_INVALIDATE_EN (R)	4	0x0	Memory Write and Invalidate Enable This bit is always 0 because the RS780 does not generate memory write and invalidate commands. 0=Disable 1=Enable
PAL_SNOOP_EN (R)	5	0x0	VGA Palette Snoop Enable This bit is always 0 indicating that the RS780 does not snoop the VGA palette address range. 0=Disable 1=Enable
PARITY_ERROR_EN (R)	6	0x0	Parity Error Response This bit is always 0 because the RS780 does not report data parity errors. 0=Disable 1=Enable
Reserved0 (R)	7	0x0	This bit is reserved in PCI 2.3. It is hardwired to 0. 0=Disable 1=Enable
SERR_EN	8	0x0	System Error Enable Controls the assertion of SERR# 0=Disable 1=Enable
FAST_B2B_EN	9	0x0	Fast Back-to-Back to Different Devices Enable This bit is always 0 because the RS780 does not allow generation of fast back-to-back transactions to different agents. 0=Disable 1=Enable
Reserved (R)	15:10	0x0	

NB_STATUS - RW - 16 bits - nbconfig:0x6			
Field Name	**Bits**	**Default**	**Description**
CAP_LIST (R)	4	0x1	Capabilities List This bit is set to indicate that this device's configuration space supports a capabilities list.
PCI_66_EN (R)	5	0x1	66-MHz Capable Indicate that the RS780 supports 66 MHz PCI operation
Reserved (R)	6	0x0	
FAST_BACK_CAPABLE (R)	7	0x0	Fast Back-to-Back Capable This bit is always 0 indicating that the RS780, as a target, is not capable of accepting fast back-to-back transactions when the transactions are not to the same agent.
DEVSEL_TIMING (R)	10:9	0x1	DEVSEL# Timing This bit field defines the timing of DEVSEL# on the RS780. The device only supports medium DEVSEL# timing.
SIGNAL_TARGET_ABORT (R)	11	0x0	Signaled Target Abort This bit is always 0 because the RS780 does not terminate transactions with target aborts. 0=No Abort 1=Target Abort asserted
RECEIVED_TARGET_ABORT	12	0x0	Received Target Abort This bit is set by whenever a CPU to PCI transaction (except for a special cycle) is terminated due to a target-abort. This bit is cleared by writing a 1. 0=Inactive 1=Active

RECEIVED_MASTER_ABORT	13	0x0	Received Master Abort This bit is set whenever a CPU to PCI transaction (except for a special cycle) is terminated due to a master-abort. This bit is cleared by writing a 1. 0=Inactive 1=Active
SIGNALED_SYSTEM_ERROR	14	0x0	Signaled System Error This bit is set whenever the RS780 generates a System Error and asserts the SERR# line (currently only GART Error). This bit is cleared by writing a 1. 0=No Error 1=SERR asserted
PARITY_ERROR_DETECTED (R)	15	0x0	Detected Parity Error This bit is always 0 because the RS780 does not support data parity checking.
General NB status Flags			

NB_REVISION_ID - R - 8 bits - nbconfig:0x8

Field Name	Bits	Default	Description
MINOR_REV_ID	3:0	0x0	Identifies the stepping number of the device
MAJOR_REV_ID	7:4	0x0	Identifies the revision number of the device
Revision Identification			

NB_REGPROG_INF - R - 8 bits - nbconfig:0x9

Field Name	Bits	Default	Description
REG_LEVEL_PROG_INF	7:0	0x0	Indicates a Host bridge.
Program Interface			

NB_SUB_CLASS - R - 8 bits - nbconfig:0xA

Field Name	Bits	Default	Description
SUB_CLASS_INF	7	0x0	Indicates a Host bridge
Sub-Class Code			

NB_BASE_CODE - R - 8 bits - nbconfig:0xB

Field Name	Bits	Default	Description
BASE_CLASS_CODE	7:0	0x6	Indicates a Bridge device
Class Code			

NB_CACHE_LINE - R - 8 bits - nbconfig:0xC

Field Name	Bits	Default	Description
CACHE_LINE_SIZE	7:0	0x0	
Cache Line Size			

NB_LATENCY - RW - 8 bits - nbconfig:0xD			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER	7:0	0x0	This bit field defines the minimum amount of time, in PCI clock cycles, that the bus master can retain ownership of the bus. This is mandatory for masters that are capable of performing a burst consisting of more than two data phases
Latency Timer			

NB_HEADER - R - 8 bits - nbconfig:0xE			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE	6:0	0x0	Bits [6:5] are 0, indicating that Type 00 Configuration Space Header format is supported.
DEVICE_TYPE	7	0x0	Bit [7] is always 0, indicating that the RS780's northbridge block is a single function device 0=Single-Function Device 1=Multi-Function Device
Header Type			

NB_BIST - R - 8 bits - nbconfig:0xF			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP	3:0	0x0	
BIST_STRT	6	0x0	
BIST_CAP	7	0x0	
Built-in-self-test			

NB_HT3_Power_management_Capability - RW - 32 bits - nbconfig:0xF8			
Field Name	**Bits**	**Default**	**Description**
Capability_ID (R)	7:0	0x8	
Capability_Pointer (R)	15:8	0x0	
Reg_Ind	19:16	0x0	
Reserved_26_20 (R)	26:20	0x0	
Capability_TYPE (R)	31:27	0x1c	

NB_HT3_Power_management_data_port - RW - 32 bits - nbconfig:0xFC			
Field Name	**Bits**	**Default**	**Description**
CDL_0 (R)	0	0x0	
CDL_1 (R)	1	0x0	
CDL_2 (R)	2	0x0	
CDL_3 (R)	3	0x0	
CDL_4 (R)	4	0x0	
CDL_5 (R)	5	0x0	
CDL_15_6 (R)	15:6	0x0	
CDL_16	16	0x0	
CDL_17	17	0x0	

CDL_18	18	0x0	
CDL_19	19	0x0	
CDL_20	20	0x0	
CDL_21	21	0x0	
spare_31_22 (R)	31:22	0x0	

NB_BAR1_RCRB - RW - 32 bits - nbconfig:0x14

Field Name	Bits	Default	Description
MEM_IO (R)	0	0x0	Memory This bit is hardwired to 0 to indicate that this base address register maps into memory space 0=Memory 1=I/O
_TYPE (R)	2:1	0x0	
PREFETCH_EN (R)	3	0x0	Unprefetchable This bit is hardwired to 0 to indicate that this range is un-prefetchable
RCRB_BASE	31:12	0x0	Base Address High[31:12] This filed is used to define a 4K memory mapped root complex register block
Descriptor for memory mapped RCRB registers			

NB_BAR2_PM2 - RW - 32 bits - nbconfig:0x18

Field Name	Bits	Default	Description
MEM_IO (R)	0	0x1	I/O Space This bit is hardwired to 1 to indicate that this base address register maps into x86 I/O space. 0=Memory 1=I/O
RESERVED (R)	1	0x0	
PM2_BASE_LOW (R)	4:2	0x0	This field specifies that there are 8 DWORD registers allocated to this space.
PM2_BASE	31:5	0x0	PM2_BLK Base This bit field forms the upper part of BAR2. This field is loaded by the BIOS software and specifies the base of PM2_BLK.
Descriptor for Power management PM2 Control Block			

NB_BAR3_PCIEXP_MMCFG - RW - 32 bits - nbconfig:0x1C

Field Name	Bits	Default	Description
MEM_IO (R)	0	0x0	Memory This bit is hardwired to 0 to indicate that this base address register maps into memory space 0=Memory 1=I/O
_TYPE (R)	2:1	0x2	
PREFETCH_EN (R)	3	0x0	Prefetchable This bit is hardwired to 1 to indicate that this range is prefetchable

MEM_BASE_LOW (R)	20:4	0x0	Base Address Low This bit field is hardwired to return zeros to indicate that xx Kbytes are allocated to PCI Express Configuration Registers.
MEM_BASE_HIGH	31:21	0x0	Base Address High This bit field forms the upper part of BAR3. This field is loaded by the BIOS software
Descriptor for memory mapped PCI Express Configuration registers			

NB_BAR3_UPPER_PCIEXP_MMCFG - RW - 32 bits - nbconfig:0x20			
Field Name	**Bits**	**Default**	**Description**
MEM_BASE_UPPER	31:0	0x0	Upper 32 bit of BAR3 base address
Descriptor for upper part of memory mapped PCI Express Configuration registers			

NB_ADAPTER_ID - R - 32 bits - nbconfig:0x2C			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID *(mirror of NB_ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)*	15:0	0x0	
SUBSYSTEM_ID *(mirror of NB_ADAPTER_ID_W:SUBSYSTEM_ID)*	31:16	0x0	
Subsystem Vendor ID and Subsystem ID register			

NB_CAPABILITIES_PTR - R - 32 bits - nbconfig:0x34			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR	7:0	0xc4	This field contains a byte offset into a device's configuration space containing the first item in the capabilities list. If no next item exists, then it is set to null.
Capabilities Pointer			

NB_PCI_CTRL - RW - 32 bits - nbconfig:0x4C			
Field Name	**Bits**	**Default**	**Description**
FUNCTION_1_ENABLE	0	0x0	Enables access to Bus0Dev0Fun1 0=Disable 1=Enable
APIC_ENABLE	1	0x1	Not used 0=Disable 1=Enable
AlwaysUnLk	2	0x1	If set, always issues UnLk request for CPU lock transaction. If not set, only issues UnLk when RdLk is successful 0=Disable 1=Enable

Cf8Dis	3	0x0	Disables IO 0xCF8 cycle to nbcfg block 0=Enable 1=Disable
PMEDis	4	0x0	Disables PME message generation 0=Enable 1=Disable
SErrDis	5	0x0	Disables SErr message generation 0=Enable 1=Disable
BMMsgEn	6	0x0	Enables BM_Set message generation 0=Disable 1=Enable
DisLockP2P	7	0x0	If set, p2p could sneak into MemRdLk sequence. If not set, blocks p2p during CPU lock transactions 0=Enable 1=Disable
PMArbDisSel	10:8	0x0	Setting bit [0] will disable BIF request when PMArbDis is set. Setting bit [1] will disable rx0(graphics pcie) DMA request when PMArbDis is set. Setting bit [2] will disable rx1(SB and general purpose pcie) DMA request when PMArbDis is set.
CsrStatus	11	0x0	1 means CSR is detected. Write 1 to clear this bit. Writing 0 has no effect 0=Inactive 1=Active
CfgRdTime	14:12	0x2	3-bit setting for RBBM read data bus data latch latency
P2PDynamicClkOff	15	0x0	If set to 1, dynamic clock has to be turned off in order to support p2p traffic 0=Enable 1=Disable
WakeC2En	16	0x0	1 means enable Wake_from_C2 message. 0 means disable 0=Enable 1=Disable
BAR2_PM2Enable	17	0x0	Enables read/write access to NB_BAR2_PM2 register. Clearing this bit could hide BAR2. 0=Disable 1=Enable
P4IntEnable	18	0x0	Enables NB to accept A4 interrupt request from SB 0=Disable 1=Enable
SLPEnable	20	0x0	Enables SLP logic in NB 0=Enable 1=Disable
SLP_Pad_Enable	21	0x0	Enables SLP# pad output 0=Enable 1=Disable
BAR1_Enable	22	0x0	Enables read/write access to NB_BAR1_RCRB register. Clearing this bit could hide BAR1 0=Enable 1=Disable
MMIOEnable	23	0x0	Enables MMIO decoding 0=Enable 1=Disable
IsocArbMode	24	0x0	If set, it checks the IOCIsocArbiter setting for arbitration. If not set, it checks IsocHiPr for priority. 0=Enable 1=Disable
IsocHiPr	25	0x0	If set, isoc has high priority. If not set, the regular channel has high priority 0=Enable 1=Disable

HPDis	26	0x0	Disables HP message generation 0=Enable 1=Disable
PCI Control Register			

NB_ADAPTER_ID_W - RW - 32 bits - nbconfig:0x50			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x1022	
SUBSYSTEM_ID	31:16	0x9600	
Subsystem Vendor ID and Subsystem ID write register			

NB_UNITID_CLUMPING_CAPABILITY - R - 32 bits - nbconfig:0x54			
Field Name	**Bits**	**Default**	**Description**
CAPABILITY_ID	7:0	0x8	Indicates this has Hypertransport capability
CAPABILITY_POINTER	15:8	0x40	Pointer to the next configuration space capability
RESERVED	26:16	0x0	Reserved for future use. This register controls no hardware
CAPABILITY_TYPE	31:27	0x12	Indicate this has UnitID Clumping capability

NB_UNITID_CLUMPING_SUPPORT - R - 32 bits - nbconfig:0x58			
Field Name	**Bits**	**Default**	**Description**
RESERVED_0	0	0x0	Reserved for future use. This register controls no hardware
SUPPORT	31:1	0x0	Indicates which on-board UnitIDs support the clumping capability

NB_UNITID_CLUMPING_ENABLE - RW - 32 bits - nbconfig:0x5C			
Field Name	**Bits**	**Default**	**Description**
RESERVED_0 (R)	0	0x0	Reserved for future use. This register controls no hardware
ENABLE	31:1	0x0	Enables clumping for selected UnitIDs. See the *AMD RS780 Register Programming Requirements* document on how to enable this feature.

NB_HT_ERROR_RETRY_CAPABILITY - R - 32 bits - nbconfig:0x40			
Field Name	**Bits**	**Default**	**Description**
CAPABILITY_ID	7:0	0x8	This indicates this has Hypertransport capability
CAPABILITY_POINTER	15:8	0x9c	Pointer to the next configuration space capability
RESERVED	26:16	0x0	Reserved for future use. This register controls no hardware
CAPABILITY_TYPE	31:27	0x18	Indicate this has Error Retry capability

NB_HT_ERROR_RETRY_CONTROL_STATUS - RW - 32 bits - nbconfig:0x44			
Field Name	**Bits**	**Default**	**Description**
LINK_RETRY_EN_0	0	0x0	Enables Error Retry Mode. This register requires a warm-reset to take effect
FORCE_SINGLE_ERROR_0	1	0x0	Forces an upstream error on the Hypertransport link. This register is automatically cleared by hardware
ROLLOVER_NONF_EN_0 (R)	2	0x0	Reserved for future use. This register controls no hardware
FORCE_SINGLE_STOMP_0	3	0x0	Forces an upstream stomp packet on the Hypertransport link. This register is automatically cleared by hardware
RETRY_NONF_EN_0 (R)	4	0x0	Reserved for future use. This register controls no hardware
RETRY_FATAL_EN_0 (R)	5	0x0	Reserved for future use. This register controls no hardware
ALLOWED_ATTEMPTS_0	7:6	0x3	Indicates the number of short training attempts to make before attempting full training.
RETRY_SENT_0	8	0x0	Indicates the link sent a disconnect Nop to initiate a retry sequence. Write 1 to clear
COUNT_ROLLOVER_0	9	0x0	Indicates the retry counter has rolled over. Write 1 to clear
STOMP_RECEIVED_0	10	0x0	Indicates that a stomp packet has been received. Write 1 to clear
RESERVED_15_11 (R)	15:11	0x0	Reserved for future use. This register controls no hardware
reserved_23_16 (R)	23:16	0x0	Reserved for future use. This register controls no hardware
reserved_31_24 (R)	31:24	0x0	Reserved for future use. This register controls no hardware

NB_HT_ERROR_RETRY_COUNT - RW - 32 bits - nbconfig:0x48			
Field Name	**Bits**	**Default**	**Description**
RETRY_COUNT_0	15:0	0x0	Indicates the number of retry sequences the hardware has made
reserved_31_16 (R)	31:16	0x0	Reserved for future use. This register controls no hardware

NB_HT3_CAPABILITY - RW - 32 bits - nbconfig:0x9C			
Field Name	**Bits**	**Default**	**Description**
CAPABILITY_ID (R)	7:0	0x8	Indicates this has Hypertransport capability
CAPABILITY_POINTER (R)	15:8	0xf8	Pointer to the next configuration space capability
REG_IND	17:16	0x0	Index 00=Gen3 Configuration Registers 01=Receiver BIST Registers 10=Transmitter BIST Registers
UCC (R)	18	0x0	1 indicates support for unthrottled commands
BIST_CAP (R)	19	0x0	1 indicates support for the BIST feature
CPIC (R)	20	0x0	1 indicates support for the command packet insertion feature
LS3C (R)	21	0x0	1 indicates support for the LS3 low-power link state
SLCC (R)	22	0x0	
RESERVED (R)	23	0x0	Reserved for future use
CAPABILITY_TYPE (R)	31:24	0xd0	Indicates this has Hypertransport 3 capability

NB_HT3_GLOBAL_LINK_TRAIN - RW - 32 bits - nbconfig:0xA0			
Field Name	**Bits**	**Default**	**Description**
T0_TIME	5:0	0x3a	Defines the amount of time spent in the Training 0 state after recovering from LDTSTOP. See the Hypertransport 3 specification for the encoding
reserved_7_6 (R)	7:6	0x0	
CONNDLY	8	0x0	Connect Delay. Delays the effects of TXOFF until LDTSTOP or Warm Reset
RXCALEE	9	0x0	This register controls no hardware
RETRYFORCE	11:10	0x0	Retry Force 00=No forced retries 01=Force retry every 250us 10=Force retry every 500us 11=Force retry every 1ms
reserved_12 (R)	12	0x0	Reserved for future use. This register controls no hardware
RSV_16_13	16:13	0x0	
FullT0Time	22:17	0x3a	
RSV_31_23	31:23	0x0	

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_GLOBAL_LINK_TRAIN and the fields are as listed in the above table.

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Pattern_control:

FieldName	Bits	Default
Order	2:0	0x0
PatCnt	9:3	0X0
ModSel	12:10	0X0
ModCnt	19:13	0X0
ConstSel	20	0X0
ConstCnt	25:21	0X0
Reserved (Access R)	31:26	0X0

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Pattern_control:

FieldName	Bits	Default
Order	2:0	0x0
PatCnt	9:3	0x0
ModSel	12:10	0x0
ModCnt	19:13	0x0
ConstSel	20	0x0
ConstCnt	25:21	0x0
Reserved (Access R)	31:26	0x0

NB_HT3_LINK_TRANSMITTER_CONF_0 - RW - 32 bits - nbconfig:0xA4			
Field Name	**Bits**	**Default**	**Description**
DP1	4:0	0x0	Reserved for future use. This register controls no hardware
reserved_12_5	12:5	0x0	Reserved for future use. This register controls no hardware
COMPLIANCE	15:13	0x0	DC Compliance Test 000=Normal Operation 001=Send TxHiZ 010=Send TxL0 Logic 0 011=Send TxL1 Logic 1 100=Reserved 101=Send TxIdle 110=Reserved 111=Reserved
MARGIN_LEVEL	18:16	0x0	Sets transmitter attenuation level. 0 means no attenuation
rsv_20_19 (R)	20:19	0x0	Reserved for future use. This register controls no hardware
RSV_23_21	23:21	0x0	Reserved for future use. This register controls no hardware
DL1	26:24	0x5	Sets transmitter deemphasis level
rsv_28_27 (R)	28:27	0x0	Reserved for future use. This register controls no hardware
RSV_29 (R)	29	0x0	Reserved for future use. This register controls no hardware
PREEN	30	0x0	Reserved for future use. This register controls no hardware
DEEMPEN	31	0x0	Enables transmitter post-cursor deemphasis

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_TRANSMITTER_CONF_0 and the fields are as listed in the above table.

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Pattern_Buffer_1:

FieldName	Bits	Default
Pattern_1	23:0	0x0
Reserved (Access R)	31:24	0x0

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Pattern_Buffer_1:

FieldName	Bits	Default
Pattern_1	23:0	0x0
Reserved (Access R)	31:24	0x0

NB_HT3_LINK_RECEIVER_CONF_0 - RW - 32 bits - nbconfig:0xA8			
Field Name	**Bits**	**Default**	**Description**
COMPLIANCE	1:0	0x0	Receiver Compliance 00=Normal Operation 01=Reserved 10=RxOff 11=Reserved
RESERVED_7_2 (R)	7:2	0x0	Reserved for future use. This register controls no hardware
EQLvL (R)	9:8	0x0	Reserved for future use. This register controls no hardware
RESERVED_14_10	14:10	0x0	Reserved for future use. This register controls no hardware
EQEn (R)	15	0x0	Reserved for future use. This register controls no hardware
MGNINDX	19:16	0x0	Sets time-margining level
rsv_22_20 (R)	22:20	0x0	Reserved for future use. This register controls no hardware
RESERVED_29_23 (R)	29:23	0x0	Reserved for future use. This register controls no hardware
MGNDIR	30	0x0	Controls no hardware. Margining is applied equally to both sides of the data eye
MGNEN	31	0x0	Enables time-margining

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_RECEIVER_CONF_0 and the fields are as listed in the above table.

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Mask:

FieldName	Bits	Default
CTL_CAD	17:0	0x3FFFF
Reserved (Access R)	31:18	0x0

When REG_IND of reg NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Mask:

FieldName	Bits	Default
CTL_CAD	17:0	0x3FFFF
Reserved (Access R)	31:18	0x0

NB_HT3_LINK_TRAINING_0 - RW - 32 bits - nbconfig:0xAC			
Field Name	**Bits**	**Default**	**Description**
GANGED (R)	0	0x1	Read-only 1. This device only support ganged operation
AC (R)	1	0x0	Read-only 0. This device does not support AC-coupled mode
EIGHT_TO_TEN_BIT_EN (R)	2	0x0	Read-only 0. This device does not support 8b/10b coding
SCREN	3	0x0	Enables Scrambler
TOTALATTEMPT	6:4	0x7	Total Attempts. Defines the number of long retry attempts made during failed training sequences
LSSel	8:7	0x0	LS Select 00=LS1 - CLK running. CAD/CTL sending TxIdle 01=Reserved 10=LS2 - CLK/CAD/CTL sending TxIdle 11=LS3 - CLK/CAD/CTL sending either HiZ or TxGndTrm
HotPlugEn (R)	9	0x0	Read-only 0. This device does not support hot-plugging
BISTEn	10	0x0	Built-in Self-Test Enable
ILMEn	11	0x0	Internal Loopback Mode Enable
LaneSel	13:12	0x0	Lane Select. Refer to the Hypertransport 3 specification for details regarding this register
DISCMDTHRT	14	0x0	Disables Command Throttling
RESERVED_15 (R)	15	0x0	Reserved for future use. This register controls no hardware
SerLane	19:16	0x0	Serial Lane Select. Refer to the Hypertransport 3 specification for details regarding this register
CPIEn	20	0x0	Reserved for future use. This register controls no hardware
TxLSSel	22:21	0x0	
RxInLnSt	24:23	0x0	
TxInLnSt	26:25	0x0	
LS1D	27	0x0	
reserved_31_28	31:28	0x0	

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_TRAINING_0 and the fields are as listed in the above table.

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Inversion:

FieldName	Bits	Default
Inversion	17:0	0x0
Reserved (Access R)	31:18	0x0

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Inversion:

FieldName	Bits	Default
Inversion	17:0	0x0
Reserved (Access R)	31:18	0x0

NB_HT3_RESERVED - RW - 32 bits - nbconfig:0xB0			
Field Name	**Bits**	**Default**	**Description**
RESERVED_31_0	31:0	0x0	Reserved when REG_IND = 00. This register controls no hardware

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_RESERVED and the fields are as listed in the above table.

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Pattern_Buffer_2:

FieldName	Bits	Default
Pattern_2	23:0	0x0
Reserved (Access R)	31:24	0x0

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Pattern_Buffer_2:

FieldName	Bits	Default
Pattern_2	23:0	0x0
Reserved (Access R)	31:24	0x0

NB_HT3_LINK_TRANSMITTER_CONF_1 - RW - 32 bits - nbconfig:0xB4			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	Reserved when REG_IND = 00. This register controls no hardware

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_TRANSMITTER_CONF_1 and the fields are as listed in the above table.

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Pattern_Buffer_2_Select :

FieldName	Bits	Default
Pattern_Buffer_2_Enable	17:0	0x0

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Pattern_Buffer_2_Select:

FieldName	Bits	Default
Pattern_Buffer_2_Enable	17:0	0x0

NB_HT3_LINK_RECEIVER_CONF_1 - RW - 32 bits - nbconfig:0xB8			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	Reserved when REG_IND = 00. This register controls no hardware

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_RECEIVER_CONF_1 and the fields are as listed in the above table.

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Pattern_Buffer_Extension:

FieldName	Bits	Default
Pattern_Buffer_1	15:0	0x0
Pattern_Buffer_2	31:16	0x0

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Pattern_Buffer_Extension:

FieldName	Bits	Default
Pattern_Buffer_1	15:0	0x0
Pattern_Buffer_2	31:16	0x0

NB_HT3_LINK_TRAINING_1 - RW - 32 bits - nbconfig:0xBC			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	Reserved when REG_IND = 00. This register controls no hardware

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_LINK_TRAINING_1 and the fields are as listed in the above table.

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Scramble:

FieldName	Bits	Default
Scramble	17:0	0x0
Reserved (Access R)	31:18	0x0

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Transmitter_Scramble:

FieldName	Bits	Default
Scramble	17:0	0x0
Reserved (Access R)	31:18	0x0

NB_HT3_BIST_CONTROL - RW - 32 bits - nbconfig:0xC0			
Field Name	**Bits**	**Default**	**Description**
RSV_0 (R)	0	0x0	Reserved for future use. This register controls no hardware
RxDis	1	0x0	Receiver Disable. The transmitter will advance using the minimal number of training sequences. Receiver BIST checking is disabled.
RESERVED_4_2 (R)	4:2	0x0	Reserved for future use. This register controls no hardware
INVROTEN	5	0x0	Enables Inversion Rotate
ERRSTAT	7:6	0x0	Error Status 00=No Error 01=Training Error 10=Pattern Miscompare 11=Reserved
ERRLNNUM	12:8	0x0	Error Lane Number. Indicates the lane number where the first error was detectetd
RESERVED_15_13 (R)	15:13	0x0	Reserved for future use. This register controls no hardware
ERRCNT	26:16	0x0	Error Count. Indicates the number of errors detected during BIST operation
RESERVED_30_27 (R)	30:27	0x0	Reserved for future use. This register controls no hardware
width (R)	31	0x0	Read-only 1. Indicates the on-board BIST engine is 16-bits wide

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b00, the register name is NB_HT3_BIST_CONTROL and the fields are as listed in the above table.

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b01, the register name and fields are defined as follows:

NB_HT3_Receiver_Error:

FieldName	Bits	Default
Receiver_error	17:0	0x0
Reserved (Access R)	31:18	0x0

When REG_IND of register NB_HT3_CAPABILITY are set to 2'b10, the register name and fields are defined as follows:

NB_HT3_Reserved:

FieldName	Bits	Default
Reserved (Access R)	31:0	0x0

NB_FDHC - RW - 8 bits - nbconfig:0x68			
Field Name	**Bits**	**Default**	**Description**
MEM_HOLE_ENABLE	7:6	0x0	Hole Enable 00=No hole 01=Hole at 512KB - 640KB 10=Hole at 15MB - 16MB 11=Reserved

Fixed SDRAM Hole Control required for Slot-1 operation.

NB_SMRAM - RW - 8 bits - nbconfig:0x69			
Field Name	**Bits**	**Default**	**Description**
SMM_LOCATION	2:0	0x2	0x2: SMM space at 640KB-768KB. Any other encoding disables this area.
GLOBAL_SMRAM_ENABLE	3	0x0	SMM Space globally enabled Once the MM_SPACE_LOCKED bit is set, this cannot be changed until after reset. 0=Disable 1=Enable
SMM_SPACE_LOCKED	4	0x0	SMM Space Locked If set, SMM_LOCATION cannot be changed until after reset. It can only be written once. 0=Unlocked 1=Locked
SMM_SPACE_OPEN	6:5	0x0	SMM Space Opened/Closed Once the SMM_SPACE_LOCKED bit is set, bit [6] cannot be changed until after reset. 0=Open for CPU transactions to SMM memory 1=Closed 2=Open 3=Reserved
System Management RAM configuration. This Register is only used in Slot-1 interface mode.			

NB_EXSMRAM - RW - 8 bits - nbconfig:0x6A			
Field Name	**Bits**	**Default**	**Description**
TSEG_ENABLE	0	0x0	Enables TSEG space. Two possible locations (based on HI_SMRAM_ENABLE): (TOM-TSEG_SIZE) - TOM or (256MB+TOM-TSEG_SIZE) - (256MB+TOM) 0=Disable 1=Enable
TSEG_SIZE	2:1	0x0	0=2MB 1=8MB 2=512KB 3=1MB
Reserved0	5	0x1	Reserved for future use.
EX_SMRAM_ERROR	6	0x0	This bit is set if an access is attempted while the extended SMM area is disabled
HI_SMRAM_ENABLE	7	0x0	Enable high SMM/TSEG space. For SMM: (256MB+640KB) - (256MB+1MB). Maps to (640KB - 1MB). For TSEG: (256MB+TOM-TSEG_SIZE) - (256MB+TOM). Maps to (TOM-TSEG_SIZE) - TOM. 0=Disable 1=Enable
Extended System Management RAM control register. This register controls access to the extended SMM range in system memory. It is only used in Slot-1 interface mode.			

NB_PMCR - RW - 8 bits - nbconfig:0x6B			
Field Name	**Bits**	**Default**	**Description**
ACPI_CTL_REG_EN (R)	0	0x0	Always forced to 0 0=Disable 1=Enable
Power Management Control			

NB_STRAP_READ_BACK - RW - 32 bits - nbconfig:0x6C			
Field Name	**Bits**	**Default**	**Description**
DISABLE_EFUSE_PGM (R)	0	0x0	
DEVICE_ID (R)	1	0x0	
MOBILE_GFX (R)	2	0x0	
MACROVISION_DISABLE (R)	3	0x0	
EFUSE_DISP_KEYS_VALID (R)	4	0x0	
AUDIO_DISABLE (R)	5	0x0	
HW_EFUSE_select	6	0x0	
STRAP_SIDE_PORT_ENb	7	0x0	
strap_debug_bus_enb (R)	8	0x0	
spare_9 (R)	9	0x0	
spare_10 (R)	10	0x0	
spare_11_13 (R)	13:11	0x0	
CF_DISABLE (R)	14	0x0	
product_test (R)	15	0x0	0=Short Timers for Production Test 1=Normal Operation
DisableHT3Capability (R)	16	0x0	
DisableHT1200Capability (R)	17	0x0	
DisableHT1400Capability (R)	18	0x0	
DisableHT1600Capability (R)	19	0x0	
DisableHT1800Capability (R)	20	0x0	
DisableHT2000Capability (R)	21	0x0	
DisableHT2200Capability (R)	22	0x0	
DisableHT2400Capability (R)	23	0x0	
DisableHT2600Capability (R)	24	0x0	
DisableCLMC (R)	25	0x0	
spare_31_26 (R)	31:26	0x20	
Strap Read Back Register			

SCRATCH_NBCFG - RW - 32 bits - nbconfig:0x78			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	All bits in this register can be written to, and read from, but it does not control anything.
This register is used for scratch reading and writing			

NB_HT_TRANS_COMP_CNTL - RW - 32 bits - HTIUNBIND:0x1			
Field Name	**Bits**	**Default**	**Description**
TXP_COMPDATA	4:0	0xc	Calculates the compensation value for the transmitter falling edge
TXP_CTL	6:5	0x0	Transmitter falling edge PHY control value 00=Apply TXP_CALCCOMP directly 01=Apply TXP_COMPDATA directly 10=Apply the sum of TXP_CALCCOMP and TXP_COMPDATA 11=Apply the diff of TXP_CALCCOMP and TXP_COMPDATA
TXP_CALCCOMP (R)	12:8	0xc	Transmitter falling edge compensation circuitry data value
RESERVED_15_13	15:13	0x0	Bit [15]=CfgHTiu_HT_EMP_EN_TST Bit [14]=CfgHTiu_HT_TX_COMPOVR Bit [13]=CfgHTiu_HT_TX_FCOMPCYC
TXN_COMPDATA	20:16	0xc	Transmitter falling edge compensation circuitry data value
TXN_CTL	22:21	0x0	Transmitter falling edge PHY control value 00=Apply TXN_CALCCOMP directly 01=Apply TXN_COMPDATA directly 10=Apply the sum of TXN_CALCCOMP and TXN_COMPDATA 11=Apply the diff of TXN_CALCCOMP and TXN_COMPDATA
TXN_CALCCOMP (R)	28:24	0xc	Calculates the compensation value for the transmitter falling edge
RESERVED_31to29	31:29	0x0	Bits [31:30]=CfgHTiu_HT_TST Bit [29]=CfgHTiu_HT_EMP_EN
HT transmitter comp control			

NB_IOC_CFG_CNTL - RW - 32 bits - nbconfig:0x7C			
Field Name	**Bits**	**Default**	**Description**
FORCE_INTGFX_DISABLE	0	0x0	Forces the pin strap to disable, regardless of the actual state of the pin (DACHSYNC). This will disable the apc bridge access if present. 0=Normal 1=Disable
CFG_Q_F1000_800	1	0x0	0=Disable 1=Enable
F1000_800_en	2	0x0	0=Disable 1=Enable
spare_27_3	27:3	0x0	
PcieMemCfg_Select	28	0x0	0=Disable 1=Enable
NB_BAR3_PCIEXP_REG_RDEN	29	0x1	0=Disable 1=Enable
NB_BAR3_PCIEXP_REG_WREN	30	0x0	Enables writes to the BAR3 register 0=Disable 1=Enable
IOC CFG control register			

NB_HT_CLK_CNTL_RECEIVER_COMP_CNTL - RW - 32 bits - HTIUNBIND:0x0			
Field Name	**Bits**	**Default**	**Description**
RX_COMPDATA	4:0	0x10	Transmitter rising edge compensation circuitry data value
RX_CTL	6:5	0x0	Receiver rising edge PHY control value 00=Apply RX_CALCOMP directly as the compensation 01=Apply RX_COMPDATA directly as the compensation 10=Apply the sum of RX_CALCOMP and RX_COMPDATA 11=Apply the diff of RX_CALCOMP and RX_COMPDATA
RESERVED_7	7	0x0	
RX_CALCCOMP (R)	12:8	0x10	Calculated compensation value for the receiver
RESERVED_14_13	14:13	0x0	Bit [14]=CfgHTiu_HT_RX_COMPOVR Bit [13]=CfgHTiu_HT_RX_FCOMPCYC
SUCU	15	0x0	Speeds up compensation update 0=Link PHY compensation values are allowed to changed every 1ms 1=Link PHY compensation values are allowed to changed every 1us
ICGSMAF	23:16	0x0	Internal clock gating system management 0=No power reduction 1=IC power is reduced through gatind of internal clocks
REVERVED_25to24 (R)	25:24	0x0	Bit [25]=CfgHTiu_HT_TX_UPDATE Bit [24]=CfgHTiu_HT_RX_UPDATE
RESERVED_29to26	29:26	0x0	
SULS	30	0x0	Speeds up connection sequence for frequency change 0=PLL lock timer is 100 us 1=PLL lock timer is 1us
CGEN	31	0x0	Enables Clock gating 0=Internal clock gating is disabled 1=Internal clock gating is enabled
HT_CLK_CNTL_RECEIVER_COMP_CNTL			

NB_HT_LINK_COMMAND - RW - 32 bits - nbconfig:0xC4			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x8	Specifies the capability ID for the link configuration space
NEXT_PTR (R)	15:8	0x54	Read only register pointing to the next item in the capability list
BASE_UNIT_ID	20:16	0x0	Specifies the link protocol base Unit ID. Relocating the base Unit ID is not supported
UNIT_ID_COUNT (R)	25:21	0xc	Specifies the number of Unit IDs used by the chip
MASTER_HOST (R)	26	0x0	Should always be set to 0
DEFAULT_DIRECTION (R)	27	0x0	Should always be set to 0
DROP_ON_UNINIT_LINK	28	0x0	Should always be set to 0
SLAVE_PRIMARY_TYPE (R)	31:29	0x0	Read only
HT Link command			

NB_HT_LINK_CONF_CNTL - RW - 32 bits - nbconfig:0xC8			
Field Name	**Bits**	**Default**	**Description**
CRC_FLOOD_ENABLE	1	0x0	Flood enable 0=CRC errors do not result in a sync flood 1=CRC errors result in a sync flood
CRC_ERROR_COMMAND	3	0x0	CRC error command 0=Transmitter CRC value match the values calculated per the link specification 1=The link tranmission logic generates erroneous CRC value
LINK_FAILURE	4	0x0	This bit is set when CRC error is detected. It is cleared by PWROK
INIT_COMPLETE	5	0x0	This bit is set when low level link initialization has successfully completed. If the device on the other side is unable to properly perform link initilization, then the bit is not set
END_OF_CHAIN (R)	6	0x0	Read write 1 only 1=Fix to 1
TRANSMITTER_OFF	7	0x0	Read-write 1 only 1=No output signals on the link toggle. The input link receivers are disabled and pins may float
CRC_ERROR_DETECTED	9:8	0x0	Read. Set by hardware. Bit [9] applies to upper byte of the link and bit [8] applies to the lower byte. When this bit is one, the hardware detected a CRC error on the incoming link. It is cleared by PWROK
IsocEn	12	0x0	Enables Isochronous flow-control mode. This register requires a warm-reset to take effect. Refer to the appropriate processor BKDG on additional settings required to enable IFCM
LDT3S_ENABLE	13	0x0	Enables Link three state 0=During the disconnect sequence, the link transmitter is driven but in and underfined state 1=During the disconnect sequence, the link transmitter is placed into a high impedance state. It is cleared by PWROK
EXTENDED_CNTL_TIME	14	0x0	Specifies the time in which the control is held 0=At least 16 bit time 1=About 50 microseconds. It is cleared by PWROK
MAX_LINK_WIDTH_IN (R)	18:16	0x1	Specifies the operating width of the incomming to be 16 bits for side A
MAX_LINK_WIDTH_OUT (R)	22:20	0x1	Specifies the operating width of the outgoing to be 16 bits for side A
LINK_WIDTH_IN	26:24	0x0	Specifies the operation of the input width 000=8 bits 001=16 bits 100=2 bits (not supported) 101=4 bits (not supported) 111=Not connected. It is cleared by PWROK
LINK_WIDTH_OUT	30:28	0x0	Specifies the operating of the output width 000=8 bits 001=16 bits 100=2 bits (not supported) 101=4 bits (not supported) 111=Not connected. It is cleared by PWROK
HT link configuration control			

NB_HT_LINK_END - R - 32 bits - nbconfig:0xCC			
Field Name	**Bits**	**Default**	**Description**
LINK_FAILURE	4	0x1	Device implement one link in the chain, hardwire to 1
END_OF_CHAIN	6	0x1	Device implement one link in the chain, hardwire to 1
TRANSMITTER_OFF	7	0x1	Device implement one link in the chain, hardwire to 1
HT Link end			

NB_HT_LINK_FREQ_CAP_A - RW - 32 bits - nbconfig:0xD0			
Field Name	**Bits**	**Default**	**Description**
MINOR_REVISION (R)	4:0	0x0	Indicates the minor revision of the Hypertransport specification this device supports
MAJOR_REVISION (R)	7:5	0x3	Indicates the major revision of the Hypertransport specification this device supports
LINK_FREQUENCY_A	11:8	0x0	Specified the link side A frequency 0h=200Mhz 1h=Reserved 2h=400Mhz 3h=Reserved 4h=600Mhz 5h=800Mhz 6h=1000MHz 7h=1200MHz 8h=1400MHz 9h=1600MHz ah=1800MHz bh=2000MHz ch=2200MHz dh=2400MHz eh=2600MHz fh=Reserved. It is cleared by PWROK
Protocol_Error	12	0x0	
Overflow_Error	13	0x0	
LINK_FREQ_CAP_A	31:16	0x7ff5	Indicates that the A side of channel supports 200, 400, 800, 1000 Mhz link frequency
HT link frequency channel A			

NB_HT_LINK_FREQ_CAP_B - R - 32 bits - nbconfig:0xD4			
Field Name	**Bits**	**Default**	**Description**
LINK_DEVICE_FEATURE_CAP	7:0	0x2	Indicate which optional features are supported by the device
HT link frequency channel B			

NB_HT_ENUMERATION_SCRATCHPAD - RW - 32 bits - nbconfig:0xD8			
Field Name	**Bits**	**Default**	**Description**
Protocol_Error_Flood_Enable	16	0x0	Enables Sync Flood on protocol errors. This bit only works in Hypertransport 1 mode
Overflow_Error_Flood_Enable	17	0x0	Enables Sync Flood on flow-control buffer overflow errors. This bit only works in Hypertransport 1 mode
Response_Error	25	0x0	Indicates an error was detected in a downstream response packet
HT scratch pad			

NB_HT_MEMORY_BASE_UPPER - RW - 32 bits - nbconfig:0xDC			
Field Name	**Bits**	**Default**	**Description**
MEMORY_BASE_UPPER_8BIT	7:0	0x0	Extends the nonprefetchable memory base register defined for bridges to 40 bits
MEMORY_LIMIT_UPPER_8BIT	15:8	0x0	Extends the nonprefetchable memory limit register defined for bridges to 40 bits
BUS_NUMBER (R)	23:16	0x0	Contains values of bus number captured from type 0
HT memory upper base			

IOC_PCIE_D2_CSR_Count - RW - 32 bits - NBMISCIND:0x50			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D2_CNTL - RW - 32 bits - NBMISCIND:0x51			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D3_CSR_Count - RW - 32 bits - NBMISCIND:0x52			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D3_CNTL - RW - 32 bits - NBMISCIND:0x53			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D4_CSR_Count - RW - 32 bits - NBMISCIND:0x54			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D4_CNTL - RW - 32 bits - NBMISCIND:0x55			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D5_CSR_Count - RW - 32 bits - NBMISCIND:0x56			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D5_CNTL - RW - 32 bits - NBMISCIND:0x57			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D6_CSR_Count - RW - 32 bits - NBMISCIND:0x58			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D6_CNTL - RW - 32 bits - NBMISCIND:0x59			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D7_CSR_Count - RW - 32 bits - NBMISCIND:0x5A			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D7_CNTL - RW - 32 bits - NBMISCIND:0x5B			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D9_CSR_Count - RW - 32 bits - NBMISCIND:0x5C			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D9_CNTL - RW - 32 bits - NBMISCIND:0x5D			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D10_CSR_Count - RW - 32 bits - NBMISCIND:0x5E			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D10_CNTL - RW - 32 bits - NBMISCIND:0x5F			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D11_CSR_Count - RW - 32 bits - NBMISCIND:0x60			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D11_CNTL - RW - 32 bits - NBMISCIND:0x61			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D12_CSR_Count - RW - 32 bits - NBMISCIND:0x62			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D12_CNTL - RW - 32 bits - NBMISCIND:0x63			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

NB_PCI_ARB - RW - 32 bits - nbconfig:0x84			
Field Name	**Bits**	**Default**	**Description**
RCRB_ENABLE	0	0x0	Enables RCRB memory mapped cfg access through BAR1 0=Disable 1=Enable
PM2_SB_ENABLE	2	0x0	Enables PM2_CNTL(BAR2) IO mapped cfg write access to be broadcast to both NB and SB. 0=Disable 1=Enable
EV6MODE	4	0x0	EV6 Mode Indicates that the PCI interfaces have to decode memory range from 640K to 1M. 0=Enable 1=Disable
_14M_HOLE	5	0x0	14M Memory Hole Creates a hole in memory from 14 Mb to 15 Mb. This register is used by the PCI decode logic to know when to accept a cycle from an external PCI master. When set, the PCI decode logic does not assert a match for addresses falling in this range. 0=Disable 1=Enable

_15M_HOLE	6	0x0	15M Memory Hole Creates a hole in memory from 15 Mb to 16 Mb. This register is used by the PCI decode logic to know when to accept a cycle from an external PCI master. When set, the PCI decode logic does not assert a match for addresses falling in this range. 0=Disable 1=Enable
PM_REG_ENABLE	7	0x0	Power Management Register Enable Enables BAR2 IO access decoding 0=Disable 1=Enable
PMEMode	8	0x0	PME message mode 0=PME_Turn_Off is triggered by STP_GNT(S3) request from BIU 1=PME_Turn_Off is triggered by writing 1 to PMETurnOff bit (0x84[9]). 0=Disable 1=Enable
PMETurnOff	9	0x0	PME_Turn_Off message trigger In case PMEMode is set, writing 1 to this bit will trigger a PME_Turn_Off message to all downstream devices. This bit is reset only then the system power is off. 0=Disable 1=Enable
READ_DATA_ERROR_DISABLE	12	0x0	Not used in the RS780. 0=Enable 1=Disable
MDA_DEBUG	15	0x0	MDA Debug This bit allows monochrome display adapters (MDA) to be used simultaneously with AGP cards for the debugging of AGP device drivers. The behavior of the RS780 display adapters is a function of this bit. The VGA Enable in (D1:0x3C[19]) is as follows: MDA Address Ranges: Memory: 0B0000h-0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh VGA = 0, MDA = 0: All MDA and VGA references go to PCI VGA = 0, MDA = 1: Operation undefined VGA = 1, MDA = 0: All VGA references go to AGP, MDA only (I/O 3BFh) go to PCI VGA =1, MDA = 1: All VGA references go to AGP, All MDA (including memory) go to PCI 0=Disable 1=Enable
BAR3BusRange	18:16	0x0	0=BAR3[27:20] are all used for bus number decoding so BAR3 memory map range is [39:28] 1=BAR3[20] is used for bus number decoding so memory map range is [39:21] 2=BAR3[21:20] are used for bus number decoding so memory map range is [39:22] 3=BAR3[22:20] are used for bus number decoding so memory range is [39:23] ... 7=[26:20] are used for bus number decoding so memory map range is [39:27] 0=Disable 1=Enable

AGP_VGA_BIOS	31:24	0x3	AGP VGA BIOS Indicates that the corresponding (16K) segment should be mapped to AGP's PCI bus. Bit [24] corresponds to the addresses 0xC0000-0xC3FFF, and bit [31] maps addresses 0xDC000-0xDFFFF to AGP's PCI interface. One or more of these bits should be set if the AGP graphics card has a ROM BIOS.
This register provides general PCI arbiter mode control			

NB_CFG_STAT - RW - 32 bits - nbconfig:0x88			
Field Name	**Bits**	**Default**	**Description**
CPU_DIVIDER (R)	3:0	0x0	CPU Divider Contains the CPU divider field supplied by the Slot-A CPU card. Together with [20] and the Bus Len field, this allows the RS780 to properly program the system bus init logic using the SIP protocol.
OUT_CLK_DELAY (R)	4	0x0	OUTCLK Enable Indicates that the CPU will delay the OUTCLK to the RS780. When reset the motherboard is expected to provide a delay in the etch to center the OUTCLK with the data. 0=Disable 1=Enable
IN_CLK_DELAY (R)	5	0x0	INCLK Enable Indicates that the RS780 will delay the INCLK to the CPU. When reset the motherboard is expected to provide a delay in the etch to center the INCLK with the data. 0=Disable 1=Enable
Reserved0 (R)	7	0x0	
Reserved1 (R)	17:16	0x0	
SYS_CLK_MUX (R)	28:26	0x0	System Clock Mux. For internal testing only
This register allows the BIOS software to determine what system initialization states have been programmed by resistor strappings (CPU card, motherboard etc.).			

NB_GC_STRAPS - RW - 32 bits - nbconfig:0x8C			
Field Name	**Bits**	**Default**	**Description**
EXTGFX_ENABLE	0	0x1	External Graphic Enable 0=Disable 1=Enable
INTGFX_ENABLE (R)	1	0x1	0=Disable 1=Enable
VGA_DISABLE	2	0x0	0=Enable 1=Disable
ID_DISABLE	3	0x0	0=Enable 1=Disable
APERTURE_SIZE	6:4	0x3	0=128MB 1=256MB 2=64MB 3=32MB 4=512MB 5=1GB 6=2GB 7=4GB
F1_MULTI_FUNC_ENABLE	7	0x0	
F2_MULTI_FUNC_ENABLE	8	0x0	
GFX_DEBUG_BAR_ENABLE	9	0x0	

GFX_DEBUG_DECODE_ENABLE	10	0x0	
ENINTb	11	0x0	
VE (R)	12	0x0	
EXT_MEM_EN	13	0x1	
BLANK_ROM	14	0x0	
POWER_ON_STRAPS	27:16	0x0	Extra strapping signals
MOBILE (R)	28	0x0	This is the value of the pin strap on the DAC_VSYNC pin during strap capture. The strap name is STRAP_MOBILE_GFX. This pinstrap changes the Device ID of the Internal Graphics Device and allows C3 functionality ala STP_AGP#/AGP_BUSY#. When Pinstrap is 1, it selects the mobile graphics device ID. When Pinstrap is 0, it selects the desktop graphics device ID.
CHG_ID (R)	31:29	0x0	CHANGE_ID from nb_efuse.
Graphics Controller strap access register			

NB_TOP_OF_DRAM_SLOT1 - RW - 32 bits - nbconfig:0x90			
Field Name	**Bits**	**Default**	**Description**
TOP_OF_DRAM	31:23	0x0	PCI Memory Top This 8-bit field is compared to the incoming PCI Bus master address to determine if a memory cycle falls within the RS780's DRAM region. The BIOS should write to this field following the completion of the memory sizing algorithm, after it has determined the total size of the installed memory.
This register is used to define the top of main system memory. It is used to compare the memory addresses of an external PCI master to determine if it is in the range of the RS780's system DRAM. If the address compares then the RS780 will respond to the bus master access by asserting DEVSEL#			

NB_PERF_CNT_CTRL - RW - 32 bits - nbconfig:0xF4			
Field Name	**Bits**	**Default**	**Description**
GLOBE_CNT_EN	0	0x0	0=Stop all counters 1=Start all counters
GLOBE_SHADOW_WR (W)	1	0x0	Write 1 to load the counter shadow registers. The read back value has no meaning.
GLOBE_PERF_RESET (W)	2	0x0	Write 1 for Global RESET of ALL counters. The read back value has no meaning. 0=Toggle Global Reset to all Counters
GLOBE_SHADOW_DELAY	11:8	0x0	Programmable Pulse width for Global Shadow Write Toggle
GLOBE_SHADOW_DELAY_EN	15	0x1	Enables the Programmable Pulse with for Global Shadow Write Toggle 0=Disable 1=Enable
GLOBE_PERF_RESET_DELAY	19:16	0x0	Programmable Pulse width for Global Perf Reset Toggle
GLOBE_PERF_RESET_DELAY_EN	23	0x1	Enables the Programmable Pulse width for Global Perf Reset Toggle 0=Disable 1=Enable
Performance Counters Control Register			

NB_MC_IND_INDEX - RW - 32 bits - nbconfig:0x70			
Field Name	**Bits**	**Default**	**Description**
MC_IND_ADDR	15:0	0x0	
MC_IND_SEQ_RBS_0	16	0x0	0=Do not access sequencer+gfx return bus block 0 (channels A+B) 1=Access sequencer+gfx return bus block 0 (channels A+B)
MC_IND_SEQ_RBS_1	17	0x0	0=Do not access sequencer+gfx return bus block 1 (channels C+D) 1=Access sequencer+gfx return bus block 1 (channels C+D)
MC_IND_SEQ_RBS_2	18	0x0	0=Do not access sequencer+gfx return bus block 2 (channels E+F) 1=Access sequencer+gfx return bus block 2 (channels E+F)
MC_IND_SEQ_RBS_3	19	0x0	0=Do not access sequencer+gfx return bus block 3 (channels G+H) 1=Access sequencer+gfx return bus block 3 (channels G+H)
MC_IND_AIC_RBS	20	0x0	0=Do not access aic+cpvf and glb return bus block 1=Access aic+cpvf and glb return bus block
MC_IND_CITF_ARB0	21	0x0	0=Do not access client MCT interface+arbitration block 1=Access client MCT interface+arbitration block
MC_IND_CITF_ARB1	22	0x0	0=Do not access client MCB interface+arbitration block 1=Access client MCB interface+arbitration block
MC_IND_WR_EN	23	0x0	0=Disable write capability (read only) 1=Enable write capability
MC_IND_RD_INV	24	0x0	0=Do not invert data on return bus 1=Invert data on return bus
Index register for accessing MC indirect registers in mmreg (mcind) space. Note: Only mcind 0x10-38 are accessible			

NB_MC_IND_DATA - RW - 32 bits - nbconfig:0x74			
Field Name	**Bits**	**Default**	**Description**
MC_IND_DATA	31:0	0x0	
Data register for accessing MC indirect registers in mmreg (mcind) space. Note: Only mcind 0x10-38 are accessible			

2.2 PCIE Configuration Registers

PCIE_PORT_INDEX - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xE0			
Field Name	**Bits**	**Default**	**Description**
PCIE_INDEX	7:0	0x0	Index of bifdecp
Index register for the PCI Express port indirect registers			

PCIE_PORT_DATA - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xE4			
Field Name	**Bits**	**Default**	**Description**
PCIE_DATA	31:0	0x0	Data of bifdecp
Data register for the PCI Express port indirect registers			

NB_PCIE_VENDOR_ID - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x0			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID (R)	15:0	0x0	

NB_PCIE_DEVICE_ID - R - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x2			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x0	

NB_PCIE_COMMAND - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x4			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN	0	0x0	0=Disable 1=Enable
MEM_ACCESS_EN	1	0x0	0=Disable 1=Enable
BUS_MASTER_EN	2	0x0	0=Disable 1=Enable
SPECIAL_CYCLE_EN (R)	3	0x0	0=Disable 1=Enable
MEM_WRITE_INVALIDATE_EN (R)	4	0x0	0=Disable 1=Enable
PAL_SNOOP_EN (R)	5	0x0	0=Disable 1=Enable
PARITY_ERROR_RESPONSE	6	0x0	0=Disable 1=Enable
AD_STEPPING (R)	7	0x0	0=Disable 1=Enable
SERR_EN	8	0x0	0=Disable 1=Enable
FAST_B2B_EN (R)	9	0x0	0=Disable 1=Enable
INT_DIS	10	0x0	0=Enable 1=Disable

NB_PCIE_STATUS - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x6			
Field Name	**Bits**	**Default**	**Description**
INT_STATUS (R)	3	0x0	
CAP_LIST (R)	4	0x1	
PCI_66_EN (R)	5	0x0	
UDF_EN (R)	6	0x0	0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	
MASTER_DATA_PARITY_ERROR (R)	8	0x0	0=Inactive 1=Active
DEVSEL_TIMING (R)	10:9	0x0	
SIGNAL_TARGET_ABORT (R)	11	0x0	0=No Abort 1=Target Abort
RECEIVED_TARGET_ABORT (R)	12	0x0	0=Inactive 1=Active
RECEIVED_MASTER_ABORT (R)	13	0x0	0=Inactive 1=Active
SIGNALED_SYSTEM_ERROR	14	0x0	0=No Error 1=SERR assert
PARITY_ERROR_DETECTED (R)	15	0x0	

NB_PCIE_REVISION_ID - R - 8 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x8			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	
MAJOR_REV_ID	7:4	0x0	

NB_PCIE_PROG_INTERFACE - R - 8 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x9			
Field Name	**Bits**	**Default**	**Description**
PROG_INTERFACE	7:0	0x0	

NB_PCIE_SUB_CLASS - R - 8 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xA			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS	7:0	0x0	

NB_PCIE_BASE_CLASS - R - 8 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xB			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS	7:0	0x0	

NB_PCIE_CACHE_LINE - RW - 8 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xC			
Field Name	**Bits**	**Default**	**Description**
CACHE_LINE_SIZE	7:0	0x0	

NB_PCIE_LATENCY - RW - 8 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xD			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER (R)	7:0	0x0	

NB_PCIE_HEADER - RW - 8 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xE			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE (R)	6:0	0x1	
DEVICE_TYPE (R)	7	0x0	0=Single-Function Device 1=Multi-Function Device

NB_PCIE_BIST - RW - 8 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xF			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP (R)	3:0	0x0	
BIST_STRT (R)	6	0x0	
BIST_CAP (R)	7	0x0	

NB_PCIE_SUB_BUS_NUMBER_LATENCY - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x18			
Field Name	**Bits**	**Default**	**Description**
PRIMARY_BUS	7:0	0x0	
SECONDARY_BUS	15:8	0x0	
SUB_BUS_NUM	23:16	0x0	
SECONDARY_LATENCY_TIMER (R)	31:24	0x0	

NB_PCIE_IO_BASE_LIMIT - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x1C			
Field Name	**Bits**	**Default**	**Description**
IO_BASE_TYPE (R)	3:0	0x1	0=16-bit 1=32-bit
IO_BASE	7:4	0x0	
IO_LIMIT_TYPE (R)	11:8	0x1	0=16-bit 1=32-bit
IO_LIMIT	15:12	0x0	

NB_PCIE_SECONDARY_STATUS - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x1E			
Field Name	**Bits**	**Default**	**Description**
CAP_LIST (R)	4	0x0	
PCI_66_EN (R)	5	0x0	
UDF_EN (R)	6	0x0	0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	
MASTER_DATA_PARITY_ERROR	8	0x0	0=No error 1=Parity error
DEVSEL_TIMING (R)	10:9	0x0	
SIGNAL_TARGET_ABORT (R)	11	0x0	0=No Abort 1=Target Abort asserted
RECEIVED_TARGET_ABORT	12	0x0	0=No CA Received 1=Received Completion Abort
RECEIVED_MASTER_ABORT	13	0x0	0=No UR Received 1=Received Unsupported Request
RECEIVED_SYSTEM_ERROR	14	0x0	0=No Error 1=Sent Error Meesage
PARITY_ERROR_DETECTED	15	0x0	0=No Error 1=Received Poisoned TLP

NB_PCIE_MEM_BASE_LIMIT - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x20			
Field Name	**Bits**	**Default**	**Description**
MEM_BASE_TYPE (R)	3:0	0x0	0=32-bit 1=64-bit
MEM_BASE_31_20	15:4	0x0	
MEM_LIMIT_TYPE (R)	19:16	0x0	0=32-bit 1=64-bit
MEM_LIMIT_31_20	31:20	0x0	

NB_PCIE_PREF_BASE_LIMIT - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x24			
Field Name	**Bits**	**Default**	**Description**
PREF_MEM_BASE_TYPE (R)	3:0	0x1	0=32-bit 1=64-bit
PREF_MEM_BASE_31_20	15:4	0x0	
PREF_MEM_LIMIT_TYPE (R)	19:16	0x1	0=32-bit 1=64-bit
PREF_MEM_LIMIT_31_20	31:20	0x0	

NB_PCIE_PREF_BASE_UPPER - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x28			
Field Name	**Bits**	**Default**	**Description**
PREF_BASE_UPPER	31:0	0x0	

NB_PCIE_PREF_LIMIT_UPPER - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x2C			
Field Name	**Bits**	**Default**	**Description**
PREF_LIMIT_UPPER	31:0	0x0	

NB_PCIE_IO_BASE_LIMIT_HI - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x30			
Field Name	**Bits**	**Default**	**Description**
IO_BASE_31_16	15:0	0x0	
IO_LIMIT_31_16	31:16	0x0	

NB_PCIE_IRQ_BRIDGE_CNTL - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x3E			
Field Name	**Bits**	**Default**	**Description**
PARITY_RESPONSE_EN	0	0x0	
SERR_EN	1	0x0	
ISA_EN	2	0x0	
VGA_EN	3	0x0	
VGA_DEC	4	0x0	
MASTER_ABORT_MODE (R)	5	0x0	
SECONDARY_BUS_RESET	6	0x0	0=Run 1=Reset
FAST_B2B_EN (R)	7	0x0	0=Disable 1=Enable

NB_PCIE_CAP_PTR - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x34			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR (R)	7:0	0x50	50=Point to PM Capability

NB_PCIE_INTERRUPT_LINE - RW - 8 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x3C			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_LINE	7:0	0xff	

NB_PCIE_INTERRUPT_PIN - RW - 8 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x3D			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_PIN	7:0	0x0	Note: Bits [7:3] of this field are hardwired to 0.

NB_PCIE_PMI_CAP_LIST - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x50			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x1	1=PCIE Power Management Registers
NEXT_PTR (R)	15:8	0x58	

NB_PCIE_PMI_CAP - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x52			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	2:0	0x3	3=PMI Spec 1.2
PME_CLOCK (R)	3	0x0	
DEV_SPECIFIC_INIT (R)	5	0x0	
AUX_CURRENT	8:6	0x0	
D1_SUPPORT (R)	9	0x0	1=Support D1 PM State.
D2_SUPPORT (R)	10	0x0	1=Support D2 PM State.
PME_SUPPORT (R)	15:11	0x0	

NB_PCIE_PMI_STATUS_CNTL - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x54			
Field Name	**Bits**	**Default**	**Description**
POWER_STATE	1:0	0x0	
NO_SOFT_RESET (R)	3	0x0	
PME_EN	8	0x0	
DATA_SELECT (R)	12:9	0x0	
DATA_SCALE (R)	14:13	0x0	
PME_STATUS	15	0x0	
B2_B3_SUPPORT (R)	22	0x0	
BUS_PWR_EN (R)	23	0x0	
PMI_DATA (R)	31:24	0x0	

NB_PCIE_CAP_LIST - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x58			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x10	10=PCI Express capable
NEXT_PTR (R)	15:8	0xa0	

NB_PCIE_CAP - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x5A			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	3:0	0x2	0=PCI Express Cap Version
DEVICE_TYPE (R)	7:4	0x4	0=PCI Express Endpoint 1=Legacy PCI Express Endpoint 4=PCI Express Root Complex
SLOT_IMPLEMENTED	8	0x0	
INT_MESSAGE_NUM (R)	13:9	0x0	
TCS_ROUTING_SUPPORTED (R)	14	0x0	

NB_PCIE_DEVICE_CAP - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x5C			
Field Name	**Bits**	**Default**	**Description**
MAX_PAYLOAD_SUPPORT (R)	2:0	0x0	0=128B size
PHANTOM_FUNC (R)	4:3	0x0	0=No Phantom Functions
EXTENDED_TAG (R)	5	0x1	0=5 Bit Tag Supported 1=8 Bit Tag Supported
L0S_ACCEPTABLE_LATENCY (R)	8:6	0x0	
L1_ACCEPTABLE_LATENCY (R)	11:9	0x0	
ROLE_BASED_ERR_REPORTING (R)	15	0x0	0=Role-Based Error Reporting Disabled 1=Role-Based Error Reporting Enabled
CAPTURED_SLOT_POWER_LIMIT (R)	25:18	0x0	
CAPTURED_SLOT_POWER_SCALE (R)	27:26	0x0	
FLR_CAPABLE (R)	28	0x0	

NB_PCIE_DEVICE_CNTL - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x60			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_EN	0	0x0	0=Disable 1=Enable
NON_FATAL_ERR_EN	1	0x0	0=Disable 1=Enable
FATAL_ERR_EN	2	0x0	0=Disable 1=Enable
USR_REPORT_EN	3	0x0	0=Disable 1=Enable
RELAXED_ORD_EN	4	0x1	0=Disable 1=Enable
MAX_PAYLOAD_SIZE (R)	7:5	0x0	0=128B size
EXTENDED_TAG_EN	8	0x0	0=Disable 1=Enable
PHANTOM_FUNC_EN (R)	9	0x0	0=Disable 1=Enable
AUX_POWER_PM_EN (R)	10	0x0	0=Disable 1=Enable
NO_SNOOP_EN	11	0x1	0=Disable 1=Enable
MAX_REQUEST_SIZE (R)	14:12	0x0	0=128B size
BRIDGE_CFG_RETRY_EN (R)	15	0x0	0=Disable 1=Enable

NB_PCIE_DEVICE_STATUS - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x62			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR	0	0x0	
NON_FATAL_ERR	1	0x0	
FATAL_ERR	2	0x0	
USR_DETECTED	3	0x0	
AUX_PWR	4	0x0	
TRANSACTIONS_PEND (R)	5	0x0	

NB_PCIE_LINK_CAP - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x64			
Field Name	**Bits**	**Default**	**Description**
LINK_SPEED (R)	3:0	0x1	1=2.5 Gb/s 2=5.0 Gb/s
LINK_WIDTH (R)	9:4	0x0	1 = x1 2 = x2 4 = x4 8 = x8 12 = x12 16 = x16 32 = x32
PM_SUPPORT (R)	11:10	0x3	
L0S_EXIT_LATENCY (R)	14:12	0x1	
L1_EXIT_LATENCY (R)	17:15	0x2	
CLOCK_POWER_MANAGEMENT (R)	18	0x0	
SURPRISE_DOWN_ERR_REPORTING (R)	19	0x0	
DL_ACTIVE_REPORTING_CAPABLE (R)	20	0x0	
LINK_BW_NOTIFICATION_CAP (R)	21	0x0	
PORT_NUMBER (R)	31:24	0x0	

NB_PCIE_LINK_CNTL - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x68			
Field Name	**Bits**	**Default**	**Description**
PM_CONTROL	1:0	0x0	
READ_CPL_BOUNDARY (R)	3	0x0	0=64 Byte 1=128 Byte
LINK_DIS	4	0x0	
RETRAIN_LINK (W)	5	0x0	
COMMON_CLOCK_CFG	6	0x0	
EXTENDED_SYNC	7	0x0	
CLOCK_POWER_MANAGEMENT_EN	8	0x0	
HW_AUTONOMOUS_WIDTH_DISABLE	9	0x0	
LINK_BW_MANAGEMENT_INT_EN	10	0x0	
LINK_AUTONOMOUS_BW_INT_EN	11	0x0	

NB_PCIE_LINK_STATUS - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x6A			
Field Name	**Bits**	**Default**	**Description**
CURRENT_LINK_SPEED (R)	3:0	0x1	1=2.5 Gb/s 2=5.0 Gb/s
NEGOTIATED_LINK_WIDTH (R)	9:4	0x0	1 = x1 2 = x2 4 = x4 8 = x8 12 = x12 16 = x16 32 = x32
LINK_TRAINING (R)	11	0x0	
SLOT_CLOCK_CFG (R)	12	0x1	0=Diff Clock 1=Same Clock
DL_ACTIVE (R)	13	0x0	
LINK_BW_MANAGEMENT_STATUS	14	0x0	
LINK_AUTONOMOUS_BW_STATUS	15	0x0	

NB_PCIE_SLOT_CAP - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x6C			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESENT (R)	0	0x0	
PWR_CONTROLLER_PRESENT (R)	1	0x0	
MRL_SENSOR_PRESENT (R)	2	0x0	
ATTN_INDICATOR_PRESENT (R)	3	0x0	
PWR_INDICATOR_PRESENT (R)	4	0x0	
HOTPLUG_SURPRISE	5	0x0	
HOTPLUG_CAPABLE	6	0x0	
SLOT_PWR_LIMIT_VALUE	14:7	0x0	
SLOT_PWR_LIMIT_SCALE	16:15	0x0	
ELECTROMECH_INTERLOCK_PRESENT (R)	17	0x0	
NO_COMMAND_COMPLETED_SUPPORTED (R)	18	0x1	
PHYSICAL_SLOT_NUM	31:19	0x0	

NB_PCIE_SLOT_CNTL - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x70			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESSED_EN (R)	0	0x0	
PWR_FAULT_DETECTED_EN (R)	1	0x0	
MRL_SENSOR_CHANGED_EN (R)	2	0x0	
PRESENCE_DETECT_CHANGED_EN	3	0x0	
COMMAND_COMPLETED_INTR_EN (R)	4	0x0	
HOTPLUG_INTR_EN	5	0x0	

ATTN_INDICATOR_CNTL (R)	7:6	0x0	
PWR_INDICATOR_CNTL (R)	9:8	0x0	
PWR_CONTROLLER_CNTL (R)	10	0x0	
ELECTOMECH_INTERLOCK_CNTL (R)	11	0x0	
DL_STATE_CHANGED_EN	12	0x0	

NB_PCIE_SLOT_STATUS - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x72

Field Name	Bits	Default	Description
ATTN_BUTTON_PRESSED (R)	0	0x0	
PRESENCE_DETECT_CHANGED	3	0x0	
COMMAND_COMPLETED (R)	4	0x0	
PRESENCE_DETECT_STATE (R)	6	0x0	
ELECTROMECH_INTERLOCK_STATUS (R)	7	0x0	
DL_STATE_CHANGED	8	0x0	

NB_PCIE_ROOT_CNTL - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x74

Field Name	Bits	Default	Description
SERR_ON_CORR_ERR_EN	0	0x0	
SERR_ON_NONFATAL_ERR_EN	1	0x0	
SERR_ON_FATAL_ERR_EN	2	0x0	
PM_INTERRUPT_EN	3	0x0	
CRS_SOFTWARE_VISIBILITY_EN	4	0x0	

NB_PCIE_ROOT_CAP - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x76

Field Name	Bits	Default	Description
CRS_SOFTWARE_VISIBILITY (R)	0	0x1	

NB_PCIE_ROOT_STATUS - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x78

Field Name	Bits	Default	Description
PME_REQUESTOR_ID (R)	15:0	0x0	
PME_STATUS	16	0x0	
PME_PENDING (R)	17	0x0	

NB_PCIE_DEVICE_CAP2 - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x7C			
Field Name	**Bits**	**Default**	**Description**
CPL_TIMEOUT_RANGE_SUP (R)	3:0	0x0	
CPL_TIMEOUT_DIS_SUP (R)	4	0x0	

NB_PCIE_DEVICE_CNTL2 - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x80			
Field Name	**Bits**	**Default**	**Description**
CPL_TIMEOUT_VALUE	3:0	0x0	
CPL_TIMEOUT_DIS	4	0x0	

NB_PCIE_DEVICE_STATUS2 - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x82			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	

NB_PCIE_LINK_CAP2 - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x84			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	31:0	0x0	

NB_PCIE_LINK_CNTL2 - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x88			
Field Name	**Bits**	**Default**	**Description**
TARGET_LINK_SPEED	3:0	0x1	
ENTER_COMPLIANCE	4	0x0	
HW_AUTONOMOUS_SPEED_DISABLE	5	0x0	
SELECTABLE_DEEMPHASIS (R)	6	0x0	
XMIT_MARGIN	9:7	0x0	
ENTER_MOD_COMPLIANCE	10	0x0	
COMPLIANCE_SOS	11	0x0	
COMPLIANCE_DEEMPHASIS	12	0x0	0 = -6 dB 1 = -3 dB

NB_PCIE_LINK_STATUS2 - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x8A			
Field Name	**Bits**	**Default**	**Description**
CUR_DEEMPHASIS_LEVEL (R)	0	0x0	

NB_PCIE_SLOT_CAP2 - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x8C			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	31:0	0x0	

NB_PCIE_SLOT_CNTL2 - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x90			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	

NB_PCIE_SLOT_STATUS2 - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x92			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	

NB_PCIE_MSI_CAP_LIST - R - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xA0			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x5	
NEXT_PTR	15:8	0xb0	

NB_PCIE_MSI_MSG_CNTL - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xA2			
Field Name	**Bits**	**Default**	**Description**
MSI_EN	0	0x0	0=Disable 1=Enable
MSI_MULTI_CAP (R)	3:1	0x0	0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_MULTI_EN	6:4	0x0	0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_64BIT (R)	7	0x0	0=Not capable of generating 1 64-bit message address 1=Capable of generating 1 64-bit message address

NB_PCIE_MSI_MSG_ADDR_LO - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xA4			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_LO	31:2	0x0	

NB_PCIE_MSI_MSG_ADDR_HI - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xA8			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_HI (R)	31:0	0x0	

NB_PCIE_MSI_MSG_DATA_64 - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xAC			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA_64 (R)	15:0	0x0	

NB_PCIE_MSI_MSG_DATA - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xA8			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA	15:0	0x0	

NB_PCIE_SSID_CAP_LIST - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xB0			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0xd	
NEXT_PTR (R)	15:8	0xb8	

NB_PCIE_SSID_ID - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xB4			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x0	
SUBSYSTEM_ID	31:16	0x0	

NB_PCIE_MSI_MAP_CAP_LIST - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0xB8			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x8	
NEXT_PTR (R)	15:8	0x0	
EN (R)	16	0x1	
FIXD (R)	17	0x1	
CAP_TYPE (R)	31:27	0x15	

NB_PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x100			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0xb	
CAP_VER	19:16	0x1	
NEXT_PTR	31:20	0x110	

NB_PCIE_VENDOR_SPECIFIC_HDR - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x104			
Field Name	**Bits**	**Default**	**Description**
VSEC_ID	15:0	0x1	
VSEC_REV	19:16	0x1	
VSEC_LENGTH	31:20	0x10	

NB_PCIE_VENDOR_SPECIFIC1 - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x108			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	

NB_PCIE_VENDOR_SPECIFIC2 - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x10C			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	

NB_PCIE_VC_ENH_CAP_LIST - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x110			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x2	
CAP_VER	19:16	0x1	
NEXT_PTR	31:20	0x140	

NB_PCIE_PORT_VC_CAP_REG1 - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x114			
Field Name	**Bits**	**Default**	**Description**
EXT_VC_COUNT	2:0	0x0	
LOW_PRIORITY_EXT_VC_COUNT	6:4	0x0	
REF_CLK	9:8	0x0	
PORT_ARB_TABLE_ENTRY_SIZE	11:10	0x0	

NB_PCIE_PORT_VC_CAP_REG2 - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x118			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_CAP	7:0	0x0	
VC_ARB_TABLE_OFFSET	31:24	0x0	

NB_PCIE_PORT_VC_CNTL - RW - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x11C			
Field Name	**Bits**	**Default**	**Description**
LOAD_VC_ARB_TABLE (R)	0	0x0	
VC_ARB_SELECT	3:1	0x0	

NB_PCIE_PORT_VC_STATUS - R - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x11E			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_TABLE_STATUS	0	0x0	

NB_PCIE_VC0_RESOURCE_CAP - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x120			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x1	
REJECT_SNOOP_TRANS	15	0x0	
MAX_TIME_SLOTS	21:16	0x0	
PORT_ARB_TABLE_OFFSET	31:24	0x0	

NB_PCIE_VC0_RESOURCE_CNTL - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x124			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x1	
TC_VC_MAP_TC1_7	7:1	0x7f	
LOAD_PORT_ARB_TABLE (R)	16	0x0	
PORT_ARB_SELECT	19:17	0x0	
VC_ID (R)	26:24	0x0	
VC_ENABLE (R)	31	0x1	

NB_PCIE_VC0_RESOURCE_STATUS - R - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x12A			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	
VC_NEGOTIATION_PENDING	1	0x1	

NB_PCIE_VC1_RESOURCE_CAP - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x12C			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x1	
REJECT_SNOOP_TRANS	15	0x0	
MAX_TIME_SLOTS	21:16	0x0	
PORT_ARB_TABLE_OFFSET	31:24	0x0	

NB_PCIE_VC1_RESOURCE_CNTL - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x130			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x0	
TC_VC_MAP_TC1_7	7:1	0x0	
LOAD_PORT_ARB_TABLE (R)	16	0x0	
PORT_ARB_SELECT	19:17	0x0	
VC_ID	26:24	0x0	
VC_ENABLE	31	0x0	

NB_PCIE_VC1_RESOURCE_STATUS - R - 16 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x136			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	
VC_NEGOTIATION_PENDING	1	0x1	

NB_PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x140			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	15:0	0x3	
CAP_VER (R)	19:16	0x1	
NEXT_PTR (R)	31:20	0x150	

NB_PCIE_DEV_SERIAL_NUM_DW1 - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x144			
Field Name	**Bits**	**Default**	**Description**
SERIAL_NUMBER_LO	31:0	0x0	

NB_PCIE_DEV_SERIAL_NUM_DW2 - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x148			
Field Name	**Bits**	**Default**	**Description**
SERIAL_NUMBER_HI	31:0	0x0	

NB_PCIE_ADV_ERR_RPT_ENH_CAP_LIST - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x150			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	15:0	0x1	
CAP_VER (R)	19:16	0x1	
NEXT_PTR (R)	31:20	0x190	

NB_PCIE_UNCORR_ERR_STATUS - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x154			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_STATUS	4	0x0	
SURPDN_ERR_STATUS (R)	5	0x0	
PSN_ERR_STATUS	12	0x0	
FC_ERR_STATUS (R)	13	0x0	
CPL_TIMEOUT_STATUS	14	0x0	
CPL_ABORT_ERR_STATUS (R)	15	0x0	
UNEXP_CPL_STATUS	16	0x0	

RCV_OVFL_STATUS (R)	17	0x0	
MAL_TLP_STATUS	18	0x0	
ECRC_ERR_STATUS (R)	19	0x0	
UNSUPP_REQ_ERR_STATUS	20	0x0	
ACS_VIOLATION_STATUS	21	0x0	

NB_PCIE_UNCORR_ERR_MASK - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x158

Field Name	Bits	Default	Description
DLP_ERR_MASK	4	0x0	
SURPDN_ERR_MASK (R)	5	0x0	
PSN_ERR_MASK	12	0x0	
FC_ERR_MASK (R)	13	0x0	
CPL_TIMEOUT_MASK	14	0x0	
CPL_ABORT_ERR_MASK (R)	15	0x0	
UNEXP_CPL_MASK	16	0x0	
RCV_OVFL_MASK (R)	17	0x0	
MAL_TLP_MASK	18	0x0	
ECRC_ERR_MASK (R)	19	0x0	
UNSUPP_REQ_ERR_MASK	20	0x0	
ACS_VIOLATION_MASK	21	0x0	

NB_PCIE_UNCORR_ERR_SEVERITY - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x15C

Field Name	Bits	Default	Description
DLP_ERR_SEVERITY	4	0x1	
SURPDN_ERR_SEVERITY (R)	5	0x1	
PSN_ERR_SEVERITY	12	0x0	
FC_ERR_SEVERITY (R)	13	0x1	
CPL_TIMEOUT_SEVERITY	14	0x0	
CPL_ABORT_ERR_SEVERITY (R)	15	0x0	
UNEXP_CPL_SEVERITY	16	0x0	
RCV_OVFL_SEVERITY (R)	17	0x1	
MAL_TLP_SEVERITY	18	0x1	
ECRC_ERR_SEVERITY (R)	19	0x0	
UNSUPP_REQ_ERR_SEVERITY	20	0x0	
ACS_VIOLATION_SEVERITY	21	0x0	

NB_PCIE_CORR_ERR_STATUS - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x160

Field Name	Bits	Default	Description
RCV_ERR_STATUS	0	0x0	
BAD_TLP_STATUS	6	0x0	
BAD_DLLP_STATUS	7	0x0	
REPLAY_NUM_ROLLOVER_STATUS	8	0x0	
REPLAY_TIMER_TIMEOUT_STATUS	12	0x0	
ADVISORY_NONFATAL_ERR_STATUS	13	0x0	

NB_PCIE_CORR_ERR_MASK - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x164			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_MASK	0	0x0	
BAD_TLP_MASK	6	0x0	
BAD_DLLP_MASK	7	0x0	
REPLAY_NUM_ROLLOVER_MASK	8	0x0	
REPLAY_TIMER_TIMEOUT_MASK	12	0x0	
ADVISORY_NONFATAL_ERR_MASK	13	0x1	

NB_PCIE_ADV_ERR_CAP_CNTL - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x168			
Field Name	**Bits**	**Default**	**Description**
FIRST_ERR_PTR (R)	4:0	0x0	
ECRC_GEN_CAP (R)	5	0x0	
ECRC_GEN_EN (R)	6	0x0	
ECRC_CHECK_CAP (R)	7	0x0	
ECRC_CHECK_EN (R)	8	0x0	

NB_PCIE_HDR_LOG0 - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x16C			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	

NB_PCIE_HDR_LOG1 - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x170			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	

NB_PCIE_HDR_LOG2 - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x174			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	

NB_PCIE_HDR_LOG3 - R - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x178			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	

NB_PCIE_ROOT_ERR_CMD - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x17C			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_REP_EN	0	0x0	
NONFATAL_ERR_REP_EN	1	0x0	
FATAL_ERR_REP_EN	2	0x0	

NB_PCIE_ROOT_ERR_STATUS - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x180			
Field Name	**Bits**	**Default**	**Description**
ERR_CORR_RCVD	0	0x0	
MULT_ERR_CORR_RCVD	1	0x0	
ERR_FATAL_NONFATAL_RCVD	2	0x0	
MULT_ERR_FATAL_NONFATAL_RCVD	3	0x0	
FIRST_UNCORRECTABLE_FATAL	4	0x0	
NONFATAL_ERROR_MSG_RCVD	5	0x0	
FATAL_ERROR_MSG_RCVD	6	0x0	
ADV_ERR_INT_MSG_NUM (R)	31:27	0x0	

NB_PCIE_ERR_SRC_ID - RW - 32 bits - pcieConfigDev[12:2], pcieConfigDev11, pcieConfigDev12, pcieConfigDev2, pcieConfigDev3, pcieConfigDev4, pcieConfigDev5, pcieConfigDev6, pcieConfigDev7, pcieConfigDev8,pcieConfigDev9:0x184			
Field Name	**Bits**	**Default**	**Description**
ERR_COR_SRC_ID (R)	15:0	0x0	
ERR_FATAL_NONFATAL_SRC_ID (R)	31:16	0x0	

2.3 APC Configuration Registers

APC_VENDOR_ID - R - 16 bits - apcconfig:0x0			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID	15:0	0x1022	Vendor Identifier This 16-bit field identifies the manufacturer of the device: Advanced Micro Devices, Inc.

APC_DEVICE_ID - R - 16 bits - apcconfig:0x2			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x9602	Device Identifier This 16-bit field is assigned by the device manufacturer and identifies the type of device. The current northbridge Device ID assignment is 7912

APC_COMMAND - RW - 16 bits - apcconfig:0x4			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN	0	0x0	I/O Access Enable This bit is always 0 because the RS780 does not respond to I/O cycles on the PCI Bus. 0=Disable 1=Enable
MEM_ACCESS_EN	1	0x0	Memory Access Enable Controls whether PCI memory accesses to system memory are accepted 0=Disable 1=Enable
BUS_MASTER_EN	2	0x0	Bus Master Enable This bit is always set, indicating that the RS780 is allowed to act as a bus master on the PCI Bus. 0=Disable 1=Enable
SPECIAL_CYCLE_EN (R)	3	0x0	Special Cycle This bit is always 0 because the RS780 ignores PCI special cycles. 0=Disable 1=Enable
MEM_WRITE_INVALIDATE_EN (R)	4	0x0	Memory Write and Invalidate Enable This bit is always 0 because the RS780 does not generate memory write and invalidate commands. 0=Disable 1=Enable
PAL_SNOOP_EN (R)	5	0x0	VGA Palette Snoop Enable This bit is always 0 indicating that the RS780 does not snoop the VGA palette address range. 0=Disable 1=Enable

PARITY_ERROR_EN (R)	6	0x0	Parity Error Response This bit is always 0 because the RS780 does not report data parity errors. 0=Disable 1=Enable
Reserved0 (R)	7	0x0	0=Disable 1=Enable
SERR_EN	8	0x0	System Error Enable Controls the assertion of SERR# 0=Disable 1=Enable
FAST_B2B_EN (R)	9	0x0	Fast Back-to-Back to Different Devices Enable This bit is always 0, because the RS780 does not allow generation of fast back-to-back transactions to different agents. 0=Disable 1=Enable
Reserved (R)	15:10	0x0	This bit is reserved in PCI 2.3, hardwire to 0.
The AGP/PCI Command and Status register provides coarse control over the PCI-PCI bridge function within the RS780. This register controls the ability to generate and respond to PCI cycles on both the AGP bus and the PCI bus.			

APC_STATUS - RW - 16 bits - apcconfig:0x6			
Field Name	**Bits**	**Default**	**Description**
Reserved (R)	3:0	0x0	
CAP_LIST (R)	4	0x1	Capabilities List This bit is set to indicate that this device's configuration space supports a capabilities list.
PCI_66_EN (R)	5	0x1	66-MHz Capable Indicate that the RS780 supports 66 MHz PCI operation
UDF_EN (R)	6	0x0	User-Definable Features This bit is always 0 indicating that UDF is not supported by the RS780. 0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	Fast Back-to-Back Capable This bit is always 0 indicating that the RS780, as a target, is not capable of accepting fast back-to-back transactions when the transactions are not to the same agent.
DEVSEL_TIMING (R)	10:9	0x1	DEVSEL# Timing Defines the timing of DEVSEL# on the RS780. The device only supports medium DEVSEL# timing.
SIGNAL_TARGET_ABORT (R)	11	0x0	Signaled Target Abort This bit is always 0 because the RS780 does not terminate transactions with target aborts. 0=No Abort 1=Target Abort asserted
RECEIVED_TARGET_ABORT (R)	12	0x0	Received Target Abort This bit is set whenever a CPU to PCI transaction (except for a special cycle) is terminated due to a target-abort. This bit is cleared by writing a 1. 0=Inactive 1=Active
RECEIVED_MASTER_ABORT (R)	13	0x0	Received Master Abort This bit is set whenever a CPU to PCI transaction (except for a special cycle) is terminated due to a master-abort. This bit is cleared by writing a 1. 0=Inactive 1=Active

SIGNALED_SYSTEM_ERROR	14	0x0	Signaled System Error This bit is set whenever the RS780 generates a System Error and asserts the SERR# line (currently only GART Error). This bit is cleared by writing a 1. 0=No Error 1=SERR asserted
PARITY_ERROR_DETECTED (R)	15	0x0	Detected Parity Error This bit is always 0 because the RS780 does not support data parity checking.
The AGP/PCI Command and Status register provides coarse control over the PCI-PCI bridge function within the RS780. This register controls the ability to generate and respond to PCI cycles on both the AGP bus and the PCI bus.			

APC_REVISION_ID - R - 8 bits - apcconfig:0x8			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Identifies the stepping number of the device
MAJOR_REV_ID	7:4	0x0	Identifies the revision number of the device
Revision Identification			

APC_REGPROG_INF - R - 8 bits - apcconfig:0x9			
Field Name	**Bits**	**Default**	**Description**
REG_LEVEL_PROG_INF	7:0	0x0	Indicates a PCI/PCI bridge.
Program Interface			

APC_SUB_CLASS - R - 8 bits - apcconfig:0xA			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS_INF	7:0	0x4	4=Indicates a PCI/PCI bridge
Sub-Class Code			

APC_BASE_CODE - R - 8 bits - apcconfig:0xB			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS_CODE	7:0	0x6	Indicates a general Bridge device
Class Code			

APC_CACHE_LINE - R - 8 bits - apcconfig:0xC			
Field Name	**Bits**	**Default**	**Description**
CACHE_LINE_SIZE	7:0	0x0	
Cache Line Size			

APC_LATENCY - RW - 8 bits - apcconfig:0xD			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER	7:0	0x0	Defines the minimum amount of time in PCI clock cycles that the bus master can retain ownership of the bus. This is mandatory for masters that are capable of performing a burst consisting of more than two data phases
Latency Timer			

APC_HEADER - R - 8 bits - apcconfig:0xE			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE	7:0	0x1	Bits [6:5] are 0, indicating that Type 00 Configuration Space Header format is supported.
Header Type			

APC_BIST - R - 8 bits - apcconfig:0xF			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP	3:0	0x0	
BIST_STRT	6	0x0	
BIST_CAP	7	0x0	
Built-in-self-test			

APC_SUB_BUS_NUMBER_LATENCY - RW - 32 bits - apcconfig:0x18			
Field Name	**Bits**	**Default**	**Description**
PRIMARY_BUS	7:0	0x0	Primary Bus Number Records the number of the PCI bus that the primary interface of the bridge is connected to. The bridge uses this to decode type 1 configuration transactions on the secondary interface that should be converted to Special Cycle transactions on the primary interface.
SECONDARY_BUS	15:8	0x0	Secondary Bus Number Records the number of the PCI bus that the secondary interface of the bridge is connected to. The bridge use this to determine when to respond to type 1 configuration transactions on the primary interface and convert them to type 0 transactions on the secondary interface.
SUB_BUS_NUMBER	23:16	0x0	Sub-Bus Number Records the number of the highest numbered PCI bus that is behind (or subordinate to) a bridge. The bridge uses this in conjuction with the Secondary Bus Number register to determine when to respond to type 1 configuration transactions on the primary interface and to pass them on to the secondary interface.
SECONDARY_LATENCY_TIMER	31:24	0x0	Secondary Latency Timer Adheres to the definition of the Latency Timer in the PCI Local Bus Specification but only applies to the secondary interface of a PCI to PCI bridge.
This Sub bus number and secondary bus latency timer			

APC_AGP_PCI_IOBASE_LIMIT - RW - 16 bits - apcconfig:0x1C			
Field Name	**Bits**	**Default**	**Description**
IO_BASE_R (R)	3:0	0x1	
IO_BASE	7:4	0x0	
IO_LIMIT_R (R)	11:8	0x1	
IO_LIMIT	15:12	0x0	

APC_AGP_PCI_STATUS - RW - 16 bits - apcconfig:0x1E			
Field Name	**Bits**	**Default**	**Description**
CAP_LIST (R)	4	0x0	
_66M (R)	5	0x1	
UDF_EN (R)	6	0x0	0=Disable 1=Enable
FAST_B2B_CAPABLE (R)	7	0x0	
DATA_PERR (R)	8	0x0	
DEVSEL_TIMING (R)	10:9	0x1	
SIGNAL_TARGET_ABORT (R)	11	0x0	0=No Abort 1=Target Abort asserted
TARGET_ABORT	12	0x0	0=Inactive 1=Active
MASTER_ABORT	13	0x0	0=Inactive 1=Active
SYSTEM_ERROR	14	0x0	0=No Error 1=SERR asserted
PARITY_ERROR (R)	15	0x0	

APC_AGP_PCI_MEMORY_LIMIT_BASE - RW - 32 bits - apcconfig:0x20			
Field Name	**Bits**	**Default**	**Description**
MEM_BASE_31_20	15:4	0x0	
MEM_LIMIT_31_20	31:20	0x0	

APC_AGP_PCI_PREFETCHABLE_LIMIT_BASE - RW - 32 bits - apcconfig:0x24			
Field Name	**Bits**	**Default**	**Description**
PREF_MEM_BASE_R (R)	3:0	0x1	0h=32-bit memory decoder 1h=64-bit memory decoder
PREF_MEM_BASE_31_20	15:4	0x0	Prefetchable Memory Base Address Prefetchable Memory Base Address defines the base address of the prefetchable address range used by the AGP target (graphics controller) where control registers and FIFO-like communication interfaces are mapped. Bits [15:4] correspond to address bits [31:20]. The lower 20 bits of the address are assumed to be 0. The memory address range adheres to 1-Mbyte alignment and granularity.
PREF_MEM_LIMIT_R (R)	19:16	0x1	0h=32-bit memory decoder, 1h=64-bit memory decoder.
PREF_MEM_LIMIT_31_20	31:20	0x0	Prefetchable Memory Limit Address Prefetchable Memory Limit Address defines the top address of the prefetchable address range used by the AGP target (graphics controller) where control registers and FIFO-like communication interfaces are mapped. The lower 20 bits of address are assumed to be 0xFFFFF. The memory address range adheres to 1-Mbyte alignment and granularity.
This register defines the base and the size of the prefetchable memory area within the AGP address space			

APC_AGP_PCI_PREFETCHABLE_BASE_Upper - RW - 32 bits - apcconfig:0x28			
Field Name	**Bits**	**Default**	**Description**
PREF_MEM_BASE_39_32	7:0	0x0	
This register defines the upper base of prefetchable memory area			

APC_AGP_PCI_PREFETCHABLE_LIMIT_Upper - RW - 32 bits - apcconfig:0x2C			
Field Name	**Bits**	**Default**	**Description**
PREF_MEM_LIMIT_39_32	7:0	0x0	
This register defines the upper limit of prefetchable memory area			

APC_CAPABILITIES_PTR - R - 32 bits - apcconfig:0x34			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR	7:0	0x44	This field contains a byte offset into a device's configuration space containing the first item in the capabilities list. If no next item exists, then it is set to null. It is hardwired to 0xB0 to indicate SSID capabilities.
Capabilities Pointer			

APC_MISC_DEVICE_CTRL - RW - 32 bits - apcconfig:0x40			
Field Name	**Bits**	**Default**	**Description**
INT_PIN_CTRL	0	0x0	0=Read-Only 1=Read-Writeable
ApcOrderDisable	1	0x0	If not set, the APC ordering rule is forced. If set, then the APC ordering rule is not forced. 0=Enable 1=Disable
ApcP2PDis	2	0x0	If not set, P2P memory writes targeted at internal graphics is enabled. 0=Enable 1=Disable
ApcIntSelMode	3	0x0	If set, Interrupt ABCE will be mapped as EFGH.
StpAgpMode	4	0x0	If not set, PMArbDis = STP_AGP. If set, only STP_AGP_Assert message could tigger STP_AGP.
ApcBMSetDis	5	0x0	If not set, falling edge of BIF_MST_IDLE# will trigger BM_Set message if BM_STS was 0 (BMMsgEn has to be set first to enable BM_Set message generation) 0=Enable 1=Disable
ApcBMSetDis_AGPBUSY	6	0x0	If not set, AGP_BUSY will trigger BM_Set message if BM_STS is 0 (BMMsgEn has to be set first to enable BM_Set message generation) 0=Enable 1=Disable

APC_HT_MSI_CAP - R - 32 bits - apcconfig:0x44			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x8	
CAP_POINTER	15:8	0xb0	
EN	16	0x1	
Fixd	17	0x1	
RESERVED_26_18	26:18	0x0	
CAPABILITY_TYPE	31:27	0x15	

APC_ADAPTER_ID_W - RW - 32 bits - apcconfig:0x4C			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x1022	
SUBSYSTEM_ID	31:16	0x9602	
Subsystem Vendor ID and Subsystem ID write register			

APC_SSID_CAP_ID - R - 32 bits - apcconfig:0xB0			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0xd	CapID
NEXT_PTR	15:8	0x0	Next Pointer Pointer to the next item in the capabilities list.
Reserved	31:16	0x0	
This read-only register describes the SSID implemented (1.2)			

APC_SSID - R - 32 bits - apcconfig:0xB4			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID *(mirror of APC_ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)*	15:0	0x0	
SUBSYSTEM_ID *(mirror of APC_ADAPTER_ID_W:SUBSYSTEM_ID)*	31:16	0x0	
Subsystem Vendor ID and Subsystem ID register			

2.4 Clock Configuration Registers

OSC_CONTROL - RW - 32 bits - clkconfig:0x40			
Field Name	**Bits**	**Default**	**Description**
OSC_EN	0	0x1	SCRATCH: Can write and read to this register, but it controls nothing. 0=Disable 1=Enable
XTAL_LOW_GAIN	1	0x0	SCRATCH: Can write and read to this register, but it controls nothing. 0=High Gain 1=Low Gain
Reserved0 (R)	3	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPU_STOP_ENABLE	4	0x0	SCRATCH: Can write and read to this register, but it controls nothing. 0=Disable 1=Enable
DC_STOP_ENABLE	5	0x0	SCRATCH: Can write and read to this register, but it controls nothing. 0=Disable 1=Enable
GFX_REFCLK_OE_TOGGLE	6	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
GPP_REFCLK_OE_TOGGLE	7	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
SB_REFCLK_OE_TOGGLE	8	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
Reserved1 (R)	11	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPUCLK_SE_OE_TOGGLE	12	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPUCLK_DIFF_OE_TOGGLE	13	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
REF_14M_OE_TOGGLE	14	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
ON_CHIP_CLOCK_GENERATOR (R)	18	0x1	SCRATCH: Can write and read to this register, but it controls nothing. 0=External clock 1=Internal clock
SYSCLK_OE_TOGGLE	19	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
MEMCLK_OE_TOGGLE	20	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
Scratch register			

CPLL_CONTROL - RW - 32 bits - clkconfig:0x44			
Field Name	**Bits**	**Default**	**Description**
CPLL_REFSEL	0	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_REF_DELAY	1	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_VCO_DELAY	2	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_SKEW4X	5:3	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_SKEW2X	8:6	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_SKEW1X_CORE	11:9	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_CTL	16:12	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CDLL_FREQ_SEL	20:17	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_LF_MODE	24:21	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
RESERVED	27:25	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_MODE (R)	31:28	0x0	SCRATCH: Can write and read to this register, but it controls nothing.

MC_CLK_CNTRL - RW - 16 bits - clkconfig:0x58			
Field Name	**Bits**	**Default**	**Description**
MC_CLKSPEED	1:0	0x0	Frequency of Memory Controller clock 0=66 MHz 1=100 MHz 2=133 MHz 3=undefined
MC_USE_CLKSPEED	2	0x0	Matches MC clock to frontside bus or uses register value. 0=Use fronside bus clk speed 1=Use MC_CLKSPEED value
Control registers for Memory Controller clock speed			

DELAY_SET_IOC_CCLK - RW - 32 bits - clkconfig:0x5C			
Field Name	**Bits**	**Default**	**Description**
DELAY_SET_ioc_cclk_mst	4:0	0x2	SCRATCH: Can write and read to this register, but it controls nothing.
DELAY_SET_ioc_cclk_slv	9:5	0x2	SCRATCH: Can write and read to this register, but it controls nothing.
Delay register			

MC_CLK_INDEX - RW - 32 bits - clkconfig:0x60			
Field Name	**Bits**	**Default**	**Description**
MC_CLK_IND_ADDR	17:0	0x0	
spare_31_18 (R)	31:18	0x0	

MC_CLK_DATA - RW - 32 bits - clkconfig:0x64			
Field Name	**Bits**	**Default**	**Description**
MC_CLK_IND_DATA	31:0	0x0	

CT_DISABLE_BIU - RW - 32 bits - clkconfig:0x68			
Field Name	**Bits**	**Default**	**Description**
BIU_NB1_CPUSTOP_DIS	0	0x1	
BIU_NB2_CPUSTOP_DIS	1	0x1	
BIU_CCLK_C3	2	0x1	
BIU_MCLK_C3	3	0x1	
BIU_CCLK_IO_PAD	4	0x1	
SYNC_DBL_FLP_EN	5	0x0	
DELAY_SET_gpp_cclk	10:6	0x2	
DELAY_SET_gpp_mclk	15:11	0x2	
iCFG_CT_DISABLE_BIU_IO_CCLK4X_P	16	0x1	
iCFG_CT_DISABLE_BIU_IO_CCLK4X_N	17	0x1	
Disable BIU Control			

PLL_VOLTAGE_REG_CNTL - RW - 32 bits - clkconfig:0x6C			
Field Name	**Bits**	**Default**	**Description**
NB_RSBEN	0	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
NB_REG_OVERRIDE	1	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
NB_RBGADJ	7:4	0x8	SCRATCH: Can write and read to this register, but it controls nothing.
Scratch register			

CPLL_CONTROL3 - RW - 32 bits - clkconfig:0x70			
Field Name	**Bits**	**Default**	**Description**
DLL_BIAS	2:0	0x1	SCRATCH: Can write and read to this register, but it controls nothing.
DLL_CPP	4:3	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
DLL_CPN	6:5	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
VCOREF	8:7	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CALREF	10:9	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
SKEW_REF	12:11	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
SKEW_FB	14:13	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
REF_DELAY	19:15	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
FB_DELAY	24:20	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
RESERVED	31:25	0x1	SCRATCH: Can write and read to this register, but it controls nothing.
cpp control3			

GC_CLK_CNTRL - RW - 8 bits - clkconfig:0x74			
Field Name	**Bits**	**Default**	**Description**
spare_0 (R)	0	0x0	
GC_STATE (R)	4:3	0x0	To restart the GC do the following: (1) Clear CG_BCLKSTATE to force the internal BCLK (in GC) to run (2) Write BIF:PM_STATUS[PMI_POWER_STATE] to 2'b00 to start WAKEUP sequence (3) Wait until GC_STATE reports a value of 2'b00 (4) Wait 100 us before sending more GC requests to GC (5) Set bit CG_BCLKSTATE to allow state transition. 0=GC has transitioned to D0 1= 2= 3=GC has transitioned to suspend and 61us later all BCLK in the GC will stop
spare_5 (R)	5	0x0	
Graphics Controller Clock Control			

MC_DATA_DLL_CNTRL_A - RW - 32 bits - clkconfig:0x80			
Field Name	**Bits**	**Default**	**Description**
DLL_DA_IN_TRIM0	3:0	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
DLL_DA_OUT_TRIM0	7:4	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
DLL_DA_IN_TRIM1	11:8	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
DLL_DA_OUT_TRIM1	15:12	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
DLL_DA_IN_TRIM2	19:16	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
DLL_DA_OUT_TRIM2	23:20	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
DLL_DA_IN_TRIM3	27:24	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
DLL_DA_OUT_TRIM3	31:28	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
Scratch register			

SCRATCH_CLKCFG - RW - 32 bits - clkconfig:0x84			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	Can write and read to this register, but it controls nothing.
Scratch Register for the CLKCFG register space.			

CG_MISC_INPUT_1 - RW - 32 bits - clkconfig:0x78			
Field Name	**Bits**	**Default**	**Description**
CG_MISC_INPUT_2	31:0	0x0	
Misc input for CG			

CG_MISC_INPUT_2 - RW - 32 bits - clkconfig:0x7C			
Field Name	**Bits**	**Default**	**Description**
CG_MISC_INPUT_2	31:0	0x0	Misc input for CG
Misc input for CG			

MC_ACMD_DLL_CNTRL_A - RW - 8 bits - clkconfig:0x88			
Field Name	**Bits**	**Default**	**Description**
DLL_CA_IN_TRIM	3:0	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
DLL_CA_OUT_TRIM	7:4	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
Scratch register			

MC_ACMD_DLL_CNTRL_B - RW - 8 bits - clkconfig:0x89			
Field Name	**Bits**	**Default**	**Description**
DLL_CB_IN_TRIM	3:0	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
DLL_CB_OUT_TRIM	7:4	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
Scratch register			

CLKGATE_DISABLE2 - RW - 32 bits - clkconfig:0x8C			
Field Name	**Bits**	**Default**	**Description**
spare_0	0	0x1	
spare_1	1	0x1	
spare_2	2	0x1	
spare_3	3	0x1	
spare_4	4	0x1	
spare_5	5	0x1	
spare_8	8	0x1	
spare_9	9	0x1	
spare_10	10	0x1	
spare_11	11	0x1	
spare_12	12	0x1	
CLKGATE_DIS_IOC_CCLK_MST	13	0x1	Disables clock gating for IOC MST LCLK branch
CLKGATE_DIS_IOC_CCLK_SLV	14	0x1	Disables clock gating for IOC SLV LCLK branch
spare_18	18	0x1	
GFX_SCLK_DISABLE	20	0x0	Disables GFX engine clock
GFX_DISPCLK_DISABLE	21	0x0	Disables GFX display clock
spare_22	22	0x1	
spare_23	23	0x1	
iCFG_CT_DISABLE_LCLK_BIF	24	0x1	
CFG_CT_DISABLE_MCLK_BIF	25	0x1	Disables clock gating for MCLK going to BIF branch
DISABLE_DYNAMIC_CLK_GATING	26	0x1	
MC_DELAY_TIMER_EXTEND	30	0x0	Extends the delay timer for MEMORY clocks 0=16 clocks 1=32 clocks
dis_watchdog_timer	31	0x1	
Register Description.			

CG_MISC_INPUT_3 - RW - 32 bits - clkconfig:0x90			
Field Name	**Bits**	**Default**	**Description**
CG_cc_max_sclk	7:0	0xff	
CG_cc_overclock_dis	8	0x1	
CFG_DISABLE_DYNAMIC_SCLK_GATING	9	0x1	
Register Description.			

CLKGATE_DISABLE - RW - 32 bits - clkconfig:0x94			
Field Name	**Bits**	**Default**	**Description**
spare_0	0	0x1	0=Enable 1=Disable
CPUCLK_STOP_MISC	1	0x1	Disables CPUCLK_STOP stopping CFG and IG2R6 BCLK and CCLK 0=Enable 1=Disable
spare_2	2	0x1	0=Enable 1=Disable
spare_3	3	0x1	0=Enable 1=Disable
spare_4	4	0x1	0=Enable 1=Disable
SPARE_7	7	0x0	0=Enable 1=Disable
ENABLE_ANALOG_DLLs	8	0x1	SCRATCH: Can write and read to this register, but it controls nothing. 0=Disable 1=Enable
spare_9	9	0x1	0=Enable 1=Disable
spare_10	10	0x1	0=Enable 1=Disable
spare_11	11	0x1	0=Enable 1=Disable
spare_12	12	0x1	0=Enable 1=Disable
spare_13	13	0x1	0=Enable 1=Disable
spare_14	14	0x1	0=Enable 1=Disable
spare_15	15	0x1	0=Enable 1=Disable
CLKGATE_DIS_GFX_TXCLK	16	0x1	Disables clock gating for GFX_LCLK branch
spare_17	17	0x1	0=Enable 1=Disable
spare_18	18	0x1	0=Enable 1=Disable
spare_19	19	0x1	0=Enable 1=Disable
spare_20	20	0x1	0=Enable 1=Disable
spare_21	21	0x1	0=Enable 1=Disable
spare_22	22	0x1	0=Enable 1=Disable
spare_23	23	0x1	0=Enable 1=Disable
CLKGATE_DIS_GPPSB_LCLK	24	0x1	0=Enable 1=Disable
spare_25	25	0x1	0=Enable 1=Disable
CLKGATE_IOC_GFX	26	0x1	0=Enable 1=Disable
CLKGATE_IOC_SLV_GFX	27	0x1	0=Enable 1=Disable
CLKGATE_DIS_CFG_S1X	28	0x1	Disables clock gating for SCLK1X going to cfg 0=Enable 1=Disable

spare	29	0x1	0=Enable 1=Disable
DEEP_S1_DISABLE	30	0x1	If enabled, S1 mode (CPU_STOP active) will power down SPLL, BPLL, and MPLL. Otherwise, S1 mode will gate clocks only. 0=Enable 1=Disable
DISABLE_CLKGATE_GPP2_LCLK	31	0x1	0=Enable 1=Disable
Register Description.			

CPLL_CONTROL2 - RW - 32 bits - clkconfig:0x98			
Field Name	**Bits**	**Default**	**Description**
CPLL_SKEW1XA	2:0	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_SKEW1XB	5:3	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_IOBUFSEL	6	0x1	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_SPARE	11:7	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_FLOAT	16:12	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
RESERVED	20:17	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CPLL_CP_RB (R)	24:21	0x0	Not used
CPLL_VCO_MODE_RB (R)	26:25	0x0	Not used
CPLL_FWDIV_RB (R)	28:27	0x0	Not used
STRAP_FREQ_SPEED (R)	31:29	0x0	Not used
cppl control2			

NBCLK_IO_CONTROL - RW - 32 bits - clkconfig:0xBC			
Field Name	**Bits**	**Default**	**Description**
SYSCLK_SP	1:0	0x3	SCRATCH: Can write and read to this register, but it controls nothing.
SYSCLK_SPB	3:2	0x3	SCRATCH: Can write and read to this register, but it controls nothing.
SYSCLK_SRP	5:4	0x3	SCRATCH: Can write and read to this register, but it controls nothing.
SYSCLK_SRPB	7:6	0x3	SCRATCH: Can write and read to this register, but it controls nothing.
SYS_FBCLKOUT_SP	9:8	0x3	SCRATCH: Can write and read to this register, but it controls nothing.
SYS_FBCLKOUT_SPB	11:10	0x3	SCRATCH: Can write and read to this register, but it controls nothing.
SYS_FBCLKOUT_SRP	13:12	0x3	SCRATCH: Can write and read to this register, but it controls nothing.
SYS_FBCLKOUT_SRPB	15:14	0x3	SCRATCH: Can write and read to this register, but it controls nothing.
IOSPLL_IPWDN	16	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
IOSPLL_IBYPASS	17	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
IOSPLL_IREF_DELAY	18	0x0	SCRATCH: Can write and read to this register, but it controls nothing.

IOSPLL_IVCO_DELAY	19	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
IOSPLL_IICP	21:20	0x1	SCRATCH: Can write and read to this register, but it controls nothing.
IOSPLL_ICPBW	22	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
IOSPLL_IVCOBW	23	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
IOSPLL_ISKEW_4X	24	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
IOSPLL_IPLL_CNTL	31:28	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
Scratch register			

CLK_TOP_THERMAL_ALERT_INTR_EN - RW - 32 bits - clkconfig:0xC0

Field Name	Bits	Default	Description
spare_0	0	0x0	
spare_1_31	31:1	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
Scratch register			

CLK_TOP_THERMAL_ALERT_STATUS - RW - 32 bits - clkconfig:0xC4

Field Name	Bits	Default	Description
spare_0_31	31:0	0x0	
Scratch register			

CLK_TOP_THERMAL_ALERT_WAIT_WINDOW - RW - 32 bits - clkconfig:0xC8

Field Name	Bits	Default	Description
spare_0_29	29:0	0x0	
spare_30_31	31:30	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
Scratch register			

clk_top_pwm3_ctrl - RW - 32 bits - clkconfig:0xCC

Field Name	Bits	Default	Description
ct_pwm3_en	0	0x0	
ct_pwm3_NumberOfCyclesInPeriod	12:1	0x0	
ct_pwm3_NumberOfHighCyclesInPeriod	24:13	0x0	Bit [10]=1 to stop efuse clock Bit [11]=1 to stop strap clock
ct_pwm3_io_oe	25	0x0	
This register is for pwm3_ctrl			

CLK_TOP_PWM7_CNTL - RW - 32 bits - clkconfig:0x48			
Field Name	**Bits**	**Default**	**Description**
PWM_HIGH_VOLTAGE	11:0	0x0	
PWM_TIMER_VAL	15:12	0x0	
RESERVED	30:16	0x0	
CLK_TOP_PWM_EN	31	0x0	

clk_top_pwm4_ctrl - RW - 32 bits - clkconfig:0x4C			
Field Name	**Bits**	**Default**	**Description**
ct_pwm4_en	0	0x0	
ct_pwm4_NumberOfCyclesInPeriod	12:1	0x0	
ct_pwm4_NumberOfHighCyclesInPeriod	24:13	0x0	
ct_pwm4_io_oe	25	0x0	

clk_top_pwm5_ctrl - RW - 32 bits - clkconfig:0x50			
Field Name	**Bits**	**Default**	**Description**
ct_pwm5_en	0	0x0	
ct_pwm5_NumberOfCyclesInPeriod	12:1	0x0	
ct_pwm5_NumberOfHighCyclesInPeriod	24:13	0x0	
ct_pwm5_io_oe	25	0x0	

clk_top_pwm6_ctrl - RW - 32 bits - clkconfig:0x54			
Field Name	**Bits**	**Default**	**Description**
ct_pwm6_en	0	0x0	
ct_pwm6_NumberOfCyclesInPeriod	12:1	0x0	
ct_pwm6_NumberOfHighCyclesInPeriod	24:13	0x0	
ct_pwm6_io_oe	25	0x0	

GPIO_ctrl - RW - 32 bits - clkconfig:0xDC			
Field Name	**Bits**	**Default**	**Description**
GPIO_1_OE	0	0x0	
GPIO_1_A	1	0x0	
GPIO_1_Y (R)	2	0x0	
GPIO_2_OE	4	0x0	
GPIO_2_A	5	0x0	
GPIO_2_Y (R)	6	0x0	
GPIO_3_OE	8	0x0	
GPIO_3_A	9	0x0	
GPIO_3_Y (R)	10	0x0	
GPIO_4_OE	12	0x0	
GPIO_4_A	13	0x0	

GPIO_4_Y (R)	14	0x0	
GPIO_5_OE	16	0x0	
GPIO_5_A	17	0x0	
GPIO_5_Y (R)	18	0x0	

clk_top_spare_pll - RW - 32 bits - clkconfig:0xD0			
Field Name	**Bits**	**Default**	**Description**
ct_spare_pll_ctl	31:0	0x0	
This register is a spare			

CLK_CFG_HTPLL_CNTL - RW - 32 bits - clkconfig:0xD4			
Field Name	**Bits**	**Default**	**Description**
CLK_CFG_HTPLL_IPCP	2:0	0x4	
CLK_CFG_HTPLL_IDB1CLK0SC	5:3	0x5	
CLK_CFG_HTPLL_IDB1CLK3SC	8:6	0x5	
CLK_CFG_HTPLL_IDB4CLKSC	11:9	0x5	
CLK_CFG_HTPLL_ITXCLKSC	14:12	0x7	
CLK_CFG_HTPLL_IVCO_MODE	16:15	0x0	
CLK_CFG_HTPLL_IPLL_CTL	21:17	0x0	
CLK_CFG_HTPLL_ITMONEN	22	0x0	
CLK_CFG_HTPLL_PWDN	23	0x0	
iCFG_HT_HTPLL_ITXCLKINV	24	0x0	
iCFG_HT_HTPLL_ICLK0SEL	25	0x0	
iCFG_HT_HTPLL_ICLK3SEL	26	0x0	
iCFG_HT_HTPLL_IVCOREF	28:27	0x0	
iCFG_HT_HTPLL_ICALREF	30:29	0x0	
iCFG_HT_HTPLL_ITSTCLK	31	0x0	

CLK_TOP_SPARE_A - RW - 32 bits - clkconfig:0xE0			
Field Name	**Bits**	**Default**	**Description**
MCLK_SWITCH_GFX_EN	0	0x0	
spare_7_1	7:1	0x0	Bit [1]=REG_ENABLE_ASYNC_OPT Bit [2]=Switch MC GUI & HOST IDLES to 1
CFG_B1X_CPUSTOP_DIS	8	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
CFG_S1X_CPUSTOP_DIS	9	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
spare_15_10	15:10	0x0	
OSC_PU	16	0x1	SCRATCH: Can write and read to this register, but it controls nothing.
OSC_PD	17	0x0	SCRATCH: Can write and read to this register, but it controls nothing.
OSC_SRP	18	0x1	SCRATCH: Can write and read to this register, but it controls nothing.
OSC_SRN	19	0x1	SCRATCH: Can write and read to this register, but it controls nothing.
OSC_SP	23:20	0x4	SCRATCH: Can write and read to this register, but it controls nothing.
OSC_SN	27:24	0x7	SCRATCH: Can write and read to this register, but it controls nothing.
spare_31_28	31:28	0x0	
Misc. register for clk_top.			

CLK_TOP_SPARE_B - RW - 32 bits - clkconfig:0xE4			
Field Name	**Bits**	**Default**	**Description**
CLK_TOP_SPAREB	31:0	0xc	Bits [7:0]=oscin pad control (bits [7:5] inverted on the pad) Bits [9:8]=spll_gfx_macro control bits (bit [8] inverted) Bits [11:10]=LVM control Bits [15:14]=mfreq_cntl
Misc. register for clk_top			

CLK_TOP_SPARE_C - RW - 32 bits - clkconfig:0xE8			
Field Name	**Bits**	**Default**	**Description**
CLK_TOP_SPAREC	31:0	0x0	Bit [0]=Extend IOC PM timer Bits [8:2]=HTPLL ILF_MODE [8:2] Bit [12]=Disable htiu LCLK RX clock gating Bit [13]=Disable htiu dynamic LCLK RX clock gating Bit [14]=Disable TXPHY dynamic clocking Bi t[16]=HTPLL_IPCP[3] Bit [17]=Stops clock branch to IOC GFX
Misc. register for clk_top			

CLK_TOP_SPARE_D - RW - 32 bits - clkconfig:0xEC			
Field Name	**Bits**	**Default**	**Description**
LOAD_EEPROM_STRAPSb (R)	0	0x1	
STRAP_SIDE_PORTb (R)	1	0x1	
CLK_TOP_SPARED_31_2 (R)	31:2	0x0	
Misc. status register for clk_top			

clk_top_pwm1_ctrl - RW - 32 bits - clkconfig:0xB0			
Field Name	**Bits**	**Default**	**Description**
ct_pwm1_NumberOfCyclesInPeriod	11:0	0x0	
ct_pwm1_NumberOfHighCyclesInPeriod	23:12	0x0	
ct_pwm1_en	24	0x0	
ct_pwm1_io_oe	25	0x0	
clk_top_pwm1_ctrl			

clk_top_pwm2_ctrl - RW - 32 bits - clkconfig:0xB4			
Field Name	**Bits**	**Default**	**Description**
ct_pwm2_NumberOfCyclesInPeriod	11:0	0x0	
ct_pwm2_NumberOfHighCyclesInPeriod	23:12	0x0	
ct_pwm2_en	24	0x0	
ct_pwm2_io_oe	25	0x0	
clk_top_pwm2_ctrl			

clk_top_test_ctrl - RW - 32 bits - clkconfig:0xB8			
Field Name	**Bits**	**Default**	**Description**
ct_test_clk_sel	5:0	0x0	
ct_test_clk_en	6	0x0	
ct_test_clk_oe	7	0x0	
ct_test_clk_spare	31:16	0x0	
clk_top_test_ctrl			

CFG_CT_CLKGATE_HTIU - RW - 32 bits - clkconfig:0xF8			
Field Name	**Bits**	**Default**	**Description**
DISABLE_CLKGATE_HTIU_LCLK_HTM	0	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_HTM	1	0x1	
DISABLE_CLKGATE_HTIU_LCLK_RP	2	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_RP	3	0x1	
DISABLE_CLKGATE_HTIU_LCLK_FCB	4	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_FCB	5	0x1	
DISABLE_CLKGATE_HTIU_LCLK_GCM	6	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_GCM	7	0x1	
DISABLE_CLKGATE_HTIU_LCLK_NB1	8	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_NB1	9	0x1	
DISABLE_CLKGATE_HTIU_LCLK_NB2	10	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_NB2	11	0x1	
ILF_MODE	13:12	0x0	
DISABLE_CLKGATE_HTIU_LCLK_RX	14	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_RX	15	0x1	
DISABLE_CLKGATE_HTIU_LCLK_NB3	16	0x1	
DISABLE_DYNAMIC_CLKGATE_HTIU_LCLK_NB3	17	0x1	

CLK_MISC_INDEX - RW - 32 bits - clkconfig:0xF0			
Field Name	**Bits**	**Default**	**Description**
CLK_MISC_IND_ADDR	7:0	0x0	
CLK_MISC_IND_WR_EN	8	0x0	0=Disable writes to CLK_MISC_DATA 1=Enable writing to CLK_MISC_DATA

CLK_MISC_DATA - RW - 32 bits - clkconfig:0xF4			
Field Name	**Bits**	**Default**	**Description**
CLKMISCDATA	31:0	0x0	

ILA_CLK_INDEX - RW - 32 bits - clkconfig:0x9C			
Field Name	**Bits**	**Default**	**Description**
ILA_CLK_IND_ADDR	6:0	0x0	
ILA_CLK_IND_WR_EN	7	0x0	0=Disable writes to ILA_CLK_DATA 1=Enable writing to ILA_CLK_DATA

ILA_CLK_DATA - RW - 32 bits - clkconfig:0xA0			
Field Name	**Bits**	**Default**	**Description**
ILA_CLK_DATA	31:0	0x0	

2.5 Graphics Controller Registers

VENDOR_ID - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x0			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID (R)	15:0	0x0	This field identifies the manufacturer of the device. 0FFFFh is an invalid value for Vendor ID.
Vendor Identification			

DEVICE_ID - R - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x2			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x0	This field identifies the particular device. This identifier is allocated by the vendor.
Device Identification			

COMMAND - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x4			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN	0	0x0	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. The state after RST# is 0. 0=Disable 1=Enable
MEM_ACCESS_EN	1	0x0	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. the state after RST# is 0. 0=Disable 1=Enable
BUS_MASTER_EN	2	0x0	Controls the ability of a PCI Express Endpoint to issue Memory and I/O Read/Write Requests, and the ability of a Root or Switch Port to forward Memory and I/O Read/Write Requests in the upstream direction. 0=Disable 1=Enable
SPECIAL_CYCLE_EN (R)	3	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
MEM_WRITE_INVALIDATE_EN (R)	4	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
PAL_SNOOP_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
PARITY_ERROR_RESPONSE	6	0x0	Parity Error Response. The default value of this field is 0. 0=Disable 1=Enable
AD_STEPPING (R)	7	0x0	Address and Data Stepping. Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable

SERR_EN	8	0x0	Enables the reporting of Non-fatal and Fatal errors detected by the device to the Root Complex. 0=Disable 1=Enable
FAST_B2B_EN (R)	9	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
INT_DIS	10	0x0	Controls the ability of a PCI Express device to generate INTx interrupt Messages. When set, devices are prevented from generating INTx interrupt Messages. The default value is 0. 0=Enable 1=Disable
The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.			

STATUS - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x6			
Field Name	**Bits**	**Default**	**Description**
INT_STATUS (R)	3	0x0	Indicates that an INTx interrupt Message is pending internally to the device.
CAP_LIST (R)	4	0x1	Indicates the presence of an extended capability list item. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit must be set to 1.
PCI_66_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0.
UDF_EN (R)	6	0x0	User Defined Status Enable 0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	Does not apply to PCI Express. Hardwired to 0.
MASTER_DATA_PARITY_ERROR	8	0x0	This bit is set by Requestor if its Parity Error Enable bit is set and either of the following two conditions occurs: (1) Requestor receives a Completion marked poisoned (2) Requestor poisons a write Request 0=Inactive 1=Active
DEVSEL_TIMING (R)	10:9	0x0	Does not apply to PCI Express. Hardwired to 0.
SIGNAL_TARGET_ABORT (R)	11	0x0	This bit is set when a device completes a Request using Completer Abort Completion Status. 0=No Abort 1=Target Abort
RECEIVED_TARGET_ABORT	12	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=Inactive 1=Active
RECEIVED_MASTER_ABORT	13	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=Inactive 1=Active
SIGNALED_SYSTEM_ERROR	14	0x0	This bit must be set whenever the device asserts SERR#. 0=No Error 1=SERR assert
PARITY_ERROR_DETECTED	15	0x0	This bit is set when a device sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1.
The Status register is used to record status information for PCI bus related events.			

REVISION_ID - R - 8 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x8			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Major revision ID. Set by the vendor.
MAJOR_REV_ID	7:4	0x0	Minor revision ID. Set by the vendor.
Specifies a device specific revision identifier. The value is chosen by the vendor.			

PROG_INTERFACE - R - 8 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x9			
Field Name	**Bits**	**Default**	**Description**
PROG_INTERFACE	7:0	0x0	Unused (only used in a test environment).
Register-Level Programming Interface Register			

SUB_CLASS - R - 8 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0xA			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS	7:0	0x0	The Class Code register is read-only and is used with the Base Class Code to identify the specific type of device.
Sub Class Code Register			

BASE_CLASS - R - 8 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0xB			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS	7:0	0x0	The Class Code register is read-only and is used to identify the generic function of the device.
Base Class Code Register			

CACHE_LINE - RW - 8 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0xC			
Field Name	**Bits**	**Default**	**Description**
CACHE_LINE_SIZE	7:0	0x0	This read/write register specifies the system cacheline size in units of DWORDs.
Cache Line Size Register			

LATENCY - RW - 8 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0xD			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER (R)	7:0	0x0	Primary/Master latency timer does not apply to PCI Express. Register is hardwired to 0.
Master Latency Timer Register			

HEADER - RW - 8 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0xE			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE (R)	6:0	0x0	Type 0 or Type 1 Configuration Space
DEVICE_TYPE (R)	7	0x0	Single function or multi function device 0=Single-Function Device 1=Multi-Function Device
Configuration Space Header			

BIST - RW - 8 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0xF			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP (R)	3:0	0x0	A value of 0 means the device has passed its test. Non-zero values mean the device failed. Device-specific failure codes can be encoded in the non-zero value.
BIST_STRT (R)	6	0x0	Write a 1 to invoke BIST. Device resets the bit when BIST is complete. Software should fail the device if BIST is not complete after 2 seconds.
BIST_CAP (R)	7	0x0	This bit is read-only and returns 1 the bridge supports BIST, otherwise 0 is returned
Built In Self Test Register used for control and status of built-in self tests			

BASE_ADDR_1 - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x10			
Field Name	**Bits**	**Default**	**Description**
BASE_ADDR	31:0	0x0	
PCI CFG BAR Registers			

BASE_ADDR_2 - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x14			
Field Name	**Bits**	**Default**	**Description**
BASE_ADDR	31:0	0x0	
PCI CFG BAR Registers			

BASE_ADDR_3 - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x18			
Field Name	**Bits**	**Default**	**Description**
BASE_ADDR	31:0	0x0	
PCI CFG BAR Registers			

BASE_ADDR_4 - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x1C			
Field Name	**Bits**	**Default**	**Description**
BASE_ADDR	31:0	0x0	
PCI CFG BAR Registers			

BASE_ADDR_5 - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x20			
Field Name	**Bits**	**Default**	**Description**
BASE_ADDR	31:0	0x0	
PCI CFG BAR Registers			

BASE_ADDR_6 - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x24			
Field Name	**Bits**	**Default**	**Description**
BASE_ADDR	31:0	0x0	
PCI CFG BAR Registers			

ROM_BASE_ADDR - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x30			
Field Name	**Bits**	**Default**	**Description**
BASE_ADDR	31:0	0x0	
PCI CFG BAR Registers			

CAP_PTR - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x34			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR (R)	7:0	0x50	Pointer to a linked list of additional capabilities implemented by this device. 50=Point to PM Capability
Capability Pointer			

INTERRUPT_LINE - RW - 8 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x3C			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_LINE	7:0	0xff	Interrupt Line register communicates interrupt line routing information.
Interrupt Line Register			

INTERRUPT_PIN - RW - 8 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x3D			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_PIN (R)	7:0	0x0	The Interrupt Pin is a read-only register that identifies the legacy interrupt Message(s) the device (or device function) uses. Note: Bits [7:3] of this field are hardwired to 0.
Interrupt Pin Register			

ADAPTER_ID - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x2C			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID *(mirror of ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)*	15:0	0x0	Subsystem Vendor ID. Specified by the vendor.
SUBSYSTEM_ID *(mirror of ADAPTER_ID_W:SUBSYSTEM_ID)*	31:16	0x0	Subsystem ID. Specified by the vendor.
Subsystem Vendor and Subsystem ID Register			

MIN_GRANT - RW - 8 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x3E			
Field Name	**Bits**	**Default**	**Description**
MIN_GNT (R)	7:0	0x0	Registers do not apply to PCI Express. Hardwired to 0.

MAX_LATENCY - RW - 8 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x3F			
Field Name	**Bits**	**Default**	**Description**
MAX_LAT (R)	7:0	0x0	Registers do not apply to PCI Express. Hardwired to 0.

ADAPTER_ID_W - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x4C			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x0	Subsystem Vendor ID. Specified by the vendor.
SUBSYSTEM_ID	31:16	0x0	Subsystem Vendor ID. Specified by the vendor.
Adapter ID			

PMI_CAP_LIST - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x50			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x1	Capability ID Must be set to 01h 1=PCIE Power Management Registers
NEXT_PTR (R)	15:8	0x58	Next Capability Pointer. The offset to the next PCI capability structure or 00h if no other items exist in the linked list of capabilities.
Power Management Capbility List			

PMI_CAP - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x52			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	2:0	0x3	Version 3=PMI Spec 1.2
PME_CLOCK (R)	3	0x0	Does not apply to PCI Express. Hardwired to 0.
DEV_SPECIFIC_INIT (R)	5	0x0	Device Specific Initialization
AUX_CURRENT (R)	8:6	0x0	AUX Current
D1_SUPPORT (R)	9	0x0	D1 Support 1=Support D1 PM State.
D2_SUPPORT (R)	10	0x0	D2 Support 1=Support D2 PM State.
PME_SUPPORT (R)	15:11	0x0	For a device, this indicates the power states in which the device may generate a PME.
Power Management Capabilities Register			

PMI_STATUS_CNTL - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x54			
Field Name	**Bits**	**Default**	**Description**
POWER_STATE	1:0	0x0	Power State
NO_SOFT_RESET (R)	3	0x0	
PME_EN (R)	8	0x0	PME Enable
DATA_SELECT (R)	12:9	0x0	Data Select
DATA_SCALE (R)	14:13	0x0	Data Scale
PME_STATUS (R)	15	0x0	PME Status
B2_B3_SUPPORT (R)	22	0x0	B2/B3 Support Does not apply to PCI Express. Hardwired to 0.
BUS_PWR_EN (R)	23	0x0	Bus Power/Clock Control Enable Does not apply to PCI Express. Hardwired to 0.
PMI_DATA (R)	31:24	0x0	Data
Power Management Status/Control Register			

PCIE_CAP_LIST - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x58			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x10	Indicates the PCI Express Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure. 10=PCI Express capable
NEXT_PTR (R)	15:8	0xa0	Next Capability Pointer. The offset to the next PCI capability structure or 00h if no other items exist in the linked list of capabilities.
The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 2.3 configuration space capability list.			

PCIE_CAP - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x5A			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	3:0	0x2	Indicates PCI-SIG defined PCI Express capability structure version number. 0=PCI Express Cap Version
DEVICE_TYPE (R)	7:4	0x0	Indicates the type of PCI Express logical device. 0=PCI Express Endpoint 1=Legacy PCI Express Endpoint 4=PCI Express Root Complex
SLOT_IMPLEMENTED (R)	8	0x0	This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot
INT_MESSAGE_NUM (R)	13:9	0x0	Interrupt Message Number.
TCS_ROUTING_SUPPORTED (R)	14	0x0	Trusted Configuration Routing supported.
The PCI Express Capabilities register identifies PCI Express device type and associated capabilities.			

DEVICE_CAP - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x5C			
Field Name	**Bits**	**Default**	**Description**
MAX_PAYLOAD_SUPPORT (R)	2:0	0x0	This field indicates the maximum payload size that the device can support for TLPs. 0=128B size
PHANTOM_FUNC (R)	4:3	0x0	This field indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers with the Tag identifier. 0=No Phantom Functions
EXTENDED_TAG (R)	5	0x1	This field indicates the maximum supported size of the Tag field as a Requester. 0=5 Bit Tag Supported 1=8 Bit Tag Supported
L0S_ACCEPTABLE_LATENCY (R)	8:6	0x0	This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state.
L1_ACCEPTABLE_LATENCY (R)	11:9	0x0	This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state.
ROLE_BASED_ERR_REPORTING (R)	15	0x0	0=Role-Based Error Reporting Disabled 1=Role-Based Error Reporting Enabled
CAPTURED_SLOT_POWER_LIMIT (R)	25:18	0x0	(Upstream Ports only). In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot.
CAPTURED_SLOT_POWER_SCALE (R)	27:26	0x0	Specifies the scale used for the Slot Power Limit Value.
FLR_CAPABLE (R)	28	0x0	This field indicates that a device is capable of initiating Function Level Resets.
The Device Capabilities register identifies PCI Express device specific capabilities.			

DEVICE_CNTL - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x60			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_EN	0	0x0	Controls the reporting of correctable errors. The default value of this field is 0. 0=Disable 1=Enable
NON_FATAL_ERR_EN	1	0x0	Controls the reporting of Non-fatal errors. The default value of this field is 0. 0=Disable 1=Enable
FATAL_ERR_EN	2	0x0	Controls the reporting of Fatal errors. The default value of this field is 0. 0=Disable 1=Enable
USR_REPORT_EN	3	0x0	Enables the reporting of Unsupported Requests. The default value of this field is 0. 0=Disable 1=Enable
RELAXED_ORD_EN	4	0x1	If this bit is set, the device is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. The default value of this bit is 1. 0=Disable 1=Enable
MAX_PAYLOAD_SIZE (R)	7:5	0x0	This field sets maximum TLP payload size for the device. The default value of this field is 000b. 0=128B size
EXTENDED_TAG_EN	8	0x0	Enables a device to use an 8-bit Tag field as a requester. If the bit is cleared, the device is restricted to a 5-bit Tag field. Default value of this field is 0. 0=Disable 1=Enable
PHANTOM_FUNC_EN (R)	9	0x0	Enables a device to use unclaimed functions as Phantom Functions to extend the number of outstanding transaction identifiers. If the bit is cleared, the device is not allowed to use Phantom Functions. 0=Disable 1=Enable
AUX_POWER_PM_EN (R)	10	0x0	Enables a device to draw AUX power independent of PME AUX power. 0=Disable 1=Enable
NO_SNOOP_EN	11	0x1	If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. Default value of this bit is 1. 0=Disable 1=Enable
MAX_REQUEST_SIZE (R)	14:12	0x0	Sets the maximum Read Request size for the Device as a Requester. Default value of this field is 010b. 0=128B size
BRIDGE_CFG_RETRY_EN (R)	15	0x0	0=Disable 1=Enable
The Device Control register controls PCI Express device specific parameters.			

DEVICE_STATUS - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x62			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR	0	0x0	Indicates status of correctable errors detected.
NON_FATAL_ERR	1	0x0	Indicates status of Nonfatal errors detected.
FATAL_ERR	2	0x0	Indicates status of Fatal errors detected.
USR_DETECTED	3	0x0	Indicates that the device received an Unsupported Request.
AUX_PWR (R)	4	0x0	Devices that require AUX power report this bit as set if AUX power is detected by the device.
TRANSACTIONS_PEND (R)	5	0x0	Endpoints: Indicates that the device has issued Non-Posted Requests which have not been completed. Root and Switch Ports: Indicates that a Port has issued Non-Posted Requests on its own behalf (using the Port's own Requester ID) which have not been completed.
The Device Status register provides information about PCI Express device specific parameters.			

LINK_CAP - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x64			
Field Name	**Bits**	**Default**	**Description**
LINK_SPEED (R)	3:0	0x1	Indicates the maximum Link speed of the given PCI Express Link. 1=2.5 Gb/s 2=5.0 Gb/s
LINK_WIDTH (R)	9:4	0x0	Indicates the maximum width of the given PCI Express Link. 1 = x1 2 = x2 4 = x4 8 = x8 12 = x12 16 = x16 32 = x32
PM_SUPPORT (R)	11:10	0x3	Indicates the level of ASPM supported on the given PCI Express Link.
L0S_EXIT_LATENCY (R)	14:12	0x1	Indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
L1_EXIT_LATENCY (R)	17:15	0x2	Indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
CLOCK_POWER_MANAGEMENT (R)	18	0x0	
SURPRISE_DOWN_ERR_REPORTING (R)	19	0x0	
DL_ACTIVE_REPORTING_CAPABLE (R)	20	0x0	
LINK_BW_NOTIFICATION_CAP (R)	21	0x0	
PORT_NUMBER (R)	31:24	0x0	Indicates the PCI Express Port number for the given PCI Express Link.
The Link Capabilities register identifies PCI Express Link specific capabilities.			

LINK_CNTL - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x68			
Field Name	**Bits**	**Default**	**Description**
PM_CONTROL	1:0	0x0	Controls the level of ASPM supported on the given PCI Express Link. Defined encodings are: 00b=Disabled 01b=L0s Entry Enabled 10b=L1 Entry Enabled 11b=L0s and L1 Entry Enabled
READ_CPL_BOUNDARY (R)	3	0x0	Read Completion Boundary. Indicates the RCB value for the Root Port 0=64 Byte 1=128 Byte
LINK_DIS (R)	4	0x0	Disables the Link when set to 1b. The default value of this field is 0b.
RETRAIN_LINK (R)	5	0x0	A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. Reads of this bit always return 0b.
COMMON_CLOCK_CFG	6	0x0	Indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. The default value of this field is 0b.
EXTENDED_SYNC	7	0x0	Forces the transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP ordered set
CLOCK_POWER_MANAGEMENT_EN	8	0x0	Determines if the device is permitted to use CLKREQ# signal to power manage link clock.
HW_AUTONOMOUS_WIDTH_DISABLE	9	0x0	When set to 1, this bit disables hardware from changing the link width for reasons other than attempting to correct unreliable link operation by reducing link width.
LINK_BW_MANAGEMENT_INT_EN (R)	10	0x0	
LINK_AUTONOMOUS_BW_INT_EN (R)	11	0x0	
The Link Control register controls PCI Express Link specific parameters.			

LINK_STATUS - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x6A			
Field Name	**Bits**	**Default**	**Description**
CURRENT_LINK_SPEED (R)	3:0	0x1	Indicates the negotiated Link speed of the given PCI Express Link 1=2.5 Gb/s 2=5.0 Gb/s
NEGOTIATED_LINK_WIDTH (R)	9:4	0x0	Indicates the negotiated width of the given PCI Express Link. The defined encodings are as follows: 000001b = x1 000010b = x2 000100b = x4 001000b = x8 001100b = x12 010000b = x16 100000b = x32 All other encodings are reserved. 1 = x1 2 = x2 4 = x4 8 = x8 12 = x12 16 = x16 32 = x32
LINK_TRAINING (R)	11	0x0	This read-only bit indicates that Link training is in progress (Physical Layer LTSSM in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
SLOT_CLOCK_CFG (R)	12	0x1	Indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be clear. 0=Diff Clock 1=Same Clock
DL_ACTIVE (R)	13	0x0	
LINK_BW_MANAGEMENT_STATUS (R)	14	0x0	
LINK_AUTONOMOUS_BW_STATUS (R)	15	0x0	
The Link Status register provides information about PCI Express Link specific parameters.			

DEVICE_CAP2 - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x7C			
Field Name	**Bits**	**Default**	**Description**
CPL_TIMEOUT_RANGE_SUP (R)	3:0	0x0	PCIE completion timeout range supported
CPL_TIMEOUT_DIS_SUP (R)	4	0x0	PCIE completion timeout disabled supported
The Device Capabilities 2 register identifies PCI Express device specific capabilities.			

DEVICE_CNTL2 - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x80			
Field Name	**Bits**	**Default**	**Description**
CPL_TIMEOUT_VALUE	3:0	0x0	PCIE completion timeout value
CPL_TIMEOUT_DIS	4	0x0	Disable PCIE completion timeout
The Device Control 2 register controls PCI Express device specific parameters.			

DEVICE_STATUS2 - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x82			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	
The Device Status 2 register provides information about PCI Express device specific parameters.			

LINK_CAP2 - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x84			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	31:0	0x0	
The Link Capabilities 2 register identifies PCI Express Link specific capabilities.			

LINK_CNTL2 - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x88			
Field Name	**Bits**	**Default**	**Description**
TARGET_LINK_SPEED	3:0	0x1	The upper limit on the operational speed. This field restricts the data rate values advertised by an upstream component.
ENTER_COMPLIANCE	4	0x0	Forces a port's transmitter to enter Compliance.
HW_AUTONOMOUS_SPEED_DISABLE	5	0x0	Controls the component's ability to autonomously direct changes in link speed.
SELECTABLE_DEEMPHASIS (R)	6	0x0	Selectable de-emphasis (in GEN 2 data rate) 0 = -6dB 1 = -3.6dB
XMIT_MARGIN	9:7	0x0	Control the value of the non-deemphasized voltage level at the transmitter pins
ENTER_MOD_COMPLIANCE	10	0x0	LTSSM transmits modified compliance pattern in Polling.Compliance if this bit is set to 1.
COMPLIANCE_SOS	11	0x0	When set to 1, the LTSSM is required to send SOS perioldically in between the (modified) compliance patterns.
COMPLIANCE_DEEMPHASIS	12	0x0	Sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the 'enter compliance' bit being 1b. When the link is operating at 2.5 GT/s, the setting of this bit has no effect. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. 0 = -6 dB 1 = -3dB
The Link Control 2 register controls PCI Express Link specific parameters.			

LINK_STATUS2 - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x8A			
Field Name	**Bits**	**Default**	**Description**
CUR_DEEMPHASIS_LEVEL (R)	0	0x0	When the link is operating at 5GT/s speed, this bit reflects the level of de-emphasis.
The Link Status 2 register provides information about PCI Express Link specific parameters.			

MSI_CAP_LIST - R - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0xA0			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x5	Register identifies if a device function is MSI capable
NEXT_PTR	15:8	0x0	Pointer to the next item on the capabilities list
Message Signaled Interrupt Capability Registers			

MSI_MSG_CNTL - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0xA2			
Field Name	**Bits**	**Default**	**Description**
MSI_EN	0	0x0	Enables MSI messaging 0=Disable 1=Enable
MSI_MULTI_CAP (R)	3:1	0x0	Multiple Message Capable register is read to determine the number of requested messages. 0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_MULTI_EN	6:4	0x0	Multiple Message Enable register is written to indicate the number of allocated messages. 0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_64BIT (R)	7	0x0	Signifies if a device function is capable of generating a 64-bit message address 0=Not capable of generating 1 64-bit message address 1=Capable of generating 1 64-bit message address
Message Signaled Interrupts Control Register			

MSI_MSG_ADDR_LO - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0xA4			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_LO	31:2	0x0	Message Lower Address. Use lower 32-bits of address
Message Lower Address			

MSI_MSG_ADDR_HI - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0xA8			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_HI	31:0	0x0	Message Upper Address. Use upper 32-bit of address
Message Upper Address			

MSI_MSG_DATA_64 - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0xAC			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA_64	15:0	0x0	Message Data. System specified.
64-bit MSI Message Data			

MSI_MSG_DATA - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0xA8			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA	15:0	0x0	Message Data. System specified.
MSI Message Data			

PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x100			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0xb	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x110	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
Vendor Specific Capability			

PCIE_VENDOR_SPECIFIC_HDR - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x104			
Field Name	**Bits**	**Default**	**Description**
VSEC_ID	15:0	0x1	Vendor-defined ID number.
VSEC_REV	19:16	0x1	Vendor-defined revision number.
VSEC_LENGTH	31:20	0x10	Number of bytes in the entire VSEC structure.
Vendor Specific Header			

PCIE_VENDOR_SPECIFIC1 - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x108			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	PCIE scratch register.
Vendor-Specific Scratch Register 1			

PCIE_VENDOR_SPECIFIC2 - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x10C			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	PCIE scratch register.
Vendor-Specific Scratch Register 2			

PCIE_VC_ENH_CAP_LIST - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x110			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x2	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x140	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
Virtual Channel Enhanced Capability Header			

PCIE_PORT_VC_CAP_REG1 - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x114			
Field Name	**Bits**	**Default**	**Description**
EXT_VC_COUNT	2:0	0x0	Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. This field is valid for all devices.
LOW_PRIORITY_EXT_VC_COUNT	6:4	0x0	Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC group
REF_CLK	9:8	0x0	Indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration.
PORT_ARB_TABLE_ENTRY_SIZE	11:10	0x0	Indicates the size (in bits) of Port Arbitration table entry in the device.
Port VC Capability Register 1			

PCIE_PORT_VC_CAP_REG2 - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x118			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_CAP	7:0	0x0	Indicates the types of VC Arbitration supported by the device for the Low Priority Virtual Channel group
VC_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the VC Arbitration Table.
Port VC Capability Register 2			

PCIE_PORT_VC_CNTL - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x11C			
Field Name	**Bits**	**Default**	**Description**
LOAD_VC_ARB_TABLE (R)	0	0x0	Used for software to update the VC Arbitration Table.
VC_ARB_SELECT	3:1	0x0	Used for software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes
Port VC Control Register			

PCIE_PORT_VC_STATUS - R - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x11E			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the VC Arbitration Table
Port VC Status Register			

PCIE_VC0_RESOURCE_CAP - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x120			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x1	Indicates types of Port Arbitration supported by the VC resource.
REJECT_SNOOP_TRANS	15	0x0	When set to zero, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC
MAX_TIME_SLOTS	21:16	0x0	Indicates the maximum number of time slots that the VC resource is capable of supporting
PORT_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the Port Arbitration Table associated with the VC resource.
VC0 Resource Capability Register			

PCIE_VC0_RESOURCE_CNTL - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x124			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x1	Indicates the TCs that are mapped to the VC resource
TC_VC_MAP_TC1_7	7:1	0x7f	Indicates the TCs that are mapped to the VC resource
LOAD_PORT_ARB_TABLE (R)	16	0x0	Updates the Port Arbitration logic from the Port Arbitration Table for the VC resource.
PORT_ARB_SELECT	19:17	0x0	Configures the VC resource to provide a particular Port Arbitration service.
VC_ID (R)	26:24	0x0	Assigns a VC ID to the VC resource
VC_ENABLE (R)	31	0x1	Enables a Virtual Channel.
VC0 Resource Control Register			

PCIE_VC0_RESOURCE_STATUS - R - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x12A			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the Port Arbitration Table associated with the VC resource
VC_NEGOTIATION_PENDING	1	0x1	Indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state
VC0 Resource Status Register			

PCIE_VC1_RESOURCE_CAP - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x12C			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x1	Indicates types of Port Arbitration supported by the VC resource.
REJECT_SNOOP_TRANS	15	0x0	When set to 0, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC
MAX_TIME_SLOTS	21:16	0x0	Indicates the maximum number of time slots that the VC resource is capable of supporting
PORT_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the Port Arbitration Table associated with the VC resource.
VC1 Resource Capability Register			

PCIE_VC1_RESOURCE_CNTL - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x130			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x0	Indicates the TCs that are mapped to the VC resource
TC_VC_MAP_TC1_7	7:1	0x0	Indicates the TCs that are mapped to the VC resource
LOAD_PORT_ARB_TABLE (R)	16	0x0	Updates the Port Arbitration logic from the Port Arbitration Table for the VC resource.
PORT_ARB_SELECT	19:17	0x0	Configures the VC resource to provide a particular Port Arbitration service.
VC_ID	26:24	0x0	Assigns a VC ID to the VC resource
VC_ENABLE	31	0x0	Enables a Virtual Channel.
VC1 Resource Control Register			

PCIE_VC1_RESOURCE_STATUS - R - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x136			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the Port Arbitration Table associated with the VC resource
VC_NEGOTIATION_PENDING	1	0x1	Indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state
VC1 Resource Status Register			

PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x140			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	15:0	0x3	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER (R)	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR (R)	31:20	0x150	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
Device Serial Number Enhanced Capability header			

PCIE_DEV_SERIAL_NUM_DW1 - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x144			
Field Name	**Bits**	**Default**	**Description**
SERIAL_NUMBER_LO	31:0	0x0	Lower 32-bits of IEEE defined 64-bit extended unique identifier. (EUI-64)
PCI-Express Device Serial Number (1st DW)			

PCIE_DEV_SERIAL_NUM_DW2 - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x148			
Field Name	**Bits**	**Default**	**Description**
SERIAL_NUMBER_HI	31:0	0x0	Upper 32-bits of IEEE defined 64-bit extended unique identifier. (EUI-64)
PCI-Express Device Serial Number (2nd DW)			

PCIE_ADV_ERR_RPT_ENH_CAP_LIST - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x150			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	15:0	0x1	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER (R)	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR (R)	31:20	0x190	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
Advanced Error Reporting Enhanced Capability header			

PCIE_UNCORR_ERR_STATUS - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x154			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_STATUS	4	0x0	Data Link Protocol Error Status
SURPDN_ERR_STATUS (R)	5	0x0	
PSN_ERR_STATUS	12	0x0	Poisoned TLP Status
FC_ERR_STATUS (R)	13	0x0	Flow Control Protocol Error Status
CPL_TIMEOUT_STATUS	14	0x0	Completion Timeout Status
CPL_ABORT_ERR_STATUS (R)	15	0x0	Completer Abort Status
UNEXP_CPL_STATUS	16	0x0	Unexpected Completion Status
RCV_OVFL_STATUS (R)	17	0x0	Receiver Overflow Status
MAL_TLP_STATUS	18	0x0	Malformed TLP Status
ECRC_ERR_STATUS (R)	19	0x0	ECRC Error Status
UNSUPP_REQ_ERR_STATUS	20	0x0	Unsupported Request Error Status
ACS_VIOLATION_STATUS	21	0x0	ACS Violation Status
The Uncorrectable Error Status register reports error status of individual error sources on a PCI Express device.			

PCIE_UNCORR_ERR_MASK - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x158			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_MASK	4	0x0	Data Link Protocol Error Mask
SURPDN_ERR_MASK (R)	5	0x0	
PSN_ERR_MASK	12	0x0	Poisoned TLP Mask
FC_ERR_MASK (R)	13	0x0	Flow Control Protocol Error Mask
CPL_TIMEOUT_MASK	14	0x0	Completion Timeout Mask
CPL_ABORT_ERR_MASK (R)	15	0x0	Completer Abort Mask
UNEXP_CPL_MASK	16	0x0	Unexpected Completion Mask
RCV_OVFL_MASK (R)	17	0x0	Receiver Overflow Mask
MAL_TLP_MASK	18	0x0	Malformed TLP Mask
ECRC_ERR_MASK (R)	19	0x0	ECRC Error Mask
UNSUPP_REQ_ERR_MASK	20	0x0	Unsupported Request Error Mask
ACS_VIOLATION_MASK	21	0x0	ACS Violation mask
The Uncorrectable Error Mask register controls reporting of individual errors by the device to the PCI Express Root Complex via a PCI Express error Message.			

PCIE_UNCORR_ERR_SEVERITY - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x15C			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_SEVERITY	4	0x1	Data Link Protocol Error Severity
SURPDN_ERR_SEVERITY (R)	5	0x1	
PSN_ERR_SEVERITY	12	0x0	Poisoned TLP Severity
FC_ERR_SEVERITY (R)	13	0x1	Flow Control Protocol Error Severity
CPL_TIMEOUT_SEVERITY	14	0x0	Completion Timeout Error Severity
CPL_ABORT_ERR_SEVERITY (R)	15	0x0	Completer Abort Error Severity
UNEXP_CPL_SEVERITY	16	0x0	Unexpected Completion Error Severity
RCV_OVFL_SEVERITY (R)	17	0x1	Receiver Overflow Error Severity
MAL_TLP_SEVERITY	18	0x1	Malformed TLP Severity
ECRC_ERR_SEVERITY (R)	19	0x0	ECRC Error Severity
UNSUPP_REQ_ERR_SEVERITY	20	0x0	Unsupported Request Error Severity
ACS_VIOLATION_SEVERITY	21	0x0	ACS Violation severity
The Uncorrectable Error Severity register controls whether an individual error is reported as a Nonfatal or Fatal error.			

PCIE_CORR_ERR_STATUS - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x160			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_STATUS	0	0x0	Receiver Error Status (
BAD_TLP_STATUS	6	0x0	Bad TLP Status
BAD_DLLP_STATUS	7	0x0	Bad DLLP Status
REPLAY_NUM_ROLLOVER_STATUS	8	0x0	REPLAY_NUM Rollover Status
REPLAY_TIMER_TIMEOUT_STATUS	12	0x0	Replay Timer Timeout Status
ADVISORY_NONFATAL_ERR_STATUS	13	0x0	
The Correctable Error Status register reports error status of individual correctable error sources on a PCI Express device.			

PCIE_CORR_ERR_MASK - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x164			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_MASK	0	0x0	Receiver Error Mask
BAD_TLP_MASK	6	0x0	Bad TLP Mask
BAD_DLLP_MASK	7	0x0	Bad DLLP Mask
REPLAY_NUM_ROLLOVER_MASK	8	0x0	REPLAY_NUM Rollover Mask
REPLAY_TIMER_TIMEOUT_MASK	12	0x0	Replay Timer Timeout Mask
ADVISORY_NONFATAL_ERR_MASK	13	0x1	
The Correctable Error Mask register controls reporting of individual correctable errors by device to the PCI Express Root Complex via a PCI Express error Message.			

PCIE_ADV_ERR_CAP_CNTL - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x168			
Field Name	**Bits**	**Default**	**Description**
FIRST_ERR_PTR (R)	4:0	0x0	The First Error Pointer is a read-only register that identifies the bit position of the first error reported in the Uncorrectable Error Status register.
ECRC_GEN_CAP (R)	5	0x0	Indicates that the device is capable of generating ECRC
ECRC_GEN_EN	6	0x0	Enables ECRC generation. Default value of this field is 0.
ECRC_CHECK_CAP (R)	7	0x0	Indicates that the device is capable of checking ECRC
ECRC_CHECK_EN	8	0x0	Enables ECRC checking. Default value of this field is 0.
Advanced Error Capabilities and Control Register			

PCIE_HDR_LOG0 - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x16C			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 1st DW
Header Log Register captures the Header for the TLP corresponding to a detected error.			

PCIE_HDR_LOG1 - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x170			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 2nd DW
Header Log Register			

PCIE_HDR_LOG2 - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x174			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 3rd DW
Header Log Register			

PCIE_HDR_LOG3 - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x178			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 4th DW
Header Log Register			

PCIE_CAC_ENH_CAP_LIST - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x190			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0xc	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x0	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
Configuration Access Correlation Enhanced Capability Header			

PCIE_CAC_DEVICE_CORRELATION - R - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x194			
Field Name	**Bits**	**Default**	**Description**
DEVICE_CORRELATION *(mirror of PCIE_TRUSTED_CAC_DEVICE_CORRELATION:DEVICE_CORRELATION)*	31:0	0x0	Device Correlation information. Read-only mirror from the Configuration Access Correlation Trusted Capability.
Used to confirm that Standard Configuration Requests and Trusted Configuration Requests are targeting the same device.			

2.6 Power Management Registers

PMI_CAP_LIST - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x50			
Field Name	**Bits**	**Default**	**Description**
CAP_ID (R)	7:0	0x1	Capability ID Must be set to 01h 1=PCIE Power Management Registers
NEXT_PTR (R)	15:8	0x58	Next Capability Pointer. The offset to the next PCI capability structure or 00h if no other items exist in the linked list of capabilities.
Power Management Capbility List			

PMI_CAP - RW - 16 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x52			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	2:0	0x3	Version 3=PMI Spec 1.2
PME_CLOCK (R)	3	0x0	Does not apply to PCI Express. Hardwired to 0.
DEV_SPECIFIC_INIT (R)	5	0x0	Device Specific Initialization
AUX_CURRENT (R)	8:6	0x0	AUX Current
D1_SUPPORT (R)	9	0x0	D1 Support 1=Support D1 PM State.
D2_SUPPORT (R)	10	0x0	D2 Support 1=Support D2 PM State.
PME_SUPPORT (R)	15:11	0x0	For a device, this indicates the power states in which the device may generate a PME.
Power Management Capabilities Register			

PMI_STATUS_CNTL - RW - 32 bits - AudioPcie, GpuF0Pcie,GpuF1Pcie:0x54			
Field Name	**Bits**	**Default**	**Description**
POWER_STATE	1:0	0x0	Power State
NO_SOFT_RESET (R)	3	0x0	
PME_EN (R)	8	0x0	PME Enable
DATA_SELECT (R)	12:9	0x0	Data Select
DATA_SCALE (R)	14:13	0x0	Data Scale
PME_STATUS (R)	15	0x0	PME Status
B2_B3_SUPPORT (R)	22	0x0	B2/B3 Support Does not apply to PCI Express. Hardwired to 0.
BUS_PWR_EN (R)	23	0x0	Bus Power/Clock Control Enable Does not apply to PCI Express. Hardwired to 0.
PMI_DATA (R)	31:24	0x0	Data
Power Management Status/Control Register			

2.7 Bus Interface Registers

MM_INDEX - RW - 32 bits - GpuF0MMReg,GpuIOReg:0x0			
Field Name	**Bits**	**Default**	**Description**
MM_OFFSET	30:0	0x0	This field specifies the offset (in MM space) of the register or the offset in FB memory to be accessed. All accesses must be dword aligned, therefore, bits [1:0] are tied to 0. Note: Bits [1:0] of this field are hardwired to 0.
MM_APER	31	0x0	This bit specifies whether the address offset is for Register aperture or FB aperture (Linear Aperture). 0=Register Aperture 1=Linear Aperture 0
General Memory Access. The MM_INDEX and MM_DATA pair of registers are used to indirectly accessed all other memory mapped registers in the lower 64KB space and the Frame buffer.			

MM_DATA - RW - 32 bits - GpuF0MMReg,GpuIOReg:0x4			
Field Name	**Bits**	**Default**	**Description**
MM_DATA	31:0	0x0	This field contains the data to be written to or the data read from the address specified in MM_INDEX.
General Memory Access. The MM_INDEX and MM_DATA pair of registers are used to indirectly access all other BIF memory mapped registers and the frame buffer.			

MM_CFGREGS_CNTL - RW - 32 bits -, GpuF0MMReg:0x544C			
Field Name	**Bits**	**Default**	**Description**
MM_CFG_FUNC_SEL	2:0	0x0	Only 1 function's CFG registers can be selected to map in memory-mapped space. 0=F0 1=F1 2=F2 3=F3 4=F4 5=F5 6=F6 7=F7
MM_WR_TO_CFG_EN	3	0x0	Enables memory-mapped register writes to configuration space registers 0=Disable 1=Enable
Memory-mapped CFG space registers control			

2.8 Video Graphics Array (VGA) Registers

2.8.1 VGA Control/Status Registers

GENFC_RD - R - 8 bits - GpuF0MMReg,VGA_IO:0x3CA			
Field Name	**Bits**	**Default**	**Description**
VSYNC_SEL_R *(mirror of GENFC_WT:VSYNC_SEL_W)*	3	0x0	Veritcal sync select (read). 0=Normal vertical sync 1=Sync is 'vertical sync' ORed with 'vertical display enable'
Feature Control Regsiter (Read)			

GENFC_WT - W - 8 bits - GpuF0MMReg:0x3BA, GpuF0MMReg:0x3DA, VGA_IO:0x3BA, VGA_IO:0x3DA			
Field Name	**Bits**	**Default**	**Description**
VSYNC_SEL_W	3	0x0	Vertical sync select (write). 0=Normal vertical sync 1=Sync is 'vertical sync' ORed with 'vertical display enable'
Feature Control Register (Read)			

GENMO_WT - W - 8 bits - GpuF0MMReg,VGA_IO:0x3C2			
Field Name	**Bits**	**Default**	**Description**
GENMO_MONO_ADDRESS_B	0	0x0	0=Monochrome emulation, regs at 0x3Bx 1=Color/Graphic emulation, regs at 0x3Dx
VGA_RAM_EN	1	0x0	0=Disable 1=Enable
VGA_CKSEL	3:2	0x0	0=25.1744MHz (640 Pels) 1=28.3212MHz (720 Pels) 2=Reserved 3=Reserved
ODD_EVEN_MD_PGSEL	5	0x0	0=Selects odd (high) memory locations 1=Selects even (low) memory locations
VGA_HSYNC_POL	6	0x0	
VGA_VSYNC_POL	7	0x0	

GENMO_RD - R - 8 bits - GpuF0MMReg,VGA_IO:0x3CC			
Field Name	**Bits**	**Default**	**Description**
GENMO_MONO_ADDRESS_B *(mirror of GENMO_WT:GENMO_MONO_ADDRESS_B)*	0	0x0	0=Monochrome emulation, regs at 0x3Bx 1=Color/Graphic emulation, regs at 0x3Dx
VGA_RAM_EN *(mirror of GENMO_WT:VGA_RAM_EN)*	1	0x0	0=Disable 1=Enable
VGA_CKSEL *(mirror of GENMO_WT:VGA_CKSEL)*	3:2	0x0	0=25.1744MHz (640 Pels) 1=28.3212MHz (720 Pels) 2=Reserved 3=Reserved
ODD_EVEN_MD_PGSEL *(mirror of GENMO_WT:ODD_EVEN_MD_PGSEL)*	5	0x0	0=Selects odd (high) memory locations 1=Selects even (low) memory locations
VGA_HSYNC_POL *(mirror of GENMO_WT:VGA_HSYNC_POL)*	6	0x0	
VGA_VSYNC_POL *(mirror of GENMO_WT:VGA_VSYNC_POL)*	7	0x0	

GENENB - R - 8 bits - GpuF0MMReg,VGA_IO:0x3C3			
Field Name	**Bits**	**Default**	**Description**
BLK_IO_BASE	7:0	0x0	

GENS0 - R - 8 bits - GpuF0MMReg,VGA_IO:0x3C2			
Field Name	**Bits**	**Default**	**Description**
SENSE_SWITCH	4	0x0	DAC comparator read back. Used for monitor detection. Mirror of DAC_CMP_OUTPUT@DAC_CNTL. See description there.
CRT_INTR	7	0x0	CRT Interrupt: 0=Vertical retrace interrupt is cleared 1=Vertical retrace interrupt is pending
Input Status 0 Register			

GENS1 - R - 8 bits - GpuF0MMReg:0x3BA, GpuF0MMReg:0x3DA, VGA_IO:0x3BA, VGA_IO:0x3DA			
Field Name	**Bits**	**Default**	**Description**
NO_DISPLAY	0	0x0	Display enable. 0=Enable 1=Disable
VGA_VSTATUS	3	0x0	Vertical Retrace Status. 0=Vertical retrace not active 1=Vertical retrace active
PIXEL_READ_BACK	5:4	0x0	Diagnostic bits 0, 1 respectively. These two bits are connected to two of the eight colour outputs (P7:P0) of the attribute controller. Connections are controlled by ATTR12(5,4) as follows: 0=P2,P0 1=P5,P4 2=P3,P1 3=P7,P6
Input Status 1 Register			

2.8.2 VGA DAC Control Registers

DAC_CONTROL - RW - 32 bits - [INST0] GpuF0MMReg:0x7058, [INST1] GpuF0MMReg:0x7158			
Field Name	**Bits**	**Default**	**Description**
DAC_DFORCE_EN	0	0x0	DAC asynchronous data force enable. Can be used for sync force as well but DAC_FORCE_OUTPUT_CNTL achieves the same goal with a more complete feature set. Asynchronous force requires DAC_x_ASYNC_ENABLE in DAC_COMPARATOR_ENABLE to be set as well. Drives DFORCE_EN pin on macro. Forces all DAC channels to DAC_FORCE_DATA value. Overrides DAC_FORCE_OUTPUT_CNTL/DAC_FORCE_DATA_EN control.
DAC_TV_ENABLE	8	0x0	
DAC_ZSCALE_SHIFT	16	0x0	DAC zero scale shift enable. Causes DAC to add a small offset to the levels of all outputs. Drives DAC ZSCALE_SHIFT pin.

DAC_DATA - RW - 8 bits - GpuF0MMReg,VGA_IO:0x3C9			
Field Name	**Bits**	**Default**	**Description**
DAC_DATA	5:0	0x0	VGA Palette (DAC) Data. Use DAC_R_INDEX and DAC_W_INDEX to set read or write mode, and entry to access. Access order is Red, Green, Blue, and then auto-increment occurs to next entry. DAC_8BIT_EN controls whether 6 or 8 bit access.
VGA Palette (DAC) Data			

DAC_MASK - RW - 8 bits - GpuF0MMReg,VGA_IO:0x3C6			
Field Name	**Bits**	**Default**	**Description**
DAC_MASK	7:0	0x0	Masks off usage of individual palette index bits before pixel index is looked-up in the palette. 0=Do not use this bit of the index 1=Use this bit of the index Only has an effect in VGA emulation modes (CRTC_EXT_DISP_EN=0), not for VESA modes or extended display modes.
Palette index mask for VGA emulation modes.			

DAC_R_INDEX - RW - 8 bits - GpuF0MMReg,VGA_IO:0x3C7			
Field Name	**Bits**	**Default**	**Description**
DAC_R_INDEX	7:0	0x0	Write: Sets the index for a palette (DAC) read operation. Index auto-increments after every third read of DAC_DATA. Read: Indicates if palette in read or write mode. 0=Palette in write mode (DAC_W_INDEX last written). 3=Palette in read mode (DAC_R_INDEX last written). Also see DAC_W_INDEX.
Palette (DAC) Read Index			

DAC_W_INDEX - RW - 8 bits - GpuF0MMReg,VGA_IO:0x3C8			
Field Name	**Bits**	**Default**	**Description**
DAC_W_INDEX	7:0	0x0	Sets the index for a palette (DAC) write operation. Index auto-increments after every third write of DAC_DATA. Aslo see DAC_R_INDEX.
Palette (DAC) Write Index			

2.8.3 VGA Sequencer Registers

SEQ00 - RW - 8 bits - VGASEQIND:0x0			
Field Name	**Bits**	**Default**	**Description**
SEQ_RST0B	0	0x1	Synchronous reset bit 0: 0=Follows SEQ_RST1B 1=Sequencer runs unless SEQ_RST1B=0
SEQ_RST1B	1	0x1	Synchronous reset bit 1: 0=Disable character clock, display requests, and H/V syncs 1=Sequencer runs unless SEQ_RST0B=0
Reset Register			

SEQ01 - RW - 8 bits - VGASEQIND:0x1			
Field Name	**Bits**	**Default**	**Description**
SEQ_DOT8	0	0x1	8/9 Dot Clocks (Modes 1, 2, 3, and 7 use 9-dot characters. To change bit 0, GENVS(0) must be logical 0). 0=9 dot char clock. Modes 0, 1, 2, 3 & 7 1=8 dot char clock.
SEQ_SHIFT2	2	0x0	Shift load bits. 0=Load video serializer every clock, if SEQ_SHIFT4=0 1=Load video serializer every other clock, if SEQ_SHIFT4=0
SEQ_PCLKBY2	3	0x0	Dot Clock (typically, 320 and 360 horizontal modes use divide-by-2 to provide 40 column displays. To change this bit SEQ00[0:0] must be first set to 0) 0=Dot clock is normal 1=Dot clock is divided by 2
SEQ_SHIFT4	4	0x0	Shift load bits. 0=SEQ_SHIFT2 determines serializer loading 1=Load video serializer every fourth clock. Ignore SEQ_SHIFT2
SEQ_MAXBW	5	0x1	Screen off. 0=Normal. Screen on 1=Sreen off and blanked. CPU has uninterrupted access to frame buffer
Clock Mode Register			

SEQ02 - RW - 8 bits - VGASEQIND:0x2			
Field Name	**Bits**	**Default**	**Description**
SEQ_MAP0_EN	0	0x0	0=Disable write to memory map 0 1=Enable write to memory map 0
SEQ_MAP1_EN	1	0x0	0=Disable write to memory map 1 1=Enable write to memory map 1
SEQ_MAP2_EN	2	0x0	0=Disable write to memory map 2 1=Enable write to memory map 2
SEQ_MAP3_EN	3	0x0	0=Disable write to memory map 3 1=Enable write to memory map 3

SEQ03 - RW - 8 bits - VGASEQIND:0x3			
Field Name	**Bits**	**Default**	**Description**
SEQ_FONT_B1	0	0x0	Character Map Select B Bit 1
SEQ_FONT_B2	1	0x0	Character Map Select B Bit 2
SEQ_FONT_A1	2	0x0	Character Map Select A Bit 1
SEQ_FONT_A2	3	0x0	Character Map Select A Bit 2
SEQ_FONT_B0	4	0x0	Character Map Select B Bit 0
SEQ_FONT_A0	5	0x0	Character Map Select A Bit 0
Character Map Select Register			

SEQ04 - RW - 8 bits - VGASEQIND:0x4			
Field Name	**Bits**	**Default**	**Description**
SEQ_256K	1	0x0	0=64KB memory present. Has no effect since 256KB always available 1=256KB memory present
SEQ_ODDEVEN	2	0x0	0=Even CPU address (A0=0) accesses maps 0 and 2. Odd address accesses maps 1 and 3 1=Enables sequential access to maps for odd/even modes. SEQ02 (Map Mask) selects which maps are used
SEQ_CHAIN	3	0x0	0=Enables sequential access to maps. SEQ02 (Map Mask) selects which maps are used 1=For 256 color modes. Map select by CPU address bits A1:A0

SEQ8_IDX - RW - 8 bits - GpuF0MMReg,VGA_IO:0x3C4			
Field Name	**Bits**	**Default**	**Description**
SEQ_IDX	2:0	0x0	

SEQ8_DATA - RW - 8 bits - GpuF0MMReg,VGA_IO:0x3C5			
Field Name	**Bits**	**Default**	**Description**
SEQ_DATA	7:0	0x0	

2.8.4 VGA CRT Registers

CRTC8_IDX - RW - 8 bits - GpuF0MMReg:0x3B4, GpuF0MMReg:0x3D4, VGA_IO:0x3B4, VGA_IO:0x3D4			
Field Name	**Bits**	**Default**	**Description**
VCRTC_IDX	5:0	0x0	

CRTC8_DATA - RW - 8 bits - GpuF0MMReg:0x3B5, GpuF0MMReg:0x3D5, VGA_IO:0x3B5, VGA_IO:0x3D5			
Field Name	**Bits**	**Default**	**Description**
VCRTC_DATA	7:0	0x0	

CRT00 - RW - 8 bits - VGACRTIND:0x0			
Field Name	**Bits**	**Default**	**Description**
H_TOTAL	7:0	0x0	Defines the active horizontal display in a scan line, including the retrace period. The value is five less than the total number of displayed characters in a scan line.
Horizontal Total Register			

CRT01 - RW - 8 bits - VGACRTIND:0x1			
Field Name	**Bits**	**Default**	**Description**
H_DISP_END	7:0	0x0	Defines the active horizontal dispaly in a scan line. The value is one less than the total number of displayed characters in a scan line.
Horizontal Display Enable End Register			

CRT02 - RW - 8 bits - VGACRTIND:0x2			
Field Name	**Bits**	**Default**	**Description**
H_BLANK_START	7:0	0x0	Defines the horizontal character count that represents the character coune in the active display area plus the right borger. In other words, the count is from the start of active display to the start of triggering of the H blanking pulse.
Start Horizontal Blanking Register			

CRT03 - RW - 8 bits - VGACRTIND:0x3			
Field Name	**Bits**	**Default**	**Description**
H_BLANK_END	4:0	0x0	H blanking bits 4-0 respectively. These are the five low-order bits (of six bits in total) of horizontal character count for triggering the end of the horizontal blanking pulse.
H_DE_SKEW	6:5	0x0	Display-enable skew: 0=0Skew 1=1Skew 2=2Skew 3=3Skew
CR10CR11_R_DIS_B	7	0x0	Comptibility Read: 0=WrtOnlyToCRT10-11 1=WrtRdToCRT10-11
End Horizontal Blanking Register			

CRT04 - RW - 8 bits - VGACRTIND:0x4			
Field Name	**Bits**	**Default**	**Description**
H_SYNC_START	7:0	0x0	These bits define the horizontal character count at which the horizontal retrace pulse becomes active.
Start Horizontal Retrace Register			

CRT05 - RW - 8 bits - VGACRTIND:0x5			
Field Name	**Bits**	**Default**	**Description**
H_SYNC_END	4:0	0x0	H Retrace Bits (these are the 5-bit result from the sum of CRT0 plus the width of the horizontal retrace pulse, in character clock units).
H_SYNC_SKEW	6:5	0x0	H Retrace Delay bits (these two bits skew the horizontal retrace pulse).
H_BLANK_END_B5	7	0x0	H blocking end bit 5 (this is the bit of the 6-bit character count for the H blanking end pulse). The other five low-order bits are CRT03[4:0].
End Horizontal Retrace Register			

CRT06 - RW - 8 bits - VGACRTIND:0x6			
Field Name	**Bits**	**Default**	**Description**
V_TOTAL	7:0	0x0	These are the eight low-order bits of the 10-bit vertical total register. The 2 high-order bits are CRT07[5:0] in the CRTC overflow register. The value of this register represents the total number of H raster scans plus vertical retrace (active display, blanking), minus two scan lines.
Vertical Total Register			

CRT07 - RW - 8 bits - VGACRTIND:0x7			
Field Name	**Bits**	**Default**	**Description**
V_TOTAL_B8	0	0x0	V Total Bit 8 (CRT06). Bit 8 of 10 bit vertical count for V Total. For functional description see CRT06 register.
V_DISP_END_B8	1	0x0	End V Display Bit 8 (CRT12). Bit 8 of 10-bit vertical count for V Display enable. For functional desription see CRT12 register.
V_SYNC_START_B8	2	0x0	Start V Retrace Bit 8 (CRT10). Bit 8 of 10-bit veritcal count for V Retrace start. For functional description see CRT10 register.
V_BLANK_START_B8	3	0x0	Start V Blanking Bit 8 (CRT15). Bit 8 of the 10-bit vertical count for V Blanking start. For functional description see CRT15 register.
LINE_CMP_B8	4	0x0	Line compare bit 8 (CRT18). Bit 8 of the 10-bit vertical count for line compare. For functional description see CRT18 register.
V_TOTAL_B9	5	0x0	V Total Bit 9 (CRT06). Bit 9 of 10-bit vertical count for V Total. For functional description see CRT06 register.
V_DISP_END_B9	6	0x0	End V Display Bit 9 (CRT12). Bit 9 of 10-bit vertical count for V Display enable end (for functional description see CRT12 register).
V_SYNC_START_B9	7	0x0	Start V Retrace Bit (CRT10). Bit 9 of 10-bit vertical count for V Retrace start. For functional description see CRT10 register.
CRTC Overflow Register			

CRT08 - RW - 8 bits - VGACRTIND:0x8			
Field Name	**Bits**	**Default**	**Description**
ROW_SCAN_START	4:0	0x0	Preset row scan bit [4:0]. This register is used for software-controlled vertical scrolling in text or graphics modes. The value specifies the first line to be scanned after a V retrace (in the next frame). Each H Retrace pulse increments the counter by 1, up to the maximum scan line value programmed by CRT09, then the counter is cleared.
BYTE_PAN	6:5	0x0	Byte panning control bits 1 and 0 (respectively). Bits 6 and 5 extend the capability of byte panning (shifting) by up to three characters (for description H_PEL Panning register ATTR13).
Preset Row Scan Register			

CRT09 - RW - 8 bits - VGACRTIND:0x9			
Field Name	**Bits**	**Default**	**Description**
MAX_ROW_SCAN	4:0	0x0	Maximum scan line bits. These bits define a value that is the actual number of scan line per character minus 1.
V_BLANK_START_B9	5	0x0	Start V Blanking bit 9 (CRT15). Bit 9 of 10-bit veritcal count for line compare. For functional description see CRT18 register.
LINE_CMP_B9	6	0x0	Line Compare Bit 9 (CRT18). Bit 9 of 10-bit vertical count for line compare. For functional description see CRT18 register.
DOUBLE_CHAR_HEIGHT	7	0x0	200/400 line scan. Note: H/V display and blanking timings etc. (in CRT00-CRT06 registers) are not affected. 0=200LineScan 1=400LineScan
Maximum Scan Line Register			

CRT0A - RW - 8 bits - VGACRTIND:0xA			
Field Name	**Bits**	**Default**	**Description**
CURSOR_START	4:0	0x0	Cursor start bits [4:0] (respectively). These bits define a value that is the starting scan line (on a character row) for the line cursor. The 5-bit value is equal to the actual number minus one. This value is used together with the Cursor End Bits CRT0B[4:0] to determine the height of the cursor. The cursor height in VGA does not wrap around (as in EGA) and is actually absent when the 'end' value is less than the 'start' value. In EGA when the 'end' value is less, the cursor is a full block cursor the same height as the character cell.
CURSOR_DISABLE	5	0x0	Cursor on/off. 0=On 1=Off
Cursor Start Register			

CRT0B - RW - 8 bits - VGACRTIND:0xB			
Field Name	**Bits**	**Default**	**Description**
CURSOR_END	4:0	0x0	Cursor End Bits [4:0], respectively. These bits define the ending scan row (on a character line) for the line cursor. In EGA, this 5-bit value is equal to the actual number of lines plus one. The cursor height in VGA does not wrap around (as in EGA) and is actually absent when the 'end' value is less than the 'start' value. In EGA when the 'end' value is less, the cursor is a full block cursor the same height as the character cell.
CURSOR_SKEW	6:5	0x0	Cursor Skew Bits [1:0], respectively. These bits define the number of characters the cursor is to be shifted to the right (skewed) from the character pointed at by the cursor location (registers CRT0E and CRT0F), in VGA mode. Skew values when in EGA mode are enclosed in brackets.
Cursor End Register			

CRT0C - RW - 8 bits - VGACRTIND:0xC			
Field Name	**Bits**	**Default**	**Description**
DISP_START	7:0	0x0	SA bits [15:8]. These are the eight high-order bits of the 16-bit display buffer start location. The low order bits are contained in CRT0D.-In split screen mode, CRT0C = CRT0D point to the starting location of screen A (top half.) The starting address for screen B is always 0.
Start Address (High Byte) Register			

CRT0D - RW - 8 bits - VGACRTIND:0xD			
Field Name	**Bits**	**Default**	**Description**
DISP_START	7:0	0x0	SA bits [7:0]. These are the eight low-order bits of the 16-bit display buffer start location. The high-order bits are contained in CRT0C. In split creen mode, CRT0C + CRT0D points to the starting location of screen A (top half.) The starting address for screen B is always 0.
Start Address (Low Byte) Register			

CRT0E - RW - 8 bits - VGACRTIND:0xE			
Field Name	**Bits**	**Default**	**Description**
CURSOR_LOC_HI	7:0	0x0	CA bits [15:8]. These are the eight high-order bits of the 16 bit cursor start address. The low-order CA bits are contained in CRT0F. This address is relative to the start of physical display memory address pointed to by CRT0C + CRT0D. In other words, if CRT0C + CRT0D is changed, the cursor still pints to the same character as before.
Cursor Location (High Byte) Register			

CRT0F - RW - 8 bits - VGACRTIND:0xF			
Field Name	**Bits**	**Default**	**Description**
CURSOR_LOC_LO	7:0	0x0	CA bits [7:0]. These are the eight low-order bits of the 16 bit cursor start address. The high-order CA bits are contained in CRT0E. This address is relative to the start of physical display memory address pointed to by CRT0C + CRT0D. In other words, if CRT0C + T0D is changed, the cursor still points to the same character as before
Cursor Location (Low Byte) Register			

CRT10 - RW - 8 bits - VGACRTIND:0x10			
Field Name	**Bits**	**Default**	**Description**
V_SYNC_START	7:0	0x0	Bits CRT10[7:0] are the eight low-order bits of the 10-bit vertical retrace start count. The two high-order bits are CRTt07[2:7], located in the CRTC overflow register. These bits define the horizontal scan count that triggers the V retrace pulse.
Start Vertical Retrace Register			

CRT11 - RW - 8 bits - VGACRTIND:0x11			
Field Name	**Bits**	**Default**	**Description**
V_SYNC_END	3:0	0x0	V Retrace End Bits [3:0]. Bits CRT11[0:3] define the horizontal scan count that triggers the end of the V Retrace pulse.
V_INTR_CLR	4	0x0	V Retrace Interrupt Set 0=VRetraceIntCleared 1=Not Cleared
V_INTR_EN	5	0x0	V Retrace Interrupt Disabled 0=VRetraceIntEna 1=Disable
SEL5_REFRESH_CYC	6	0x0	0=3 DRAM Refresh/Horz Line 1=5 DRAM Refresh/Horz Line
C0T7_WR_ONLY	7	0x0	Write Protect (CRT00-CRT06). All register bits except CRTO7[4] are write protected. 0=EnaWrtToCRT00-07 1=C0T7B4WrtOnly
End Vertical Retrace Register			

CRT12 - RW - 8 bits - VGACRTIND:0x12			
Field Name	**Bits**	**Default**	**Description**
V_DISP_END	7:0	0x0	These are the eight low-order bits of the 10-bit register containing the horizontal scan count indicating where the active display on the screen should end. The high-order bits are CRT07 [1:6] in the CRT overflow register.
Vertical Display Enable End Register			

CRT13 - RW - 8 bits - VGACRTIND:0x13			
Field Name	**Bits**	**Default**	**Description**
DISP_PITCH	7:0	0x0	These bits define an offset value, equal to the logical line width of the screen (from the first character of the current line to the first character of the next line). Memory organization is dependent on the video mode. Bit CRT17[6] selects byte or word mode. Bit CRT14[6], which overrides the byte/word mode setting, selects Double-Word mode when it is logical one. The first character of the next line is specified by the start address (CRT0C + CRT0D) plus the offset. The offset for byte mode is 2x CRT13; for word mode, 4x; for double word mode 8x.
Offset Register			

CRT14 - RW - 8 bits - VGACRTIND:0x14			
Field Name	**Bits**	**Default**	**Description**
UNDRLN_LOC	4:0	0x0	
ADDR_CNT_BY4	5	0x0	0=Char. Clock 1=CountBy4
DOUBLE_WORD	6	0x0	0=Disable 1=DoubleWordMdEna

CRT15 - RW - 8 bits - VGACRTIND:0x15			
Field Name	**Bits**	**Default**	**Description**
V_BLANK_START	7:0	0x0	These are the eight low-order bits of the 10-bit vertical blanking start register. Bit 9 is CRT09[5]; bit 8 is CRT07[3]- The 10 bits specify the starting location of the vertical blaning pulse, in units of horizontal scan lines. The value is equal to the actual number of displayed lines minus one.
Start Vertical Blanking Register			

CRT16 - RW - 8 bits - VGACRTIND:0x16			
Field Name	**Bits**	**Default**	**Description**
V_BLANK_END	7:0	0x0	These bits define the point at which to trigger the end of the vertical blanking pulse. The location is specified in units of horizontal scan lines. The value to be storeed in this register is the seven low-order bits of the sum of 'pulse width count' plus the content of Start Vertical Blanking register (CRT15) minus one.
End Vertical Blanking Register			

CRT17 - RW - 8 bits - VGACRTIND:0x17			
Field Name	**Bits**	**Default**	**Description**
RA0_AS_A13B	0	0x0	
RA1_AS_A14B	1	0x0	
VCOUNT_BY2	2	0x0	
ADDR_CNT_BY2	3	0x0	
WRAP_A15TOA0	5	0x0	
BYTE_MODE	6	0x0	0=WordMode 1=ByteMode
CRTC_SYNC_EN	7	0x0	0=Disable HVSync 1=EnaHVSync

CRT18 - RW - 8 bits - VGACRTIND:0x18			
Field Name	**Bits**	**Default**	**Description**
LINE_CMP	7:0	0x0	These bits are the eight low-order of the 10-bit line compare register. Bit 8 is CRT07[4], bit 9 is CRT09[6]. The value of this register is used to disable scrolling on a portion of the display screen, as when split screen is active. When the vertical counter reaches this value, the memory address and row scan counters are cleared. The screen area above the line specified by the register is commonly called screen A. The screen below is screen B. Screen B cannot be scrolled, but it can panned only together with screen A, controlled by the PEL panning compatibility bit ATTR10[5]. (For a description of this control bit see ATTR10[5].)
Line Compare Register			

CRT1E - R - 8 bits - VGACRTIND:0x1E			
Field Name	**Bits**	**Default**	**Description**
GRPH_DEC_RD1	1	0x0	

CRT1F - R - 8 bits - VGACRTIND:0x1F			
Field Name	**Bits**	**Default**	**Description**
GRPH_DEC_RD0	7:0	0x0	

CRT22 - R - 8 bits - VGACRTIND:0x22			
Field Name	**Bits**	**Default**	**Description**
GRPH_LATCH_DATA	7:0	0x0	

2.8.5 VGA Graphics Registers

GRPH8_IDX - RW - 8 bits - GpuF0MMReg,VGA_IO:0x3CE			
Field Name	**Bits**	**Default**	**Description**
GRPH_IDX	3:0	0x0	

GRPH8_DATA - RW - 8 bits - GpuF0MMReg,VGA_IO:0x3CF			
Field Name	**Bits**	**Default**	**Description**
GRPH_DATA	7:0	0x0	

GRA00 - RW - 8 bits - VGAGRPHIND:0x0			
Field Name	**Bits**	**Default**	**Description**
GRPH_SET_RESET0	0	0x0	
GRPH_SET_RESET1	1	0x0	
GRPH_SET_RESET2	2	0x0	
GRPH_SET_RESET3	3	0x0	

GRA01 - RW - 8 bits - VGAGRPHIND:0x1			
Field Name	**Bits**	**Default**	**Description**
GRPH_SET_RESET_ENA0	0	0x0	
GRPH_SET_RESET_ENA1	1	0x0	
GRPH_SET_RESET_ENA2	2	0x0	
GRPH_SET_RESET_ENA3	3	0x0	

GRA02 - RW - 8 bits - VGAGRPHIND:0x2			
Field Name	**Bits**	**Default**	**Description**
GRPH_CCOMP	3:0	0x0	

GRA03 - RW - 8 bits - VGAGRPHIND:0x3			
Field Name	**Bits**	**Default**	**Description**
GRPH_ROTATE	2:0	0x0	
GRPH_FN_SEL	4:3	0x0	0=Replace 1=AND 2=OR 3=XOR

GRA04 - RW - 8 bits - VGAGRPHIND:0x4			
Field Name	**Bits**	**Default**	**Description**
GRPH_RMAP	1:0	0x0	

GRA05 - RW - 8 bits - VGAGRPHIND:0x5			
Field Name	**Bits**	**Default**	**Description**
GRPH_WRITE_MODE	1:0	0x0	0=Write mode 0 1=Write mode 1 2=Write mode 2 3=Write mode 3
GRPH_READ1	3	0x0	0=Read mode 0, byte oriented 1=Read mode 1, pixel oriented
CGA_ODDEVEN	4	0x0	0=Disable Odd/Even Addressing 1=Enable Odd/Even Addressing
GRPH_OES	5	0x0	0=Linear shift mode 1=Tiled shift mode
GRPH_PACK	6	0x0	0=Use shift register mode as per GRPH_OES 1=256 color mode, read as packed pixels, ignore GRPH_OES

GRA06 - RW - 8 bits - VGAGRPHIND:0x6			
Field Name	**Bits**	**Default**	**Description**
GRPH_GRAPHICS	0	0x0	0=Alpha Numeric Mode 1=Graphics Mode
GRPH_ODDEVEN	1	0x0	0=Normal 1=Chain Odd maps to Even
GRPH_ADRSEL	3:2	0x0	0=A0000-128K 1=A0000-64K 2=B0000-32K 3=B8000-32K

GRA07 - RW - 8 bits - VGAGRPHIND:0x7			
Field Name	**Bits**	**Default**	**Description**
GRPH_XCARE0	0	0x0	0=Ignore map 0 1=Use map 0 for read mode 1
GRPH_XCARE1	1	0x0	0=Ignore map 1 1=Use map 1 for read mode 1
GRPH_XCARE2	2	0x0	0=Ignore map 2 1=Use map 2 for read mode 1
GRPH_XCARE3	3	0x0	0=Ignore map 3 1=Use map 3 for read mode 1

GRA08 - RW - 8 bits - VGAGRPHIND:0x8			
Field Name	**Bits**	**Default**	**Description**
GRPH_BMSK	7:0	0x0	

2.8.6 VGA Attribute Registers

ATTRX - RW - 8 bits - GpuF0MMReg,VGA_IO:0x3C0			
Field Name	**Bits**	**Default**	**Description**
ATTR_IDX	4:0	0x0	ATTR Index. This index points to one of the internal registers of the attribute controller (ATTR) at addresses 0x3C1/0x3C0, for the next ATTR read/write operation. Since both the index and data registers are at the same I/O, a pointer to the registers is necessary. This pointer cna be initialized to point to the index register by a read of GENS1.
ATTR_PAL_RW_ENB	5	0x0	Palette Address Source. After loading the colour palette, this bit should be set to logical 1. 0=Processor to load 1=Memory data to access
Attribute Index Register			

ATTRDW - W - 8 bits - GpuF0MMReg,VGA_IO:0x3C0			
Field Name	**Bits**	**Default**	**Description**
ATTR_DATA	7:0	0x0	Attribute Data Write
Attribute Data Write Register			

ATTRDR - R - 8 bits - GpuF0MMReg,VGA_IO:0x3C1			
Field Name	**Bits**	**Default**	**Description**
ATTR_DATA	7:0	0x0	Attribute Data Read
Attribute Data Read Register			

ATTR00 - RW - 8 bits - VGAATTRIND:0x0			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register 0			

ATTR01 - RW - 8 bits - VGAATTRIND:0x1			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register 1			

ATTR02 - RW - 8 bits - VGAATTRIND:0x2			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register 2			

ATTR03 - RW - 8 bits - VGAATTRIND:0x3			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register 3			

ATTR04 - RW - 8 bits - VGAATTRIND:0x4			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register 4			

ATTR05 - RW - 8 bits - VGAATTRIND:0x5			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register 5			

ATTR06 - RW - 8 bits - VGAATTRIND:0x6			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register 6			

ATTR07 - RW - 8 bits - VGAATTRIND:0x7			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register 7			

ATTR08 - RW - 8 bits - VGAATTRIND:0x8			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register 8			

ATTR09 - RW - 8 bits - VGAATTRIND:0x9			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register 9			

ATTR0A - RW - 8 bits - VGAATTRIND:0xA			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register Ah (10)			

ATTR0B - RW - 8 bits - VGAATTRIND:0xB			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register Bh (11)			

ATTR0C - RW - 8 bits - VGAATTRIND:0xC			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register Ch (12)			

ATTR0D - RW - 8 bits - VGAATTRIND:0xD			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register Dh (13)			

ATTR0E - RW - 8 bits - VGAATTRIND:0xE			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits [5:0] map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register Eh (14)			

ATTR0F - RW - 8 bits - VGAATTRIND:0xF			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.
Palette Register Fh (15)			

ATTR10 - RW - 8 bits - VGAATTRIND:0x10			
Field Name	**Bits**	**Default**	**Description**
ATTR_GRPH_MODE	0	0x0	Graphics/Alphanumeric Mode 0=Alphanumeric Mode 1=Graphic Mode
ATTR_MONO_EN	1	0x0	Monochrome/Colour Attributes Select 0=Color Disp 1=Monochrome Disp
ATTR_LGRPH_EN	2	0x0	Line Graphics Enable. Must be 0 for character fonts that do not use line graphics character codes for graphics. 0 will force the 9th dot to the background colour. 1 will allow the 8th bit of the line graphics characters to be stretched to the 9th dot. 0=Disable line graphics 8th dot stretch 1=Enable line graphics 8th dot stretch
ATTR_BLINK_EN	3	0x0	Blink Enable/Background Intensity Selects whether bit 7 of the attribute controls intensity or blinking. 0=Intensity control 1=Blink control
ATTR_PANTOPONLY	5	0x0	PEL Panning Compatibility 0=Pan both halves of the screen 1=Pan only the top half screen
ATTR_PCLKBY2	6	0x0	PEL Clock Select 0=Shift register clocked every dot clock 1=For mode 13 (256 colour), 8 bits packed to form a pixel
ATTR_CSEL_EN	7	0x0	Alternate Colour Source 0=Select ATTR00-0F bits [5:4] as P5 and P4 1=Select ATTR14 bits [1:0] as P5 and P4
Mode Control Register			

ATTR11 - RW - 8 bits - VGAATTRIND:0x11			
Field Name	**Bits**	**Default**	**Description**
ATTR_OVSC	7:0	0x0	Overscan Colour
Overscan Colour Register			

ATTR12 - RW - 8 bits - VGAATTRIND:0x12			
Field Name	**Bits**	**Default**	**Description**
ATTR_MAP_EN	3:0	0x0	Enable Colour Map bits 0=Disables data from respective map from being used for video output. 1=Enables data from respective map for use in video output.
ATTR_VSMUX	5:4	0x0	Video Status Mux bits [1:0]. These are control bits for the multiplexer on colour bits P0-P7. The bit selection is also indicated at GENS1[5:4]: 00=P2, P0 01=P5, P4 10=P3, P1 11=P7, P6
Colour Map Enable Register			

ATTR13 - RW - 8 bits - VGAATTRIND:0x13			
Field Name	**Bits**	**Default**	**Description**
ATTR_PPAN	3:0	0x0	Shift Count Bits [3:0]. The shift count value (0-8) indicates how many pixle positions to shift left. Shift in respective modes Count Value: 0+,1+,2+,13 / All other 0: 1 / 0 1: 2 / - 2: 3 / 1 3: 4 / - 4: 5 / 2 5: 6 / - 6: 7 / 3 7: 8 / - 8: 0 / -
Horizontal PEL Panning Register			

ATTR14 - RW - 8 bits - VGAATTRIND:0x14			
Field Name	**Bits**	**Default**	**Description**
ATTR_CSEL1	1:0	0x0	Colour bits P5 and P4, respectively. These are the colour output bits (instead of bits 5 and 4 of the internal palette registers ATTR00-0F) when alternate colour source, bit ATTR10[7] is logical 1.
ATTR_CSEL2	3:2	0x0	Colour bits P7 and P6, respectively. These two bits are the two high-order bits of the 8-bit colour, used for rapid colour set switching (addressing different parts of the DAC colour lookup table). The lower order bits are in registers ATTR00-0F.
Colour Select Register			

2.9 Display Clock Control Registers

2.9.1 Primary Display Graphics Control Registers

D1GRPH_ENABLE - RW - 32 bits -, GpuF0MMReg:0x6100			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_ENABLE	0	0x1	Primary graphic enabled. 0=Disable 1=Enable
Primary graphic enabled.			

D1GRPH_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6104			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_DEPTH	1:0	0x0	Primary graphic pixel depth. 0=8bpp 1=16bpp 2=32bpp 3=64bpp
D1GRPH_Z	5:4	0x0	Z[1:0] value for tiling
D1GRPH_FORMAT	10:8	0x0	Primary graphic pixel format. It is used together with D1GRPH_DEPTH to define the graphic pixel format. If (D1GRPH_DEPTH = 0x0)(8 bpp) 0x0=Indexed Others=Reserved else if (D1GRPH_DEPTH = 0x1)(16 bpp) 0x0=ARGB 1555 0x1=RGB 565 0x2=ARGB 4444 0x3=Alpha index 88 0x4=Monochrome 16 0x5=BGRA 5551 Others=Reserved else if (D1GRPH_DEPTH = 0x2)(32 bpp) 0x0=ARGB 8888 0x1=ARGB 2101010 0x2=32bpp digital output 0x3=8-bit ARGB 2101010 0x4=BGRA 1010102 0x5=8-bit BGRA 1010102 0x6=RGB 111110 0x7=BGR 101111 Others=Reserved else if (D1GRPH_DEPTH = 0x3)(64 bpp) 0x0=ARGB 16161616 0x1=64bpp digital output ARGB[13:2] 0x2=64bpp digital output RGB[15:0] 0x3=64bpp digital output ARGB[11:0] 0x4=64bpp digital output BGR[15:0] Others=Reserved
D1GRPH_TILE_COMPACT_EN	12	0x0	Enables multichip tile compaction 0=Disable 1=Enable
D1GRPH_ADDRESS_TRANSLATION_ENABLE	16	0x0	Enables display 1 address translation 0=0=Physical memory 1=1=Virtual memory

D1GRPH_PRIVILEGED_ACCESS_ENABLE	17	0x0	Enables display 1 privileged page access 0=0=No priveledged access 1=1=Priveledged access
D1GRPH_ARRAY_MODE	23:20	0x0	Defines the tiling mode 0=ARRAY_LINEAR_GENERAL: Unaligned linear array 1=ARRAY_LINEAR_ALIGNED: Aligned linear array 2=ARRAY_1D_TILED_THIN1: Uses 1D 8x8x1 tiles 3=ARRAY_1D_TILED_THICK: Uses 1D 8x8x4 tiles 4=ARRAY_2D_TILED_THIN1: Uses 8x8x1 macro-tiles 5=ARRAY_2D_TILED_THIN2: Macro-tiles are 2x high 6=ARRAY_2D_TILED_THIN4: Macro-tiles are 4x high 7=ARRAY_2D_TILED_THICK: Uses 8x8x4 macro-tiles 8=ARRAY_2B_TILED_THIN1: uses row bank swapping 9=ARRAY_2B_TILED_THIN2: uses row bank swapping 10=ARRAY_2B_TILED_THIN4: uses row bank swapping 11=ARRAY_2B_TILED_THICK: uses row bank swapping 12=ARRAY_3D_TILED_THIN1: Slices are pipe rotated 13=ARRAY_3D_TILED_THICK: Slices are pipe rotated 14=ARRAY_3B_TILED_THIN1: Slices are pipe rotated 15=ARRAY_3B_TILED_THICK: Slices are pipe rotated
D1GRPH_16BIT_ALPHA_MODE	25:24	0x0	This field is only used if 64 bpp graphics bit depth and graphics/overlay blend using per-pixel alpha from graphics channel. It is used for processing 16 bit alpha. The fixed point graphics alpha value in the frame buffer is always clamped to 0.0 - 1.0 data range. 0x0=Floating point alpha (1 sign bit, 5 bit exponent, 10 bit mantissa) 0x1=Fixed point alpha with normalization from 256/256 to 255/255 to represent 1.0 0x2=Fixed point alpha with no normalization 0x3=Fixed point alpha using lower 8 bits of frame buffer value, no normalization
D1GRPH_16BIT_FIXED_ALPHA_RANGE	30:28	0x0	This register field is only used if 64 bpp graphics bit depth and D1GRPH_16BIT_ALPHA_MODE = 01 or 10. Also only used if graphics/overlay blend using per-pixel alpha from graphics channel. Final alpha blend value is rounded to 8 bits after optional normalization step (see D1GRPH_16BIT_ALPHA_MODE). 0x0=Use bits [15:0] of input alpha value for blend alpha 0x1=Use bits [14:0] of input alpha value for blend alpha 0x2=Use bits [13:0] of input alpha value for blend alpha 0x3=Use bits [12:0] of input alpha value for blend alpha 0x4=Use bits [11:0] of input alpha value for blend alpha 0x5=Use bits [10:0] of input alpha value for blend alpha 0x6=Use bits [9:0] of input alpha value for blend alpha 0x7=Use bits [8:0] of input alpha value for blend alpha
Primary graphic pixel depth and format.			

D1GRPH_LUT_SEL - RW - 32 bits -, GpuF0MMReg:0x6108			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_LUT_SEL	0	0x0	Primary graphic LUT selection. 0=Select LUTA 1=Select LUTB
D1GRPH_LUT_10BIT_BYPASS_EN	8	0x0	Enables bypass primary graphic LUT for 2101010 format 0=Use LUT 1=Bypass LUT when in 2101010 format. Ignored for other formats
D1GRPH_LUT_10BIT_BYPASS_DBL_BUF_EN	16	0x0	Enables double buffer D1GRPH_LUT_10BIT_BYPASS_EN 0=D1GRPH_LUT_10BIT_BYPASS_EN take effect right away 1=D1GRPH_LUT_10BIT_BYPASS_EN are double buffered
Primary graphic LUT selection.			

D1GRPH_SWAP_CNTL - RW - 32 bits -, GpuF0MMReg:0x610C			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_ENDIAN_SWAP	1:0	0x0	MC endian swap select 0=0=None 1=1=8in16(0xaabb=>0xbbaa) 2=2=8in32(0xaabbccdd=>0xddccbbaa) 3=3=8in64(0xaabbccddeeff0011=>0x1100ffeeddccbbaa)
D1GRPH_RED_CROSSBAR	5:4	0x0	Red crossbar select 0=0=Select from R 1=1=Select from G 2=2=Select from B 3=3=Select from A
D1GRPH_GREEN_CROSSBAR	7:6	0x0	Green crossbar select 0=0=Select from G 1=1=Select from B 2=2=Select from A 3=3=Select from R
D1GRPH_BLUE_CROSSBAR	9:8	0x0	Blue crossbar select 0=0=Select from B 1=1=Select from A 2=2=Select from R 3=3=Select from G
D1GRPH_ALPHA_CROSSBAR	11:10	0x0	Alpha crossbar select 0=0=Select from A 1=1=Select from R 2=2=Select from G 3=3=Select from B
Endian swap and component reorder control			

D1GRPH_PRIMARY_SURFACE_ADDRESS - RW - 32 bits -, GpuF0MMReg:0x6110			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_PRIMARY_DFQ_ENABLE	0	0x0	Primary surface address DFQ enable 0=0=One deep queue mode 1=1=DFQ mode
D1GRPH_PRIMARY_SURFACE_ADDRESS	31:8	0x0	Primary surface address for primary graphics in byte. It is 256 byte aligned.
Primary surface address for primary graphics in byte.			

D1GRPH_SECONDARY_SURFACE_ADDRESS - RW - 32 bits -, GpuF0MMReg:0x6118			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_SECONDARY_DFQ_ENABLE *(mirror of D1GRPH_PRIMARY_SURFACE_ADDRESS:D1GRPH_PRIMARY_DFQ_ENABLE)*	0	0x0	Secondary surface address DFQ enable 0=0=One deep queue mode 1=1=DFQ mode
D1GRPH_SECONDARY_SURFACE_ADDRESS	31:8	0x0	Secondary surface address for primary graphics in byte. It is 256 byte aligned.
Secondary surface address for primary graphics in byte.			

D1GRPH_PITCH - RW - 32 bits -, GpuF0MMReg:0x6120			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_PITCH	13:0	0x0	Primary graphic surface pitch in pixels. For Micro-tiled/Macro-tiled surface, it must be multiple of 64 pixeld in 8bpp mode. For Micro-linear/Macro-tiled surface, it must be multiple of 256 pixeld in 8bpp mode, multiple of 128 pixels in 16bpp mode and multiple of 64 pixels in 32bpp mode. For Micro-linear/Macro-linear surface, it must be multiple of 64 pixels in 8bpp mode. For other modes, it must be multiple of 32. Note: Bits [4:0] of this field are hardwired to 0.
Primary graphic surface pitch in pixels.			

D1GRPH_SURFACE_OFFSET_X - RW - 32 bits -, GpuF0MMReg:0x6124			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_SURFACE_OFFSET_X	12:0	0x0	Primary graphic X surface offset. It is 256 pixels aligned. Note: Bits [7:0] of this field are hardwired to 0.
Primary graphic X surface offset.			

D1GRPH_SURFACE_OFFSET_Y - RW - 32 bits -, GpuF0MMReg:0x6128			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_SURFACE_OFFSET_Y	12:0	0x0	Primary graphic Y surface offset. It must be even value Note: Bit [0] of this field is hardwired to 0.
Primary graphic Y surface offset.			

D1GRPH_X_START - RW - 32 bits -, GpuF0MMReg:0x612C			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_X_START	12:0	0x0	Primary graphic X start coordinate relative to the desktop coordinates.
Primary graphic X start coordinate relative to the desktop coordinates.			

D1GRPH_Y_START - RW - 32 bits -, GpuF0MMReg:0x6130			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_Y_START	12:0	0x0	Primary graphic Y start coordinate relative to the desktop coordinates.
Primary graphic Y start coordinate relative to the desktop coordinates.			

D1GRPH_X_END - RW - 32 bits -, GpuF0MMReg:0x6134			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_X_END	13:0	0x0	Primary graphic X end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K
Primary graphic X end coordinate relative to the desktop coordinates.			

D1GRPH_Y_END - RW - 32 bits -, GpuF0MMReg:0x6138			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_Y_END	13:0	0x0	Primary graphic Y end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K
Primary graphic Y end coordinate relative to the desktop coordinates.			

D1GRPH_UPDATE - RW - 32 bits -, GpuF0MMReg:0x6144			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_MODE_UPDATE_PENDING (R)	0	0x0	Primary graphic mode register update pending control. It is set to 1 after a host write to graphics mode register. It is cleared after double buffering is done. This signal is only visible through register. The graphics surface register includes: D1GRPH_DEPTH D1GRPH_FORMAT D1GRPH_SWAP_RB D1GRPH_LUT_SEL D1GRPH_LUT_10BIT_BYPASS_EN D1GRPH_ENABLE D1GRPH_X_START D1GRPH_Y_START D1GRPH_X_END D1GRPH_Y_END The mode register double buffering can only occur at vertical retrace. The double buffering occurs when D1GRPH_MODE_UPDATE_PENDING = 1 and D1GRPH_UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC1 is disabled, the registers will be updated instantly. 0=No update pending 1=Update pending
D1GRPH_MODE_UPDATE_TAKEN (R)	1	0x0	Primary graphics update taken status for mode registers. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0.
D1GRPH_SURFACE_UPDATE_PENDING (R)	2	0x0	Primary graphic surface register update pending control. If it is set to 1 after a host write to graphics surface register. It is cleared after double buffering is done. It is cleared after double buffering is done. This signal also goes to both the RBBM wait_until and to the CP_RTS_discrete inputs. The graphics surface register includes: D1GRPH_PRIMARY_SURFACE_ADDRESS D1GRPH_SECONDARY_SURFACE_ADDRESS D1GRPH_PITCH D1GRPH_SURFACE_OFFSET_X D1GRPH_SURFACE_OFFSET_Y. If D1GRPH_SURFACE_UPDATE_H_RETRACE_EN = 0, the double buffering occurs in vertical retrace when D1GRPH_SURFACE_UPDATE_PENDING = 1 and D1GRPH_UPDATE_LOCK = 0 and V_UPDATE = 1. Otherwise the double buffering happens at horizontal retrace when D1GRPH_SURFACE_UPDATE_PENDING = 1 and D1GRPH_UPDATE_LOCK = 0 and Data request for last chunk of the line is sent from DCP to DMIF. If CRTC1 is disabled, the registers will be updated instantly
D1GRPH_SURFACE_UPDATE_TAKEN (R)	3	0x0	Primary graphics update taken status for surface registers. If D1GRPH_SURFACE_UPDATE_H_RETRACE_EN = 0, it is set to 1 when double buffering occurs and cleared when V_UPDATE = 0. Otherwise, it is active for one clock cycle when double buffering occurs at the horizontal retrace.

D1GRPH_UPDATE_LOCK	16	0x0	Primary graphic register update lock control. This lock bit control both surface and mode register double buffer 0=Unlocked 1=Locked
D1GRPH_MODE_DISABLE_MULTIPLE_UPDATE	24	0x0	0=D1GRPH mode registers can be updated multiple times in one V_UPDATE period 1=D1GRPH mode registers can only be updated once in one V_UPDATE period
D1GRPH_SURFACE_DISABLE_MULTIPLE_UPDATE	28	0x0	0=D1GRPH surface registers can be updated multiple times in one V_UPDATE period 1=D1GRPH surface registers can only be updated once in one V_UPDATE period
Primary graphic update control			

D1GRPH_FLIP_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6148			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_SURFACE_UPDATE_H_RETRACE_EN	0	0x0	Enables primary graphic surface register double buffer in horizontal retrace. 0=Vertical retrace flipping 1=Horizontal retrace flipping
Enable primary graphic surface register double buffer in horizontal retrace			

D1GRPH_SURFACE_ADDRESS_INUSE - RW - 32 bits -, GpuF0MMReg:0x614C			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_SURFACE_ADDRESS_INUSE (R)	31:8	0x0	This register reads back snapshot of primary graphics surface address used for data request. The address is the signal sent to DMIF and is updated on SOF or horizontal surface update. The snapshot is triggered by writing 1 into field D1CRTC_SNAPSHOT_MANUAL_TRIGGER of CRTC register D1CRTC_SNAPSHOT_STATUS.
Snapshot of primary graphics surface address in use			

2.9.2 Primary Display Video Overlay Control Registers

D1OVL_ENABLE - RW - 32 bits -, GpuF0MMReg:0x6180			
Field Name	**Bits**	**Default**	**Description**
D1OVL_ENABLE	0	0x0	Primary overlay enabled. 0=Disable 1=Enable
Primary overlay enabled.			

D1OVL_CONTROL1 - RW - 32 bits -, GpuF0MMReg:0x6184			
Field Name	**Bits**	**Default**	**Description**
D1OVL_DEPTH	1:0	0x0	Primary overlay pixel depth 0=Reserved 1=16bpp 2=32bpp 3=Reserved
D1OVL_Z	5:4	0x0	Z[1:0] value for tiling
D1OVL_FORMAT	10:8	0x0	Primary overlay pixel format. It is used together with D1OVL_DEPTH to define the overlay format. If (D1OVL_DEPTH = 0x1)(16 bpp) 0x0=ARGB 1555 0x1=RGB 565 0x2=BGRA 5551 Others=Reserved else if (D1OVL_DEPTH = 0x2)(32 bpp) 0x0=ACrYCb 8888 or ARGB 8888 0x1=ACrYCb 2101010 or ARGB 2101010 0x2=CbACrA or BGRA 1010102 Others=Reserved
D1OVL_TILE_COMPACT_EN	12	0x0	Enables multichip tile compaction 0=Disable 1=Enable
D1OVL_ADDRESS_TRANSLATION_ENABLE	16	0x0	Enables Overlay 1 address translation 0=0=Physical memory 1=1=Virtual memory
D1OVL_PRIVILEGED_ACCESS_ENABLE	17	0x0	Enables Overlay 1 privileged access 0=0=No privileged access 1=1=Privileged access
D1OVL_ARRAY_MODE	23:20	0x0	Defines the tiling mode 0=ARRAY_LINEAR_GENERAL: Unaligned linear array 1=ARRAY_LINEAR_ALIGNED: Aligned linear array 2=ARRAY_1D_TILED_THIN1: Uses 1D 8x8x1 tiles 3=ARRAY_1D_TILED_THICK: Uses 1D 8x8x4 tiles 4=ARRAY_2D_TILED_THIN1: Uses 8x8x1 macro-tiles 5=ARRAY_2D_TILED_THIN2: Macro-tiles are 2x high 6=ARRAY_2D_TILED_THIN4: Macro-tiles are 4x high 7=ARRAY_2D_TILED_THICK: Uses 8x8x4 macro-tiles 8=ARRAY_2B_TILED_THIN1: uses row bank swapping 9=ARRAY_2B_TILED_THIN2: uses row bank swapping 10=ARRAY_2B_TILED_THIN4: uses row bank swapping 11=ARRAY_2B_TILED_THICK: uses row bank swapping 12=ARRAY_3D_TILED_THIN1: Slices are pipe rotated 13=ARRAY_3D_TILED_THICK: Slices are pipe rotated 14=ARRAY_3B_TILED_THIN1: Slices are pipe rotated 15=ARRAY_3B_TILED_THICK: Slices are pipe rotated
D1OVL_COLOR_EXPANSION_MODE	24	0x0	Primary overlay pixel format expansion mode. 0=Dynamic expansion for RGB 1=Zero expansion for YCbCr
Primary overlay pixel depth and format.			

D1OVL_CONTROL2 - RW - 32 bits -, GpuF0MMReg:0x6188			
Field Name	**Bits**	**Default**	**Description**
D1OVL_HALF_RESOLUTION_ENABLE	0	0x0	Primary overlay half resolution control 0=Disable 1=Enable
Primary overlay half resolution control			

D1OVL_SWAP_CNTL - RW - 32 bits -, GpuF0MMReg:0x618C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_ENDIAN_SWAP	1:0	0x0	MC endian swap select 0=0=None 1=1=8in16(0xaabb=>0xbbaa) 2=2=8in32(0xaabbccdd=>0xddccbbaa) 3=3=8in64(0xaabbccddeeff0011=>0x1100ffeeddccbbaa)
D1OVL_RED_CROSSBAR	5:4	0x0	Red crossbar select 0=0=Select from R 1=1=Select from G 2=2=Select from B 3=3=Select from A
D1OVL_GREEN_CROSSBAR	7:6	0x0	Green crossbar select 0=0=Select from G 1=1=Select from B 2=2=Select from A 3=3=Select from R
D1OVL_BLUE_CROSSBAR	9:8	0x0	Blue crossbar select 0=0=Select from B 1=1=Select from A 2=2=Select from R 3=3=Select from G
D1OVL_ALPHA_CROSSBAR	11:10	0x0	Alpha crossbar select 0=0=Select from A 1=1=Select from R 2=2=Select from G 3=3=Select from B
Endian swap and component reorder control			

D1OVL_SURFACE_ADDRESS - RW - 32 bits -, GpuF0MMReg:0x6190			
Field Name	**Bits**	**Default**	**Description**
D1OVL_DFQ_ENABLE	0	0x0	Surface address DFQ enable
D1OVL_SURFACE_ADDRESS	31:8	0x0	Primary overlay surface base address in byte. It is 256 bytes aligned.
Primary overlay surface base address in byte.			

D1OVL_PITCH - RW - 32 bits -, GpuF0MMReg:0x6198			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PITCH	13:0	0x0	Primary overlay surface pitch in pixels. For Micro-tiled/Macro-tiled surface, it must be multiple of 64 pixeld in 8bpp mode. For Micro-linear/Macro-tiled surface, it must be multiple of 256 pixeld in 8bpp mode, multiple of 128 pixels in 16bpp mode and multiple of 64 pixels in 32bpp mode. For Micro-linear/Macro-linear surface, it must be multiple of 64 pixels in 8bpp mode. For other modes, it must be multiple of 32. Note: Bits [4:0] of this field are hardwired to 0.
Primary overlay surface pitch in pixels.			

D1OVL_SURFACE_OFFSET_X - RW - 32 bits -, GpuF0MMReg:0x619C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_SURFACE_OFFSET_X	12:0	0x0	Primary overlay X surface offset. It is 256 pixels aligned. Note: Bits [7:0] of this field are hardwired to 0.
Primary overlay X surface offset.			

D1OVL_SURFACE_OFFSET_Y - RW - 32 bits -, GpuF0MMReg:0x61A0			
Field Name	**Bits**	**Default**	**Description**
D1OVL_SURFACE_OFFSET_Y	12:0	0x0	Primary overlay Y surface offset. It is even value. Note: Bit [0] of this field is hardwired to 0.
Primary overlay Y surface offset.			

D1OVL_START - RW - 32 bits -, GpuF0MMReg:0x61A4			
Field Name	**Bits**	**Default**	**Description**
D1OVL_Y_START	12:0	0x0	Primary overlay Y start coordinate relative to the desktop coordinates.
D1OVL_X_START	28:16	0x0	Primary overlay X start coordinate relative to the desktop coordinates.
Primary overlay X, Y start coordinate relative to the desktop coordinates.			

D1OVL_END - RW - 32 bits -, GpuF0MMReg:0x61A8			
Field Name	**Bits**	**Default**	**Description**
D1OVL_Y_END	13:0	0x0	Primary overlay Y end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K.
D1OVL_X_END	29:16	0x0	Primary overlay X end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K.
Primary overlay X, Y end coordinate relative to the desktop coordinates.			

D1OVL_UPDATE - RW - 32 bits -, GpuF0MMReg:0x61AC			
Field Name	**Bits**	**Default**	**Description**
D1OVL_UPDATE_PENDING (R)	0	0x0	Primary overlay register update pending control. It is set to 1 after a host write to overlay double buffer register. It is cleared after double buffering is done. The double buffering occurs when UPDATE_PENDING = 1 and UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC1 is disabled, the registers will be updated instantly. D1OVL double buffer registers include: D1OVL_ENABLE D1OVL_DEPTH D1OVL_FORMAT D1OVL_SWAP_RB D1OVL_COLOR_EXPANSION_MODE D1OVL_HALF_RESOLUTION_ENABLE D1OVL_SURFACE_ADDRESS D1OVL_PITCH D1OVL_SURFACE_OFFSET_X D1OVL_SURFACE_OFFSET_Y D1OVL_START D1OVL_END 0=No update pending 1=Update pending
D1OVL_UPDATE_TAKEN (R)	1	0x0	Primary overlay update taken status. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0.
D1OVL_UPDATE_LOCK	16	0x0	Primary overlay register update lock control. 0=Unlocked 1=Locked
D1OVL_DISABLE_MULTIPLE_UPDATE	24	0x0	0=D1OVL registers can be updated multiple times in one V_UPDATE period 1=D1OVL registers can only be updated once in one V_UPDATE period
Primary overlay register update			

D1OVL_SURFACE_ADDRESS_INUSE - RW - 32 bits -, GpuF0MMReg:0x61B0			
Field Name	**Bits**	**Default**	**Description**
D1OVL_SURFACE_ADDRESS_INUSE (R)	31:8	0x0	This register reads back snapshot of primary overlay surface address used for data request. The address is the signal sent to DMIF and is updated on SOF or horizontal surface update. The snapshot is triggered by writing 1 into field D1CRTC_SNAPSHOT_MANUAL_TRIGGER of CRTC register D1CRTC_SNAPSHOT_STATUS.
Snapshot of primary overlay surface address in use			

D1OVL_DFQ_CONTROL - RW - 32 bits -, GpuF0MMReg:0x61B4			
Field Name	**Bits**	**Default**	**Description**
D1OVL_DFQ_RESET	0	0x0	Reset the deep flip queue
D1OVL_DFQ_SIZE	6:4	0x0	Size of the deep flip queue 0=1 deep queue 1=2 deep queue ... 7=8 deep queue
D1OVL_DFQ_MIN_FREE_ENTRIES	10:8	0x0	Minimum # of free entries before surface pending is asserted
Control of the deep flip queue for D1 overlay			

D1OVL_DFQ_STATUS - RW - 32 bits -, GpuF0MMReg:0x61B8			
Field Name	**Bits**	**Default**	**Description**
D1OVL_DFQ_NUM_ENTRIES (R)	3:0	0x0	# of entries in deep flip queue 0=1 entry 1=2 entries ... 7=8 entries
D1OVL_DFQ_RESET_FLAG (R)	8	0x0	Sticky bit: Deep flip queue in reset
D1OVL_DFQ_RESET_ACK (W)	9	0x0	Clear D1OVL_DFQ_RESET_FLAG
Status of the deep flip queue for D1 overlay			

2.9.3 Primary Display Video Overlay Transform Registers

D1OVL_MATRIX_TRANSFORM_EN - RW - 32 bits -, GpuF0MMReg:0x6200			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_TRANSFORM_EN	0	0x0	Primary overlay matrix conversion enable 0=Disable 1=Enable
Primary overlay matrix conversion enable.			

D1OVL_MATRIX_COEF_1_1 - RW - 32 bits -, GpuF0MMReg:0x6204			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_1_1	18:0	0x198a0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D1OVL_MATRIX_SIGN_1_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_1_2 - RW - 32 bits -, GpuF0MMReg:0x6208			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_1_2	18:0	0x12a20	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D1OVL_MATRIX_SIGN_1_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_1_3 - RW - 32 bits -, GpuF0MMReg:0x620C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_1_3	18:0	0x0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D1OVL_MATRIX_SIGN_1_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_1_4 - RW - 32 bits -, GpuF0MMReg:0x6210			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_1_4	26:8	0x48700	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S11.1. Note: Bits [6:0] of this field are hardwired to 0.
D1OVL_MATRIX_SIGN_1_4	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_2_1 - RW - 32 bits -, GpuF0MMReg:0x6214			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_2_1	18:0	0x72fe0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D1OVL_MATRIX_SIGN_2_1	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_2_2 - RW - 32 bits -, GpuF0MMReg:0x6218			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_2_2	18:0	0x12a20	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D1OVL_MATRIX_SIGN_2_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_2_3 - RW - 32 bits -, GpuF0MMReg:0x621C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_2_3	18:0	0x79bc0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D1OVL_MATRIX_SIGN_2_3	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_2_4 - RW - 32 bits -, GpuF0MMReg:0x6220			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_2_4	26:8	0x22100	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S11.1. Note: Bits [6:0] of this field are hardwired to 0.
D1OVL_MATRIX_SIGN_2_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_3_1 - RW - 32 bits -, GpuF0MMReg:0x6224			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_3_1	18:0	0x0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D1OVL_MATRIX_SIGN_3_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_3_2 - RW - 32 bits -, GpuF0MMReg:0x6228			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_3_2	18:0	0x12a20	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D1OVL_MATRIX_SIGN_3_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_3_3 - RW - 32 bits -, GpuF0MMReg:0x622C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_3_3	18:0	0x20460	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D1OVL_MATRIX_SIGN_3_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_3_4 - RW - 32 bits -, GpuF0MMReg:0x6230			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_3_4	26:8	0x3af80	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S11.1. Note: Bits [6:0] of this field are hardwired to 0.
D1OVL_MATRIX_SIGN_3_4	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

2.9.4 Primary Display Video Overlay Gamma Correction Registers

D1OVL_PWL_TRANSFORM_EN - RW - 32 bits -, GpuF0MMReg:0x6280			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_TRANSFORM_EN	0	0x0	Primary overlay gamma correction enable. 0=Disable 1=Enable
Primary overlay gamma correction enable.			

D1OVL_PWL_0TOF - RW - 32 bits -, GpuF0MMReg:0x6284			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_0TOF_OFFSET	8:0	0x0	Primary overlay gamma correction non-linear offset for input 0x0-0xF. Format fix-point 8.1 (0.0 to +255.5).
D1OVL_PWL_0TOF_SLOPE	26:16	0x100	Primary overlay gamma correction non-linear slope for input 0x0-0xF. Format fix-point 3.8 (0.00 to +7.99).
Primary overlay gamma correction non-linear offset and slope for input 0x0-0xF			

D1OVL_PWL_10TO1F - RW - 32 bits -, GpuF0MMReg:0x6288			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_10TO1F_OFFSET	8:0	0x20	Primary overlay gamma correction non-linear offset for input 0x10-0x1F. Format fix-point 8.1 (0.0 to +255.5).
D1OVL_PWL_10TO1F_SLOPE	26:16	0x100	Primary overlay gamma correction non-linear slope for input 0x10-0x1F. Format fix-point 3.8 (0.00 to +7.99).
Primary overlay gamma correction non-linear offset and slope for input 0x10-0x1F			

D1OVL_PWL_20TO3F - RW - 32 bits -, GpuF0MMReg:0x628C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_20TO3F_OFFSET	9:0	0x40	Primary overlay gamma correction non-linear offset for input 0x20-0x3F. Format fix-point 9.1 (0.0 to +511.5).
D1OVL_PWL_20TO3F_SLOPE	25:16	0x100	Primary overlay gamma correction non-linear slope for input 0x20-0x3F. Format fix-point 2.8 (0.00 to +3.99).
Primary overlay gamma correction non-linear offset and slope for input 0x20-0x3F			

D1OVL_PWL_40TO7F - RW - 32 bits -, GpuF0MMReg:0x6290			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_40TO7F_OFFSET	9:0	0x80	Primary overlay gamma correction non-linear offset for input 40-7F. Format fix-point 9.1 (0.0 to +511.5).
D1OVL_PWL_40TO7F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 40-7F. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 40-7F.			

D1OVL_PWL_80TOBF - RW - 32 bits -, GpuF0MMReg:0x6294			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_80TOBF_OFFSET	10:0	0x100	Primary overlay gamma correction non-linear offset for input 80-BF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_80TOBF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 80-BF. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 80-BF.			

D1OVL_PWL_C0TOFF - RW - 32 bits -, GpuF0MMReg:0x6298			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_C0TOFF_OFFSET	10:0	0x180	Primary overlay gamma correction non-linear offset for input C0-FF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_C0TOFF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input C0-FF. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input C0-FF.			

D1OVL_PWL_100TO13F - RW - 32 bits -, GpuF0MMReg:0x629C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_100TO13F_OFFSET	10:0	0x200	Primary overlay gamma correction non-linear offset for input 100-13F. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_100TO13F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 100-13F. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 100-13F.			

D1OVL_PWL_140TO17F - RW - 32 bits -, GpuF0MMReg:0x62A0			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_140TO17F_OFFSET	10:0	0x280	Primary overlay gamma correction non-linear offset for input 140-17F. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_140TO17F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 140-17F. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 140-17F.			

D1OVL_PWL_180TO1BF - RW - 32 bits -, GpuF0MMReg:0x62A4			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_180TO1BF_OFFSET	10:0	0x300	Primary overlay gamma correction non-linear offset for input 180-1BF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_180TO1BF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 180-1BF. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 180-1BF.			

D1OVL_PWL_1C0TO1FF - RW - 32 bits -, GpuF0MMReg:0x62A8			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_1C0TO1FF_OFFSET	10:0	0x380	Primary overlay gamma correction non-linear offset for input 1C0-1FF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_1C0TO1FF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 1C0-1FF. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 1C0-1FF.			

D1OVL_PWL_200TO23F - RW - 32 bits -, GpuF0MMReg:0x62AC			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_200TO23F_OFFSET	10:0	0x400	Primary overlay gamma correction non-linear offset for input 200-23F. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_200TO23F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 200-23F. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 200-23F.			

D1OVL_PWL_240TO27F - RW - 32 bits -, GpuF0MMReg:0x62B0			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_240TO27F_OFFSET	10:0	0x480	Primary overlay gamma correction non-linear offset for input 240-27F. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_240TO27F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 240-27F. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 240-27F.			

D1OVL_PWL_280TO2BF - RW - 32 bits -, GpuF0MMReg:0x62B4			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_280TO2BF_OFFSET	10:0	0x500	Primary overlay gamma correction non-linear offset for input 280-2BF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_280TO2BF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 280-2BF. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 280-2BF.			

D1OVL_PWL_2C0TO2FF - RW - 32 bits -, GpuF0MMReg:0x62B8			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_2C0TO2FF_OFFSET	10:0	0x580	Primary overlay gamma correction non-linear offset for input 2C0-2FF. Format fix-point 10.1(0.0 to +1023.5).
D1OVL_PWL_2C0TO2FF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 2C0-2FF. Format fix-point 1.8(0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 2C0-2FF.			

D1OVL_PWL_300TO33F - RW - 32 bits -, GpuF0MMReg:0x62BC			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_300TO33F_OFFSET	10:0	0x600	Primary overlay gamma correction non-linear offset for input 300-33F. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_300TO33F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 300-33F. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 300-33F.			

D1OVL_PWL_340TO37F - RW - 32 bits -, GpuF0MMReg:0x62C0			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_340TO37F_OFFSET	10:0	0x680	Primary overlay gamma correction non-linear offset for input 340-37F. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_340TO37F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 340-37F. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 340-37F.			

D1OVL_PWL_380TO3BF - RW - 32 bits -, GpuF0MMReg:0x62C4			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_380TO3BF_OFFSET	10:0	0x700	Primary overlay gamma correction non-linear offset for input 380-3BF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_380TO3BF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 380-3BF. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 380-3BF.			

D1OVL_PWL_3C0TO3FF - RW - 32 bits -, GpuF0MMReg:0x62C8			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_3C0TO3FF_OFFSET	10:0	0x780	Primary overlay gamma correction non-linear offset for input 3C0-3FF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_3C0TO3FF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 3C0-3FF. Format fix-point 1.8 (0.00 to +1.99).
Primary overlay gamma correction non-linear offset and slope for input 3C0-3FF.			

2.9.5 Primary Display Graphics and Overlay Blending Registers

D1OVL_KEY_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6300			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_KEY_FUNCTION	1:0	0x0	Selects graphic keyer result equation for primary display. 0=GRPH1_KEY = FALSE = 0 1=GRPH1_KEY = TRUE = 1 2=GPPH1_KEY = (GRPH1_RED in range) AND (GRPH1_GREEN in range) AND (GRPH1_BLUE in range) AND(GRPH1_ALPHA in range) 3=GRPH1_KEY = not [(GRPH1_RED in range) AND (GRPH1_GREEN in range) AND (GRPH1_BLUE in range) AND(GRPH1_ALPHA in range)]
D1OVL_KEY_FUNCTION	9:8	0x0	Selects overlay keyer result equation for primary display. 0=OVL1_KEY = FALSE = 0 1=OVL1_KEY = TRUE = 1 2=OVL1_KEY = (OVL1_Cr_RED in range) AND (OVL1_Y_GREEN in range) AND (OVL1_Cb_BLUE in range) AND (OVL1_ALPHA in range) 3=OVL1_KEY = not [(OVL1_Cr_RED in range) AND (OVL1_Y_GREEN in range) AND (OVL1_Cb_BLUE in range) AND (OVL1_ALPHA in range)]
D1OVL_KEY_COMPARE_MIX	16	0x0	Selects final mix of graphics and overlay keys for primary display. 0=GRPH_OVL_KEY = GRPH_KEY or OVL_KEY 1=GRPH_OVL_KEY = GRPH_KEY and OVL_KEY
Primary display key control			

D1GRPH_ALPHA - RW - 32 bits -, GpuF0MMReg:0x6304			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_ALPHA	7:0	0xff	Global graphic alpha for use in key mode and global alpha modes. See D1OVL_ALPHA_MODE register filed for more details
Global graphic alpha for use in key mode and global alpha modes.			

D1OVL_ALPHA - RW - 32 bits -, GpuF0MMReg:0x6308			
Field Name	**Bits**	**Default**	**Description**
D1OVL_ALPHA	7:0	0xff	Global overlay alpha for use in key mode and global alpha modes. See D1OVL_ALPHA_MODE register filed for more details
Global overlay alpha for use in key mode and global alpha modes.			

D1OVL_ALPHA_CONTROL - RW - 32 bits -, GpuF0MMReg:0x630C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_ALPHA_MODE	1:0	0x0	Graphics/overlay alpha blending mode for primary controller. In any case, if there is only graphics, the input OVL_DATA is forced to blank. If there is only overlay, the input GRPH_DATA is forced to blank. 0=Keyer mode, select graphic or overlay keyer to mix graphics and overlay 1=Per pixel graphic alpha mode.Alpha blend graphic and overlay layer. The alpha from graphic pixel may be inverted according to register field 2=Global alpha mode 3=Per pixel overlay alpha mode
D1OVL_ALPHA_PREMULT	8	0x0	For use with per pixel alpha blend mode. Selects whether pre-multiplied alpha or non-multiplied alpha. 0=0x0 - When DxOVL_ALPHA_MODE = 0x1, then Pixel = PIX_ALPHA * graphics pixel + (1-PIX_ALPHA) * overlay pixel.When DxOVL_ALPHA_MODE = 0x3, then Pixel = PIX_ALPHA * overlay pixel + (1-PIX_ALPHA) * graphic pixel 1=0x1 - When DxOVL_ALPHA_MODE = 0x1, then Pixel = graphic pixel + (1-PIX_ALPHA) * overlay pixel.When DxOVL_ALPHA_MODE = 0x3, then Pixel = overlay pixel + (1-PIX_ALPHA) * graphic pixel
D1OVL_ALPHA_INV	16	0x0	For use with pixel blend mode. Apply optional inversion to the alpha value extracted form the graphics or overlay surface data. 0=PIX_ALPHA = alpha from graphics or overlay 1=PIX_ALPHA = 1 - alpha from graphics or overlay
Primary display graphics/overlay alpha blending control			

D1GRPH_KEY_RANGE_RED - RW - 32 bits -, GpuF0MMReg:0x6310			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_KEY_RED_LOW	15:0	0x0	Primary graphics keyer red component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D1GRPH_KEY_RED_HIGH	31:16	0x0	Primary graphics keyer red component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
Primary graphics keyer red component range			

D1GRPH_KEY_RANGE_GREEN - RW - 32 bits -, GpuF0MMReg:0x6314			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_KEY_GREEN_LOW	15:0	0x0	Primary graphics keyer green component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D1GRPH_KEY_GREEN_HIGH	31:16	0x0	Primary graphics keyer green component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
Primary graphics keyer green component range			

D1GRPH_KEY_RANGE_BLUE - RW - 32 bits -, GpuF0MMReg:0x6318			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_KEY_BLUE_LOW	15:0	0x0	Primary graphics keyer blue component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D1GRPH_KEY_BLUE_HIGH	31:16	0x0	Primary graphics keyer blue component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
Primary graphics keyer blue component range			

D1GRPH_KEY_RANGE_ALPHA - RW - 32 bits -, GpuF0MMReg:0x631C			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_KEY_ALPHA_LOW	15:0	0x0	Primary graphics keyer alpha component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D1GRPH_KEY_ALPHA_HIGH	31:16	0x0	Primary graphics keyer alpha component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
Primary graphics keyer alpha component range			

D1OVL_KEY_RANGE_RED_CR - RW - 32 bits -, GpuF0MMReg:0x6320			
Field Name	**Bits**	**Default**	**Description**
D1OVL_KEY_RED_CR_LOW	9:0	0x0	Primary overlay keyer red component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D1OVL_KEY_RED_CR_HIGH	25:16	0x0	Primary overlay keyer red component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
Primary overlay keyer red component range			

D1OVL_KEY_RANGE_GREEN_Y - RW - 32 bits -, GpuF0MMReg:0x6324			
Field Name	**Bits**	**Default**	**Description**
D1OVL_KEY_GREEN_Y_LOW	9:0	0x0	Primary overlay keyer green component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D1OVL_KEY_GREEN_Y_HIGH	25:16	0x0	Primary overlay keyer green component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
Primary overlay keyer green component range			

D1OVL_KEY_RANGE_BLUE_CB - RW - 32 bits -, GpuF0MMReg:0x6328			
Field Name	**Bits**	**Default**	**Description**
D1OVL_KEY_BLUE_CB_LOW	9:0	0x0	Primary overlay keyer blue component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D1OVL_KEY_BLUE_CB_HIGH	25:16	0x0	Primary overlay keyer blue component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
Primary overlay keyer blue component range			

D1OVL_KEY_ALPHA - RW - 32 bits -, GpuF0MMReg:0x632C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_KEY_ALPHA_LOW	7:0	0x0	Primary overlay keyer alpha component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D1OVL_KEY_ALPHA_HIGH	23:16	0x0	Primary overlay keyer alpha component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
Primary overlay keyer alpha component range			

2.9.6 Primary Display Color Matrix Transform Registers

D1OVL_COLOR_MATRIX_TRANSFORMATION_CNTL - RW - 32 bits -, GpuF0MMReg:0x6140			
Field Name	**Bits**	**Default**	**Description**
D1OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	2:0	0x0	Matrix transformation control for primary display overlay pixels. It is used when PIX_TYPE is 0. 0=No color space adjustment on display output of overlay pixels 1=Apply display x color spcae control on the overlay pixels based on DxCOLOR_MATRIX_COEF register settings 2=Convert overlay pixel to standard definition YCbCr(601) color space 3=Convert overlay pixels to high definition YCbCR(709) color space 4=Convert overlay pixels to high definition TVRGB color space
Matrix transformation control for primary display overlay pixels.			

D1GRPH_DFQ_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6150			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_DFQ_RESET	0	0x0	Reset the deep flip queue
D1GRPH_DFQ_SIZE	6:4	0x0	Size of the deep flip queue 0=1 deep queue 1=2 deep queue ... 7=8 deep queue
D1GRPH_DFQ_MIN_FREE_ENTRIES	10:8	0x0	Minimum # of free entries before surface pending is asserted
Control of the deep flip queue for D1 graphics			

D1GRPH_DFQ_STATUS - RW - 32 bits -, GpuF0MMReg:0x6154			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_PRIMARY_DFQ_NUM_ENTRIES (R)	3:0	0x0	# of entries in primary deep flip queue 0=1 entry 1=2 entries ... 7=8 entries
D1GRPH_SECONDARY_DFQ_NUM_ENTRIES (R)	7:4	0x0	# of entries in secondary deep flip queue 0=1 entry 1=2 entries ... 7=8 entries
D1GRPH_DFQ_RESET_FLAG (R)	8	0x0	Sticky bit: Deep flip queue in reset
D1GRPH_DFQ_RESET_ACK (W)	9	0x0	Clear D1GRPH_DFQ_RESET_FLAG
Status of the deep flip queue for D1 graphics			

D1GRPH_INTERRUPT_STATUS - RW - 32 bits -, GpuF0MMReg:0x6158			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_PFLIP_INT_OCCURRED (R)	0	0x0	Display 1 graphics surface flip occurred
D1GRPH_PFLIP_INT_CLEAR (W)	8	0x0	Write 1 to this filed will clear D1GRPH_PFLIP_INT_OCCURRED bit
Display 1 graphics interrupt status			

D1GRPH_INTERRUPT_CONTROL - RW - 32 bits -, GpuF0MMReg:0x615C			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_PFLIP_INT_MASK	0	0x0	Interrupt mask for Display 1 graphics surface flip 0=Disables interrupt 1=Enables interrupt
D1GRPH_PFLIP_INT_TYPE	8	0x0	0=Legacy level based interrupt 1=Pulse based interrupt
Display 1 graphics interrupt mask			

D1GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL - RW - 32 bits -, GpuF0MMReg:0x6380			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_COLOR_MATRIX_TRANSFORMATION_EN	0	0x0	Matrix transformation control for primary display graphics and cursor pixel. It is used when PIX_TYPE is 1. 0=Disable 1=Enable
Matrix transformation control for primary display graphics and cursor pixel.			

D1COLOR_MATRIX_COEF_1_1 - RW - 32 bits -, GpuF0MMReg:0x6384			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_1_1	16:0	0x0	Combined matrix constant C11 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S1.11(-2.00 to +1.99). Note: Bits [4:0] of this field are hardwired to 0.
D1COLOR_MATRIX_SIGN_1_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C11 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_1_2 - RW - 32 bits -, GpuF0MMReg:0x6388			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_1_2	15:0	0x0	Combined matrix constant C12 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S0.11(-1.00 to + 0.99). Note: Bits[4:0] of this field are hardwired to 0.
D1COLOR_MATRIX_SIGN_1_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C12 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_1_3 - RW - 32 bits -, GpuF0MMReg:0x638C			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_1_3	15:0	0x0	Combined matrix constant C13 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S0.11(-1.0 to +0.99). Note: Bits [4:0] of this field are hardwired to 0.
D1COLOR_MATRIX_SIGN_1_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C13 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_1_4 - RW - 32 bits -, GpuF0MMReg:0x6390			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_1_4	26:8	0x0	Combined matrix constant C14 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S11.1(-2048.5 to +2047.5). It includes subtraction of 512 offset Note: Bits [6:0] of this field are hardwired to 0.
D1COLOR_MATRIX_SIGN_1_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C14 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_2_1 - RW - 32 bits -, GpuF0MMReg:0x6394			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_2_1	15:0	0x0	Combined matrix constant C21 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S0.11(-1.00 to +0.99). Note: Bits [4:0] of this field are hardwired to 0.
D1COLOR_MATRIX_SIGN_2_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C21 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_2_2 - RW - 32 bits -, GpuF0MMReg:0x6398			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_2_2	16:0	0x0	Combined matrix constant C22 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S1.11(-2.00 to +1.99). Note: Bits [4:0] of this field are hardwired to 0.
D1COLOR_MATRIX_SIGN_2_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C22 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_2_3 - RW - 32 bits -, GpuF0MMReg:0x639C			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_2_3	15:0	0x0	Combined matrix constant C23 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S0.11(-1.00 to +0.99). Note: Bits [4:0] of this field are hardwired to 0.
D1COLOR_MATRIX_SIGN_2_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C23 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_2_4 - RW - 32 bits -, GpuF0MMReg:0x63A0			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_2_4	26:8	0x0	Combined matrix constant C24 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S11.1(-2048.5 to +2047.5). It includes subtraction of 512 offset Note: Bits [6:0] of this field are hardwired to 0.
D1COLOR_MATRIX_SIGN_2_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C24 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_3_1 - RW - 32 bits -, GpuF0MMReg:0x63A4			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_3_1	15:0	0x0	Combined matrix constant C31 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S0.11(-1.00 to +0.99). Note: Bits [4:0] of this field are hardwired to 0.
D1COLOR_MATRIX_SIGN_3_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C31 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_3_2 - RW - 32 bits -, GpuF0MMReg:0x63A8			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_3_2	15:0	0x0	Combined matrix constant C32 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S0.11(-1.00 to +0.99). Note: Bits [4:0] of this field are hardwired to 0.
D1COLOR_MATRIX_SIGN_3_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C32 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_3_3 - RW - 32 bits -, GpuF0MMReg:0x63AC			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_3_3	16:0	0x0	Combined matrix constant C33 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S1.11(-2.00 to +1.99). Note: Bits [4:0] of this field are hardwired to 0.
D1COLOR_MATRIX_SIGN_3_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C33 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_3_4 - RW - 32 bits -, GpuF0MMReg:0x63B0			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_3_4	26:8	0x0	Combined matrix constant C34 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S11.1(-2048.5 to +2047.5). It includes subtraction of 512 offset Note: Bits [6:0] of this field are hardwired to 0.
D1COLOR_MATRIX_SIGN_3_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C34 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

2.9.7 Primary Display Subsampling Registers

D1COLOR_SPACE_CONVERT - RW - 32 bits -, GpuF0MMReg:0x613C			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_SUBSAMPLE_CRCB_MODE	1:0	0x0	Sub-sampling control for primary display 0=Do not subsample CrCb(RB) 1=Subsample CrCb (RB) by using 2 tap average method 2=Subsample CrCb (RB) by using 1 tap on even pixel 3=Subsample CrCb (RB) by using 1 tap on odd pixel
Sub-sampling control for primary display.			

2.9.8 Primary Display Realtime Overlay Registers

D1OVL_RT_SKEWCOMMAND - RW - 32 bits -, GpuF0MMReg:0x6500			
Field Name	**Bits**	**Default**	**Description**
D1OVL_RT_CLEAR_GOBBLE_COUNT (W)	0	0x0	Writing 1 to this bit clears the gobbleCount. This bit has higher priority than inc_gobblecount
D1OVL_RT_INC_GOBBLE_COUNT (W)	4	0x0	Writing 1 to this bit increments the gobbleCount
D1OVL_RT_CLEAR_SUBMIT_COUNT (W)	8	0x0	Writing 1 to this bit clears the submitCount. This bit has higher priority than inc_submitcount
D1OVL_RT_INC_SUBMIT_COUNT (W)	12	0x0	Writing 1 to this bit increments the submitCount
D1OVL_RT_GOBBLE_COUNT (R)	18:16	0x0	Read only register The gobble count value increments with each inc_gobble_count, and resets with clear_gobble_count commands. It wraps around on overflow during increment.
D1OVL_RT_SUBMIT_COUNT (R)	26:24	0x0	Read only register Submits the count value which increments with each inc_submit_count, and resets with clear_submit_count commands. It wraps around on overflow during increment.
Reset or increment submit and gobble count			

D1OVL_RT_SKEWCONTROL - RW - 32 bits -, GpuF0MMReg:0x6504			
Field Name	**Bits**	**Default**	**Description**
D1OVL_RT_CAPS	2:0	0x0	Max value in submitCount and gobbleCount. This is the number of contents buffer - 1 It should reset counters before programming this field
D1OVL_RT_SKEW_MAX	6:4	0x0	Max skew allowed between gobbleCount and submitCount
Controls for submit and gobble counts			

D1OVL_RT_BAND_POSITION - RW - 32 bits -, GpuF0MMReg:0x6508			
Field Name	**Bits**	**Default**	**Description**
D1OVL_RT_TOP_SCAN	13:0	0x0	Defines the top scan line for the next RT (inclusive)
D1OVL_RT_BTM_SCAN	29:16	0x0	Defines the bottom scan line for next RT (exclusive)
the position of the top and bottom scan line for next RT			

D1OVL_RT_PROCEED_COND - RW - 32 bits -, GpuF0MMReg:0x650C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_RT_REDUCE_DELAY	0	0x0	0=Selects delay optimized scheme 1=Selects basic render behind delay scan scheme
D1OVL_RT_RT_FLIP	4	0x0	0=Selects bandSync to be exposed to CP 1=Selects frameSync to be exposed to CP
D1OVL_RT_PROCEED_ON_EOF_DISABLE	8	0x0	0=Enables unfinished bands to pass bandSync on EOF (valid only in basic scheme) 1=Disables this feature
D1OVL_RT_WITH_HELD_ON_SOF	12	0x0	0=Disables proceedOnEOF on next frameSync 1=Disables proceedOnEOF on next SOF
D1OVL_RT_CLEAR_GOBBLE_GO (W)	14	0x0	This bit clears gobbleGo. It disables another frame submit before next flip (ignored in basic scheme)
D1OVL_RT_TEAR_PROOF_HEIGHT	29:16	0x0	Defines the number of scan lines above topscan. If display starts reading from there, RT should wait
Select RT flip proceed condition			

D1OVL_RT_STAT - RW - 32 bits -, GpuF0MMReg:0x6510			
Field Name	**Bits**	**Default**	**Description**
D1OVL_RT_FIP_PROCEED_ACK (W)	0	0x0	The sticky bit clears the FIP_PROCEED FLAG flag when written
D1OVL_RT_FRAME_SYNC_ACK (W)	1	0x0	The sticky bit clears the RT_FRAME_SYNC flag when written
D1OVL_RT_OVL_START_ACK (W)	2	0x0	The sticky bit clears the OVL_START FLAG flag when written
D1OVL_RT_BAND_INVISIBLE (R)	8	0x0	Debug bit indicating that overlay scanning in invisble region
D1OVL_RT_BAND_SYNC (R)	9	0x0	Debug bit indicating that overlay bottom scan is less the line counter
D1OVL_RT_EOF_PRPCEED (R)	10	0x0	Debug bit indicating that overlay is ended. Set at eof and reset at overlay start
D1OVL_RT_FIP_PROCEED (R)	11	0x0	Sticky debug bit that set when RT_FLIP_PROCEED signal asserted.
D1OVL_RT_FRAME_SYNC (R)	12	0x0	Sticky debug bit indicating that overlay start set and a new submission occured
D1OVL_RT_GOBBLE_GO (R)	13	0x0	Debug bit that set on frame_sync and clear at gobbleclr
D1OVL_RT_NEW_SUBMIT (R)	14	0x0	Debug bit indicating a new submission occurred
D1OVL_RT_OVL_START (R)	15	0x0	Debug bit indicating that line buffer detects start of overlay being accessed
D1OVL_RT_OVL_ENDED (R)	16	0x0	Debug bit indicating that line buffer detects that the end of overlay being accessed
D1OVL_RT_SAFE_ZONE (R)	17	0x0	Debug bit indicating that overlay is scaning in safe zone
D1OVL_RT_SWITCH_REGIONS (R)	18	0x0	Debug bit showing the postion of scan region relative to display
D1OVL_SKEW_MAX_REACHED (R)	19	0x0	Debug bit indicating that line buffer detected maximum skew reached
D1OVL_LINE_COUNTER (R)	31:20	0x0	Debug bit showing display line counter value
Status Bits			

2.9.9 Primary Display Hardware Cursor Registers

D1CUR_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6400			
Field Name	**Bits**	**Default**	**Description**
D1CURSOR_EN	0	0x0	Primary display hardware cursor enabled. 0=Disable 1=Enable
D1CURSOR_MODE	9:8	0x0	Primary display hardware cursor mode. For 2bpp mode, each line of cursor data is stored in memory as 16 bits of AND data followed by 16 bits XOR data. For color AND/XOR mode, each pixel is stored sequentially in memory as 32bits each in aRGB8888 format with bit 31 of each DWord being the AND bit. For the color alpha modes the format is also 32bpp aRGB8888 with all 8 bits of the alpha being used.All HW cursor lines must be 64 pixels wide and all lines must be stored sequentially in memory. 0=Mono (2bpp) 1=Color 24bpp + 1 bit AND (32bpp) 2=Color 24bpp + 8 bit alpha (32bpp) premultiplied alpha 3=Color 24bpp + 8 bit alpha (32bpp)unmultiplied alpha

D1CURSOR_2X_MAGNIFY	16	0x0	Primary display hardware cursor 2x2 magnification. 0=No 2x2 magnification 1=2x2 magnification in horizontal and vertical direction
D1CURSOR_FORCE_MC_ON	20	0x0	When set, if the incoming data is in D1 cursor region, DCP_LB_cursor1_allow_stutter is set. This field in this double bufferred register is not double buffered
Primary display hardware control			

D1CUR_SURFACE_ADDRESS - RW - 32 bits -, GpuF0MMReg:0x6408			
Field Name	**Bits**	**Default**	**Description**
D1CURSOR_SURFACE_ADDRESS	31:0	0x0	Primary display hardware cursor surface base address in byte. It is 4K byte aligned. Note: Bits {11:0] of this field are hardwired to 0.
Primary display hardware cursor surface base address.			

D1CUR_SIZE - RW - 32 bits -, GpuF0MMReg:0x6410			
Field Name	**Bits**	**Default**	**Description**
D1CURSOR_HEIGHT	5:0	0x0	Primary display hardware cursor height minus 1.
D1CURSOR_WIDTH	21:16	0x0	Primary display hardware cursor width minus 1.
Primary display hardware size			

D1CUR_POSITION - RW - 32 bits -, GpuF0MMReg:0x6414			
Field Name	**Bits**	**Default**	**Description**
D1CURSOR_Y_POSITION	12:0	0x0	Primary display hardware cursor X coordinate at the hot spot relative to the desktop coordinates.
D1CURSOR_X_POSITION	28:16	0x0	Primary display hardware cursor X coordinate at the hot spot relative to the desktop coordinates.
Primary display hardware cursor position			

D1CUR_HOT_SPOT - RW - 32 bits -, GpuF0MMReg:0x6418			
Field Name	**Bits**	**Default**	**Description**
D1CURSOR_HOT_SPOT_Y	5:0	0x0	Primary display hardware cursor hot spot X length relative to the top left corner.
D1CURSOR_HOT_SPOT_X	21:16	0x0	Primary display hardware cursor hot spot Y length relative to the top left corner.
Primary display hardware cursor hot spot position			

D1CUR_COLOR1 - RW - 32 bits -, GpuF0MMReg:0x641C			
Field Name	**Bits**	**Default**	**Description**
D1CUR_COLOR1_BLUE	7:0	0x0	Primary display hardware cursor blue component of color 1.
D1CUR_COLOR1_GREEN	15:8	0x0	Primary display hardware cursor green component of color 1.
D1CUR_COLOR1_RED	23:16	0x0	Primary display hardware cursor red component of color 1.
Primary display hardware cursor color 1.			

D1CUR_COLOR2 - RW - 32 bits -, GpuF0MMReg:0x6420			
Field Name	**Bits**	**Default**	**Description**
D1CUR_COLOR2_BLUE	7:0	0x0	Primary display hardware cursor blue component of color 2.
D1CUR_COLOR2_GREEN	15:8	0x0	Primary display hardware cursor green component of color 2.
D1CUR_COLOR2_RED	23:16	0x0	Primary display hardware cursor red component of color 2.
Primary display hardware cursor color 2.			

D1CUR_UPDATE - RW - 32 bits -, GpuF0MMReg:0x6424			
Field Name	**Bits**	**Default**	**Description**
D1CURSOR_UPDATE_PENDING (R)	0	0x0	Primary display hardware cursor update pending status. It is set to 1 after a host write to cursor double buffer register. It is cleared after double buffering is done. The double buffering occurs when D1CURSOR_UPDATE_PENDING = 1 and D1CURSOR_UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC1 is disabled, the registers will be updated instantly. The D1CUR double buffer registers are: D1CURSOR_EN D1CURSOR_MODE D1CURSOR_2X_MAGNIFY D1CURSOR_SURFACE_ADDRESS D1CURSOR_HEIGHT D1CURSOR_WIDTH D1CURSOR_X_POSITION D1CURSOR_Y_POSITION D1CURSOR_HOT_SPOT_X D1CURSOR_HOT_SPOT_Y 0=No update pending 1=Update pending
D1CURSOR_UPDATE_TAKEN (R)	1	0x0	Primary display hardware cursor update taken status. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0
D1CURSOR_UPDATE_LOCK	16	0x0	Primary display hardware cursor update lock control. 0=Unlocked 1=Locked
D1CURSOR_DISABLE_MULTIPLE_UPDATE	24	0x0	0=D1CURSOR registers can be updated multiple times in one V_UPDATE period 1=D1CURSOR registers can only be updated once in one V_UPDATE period

2.9.10 Primary Display Hardware Icon Registers

D1ICON_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6440			
Field Name	**Bits**	**Default**	**Description**
D1ICON_ENABLE	0	0x0	Primary display hardware icon enable. 0=Disable 1=Enable
D1ICON_2X_MAGNIFY	16	0x0	Primary display hardware icon 2x2 magnification. 0=No 2x2 magnification 1=2x2 magnification in horizontal and vertical direction
D1ICON_FORCE_MC_ON	20	0x0	When set, if the incoming data is in D1 icon region, DCP_LB_icon1_allow_stutter is set. This field in this double bufferred register is not double buffered.
Primary display hardware icon control.			

D1ICON_SURFACE_ADDRESS - RW - 32 bits -, GpuF0MMReg:0x6448			
Field Name	**Bits**	**Default**	**Description**
D1ICON_SURFACE_ADDRESS	31:0	0x0	Primary display hardware icon surface base address in byte. It is 4K byte aligned. Note: Bits [11:0] of this field are hardwired to 0.
Primary display hardware icon surface base address.			

D1ICON_SIZE - RW - 32 bits -, GpuF0MMReg:0x6450			
Field Name	**Bits**	**Default**	**Description**
D1ICON_HEIGHT	6:0	0x0	Primary display hardware icon height minus 1.
D1ICON_WIDTH	22:16	0x0	Primary display hardware icon width minus 1.
Primary display hardware icon size.			

D1ICON_START_POSITION - RW - 32 bits -, GpuF0MMReg:0x6454			
Field Name	**Bits**	**Default**	**Description**
D1ICON_Y_POSITION	12:0	0x0	Primary display hardware icon Y start coordinate related to the desktop coordinates. Note: The icon cannot be off the top and off the left edge of the display surface. But it can be off the bottom and off the right edge of the display.
D1ICON_X_POSITION	28:16	0x0	Primary display hardware icon X start coordinate relative to the desktop coordinates. Note: The icon cannot be off the top and off the left edge of the display surface. But it can be off the bottom and off the right edge of the display.
Primary display hardware icon position			

D1ICON_COLOR1 - RW - 32 bits -, GpuF0MMReg:0x6458			
Field Name	**Bits**	**Default**	**Description**
D1ICON_COLOR1_BLUE	7:0	0x0	Primary display hardware icon blue component of color 1.
D1ICON_COLOR1_GREEN	15:8	0x0	Primary display hardware icon green component of color 1.
D1ICON_COLOR1_RED	23:16	0x0	Primary display hardware icon red component of color 1.
Primary display hardware icon color 1.			

D1ICON_COLOR2 - RW - 32 bits -, GpuF0MMReg:0x645C			
Field Name	**Bits**	**Default**	**Description**
D1ICON_COLOR2_BLUE	7:0	0x0	Primary display hardware icon blue component of color 2.
D1ICON_COLOR2_GREEN	15:8	0x0	Primary display hardware icon green component of color 2.
D1ICON_COLOR2_RED	23:16	0x0	Primary display hardware icon red component of color 2.
Primary display hardware icon color 2.			

D1ICON_UPDATE - RW - 32 bits -, GpuF0MMReg:0x6460			
Field Name	**Bits**	**Default**	**Description**
D1ICON_UPDATE_PENDING (R)	0	0x0	Primary display hardware icon update Pending status. It is set to 1 after a host write to icon double buffer register. It is cleared after double buffering is done. The double buffering occurs when D1ICON_UPDATE_PENDING = 1 and D1ICON_UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC1 is disabled, the registers will be updated instantly. D1IOCN double buffer registers include : D1ICON_ENABLE D1ICON_2X_MAGNIFY D1ICON_SURFACE_ADDRESS D1ICON_HEIGHT D1ICON_WIDTH D1ICON_Y_POSITION D1ICON_X_POSITION 0=No update pending 1=Update pending
D1ICON_UPDATE_TAKEN (R)	1	0x0	Primary display hardware icon update Taken status. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0
D1ICON_UPDATE_LOCK	16	0x0	Primary display hardware icon update lock control. 0=Unlocked 1=Locked
D1ICON_DISABLE_MULTIPLE_UPDATE	24	0x0	0=D1ICON registers can be updated multiple times in one V_UPDATE period 1=D1ICON registers can only be updated once in one V_UPDATE period
Primary display hardware icon update control			

2.9.11 Primary Display Multi-VPU Control Registers

D1_MVP_AFR_FLIP_MODE - RW - 32 bits -, GpuF0MMReg:0x6514			
Field Name	**Bits**	**Default**	**Description**
D1_MVP_AFR_FLIP_MODE	1:0	0x0	10=Real flip 11=Dummy flip
S/W writes to this register in AFR mode for display 1 page flip			

D1_MVP_AFR_FLIP_FIFO_CNTL - RW - 32 bits -, GpuF0MMReg:0x6518			
Field Name	**Bits**	**Default**	**Description**
D1_MVP_AFR_FLIP_FIFO_NUM_ENTRIES (R)	3:0	0x0	Number of valid entries in the AFR flip FIFO
D1_MVP_AFR_FLIP_FIFO_RESET	4	0x0	Resets the AFR flip FIFO
D1_MVP_AFR_FLIP_FIFO_RESET_FLAG (R)	8	0x0	Sticky bit of the AFR flip fifo reset status
D1_MVP_AFR_FLIP_FIFO_RESET_ACK	12	0x0	Clears the DC_LB_MVP_AFR_FLIP_RESET_FLAG register bit
This register controls AFR Flip FIFO in display 1			

D1_MVP_FLIP_LINE_NUM_INSERT - RW - 32 bits -, GpuF0MMReg:0x651C			
Field Name	**Bits**	**Default**	**Description**
D1_MVP_FLIP_LINE_NUM_INSERT_MODE	1:0	0x2	00=No insertion: 0 is appended 01=Debug: insert D1_MVP_FLIP_LINE_NUM_INSERT register value; 10 - normal Hsync mode, insert the sum of LB line number + DC_LB_MVP_FLIP_LINE_NUM_OFFSET
D1_MVP_FLIP_LINE_NUM_INSERT	21:8	0x0	Used for debug purpose. This is what will be the line number carried to downstream GPUs if D1_MVP_FLIP_LINE_NUM_INSERT_EN is set
D1_MVP_FLIP_LINE_NUM_OFFSET	29:24	0x0	Used in normal HSYNC flipping operation. This is the number added to the current LB (desktop) line number for carrying to the downstream GPUs
D1_MVP_FLIP_AUTO_ENABLE	30	0x0	Enables automatic AFR/SFR flipping for display 1
This register controls line number insertion for the Hsync flipping mode in display 1			

D1CRTC_MVP_CONTROL1 - RW - 32 bits -, GpuF0MMReg:0x6038			
Field Name	**Bits**	**Default**	**Description**
MVP_EN	0	0x0	Enables MVP feature
MVP_MIXER_MODE	6:4	0x0	000=Split mode/super-tile mode 001=AFR manual (driver control) 010=AFR (switching) 011=AFR manual switch (set inband control character through register) 100=SuperAA with gamma and degamma enabled 101=SuperAA with only gamma enabled
MVP_MIXER_SLAVE_SEL	8	0x0	0=In AFR manual (drive control) mode, use master inputs in the next frame 1=Use the slave input

MVP_MIXER_SLAVE_SEL_DELAY_UNTIL_END_OF_BLANK	9	0x0	0=MVP_MIXER_SLAVE_SEL takes effect immediately 1=MVP_MIXER_SLAVE_SEL does not take effect until end of horizontal or vertical blank region
MVP_ARBITRATION_MODE_FOR_AFR_MANUAL_SWITCH_MODE	10	0x0	Arbitration scheme used when both master and slave GPU switch AFR flip queue status 0=Pixel source comes from the GPU which last make the switch 1=Pixel source changes to the GPU which is not currently displayed
MVP_RATE_CONTROL	12	0x0	0=DDR 1=SDR
MVP_CHANNEL_CONTROL	16	0x0	0=Single channel 1=Dual channel
MVP_GPU_CHAIN_LOCATION	21:20	0x0	The location of the GPU in a chain 00=Master GPU 01=Middle GPU 10=Head slave GPU (or slave GPU in dual-GPU system
MVP_DISABLE_MSB_EXPAND	24	0x0	How to expand each color component of pixel data from slave GPU from 8 to 10 bits 0=Dynamic expansion 1=Pad 0s
MVP_30BPP_EN	28	0x0	Enables 30bpp operation
MVP_TERMINATION_CNTL_A	30	0x0	Controls DVP termination resistors
MVP_TERMINATION_CNTL_B	31	0x0	Controls DVP termination resistors
MVP Control 1			

D1CRTC_MVP_CONTROL2 - RW - 32 bits -, GpuF0MMReg:0x603C			
Field Name	**Bits**	**Default**	**Description**
MVP_MUX_DE_DVOCNTL0_SEL	0	0x0	0=Selects DVOCNT2 1=Selects DVOCNT0
MVP_MUX_DE_DVOCNTL2_SEL	4	0x0	0=Selects DVOCNT2 1=Selects DVOCNT0
MVP_MUXA_CLK_SEL	8	0x0	0=Selects CLKA 1=Selects CLKB
MVP_MUXB_CLK_SEL	12	0x0	0=Selects CLKA 1=Selects CLKB
MVP_DVOCNTL_MUX	16	0x0	0=DVOCNTL[2:0] = DVO_DE, DVO_HSYNC, DVO_VSYNC 1=DVOCNTL[2:0] = DVO_DE, MVP_DVOCLK_C, DVO_DE
MVP_FLOW_CONTROL_OUT_EN	20	0x0	Enables flow_control_out
MVP_SWAP_LOCK_OUT_EN	24	0x0	0=Swap_lock_out is not enabled 1=Enable swap_lock out in GPIO
MVP_SWAP_AB_IN_DC_DDR	28	0x1	1=Swap in A & B data in dual channel DDR mode. This is the default
MVP Control 2			

D1CRTC_MVP_FIFO_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6040			
Field Name	**Bits**	**Default**	**Description**
MVP_STOP_SLAVE_WM	7:0	0x8	At the period after the start of DE from slave GPU, if MVP FIFO level exceeds this watermark, flow control is asserted
MVP_PAUSE_SLAVE_WM	15:8	0x8	In the middle of receiving a raster line from the slave GPU, if MVP FIFO level falls below this watermark, flow control signal is asserted for MVP_PAUSE_SLAVE_CNT cycles
MVP_PAUSE_SLAVE_CNT	23:16	0x4	In the middle of receiving a raster line from the slave GPU, if MVP FIFO level falls below this watermark, flow control signal is asserted for MVP_PAUSE_SLAVE_CNT cycles
MVP FIFO Control			

D1CRTC_MVP_FIFO_STATUS - RW - 32 bits -, GpuF0MMReg:0x6044			
Field Name	**Bits**	**Default**	**Description**
MVP_FIFO_LEVEL (R)	7:0	0x0	MVP FIFO level, in # of pixels
MVP_FIFO_OVERFLOW (R)	8	0x0	MVP FIFO overflows
MVP_FIFO_OVERFLOW_OCCURRED (R)	12	0x0	Sticky bit - MVP FIFO overflow has occurred
MVP_FIFO_OVERFLOW_ACK	16	0x0	Resets MVP_FIFO_OVERFLOW_OCCURRED
MVP_FIFO_UNDERFLOW (R)	20	0x0	MVP FIFO underflows
MVP_FIFO_UNDERFLOW_OCCURRED (R)	24	0x0	Sticky bit - MVP FIFO underflows occurred
MVP_FIFO_UNDERFLOW_ACK	28	0x0	Resets MVP_FIFO_UNDERFLOW_OCCURRED
MVP_FIFO_ERROR_MASK	30	0x0	Set to 1 to enable interrupt on mvp fifo overflow or underflow event
MVP_FIFO_ERROR_INT_STATUS (R)	31	0x0	Fifo error status flag (masked OR of fifo over/uderflow)
MVP FIFO Status			

D1CRTC_MVP_SLAVE_STATUS - RW - 32 bits -, GpuF0MMReg:0x6048			
Field Name	**Bits**	**Default**	**Description**
MVP_SLAVE_PIXELS_PER_LINE_RCVED (R)	12:0	0x0	The number of active pixels per line received from the slave GPU
MVP_SLAVE_LINES_PER_FRAME_RCVED (R)	28:16	0x0	The number of active lines per frame received from the slave GPU
MVP Slave Status			

D1CRTC_MVP_INBAND_CNTL_CAP - RW - 32 bits -, GpuF0MMReg:0x604C			
Field Name	**Bits**	**Default**	**Description**
MVP_IGNOR_INBAND_CNTL	0	0x1	Master GPU ignors the inband control signal
MVP_PASSING_INBAND_CNTL_EN	4	0x0	Slave GPU passes upstream slave GPU to downstream slave GPU/master GPU
MVP_INBAND_CNTL_CHAR_CAP (R)	31:8	0x0	Inband control signal received from slave GPU
MVP Capture Inband Control			

D1CRTC_MVP_INBAND_CNTL_INSERT - RW - 32 bits -, GpuF0MMReg:0x6050			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_MVP_INBAND_OUT_MODE	1:0	0x0	00=Disable inband insertion 01=Used for debug only: insert register MVP_INBAND_CNTL_CHAR_INSERT 10=Normal mode: insert the character generated by MVP_mixer
D1CRTC_MVP_INBAND_CNTL_CHAR_INSERT	31:8	0x0	Used for debug only: 24-bit control character for insertion
MVP Insert Inband Control			

D1CRTC_MVP_INBAND_CNTL_INSERT_TIMER - RW - 32 bits -, GpuF0MMReg:0x6054			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_MVP_INBAND_CNTL_CHAR_INSERT_TIMER	7:0	0x8	The number of clock cycles the character insertion trigger from the line buffer needs to be ahead of end of lines for CRTC to insert the in-band control character
MVP Insert Inband Control Timer			

D1CRTC_MVP_BLACK_KEYER - RW - 32 bits -, GpuF0MMReg:0x6058			
Field Name	**Bits**	**Default**	**Description**
MVP_BLACK_KEYER_R	9:0	0x0	Black keyer value, for red pixel
MVP_BLACK_KEYER_G	19:10	0x0	Black keyer value, for green pixel
MVP_BLACK_KEYER_B	29:20	0x0	Black keyer value, for blue pixel
MVP Black keyer for smoothing out pixels after black keyer in LB in SFR mode			

D1CRTC_MVP_STATUS - RW - 32 bits -, GpuF0MMReg:0x605C			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_FLIP_NOW_OCCURRED (R)	0	0x0	Reports whether flip_now has occurred. A sticky bit. 0=Has not occurred 1=Has occurred
D1CRTC_AFR_HSYNC_SWITCH_DONE_OCCURRED (R)	4	0x0	Reports whether afr_hsync_switch_done has occurred. A sticky bit. 0=Has not occurred 1=Has occurred
D1CRTC_FLIP_NOW_CLEAR (W)	16	0x0	Clears the sticky bit D1CRTC_FLIP_NOW_OCCURRED when written with '1'
D1CRTC_AFR_HSYNC_SWITCH_DONE_CLEAR (W)	20	0x0	Clears the sticky bit D1CRTC_AFR_HSYNC_SWITCH_DONE_OCCURRED when written with '1'
Reports status for MVP flipping in CRTC1			

D2CRTC_MVP_INBAND_CNTL_INSERT - RW - 32 bits -, GpuF0MMReg:0x6838			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_MVP_INBAND_OUT_MODE	1:0	0x0	00=Disable inband insertion 01=Used for debug only: insert register MVP_INBAND_CNTL_CHAR_INSERT 10=Normal mode: insert the character generated by MVP_mixer
D2CRTC_MVP_INBAND_CNTL_CHAR_INSERT	31:8	0x0	Used for debug only: 24-bit control character for insertion
MVP Insert Inband Control for CRTC2			

D2CRTC_MVP_INBAND_CNTL_INSERT_TIMER - RW - 32 bits -, GpuF0MMReg:0x683C			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_MVP_INBAND_CNTL_CHAR_INSERT_TIMER	7:0	0x8	The number of clock cycles the character insertion trigger from the line buffer needs to be ahead of end of lines for CRTC to insert the in-band control character
MVP Insert Inband Control Timer for CRTC2			

D1CRTC_MVP_CRC_CNTL - RW - 32 bits -, GpuF0MMReg:0x6840			
Field Name	**Bits**	**Default**	**Description**
MVP_CRC_BLUE_MASK	7:0	0xff	Mask bit for blue component
MVP_CRC_GREEN_MASK	15:8	0xff	Mask bit for green component
MVP_CRC_RED_MASK	23:16	0xff	Mask bit for red component
MVP_CRC_EN	28	0x0	0=CRC disabled 1=CRC enabled
CRC control register for MVP			

D1CRTC_MVP_CRC_RESULT - RW - 32 bits -, GpuF0MMReg:0x6844			
Field Name	**Bits**	**Default**	**Description**
MVP_CRC_BLUE_RESULT (R)	7:0	0x0	CRC result for each frame (DE region only) - Blue component
MVP_CRC_GREEN_RESULT (R)	15:8	0x0	CRC result for each frame (DE region only) - Green component
MVP_CRC_RED_RESULT (R)	23:16	0x0	CRC result for each frame (DE region only) - Red component
CRC result for each frame			

D1CRTC_MVP_CRC2_CNTL - RW - 32 bits -, GpuF0MMReg:0x6848			
Field Name	**Bits**	**Default**	**Description**
MVP_CRC2_BLUE_MASK	7:0	0xff	Mask bit for blue component
MVP_CRC2_GREEN_MASK	15:8	0xff	Mask bit for green component
MVP_CRC2_RED_MASK	23:16	0xff	Mask bit for red component
MVP_CRC2_EN	28	0x0	0=CRC2 disabled 1=CRC2 enabled
CRC2 control register for MVP			

D1CRTC_MVP_CRC2_RESULT - RW - 32 bits -, GpuF0MMReg:0x684C			
Field Name	**Bits**	**Default**	**Description**
MVP_CRC2_BLUE_RESULT (R)	7:0	0x0	CRC2 result for each frame (DE region only) - Blue component
MVP_CRC2_GREEN_RESULT (R)	15:8	0x0	CRC2 result for each frame (DE region only) - Green component
MVP_CRC2_RED_RESULT (R)	23:16	0x0	CRC2 result for each frame (DE region only) - Red component
CRC2 result for each frame			

D1CRTC_MVP_CONTROL3 - RW - 32 bits -, GpuF0MMReg:0x6850			
Field Name	**Bits**	**Default**	**Description**
MVP_RESET_IN_BETWEEN_FRAMES	0	0x1	1=Reset pointers, state machines of the MVP receiving logic between frames
MVP_DDR_SC_AB_SEL	4	0x0	0=Select bundle A in DDR single channel mode 1=Select bundle B
MVP_DDR_SC_B_START_MODE	8	0x0	0=Assuming the read & write clocks for meso-FIFO B is meso-chronous 1=Assuming they are synchronous
MVP_FLOW_CONTROL_OUT_FORCE_ONE	12	0x0	1=Force flow_control_out to 1
MVP_FLOW_CONTROL_OUT_FORCE_ZERO	16	0x0	1=Force flow_control_out to 0
MVP_FLOW_CONTROL_CASCADE_EN	20	0x0	1=Cascade flow control in multi-GPU
MVP_SWAP_48BIT_EN	24	0x0	1=Swap the least & most signficant 24 bits of the data as they read out of the FIFO
MVP_FLOW_CONTROL_IN_CAP (R)	28	0x0	Capture flow_control_in, used for diagnostics
MVP Control Register 3			

D1CRTC_MVP_RECEIVE_CNT_CNTL1 - RW - 32 bits -, GpuF0MMReg:0x6854			
Field Name	**Bits**	**Default**	**Description**
MVP_SLAVE_PIXEL_ERROR_CNT (R)	12:0	0x0	Count # of pixels in a line that is wrong, reset by active edge of hsync
MVP_SLAVE_LINE_ERROR_CNT (R)	28:16	0x0	Count # of lines in a frame that is wrong, reset by frame start
MVP_SLAVE_DATA_CHK_EN	31	0x1	Enable line & pixel counter, should be enabled a couple of frames after master is enabled
MVP Receive Counter Control 1			

D1CRTC_MVP_RECEIVE_CNT_CNTL2 - RW - 32 bits -, GpuF0MMReg:0x6858			
Field Name	**Bits**	**Default**	**Description**
MVP_SLAVE_FRAME_ERROR_CNT (R)	12:0	0x0	Count # of frames that is wrong
MVP_SLAVE_FRAME_ERROR_CNT_RESET	31	0x0	Reset MVP_SLAVE_FRAME_ERROR_CNT
MVP Receiver Counter Control 2			

2.9.12 Secondary Display Graphics Control Registers

D2GRPH_ENABLE - RW - 32 bits -, GpuF0MMReg:0x6900			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_ENABLE	0	0x1	Secondary graphic enabled. 0=Disable 1=Enable
Secondary graphic enabled.			

D2GRPH_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6904			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_DEPTH	1:0	0x0	Secondary graphic pixel depth. 0=8bpp 1=16bpp 2=32bpp 3=64bpp
D2GRPH_Z	5:4	0x0	Z[1:0] value for tiling
D2GRPH_FORMAT	10:8	0x0	Secondary graphic pixel format. It is used together with D1GRPH_DEPTH to define the graphic pixel format. If (D1GRPH_DEPTH = 0x0)(8 bpp) 0x0=Indexed Others=Reserved else if (D1GRPH_DEPTH = 0x1)(16 bpp) 0x0=ARGB 1555 0x1=RGB 565 0x2=ARGB 4444 0x3=Alpha index 88 0x4=Monochrome 16 0x5=BGRA 5551 Others - reserved else if (D1GRPH_DEPTH = 0x2)(32 bpp) 0x0=ARGB 8888 0x1=ARGB 2101010 0x2=32bpp digital output 0x3=8-bit ARGB 2101010 0x4=BGRA 1010102 0x5=8-bit BGRA 1010102 0x6=RGB 111110 0x7=BGR 101111 Others=Reserved else if (D1GRPH_DEPTH = 0x3)(64 bpp) 0x0=ARGB 16161616 0x1=64bpp digital output ARGB[13:2] 0x2=64bpp digital output RGB[15:0] 0x3=64bpp digital output ARGB[11:0] 0x4=64bpp digital output BGR[15:0] Others=Reserved
D2GRPH_TILE_COMPACT_EN	12	0x0	Enables multichip tile compaction 0=Disable 1=Enable
D2GRPH_ADDRESS_TRANSLATION_ENABLE	16	0x0	Enables display 2 address translation 0=0=Physical memory 1=1=Virtual memory
D2GRPH_PRIVILEGED_ACCESS_ENABLE	17	0x0	Enables display 2 privileged page access 0=0=No priveledged access 1=1=Priveledged access

D2GRPH_ARRAY_MODE	23:20	0x0	Defines the tiling mode 0=ARRAY_LINEAR_GENERAL: Unaligned linear array 1=ARRAY_LINEAR_ALIGNED: Aligned linear array 2=ARRAY_1D_TILED_THIN1: Uses 1D 8x8x1 tiles 3=ARRAY_1D_TILED_THICK: Uses 1D 8x8x4 tiles 4=ARRAY_2D_TILED_THIN1: Uses 8x8x1 macro-tiles 5=ARRAY_2D_TILED_THIN2: Macro-tiles are 2x high 6=ARRAY_2D_TILED_THIN4: Macro-tiles are 4x high 7=ARRAY_2D_TILED_THICK: Uses 8x8x4 macro-tiles 8=ARRAY_2B_TILED_THIN1: uses row bank swapping 9=ARRAY_2B_TILED_THIN2: uses row bank swapping 10=ARRAY_2B_TILED_THIN4: uses row bank swapping 11=ARRAY_2B_TILED_THICK: uses row bank swapping 12=ARRAY_3D_TILED_THIN1: Slices are pipe rotated 13=ARRAY_3D_TILED_THICK: Slices are pipe rotated 14=ARRAY_3B_TILED_THIN1: Slices are pipe rotated 15=ARRAY_3B_TILED_THICK: Slices are pipe rotated
D2GRPH_16BIT_ALPHA_MODE	25:24	0x0	This field is only used if 64 bpp graphics bit depth and graphics/overlay blend using per-pixel alpha from graphics channel. It is used for processing 16 bit alpha. The fixed point graphics alpha value in the frame buffer is always clamped to 0.0 - 1.0 data range. 0x0=Floating point alpha (1 sign bit, 5 bit exponent, 10 bit mantissa) 0x1=Fixed point alpha with normalization from 256/256 to 255/255 to represent 1.0 0x2=Fixed point alpha with no normalization 0x3=Fixed point alpha using lower 8 bits of frame buffer value, no normalization
D2GRPH_16BIT_FIXED_ALPHA_RANGE	30:28	0x0	This register field is only used if 64 bpp graphics bit depth and D2GRPH_16BIT_ALPHA_MODE = 01 or 10. Also only used if graphics/overlay blend using per-pixel alpha from graphics channel. Final alpha blend value is rounded to 8 bits after optional normalization step (see D2GRPH_16BIT_ALPHA_MODE). 0x0=Use bits [15:0] of input alpha value for blend alpha 0x1=Use bits [14:0] of input alpha value for blend alpha 0x2=Use bits [13:0] of input alpha value for blend alpha 0x3=Use bits [12:0] of input alpha value for blend alpha 0x4=Use bits [11:0] of input alpha value for blend alpha 0x5=Use bits [10:0] of input alpha value for blend alpha 0x6=Use bits [9:0] of input alpha value for blend alpha 0x7=Use bits [8:0] of input alpha value for blend alpha
Secondary graphic pixel depth and format.			

D2GRPH_LUT_SEL - RW - 32 bits -, GpuF0MMReg:0x6908			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_LUT_SEL	0	0x0	Secondary graphic LUT selection. 0=Select LUTA 1=Select LUTB
D2GRPH_LUT_10BIT_BYPASS_EN	8	0x0	Enables bypass secondary graphic LUT for 2101010 format 0=Use LUT 1=Bypass LUT when in 2101010 format. Ignored for other formats
D2GRPH_LUT_10BIT_BYPASS_DBL_BUF_EN	16	0x0	Enables double buffer D2GRPH_LUT_10BIT_BYPASS_EN 0=D1GRPH_LUT_10BIT_BYPASS_EN take effect right away 1=D1GRPH_LUT_10BIT_BYPASS_EN are double buffered
Secondary graphic LUT selection.			

D2GRPH_SWAP_CNTL - RW - 32 bits -, GpuF0MMReg:0x690C			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_ENDIAN_SWAP	1:0	0x0	MC endian swap select 0=0=None 1=1=8in16(0xaabb=>0xbbaa) 2=2=8in32(0xaabbccdd=>0xddccbbaa) 3=3=8in64(0xaabbccddeeff0011=>0x1100ffeeddccbbaa)
D2GRPH_RED_CROSSBAR	5:4	0x0	Red crossbar select 0=0=Select from R 1=1=Select from G 2=2=Select from B 3=3=Select from A
D2GRPH_GREEN_CROSSBAR	7:6	0x0	Green crossbar select 0=0=Select from G 1=1=Select from B 2=2=Select from A 3=3=Select from R
D2GRPH_BLUE_CROSSBAR	9:8	0x0	Blue crossbar select 0=0=Select from B 1=1=Select from A 2=2=Select from R 3=3=Select from G
D2GRPH_ALPHA_CROSSBAR	11:10	0x0	Alpha crossbar select 0=0=Select from A 1=1=Select from R 2=2=Select from G 3=3=Select from B
Endian swap and component reorder control			

D2GRPH_PRIMARY_SURFACE_ADDRESS - RW - 32 bits -, GpuF0MMReg:0x6910			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_PRIMARY_DFQ_ENABLE	0	0x0	Primary surface address DFQ enable 0=0=One deep queue mode 1=1=DFQ mode
D2GRPH_PRIMARY_SURFACE_ADDRESS	31:8	0x0	Secondary surface address for secondary graphics in byte. It is 256 byte aligned.
Secondary surface address for secondary graphics in byte.			

D2GRPH_SECONDARY_SURFACE_ADDRESS - RW - 32 bits -, GpuF0MMReg:0x6918			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_SECONDARY_DFQ_ENABLE *(mirror of D2GRPH_PRIMARY_SURFACE_ADDRESS:D2GRPH_PRIMARY_DFQ_ENABLE)*	0	0x0	Secondary surface address DFQ enable 0=0=One deep queue mode 1=1=DFQ mode
D2GRPH_SECONDARY_SURFACE_ADDRESS	31:8	0x0	Secondary surface address for secondary graphics in byte. It is 256 byte aligned.
Secondary surface address for secondary graphics in byte.			

D2GRPH_PITCH - RW - 32 bits -, GpuF0MMReg:0x6920			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_PITCH	13:0	0x0	Secondary graphic surface pitch in pixels. For Micro-tiled/Macro-tiled surface, it must be multiple of 64 pixeld in 8bpp mode. For Micro-linear/Macro-tiled surface, it must be multiple of 256 pixeld in 8bpp mode, multiple of 128 pixels in 16bpp mode and multiple of 64 pixels in 32bpp mode. For Micro-linear/Macro-linear surface, it must be multiple of 64 pixels in 8bpp mode. For other modes, it must be multiple of 32. Note: Bits [4:0] of this field are hardwired to 0.
Secondary graphic surface pitch in pixels.			

D2GRPH_SURFACE_OFFSET_X - RW - 32 bits -, GpuF0MMReg:0x6924			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_SURFACE_OFFSET_X	12:0	0x0	Secondary graphic X surface offset. It is 256 pixels aligned. Note: Bits [7:o] of this field are hardwired to 0.
Secondary graphic X surface offset.			

D2GRPH_SURFACE_OFFSET_Y - RW - 32 bits -, GpuF0MMReg:0x6928			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_SURFACE_OFFSET_Y	12:0	0x0	Secondary graphic Y surface offset. It must be even value Note: Bit [0] of this field is hardwired to 0.
Secondary graphic Y surface offset.			

D2GRPH_X_START - RW - 32 bits -, GpuF0MMReg:0x692C			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_X_START	12:0	0x0	Secondary graphic X start coordinate relative to the desktop coordinates.
Secondary graphic X start coordinate relative to the desktop coordinates.			

D2GRPH_Y_START - RW - 32 bits -, GpuF0MMReg:0x6930			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_Y_START	12:0	0x0	Secondary graphic Y start coordinate relative to the desktop coordinates.
Secondary graphic Y start coordinate relative to the desktop coordinates.			

D2GRPH_X_END - RW - 32 bits -, GpuF0MMReg:0x6934			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_X_END	13:0	0x0	Secondary graphic X end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K
Secondary graphic X end coordinate relative to the desktop coordinates.			

D2GRPH_Y_END - RW - 32 bits -, GpuF0MMReg:0x6938			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_Y_END	13:0	0x0	Secondary graphic Y end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K
Secondary graphic Y end coordinate relative to the desktop coordinates.			

D2GRPH_UPDATE - RW - 32 bits -, GpuF0MMReg:0x6944			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_MODE_UPDATE_PENDING (R)	0	0x0	Secondary graphic mode register update pending control. It is set to 1 after a host write to graphics mode register. It is cleared after double buffering is done. This signal is only visible through register. The graphics surface register includes: D2GRPH_DEPTH D2GRPH_FORMAT D2GRPH_SWAP_RB D2GRPH_LUT_SEL D2GRPH_LUT_10BIT_BYPASS_EN D2GRPH_ENABLE D2GRPH_X_START D2GRPH_Y_START D2GRPH_X_END D2GRPH_Y_END The mode register double buffering can only occur at vertical retrace. The double buffering occurs when D2GRPH_MODE_UPDATE_PENDING = 1 and D2GRPH_UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC2 is disabled, the registers will be updated instantly. 0=No update pending 1=Update pending
D2GRPH_MODE_UPDATE_TAKEN (R)	1	0x0	Secondary graphics update taken status for mode registers. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0.
D2GRPH_SURFACE_UPDATE_PENDING (R)	2	0x0	Secondary graphic surface register update pending control. If it is set to 1 after a host write to graphics surface register. It is cleared after double buffering is done. It is cleared after double buffering is done. This signal also goes to both the RBBM wait_until and to the CP_RTS_discrete inputs. The graphics surface register includes: D2GRPH_PRIMARY_SURFACE_ADDRESS D2GRPH_SECONDARY_SURFACE_ADDRESS D2GRPH_PITCH D2GRPH_SURFACE_OFFSET_X D2GRPH_SURFACE_OFFSET_Y. If D2GRPH_SURFACE_UPDATE_H_RETRACE_EN = 0, the double buffering occurs in vertical retrace when D2GRPH_SURFACE_UPDATE_PENDING = 1 and D2GRPH_UPDATE_LOCK = 0 and V_UPDATE = 1. Otherwise the double buffering happens at horizontal retrace when D2GRPH_SURFACE_UPDATE_PENDING = 1 and D2GRPH_UPDATE_LOCK = 0 and Data request for last chunk of the line is sent from DCP to DMIF. If CRTC2 is disabled, the registers will be updated instantly.

D2GRPH_SURFACE_UPDATE_TAKEN (R)	3	0x0	Secondary graphics update taken status for surface registers. If D2GRPH_SURFACE_UPDATE_H_RETRACE_EN = 0, it is set to 1 when double buffering occurs and cleared when V_UPDATE = 0. Otherwise, it is active for one clock cycle when double buffering occurs at the horizontal retrace.
D2GRPH_UPDATE_LOCK	16	0x0	Secondary graphic register update lock control. This lock bit control both surface and mode register double buffer 0=Unlocked 1=Locked
D2GRPH_MODE_DISABLE_MULTIPLE_UPDATE	24	0x0	0=D2GRPH mode registers can be updated multiple times in one V_UPDATE period 1=D2GRPH mode registers can only be updated once in one V_UPDATE period
D2GRPH_SURFACE_DISABLE_MULTIPLE_UPDATE	28	0x0	0=D2GRPH surface registers can be updated multiple times in one V_UPDATE period 1=D2GRPH surface registers can only be updated once in one V_UPDATE period
Secondary graphic update control			

D2GRPH_FLIP_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6948			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_SURFACE_UPDATE_H_RETRACE_EN	0	0x0	Enable secondary graphic surface register double buffer in horizontal retrace. 0=Vertical retrace flipping 1=Horizontal retrace flipping
Enable secondary graphic surface register double buffer in horizontal retrace			

D2GRPH_SURFACE_ADDRESS_INUSE - RW - 32 bits -, GpuF0MMReg:0x694C			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_SURFACE_ADDRESS_INUSE (R)	31:8	0x0	This register reads back snapshot of secondary graphics surface address used for data request. The address is the signal sent to DMIF and is updated on SOF or horizontal surface update. The snapshot is triggered by writing 1 into field D1CRTC_SNAPSHOT_MANUAL_TRIGGER of CRTC register D1CRTC_SNAPSHOT_STATUS.
Snapshot of secondary graphics surface address in use			

2.9.13 Secondary Display Video Overlay Control Registers

D2OVL_ENABLE - RW - 32 bits - [GpuF0MMReg:0x6980]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_ENABLE	0	0x0	Secondary overlay enabled. 0=Disable 1=Enable
Secondary overlay enabled.			

D2OVL_CONTROL1 - RW - 32 bits - [GpuF0MMReg:0x6984]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_DEPTH	1:0	0x0	Secondary overlay pixel depth 0=Reserved 1=16bpp 2=32bpp 3=reserved
D2OVL_Z	5:4	0x0	Z[1:0] value for tiling
D2OVL_FORMAT	10:8	0x0	Secondary overlay pixel format. It is used together with D1OVL_DEPTH to define the overlay format. If (D1OVL_DEPTH = 0x1)(16 bpp) 0x0=ARGB 1555 0x1=RGB 565 0x2=BGRA 5551 Others=Reserved else if (D1OVL_DEPTH = 0x2)(32 bpp) 0x0=ACrYCb 8888 or ARGB 8888 0x1=ACrYCb 2101010 or ARGB 2101010 0x2=CbACrA or BGRA 1010102 Others=Reserved
D2OVL_TILE_COMPACT_EN	12	0x0	Enables multichip tile compaction 0=Enables multichip tile compaction
D2OVL_ADDRESS_TRANSLATION_ENABLE	16	0x0	Enables Overlay 2 address translation 0=0=Physical memory 1=1=Virtual memory
D2OVL_PRIVILEGED_ACCESS_ENABLE	17	0x0	Enables overlay 2 privileged page access 0=0=No privileged access 1=1=Privileged access
D2OVL_ARRAY_MODE	23:20	0x0	Defines the tiling mode 0=ARRAY_LINEAR_GENERAL: Unaligned linear array 1=ARRAY_LINEAR_ALIGNED: Aligned linear array 2=ARRAY_1D_TILED_THIN1: Uses 1D 8x8x1 tiles 3=ARRAY_1D_TILED_THICK: Uses 1D 8x8x4 tiles 4=ARRAY_2D_TILED_THIN1: Uses 8x8x1 macro-tiles 5=ARRAY_2D_TILED_THIN2: Macro-tiles are 2x high 6=ARRAY_2D_TILED_THIN4: Macro-tiles are 4x high 7=ARRAY_2D_TILED_THICK: Uses 8x8x4 macro-tiles 8=ARRAY_2B_TILED_THIN1: uses row bank swapping 9=ARRAY_2B_TILED_THIN2: uses row bank swapping 10=ARRAY_2B_TILED_THIN4: uses row bank swapping 11=ARRAY_2B_TILED_THICK: uses row bank swapping 12=ARRAY_3D_TILED_THIN1: Slices are pipe rotated 13=ARRAY_3D_TILED_THICK: Slices are pipe rotated 14=ARRAY_3B_TILED_THIN1: Slices are pipe rotated 15=ARRAY_3B_TILED_THICK: Slices are pipe rotated
D2OVL_COLOR_EXPANSION_MODE	24	0x0	Secondary overlay pixel format expansion mode. 0=Dynamic expansion for RGB 1=Zero expansion for YCbCr
Secondary overlay pixel depth and format.			

D2OVL_CONTROL2 - RW - 32 bits - [GpuF0MMReg:0x6988]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_HALF_RESOLUTION_ENABLE	0	0x0	Secondary overlay half resolution control 0=Disable 1=Enable
Secondary overlay half resolution control			

D2OVL_SWAP_CNTL - RW - 32 bits - [GpuF0MMReg:0x698C]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_ENDIAN_SWAP	1:0	0x0	MC endian swap select 0=0=None 1=1=8in16(0xaabb=>0xbbaa) 2=2=8in32(0xaabbccdd=>0xddccbbaa) 3=3=8in64(0xaabbccddeeff0011=>0x1100ffeeddccbbaa)
D2OVL_RED_CROSSBAR	5:4	0x0	Red Crossbar select 0=0=Select from R 1=1=Select from G 2=2=Select from B 3=3=Select from A
D2OVL_GREEN_CROSSBAR	7:6	0x0	Green Crossbar select 0=0=Select from G 1=1=Select from B 2=2=Select from A 3=3=Select from R
D2OVL_BLUE_CROSSBAR	9:8	0x0	Blue Crossbar select 0=0=Select from B 1=1=Select from A 2=2=Select from R 3=3=Select from G
D2OVL_ALPHA_CROSSBAR	11:10	0x0	Alpha Crossbar select 0=0=Select from A 1=1=Select from R 2=2=Select from G 3=3=Select from B
Endian swap and component reorder control			

D2OVL_SURFACE_ADDRESS - RW - 32 bits - [GpuF0MMReg:0x6990]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_DFQ_ENABLE	0	0x0	Secondary overlay surface address DFQ enable
D2OVL_SURFACE_ADDRESS	31:8	0x0	Secondary overlay surface base address in byte. It is 256 bytes aligned.
Secondary overlay surface base address in byte.			

D2OVL_PITCH - RW - 32 bits - [GpuF0MMReg:0x6998]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PITCH	13:0	0x0	Secondary overlay surface pitch in pixels. For Micro-tiled/Macro-tiled surface, it must be multiple of 64 pixeld in 8bpp mode. For Micro-linear/Macro-tiled surface, it must be multiple of 256 pixeld in 8bpp mode, multiple of 128 pixels in 16bpp mode and multiple of 64 pixels in 32bpp mode. For Micro-linear/Macro-linear surface, it must be multiple of 64 pixels in 8bpp mode. For other modes, it must be multiple of 32. Note: Bits [4:0] of this field are hardwired to 0.
Secondary overlay surface pitch in pixels.			

D2OVL_SURFACE_OFFSET_X - RW - 32 bits - [GpuF0MMReg:0x699C]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_SURFACE_OFFSET_X	12:0	0x0	Secondary overlay X surface offset. It is 256 pixels aligned. Note: Bits [7:0] of this field are hardwired to 0.
Secondary overlay X surface offset.			

D2OVL_SURFACE_OFFSET_Y - RW - 32 bits - [GpuF0MMReg:0x69A0]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_SURFACE_OFFSET_Y	12:0	0x0	Secondary overlay Y surface offset. It is even value. Note: Bit [0] of this field is hardwired to 0.
Secondary overlay Y surface offset.			

D2OVL_START - RW - 32 bits - [GpuF0MMReg:0x69A4]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_Y_START	12:0	0x0	Secondary overlay Y start coordinate relative to the desktop coordinates.
D2OVL_X_START	28:16	0x0	Secondary overlay X start coordinate relative to the desktop coordinates.
Secondary overlay X, Y start coordinate relative to the desktop coordinates.			

D2OVL_END - RW - 32 bits - [GpuF0MMReg:0x69A8]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_Y_END	13:0	0x0	Secondary overlay Y end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K
D2OVL_X_END	29:16	0x0	Secondary overlay X end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K
Secondary overlay X, Y end coordinate relative to the desktop coordinates.			

D2OVL_UPDATE - RW - 32 bits - [GpuF0MMReg:0x69AC]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_UPDATE_PENDING (R)	0	0x0	Secondary overlay register update pending control. It is set to 1 after a host write to overlay double buffer register. It is cleared after double buffering is done. The double buffering occurs when UPDATE_PENDING = 1 and UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC2 is disabled, the registers will be updated instantly. D2OVL double buffer registers include: D2OVL_ENABLE D2OVL_DEPTH D2OVL_FORMAT D2OVL_SWAP_RB D2OVL_COLOR_EXPANSION_MODE D2OVL_HALF_RESOLUTION_ENABLE D2OVL_SURFACE_ADDRESS D2OVL_PITCH D2OVL_SURFACE_OFFSET_X D2OVL_SURFACE_OFFSET_Y D2OVL_START D2OVL_END 0=No update pending 1=Update pending
D2OVL_UPDATE_TAKEN (R)	1	0x0	Secondary overlay update taken status. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0.
D2OVL_UPDATE_LOCK	16	0x0	Secondary overlay register update lock control. 0=Unlocked 1=Locked
D2OVL_DISABLE_MULTIPLE_UPDATE	24	0x0	0=D2OVL registers can be updated multiple times in one V_UPDATE period 1=D2OVL registers can only be updated once in one V_UPDATE period
Secondary overlay register update			

D2OVL_SURFACE_ADDRESS_INUSE - RW - 32 bits - [GpuF0MMReg:0x69B0]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_SURFACE_ADDRESS_INUSE (R)	31:8	0x0	This register reads back snapshot of secondary overlay surface address used for data request. The address is the signal sent to DMIF and is updated on SOF or horizontal surface update. The snapshot is triggered by writing 1 into field D1CRTC_SNAPSHOT_MANUAL_TRIGGER of CRTC register D1CRTC_SNAPSHOT_STATUS.
Snapshot of secondary overlay surface address in use			

D2OVL_DFQ_CONTROL - RW - 32 bits - [GpuF0MMReg:0x69B4]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_DFQ_RESET	0	0x0	Reset the deep flip queue
D2OVL_DFQ_SIZE	6:4	0x0	Size of the deep flip queue 0=1 deep queue 1=2 deep queue ... 7=8 deep queue
D2OVL_DFQ_MIN_FREE_ENTRIES	10:8	0x0	Minimum # of free entries before surface pending is asserted
Control of the deep flip queue for D2 overlay			

D2OVL_DFQ_STATUS - RW - 32 bits - [GpuF0MMReg:0x69B8]			
Field Name	**Bits**	**Default**	**Description**
D2OVL_DFQ_NUM_ENTRIES (R)	3:0	0x0	# of entries in deep flip queue 0=1 entry 1=2 entries ... 7=8 entries
D2OVL_DFQ_RESET_FLAG (R)	8	0x0	Sticky bit: Deep flip queue in reset
D2OVL_DFQ_RESET_ACK (W)	9	0x0	Clear D2OVL_DFQ_RESET_FLAG
Status of the deep flip queue for D2 overlay			

2.9.14 Secondary Display Video Overlay Transform Registers

D2OVL_MATRIX_TRANSFORM_EN - RW - 32 bits -, GpuF0MMReg:0x6A00			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_TRANSFORM_EN	0	0x0	Secondary overlay matrix conversion enable 0=Disable 1=Enable
Secondary overlay matrix conversion enable.			

D2OVL_MATRIX_COEF_1_1 - RW - 32 bits -, GpuF0MMReg:0x6A04			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_1_1	18:0	0x198a0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D2OVL_MATRIX_SIGN_1_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_1_2 - RW - 32 bits -, GpuF0MMReg:0x6A08			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_1_2	18:0	0x12a20	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D2OVL_MATRIX_SIGN_1_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_1_3 - RW - 32 bits -, GpuF0MMReg:0x6A0C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_1_3	18:0	0x0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D2OVL_MATRIX_SIGN_1_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_1_4 - RW - 32 bits -, GpuF0MMReg:0x6A10			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_1_4	26:8	0x48700	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S11.1. Note: Bits [6:0] of this field are hardwired to 0.
D2OVL_MATRIX_SIGN_1_4	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_2_1 - RW - 32 bits -, GpuF0MMReg:0x6A14			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_2_1	18:0	0x72fe0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D2OVL_MATRIX_SIGN_2_1	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_2_2 - RW - 32 bits -, GpuF0MMReg:0x6A18			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_2_2	18:0	0x12a20	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D2OVL_MATRIX_SIGN_2_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_2_3 - RW - 32 bits -, GpuF0MMReg:0x6A1C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_2_3	18:0	0x79bc0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D2OVL_MATRIX_SIGN_2_3	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_2_4 - RW - 32 bits -, GpuF0MMReg:0x6A20			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_2_4	26:8	0x22100	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S11.1. Note: Bits [6:0] of this field are hardwired to 0.
D2OVL_MATRIX_SIGN_2_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_3_1 - RW - 32 bits -, GpuF0MMReg:0x6A24			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_3_1	18:0	0x0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D2OVL_MATRIX_SIGN_3_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_3_2 - RW - 32 bits -, GpuF0MMReg:0x6A28			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_3_2	18:0	0x12a20	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D2OVL_MATRIX_SIGN_3_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_3_3 - RW - 32 bits -, GpuF0MMReg:0x6A2C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_3_3	18:0	0x20460	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. Note: Bits [4:0] of this field are hardwired to 0.
D2OVL_MATRIX_SIGN_3_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_3_4 - RW - 32 bits -, GpuF0MMReg:0x6A30			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_3_4	26:8	0x3af80	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S11.1. Note: Bits [6:0] of this field are hardwired to 0.
D2OVL_MATRIX_SIGN_3_4	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL - RW - 32 bits -, GpuF0MMReg:0x6940			
Field Name	**Bits**	**Default**	**Description**
D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	2:0	0x0	Matrix transformation control for secondary display overlay pixels. It is used when PIX_TYPE is 0.
Matrix transformation control for secondary display overlay pixels.			

2.9.15 Secondary Display Video Overlay Gamma Correction Registers

D2OVL_PWL_TRANSFORM_EN - RW - 32 bits -, GpuF0MMReg:0x6A80			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_TRANSFORM_EN	0	0x0	Secondary overlay gamma correction enable. 0=Disable 1=Enable
Secondary overlay gamma correction enable.			

D2OVL_PWL_0TOF - RW - 32 bits -, GpuF0MMReg:0x6A84			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_0TOF_OFFSET	8:0	0x0	Secondary overlay gamma correction non-linear offset for input 0x0-0xF. Format fix-point 8.1 (0.0 to +255.5).
D2OVL_PWL_0TOF_SLOPE	26:16	0x100	Secondary overlay gamma correction non-linear slope for input 0x0-0xF. Format fix-point 3.8 (0.00 to +7.99).
Secondary overlay gamma correction non-linear offset and slope for input 0x0-0xF			

D2OVL_PWL_10TO1F - RW - 32 bits -, GpuF0MMReg:0x6A88			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_10TO1F_OFFSET	8:0	0x20	Secondary overlay gamma correction non-linear offset for input 0x10-0x1F. Format fix-point 8.1 (0.0 to +255.5).
D2OVL_PWL_10TO1F_SLOPE	26:16	0x100	Secondary overlay gamma correction non-linear slope for input 0x10-0x1F. Format fix-point 3.8 (0.00 to +7.99).
Secondary overlay gamma correction non-linear offset and slope for input 0x10-0x1F			

D2OVL_PWL_20TO3F - RW - 32 bits -, GpuF0MMReg:0x6A8C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_20TO3F_OFFSET	9:0	0x40	Secondary overlay gamma correction non-linear offset for input 0x20-0x3F. Format fix-point 9.1 (0.0 to +511.5).
D2OVL_PWL_20TO3F_SLOPE	25:16	0x100	Secondary overlay gamma correction non-linear slope for input 0x20-0x3F. Format fix-point 2.8 (0.00 to +3.99).
Secondary overlay gamma correction non-linear offset and slope for input 0x20-0x3F			

D2OVL_PWL_40TO7F - RW - 32 bits -, GpuF0MMReg:0x6A90			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_40TO7F_OFFSET	9:0	0x80	Secondary overlay gamma correction non-linear offset for input 40-7F. Format fix-point 9.1 (0.0 to +511.5).
D2OVL_PWL_40TO7F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 40-7F. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 40-7F.			

D2OVL_PWL_80TOBF - RW - 32 bits -, GpuF0MMReg:0x6A94			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_80TOBF_OFFSET	10:0	0x100	Secondary overlay gamma correction non-linear offset for input 80-BF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_80TOBF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 80-BF. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 80-BF.			

D2OVL_PWL_C0TOFF - RW - 32 bits -, GpuF0MMReg:0x6A98			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_C0TOFF_OFFSET	10:0	0x180	Secondary overlay gamma correction non-linear offset for input C0-FF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_C0TOFF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input C0-FF. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input C0-FF.			

D2OVL_PWL_100TO13F - RW - 32 bits -, GpuF0MMReg:0x6A9C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_100TO13F_OFFSET	10:0	0x200	Secondary overlay gamma correction non-linear offset for input 100-13F. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_100TO13F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 100-13F. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 100-13F.			

D2OVL_PWL_140TO17F - RW - 32 bits -, GpuF0MMReg:0x6AA0			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_140TO17F_OFFSET	10:0	0x280	Secondary overlay gamma correction non-linear offset for input 140-17F. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_140TO17F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 140-17F. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 140-17F.			

D2OVL_PWL_180TO1BF - RW - 32 bits -, GpuF0MMReg:0x6AA4			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_180TO1BF_OFFSET	10:0	0x300	Secondary overlay gamma correction non-linear offset for input 180-1BF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_180TO1BF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 180-1BF. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 180-1BF.			

D2OVL_PWL_1C0TO1FF - RW - 32 bits -, GpuF0MMReg:0x6AA8			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_1C0TO1FF_OFFSET	10:0	0x380	Secondary overlay gamma correction non-linear offset for input 1C0-1FF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_1C0TO1FF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 1C0-1FF. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 1C0-1FF.			

D2OVL_PWL_200TO23F - RW - 32 bits -, GpuF0MMReg:0x6AAC			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_200TO23F_OFFSET	10:0	0x400	Secondary overlay gamma correction non-linear offset for input 200-23F. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_200TO23F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 200-23F. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 200-23F.			

D2OVL_PWL_240TO27F - RW - 32 bits -, GpuF0MMReg:0x6AB0			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_240TO27F_OFFSET	10:0	0x480	Secondary overlay gamma correction non-linear offset for input 240-27F. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_240TO27F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 240-27F. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 240-27F.			

D2OVL_PWL_280TO2BF - RW - 32 bits -, GpuF0MMReg:0x6AB4			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_280TO2BF_OFFSET	10:0	0x500	Secondary overlay gamma correction non-linear offset for input 280-2BF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_280TO2BF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 280-2BF. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 280-2BF.			

D2OVL_PWL_2C0TO2FF - RW - 32 bits -, GpuF0MMReg:0x6AB8			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_2C0TO2FF_OFFSET	10:0	0x580	Secondary overlay gamma correction non-linear offset for input 2C0-2FF. Format fix-point 10.1(0.0 to +1023.5).
D2OVL_PWL_2C0TO2FF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 2C0-2FF. Format fix-point 1.8(0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 2C0-2FF.			

D2OVL_PWL_300TO33F - RW - 32 bits -, GpuF0MMReg:0x6ABC			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_300TO33F_OFFSET	10:0	0x600	Secondary overlay gamma correction non-linear offset for input 300-33F. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_300TO33F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 300-33F. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 300-33F.			

D2OVL_PWL_340TO37F - RW - 32 bits -, GpuF0MMReg:0x6AC0			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_340TO37F_OFFSET	10:0	0x680	Secondary overlay gamma correction non-linear offset for input 340-37F. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_340TO37F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 340-37F. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 340-37F.			

D2OVL_PWL_380TO3BF - RW - 32 bits -, GpuF0MMReg:0x6AC4			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_380TO3BF_OFFSET	10:0	0x700	Secondary overlay gamma correction non-linear offset for input 380-3BF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_380TO3BF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 380-3BF. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 380-3BF.			

D2OVL_PWL_3C0TO3FF - RW - 32 bits -, GpuF0MMReg:0x6AC8			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_3C0TO3FF_OFFSET	10:0	0x780	Secondary overlay gamma correction non-linear offset for input 3C0-3FF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_3C0TO3FF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 3C0-3FF. Format fix-point 1.8 (0.00 to +1.99).
Secondary overlay gamma correction non-linear offset and slope for input 3C0-3FF.			

D2OVL_KEY_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6B00			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_KEY_FUNCTION	1:0	0x0	Selects graphic keyer result equation for secondary display. 0=GRPH2_KEY = FALSE = 0 1=GRPH2_KEY = TRUE = 1 2=GPPH2_KEY = (GRPH2_RED in range) AND (GRPH2_GREEN in range) AND (GRPH2_BLUE in range) AND (GRPH2_ALPHA in range) 3=GRPH2_KEY = not [(GRPH2_RED in range) AND (GRPH2_GREEN in range) AND (GRPH2_BLUE in range) AND (GRPH2_ALPHA in range)]
D2OVL_KEY_FUNCTION	9:8	0x0	Selects overlay keyer result equation for secondary display. 0=OVL2_KEY = FALSE = 0 1=OVL2_KEY = TRUE = 1 2=OVL2_KEY = (OVL2_Cr_RED in range) AND (OVL2_Y_GREEN in range) AND (OVL2_Cb_BLUE in range) AND (OVL2_ALPHA in range) 3=OVL2_KEY = not [(OVL2_Cr_RED in range) AND (OVL2_Y_GREEN in range) AND (OVL2_Cb_BLUE in range) AND (OVL2_ALPHA in range)]
D2OVL_KEY_COMPARE_MIX	16	0x0	Selects final mix of graphics and overlay keys for secondary display. 0=GRPH_OVL_KEY = GRPH_KEY or OVL_KEY 1=GRPH_OVL_KEY = GRPH_KEY and OVL_KEY
Secondary display key control			

2.9.16 Secondary Display Graphics and Overlay Blending Registers

D2GRPH_ALPHA - RW - 32 bits -, GpuF0MMReg:0x6B04			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_ALPHA	7:0	0xff	Global graphic alpha for use in key mode and global alpha modes. See D2OVL_ALPHA_MODE register filed for more details
Global graphic alpha for use in key mode and global alpha modes.			

D2OVL_ALPHA - RW - 32 bits -, GpuF0MMReg:0x6B08			
Field Name	**Bits**	**Default**	**Description**
D2OVL_ALPHA	7:0	0xff	Global overlay alpha for use in key mode and global alpha modes. See D2OVL_ALPHA_MODE register filed for more details
Global overlay alpha for use in key mode and global alpha modes.			

D2OVL_ALPHA_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6B0C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_ALPHA_MODE	1:0	0x0	Graphics/overlay alpha blending mode for secondary controller. In any case, if there is only graphics, the input OVL_DATA is forced to blank. If there is only overlay, the input GRPH_DATA is forced to blank. 0=Keyer mode, select graphic or overlay keyer to mix graphics and overlay 1=Per pixel graphic alpha mode.Alpha blend graphic and overlay layer. The alpha from graphic pixel may be inverted according to register field 2=Global alpha mode 3=Per pixel overlay alpha mode
D2OVL_ALPHA_PREMULT	8	0x0	For use with per pixel alpha blend mode. Selects whether pre-multiplied alpha or non-multiplied alpha. 0=0x0 - When DxOVL_ALPHA_MODE = 0x1, then Pixel = PIX_ALPHA * graphics pixel + (1-PIX_ALPHA) * overlay pixel.When DxOVL_ALPHA_MODE = 0x3, then Pixel = PIX_ALPHA * overlay pixel + (1-PIX_ALPHA) * graphic pixel 1=0x1 - When DxOVL_ALPHA_MODE = 0x1, then Pixel = graphic pixel + (1-PIX_ALPHA) * overlay pixel.When DxOVL_ALPHA_MODE = 0x3, then Pixel = overlay pixel + (1-PIX_ALPHA) * graphic pixel
D2OVL_ALPHA_INV	16	0x0	For use with pixel blend mode. Apply optional inversion to the alpha value extracted form the graphics or overlay surface data. 0=PIX_ALPHA = alpha from graphics or overlay 1=PIX_ALPHA = 1 - alpha from graphics or overlay
Secondary display graphics/overlay alpha blending control			

D2GRPH_KEY_RANGE_RED - RW - 32 bits -, GpuF0MMReg:0x6B10			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_KEY_RED_LOW	15:0	0x0	Secondary graphics keyer red component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D2GRPH_KEY_RED_HIGH	31:16	0x0	Secondary graphics keyer red component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
Secondary graphics keyer red component range			

D2GRPH_KEY_RANGE_GREEN - RW - 32 bits -, GpuF0MMReg:0x6B14			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_KEY_GREEN_LOW	15:0	0x0	Secondary graphics keyer green component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D2GRPH_KEY_GREEN_HIGH	31:16	0x0	Secondary graphics keyer green component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
Secondary graphics keyer green component range			

D2GRPH_KEY_RANGE_BLUE - RW - 32 bits -, GpuF0MMReg:0x6B18			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_KEY_BLUE_LOW	15:0	0x0	Secondary graphics keyer blue component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D2GRPH_KEY_BLUE_HIGH	31:16	0x0	Secondary graphics keyer blue component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
Secondary graphics keyer blue component range			

D2GRPH_KEY_RANGE_ALPHA - RW - 32 bits -, GpuF0MMReg:0x6B1C			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_KEY_ALPHA_LOW	15:0	0x0	Secondary graphics keyer alpha component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D2GRPH_KEY_ALPHA_HIGH	31:16	0x0	Secondary graphics keyer alpha component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
Secondary graphics keyer alpha component range			

D2OVL_KEY_RANGE_RED_CR - RW - 32 bits -, GpuF0MMReg:0x6B20			
Field Name	**Bits**	**Default**	**Description**
D2OVL_KEY_RED_CR_LOW	9:0	0x0	Secondary overlay keyer red component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D2OVL_KEY_RED_CR_HIGH	25:16	0x0	Secondary overlay keyer red component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
Secondary overlay keyer red component range			

D2OVL_KEY_RANGE_GREEN_Y - RW - 32 bits -, GpuF0MMReg:0x6B24			
Field Name	**Bits**	**Default**	**Description**
D2OVL_KEY_GREEN_Y_LOW	9:0	0x0	Secondary overlay keyer green component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D2OVL_KEY_GREEN_Y_HIGH	25:16	0x0	Secondary overlay keyer green component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
Secondary overlay keyer green component range			

D2OVL_KEY_RANGE_BLUE_CB - RW - 32 bits -, GpuF0MMReg:0x6B28			
Field Name	**Bits**	**Default**	**Description**
D2OVL_KEY_BLUE_CB_LOW	9:0	0x0	Secondary overlay keyer blue component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D2OVL_KEY_BLUE_CB_HIGH	25:16	0x0	Secondary overlay keyer blue component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
Secondary overlay keyer blue component range			

D2OVL_KEY_ALPHA - RW - 32 bits -, GpuF0MMReg:0x6B2C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_KEY_ALPHA_LOW	7:0	0x0	Secondary overlay keyer alpha component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D2OVL_KEY_ALPHA_HIGH	23:16	0x0	Secondary overlay keyer alpha component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
Secondary overlay keyer alpha component range			

2.9.17 Secondary Display Color Matrix Transform Registers

D2GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL - RW - 32 bits -, GpuF0MMReg:0x6B80			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_COLOR_MATRIX_TRANSFORMATION_EN	0	0x0	Matrix transformation control for secondary display graphics and cursor pixel. It is used when PIX_TYPE is 1. 0=Disable 1=Enable
Matrix transformation control for secondary display graphics and cursor pixel.			

D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL - RW - 32 bits -, GpuF0MMReg:0x6940			
Field Name	**Bits**	**Default**	**Description**
D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	2:0	0x0	Matrix transformation control for secondary display overlay pixels. It is used when PIX_TYPE is 0.
Matrix transformation control for secondary display overlay pixels.			

D2COLOR_MATRIX_COEF_1_1 - RW - 32 bits -, GpuF0MMReg:0x6B84			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_1_1	16:0	0x0	Combined matrix constant C11 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S1.11(-2.00 to +1.99). Note: Bits [4:0] of this field are hardwired to 0.
D2COLOR_MATRIX_SIGN_1_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C11 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_1_2 - RW - 32 bits -, GpuF0MMReg:0x6B88			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_1_2	15:0	0x0	Combined matrix constant C12 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S0.11(-1.00 to + 0.99). Note: Bits [4:0] of this field are hardwired to 0.
D2COLOR_MATRIX_SIGN_1_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C12 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_1_3 - RW - 32 bits -, GpuF0MMReg:0x6B8C			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_1_3	15:0	0x0	Combined matrix constant C13 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S0.11(-1.0 to +0.99). Note: Bits [4:0] of this field are hardwired to 0.
D2COLOR_MATRIX_SIGN_1_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C13 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_1_4 - RW - 32 bits -, GpuF0MMReg:0x6B90			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_1_4	26:8	0x0	Combined matrix constant C14 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S11.1(-2048.5 to +2047.5). It includes subtraction of 512 offset Note: Bits [6:0] of this field are hardwired to 0.
D2COLOR_MATRIX_SIGN_1_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C14 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_2_1 - RW - 32 bits -, GpuF0MMReg:0x6B94			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_2_1	15:0	0x0	Combined matrix constant C21 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S0.11(-1.00 to +0.99). Note: Bits [4:0] of this field are hardwired to 0.
D2COLOR_MATRIX_SIGN_2_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C21 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_2_2 - RW - 32 bits -, GpuF0MMReg:0x6B98			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_2_2	16:0	0x0	Combined matrix constant C22 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S1.11(-2.00 to +1.99). Note: Bits [4:0] of this field are hardwired to 0.
D2COLOR_MATRIX_SIGN_2_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C22 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_2_3 - RW - 32 bits -, GpuF0MMReg:0x6B9C			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_2_3	15:0	0x0	Combined matrix constant C23 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S0.11(-1.00 to +0.99). Note: Bits [4:0] of this field are hardwired to 0.
D2COLOR_MATRIX_SIGN_2_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C23 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_2_4 - RW - 32 bits -, GpuF0MMReg:0x6BA0			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_2_4	26:8	0x0	Combined matrix constant C24 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S11.1(-2048.5 to +2047.5). It includes subtraction of 512 offset Note: Bits [6:0] of this field are hardwired to 0.
D2COLOR_MATRIX_SIGN_2_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C24 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_3_1 - RW - 32 bits -, GpuF0MMReg:0x6BA4			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_3_1	15:0	0x0	Combined matrix constant C31 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S0.11(-1.00 to +0.99). Note: Bits [4:0] of this field are hardwired to 0.
D2COLOR_MATRIX_SIGN_3_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C31 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_3_2 - RW - 32 bits -, GpuF0MMReg:0x6BA8			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_3_2	15:0	0x0	Combined matrix constant C32 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S0.11(-1.00 to +0.99). Note: Bits [4:0] of this field are hardwired to 0.
D2COLOR_MATRIX_SIGN_3_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C32 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_3_3 - RW - 32 bits -, GpuF0MMReg:0x6BAC			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_3_3	16:0	0x0	Combined matrix constant C33 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S1.11(-2.00 to +1.99). Note: Bits [4:0] of this field are hardwired to 0.
D2COLOR_MATRIX_SIGN_3_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C33 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_3_4 - RW - 32 bits -, GpuF0MMReg:0x6BB0			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_3_4	26:8	0x0	Combined matrix constant C34 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S11.1(-2048.5 to +2047.5). It includes subtraction of 512 offset Note: Bits [6:0] of this field are hardwired to 0.
D2COLOR_MATRIX_SIGN_3_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C34 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

2.9.18 Secondary Display Subsampling Registers

D2COLOR_SPACE_CONVERT - RW - 32 bits -, GpuF0MMReg:0x693C			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_SUBSAMPLE_CRCB_MODE	1:0	0x0	Sub-sampling control for secondary display 0=Do not subsample CrCb(RB) 1=Subsample CrCb (RB) by using 2 tap average method 2=Subsample CrCb (RB) by using 1 tap on even pixel 3=Subsample CrCb (RB) by using 1 tap on odd pixel
Sub-sampling control for secondary display.			

2.9.19 Secondary Display Realtime Overlay Registers

D2OVL_RT_SKEWCOMMAND - RW - 32 bits -, GpuF0MMReg:0x6D00			
Field Name	**Bits**	**Default**	**Description**
D2OVL_RT_CLEAR_GOBBLE_COUNT (W)	0	0x0	Writing 1 to this bit clears the gobbleCount. This bit has higher priority than inc_gobblecount
D2OVL_RT_INC_GOBBLE_COUNT (W)	4	0x0	Writing 1 to this bit increments the gobbleCount
D2OVL_RT_CLEAR_SUBMIT_COUNT (W)	8	0x0	Writing 1 to this bit clears the submitCount. This bit has higher priority than inc_submitcount
D2OVL_RT_INC_SUBMIT_COUNT (W)	12	0x0	Writing 1 to this bit increments the submitCount
D2OVL_RT_GOBBLE_COUNT (R)	18:16	0x0	Read only register The gobble count value which increments with each inc_gobble_count, and resets with clear_gobble_count commands. It wraps around on overflow during increment.
D2OVL_RT_SUBMIT_COUNT (R)	22:20	0x0	read only register Submits the count value which increments with each inc_submit_count, and resets with clear_submit_count commands. It wraps around on overflow during increment.
Reset or increment submit and gobble count			

D2OVL_RT_SKEWCONTROL - RW - 32 bits -, GpuF0MMReg:0x6D04			
Field Name	**Bits**	**Default**	**Description**
D2OVL_RT_CAPS	2:0	0x0	Max value in submitCount and gobbleCount. This is the number of contents buffer - 1. It should reset counters before programming this field
D2OVL_RT_SKEW_MAX	6:4	0x0	Max skew allowed between gobbleCount and submitCount
Controls for submit and gobble counts			

D2OVL_RT_BAND_POSITION - RW - 32 bits -, GpuF0MMReg:0x6D08			
Field Name	**Bits**	**Default**	**Description**
D2OVL_RT_TOP_SCAN	13:0	0x0	Defines the top scan line for the next RT (inclusive)
D2OVL_RT_BTM_SCAN	29:16	0x0	Defines the bottom scan line for next RT (exclusive)
The position of the top and bottom scan line for next RT			

D2OVL_RT_PROCEED_COND - RW - 32 bits -, GpuF0MMReg:0x6D0C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_RT_REDUCE_DELAY	0	0x0	0=Selects delay optimized scheme 1=Selects basic render behind delay scan scheme
D2OVL_RT_RT_FLIP	4	0x0	0=Selects bandSync to be exposed to CP 1=Selects frameSync to be exposed to CP
D2OVL_RT_PROCEED_ON_EOF_DISABLE	8	0x0	0=Enables unfinished bands to pass bandSync on EOF (valid only in basic scheme) 1=Disables this feature
D2OVL_RT_WITH_HELD_ON_SOF	12	0x0	0=Disables proceedOnEOF on next frameSync 1=Disables proceedOnEOF on next SOF
D2OVL_RT_CLEAR_GOBBLE_GO (W)	14	0x0	This bit clears gobbleGo. It disables another frame submit before next flip (ignored in basic scheme)
D2OVL_RT_TEAR_PROOF_HEIGHT	29:16	0x0	Defines the number of scan lines above topscan. If display starts reading from there, RT should wait
Select RT flip proceed condition			

D2OVL_RT_STAT - RW - 32 bits -, GpuF0MMReg:0x6D10			
Field Name	**Bits**	**Default**	**Description**
D2OVL_RT_FIP_PROCEED_ACK (W)	0	0x0	The sticky bit clears the FIP_PROCEED FLAG flag when written
D2OVL_RT_FRAME_SYNC_ACK (W)	1	0x0	The sticky bit clears the RT_FRAME_SYNC flag when written
D2OVL_RT_OVL_START_ACK (W)	2	0x0	The sticky bit clears the OVL_START FLAG flag when written
D2OVL_RT_BAND_INVISIBLE (R)	8	0x0	Debug bit indicating that overlay scanning in invisble region
D2OVL_RT_BAND_SYNC (R)	9	0x0	Debug bit indicating that overlay bottom scan is less the line counter
D2OVL_RT_EOF_PRPCEED (R)	10	0x0	Debug bit indicating that overlay is ended. Set at eof and reset at overlay start
D2OVL_RT_FIP_PROCEED (R)	11	0x0	Sticky debug bit that set when RT_FLIP_PROCEED signal asserted.
D2OVL_RT_FRAME_SYNC (R)	12	0x0	Sticky debug bit indicating that overlay start set and a new submission occured

D2OVL_RT_GOBBLE_GO (R)	13	0x0	Debug bit that set on frame_sync and clear at gobbleclr
D2OVL_RT_NEW_SUBMIT (R)	14	0x0	Debug bit indicating a new submission occurred
D2OVL_RT_OVL_START (R)	15	0x0	Debug bit indicating that line buffer detects start of overlay being accessed
D2OVL_RT_OVL_ENDED (R)	16	0x0	Debug bit indicating that line buffer detects that the end of overlay being accessed
D2OVL_RT_SAFE_ZONE (R)	17	0x0	Debug bit indicating that overlay is scaning in safe zone
D2OVL_RT_SWITCH_REGIONS (R)	18	0x0	Debug bit showing the postion of scan region relative to display
D2OVL_SKEW_MAX_REACHED (R)	19	0x0	Debug bit indicating that line buffer detected maximum skew reached
D2OVL_LINE_COUNTER (R)	31:20	0x0	debug bit showing display line counter value
Status Bits			

2.9.20 Secondary Display Hardware Cursor Registers

D2CUR_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6C00			
Field Name	**Bits**	**Default**	**Description**
D2CURSOR_EN	0	0x0	Secondary display hardware cursor enabled. 0=Disable 1=Enable
D2CURSOR_MODE	9:8	0x0	Secondary display hardware cursor mode. For 2bpp mode, each line of cursor data is stored in memory as 16 bits of AND data followed by 16 bits XOR data. For color AND/XOR mode, each pixel is stored sequentially in memory as 32bits each in aRGB8888 format with bit 31 of each DWord being the AND bit. For the color alpha modes the format is also 32bpp aRGB8888 with all 8 bits of the alpha being used.All HW cursor lines must be 64 pixels wide and all lines must be stored sequentially in memory. 0=Mono (2bpp) 1=Color 24bpp + 1 bit AND (32bpp) 2=Color 24bpp + 8 bit alpha (32bpp) premultiplied alpha 3=Color 24bpp + 8 bit alpha (32bpp)unmultiplied alpha
D2CURSOR_2X_MAGNIFY	16	0x0	Secondary display hardware cursor 2x2 magnification. 0=No 2x2 magnification 1=2x2 magnification in horizontal and vertical direction
D2CURSOR_FORCE_MC_ON	20	0x0	When set, if the incoming data is in D1 cursor region, DCP_LB_cursor1_allow_stutter is set. This field in this double bufferred register is not double buffered.
Secondary display hardware control			

D2CUR_SURFACE_ADDRESS - RW - 32 bits -, GpuF0MMReg:0x6C08			
Field Name	**Bits**	**Default**	**Description**
D2CURSOR_SURFACE_ADDRESS	31:0	0x0	Secondary display hardware cursor surface base address in byte. It is 4K byte aligned. Note: Bits [11:0] of this field are hardwired to 0.
Secondary display hardware cursor surface base address.			

D2CUR_SIZE - RW - 32 bits -, GpuF0MMReg:0x6C10			
Field Name	**Bits**	**Default**	**Description**
D2CURSOR_HEIGHT	5:0	0x0	Secondary display hardware cursor height minus 1.
D2CURSOR_WIDTH	21:16	0x0	Secondary display hardware cursor width minus 1.
Secondary display hardware size			

D2CUR_POSITION - RW - 32 bits -, GpuF0MMReg:0x6C14			
Field Name	**Bits**	**Default**	**Description**
D2CURSOR_Y_POSITION	12:0	0x0	Secondary display hardware cursor X coordinate at the hot spot relative to the desktop coordinates.
D2CURSOR_X_POSITION	28:16	0x0	Secondary display hardware cursor X coordinate at the hot spot relative to the desktop coordinates.
Secondary display hardware cursor position			

D2CUR_HOT_SPOT - RW - 32 bits -, GpuF0MMReg:0x6C18			
Field Name	**Bits**	**Default**	**Description**
D2CURSOR_HOT_SPOT_Y	5:0	0x0	Secondary display hardware cursor hot spot X length relative to the top left corner.
D2CURSOR_HOT_SPOT_X	21:16	0x0	Secondary display hardware cursor hot spot Y length relative to the top left corner.
Secondary display hardware cursor hot spot position			

D2CUR_COLOR1 - RW - 32 bits -, GpuF0MMReg:0x6C1C			
Field Name	**Bits**	**Default**	**Description**
D2CUR_COLOR1_BLUE	7:0	0x0	Secondary display hardware cursor blue component of color 1.
D2CUR_COLOR1_GREEN	15:8	0x0	Secondary display hardware cursor green component of color 1.
D2CUR_COLOR1_RED	23:16	0x0	Secondary display hardware cursor red component of color 1.
Secondary display hardware cursor color 1.			

D2CUR_COLOR2 - RW - 32 bits -, GpuF0MMReg:0x6C20			
Field Name	**Bits**	**Default**	**Description**
D2CUR_COLOR2_BLUE	7:0	0x0	Secondary display hardware cursor blue component of color 2.
D2CUR_COLOR2_GREEN	15:8	0x0	Secondary display hardware cursor green component of color 2.
D2CUR_COLOR2_RED	23:16	0x0	Secondary display hardware cursor red component of color 2.
Secondary display hardware cursor color 2.			

D2CUR_UPDATE - RW - 32 bits -, GpuF0MMReg:0x6C24			
Field Name	**Bits**	**Default**	**Description**
D2CURSOR_UPDATE_PENDING (R)	0	0x0	Secondary display hardware cursor update pending status. It is set to 1 after a host write to cursor double buffer register. It is cleared after double buffering is done. The double buffering occurs when D2CURSOR_UPDATE_PENDING = 1 and D2CURSOR_UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC2 is disabled, the registers will be updated instantly. The D2CUR double buffer registers are: D2CURSOR_EN D2CURSOR_MODE D2CURSOR_2X_MAGNIFY D2CURSOR_SURFACE_ADDRESS D2CURSOR_HEIGHT D2CURSOR_WIDTH D2CURSOR_X_POSITION D2CURSOR_Y_POSITION D2CURSOR_HOT_SPOT_X D2CURSOR_HOT_SPOT_Y 0=No update pending 1=Update pending
D2CURSOR_UPDATE_TAKEN (R)	1	0x0	Secondary display hardware cursor update taken status. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0
D2CURSOR_UPDATE_LOCK	16	0x0	Secondary display hardware cursor update lock control. 0=Unlocked 1=Locked
D2CURSOR_DISABLE_MULTIPLE_UPDATE	24	0x0	0=D2CURSOR registers can be updated multiple times in one V_UPDATE period 1=D2CURSOR registers can only be updated once in one V_UPDATE period

2.9.21 Secondary Display Hardware Icon Registers

D2ICON_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6C40			
Field Name	**Bits**	**Default**	**Description**
D2ICON_ENABLE	0	0x0	Secondary display hardware icon enable. 0=Disable 1=Enable
D2ICON_2X_MAGNIFY	16	0x0	Secondary display hardware icon 2x2 magnification. 0=No 2x2 magnification 1=2x2 magnification in horizontal and vertical direction
D2ICON_FORCE_MC_ON	20	0x0	When set, if the incoming data is in D1 icon region, DCP_LB_icon2_allow_stutter is set. This field in this double bufferred register is not double buffered.
Secondary display hardware icon control.			

D2ICON_SURFACE_ADDRESS - RW - 32 bits -, GpuF0MMReg:0x6C48			
Field Name	**Bits**	**Default**	**Description**
D2ICON_SURFACE_ADDRESS	31:0	0x0	Secondary display hardware icon surface base address in byte. It is 4K byte aligned. Note: Bits [11:0] of this field are hardwired to 0.
Secondary display hardware icon surface base address.			

D2ICON_SIZE - RW - 32 bits -, GpuF0MMReg:0x6C50			
Field Name	**Bits**	**Default**	**Description**
D2ICON_HEIGHT	6:0	0x0	Secondary display hardware icon height minus 1.
D2ICON_WIDTH	22:16	0x0	Secondary display hardware icon width minus 1.
Secondary display hardware icon size.			

D2ICON_START_POSITION - RW - 32 bits -, GpuF0MMReg:0x6C54			
Field Name	**Bits**	**Default**	**Description**
D2ICON_Y_POSITION	12:0	0x0	Secondary display hardware icon Y start coordinate related to the desktop coordinates. Note: The icon cannot be off the top and off the left edge of the display surface. But it can be off the bottom and off the right edge of the display.
D2ICON_X_POSITION	28:16	0x0	Secondary display hardware icon X start coordinate relative to the desktop coordinates. Note: The Icon cannot be off the top and off the left edge of the display surface. But it can be off the bottom and off the right edge of the display.
Secondary display hardware icon position			

D2ICON_COLOR1 - RW - 32 bits -, GpuF0MMReg:0x6C58			
Field Name	**Bits**	**Default**	**Description**
D2ICON_COLOR1_BLUE	7:0	0x0	Secondary display hardware icon blue component of color 1.
D2ICON_COLOR1_GREEN	15:8	0x0	Secondary display hardware icon green component of color 1.
D2ICON_COLOR1_RED	23:16	0x0	Secondary display hardware icon red component of color 1.
Secondary display hardware icon color 1.			

D2ICON_COLOR2 - RW - 32 bits -, GpuF0MMReg:0x6C5C			
Field Name	**Bits**	**Default**	**Description**
D2ICON_COLOR2_BLUE	7:0	0x0	Secondary display hardware icon blue component of color 2.
D2ICON_COLOR2_GREEN	15:8	0x0	Secondary display hardware icon green component of color 2.
D2ICON_COLOR2_RED	23:16	0x0	Secondary display hardware icon red component of color 2.
Secondary display hardware icon color 2.			

D2ICON_UPDATE - RW - 32 bits -, GpuF0MMReg:0x6C60			
Field Name	**Bits**	**Default**	**Description**
D2ICON_UPDATE_PENDING (R)	0	0x0	Secondary display hardware icon update Pending status. It is set to 1 after a host write to icon double buffer register. It is cleared after double buffering is done. The double buffering occurs when D2ICON_UPDATE_PENDING = 1 and D2ICON_UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC2 is disabled, the registers will be updated instantly. D2IOCN double buffer registers include : D2ICON_ENABLE D2ICON_2X_MAGNIFY D2ICON_SURFACE_ADDRESS D2ICON_HEIGHT D2ICON_WIDTH D2ICON_Y_POSITION D2ICON_X_POSITION 0=No update pending 1=Update pending
D2ICON_UPDATE_TAKEN (R)	1	0x0	Secondary display hardware icon update Taken status. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0
D2ICON_UPDATE_LOCK	16	0x0	Secondary display hardware icon update lock control. 0=Unlocked 1=Locked
D2ICON_DISABLE_MULTIPLE_UPDATE	24	0x0	0=D2ICON registers can be updated multiple times in one V_UPDATE period 1=D2ICON registers can only be updated once in one V_UPDATE period
Secondary display hardware icon update control			

2.9.22 Secondary Display Multi-VPU Control Registers

D2_MVP_AFR_FLIP_MODE - RW - 32 bits -, GpuF0MMReg:0x65E8			
Field Name	**Bits**	**Default**	**Description**
D2_MVP_AFR_FLIP_MODE	1:0	0x0	10=Real flip 11=Dummy flip
S/W writes to this register in AFR mode for display 2 page flip			

D2_MVP_AFR_FLIP_FIFO_CNTL - RW - 32 bits -, GpuF0MMReg:0x65EC			
Field Name	**Bits**	**Default**	**Description**
D2_MVP_AFR_FLIP_FIFO_NUM_ENTRIES (R)	3:0	0x0	Number of valid entries in the AFR flip FIFO
D2_MVP_AFR_FLIP_FIFO_RESET	4	0x0	Reset the AFR flip FIFO
D2_MVP_AFR_FLIP_FIFO_RESET_FLAG (R)	8	0x0	Sticky bit of the AFR flip fifo reset status
D2_MVP_AFR_FLIP_FIFO_RESET_ACK	12	0x0	Clear the DC_LB_MVP_AFR_FLIP_RESET_FLAG register bit
This register controls AFR Flip FIFO in display 2			

D2_MVP_FLIP_LINE_NUM_INSERT - RW - 32 bits -, GpuF0MMReg:0x65F0			
Field Name	**Bits**	**Default**	**Description**
D2_MVP_FLIP_LINE_NUM_INSERT_MODE	1:0	0x2	00=No insertion: 0 is appended 01=Debug: insert D2_MVP_FLIP_LINE_NUM_INSERT regiser value 10=Normal Hsync mode, insert the sum of LB line number + DC_LB_MVP_FLIP_LINE_NUM_OFFSET
D2_MVP_FLIP_LINE_NUM_INSERT	21:8	0x0	Used for debug purposes. This is will be the line number carried to downstream GPUs if D2_MVP_FLIP_LINE_NUM_INSERT_EN is set
D2_MVP_FLIP_LINE_NUM_OFFSET	29:24	0x0	Used in normal HSYNC flipping operation. This is the number added to the current LB (desktop) line number for carrying to the downstream GPUs
D2_MVP_FLIP_AUTO_ENABLE	30	0x0	Enables automatic AFR/SFR flipping for display 2
This register controls line number insertion for the Hsync flipping mode in display 2			

2.9.23 Display Look Up Table Control Registers

DC_LUT_RW_SELECT - RW - 32 bits -, GpuF0MMReg:0x6480			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_RW_SELECT	0	0x0	LUT host Read/write selection. 0=Host reads/writes to the LUT access the LUTA 1=Host reads/writes to the LUT access the LUTB
LUT host Read/write selection.			

DC_LUT_RW_MODE - RW - 32 bits -, GpuF0MMReg:0x6484			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_RW_MODE	0	0x0	LUT host read/write mode. 0=Host reads/writes to the LUT in 256-entry table mode 1=Host reads/writes to the LUT in piece wise linear (PWL) mode
LUT host read/write mode.			

DC_LUT_RW_INDEX - RW - 32 bits -, GpuF0MMReg:0x6488			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_RW_INDEX	7:0	0x0	LUT index for host read/write. In 256-entry table mode: LUT_ADDR[6:0] = INDEX[7:1]. INDEX[0] is used to select LUT lower or upper 10 bits. In piece wise linear (PWL) mode: LUT_ADDR[6:0] = INDEX[6:0]. INDEX[7] is not used
LUT index for host read/write.			

DC_LUT_SEQ_COLOR - RW - 32 bits -, GpuF0MMReg:0x648C			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_SEQ_COLOR	15:0	0x0	Sequential 10-bit R,G,B host read/write for LUT 256-entry table mode. After reset or writing DC_LUT_RW_INDEX register, first DC_LUT_SEQ_COLOR access is for red component, the second one is for green component and the third one is for blue component. Always access this register three times for one LUT entry in LUT 256-entry table mode. The LUT index is increased by 1 when LUT blue data is accessed. This allow you to access the next LUT entry without programming DC_LUT_RW_INDEX again. Note: Bits [5:0] of this field are hardwired to 0.
Sequential 10-bit R,G,B host read/write for LUT 256-entry table mode.			

DC_LUT_PWL_DATA - RW - 32 bits -, GpuF0MMReg:0x6490			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_BASE	15:0	0x0	Linear interpolation of base value for host read/write. Note: Bits [5:0] of this field are hardwired to 0.
DC_LUT_DELTA	31:16	0x0	Linear interpolation of delta value for host read/write. The LUT index is increased by 1 when register DC_LUT_PWL_DATA is accessed. Note: Bits [5:0] of this field are hardwired to 0.
Linear interpolation of base and delta host read/write for LUT PWL mode			

DC_LUT_30_COLOR - RW - 32 bits -, GpuF0MMReg:0x6494			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_COLOR_10_BLUE	9:0	0x0	10-bit blue value for host read/write. The LUT index is increased by 1 when register DC_LUT_30_COLOR is accessed.
DC_LUT_COLOR_10_GREEN	19:10	0x0	10-bit green value for host read/write.
DC_LUT_COLOR_10_RED	29:20	0x0	10-bit red value for host read/write.
Host read/write LUT R,G,B value for LUT 256-entry table mode			

DC_LUT_READ_PIPE_SELECT - RW - 32 bits -, GpuF0MMReg:0x6498			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_READ_PIPE_SELECT	0	0x0	LUT pipe selection for host read. 0=Host read select pipe 0 1=Host read select pipe 1
LUT pipe selection for host read.			

DC_LUT_WRITE_EN_MASK - RW - 32 bits -, GpuF0MMReg:0x649C			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_WRITE_EN_MASK	5:0	0x3f	Look-up table macro write enable mask for host write. For each bit Bit[0]=For pipe 1, B macro Bit[1]=For pipe 1, G macro Bit[2]=For pipe 1, R macro Bit[3]=For pipe 0, B macro Bit[4]=For pipe 0, G macro Bit[5]=For pipe 0, R macro 0=Host write disable 1=Host write enable
Look-up table macro write enable mask for host write.			

DC_LUT_AUTOFILL - RW - 32 bits -, GpuF0MMReg:0x64A0			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_AUTOFILL (W)	0	0x0	Enables LUT autofill when 1 is written into this field 0=No effect 1=Start LUT autofill
DC_LUT_AUTOFILL_DONE (R)	1	0x0	LUT autofill is done 0=LUT autofill is not completed 1=LUT autofill is done
LUT autofill control			

2.9.24 Display Controller Look Up Table A Registers

DC_LUTA_CONTROL - RW - 32 bits -, GpuF0MMReg:0x64C0			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_INC_B	3:0	0x0	Exponent of Power-of-two of blue data increment of LUTA palette. If INC = 0, LUT 256-entry table mode is enabled. LUT_INDEX = PIX_DATA[7:0]. Output = LUT_DATA[LUT_INDEX]. If INC > 0, LUT PWL mode is enabled with 128 entries of base and delta values. LUT_INDEX = PIX_DATA[INC+6:INC]. Mult = PIX_DATA[INC-1:0]. Base = LUT_BASE[LUT_INDEX]. Delta = LUT_DELTA[LUT_INDEX]. Output = Base + (Mult * Delta) / increment 0=Blue data increment = N/A 1=Blue data increment = 2 2=Blue data increment = 4 3=Blue data increment = 8 4=Blue data increment = 16 5=Blue data increment = 32 6=Blue data increment = 64 7=Blue data increment = 128 8=Blue data increment = 256 9=Blue data increment = 512
DC_LUTA_DATA_B_SIGNED_EN	4	0x0	Frame buffer blue data signed enable for look-up table A. 0=Blue data is unsigned 1=Blue data is signed
DC_LUTA_DATA_B_FLOAT_POINT_EN	5	0x0	Frame buffer blue data float point enable for look-up table A. 0=Blue data is fix point 1=Blue data is float point

DC_LUTA_INC_G	11:8	0x0	Exponent of Power-of-two of green data increment of LUTA palette. If INC = 0, LUT 256-entry table mode is enabled. LUT_INDEX = PIX_DATA[7:0]. Output = LUT_DATA[LUT_INDEX]. If INC > 0, LUT PWL mode is enabled with 128 entries of base and delta values. LUT_INDEX = PIX_DATA[INC+6:INC]. Mult = PIX_DATA[INC-1:0]. Base = LUT_BASE[LUT_INDEX]. Delta = LUT_DELTA[LUT_INDEX]. Output = Base + (Mult * Delta) / increment 0=Green data increment = N/A 1=Green data increment = 2 2=Green data increment = 4 3=Green data increment = 8 4=Green data increment = 16 5=Green data increment = 32 6=Green data increment = 64 7=Green data increment = 128 8=Green data increment = 256 9=Green data increment = 512
DC_LUTA_DATA_G_SIGNED_EN	12	0x0	Frame buffer green data signed enable for look-up table A. 0=Green data is unsigned 1=Green data is signed
DC_LUTA_DATA_G_FLOAT_POINT_EN	13	0x0	Frame buffer green data float point enable for look-up table A. 0=Green data is fix point 1=Green data is float point
DC_LUTA_INC_R	19:16	0x0	Exponent of Power-of-two of red data increment of LUTA palette. If INC = 0, LUT 256-entry table mode is enabled. LUT_INDEX = PIX_DATA[7:0]. Output = LUT_DATA[LUT_INDEX]. If INC > 0, LUT PWL mode is enabled with 128 entries of base and delta values. LUT_INDEX = PIX_DATA[INC+6:INC]. Mult = PIX_DATA[INC-1:0]. Base = LUT_BASE[LUT_INDEX]. Delta = LUT_DELTA[LUT_INDEX]. Output = Base + (Mult * Delta) / increment 0=Red data increment = N/A 1=Red data increment = 2 2=Red data increment = 4 3=Red data increment = 8 4=Red data increment = 16 5=Red data increment = 32 6=Red data increment = 64 7=Red data increment = 128 8=Red data increment = 256 9=Red data increment = 512
DC_LUTA_DATA_R_SIGNED_EN	20	0x0	Frame buffer red data signed enable for look-up table A. 0=Red data is unsigned 1=Red data is signed
DC_LUTA_DATA_R_FLOAT_POINT_EN	21	0x0	Frame buffer red data float point enable for look-up table A. 0=Red data is fix point 1=Red data is float point
LUTA mode control			

DC_LUTA_BLACK_OFFSET_BLUE - RW - 32 bits -, GpuF0MMReg:0x64C4			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_BLACK_OFFSET_BLUE	15:0	0x0	Black value offset of blue component for LUTA.
Black value offset of blue component for LUTA.			

DC_LUTA_BLACK_OFFSET_GREEN - RW - 32 bits -, GpuF0MMReg:0x64C8			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_BLACK_OFFSET_GREEN	15:0	0x0	Black value offset of green component for LUTA.
Black value offset of green component for LUTA.			

DC_LUTA_BLACK_OFFSET_RED - RW - 32 bits -, GpuF0MMReg:0x64CC			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_BLACK_OFFSET_RED	15:0	0x0	Black value offset of red component for LUTA.
Black value offset of red component for LUTA.			

DC_LUTA_WHITE_OFFSET_BLUE - RW - 32 bits -, GpuF0MMReg:0x64D0			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_WHITE_OFFSET_BLUE	15:0	0xffff	White value offset of blue component for LUTA
White value offset of blue component for LUTA.			

DC_LUTA_WHITE_OFFSET_GREEN - RW - 32 bits -, GpuF0MMReg:0x64D4			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_WHITE_OFFSET_GREEN	15:0	0xffff	White value offset of green component for LUTA
White value offset of green component for LUTA			

DC_LUTA_WHITE_OFFSET_RED - RW - 32 bits -, GpuF0MMReg:0x64D8			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_WHITE_OFFSET_RED	15:0	0xffff	White value offset of red component for LUTA
White value offset of red component for LUTA			

2.9.25 Display Controller Look Up Table B Registers

DC_LUTB_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6CC0			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_INC_B	3:0	0x0	Exponent of Power-of-two of blue data increment of LUTB palette. If INC = 0, LUT 256-entry table mode is enabled. LUT_INDEX = PIX_DATA[7:0]. Output = LUT_DATA[LUT_INDEX]. If INC > 0, LUT PWL mode is enabled with 128 entries of base and delta values. LUT_INDEX = PIX_DATA[INC+6:INC]. Mult = PIX_DATA[INC-1:0]. Base = LUT_BASE[LUT_INDEX]. Delta = LUT_DELTA[LUT_INDEX]. Output = Base + (Mult * Delta) / increment 0=Blue data increment = N/A 1=Blue data increment = 2 2=Blue data increment = 4 3=Blue data increment = 8 4=Blue data increment = 16 5=Blue data increment = 32 6=Blue data increment = 64 7=Blue data increment = 128 8=Blue data increment = 256 9=Blue data increment = 512
DC_LUTB_DATA_B_SIGNED_EN	4	0x0	Frame buffer blue data signed enable for look-up table A. 0=Blue data is unsigned 1=Blue data is signed
DC_LUTB_DATA_B_FLOAT_POINT_EN	5	0x0	Frame buffer blue data float point enable for look-up table A. 0=Blue data is fix point 1=Blue data is float point
DC_LUTB_INC_G	11:8	0x0	Exponent of Power-of-two of green data increment of LUTB palette. If INC = 0, LUT 256-entry table mode is enabled. LUT_INDEX = PIX_DATA[7:0]. Output = LUT_DATA[LUT_INDEX]. If INC > 0, LUT PWL mode is enabled with 128 entries of base and delta values. LUT_INDEX = PIX_DATA[INC+6:INC]. Mult = PIX_DATA[INC-1:0]. Base = LUT_BASE[LUT_INDEX]. Delta = LUT_DELTA[LUT_INDEX]. Output = Base + (Mult * Delta) / increment 0=Green data increment = N/A 1=Green data increment = 2 2=Green data increment = 4 3=Green data increment = 8 4=Green data increment = 16 5=Green data increment = 32 6=Green data increment = 64 7=Green data increment = 128 8=Green data increment = 256 9=Green data increment = 512

DC_LUTB_DATA_G_SIGNED_EN	12	0x0	Frame buffer green data signed enable for look-up table A. 0=Green data is unsigned 1=Green data is signed
DC_LUTB_DATA_G_FLOAT_POINT_EN	13	0x0	Frame buffer green data float point enable for look-up table A. 0=Green data is fix point 1=Green data is float point
DC_LUTB_INC_R	19:16	0x0	Exponent of Power-of-two of red data increment of LUTB palette. If INC = 0, LUT 256-entry table mode is enabled. LUT_INDEX = PIX_DATA[7:0]. Output = LUT_DATA[LUT_INDEX]. If INC > 0, LUT PWL mode is enabled with 128 entries of base and delta values. LUT_INDEX = PIX_DATA[INC+6:INC]. Mult = PIX_DATA[INC-1:0]. Base = LUT_BASE[LUT_INDEX]. Delta = LUT_DELTA[LUT_INDEX]. Output = Base + (Mult * Delta) / increment 0=Red data increment = N/A 1=Red data increment = 2 2=Red data increment = 4 3=Red data increment = 8 4=Red data increment = 16 5=Red data increment = 32 6=Red data increment = 64 7=Red data increment = 128 8=Red data increment = 256 9=Red data increment = 512
DC_LUTB_DATA_R_SIGNED_EN	20	0x0	Frame buffer red data signed enable for look-up table A. 0=Red data is unsigned 1=Red data is signed
DC_LUTB_DATA_R_FLOAT_POINT_EN	21	0x0	Frame buffer red data float point enable for look-up table A. 0=Red data is fix point 1=Red data is float point
LUTB mode control			

DC_LUTB_BLACK_OFFSET_BLUE - RW - 32 bits -, GpuF0MMReg:0x6CC4			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_BLACK_OFFSET_BLUE	15:0	0x0	Black value offset of blue component for LUTB.
Black value offset of blue component for LUTB.			

DC_LUTB_BLACK_OFFSET_GREEN - RW - 32 bits -, GpuF0MMReg:0x6CC8			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_BLACK_OFFSET_GREEN	15:0	0x0	Black value offset of green component for LUTB.
Black value offset of green component for LUTB.			

DC_LUTB_BLACK_OFFSET_RED - RW - 32 bits -, GpuF0MMReg:0x6CCC			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_BLACK_OFFSET_RED	15:0	0x0	Black value offset of red component for LUTB.
Black value offset of red component for LUTB.			

DC_LUTB_WHITE_OFFSET_BLUE - RW - 32 bits -, GpuF0MMReg:0x6CD0			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_WHITE_OFFSET_BLUE	15:0	0xffff	White value offset of blue component for LUTB
White value offset of blue component for LUTB.			

DC_LUTB_WHITE_OFFSET_GREEN - RW - 32 bits -, GpuF0MMReg:0x6CD4			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_WHITE_OFFSET_GREEN	15:0	0xffff	White value offset of green component for LUTB
White value offset of green component for LUTB			

DC_LUTB_WHITE_OFFSET_RED - RW - 32 bits -, GpuF0MMReg:0x6CD8			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_WHITE_OFFSET_RED	15:0	0xffff	White value offset of red component for LUTB
White value offset of red component for LUTB			

2.9.26 Display Controller CRC Registers

DCP_CRC_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6C80			
Field Name	**Bits**	**Default**	**Description**
DCP_CRC_ENABLE	0	0x0	Enables DCP CRC.
DCP_CRC_DISPLAY_SEL	1	0x0	Select display number for DCP CRC. 0=From display 1 1=From display 2
DCP_CRC_SOURCE_SEL	4:2	0x0	Select data source for DCP CRC. 0=DCP to LB pixel data 1=Lower 32 bits of graphics input data to DCP from DMIF 2=Upper 32 bits of graphics input data to DCP from DMIF 3=Overlay input data to DCP from DMIF 4=DCP to LB control signals TAG[2:0] and end of chunk
DCP CRC control			

DCP_CRC_MASK - RW - 32 bits -, GpuF0MMReg:0x6C84			
Field Name	**Bits**	**Default**	**Description**
DCP_CRC_MASK	31:0	0x0	Mask bits to apply to DCP CRC function. Allows CRC of only specific color and/or specific bits if wanted. Ignore those bits with mask bits to be 0
Mask bits to apply to DCP CRC function.			

DCP_CRC_P0_CURRENT - RW - 32 bits -, GpuF0MMReg:0x6C88			
Field Name	**Bits**	**Default**	**Description**
DCP_CRC_P0_CURRENT (R)	31:0	0x0	Current value of CRC for current frame pipe 0.
Current value of CRC for current frame pipe 0.			

DCP_CRC_P1_CURRENT - RW - 32 bits -, GpuF0MMReg:0x6C8C			
Field Name	**Bits**	**Default**	**Description**
DCP_CRC_P1_CURRENT (R)	31:0	0x0	Current value of CRC for current frame pipe 1.
Current value of CRC for current frame pipe 1.			

DCP_CRC_P0_LAST - RW - 32 bits -, GpuF0MMReg:0x6C90			
Field Name	**Bits**	**Default**	**Description**
DCP_CRC_P0_LAST (R)	31:0	0x0	Final value of CRC for previous frame pipe 0.
Final value of CRC for previous frame pipe 0.			

DCP_CRC_P1_LAST - RW - 32 bits -, GpuF0MMReg:0x6C94			
Field Name	**Bits**	**Default**	**Description**
DCP_CRC_P1_LAST (R)	31:0	0x0	Final value of CRC for previous frame pipe 1.
Final value of CRC for previous frame pipe 1.			

2.9.27 Display Controller to Line Buffer Control Registers

DCP_LB_DATA_GAP_BETWEEN_CHUNK - RW - 32 bits -, GpuF0MMReg:0x6CBC			
Field Name	**Bits**	**Default**	**Description**
DCP_LB_GAP_BETWEEN_CHUNK_20BPP	3:0	0x5	This register is used to control gap between data chunks sent from DCP to LB when the next LB data chunk is in 20bpp mode. The gap between current chunk and next chunk will be register value plus 1. The default value is 5. If any display has 32bpp digital output enabled, this valus should be set to 6.
DCP_LB_GAP_BETWEEN_CHUNK_30BPP	7:4	0x1	This register is used to control gap between data chunks sent from DCP to LB when the next LB data chunk is in 30bpp mode. The gap between current chunk and next chunk will be register value plus 1. The default value is 1. If any display has 32bpp digital output enabled, this valus should be set to 4
DCP LB chunk gap control			

2.9.28 Display/Memory Interface Control and Status Registers

DCP_TILING_CONFIG - RW - 32 bits -, GpuF0MMReg:0x6CA0			
Field Name	**Bits**	**Default**	**Description**
PIPE_TILING	3:1	0x3	This specifies the number of logical rendering pipes to use in the tiling pattern. Typically this should match the number of memory channels. 0=CONFIG_1_PIPE: 1 logical rendering pipe 1=CONFIG_2_PIPE: 2 logical rendering pipes 2=CONFIG_4_PIPE: 4 logical rendering pipes 3=CONFIG_8_PIPE: 8 logical rendering pipes
BANK_TILING	5:4	0x0	This specifies the number of logical banks to use in the tiling pattern. Typically this should match the number of physical banks in the DRAMs, though it can be smaller (e.g. for DRAMs that have more banks than the tiling supports) or larger (e.g. if rank selection is treated as a logical bank bit). 0=CONFIG_4_BANK: 4 logical DRAM banks 1=CONFIG_8_BANK: 8 logical DRAM banks
GROUP_SIZE	7:6	0x0	This specifies the memory interleave group size. All surfaces must be aligned to start at a group interleave boundary. Sequential reads or writes in device address space access this many bytes from each memory channel in turn. Therefore this value determines the maximum DRAM burst size for sequential accesses. 0=CONFIG_256B_GROUP: 256B memory interleve groups 1=CONFIG_512B_GROUP: 512B memory interleve groups

ROW_TILING	10:8	0x2	This specifies a DRAM row size for use in tiling, within a given bank of a given memory channel. This may be smaller than the actual DRAM row size, but should not be larger. The tiling pattern switches banks at these row boundaries and clients may also use this field to determine whether two accesses might be in the same row. These strategies are not effective for scattered virtual memorty mappings. 0=CONFIG_1KB_ROW: Treat 1KB as DRAM row boundary 1=CONFIG_2KB_ROW: Treat 2KB as DRAM row boundary 2=CONFIG_4KB_ROW: Treat 4KB as DRAM row boundary 3=CONFIG_8KB_ROW: Treat 8KB as DRAM row boundary
BANK_SWAPS	13:11	0x1	When performing display reads, this specifies the maximum number of bytes accessed per memory channel within each bank before switching banks. This affects the DRAM burst length for display accesses. The actual burst length may be less, depending on the row size above and on whether the display access starts in the middle of a bank swap sequence. This also ensures that crossing a DRAM row boundary switches banks, provided that the virtual page mapping is aligned properly. 0=CONFIG_128B_SWAPS: Perform bank swap after 128B 1=CONFIG_256B_SWAPS: Perform bank swap after 256B 2=CONFIG_512B_SWAPS: Perform bank swap after 512B 3=CONFIG_1KB_SWAPS: Perform bank swap after 1KB
SAMPLE_SPLIT	15:14	0x3	This controls the number of bytes per tile that may be used to store multiple samples of fragments. If multi-sample data requires more bytes than this per tile, it is split into multiple slices. 0=CONFIG_1KB_SPLIT: Split multi-sample tiles over 1KB 1=CONFIG_2KB_SPLIT: Split multi-sample tiles over 2KB 2=CONFIG_4KB_SPLIT: Split multi-sample tiles over 4KB 3=CONFIG_8KB_SPLIT: Split multi-sample tiles over 8KB
This register is a copy of PDMA_TILING_CONFIG and may ONLY be written when the chip is idle, and MUST be matched by a write to GB_TILING_CONFIG, PDMA_TILING_CONFIG and all copies of *TILING_CONFIG. It affects the 2D tiling modes, so writing to it invalidates all 2D tiled surfaces.			

DCP_MULTI_CHIP_CNTL - RW - 32 bits -, GpuF0MMReg:0x6CA4			
Field Name	**Bits**	**Default**	**Description**
LOG2_NUM_CHIPS	2:0	0x0	Log2 of the number of chips in the multi-chip configuration.
MULTI_CHIP_TILE_SIZE	4:3	0x0	Size of the tile per chip within each super-tile. 0=16 x 16 pixel tile per chip. 1=32 x 32 pixel tile per chip. 2=64 x 64 pixel tile per chip. 3=128x128 pixel tile per chip.
Should be programmed with the same value as PA_SC_MULTI_CHIP_CNTL. Controls the Screen Divisioning for Multi-Chip Configurations			

DMIF_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6CB0			
Field Name	**Bits**	**Default**	**Description**
DMIF_BUFF_SIZE	1:0	0x0	DMIF memory size. 0x0=Full memory size, 384x256bits. 0x1=2/3 memory size. 0x2=1/3 memory size. 0x3=Reserved
DMIF_D1_REQ_BURST_SIZE	10:8	0x2	DMIF request burst size for display 1. 0x0=1 request. 0x1=2 requests. 0x2=4 requests. 0x3=8 requests. 0x4=16 requests.
DMIF_D2_REQ_BURST_SIZE	18:16	0x2	DMIF request burst size for display 2. 0x0=1 request. 0x1=2 requests. 0x2=4 requests. 0x3=8 requests. 0x4=16 requests.
DMIF control register			

DMIF_STATUS - RW - 32 bits -, GpuF0MMReg:0x6CB4			
Field Name	**Bits**	**Default**	**Description**
DMIF_MC_SEND_ON_IDLE (R)	0	0x0	This register bit is set to 1 if MH returns data to DMIF when there is no pending request. It is sticky bit. Once this bit is set to high, it will stay high until it is cleared by writing 1 to register DMIF_CLEAR_MH_DATA_ON_IDLE 0=MC does not send data to DMIF when there is no data request pending 1=MH sends data to DMIF when there is no data pending request.
DMIF_CLEAR_MC_SEND_ON_IDLE (W)	1	0x0	This register bit is used to clear register DMIF_MH_SEND_ON_IDLE 0=No effect 1=Clear register bit DMIF_MH_SEND_ON_IDLE
DMIF_MC_LATENCY_COUNTER_ENABLE	8	0x0	0=Disable MC latency counter 1=Enable MC latency counter
This is a debug register. DMIF status.			

2.9.29 MCIF Control Registers

MCIF_CONTROL - RW - 32 bits -, GpuF0MMReg:0x6CB8			
Field Name	**Bits**	**Default**	**Description**
MCIF_BUFF_SIZE	1:0	0x0	MCIF memory size. 0x0=Full memory size, 16x143bits. 0x1=3/4 memory size. 0x2=1/2 memory size. 0x3=1/4 memory size.
ADDRESS_TRANSLATION_ENABLE	4	0x0	Enables address translation for vga, cursor and icon memory controller requests 0=Disable 1=Enable
PRIVILEGED_ACCESS_ENABLE	8	0x0	Enables privileged page access for vga, cursor and icon memory controller requests 0=Disable 1=Enable
LOW_READ_URG_LEVEL	23:16	0x0	This is the urgency level for vga, cursor, icon and vip reads when they are all in low priority
MC_CLEAN_DEASSERT_LATENCY	29:24	0x10	This is the number of cycles mcif will wait after a write is transfered to the memory controller and before looking at the clean signal from the memory controller
MCIF_MC_LATENCY_COUNTER_ENABLE	30	0x0	0=Disable MC latency counter 1=Enable MC latency counter
MCIF control register			

2.9.30 Multi VPU Control Registers

DC_MVP_LB_CONTROL - RW - 32 bits -, GpuF0MMReg:0x65F4			
Field Name	**Bits**	**Default**	**Description**
D1_MVP_SWAP_LOCK_IN_MODE	1:0	0x1	01 - force input to 1, used for master GPU; 10 - use swap_lock_in, used for slave GPU or middle GPU; 01 is the default
D2_MVP_SWAP_LOCK_IN_MODE	5:4	0x2	01 - force input to 1, used for master GPU; 10 - use swap_lock_in, used for slave GPU or middle GPU; 10 is the default
DC_MVP_SWAP_LOCK_OUT_SEL	8	0x0	0 - use D1 swap out output, 1 - use D2 swap out output; default is D1 swap out
DC_MVP_SWAP_LOCK_OUT_FORCE_ONE	12	0x0	Force Swap_lock to be one
DC_MVP_SWAP_LOCK_OUT_FORCE_ZERO	16	0x0	Force Swap_lock to be zero
DC_MVP_D1_DFQ_EN	18	0x0	Enable DFQ in multi-GPU mode to select update_pending from DFQ engine
DC_MVP_D2_DFQ_EN	19	0x0	Enable DFQ in multi-GPU mode to select update_pending from DFQ engine
DC_MVP_D1_SWAP_LOCK_STATUS (R)	20	0x0	D1 swap_lock status
DC_MVP_D2_SWAP_LOCK_STATUS (R)	24	0x0	D2 swap_lock status
DC_MVP_SWAP_LOCK_IN_CAP (R)	28	0x0	Capture swap_lock_in, used in diagnostic mode
DC_MVP_SPARE_FLOPS (R)	31	0x0	USED for keeping spare flops (ECO)
DC MVP LB control register			

2.10 TV Output Registers

SD1_MAIN_CNTL2 - RW - 32 bits -, GpuF0MMReg:0x5E00			
Field Name	**Bits**	**Default**	**Description**
SD1_TVOUT_EN	0	0x0	0=Disable TVOUT block 1=Enable TVOUT block
SD1_HDTV_SEL	1	0x0	0=SDTV/NTSC/PAL enable 1=HDTV enable
SD1_IKOS_CAP_FRAME_PULSE	2	0x0	0=CAP_FRAME_PULSE occurs at end of each field or frame depending on mode 1=CAP_FRAME_PULSE occurs at the end of the second line after CRTC sends frame_start
TVOUT_RBBMIF_RDWR_TIMEOUT_DIS	31	0x0	0=Enable RBBMIF read/write timeout logic 1=Disable RBBMIF read/write timeout logic

SD1_Y_BREAK_POINT_SETTING - RW - 32 bits -, GpuF0MMReg:0x5E98			
Field Name	**Bits**	**Default**	**Description**
SD1_Y_GAIN_LIMIT	10:0	0x2ff	Gain (contrast) limit constant for the luminanace (Y) portion of the video signal. The range of this limiter is between 0 and 0x5FF
SD1_Y_BREAK_EN	16	0x0	Enables/Disable the Y gain break. When enabled, the Y component of the video signal will be attenuated by one half, for the portion that exeeds the SD1_Y_GAIN_LIMIT value 0=Disable 1=Enable
Contrast control register for Luminance portion of the video signal			

SD1_U_V_BREAK_POINT_SETTINGS - RW - 32 bits -, GpuF0MMReg:0x5E9C			
Field Name	**Bits**	**Default**	**Description**
SD1_U_GAIN_LIMIT	9:0	0x150	Gain (saturation) limit constant for the U portions of the chrominanace video signal. The range of this limiter is between 0 and 0x17f
SD1_U_BREAK_EN	12	0x0	Enables/Disable the U gain break. When enabled, the U components of the video signal will be attenuated by one half, for the portion that exeeds the SD1_U_GAIN_LIMIT value 0=Disable 1=Enable
SD1_V_GAIN_LIMIT	25:16	0x1d7	Gain (saturation) limit constant for the V portions of the chrominanace video signal. The range of this limiter is between 0 and 0x17f
SD1_V_BREAK_EN	28	0x0	Enables/Disable the V gain break. When enabled, the V components of the video signal will be attenuated by one half, for the portion that exeeds the SD1_V_GAIN_LIMIT value 0=Disable 1=Enable
Saturation control register for the Chrominance portion of the video signal			

SD1_Y_AND_PASSTHRU_GAIN_SETTINGS - RW - 32 bits -, GpuF0MMReg:0x5EA0			
Field Name	**Bits**	**Default**	**Description**
SD1_Y_GAIN	8:0	0x100	Unsigned 1.8 bit gain (contrast) value for the luminanace (Y) portion of the video signal. The maximum value is 100110011 (gain = 1.20).
SD1_VBI_PASSTHRU_GAIN	24:16	0x100	Unsigned 1.8 bit gain (contrast) value for the VBI pass through signal. The maximum value is 100110011 (gain = 1.20).
Contains contrast information for luminance video			

SD1_U_AND_V_GAIN_SETTINGS - RW - 32 bits -, GpuF0MMReg:0x5EA4			
Field Name	**Bits**	**Default**	**Description**
SD1_U_GAIN	8:0	0x100	Unsigned 1.8 bit gain setting for the U portions of the chrominance video signal. The maximum value is 100100000 (gain = 1.125). Values over 1.125 will be limited to 1.125.
SD1_V_GAIN	24:16	0x100	Unsigned 1.8 bit gain setting for the V portions of the chrominance video signal. The maximum value is 100100000 (gain = 1.125). Values over 1.125 will be limited to 1.125.
Contains saturation information for chrominance video			

SD1_LUMA_BLANK_SETUP_LEVELS - RW - 32 bits -, GpuF0MMReg:0x5EA8			
Field Name	**Bits**	**Default**	**Description**
SD1_BLANK_LEVEL	8:0	0xeb	Indicates the digital value of the luminance blanking level and is defined as SD1_LUMA_SYNC_TIP_LEVELS.SD1_Y_SYNC_TIP_LEVEL + digital equivalent of blank above sync tip. This blank above sync tip can be calculated by converting the sync voltage: (Sync Amplitude/Full Range DAC Amplitude for given Standard) * 1023(full input range of DAC)
SD1_SETUP_LEVEL	24:16	0xeb	Indicates the digital value of the black level in NTSC and is defined as SD1_BLANK_LEVEL + digital equivalent of black above blank level. This black above blank can be calculated by converting the pedestal IRE: (Setup IRE/Full White IRE) * Full Digital White = (7.5/92.5) * 512 = 42. SD1_SETUP_LEVEL = SD1_BLANK_LEVEL for all standards but NTSC
Indicates the SDTV1 luminance blank and setup levels for Composite, S-Video, 480i & 480p Component, and RGB with sync on green outputs			

SD1_RGB_OR_PBPR_BLANK_LEVEL - RW - 32 bits -, GpuF0MMReg:0x5EAC			
Field Name	**Bits**	**Default**	**Description**
SD1_RGB_OR_PBPR_BLANK_LEVEL	8:0	0xeb	Indicates the digital value of the luminance blanking level for Red and Blue if generating a RGB with sync on Green or the blank level for Pb & Pr, if set to a Component 480I or 480P mode. The mid range value of 512 is usually used in the PbPr case
SDTV1 Blank Level register for RGB with sync on Green if SD1_MAIN_CNTL.SD1_BLANK_ON_RB_SEL = 1 or for Component Pb and Pr			

SD1_LUMA_SYNC_TIP_LEVELS - RW - 32 bits -, GpuF0MMReg:0x5EB0			
Field Name	**Bits**	**Default**	**Description**
SD1_Y_SYNC_TIP_LEVEL	8:0	0x10	Indicates the digital value of the luminance sync tip or synchronization level. Usually set at 16 to give a 20 mV margin above the zero DAC level
SD1_PBPR_SYNC_TIP_LEVEL	24:16	0x111	Indicates the digital value of the Pb and Pr sync tip level and is defined as SD1_RGB_OR_PBPR_BLANK_LEVEL - digital equivalent of blank above sync tip. See the SD1_LUMA_BLANK_SETUP_LEVELS.SD1_BLANK_LEVEL description for the blank above sync tip calculation. If no synchronizing pulses are required for Pb and Pr, set SD1_PBPR_SYNC_TIP_LEVEL = SD1_RGB_OR_PBPR_BLANK_LEVEL
SDTV1 Sync Tip register for Luminance or for Component Pb and Pr			

SD1_LUMA_FILT_CNTL - RW - 32 bits -, GpuF0MMReg:0x5EB4			
Field Name	**Bits**	**Default**	**Description**
SD1_YFLT_EN	0	0x1	Enables/Disables the Luminance filter
SD1_COMPY_OUT_BLEND	11:8	0x4	Controls sharpness blending of luma filters for Composite output. Bits [3:2] select the alternate filter: 00=Composite 01=S-video 10=1:1 Slew 11=Raw un-filtered data Bits [1:0] controls a 2-bit alpha blend: 00=100% alternate filter 01=75% alternate filter, 25% base filter 10=50% alternate filter, 50% base filter 11=25% alternate filter, 75% base filter The Composite filter is the base filter for the Composite output.

SD1_SVIDY_OUT_BLEND	15:12	0x0	Controls sharpness blending of luma filters for S-Video output. Bits [3:2] select the alternate filter: 00=S-Video 01=Composite 10=1:1 Slew 11=Raw un-filtered data Bits [1:0] controls a 2-bit alpha blend: 00=100% alternate filter 01=75% alternate filter, 25% base filter 10=50% alternate filter, 50% base filter 11=25% alternate filter, 75% base filter The S-Video filter is the base filter for the S-Video output.
SD1_COMP_PASSTHRU_BLEND	19:16	0x0	Controls sharpness blending of luma filters for Composite VBI passthrough output. Bits [3:2] select the alternate filter: 00=Composite 01=S-video 10=1:1 Slew 11=Raw un-filtered data Bits [1:0] controls a 2-bit alpha blend: 00=100% alternate filter 01=75% alternate filter, 25% base filter 10=50% alternate filter, 50% base filter 11=25% alternate filter, 75% base filter The Composite filter is the base filter for the Composite VBI passthrough output.
SD1_SVID_PASSTHRU_BLEND	23:20	0x0	Controls sharpness blending of luma filters for S-Video VBI passthrough output. Bits [3:2] select the alternate filter: 00=S-Video 01=Composite 10=1:1 Slew 11=Raw un-filtered data Bits [1:0] controls a 2-bit alpha blend: 00=100% alternate filter 01=75% alternate filter, 25% base filter 10=50% alternate filter, 50% base filter 11=25% alternate filter, 75% base filter The S-Video filter is the base filter for the S-Video VBI passthrough output.
SD1_OUTSIDE_ACTIVE_SLEW_EN	24	0x1	Enables/Disables Slewing of the video signal during the blank region. If disabled, the blank region of the video signal will be filtered with the filter settings specified above(_BLEND) for the active portion of the video signal. If enabled the blank region of the video signal will be slewed
SD1_INSIDE_ACTIVE_SLEW_EN	25	0x0	Enables/Disables Slewing of the video signal during the active region. If disabled, the active portion of the video signal will be filtered with _BLEND settings specified bove. If enabled, the active portion of the video signal will be slewed and no other filter settings will apply
SD1_LUMA_DITHER_SEL	29:28	0x0	Controls the addition of dither to Luminance data. Choices are truncate, round, dither with random number, dither with previous data
Specifies filter settings and dither settings(first) for Luminance video signal			

SD1_LUMA_COMB_FILT_CNTL1 - RW - 32 bits -, GpuF0MMReg:0x5EB8			
Field Name	**Bits**	**Default**	**Description**
SD1_COMB_EN	0	0x0	Enables/Disables the Combing on composite video output
SD1_DISABLE_FIRST_LAST	1	0x0	Enables/Disables Combing on the first and last active lines of the composite video output
SD1_COMB_LINE_SEL	9:8	0x0	Selects between 3 line comb, or 2 line from upper or lower two pair of lines
SD1_P2	21:16	0x0	Reference level for AGC nominal 0x20
SD1_P3	30:24	0x0	Gain up value for AGC
Comb filter register control 1			

SD1_LUMA_COMB_FILT_CNTL2 - RW - 32 bits -, GpuF0MMReg:0x5EBC			
Field Name	**Bits**	**Default**	**Description**
SD1_P4	7:0	0x0	Lowers clip limit or force for AGC multiplier
SD1_P5	8	0x0	Selects control curve multiplier inputs
SD1_P6	21:16	0x0	Sets coring level for nominal signals
SD1_P7	27:24	0x0	Controls the slope of the coring process to be below the P6 threshold
Comb filter register control 2			

SD1_LUMA_COMB_FILT_CNTL3 - RW - 32 bits -, GpuF0MMReg:0x5EC0			
Field Name	**Bits**	**Default**	**Description**
SD1_P10	5:0	0x0	Gain of bandpassed centre line to subtract from the Y for composite. Notch level
SD1_P8	16:8	0x0	Sets the final gain level for the control signal. Diagonal false color level
SD1_P9	26:20	0x0	Upper clip limit or force for final control signal
Comb filter register control 3			

SD1_LUMA_COMB_FILT_CNTL4 - RW - 32 bits -, GpuF0MMReg:0x5EC4			
Field Name	**Bits**	**Default**	**Description**
SD1_P11	5:0	0x0	Gain of checker board false color to subtract
SD1_FORCE_P9	8	0x0	Forces upper value for P9
Comb filter register control 4			

SD1_VIDOUT_MUX_CNTL - RW - 32 bits -, GpuF0MMReg:0x5EC8			
Field Name	**Bits**	**Default**	**Description**
SD1_VIDEO_SELECT_MUX0_EN	0	0x1	Enables/Disables the output mux 0 0=Send data 0 1=Send data as selected by RED_MX
SD1_VIDEO_SELECT_MUX1_EN	1	0x1	Enables/Disables the output mux 1 0=Send data 0 1=Send data as selected by GRN_MX
SD1_VIDEO_SELECT_MUX2_EN	2	0x1	Enables/Disables the output mux 2 0=Send data 0 1=Send data as selected by BLU_MX
SD1_VIDEO_SELECT_MUX0	7:4	0x1	Output Mux selection for first SDTV1 output, which is normally routed to the triple DAC output DAC4_CHROMA 0=iSVID_Y 1=iSVID_C 2=iCOMP 3=iGREEN 4=iBLUE 5=iRED 6=iYPBPR_Y 7=iPB 8=iPR 9=irf_FORCE_DAC_DATA 10=iDBG_INPUT_Y 11=iDBG_GAINED_Y 12=iDBG_YFORFILT 13=iDBG_SYNCb 14=iDBG_END_OF_STANDARD_FRAME 15=iDBG_RGB_Y
SD1_VIDEO_SELECT_MUX1	11:8	0x2	Output Mux selection for second SDTV1 output, which is normally routed to the triple DAC output DAC6_COMP 0=iSVID_Y 1=iSVID_C 2=iCOMP 3=iGREEN 4=iBLUE 5=iRED 6=iYPBPR_Y 7=iPB 8=iPR 9=irf_FORCE_DAC_DATA 10=iDBG_INPUT_Y 11=iDBG_GAINED_Y 12=iDBG_YFORFILT 13=iDBG_SYNCb 14=iDBG_END_OF_STANDARD_FRAME 15=iDBG_RGB_Y

SD1_VIDEO_SELECT_MUX2	15:12	0x0	Output Mux selection for third SDTV1 output, which is normally routed to the triple DAC output DAC5_LUMA 0=iSVID_Y 1=iSVID_C 2=iCOMP 3=iGREEN 4=iBLUE 5=iRED 6=iYPBPR_Y 7=iPB 8=iPR 9=irf_FORCE_DAC_DATA 10=iDBG_INPUT_Y 11=iDBG_GAINED_Y 12=iDBG_YFORFILT 13=iDBG_SYNCb 14=iDBG_END_OF_STANDARD_FRAME 15=iDBG_RGB_Y
SD1_ENCODER_BYPASS_EN	28	0x0	0=Bypass Encoder with DC offset in U,V 1=Bypass Encoder without any changes
SD1_VIDEO_OUTPUT_DITHER_SEL	31:30	0x0	Controls the addition of dither to all the output. Choices are truncate, round, dither with random number, dither with previous data
SDTV1 encoder output selection control register			

SD1_FORCE_DAC_DATA - RW - 32 bits -, GpuF0MMReg:0x5ECC			
Field Name	**Bits**	**Default**	**Description**
SD1_FORCE_DAC_DATA	9:0	0x0	Specifies a 10 bit value to be routed to those DAC(s) with the corresponding output selection mux(SD1_VIDOUT_MUX_CNTL.SD1_VIDEO_SELECT_MUX1 to .SD1_VIDEO_SELECT_MUX2) set to 9. The following registers must also be programmed: DAC_MUX_OUT_CNTL.MUX_CNTL_EN = 0 and DTO1_VCLK_DENOMIN.DTO1_EN = 0
This register allows data to be directly applied to the triple DACs			

SD1_CHROMA_MOD_CNTL - RW - 32 bits -, GpuF0MMReg:0x5EF0			
Field Name	**Bits**	**Default**	**Description**
SD1_U_BURST_LEVEL	8:0	0x1b2	U component burst level For NTSC: -(20IRE/92.5IRE) * 512 =0x191 For PAL: -(Sin45)*(21.5/100IRE)*512 = 0x1B2
SD1_V_BURST_LEVEL	24:16	0x4e	V component burst level For NTSC: = 0x0 For PAL: (cos45)*(21.5IRE/100IRE)*512 = 0x4E
SD1_COL_SC_SECOND_CORR_EN	26	0x0	When set to 1 in NTSC/PAL modes, the Sub-Carrier DTO Accumulator is incremented by a second correction set by SD1_SCM_COL_SC_INC_CORR and SD1_SCM_COL_SC_DENOMIN 0=Normal Sub-Carrier DTO correction with SD1_COL_SC_DENOMIN,SD1_COL_SC_INC,SD1_COL_SC_INC_CORR 1=Additional Sub-Carrier DTO correction controlled by SD1_SCM_COL_SC_DENOMIN, SD1_SCM_COL_SC_INC_CORR
SD1_CHROMA_PRE_MOD_DELAY_EN	27	0x0	When rf_PIX_DELAY_SEL = 0, sets the pixel delay alignment of chrominance signal before or after modulation
SD1_FORCE_BLACK_WHITE	29	0x0	Forces U and V values to be zero 0=colour ON 1=colour OFF
SD1_FORCE_BURST_ALWAYS	30	0x0	Active data will be ignored and Burst will be inserted all the way through 0=Normal Colour Burst production in encoder 1=Colour Burst fills the entire TV frame
SD1_UVFLT_EN	31	0x1	If enabled, U and V data gets filtered in U and V filters respectively or else no filtering occurs 0=Bypass U and V filters 1=Enable U and V filters
Chroma modulation control register			

SD1_COL_SC_DENOMIN - RW - 32 bits -, GpuF0MMReg:0x5EF4			
Field Name	**Bits**	**Default**	**Description**
SD1_COL_SC_DENOMIN	24:0	0x2	This register value determines when SD1_COL_SC_INC_CORR register value should be used as the Increment value for Sub-Carrier DTO Accumulato
Denominator portion of the correction factor. This field is used in NTSC/PAL mode and during Secam DB component generation			

SD1_COL_SC_INC - RW - 32 bits -, GpuF0MMReg:0x5EF8			
Field Name	**Bits**	**Default**	**Description**
SD1_COL_SC_INC	28:0	0x15555555	This is the increment value the Sub-Carrier DTO need to increment by every cycle except when the count of SD1_SCM_COL_SC_DENOMIN is reached. When the count of SD1_SCM_COL_SC_DENOMIN is reached, we will increment the accumulator by SD1_COL_SC_INC_CORR instead of COL_SC_INC. Use ssdtve.cpp to program this field
Increment value for Sub-Carrier DTO Accumulator. Used for NTSC/PAL sin/cos generation. In Secam mode, used for DB component generation			

SD1_COL_SC_INC_CORR - RW - 32 bits -, GpuF0MMReg:0x5EFC			
Field Name	**Bits**	**Default**	**Description**
SD1_COL_SC_INC_CORR	28:0	0x15555556	SD1_COL_SC_INC register value plus the correction factor. This total value will be the new Sub-Carrier DTO Accumulator increment when a count determined by SD1_SCM_COL_SC_DENOMIN register field is reached
Increment value for Sub-Carrier DTO Accumulator + Numerator portion of the required correction factor. This field is used in NTSC/PAL mode and during Secam DB component generation			

SD1_SCM_COL_SC_DENOMIN - RW - 32 bits -, GpuF0MMReg:0x5F00			
Field Name	**Bits**	**Default**	**Description**
SD1_SCM_COL_SC_DENOMIN	24:0	0x0	This register value determines when SD1_SCM_COL_SC_INC_CORR register value should be used as the Increment value for Sub-Carrier DTO Accumulator
This field is used only for Secam DR component generation. Denominator portion of the correction factor			

SD1_SCM_COL_SC_INC - RW - 32 bits -, GpuF0MMReg:0x5F04			
Field Name	**Bits**	**Default**	**Description**
SD1_SCM_COL_SC_INC	28:0	0x1533a6ae	This is the increment value the Sub-Carrier DTO need to increment by every cycle except when the count of SD1_SCM_COL_SC_DENOMIN is reached. When the count of SD1_SCM_COL_SC_DENOMIN is reached, we will increment the accumulator by SD1_SCM_COL_SC_INC_CORR insead of SD1_SCM_COL_SC_INC
This field is used only for Secam DR component generation. Increment value for Sub-Carrier DTO Accumulator.			

SD1_SCM_COL_SC_INC_CORR - RW - 32 bits -, GpuF0MMReg:0x5F08			
Field Name	**Bits**	**Default**	**Description**
SD1_SCM_COL_SC_INC_CORR	28:0	0x1533a6ae	SD1_COL_SC_INC register value plus the correction factor. This total value will be the new Sub-Carrier DTO Accumulator increment when a count determined by SD1_SCM_COL_SC_DENOMIN register field is reached
Increment value for Sub-Carrier DTO Accumulator + Numerator portion of the required correction factor			

SD1_SCM_MOD_CNTL - RW - 32 bits -, GpuF0MMReg:0x5F0C			
Field Name	**Bits**	**Default**	**Description**
SD1_SCM_BURST_GAIN	11:0	0x203	This register field value determines the amplitude of DR and DB signals
SD1_SCM_NOTCH_TUNER	21:16	0x2c	Sets the center of Secam high frequency subcarrier pre-emphasis filter at 4.286MHz frequency. Can be fine tuned in KHz granularity if required
SD1_SCM_ENABLE	24	0x0	Enables Secam mode there by generating Secam DR/DB color components. Setting this field high will disa ble NTSC and PAL color modulation
SD1_SCM_RST_DTO_ON_BLANK	25	0x0	Qualifier required to reset the Sub-Carrier DTO accumulator when in Secam mode. In Secam mode, DTO is reset during b lanking period
SD1_SCM_INVERT_PHASE_EN	26	0x0	Enables phase inversion of the DR and DB subcarriers
SD1_INVERT_SCM_3LINE	27	0x0	Swaps inversions specific to fields
SD1_SCM_3LINE_INIT	29:28	0x0	This field value is loaded into an internal mod 2 counter. If loaded by 0, the count values are 0,1,2 corresponding to phase values of 0,0,180. If loaded by 1, the count values are 1,2,0 corresponding to phase values of 0,180,0 and so on
SD1_SCM_2LINE_EN	30	0x0	Sets the internal counter into a mod 1 mode and the corresponding phase values are 0 and 180
SD1_SCM_DTO_LIMIT_EN	31	0x1	When set, the frequency swing of DR/DB components will be limited to a specific range . The register fields SD1_SCM_MIN_DTO_SWING and SD1_SCM_MAX_DTO_SWING will set the range, If this field is not set, there will be no limit set on the frequency swing
Secam modulation control register			

SD1_SCM_DB_DR_SCALE_FACTORS - RW - 32 bits -, GpuF0MMReg:0x5F10			
Field Name	**Bits**	**Default**	**Description**
SD1_SCM_DB_SCALE_FACTOR	15:0	0xa5f5	This field value is multiplied to the 'U' output of the low frequency pre-emphasis filter to generate the frequency deviation for the DB component
SD1_SCM_DR_SCALE_FACTOR	31:16	0x8c99	This field value is multiplied to the 'V' output of the low frequency pre-emphasis filter to generate the frequency deviation for the DR component
Used for generating the required frequency deviation for DR and DB components			

SD1_SCM_MIN_DTO_SWING - RW - 32 bits -, GpuF0MMReg:0x5F14			
Field Name	**Bits**	**Default**	**Description**
SD1_SCM_MIN_DTO_SWING	27:0	0x9620639	Sets the minimum frequency swing. Will take effect only when SD1_SCM_DTO_LIMIT_EN register field is set
Sets the minimum frequency swing for DR/DB components			

SD1_SCM_MAX_DTO_SWING - RW - 32 bits -, GpuF0MMReg:0x5F18			
Field Name	**Bits**	**Default**	**Description**
SD1_SCM_MAX_DTO_SWING	27:0	0xb713ce4	Sets the maximum frequency swing. Will take effect only when SD1_SCM_DTO_LIMIT_EN register field is set
Sets the maximum frequency swing for DR/DB components			

SD1_CRC_CNTL - RW - 32 bits -, GpuF0MMReg:0x5F1C			
Field Name	**Bits**	**Default**	**Description**
SD1_CRC_EN	0	0x0	Enables the CRC signature generation on those output(s) as selected by SD1_CRC_DATAIN_SEL 0=Reset/Disable 1=Enable
SD1_CRC_DATAIN_SEL	5:4	0x0	Selects the SDTV1 output(s) on which the CRC generation is to be performed 0=V0V1V2 1=V0 only 2=V1 only 3=V2 only
SD1_RST_SC_ON_FSYNC_4CRC	7	0x0	Forces the sub-carrier to be reset at every frame synchronization pulse to allow CRC generation across something other than the standard number of fields per frame(4 for NTSC, 8 for PAL) 0=Normal free running Sub-Carrier 1=Enable reset of Sub-Carrier every Frame Sync
SD1_PROGRESSIVE_MODE_CRC	8	0x0	Select interlaced of progressive mode CRC generation 0=CRC generation for interlaced modes 1=CRC generation for progressive modes
Controls the production of CRC signatures from the SDTV1 encoder output(s)			

SD1_VIDEO_PORT_SIG - RW - 32 bits -, GpuF0MMReg:0x5F20			
Field Name	**Bits**	**Default**	**Description**
SD1_CRC_SIG (R)	29:0	0x0	SD1_CRC_SIG(9:0) - CRC signature of VIDEO_0 output SD1_CRC_SIG(19:10) - CRC signature of VIDEO_1 output SD1_CRC_SIG(29:20) - CRC signature of VIDEO_2 output
Read only register containing the CRC signatures for VIDEO_0, VIDEO_1, and VIDEO_2 outputs of the SDTV1 encoder			

SD1_SDTV0_DEBUG - RW - 32 bits -, GpuF0MMReg:0x5F28			
Field Name	**Bits**	**Default**	**Description**
SD1_SDTV0_DEBUG	31:0	0xffff	SD1_SDTV0_DEBUG(31:0) Unassigned SD1_SDTV0_DEBUG(16) - Enable TVVBI muxing to debug bus
The bits in this register can be assigned control functions, if the debugging process yields additional needs			

SD1_COL_SC_PHASE_CNTL - RW - 32 bits -, GpuF0MMReg:0x5FD4			
Field Name	**Bits**	**Default**	**Description**
SD1_COL_SC_PHASE_INIT	15:0	0x0	Add phase offset to the Sub-Carrier DTO
Phase offset to the Sub-Carrier DTO			

SD1_LUMA_OFFSET_LIMIT - RW - 32 bits -, GpuF0MMReg:0x5F8C			
Field Name	**Bits**	**Default**	**Description**
SD1_LUMA_OFFSET	9:0	0x0	Luma offset value used in conjunction with SD1_Y_GAIN for color conversion.
SD1_LUMA_LIMIT	21:12	0x0	Luma limit used for color conversion
SD1_YC_OFFSET_LIMIT_BYPASS	24	0x0	0=Luma and chroma data are both offset. Luma data is limited 1=Bypass offset/limiting logic and sign extend luma and chroma data
Luma offset used for color conversion			

SD1_CHROMA_OFFSET - RW - 32 bits -, GpuF0MMReg:0x5F90			
Field Name	**Bits**	**Default**	**Description**
SD1_CHROMA_OFFSET	9:0	0x0	Chroma offset value used in conjunction with SD1_U_GAIN & SD1_V_GAIN for color conversion.
Chroma offset used for color conversion			

SD1_UPSAMPLE_MODE - RW - 32 bits -, GpuF0MMReg:0x5F94			
Field Name	**Bits**	**Default**	**Description**
SD1_FOUR_TAP_MODE	0	0x0	
SD1_UPSAMP_PICK_NEAR	4	0x0	

SD1_CRTC_HV_START - RW - 32 bits -, GpuF0MMReg:0x5F98			
Field Name	**Bits**	**Default**	**Description**
SD1_CRTC_H_START	12:0	0x0	CRTC horizontal capture frame pulse start.
SD1_CRTC_V_START	28:16	0x0	CRTC vertical capture frame pulse start. Note: In interlace mode, CRTC counts every other line, while TVOUT counts every line
CRTC capture pulse start location			

SD1_CRTC_TV_FRAMESTART_CNTL - RW - 32 bits -, GpuF0MMReg:0x5F9C			
Field Name	**Bits**	**Default**	**Description**
SD1_CRTC_TV_FRAMESTART_FREQ	1:0	0x0	0=TV FRAMESTART happens every 2 fields 1=TV FRAMESTART happens every 4 fields, NTSC standard 2=TV FRAMESTART happens every 8 fields, PAL standard 3=reserved

2.11 LVTMA Registers

LVTMA_DATA_SYNCHRONIZATION - RW - 32 bits -, GpuF0MMReg:0x7F98			
Field Name	**Bits**	**Default**	**Description**
LVTMA_DSYNSEL	0	0x1	0=Disable 1=Enable
LVTMA_PFREQCHG (W)	8	0x0	

LVTMA_PWRSEQ_REF_DIV - RW - 32 bits -, GpuF0MMReg:0x7F88			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PWRSEQ_REF_DIV	11:0	0x0	
LVTMA_BL_MOD_REF_DIV	27:16	0x0	

LVTMA_PWRSEQ_DELAY1 - RW - 32 bits -, GpuF0MMReg:0x7F8C			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PWRUP_DELAY1	7:0	0x0	
LVTMA_PWRUP_DELAY2	15:8	0x0	
LVTMA_PWRDN_DELAY1	23:16	0x0	
LVTMA_PWRDN_DELAY2	31:24	0x0	

LVTMA_PWRSEQ_DELAY2 - RW - 32 bits -, GpuF0MMReg:0x7F90			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PWRDN_MIN_LENGTH	7:0	0x0	

LVTMA_PWRSEQ_CNTL - RW - 32 bits -, GpuF0MMReg:0x7F80			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PWRSEQ_EN	0	0x0	
LVTMA_PWRSEQ_DISABLE_SYNCEN_ CONTROL_OF_TX_EN	1	0x0	
LVTMA_PLL_ENABLE_PWRSEQ_MASK	2	0x0	0=Power Sequencer cannot override PLL enable 1=Power Sequencer can override PLL enable
LVTMA_PLL_RESET_PWRSEQ_MASK	3	0x0	0=Power Sequencer cannot override PLL reset 1=Power Sequencer can override PLL reset
LVTMA_PWRSEQ_TARGET_STATE	4	0x0	
LVTMA_SYNCEN	8	0x0	
LVTMA_SYNCEN_OVRD	9	0x0	0=Disable 1=Enable
LVTMA_SYNCEN_POL	10	0x0	0=Non-invert 1=Invert
LVTMA_DIGON	16	0x0	

LVTMA_DIGON_OVRD	17	0x0	0=Disable 1=Enable
LVTMA_DIGON_POL	18	0x0	0=Non-invert 1=Invert
LVTMA_BLON	24	0x0	
LVTMA_BLON_OVRD	25	0x0	0=Disable 1=Enable
LVTMA_BLON_POL	26	0x0	0=Non-invert 1=Invert

LVTMA_PWRSEQ_STATE - RW - 32 bits -, GpuF0MMReg:0x7F84

Field Name	Bits	Default	Description
LVTMA_PWRSEQ_TARGET_STATE_R (R)	0	0x0	0=Power down 1=Power up
LVTMA_PWRSEQ_DIGON (R)	1	0x0	0=Off 1=On
LVTMA_PWRSEQ_SYNCEN (R)	2	0x0	0=Off 1=On
LVTMA_PWRSEQ_BLON (R)	3	0x0	0=Off 1=On
LVTMA_PWRSEQ_DONE (R)	4	0x0	0=Active 1=Done
LVTMA_PWRSEQ_STATE (R)	11:8	0x0	0=DISABLED: D=0, B=0, S=LVTMA_PWRSEQ_TARGET_STATE_R 1=POWERUP0: D=0 S=0 B=0 2=POWERUP1: D=1 S=0 B=0 3=POWERUP2: D=1 S=1 B=0 4=POWERUP_DONE: D=1 S=1 B=1 5=POWERDOWN0: D=1 S=1 B=1 6=POWERDOWN1: D=1 S=1 B=0 7=POWERDOWN2: D=1 S=0 B=0 8=POWERDOWN_DELAY: D=0 S=0 B=0 Ignore powerup request 9=POWERDOWN_DONE: D=0 S=0 B=0

LVTMA_BL_MOD_CNTL - RW - 32 bits -, GpuF0MMReg:0x7F94

Field Name	Bits	Default	Description
LVTMA_BL_MOD_EN	0	0x0	0=Disable LCD backlight modulation 1=Enable LCD backlight modulation
LVTMA_BL_MOD_LEVEL	15:8	0x0	
LVTMA_BL_MOD_RES	23:16	0xff	

LVTMA_TRANSMITTER_ENABLE - RW - 32 bits -, GpuF0MMReg:0x7F04			
Field Name	**Bits**	**Default**	**Description**
LVTMA_LNK0EN	0	0x0	LVTMA link0 data channel 0 enable (ICH0EN)(set to 1 whenever LVTM is enabled)
LVTMA_LNK1EN	1	0x0	LVTMA link0 data channel 1 enable (ICH1EN)(set to 1 whenever LVTM is enabled)
LVTMA_LNK2EN	2	0x0	LVTMA link0 data channel 2 enable (ICH2EN)(set to 1 whenever LVTM is enabled)
LVTMA_LNK3EN	3	0x0	LVTMA link0 data channel 3 enable (ICH3EN)(set to 1 whenever LVTM is enabled)
LVTMA_LNK4EN	4	0x0	LVTMA link0 data channel 4 enable (ICH4EN)(set to 1 when LVTM is enabled and in 24bpp LVDS mode)
LVTMA_LNK5EN	5	0x0	LVTMA link1 data channel 6 enable (ICH5EN)(set to 1 when LVTM is enabled and in dual-link mode)
LVTMA_LNK6EN	6	0x0	LVTMA link1 data channel 7 enable (ICH6EN)(set to 1 when LVTM is enabled and in dual-link mode)
LVTMA_LNK7EN	7	0x0	LVTMA link1 data channel 8 enable (ICH7EN)(set to 1 when LVTM is enabled and in dual-link mode)
LVTMA_LNK8EN	8	0x0	LVTMA link1 data channel 5 enable (ICH8EN)(set to 1 when LVTM is enabled and in LVDS dual-link mode)
LVTMA_LNK9EN	9	0x0	LVTMA link1 data channel 9 enable (ICH9EN)(set to 1 when LVTM is enabled and in 24bpp LVDS dual-link mode)
LVTMA_LNKEN_HPD_MASK	16	0x0	0=Disallow 1=Allow override of LVTMA_LNKxEN by HPD on disconnect 0=Result from HPD circuit can not override LVTMA_LNKxEN 1=Result from HPD circuit overrides LVTMA_LNKxEN on disconnect

LVTMA_LOAD_DETECT - RW - 32 bits -, GpuF0MMReg:0x7F08			
Field Name	**Bits**	**Default**	**Description**
LVTMA_LOAD_DETECT_ENABLE	0	0x1	0=Disable 1=Enable LVTMA macro load detect functionDrives IMSEN macro inputNote: macro doesn't currently have this function, but leave register or placeholder here for future implementations
LVTMA_LOAD_DETECT (R)	4	0x0	From LVTMA macro load detect output 0=No load detected 1=Load detectedNote: macro doesn't currently have this function, but leave register or placeholder here for future implementations
RTL support for this feature is included although LVTM macro doesn't support it yet			

LVTMA_MACRO_CONTROL - RW - 32 bits -, GpuF0MMReg:0x7F0C			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PLL_CP_GAIN	5:0	0x3	LVTMA PLL charge-pump gain control. Go to IPPLCP(5:0) pins of LVTMA macro.
LVTMA_PLL_VCO_GAIN	13:8	0x4	LVTMA PLL VCO gain control. Go to IPPLVG(5:0) pins of LVTMA macro.
LVTMA_PLL_DUTY_CYCLE	19:16	0x2	LVTMA PLL duty cycle control. Go to IPPLDC(1:0) pins of LVTMA macro.
LVTMA_PLL_LFCAP_ADJ	23:20	0x0	
LVTMA_IPLT	28:24	0x0	Reserved pins for lvtm macro
LVTMA_ICOSEL	31	0x0	PLL ICO select

LVTMA_TRANSMITTER_CONTROL - RW - 32 bits -, GpuF0MMReg:0x7F00			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PLL_ENABLE	0	0x0	LVTMA transmitter PLL enable. 0=LVTMA Transmitter PLL is disabled 1=LVTMA Transmitter PLL is enabled
LVTMA_PLL_RESET	1	0x1	LVTMA transmitter PLL reset. PLL will start the locking acquisition process once this becomes low.
LVTMA_IDSCKSEL	4	0x1	0=LVTM Transmitter uses pclk_lvtma (IPIXCLK) 1=LVTM Transmitter uses pclk_lvtma_direct (IDCLK)
LVTMA_BGSLEEP	5	0x0	LVTMA Bandgap macro disable. Set to 0 for normal operation (hardware will enable the macro whenever LVTMA is active), 1 to turn the bandgap macro off regardless of LVTMA status.Note that LVTMA shares the bandgap macro with DACB. For the shared macro either DACB or LVTMA can turn the macro on. Set to 0 in LVDS mode, 1 in TMDS mode. 0=Normal operation 1=Disable bandgap
LVTMA_IDCLK_SEL	6	0x0	0=Use single ended clock selection from LVTMA_IDSCKSEL 1=Use differential post divider input from DPLL
LVTMA_TMCLK	8	0x0	(Only bit0 is used in LVTM macro) For macro debug only
LVTMA_TMCLK_FROM_PADS	13	0x0	0=Input to ITMCLK pins on macro come from LVTMA_TMCLK field 1=Input to ITMCLK pins on macro come from pads
LVTMA_TDCLK	14	0x0	For macro debug only
LVTMA_TDCLK_FROM_PADS	15	0x0	0=Input to ITDCLK pin on macro comes from LVTMA_TDCLK field 1=Input to ITDCLK pin on macro comes from pads
LVTMA_BYPASS_PLL	28	0x1	Controls ICHCSEL1 pin on LVTM macro 0=Coherent mode: transmitted clock is PLL output 1=Incoherent mode: transmitted clock is PLL input
LVTMA_USE_CLK_DATA	29	0x0	Controls ICHCSEL2 pin on LVTM macro. Use to determine whether clock comes from PLL output or serialized LVTMA_CLK_PATTERN. See macro spec for recommended settings in TMDS and LVDS modes 0=Use serialized data (LVTMA_CLK_PATTERN) as clock 1=Use clock selected by LVTMA_BYPASS_PLL (ICHCSEL1)
LVTMA_MODE	30	0x0	
LVTMA_INPUT_TEST_CLK_SEL	31	0x0	Controls ITCLKSEL pin on LVTM macro

LVTMA_REG_TEST_OUTPUT - RW - 32 bits -, GpuF0MMReg:0x7F10			
Field Name	**Bits**	**Default**	**Description**
LVTMA_REG_TEST_OUTPUT (R)	9:0	0x0	From LVTMA macro OTDAT(9:0) outputs
LVTMA_OTEST (R)	13:12	0x0	From LVTMA macro OTEST(1:0) outputs
LVTMA_TEST_CNTL	21:16	0x0	Drives LVTMA macro ITEST(5:0) control bits (for debug only)

LVTMA_TRANSMITTER_DEBUG - RW - 32 bits -, GpuF0MMReg:0x7F14			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PLL_DEBUG	7:0	0x0	Drives ITPL pins on LVTMA macro (This functionality does not exist - pins are unconnected)
LVTMA_TX_DEBUG	11:8	0x0	Drives ITX pins on LVTMA macro (This functionality does not exist - pins are unconnected)
Reserved for debugging purposes			

LVTMA_TRANSMITTER_ADJUST - RW - 32 bits -, GpuF0MMReg:0x7F18			
Field Name	**Bits**	**Default**	**Description**
LVTMA_TXOP	4:0	0x0	Transmitter opam adjustment
LVTMA_NTXVS	13:8	0x0	Bias ccurrent control for output driver for n current source
LVTMA_PTXVS	20:16	0x0	Bias ccurrent control for output driver for p current source
LVTMA_PTXSR	23:21	0x0	
LVTMA_TXT	28:24	0x0	Reserved for transmitter
LVTMA_PUDSEL	30	0x0	Output driver pull-down selection
LVTMA_REFSEL	31	0x0	Current source selft bias selection
LVTM macro transmitter adjustment control in split mode			

LVTMA_PREEMPHASIS_CONTROL - RW - 32 bits -, GpuF0MMReg:0x7F1C			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PREMPHEN	0	0x0	Pre-emphasi enable
LVTMA_PREMCHSEL	2	0x0	Pre-emphasi clock channel selection
LVTMA_PREMPH_DV	7:4	0x0	Pre-emphasi pulse height control
LVTMA_PREMPH_DT	15:12	0x0	Pre-emphasi pulse width control
LVTMA_NTXSPREM	24:20	0x0	Pre-emphasi n-bias control
LVTMA_PREMPHEN_SEL	30:28	0x0	
LVTM macro pre-emphasis control			

2.12 Northbridge Memory Controller Indirect Registers

MC_SYSTEM_STATUS - RW - 32 bits - NBMCIND:0x0			
Field Name	**Bits**	**Default**	**Description**
MC_SYSTEM_IDLE (R)	0	0x0	Indicates that there are no pending or in-process memory requests. This includes all pending or in-process requests to system memory. 0=Not Idle 1=Idle
MC_SEQUENCER_IDLE (R)	1	0x0	Indicates that there are no pending or in-process frame buffer requests. This does not include status on pending or in-process requests to system memory. 0=Not Idle 1=Idle
MC_ARBITER_IDLE (R)	2	0x0	Indicates that there are no pending or in-process frame buffer requests. This does not include status on pending or in-process requests to system memory. 0=Not Idle 1=Idle
MC_SELECT_PM (R)	3	0x0	Memory power management selection read back
MC_STATUS_15_4 (R)	15:4	0x0	
MCA_INIT_EXECUTED (R)	16	0x0	Channel A SDRAM Init in Process Indicates that the last MCA_INIT_EXECUTE operation has completed for the A channel. Note: Do not inititiate a new MCA_INIT_EXECUTE operation until 'Ready' is indicated. 0=SDRAM Init in Process 1=Ready
MCA_IDLE (R)	17	0x0	Channel A memory controller idle. 0=Not idle (busy) 1=Idle (not busy)
MCA_SEQ_IDLE (R)	18	0x0	Channel A memory controller sequencer idle 0=Not idle (busy) 1=Idle (not busy)
MCA_ARB_IDLE (R)	19	0x0	Channel A memory controller arbiter idle 0=Not idle (busy) 1=Idle (not busy)
MC_STATUS_31_20 (R)	31:20	0x0	
Memory controller system status			

MC_GENERAL_PURPOSE - RW - 32 bits - NBMCIND:0x1			
Field Name	**Bits**	**Default**	**Description**
MC_STARTUP	0	0x0	Setting this bit forces the MC's SDRAM mode state machine from the initial power-on state into the 'operating' state. This bit needs to be set after initial power up, before the system memory can be accessed.
MC_RESTART	1	0x0	Setting this bit forces the MC's SDRAM mode state machine from the initial power-on state into the 'parked' state. This bit needs to be set after initial power up if the SDRAM is in self-refresh mode after a 'suspend-to-RAM' operation. After the mode state machine has reached the 'parked' state, the memory will be taken out of 'self-refresh' as soon as the hardware signal DC_STOP has been deasserted and the state machine will transition into the 'operating' state.
MC_POWERED_UP	2	0x0	All clocks ready. This bit must be set on power up after initializing all clocks in order to procede with MC initialization. When 0, force CKE low, and tristate all other signals.
MC_POWERED_UP2	3	0x0	All clocks ready. This bit must be set after power up, on self refresh exit, after initializing all clocks in order to procede with MC initialization. When 0, force CKE low, and tristate all other signals.
MC_PWRDN_MODE	5:4	0x0	Selects the source for the power down event 0=DC_STOP/SUSTAT 1=CPU Special Cycle (AMD) 2=Both 3=None
MC_POWER_DOWN	6	0x0	Setting this bit forces the MC's SDRAM mode state machine from the 'operating' state into the 'parked' state. The parking sequence takes a certain time and the processor needs to monitor the state machine to make sure that the 'parked' state has been reached before the power to the NB core is removed.
MC_GFX_PWRDN_ENABLE	7	0x0	Enables power down for external graphics
MC_SUSPEND_DISABLE	8	0x0	Disables suspend 0=Suspend enabled 1=Suspend disabled
MC_SUSPEND_TRISTATE	9	0x1	Enables tristate in suspend 0=Do not tristate in suspend 1=Tristate in suspend
MC_SUSPEND_CLEAN_MC	10	0x0	When going to suspend, clean MC (no stuck requests in MC)
MC_SUSPEND_DYNAMIC	11	0x0	Dynamic self refresh when the CPU is in S3 and the display is in shutter mode
MC_SUSPEND_DELAY	15:12	0x8	Delay to enter self refresh when the CPU is in S3 and the display is in shutter mode (x4 clocks)
MC_TEST_OUT	16	0x0	Test clocks out on MC 0=Nominal 1=Test
MC_DVO_OUT	17	0x0	DVO out on MC 0 = Nominal 1 = DVO
MC_VMODE	18	0x1	Memory interface receiver voltage 0=Interface voltage 1=Transfer voltage
MC_SUSPEND_DO_NOT	19	0x0	Disables suspend self refresh 0=Suspend self refresh 1=Suspend do not self refresh

MC_TCLKS	23:20	0x1	Memory clock settling time. Memory spec. Register x16 clocks
MC_TDLLR	27:24	0x8	DLL reset pulse. 1us. Register x64 clocks
MC_TDLLL	31:28	0x8	DLL lock time. 500 clock. Register x64 clocks
Memory controller general purpose register			

MC_GENERAL_PURPOSE_2 - RW - 32 bits - NBMCIND:0x2			
Field Name	**Bits**	**Default**	**Description**
RESERVED0	8:0	0x0	
OPTIMIZE_ZERO_BE_SP	9	0x1	Drop zero-byte writes in sideport if set
MEM_SUS_STAT_EN	10	0x0	When TVCLKIN is used as SUS_STATb signal this bit must be set to 1; otherwise, this bit is set to 0
MEM_D3_RBS_IDLE	11	0x0	
MEM_D3_MCB_IDLE	12	0x0	
RESERVED13	15:13	0x0	
REG_RD_DELAY	18:16	0x3	
STUTTER_IGNORE_C3	19	0x0	
MCLK_SRC_USE_MPLL	20	0x0	
RESERVED21	28:21	0x0	
DBL_FLOP_EN	29	0x0	
DEBUGBUS_CYCLE_EN	30	0x0	Enables to cycle all available debug bus signals every 16 clocks 0=Disable 1=Enable
MC_INIT_COMPLETE	31	0x0	As long as this bit is '0', the MC will not accept requests from the clients. This is used primarily to block requests when the MC might mishandle them, such as when the FB or AGP apertures are undefined or unstable. 0=Register Initialization Not Complete 1=Register Initialization Complete
Memory controller general purpose register			

MC_GENERAL_PURPOSE_3 - RW - 32 bits - NBMCIND:0x3			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	

MC_IMP_CTRL_CNTL - RW - 32 bits - NBMCIND:0x4			
Field Name	**Bits**	**Default**	**Description**
MC_IC_UPDATE_RATE	4:0	0x18	Update rate MCLK*2**n 0x0=Minimum 0x1F=Maximum
RESERVED5	7:5	0x0	
MC_IC_SAMPLE_RATE	12:8	0x10	Sample rate MCLK*2**n 0x0=Minimum 0x1F=Maximum
RESERVED13	15:13	0x0	
MC_IC_SAMPLE_SETTLE	19:16	0x8	Sample settle MCLK*2**n 0x0=Minimum 0xF=Maximum
MC_IC_INC_THRESHOLD	23:20	0x8	Number of over samples to increase strength 0x0=0 0xF=15
MC_IC_DEC_THRESHOLD	27:24	0x8	Number of under samples to decrease strength 0x0=0 0xF=15
MC_IC_OSC	28	0x0	Impedance controller oscillation mode 0=Stay at higher strength when oscillate 1=Oscillate when oscillate
MC_IC_SUSPEND	29	0x0	Impedance controller on/off in self refresh 0=Impedance controller on in self refresh 1=Impedance controller off in self refresh
RESERVED30	30	0x0	
MC_IC_ENABLE	31	0x0	Impedance controller enable 0=Off 1=On
Memory controller impedance controller setting			

MC_IMP_CTRL_REF - RW - 32 bits - NBMCIND:0x5			
Field Name	**Bits**	**Default**	**Description**
MC_STRENGTH_N_REF	3:0	0xb	Reference N strength 0x0=Weakest 0xF=Strongest
MC_STRENGTH_P_REF	7:4	0xb	Reference P strength 0x0=Weakest 0xF=Strongest
MC_STR_READ_BACK_N_REF (R)	11:8	0x0	Reference N strength read back 0x0=Weakest 0xF=Strongest
MC_STR_READ_BACK_P_REF (R)	15:12	0x0	Reference P strength read back 0x0=Weakest 0xF=Strongest
MC_IC_N_LOCKED (R)	16	0x0	Impedance controller N strength locked read back 0x0=Not locked 0x1=Locked
MC_IC_P_LOCKED (R)	17	0x0	Impedance controller P strength locked read back 0x0=Not locked 0x1=Locked
MC_IC_N_OSCILLATION (R)	18	0x0	Impedance controller N strength oscillation read back 0x0=No oscillation 0x1=Oscillation

MC_IC_P_OSCILLATION (R)	19	0x0	Impedance controller P strength oscillation read back 0x0=No oscillation 0x1=Oscillation
RESERVED20	31:20	0x0	
Memory controller impedance controller reference strength and read back			

MC_MPLL_CONTROL - RW - 32 bits - NBMCIND:0x6			
Field Name	**Bits**	**Default**	**Description**
MPLL_CAL_TRIGGER	0	0x0	Memory PLL calibration trigger. Set from 0 to 1 to start calibration
MPLL_LOCKED (R)	1	0x0	Memory PLL locking read back status. 0=No lock 1=PLL lock
MPLL_SKEW1X_CORE	4:2	0x0	Not used
MPLL_SKEW2	7:5	0x0	2X output clock (O2X) skew control
MPLL_SKEW1	10:8	0x0	1X output clock (O1X) skew control
MPLL_SKEW_DLY	14:11	0x0	Not used
MPLL_DLL_CLEN	15	0x0	Not used
MPLL_DLL_PWDN	16	0x0	Core-clock tree cancellation DLL power-down
MPLL_SKEW_TREE	19:17	0x0	Not used
MPLL_VCOREF	23:20	0x0	VCO input reference voltage setting
MPLL_CALREF	27:24	0x0	2nd VCO input reference voltage setting
MPLL_BYPASS	28	0x0	Bypass mode enable for test clocks 0=Disable 1=Enable
MPLL_POWERDOWN_DLY	30:29	0x0	Not used 0=1 ms 1=2 ms 2=4 ms 3=8 ms
MPLL_POWERDOWN	31	0x0	Power-down Enable. 0=Normal operation 1=Power down
This register controls the Memory PLL. The divider fields will assume default values based on power-on-strap options. To change the frequency, this register can be written by the CPU.			

MC_MPLL_CONTROL2 - RW - 32 bits - NBMCIND:0x7			
Field Name	**Bits**	**Default**	**Description**
MPLL_FBDIV	8:0	0x0	Comprises 3-bit CMOS divider followed by 6-bit CMOS divider. Bits [2:0] control the 3-bit CMOS divider, and bits [8:3] control the 6-bit CMOS divider.
MPLL_REFDIV	13:9	0x0	Reference clock input divider ratio from 1 to 32.
MPLL_POSTDIV	15:14	0x0	Divide by 1/2/3/4 post divider ratio.
MPLL_CP	19:16	0x0	Charge-pump current setting.
MPLL_VCO_MODE	21:20	0x0	VCO mode setting
RESERVED	23:22	0x0	
MPLL_DLL_FRE_SEL	27:24	0x0	Not used
MPLL_LF_MODE	31:28	0x0	Loop filter mode setting.
This register controls the memory PLL frequency.			

MC_MPLL_CONTROL3 - RW - 32 bits - NBMCIND:0x8			
Field Name	**Bits**	**Default**	**Description**
MPLL_REF_DELAY	1:0	0x0	Not used
MPLL_VCO_DELAY	3:2	0x0	Not used
MPLL_CTL	8:4	0x0	Misc. PLL programming bits. IPLL_CTL[4] enables calibration override. When IPLL_CTL[4] = 0, the four calibration bits are set by the calibration loop. When IPLL_CTL[4]=1, the four bits are set through IPLL_CTL[3:0]
MPLL_IOBUFSEL	9	0x1	Not used
MPLL_REFCLK_SEL	10	0x0	Reference clock input select. 0 chooses IREF_1X 1 chooses ITCLK_1X
MPLL_PLLBIAS	12:11	0x1	Bias current trim. IBIAS[1:0] 00 = -8% 01 = 0% 10 = +12% 11 = +25%
MPLL_SPARE	17:13	0x0	Bits [4:0]=Spare pins reserved for PLL. Bits [7:5]=Programmable current control for SCL for PLL 000 = -20% 001 = -10% 010 = 0% (default) 011 = 10% 100 = 20% 101 = 30% 110 = 40% 111 = 50% Bits [9:8]=Programmable current control for SCL for DLL 00 = 0% (default) 01 = 10% 10 = 20% 11 = 30%
MPLL_SCLBIAS	20:18	0x0	
MPLL_DLLBIAS	22:21	0x0	
MPLL_REFSEL	23	0x0	
MPLL_SPARE0	27:24	0x0	
MPLL_MODE (R)	31:28	0x0	VCO operating mode status flags
This register controls the memory PLL.			

MC_MPLL_FREQ_CONTROL - RW - 32 bits - NBMCIND:0x9			
Field Name	**Bits**	**Default**	**Description**
MPLL_PM_EN	0	0x0	Dynamic MCLK switch enable
MPLL_FREQ_SEL	1	0x0	0=Use normal MPLL registers to set memory frequency 1=Use PM MPLL registers to set memory frequency
DISP_BLANK_CNTL	3:2	0x2	0=No blanking during frequency switch 1=Blank assertion only 2=Blank assertion and deassertion 3=Register control blank
DISP_BLANK_VAL	4	0x0	Register control blank value
MEM_SELF_REFRESH_ONLY	5	0x0	0=Self refresh is followed by frequency switching 1=Self refresh only
PM_SWITCHMCLK_BUSY (R)	6	0x0	0=MCLK is stable 1=MCLK switching is in progress
PM_FREQ_CNTL_RESET	7	0x0	Reset dynamic MCLK state machine
PM_MPLL_CP	11:8	0x0	PM mode Charge-pump current setting
PM_MPLL_VCO_MODE	13:12	0x0	PM mode VCO mode setting

RESERVED14	15:14	0x0	
PM_MPLL_LF_MODE	19:16	0x0	PM mode Loop filter mode setting.
PM_MPLL_DLL_FRE_SEL	23:20	0x0	Not used
RESERVED24	27:24	0x0	
MPLL_SLOWMCLK	28	0x0	0=MCLK is equal to or faster than CCLK in normal mode 1=MCLK is slower than CCLK in normal mode
PM_MPLL_SLOWMCLK	29	0x0	0=MCLK is equal to or faster than CCLK in PM mode 1=MCLK is slower than CCLK in PM mode
DLL_CORE_TEST_CLK	30	0x0	Bring it out on channel B CKE 3
RESERVED31	31	0x0	

MC_MPLL_SEQ_CONTROL - RW - 32 bits - NBMCIND:0xA			
Field Name	**Bits**	**Default**	**Description**
MPLL_RESET_PULSE_WIDTH	3:0	0x1	Not used
MDLL_RESET_PULSE_WIDTH	7:4	0x1	Not used
MPLL_CAL_S_TIME	11:8	0x4	VCO calibration setup time = MPLL_CAL_S_TIME * 512 * 10 ns
MPLL_CAL_H_TIME	15:12	0x5	VCO calibration hold time = MPLL_CAL_H_TIME * 4 * 10 ns
MPLL_LOCK_TIME	23:16	0x50	MPLL lock time = MPLL_LOCK_TIME * 256 * 10 ns
MDLL_LOCK_TIME	31:24	0x50	MDLL lock time = MDLL_LOCK_TIME * 256 * 10 ns

MC_MPLL_DIV_CONTROL - RW - 32 bits - NBMCIND:0xB			
Field Name	**Bits**	**Default**	**Description**
PM_MPLL_FBDIV	8:0	0x0	PM mode feedback divider
PM_MPLL_REFDIV	13:9	0x0	PM mode reference divider
PM_MPLL_POSTDIV	15:14	0x0	PM mode post divider
MPLL_DLL_CPP	17:16	0x0	Control charge pump source current 0=Off 1=On
MPLL_DLL_CPN	19:18	0x0	Control charge pump sink current 0=Off 1=On
MPLL_DLL_CPCAL_SEL	20	0x1	Selects the calibration or the manual setting for the charge pump current mirror 0=Select manual setting 1=Select calibration setting
RESERVED	31:21	0x0	Bits [1:0]=Memory DLL reference clock skew control Bits [3:2]=Memory DLL feedback clock skew control Bit [4]: 1=Enable pre-clock tree PLL clock on MEM DQ14 pad Bit [5]: 1=Enable post-clock tree PLL clock on MEM DQ15 pad

MC_MCLK_CONTROL - RW - 32 bits - NBMCIND:0xC			
Field Name	**Bits**	**Default**	**Description**
CLKGATE_DIS_MCLK_SEQ	0	0x1	Disables clock gating for MCLK going to seq, arb_seq_buf, mc_seq_dissect, rbs_seq, mc_rddata_capture
CLKGATE_DIS_SCLK_BARB	1	0x1	Disables clock gating for SCLK going to mcb_arb, rbs_htiu
CLKGATE_DIS_SCLK_DARB	2	0x1	Disables clock gating for SCLK going to mcd_arb, rbs_seq, arb_seq_buf, srbm_intfc, cfg_intfc
CLKGATE_DIS_LCLK	3	0x1	Disables clock gating for LCLK going to mcb_arb, rbs_htiu
CLKGATE_DIS_MCLK_IO	4	0x1	Disables clock gating for MCLK going to io
RESERVED5	23:5	0x0	
DELAY_SET_MCLK	28:24	0xf	Extends the delay timer for MCLK1X branches from 0 to 32 clocks
RESERVED29	31:29	0x0	

NB_MEM_CH_CNTL0 - RW - 32 bits - NBMCIND:0xD			
Field Name	**Bits**	**Default**	**Description**
INTERLEAVE_MODE	1:0	0x0	This field defines the interleave mode between memory channels. In 'Coarse interleaved' mode the primary channel, which is SP, occupies the lower part of system memory address space. In 'Interleaved' mode memory access alternates between both channels (every 128 bytes or 256 bytes). 0=Single Channel 1=Fine Interleaved 2=Reserved 3=Coarse Interleaved
PRIMARY_CHANNEL	2	0x1	The primary channel will be SP always under dual-channel configuration. The only case that UMA would be the primary channel is under the UMA-only configuration. The memory controller uses that information to properly interleave accesses between channels. 0=Channel A 1=Channel B
NUMBER_CHANNEL	3	0x0	This specifies single/dual memory channel mode 0=One channel 1=Two channels
BANK_2_MAP	7:4	0x6	Memory bank bit 2 mapping, address bits [20:7] can be used, for values being 0 to 13. The default value is 6, meaning address bit [13] is used as bank[0]
BANK_0_MAP	15:12	0x4	Memory bank bit 0 mapping, address bits [20:7] can be used, for values being 0 to 13. The default value is 4, meaning address bit [11] is used as bank[0]
BANK_1_MAP	19:16	0x5	Memory bank bit 1 mapping, address bits [20:7] can be used, for values being 0 to 13. The default value is 5, meaning address bit 12 is used as bank[1]
INTERLEAVE_START	31:20	0x0	The address space below Interleave-Start will be mapped to the Primary-Channel and will be treated as if operating in single channel mode.
Memory Control channel register0			

NB_MEM_CH_CNTL1 - RW - 32 bits - NBMCIND:0xE			
Field Name	**Bits**	**Default**	**Description**
INTERLEAVE_END	11:0	0x0	The address space above Interleave-End will be mapped to the Secondary-Channel, which is UMA, and will be treated as if operating in single channel mode.
INTERLEAVE_RATIO	27:12	0xaaaa	This 16-bit register defines the ratio of arbitration between SP and UMA. 0 means that SP will win the arbitration and 1 means that UMA will win the arbitration. For example, the value 1111111111100000 will have SP being selected for 5 consecutive times and UMA being selected for the rest of the 11 times.
Memory Control channel register1			

NB_MEM_CH_CNTL2 - RW - 32 bits - NBMCIND:0xF			
Field Name	**Bits**	**Default**	**Description**
K8_INTERLEAVE_SIZE	7:0	0x0	Specifies the interleave size of FB on the UMA side. The unit is 1Mbyte.
Memory Control channel register2			

MC_FB_LOCATION - RW - 32 bits - NBMCIND:0x10			
Field Name	**Bits**	**Default**	**Description**
MC_FB_START	15:0	0x0	Start of local frame buffer section in the internal address space. Note: Bits [7:0] of this field are hardwired to 0.
MC_FB_TOP	31:16	0xff	Top of local frame buffer section in the internal address space. Note: Bits [7:0] of this field are hardwired to 1.
This register defines the base address and the top of memory of the reserved memory area that is allocated to the frame buffer			

K8_FB_LOCATION - RW - 32 bits - NBMCIND:0x11			
Field Name	**Bits**	**Default**	**Description**
K8_FB_START	31:0	0x0	Indicates the start of the frame buffer in the K8's system memory. The frame buffer in system memory is not allowed to span across 4G boundaries. Note: Bits [4:0] of this field are hardwired to 0.
Start of frame buffer in shared K8 system memory			

MC_MISC_UMA_CNTL - RW - 32 bits - NBMCIND:0x12			
Field Name	**Bits**	**Default**	**Description**
K8_40BIT_ADDR_EXTENSION	7:0	0x0	Upper fixed 8-bits of the 40-bit K8 address space. All address directed at the K8 frame buffer memory will be prefixed with this value
BANKGROUP_SEL	14:8	0x0	Register to select whether to use bank, rank, or channel bits to form bank group in UMA arb. Bits [1:0] controls new_bank[0] 2'b00=old_bank[0] 2'b01=rank[0] 2'b10=rank[1] 2'b11=channel Bits [3:2] controls new_bank[1] 2'b00=old_bank[1] 2'b01=rank[0] 2'b10=rank[1] 2'b11=channel Bits [5:4] controls new_bank[2] 2'b00=old_bank[2] 2'b01=rank[0] 2'b10=rank[1] 2'b11=channel Bit [6] controls whether to match the channel in determining the page match in the tail manager
CNTL_SPARE	30:15	0x0	
SIDE_PORT_PRESENT_W (W)	31	0x0	0=Sideport not present 1=Sideport present
SIDE_PORT_PRESENT_R (R)	31	0x0	0=Sideport not present 1=Sideport present

MC_UMA_ADDRESS_SWIZZLE_0 - RW - 32 bits - NBMCIND:0x13			
Field Name	**Bits**	**Default**	**Description**
A6_MAP	3:0	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved

A7_MAP	7:4	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved
A8_MAP	11:8	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved
A9_MAP	15:12	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved

A10_MAP	19:16	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved
A11_MAP	23:20	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved
A12_MAP	27:24	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved

A13_MAP	31:28	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved

MC_UMA_ADDRESS_SWIZZLE_1 - RW - 32 bits - NBMCIND:0x14			
Field Name	**Bits**	**Default**	**Description**
A14_MAP	3:0	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved
A15_MAP	7:4	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved

A16_MAP	11:8	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved
A17_MAP	15:12	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved
A18_MAP	19:16	0x0	0=No swap 1=A6 2=A7 3=A8 4=A9 5=A10 6=A11 7=A12 8=A13 9=A14 10=A15 11=A16 12=A17 13=A18 14=Reserved 15=Reserved
SPARE_ADDRESS	31:20	0x0	

MC_CREDITS_CONTROL - RW - 32 bits - NBMCIND:0x15			
Field Name	**Bits**	**Default**	**Description**
RBS_SEQ_XB_CREDITS_LCL	3:0	0x8	Number of credits for rbs_seq to xb(local) interface
RBS_SEQ_XB_CREDITS_RB	7:4	0x8	Number of credits for rbs_seq to xb(remote) interface
RBS_HTIU_XB_CREDITS_LCL	11:8	0x8	Number of credits for rbs_htiu to xb(local) interface
RBS_HTIU_XB_CREDITS_RB	15:12	0x8	Number of credits for rbs_htiu to xb(remote) interface
VM_ISOC_DISP_CREDITS	19:16	0xc	
VM_ISOC_GENERIC_CREDITS	23:20	0xc	
ISOC_HTIU_CREDITS	27:24	0x8	
Control for credit/debit interfaces			

MC_ISOC_CONTROL - RW - 32 bits - NBMCIND:0x16			
Field Name	**Bits**	**Default**	**Description**
REG_NON_SNOOP_TO_UMA	0	0x1	Non-snoop GART requests go to HTIU/UMA instead of BIF
REG_DMIF_TO_ISOC	1	0x1	Routes requests from this client to isochronous UMA request channel
REG_DRMDMA_TO_ISOC	2	0x0	Routes requests from this client to isochronous UMA request channel
REG_CB_TO_ISOC	3	0x0	Routes requests from this client to isochronous UMA request channel
REG_DB_TO_ISOC	4	0x0	Routes requests from this client to isochronous UMA request channel
REG_SH_TO_ISOC	5	0x0	Routes requests from this client to isochronous UMA request channel
REG_CP_TO_ISOC	6	0x0	Routes requests from this client to isochronous UMA request channel
REG_VGT_TO_ISOC	7	0x0	Routes requests from this client to isochronous UMA request channel
REG_TC_TO_ISOC	8	0x0	Routes requests from this client to isochronous UMA request channel
REG_SMX_TO_ISOC	9	0x0	Routes requests from this client to isochronous UMA request channel
REG_MCIF_TO_ISOC	10	0x1	Routes requests from this client to isochronous UMA request channel
REG_HDP_TO_ISOC	11	0x0	Routes requests from this client to isochronous UMA request channel
REG_UMC_TO_ISOC	12	0x0	Routes requests from this client to isochronous UMA request channel
REG_VMC_TO_ISOC	13	0x1	Routes requests from this client to isochronous UMA request channel
REG_SEM_TO_ISOC	14	0x0	Routes requests from this client to isochronous UMA request channel
REG_UVD_TO_ISOC	15	0x0	Routes requests from this client to isochronous UMA request channel
REG_AVP_TO_ISOC	16	0x0	Routes requests from this client to isochronous UMA request channel
REG_MC_HTIU_ISOC_CREDITS	20:17	0x7	
Control register for routing clients to isoc UMA request channel			

MC_ISOC_ARB_CNTL - RW - 32 bits - NBMCIND:0x17			
Field Name	**Bits**	**Default**	**Description**
MCBR_BURST_COUNT	3:0	0x4	When MCBR FIFO wins arbitration it ensures that it generates a burst of MCBR_BURST_COUNT requests
DMIFR_PRI_ON_STALL	4	0x1	Includes dmifr stall signal in priority generation
MCIFR_PRI_ON_STALL	5	0x0	Includes mcifr stall signal in priority generation
UVDR_PRI_ON_STALL	6	0x0	Includes uvdr stall signal in priority generation
VMCR_PRI_ON_STALL	7	0x1	Includes vmcr stall signal in priority generation
MC_DISP0R_INIT_LAT	11:8	0x0	Raises the service priority after VALUE * 16 MCLKs to prevent staleness of DMIF client
MC_MCBR_INIT_LAT	16:12	0x1	Raises the service priority after VALUE * 8 MCLKs to prevent staleness of VMC, UVD, and MCIF clients
MC_MCDWR_INIT_LAT	20:17	0x0	Raises the service priority after VALUE * 16 MCLKs to prevent staleness of MCDW clients
SAME_PAGE_PRIO	24:21	0xf	
GFXRD_BANK_LIMIT	29:25	0x8	Masking VALUE * 4 clocks for bank access
USE_FIX_ORDER	30	0x1	0=Round robbin arbitration is used in isoc channel for priority requests 1=Enable to use fix order arbitration in isoc channel for priority requests
USE_EFF_BASED	31	0x1	0=Round robbin arbitration is used in isoc channel for priority requests 1=Enable to use effeciency based arbitration in isoc channel for priority requests
Misc controls for isoc arbiter			

MC_ISOC_ARB_CNTL2 - RW - 32 bits - NBMCIND:0x18			
Field Name	**Bits**	**Default**	**Description**
DMIFR_PRI_THRESHOLD	7:0	0xf	dmifr priority threshold 0x00=Always 0xff=Never
MCIFR_PRI_THRESHOLD	15:8	0xff	mcifr priority threshold 0x00=Always 0xff=Never
UVDR_PRI_THRESHOLD	23:16	0xff	uvdr priority threshold 0x00=Always 0xff=Never
VMCR_PRI_THRESHOLD	31:24	0x1	vmcr priority threshold 0x00=Always 0xff=Never
Misc controls for isoc arbiter			

MC_ISOC_BW_LIM_WINDOW - RW - 32 bits - NBMCIND:0x19			
Field Name	**Bits**	**Default**	**Description**
ISOC_BW_LIM_WINDOW	31:0	0x0	Isoc bandwidth limiter window setting
Isoc bandwidth limiter window setting			

MC_ISOC_BW_LIM_MAX - RW - 32 bits - NBMCIND:0x1A

Field Name	Bits	Default	Description
ISOC_BW_LIM_MAX	31:0	0x0	Isoc bandwidth limiter window setting
Isoc bandwidth limiter maximum setting			

MC_ISOC_BW_LIM_CNTL - RW - 32 bits - NBMCIND:0x1B			
Field Name	**Bits**	**Default**	**Description**
ISOC_BW_LIM_DISP_IDLE_TIMER	15:0	0x0	
ISOC_BW_LIM_GLB_EN	16	0x0	
ISOC_BW_LIM_DISP_TIMER_EN	17	0x0	
ISOC_BW_LIM_CLK_EVENT_EN	18	0x0	
ISOC_BW_LIM_TX_EVENT_EN	19	0x0	
ISOC_BW_LIM_VF_EVENT_EN	20	0x0	
ISOC_BW_LIM_UVD_EVENT_EN	21	0x0	
ISOC_BW_LIM_DMIF_EVENT_EN	22	0x0	
ISOC_BW_LIM_THROT_EN	23	0x0	
Isoc bandwidth limiter control register			

MC_LATENCY_COUNT_CNTL - RW - 32 bits - NBMCIND:0x1C			
Field Name	**Bits**	**Default**	**Description**
MCB_CLIENT_SEL	3:0	0x0	Selects which clients to measure latency 4'b0000=DMIF 4'b0001=MCIF 4'b0010=HDP 4'b0011=Reserved 4'b0100=UMC 4'b0101=VMC 4'b0110=SEM 4'b0111=UVD 4'b1000=Reserved 4'b1001=AVP 4'b1010-4'b1111=Reserved
MCD_CLIENT_SEL	7:4	0x0	Selects which clients to measure latency 4'b0000=DRMDMA 4'b0001=CB0 4'b0010=DB0 4'b0011=SH 4'b0100=CP 4'b0101=Reserved 4'b0110=VGT 4'b0111=TC0 4'b1000=SMX 4'b1001-4'b1111=Reserved
RESERVED	30:8	0x0	
LATENCY_COUNT_EN	31	0x0	
Controls for latency counter (average latency is measured in performance counter events			

MCB_LATENCY_COUNT_EVENT_SP - R - 32 bits - NBMCIND:0x1D			
Field Name	**Bits**	**Default**	**Description**
MIN_LATENCY	15:0	0x0	Minimum latency during the period of enabling sclk performance counter events 0x84 and 0x85
MAX_LATENCY	31:16	0x0	Maximum latency during the period of enabling sclk performance counter events 0x84 and 0x85
Min/Max sideport latency readback from latency counter for clients in mcb tile			

MCB_LATENCY_COUNT_EVENT_BIF - R - 32 bits - NBMCIND:0x1E			
Field Name	**Bits**	**Default**	**Description**
MIN_LATENCY	15:0	0x0	Minimum latency during the period of enabling sclk performance counter events 0x84 and 0x85
MAX_LATENCY	31:16	0x0	Maximum latency during the period of enabling sclk performance counter events 0x84 and 0x85
Min/Max BIF path latency readback from latency counter for clients in mcb tile			

MCB_LATENCY_COUNT_EVENT_UMA - R - 32 bits - NBMCIND:0x1F			
Field Name	**Bits**	**Default**	**Description**
MIN_LATENCY	15:0	0x0	Minimum latency during the period of enabling sclk performance counter events 0x84 and 0x85
MAX_LATENCY	31:16	0x0	Maximum latency during the period of enabling sclk performance counter events 0x84 and 0x85
Min/Max UMA path latency readback from latency counter for clients in mcb tile			

MCD_LATENCY_COUNT_EVENT_SP - R - 32 bits - NBMCIND:0x20			
Field Name	**Bits**	**Default**	**Description**
MIN_LATENCY	15:0	0x0	Minimum latency during the period of enabling sclk performance counter events 0x84 and 0x85
MAX_LATENCY	31:16	0x0	Maximum latency during the period of enabling sclk performance counter events 0x84 and 0x85
Min/Max sideport latency readback from latency counter for clients in mcb tile			

MCD_LATENCY_COUNT_EVENT_BIF - R - 32 bits - NBMCIND:0x21			
Field Name	**Bits**	**Default**	**Description**
MIN_LATENCY	15:0	0x0	Minimum latency during the period of enabling sclk performance counter events 0x84 and 0x85
MAX_LATENCY	31:16	0x0	Maximum latency during the period of enabling sclk performance counter events 0x84 and 0x85
Min/Max BIF path latency readback from latency counter for clients in mcb tile			

MCD_LATENCY_COUNT_EVENT_UMA - R - 32 bits - NBMCIND:0x22			
Field Name	**Bits**	**Default**	**Description**
MIN_LATENCY	15:0	0x0	Minimum latency during the period of enabling sclk performance counter events 0x84 and 0x85
MAX_LATENCY	31:16	0x0	Maximum latency during the period of enabling sclk performance counter events 0x84 and 0x85
Min/Max UMA path latency readback from latency counter for clients in mcb tile			

MC_HTIU_GFX_RD_URGENT_CONTROL - RW - 32 bits - NBMCIND:0x23			
Field Name	**Bits**	**Default**	**Description**
MC_HTIU_GFX_RD_URGENT_CONTROL	31:0	0x11111111	Bits [7:0]=MC-HTIU read urgent threshold 0x00=Always urgent 0xFF=Never urgent) Bits [26:20]=Maximum dmif isoc reads allowed between citf and htiu isoc 0xEF=No limit Bit [28]=Force dmifr_isoc_inpipe signal Bit [29]=Force mcifr_isoc_inpipe signal Bit [30]=Force uvdr_isoc_inpipe signal Bit [31]=Force vmcr_isoc_inpipe signal

MC_HTIU_GFX_WR_URGENT_CONTROL - RW - 32 bits - NBMCIND:0x24			
Field Name	**Bits**	**Default**	**Description**
MC_HTIU_GFX_WR_URGENT_CONTROL	31:0	0x10	Bits [7:0]=MC-HTIU write urgent threshold 0x00=Always urgent 0xFF=Never urgent

MC_HTIU_ISOC_URGENT_CONTROL - RW - 32 bits - NBMCIND:0x25			
Field Name	**Bits**	**Default**	**Description**
MC_HTIU_ISOC_URGENT_CONTROL	31:0	0x10	Bit [0]=dmifr urgent on stall Bits [7:1]=dmifr urgency threshold Bit [8]=mcifr urgent on stall Bits [15:9]=mcifr urgency threshold Bit [16]=uvdr urgent on stall Bits [23:17]=uvdr urgency threshold Bit [24]=vmcr urgent on stall Bits [31:25]=vmcr urgency threshold

HT_CLMC_I - RW - 32 bits - NBMCIND:0x29			
Field Name	**Bits**	**Default**	**Description**
ACDCSel	0	0x0	Selects AC/DC link frequency setting
RegLMM	4:1	0x0	Sets LMM (default is LMM0)
RegLWup	7:5	0x0	Sets upstream LW (default is 8-bit)
RegLWdn	10:8	0x0	Sets downstream LW (default is 8-bit)
RegFreqAC	14:11	0x0	Sets AC link frequency (default is 200MHz)
RegFreqDC	18:15	0x0	Sets DC link frequency (default is 200MHz)
LMMSel	20:19	0x1	Selects LMM (default is LMM0)
LWSel	22:21	0x1	Selects Up/Down LW (default is CfgLW)
FreqSel	24:23	0x0	Selects link frequency (default is CfgFreq)
MaxUpLW	27:25	0x1	Max allowable Up LW (default is 16-bit)
MaxDnLW	30:28	0x1	Max allowable Down LW (default is 16-bit)
McuLMM_TimerSel	31	0x0	Uses MCU LMM timers instead

HT_CLMC_II - RW - 32 bits - NBMCIND:0x2A			
Field Name	**Bits**	**Default**	**Description**
MinUpLW	2:0	0x0	Min allowable Up LW (default is 4-bit)
MinDnLW	5:3	0x0	Min allowable Down LW (default is 4-bit)
ForceAssert	6	0x1	Forces extra LDTSTOP assertion
LdtStopBypassMode	8:7	0x0	Chooses conditions for full/bypass paths
LookAtInactiveRX	9	0x0	Includes inactive RX lanes in CILR
LookAtFBC	10	0x1	Includes FBC status
ForceAllowLdtStop	11	0x0	Forces AllowLdtStop high
ForceCILRAfterCDLR	12	0x0	Forces CILR after CDLR
BWEstmMode	14:13	0x0	Estimation mode
HT_CLMC_II_SPARE15	15	0x0	
UpLWStutterEn	16	0x1	Enables upstream stutter mode LW
DnLWStutterEn	17	0x1	Enables downstream stutter mode LW
LegacyStutterEn	18	0x1	Enables 'legacy' stutter mode to do disconnect
HtTwoBitEn	19	0x0	Considers 2-bit LW in BW estimation
HtFourBitEn	20	0x0	Considers 4-bit LW in BW estimation
UseProgMaxLW	21	0x0	Controls use of programmable max LW limit
BypassVblankWait	22	0x0	Controls the wait on Vblank during frequency updates
HT_CLMC_II_SPARE	31:23	0x0	

HT_ARB_I - RW - 32 bits - NBMCIND:0x2B			
Field Name	**Bits**	**Default**	**Description**
MaskedWriteCredits	3:0	0x0	Number of write credits to mask
MaxGFXReadRequests	11:4	0xff	Maximum number of outstanding GFX reads
IOCTimeoutThreshold	19:12	0xf	IOC timeout value
IOCTimeoutBurst	23:20	0x1	Number of IOC requests to send before resetting the IOC timeout counter
TargetReservedIsocCredits	31:24	0x7	Number of reserved Isoc credits

HT_ARB_II - RW - 32 bits - NBMCIND:0x2C			
Field Name	**Bits**	**Default**	**Description**
IsocReadBurstSize	4:0	0x8	Targets the number of Isoc reads before switching to non-Isoc reads
NormalReadBurstSize	9:5	0x8	Burst size for normal reads
AnyReadBurstSize	14:10	0x8	Burst size for any read
WriteBurstSize	19:15	0x8	Burst size for writes
HT_ARB_II_SPARE	31:20	0x0	

HT_FORCE_I - RW - 32 bits - NBMCIND:0x2D			
Field Name	**Bits**	**Default**	**Description**
ForcePostedToIsoc	31:0	0x0	

HT_FORCE_II - RW - 32 bits - NBMCIND:0x2E			
Field Name	**Bits**	**Default**	**Description**
ForceNonPostedToIsoc	31:0	0x0	

HT_FORCE_III - RW - 32 bits - NBMCIND:0x2F			
Field Name	**Bits**	**Default**	**Description**
ForceNonZeroSeqID	31:0	0x0	

CPU_DRAM0_CS0_BASE - RW - 32 bits - NBMCIND:0x30			
Field Name	**Bits**	**Default**	**Description**
CSEnable	0	0x1	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x0	

CPU_DRAM0_CS1_BASE - RW - 32 bits - NBMCIND:0x31			
Field Name	**Bits**	**Default**	**Description**
CSEnable	0	0x1	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x40	

CPU_DRAM0_CS2_BASE - RW - 32 bits - NBMCIND:0x32			
Field Name	**Bits**	**Default**	**Description**
CSEnable	0	0x0	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x80	

CPU_DRAM0_CS3_BASE - RW - 32 bits - NBMCIND:0x33			
Field Name	**Bits**	**Default**	**Description**
CSEnable	0	0x0	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x80	

CPU_DRAM0_CS4_BASE - RW - 32 bits - NBMCIND:0x34			
Field Name	**Bits**	**Default**	**Description**
CSEnable	0	0x0	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x80	

CPU_DRAM0_CS5_BASE - RW - 32 bits - NBMCIND:0x35			
Field Name	**Bits**	**Default**	**Description**
CSEnable	0	0x0	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x80	

CPU_DRAM0_CS6_BASE - RW - 32 bits - NBMCIND:0x36			
Field Name	**Bits**	**Default**	**Description**
CSEnable	0	0x0	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x80	

CPU_DRAM0_CS7_BASE - RW - 32 bits - NBMCIND:0x37

Field Name	Bits	Default	Description
CSEnable	0	0x0	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x80	

CPU_DRAM0_CS01_MASK - RW - 32 bits - NBMCIND:0x38			
Field Name	**Bits**	**Default**	**Description**
AddrMask21_13	13:5	0x1ff	
AddrMask36_27	28:19	0x1f	

CPU_DRAM0_CS23_MASK - RW - 32 bits - NBMCIND:0x39			
Field Name	**Bits**	**Default**	**Description**
AddrMask21_13	13:5	0x1ff	
AddrMask36_27	28:19	0x3ff	

CPU_DRAM0_CS45_MASK - RW - 32 bits - NBMCIND:0x3A			
Field Name	**Bits**	**Default**	**Description**
AddrMask21_13	13:5	0x1ff	
AddrMask36_27	28:19	0x3ff	

CPU_DRAM0_CS67_MASK - RW - 32 bits - NBMCIND:0x3B			
Field Name	**Bits**	**Default**	**Description**
AddrMask21_13	13:5	0x1ff	
AddrMask36_27	28:19	0x3ff	

CPU_DRAM0_BANK_ADDR_MAPPING - RW - 32 bits - NBMCIND:0x3C			
Field Name	**Bits**	**Default**	**Description**
Dimm0AddrMap	3:0	0xb	0=128MB 1=256MB 2=512MB 3=512MB 4=512MB 5=1GB 6=1GB 7=2GB 8=2GB 9=4GB 10=4GB 11=8GB 12=Reserved 13=Reserved 14=Reserved 15=Reserved
Dimm1AddrMap	7:4	0xb	0=128MB 1=256MB 2=512MB 3=512MB 4=512MB 5=1GB 6=1GB 7=2GB 8=2GB 9=4GB 10=4GB 11=8GB 12=Reserved 13=Reserved 14=Reserved 15=Reserved
Dimm2AddrMap	11:8	0x0	0=128MB 1=256MB 2=512MB 3=512MB 4=512MB 5=1GB 6=1GB 7=2GB 8=2GB 9=4GB 10=4GB 11=8GB 12=Reserved 13=Reserved 14=Reserved 15=Reserved

Dimm3AddrMap	15:12	0x0	0=128MB 1=256MB 2=512MB 3=512MB 4=512MB 5=1GB 6=1GB 7=2GB 8=2GB 9=4GB 10=4GB 11=8GB 12=Reserved 13=Reserved 14=Reserved 15=Reserved
BankSwizzleMode	16	0x0	0=Don't remap DRAM device bank address bits 1=Remap DRAM device bank address bits
Ddr3Mode	17	0x0	0=Non-DDR3 1=DDR3
BurstLength32	18	0x0	0=64-byte mode 1=32-byte mode

CPU_DRAM1_CS0_BASE - RW - 32 bits - NBMCIND:0x3D

Field Name	Bits	Default	Description
CSEnable	0	0x1	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x0	

CPU_DRAM1_CS1_BASE - RW - 32 bits - NBMCIND:0x3E

Field Name	Bits	Default	Description
CSEnable	0	0x1	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x40	

CPU_DRAM1_CS2_BASE - RW - 32 bits - NBMCIND:0x3F

Field Name	Bits	Default	Description
CSEnable	0	0x0	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x80	

CPU_DRAM1_CS3_BASE - RW - 32 bits - NBMCIND:0x40			
Field Name	**Bits**	**Default**	**Description**
CSEnable	0	0x0	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x80	

CPU_DRAM1_CS4_BASE - RW - 32 bits - NBMCIND:0x41			
Field Name	**Bits**	**Default**	**Description**
CSEnable	0	0x0	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x80	

CPU_DRAM1_CS5_BASE - RW - 32 bits - NBMCIND:0x42			
Field Name	**Bits**	**Default**	**Description**
CSEnable	0	0x0	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x80	

CPU_DRAM1_CS6_BASE - RW - 32 bits - NBMCIND:0x43			
Field Name	**Bits**	**Default**	**Description**
CSEnable	0	0x0	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x80	

CPU_DRAM1_CS7_BASE - RW - 32 bits - NBMCIND:0x44			
Field Name	**Bits**	**Default**	**Description**
CSEnable	0	0x0	0=Chip-Select not enabled 1=Chip-Select enabled
BaseAddr21_13	13:5	0x0	
BaseAddr36_27	28:19	0x80	

CPU_DRAM1_CS01_MASK - RW - 32 bits - NBMCIND:0x45			
Field Name	**Bits**	**Default**	**Description**
AddrMask21_13	13:5	0x1ff	
AddrMask36_27	28:19	0x1f	

CPU_DRAM1_CS23_MASK - RW - 32 bits - NBMCIND:0x46			
Field Name	**Bits**	**Default**	**Description**
AddrMask21_13	13:5	0x1ff	
AddrMask36_27	28:19	0x3ff	

CPU_DRAM1_CS45_MASK - RW - 32 bits - NBMCIND:0x47			
Field Name	**Bits**	**Default**	**Description**
AddrMask21_13	13:5	0x1ff	
AddrMask36_27	28:19	0x3ff	

CPU_DRAM1_CS67_MASK - RW - 32 bits - NBMCIND:0x48			
Field Name	**Bits**	**Default**	**Description**
AddrMask21_13	13:5	0x1ff	
AddrMask36_27	28:19	0x3ff	

CPU_DRAM1_BANK_ADDR_MAPPING - RW - 32 bits - NBMCIND:0x49			
Field Name	**Bits**	**Default**	**Description**
Dimm0AddrMap	3:0	0xb	0=128MB 1=256MB 2=512MB 3=512MB 4=512MB 5=1GB 6=1GB 7=2GB 8=2GB 9=4GB 10=4GB 11=8GB 12=Reserved 13=Reserved 14=Reserved 15=Reserved

Dimm1AddrMap	7:4	0xb	0=128MB 1=256MB 2=512MB 3=512MB 4=512MB 5=1GB 6=1GB 7=2GB 8=2GB 9=4GB 10=4GB 11=8GB 12=Reserved 13=Reserved 14=Reserved 15=Reserved
Dimm2AddrMap	11:8	0x0	0=128MB 1=256MB 2=512MB 3=512MB 4=512MB 5=1GB 6=1GB 7=2GB 8=2GB 9=4GB 10=4GB 11=8GB 12=Reserved 13=Reserved 14=Reserved 15=Reserved
Dimm3AddrMap	15:12	0x0	0=128MB 1=256MB 2=512MB 3=512MB 4=512MB 5=1GB 6=1GB 7=2GB 8=2GB 9=4GB 10=4GB 11=8GB 12=Reserved 13=Reserved 14=Reserved 15=Reserved
BankSwizzleMode	16	0x0	0=Don't remap DRAM device bank address bits 1=Remap DRAM device bank address bits
Ddr3Mode	17	0x0	0=Non-DDR3 1=DDR3
BurstLength32	18	0x0	0=64-byte mode 1=32-byte mode

CPU_DRAM_CNTL_SELECT_LO - RW - 32 bits - NBMCIND:0x4A			
Field Name	**Bits**	**Default**	**Description**
DctSelHiRngEn	0	0x1	
DctSelHi	1	0x1	
DctSelIntLvEn	2	0x1	
DctGangEn	4	0x0	
DctSelIntLvAddr	7:6	0x0	
DctSelBaseAddr39_27	23:11	0x40	
DramEccEn	24	0x0	

CPU_DRAM_CNTL_SELECT_HI - RW - 32 bits - NBMCIND:0x4B			
Field Name	**Bits**	**Default**	**Description**
DctSelBaseOffset_39_26	23:10	0x0	

CPU_DRAM_BASE_SYSTEM_ADDRESS - RW - 32 bits - NBMCIND:0x4C			
Field Name	**Bits**	**Default**	**Description**
DramBaseAddr39_24	31:16	0x0	

CPU_DRAM_HOLE_ADDRESS - RW - 32 bits - NBMCIND:0x4D			
Field Name	**Bits**	**Default**	**Description**
DramHoleValid	0	0x0	
DramHoleOffset31_23	15:7	0x0	
DramHoleBase31_24	31:24	0x0	

CPU_DRAM_LIMIT_SYSTEM_ADDRESS - RW - 32 bits - NBMCIND:0x4E			
Field Name	**Bits**	**Default**	**Description**
DramLimitAddr39_24	31:16	0x0	

MC_DEBUG - RW - 32 bits - NBMCIND:0x4F			
Field Name	**Bits**	**Default**	**Description**
INT_DEBUG_MUX	5:0	0x0	Selects internal debug bus
INT_DEBUG_BLOCK	7:6	0x0	Selects internal debug block
INT_DEBUG_EN	8	0x0	Enables internal debug bus
TESTBUS_INT (R)	31:16	0x0	Read back of internal debug bus

MC_BIST_CNTL0 - RW - 32 bits - NBMCIND:0x5C			
Field Name	**Bits**	**Default**	**Description**
BIST_DONE (R)	0	0x0	Set to 0 when BIST_RUN or BIST_RESET_N is 0. Set to 1 when the bist read/write is done either normally or due to mismatch
BIST_MISMATCH_CYCLE (R)	3:1	0x0	Records the cycle which caused the mismatch. 3'b000: cycle1 of burst1; 3'b100: cycle1 of burst2; 3'b001: cycle2 of burst1; 3'b1001 cycle2 of burst2; 3'b010: cycle3 of burst1; 3'b110: cycle3 of burst2; 3'b011: cycle4 of burst1; 3'b111: cycle4 of burst2;
BIST_RUN	4	0x0	0=Not Enable 1=Enable
BIST_RESET_N	5	0x0	0=Resets mcbist, but doesn't disturb read-only mcbist values. 1=Active
BIST_MISMATCH_STATUS	7:6	0x0	0=Data (64 bit) mismatch info. Info would be ORed with subsequent reads 1=Keeps first mismatch data info as sticky 2=Address 32'd0,addr[26:0],5'd0 mismatch info. is updated at every mismatch 3=Keep first address info sticky
BIST_RW_CREDITS	13:8	0x4	BIST read/write credit/debit interface credits
BIST_RW_CREDITS_SEL	15:14	0x0	BIST read/write credit/debit interface credits select
RESERVED16	31:16	0x0	
First control register of MCBIST			

MC_BIST_CNTL1 - RW - 32 bits - NBMCIND:0x5D			
Field Name	**Bits**	**Default**	**Description**
BIST_MISMATCH_STKY (R)	0	0x0	0=When BIST_RUN is 0 1=Read mismatch
BIST_RDWR_EN	2:1	0x0	0=No op 1=Activate write client only 2=Activate read client only 3=Activate both read & write clients
BIST_SADDR_SEL	4:3	0x0	0=No op 1=Set start write-address 2=Set start read-address 3=Set both start read and start write addresses
BIST_CYC	7:5	0x0	0=No op 1=Run for 2 read (and/or write) bursts 2=Run for 4 read (and/or write) bursts 3=Reserved 4=Run for 32 read (and/or write) bursts 5=Reserved 6=Reserved 7=Run continuously until there is a mismatch-stop, or end-address stop
BIST_DATA_CMP	8	0x0	0=Read data is compared against expected data 1=Read data is not compared (there is, therfore, no question of mismtach)
BIST_MISMATCH_STOP	9	0x0	0=Do not stop if read mismatch 1=Stop if read mismatch
BIST_ADDR_BND	10	0x0	0=Use read address for end-address stop 1=Use write address for end-address stop

BIST_ADDR_LOOP	11	0x0	0=Stop based on BIST_CYC 1=Keep looping read (and/or write) operations between start and end adresses
BIST_WADDR_GEN	14:12	0x0	0=wr_addr[26:0] = wr_addr[26:0] + 1 1=wr_addr[26:0] = wr_addr[26:0] - 1 2=wr_addr[26:0] = wr_addr[26:0] + 4 3=wr_addr[26:0] = wr_addr[26:0] - 4 4=wr_addr[26:5] = wr_addr[26:5] + 1 5=wr_addr[26:5] = wr_addr[26:5] - 1 6=wr_addr[26:13] = wr_addr[26:13] + 1 7=wr_addr[26:13] = wr_addr[26:13] - 1
BIST_RADDR_GEN	17:15	0x0	0=rd_addr[26:0] = rd_addr[26:0] + 1 1=rd_addr[26:0] = rd_addr[26:0] - 1 2=rd_addr[26:0] = rd_addr[26:0] + 4 3=rd_addr[26:0] = rd_addr[26:0] - 4 4=rd_addr[26:5] = rd_addr[26:5] + 1 5=rd_addr[26:5] = rd_addr[26:5] - 1 6=rd_addr[26:13] = rd_addr[26:13] + 1 7=rd_addr[26:13] = rd_addr[26:13] - 1
BIST_END_ADDR	31:18	0x0	read/write upper address (addr[31:18])
Second control register of MCBIST. Bits [31:5] of this register is also used as starting address (BIST_START_ADDR). Refer to bit field BIST_SADDR_SEL for details.			

MC_BIST_MISMATCH_L - RW - 32 bits - NBMCIND:0x5E			
Field Name	**Bits**	**Default**	**Description**
BIST_MISMATCH_L (R)	31:0	0x0	Refer to BIST_MISMATCH_STATUS for setting
Lower 32 bits of the 64 bits mcbist read mismatch info			

MC_BIST_MISMATCH_H - RW - 32 bits - NBMCIND:0x5F			
Field Name	**Bits**	**Default**	**Description**
BIST_MISMATCH_H (R)	31:0	0x0	Refer to BIST_MISMATCH_STATUS for setting
Upper 32 bits of the 64 bits mcbist read mismatch info			

MC_BIST_PATTERN0L - RW - 32 bits - NBMCIND:0x60			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN0L	31:0	0x0	32 bit data pattern
Lower half of DW0 (double word 0) of data pattern. MCBIST uses 8 user defiend DWs to generate two consecutive data bursts - each of 4x64 bits.burst_one[255:0] = MC_BIST_PATTERN3H, MC_BIST_PATTERN3L, MC_BIST_PATTERN2H, MC_BIST_PATTERN2L, MC_BIST_PATTERN1H, MC_BIST_PATTERN1L, MC_BIST_PATTERN0H, MC_BIST_PATTERN0L. Similarly burst-two is defined by other 8 registers. These registers are per mcbist engine based			

MC_BIST_PATTERN0H - RW - 32 bits - NBMCIND:0x61			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN0H	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN1L - RW - 32 bits - NBMCIND:0x62			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN1L	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN1H - RW - 32 bits - NBMCIND:0x63			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN1H	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN2L - RW - 32 bits - NBMCIND:0x64			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN2L	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN2H - RW - 32 bits - NBMCIND:0x65			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN2H	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN3L - RW - 32 bits - NBMCIND:0x66			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN3L	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN3H - RW - 32 bits - NBMCIND:0x67			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN3H	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN4L - RW - 32 bits - NBMCIND:0x68			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN4L	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN4H - RW - 32 bits - NBMCIND:0x69			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN4H	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN5L - RW - 32 bits - NBMCIND:0x6A			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN5L	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN5H - RW - 32 bits - NBMCIND:0x6B			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN5H	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN6L - RW - 32 bits - NBMCIND:0x6C			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN6L	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN6H - RW - 32 bits - NBMCIND:0x6D			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN6H	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN7L - RW - 32 bits - NBMCIND:0x6E			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN7L	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MC_BIST_PATTERN7H - RW - 32 bits - NBMCIND:0x6F			
Field Name	**Bits**	**Default**	**Description**
BIST_PATTERN7H	31:0	0x0	32 bit data pattern
Refer to MC_BIST_PATTERN0L			

MCA_MEMORY_INIT_MRS - RW - 32 bits - NBMCIND:0xA0			
Field Name	**Bits**	**Default**	**Description**
MCA_MODE_REG	19:0	0x0	Value to be loaded in memory mode register in nominal mode Bits [14:0]=ADDRESS[14:0] Bit [15]=RESERVED Bits [18:16]=BANK[2:0] Bit [19]=RESERVED
MCA_INIT_CS_MRS	23:20	0xf	Channel A CS to be initialized 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_INIT_SEQ	28:24	0x0	Initialization sequence selection for execution 0=Whole initialization sequence selected for execution 1-31=Initialization sequence selected for execution
MCA_INIT_IDLE	29	0x0	Forces MC channel A idle before initialization execution. 0=MC not forced idle before initialization execution 1=MC forced idle before initialization execution
MCA_INIT_COMPLETE	30	0x0	As long as this bit is '0', the MCA will not accept requests from the clients. It is used primarily to block requests when the MCA might mishandle them, such as when the FB or AGP apertures are undefined or unstable. 0=Register Initialization Not Complete 1=Register Initialization Complete
MCA_INIT_EXECUTE	31	0x0	The MC will execute software initialization command or whole hardware initialization sequence on a transition from 0 to 1 for memory controller MCA 0=Normal 1=Execute initialization command
Memory controller A memory initialization nominal			

MCA_MEMORY_INIT_EMRS - RW - 32 bits - NBMCIND:0xA1			
Field Name	**Bits**	**Default**	**Description**
MCA_EXT_MODE_REG	19:0	0x10000	Value to be loaded in memory mode register in nominal mode. Bits [14:0]=ADDRESS[14:0] Bit [15]=RESERVED Bits [18:16]=BANK[2:0] Bit [19]=RESERVED
MCA_INIT_CS_EMRS	23:20	0xf	Channel A CS to be initialized 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_INIT_DLL	24	0x1	Enables the execution of memory DLL reset mode register command for nominal mode initialization sequence
MCA_INIT_OCD	25	0x0	Drive 0/1 for OCD drive extended mode register command for nominal mode initialization sequence
MCA_INIT_ZQC	26	0x0	Initializes ZQC one by one CS (nominal) or all CS together. 0=Increment CS counter for each ZQC command executed in the same initialization sequence 1=SEND ZQC command to all CS
MCA_INIT_MPR	27	0x0	Enables MPR read

MCA_INIT_DQSS	28	0x0	Strobe sample by internal clock enable 0=Strobe sample by internal clock disabled 1=Strobe sample by internal clock enabled
MCA_INIT_WL	29	0x0	DDR3 write levelization command enable 0=Write levelization pulse only 1=Write levelization command and pulse
RESERVED30	31:30	0x0	
Memory controller A memory initialization nominal			

MCA_MEMORY_INIT_EMRS2 - RW - 32 bits - NBMCIND:0xA2			
Field Name	**Bits**	**Default**	**Description**
MCA_EXT2_MODE_REG	19:0	0x20000	Value to be loaded in memory mode register in nominal mode. Bits [14:0]=ADDRESS[14:0] Bit [15]=RESERVED Bits [18:16]=BANK[2:0] Bit [19]=RESERVED
MCA_INIT_CS_EMRS2	23:20	0xf	Channel A CS to be initialized 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_TWLODTEN	27:24	0x4	DDR3 ODT write levelization, tDQSS margining, x4 clocks 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TWLDQSEN	31:28	0x7	DDR3 ODT write levelization, tDQSS margining, x4 clocks 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
Memory controller A memory initialization nominal			

MCA_MEMORY_INIT_EMRS3 - RW - 32 bits - NBMCIND:0xA3			
Field Name	**Bits**	**Default**	**Description**
MCA_EXT3_MODE_REG	19:0	0x30000	Value to be loaded in memory mode register in nominal mode Bits [14:0]=ADDRESS[14:0] Bit [15]=RESERVED Bits [18:16]=BANK[2:0] Bit [19]=RESERVED
MCA_INIT_CS_EMRS3	23:20	0xf	Channel A CS to be initialized 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_TWLMRD	27:24	0xa	DDR3 ODT write levelization, tDQSS margining, x4 clocks 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TDLL	31:28	0x4	Channel A DLL reset time, x64 clocks
Memory controller A memory initialization nominal			

MCA_MEMORY_INIT_SEQUENCE_1 - RW - 32 bits - NBMCIND:0xA4			
Field Name	**Bits**	**Default**	**Description**
MCA_INIT_SEQ_OP_1	3:0	0x1	Operation #1 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_2	7:4	0x5	Operation #2 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_3	11:8	0x8	Operation #3 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_4	15:12	0x4	Operation #4 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_5	19:16	0x2	Operation #5 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_6	23:20	0x2	Operation #6 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_7	27:24	0x2	Operation #7 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_8	31:28	0x2	Operation #8 to be executed in memory intialization sequence
Memory controller A initialization sequnce first chunk. Initialization operation selection: 0=NOP 1=PRECHARGE ALL 2=REFRESH 3=ZQC 4=MRS 5=EMRS 6=EMRS2 7=EMRS3 8=MRS DLL reset 9=EMRS OCD default A=OCD adjust B=OCD drive C=Write levelization D=NOP 10 clocks E=NOP 50 clocks F=NOP 255 clocks			

MCA_MEMORY_INIT_SEQUENCE_2 - RW - 32 bits - NBMCIND:0xA5			
Field Name	**Bits**	**Default**	**Description**
MCA_INIT_SEQ_OP_9	3:0	0x0	Operation #9 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_10	7:4	0x0	Operation #10 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_11	11:8	0x0	Operation #11 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_12	15:12	0x0	Operation #12 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_13	19:16	0x0	Operation #13 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_14	23:20	0x0	Operation #14 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_15	27:24	0x0	Operation #15 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_16	31:28	0x0	Operation #16 to be executed in memory intialization sequence

Memory controller A initialization sequnce second chunk.
Initialization operation selection:
0=NOP
1=PRECHARGE ALL
2=REFRESH
3=ZQC
4=MRS
5=EMRS
6=EMRS2
7=EMRS3
8=MRS DLL reset
9=EMRS OCD default
A=OCD adjust
B=OCD drive
C=Write levelization
D=NOP 10 clocks
E=NOP 50 clocks
F=NOP 255 clocks

MCA_MEMORY_INIT_SEQUENCE_3 - RW - 32 bits - NBMCIND:0xA6			
Field Name	**Bits**	**Default**	**Description**
MCA_INIT_SEQ_OP_17	3:0	0x0	Operation #17 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_18	7:4	0x0	Operation #18 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_19	11:8	0x0	Operation #19 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_20	15:12	0x0	Operation #20 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_21	19:16	0x0	Operation #21 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_22	23:20	0x0	Operation #22 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_23	27:24	0x0	Operation #23 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_24	31:28	0x0	Operation #24 to be executed in memory intialization sequence
Memory controller A initialization sequnce third chunk. Initialization operation selection: 0=NOP 1=PRECHARGE ALL 2=REFRESH 3=ZQC 4=MRS 5=EMRS 6=EMRS2 7=EMRS3 8=MRS DLL reset 9=EMRS OCD default A=OCD adjust B=OCD drive C=Write levelization D=NOP 10 clocks E=NOP 50 clocks F=NOP 255 clocks			

MCA_MEMORY_INIT_SEQUENCE_4 - RW - 32 bits - NBMCIND:0xA7			
Field Name	**Bits**	**Default**	**Description**
MCA_INIT_SEQ_OP_25	3:0	0x0	Operation #25 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_26	7:4	0x0	Operation #26 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_27	11:8	0x0	Operation #27 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_28	15:12	0x0	Operation #28 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_29	19:16	0x0	Operation #29 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_30	23:20	0x0	Operation #30 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_31	27:24	0x0	Operation #31 to be executed in memory intialization sequence
MCA_INIT_SEQ_OP_32	31:28	0x0	Operation #32 to be executed in memory intialization sequence

Memory controller A initialization sequnce fourth chunk.
Initialization operation selection:
0=NOP
1=PRECHARGE ALL
2=REFRESH
3=ZQC
4=MRS
5=EMRS
6=EMRS2
7=EMRS3
8=MRS DLL reset
9=EMRS OCD default
A=OCD adjust
B=OCD drive
C=Write levelization
D=NOP 10 clocks
E=NOP 50 clocks
F=NOP 255 clocks

MCA_TIMING_PARAMETERS_1 - RW - 32 bits - NBMCIND:0xA8			
Field Name	**Bits**	**Default**	**Description**
MCA_RD_LAT	3:0	0x4	Memory CAS Latency 0=0 clock (not supported) 1=1 clock (not supported) 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_WR_LAT	7:4	0x3	Memory Write Latency 0=0 clock (not supported) 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TRCDR	11:8	0x8	Active to Read delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRCDW	15:12	0x8	Active to Write delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRP	19:16	0x8	Precharge command period 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRTP	23:20	0x4	Internal Read to Precharge command delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock

MCA_TWR	27:24	0x8	Write recovery time 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRRD	31:28	0x6	Active bank A to Active bank B command period 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
Memory controller A timing parameters, set 1			

MCA_TIMING_PARAMETERS_2 - RW - 32 bits - NBMCIND:0xA9			
Field Name	**Bits**	**Default**	**Description**
MCA_TRAS	7:0	0x18	Active to Precharge command 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 29=29 clock 30=30 clock 31=31 clock
MCA_TRC	15:8	0x20	Row Cycle time, Active to Active/Auto-Refresh command period 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 125=125 clock 126=126 clock 127=127 clock
MCA_TRFC	23:16	0x28	Auto-Refresh to Active/Auto-Refresh command period 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 125=125 clock 126=126 clock 127=127 clock
MCA_TREFI	31:24	0x10	1 memory refresh is performed every TREFI*64 MCLK cycles
Memory controller A timing parameters, set 2			

MCA_TIMING_PARAMETERS_3 - RW - 32 bits - NBMCIND:0xAA

Field Name	Bits	Default	Description
MCA_TRTR_CS	3:0	0x1	Read to Read command to different CS 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TRTW	7:4	0x2	Read to Write bus turnaround 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWTR	11:8	0x4	Internal Write to Read command delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWTR_CS	15:12	0x2	Write to Read command to different CS 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWTW_CS	19:16	0x1	Write to Write command to different CS 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4 = 4 clock 5 = 5 clock 6 = 6 clock 7 = 7 clock
MCA_TCCD	23:20	0x2	CAS to CAS command delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock

MCA_TCKE	27:24	0x3	CKE minimum high and low pulse width 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TXP	31:28	0x2	Exit precharge power down to any valid command 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
Memory controller A timing parameters, set 3			

MCA_TIMING_PARAMETERS_4 - RW - 32 bits - NBMCIND:0xAB			
Field Name	**Bits**	**Default**	**Description**
MCA_TXARDS	3:0	0x6	Exit active power down to read command 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TAXPD	7:4	0x8	ODT power down exit latency 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRPALL	11:8	0x2	Precharge all for 8 bank memories 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TFAW	15:12	0x2	Back to back activate rolling window 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock

MCA_TZQCL	19:16	0x8	Impedance calibration long timing, can be merged with DLL time, x64 clocks
MCA_TZQCS	23:20	0x4	Impedance calibration short timing, x64 clocks
MCA_TZQCI	27:24	0x1	Impedance calibration interval, x4096 refresh cycles
MCA_TMRD	31:28	0x2	Mode register set command cycle time 0=0 clock 1=1 clock ... 15=15 clock
Memory controller A timing parameters, set 4			

MCA_MEMORY_TYPE - RW - 32 bits - NBMCIND:0xAC			
Field Name	**Bits**	**Default**	**Description**
MCA_MODE_CS0	3:0	0x0	MCA CS0 memory size 0=Unpopulated chip select 4=32MB (16Mbx16) 5=64MB (32Mbx8) 6=128MB (64Mbx8) 10=64MB (32Mbx16) 11=128MB (64Mbx16)
MCA_AP_BIT	4	0x0	MCA Auto Precharge bit 0=A10 1=A8
RESERVED5	7:5	0x0	
Memory controller A memory size and type			

MCA_SEQ_CONTROL - RW - 32 bits - NBMCIND:0xB0			
Field Name	**Bits**	**Default**	**Description**
MCA_SEQ_MCIFR_URG_EN	0	0x0	Channel A urgent MCIF read. If mcif read is urgent and it is found in the command fifo then flush it out. 0=Disable flushing out of urgent mcif reads 1=Enable flushing out of urgent mcif reads
MCA_SEQ_DMIFR_URG_EN	1	0x0	Channel A urgent DMIF read. If dmif read is urgent and it is found in the command fifo then flush it out. 0=Disable flushing out of urgent dmif reads 1=Enable flushing out of urgent dmif reads
MCA_SEQ_AZR_URG_EN	2	0x0	Channel A urgent AZ read. If az read is urgent and it is found in the command fifo then flush it out. 0=Disable flushing out of urgent az reads 1=Enable flushing out of urgent az reads
MCA_SEQ_BIUW_URG_EN	3	0x0	Channel A urgent BIU write. If biu write is urgent and it is found in the command fifo then flush it out. 0=Disable flushing out of urgent biu writes 1=Enable flushing out of urgent biu writes
MCA_DQ_PRE	5:4	0x0	Write data preamble / postamble 0=Low 1=High 2=Opposite of first / last data 3=Same as first / last data
MCA_AP_DISABLE	6	0x0	Channel A auto precharge disable 0=Auto recharge enabled 1=Auto precharge disabled
MCA_CKE_FOR_ODT	7	0x0	Channel A ODT CKE stall 0=No stall 1=Stall

MCA_BURST_LENGTH_8	8	0x0	Obsolete. Channel A is always in burst length of 8 regardless of this field. Channel A Burst Length 1=Burst Length 8
MCA_2T_TIMING	9	0x0	Channel A timing mode 0=1T timing 1=2T timing
MCA_3T_TIMING	10	0x0	Channel A timing mode 0=1T timing 1=3T timing
RESERVED11	11	0x0	
MCA_CMD_HOLD	12	0x0	Channel A command hold to minimize transition 0=Do not hold command 1=Hold command
MCA_DATA_HOLD	13	0x0	Channel A data hold to minimize transition 0=Do not hold data 1=Hold data
RESERVED14	19:14	0x0	
MCA_TCKED	23:20	0x8	Channel A CKE time delay, time from CKE condition to CKE low, x4 clocks 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TTRSTD	27:24	0x8	Channel A tristate time delay, time from tristate condition to tristate, x4 clocks 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TTRST	31:28	0x4	Channel A tristate time, time from tristate to full drive 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
Memory controller A sequencer control			

MCA_RECEIVING - RW - 32 bits - NBMCIND:0xB1			
Field Name	**Bits**	**Default**	**Description**
MCA_DQ_TRANSFER	3:0	0x3	Channel A read data transfer from strobe flops to core clock flops 0=CL+0clock 1=CL+1clock 2=CL+2clock 3=CL+3clock 4=CL+4clock
MCA_DQS_RST_PLS	5:4	0x2	Channel A read strobe reset pulse 0=Quarter pulse, Quarter postion 1=Half pulse, Quarter position 2=Half pulse, Half position 3=Reserved
MCA_DQ_DQS_REC_DYNAMIC	6	0x0	Channel A data and strobe receiver enable control 0=Always enabled 1=Enabled for read only
MCA_DQ_TRANSFER_FALL	7	0x0	Channel A read data transfer from strobe flops to negative edge core clock flops 0=Use positive edge flops 1=Use negative edge flops
MCA_DQS_ARRIVAL	11:8	0x2	Channel A input strobe reset removal edge 0=CL 1=CL+0.25 2=CL+0.50 3=CL+0.75 4=CL+1.00 5=CL+1.25 6=CL+1.50 7=CL+1.75 8=CL+2.00 9=CL+2.25 10=CL+2.50 11=CL+2.75 12=CL+3.00 13=CL+3.25 14=CL+3.50 15=CL+3.75
MCA_IN_TERM_START_DQ	12	0x0	Channel A data input termination turning on for read preceded by write 0=Turning on half clock after OE off 1=Turning on when OE off
MCA_IN_TERM_STOP_DQ	13	0x0	Channel A data input termination turning off for read followed by write 0=Turning off half clock before OE on 1=Turning off when OE on
MCA_IN_TERM_START_DQS	14	0x0	Channel A strobe input termination turning on for read preceded by write 0=Turning on half clock after OE off 1=Turning on when OE off
MCA_IN_TERM_STOP_DQS	15	0x0	Channel A strobe input termination turning off for read followed by write 0=Turning off half clock before OE on 1=Turning off when OE on

MCA_IN_TERM_N_DQ	18:16	0x3	Channel A data input N termination, 3 pull-down resistors 300 Ohm 0=Termination off 1=300 Ohm pull-down 3=150 Ohm pull-down 7=100 Ohm pull-down
RESERVED19	19	0x0	
MCA_IN_TERM_P_DQ	22:20	0x3	Channel A data input P termination, 3 pull-up resistors 300 Ohm 0=Termination off 1=300 Ohm pull-up 3=150 Ohm pull-up 7=100 Ohm pull-up
RESERVED23	23	0x0	
MCA_IN_TERM_N_DQS	26:24	0x3	Channel A strobe input N termination, 3 pull-down resistors 300 Ohm 0=Termination off 1=300 Ohm pull-down 3=150 Ohm pull-down 7=100 Ohm pull-down
RESERVED27	27	0x0	
MCA_IN_TERM_P_DQS	30:28	0x3	Channel A strobe input P termination, 3 pull-up resistors 300 Ohm 0=Termination off 1=300 Ohm pull-up 3=150 Ohm pull-up 7=100 Ohm pull-up
RESERVED31	31	0x0	
Memory controller A receiving control			

MCA_IN_TIMING_DQS_3210 - RW - 32 bits - NBMCIND:0xB2			
Field Name	**Bits**	**Default**	**Description**
MCA_DQS_ARRIVAL_0	3:0	0x2	Channel A byte 0 input strobe reset removal edge 0=CL 1=CL+0.25 2=CL+0.50 3=CL+0.75 4=CL+1.00 5=CL+1.25 6=CL+1.50 7=CL+1.75 8=CL+2.00 9=CL+2.25 10=CL+2.50 11=CL+2.75 12=CL+3.00 13=CL+3.25 14=CL+3.50 15=CL+3.75 16=CL+4.00 17=CL+4.25
RESERVED4	7:4	0x0	

MCA_DQS_ARRIVAL_1	11:8	0x2	Channel A byte 1 input strobe reset removal edge 0=CL 1=CL+0.25 2=CL+0.50 3=CL+0.75 4=CL+1.00 5=CL+1.25 6=CL+1.50 7=CL+1.75 8=CL+2.00 9=CL+2.25 10=CL+2.50 11=CL+2.75 12=CL+3.00 13=CL+3.25 14=CL+3.50 15=CL+3.75 16=CL+4.00 17=CL+4.25
RESERVED12	15:12	0x0	
Channel A input strobe gating timing			

MCA_DRIVING - RW - 32 bits - NBMCIND:0xB4			
Field Name	**Bits**	**Default**	**Description**
MCA_CK_ENABLE	5:0	0x0	Channel A clock pair select enable 0=Particular clock pair disabled 1=Particular clock pair enabled
MCA_CKE_ENABLE	6	0x0	Channel A CKE enable 0=CKE disabled, forced low 1=CKE enabled, high or dynamic
MCA_CKE_DYNAMIC	7	0x0	Channel A CKE dynamic 0=CKE high when enabled 1=CKE dynamic when enabled, high or low depending on activity, active or precharge power down
MCA_ODT_ENABLE	8	0x0	Channel A ODT enable 0=ODT forced 0 1=ODT enabled
MCA_ODT_DYNAMIC	9	0x1	Channel A ODT dynamic 0=ODT forced 1 if enabled 1=ODT dynamic if enabled
MCA_ODT_READ	10	0x0	Channel A ODT enable for read 0=ODT disabled for read 1=ODT enabled for read
MCA_ODT_WRITE	11	0x1	Channel A ODT enable for write 0=ODT disabled for write 1=ODT enabled for write
MCA_ODTR_POSITION	13:12	0x0	Channel A ODT read position When ODTX 0, read latency dependent When ODTX 1, read command dependent 0=ODT start at RL-3 for ODTX 0, ODT start at RD for ODTX1 1=ODT start at RL-2 for ODTX 0, ODT start at RD+1 for ODTX 1 2= 3=

MCA_ODTR_LENGTH	15:14	0x0	Channel A ODT read length 0=ODT length BL/2+1 1=ODT length BL/2+2 2= 3=
MCA_ODTW_POSITION	17:16	0x0	Channel A ODT write position When ODTX 0, write latency dependent When ODTX 1, write command dependent 0=ODT start at WL-3 for ODTX 0, ODT start at WR for ODTX1 1=ODT start at WL-2 for ODTX 0, ODT start at WR+1 for ODTX 1 2= 3=
MCA_ODTW_LENGTH	19:18	0x0	Channel A ODT write length 0=ODT length BL/2+1 1=ODT length BL/2+2 2= 3=
MCA_ODT_STALL	20	0x0	Channel A ODT stall first write 0=No stall 1=Stall
MCA_ODTX	21	0x0	Channel A ODTX enable 0=ODTX disable 1=ODTX enable
MCA_ODTX_1T	22	0x0	Channel A ODTX 1T 0=1T/2T/3T 1=1T
MCA_ODTX_POSITION	23	0x0	Channel A ODTX position 0=ODTX start as set with ODT_START 1=ODT start one clock later then set with ODT_START
MCA_DQS_PRE	25:24	0x1	Channel A strobe output preamble 0=0.5 clock 1=1 clock 2=1.5 clock 3=2 clock
MCA_DQS_POST	27:26	0x1	Channel A strobe output postamble 0=0.5 clock 1=1 clock 2=1.5 clock 3=2 clock
MCA_DQSX_PRE	28	0x0	Channel A DQS preamble pulse 0=As set with DQS_PRE 1=One clock reduced DQS_PRE
MCA_DQSX_POST	29	0x0	Channel A DQS postamble pulse 0=As set with DQS_POST 1=One clock reduced DQS_POST
MCA_DQSX_PRE_PLS	30	0x0	Channel A DQS preamble pulse 0=Preamble low 1=Preamble pulse
MCA_DQSX_PRE_HI	31	0x0	Channel A DQS preamble/postamble high 0=Preamble low 1=Preamble high
Memory controller A driving control			

MCA_OUT_TIMING - RW - 32 bits - NBMCIND:0xB5			
Field Name	**Bits**	**Default**	**Description**
MCA_OUT_TIMING_CK	2:0	0x4	Channel A clock output timing 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
MCA_PAD_BYPASS_CK	3	0x1	Channel A clock bypassing pad flops 0=Through pad flops 1=Bypass pad flops
MCA_OUT_TIMING_CKE	6:4	0x5	Channel A CKE output timing 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
MCA_PAD_BYPASS_CKE	7	0x1	Channel A CKE bypassing pad flops 0=Through pad flops 1=Bypass pad flops
MCA_OUT_TIMING_CS	10:8	0x5	Channel A CS output timing 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
MCA_PAD_BYPASS_CS	11	0x1	Channel A CS bypassing pad flops 0=Through pad flops 1=Bypass pad flops
MCA_OUT_TIMING_CMD	14:12	0x5	Channel A address andcommand output timing 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
MCA_PAD_BYPASS_CMD	15	0x1	Channel A address and command bypassing pad flops 0=Through pad flops 1=Bypass pad flops

MCA_OUT_TIMING_ODT	18:16	0x5	Channel A ODT output timing 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
MCA_PAD_BYPASS_ODT	19	0x1	Channel A ODT bypassing pad flops 0=Through pad flops 1=Bypass pad flops
MCA_OUT_TIMING_DQ	22:20	0x3	Channel A DQ output timing 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
MCA_PAD_BYPASS_DQ	23	0x1	Channel A data and mask bypassing pad flops 0=Through pad flops 1=Bypass pad flops
MCA_OUT_TIMING_DQS	26:24	0x4	Channel A DQS output timing 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
MCA_PAD_BYPASS_DQS	27	0x1	Channel A strobe bypassing pad flops 0=Through pad flops 1=Bypass pad flops
MCA_MX1X2X_CK	29:28	0x0	Channel A clock output data/mask phase range 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
RESERVED30	31:30	0x0	
Memory controller A output timing			

MCA_OUT_TIMING_DQ - RW - 32 bits - NBMCIND:0xB6			
Field Name	**Bits**	**Default**	**Description**
MCA_OUT_TIMING_DQ_B0	3:0	0x3	Channel A byte 0 data and mask output timing 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
MCA_OUT_TIMING_DQ_B1	7:4	0x3	Channel A byte 1 data and mask output timing 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
Channel A output data and mask timing			

MCA_OUT_TIMING_DQS - RW - 32 bits - NBMCIND:0xB7			
Field Name	**Bits**	**Default**	**Description**
MCA_OUT_TIMING_DQS_0	3:0	0x4	Channel A byte 0 strobe output timing 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
MCA_OUT_TIMING_DQS_1	7:4	0x4	Channel A byte 1 strobe output timing 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
Channel A output strobe timing			

MCA_STRENGTH_N - RW - 32 bits - NBMCIND:0xB8			
Field Name	**Bits**	**Default**	**Description**
MCA_STRENGTH_N_CK	3:0	0xb	Channel A clock (nominal and complement) strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_CKE	7:4	0xb	Channel A CKE strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_CS	11:8	0xb	Channel A CS strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_CMD	15:12	0xb	Channel A RAS/CAS/WE and address strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_ODT	19:16	0xb	Channel A ODT strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_DQ	23:20	0xb	Channel A data and mask strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_DQS	27:24	0xb	Channel A strobe (nominal and complement) strength N driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_N_XXX	31:28	0xb	Channel A spare strength N driver 0=Minimum strength 15=Maximum strength
Memory controller A strength N			

MCA_STRENGTH_P - RW - 32 bits - NBMCIND:0xB9			
Field Name	**Bits**	**Default**	**Description**
MCA_STRENGTH_P_CK	3:0	0xb	Channel A clock (nominal and complement) strength P driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_P_CKE	7:4	0xb	Channel A CKE strength P driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_P_CS	11:8	0xb	Channel A CS strength P driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_P_CMD	15:12	0xb	Channel A RAS/CAS/WE and address strength P driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_P_ODT	19:16	0xb	Channel A ODT strength P driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_P_DQ	23:20	0xb	Channel A data and mask strength P driver 0=Minimum strength 15=Maximum strength
MCA_STRENGTH_P_DQS	27:24	0xb	Channel A strobe (nominal and complement) strength P driver 0=Minimum strength 15=Maximum strength

MCA_STRENGTH_P_XXX	31:28	0xb	Channel A spare strength P driver 0=Minimum strength 15=Maximum strength
Memory controller A strength P			

MCA_STRENGTH_STEP - RW - 32 bits - NBMCIND:0xBA			
Field Name	**Bits**	**Default**	**Description**
MCA_STR_STEP_N_CK	1:0	0x1	Channel A clock (nominal and complemenat) impedance controller adjustment step for strength N driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_P_CK	3:2	0x1	Channel A clock (nominal and complemenat) impedance controller adjustment step for strength P driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_N_CKE	5:4	0x1	Channel A CKE impedance controller adjustment step for strength N driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_P_CKE	7:6	0x1	Channel A CKE impedance controller adjustment step for strength P driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_N_CS	9:8	0x1	Channel A CS impedance controller adjustment step for strength N driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_P_CS	11:10	0x1	Channel A CS impedance controller adjustment step for strength P driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_N_CMD	13:12	0x1	Channel A RAS/CAS/WE and address impedance controller adjustment step for strength N driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_P_CMD	15:14	0x1	Channel A RAS/CAS/WE and address impedance controller adjustment step for strength P driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment

MCA_STR_STEP_N_ODT	17:16	0x1	Channel A ODT impedance controller adjustment step for strength N driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_P_ODT	19:18	0x1	Channel A ODT impedance controller adjustment step for strength P driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_N_DQ	21:20	0x1	Channel A data and mask impedance controller adjustment step for strength N driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_P_DQ	23:22	0x1	Channel A data and mask impedance controller adjustment step for strength P driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_N_DQS	25:24	0x1	Channel A strobe (nominal and complement) impedance controller adjustment step for strength N driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_P_DQS	27:26	0x1	Channel A strobe (nominal and complement) impedance controller adjustment step for strength P driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_N_XXX	29:28	0x1	Channel A spare impedance controller adjustment step for strength N driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
MCA_STR_STEP_P_XXX	31:30	0x1	Channel A spare impedance controller adjustment step for strength P driver 0=0 step, no adjustment 1=1 step, adjustment the same as reference 2=2 step, higher than reference adjustment 3=3 step, higher than reference adjustment
Memory controller A impedance controller adjustment step for strength			

MCA_STRENGTH_READ_BACK_N - RW - 32 bits - NBMCIND:0xBB			
Field Name	**Bits**	**Default**	**Description**
MCA_STR_READ_BACK_N_CK (R)	3:0	0x0	Channel A clock (nominal and complemenat) read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_CKE (R)	7:4	0x0	Channel A CKE read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_CS (R)	11:8	0x0	Channel A CS read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_CMD (R)	15:12	0x0	Channel A RAS/CAS/WE and address read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_ODT (R)	19:16	0x0	Channel A ODT read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_DQ (R)	23:20	0x0	Channel A data and mask read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_DQS (R)	27:24	0x0	Channel A strobe (nominal and complement) read back strength N driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_N_XXX (R)	31:28	0x0	Channel A spare read back strength N driver 0=Minimum strength 15=Maximum strength
Memory controller A strength N read back			

MCA_STRENGTH_READ_BACK_P - RW - 32 bits - NBMCIND:0xBC			
Field Name	**Bits**	**Default**	**Description**
MCA_STR_READ_BACK_P_CK (R)	3:0	0x0	Channel A clock (nominal and complement) read back strength P driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_P_CKE (R)	7:4	0x0	Channel A CKE read back strength P driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_P_CS (R)	11:8	0x0	Channel A CS read back strength P driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_P_CMD (R)	15:12	0x0	Channel A RAS/CAS/WE and address read back strength P driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_P_ODT (R)	19:16	0x0	Channel A ODT read back strength P driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_P_DQ (R)	23:20	0x0	Channel A data and mask read back strength P driver 0=Minimum strength 15=Maximum strength

MCA_STR_READ_BACK_P_DQS (R)	27:24	0x0	Channel A strobe (nominal and complement) read back strength P driver 0=Minimum strength 15=Maximum strength
MCA_STR_READ_BACK_P_XXX (R)	31:28	0x0	Channel A spare read back strength P driver 0=Minimum strength 15=Maximum strength
Memory controller A strength P read back			

MCA_PREBUF_SLEW_N - RW - 32 bits - NBMCIND:0xC1			
Field Name	**Bits**	**Default**	**Description**
MCA_PREBUF_SLEW_N_CK	3:0	0x0	Channel A clock (nominal and complemenat) prebuffer slew N control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_N_CKE	7:4	0x0	Channel A CKE prebuffer slew N control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_N_CS	11:8	0x0	Channel A CS prebuffer slew N control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_N_CMD	15:12	0x0	Channel A RAS/CAS/WE and address prebuffer slew N control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_N_ODT	19:16	0x0	Channel A ODT prebuffer slew N control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_N_DQ	23:20	0x0	Channel A data and mask prebuffer slew N control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_N_DQS	27:24	0x0	Channel A strobe (nominal and complement) prebuffer slew N control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_N_XXX	31:28	0x0	Channel A spare prebuffer slew N control 0=Slow edge 15=Fast edge
Channel A prebuffer slew N control			

MCA_PREBUF_SLEW_P - RW - 32 bits - NBMCIND:0xC2			
Field Name	**Bits**	**Default**	**Description**
MCA_PREBUF_SLEW_P_CK	3:0	0x0	Channel A clock (nominal and complemenat) prebuffer slew P control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_P_CKE	7:4	0x0	Channel A CKE prebuffer slew P control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_P_CS	11:8	0x0	Channel A CS prebuffer slew P control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_P_CMD	15:12	0x0	Channel A RAS/CAS/WE and address prebuffer slew P control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_P_ODT	19:16	0x0	Channel A ODT prebuffer slew P control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_P_DQ	23:20	0x0	Channel A data and mask prebuffer slew P control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_P_DQS	27:24	0x0	Channel A strobe (nominal and complement) prebuffer slew P control 0=Slow edge 15=Fast edge
MCA_PREBUF_SLEW_P_XXX	31:28	0x0	Channel A spare prebuffer slew P control 0=Slow edge 15=Fast edge
Channel A prebuffer slew P control			

MCA_GENERAL_PURPOSE - RW - 32 bits - NBMCIND:0xC3			
Field Name	**Bits**	**Default**	**Description**
MCA_TRST_FORCE	0	0x0	Channel A all signals tristate force 0=Nominal 1=Tristate
MCA_TRST_DYNAMIC	1	0x0	Channel A all signals tristate when dynamic CKE low, except clock runing and ODT low 0=Nominal 1=Tristate
MCA_TRST_CK	2	0x0	Channel A tristate clock when tristate dynamic CKE low 0=Nominal 1=Tristate
MCA_TRST_DLL	3	0x0	Channel A reset memory DLL after exiting tristate dynamic CKE low with clock tristate 0=Do not reset memory DLL 1=Reset memory DLL
MCA_TRST_SELFREF	4	0x0	Channel A enter self refresh when tristate dynamic CKE low 0=Do not do anything 1=Enter self refresh
MCA_DQ_DQS_FORCE_TERM	5	0x0	Channel A force ASIC DQ and DQS pads termination force 0=Nominal operation, termination on during read only 1=Termination on always
MCA_DQ_DQS_FORCE_LOW	6	0x0	Channel A force ASIC DQ and DQS pads drive low 0=Nominal operation 1=Force drive low DQ/DQS

MCA_DQ_DQS_FORCE_HIGH	7	0x0	Channel A force ASIC DQ and DQS pads drive high 0=Nominal operation 1=Force drive high DQ/DQS
MCA_DLL_PWRDN	8	0x1	Channel A all DLL master power down
MCA_DLL_RESET	9	0x1	Channel A all DLL master reset
MCA_DLL_TEST	10	0x0	Channel A all DLL master test
MCA_REF_DISABLE	11	0x1	Disables refreshing when set
MCA_REF_URGENCY	15:12	0x6	Number of pending refreshes until refresh becomes urgent
MCA_IO_BIAS_CK	16	0x0	Enables MC IO CK bias current
MCA_IO_BIAS_CKE	17	0x0	Enables MC IO CKE bias current
MCA_IO_BIAS_CS	18	0x0	Enables MC IO CS bias current
MCA_IO_BIAS_CMD	19	0x0	Enables MC IO CMD bias current
MCA_IO_BIAS_ODT	20	0x0	Enables MC IO ODT bias current
MCA_IO_BIAS_DQ	21	0x0	Enables MC IO DQ bias current
MCA_IO_BIAS_DQS	22	0x0	Enables MC IO DQS bias current
MCA_IO_BIAS_XXX	23	0x0	Enables MC IO XXX bias current
MCA_REF_HI_PRI	24	0x0	Enables hi priority refreshes
MCA_DLL_BYPASS	25	0x0	Channel A all DLL bypass
MCA_ZQCX	26	0x0	Channel A nominal operation ZQC 0=ZQCS 1=ZQCL
RESERVED27	27	0x0	
MCA_REF_URGENCYX	31:28	0x8	Number of pending refreshes until refresh becomes extremely urgent
Memory controller A general purpose control			

MCA_GENERAL_PURPOSE_2 - RW - 32 bits - NBMCIND:0xC4			
Field Name	**Bits**	**Default**	**Description**
MCA_OUT_TIMING_CK_PM	2:0	0x4	Channel A clock output timing in power management mode 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
RESERVED3	3	0x0	
MCA_OUT_TIMING_CKE_PM	6:4	0x5	Channel A CKE output timing in power management mode 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
RESERVED7	7	0x0	
MCA_OUT_TIMING_CS_PM	10:8	0x5	Channel A CS output timing in power management mode 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
RESERVED11	11	0x0	

MCA_OUT_TIMING_CMD_PM	14:12	0x5	Channel A address andcommand output timing in power management mode 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
RESERVED15	15	0x0	
MCA_OUT_TIMING_ODT_PM	18:16	0x5	Channel A ODT output timing in power management mode 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
RESERVED19	19	0x0	
MCA_OUT_TIMING_DQ_PM	22:20	0x3	Channel A DQ output timing in power management mode 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
RESERVED23	23	0x0	
MCA_OUT_TIMING_DQS_PM	26:24	0x4	Channel A DQS output timing in power management mode 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
RESERVED27	27	0x0	
MCA_MX1X2X_CK_PM	29:28	0x0	Channel A clock 1 output data/mask phase range in power management mode 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
RESERVED30	31:30	0x0	
Memory controller A general purpose control 2			

MCA_OCD_CONTROL - RW - 32 bits - NBMCIND:0xC5			
Field Name	**Bits**	**Default**	**Description**
MCA_OCD_CONTROL_BYTE0	3:0	0x0	Channel A OCD control data BYTE 0
MCA_OCD_CONTROL_BYTE1	7:4	0x0	Channel A OCD control data BYTE 0
Memory controller A OCD control data			

MCA_DQ_DQS_READ_BACK - RW - 32 bits - NBMCIND:0xC6			
Field Name	**Bits**	**Default**	**Description**
MCA_READ_BACK_BYTE0 (R)	0	0x0	Channel A read back data byte 0 0=All 0 when OCD drive 0, some 0 when OCD drive 1 1=Some 1 when OCD drive 0, all 1 when OCD drive 1
MCA_READ_BACK_BYTE1 (R)	1	0x0	Channel A read back data byte 1 0=All 0 when OCD drive 0, some 0 when OCD drive 1 1=Some 1 when OCD drive 0, all 1 when OCD drive 1
MCA_READ_BACK_DQS0 (R)	8	0x0	Channel A read back strobe byte 0 0=0 1=1
MCA_READ_BACK_DQS1 (R)	9	0x0	Channel A read back strobe byte 1 0=0 1=1
MCA_READ_BACK_DQ_LSB (R)	23:16	0x0	Channel A read back data LSB bits [7:0] 0=0 1=1
MCA_READ_BACK_DQ_MSB (R)	31:24	0x0	Channel A read back data MSB bits [15:8] 0=0 1=1
Memory controller A data and strobe read back			

MCA_DQS_CLK_READ_BACK - RW - 32 bits - NBMCIND:0xC7			
Field Name	**Bits**	**Default**	**Description**
MCA_SAMPLE_RISE1_DQS0 (R)	0	0x0	Channel A read strobe 0 sampled with first internal clock rising edge
MCA_SAMPLE_RISE1_DQS1 (R)	4	0x0	Channel A read strobe 1 sampled with first internal clock rising edge
Memory controller A read strobe sampled by internal clock read back			

MCA_MEMORY_INIT_MRS_PM - RW - 32 bits - NBMCIND:0xC8			
Field Name	**Bits**	**Default**	**Description**
MCA_MODE_REG_PM	19:0	0x0	Value to be loaded in memory mode register in power management mode Bits [14:0]=ADDRESS[14:0] Bit [15]=RESERVED Bits [18:16]=BANK[2:0] Bit [19]=RESERVED
MCA_INIT_CS_MRS_PM	23:20	0xf	Channel A CS to be initialized in power management mode 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_DQ_TRANSFER_PM	27:24	0x3	Channel N read data transfer from strobe flops to core clock flops in power management mode 0=CL+0clock 1=CL+1clock 2=CL+2clock 3=CL+3clock 4=CL+4clock
MCA_DQS_ARRIVAL_PM	31:28	0x2	Channel A input strobe reset removal edge in power management mode 0=CL 1=CL+0.25 2=CL+0.50 3=CL+0.75 4=CL+1.00 5=CL+1.25 6=CL+1.50 7=CL+1.75 8=CL+2.00 9=CL+2.25 10=CL+2.50 11=CL+2.75 12=CL+3.00 13=CL+3.25 14=CL+3.50 15=CL+3.75
Memory controller A memory initialization power management			

MCA_MEMORY_INIT_EMRS_PM - RW - 32 bits - NBMCIND:0xC9			
Field Name	**Bits**	**Default**	**Description**
MCA_EXT_MODE_REG_PM	19:0	0x10000	Value to be loaded in memory mode register in power management mode. Bits [14:0]=ADDRESS[14:0] Bit [15]=RESERVED Bits [18:16]=BANK[2:0] Bit [19]=RESERVED
MCA_INIT_CS_EMRS_PM	23:20	0xf	Channel A CS to be initialized in power management mode. 4'b0001= CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_INIT_DLL_PM	24	0x1	Enables the execution of memory DLL reset mode register command for power management mode initialization sequence
MCA_CKE_DYNAMIC_PM	25	0x0	Channel A CKE dynamic in power management 0=CKE high when enabled 1=CKE dynamic when enabled, high or low depending on activity, active or precharge power down
MCA_TRST_DYNAMIC_PM	26	0x0	Channel A all signals tristate when CKE low, except clock runing and ODT low, active and precharge power down in power management mode 0=Nominal 1=Tristate
MCA_TRST_CK_PM	27	0x0	Channel A tristate clock when tristate dynamic CKE low in power management mode 0=Nominal 1=Tristate
MCA_DQ_TRANSFER_FALL_PM	28	0x0	Channel A read data transfer from strobe flops to negative edge core clock flops in power management mode. 0=Use positive edge flops 1=Use negative edge flops
MCA_ODT_STALL_PM	29	0x0	Channel A ODT stall first write in power management mode 0=No stall 1=Stall
MCA_2T_TIMING_PM	30	0x0	Channel A timing in power management mode. 0=1T timing 1=2T timing
MCA_3T_TIMING_PM	31	0x0	Channel A timing in power management mode. 0=1T timing 1=3T timing
Memory controller A memory initialization power management			

MCA_MEMORY_INIT_EMRS2_PM - RW - 32 bits - NBMCIND:0xCA			
Field Name	**Bits**	**Default**	**Description**
MCA_EXT2_MODE_REG_PM	19:0	0x20000	Value to be loaded in memory mode register in power management mode Bits [14:0]=ADDRESS[14:0] Bit [15]=RESERVED Bits [18:16]=BANK[2:0] Bit [19]=RESERVED
MCA_INIT_CS_EMRS2_PM	23:20	0xf	Channel A CS to be initialized in power management mode 4'b0001=CS0/ 4'b0010= CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_ODTR_POSITION_PM	25:24	0x0	Channel A ODT read position When ODTX 0, read latency dependent When ODTX 1, read command dependent 0=ODT start at RL-3 for ODTX 0, ODT start at RD for ODTX1 1=ODT start at RL-2 for ODTX 0, ODT start at RD+1 for ODTX 1 2= 3=
MCA_ODTR_LENGTH_PM	27:26	0x0	Channel A ODT read length in power management mode 0=ODT length BL/2+1 1=ODT length BL/2+2 2= 3=
MCA_ODTW_POSITION_PM	29:28	0x0	Channel A ODT write position When ODTX 0, write latency dependent When ODTX 1, write command dependent 0=ODT start at WL-3 for ODTX 0, ODT start at WR for ODTX1 1=ODT start at WL-2 for ODTX 0, ODT start at WR+1 for ODTX 1 2= 3=
MCA_ODTW_LENGTH_PM	31:30	0x0	Channel A ODT write length in power management mode. 0=ODT length BL/2+1 1=ODT length BL/2+2 2= 3=
Memory controller A memory initialization power management			

MCA_MEMORY_INIT_EMRS3_PM - RW - 32 bits - NBMCIND:0xCB			
Field Name	**Bits**	**Default**	**Description**
MCA_EXT3_MODE_REG_PM	19:0	0x30000	Value to be loaded in memory mode register in power management mode Bits [14:0]=ADDRESS[14:0] Bit [15]=RESERVED Bits [18:16]=BANK[2:0] Bit [19]=RESERVED
MCA_INIT_CS_EMRS3_PM	23:20	0xf	Channel A CS to be initialized in power management mode 4'b0001=CS0/ 4'b0010=CS1/ 4'b0100=CS2/ 4'b1000=CS3/
MCA_DQS_PRE_PM	25:24	0x1	Channel A strobe output preamble in power management mode 0=0.5 clock 1=1 clock 2=1.5 clock 3=2 clock
MCA_DQS_POST_PM	27:26	0x1	Channel A strobe output postamble in power management mode 0=0.5 clock 1=1 clock 2=1.5 clock 3=2 clock
MCA_DQSX_PRE_PM	28	0x0	Channel A DQS preamble pulse in power management mode 0=As set with DQS_PRE 1=One clock reduced DQS_PRE
MCA_DQSX_POST_PM	29	0x0	Channel A DQS postamble pulse in power management mode 0=As set with DQS_POST 1=One clock reduced DQS_POST
RESERVED30	31:30	0x0	
Memory controller A memory initialization power management			

MCA_TIMING_PARAMETERS_1_PM - RW - 32 bits - NBMCIND:0xCC			
Field Name	**Bits**	**Default**	**Description**
MCA_RD_LAT_PM	3:0	0x4	Memory CAS Latency 0=0 clock (not supported) 1=1 clock (not supported) 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_WR_LAT_PM	7:4	0x3	Memory Write Latency 0=0 clock (not supported) 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TRCDR_PM	11:8	0x8	Active to Read delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRCDW_PM	15:12	0x8	Active to Write delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRP_PM	19:16	0x8	Precharge command period 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRTP_PM	23:20	0x4	Internal Read to Precharge command delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock

MCA_TWR_PM	27:24	0x8	Write recovery time 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRRD_PM	31:28	0x6	Active bank A to Active bank B command period 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
Memory controller A timing parameters in power management mode, set 1			

MCA_TIMING_PARAMETERS_2_PM - RW - 32 bits - NBMCIND:0xCD			
Field Name	**Bits**	**Default**	**Description**
MCA_TRAS_PM	7:0	0x18	Active to Precharge command 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 29=29 clock 30=30 clock 31=31 clock
MCA_TRC_PM	15:8	0x20	Row Cycle time. Active to Active/Auto-Refresh command period 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 125=125 clock 126=126 clock 127=127 clock
MCA_TRFC_PM	23:16	0x28	Auto-Refresh to Active/Auto-Refresh command period 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 125=125 clock 126=126 clock 127=127 clock
MCA_TREFI_PM	31:24	0x10	1 memory refresh is performed every TREFI*64 MCLK cycles.
Memory controller A timing parameters in power management mode, set 2			

MCA_TIMING_PARAMETERS_3_PM - RW - 32 bits - NBMCIND:0xCE

Field Name	Bits	Default	Description
MCA_TRTR_CS_PM	3:0	0x1	Read to Read command to different CS 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TRTW_PM	7:4	0x2	Read to Write bus turnaround 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWTR_PM	11:8	0x4	Internal Write to Read command delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWTR_CS_PM	15:12	0x2	Write to Read command to different CS 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TWTW_CS_PM	19:16	0x1	Write to Write command to different CS 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TCCD_PM	23:20	0x2	CAS to CAS command delay 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock

MCA_TCKE_PM	27:24	0x3	CKE minimum high and low pulse width 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
MCA_TXP_PM	31:28	0x3	Exit precharge power down to any valid command 0=0 clock 1=1 clock 2=2 clock 3=3 clock 4=4 clock 5=5 clock 6=6 clock 7=7 clock
Memory controller A timing parameters in power management mode, set 3			

MCA_TIMING_PARAMETERS_4_PM - RW - 32 bits - NBMCIND:0xCF			
Field Name	**Bits**	**Default**	**Description**
MCA_TXARDS_PM	3:0	0x6	Exit active power down to read command 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TAXPD_PM	7:4	0x8	ODT power down exit latency 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TRPALL_PM	11:8	0x2	Precharge all for 8 bank memories 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock
MCA_TFAW_PM	15:12	0x2	Back to back activate rolling window 0=0 clock 1=1 clock 2=2 clock 3=3 clock … 13=13 clock 14=14 clock 15=15 clock

MCA_TZQCL_PM	19:16	0x8	Impedance calibration long timing, can be merged with DLL time, x64 clocks
MCA_TZQCS_PM	23:20	0x4	Impedance calibration short timing, x64 clocks
MCA_TZQCI_PM	27:24	0x1	Impedance calibration interval, x256 refresh cycles
MCA_TMRD_PM	31:28	0x2	Mode register set command cycle time 0=0 clock 1=1 clock ... 15=15 clock
Memory controller A timing parameters in power management mode, set 4			

MCA_IN_TIMING_DQS_3210_PM - RW - 32 bits - NBMCIND:0xD0			
Field Name	**Bits**	**Default**	**Description**
MCA_DQS_ARRIVAL_0_PM	3:0	0x2	Channel A byte 0 input strobe reset removal edge in power management mode 0=CL 1=CL+0.25 2=CL+0.50 3=CL+0.75 4=CL+1.00 5=CL+1.25 6=CL+1.50 7=CL+1.75 8=CL+2.00 9=CL+2.25 10=CL+2.50 11=CL+2.75 12=CL+3.00 13=CL+3.25 14=CL+3.50 15=CL+3.75 16=CL+4.00 17=CL+4.25
RESERVED4	7:4	0x0	
MCA_DQS_ARRIVAL_1_PM	11:8	0x2	Channel A byte 1 input strobe reset removal edge in power management mode 0=CL 1=CL+0.25 2=CL+0.50 3=CL+0.75 4=CL+1.00 5=CL+1.25 6=CL+1.50 7=CL+1.75 8=CL+2.00 9=CL+2.25 10=CL+2.50 11=CL+2.75 12=CL+3.00 13=CL+3.25 14=CL+3.50 15=CL+3.75 16=CL+4.00 17=CL+4.25
RESERVED12	15:12	0x0	
Channel A input strobe gating timing in power management mode			

MCA_OUT_TIMING_DQ_PM - RW - 32 bits - NBMCIND:0xD2			
Field Name	**Bits**	**Default**	**Description**
MCA_OUT_TIMING_DQ_B0_PM	3:0	0x3	Channel A byte 0 data and mask output timing in power management mode 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
MCA_OUT_TIMING_DQ_B1_PM	7:4	0x3	Channel A byte 1 data and mask output timing in power management mode 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
Channel A output data and mask timing in power management mode			

MCA_OUT_TIMING_DQS_PM - RW - 32 bits - NBMCIND:0xD3			
Field Name	**Bits**	**Default**	**Description**
MCA_OUT_TIMING_DQS_0_PM	3:0	0x4	Channel A byte 0 strobe output timing in power management mode 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
MCA_OUT_TIMING_DQS_1_PM	7:4	0x4	Channel A byte 1 strobe output timing in power management mode 0 = -1 clock delay 1 = -3/4 clock delay 2 = -1/2 clock delay 3 = -1/4 clock delay 4 = 0 clock delay 5 = 1/4 clock delay 6 = 1/2 clock delay 7 = 3/4 clock delay
Channel A output strobe timing in power management mode			

MCA_MX1X2X_DQ - RW - 32 bits - NBMCIND:0xD6			
Field Name	**Bits**	**Default**	**Description**
MCA_MX1X2X_DQ_B0	1:0	0x0	Channel A byte 0 output data/mask phase range 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
MCA_MX1X2X_DQ_B1	3:2	0x0	Channel A byte 1 output data/mask phase range 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
MCA_MX1X2X_DQ_B0_PM	17:16	0x0	Channel A byte 0 output data/mask phase range in power management mode 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
MCA_MX1X2X_DQ_B1_PM	19:18	0x0	Channel A byte 1 output data/mask phase range in power management mode 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
Channel A output data/mask phase range			

MCA_MX1X2X_DQS - RW - 32 bits - NBMCIND:0xD7			
Field Name	**Bits**	**Default**	**Description**
MCA_MX1X2X_DQS_0	1:0	0x0	Channel A byte 0 output strobe phase range 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Yhree quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock

MCA_MX1X2X_DQS_1	3:2	0x0	Channel A byte 1 output strobe phase range 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
MCA_MX1X2X_DQS_0_PM	17:16	0x0	Channel A byte 0 output strobe phase range in power management mode 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
MCA_MX1X2X_DQS_1_PM	19:18	0x0	Channel A byte 1 output strobe phase range in power management mode 0=Nominal, inverted 1x clock 1=Quarter clock delay, 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock 2=Half clock delay, 1x clock 3=Three quarters clock delay, inverted 1x clock sampled with 2x rising edge clock and resampled with 2x falling edge clock
Channel A output strobe phase range			

MCA_DLL_MASTER_0 - RW - 32 bits - NBMCIND:0xD8			
Field Name	**Bits**	**Default**	**Description**
MCA_DLL_ADJ_MSTR_0	7:0	0xa0	Channel A byte 0 DLL master 160 (0xA0)
MCA_DLL_TSTCTRL_0	13:8	0x0	Channel A byte 0 DLL test/control select
MCA_DLL_PWRDN_0	14	0x0	Channel A byte 0 DLL power down
MCA_DLL_RESET_0	15	0x0	Channel A byte 0 DLL reset
MCA_DLL_ADJ_MSTR_0_PM	23:16	0xa0	Channel A byte 0 DLL master in power management mode 160 (0xA0)
RESERVED24	28:24	0x0	
MCA_DLL_BYPASS_0	29	0x0	Channel A byte 0 DLL bypass
MCA_DLL_BYPASS_0_PM	30	0x0	Channel A byte 0 DLL bypass in power management mode
MCA_DLL_RESET_0_PM	31	0x0	Channel A byte 0 DLL reset in power management mode
Channel A byte 0 DLL master			

MCA_DLL_MASTER_1 - RW - 32 bits - NBMCIND:0xD9			
Field Name	**Bits**	**Default**	**Description**
MCA_DLL_ADJ_MSTR_1	7:0	0xa0	Channel A byte 1 DLL master 160 (0xA0)
MCA_DLL_TSTCTRL_1	13:8	0x0	Channel A byte 1 DLL test/control select
MCA_DLL_PWRDN_1	14	0x0	Channel A byte 1 DLL power down
MCA_DLL_RESET_1	15	0x0	Channel A byte 1 DLL reset
MCA_DLL_ADJ_MSTR_1_PM	23:16	0xa0	Channel A byte 1 DLL master in power management mode 160 (0xA0)
RESERVED24	28:24	0x0	
MCA_DLL_BYPASS_1	29	0x0	Channel A byte 1 DLL bypass
MCA_DLL_BYPASS_1_PM	30	0x0	Channel A byte 1 DLL bypass in power management mode
MCA_DLL_RESET_1_PM	31	0x0	Channel A byte 1 DLL reset in power management mode
Channel A byte 1 DLL master			

MCA_DLL_SLAVE_RD_0 - RW - 32 bits - NBMCIND:0xE0			
Field Name	**Bits**	**Default**	**Description**
MCA_DLL_ADJ_DQSR_0	7:0	0x38	Channel A byte 0 input strobe rising edge phase 56 (0x38), half 2x, quarter 1x 136 (0x88), full 2x, half 1x
MCA_DLL_ADJ_DQSR_0_PM	23:16	0x38	Channel A byte 0 input strobe rising edge phase in power management mode 56 (0x38), half 2x, quarter 1x 136 (0x88), full 2x, half 1x
Channel A byte 0 input strobe phase			

MCA_DLL_SLAVE_RD_1 - RW - 32 bits - NBMCIND:0xE1			
Field Name	**Bits**	**Default**	**Description**
MCA_DLL_ADJ_DQSR_1	7:0	0x38	Channel A byte 1 input strobe rising edge phase 56 (0x38), half 2x, quarter 1x 136 (0x88), full 2x, half 1x
MCA_DLL_ADJ_DQSR_1_PM	23:16	0x38	Channel A byte 1 input strobe rising edge phase in power management mode 56 (0x38), half 2x, quarter 1x 136 (0x88), full 2x, half 1x
Channel A byte 1 input strobe phase			

MCA_DLL_SLAVE_WR_0 - RW - 32 bits - NBMCIND:0xE8			
Field Name	**Bits**	**Default**	**Description**
MCA_DLL_ADJ_DQ_B0	7:0	0x38	Channel A byte 0 data and mask output phase 56 (0x38), half 2x, quarter 1x 136 (0x88), full 2x, half 1x
MCA_DLL_ADJ_DQ_B0_PM	23:16	0x38	Channel A byte 0 data and mask output phase in power management mode 56 (0x38), half 2x, quarter 1x 136 (0x88), full 2x, half 1x
Channel A byte 0 output phase			

MCA_DLL_SLAVE_WR_1 - RW - 32 bits - NBMCIND:0xE9			
Field Name	**Bits**	**Default**	**Description**
MCA_DLL_ADJ_DQ_B1	7:0	0x38	Channel A byte 1 data and mask output phase 56 (0x38), half 2x, quarter 1x 136 (0x88), full 2x, half 1x
MCA_DLL_ADJ_DQ_B1_PM	23:16	0x38	Channel A byte 1 data and mask output phase in power management mode 56 (0x38), half 2x, quarter 1x 136 (0x88), full 2x, half 1x
Channel A byte 1 output phase			

MCA_RESERVED_0 - RW - 32 bits - NBMCIND:0xF0			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_1 - RW - 32 bits - NBMCIND:0xF1			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_2 - RW - 32 bits - NBMCIND:0xF2			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_3 - RW - 32 bits - NBMCIND:0xF3			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_4 - RW - 32 bits - NBMCIND:0xF4			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_5 - RW - 32 bits - NBMCIND:0xF5			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_6 - RW - 32 bits - NBMCIND:0xF6			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

MCA_RESERVED_7 - RW - 32 bits - NBMCIND:0xF7			
Field Name	**Bits**	**Default**	**Description**
RESERVED	31:0	0x0	
Memory controller reserved for future use			

2.13 Northbridge Miscellaneous Indirect Registers

NB_CNTL - RW - 32 bits - NBMISCIND:0x0			
Field Name	**Bits**	**Default**	**Description**
HIDE_NB_AGP_CAP	0	0x0	Lower 32 bits of HTIU performance counter 0 0=Visible (Enable) 1=Hide (Disable)
HIDE_P2P_AGP_CAP	1	0x1	0=Visible (Enable) 1=Hide (Disable)
HIDE_NB_GART_BAR	2	0x0	0=Visible (Enable) 1=Hide (Disable)
HIDE_MMCFG_BAR	3	0x0	0=Visible (Enable) 1=Hide (Disable)
AGPMODE30	4	0x0	0=Disable 1=Enable AGP3.0 REGISTER MODE
AGP30ENHANCED	5	0x0	0=Disable 1=Enable ENHANCED AGP3.0 MODE
NB_SB_CFG_EN	6	0x0	0=Disable 1=Enable
HWINIT_WR_LOCK	7	0x0	0=Disable 1=Enable
STRAP_MSI_ENABLE	10	0x1	0=Disable 1=Enable
TESTMODE_ENABLE (R)	13	0x0	
COM_PORT_MODE (R)	14	0x0	
ROM_CTRL_POST	31:16	0x0	
HTIU performance counter 0			

NB_IOC_DEBUG - RW - 32 bits - NBMISCIND:0x1			
Field Name	**Bits**	**Default**	**Description**
SLI_OVERWRITE_EN	0	0x0	
NB_IOC_DEBUG_RW	15:1	0x0	
IOC_MultiReqVldErr (R)	16	0x0	
IOC_MemMapCfgErr (R)	17	0x0	
NB_IOC_DEBUG_RO (R)	31:18	0x0	

NB_SPARE1 - RW - 32 bits - NBMISCIND:0x2			
Field Name	**Bits**	**Default**	**Description**
NB_SPARE1_RW	15:0	0x0	
NB_SPARE1_RO (R)	31:16	0x0	

NB_STRAPS_READBACK_MUX - RW - 32 bits - NBMISCIND:0x3			
Field Name	**Bits**	**Default**	**Description**
SELECT	7:0	0x0	

NB_STRAPS_READBACK_DATA - R - 32 bits - NBMISCIND:0x4			
Field Name	**Bits**	**Default**	**Description**
READ	31:0	0x0	

DFT_CNTL0 - RW - 32 bits - NBMISCIND:0x5			
Field Name	**Bits**	**Default**	**Description**
TEST_DEBUG_EN	0	0x0	
SCAN_DEBUG_BUS_SELECT	4:1	0x0	
TEST_DEBUG_OUT_EN	8:5	0x0	
EN_GFX_NB_DUAL_OUT	9	0x0	
NB_DUAL_OUT_SELECT	10	0x0	
GFX_DUAL_OUT_SELECT	11	0x0	
GFX_DEBUG_OUT_SELECT	12	0x0	
NB_GFX_OUT_SELECT	13	0x0	
UVD_JTAG_MODE	14	0x0	
DC_TEST_DEBUG_OVERRIDE	15	0x0	
GPIO_DEBUG_BUS_MUX_SEL0	19:16	0x0	
GPIO_DEBUG_BUS_MUX_SEL1	23:20	0x1	
GPIO_DEBUG_BUS_MUX_SEL2	27:24	0x2	
GPIO_DEBUG_BUS_MUX_SEL3	31:28	0x3	

DFT_CNTL1 - RW - 32 bits - NBMISCIND:0x6			
Field Name	**Bits**	**Default**	**Description**
TEST_DEBUG_COUNTER_EN	0	0x0	
TEST_DEBUG_IN_EN	1	0x0	
DEBUG_TESTCLKIN	2	0x0	
TEST_CLK0_INV	3	0x0	
DFT_MISC	14:4	0x0	
DEBUG_BUS_LOCK_EN	15	0x0	
COM_PORT_OE	17:16	0x0	
COM_PORT_OUT	19:18	0x0	
COM_PORT_IN (R)	20	0x0	

PCIE_PDNB_CNTL - RW - 32 bits - NBMISCIND:0x7			
Field Name	**Bits**	**Default**	**Description**
ENABLE_CLKGATE_GFX_TXCLK	0	0x0	
ENABLE_CLKGATE_GFX_TXCLK_L0S	1	0x0	
ENABLE_CLKGATE_GFX_TXCLK_SND_RCV	2	0x0	
GFX_PERM2_TXCLK_STOP	3	0x0	
ENABLE_CLKGATE_GPPSB_TXCLK	4	0x0	
ENABLE_CLKGATE_GPPSB_TXCLK_L0S	5	0x0	
ENABLE_CLKGATE_GPPSB_TXCLK_SND_RCV	6	0x0	
GPPSB_PERM2_TXCLK_STOP	7	0x0	
ENABLE_CLKGATE_GPP_TXCLK	8	0x0	

ENABLE_CLKGATE_GPP_TXCLK_L0S	9	0x0	
ENABLE_CLKGATE_GPP_TXCLK_SND_RCV	10	0x0	
GPP_PERM2_TXCLK_STOP	11	0x0	
GFX_TXCLK_SND_RCV_0_SEL	12	0x0	
GFX_TXCLK_SND_RCV_1_SEL	13	0x0	
GFX_TXCLK_SND_RCV_2_SEL	14	0x0	
GFX_TXCLK_SND_RCV_3_SEL	15	0x0	
GFX_TXCLK_SEL	16	0x0	
SPARE	19:17	0x0	
IO_TXCLK_A_SEL	21:20	0x0	
IO_TXCLK_B_SEL	23:22	0x0	
IO_TXCLK_C_SEL	25:24	0x0	
DISP_FIFO_RCLK0_SEL	28:26	0x0	
DISP_FIFO_RCLK1_SEL	31:29	0x0	

PCIE_LINK_CFG - RW - 32 bits - NBMISCIND:0x8			
Field Name	**Bits**	**Default**	**Description**
SW_RESET_DURATION_GFX	1:0	0x0	
ATOMIC_SW_RESET_GFX	2	0x0	
RST_cor_reset_GFX	3	0x0	
HOLD_TRAIN0_GFX	4	0x1	0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN1_GFX	5	0x1	0=Allow Link Training 1=Hold (Prevent) Link Training
RST_reg_reset_GFX	6	0x0	
RST_phy_reset_GFX	7	0x0	
MULTIPORT_CONFIG_GFX	11:8	0x0	0=Port A only 1=Port A and Port B
RESERVED_GFX	12	0x0	
RST_sty_reset_GFX	13	0x0	
CALIB_RESET_GFX	14	0x0	0=Disable 1=Enable
GLOBAL_RESET_GFX	15	0x0	0=Disable 1=Enable
SW_RESET_DURATION_GPPSB	17:16	0x0	
ATOMIC_SW_RESET_GPPSB	18	0x0	
RST_cor_reset_GPPSB	19	0x0	
HOLD_TRAIN0_GPPSB	20	0x0	0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN1_GPPSB	21	0x1	0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN2_GPPSB	22	0x1	0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN3_GPPSB	23	0x1	0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN4_GPPSB	24	0x1	0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN5_GPPSB	25	0x1	0=Allow Link Training 1=Hold (Prevent) Link Training
HOLD_TRAIN6_GPPSB	26	0x1	0=Allow Link Training 1=Hold (Prevent) Link Training
RST_reg_reset_GPPSB	27	0x0	
RST_phy_reset_GPPSB	28	0x0	
RST_sty_reset_GPPSB	29	0x0	
CALIB_RESET_GPPSB	30	0x0	0=Disable 1=Enable
GLOBAL_RESET_GPPSB	31	0x0	0=Disable 1=Enable

IOC_DMA_ARBITER - RW - 32 bits - NBMISCIND:0x9			
Field Name	**Bits**	**Default**	**Description**
DMA_ARBITER	31:0	0x0	

IOC_PCIE_CSR_Count - RW - 32 bits - NBMISCIND:0xA			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_CNTL - RW - 32 bits - NBMISCIND:0xB			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
C3STPCLKDectecEn	4	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	
IOC_SB_SetPowEn	21	0x0	
IOC_SetDMAInValidEn	22	0x1	
IOC_SB_SetPMETurnOffEn	23	0x0	
LockOrderingByPassDisable	24	0x0	
DMAInvalidMode	26	0x0	
CfgDat_Enable_NS_Ordering	27	0x0	
CrsIDRdEn	28	0x0	0=Enable 1=Disable

IOC_P2P_CNTL - RW - 32 bits - NBMISCIND:0xC			
Field Name	**Bits**	**Default**	**Description**
Dev2BridgeDis	2	0x0	
Dev3BridgeDis	3	0x0	
Dev4BridgeDis	4	0x0	
Dev5BridgeDis	5	0x0	
Dev6BridgeDis	6	0x0	
Dev7BridgeDis	7	0x0	
GfxMetaCtl	8	0x1	
SBMetaCtl	9	0x1	
MsgMetaCtl	10	0x1	
DLDownResetEn	11	0x0	
NonDev0ToSBEn	12	0x1	
GSMEnable	13	0x0	
BMREQPinEnable	14	0x0	
Dev9BridgeDis	16	0x0	
Dev10BridgeDis	17	0x0	
Dev11BridgeDis	18	0x0	
Dev12BridgeDis	19	0x0	

IOCIsocMapAddr_LO - RW - 32 bits - NBMISCIND:0xE			
Field Name	**Bits**	**Default**	**Description**
IsocMapAdd_LO	31:6	0x0	

IOCIsocMapAddr_HI - RW - 32 bits - NBMISCIND:0xF			
Field Name	**Bits**	**Default**	**Description**
IsocMapAdd_HI	7:0	0x0	

DFT_CNTL2 - RW - 32 bits - NBMISCIND:0x10			
Field Name	**Bits**	**Default**	**Description**
TEST_DEBUG_READBACK (R)	15:0	0x0	
AUX_DEBUG_BUS_MUX_SEL0	19:16	0x4	
AUX_DEBUG_BUS_MUX_SEL1	23:20	0x5	
AUX_DEBUG_BUS_MUX_SEL2	27:24	0x6	
AUX_DEBUG_BUS_MUX_SEL3	31:28	0x7	

NB_BUS_NUM_CNTL - RW - 32 bits - NBMISCIND:0x11			
Field Name	**Bits**	**Default**	**Description**
NB_BUS_NUM	7:0	0x0	
NB_BUS_LAT_Mode	8	0x0	

PCIE_CORE_ARB - RW - 32 bits - NBMISCIND:0x12			
Field Name	**Bits**	**Default**	**Description**
PCIE_GFX_ARB	15:0	0x5555	
PCIE_GPPSB_ARB	31:16	0x5555	

NB_TOM_PCI - RW - 32 bits - NBMISCIND:0x16			
Field Name	**Bits**	**Default**	**Description**
SAME_AS_TOM_BIU	0	0x1	
TOM_FOR_PCI	31:16	0x0	

NB_MMIOBASE - RW - 32 bits - NBMISCIND:0x17			
Field Name	**Bits**	**Default**	**Description**
MMIOBASE	31:8	0x0	

NB_MMIOLIMIT - RW - 32 bits - NBMISCIND:0x18			
Field Name	**Bits**	**Default**	**Description**
MMIOLIMIT	31:8	0x0	

NB_BIF_SPARE - RW - 32 bits - NBMISCIND:0x1E			
Field Name	**Bits**	**Default**	**Description**
CFG_BIF_SPARE	31:0	0x0	[31:10]=Unused [9]=MSI_BE_FIX_DIS (A12) [8]=CFG_BIF_BIOS_ROM_EN [7]=BIF_MEM_AP_SIZE_STRAP_SEL [6]=BIF_AUDIO_EN_STRAP_SEL [5]=RCU_BIF_config_done [4]=SLV_BD_RAD_FORCE_EN [3]=SLV_BD_RAD_MWr4_DIS [2]=SLV_BD_RAD_MWr3_DIS [1]=CFG_BIF_MSI_EN [0]=reg_BIF_RST_DIS

NB_INTERRUPT_PIN - RW - 32 bits - NBMISCIND:0x1F			
Field Name	**Bits**	**Default**	**Description**
REG_AP_SIZE	1:0	0x1	
GFX_INTERRUPT_PIN	2	0x0	
F2_INTERRUPT_PIN	3	0x0	
CFG_GC_IO_BAR_DIS	4	0x0	
CFG_GC_64BAR_EN_A	5	0x0	
CFG_GC_NONLEGACY_DEVICE_TYPE_EN	6	0x0	
BIF_PCIE_EN	7	0x0	

NB_PROG_DEVICE_REMAP_0 - RW - 32 bits - NBMISCIND:0x20			
Field Name	**Bits**	**Default**	**Description**
NB_PROG_DEVMAP_EN	0	0x0	
IOC_PCIE_Dev_Remap_Dis	1	0x1	
GPP_PORT2_DEVMAP	7:4	0x0	
GPP_PORT3_DEVMAP	11:8	0x0	
GPP_PORT4_DEVMAP	15:12	0x0	
GPP_PORT5_DEVMAP	19:16	0x0	
GPP_PORT6_DEVMAP	23:20	0x0	
GPP_PORT7_DEVMAP	27:24	0x0	
GPP_PORT9_DEVMAP	31:28	0x0	

NB_PROG_DEVICE_REMAP_1 - RW - 32 bits - NBMISCIND:0x21			
Field Name	**Bits**	**Default**	**Description**
GPP_PORT10_DEVMAP	3:0	0x0	
GPP_PORT11_DEVMAP	7:4	0x0	
GPP_PORT12_DEVMAP	11:8	0x0	

IOC_LAT_PERF_CNTR_CNTL - RW - 32 bits - NBMISCIND:0x30			
Field Name	**Bits**	**Default**	**Description**
LAT_PERF_CNTR_EN	0	0x0	
LAT_PERF_CNTR_FREEZE	1	0x0	
LAT_PERF_PATH_SEL	4:2	0x0	
LAT_PERF_CNTR_SEL	7:5	0x0	

IOC_LAT_PERF_CNTR_OUT - R - 32 bits - NBMISCIND:0x31			
Field Name	**Bits**	**Default**	**Description**
LAT_PERF_CNTR	31:0	0x0	

PCIE_NBCFG_REG2 - RW - 32 bits - NBMISCIND:0x32			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_31to0	31:0	0x1	

PCIE_NBCFG_REG3 - RW - 32 bits - NBMISCIND:0x33			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_63to32	31:0	0x0	

PCIE_NBCFG_REG4 - RW - 32 bits - NBMISCIND:0x34			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_95to64	31:0	0xcbfa0022	

PCIE_NBCFG_REG5 - RW - 32 bits - NBMISCIND:0x35			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_127to96	31:0	0x18ca887	

PCIE_NBCFG_REG6 - RW - 32 bits - NBMISCIND:0x36			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_159to128	31:0	0xc63	

PCIE_NBCFG_REG7 - RW - 32 bits - NBMISCIND:0x37			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_191to160	31:0	0x200000	

PCIE_NBCFG_REG8 - RW - 32 bits - NBMISCIND:0x38			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_223to192	31:0	0x94c3396	

PCIE_NBCFG_REG9 - RW - 32 bits - NBMISCIND:0x39			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_255to224	31:0	0xb0b01c00	
PCIE_NBCFG_REG_255to224	31:0	0xb0b01c00	

PCIE_NBCFG_REGA - RW - 32 bits - NBMISCIND:0x22			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_287to256	31:0	0x78	

PCIE_NBCFG_REGB - RW - 32 bits - NBMISCIND:0x23			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_319to288	31:0	0x8001600	

PCIE_NBCFG_REGC - RW - 32 bits - NBMISCIND:0x24			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_351to320	31:0	0x5af80a2e	

PCIE_NBCFG_REGD - RW - 32 bits - NBMISCIND:0x25			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_383to352	31:0	0x46300500	

PCIE_NBCFG_REGE - RW - 32 bits - NBMISCIND:0x26			
Field Name	**Bits**	**Default**	**Description**
PCIE_NBCFG_REG_415to384	31:0	0x6	

PCIE_NBCFG_REGF - RW - 32 bits - NBMISCIND:0x27			
Field Name	**Bits**	**Default**	**Description**
PCIE_TX_MUX_LEVEL1_0	0	0x0	
PCIE_TX_MUX_LEVEL1_1	1	0x0	
PCIE_TX_MUX_LEVEL1_2	2	0x0	
PCIE_TX_MUX_LEVEL1_3	3	0x0	
PCIE_TX_MUX_LEVEL2_0	4	0x0	

PCIE_TX_MUX_LEVEL2_1	5	0x0	
PCIE_TX_MUX_LEVEL2_2	6	0x0	
PCIE_TX_MUX_LEVEL2_3	7	0x0	
PCIE_RX_MUX_SEL0	9:8	0x0	
PCIE_RX_MUX_SEL1	11:10	0x0	
PCIE_RX_MUX_SEL2	13:12	0x0	
PCIE_RX_MUX_SEL3	15:14	0x0	
REG_B_P90TX_DRV_STR_A	17:16	0x0	
REG_B_P90TX_DRV_STR_B	19:18	0x0	
REG_B_P90TX_DRV_STR_C	21:20	0x0	
REG_B_PG2TX_CLK_DIV_A	24:22	0x0	
REG_B_PG2TX_CLK_DIV_B	27:25	0x0	
REG_B_PG2TX_CLK_DIV_C	30:28	0x0	
PCIE_DISP_FIFO_NChg3En	31	0x0	

PCIE_NBCFG_REG10 - RW - 32 bits - NBMISCIND:0x28

Field Name	Bits	Default	Description
Reg_Turn_Off_Both_PLLs	1:0	0x1	
WRESET_FIFO1	2	0x0	
RRESET_FIFO1	3	0x0	
WRESET_FIFO2	4	0x0	
RRESET_FIFO2	5	0x0	
B_PREFCLK_SEL_A	7:6	0x0	
B_PREFCLK_SEL_B	9:8	0x0	
B_PREFCLK_SEL_C	11:10	0x0	
DISP_LINK_CLK_SEL	13:12	0x0	
PCIE_TX_MUX_LEVEL0	14	0x0	
SPARE0	15	0x0	
PCIE_DDI_MUX_LEVEL0_1	16	0x0	
PCIE_DDI_MUX_LEVEL0_2	17	0x0	
PCIE_DDI_MUX_LEVEL1_0	18	0x0	
PCIE_DDI_MUX_LEVEL1_1	19	0x0	
PCIE_DDI_MUX_LEVEL1_2	20	0x0	
PCIE_DDI_MUX_LEVEL1_3	21	0x0	
REG_B_PRX_PDNB_D	22	0x0	
PCIE_DISP_FIFO_CfgDualLink	23	0x0	
SDVO_CLK_lane3_SEL	24	0x0	
SDVO_CLK_lane7_SEL	25	0x0	
SDVO_CLK_lane11_SEL	26	0x0	
SDVO_CLK_lane12_SEL	27	0x0	
SPARE	29:28	0x0	
REG_B_PTX_BYPASS_EN_A2	30	0x0	
REG_B_PTX_BYPASS_EN_B2	31	0x0	

PCIE_NBCFG_REG11 - RW - 32 bits - NBMISCIND:0x29

Field Name	Bits	Default	Description
REG_B_PTX_CM_HIGHI_A	3:0	0x0	
REG_B_PTX_EN_A	4	0x0	
REG_B_PTX_PDNB_A	5	0x0	
REG_B_PRX_PDNB_A	6	0x0	
REG_B_P90PLL_CLKF_A	13:7	0x0	
REG_B_PG2RX_CLK_DIV_A	15:14	0x0	
REG_B_P90PLL_IBIAS_A	25:16	0x0	
REG_B_PPLL_PDNB_A	26	0x0	
REG_B_PG2PLL_TMDS_MODE_A	27	0x0	
REG_B_PTX_BYPASS_EN_A	28	0x0	
REG_B_PG2PLL_1X_CLK_DIV_A	31:29	0x0	

PCIE_NBCFG_REG12 - RW - 32 bits - NBMISCIND:0x2A			
Field Name	**Bits**	**Default**	**Description**
REG_B_PTX_CM_HIGHI_B	3:0	0x0	
REG_B_PTX_EN_B	4	0x0	
REG_B_PTX_PDNB_B	5	0x0	
REG_B_PRX_PDNB_B	6	0x0	
REG_B_P90PLL_CLKF_B	13:7	0x0	
REG_B_PG2RX_CLK_DIV_B	15:14	0x0	
REG_B_P90PLL_IBIAS_B	25:16	0x0	
REG_B_PPLL_PDNB_B	26	0x0	
REG_B_PG2PLL_TMDS_MODE_B	27	0x0	
REG_B_PTX_BYPASS_EN_B	28	0x0	
REG_B_PG2PLL_1X_CLK_DIV_B	31:29	0x0	

PCIE_NBCFG_REG13 - RW - 32 bits - NBMISCIND:0x2B			
Field Name	**Bits**	**Default**	**Description**
REG_B_PTX_CM_HIGHI_C	3:0	0x0	
REG_B_PTX_EN_C	4	0x0	
REG_B_PTX_PDNB_C	5	0x0	
REG_B_PRX_PDNB_C	6	0x0	
REG_B_P90PLL_CLKF_C	13:7	0x0	
REG_B_PG2RX_CLK_DIV_C	15:14	0x0	
REG_B_P90PLL_IBIAS_C	25:16	0x0	
REG_B_PPLL_PDNB_C	26	0x0	
REG_B_PG2PLL_TMDS_MODE_C	27	0x0	
REG_B_PTX_BYPASS_EN_C	28	0x0	
REG_B_PG2PLL_1X_CLK_DIV_C	31:29	0x0	

PCIE_NBCFG_REG14 - RW - 32 bits - NBMISCIND:0x2C			
Field Name	**Bits**	**Default**	**Description**
REG_B_P90TX_DEEMPH_STR_A	7:0	0x0	
REG_B_P90TX_DEEMPH_STR_B	15:8	0x0	
REG_B_P90TX_DEEMPH_STR_C	23:16	0x0	
REG_B_PTX_DEEMPH_EN_A	24	0x0	
REG_B_PTX_DEEMPH_EN_B	25	0x0	
REG_B_PTX_DEEMPH_EN_C	26	0x0	
REG_B_PRX_NC_DATA_EN_0	27	0x0	
REG_B_PRX_NC_DATA_EN_15	28	0x0	
REG_B_PTX_BYPASS_EN_D	29	0x0	
RX_ASRT_DET_CNTL_INT_EN_CH0	30	0x0	
RX_ASRT_DET_CNTL_INT_EN_CH1	31	0x0	

PCIE_NBCFG_REG17 - RW - 32 bits - NBMISCIND:0x2F			
Field Name	**Bits**	**Default**	**Description**
REG_B_P90PLL_CLKR_A	4:0	0x0	
REG_B_P90PLL_CLKR_B	9:5	0x0	
REG_B_P90PLL_CLKR_C	14:10	0x0	
SPARE	15	0x0	
B_PTX_PDNB_0	16	0x1	

B_PTX_PDNB_1	17	0x1	
B_PTX_PDNB_2	18	0x1	
B_PTX_PDNB_3	19	0x1	
B_PTX_PDNB_4	20	0x1	
B_PTX_PDNB_5	21	0x1	
B_PTX_PDNB_6	22	0x1	
B_PTX_PDNB_7	23	0x1	
B_PTX_PDNB_8	24	0x1	
B_PTX_PDNB_9	25	0x1	
B_PTX_PDNB_10	26	0x1	
B_PTX_PDNB_11	27	0x1	
B_PTX_PDNB_12	28	0x1	
B_PTX_PDNB_13	29	0x1	
B_PTX_PDNB_14	30	0x1	
B_PTX_PDNB_15	31	0x1	

PCIE_NBCFG_REG15 - RW - 32 bits - NBMISCIND:0x2D

Field Name	Bits	Default	Description
SW_RESET_DURATION_GPP	1:0	0x0	
ATOMIC_SW_RESET_GPP	2	0x0	
RST_cor_reset_GPP	3	0x0	
HOLD_TRAIN0_GPP	4	0x1	
HOLD_TRAIN1_GPP	5	0x1	
RESERVED	6	0x0	
LINK_CONFIG	10:7	0x3	
RST_reg_reset_GPP	11	0x0	
RST_phy_reset_GPP	12	0x0	
RST_sty_reset_GPP	13	0x0	
CALIB_RESET_GPP	14	0x0	
GLOBAL_RESET_GPP	15	0x0	
RX_ASRT_DET_CNTL_INT_DEASRT_COUNT	23:16	0x0	
RX_ASRT_DET_CNTL_INT_ASRT_COUNT	31:24	0x0	

PCIE_NBCFG_REG16 - RW - 32 bits - NBMISCIND:0x2E

Field Name	Bits	Default	Description
B_PPLL_PDNB_FEN_GFX_A	0	0x0	
B_PPLL_PDNB_FEN_GFX_B	1	0x0	
B_PPLL_PDNB_FEN_GFX_C	2	0x0	
SPARE0	3	0x0	
B_PPLL_PDNB_FDIS_GFX_A	4	0x0	
B_PPLL_PDNB_FDIS_GFX_B	5	0x0	
B_PPLL_PDNB_FDIS_GFX_C	6	0x0	
SPARE1	7	0x0	
B_P90PLL_BUF_PDNB_TX_FEN_GFX_A	8	0x0	
B_P90PLL_BUF_PDNB_TX_FEN_GFX_B	9	0x0	
B_P90PLL_BUF_PDNB_TX_FEN_GFX_C	10	0x0	
SPARE2	11	0x0	
B_P90PLL_BUF_PDNB_RX_FEN_GFX_A	12	0x0	
B_P90PLL_BUF_PDNB_RX_FEN_GFX_B	13	0x0	
B_P90PLL_BUF_PDNB_RX_FEN_GFX_C	14	0x0	

SPARE3	15	0x0	
B_P90PLL_BUF_PDNB_TX_FDIS_GFX_A	16	0x0	
B_P90PLL_BUF_PDNB_TX_FDIS_GFX_B	17	0x0	
B_P90PLL_BUF_PDNB_TX_FDIS_GFX_C	18	0x0	
SPARE4	19	0x0	
B_P90PLL_BUF_PDNB_RX_FDIS_GFX_A	20	0x0	
B_P90PLL_BUF_PDNB_RX_FDIS_GFX_B	21	0x0	
B_P90PLL_BUF_PDNB_RX_FDIS_GFX_C	22	0x0	
B_PPLL_PDNB_FEN_GPPSB	23	0x0	
B_P90PLL_BUF_PDNB_TX_FEN_GPPSB	24	0x0	
B_P90PLL_BUF_PDNB_RX_FEN_GPPSB	25	0x0	
B_PPLL_PDNB_FEN_GPP	26	0x0	
B_PPLL_PDNB_FDIS_GPP	27	0x0	
B_P90PLL_BUF_PDNB_TX_FEN_GPP	28	0x0	
B_P90PLL_BUF_PDNB_RX_FEN_GPP	29	0x0	
B_P90PLL_BUF_PDNB_TX_FDIS_GPP	30	0x0	
B_P90PLL_BUF_PDNB_RX_FDIS_GPP	31	0x0	

NB_BROADCAST_BASE_LO - RW - 32 bits - NBMISCIND:0x3A

Field Name	Bits	Default	Description
GPU_FB_BROADCAST_BASE_LO	31:20	0x0	

NB_BROADCAST_BASE_HI - RW - 32 bits - NBMISCIND:0x3B

Field Name	Bits	Default	Description
GPU_FB_BROADCAST_BASE_HI	31:0	0x0	

NB_BROADCAST_CNTL - RW - 32 bits - NBMISCIND:0x3C

Field Name	Bits	Default	Description
GPU_FB_BROADCAST_SIZE	7:0	0x0	
GPU_FB_BROADCAST_PRIMARY	8	0x0	
GPU_FB_BROADCAST_EN	9	0x0	
GPU_FB_BROADCAST_OFFSET	31:12	0x0	

NB_APIC_P2P_CNTL - RW - 32 bits - NBMISCIND:0x3D

Field Name	Bits	Default	Description
APIC_D2_Enable	0	0x0	
APIC_D3_Enable	1	0x0	
APIC_D4_Enable	2	0x0	
APIC_D5_Enable	3	0x0	
APIC_D6_Enable	4	0x0	

APIC_D7_Enable	5	0x0	
APIC_D9_Enable	6	0x0	
APIC_D10_Enable	7	0x0	
APIC_D11_Enable	8	0x0	
APIC_D12_Enable	9	0x0	

NB_APIC_P2P_RANGE_0 - RW - 32 bits - NBMISCIND:0x3E			
Field Name	**Bits**	**Default**	**Description**
APIC_D2_Range	7:0	0x0	
APIC_D3_Range	15:8	0x0	
APIC_D4_Range	23:16	0x0	
APIC_D5_Range	31:24	0x0	

NB_APIC_P2P_RANGE_1 - RW - 32 bits - NBMISCIND:0x3F			
Field Name	**Bits**	**Default**	**Description**
APIC_D6_Range	7:0	0x0	
APIC_D7_Range	15:8	0x0	
APIC_D9_Range	23:16	0x0	
APIC_D10_Range	31:24	0x0	

GPIO_PAD - RW - 32 bits - NBMISCIND:0x40			
Field Name	**Bits**	**Default**	**Description**
GPIO_TMDS_HPD_OR	0	0x0	
GPIO_DDC_DATA_OR	1	0x0	
GPIO_I2C_CLK_OR	2	0x0	
GPIO_I2C_DATA_OR	3	0x0	
GPIO_STRP_DATA_OR	4	0x0	
GPIO_DAC_SDA_OR	5	0x0	
GPIO_DAC_HSYNC_OR	6	0x0	
GPIO_DAC_VSYNC_OR	7	0x0	
GPIO_LVDS_ENA_BL_OR	8	0x0	
GPIO_LVDS_DIGON_OR	9	0x0	
GPIO_LVDS_BLON_OR	10	0x0	
GPIO_CPU_SLPb_OR	11	0x0	
GPIO_HPD_OR	12	0x0	
PAD_0_spare_15_13	15:13	0x0	
GPIO_TMDS_HPD_A	16	0x0	
GPIO_DDC_DATA_A	17	0x0	
GPIO_I2C_CLK_A	18	0x0	
GPIO_I2C_DATA_A	19	0x0	
GPIO_STRP_DATA_A	20	0x0	
GPIO_DAC_SDA_A	21	0x0	
GPIO_DAC_HSYNC_A	22	0x0	
GPIO_DAC_VSYNC_A	23	0x0	
GPIO_LVDS_ENA_BL_A	24	0x0	
GPIO_LVDS_DIGON_A	25	0x0	
GPIO_LVDS_BLON_A	26	0x0	
GPIO_CPU_SLPb_A	27	0x0	
GPIO_HPD_A	28	0x0	
PAD_0_spare_31_29	31:29	0x0	

GPIO_PAD_CNTL_PU_PD - RW - 32 bits - NBMISCIND:0x41			
Field Name	**Bits**	**Default**	**Description**
GPIO_TMDS_HPD_PU	0	0x1	
GPIO_DDC_DATA_PU	1	0x1	
GPIO_I2C_CLK_PU	2	0x1	
GPIO_I2C_DATA_PU	3	0x1	
GPIO_STRP_DATA_PU	4	0x1	
GPIO_DAC_SDA_PU	5	0x1	
GPIO_DAC_HSYNC_PU	6	0x1	
GPIO_DAC_VSYNC_PU	7	0x1	
GPIO_LVDS_ENA_BL_PU	8	0x1	
GPIO_LVDS_DIGON_PU	9	0x1	
GPIO_LVDS_BLON_PU	10	0x1	
GPIO_CPU_SLPb_PU	11	0x1	
GPIO_HPD_PU	12	0x1	
spare_15_13	15:13	0x0	
GPIO_TMDS_HPD_PD	16	0x0	
GPIO_DDC_DATA_PD	17	0x0	
GPIO_I2C_CLK_PD	18	0x0	
GPIO_I2C_DATA_PD	19	0x0	
GPIO_STRP_DATA_PD	20	0x0	
GPIO_DAC_SDA_PD	21	0x0	
GPIO_DAC_HSYNC_PD	22	0x0	
GPIO_DAC_VSYNC_PD	23	0x0	
GPIO_LVDS_ENA_BL_PD	24	0x0	
GPIO_LVDS_DIGON_PD	25	0x0	
GPIO_LVDS_BLON_PD	26	0x0	
GPIO_CPU_SLPb_PD	27	0x0	
GPIO_HPD_PD	28	0x0	
spare_31_29	31:29	0x0	

GPIO_PAD_SCHMEM_OE - RW - 32 bits - NBMISCIND:0x42			
Field Name	**Bits**	**Default**	**Description**
GPIO_TMDS_HPD_SCHMEN	0	0x1	
GPIO_DDC_DATA_SCHMEN	1	0x1	
GPIO_I2C_CLK_SCHMEN	2	0x1	
GPIO_I2C_DATA_SCHMEN	3	0x1	
GPIO_STRP_DATA_SCHMEN	4	0x1	
GPIO_DAC_SDA_SCHMEN	5	0x1	
GPIO_DAC_HSYNC_SCHMEN	6	0x1	
GPIO_DAC_VSYNC_SCHMEN	7	0x1	
GPIO_LVDS_ENA_BL_SCHMEN	8	0x1	
GPIO_LVDS_DIGON_SCHMEN	9	0x1	
GPIO_LVDS_BLON_SCGMEN	10	0x1	
GPIO_CPU_SLPb_SCHMEN	11	0x1	
GPIO_HPD_SCHMEN	12	0x1	
spare_15_13	15:13	0x0	
GPIO_TMDS_HPD_OE	16	0x0	
GPIO_DDC_DATA_OE	17	0x0	
GPIO_I2C_CLK_OE	18	0x0	
GPIO_I2C_DATA_OE	19	0x0	
GPIO_STRP_DATA_OE	20	0x0	
GPIO_DAC_SDA_OE	21	0x0	
GPIO_DAC_HSYNC_OE	22	0x0	
GPIO_DAC_VSYNC_OE	23	0x0	
GPIO_LVDS_ENA_BL_OE	24	0x0	
GPIO_LVDS_DIGON_OE	25	0x0	
GPIO_LVDS_BLON_OE	26	0x0	

GPIO_CPU_SLPb_OE	27	0x0	
GPIO_HPD_OE	28	0x0	
spare_31_29	31:29	0x0	

GPIO_PAD_SP_SN - RW - 32 bits - NBMISCIND:0x43			
Field Name	**Bits**	**Default**	**Description**
GPIO_SRP	0	0x1	
GPIO_SRN	1	0x1	
GPIO_SP_3	2	0x0	
GPIO_SP_2	3	0x0	
GPIO_SP_1	4	0x1	
GPIO_SP_0	5	0x1	
GPIO_SN_3	6	0x0	
GPIO_SN_2	7	0x0	
GPIO_SN_1	8	0x1	
GPIO_SN_0	9	0x1	
GPIO_HPD_SRN	10	0x1	
GPIO_HPD_SRP	11	0x1	

DFT_VIP_IO_GPIO - RW - 32 bits - NBMISCIND:0x44			
Field Name	**Bits**	**Default**	**Description**
DFT_GPIO_OE	5:0	0x0	
DFT_GPIO_A	13:8	0x0	
DFT_GPIO_Y (R)	21:16	0x0	
VIP_IO_TVCLKIN_GPIO_EN	24	0x0	
VIP_IO_TVCLKIN_GPIO_A	25	0x0	
VIP_IO_TVCLKIN_GPIO_Y (R)	26	0x1	

DFT_VIP_IO_GPIO_OR - RW - 32 bits - NBMISCIND:0x45			
Field Name	**Bits**	**Default**	**Description**
DFT_GPIO_OR	5:0	0x0	
VIP_IO_TVCLKIN_GPIO_OR	8	0x0	

IOC_PCIE_D2_CSR_Count - RW - 32 bits - NBMISCIND:0x50			
Field Name	**Bits**	**Default**	**Description**
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D2_CNTL - RW - 32 bits - NBMISCIND:0x51			
Field Name	**Bits**	**Default**	**Description**
DmaFixRelaxOrder	0	0x0	

DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D3_CSR_Count - RW - 32 bits - NBMISCIND:0x52

Field Name	Bits	Default	Description
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D3_CNTL - RW - 32 bits - NBMISCIND:0x53

Field Name	Bits	Default	Description
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D4_CSR_Count - RW - 32 bits - NBMISCIND:0x54

Field Name	Bits	Default	Description
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D4_CNTL - RW - 32 bits - NBMISCIND:0x55

Field Name	Bits	Default	Description
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	

DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D5_CSR_Count - RW - 32 bits - NBMISCIND:0x56

Field Name	Bits	Default	Description
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D5_CNTL - RW - 32 bits - NBMISCIND:0x57

Field Name	Bits	Default	Description
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D6_CSR_Count - RW - 32 bits - NBMISCIND:0x58

Field Name	Bits	Default	Description
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D6_CNTL - RW - 32 bits - NBMISCIND:0x59

Field Name	Bits	Default	Description
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	

DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D7_CSR_Count - RW - 32 bits - NBMISCIND:0x5A

Field Name	Bits	Default	Description
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D7_CNTL - RW - 32 bits - NBMISCIND:0x5B

Field Name	Bits	Default	Description
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D9_CSR_Count - RW - 32 bits - NBMISCIND:0x5C

Field Name	Bits	Default	Description
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D9_CNTL - RW - 32 bits - NBMISCIND:0x5D

Field Name	Bits	Default	Description
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	

P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D10_CSR_Count - RW - 32 bits - NBMISCIND:0x5E

Field Name	Bits	Default	Description
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D10_CNTL - RW - 32 bits - NBMISCIND:0x5F

Field Name	Bits	Default	Description
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D11_CSR_Count - RW - 32 bits - NBMISCIND:0x60

Field Name	Bits	Default	Description
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D11_CNTL - RW - 32 bits - NBMISCIND:0x61

Field Name	Bits	Default	Description
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	

P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

IOC_PCIE_D12_CSR_Count - RW - 32 bits - NBMISCIND:0x62

Field Name	Bits	Default	Description
CsrDelayCount	23:0	0x0	
CsrLimitCount	31:24	0x0	

IOC_PCIE_D12_CNTL - RW - 32 bits - NBMISCIND:0x63

Field Name	Bits	Default	Description
DmaFixRelaxOrder	0	0x0	
DmaForceSnoop	1	0x0	
DmaFixAttrEn	2	0x0	
P2pDis	3	0x0	
BMSetDis	7	0x0	
XactOrder	8	0x1	
BlockNonSp	9	0x0	
BlockSnoop	10	0x0	
MstRelaxOrder	11	0x0	
MstRelaxOrderEn	12	0x0	
MstNSoopEn	13	0x0	
ExtDevPlug	16	0x0	
ExtDevCsrEn	17	0x0	
CsrEnable	18	0x0	
IntSelMod	19	0x0	
SetPowEn	20	0x0	

StrapsOutputMux_0 - RW - 32 bits - NBMISCIND:0x70

Field Name	Bits	Default	Description
StrapsOutputMux_0	31:0	0x0	

StrapsOutputMux_1 - RW - 32 bits - NBMISCIND:0x71

Field Name	Bits	Default	Description
StrapsOutputMux_1	31:0	0x0	

StrapsOutputMux_2 - RW - 32 bits - NBMISCIND:0x72			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_2	31:0	0x0	

StrapsOutputMux_3 - RW - 32 bits - NBMISCIND:0x73			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_3	31:0	0x0	

StrapsOutputMux_4 - RW - 32 bits - NBMISCIND:0x64			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_4	31:0	0x0	

StrapsOutputMux_5 - RW - 32 bits - NBMISCIND:0x65			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_5	31:0	0x0	

StrapsOutputMux_6 - RW - 32 bits - NBMISCIND:0x66			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_6	31:0	0x0	

StrapsOutputMux_7 - RW - 32 bits - NBMISCIND:0x67			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_7	31:0	0x0	

StrapsOutputMux_8 - RW - 32 bits - NBMISCIND:0x68			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_8	31:0	0x0	

StrapsOutputMux_9 - RW - 32 bits - NBMISCIND:0x69			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_9	31:0	0x0	

StrapsOutputMux_A - RW - 32 bits - NBMISCIND:0x6A			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_A	31:0	0x0	

StrapsOutputMux_B - RW - 32 bits - NBMISCIND:0x6B			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_B	31:0	0x0	

StrapsOutputMux_C - RW - 32 bits - NBMISCIND:0x6C			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_C	31:0	0x0	

StrapsOutputMux_D - RW - 32 bits - NBMISCIND:0x6D			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_D	31:0	0x0	

StrapsOutputMux_E - RW - 32 bits - NBMISCIND:0x6E			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_E	31:0	0x0	

StrapsOutputMux_F - RW - 32 bits - NBMISCIND:0x6F			
Field Name	**Bits**	**Default**	**Description**
StrapsOutputMux_F	31:0	0x0	

SCRATCH_4 - RW - 32 bits - NBMISCIND:0x74			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_4	31:0	0x0	

SCRATCH_5 - RW - 32 bits - NBMISCIND:0x75			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_5	31:0	0x0	

SCRATCH_6 - RW - 32 bits - NBMISCIND:0x76			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_6	31:0	0x0	

SCRATCH_7 - RW - 32 bits - NBMISCIND:0x77			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_7	31:0	0x0	

SCRATCH_8 - RW - 32 bits - NBMISCIND:0x78			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_8	31:0	0x0	

SCRATCH_9 - RW - 32 bits - NBMISCIND:0x79			
Field Name	**Bits**	**Default**	**Description**
SCRATCH_9	31:0	0x0	

DFT_CNTL3 - RW - 32 bits - NBMISCIND:0x7B			
Field Name	**Bits**	**Default**	**Description**
TEST_DEBUG_IDSEL_3	6:0	0x0	
TEST_DEBUG_MUX_3	12:7	0x0	
TEST_DEBUG_COUNTER_EN_3	14	0x0	
TEST_DEBUG_CLK0_INV	15	0x0	
TEST_DEBUG_MULTIBLOCK_EN	16	0x0	

TEST_DEBUG_BUS_BLK1	17	0x0	
TEST_DEBUG_BUS_BLK2	18	0x0	
TEST_DEBUG_MUX_BLK2	24:19	0x0	
TEST_DEBUG_IDSEL_BLK2	31:25	0x0	

DFT_CNTL4 - RW - 32 bits - NBMISCIND:0x1D			
Field Name	**Bits**	**Default**	**Description**
dbg_block_select_0	5:0	0x0	
dbg_group_select_0	10:6	0x0	
dbg_mux_select_0	11	0x0	
dbg_block_select_1	17:12	0x0	
dbg_group_select_1	22:18	0x0	
dbg_mux_select_1	23	0x0	
dbg_control_load	24	0x0	
TC_OVERRIDE_for_GFX_debug_bus	25	0x0	
Reserved	31:26	0x0	

IOC_JTAG_CNTL - RW - 32 bits - NBMISCIND:0x47			
Field Name	**Bits**	**Default**	**Description**
JTAGARB_DEL	15:0	0xb	

PCIE_GFX_P2P_CONTROL - RW - 32 bits - NBMISCIND:0x48			
Field Name	**Bits**	**Default**	**Description**
D2P2PSnoopMode	0	0x1	
D3P2PSnoopMode	1	0x1	
D11P2PSnoopMode	2	0x1	
D12P2PSnoopMode	3	0x1	
D2P2PRelaxMode	4	0x1	
D3P2PRelaxMode	5	0x1	
D11P2PRelaxMode	6	0x1	
D12P2PRelaxMode	7	0x1	
P2PPcieDis	8	0x1	
GFX_DisBuffer	9	0x0	
GFX2_DisBuffer	10	0x0	
Eff_rr_mod	11	0x0	
CfgPciC_DisP2pLock	12	0x0	
Eff_mask	31:16	0xffff	

PCIE_GFX_P2P_ARBITRER_CONTROL - RW - 32 bits - NBMISCIND:0x49			
Field Name	**Bits**	**Default**	**Description**
Eff_size_a	7:0	0x4	
Eff_size_b	15:8	0x4	
Eff_size_c	23:16	0x8	

GPIO_SDVO_HPD - RW - 32 bits - NBMISCIND:0x4A			
Field Name	**Bits**	**Default**	**Description**
GPIO_SDVO_HPD_SEL	7:0	0x0	

2.14 PCIE Indirect Registers

PCIE_RESERVED - R - 32 bits - PCIEIND:0x0			
Field Name	**Bits**	**Default**	**Description**
PCIE_RESERVED	31:0	0xffffffff	Reserved
Reserved			

PCIE_SCRATCH - RW - 32 bits - PCIEIND:0x1			
Field Name	**Bits**	**Default**	**Description**
PCIE_SCRATCH	31:0	0x0	Software test register
Software test register			

PCIE_HW_DEBUG - RW - 32 bits - PCIEIND:0x2			
Field Name	**Bits**	**Default**	**Description**
HW_00_DEBUG	0	0x0	Bit [0]
HW_01_DEBUG	1	0x1	Bit [1]
HW_02_DEBUG	2	0x0	Bit [2]
HW_03_DEBUG	3	0x0	Bit [3]
HW_04_DEBUG	4	0x0	Bit [4]
HW_05_DEBUG	5	0x0	Bit [5]
HW_06_DEBUG	6	0x0	Bit [6]
HW_07_DEBUG	7	0x0	Bit [7]
HW_08_DEBUG	8	0x0	Bit [8]
HW_09_DEBUG	9	0x0	Bit [9]
HW_10_DEBUG	10	0x0	Bit [10]
HW_11_DEBUG	11	0x0	Bit [11]
HW_12_DEBUG	12	0x0	Bit [12]
HW_13_DEBUG	13	0x0	Bit [13]
HW_14_DEBUG	14	0x0	Bit [14]
HW_15_DEBUG	15	0x0	Bit [15]
Hardware debug register			

PCIE_RX_NUM_NACK - R - 32 bits - PCIEIND:0xE			
Field Name	**Bits**	**Default**	**Description**
RX_NUM_NACK	31:0	0x0	Total number of nacks received
Num nacks received			

PCIE_RX_NUM_NACK_GENERATED - R - 32 bits - PCIEIND:0xF			
Field Name	**Bits**	**Default**	**Description**
RX_NUM_NACK_GENERATED	31:0	0x0	Total number of nacks generated
Num nacks generated			

PCIE_CNTL - RW - 32 bits - PCIEIND:0x10			
Field Name	**Bits**	**Default**	**Description**
HWINIT_WR_LOCK	0	0x0	Hardware write lock 0=HWInit registers unlocked 1=Lock HWInit registers
UR_ERR_REPORT_DIS	7	0x0	UR error reporting disable for TX
PCIE_HT_NP_MEM_WRITE	9	0x0	Memory write mapping enable
RX_SB_ADJ_PAYLOAD_SIZE	12:10	0x2	SB payload size 2=16 bytes 3=32 bytes 4=64 bytes
RX_SB_COMPLETE_FULL_FIX	13	0x1	
RX_SB_REJECT_IF_FULL	14	0x0	
RX_RCB_REORDER_EN	16	0x1	RCB ordering enable 0=No re-ordering 1=Re-ordering
RX_RCB_INVALID_SIZE_DIS	17	0x1	RCB invalid size disable
RX_RCB_UNEXP_CPL_DIS	18	0x0	RCB unexpect cpl disable
RX_RCB_CPL_TIMEOUT_TEST_MODE	19	0x0	RCB cpl timeout test mode
RX_RCB_CHANNEL_ORDERING	20	0x0	GFX only 1=Completion reordering within Snooped/Non-Snooped channel 0=Completion reordering both channels together (default)
RX_RCB_WRONG_ATTR_DIS	21	0x1	RCB invalid attributes check for received completions disable
RX_RCB_WRONG_FUNCNUM_DIS	22	0x1	RCB invalid function number check for received completions disable
LC_PREVENT_SPD_CHG_OVERLAP	23	0x1	Prevents two speed change requests in opposite directions during the same clock cycle
TX_CPL_DEBUG	29:24	0x0	CPL debug
RX_CPL_POSTED_REQ_ORD_EN	31	0x1	CPL request ordering enable 0=Disable RX request ordering 1=Enable RX request ordering
PCIExpress control register			

PCIE_CONFIG_CNTL - RW - 32 bits - PCIEIND:0x11			
Field Name	**Bits**	**Default**	**Description**
DYN_CLK_LATENCY	3:0	0x7	Dynamic Clock Latency
PCIExpress Configuration Control Register			

PCIE_DEBUG_CNTL - RW - 32 bits - PCIEIND:0x12			
Field Name	**Bits**	**Default**	**Description**
DEBUG_PORT_EN	7:0	0x1	Debug Bus Port Enable 1=Port A 2=Port B 4=Port C 8=Port D 16=Port E 32=Port F 64=Port G 128=Port H
DEBUG_SELECT	8	0x0	Debug Bus Select. This is for additional muxing (e.g. VC0 vs. VC1)
DEBUG_LANE_EN	31:16	0x1	Debug Lane Enable Lane0=1 Lane1=2 Lane2=4 Lane3=8 Lane4=16 Lane5=32 Lane6=64 Lane7=128 Lane8=256 Lane9=512 Lane10=1024 Lane11=2048 Lane12=4096 Lane13=8192 Lane14=16384 Lane15=32768
Debug Bus Control Register			

PCIE_RTR_CPL_TIMEOUT_STATUS - RW - 32 bits - PCIEIND:0x13			
Field Name	**Bits**	**Default**	**Description**
CI_SLV_R_RTR_ERROR	0	0x0	Slave req interface. 1 indicates slv RTR was de-asserted for more than the # of cycles programmed in the CNTL register. This bit remains asserted until it is cleared by writing a 1.
CI_MST_R_RTR_ERROR	1	0x0	Master req interface. 1 indicates mst req RTR was de-asserted for more than the # of cycles programmed in the CNTL register. This bit remains asserted until it is cleared by writing a 1.
CI_MST_C_RTR_ERROR	2	0x0	Master completion interface. 1 indicates mst cpl RTR was de-asserted for more than the # of cycles programmed in the CNTL register. This bit remains asserted until it is cleared by writing a 1.
REG_R_RTR_ERROR	3	0x0	Register req interface. 1 indicates reg req RTR was de-asserted for more than the # of cycles programmed in the CNTL register. This bit remains asserted until it is cleared by writing a 1.
TX_SLVCPL_TIMEOUT_ERROR	4	0x0	Slave completion interface. 1 indicates slv cpl hasn't been received for more than the # of cycles programmed in the CNTL register. This bit remains asserted until it is cleared by writing a 1. For RC this bit is for the Snoop channel.

TX_SLVCPL_NS_TIMEOUT_ERROR	5	0x0	Slave completion interface. 1 indicates slv cpl hasn't been received for more than the # of cycles programmed in the CNTL register. This bit remains asserted until it is cleared by writing a 1. For RC this bit is for the Non-Snoop channel.
CI_SLV_R_RTR_STATUS (R)	16	0x0	
CI_MST_R_RTR_STATUS (R)	17	0x0	
CI_MST_C_RTR_STATUS (R)	18	0x0	
REG_R_RTR_STATUS (R)	19	0x0	
TX_SLVCPL_TIMEOUT_STATUS (R)	20	0x0	
TX_SLVCPL_NS_TIMEOUT_STATUS (R)	21	0x0	
Status register for rtr/cpl timeout			

PCIE_CI_SLV_R_RTR_TIMEOUT_CNTL - RW - 32 bits - PCIEIND:0x14

Field Name	Bits	Default	Description
CI_SLV_R_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the slv req RTR timer
CI_SLV_R_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in SLV_R_CLK) how long the RTR must be de-asserted before an error is flagged. This value is [31:4]. Bits [3:0] are zero. The min # of cylces is 0x10 (programming this field to 0x1)
Control register for slave request RTR timeout			

PCIE_CI_MST_R_RTR_TIMEOUT_CNTL - RW - 32 bits - PCIEIND:0x15

Field Name	Bits	Default	Description
CI_MST_R_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the master req RTR timer
CI_MST_R_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in MST_R_CLK) how long the RTR must be de-asserted before an error is flagged. This value is [31:4]. Bits 3:0 are zero. The min # of cylces is 0x10 (programming this field to 0x1)
Control register for master request RTR timeout			

PCIE_CI_MST_C_RTR_TIMEOUT_CNTL - RW - 32 bits - PCIEIND:0x16

Field Name	Bits	Default	Description
CI_MST_C_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the master cpl RTR timer
CI_MST_C_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in MST_C_CLK) how long the RTR must be de-asserted before an error is flagged. This value is [31:4]. Bits [3:0] are zero. The min # of cylces is 0x10 (programming this field to 0x1)
Control register for master completion RTR timeout			

PCIE_REG_R_RTR_TIMEOUT_CNTL - RW - 32 bits - PCIEIND:0x17

Field Name	Bits	Default	Description
REG_R_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the register req RTR timer
REG_R_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in REG_R_CLK) how long the RTR must be de-asserted before an error is flagged. This value is [31:4]. Bits 3:0 are zero. The min # of cylces is 0x10 (programming this field to 0x1)
Control register for register request RTR timeout			

PCIE_TX_SLVCPL_TIMEOUT_CNTL - RW - 32 bits - PCIEIND:0x18			
Field Name	**Bits**	**Default**	**Description**
TX_SLVCPL_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the slave cpl timer
TX_SLVCPL_TIMEOUT_VC	3	0x0	Controls which virtual channel to monitor the cpl 0=VC0 1=VC1
TX_SLVCPL_TIMEOUT_VALUE	31:4	0xffff	Value that indicates, in the # of cycles (in SLV_C_CLK/SLV_S_CCLK), how long to wait for cpl before an error is flagged. This value is [31:4]. Bits [3:0] are zero. The min # of cylces is 0x10 (programming this field to 0x1)
Control register for slave completion timeout - snoop channel for RC			

PCIE_TX_SLVCPL_NS_TIMEOUT_CNTL - RW - 32 bits - PCIEIND:0x19			
Field Name	**Bits**	**Default**	**Description**
TX_SLVCPL_NS_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the slave cpl timer
TX_SLVCPL_NS_TIMEOUT_VC	3	0x0	Controls which channel to monitor the cpl, 0 - VC0, 1 - VC1
TX_SLVCPL_NS_TIMEOUT_VALUE	31:4	0xffff0	Value that indicates, in the # of cycles (in SLV_C_CLK/SLV_S_CCLK), how long to wait for cpl before an error is flagged. This value is [31:4]. Bits [3:0] are zero. The min # of cylces is 0x10 (programming this field to 0x1)
Control register for slave completion timeout - non-snoop channel			

PCIE_CNTL2 - RW - 32 bits - PCIEIND:0x1C			
Field Name	**Bits**	**Default**	**Description**
TX_ARB_ROUND_ROBIN_EN	0	0x0	TX round-robin arbitration enabled (for RC only)
TX_ARB_SLV_LIMIT	5:1	0x0	TX slave arbitration limit
TX_ARB_MST_LIMIT	10:6	0x0	TX master arbitration limit

PCIE_CI_CNTL - RW - 32 bits - PCIEIND:0x20			
Field Name	**Bits**	**Default**	**Description**
CI_SLAVE_SPLIT_MODE	2	0x0	0=RC - Full completions from Channel A or B 1=RC - Completions split on Channel A and B evenly
CI_SLAVE_GEN_USR_DIS	3	0x0	Sends USR for invalid addresses 0=Sends USR for invalid addresses 1=Disables slave from sending USR, and instead sends a successful CMPLT_D with dummy data.
CI_MST_CMPL_DUMMY_DATA	4	0x1	0xDEADBEEF or 0xFFFFFFFF 0=0xDEADBEEF 1=0xFFFFFFFF
CI_SLV_RC_RD_REQ_SIZE	7:6	0x1	Slave read requests supported size to client. 0=32/64 byte requests supported 1=64 byte requests only 2=16/32/64
CI_SLV_ORDERING_DIS	8	0x0	Disables slave ordering logic 0=Enable slave ordering logic 1=Disable slave ordering logic
CI_RC_ORDERING_DIS	9	0x0	Disables RC ordering logic 0=Enable RC ordering logic 1=Disable RC ordering logic
CI_SLV_CPL_ALLOC_DIS	10	0x0	Slave CPL buffer is sub-divided or not 0=Slave CPL buffer is sub-divided between ports based on number of lanes active 1=Slave CPL buffer is not sub-divided
CI_SLV_CPL_ALLOC_MODE	11	0x0	Slave Cpl buffer method for sub-division 0=Dynamic 1=Register limits CI_SLV_CPL_STATIC_ALLOC_LIMIT_(N)S
TX_SLV_CPL_DELAY_EN	13	0x0	Enables Delay on Slave Completion Data path. RC only
TX_SLV_CPL_DELAY_TIMER	23:14	0x0	Delay timeout. Effective delay = 7 * TIMER * SLV_S_C_CLK_period
CI_SLV_REQ_DELAY_EN	24	0x0	Enables Delay on Slave Request path
CI_SLV_REQ_DELAY_TIMER	30:25	0x0	Delay timeout. Effective delay = 4 * TIMER * SLV_R_CLK_period
Chip interface control register			

PCIE_BUS_CNTL - RW - 32 bits - PCIEIND:0x21			
Field Name	**Bits**	**Default**	**Description**
BUS_DBL_RESYNC	0	0x1	Double flop the sync module 0=Normal 1=Add extra resynchronizing clock
PMI_INT_DIS	6	0x0	PMI Interrupt Disable 0=Normal 1=Disable
IMMEDIATE_PMI_DIS	7	0x0	Immediate PMI Disable 0=Enable 1=Disable
PCI Express Bus Control Register			

PCIE_LC_STATE6 - R - 32 bits - PCIEIND:0x22			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE24	5:0	0x0	24th previous state
LC_PREV_STATE25	13:8	0x0	25th previous state
LC_PREV_STATE26	21:16	0x0	26th previous state
LC_PREV_STATE27	29:24	0x0	27th previous state
Link Control State Registers			

PCIE_LC_STATE7 - R - 32 bits - PCIEIND:0x23			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE28	5:0	0x0	28th previous state
LC_PREV_STATE29	13:8	0x0	29th previous state
LC_PREV_STATE30	21:16	0x0	30th previous state
LC_PREV_STATE31	29:24	0x0	31st previous state
Link Control State Registers			

PCIE_LC_STATE8 - R - 32 bits - PCIEIND:0x24			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE32	5:0	0x0	32nd previous state
LC_PREV_STATE33	13:8	0x0	33rd previous state
LC_PREV_STATE34	21:16	0x0	34th previous state
LC_PREV_STATE35	29:24	0x0	35th previous state
Link Control State Registers			

PCIE_LC_STATE9 - R - 32 bits - PCIEIND:0x25			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE36	5:0	0x0	36th previous state
LC_PREV_STATE37	13:8	0x0	37th previous state
LC_PREV_STATE38	21:16	0x0	38th previous state
LC_PREV_STATE39	29:24	0x0	39th previous state
Link Control State Registers			

PCIE_LC_STATE10 - R - 32 bits - PCIEIND:0x26			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE40	5:0	0x0	40th previous state
LC_PREV_STATE41	13:8	0x0	41st previous state
LC_PREV_STATE42	21:16	0x0	42nd previous state
LC_PREV_STATE43	29:24	0x0	43rd previous state
Link Control State Registers			

PCIE_LC_STATE11 - R - 32 bits - PCIEIND:0x27			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE44	5:0	0x0	44th previous state
LC_PREV_STATE45	13:8	0x0	45th previous state
LC_PREV_STATE46	21:16	0x0	46th previous state
LC_PREV_STATE47	29:24	0x0	47th previous state
Link Control State Registers			

PCIE_LC_STATUS1 - R - 32 bits - PCIEIND:0x28			
Field Name	**Bits**	**Default**	**Description**
LC_REVERSE_RCVR	0	0x0	
LC_REVERSE_XMIT	1	0x0	
LC_OPERATING_LINK_WIDTH	4:2	0x0	
LC_DETECTED_LINK_WIDTH	7:5	0x0	
Link Control Status Register 1			

PCIE_LC_STATUS2 - R - 32 bits - PCIEIND:0x29			
Field Name	**Bits**	**Default**	**Description**
LC_TOTAL_INACTIVE_LANES	15:0	0x0	
LC_TURN_ON_LANE	31:16	0x0	
Link Control Status Register 2			

PCIE_WPR_CNTL - RW - 32 bits - PCIEIND:0x30			
Field Name	**Bits**	**Default**	**Description**
WPR_RESET_HOT_RST_EN	0	0x1	Enables Hot Reset feature.
WPR_RESET_LNK_DWN_EN	1	0x0	Enables Link down reset feature.
WPR_RESET_LNK_DIS_EN	2	0x1	Enables Link disable reset feature.
WPR_RESET_COR_EN	3	0x0	Enables external CORE reset feature.
WPR_RESET_REG_EN	4	0x0	Enables external REGISTER reset feature.
WPR_RESET_STY_EN	5	0x0	Enables external Stickybit Register reset feature.
WPR_RESET_PHY_EN	6	0x0	Enables external PHY reset feature.
WPR Control Register			

PCIE_RX_LAST_TLP0 - R - 32 bits - PCIEIND:0x31			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP0	31:0	0x0	Bits [31:0]
Last received TLP			

PCIE_RX_LAST_TLP1 - R - 32 bits - PCIEIND:0x32			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP1	31:0	0x0	Bits [63:32]
Last received TLP			

PCIE_RX_LAST_TLP2 - R - 32 bits - PCIEIND:0x33			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP2	31:0	0x0	Bits [95:64]
Last received TLP			

PCIE_RX_LAST_TLP3 - R - 32 bits - PCIEIND:0x34			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP3	31:0	0x0	Bits [127:96]
Last received TLP			

PCIE_TX_LAST_TLP0 - R - 32 bits - PCIEIND:0x35			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP0	31:0	0x0	Bits [31:0]
Last transmitted TLP			

PCIE_TX_LAST_TLP1 - R - 32 bits - PCIEIND:0x36			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP1	31:0	0x0	Bits [63:32]
Last transmitted TLP			

PCIE_TX_LAST_TLP2 - R - 32 bits - PCIEIND:0x37			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP2	31:0	0x0	Bits [95:64]
Last transmitted TLP			

PCIE_TX_LAST_TLP3 - R - 32 bits - PCIEIND:0x38			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP3	31:0	0x0	Bits [127:96]
Last transmitted TLP			

PCIE_I2C_DEBUG_BUS - R - 32 bits - PCIEIND:0x39			
Field Name	**Bits**	**Default**	**Description**
DEBUG_SEL_BLK1	5:0	0x0	
DEBUG_SEL_BLK2	11:6	0x0	
DEBUG_MUX_BLK1	17:12	0x0	
DEBUG_MUX_BLK2	23:18	0x0	
DEBUG_BUS_BLK1	24	0x0	
DEBUG_BUS_BLK2	25	0x0	
DEBUG_EN	26	0x0	
DEBUG_MULTIBLOCK_EN	27	0x0	
DEBUG_RESERVE	31:28	0x0	

PCIE_I2C_REG_ADDR_EXPAND - RW - 32 bits - PCIEIND:0x3A			
Field Name	**Bits**	**Default**	**Description**
I2C_REG_ADDR (R)	16:0	0x0	
BDI2C_CPLDATA_RTN_EXPAND	20:17	0x0	
BDREG_CPLDATA_RTN_EXPAND	24:21	0x3	

PCIE_I2C_REG_DATA - R - 32 bits - PCIEIND:0x3B			
Field Name	**Bits**	**Default**	**Description**
I2C_REG_DATA	31:0	0x0	

PCIE_CFG_CNTL - RW - 32 bits - PCIEIND:0x3C			
Field Name	**Bits**	**Default**	**Description**
CFG_EN_DEC_TO_GEN2_HIDDEN_REG	0	0x0	Enables decoding of GEN2 hidden registers
CFG_EN_DEC_TO_HIDDEN_REG	1	0x0	Enables decoding of hidden registers (excluding GEN2)
Configuration space control register			

PCIE_P_CNTL - RW - 32 bits - PCIEIND:0x40			
Field Name	**Bits**	**Default**	**Description**
P_PWRDN_EN	0	0x0	Enables powering down transmitter and receiver pads along with PLL macros
P_SYMALIGN_MODE	1	0x0	Data Valid generation bit iMODE = 0 (Relax Mode): Update its symbol right away when detect any bit shift, i.e. data_valid will always assert. iMODE = 1 (Aggressive Mode): Need confirmation before muxing out the data 0=Relax Mode. Update symbol lock right away when detected bit shifts without waiting for confirmation 1=Aggressive Mode. Always need confirmation for asserting Data Valid
P_ENABLE_PLL_LOCKING_IN_QUICKSIM	2	0x0	Enables actual PLL locking time (30us) when QUICKSIM=1 for simulation purpose. 0=PLL locking time is minimal when QUICKSIM=1 1=Enable normal PLL locking time when QUICKSIM=1
P_PLL_PWRDN_IN_L1L23	3	0x0	Enables PLL powerdown in L1 or L23 Ready states (only if all the associated LC's are in Sates L1 / L23 corresponding to 4 / 2 lanes based on mpConfig and architecture) 0=PLL is always running regardless of Link States 1=PLL will be turned off during L1
P_PLL_BUF_PDNB	4	0x1	Disables 10X clock pad on a per PLL basis. Should be 1'b0 in order to activate this powersafe feature 0=Enable PLL Buffer to power down during L1 1=Always keep PLL Buffer running
P_TXCLK_SND_PWRDN	5	0x0	Enables powering down TXCLK clock pads on the transmit side. Each clock pad corresponds to logic associated with 4 lanes.
P_TXCLK_RCV_PWRDN	6	0x0	Enables powering down TXCLK clock pads on the receive side. Each clock pad corresponds to logic associated with 4 lanes.
PI_SYMALIGN_DIS_ELIDLE	7	0x0	Symbol Alignment Statemachine control signal: iDIS_ELIDLE = 0. ElectIdle assertion will be effective in state machine re-initialization. iDIS_ELIDLE = 1. ElectIdle will be ineffective in state machine re-initialization
P_MASK_RCVR_EIDLE_EN	8	0x0	Enables EIDLE mask for powered down receivers 0=Dont intercept ELEC_IDLE in power down 1=Intercept ELEC_IDLE in RX power down
P_PLL_PDNB	9	0x1	Enables PLL only (not the buffer) to power down in L1 or L23ready states. 0=Enable PLL to power down during L1 1=Always keep PLL running
P_EBUF_SYNC_MODE	10	0x0	0=Double flops 1=Single flop
P_LDSK_MASK_RCVR_ELEC_IDLE	11	0x0	0=GEN1:not mask-off; GEN2: mask-off 1=Mask-off for GEN1 and GEN2
P_ALLOW_PRX_FRONTEND_SHUTOFF	12	0x0	Enables PHY's RX FRONTEND to shut off during L1 when PLL power down is enabled. 0=RX Frontend is always power on 1=RX Frontend is shutoff during L1 when PLL power down is enabled
P_ALWAYS_USE_FAST_TXCLK	13	0x0	Bypasses TXCLK_SWITCH and uses 500MHz TXCLK from PLL for both GEN1 and GEN2 speed. 0=TXCLK will be either 250MHz or 500MHz depends on port speeds 1=Bypass TXCLK_SWITCH and always use 500MHz TXCLK

P_ELEC_IDLE_MODE	15:14	0x0	Electrical Idle Mode for PI (Physical Layer). 0=GEN1 - entry:PHY, exit:PHY; GEN2 - entry:infer, exit:PHY 1=GEN1 - entry:infer, exit:PHY; GEN2 - entry:infer, exit PHY 2=GEN1 - entry:PHY, exit:PHY; GEN2 - entry:PHY, exit:PHY 3=Reserved
RXP_XBAR_MUX0	17:16	0x0	Data routing cross bar mux (default 1'b0)
RXP_XBAR_MUX1	19:18	0x1	Data routing cross bar mux (default 1'b1)
RXP_XBAR_MUX2	21:20	0x2	Data routing cross bar mux (default 1'b2)
RXP_XBAR_MUX3	23:22	0x3	Data routing cross bar mux (default 1'b3)
PI_RXEN_GATER	27:24	0x2	
RXP_REALIGN_ON_EACH_TSX_OR_SKP	28	0x1	0=LDSK only taking deskew on deskewing error detect 1=taking deskew on every TSX and SKP OS
LC_RXP_DONT_ALIGN_ON_TSx	29	0x1	Control Lane Deskew TS detection in L1 and L23 0=Don't mask out TS ordered sets during L1 and L23 1=Mask out lane deskew TSx detection during L1 and L23
B_PG2RX_CR_EN_MODE	30	0x0	PHY's CDR Locking (CR_EN) mode 0=CR_EN is LTSSM driven. 1=CR_EN is PHY driven, based on P90_BRX_ELEC_IDLE_ASYNC
RXP_NAK_FIX_IN_MODE1_EN	31	0x0	0=Disable RXP deskew failure fix in low latency mode or Mode 1 1=Enable RXP deskew fix in Mode 1
PHY Control Register			

PCIE_P_BUF_STATUS - RW - 32 bits - PCIEIND:0x41			
Field Name	**Bits**	**Default**	**Description**
P_ELASTIC_BUF_OVERFLOW_0	0	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 0
P_ELASTIC_BUF_OVERFLOW_1	1	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 1
P_ELASTIC_BUF_OVERFLOW_2	2	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 2
P_ELASTIC_BUF_OVERFLOW_3	3	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 3
P_ELASTIC_BUF_OVERFLOW_4	4	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 4
P_ELASTIC_BUF_OVERFLOW_5	5	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 5
P_ELASTIC_BUF_OVERFLOW_6	6	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 6
P_ELASTIC_BUF_OVERFLOW_7	7	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 7
P_ELASTIC_BUF_OVERFLOW_8	8	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 8
P_ELASTIC_BUF_OVERFLOW_9	9	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 9
P_ELASTIC_BUF_OVERFLOW_10	10	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 10
P_ELASTIC_BUF_OVERFLOW_11	11	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 11
P_ELASTIC_BUF_OVERFLOW_12	12	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 12
P_ELASTIC_BUF_OVERFLOW_13	13	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 13
P_ELASTIC_BUF_OVERFLOW_14	14	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 14
P_ELASTIC_BUF_OVERFLOW_15	15	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 15
P_DESKEW_BUF_OVERFLOW_0	16	0x0	Symbol skew buffer over/underflow: lane 0
P_DESKEW_BUF_OVERFLOW_1	17	0x0	Symbol skew buffer over/underflow: lane 1
P_DESKEW_BUF_OVERFLOW_2	18	0x0	Symbol skew buffer over/underflow: lane 2
P_DESKEW_BUF_OVERFLOW_3	19	0x0	Symbol skew buffer over/underflow: lane 3
P_DESKEW_BUF_OVERFLOW_4	20	0x0	Symbol skew buffer over/underflow: lane 4
P_DESKEW_BUF_OVERFLOW_5	21	0x0	Symbol skew buffer over/underflow: lane 5
P_DESKEW_BUF_OVERFLOW_6	22	0x0	Symbol skew buffer over/underflow: lane 6
P_DESKEW_BUF_OVERFLOW_7	23	0x0	Symbol skew buffer over/underflow: lane 7
P_DESKEW_BUF_OVERFLOW_8	24	0x0	Symbol skew buffer over/underflow: lane 8
P_DESKEW_BUF_OVERFLOW_9	25	0x0	Symbol skew buffer over/underflow: lane 9
P_DESKEW_BUF_OVERFLOW_10	26	0x0	Symbol skew buffer over/underflow: lane 10
P_DESKEW_BUF_OVERFLOW_11	27	0x0	Symbol skew buffer over/underflow: lane 11
P_DESKEW_BUF_OVERFLOW_12	28	0x0	Symbol skew buffer over/underflow: lane 12
P_DESKEW_BUF_OVERFLOW_13	29	0x0	Symbol skew buffer over/underflow: lane 13
P_DESKEW_BUF_OVERFLOW_14	30	0x0	Symbol skew buffer over/underflow: lane 14

P_DESKEW_BUF_OVERFLOW_15	31	0x0	Symbol skew buffer over/underflow: lane 15
PHY BUFFER STATUS REGISTER			

PCIE_P_DECODER_STATUS - RW - 32 bits - PCIEIND:0x42			
Field Name	**Bits**	**Default**	**Description**
P_DECODE_ERR_0	0	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_1	1	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_2	2	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_3	3	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_4	4	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_5	5	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_6	6	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_7	7	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_8	8	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_9	9	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_10	10	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_11	11	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_12	12	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_13	13	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_14	14	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_15	15	0x0	Indicates which lane has the decoding error (i.e. cannot decode the incoming data) Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_0	16	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_1	17	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_2	18	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc

P_DISPARITY_ERR_3	19	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_4	20	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_5	21	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_6	22	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_7	23	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_8	24	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_9	25	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_10	26	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_11	27	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_12	28	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_13	29	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_14	30	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_15	31	0x0	Indicates which lane has the link error Bit [15] => Lane 15 (0 = OK, 1 = error), etc
PHY DECODER STATUS REGISTER			

PCIE_P_MISC_DEBUG_STATUS - RW - 32 bits - PCIEIND:0x43			
Field Name	**Bits**	**Default**	**Description**
P_LANE_REVERSAL (R)	2	0x0	Lane Reversal 0=All lane order is normal 1=All lane order is reversed
P_HW_DEBUG	15:4	0x0	
P_INSERT_ERROR_0	16	0x0	Transmit invalid symbol 10'b0001111001 on lane 0 0=Normal Operation 1=Inserting error on Transmitting Lane0 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_1	17	0x0	Transmit invalid symbol 10'b0001111001 on lane 1 0=Normal Operation 1=Inserting error on Transmitting Lane1 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_2	18	0x0	Transmit invalid symbol 10'b0001111001 on lane 2 0=Normal Operation 1=Inserting error on Transmitting Lane2 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_3	19	0x0	Transmit invalid symbol 10'b0001111001 on lane 3 0=Normal Operation 1=Inserting error on Transmitting Lane3 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_4	20	0x0	Transmit invalid symbol 10'b0001111001 on lane 4 0=Normal Operation 1=Inserting error on Transmitting Lane4 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_5	21	0x0	Transmit invalid symbol 10'b0001111001 on lane 5 0=Normal Operation 1=Inserting error on Transmitting Lane5 by replacing one symbol with an invalid symbol

P_INSERT_ERROR_6	22	0x0	Transmit invalid symbol 10'b0001111001 on lane 6 0=Normal Operation 1=Inserting error on Transmitting Lane6 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_7	23	0x0	Transmit invalid symbol 10'b0001111001 on lane 7 0=Normal Operation 1=Inserting error on Transmitting Lane7 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_8	24	0x0	Transmit invalid symbol 10'b0001111001 on lane 8 0=Normal Operation 1=Inserting error on Transmitting Lane8 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_9	25	0x0	Transmit invalid symbol 10'b0001111001 on lane 9 0=Normal Operation 1=Inserting error on Transmitting Lane9 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_10	26	0x0	Transmit invalid symbol 10'b0001111001 on lane 10 0=Normal Operation 1=Inserting error on Transmitting Lane10 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_11	27	0x0	Transmit invalid symbol 10'b0001111001 on lane 11 0=Normal Operation 1=Inserting error on Transmitting Lane11 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_12	28	0x0	Transmit invalid symbol 10'b0001111001 on lane 12 0=Normal Operation 1=Inserting error on Transmitting Lane12 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_13	29	0x0	Transmit invalid symbol 10'b0001111001 on lane 13 0=Normal Operation 1=Inserting error on Transmitting Lane13 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_14	30	0x0	Transmit invalid symbol 10'b0001111001 on lane 14 0=Normal Operation 1=Inserting error on Transmitting Lane14 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_15	31	0x0	Transmit invalid symbol 10'b0001111001 on lane 15 0=Normal Operation 1=Inserting error on Transmitting Lane15 by replacing one symbol with an invalid symbol
PHY MISCELLANEOUS DEBUG STATUS REGISTER			

PCIE_P_PLL_CNTL - RW - 32 bits - PCIEIND:0x44			
Field Name	**Bits**	**Default**	**Description**
P_VCOREF	1:0	0x0	Control signal generation used in calibrating PLL's 0=OFF 1=VDD/4 2=VDD/2 3=3VDD/4
P_CALREF	3:2	0x0	Control signal generation used in calibrating PLL's 0=OFF 1=VDD/2 2=2VDD/3 3=5VDD/6
PHY PLL CONTROL REGISTER			

PCIE_P_RCVR_DEBUG_CNTL - RW - 32 bits - PCIEIND:0x45			
Field Name	**Bits**	**Default**	**Description**
P_FORCE_SYMBOL_UNLOCK_0	0	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane0
P_FORCE_SYMBOL_UNLOCK_1	1	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane1
P_FORCE_SYMBOL_UNLOCK_2	2	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane2
P_FORCE_SYMBOL_UNLOCK_3	3	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane3
P_FORCE_SYMBOL_UNLOCK_4	4	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane4
P_FORCE_SYMBOL_UNLOCK_5	5	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane5
P_FORCE_SYMBOL_UNLOCK_6	6	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane6
P_FORCE_SYMBOL_UNLOCK_7	7	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane7
P_FORCE_SYMBOL_UNLOCK_8	8	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane8
P_FORCE_SYMBOL_UNLOCK_9	9	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane9
P_FORCE_SYMBOL_UNLOCK_10	10	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane10
P_FORCE_SYMBOL_UNLOCK_11	11	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane11
P_FORCE_SYMBOL_UNLOCK_12	12	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane12
P_FORCE_SYMBOL_UNLOCK_13	13	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane13
P_FORCE_SYMBOL_UNLOCK_14	14	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane14
P_FORCE_SYMBOL_UNLOCK_15	15	0x0	0=Normal Operation 1=Force symalign to lose symbol lock on lane15
P_CORRUPT_SYMBOL_0	16	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane0 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_1	17	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane1 by replacing one symbol with PAD symbol

P_CORRUPT_SYMBOL_2	18	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane2 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_3	19	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane3 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_4	20	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane4 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_5	21	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane5 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_6	22	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane6 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_7	23	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane7 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_8	24	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane8 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_9	25	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane9 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_10	26	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane10 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_11	27	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane11 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_12	28	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane12 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_13	29	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane13 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_14	30	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane14 by replacing one symbol with PAD symbol
P_CORRUPT_SYMBOL_15	31	0x0	0=Normal Operation 1=Corrupting incoming symbol on Lane15 by replacing one symbol with PAD symbol

PCIE_P_SYMSYNC_CTL - RW - 32 bits - PCIEIND:0x46			
Field Name	**Bits**	**Default**	**Description**
P_SYMSYNC_ELECT_IDLE_DET_EN	0	0x1	Use Electrical Idle Detect to filter out garbage data
P_SYMSYNC_SYNC_MODE	1	0x0	SYMSYNC synchronous mode 1=Look for iMGood consecutive good COMMAs 0=Look for iMGood consecutive good symbols
P_SYMSYNC_M_GOOD	9:2	0x7	M parameter of Good symbols or Commas (should be greater than two)
P_SYMSYNC_N_BAD	17:10	0x1	N parameter of Bad symbols (can be 1 or more)
P_SYMSYNC_PAD_MODE	19:18	0x3	Mode select of Good known symbols for replacement of the Bad symbols
P_SYMSYNC_BYPASS_MODE	20	0x1	Bypass mode. 1 just let data and DValid flow through 0=Enable Symsync 1=Bypass Symsync and Disable Symsync
P_SYMSYNC_ENABLE_IN_GEN1	21	0x0	Enables Symsync for GEN1 0=SYMSYNC is enabled for GEN2 only 1=Enable Symsync for GEN1 as well
SYMSYNC Control Registers			

PCIE_P_RXP_ERR_RETRAIN_CTL - RW - 32 bits - PCIEIND:0x47			
Field Name	**Bits**	**Default**	**Description**
P_RXP_THRESH_DISP_ERR	7:0	0x0	Bit [7]=Enable disparity error threshold counter Bits [6:0]=Disparity error threshold
P_RXP_THRESH_CODE_ERR	15:8	0x0	Bit [7]=Enable code error threshold counter Bits [6:0]=Code error threshold
P_RXP_THRESH_CLEARSKP	24	0x0	0=Don't clear error threshold counters when deskewing on SKP OS 1=Clear error threshold counters when deskewing on SKP OS
P_RXP_DCB_ERR_RETRAIN	25	0x0	0=Disable DCB error directing retrain 1=Enable DCB error directing retrain

PCIE_PI_RCVL0S_FTS_DET - RW - 32 bits - PCIEIND:0x50			
Field Name	**Bits**	**Default**	**Description**
PI_RCVL0S_FTS_DET_RST (W)	0	0x0	Writing 1 will reset the min/max count
PI_RCVL0S_FTS_DET_MIN (R)	13:1	0x1fff	Min # of FTS order set detected during RCV L0s
PI_RCVL0S_FTS_DET_MAX (R)	28:16	0x0	Max # of FTS order set detected during RCV L0s
Number of FTS order set detected during RCV L0s			

PCIE_P_IMP_CNTL_STRENGTH - RW - 32 bits - PCIEIND:0x60			
Field Name	**Bits**	**Default**	**Description**
P_TX_STR_CNTL_READ_BACK (R)	3:0	0x0	Stores the readback value of current controller
P_TX_IMP_CNTL_READ_BACK (R)	7:4	0x0	Stores the readback value of TX impedance controller
P_RX_IMP_CNTL_READ_BACK (R)	11:8	0x0	Stores the readback value of RX impedance controller
P_TX_STR_CNTL	19:16	0x7	Sets the initial default current strength to 4'b0111
P_TX_IMP_CNTL	23:20	0x6	Default TX impedance control value
P_RX_IMP_CNTL	27:24	0x6	Default RX impedance control value
PI_HALT_IMP_CAL	28	0x0	
P_PAD_MANUAL_OVERRIDE	31	0x0	Enables Current and Impedance control values to override 0=Allow normal impedance compensation operation 1=Default to manual settings
PHY IMPEDANCE CONTROL STRENGTH REGISTER			

PCIE_P_IMP_CNTL_UPDATE - RW - 32 bits - PCIEIND:0x61			
Field Name	**Bits**	**Default**	**Description**
P_IMP_PAD_UPDATE_RATE	4:0	0xe	PAD's update interval 0=PHY130 default 0xf 1=PHY90 default 0xe
P_IMP_PAD_SAMPLE_DELAY	12:8	0x1	Sampling window
P_IMP_PAD_INC_THRESHOLD	20:16	0x18	Incremental resolution
P_IMP_PAD_DEC_THRESHOLD	28:24	0x8	Decremental resolution
Impedance PAD defaults			

PCIE_P_STR_CNTL_UPDATE - RW - 32 bits - PCIEIND:0x62			
Field Name	**Bits**	**Default**	**Description**
P_STR_PAD_UPDATE_RATE	4:0	0xf	PAD's update interval 0=PHY130 default 0xf 1=PHY90 default 0xe
P_STR_PAD_SAMPLE_DELAY	12:8	0x1	Sampling window
P_STR_PAD_INC_THRESHOLD	20:16	0x18	Incremental resolution
P_STR_PAD_DEC_THRESHOLD	28:24	0x8	Decremental resolution
Current PAD defaults			

PCIE_P_PAD_MISC_CNTL - RW - 32 bits - PCIEIND:0x63			
Field Name	**Bits**	**Default**	**Description**
P_PAD_I_DUMMYOUT (R)	0	0x0	Input from analog. 0 if PMOS cur is stronger
P_PAD_IMP_DUMMYOUT (R)	1	0x0	Input from analog. 0 if PMOS imp is stronger
P_PAD_IMP_TESTOUT (R)	2	0x0	Input from analog. 1 if NMOS imp is stronger
P_LINK_RETRAIN_ON_ERR_EN	3	0x0	Disables error counts in LaneDeskew if Symbol unlocking, Code Errors or Deskew Errors are detected
P_PLLCAL_INC_LOWER_PHASE	6:4	0x1	0=0us 1=1us 2=2us 3=4us 4=8us 5=12us 6=16us 7=24us
Pad Miscellaneous Control Registers			

PCIE_P_PAD_FORCE_EN - RW - 32 bits - PCIEIND:0x64			
Field Name	**Bits**	**Default**	**Description**
B_PTX_PDNB_FEN	7:0	0x0	Forces B_PTX_PDNB to enable TX pad
B_PRX_PDNB_FEN	15:8	0x0	Forces B_PRX_RDNB to enable RX pad
B_PPLL_PDNB_FEN	19:16	0x0	Forces B_PPLL_PDNB to enable PLL
B_PPLL_BUF_PDNB_FEN	23:20	0x0	Forces B_PPLL_BUF_PDNB to enable 10x driver in PLL
B_PI_DREN_FEN	24	0x0	Forces B_PI_DREN to enable current calibration pad
B_PBG_PDNB_FEN	25	0x0	Forces B_PBG_PDNB to enable Bandgap circuit in current calibration pad
B_PIMP_TX_PDNB_FEN	26	0x0	Forces B_PIMP_TX_PDNB to enable TX impedance calibration pad
B_PIMP_RX_PDNB_FEN	27	0x0	Forces B_PIMP_RX_PDNB to enable RX impedance calibration pad
Powerdown enable signals used by the wrapper			

PCIE_P_PAD_FORCE_DIS - RW - 32 bits - PCIEIND:0x65			
Field Name	**Bits**	**Default**	**Description**
B_PTX_PDNB_FDIS	7:0	0x0	Forces B_PTX_PDNB to disable TX pad
B_PRX_PDNB_FDIS	15:8	0x0	Forces B_PRX_PDNB to disable RX pad
B_PPLL_PDNB_FDIS	19:16	0x0	Forces B_PPLL_PDNB to disable PLL
B_PPLL_BUF_PDNB_FDIS	23:20	0x0	Forces B_PPLL_BUF_PDNB to disable 10x driver in PLL
B_PI_DREN_FDIS	24	0x0	Forces B_PI_DREN to disable current calibration pad
B_PBG_PDNB_FDIS	25	0x0	Forces B_PBG_PDNB to disable Bandgap circuit in current calibration pad
B_PIMP_TX_PDNB_FDIS	26	0x0	Forces B_PIMP_TX_PDNB to disable TX impedance calibration pad
B_PIMP_RX_PDNB_FDIS	27	0x0	Forces B_PIMP_TX_PDNB to disable RX impedance calibration pad
Powerdown disable signals used by the wrapper			

PCIE_PERF_LATENCY_CNTL - RW - 32 bits - PCIEIND:0x70			
Field Name	**Bits**	**Default**	**Description**
TIMER_EN	0	0x0	Enables Latency Timer 0=Disable timer 1=Enable timer
TIMER_SHADOW_WR (W)	1	0x0	Shadow Register Write. Write 1 to update shadow registers 0=N/A 1=Write 1 to shadow write
TIMER_RESET (W)	2	0x0	Reset Latency Timer. Write 1 to clear latency timer counters 0=N/A 1=Write 1 to reset
PORT_NUM	6:4	0x0	Port Number. Should always be programmed to 000 0=Port 0 1=Port 1 2=Port 2 3=Port 3 4=Port 4 5=Port 5
PORT_MODE	7	0x0	Port Mode. Should always be programmed to 0 0=All ports 1=Single port
SNOOP	8	0x0	Excludes/Includes Snoop requests 0=Do not include snoop requests 1=Include snoop requests
NO_SNOOP	9	0x0	Excludes/Includes Non-Snoop requests 0=Do not include no snoop requests 1=Include no snoop requests
MEM_REQ	10	0x0	Excludes/Includes Memory requests 0=Do not include MEM requests 1=Include MEM requests
CFG_IO_REQ	11	0x0	Excludes/Includes CFG and I/O requests 0=Do not include CFG or I/O requests 1=Include CFG or I/O requests
REQ_ID_MODE	12	0x0	Requester ID Mode. Unfiltered/Filtered by Requester ID 0=Do not filter by requester ID 1=Filter by requester ID
TAG_MODE	13	0x0	Tag Mode. Unfiltered/Filters by Tag 0=Do not filter by tag 1=Filter by tag
CPL_MODE	14	0x0	Completion Mode. First Data/Last Data 0=First Data 1=Last Data
TRAFFIC_CLASS	23:16	0x0	Traffic Class filter bits. Bit [n] of this field must be set in order to measure the latency of requests with traffic class n (n = 0 -> 7). Bits can be set concurrently.
Latency Timer Control Register			

PCIE_PERF_LATENCY_REQ_ID - RW - 32 bits - PCIEIND:0x71			
Field Name	**Bits**	**Default**	**Description**
REQUESTER_ID	15:0	0x0	Requester ID Value
REQUESTER_MASK	31:16	0xffff	Requester ID Mask
Filter to select requests for a particular Requester ID			

PCIE_PERF_LATENCY_TAG - RW - 32 bits - PCIEIND:0x72			
Field Name	**Bits**	**Default**	**Description**
TAG	7:0	0x0	Tag Value
TAG_MASK	15:8	0xff	Tag Mask
Filter to select requests for a particular Tag			

PCIE_PERF_LATENCY_THRESHOLD - RW - 32 bits - PCIEIND:0x73			
Field Name	**Bits**	**Default**	**Description**
THRESHOLD	15:0	0xffff	Latency Threshold value in TXCLKs
Latency Threshold used to count requests outside of acceptable time limit			

PCIE_PERF_LATENCY_MAX - R - 32 bits - PCIEIND:0x74			
Field Name	**Bits**	**Default**	**Description**
PEAK	15:0	0x0	Number of TXCLKs for peak latency request
REQUESTER_ID	31:16	0x0	Requester ID for peak latency request
Current peak latency time with Requester ID			

PCIE_PERF_LATENCY_TIMER_LO - R - 32 bits - PCIEIND:0x75			
Field Name	**Bits**	**Default**	**Description**
TIMER_LO	31:0	0x0	Lower 32 bits of cumulative latency timer
Counter for cumulative request latency - LOWER BITS			

PCIE_PERF_LATENCY_TIMER_HI - R - 32 bits - PCIEIND:0x76			
Field Name	**Bits**	**Default**	**Description**
TIMER_HI	31:0	0x0	Upper 32 bits of cumulative latency timer. Note: Bits [31:16] of this field are hardwired to 0.
Counter for cumulative request latency - UPPER BITS			

PCIE_PERF_LATENCY_COUNTER0 - R - 32 bits - PCIEIND:0x77			
Field Name	**Bits**	**Default**	**Description**
NUM_REQ	31:0	0x0	Number of requests measured
Counter for number of requests measured			

PCIE_PERF_LATENCY_COUNTER1 - R - 32 bits - PCIEIND:0x78			
Field Name	**Bits**	**Default**	**Description**
NUM_EXCEED	31:0	0x0	Number of requests exceeding latency threshold
Counter for number of requests exceeding latency threshold			

PCIE_PERF_MAS_ACC_START_LO - RW - 32 bits - PCIEIND:0xA0			
Field Name	**Bits**	**Default**	**Description**
PERF_MAS_ACC_START_LO	31:2	0x0	Start addr value (bits [31:2])
Master access start addr (bits 31:2) for performance event only - master access outside aperature will be counted			

PCIE_PERF_MAS_ACC_END_LO - RW - 32 bits - PCIEIND:0xA1			
Field Name	**Bits**	**Default**	**Description**
PERF_MAS_ACC_END_LO	31:2	0x0	End addr value (bits 31:2)
Master access end addr (bits [31:2]) aperature for performance event only - master access outside aperature will be counted			

PCIE_PERF_MAS_ACC_START_END_HI - RW - 32 bits - PCIEIND:0xA2			
Field Name	**Bits**	**Default**	**Description**
PERF_MAS_ACC_START_HI	7:0	0x0	Start addr upper bits [39:32)]
PERF_MAS_ACC_END_HI	15:8	0x0	End addr upper bits [39:32)]
Master access upper addr value for performance event only - master access outside aperature will be counted			

PCIE_PERF_SLV_ACC_LO - RW - 32 bits - PCIEIND:0xA3			
Field Name	**Bits**	**Default**	**Description**
PERF_SLV_ACC_LO	31:2	0x0	Addr lower bits [31:2]
Slave access addr value for performance counter only - slave access to defined addr will be counted			

PCIE_PERF_SLV_ACC_HI - RW - 32 bits - PCIEIND:0xA4			
Field Name	**Bits**	**Default**	**Description**
PERF_SLV_ACC_HI	31:0	0x0	Upper addr bits [63:32)]
Slave access addr value for performance counter only - slave access to defined addr will be counted			

PCIE_STRAP_MISC - RW - 32 bits - PCIEIND:0xC0			
Field Name	**Bits**	**Default**	**Description**
STRAP_LINK_CONFIG	3:0	0x0	
STRAP_TRUSTED_CFG_EN	4	0x0	
STRAP_PWRSAVE_PEIDL_GOOD	5	0x0	
STRAP_BYPASS_SCRAMBLER	6	0x0	
STRAP_PHY_RCVRDET_3NF	7	0x0	
STRAP_F0_AER_EN	8	0x0	
STRAP_F0_EN	9	0x0	
STRAP_F0_MSI_EN	10	0x0	
STRAP_CLK_PM_EN	24	0x0	
STRAP_ECN1P1_EN	25	0x0	
STRAP_EXT_VC_COUNT	26	0x0	
STRAP_LEGACY_DEVICE_TYPE_EN	27	0x0	
STRAP_REVERSE_ALL	28	0x0	
Misc strap loadable register values			

PCIE_STRAP_MISC2 - RW - 32 bits - PCIEIND:0xC1			
Field Name	**Bits**	**Default**	**Description**
STRAP_LINK_BW_NOTIFICATION_CAP_EN	0	0x0	
STRAP_GEN2_COMPLIANCE	1	0x0	
STRAP_MSTCPL_TIMEOUT_EN	2	0x0	
Misc strap loadable register values 2			

PCIE_STRAP_PI - RW - 32 bits - PCIEIND:0xC2			
Field Name	**Bits**	**Default**	**Description**
STRAP_QUICKSIM_START	0	0x0	
STRAP_BACKGROUND_IMP_CAL	1	0x0	
STRAP_IMP_MANUAL_OVERRIDE	2	0x0	
STRAP_PAD_RX_MANUAL_IMPEDANCE	6:3	0x0	
STRAP_PAD_TX_MANUAL_IMPEDANCE	10:7	0x0	
STRAP_ELAST_WATERMARK	12:11	0x0	
STRAP_RXP_LAT_REDUCTION_DIS	13	0x0	
STRAP_LDSK_X1_BYPASS	14	0x0	
STRAP_STAGGER_CNTL	16:15	0x0	
STRAP_TX_PDNB_MODE	17	0x0	
STRAP_VCO_MODE	19:18	0x0	
STRAP_INIT_REAL_PES_MODE	20	0x0	
STRAP_INC_PLLCAL_PHASE	24:21	0x0	
STRAP_PHY_RX_INCAL_FORCE	25	0x0	
STRAP_EXTDEV_EN	27:26	0x0	
STRAP_TEST_TOGGLE_PATTERN	28	0x0	
STRAP_TEST_TOGGLE_MODE	29	0x0	
STRAP_SHUTOFF_PORTS_FOR_SYM_ERR	30	0x0	
STRAP_BYPASS_LDSK_TO_LC	31	0x0	0=To_LC lane data sourced from LDSK output 1=To_LC lane data sourced from LDSK input
Misc PI strap loadable register values			

PCIE_B_P90_CNTL - RW - 32 bits - PCIEIND:0xC3			
Field Name	**Bits**	**Default**	**Description**
B_P90IMP_BACKUP	3:0	0x0	
B_P90PLL_BACKUP	31:12	0x0	

PCIE_STRAP_I2C_BD - RW - 32 bits - PCIEIND:0xC4			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_I2C_SLV_ADR	6:0	0x0	
STRAP_BIF_DBG_I2C_EN	7	0x0	
I2C Straps			

PCIE_P90RX_PRBS10_CNTL - RW - 32 bits - PCIEIND:0xC6			
Field Name	**Bits**	**Default**	**Description**
P90RX_PRBS10_CLR	15:0	0x0	
P90TX_PRBS10_EN	31:16	0x0	

PCIE_P90_BRX_PRBS10_ER - R - 32 bits - PCIEIND:0xC7			
Field Name	**Bits**	**Default**	**Description**
P90_BRX_PRBS10_ER	15:0	0x0	

PCIE_PRBS_CLR - RW - 32 bits - PCIEIND:0xC8			
Field Name	**Bits**	**Default**	**Description**
PRBS_CLR	15:0	0x0	
PRBS_CHECKER_DEBUG_BUS_SELECT	19:16	0x0	0=Checker 0 debug bus 1=Checker 1 debug bus 2=Etc

PCIE_PRBS_STATUS1 - R - 32 bits - PCIEIND:0xC9			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRSTAT	15:0	0x0	
PRBS_LOCKED	31:16	0x0	

PCIE_PRBS_STATUS2 - R - 32 bits - PCIEIND:0xCA			
Field Name	**Bits**	**Default**	**Description**
PRBS_BITCNT_DONE	15:0	0x0	

PCIE_PRBS_FREERUN - RW - 32 bits - PCIEIND:0xCB			
Field Name	**Bits**	**Default**	**Description**
PRBS_FREERUN	15:0	0x0	

PCIE_PRBS_MISC - RW - 32 bits - PCIEIND:0xCC			
Field Name	**Bits**	**Default**	**Description**
PRBS_EN	0	0x0	0=PRBS GEN disable 1=PRBS GEN enable
PRBS_TEST_MODE	2:1	0x0	0=PRBS23 1=PRBS31 2=COUNTER 3=USER DEFINED
PRBS_USER_PATTERN_TOGGLE	3	0x0	0=Replicate user pattern1 1=Toggle user pattern1 and pattern2
PRBS_8BIT_SEL	4	0x0	0=10 BIT 1=8 BIT
PRBS_COMMA_NUM	6:5	0x0	0=4 1=8 2=16 3=32
PRBS_LOCK_CNT	11:7	0x0	
PRBS_GEN2_SPEED	15	0x0	0=GEN1 speed 1=GEN2 speed
PRBS_CHK_ERR_MASK	31:16	0x0	

PCIE_PRBS_USER_PATTERN - RW - 32 bits - PCIEIND:0xCD			
Field Name	**Bits**	**Default**	**Description**
PRBS_USER_DEFINE_PATTERN	29:0	0x0	

PCIE_PRBS_LO_BITCNT - RW - 32 bits - PCIEIND:0xCE			
Field Name	**Bits**	**Default**	**Description**
PRBS_LO_BITCNT	31:0	0x0	

PCIE_PRBS_HI_BITCNT - RW - 32 bits - PCIEIND:0xCF			
Field Name	**Bits**	**Default**	**Description**
PRBS_HI_BITCNT	7:0	0x0	

PCIE_PRBS_ERRCNT_0 - R - 32 bits - PCIEIND:0xD0			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_0	31:0	0x0	

PCIE_PRBS_ERRCNT_1 - R - 32 bits - PCIEIND:0xD1			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_1	31:0	0x0	

PCIE_PRBS_ERRCNT_2 - R - 32 bits - PCIEIND:0xD2			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_2	31:0	0x0	

PCIE_PRBS_ERRCNT_3 - R - 32 bits - PCIEIND:0xD3			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_3	31:0	0x0	

PCIE_PRBS_ERRCNT_4 - R - 32 bits - PCIEIND:0xD4			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_4	31:0	0x0	

PCIE_PRBS_ERRCNT_5 - R - 32 bits - PCIEIND:0xD5			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_5	31:0	0x0	

PCIE_PRBS_ERRCNT_6 - R - 32 bits - PCIEIND:0xD6			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_6	31:0	0x0	

PCIE_PRBS_ERRCNT_7 - R - 32 bits - PCIEIND:0xD7			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_7	31:0	0x0	

PCIE_PRBS_ERRCNT_8 - R - 32 bits - PCIEIND:0xD8			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_8	31:0	0x0	

PCIE_PRBS_ERRCNT_9 - R - 32 bits - PCIEIND:0xD9			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_9	31:0	0x0	

PCIE_PRBS_ERRCNT_10 - R - 32 bits - PCIEIND:0xDA			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_10	31:0	0x0	

PCIE_PRBS_ERRCNT_11 - R - 32 bits - PCIEIND:0xDB			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_11	31:0	0x0	

PCIE_PRBS_ERRCNT_12 - R - 32 bits - PCIEIND:0xDC			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_12	31:0	0x0	

PCIE_PRBS_ERRCNT_13 - R - 32 bits - PCIEIND:0xDD			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_13	31:0	0x0	

PCIE_PRBS_ERRCNT_14 - R - 32 bits - PCIEIND:0xDE			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_14	31:0	0x0	

PCIE_PRBS_ERRCNT_15 - R - 32 bits - PCIEIND:0xDF			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_15	31:0	0x0	

PCIE_P_DECODE_ERR_CNTL - RW - 32 bits - PCIEIND:0xEF			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_RESET	15:0	0x0	
DISPARITY_ERR_CNT_RESET	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_0 - R - 32 bits - PCIEIND:0xF0			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_0	15:0	0x0	
DISPARITY_ERR_CNT_0	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_1 - R - 32 bits - PCIEIND:0xF1			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_1	15:0	0x0	
DISPARITY_ERR_CNT_1	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_2 - R - 32 bits - PCIEIND:0xF2			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_2	15:0	0x0	
DISPARITY_ERR_CNT_2	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_3 - R - 32 bits - PCIEIND:0xF3			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_3	15:0	0x0	
DISPARITY_ERR_CNT_3	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_4 - R - 32 bits - PCIEIND:0xF4			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_4	15:0	0x0	
DISPARITY_ERR_CNT_4	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_5 - R - 32 bits - PCIEIND:0xF5			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_5	15:0	0x0	
DISPARITY_ERR_CNT_5	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_6 - R - 32 bits - PCIEIND:0xF6			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_6	15:0	0x0	
DISPARITY_ERR_CNT_6	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_7 - R - 32 bits - PCIEIND:0xF7			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_7	15:0	0x0	
DISPARITY_ERR_CNT_7	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_8 - R - 32 bits - PCIEIND:0xF8			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_8	15:0	0x0	
DISPARITY_ERR_CNT_8	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_9 - R - 32 bits - PCIEIND:0xF9			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_9	15:0	0x0	
DISPARITY_ERR_CNT_9	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_10 - R - 32 bits - PCIEIND:0xFA			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_10	15:0	0x0	
DISPARITY_ERR_CNT_10	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_11 - R - 32 bits - PCIEIND:0xFB			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_11	15:0	0x0	
DISPARITY_ERR_CNT_11	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_12 - R - 32 bits - PCIEIND:0xFC			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_12	15:0	0x0	
DISPARITY_ERR_CNT_12	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_13 - R - 32 bits - PCIEIND:0xFD			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_13	15:0	0x0	
DISPARITY_ERR_CNT_13	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_14 - R - 32 bits - PCIEIND:0xFE			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_14	15:0	0x0	
DISPARITY_ERR_CNT_14	31:16	0x0	

PCIE_P_DECODE_ERR_CNT_15 - R - 32 bits - PCIEIND:0xFF			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_15	15:0	0x0	
DISPARITY_ERR_CNT_15	31:16	0x0	

PCIEP_RESERVED - R - 32 bits - PCIEIND_P:0x0			
Field Name	**Bits**	**Default**	**Description**
PCIEP_RESERVED	31:0	0xffffffff	Reserved
Reserved			

PCIEP_SCRATCH - RW - 32 bits - PCIEIND_P:0x1			
Field Name	**Bits**	**Default**	**Description**
PCIEP_SCRATCH	31:0	0x0	Scratch Register
Scratch Register			

PCIEP_HW_DEBUG - RW - 32 bits - PCIEIND_P:0x2			
Field Name	**Bits**	**Default**	**Description**
HW_00_DEBUG	0	0x0	Bit [0]
HW_01_DEBUG	1	0x0	Bit [1]
HW_02_DEBUG	2	0x0	Bit [2]
HW_03_DEBUG	3	0x0	Bit [3]
HW_04_DEBUG	4	0x0	Bit [4]
HW_05_DEBUG	5	0x0	Bit [5]
HW_06_DEBUG	6	0x0	Bit [6]
HW_07_DEBUG	7	0x0	Bit [7]
HW_08_DEBUG	8	0x0	Bit [8]
HW_09_DEBUG	9	0x0	Bit [9]
HW_10_DEBUG	10	0x0	Bit [10]
HW_11_DEBUG	11	0x0	Bit [11]
HW_12_DEBUG	12	0x0	Bit [12]
HW_13_DEBUG	13	0x0	Bit [13]
HW_14_DEBUG	14	0x0	REGS_LC_NO_TSx_PAD_RCVD_DIS. Training sets can contain link and lane numbers set to PAD when transitioning from Polling.Active to Detect.Idle.
HW_15_DEBUG	15	0x0	REGS_LC_ALLOW_TX_L1_CONTROL. Allow TX to prevent LC from going to L1 when there are outstanding completions.
Hardware Debug Register			

PCIEP_PORT_CNTL - RW - 32 bits - PCIEIND_P:0x10			
Field Name	**Bits**	**Default**	**Description**
SLV_PORT_REQ_EN	0	0x1	Suspends all slave requests to client 0=Allow slave to be suspended 1=Ignore slave suspend signal
CI_SNOOP_OVERRIDE	1	0x0	Forces all slave requests to be snoop requests 0=Do not force all slave requests to be snoop requests 1=Force all slave requests to be snoop requests
HOTPLUG_MSG_EN	2	0x0	Enables hot-plug messages 0=Disable hot-plug messages 1=Enable hot-plug messages
NATIVE_PME_EN	3	0x1	Enables native PME 0=Disable native PME 1=Enable native PME
SEQNUM_DEBUG_MODE	4	0x0	Enables debug sequence number 0=Normal operation 1=Enable debug sequence number test mode
PMI_BM_DIS	5	0x0	0=Normal 1=Disable
CI_SLV_CPL_STATIC_ALLOC_LIMIT_S	14:8	0x0	Limit for outstanding Slave Snooped Non-Posted request to Slave 0=128
CI_SLV_CPL_STATIC_ALLOC_LIMIT_NS	22:16	0x0	Limit for outstanding Slave Non-Snooped Non-Posted request to Slave 0=128
Port Control Register			

PCIE_TX_CNTL - RW - 32 bits - PCIEIND_P:0x20			
Field Name	**Bits**	**Default**	**Description**
TX_REPLAY_NUM_COUNT (R)	9:0	0x0	TX Replay Number Counter. Keeps track of the number of replays that have occured
TX_SNR_OVERRIDE	11:10	0x0	Snoop Not Required Override. Control of the Snoop bit for master requests 0=Generate bit as normal 1=Override equation, and always set bit 2=Override equation, and always clear bit 3=Invalid
TX_RO_OVERRIDE	13:12	0x0	Relaxed Ordering Override. Controls relaxed ordering bit for master requests 0=Generate bit as normal 1=Override equation, and always set bit 2=Override equation, and always clear bit 3=Invalid
TX_PACK_PACKET_DIS	14	0x0	Packet Packing Disable. Back-to-back packing of TLP and DLLP 0=Place packets as close as allowable 1=Place STP/SDP in lane 0 only
TX_GENERATE_CRC_ERR	15	0x0	Generates CRC errors from TX by zeroing CRC field. 0=Generate proper CRC 1=Generate bad CRC
TX_GAP_BTW_PKTS	18:16	0x0	Number of idle cycles between DLLP and TLP
TX_FLUSH_TLP_DIS	19	0x1	Disables flushing TLPs when Data Link is down 0=Normal 1=Disable
TX_CPL_PASS_P	20	0x1	Ordering rule. Let Completion Pass Posted 0=no pass 1=CPL pass
TX_NP_PASS_P	21	0x0	Ordering rule. Let Non-Posted Pass Posted 0=no pass 1=NP pass
TX_FC_UPDATE_TIMEOUT_SEL	25:24	0x2	To adjust the length of the timeout interval before sending out flow control update 0=Disable flow control 1=4x clock cycle 2=1024x clock cycle 3=4096x clock cycle
TX_FC_UPDATE_TIMEOUT	31:26	0x7	Interval length to send flow control update
TX Control Register			

PCIE_TX_REQUESTER_ID - RW - 32 bits - PCIEIND_P:0x21			
Field Name	**Bits**	**Default**	**Description**
TX_REQUESTER_ID_FUNCTION (R)	2:0	0x0	Function ID of Requester for Master transactions or Completer for Slave Completions
TX_REQUESTER_ID_DEVICE	7:3	0x0	Device ID of Requester for Master transactions or Completer for Slave Completions
TX_REQUESTER_ID_BUS	15:8	0x0	Bus ID of Requester for Master transactions or Completer for Slave Completions
TX Requester ID Register			

PCIE_TX_VENDOR_SPECIFIC - RW - 32 bits - PCIEIND_P:0x22			
Field Name	**Bits**	**Default**	**Description**
TX_VENDOR_DATA	23:0	0x0	Writing to this register generates a Vendor Specific DLLP using Vendor Data for the payload
TX Vendor Specific DLLP			

PCIE_TX_REQUEST_NUM_CNTL - RW - 32 bits - PCIEIND_P:0x23			
Field Name	**Bits**	**Default**	**Description**
TX_NUM_P_ACK	5:0	0x10	Number of Posted requests sent out before ACK
TX_NUM_P_ACK_EN	7	0x0	Enable for number of Posted requests sent out before ACK
TX_NUM_NP_ACK	13:8	0x2	Number of Non-Posted (VC1 amd VC1) requests sent out before ACK
TX_NUM_NP_VC1_ACK_EN	14	0x0	Enable for number of Non-Posted VC1 requests sent out before ACK
TX_NUM_NP_ACK_EN	15	0x0	Enable for number of Non-Posted requests sent out before ACK
TX_NUM_CPL_ACK	21:16	0x1c	Number of Completions sent out before ACK
TX_NUM_CPL_ACK_EN	23	0x0	Enable for number of Completions sent out before ACK
TX_NUM_OUTSTANDING_NP	29:24	0x2	Number of Non-posted (VC0 and VC1) requests sent out before completion
TX_NUM_OUTSTANDING_NP_VC1_EN	30	0x0	Enable for number of Non-posted VC1 requests sent out before completion
TX_NUM_OUTSTANDING_NP_EN	31	0x0	Enable for number of Non-posted requests sent out before completion
TX Request Num Control Register			

PCIE_TX_SEQ - R - 32 bits - PCIEIND_P:0x24			
Field Name	**Bits**	**Default**	**Description**
TX_NEXT_TRANSMIT_SEQ	11:0	0x0	Next Transmit Sequence Number to send out
TX_ACKD_SEQ	27:16	0x0	Last Acknowledged Sequence Number
TX Sequence Register			

PCIE_TX_REPLAY - RW - 32 bits - PCIEIND_P:0x25			
Field Name	**Bits**	**Default**	**Description**
TX_REPLAY_NUM	9:0	0x3	Controls Replay Number before Link goes to Retrain
TX_REPLAY_TIMER_OVERWRITE	15	0x0	Trigger for Replay Timer
TX_REPLAY_TIMER	31:16	0x90	Replay Timer - when expired do Replay
TX Replay Register			

PCIE_TX_ACK_LATENCY_LIMIT - RW - 32 bits - PCIEIND_P:0x26			
Field Name	**Bits**	**Default**	**Description**
TX_ACK_LATENCY_LIMIT	7:0	0x0	ACK Latency Limit for scheduling ACK DLLP transmission
TX_ACK_LATENCY_LIMIT_OVERWRITE	8	0x0	Use register value instead of hardware value from link width
TX ACK Latency Limit			

PCIE_TX_CREDITS_ADVT_P - R - 32 bits - PCIEIND_P:0x30			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ADVT_PD	11:0	0x0	Posted data credits
TX_CREDITS_ADVT_PH	23:16	0x0	Posted header credits
Posted advertised credits			

PCIE_TX_CREDITS_ADVT_NP - R - 32 bits - PCIEIND_P:0x31			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ADVT_NPD	11:0	0x0	Non-posted data credits
TX_CREDITS_ADVT_NPH	23:16	0x0	Non-posted header credits
Non-posted advertised credits			

PCIE_TX_CREDITS_ADVT_CPL - R - 32 bits - PCIEIND_P:0x32			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ADVT_CPLD	11:0	0x0	Completion data credits
TX_CREDITS_ADVT_CPLH	23:16	0x0	Completion header credits
Completion advertised credits			

PCIE_TX_CREDITS_INIT_P - R - 32 bits - PCIEIND_P:0x33			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_INIT_PD	11:0	0x0	Posted data credits
TX_CREDITS_INIT_PH	23:16	0x0	Posted header credits
Posted initial credits			

PCIE_TX_CREDITS_INIT_NP - R - 32 bits - PCIEIND_P:0x34			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_INIT_NPD	11:0	0x0	Non-posted data credits
TX_CREDITS_INIT_NPH	23:16	0x0	Non-posted header credits
Non-posted initial credits			

PCIE_TX_CREDITS_INIT_CPL - R - 32 bits - PCIEIND_P:0x35			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_INIT_CPLD	11:0	0x0	Completion data credits
TX_CREDITS_INIT_CPLH	23:16	0x0	Completion header credits
Completion initial credits			

PCIE_TX_CREDITS_STATUS - RW - 32 bits - PCIEIND_P:0x36			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ERR_PD	0	0x0	RW1C - Posted Data Credits Error
TX_CREDITS_ERR_PH	1	0x0	RW1C - Posted Header Credits Error
TX_CREDITS_ERR_NPD	2	0x0	RW1C - Non-posted Data Credits Error
TX_CREDITS_ERR_NPH	3	0x0	RW1C - Non-posted Header Credits Error
TX_CREDITS_ERR_CPLD	4	0x0	RW1C - Cpl Data Credits Error
TX_CREDITS_ERR_CPLH	5	0x0	RW1C - Cpl Header Credits Error
TX_CREDITS_CUR_STATUS_PD (R)	16	0x0	The current status of the posted data credits
TX_CREDITS_CUR_STATUS_PH (R)	17	0x0	The current status of the posted header credits
TX_CREDITS_CUR_STATUS_NPD (R)	18	0x0	The current status of the non-posted data credits
TX_CREDITS_CUR_STATUS_NPH (R)	19	0x0	The current status of the non-posted header credits
TX_CREDITS_CUR_STATUS_CPLD (R)	20	0x0	The current status of the cpl data credits
TX_CREDITS_CUR_STATUS_CPLH (R)	21	0x0	The current status of the cpl header credits
TX Credits status. When set to 1, remaining credits > init credits. Status bit will remain 1 until a 1 is written to it.			

PCIE_P_PORT_LANE_STATUS - RW - 32 bits - PCIEIND_P:0x50			
Field Name	**Bits**	**Default**	**Description**
PORT_LANE_REVERSAL (R)	0	0x0	Reverse lanes and control signals associated with a port 0=Port Lane order is normal 1=Port Lane order is reversed
PHY_LINK_WIDTH (R)	6:1	0x0	Link Width 0=6'b00_0000 disabled 1=6'b00_0001 x1 2=6'b00_0010 x2 3=6'b00_0100 x4 4=6'b00_1000 x8 5=6'b01_0000 x12 6=6'b10_0000 x16
Port-Lane Status Register			

PCIE_FC_P - RW - 32 bits - PCIEIND_P:0x60			
Field Name	**Bits**	**Default**	**Description**
PD_CREDITS	7:0	0x8	Posted Data Flow Control Advertised Credits
PH_CREDITS	15:8	0x2	Posted Header Flow Control Advertised Credits
Posted Flow Control Registers			

PCIE_FC_NP - RW - 32 bits - PCIEIND_P:0x61			
Field Name	**Bits**	**Default**	**Description**
NPD_CREDITS	7:0	0x2	Non-Posted Data Flow Control Advertised Credits
NPH_CREDITS	15:8	0x2	Non-Posted Header Flow Control Advertised Credits
Non-Posted Flow Control Registers			

PCIE_FC_CPL - RW - 32 bits - PCIEIND_P:0x62			
Field Name	**Bits**	**Default**	**Description**
CPLD_CREDITS	7:0	0x0	Completion Data Flow Control Credits
CPLH_CREDITS	15:8	0x0	Completion Header Flow Control Credits
Completion Flow Control Registers			

PCIE_ERR_CNTL - RW - 32 bits - PCIEIND_P:0x6A			
Field Name	**Bits**	**Default**	**Description**
ERR_REPORTING_DIS	0	0x0	Disables PCI Express Advanced Error Reporting
ERR_GEN_INTERRUPT	1	0x0	Enables Interrupt Generation for errors
SYM_UNLOCKED_EN	2	0x0	Enables Reporting of Symbol Unlocked Errors 0=Disable reporting unlocked symbol errors 1=Report unlocked symbol errors
Error Control Registers			

PCIE_RX_CNTL - RW - 32 bits - PCIEIND_P:0x70			
Field Name	**Bits**	**Default**	**Description**
RX_IGNORE_IO_ERR	0	0x0	Ignores Malformed I/O TLP Errors
RX_IGNORE_BE_ERR	1	0x0	Ignores Malformed Byte Enable TLP Errors
RX_IGNORE_MSG_ERR	2	0x0	Ignores Malformed Message Error
RX_IGNORE_CRC_ERR (R)	3	0x0	Ignores CRC Errors
RX_IGNORE_CFG_ERR	4	0x0	Ignores Malformed Configuration Errors
RX_IGNORE_CPL_ERR	5	0x0	Ignores Malformed Completion Errors
RX_IGNORE_EP_ERR	6	0x0	Ignores Malformed EP Errors
RX_IGNORE_LEN_MISMATCH_ERR	7	0x0	Ignores Malformed Length Mismatch Errors
RX_IGNORE_MAX_PAYLOAD_ERR	8	0x0	Ignores Malformed Maximum Payload Errors
RX_IGNORE_TC_ERR	9	0x0	Ignores Malformed Traffic Class Errors
RX_IGNORE_CFG_UR	10	0x0	Reserved
RX_IGNORE_IO_UR	11	0x0	Reserved
RX_IGNORE_VEND0_UR	12	0x0	Ignores Vendor Type 0 Messages
RX_NAK_IF_FIFO_FULL	13	0x0	Sends NAK if RX internal FIFO is full
RX_GEN_ONE_NAK	14	0x1	Generates NAK only for the first bad packet until replayed
RX_FC_INIT_FROM_REG	15	0x0	Flow Control Initialization from registers 0=Init FC from FIFO sizes 1=Init FC from registers
RX_RCB_CPL_TIMEOUT	18:16	0x0	RCB cpl timeout 0=Disable 1=50us 2=10ms 3=25ms 4=50ms 5=100ms 6=500ms 7=1ms
RX_RCB_CPL_TIMEOUT_MODE	19	0x0	RCB cpl timeout on link down
RX_PCIE_CPL_TIMEOUT_DIS	20	0x0	
RX Control Register			

PCIE_RX_LASTACK_SEQNUM - R - 32 bits - PCIEIND_P:0x71			
Field Name	**Bits**	**Default**	**Description**
RX_LASTACK_SEQNUM	11:0	0x0	Last Acked sequence number
RX Last Acked Sequence Number Register			

PCIE_RX_VENDOR_SPECIFIC - R - 32 bits - PCIEIND_P:0x72			
Field Name	**Bits**	**Default**	**Description**
RX_VENDOR_DATA	23:0	0x0	Writing to this register will re-arm to capture the next Vendor Specific DLLP
RX_VENDOR_STATUS	24	0x0	Indicates that a Vendor Specific DLLP was decoded, and that Vendor Data was captured
RX Vendor Specific DLLP			

PCIE_RX_CREDITS_ALLOCATED_P - R - 32 bits - PCIEIND_P:0x80			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_PD	11:0	0x0	For posted TLP data, the number of FC units granted to transmitter since initialization, modulo 4096
RX_CREDITS_ALLOCATED_PH	23:16	0x0	For posted TLP header, the number of FC units granted to transmitter since initialization, modulo 256
RX Credits Allocated Register (Posted)			

PCIE_RX_CREDITS_ALLOCATED_NP - R - 32 bits - PCIEIND_P:0x81			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_NPD	11:0	0x0	For non-posted TLP data, the number of FC units granted to transmitter since initialization, modulo 4096
RX_CREDITS_ALLOCATED_NPH	23:16	0x0	For non-posted TLP header, the number of FC units granted to transmitter since initialization, modulo 256
RX Credits Allocated Register (Non-Posted)			

PCIE_RX_CREDITS_ALLOCATED_CPL - R - 32 bits - PCIEIND_P:0x82			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_CPLD	11:0	0x0	For completion TLP data, the number of FC units granted to transmitter since initialization, modulo 4096
RX_CREDITS_ALLOCATED_CPLH	23:16	0x0	For completion TLP header, the number of FC units granted to transmitter since initialization, modulo 256
RX Credits Allocated Register (Completion)			

PCIE_RX_CREDITS_RECEIVED_P - R - 32 bits - PCIEIND_P:0x83			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_PD	11:0	0x0	For posted TLP data, the number of FC units consumed by valid TLP received since initialization, modulo 4096
RX_CREDITS_RECEIVED_PH	23:16	0x0	For posted TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256
RX Credits Received Register (Posted)			

PCIE_RX_CREDITS_RECEIVED_NP - R - 32 bits - PCIEIND_P:0x84			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_NPD	11:0	0x0	For non-posted TLP data, the number of FC units consumed by valid TLP received since initialization, modulo 4096
RX_CREDITS_RECEIVED_NPH	23:16	0x0	For non-posted TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256
RX Credits Received Register (Non-Posted)			

PCIE_RX_CREDITS_RECEIVED_CPL - R - 32 bits - PCIEIND_P:0x85			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_CPLD	11:0	0x0	For completion TLP data, the number of FC units consumed by valid TLP received since initialization, module 4096
RX_CREDITS_RECEIVED_CPLH	23:16	0x0	For completion TLP header, the number of FC units consumed by valid TLP received since initialization, module 256
RX Credits Received Register (Completion)			

PCIE_LC_CNTL - RW - 32 bits - PCIEIND_P:0xA0			
Field Name	**Bits**	**Default**	**Description**
LC_CM_HI_ENABLE_COUNT	0	0x0	Enables count for CM_HIGH - when transmitter is to be turned on stop when the counter reaches CM_HI_COUNT_LIMIT_ON. If number of lanes = 1 or 2: CM_HI_COUNT_LIMIT_ON = 12 or 10. If number of lanes = 3 or 4: CM_HI_COUNT_LIMIT_ON = 10 or 12. If number of lanes > 4: CM_HI_COUNT_LIMIT_ON = 10 or 15.
LC_DONT_ENTER_L23_IN_D0	1	0x0	Do not enter L23 in D0 state.
LC_RESET_L_IDLE_COUNT_EN	2	0x0	Enables reset of electrical idle counter.
LC_RESET_LINK	3	0x0	Reset an individual link without resetting the other ports.
LC_16X_CLEAR_TX_PIPE	7:4	0x5	Adjusts the time that the LC waits for the pipe to be idle. Setting this field to 0 results in the maximum time. Otherwise, the delay increases as this field is incremented.
LC_L0S_INACTIVITY	11:8	0x0	L0s inactivity timer setting 0=L0s is disabled 1=40ns 2=80ns 3=120ns 4=200ns 5=400ns 6=1us 7=2us 8=4us 9=10us 10=40us 11=100us 12=400us 13=1ms 14=4ms

LC_L1_INACTIVITY	15:12	0x0	L1 inactivity timer setting 0=L1 is disabled 1=1us 2=2us 3=4us 4=10us 5=20us 6=40us 7=100us 8=400us 9=1ms 10=4ms 11=10ms 12=40ms 13=100ms 14=400ms
LC_PMI_TO_L1_DIS	16	0x0	Disables the transition to L1 caused by programming PMI_STATE to non-D0
LC_INC_N_FTS_EN	17	0x0	Enables incrementing N_FTS for each transition to recovery
LC_LOOK_FOR_IDLE_IN_L1L23	19:18	0x0	Controls the number of clocks to wait for Electrical Idle set in L1, L23 0=250 1=100 2=10000 3=3000000
LC_FACTOR_IN_EXT_SYNC	20	0x0	Factors in the extended sync bit in the calculation for the replay timer adjustment
LC_WAIT_FOR_PM_ACK_DIS	21	0x0	Disables waiting for PM_ACK in L23 ready entry handshake
LC_WAKE_FROM_L23	22	0x0	For upstream component, wake the link from L23 ready
LC_L1_IMMEDIATE_ACK	23	0x0	Always ACK an ASPM L1 entry DLLP (ie. never generate PM_NAK)
LC_ASPM_TO_L1_DIS	24	0x0	Disables ASPM L1
LC_DELAY_COUNT	26:25	0x0	Controls minimum amount of time to stay in L0s or L1 0=255/ 4095 (Power-down) 1=1250 / 16383 (Power-down) 2=5000/ 65535 (Power-down) 3=25000 / 262143 (Power-down)
LC_DELAY_L0S_EXIT	27	0x0	Enables staying in L0s for a minimum time
LC_DELAY_L1_EXIT	28	0x0	Enables staying in L1 for a minimum time
LC_EXTEND_WAIT_FOR_EL_IDLE	29	0x1	Waits for Electrical idle in L1/L23 ready value
LC_ESCAPE_L1L23_EN	30	0x1	Enables L1/L23 entry escape arcs
LC_GATE_RCVR_IDLE	31	0x0	Ignores PHY Electrical idle detector 0=LC will look for PE_LC_IdleDetected 1=To gate off PE_LC_IdleDetected to LC, so that LC never sees receivers enter EIDLE
Link Control Register			

PCIE_LC_CNTL2 - RW - 32 bits - PCIEIND_P:0xB1			
Field Name	**Bits**	**Default**	**Description**
LC_TIMED_OUT_STATE (R)	5:0	0x0	States that the LC was in when the deadman timer expired
LC_STATE_TIMED_OUT	6	0x0	Deadman timer expired.
LC_LOOK_FOR_BW_REDUCTION	7	0x1	Enables check for bandwidth change when reporting Link Bandwidth Notification Status. 0=Do not check if bandwidth was reduced. 1=Check if bandwidth was reduced.
LC_MORE_TS2_EN	8	0x0	Sends out 128 sets instead of 16.
LC_X12_NEGOTIATION_DIS	9	0x1	Disables x12 negotiation.
LC_LINK_UP_REVERSAL_EN	10	0x0	Allows reversal for a wider width in link up.
LC_ILLEGAL_STATE	11	0x0	The LC is in an illegal state.

LC_ILLEGAL_STATE_RESTART_EN	12	0x0	Enables the LC to be restarted when it is in an illegal state.
LC_WAIT_FOR_OTHER_LANES_MODE	13	0x0	Eliminates delay introduced by waiting for other lanes. 0=Timer based 1=Identical Training Set based
LC_ELEC_IDLE_MODE	15:14	0x0	Electrical Idle Mode for LC. 0=GEN1 - entry:PHY, exit:PHY; GEN2 - entry:infer, exit:PHY 1=GEN1 - entry:infer, exit:PHY; GEN2 - entry:infer, exit PHY 2=GEN1 - entry:PHY, exit:PHY; GEN2 - entry:PHY, exit:PHY 3=Reserved
LC_DISABLE_INFERRED_ELEC_IDLE_DET	16	0x0	Disables Inferred Electrical Idle detection. 0=Inferred Electrical Idle Detection is enabled 1=Inferred Electrical Idle Detection is disabled
LC_ALLOW_PDWN_IN_L1	17	0x0	Sets the BIF_CHIP_CLK_PDWN output to 1 when the LC is in the L1 state.
LC_ALLOW_PDWN_IN_L23	18	0x0	Sets the BIF_CHIP_CLK_PDWN output to 1 when the LC is in the L23_Ready state.
LC_DEASSERT_RX_EN_IN_L0S	19	0x0	Turns off transmitters when the link is in L0s.
LC_BLOCK_EL_IDLE_IN_L0	20	0x0	Prevents the Electrical Idle from causing a transition from Rcv_L0 to Rcv_L0s.
LC_RCV_L0_TO_RCV_L0S_DIS	21	0x0	Disables transition from Rcv_L0 to Rcv_L0s
LC_ASSERT_INACTIVE_DURING_HOLD	22	0x0	Asserts the INACTIVE_LANES signals when CHIP_BIF_hold_training is high.
LC_WAIT_FOR_LANES_IN_LW_NEG	24:23	0x0	
LC_PWR_DOWN_NEG_OFF_LANES	25	0x1	
LC_DISABLE_LOST_SYM_LOCK_ARCS	26	0x1	
LC_LINK_BW_NOTIFICATION_DIS	27	0x0	
LC_ENABLE_RX_CR_EN_DEASSERTION	28	0x0	Enables the deassertion of PG2RX_CR_EN to lock clock recovery parameter when lane is in electrical idle 0=CR_EN is always asserted 1=CR_EN is deasserted when RX_EN is deasserted during L0s/L1 and inactive lanes
LC_TEST_TIMER_SEL	30:29	0x0	State timeout select 0=LTSSM uses spec compliant timeout values. 1=LTSSM uses simulation timeout values. 2=LTSSM uses decreased timeout values for lab testing. 3=Reserved
LC_ENABLE_INFERRED_ELEC_IDLE_FOR_PI	31	0x1	Enables Inferred Electrical Idle Detection for PI (Physical Layer blocks) 0=Inferred Electrical Idle Detection is disabled for PI (Physical Layer block) 1=Inferred Electrical Idle Detection is enabled for PI (Physical Layer block)
Link Control Register 2			

PCIE_LC_CNTL3 - RW - 32 bits - PCIEIND_P:0xB5			
Field Name	**Bits**	**Default**	**Description**
LC_SELECT_DEEMPHASIS	0	0x0	Downstream De-Emphasis 0 = -6dB De-emphasis required 1 = -3.5dB De-emphasis required
LC_SELECT_DEEMPHASIS_CNTL	2:1	0x0	Upstream De-Emphasis control 0=Use De-emphasis from CSR. 1=Use De-emphasis from downstream component. 2=Use -6dB De-emphasis. 3=Use -3.5dB De-emphasis.
LC_RCVD_DEEMPHASIS (R)	3	0x0	De-emphasis setting advertised by other end.

LC_COMP_TO_DETECT	4	0x0	Modified Compliance Pattern control 0=No action taken. 1=Transition LTSSM from Polling.Compliance to Detect if sending out Modified Compliance Pattern due to receipt of TS1s.
LC_RESET_TSX_CNT_IN_RLOCK_EN	5	0x1	TS Ordered Set Counter Control in Recovery.RcvrLock 0=No change in Training Sequence counter when DIRECTED_SPEED_CHANGE asserted in Recovery.RcvrLock. 1=Reset Training Sequence counter when DIRECTED_SPEED_CHANGE is asserted in Recovery.RcvrLock.
Link Control Register 3			

PCIE_LC_BW_CHANGE_CNTL - RW - 32 bits - PCIEIND_P:0xB2			
Field Name	**Bits**	**Default**	**Description**
LC_BW_CHANGE_INT_EN	0	0x0	Enables Interrupt when the link bandwidth changes.
LC_HW_INIT_SPEED_CHANGE (R)	1	0x0	Link speed changed due to a hardware initiated speed negotiation.
LC_SW_INIT_SPEED_CHANGE (R)	2	0x0	Link speed changed due to a software initiated speed negotiation.
LC_OTHER_INIT_SPEED_CHANGE (R)	3	0x0	Link speed changed due to a speed negotiation initiated by the other end of the link.
LC_RELIABILITY_SPEED_CHANGE (R)	4	0x0	Link speed changed due to a reliability issue at the current speed.
LC_FAILED_SPEED_NEG (R)	5	0x0	Link speed change failed and link speed was reverted to initial speed.
LC_LONG_LW_CHANGE (R)	6	0x0	Link width was changed due to a long dynamic link width reconfiguration.
LC_SHORT_LW_CHANGE (R)	7	0x0	Link width was changed due to a short dynamic link width reconfiguration.
LC_LW_CHANGE_OTHER (R)	8	0x0	Link width changed and the change was initiated by the other end of the link.
LC_LW_CHANGE_FAILED (R)	9	0x0	Link width change was initiated by the width was not changed.
LC_LINK_BW_NOTIFICATION_DETECT_MODE	10	0x0	Control Link Bandwidth Management for speed changes in Detect. 0=Disable Link Bandwidth Management Capabilities in Detect. 1=Update LINK_BW_MANAGEMENT_STATUS when speed changes in Detect.
LC Bandwidth Change Notification Control Register			

PCIE_LC_TRAINING_CNTL - RW - 32 bits - PCIEIND_P:0xA1			
Field Name	**Bits**	**Default**	**Description**
LC_TRAINING_CNTL	3:0	0x0	Training control bits in training sets 0=Reserved 1=Disable Link 2=Loopback 3=Disable Scrambling. The training control signal will be asserted in the TS when the associated bit is set to 1.
LC_COMPLIANCE_RECEIVE	4	0x0	Control for the Compliance Receive bit in Training Sequence 1 Ordered Sets.
LC_LOOK_FOR_MORE_NON_MATCHING_TS1	5	0x0	Look for more non-matching TS1 ordered sets.

LC_POINT_7_PLUS_EN	6	0x1	Enables PCIe 2.0 Revision 0.9 features that are included in the Revision 0.7 compliant code.
LC_L1_LONG_WAKE_FIX_EN	7	0x1	Enables fix for FTS going to L1 problem
LC_POWER_STATE (R)	10:8	0x0	Link Power state
LC_DONT_GO_TO_L0S_IF_L1_ARMED	11	0x0	Prevents the LTSSM from going to Rcv_L0s if it has already acknowledged a request to go to L1 but it hasn't transitioned there yet.
LC_INIT_SPD_CHG_WITH_CSR_EN	12	0x1	Control PCIe 2.0 clause that states that directed_speed_change should be set if the Retrain Link bit is set to 1 and the Target Link Speed is not equal to the current link speed. 0=Speed negotiation will not be initiated by RETRAIN_LINK Configuration bit 1=Speed Negotiation can be initiated if RETRAIN_LINK is set and Target Link Speed does not equal the current link speed
LC_EXTEND_WAIT_FOR_SKP	16	0x1	Extends the timer when in Rcv_L0s_Skp state. The bit is inverted before being used.
LC_AUTONOMOUS_CHANGE_OFF	17	0x0	'Autonomous Change' Data Rate Identifier Control 0='Autonomous Change' is reported as defined in the PCIE 2.0 specification. 1=Do not report 'Autonomous Change'.
LC_UPCONFIGURE_CAP_OFF	18	0x0	'Upconfigurat Capability' Data Rate Identifier Control 0='Upconfigure Capability' is reported as defined in the PCIE 2.0 specification. 1=Do not report 'Upconfigure Capability'.
LC_STATIC_TX_PIPE_COUNT_EN	21	0x0	Use the same WAIT_FOR_EMPTY_PIPE values for all link widths when going to L1 or L23.
LC_ASPM_L1_NAK_TIMER_SEL	23:22	0x0	Select timer value to be used when a request to go to L1 is declined i.e. NAK is sent. 0=9.5us 1=3.2us 2=1.6us 3=0.8us
LC_DONT_DEASSERT_RX_EN_IN_R_SPEED	24	0x0	Prevents deassertion of RX_EN during Recovery.Speed.
LC_DONT_DEASSERT_RX_EN_IN_TEST	25	0x0	Prevents deassertion of RX_EN during Polling.Compliance and Loopback.
LC_RESET_ASPM_L1_NAK_TIMER	26	0x1	Prevents L1 Nak Counter from being continuously reset before it has expired (i.e. reached 9.5us) if additional ASPM L1 requests received. 0=Don't reset the 9.5us L1 Nak Counter if additional ASPM L1 requests received. 1=Reset the 9.5us L1 Nak Counter if additional ASPM L1 requests received before counter finishes.
LC_DEBUG_1	27	0x0	Added this bit in case fields are needed after registers are frozen.
LC_DEBUG_2	28	0x0	Added this bit in case fields are needed after registers are frozen.
LC_DEBUG_3	29	0x0	Added this bit in case fields are needed after registers are frozen.
LC_DEBUG_4	30	0x0	Added this bit in case fields are needed after registers are frozen.
LC_DEBUG_5	31	0x0	Added this bit in case fields are needed after registers are frozen.
LC Training Control Register			

PCIE_LC_LINK_WIDTH_CNTL - RW - 32 bits - PCIEIND_P:0xA2			
Field Name	**Bits**	**Default**	**Description**
LC_LINK_WIDTH	2:0	0x6	Reserved
LC_LINK_WIDTH_RD (R)	6:4	0x0	Read back link width
LC_RECONFIG_ARC_MISSING_ESCAPE	7	0x0	Reserved
LC_RECONFIG_NOW	8	0x0	Reserved
LC_RENEGOTIATION_SUPPORT (R)	9	0x0	Reserved 0=Other end does not support link width renegotiation. 1=Other end does support link width renegotiation.
LC_RENEGOTIATE_EN	10	0x0	Enables re-negotiation
LC_SHORT_RECONFIG_EN	11	0x0	Reserved
LC_UPCONFIGURE_SUPPORT	12	0x0	
LC_UPCONFIGURE_DIS	13	0x0	
LC_UPCFG_WAIT_FOR_RCVR_DIS	14	0x0	0=Enable 1=Disable
LC_UPCFG_TIMER_SEL	15	0x0	0=1 msec 1=use LC_WAIT_FOR_LANES_IN_LW_NEG values
LC_DEASSERT_TX_PDNB	16	0x0	TX_PDNB Control for unused lanes 0=Keep TX_PDNB asserts for unused lanes. 1=Deassert TX_PDNB for unused lanes
LC_L1_RECONFIG_EN	17	0x0	Control for link width change in L1 state. 0=Link width reconfiguration can not be initiated from L1. 1=Link width reconfiguration can be initiated from L1.
Link Width Control			

PCIE_LC_N_FTS_CNTL - RW - 32 bits - PCIEIND_P:0xA3			
Field Name	**Bits**	**Default**	**Description**
LC_XMIT_N_FTS	7:0	0xc	Number of FTS to override the strap value
LC_XMIT_N_FTS_OVERRIDE_EN	8	0x0	Enables the previous field to override the strap value.
LC_XMIT_FTS_BEFORE_RECOVERY	9	0x0	Transmit FTS before Recovery.
LC_XMIT_N_FTS_LIMIT	23:16	0xff	Limit that the number of FTS can increment to when incrementing is enabled.
LC_N_FTS (R)	31:24	0x0	Number of FTS captured from the other end of the link.
LC Number of FTS Control			

PCIE_LC_SPEED_CNTL - RW - 32 bits - PCIEIND_P:0xA4			
Field Name	**Bits**	**Default**	**Description**
LC_GEN2_EN_STRAP	0	0x0	PCIE Generation 2 enable bit. Strap Loadable. 0=Gen1 only support. 1=Gen2 supported.
LC_TARGET_LINK_SPEED_OVERRIDE_EN	1	0x0	Enables the overriding of the Target Link Speed configuration register. 0=Disable override. 1=Override Target Link Speed with LC_TARGET_LINK_SPEED_OVERRIDE.
LC_TARGET_LINK_SPEED_OVERRIDE	2	0x0	Value used instead of Target Link Speed when override enable is set. 0=Gen2 not supported when override is enabled. 1=Gen2 supported when override is enabled.
LC_FORCE_EN_SW_SPEED_CHANGE	3	0x0	Forces the bif_core to allow speed changes initiated by private registers.
LC_FORCE_DIS_SW_SPEED_CHANGE	4	0x0	Disables speed changes initiated by the bif_core private registers.
LC_FORCE_EN_HW_SPEED_CHANGE	5	0x0	Forces the bif_core to allow speed changes initiated by the chip interface (based on voltage levels).
LC_FORCE_DIS_HW_SPEED_CHANGE	6	0x1	Disables speed changes initiated by the chip interface (based on voltage levels).
LC_INITIATE_LINK_SPEED_CHANGE	7	0x0	Initiates speed negotiation when allowed by the register settings.
LC_SPEED_CHANGE_ATTEMPTS_ALLOWED	9:8	0x0	Determines the number of speed change attempts that are allowed.
LC_SPEED_CHANGE_ATTEMPT_FAILED (R)	10	0x0	Number of speed change attempts allowed has been reached. This bit and the related counter can be cleared using the LC_CLR_FAILED_SPD_CHANGE_CNT bit.
LC_CURRENT_DATA_RATE (R)	11	0x0	0=Gen1 1=Gen2
LC_HW_VOLTAGE_IF_CONTROL	13:12	0x0	Controls the chip/bif_core speed control interface. 0=Ignore CHIP/BIF voltage interface. Voltage level is always assumed to be high. 1=CHIP/BIF voltage interface is enabled. 2=CHIP only allowed to lower or raise the voltage when the BIF is running at Gen1 data rate. CHIP must be running at high voltage if BIF is running at Gen2 data rate.
LC_VOLTAGE_TIMER_SEL	17:14	0xa	Controls the circuit that filters noise out of the chip/bif_core voltage interface. 0=No Delay 1=10ns 2=100ns 3=1us 4=10us 5=100us 6=1ms 7=10ms 8=100ms 9=500ms 10=1sec 11=2sec 12=5sec 13=10sec 14=15sec 15=20sec
LC_GO_TO_RECOVERY	18	0x0	Forces the Link to Recovery. Only applicable when link in L0 state.

LC_N_EIE_SEL	19	0x0	Selects the number of EIE (K28.7) symbols that are going to be sent when running at Gen2 speed and the link is exiting L0s. 0=Send 4 EIE (K28.7) symbols before transmitting FTS when exiting L0s at Gen2 speed. 1=Send 8 EIE (K28.7) symbols before transmitting FTS when exiting L0s at Gen2 speed.
LC_DONT_CLR_TARGET_SPD_CHANGE_STATUS	20	0x0	0=Clear speed negotiation failure initiated by Target Link Speed in Detect. 1=Speed negotiation failure initiated by Target Link Speed is only allowed to fail once.
LC_CLR_FAILED_SPD_CHANGE_CNT	21	0x0	This field will clear the LC_SPEED_CHANGE_ATTEMPT_FAILED field when a '1' is written to it. 0=No Change 1=Clear LC_SPEED_CHANGE_ATTEMPT_FAILED register bit so that more SW or HW(Voltage) initiated speed negotiations can be initiated.
LC_1_OR_MORE_TS2_SPEED_ARC_EN	22	0x0	0=Don't allow transition from Recovery.RcvrCfg to Recovery.Speed if 1 to 7 TS2s are received. 1=Allow the the transition from Recovery.RcvrCfg to Recovery.Speed if 1 to 7 TS2s with speed_change are received.
LC_OTHER_SIDE_EVER_SENT_GEN2 (R)	23	0x0	0=Other side of link has never advertised that it supports Gen2. 1=Other side of the link has ever advertised that it supports Gen2 - although it may not currently support Gen2.
LC_OTHER_SIDE_SUPPORTS_GEN2 (R)	24	0x0	0=Other side of the link does not currently advertise that it supports Gen2. 1=Other side of the link currently supports Gen2.
LC_AUTO_RECOVERY_DIS	25	0x1	0=Automatically go to Recovery in order to advertise that a change in Gen2 support has occured due to a voltage increase. 1=Do not automatically go to Recovery.
LC_SPEED_CHANGE_STATUS	26	0x0	This will gate a HW (i.e. voltage) initiated change to Gen2 when set to 1. 0=No status. 1=Tried to change to Gen2 speed and other end refused. Asserted when the other side no longer supports Gen2.
LC_DATA_RATE_ADVERTISED (R)	27	0x0	0=Only Gen1 support advertised. 1=Gen2 support advertised.
LC_CHECK_DATA_RATE	28	0x1	Determines if the LC is going to check the DATA RATE symbol if the LC_GEN2_EN_STRAP bit is not set. 0=Only check the DATA RATE identifiers when Gen2 is supported. 1=Always check the DATA RATE identifiers regardless of Gen2.
LC_MULT_UPSTREAM_AUTO_SPD_CHNG_EN	29	0x0	Allows the upstream component to initiate speed changes to the highest link speed supported by both ends of the link. Note that multiple speed changes are only allowed if there aren't any failures in previous speed change attempts. Also, note that the STRAP_BIF_AUTO_RC_SPEED_NEGOTIATION_DIS must be 0. 0=The upstream component will only try to automatically change the link to the highest link speed supported by both ends once, regardless of whether the change is successful or not. 1=The upstream component can automatically initiate multiple speed changes.

LC_INIT_SPEED_NEG_IN_L0s_EN	30	0x0	0=Do not allow a speed change to be initialized when in the L0s state. 1=Allow speed change negotiations to be initialized from L0s.
LC_INIT_SPEED_NEG_IN_L1_EN	31	0x0	0=Do not allow a speed change to be initialized when in the L1 state. 1=Allow speed change negotiations to be initialized from L1.
Data Rate Control			

PCIE_LC_CDR_CNTL - RW - 32 bits - PCIEIND_P:0xB3

Field Name	Bits	Default	Description
LC_CDR_TEST_OFF	11:0	0x60	
LC_CDR_TEST_SETS	23:12	0x18	
LC_CDR_SET_TYPE	25:24	0x1	
CDR Control Register			

PCIE_LC_LANE_CNTL - RW - 32 bits - PCIEIND_P:0xB4

Field Name	Bits	Default	Description
LC_CORRUPTED_LANES (R)	15:0	0x0	Indicates if that associated lane had trouble during training.
LC_LANE_DIS	31:16	0x0	Permanently disable associated lane.
Lane Status and Control Register			

PCIE_LC_STATE0 - R - 32 bits - PCIEIND_P:0xA5

Field Name	Bits	Default	Description
LC_CURRENT_STATE	5:0	0x0	Current LC State
LC_PREV_STATE1	13:8	0x0	1st Previous LC State
LC_PREV_STATE2	21:16	0x0	2nd Previous LC State
LC_PREV_STATE3	29:24	0x0	3rd Previous LC State
Link Control State Register			

PCIE_LC_STATE1 - R - 32 bits - PCIEIND_P:0xA6

Field Name	Bits	Default	Description
LC_PREV_STATE4	5:0	0x0	4th Previous LC State
LC_PREV_STATE5	13:8	0x0	5th Previous LC State
LC_PREV_STATE6	21:16	0x0	6th Previous LC State
LC_PREV_STATE7	29:24	0x0	7th Previous LC State
Link Control State Register			

PCIE_LC_STATE2 - R - 32 bits - PCIEIND_P:0xA7

Field Name	Bits	Default	Description
LC_PREV_STATE8	5:0	0x0	8th Previous LC State
LC_PREV_STATE9	13:8	0x0	9th Previous LC State
LC_PREV_STATE10	21:16	0x0	10th Previous LC State
LC_PREV_STATE11	29:24	0x0	11th Previous LC State
Link Control State Register			

PCIE_LC_STATE3 - R - 32 bits - PCIEIND_P:0xA8			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE12	5:0	0x0	12th Previous LC State
LC_PREV_STATE13	13:8	0x0	13th Previous LC State
LC_PREV_STATE14	21:16	0x0	14th Previous LC State
LC_PREV_STATE15	29:24	0x0	15th Previous LC State
Link Control State Register			

PCIE_LC_STATE4 - R - 32 bits - PCIEIND_P:0xA9			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE16	5:0	0x0	16th Previous LC State
LC_PREV_STATE17	13:8	0x0	17th Previous LC State
LC_PREV_STATE18	21:16	0x0	18th Previous LC State
LC_PREV_STATE19	29:24	0x0	19th Previous LC State
Link Control State Register			

PCIE_LC_STATE5 - R - 32 bits - PCIEIND_P:0xAA			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE20	5:0	0x0	20th Previous LC State
LC_PREV_STATE21	13:8	0x0	21st Previous LC State
LC_PREV_STATE22	21:16	0x0	22nd Previous LC State
LC_PREV_STATE23	29:24	0x0	23rd Previous LC State
Link Control State Register			

PCIEP_STRAP_LC - RW - 32 bits - PCIEIND_P:0xC0			
Field Name	**Bits**	**Default**	**Description**
STRAP_FTS_yTSx_COUNT	1:0	0x0	
STRAP_LONG_yTSx_COUNT	3:2	0x0	
STRAP_MED_yTSx_COUNT	5:4	0x0	
STRAP_SHORT_yTSx_COUNT	7:6	0x0	
STRAP_SKIP_INTERVAL	10:8	0x0	
STRAP_BYPASS_RCVR_DET	11	0x0	
STRAP_COMPLIANCE_DIS	12	0x0	
STRAP_FORCE_COMPLIANCE	13	0x0	
STRAP_REVERSE_LC_LANES	14	0x0	
STRAP_AUTO_RC_SPEED_NEGOTIATION_DIS	15	0x0	
STRAP_LANE_NEGOTIATION	18:16	0x0	Lane Negotiation Modes 0=Compliant mode, widest possible link 1=Compliant mode, fix missing lane 0 2=Compliant mode, reverse only 3=Compliant mode, reverse only, don't require the sets to be contiguous 4=Old mode, reverse only 5=Easy training mode, reverse only 6=Reliable mode, reverse only - means to reliably train, in a reliable system 7=Reserved
Misc LC strap loadable register value			

PCIEP_STRAP_MISC - RW - 32 bits - PCIEIND_P:0xC1			
Field Name	**Bits**	**Default**	**Description**
STRAP_EXIT_LATENCY	3:0	0x0	
STRAP_REVERSE_LANES	4	0x0	
Misc port strap loadable register values			

2.15 HTIU Northbridge Indirect Registers

PCI Bus 0 - Device 0 Registers

HTIU_DEBUG - RW - 32 bits - HTIUNBIND:0x5			
Field Name	**Bits**	**Default**	**Description**
HTIU_DEBUG	31:0	0x0	Bits [31:8]=Reserved Bit [7]=GSMinC3Only. Detect GSM traffic in C3 only Bit [5]=Disable response fix Bits [4:3]=Reserved Bit [2]=Extend DLL reset to be 100ns coming out of reset Bit [1]=Enable TXCLKs on debug bus. Do not turn this on in production Bit [0]=Enable RXCLKs on debug bus. Do not turn this on in production
HTIU debug			

HTIU_DOWNSTREAM_CONFIG - RW - 32 bits - HTIUNBIND:0x6			
Field Name	**Bits**	**Default**	**Description**
HTdSafeIssue	0	0x1	Setting this bit causes outstanding non-posted transactions to block the posted channel. It should be cleared to avoid a deadlock scenario 0=PW before NP done 1=PW after NP done
HTdPStreamEn	1	0x0	Downstream posted-write streaming. This register requires LDTSTOP or RESET to take effect: 0=PW Streaming Disabled 1=PW Streaming Enabled 0=Disabled 1=Enable for higher performance
CfgHTiuRdRspPassPWMode	3:2	0x0	PassPW for upstream read responses 0=00 - From request packet 1=01 - From IOC 2=10 - Always 0 3=11 - Always 1
CfgHTiuTgtDonePassPWMode	5:4	0x0	PassPW for upstream tgtdone 0=00 - From request packet 1=01 - Normally 1 but 0 for I/O cycle 2=10 - Always 0 3=11 - Always 1
CfgHTiuReqPassPWMode	7:6	0x0	PassPW for downstream requests to IOC 0=00 - From request packet 1=01 - Reserved 2=10 - Always 0 3=11 - Always 1
CfgHTiuDisableNPDWait	8	0x0	This bit should always be set to 0 for proper operation
CfgHTiuPDStage2En	9	0x0	Enables larger buffer for downstream posted data and higher performance
CfgHTiuLockIOCArb	10	0x0	Lock IOC arbiter. Should always be set to 0
CfgHTiuHtdNoErr	11	0x0	Prevents the chipset from sending error bits in upstream responses to the CPU
CfgHtiuTxMaxRspCnt	12	0x0	Reserved. This register controls no hardware
CfgHTiuLargeRspCnt	13	0x0	Enables 127 response buffer mode
ReqCompatModeDis	14	0x0	Disables Compat bit decoding in htiu. Should be set to 0 for proper operation

FIDStpGntDetect	15	0x0	Enables wait for display on StpGnt with FID SMAF detection. Should be disabled if no internal gfx
C3StpGntDetect	16	0x0	Enables wait for display on StpGnt with C3 SMAF detection. Should be disabled if no internal gfx
AllowNPPassPW	17	0x0	Enables PassPW functionality in non-posted transactions
FastNPAvail	18	0x1	Enables faster turnaround of NP buffer availability. Should be set to 1
GCMDelay	21:19	0x3	Delay between back-to-back transactions issued by GCM - should not be set lower than 0x3
GCMPCDelay	24:22	0x3	Delay between back-to-back PC transactions issued by GCM - should not be set lower than 0x3
DispIntAck	25	0x0	Ignores ACK from Display on StpGnt wait and generate ACK internally
PCIE_HT_NP_MEM_WRITE	26	0x0	Enables NP protocol over PCIE for memory-mapped writes targeting LPC. Set this bit to avoid a deadlock condition
SCAS_EN	27	0x0	Enables SCAS feature. All traffic between 1 and 2GB is mapped onto a special 64 byte storage space. Should be used for testing only
DbgCntrMode	28	0x0	Enables rotating htiu debug bus
Reserved_31_29	31:29	0x0	Bit [29]=Reserved. This register controls no hardware Bit [30]=Enables a fix for tagging downstream NP requests Bit [31]=Reserved. This register controls no hardware.

HTIU_UPSTREAM_CONFIG_0 - RW - 32 bits - HTIUNBIND:0x7			
Field Name	**Bits**	**Default**	**Description**
ioc_bw_opt_en	0	0x0	Optimizes IOC byte write by detecting Consecutive DW mask and translate the request to DW write 0=Disable 1=Enable
delay_STPCLK_en	1	0x1	Holds off upstream SMC STPCLK for FID message until DISP_ALLOW_LDTSTOP is asserted. During this time, only DISP can issue request. 0=Disable 1=Enable
delay_FID_en	2	0x1	Holds off upstream SMC FID message until DISP_ALLOW_LDTSTOP is asserted. Note: This bit should always be set to 0. 0=Disable 1=Enable
c3_delay_gfx_count_en	3	0x1	Blocks off GFX client for only 128 cycles when holding SMC STPCLK for FID message 0=Disable 1=Enable
ups_igp_arb_en	4	0x0	Selects between GCM/IGP arbitration mode 0=GCM Mode (default) 1=IGP Mode
IGP_ALL_en	5	0x0	Selects between IGP AFC/ALL arbitration mode 0=IGP_AFC Mode 1=IGP_ALL Mode
IGP_ALL_PFC_en	6	0x1	Enables Early Posted Buffer check in IGP_ALL mode 0=Disable 1=Enable
GCM_flush_urgent_np_disp	7	0x1	Flushes all Non-Posted DISP request first when received DISP urgent signal. Note: This bit should always be set to 1. 0=Disable 1=Enable

Disp_Rsv_BufCnt	11:8	0x1	Number of Non-Posted buffer reserved for DISP request 0=Min 7=Max Default is 1
disp_delay_en	12	0x0	Blocks off DISP request after N request send for T amount of cycle to allow other client to process their request 0=Disable 1=Enable
spare_14_13	14:13	0x0	
drop_zero_mask_req	15	0x0	Drops byte write request that have all zero mask 0=Disable 1=Enable
disp_delay_cnt	23:16	0x10	T amount of Cycle that DISP request will wait. Note: Each unit here represent 16 LCLK
disp_req_cnt	29:24	0x7	N DISP request send before wait
spare_31_30	31:30	0x0	Bit [30]=Enable Normal UnitID for STPCLK (FID or SB-Th) message Bit [31]=GFX Write Request PassPW enable
HTIU upstream configuration 0			

HTIU_UPSTREAM_CONFIG_1 - RW - 32 bits - HTIUNBIND:0x8			
Field Name	**Bits**	**Default**	**Description**
ISOC_DISP_urgt_pri	1:0	0x0	
ISOC_DISP_tout_pri	3:2	0x1	
ISOC_DISP_norm_pri	5:4	0x2	
ISOC_PCIE_norm_pri	7:6	0x3	
Force_All_P_Isoc	8	0x0	
Force_All_NP_Isoc	9	0x0	
CFG_CIP_ILA_pri	10	0x0	
CFG_CIP_CLMC_pri	11	0x1	
HTIU upstream configuration 1			

HTIU_UPSTREAM_CONFIG_2 - RW - 32 bits - HTIUNBIND:0x9			
Field Name	**Bits**	**Default**	**Description**
NP_Eff_Wrr_1_pri	1:0	0x0	
NP_Eff_Wrr_2_pri	3:2	0x1	
SPARE_5_4	5:4	0x0	
HTIU upstream configuration 2			

HTIU_UPSTREAM_CONFIG_3 - RW - 32 bits - HTIUNBIND:0xA			
Field Name	**Bits**	**Default**	**Description**
SPARE_15_0	15:0	0x0	
NP_Eff_Wrr_1_len_a	23:16	0x8	
NP_Eff_Wrr_1_len_b	31:24	0x8	
HTIU upstream configuration 3			

HTIU_UPSTREAM_CONFIG_4 - RW - 32 bits - HTIUNBIND:0xB			
Field Name	**Bits**	**Default**	**Description**
SPARE_15_0	15:0	0x0	
NP_Eff_Wrr_2_len_a	23:16	0x8	
NP_Eff_Wrr_2_len_b	31:24	0x8	
HTIU upstream configuration 4			

HTIU_UPSTREAM_CONFIG_5 - RW - 32 bits - HTIUNBIND:0xC			
Field Name	**Bits**	**Default**	**Description**
P_Eff_Wrr_1_pri	1:0	0x0	
P_Eff_Wrr_2_pri	3:2	0x1	
P_CIP_pri	5:4	0x2	
SPARE_7_6	7:6	0x0	
P_Eff_Wrr_1_len_a	15:8	0x8	
P_Eff_Wrr_2_len_a	23:16	0x8	
HTIU upstream configuration 5			

HTIU_UPSTREAM_CONFIG_6 - RW - 32 bits - HTIUNBIND:0xD			
Field Name	**Bits**	**Default**	**Description**
SPARE_15_0	15:0	0x0	
P_Eff_Wrr_1_len_b	23:16	0x8	
P_Eff_Wrr_1_len_c	31:24	0x8	
HTIU upstream configuration 6			

HTIU_UPSTREAM_CONFIG_7 - RW - 32 bits - HTIUNBIND:0xE			
Field Name	**Bits**	**Default**	**Description**
SPARE_15_0	15:0	0x0	
P_Eff_Wrr_2_len_b	23:16	0x8	
P_Eff_Wrr_2_len_c	31:24	0x8	
HTIU upstream configuration 7			

HTIU_UPSTREAM_CONFIG_8 - RW - 32 bits - HTIUNBIND:0xF			
Field Name	**Bits**	**Default**	**Description**
GCM_Eff_Wrr_1_pri	1:0	0x2	
GCM_ISOC_urgt_pri	3:2	0x0	
GCM_RSP_pri	5:4	0x1	
SPARE_6	6	0x0	
GCM_Eff_Reserved	7	0x0	
GCM_Eff_Wrr_1_len_c	15:8	0x8	
UrgtDispHaultTraffic	16	0x1	
HTIU upstream configuration 8			

HTIU_UPSTREAM_CONFIG_9 - RW - 32 bits - HTIUNBIND:0x10			
Field Name	**Bits**	**Default**	**Description**
GCM_Eff_Wrr_len_ab	7:0	0x8	
SPARE_15_8	15:8	0x0	
GCM_Eff_Wrr_1_len_a	23:16	0x8	
GCM_Eff_Wrr_1_len_b	31:24	0x8	
HTIU upstream configuration 9			

HTIU_UPSTREAM_CONFIG_10 - RW - 32 bits - HTIUNBIND:0x11			
Field Name	**Bits**	**Default**	**Description**
GFX_RC_PressingIsUrgent	0	0x0	
GFX_WC_PressingIsUrgent	1	0x0	
UMA_Rsv_En	2	0x0	
UMA_Rsv_BufCnt	9:4	0x7	
McWrAckFifoSz	15:12	0xf	
GfxMaxRdBufLevel	22:16	0x3f	
DspMaxRdBufLevel	30:24	0x3f	

HTIU_UPSTREAM_CONFIG_11 - RW - 32 bits - HTIUNBIND:0x12			
Field Name	**Bits**	**Default**	**Description**
ForcePostedToIsoc	31:0	0x0	

HTIU_UPSTREAM_CONFIG_12 - RW - 32 bits - HTIUNBIND:0x13			
Field Name	**Bits**	**Default**	**Description**
ForceNonPostedToIsoc	31:0	0x0	

HTIU_UPSTREAM_CONFIG_13 - RW - 32 bits - HTIUNBIND:0x77			
Field Name	**Bits**	**Default**	**Description**
ForceNonZeroSeqID	31:0	0x0	

HTIU_UPSTREAM_CONFIG_19 - RW - 32 bits - HTIUNBIND:0x14			
Field Name	**Bits**	**Default**	**Description**
IGP_ALLAFC_pri	0	0x1	Priority for AFC or ALL (request) in IGP mode 0=Highest 1=Lowest
IGP_RSP_pri	1	0x0	Priority for Response in IGP mode 0=Highest 1=Lowest
ioc_timeout_en	4	0x1	Internal IOC request timeout 0=Disable 1=Enable
gfx_timeout_en	5	0x1	Internal GFX request timeout 0=Disable 1=Enable
ioc_timeout_cnt	11:8	0x7	Internal IOC timeout counter value (each unit here represent 16 LCLK cycles)
gfx_timeout_cnt	15:12	0x7	Internal IOC timeout counter value (each unit here represent 16 LCLK cycles)
ioc_non_zero_SeqID	16	0x0	Change IOC SeqID to match UnitID 0=Disable 1=Enable
gfx_non_zero_SeqID	17	0x0	Changes GFX SeqID to match UnitID 0=Disable 1=Enable
ioc_only_mode_en	20	0x0	Bypass buffer stage in GCM arb mode to improve latency. Note: This feature is only available when in external GFX mode 0=Disable 1=Enable
P_Rsv_BufCnt	21	0x1	Reserve Posted buffer for IGP ALL mode to improve performance 0=Reserve None 1=Reserve One
HTIU upstream configuration 19			

Link_State_Control_0 - RW - 32 bits - HTIUNBIND:0x15			
Field Name	**Bits**	**Default**	**Description**
HT2InitTmr	19:0	0xfffff	Timeout time for HT1 initialization sequence in HT2 mode. This counter counts in LCLK cycles. This register is cleared on POWERGOOD and not RESET
HT1Bypass	20	0x0	Reserved. This register controls no hardware. This register is cleared on POWERGOOD and not RESET
ExtendedSMCEn	21	0x0	Enables upstream decoding of 12-bit system management messages. This register is cleared on POWERGOOD and not RESET
StrictTM4Detection	22	0x0	Ensures that all active lanes see Training Marker 4 at the same time during HT3 initialization. A failure of this check results in an immediate retry. This register is cleared on POWERGOOD and not RESET
GSMAllMode	23	0x0	GSM All Mode. This register is cleared on POWERGOOD and not RESET 1=In lta stage, identifies all requests as GSM requests 0=In lta stage, only indicates GSM requests as GSM requests
LS2HotMode	24	0x0	HT LS2 Hot Mode. This register is cleared on POWERGOOD and not RESET 1=Use HT transmit clock to keep receiver DLLs running during LS2 0=DLLs are placed into either reset or powerdown state during LS2
HT3HiZMode	25	0x0	HT LS3 Transmitter HiZ Mode. This register is cleared on POWERGOOD and not RESET 1=HT transmitter goes into the HiZ state during LS3 0=HT transmitter goes into the TxGndTrm state during LS3
LS3TermDis	26	0x0	HT LS3 Receiver Termination Disable 1=HT receiver termination is disabled during LS3 0=HT receiver termination is enabled during LS3
LS2DLLPwrDn	27	0x0	HT LS2 DLL Power Down Mode 1=HT receiver DLLs are powered down during LS2 0=HT receiver DLLs are not powered down during LS2.
TimeMarginMode	28	0x0	HT Receiver Time Margining Mode 1=Enable time margining only during operational, bist and loopback modes 0=Enable time margining whenever clock recovery is active including training 1,2,3 states
MinDisconTmr	29	0x0	HT Minimum Disconnection Time Timer 1=Force link state controller to stay in the disconnected state for at least 100ns. This applies to both HT1 and HT3 modes 0=No minimum time to stay in the disconnected state
RxVBControl	30	0x0	Receiver VBias Control 1=HT receiver VBias is disabled whenever receiver termination is disabled 0=HT receiver VBias is always enabled
TxVBControl	31	0x0	Transmitter VBias Control 1=HT transmitter VBias is disabled whenever all lanes are in HiZ 0=HT transmitter VBias is always enabled

Link_State_Control_1 - RW - 32 bits - HTIUNBIND:0x16			
Field Name	**Bits**	**Default**	**Description**
HT1ReconCnt	9:0	0x190	HT1 reconnection timer. This timer determines the delay before HT1 initialization used to enable the transmitter and allow it to stabilize. It counts on LCLK
spare_15_10	15:10	0x0	
HT1ReconCntRxEn	25:16	0xc8	HT1 receiver reconnection timer. This timer determines when during HT1ReconCnt, the receiver is enabled before HT1 initialization. It counts on LCLK
All bits in this register are reset on POWERGOOD and not RESET			

Link_State_Control_2 - RW - 32 bits - HTIUNBIND:0x17			
Field Name	**Bits**	**Default**	**Description**
HT1AltCTLInit	0	0x0	Reserved. This register controls no hardware
InfiniteShortRetry	1	0x0	Enables an infinite number of HT3 short retry attempts.
InfiniteLongRetry	2	0x0	Enables an infinite number of HT3 long retry attempts.
ForceHT2AtHT3Freq	3	0x0	Enables Hypertransport 2 behaviour even at Hypertransport 3 frequencies
TmrDlyToTR1	11:4	0xf	This timer control the number of LCLK the link state controller is delayed before entering the Training 1 state.
TmrExitDisc1usOverride	15	0x0	Allows the timer used to exit the HT3 disconnected state to be overridden.
TmrExitDisc1us	26:16	0x0	This register controls the override value for the time used in exiting the HT3 disconnected state. It counts in LCLKs
DisableResetTmr1	27	0x1	
WholeFBCompressEn	28	0x0	
AltVidEn	29	0x0	
GSMinC3Only	30	0x0	
All bits in this register are reset on POWERGOOD and not RESET			

Link_State_Control_3 - RW - 32 bits - HTIUNBIND:0x18			
Field Name	**Bits**	**Default**	**Description**
Tmr200ns	7:0	0x0	Controls the override value for the 200ns timers. It counts in LCLKs.
Tmr0_200us	27:8	0x0	Controls the override value for the 200us timer used by Tmr0. It counts in LCLKs.
Tmr200nsOverride	30	0x0	Allows the 200ns timers used by the ht link state controller to be overridden.
Tmr0_200usOverride	31	0x0	Allows the 200us timer used for Tmr0 to be overridden.
All bits in this register are reset on POWERGOOD and not RESET			

Link_State_Control_4 - RW - 32 bits - HTIUNBIND:0x19			
Field Name	**Bits**	**Default**	**Description**
Tmr1	19:0	0x0	Controls the override value for Tmr1. It counts in LCLKs.
Tmr1Override	31	0x0	Allows Tmr1 to be overridden.
All bits in this register are reset on POWERGOOD and not RESET			

Link_State_Control_5 - RW - 32 bits - HTIUNBIND:0x1A			
Field Name	**Bits**	**Default**	**Description**
Tmr2	19:0	0x0	Controls the override value for Tmr2. It counts in LCLKs.
Tmr2Override	31	0x0	Allows Tmr2 to be overridden.
All bits in this register are reset on POWERGOOD and not RESET			

Link_State_Control_6 - RW - 32 bits - HTIUNBIND:0x1B			
Field Name	**Bits**	**Default**	**Description**
Tmr3	19:0	0x0	Controls the override value for Tmr3. It counts in LCLKs.
Tmr3Override	31	0x0	Allows Tmr3 to be overridden.
All bits in this register are reset on POWERGOOD and not RESET			

Link_State_Control_7 - RW - 32 bits - HTIUNBIND:0x1C			
Field Name	**Bits**	**Default**	**Description**
IdleTmrLimit	15:0	0x0	Controls the initial value of the Idle Timer. It counts in increments of 100ns. This register is cleared on POWERGOOD and not RESET.
IdleTmrEnable	16	0x0	Enables the HT3 Idle Timer. If the Idle Timer is expires during the disconnected state, then a full 200us period is used for training 0. This register is cleared on POWERGOOD and not RESET.
GSMConditionEnable	31:17	0x0	Enables pipeline conditions to detect GSM requests Bit [0]=HT link initialization Bit [1]=ioc_slave P request Bit [2]=ioc_slave NP request Bit [3]=pcie_slave NP request Bit [4]=arb_p request Bit [5]=arb_np request Bit [6]=arb_np isoc request Bit [7]=txl request Bit [8]=lta request Bit [9]=lretry request Bit [10]=txcrc request Bit [11]=htioc_tagxlt tags outstanding

Receiver_Control_0 - RW - 32 bits - HTIUNBIND:0x1D			
Field Name	**Bits**	**Default**	**Description**
T1PhaseLock	0	0x0	Receiver Training 1 Phase Lock. This register is cleared on POWERGOOD and not RESET 1=HT receiver obtains symbol lock in during Training 1 state 0=HT receiver obtains symbol lock in during Training 2 state
StrictT2ToT3	1	0x1	Reciever Strict Training 2 to Training 3 Mode. This register is cleared on POWERGOOD and not RESET 1=HT receiver only transitions from training 2 to training 3 states on a training sequence boundary 0=HT receiver can transition from training 2 to training 3 in the middle of a training sequence
DataRateMatchDis	2	0x0	Data-rate Matching Disable. This register is cleared on POWERGOOD and not RESET 1=Disable data-rate matching capabilities in the HT receiver 0=Enable data-rate matching capabilities in the HT receiver
HT3ModeAllowAnyInsertion	3	0x0	HT3 Receiver Inserted Command Mode. This register is cleared on POWERGOOD and not RESET 1=HT receiver can handle only NOP inserted commands in HT3 mode 0=HT receiver can handle non-NOP non-data inserted commands in HT3 mode.
DisableSyncFloodDetect	4	0x0	Sync Flood Detection Disable. This register is for debugging pruposes. This register is cleared on POWERGOOD and not RESET 1=HT receiver can detect the sync flood pattern and propagate that state to the transmitter 0=HT receiver cannot detect the sync flood state.
SaferSyncFlood	5	0x0	Reserved. This register controls no hardware. This register is cleared on POWERGOOD and not RESET
HT3HardDisconnect	6	0x0	HT3 Receiver Hard Disconnect Mode. This register is cleared on POWERGOOD and not RESET 1=HT receiver shuts off immediately after receiving disconnect NOP 0=HT receiver stays on after receiving disconnect NOP to look for additional disconnect NOPs
RxScramblerDisable	7	0x0	Receiver Scrambler Disable. This register is cleared on POWERGOOD and not RESET 1=HT receiver scrambler is turned off 0=HT receiver scrambler is controlled by the standard scrambler enable bit.
CRCErrorStorageEn	8	0x0	Enables CRC Error Storage 1=Enable CRC Error Storage. 1 incorrect CRC is stored for debugging purposes 0=Disable CRC Error Storage.
CRCErrorStorageMode	9	0x0	CRC Error Storage Mode 1=Capture last CRC Error 0=Capture first CRC Error
CRCErrorStorageClear	10	0x0	CRC Error Storage Clear 1=Clear CRC Error Storage register 0=CRC Error Storage register is writable by hardware
CrcErrorStorageValid (R)	11	0x0	CRC Error Storage Valid 1=CRC Error Storage contains valid data. 0=CRC Error Storage does not contains valid data.

SEMDecode	12	0x0	SEM Decode 1=Enable explicit decoding of SEM packets. 0=Use default decoding for SEM packets.
ExtendedSMDecode	13	0x0	Extended System Management Decode 1=Enable decoding of 12-bit system management packets from the host 0=Only decode 8-bit system management packets from the host.
ForceBCToSB	14	0x0	Forces Broadcast Packets to Southbridge 1=All broadcast packets are forced to go to southbridge. 0=Broadcast packet addresses are decoded by IOC.
PMask	31:16	0xffff	Posted FCB Masking. This register is reset on POWERGOOD and requires a warm reset to take effect. All bits that are set to 1 mask off a posted flow-control buffer. This register is used to test reduced hardware configurations.

Receiver_Control_1 - RW - 32 bits - HTIUNBIND:0x1E

Field Name	Bits	Default	Description
ProtocolDecodeCheckEn	31:0	0x0	

Receiver_Control_2 - R - 32 bits - HTIUNBIND:0x1F

Field Name	Bits	Default	Description
CRCErrorStorageExpected	31:0	0x0	

Receiver_Control_3 - R - 32 bits - HTIUNBIND:0x20

Field Name	Bits	Default	Description
CRCErrorStorageReceived	31:0	0x0	

HT_BIST_Extended_Control_0 - RW - 32 bits - HTIUNBIND:0x21

Field Name	Bits	Default	Description
ErrCountLaneSel	4:0	0x0	
prbs_enable	5	0x0	
HT1_BIST_MODE	6	0x0	

HT_BIST_Extended_Control_1 - R - 32 bits - HTIUNBIND:0x22

Field Name	Bits	Default	Description
ErrCountLane	31:0	0x0	

Transmiter_Control_0 - RW - 32 bits - HTIUNBIND:0x23			
Field Name	**Bits**	**Default**	**Description**
TxPipeOkToRd	3:0	0x7	Defines the number of entry seperating the read and write pointer in the Transmit Fifo. Note: Acceptable value are 1-7. Do not program to 0. LDTSTOP/Reset is needed to update the value)
TxScrambleDisable	4	0x0	Disables the Transmit Scrambler 0=Force Tx Scrambler to be disable 1=Allow Tx Scrambler to be control by HT3 standard register
ZeroReqCrc	5	0x0	Forces a single per packet crc error on a request (the event is edge detect) 0=STOP per packet crc error on a request 1=Trigger per packet crc error on a request
TxTmrOverride	6	0x0	Enables Override for 200ns timer. Change the delay to different value 0=Normal 200ns delay 1=Delay base on TxTmr
Spare (R)	7	0x0	
TxTmr	15:8	0x0	Override Value for the 200ns timer. (LCLK period * TxTmr = New delay)
CheckInvalidSMC	16	0x0	Detects Invalid SMC and transform it to all zero command 0=Disable checking for invalid SMC, forward all SMC upstream 1=Enable checking for invalid SMC
NopAccumEn	17	0x0	Accumulates Buffer release info in Nop 0=Disable Nop Buffer release Accumulation (more single buffer release) 1=Enable Nop Buffer release to accumulate over period of 4 LCLK before pushing into the Nop fifo
CrcWrapDisable	18	0x0	NA. Considered as spare
AckDetCnt	22:19	0x0	Wait time before detect changes in RxNextPktToAck and trigger Nop insertion. Note: InsertAckNopEn nees to be set for this counter to take effect)
InsertAckNopEn	23	0x0	Insert Nop base on perodic detection of RxNextPktToAck 0=Normal mode, detect change of RxNextPktToAck every cycle 1=Periodic mode, detect change of RxNextPktToAck base on a counter. Note: Period is defined by AckDetCnt
HalfRetryBuf	24	0x0	Half the size of retry buffer (update on reset only) 0=Use full retry buffer (64 entries) 1=Use half retry buffer (32 entries)
WaitForRetryAck	25	0x0	Wait until all the retry request got acknowledged 0=Do not wait for retry request acknowledge, send other request right after retry buffer is empty 1=Wait for retry request acknowledge, delay sending any new request
TxResetHT1Dis	26	0x0	NA. Considered as spare
TxClkGateEn	27	0x0	
TxResetHT3En	28	0x0	

Transmiter_Control_1 - RW - 32 bits - HTIUNBIND:0x24			
Field Name	**Bits**	**Default**	**Description**
VC1_UrAddr_upper	31:0	0x0	

Transmiter_Control_2 - RW - 32 bits - HTIUNBIND:0x25			
Field Name	**Bits**	**Default**	**Description**
Reserved_2_3_0	3:0	0x0	
VC1_UrAddr_lower	7:4	0x0	
Reserved_2_31_8	31:8	0x0	

NB_HT_CLK_CNTL_RECEIVER_COMP_CNTL - RW - 32 bits - HTIUNBIND:0x0			
Field Name	**Bits**	**Default**	**Description**
RX_COMPDATA	4:0	0x10	Transmitter rising edge compensation circuitry data value
RX_CTL	6:5	0x0	Receiver rising edge PHY control value 00=Apply RX_CALCOMP directly as the compensation 01=Apply RX_COMPDATA directly as the compensatio 10=Apply the sum of RX_CALCOMP and RX_COMPDATA 11=Apply the diff of RX_CALCOMP and RX_COMPDATA
RESERVED_7	7	0x0	
RX_CALCCOMP (R)	12:8	0x10	Calculated compensation value for the receiver
RESERVED_14_13	14:13	0x0	Bit [14]=CfgHTiu_HT_RX_COMPOVR Bit [13]=CfgHTiu_HT_RX_FCOMPCYC
SUCU	15	0x0	Speeds up compensation update 0=Link PHY compensation values are allowed to changed every 1ms 1=Link PHY compensation values are allowed to changed every 1us
ICGSMAF	23:16	0x0	Internal clock gating system management 0=No power reduction 1=IC power is reduced through gatind of internal clocks
REVERVED_25to24 (R)	25:24	0x0	Bit [25]=CfgHTiu_HT_TX_UPDATE Bit [24]=CfgHTiu_HT_RX_UPDATE
RESERVED_29to26	29:26	0x0	
SULS	30	0x0	Speeds up connection sequence for frequency change 0=PLL lock timer is 100 us 1=PLL lock timer is 1us
CGEN	31	0x0	Clock gating enable 0=Internal clock gating is disabled 1=Internal clock gating is enabled
HT_CLK_CNTL_RECEIVER_COMP_CNTL			

NB_HT_TRANS_COMP_CNTL - RW - 32 bits - HTIUNBIND:0x1			
Field Name	**Bits**	**Default**	**Description**
TXP_COMPDATA	4:0	0xc	Calculates the compensation value for the transmitter falling edge
TXP_CTL	6:5	0x0	Transmitter falling edge PHY control value 00=Apply TXP_CALCCOMP directly 01=Apply TXP_COMPDATA directly 10=Apply the sum of TXP_CALCCOMP and TXP_COMPDATA 11=Apply the diff of TXP_CALCCOMP and TXP_COMPDATA
TXP_CALCCOMP (R)	12:8	0xc	Transmitter falling edge compensation circuitry data value
RESERVED_15_13	15:13	0x0	Bit [15]=CfgHTiu_HT_EMP_EN_TST Bit [14]=CfgHTiu_HT_TX_COMPOVR Bit [13]=CfgHTiu_HT_TX_FCOMPCYC
TXN_COMPDATA	20:16	0xc	Transmitter falling edge compensation circuitry data value
TXN_CTL	22:21	0x0	Transmitter falling edge PHY control value 00=Apply TXN_CALCCOMP directly 01=Apply TXN_COMPDATA directly 10=Apply the sum of TXN_CALCCOMP and TXN_COMPDATA 11=Apply the diff of TXN_CALCCOMP and TXN_COMPDATA
TXN_CALCCOMP (R)	28:24	0xc	Calculates the compensation value for the transmitter falling edge
RESERVED_31to29	31:29	0x0	Bits [31:30]=CfgHTiu_HT_TST Bit [29]=CfgHTiu_HT_EMP_EN
HT transmitter comp control			

NB_LOWER_TOP_OF_DRAM2 - RW - 32 bits - HTIUNBIND:0x30			
Field Name	**Bits**	**Default**	**Description**
ENABLE	0	0x0	
LOWER_TOM2	31:23	0x0	
Top of lower Extended RAM			

NB_UPPER_TOP_OF_DRAM2 - RW - 32 bits - HTIUNBIND:0x31			
Field Name	**Bits**	**Default**	**Description**
UPPER_TOM2	7:0	0x0	
Top of upper Extended RAM			

NB_HTIU_CFG - RW - 32 bits - HTIUNBIND:0x32			
Field Name	**Bits**	**Default**	**Description**
spare_27_0	27:0	0x0	
NB_BAR3_PCIEXP_ENABLE	28	0x0	Enables PCI-E memory mapped register 0=Disable 1=Enable
spare_30_29	30:29	0x0	
HT_CTL1_FREEZE	31	0x1	Keeps CTL[1] bit always high 0=Disable 1=Enable

HT3PHY_CNTL_1 - RW - 32 bits - HTIUNBIND:0x26			
Field Name	**Bits**	**Default**	**Description**
RX_DATA_DEL_0	1:0	0x0	HT1 receiver low data 0 delay setting
RX_DATA_DEL_1	3:2	0x0	HT1 receiver low data 1 delay setting
RX_DATA_DEL_2	5:4	0x0	HT1 receiver low data 2 delay setting
RX_DATA_DEL_3	7:6	0x0	HT1 receiver low data 3 delay setting
RX_DATA_DEL_4	9:8	0x0	HT1 receiver low data 4 delay setting
RX_DATA_DEL_5	11:10	0x0	HT1 receiver low data 5 delay setting
RX_DATA_DEL_6	13:12	0x0	HT1 receiver low data 6 delay setting
RX_DATA_DEL_7	15:14	0x0	HT1 receiver low data 7 delay setting
RX_DATA_DEL_8	17:16	0x0	HT1 receiver low control delay setting
RX_DATA_DEL_9	19:18	0x0	HT1 receiver high data 0 delay setting
RX_DATA_DEL_10	21:20	0x0	HT1 receiver high data 1 delay setting
RX_DATA_DEL_11	23:22	0x0	HT1 receiver high data 2 delay setting
RX_DATA_DEL_12	25:24	0x0	HT1 receiver high data 3 delay setting
RX_DATA_DEL_13	27:26	0x0	HT1 receiver high data 4 delay setting
RX_DATA_DEL_14	29:28	0x0	HT1 receiver high data 5 delay setting
RX_DATA_DEL_15	31:30	0x0	HT1 receiver high data 6 delay setting

HT3PHY_CNTL_2 - RW - 32 bits - HTIUNBIND:0x27			
Field Name	**Bits**	**Default**	**Description**
RX_DATA_DEL_16	1:0	0x0	HT1 receiver high data 7 delay setting
RX_DATA_DEL_17	3:2	0x0	HT1 receiver high control delay setting
RX_CLK_DEL_0	5:4	0x0	HT1 receiver low clock 0 delay setting
RX_CLK_DEL_1	7:6	0x0	HT1 receiver low clock 1 delay setting
RX_CLK_DEL_2	9:8	0x0	HT1 receiver low clock 2 delay setting
RX_CLK_DEL_3	11:10	0x0	HT1 receiver low clock 3 delay setting
RX_CLK_DEL_4	13:12	0x0	HT1 receiver low clock 4 delay setting
RX_CLK_DEL_5	15:14	0x0	HT1 receiver low clock 5 delay setting
RX_CLK_DEL_6	17:16	0x0	HT1 receiver low clock 6 delay setting
RX_CLK_DEL_7	19:18	0x0	HT1 receiver low clock 7 delay setting
RX_CLK_DEL_8	21:20	0x0	HT1 receiver low clock 8 delay setting
RX_CLK_DEL_9	23:22	0x0	HT1 receiver high clock 0 delay setting
RX_CLK_DEL_10	25:24	0x0	HT1 receiver high clock 1 delay setting
RX_CLK_DEL_11	27:26	0x0	HT1 receiver high clock 2 delay setting
RX_CLK_DEL_12	29:28	0x0	HT1 receiver high clock 3 delay setting
RX_CLK_DEL_13	31:30	0x0	HT1 receiver high clock 4 delay setting

HT3PHY_CNTL_3 - RW - 32 bits - HTIUNBIND:0x28			
Field Name	**Bits**	**Default**	**Description**
RX_CLK_DEL_14	1:0	0x0	HT1 receiver high clock 5 delay setting
RX_CLK_DEL_15	3:2	0x0	HT1 receiver high clock 6 delay setting
RX_CLK_DEL_16	5:4	0x0	HT1 receiver high clock 7 delay setting
RX_CLK_DEL_17	7:6	0x0	HT1 receiver high clock 8 delay setting
OFFSET_C_EN	8	0x0	Enables Rx receiver offset cancelation 1=Enable 0=Disable (default)
RX_CROUT_SEL	9	0x1	CR observability setting for RX_CROUT[6:0] 0=7-bit clock recovery frequency estimator output 1=7-bit clock recovery phase counter output
RX_CRFR_ON	10	0x0	0=Clock recovery frequency loop disabled 1=Clock recovery frequency loop enabled
RX_CRFR_BPASS	11	0x0	Bypasses the clock recovery Freq Estimator output with RX_CRFR[5:0].
RX_CRCTRL_BPASS	12	0x0	Bypasses the clock recovery Phase Counter output with RX_CRCTRL[6:0]
RX_CRFR	18:13	0x0	Bypass value for the clock recovery Freq Estimator output. Selected by asserting RX_CRFR_BPASS.
RX_CRFRSIZE	20:19	0x1	Clock recovery Freq Filter size.
RX_CRPHSIZE	22:21	0x1	Clock recovery Phase Filter size
RX_CRCTRL	29:23	0x0	Bypass value for the clock recovery Phase Counter output. Selected by asserting RX_CRCTRL_BPASS
RX_CR_ENABLE	30	0x1	Clock recovery (Rx_cdr) enable 0=Clock recovery parameter locked 1=Clock recovery parameter allowed to be updated according to the Rx input.
RX_CR_ENABLE_CNTL	31	0x0	External CR_ENABLE control 0=Core control 1=Register control

HT3PHY_CNTL_4 - RW - 32 bits - HTIUNBIND:0x29			
Field Name	**Bits**	**Default**	**Description**
RX_DLL_bypass	0	0x0	DLL bypass for test mode 0=Normal Operation 1=Bypass DLL
RX_DLL_reset	2:1	0x3	Reset DLL 0=Normal operation 1=Reset
RX_DLL_PWRDN	4:3	0x3	DLL power down 0=Normal operation 1=Power down
RX_DLL_CLKSEL	22:5	0x0	DLL clock inputs selection 0=clk_ina 1=clk_inb
RX_PDNB	24:23	0x3	Receiver power down (active low) 0=Power down 1=Normal operation
RX_DLL_CNTL_EN	25	0x0	External DLL control 0=Core control 1=Register control
TSTCTRL_3	26	0x0	Test control for DLL, bit [3]
PAD_UPDATE_RATE	31:27	0x3	Calibration pad update interval

HT3PHY_CNTL_5 - RW - 32 bits - HTIUNBIND:0x2A			
Field Name	**Bits**	**Default**	**Description**
CORE_TX_DRV_STR	1:0	0x0	Drive strength
TX_CLKL_PDWN	2	0x0	Power down the low clock buffers 0=Disable 1=Enable
TX_CLKH_PDWN	3	0x0	Power down the high clock buffers 0=Disable 1=Enable
TX_CLKL_TXGNDTRM_EN	4	0x0	Special HT3 power mode 0=Disable 1=Enable
TX_CLKH_TXGNDTRM_EN	5	0x0	Special HT3 power mode 0=Disable 1=Enable
CORE_TX_POWERDOWN_EN	23:6	0x0	Power down is used to disable a bit 0=Active 1=Power down
TSTCTRL_2_0	26:24	0x7	Test control for DLL, bits [2:0]
PAD_SAMPLE_DELAY	31:27	0x2	Delay in between samples for calibration

HT3PHY_CNTL_6 - RW - 32 bits - HTIUNBIND:0x2B			
Field Name	**Bits**	**Default**	**Description**
CORE_TX_TXGNDTRM_EN	17:0	0x0	Disables termination and pull down on both sides of the driver 0=Active 1=Disable
PAD_INC_THRESHOLD	22:18	0x8	Upper limit for calibration threshold
PAD_DEC_THRESHOLD	27:23	0x6	Lower limit for calibration threshold
TX_BIAS_3_0	31:28	0x0	BIAS control for transmitter. Enables the bias circuits in every bit as follows: TX_BIAS_3=Bits [3, 7, 11, 15] TX_BIAS_2=Bits [1, 5, 9, 13] TX_BIAS_1=Bits [0, 4, 8, 12] TX_BIAS_0=Bits CLKH, CLKL, CTLH, CTLL Bias circuits for bits 2, 6, 10, 14 are always enabled.

HT3PHY_CNTL_7 - RW - 32 bits - HTIUNBIND:0x2C			
Field Name	**Bits**	**Default**	**Description**
CDRAutoFreezeOn	4:0	0x0	
CDRAutoFreezeOff	12:8	0x0	
CRDAutoFreezeEn	16	0x0	

Receiver_Control_4 - RW - 32 bits - HTIUNBIND:0x33			
Field Name	**Bits**	**Default**	**Description**
PStateMask	15:0	0x0	

NB_HT_CLMC_I - RW - 32 bits - HTIUNBIND:0x34			
Field Name	**Bits**	**Default**	**Description**
ACDCSel	0	0x0	Selects AC/DC link frequency setting
RegLMM	4:1	0x0	Sets LMM; default is LMM0
RegLWup	7:5	0x0	Sets upstream LW; default is 8-bit
RegLWdn	10:8	0x0	Sets downstream LW; default is 8-bit
RegFreqAC	14:11	0x0	Sets AC link frequency; default is 200MHz
RegFreqDC	18:15	0x0	Sets DC link frequency; default is 200MHz
LMMSel	20:19	0x1	Selects LMM; default is LMM0
LWSel	22:21	0x1	Selects Up/Down LW; default is CfgLW
FreqSel	24:23	0x0	Selects link frequency; default is CfgFreq
MaxUpLW	27:25	0x1	Max allowable Up LW; default is 16-bit
MaxDnLW	30:28	0x1	Max allowable Down LW; default is 16-bit
McuLMM_TimerSel	31	0x0	Uses MCU LMM timers instead

NB_HT_CLMC_II - RW - 32 bits - HTIUNBIND:0x35			
Field Name	**Bits**	**Default**	**Description**
MinUpLW	2:0	0x0	Min allowable Up LW; default is 2-bit
MinDnLW	5:3	0x0	Min allowable Down LW; default is 2-bit
ForceAssert	6	0x1	Forces extra LDTSTOP assertion
LdtStopBypassMode	8:7	0x0	Chooses conditions for full/bypass paths
LookAtInactiveRX	9	0x0	Includes inactive RX lanes in CILR
LookAtFBC	10	0x1	Includes FBC status
ForceAllowLdtStop	11	0x0	Forces AllowLdtStop high
ForceCILRAfterCDLR	12	0x0	Forces CILR after CDLR
BWEstmMode	14:13	0x0	Estimation mode; default is display only or stutter mode
LWStutterEn	15	0x0	Enables stutter mode path for next LW
UpLWStutterEn	16	0x1	Enables upstream stutter mode LW
DnLWStutterEn	17	0x1	Enables downstream stutter mode LW
LegacyStutterEn	18	0x1	Enables legacy stutter mode to do disconnect
HtTwoBitEn	19	0x0	Consider 2-bit LW in BW estimation
HtFourBitEn	20	0x0	Consider 4-bit LW in BW estimation
UseProgMaxLW	21	0x0	Controls the use of programmable max LW limit
BypassVblankWait	22	0x0	Controls the wait on Vblank during frequency updates
SPARE_II	31:23	0x0	

NB_HT_ARB_I - RW - 32 bits - HTIUNBIND:0x36			
Field Name	**Bits**	**Default**	**Description**
HT_ARB_RegSel	0	0x0	Chooses between MCGFX and NBCFG version of arbitration registers; default is MCGFX
IOCTimeoutThreshold	8:1	0xf	IOC timeout value
IOCTimeoutBurst	12:9	0x1	Number of IOC requests to send before resetting the IOC timeout counter
TargetReservedIsocCredits	20:13	0x7	Number of reserved Isoc credits
IsocReadBurstSize	25:21	0x8	Target number of Isoc reads before switching to non-Isoc reads
NormalReadBurstSize	30:26	0x8	Burst size for normal reads
SPARE_III	31	0x0	

NB_HT_ARB_II - RW - 32 bits - HTIUNBIND:0x37			
Field Name	**Bits**	**Default**	**Description**
AnyReadBurstSize	4:0	0x8	Burst size for any read
WriteBurstSize	9:5	0x8	Burst size for writes
SPARE_IV	31:10	0x0	

LS_History0 - R - 32 bits - HTIUNBIND:0x40			
Field Name	**Bits**	**Default**	**Description**
LS_History0	31:0	0x0	Bits [5:0]=Current HT Link State Bits [11:6]=Previous HT Link State 1 Bits [17:12]=Previous HT Link State 2 Bits [23:18]=Previous HT Link State 3 Bits [29:24]=Previous HT Link State 4 Bits [31:30]=Previous HT Link State 5

LS_History1 - R - 32 bits - HTIUNBIND:0x41			
Field Name	**Bits**	**Default**	**Description**
LS_History1	31:0	0x0	Bits [3:0]=Previous HT Link State 5 Bits [9:4]=Previous HT Link State 6 Bits [15:10]=Previous HT Link State 7 Bits [21:16]=Previous HT Link State 8 Bits [27:22]=Previous HT Link State 9 Bits [31:28]=Previous HT Link State 10

LS_History2 - R - 32 bits - HTIUNBIND:0x42			
Field Name	**Bits**	**Default**	**Description**
LS_History2	31:0	0x0	Bits [1:0]=Previous HT Link State 10 Bits [7:2]=Previous HT Link State 11 Bits [13:8]=Previous HT Link State 12 Bits [19:14]=Previous HT Link State 13 Bits [25:20]=Previous HT Link State 14 Bits [31:26]=Previous HT Link State 15

LS_History3 - R - 32 bits - HTIUNBIND:0x43			
Field Name	**Bits**	**Default**	**Description**
LS_History3	31:0	0x0	Bits [5:0]=Previous HT Link State 16 Bits [11:6]=Previous HT Link State 17 Bits [17:12]=Previous HT Link State 18 Bits [23:18]=Previous HT Link State 19 Bits [29:24]=Previous HT Link State 20 Bits [31:30]=Previous HT Link State 21

LS_History4 - R - 32 bits - HTIUNBIND:0x44			
Field Name	**Bits**	**Default**	**Description**
LS_History4	31:0	0x0	Bits [3:0]=Previous HT Link State 21 Bits [9:4]=Previous HT Link State 22 Bits [15:10]=Previous HT Link State 23 Bits [21:16]=Previous HT Link State 24 Bits [27:22]=Previous HT Link State 25 Bits [31:28]=Previous HT Link State 26

LS_History5 - R - 32 bits - HTIUNBIND:0x45			
Field Name	**Bits**	**Default**	**Description**
LS_History5	31:0	0x0	Bits [1:0]=Previous HT Link State 26 Bits [7:2]=Previous HT Link State 27 Bits [13:8]=Previous HT Link State 28 Bits [19:14]=Previous HT Link State 29 Bits [25:20]=Previous HT Link State 30 Bits [31:26]=Previous HT Link State 31

TX_B_P90PLL_IBias - RW - 32 bits - HTIUNBIND:0x46			
Field Name	**Bits**	**Default**	**Description**
P90PLL_IBias	9:0	0x0	
LVM_en	16	0x0	

CLMC_I - RW - 32 bits - HTIUNBIND:0x50			
Field Name	**Bits**	**Default**	**Description**
CLMC_En	0	0x0	Global CLMC enable
CpuCores	4:1	0x0	Number of CPU cores (program 1 less than actual); default is 1 core
ForcePmHtHV	5	0x0	Forces the PM high voltage status signal high
ForceClmcPmHVReq	6	0x0	Forces the CLMC high voltage request signal high
ForceInitHaltState	7	0x0	Adjusts the CLMC halt counter at boot-up
InitCoresInHalt	12:8	0x0	Number of CPU cores already in halt at boot-up
HaltTimerVal	30:13	0x0	Time to wait after all CPU cores have halted
ClmcRegSetSel	31	0x0	Chooses between the MCCFG and HTIUNBCFG version of the registers. The default is MCCFG.

CLMC_ReadBack - R - 32 bits - HTIUNBIND:0x51			
Field Name	**Bits**	**Default**	**Description**
RbLMAFResult	3:0	0x0	Final LMAF result used to mux out LMM to HTIU
RbLWupResult	6:4	0x0	Final upstream link width result for HTIU
RbLWdnResult	9:7	0x0	Final downstream link width result for HTIU
RbFreqResult	13:10	0x0	Final frequency result for HTIU
RbNextLMM	17:14	0x0	Next calculated LMAF
RbNextUpLW	20:18	0x0	Next calculated upstream link width
RbNextDnLW	23:21	0x0	Next calculated downstream link width
RbNextFreq	27:24	0x0	Next calculated frequency
SPARE	31:28	0x0	

CLMC_CONTROL_I - RW - 32 bits - HTIUNBIND:0x52			
Field Name	**Bits**	**Default**	**Description**
LRCmdActive	2:0	0x0	CILR active command; bottom three bits
LRCmdInactive	5:3	0x0	CILR inactive command; bottom three bits
CILRTimerVal	23:6	0x186a0	Time to wait before doing next CILR; default is 10ms
SPARE_31_24	31:24	0x0	

CLMC_CONTROL_II - RW - 32 bits - HTIUNBIND:0x53			
Field Name	**Bits**	**Default**	**Description**
MinLdtStopOnTime	17:0	0xb	Min LDTSTOP assertion time; default is 1us

CLMC_CONTROL_III - RW - 32 bits - HTIUNBIND:0x54			
Field Name	**Bits**	**Default**	**Description**
MinLdtStopOffTime	17:0	0x3c	

CLMC_LMM_St1 - RW - 32 bits - HTIUNBIND:0x55			
Field Name	**Bits**	**Default**	**Description**
TrafficSel1	2:0	0x7	Determines what traffic to look for while in LMM state 1; default is to look at all traffic
LMMTimerVal1	20:3	0x2710	Timer value for LMM1 state; default is 1ms

CLMC_LMM_St2 - RW - 32 bits - HTIUNBIND:0x56			
Field Name	**Bits**	**Default**	**Description**
TrafficSel2	2:0	0x7	Determines what traffic to look for while in LMM state 2; default is to look at all traffic
LMMTimerVal2	20:3	0x9c40	Timer value for LMM2 state; default is 4ms

CLMC_LMM_St3 - RW - 32 bits - HTIUNBIND:0x57			
Field Name	**Bits**	**Default**	**Description**
TrafficSel3	2:0	0x7	Determines what traffic to look for while in LMM state 3; default is to look at all traffic
LMMTimerVal3	20:3	0x13880	Timer value for LMM3 state; default is 8ms

CLMC_LMM_St4 - RW - 32 bits - HTIUNBIND:0x58			
Field Name	**Bits**	**Default**	**Description**
TrafficSel4	2:0	0x7	Determines what traffic to look for while in LMM state 4; default is to look at all traffic
LMMTimerVal4	20:3	0x2710	Timer value for LMM4 state; default is 1ms

CLMC_LMM_St5 - RW - 32 bits - HTIUNBIND:0x59			
Field Name	**Bits**	**Default**	**Description**
TrafficSel5	2:0	0x7	Determines what traffic to look for while in LMM state 5; default is to look at all traffic
LMMTimerVal5	20:3	0x9c40	Timer value for LMM5 state; default is 4ms

CLMC_LMM_St6 - RW - 32 bits - HTIUNBIND:0x5A			
Field Name	**Bits**	**Default**	**Description**
TrafficSel6	2:0	0x7	Determines what traffic to look for while in LMM state 6; default is to look at all traffic
LMMTimerVal6	20:3	0x13380	Timer value for LMM6 state; default is 8ms

CLMC_BWESTM_I - RW - 32 bits - HTIUNBIND:0x5B			
Field Name	**Bits**	**Default**	**Description**
SetMaxLW	0	0x0	Sets the next calculated LW to the max value allowable (if LW is currently increasing)
ClientEn	17:1	0x1ffff	Chooses which clients to consider when calculating the next LW; default is to consider all clients
SPARE_31_18	31:18	0x0	

CLMC_BWESTM_ClientBw1 - RW - 32 bits - HTIUNBIND:0x5C			
Field Name	**Bits**	**Default**	**Description**
BIFbwUp	7:0	0x80	Client upstream bandwidth requirement
GFX0bwUp	15:8	0x80	Client upstream bandwidth requirement
GFX1bwUp	23:16	0x80	Client upstream bandwidth requirement
GPP0bwUp	31:24	0x80	Client upstream bandwidth requirement

CLMC_BWESTM_ClientBw2 - RW - 32 bits - HTIUNBIND:0x5D			
Field Name	**Bits**	**Default**	**Description**
GPP1bwUp	7:0	0x80	Client upstream bandwidth requirement
GPP2bwUp	15:8	0x80	Client upstream bandwidth requirement
GPP3bwUp	23:16	0x80	Client upstream bandwidth requirement
SBbwUp	31:24	0x80	Client upstream bandwidth requirement

CLMC_BWESTM_ClientBw3 - RW - 32 bits - HTIUNBIND:0x5E			
Field Name	**Bits**	**Default**	**Description**
GPP4bwUp	7:0	0x80	Client upstream bandwidth requirement
GPP5bwUp	15:8	0x80	Client upstream bandwidth requirement
GFX2bwUp	23:16	0x80	Client upstream bandwidth requirement
GFX3bwUp	31:24	0x80	Client upstream bandwidth requirement

CLMC_BWESTM_ClientBw4 - RW - 32 bits - HTIUNBIND:0x5F			
Field Name	**Bits**	**Default**	**Description**
VC1bwUp	7:0	0x80	Client upstream bandwidth requirement
IntGFXIbwUp	15:8	0x80	Client upstream bandwidth requirement
IntGFXIIbwUp	23:16	0x80	Client upstream bandwidth requirement
IntDISPIbwUp	31:24	0x80	Client upstream bandwidth requirement

CLMC_BWESTM_ClientBw5 - RW - 32 bits - HTIUNBIND:0x60			
Field Name	**Bits**	**Default**	**Description**
IntDISPIIbwUp	7:0	0x80	Client upstream bandwidth requirement
BIFbwDn	15:8	0x80	Client downstream bandwidth requirement
GFX0bwDn	23:16	0x80	Client downstream bandwidth requirement
GFX1bwDn	31:24	0x80	Client downstream bandwidth requirement

CLMC_BWESTM_ClientBw6 - RW - 32 bits - HTIUNBIND:0x61			
Field Name	**Bits**	**Default**	**Description**
GPP0bwDn	7:0	0x80	Client downstream bandwidth requirement
GPP1bwDn	15:8	0x80	Client downstream bandwidth requirement
GPP2bwDn	23:16	0x80	Client downstream bandwidth requirement
GPP3bwDn	31:24	0x80	Client downstream bandwidth requirement

CLMC_BWESTM_ClientBw7 - RW - 32 bits - HTIUNBIND:0x62			
Field Name	**Bits**	**Default**	**Description**
SBbwDn	7:0	0x80	Client downstream bandwidth requirement
GPP4bwDn	15:8	0x80	Client downstream bandwidth requirement
GPP5bwDn	23:16	0x80	Client downstream bandwidth requirement
GFX2bwDn	31:24	0x80	Client downstream bandwidth requirement

CLMC_BWESTM_ClientBw8 - RW - 32 bits - HTIUNBIND:0x63			
Field Name	**Bits**	**Default**	**Description**
GFX3bwDn	7:0	0x80	Client downstream bandwidth requirement
VC1bwDn	15:8	0x80	Client downstream bandwidth requirement
IntGFXIbwDn	23:16	0x80	Client downstream bandwidth requirement
IntGFXIIbwDn	31:24	0x80	Client downstream bandwidth requirement

CLMC_BWESTM_ClientBw9 - RW - 32 bits - HTIUNBIND:0x64			
Field Name	**Bits**	**Default**	**Description**
IntDISPIbwDn	7:0	0x80	Client downstream bandwidth requirement
IntDISPIIbwDn	15:8	0x80	Client downstream bandwidth requirement

CLMC_BWESTM_BwRange1 - RW - 32 bits - HTIUNBIND:0x65			
Field Name	**Bits**	**Default**	**Description**
CheckLMM	0	0x1	Checks for NewLMM when deciding disconnect
CheckLW	1	0x1	Checks for NewLW when deciding disconnect
CheckFreq	2	0x1	Checks for NewFreq when deciding disconnect
UseAltBWTimerRst	3	0x0	Uses the alternate method for timer restart
BypassMCU	4	0x0	Bypasses MCU for LMM and LW during StpClk
SPARE	12:5	0x0	
LW2high_LW4low	25:13	0x80	Upper/lower limit for LW2/LW4 assignment

CLMC_BWESTM_BwRange2 - RW - 32 bits - HTIUNBIND:0x66			
Field Name	**Bits**	**Default**	**Description**
LW4high_LW8low	12:0	0x800	Upper/lower limit for LW4/LW8 assignment
LW8high_LW16low	25:13	0x1000	Upper/lower limit for LW8/LW16 assignment

CLMC_BWESTM_BwRange3 - RW - 32 bits - HTIUNBIND:0x67			
Field Name	**Bits**	**Default**	**Description**
SPARE	12:0	0x0	

CLMC_BWESTM_Timer1 - RW - 32 bits - HTIUNBIND:0x68			
Field Name	**Bits**	**Default**	**Description**
IdleTimerVal	17:0	0xb	Time to wait before indicating HT link is idle; default is 1us

CLMC_BWESTM_Timer2 - RW - 32 bits - HTIUNBIND:0x69			
Field Name	**Bits**	**Default**	**Description**
LWIncTimerVal	17:0	0x5	Time to wait before sending next LW (when LW is currently increasing); default is 500ns

CLMC_BWESTM_Timer3 - RW - 32 bits - HTIUNBIND:0x6A			
Field Name	**Bits**	**Default**	**Description**
LWDecTimerVal	17:0	0xb	Time to wait before sending next LW (when LW is currently not increasing); default is 1us

CLMC_CONTROL_IV - RW - 32 bits - HTIUNBIND:0x6B			
Field Name	**Bits**	**Default**	**Description**
MinLdtStopOnTimeLMM	17:0	0xb	Min LDTSTOP assertion time for an LMM change; default is 1us

CLMC_CONTROL_V - RW - 32 bits - HTIUNBIND:0x6C			
Field Name	**Bits**	**Default**	**Description**
MinLdtStopOnTimeLW	17:0	0xb	Min LDTSTOP assertion time for an LW change; default is 1us

CLMC_CONTROL_VI - RW - 32 bits - HTIUNBIND:0x6D			
Field Name	**Bits**	**Default**	**Description**
MinLdtStopOnTimeFreq	17:0	0xb	Min LDTSTOP assertion time for a Frequency change; default is 1us

LMM1 - RW - 32 bits - HTIUNBIND:0x70			
Field Name	**Bits**	**Default**	**Description**
LMM1_T0Time	5:0	0x0	T0 training time
LMM1_FullT0Time	11:6	0x0	Full T0 training time
LMM1_RxInLnSt	13:12	0x0	RX inactive lane state
LMM1_TxInLnSt	15:14	0x0	TX inactive lane state
LMM1_RxLSSel	17:16	0x0	RX link state select
LMM1_TxLSSel	19:18	0x0	TX link state select
LMM1_Deemph	24:20	0x0	Deemphasis setting
LMM1_HiZMode	25	0x0	High impedance mode
LMM1_TermDis	26	0x0	Termination disable
LMM1_LS2DLLPwrDn	27	0x0	DLL power down in LS2
LMM1_RxVBControl	28	0x0	RX vbias control
LMM1_TxVBControl	29	0x0	TX vbias control
LMM1_Reserved	31:30	0x0	Reserved

LMM2 - RW - 32 bits - HTIUNBIND:0x71			
Field Name	**Bits**	**Default**	**Description**
LMM2_T0Time	5:0	0x0	T0 training time
LMM2_FullT0Time	11:6	0x0	Full T0 training time
LMM2_RxInLnSt	13:12	0x0	RX inactive lane state
LMM2_TxInLnSt	15:14	0x0	TX inactive lane state
LMM2_RxLSSel	17:16	0x0	RX link state select
LMM2_TxLSSel	19:18	0x0	TX link state select
LMM2_Deemph	24:20	0x0	Deemphasis setting
LMM2_HiZMode	25	0x0	High impedance mode
LMM2_TermDis	26	0x0	Termination disable
LMM2_LS2DLLPwrDn	27	0x0	DLL power down in LS2
LMM2_RxVBControl	28	0x0	RX vbias control
LMM2_TxVBControl	29	0x0	TX vbias control
LMM2_Reserved	31:30	0x0	Reserved

LMM3 - RW - 32 bits - HTIUNBIND:0x72			
Field Name	**Bits**	**Default**	**Description**
LMM3_T0Time	5:0	0x0	T0 training time
LMM3_FullT0Time	11:6	0x0	Full T0 training time
LMM3_RxInLnSt	13:12	0x0	RX inactive lane state
LMM3_TxInLnSt	15:14	0x0	TX inactive lane state
LMM3_RxLSSel	17:16	0x0	RX link state select
LMM3_TxLSSel	19:18	0x0	TX link state select
LMM3_Deemph	24:20	0x0	Deemphasis setting
LMM3_HiZMode	25	0x0	High impedance mode
LMM3_TermDis	26	0x0	Termination disable
LMM3_LS2DLLPwrDn	27	0x0	DLL power down in LS2
LMM3_RxVBControl	28	0x0	RX vbias control
LMM3_TxVBControl	29	0x0	TX vbias control
LMM3_Reserved	31:30	0x0	Reserved

LMM4 - RW - 32 bits - HTIUNBIND:0x73			
Field Name	**Bits**	**Default**	**Description**
LMM4_T0Time	5:0	0x0	T0 training time
LMM4_FullT0Time	11:6	0x0	Full T0 training time
LMM4_RxInLnSt	13:12	0x0	RX inactive lane state
LMM4_TxInLnSt	15:14	0x0	TX inactive lane state
LMM4_RxLSSel	17:16	0x0	RX link state select
LMM4_TxLSSel	19:18	0x0	TX link state select
LMM4_Deemph	24:20	0x0	Deemphasis setting
LMM4_HiZMode	25	0x0	High impedance mode
LMM4_TermDis	26	0x0	Termination disable
LMM4_LS2DLLPwrDn	27	0x0	DLL power down in LS2
LMM4_RxVBControl	28	0x0	RX vbias control
LMM4_TxVBControl	29	0x0	TX vbias control
LMM4_Reserved	31:30	0x0	Reserved

LMM5 - RW - 32 bits - HTIUNBIND:0x74			
Field Name	**Bits**	**Default**	**Description**
LMM5_T0Time	5:0	0x0	T0 training time
LMM5_FullT0Time	11:6	0x0	Full T0 training time
LMM5_RxInLnSt	13:12	0x0	RX inactive lane state
LMM5_TxInLnSt	15:14	0x0	TX inactive lane state
LMM5_RxLSSel	17:16	0x0	RX link state select
LMM5_TxLSSel	19:18	0x0	TX link state select
LMM5_Deemph	24:20	0x0	Deemphasis setting
LMM5_HiZMode	25	0x0	High impedance mode
LMM5_TermDis	26	0x0	Termination disable
LMM5_LS2DLLPwrDn	27	0x0	DLL power down in LS2
LMM5_RxVBControl	28	0x0	RX vbias control
LMM5_TxVBControl	29	0x0	TX vbias control
LMM5_Reserved	31:30	0x0	Reserved

LMM6 - RW - 32 bits - HTIUNBIND:0x75			
Field Name	**Bits**	**Default**	**Description**
LMM6_T0Time	5:0	0x0	T0 training time
LMM6_FullT0Time	11:6	0x0	Full T0 training time
LMM6_RxInLnSt	13:12	0x0	RX inactive lane state
LMM6_TxInLnSt	15:14	0x0	TX inactive lane state
LMM6_RxLSSel	17:16	0x0	RX link state select
LMM6_TxLSSel	19:18	0x0	TX link state select
LMM6_Deemph	24:20	0x0	Deemphasis setting
LMM6_HiZMode	25	0x0	High impedance mode
LMM6_TermDis	26	0x0	Termination disable
LMM6_LS2DLLPwrDn	27	0x0	DLL power down in LS2
LMM6_RxVBControl	28	0x0	RX vbias control
LMM6_TxVBControl	29	0x0	TX vbias control
LMM6_Reserved	31:30	0x0	Reserved

LMM7 - RW - 32 bits - HTIUNBIND:0x76			
Field Name	**Bits**	**Default**	**Description**
LMM7_T0Time	5:0	0x0	T0 training time
LMM7_FullT0Time	11:6	0x0	Full T0 training time
LMM7_RxInLnSt	13:12	0x0	RX inactive lane state
LMM7_TxInLnSt	15:14	0x0	TX inactive lane state
LMM7_RxLSSel	17:16	0x0	RX link state select
LMM7_TxLSSel	19:18	0x0	TX link state select
LMM7_Deemph	24:20	0x0	Deemphasis setting
LMM7_HiZMode	25	0x0	High impedance mode
LMM7_TermDis	26	0x0	Termination disable
LMM7_LS2DLLPwrDn	27	0x0	DLL power down in LS2
LMM7_RxVBControl	28	0x0	RX vbias control
LMM7_TxVBControl	29	0x0	TX vbias control
LMM7_Reserved	31:30	0x0	Reserved

NB_HTIU_SPARE - RW - 32 bits - HTIUNBIND:0x2D			
Field Name	**Bits**	**Default**	**Description**
NB_HTIU_SPARE_31_0	31:0	0x7	

HT3PHY_CNTL_8 - RW - 32 bits - HTIUNBIND:0x47			
Field Name	**Bits**	**Default**	**Description**
RX_CRCTRL_1	6:0	0x0	Bypass value for the clock recovery Phase Counter output, bit [1]. Selected by asserting RX_CRCTRL_BPASS
RSVD1	7	0x0	Reserved for future use
RX_CRCTRL_2	14:8	0x0	Bypass value for the clock recovery Phase Counter output, bit [2]. Selected by asserting RX_CRCTRL_BPASS
RSVD2	15	0x0	Reserved for future use
RX_CRCTRL_3	22:16	0x0	Bypass value for the clock recovery Phase Counter output, bit [3]. Selected by asserting RX_CRCTRL_BPASS
RSVD3	23	0x0	Reserved for future use
RX_CRCTRL_4	30:24	0x0	Bypass value for the clock recovery Phase Counter output, bit [4]. Selected by asserting RX_CRCTRL_BPASS
RSVD4	31	0x0	Reserved for future use

HT3PHY_CNTL_9 - RW - 32 bits - HTIUNBIND:0x48			
Field Name	**Bits**	**Default**	**Description**
RX_CRCTRL_5	6:0	0x0	Bypass value for the clock recovery Phase Counter output, bit [5]. Selected by asserting RX_CRCTRL_BPASS
RSVD5	7	0x0	Reserved for future use
RX_CRCTRL_6	14:8	0x0	Bypass value for the clock recovery Phase Counter output, bit [6]. Selected by asserting RX_CRCTRL_BPASS
RSVD6	15	0x0	Reserved for future use
RX_CRCTRL_7	22:16	0x0	Bypass value for the clock recovery Phase Counter output, bit [7]. Selected by asserting RX_CRCTRL_BPASS
RSVD7	23	0x0	Reserved for future use
RX_CRCTRL_CTLL	30:24	0x0	Bypass value for the clock recovery Phase Counter output, low ctl. Selected by asserting RX_CRCTRL_BPASS
RSVD8	31	0x0	Reserved for future use

HT3PHY_CNTL_10 - RW - 32 bits - HTIUNBIND:0x49			
Field Name	**Bits**	**Default**	**Description**
RX_CRCTRL_8	6:0	0x0	Bypass value for the clock recovery Phase Counter output, bit [8]. Selected by asserting RX_CRCTRL_BPASS
RSVD9	7	0x0	Reserved for future use
RX_CRCTRL_9	14:8	0x0	Bypass value for the clock recovery Phase Counter output, bit [9]. Selected by asserting RX_CRCTRL_BPASS
RSVD10	15	0x0	Reserved for future use
RX_CRCTRL_10	22:16	0x0	Bypass value for the clock recovery Phase Counter output, bit [10]. Selected by asserting RX_CRCTRL_BPASS
RSVD11	23	0x0	Reserved for future use
RX_CRCTRL_11	30:24	0x0	Bypass value for the clock recovery Phase Counter output, bit [11]. Selected by asserting RX_CRCTRL_BPASS
RSVD12	31	0x0	Reserved for future use

HT3PHY_CNTL_11 - RW - 32 bits - HTIUNBIND:0x4A			
Field Name	**Bits**	**Default**	**Description**
RX_CRCTRL_12	6:0	0x0	Bypass value for the clock recovery Phase Counter output, bit [12]. Selected by asserting RX_CRCTRL_BPASS
RSVD13	7	0x0	Reserved for future use
RX_CRCTRL_13	14:8	0x0	Bypass value for the clock recovery Phase Counter output, bit [13]. Selected by asserting RX_CRCTRL_BPASS
RSVD14	15	0x0	Reserved for future use
RX_CRCTRL_14	22:16	0x0	Bypass value for the clock recovery Phase Counter output, bit [14]. Selected by asserting RX_CRCTRL_BPASS
TX_CLK_RESET_EN_LOW_B	23	0x0	Control of reset going to low clock pad 0=Clock pad sees tx_reset 1=Clock pad has the tx_reset blocked
RX_CRCTRL_15	30:24	0x0	Bypass value for the clock recovery Phase Counter output, bit [15]. Selected by asserting RX_CRCTRL_BPASS
TX_CLK_RESET_EN_HIGH_B	31	0x0	Control of reset going to high clock pad 0=Clock pad sees tx_reset 1=Clock pad has the tx_reset blocked

HT3PHY_CNTL_12 - RW - 32 bits - HTIUNBIND:0x4B			
Field Name	**Bits**	**Default**	**Description**
RX_CRCTRL_CTLH	6:0	0x0	Bypass value for the clock recovery Phase Counter output., high ctl. Selected by asserting RX_CRCTRL_BPASS
CORE_TX_VCO_MODE	7	0x0	This signal controls the VCO range. When it is 0 VCO can operate between 2.5G - 5.2G
CORE_TX_TMDS_MODE	8	0x0	Controls the divider ratio between refclk to HTPLL and incoherent clock. It needs to be 0 since the inchoerent clock is not used.
CORE_TX_FREQ_LOCK_EN	9	0x0	HTPLL frequency lock detect enable 0=Don't force frequency lock detect 1=Force frequency lock detect
CORE_TX_PLL_FREQ_LOCK (R)	10	0x0	HTPLL locked state signal (read only) 0=Unlocked 1=Llocked
RSVD17	31:11	0x0	Bit [11] for gating phyclk during LS2 0=Not gated 1=Gated Bits [14:12] for RX_BIAS_SEL control, default = 000. Note: The rest of the bits reserved

HT3PHY_CNTL_13 - RW - 32 bits - HTIUNBIND:0x4C			
Field Name	**Bits**	**Default**	**Description**
PRBS_CLEAR	17:0	0x0	Clears the error bit of the PRBS checker inside HTPHY RX 0=Don't clear (for individual lines) 1=Clear (for individual lines)
PRBS_EN	18	0x0	Controls the PRBS generator inside HTPHY TX 0=Don't enable the PRBS generator 1=Enable the PRBS generator
RX2TX_LOOPBACK_CNTRL	20:19	0x0	Enables internal loopback between HTPHY RX and HTPHY TX. The control maps as follows: 00=No loopback 01=No loopback 10=Rx sampler data 11=DLL output
RSVD18	31:21	0x0	Bits [1:0]=MgnBw - Counter of the time margining circuit plateau: 00=16 clocks 01=8 clocks 10=4 clocks 11=2 clocks Bits [10:2]=Reserved for future use

HT3PHY_CNTL_14 - RW - 32 bits - HTIUNBIND:0x4D			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERROR (R)	17:0	0x0	Stores the error bit of the PRBS checker inside HTPHY RX 0=No errors occured (for individual lines) 1=Errors happened (for individual lines)
RSVD19	31:18	0x0	Reserved for future use

2.16 Clock Miscellaneous Indirect Registers

clk_la_shift_reg_stage0 - RW - 32 bits - CLKMISCIND:0x0			
Field Name	**Bits**	**Default**	**Description**
la_shift_reg_stage0_mask	15:0	0x0	
la_shift_reg_stage0_trigger	31:16	0x0	

clk_la_shift_reg_stage1 - RW - 32 bits - CLKMISCIND:0x1			
Field Name	**Bits**	**Default**	**Description**
la_shift_reg_stage1_mask	15:0	0x0	
la_shift_reg_stage1_trigger	31:16	0x0	

clk_la_shift_reg_stage2 - RW - 32 bits - CLKMISCIND:0x2			
Field Name	**Bits**	**Default**	**Description**
la_shift_reg_stage2_mask	15:0	0x0	
la_shift_reg_stage2_trigger	31:16	0x0	

clk_la_shift_reg_stage3 - RW - 32 bits - CLKMISCIND:0x3			
Field Name	**Bits**	**Default**	**Description**
la_shift_reg_stage3_mask	15:0	0x0	
la_shift_reg_stage3_trigger	31:16	0x0	

clk_la_shift_reg_stage4 - RW - 32 bits - CLKMISCIND:0x4			
Field Name	**Bits**	**Default**	**Description**
la_shift_reg_stage4_mask	15:0	0x0	
la_shift_reg_stage4_trigger	31:16	0x0	

clk_la_shift_reg_stage5 - RW - 32 bits - CLKMISCIND:0x5			
Field Name	**Bits**	**Default**	**Description**
la_shift_reg_stage5_mask	15:0	0x0	
la_shift_reg_stage5_trigger	31:16	0x0	

clk_la_shift_reg_stage6 - RW - 32 bits - CLKMISCIND:0x6			
Field Name	**Bits**	**Default**	**Description**
la_shift_reg_stage6_mask	15:0	0x0	
la_shift_reg_stage6_trigger	31:16	0x0	

clk_la_shift_reg_stage7 - RW - 32 bits - CLKMISCIND:0x7			
Field Name	**Bits**	**Default**	**Description**
la_shift_reg_stage7_mask	15:0	0x0	
la_shift_reg_stage7_trigger	31:16	0x0	

clk_la_config - RW - 32 bits - CLKMISCIND:0x8			
Field Name	**Bits**	**Default**	**Description**
la_config_no_cycles_capture	13:0	0x0	
spare_14_15	15:14	0x0	
la_config_byte_sel	16	0x0	
la_config_bit_mode_sel	17	0x0	
la_config_enable	18	0x0	
spare_19_31	31:19	0x0	

clk_la_status - R - 32 bits - CLKMISCIND:0x9			
Field Name	**Bits**	**Default**	**Description**
la_status_trigger_address	13:0	0x0	
spare_14_15	15:14	0x0	
la_status_done	16	0x0	
la_status_triggered	17	0x0	
spare_31_18	31:18	0x0	

Appendix A
Cross-Referenced Index

A.1 Quick Cross-Referenced Index

"All Registers Sorted By Name" on page A-2

"All Registers Sorted By Address" on page A-34

For users of the PDF version of this document: in the tables below, click on the *name* of a register to go to the description of that register found in *Chapter 2*.

A.2 All Registers Sorted By Name

Table 2-1 All Registers Sorted by Name

Name	Address	Secondary Address	Additional Address	Page
ADAPTER_ID	AudioPcie:0x2C	GpuF0Pcie:0x2C	GpuF1Pcie:0x2C	2-83
ADAPTER_ID_W	AudioPcie:0x4C	GpuF0Pcie:0x4C	GpuF1Pcie:0x4C	2-83
APC_ADAPTER_ID_W	apcconfig:0x4C			2-62
APC_AGP_PCI_IOBASE_LIMIT	apcconfig:0x1C			2-60
APC_AGP_PCI_MEMORY_LIMIT_BASE	apcconfig:0x20			2-60
APC_AGP_PCI_PREFETCHABLE_BASE_Upper	apcconfig:0x28			2-61
APC_AGP_PCI_PREFETCHABLE_LIMIT_BASE	apcconfig:0x24			2-61
APC_AGP_PCI_PREFETCHABLE_LIMIT_Upper	apcconfig:0x2C			2-61
APC_AGP_PCI_STATUS	apcconfig:0x1E			2-60
APC_BASE_CODE	apcconfig:0xB			2-58
APC_BIST	apcconfig:0xF			2-59
APC_CACHE_LINE	apcconfig:0xC			2-58
APC_CAPABILITIES_PTR	apcconfig:0x34			2-61
APC_COMMAND	apcconfig:0x4			2-56
APC_DEVICE_ID	apcconfig:0x2			2-56
APC_HEADER	apcconfig:0xE			2-59
APC_HT_MSI_CAP	apcconfig:0x44			2-62
APC_LATENCY	apcconfig:0xD			2-59
APC_MISC_DEVICE_CTRL	apcconfig:0x40			2-62
APC_REGPROG_INF	apcconfig:0x9			2-58
APC_REVISION_ID	apcconfig:0x8			2-58
APC_SSID	apcconfig:0xB4			2-63
APC_SSID_CAP_ID	apcconfig:0xB0			2-63
APC_STATUS	apcconfig:0x6			2-57
APC_SUB_BUS_NUMBER_LATENCY	apcconfig:0x18			2-59
APC_SUB_CLASS	apcconfig:0xA			2-58
APC_VENDOR_ID	apcconfig:0x0			2-56
ATTR00	VGAATTRIND:0x0			2-116
ATTR01	VGAATTRIND:0x1			2-116
ATTR02	VGAATTRIND:0x2			2-117
ATTR03	VGAATTRIND:0x3			2-117
ATTR04	VGAATTRIND:0x4			2-117
ATTR05	VGAATTRIND:0x5			2-117
ATTR06	VGAATTRIND:0x6			2-117
ATTR07	VGAATTRIND:0x7			2-118
ATTR08	VGAATTRIND:0x8			2-118
ATTR09	VGAATTRIND:0x9			2-118
ATTR0A	VGAATTRIND:0xA			2-118
ATTR0B	VGAATTRIND:0xB			2-118
ATTR0C	VGAATTRIND:0xC			2-119
ATTR0D	VGAATTRIND:0xD			2-119

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
ATTR0E	VGAATTRIND:0xE			2-119
ATTR0F	VGAATTRIND:0xF			2-119
ATTR10	VGAATTRIND:0x10			2-120
ATTR11	VGAATTRIND:0x11			2-120
ATTR12	VGAATTRIND:0x12			2-120
ATTR13	VGAATTRIND:0x13			2-121
ATTR14	VGAATTRIND:0x14			2-121
ATTRDR	GpuF0MMReg:0x3C1	VGA_IO:0x3C1		2-116
ATTRDW	GpuF0MMReg:0x3C0	VGA_IO:0x3C0		2-116
ATTRX	GpuF0MMReg:0x3C0	VGA_IO:0x3C0		2-116
BASE_ADDR_1	AudioPcie:0x10	GpuF0Pcie:0x10	GpuF1Pcie:0x10	2-81
BASE_ADDR_2	AudioPcie:0x14	GpuF0Pcie:0x14	GpuF1Pcie:0x14	2-81
BASE_ADDR_3	AudioPcie:0x18	GpuF0Pcie:0x18	GpuF1Pcie:0x18	2-81
BASE_ADDR_4	AudioPcie:0x1C	GpuF0Pcie:0x1C	GpuF1Pcie:0x1C	2-81
BASE_ADDR_5	AudioPcie:0x20	GpuF0Pcie:0x20	GpuF1Pcie:0x20	2-82
BASE_ADDR_6	AudioPcie:0x24	GpuF0Pcie:0x24	GpuF1Pcie:0x24	2-82
BASE_CLASS	AudioPcie:0xB	GpuF0Pcie:0xB	GpuF1Pcie:0xB	2-80
BIST	AudioPcie:0xF	GpuF0Pcie:0xF	GpuF1Pcie:0xF	2-81
CACHE_LINE	AudioPcie:0xC	GpuF0Pcie:0xC	GpuF1Pcie:0xC	2-80
CAP_PTR	AudioPcie:0x34	GpuF0Pcie:0x34	GpuF1Pcie:0x34	2-82
CFG_CT_CLKGATE_HTIU	clkconfig:0xF8			2-76
CG_MISC_INPUT_1	clkconfig:0x78			2-68
CG_MISC_INPUT_2	clkconfig:0x7C			2-68
CG_MISC_INPUT_3	clkconfig:0x90			2-69
CLK_CFG_HTPLL_CNTL	clkconfig:0xD4			2-74
clk_la_config	CLKMISCIND:0x8			2-407
clk_la_shift_reg_stage0	CLKMISCIND:0x0			2-406
clk_la_shift_reg_stage1	CLKMISCIND:0x1			2-406
clk_la_shift_reg_stage2	CLKMISCIND:0x2			2-406
clk_la_shift_reg_stage3	CLKMISCIND:0x3			2-406
clk_la_shift_reg_stage4	CLKMISCIND:0x4			2-406
clk_la_shift_reg_stage5	CLKMISCIND:0x5			2-406
clk_la_shift_reg_stage6	CLKMISCIND:0x6			2-407
clk_la_shift_reg_stage7	CLKMISCIND:0x7			2-407
clk_la_status	CLKMISCIND:0x9			2-407
CLK_MISC_DATA	clkconfig:0xF4			2-76
CLK_MISC_INDEX	clkconfig:0xF0			2-76
clk_top_pwm1_ctrl	clkconfig:0xB0			2-75
clk_top_pwm2_ctrl	clkconfig:0xB4			2-75
clk_top_pwm3_ctrl	clkconfig:0xCC			2-72
clk_top_pwm4_ctrl	clkconfig:0x4C			2-73
clk_top_pwm5_ctrl	clkconfig:0x50			2-73
clk_top_pwm6_ctrl	clkconfig:0x54			2-73
CLK_TOP_PWM7_CNTL	clkconfig:0x48			2-73
CLK_TOP_SPARE_A	clkconfig:0xE0			2-74

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
CLK_TOP_SPARE_B	clkconfig:0xE4			2-75
CLK_TOP_SPARE_C	clkconfig:0xE8			2-75
CLK_TOP_SPARE_D	clkconfig:0xEC			2-75
clk_top_spare_pll	clkconfig:0xD0			2-74
clk_top_test_ctrl	clkconfig:0xB8			2-76
CLK_TOP_THERMAL_ALERT_INTR_EN	clkconfig:0xC0			2-72
CLK_TOP_THERMAL_ALERT_STATUS	clkconfig:0xC4			2-72
CLK_TOP_THERMAL_ALERT_WAIT_WINDOW	clkconfig:0xC8			2-72
CLKGATE_DISABLE	clkconfig:0x94			2-70
CLKGATE_DISABLE2	clkconfig:0x8C			2-69
CLMC_BWESTM_BwRange1	HTIUNBIND:0x65			2-399
CLMC_BWESTM_BwRange2	HTIUNBIND:0x66			2-399
CLMC_BWESTM_BwRange3	HTIUNBIND:0x67			2-399
CLMC_BWESTM_ClientBw1	HTIUNBIND:0x5C			2-397
CLMC_BWESTM_ClientBw2	HTIUNBIND:0x5D			2-397
CLMC_BWESTM_ClientBw3	HTIUNBIND:0x5E			2-397
CLMC_BWESTM_ClientBw4	HTIUNBIND:0x5F			2-398
CLMC_BWESTM_ClientBw5	HTIUNBIND:0x60			2-398
CLMC_BWESTM_ClientBw6	HTIUNBIND:0x61			2-398
CLMC_BWESTM_ClientBw7	HTIUNBIND:0x62			2-398
CLMC_BWESTM_ClientBw8	HTIUNBIND:0x63			2-398
CLMC_BWESTM_ClientBw9	HTIUNBIND:0x64			2-398
CLMC_BWESTM_I	HTIUNBIND:0x5B			2-397
CLMC_BWESTM_Timer1	HTIUNBIND:0x68			2-399
CLMC_BWESTM_Timer2	HTIUNBIND:0x69			2-399
CLMC_BWESTM_Timer3	HTIUNBIND:0x6A			2-399
CLMC_CONTROL_I	HTIUNBIND:0x52			2-395
CLMC_CONTROL_II	HTIUNBIND:0x53			2-395
CLMC_CONTROL_III	HTIUNBIND:0x54			2-396
CLMC_CONTROL_IV	HTIUNBIND:0x6B			2-400
CLMC_CONTROL_V	HTIUNBIND:0x6C			2-400
CLMC_CONTROL_VI	HTIUNBIND:0x6D			2-400
CLMC_I	HTIUNBIND:0x50			2-395
CLMC_LMM_St1	HTIUNBIND:0x55			2-396
CLMC_LMM_St2	HTIUNBIND:0x56			2-396
CLMC_LMM_St3	HTIUNBIND:0x57			2-396
CLMC_LMM_St4	HTIUNBIND:0x58			2-396
CLMC_LMM_St5	HTIUNBIND:0x59			2-396
CLMC_LMM_St6	HTIUNBIND:0x5A			2-397
CLMC_ReadBack	HTIUNBIND:0x51			2-395
COMMAND	AudioPcie:0x4	GpuF0Pcie:0x4	GpuF1Pcie:0x4	2-78
CPLL_CONTROL	clkconfig:0x44			2-65
CPLL_CONTROL2	clkconfig:0x98			2-71
CPLL_CONTROL3	clkconfig:0x70			2-67

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
CPU_DRAM_BASE_SYSTEM_ADDRESS	NBMCIND:0x4C			2-251
CPU_DRAM_CNTL_SELECT_HI	NBMCIND:0x4B			2-251
CPU_DRAM_CNTL_SELECT_LO	NBMCIND:0x4A			2-251
CPU_DRAM_HOLE_ADDRESS	NBMCIND:0x4D			2-251
CPU_DRAM_LIMIT_SYSTEM_ADDRESS	NBMCIND:0x4E			2-251
CPU_DRAM0_BANK_ADDR_MAPPING	NBMCIND:0x3C			2-246
CPU_DRAM0_CS0_BASE	NBMCIND:0x30			2-243
CPU_DRAM0_CS01_MASK	NBMCIND:0x38			2-245
CPU_DRAM0_CS1_BASE	NBMCIND:0x31			2-243
CPU_DRAM0_CS2_BASE	NBMCIND:0x32			2-244
CPU_DRAM0_CS23_MASK	NBMCIND:0x39			2-245
CPU_DRAM0_CS3_BASE	NBMCIND:0x33			2-244
CPU_DRAM0_CS4_BASE	NBMCIND:0x34			2-244
CPU_DRAM0_CS45_MASK	NBMCIND:0x3A			2-245
CPU_DRAM0_CS5_BASE	NBMCIND:0x35			2-244
CPU_DRAM0_CS6_BASE	NBMCIND:0x36			2-244
CPU_DRAM0_CS67_MASK	NBMCIND:0x3B			2-245
CPU_DRAM0_CS7_BASE	NBMCIND:0x37			2-244
CPU_DRAM1_BANK_ADDR_MAPPING	NBMCIND:0x49			2-249
CPU_DRAM1_CS0_BASE	NBMCIND:0x3D			2-247
CPU_DRAM1_CS01_MASK	NBMCIND:0x45			2-249
CPU_DRAM1_CS1_BASE	NBMCIND:0x3E			2-247
CPU_DRAM1_CS2_BASE	NBMCIND:0x3F			2-247
CPU_DRAM1_CS23_MASK	NBMCIND:0x46			2-249
CPU_DRAM1_CS3_BASE	NBMCIND:0x40			2-248
CPU_DRAM1_CS4_BASE	NBMCIND:0x41			2-248
CPU_DRAM1_CS45_MASK	NBMCIND:0x47			2-249
CPU_DRAM1_CS5_BASE	NBMCIND:0x42			2-248
CPU_DRAM1_CS6_BASE	NBMCIND:0x43			2-248
CPU_DRAM1_CS67_MASK	NBMCIND:0x48			2-249
CPU_DRAM1_CS7_BASE	NBMCIND:0x44			2-248
CRT00	VGACRTIND:0x0			2-107
CRT01	VGACRTIND:0x1			2-107
CRT02	VGACRTIND:0x2			2-107
CRT03	VGACRTIND:0x3			2-107
CRT04	VGACRTIND:0x4			2-107
CRT05	VGACRTIND:0x5			2-108
CRT06	VGACRTIND:0x6			2-108
CRT07	VGACRTIND:0x7			2-108
CRT08	VGACRTIND:0x8			2-109
CRT09	VGACRTIND:0x9			2-109
CRT0A	VGACRTIND:0xA			2-109
CRT0B	VGACRTIND:0xB			2-110

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
CRT0C	VGACRTIND:0xC			2-110
CRT0D	VGACRTIND:0xD			2-110
CRT0E	VGACRTIND:0xE			2-110
CRT0F	VGACRTIND:0xF			2-111
CRT10	VGACRTIND:0x10			2-111
CRT11	VGACRTIND:0x11			2-111
CRT12	VGACRTIND:0x12			2-111
CRT13	VGACRTIND:0x13			2-112
CRT14	VGACRTIND:0x14			2-112
CRT15	VGACRTIND:0x15			2-112
CRT16	VGACRTIND:0x16			2-112
CRT17	VGACRTIND:0x17			2-113
CRT18	VGACRTIND:0x18			2-113
CRT1E	VGACRTIND:0x1E			2-113
CRT1F	VGACRTIND:0x1F			2-113
CRT22	VGACRTIND:0x22			2-113
CRTC8_DATA	GpuF0MMReg:0x3B5	GpuF0MMReg:0x3D5	VGA_IO:0x3B5 VGA_IO:0x3D5	2-106
CRTC8_IDX	GpuF0MMReg:0x3B4	GpuF0MMReg:0x3D4	VGA_IO:0x3B4 VGA_IO:0x3D4	2-106
CT_DISABLE_BIU	clkconfig:0x68			2-66
D1_MVP_AFR_FLIP_FIFO_CNTL	GpuF0MMReg:0x6518			2-154
D1_MVP_AFR_FLIP_MODE	GpuF0MMReg:0x6514			2-154
D1_MVP_FLIP_LINE_NUM_INSERT	GpuF0MMReg:0x651C			2-154
D1COLOR_MATRIX_COEF_1_1	GpuF0MMReg:0x6384			2-145
D1COLOR_MATRIX_COEF_1_2	GpuF0MMReg:0x6388			2-145
D1COLOR_MATRIX_COEF_1_3	GpuF0MMReg:0x638C			2-145
D1COLOR_MATRIX_COEF_1_4	GpuF0MMReg:0x6390			2-145
D1COLOR_MATRIX_COEF_2_1	GpuF0MMReg:0x6394			2-146
D1COLOR_MATRIX_COEF_2_2	GpuF0MMReg:0x6398			2-146
D1COLOR_MATRIX_COEF_2_3	GpuF0MMReg:0x639C			2-146
D1COLOR_MATRIX_COEF_2_4	GpuF0MMReg:0x63A0			2-146
D1COLOR_MATRIX_COEF_3_1	GpuF0MMReg:0x63A4			2-146
D1COLOR_MATRIX_COEF_3_2	GpuF0MMReg:0x63A8			2-147
D1COLOR_MATRIX_COEF_3_3	GpuF0MMReg:0x63AC			2-147
D1COLOR_MATRIX_COEF_3_4	GpuF0MMReg:0x63B0			2-147
D1COLOR_SPACE_CONVERT	GpuF0MMReg:0x613C			2-147
D1CRTC_MVP_BLACK_KEYER	GpuF0MMReg:0x6058			2-157
D1CRTC_MVP_CONTROL1	GpuF0MMReg:0x6038			2-154
D1CRTC_MVP_CONTROL2	GpuF0MMReg:0x603C			2-155
D1CRTC_MVP_CONTROL3	GpuF0MMReg:0x6850			2-159
D1CRTC_MVP_CRC_CNTL	GpuF0MMReg:0x6840			2-158
D1CRTC_MVP_CRC_RESULT	GpuF0MMReg:0x6844			2-158
D1CRTC_MVP_CRC2_CNTL	GpuF0MMReg:0x6848			2-158
D1CRTC_MVP_CRC2_RESULT	GpuF0MMReg:0x684C			2-159
D1CRTC_MVP_FIFO_CONTROL	GpuF0MMReg:0x6040			2-156

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
D1CRTC_MVP_FIFO_STATUS	GpuF0MMReg:0x6044			2-156
D1CRTC_MVP_INBAND_CNTL_CAP	GpuF0MMReg:0x604C			2-156
D1CRTC_MVP_INBAND_CNTL_INSERT	GpuF0MMReg:0x6050			2-157
D1CRTC_MVP_INBAND_CNTL_INSERT_TIMER	GpuF0MMReg:0x6054			2-157
D1CRTC_MVP_RECEIVE_CNT_CNTL1	GpuF0MMReg:0x6854			2-159
D1CRTC_MVP_RECEIVE_CNT_CNTL2	GpuF0MMReg:0x6858			2-159
D1CRTC_MVP_SLAVE_STATUS	GpuF0MMReg:0x6048			2-156
D1CRTC_MVP_STATUS	GpuF0MMReg:0x605C			2-157
D1CUR_COLOR1	GpuF0MMReg:0x641C			2-150
D1CUR_COLOR2	GpuF0MMReg:0x6420			2-151
D1CUR_CONTROL	GpuF0MMReg:0x6400			2-149
D1CUR_HOT_SPOT	GpuF0MMReg:0x6418			2-150
D1CUR_POSITION	GpuF0MMReg:0x6414			2-150
D1CUR_SIZE	GpuF0MMReg:0x6410			2-150
D1CUR_SURFACE_ADDRESS	GpuF0MMReg:0x6408			2-150
D1CUR_UPDATE	GpuF0MMReg:0x6424			2-151
D1GRPH_ALPHA	GpuF0MMReg:0x6304			2-140
D1GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL	GpuF0MMReg:0x6380			2-145
D1GRPH_CONTROL	GpuF0MMReg:0x6104			2-122
D1GRPH_DFQ_CONTROL	GpuF0MMReg:0x6150			2-144
D1GRPH_DFQ_STATUS	GpuF0MMReg:0x6154			2-144
D1GRPH_ENABLE	GpuF0MMReg:0x6100			2-122
D1GRPH_FLIP_CONTROL	GpuF0MMReg:0x6148			2-128
D1GRPH_INTERRUPT_CONTROL	GpuF0MMReg:0x615C			2-144
D1GRPH_INTERRUPT_STATUS	GpuF0MMReg:0x6158			2-144
D1GRPH_KEY_RANGE_ALPHA	GpuF0MMReg:0x631C			2-142
D1GRPH_KEY_RANGE_BLUE	GpuF0MMReg:0x6318			2-142
D1GRPH_KEY_RANGE_GREEN	GpuF0MMReg:0x6314			2-141
D1GRPH_KEY_RANGE_RED	GpuF0MMReg:0x6310			2-141
D1GRPH_LUT_SEL	GpuF0MMReg:0x6108			2-124
D1GRPH_PITCH	GpuF0MMReg:0x6120			2-125
D1GRPH_PRIMARY_SURFACE_ADDRESS	GpuF0MMReg:0x6110			2-125
D1GRPH_SECONDARY_SURFACE_ADDRESS	GpuF0MMReg:0x6118			2-125
D1GRPH_SURFACE_ADDRESS_INUSE	GpuF0MMReg:0x614C			2-128
D1GRPH_SURFACE_OFFSET_X	GpuF0MMReg:0x6124			2-125
D1GRPH_SURFACE_OFFSET_Y	GpuF0MMReg:0x6128			2-126
D1GRPH_SWAP_CNTL	GpuF0MMReg:0x610C			2-124
D1GRPH_UPDATE	GpuF0MMReg:0x6144			2-127

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
D1GRPH_X_END	GpuF0MMReg:0x6134			2-126
D1GRPH_X_START	GpuF0MMReg:0x612C			2-126
D1GRPH_Y_END	GpuF0MMReg:0x6138			2-126
D1GRPH_Y_START	GpuF0MMReg:0x6130			2-126
D1ICON_COLOR1	GpuF0MMReg:0x6458			2-153
D1ICON_COLOR2	GpuF0MMReg:0x645C			2-153
D1ICON_CONTROL	GpuF0MMReg:0x6440			2-152
D1ICON_SIZE	GpuF0MMReg:0x6450			2-152
D1ICON_START_POSITION	GpuF0MMReg:0x6454			2-152
D1ICON_SURFACE_ADDRESS	GpuF0MMReg:0x6448			2-152
D1ICON_UPDATE	GpuF0MMReg:0x6460			2-153
D1OVL_ALPHA	GpuF0MMReg:0x6308			2-140
D1OVL_ALPHA_CONTROL	GpuF0MMReg:0x630C			2-141
D1OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	GpuF0MMReg:0x6140			2-143
D1OVL_CONTROL1	GpuF0MMReg:0x6184			2-129
D1OVL_CONTROL2	GpuF0MMReg:0x6188			2-130
D1OVL_DFQ_CONTROL	GpuF0MMReg:0x61B4			2-133
D1OVL_DFQ_STATUS	GpuF0MMReg:0x61B8			2-133
D1OVL_ENABLE	GpuF0MMReg:0x6180			2-128
D1OVL_END	GpuF0MMReg:0x61A8			2-131
D1OVL_KEY_ALPHA	GpuF0MMReg:0x632C			2-143
D1OVL_KEY_CONTROL	GpuF0MMReg:0x6300			2-140
D1OVL_KEY_RANGE_BLUE_CB	GpuF0MMReg:0x6328			2-143
D1OVL_KEY_RANGE_GREEN_Y	GpuF0MMReg:0x6324			2-142
D1OVL_KEY_RANGE_RED_CR	GpuF0MMReg:0x6320			2-142
D1OVL_MATRIX_COEF_1_1	GpuF0MMReg:0x6204			2-133
D1OVL_MATRIX_COEF_1_2	GpuF0MMReg:0x6208			2-134
D1OVL_MATRIX_COEF_1_3	GpuF0MMReg:0x620C			2-134
D1OVL_MATRIX_COEF_1_4	GpuF0MMReg:0x6210			2-134
D1OVL_MATRIX_COEF_2_1	GpuF0MMReg:0x6214			2-134
D1OVL_MATRIX_COEF_2_2	GpuF0MMReg:0x6218			2-134
D1OVL_MATRIX_COEF_2_3	GpuF0MMReg:0x621C			2-135
D1OVL_MATRIX_COEF_2_4	GpuF0MMReg:0x6220			2-135
D1OVL_MATRIX_COEF_3_1	GpuF0MMReg:0x6224			2-135
D1OVL_MATRIX_COEF_3_2	GpuF0MMReg:0x6228			2-135
D1OVL_MATRIX_COEF_3_3	GpuF0MMReg:0x622C			2-135
D1OVL_MATRIX_COEF_3_4	GpuF0MMReg:0x6230			2-136
D1OVL_MATRIX_TRANSFORM_EN	GpuF0MMReg:0x6200			2-133
D1OVL_PITCH	GpuF0MMReg:0x6198			2-131
D1OVL_PWL_0TOF	GpuF0MMReg:0x6284			2-136
D1OVL_PWL_100TO13F	GpuF0MMReg:0x629C			2-137
D1OVL_PWL_10TO1F	GpuF0MMReg:0x6288			2-136
D1OVL_PWL_140TO17F	GpuF0MMReg:0x62A0			2-137
D1OVL_PWL_180TO1BF	GpuF0MMReg:0x62A4			2-138
D1OVL_PWL_1C0TO1FF	GpuF0MMReg:0x62A8			2-138

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
D1OVL_PWL_200TO23F	GpuF0MMReg:0x62AC			2-138
D1OVL_PWL_20TO3F	GpuF0MMReg:0x628C			2-136
D1OVL_PWL_240TO27F	GpuF0MMReg:0x62B0			2-138
D1OVL_PWL_280TO2BF	GpuF0MMReg:0x62B4			2-138
D1OVL_PWL_2C0TO2FF	GpuF0MMReg:0x62B8			2-139
D1OVL_PWL_300TO33F	GpuF0MMReg:0x62BC			2-139
D1OVL_PWL_340TO37F	GpuF0MMReg:0x62C0			2-139
D1OVL_PWL_380TO3BF	GpuF0MMReg:0x62C4			2-139
D1OVL_PWL_3C0TO3FF	GpuF0MMReg:0x62C8			2-139
D1OVL_PWL_40TO7F	GpuF0MMReg:0x6290			2-137
D1OVL_PWL_80TOBF	GpuF0MMReg:0x6294			2-137
D1OVL_PWL_C0TOFF	GpuF0MMReg:0x6298			2-137
D1OVL_PWL_TRANSFORM_EN	GpuF0MMReg:0x6280			2-136
D1OVL_RT_BAND_POSITION	GpuF0MMReg:0x6508			2-148
D1OVL_RT_PROCEED_COND	GpuF0MMReg:0x650C			2-148
D1OVL_RT_SKEWCOMMAND	GpuF0MMReg:0x6500			2-148
D1OVL_RT_SKEWCONTROL	GpuF0MMReg:0x6504			2-148
D1OVL_RT_STAT	GpuF0MMReg:0x6510			2-149
D1OVL_START	GpuF0MMReg:0x61A4			2-131
D1OVL_SURFACE_ADDRESS	GpuF0MMReg:0x6190			2-130
D1OVL_SURFACE_ADDRESS_INUSE	GpuF0MMReg:0x61B0			2-132
D1OVL_SURFACE_OFFSET_X	GpuF0MMReg:0x619C			2-131
D1OVL_SURFACE_OFFSET_Y	GpuF0MMReg:0x61A0			2-131
D1OVL_SWAP_CNTL	GpuF0MMReg:0x618C			2-130
D1OVL_UPDATE	GpuF0MMReg:0x61AC			2-132
D2_MVP_AFR_FLIP_FIFO_CNTL	GpuF0MMReg:0x65EC			2-192
D2_MVP_AFR_FLIP_MODE	GpuF0MMReg:0x65E8			2-192
D2_MVP_FLIP_LINE_NUM_INSERT	GpuF0MMReg:0x65F0			2-192
D2COLOR_MATRIX_COEF_1_1	GpuF0MMReg:0x6B84			2-182
D2COLOR_MATRIX_COEF_1_2	GpuF0MMReg:0x6B88			2-182
D2COLOR_MATRIX_COEF_1_3	GpuF0MMReg:0x6B8C			2-182
D2COLOR_MATRIX_COEF_1_4	GpuF0MMReg:0x6B90			2-183
D2COLOR_MATRIX_COEF_2_1	GpuF0MMReg:0x6B94			2-183
D2COLOR_MATRIX_COEF_2_2	GpuF0MMReg:0x6B98			2-183
D2COLOR_MATRIX_COEF_2_3	GpuF0MMReg:0x6B9C			2-183
D2COLOR_MATRIX_COEF_2_4	GpuF0MMReg:0x6BA0			2-184
D2COLOR_MATRIX_COEF_3_1	GpuF0MMReg:0x6BA4			2-184
D2COLOR_MATRIX_COEF_3_2	GpuF0MMReg:0x6BA8			2-184
D2COLOR_MATRIX_COEF_3_3	GpuF0MMReg:0x6BAC			2-184
D2COLOR_MATRIX_COEF_3_4	GpuF0MMReg:0x6BB0			2-185
D2COLOR_SPACE_CONVERT	GpuF0MMReg:0x693C			2-185
D2CRTC_MVP_INBAND_CNTL_INSERT	GpuF0MMReg:0x6838			2-158
D2CRTC_MVP_INBAND_CNTL_INSERT_TIMER	GpuF0MMReg:0x683C			2-158

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
D2CUR_COLOR1	GpuF0MMReg:0x6C1C			2-188
D2CUR_COLOR2	GpuF0MMReg:0x6C20			2-189
D2CUR_CONTROL	GpuF0MMReg:0x6C00			2-187
D2CUR_HOT_SPOT	GpuF0MMReg:0x6C18			2-188
D2CUR_POSITION	GpuF0MMReg:0x6C14			2-188
D2CUR_SIZE	GpuF0MMReg:0x6C10			2-188
D2CUR_SURFACE_ADDRESS	GpuF0MMReg:0x6C08			2-188
D2CUR_UPDATE	GpuF0MMReg:0x6C24			2-189
D2GRPH_ALPHA	GpuF0MMReg:0x6B04			2-179
D2GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL	GpuF0MMReg:0x6B80			2-182
D2GRPH_CONTROL	GpuF0MMReg:0x6904			2-160
D2GRPH_ENABLE	GpuF0MMReg:0x6900			2-160
D2GRPH_FLIP_CONTROL	GpuF0MMReg:0x6948			2-166
D2GRPH_KEY_RANGE_ALPHA	GpuF0MMReg:0x6B1C			2-180
D2GRPH_KEY_RANGE_BLUE	GpuF0MMReg:0x6B18			2-180
D2GRPH_KEY_RANGE_GREEN	GpuF0MMReg:0x6B14			2-180
D2GRPH_KEY_RANGE_RED	GpuF0MMReg:0x6B10			2-180
D2GRPH_LUT_SEL	GpuF0MMReg:0x6908			2-162
D2GRPH_PITCH	GpuF0MMReg:0x6920			2-163
D2GRPH_PRIMARY_SURFACE_ADDRESS	GpuF0MMReg:0x6910			2-163
D2GRPH_SECONDARY_SURFACE_ADDRESS	GpuF0MMReg:0x6918			2-163
D2GRPH_SURFACE_ADDRESS_INUSE	GpuF0MMReg:0x694C			2-166
D2GRPH_SURFACE_OFFSET_X	GpuF0MMReg:0x6924			2-163
D2GRPH_SURFACE_OFFSET_Y	GpuF0MMReg:0x6928			2-163
D2GRPH_SWAP_CNTL	GpuF0MMReg:0x690C			2-162
D2GRPH_UPDATE	GpuF0MMReg:0x6944			2-165
D2GRPH_X_END	GpuF0MMReg:0x6934			2-164
D2GRPH_X_START	GpuF0MMReg:0x692C			2-164
D2GRPH_Y_END	GpuF0MMReg:0x6938			2-164
D2GRPH_Y_START	GpuF0MMReg:0x6930			2-164
D2ICON_COLOR1	GpuF0MMReg:0x6C58			2-191
D2ICON_COLOR2	GpuF0MMReg:0x6C5C			2-191
D2ICON_CONTROL	GpuF0MMReg:0x6C40			2-190
D2ICON_SIZE	GpuF0MMReg:0x6C50			2-190
D2ICON_START_POSITION	GpuF0MMReg:0x6C54			2-190
D2ICON_SURFACE_ADDRESS	GpuF0MMReg:0x6C48			2-190
D2ICON_UPDATE	GpuF0MMReg:0x6C60			2-191
D2OVL_ALPHA	GpuF0MMReg:0x6B08			2-179
D2OVL_ALPHA_CONTROL	GpuF0MMReg:0x6B0C			2-179
D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	GpuF0MMReg:0x6940			2-174
D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	GpuF0MMReg:0x6940			2-182
D2OVL_CONTROL1	GpuF0MMReg\:0x6984			2-167

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
D2OVL_CONTROL2	GpuF0MMReg\:0x6988			2-168
D2OVL_DFQ_CONTROL	GpuF0MMReg\:0x69B4			2-171
D2OVL_DFQ_STATUS	GpuF0MMReg\:0x69B8			2-171
D2OVL_ENABLE	GpuF0MMReg\:0x6980			2-167
D2OVL_END	GpuF0MMReg\:0x69A8			2-169
D2OVL_KEY_ALPHA	GpuF0MMReg:0x6B2C			2-181
D2OVL_KEY_CONTROL	GpuF0MMReg:0x6B00			2-178
D2OVL_KEY_RANGE_BLUE_CB	GpuF0MMReg:0x6B28			2-181
D2OVL_KEY_RANGE_GREEN_Y	GpuF0MMReg:0x6B24			2-181
D2OVL_KEY_RANGE_RED_CR	GpuF0MMReg:0x6B20			2-181
D2OVL_MATRIX_COEF_1_1	GpuF0MMReg:0x6A04			2-171
D2OVL_MATRIX_COEF_1_2	GpuF0MMReg:0x6A08			2-172
D2OVL_MATRIX_COEF_1_3	GpuF0MMReg:0x6A0C			2-172
D2OVL_MATRIX_COEF_1_4	GpuF0MMReg:0x6A10			2-172
D2OVL_MATRIX_COEF_2_1	GpuF0MMReg:0x6A14			2-172
D2OVL_MATRIX_COEF_2_2	GpuF0MMReg:0x6A18			2-172
D2OVL_MATRIX_COEF_2_3	GpuF0MMReg:0x6A1C			2-173
D2OVL_MATRIX_COEF_2_4	GpuF0MMReg:0x6A20			2-173
D2OVL_MATRIX_COEF_3_1	GpuF0MMReg:0x6A24			2-173
D2OVL_MATRIX_COEF_3_2	GpuF0MMReg:0x6A28			2-173
D2OVL_MATRIX_COEF_3_3	GpuF0MMReg:0x6A2C			2-173
D2OVL_MATRIX_COEF_3_4	GpuF0MMReg:0x6A30			2-174
D2OVL_MATRIX_TRANSFORM_EN	GpuF0MMReg:0x6A00			2-171
D2OVL_PITCH	GpuF0MMReg\:0x6998			2-169
D2OVL_PWL_0TOF	GpuF0MMReg:0x6A84			2-174
D2OVL_PWL_100TO13F	GpuF0MMReg:0x6A9C			2-175
D2OVL_PWL_10TO1F	GpuF0MMReg:0x6A88			2-174
D2OVL_PWL_140TO17F	GpuF0MMReg:0x6AA0			2-176
D2OVL_PWL_180TO1BF	GpuF0MMReg:0x6AA4			2-176
D2OVL_PWL_1C0TO1FF	GpuF0MMReg:0x6AA8			2-176
D2OVL_PWL_200TO23F	GpuF0MMReg:0x6AAC			2-176
D2OVL_PWL_20TO3F	GpuF0MMReg:0x6A8C			2-175
D2OVL_PWL_240TO27F	GpuF0MMReg:0x6AB0			2-176
D2OVL_PWL_280TO2BF	GpuF0MMReg:0x6AB4			2-177
D2OVL_PWL_2C0TO2FF	GpuF0MMReg:0x6AB8			2-177
D2OVL_PWL_300TO33F	GpuF0MMReg:0x6ABC			2-177
D2OVL_PWL_340TO37F	GpuF0MMReg:0x6AC0			2-177
D2OVL_PWL_380TO3BF	GpuF0MMReg:0x6AC4			2-177
D2OVL_PWL_3C0TO3FF	GpuF0MMReg:0x6AC8			2-178
D2OVL_PWL_40TO7F	GpuF0MMReg:0x6A90			2-175
D2OVL_PWL_80TOBF	GpuF0MMReg:0x6A94			2-175
D2OVL_PWL_C0TOFF	GpuF0MMReg:0x6A98			2-175
D2OVL_PWL_TRANSFORM_EN	GpuF0MMReg:0x6A80			2-174
D2OVL_RT_BAND_POSITION	GpuF0MMReg:0x6D08			2-186
D2OVL_RT_PROCEED_COND	GpuF0MMReg:0x6D0C			2-186

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
D2OVL_RT_SKEWCOMMAND	GpuF0MMReg:0x6D00			2-185
D2OVL_RT_SKEWCONTROL	GpuF0MMReg:0x6D04			2-186
D2OVL_RT_STAT	GpuF0MMReg:0x6D10			2-186
D2OVL_START	GpuF0MMReg\:0x69A4			2-169
D2OVL_SURFACE_ADDRESS	GpuF0MMReg\:0x6990			2-168
D2OVL_SURFACE_ADDRESS_INUSE	GpuF0MMReg\:0x69B0			2-170
D2OVL_SURFACE_OFFSET_X	GpuF0MMReg\:0x699C			2-169
D2OVL_SURFACE_OFFSET_Y	GpuF0MMReg\:0x69A0			2-169
D2OVL_SWAP_CNTL	GpuF0MMReg\:0x698C			2-168
D2OVL_UPDATE	GpuF0MMReg\:0x69AC			2-170
DAC_CONTROL	GpuF0MMReg:0x7058	GpuF0MMReg:0x7158		2-103
DAC_DATA	GpuF0MMReg:0x3C9	VGA_IO:0x3C9		2-103
DAC_MASK	GpuF0MMReg:0x3C6	VGA_IO:0x3C6		2-104
DAC_R_INDEX	GpuF0MMReg:0x3C7	VGA_IO:0x3C7		2-104
DAC_W_INDEX	GpuF0MMReg:0x3C8	VGA_IO:0x3C8		2-104
DC_LUT_30_COLOR	GpuF0MMReg:0x6494			2-194
DC_LUT_AUTOFILL	GpuF0MMReg:0x64A0			2-195
DC_LUT_PWL_DATA	GpuF0MMReg:0x6490			2-194
DC_LUT_READ_PIPE_SELECT	GpuF0MMReg:0x6498			2-194
DC_LUT_RW_INDEX	GpuF0MMReg:0x6488			2-193
DC_LUT_RW_MODE	GpuF0MMReg:0x6484			2-193
DC_LUT_RW_SELECT	GpuF0MMReg:0x6480			2-193
DC_LUT_SEQ_COLOR	GpuF0MMReg:0x648C			2-193
DC_LUT_WRITE_EN_MASK	GpuF0MMReg:0x649C			2-194
DC_LUTA_BLACK_OFFSET_BLUE	GpuF0MMReg:0x64C4			2-197
DC_LUTA_BLACK_OFFSET_GREEN	GpuF0MMReg:0x64C8			2-197
DC_LUTA_BLACK_OFFSET_RED	GpuF0MMReg:0x64CC			2-197
DC_LUTA_CONTROL	GpuF0MMReg:0x64C0			2-195
DC_LUTA_WHITE_OFFSET_BLUE	GpuF0MMReg:0x64D0			2-197
DC_LUTA_WHITE_OFFSET_GREEN	GpuF0MMReg:0x64D4			2-197
DC_LUTA_WHITE_OFFSET_RED	GpuF0MMReg:0x64D8			2-197
DC_LUTB_BLACK_OFFSET_BLUE	GpuF0MMReg:0x6CC4			2-199
DC_LUTB_BLACK_OFFSET_GREEN	GpuF0MMReg:0x6CC8			2-199
DC_LUTB_BLACK_OFFSET_RED	GpuF0MMReg:0x6CCC			2-200
DC_LUTB_CONTROL	GpuF0MMReg:0x6CC0			2-198
DC_LUTB_WHITE_OFFSET_BLUE	GpuF0MMReg:0x6CD0			2-200
DC_LUTB_WHITE_OFFSET_GREEN	GpuF0MMReg:0x6CD4			2-200
DC_LUTB_WHITE_OFFSET_RED	GpuF0MMReg:0x6CD8			2-200

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
DC_MVP_LB_CONTROL	GpuF0MMReg:0x65F4			2-205
DCP_CRC_CONTROL	GpuF0MMReg:0x6C80			2-200
DCP_CRC_MASK	GpuF0MMReg:0x6C84			2-201
DCP_CRC_P0_CURRENT	GpuF0MMReg:0x6C88			2-201
DCP_CRC_P0_LAST	GpuF0MMReg:0x6C90			2-201
DCP_CRC_P1_CURRENT	GpuF0MMReg:0x6C8C			2-201
DCP_CRC_P1_LAST	GpuF0MMReg:0x6C94			2-201
DCP_LB_DATA_GAP_BETWEEN_CHUNK	GpuF0MMReg:0x6CBC			2-202
DCP_MULTI_CHIP_CNTL	GpuF0MMReg:0x6CA4			2-203
DCP_TILING_CONFIG	GpuF0MMReg:0x6CA0			2-202
DELAY_SET_IOC_CCLK	clkconfig:0x5C			2-65
DEVICE_CAP	AudioPcie:0x5C	GpuF0Pcie:0x5C	GpuF1Pcie:0x5C	2-85
DEVICE_CAP2	AudioPcie:0x7C	GpuF0Pcie:0x7C	GpuF1Pcie:0x7C	2-89
DEVICE_CNTL	AudioPcie:0x60	GpuF0Pcie:0x60	GpuF1Pcie:0x60	2-86
DEVICE_CNTL2	AudioPcie:0x80	GpuF0Pcie:0x80	GpuF1Pcie:0x80	2-89
DEVICE_ID	AudioPcie:0x2	GpuF0Pcie:0x2	GpuF1Pcie:0x2	2-78
DEVICE_STATUS	AudioPcie:0x62	GpuF0Pcie:0x62	GpuF1Pcie:0x62	2-87
DEVICE_STATUS2	AudioPcie:0x82	GpuF0Pcie:0x82	GpuF1Pcie:0x82	2-90
DFT_CNTL0	NBMISCIND:0x5			2-301
DFT_CNTL1	NBMISCIND:0x6			2-301
DFT_CNTL2	NBMISCIND:0x10			2-304
DFT_CNTL3	NBMISCIND:0x7B			2-323
DFT_CNTL4	NBMISCIND:0x1D			2-324
DFT_VIP_IO_GPIO	NBMISCIND:0x44			2-315
DFT_VIP_IO_GPIO_OR	NBMISCIND:0x45			2-315
DMIF_CONTROL	GpuF0MMReg:0x6CB0			2-204
DMIF_STATUS	GpuF0MMReg:0x6CB4			2-204
GC_CLK_CNTRL	clkconfig:0x74			2-67
GENENB	GpuF0MMReg:0x3C3	VGA_IO:0x3C3		2-102
GENFC_RD	GpuF0MMReg:0x3CA	VGA_IO:0x3CA		2-101
GENFC_WT	GpuF0MMReg:0x3BA	GpuF0MMReg:0x3DA	VGA_IO:0x3BA VGA_IO:0x3DA	2-101
GENMO_RD	GpuF0MMReg:0x3CC	VGA_IO:0x3CC		2-102
GENMO_WT	GpuF0MMReg:0x3C2	VGA_IO:0x3C2		2-101
GENS0	GpuF0MMReg:0x3C2	VGA_IO:0x3C2		2-102
GENS1	GpuF0MMReg:0x3BA	GpuF0MMReg:0x3DA	VGA_IO:0x3BA VGA_IO:0x3DA	2-103
GPIO_ctrl	clkconfig:0xDC			2-73
GPIO_PAD	NBMISCIND:0x40			2-313
GPIO_PAD_CNTL_PU_PD	NBMISCIND:0x41			2-314
GPIO_PAD_SCHMEM_OE	NBMISCIND:0x42			2-314
GPIO_PAD_SP_SN	NBMISCIND:0x43			2-315
GPIO_SDVO_HPD	NBMISCIND:0x4A			2-325
GRA00	VGAGRPHIND:0x0			2-114
GRA01	VGAGRPHIND:0x1			2-114

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
GRA02	VGAGRPHIND:0x2			2-114
GRA03	VGAGRPHIND:0x3			2-114
GRA04	VGAGRPHIND:0x4			2-115
GRA05	VGAGRPHIND:0x5			2-115
GRA06	VGAGRPHIND:0x6			2-115
GRA07	VGAGRPHIND:0x7			2-115
GRA08	VGAGRPHIND:0x8			2-115
GRPH8_DATA	GpuF0MMReg:0x3CF	VGA_IO:0x3CF		2-114
GRPH8_IDX	GpuF0MMReg:0x3CE	VGA_IO:0x3CE		2-114
HEADER	AudioPcie:0xE	GpuF0Pcie:0xE	GpuF1Pcie:0xE	2-81
HT_ARB_I	NBMCIND:0x2B			2-242
HT_ARB_II	NBMCIND:0x2C			2-243
HT_BIST_Extended_Control_0	HTIUNBIND:0x21			2-385
HT_BIST_Extended_Control_1	HTIUNBIND:0x22			2-385
HT_CLMC_I	NBMCIND:0x29			2-242
HT_CLMC_II	NBMCIND:0x2A			2-242
HT_FORCE_I	NBMCIND:0x2D			2-243
HT_FORCE_II	NBMCIND:0x2E			2-243
HT_FORCE_III	NBMCIND:0x2F			2-243
HT3PHY_CNTL_1	HTIUNBIND:0x26			2-389
HT3PHY_CNTL_10	HTIUNBIND:0x49			2-404
HT3PHY_CNTL_11	HTIUNBIND:0x4A			2-404
HT3PHY_CNTL_12	HTIUNBIND:0x4B			2-405
HT3PHY_CNTL_13	HTIUNBIND:0x4C			2-405
HT3PHY_CNTL_14	HTIUNBIND:0x4D			2-405
HT3PHY_CNTL_2	HTIUNBIND:0x27			2-389
HT3PHY_CNTL_3	HTIUNBIND:0x28			2-390
HT3PHY_CNTL_4	HTIUNBIND:0x29			2-390
HT3PHY_CNTL_5	HTIUNBIND:0x2A			2-391
HT3PHY_CNTL_6	HTIUNBIND:0x2B			2-391
HT3PHY_CNTL_7	HTIUNBIND:0x2C			2-391
HT3PHY_CNTL_8	HTIUNBIND:0x47			2-403
HT3PHY_CNTL_9	HTIUNBIND:0x48			2-403
HTIU_DEBUG	HTIUNBIND:0x5			2-375
HTIU_DOWNSTREAM_CONFIG	HTIUNBIND:0x6			2-375
HTIU_UPSTREAM_CONFIG_0	HTIUNBIND:0x7			2-376
HTIU_UPSTREAM_CONFIG_1	HTIUNBIND:0x8			2-377
HTIU_UPSTREAM_CONFIG_10	HTIUNBIND:0x11			2-379
HTIU_UPSTREAM_CONFIG_11	HTIUNBIND:0x12			2-379
HTIU_UPSTREAM_CONFIG_12	HTIUNBIND:0x13			2-379
HTIU_UPSTREAM_CONFIG_13	HTIUNBIND:0x77			2-379
HTIU_UPSTREAM_CONFIG_19	HTIUNBIND:0x14			2-380
HTIU_UPSTREAM_CONFIG_2	HTIUNBIND:0x9			2-377
HTIU_UPSTREAM_CONFIG_3	HTIUNBIND:0xA			2-377
HTIU_UPSTREAM_CONFIG_4	HTIUNBIND:0xB			2-378
HTIU_UPSTREAM_CONFIG_5	HTIUNBIND:0xC			2-378

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
HTIU_UPSTREAM_CONFIG_6	HTIUNBIND:0xD			2-378
HTIU_UPSTREAM_CONFIG_7	HTIUNBIND:0xE			2-378
HTIU_UPSTREAM_CONFIG_8	HTIUNBIND:0xF			2-378
HTIU_UPSTREAM_CONFIG_9	HTIUNBIND:0x10			2-379
ILA_CLK_DATA	clkconfig:0xA0			2-77
ILA_CLK_INDEX	clkconfig:0x9C			2-77
INTERRUPT_LINE	AudioPcie:0x3C	GpuF0Pcie:0x3C	GpuF1Pcie:0x3C	2-82
INTERRUPT_PIN	AudioPcie:0x3D	GpuF0Pcie:0x3D	GpuF1Pcie:0x3D	2-82
IOC_DMA_ARBITER	NBMISCIND:0x9			2-303
IOC_JTAG_CNTL	NBMISCIND:0x47			2-324
IOC_LAT_PERF_CNTR_CNTL	NBMISCIND:0x30			2-306
IOC_LAT_PERF_CNTR_OUT	NBMISCIND:0x31			2-306
IOC_P2P_CNTL	NBMISCIND:0xC			2-304
IOC_PCIE_CNTL	NBMISCIND:0xB			2-303
IOC_PCIE_CSR_Count	NBMISCIND:0xA			2-303
IOC_PCIE_D10_CNTL	NBMISCIND:0x5F			2-27
IOC_PCIE_D10_CNTL	NBMISCIND:0x5F			2-319
IOC_PCIE_D10_CSR_Count	NBMISCIND:0x5E			2-27
IOC_PCIE_D10_CSR_Count	NBMISCIND:0x5E			2-319
IOC_PCIE_D11_CNTL	NBMISCIND:0x61			2-27
IOC_PCIE_D11_CNTL	NBMISCIND:0x61			2-319
IOC_PCIE_D11_CSR_Count	NBMISCIND:0x60			2-27
IOC_PCIE_D11_CSR_Count	NBMISCIND:0x60			2-319
IOC_PCIE_D12_CNTL	NBMISCIND:0x63			2-28
IOC_PCIE_D12_CNTL	NBMISCIND:0x63			2-320
IOC_PCIE_D12_CSR_Count	NBMISCIND:0x62			2-28
IOC_PCIE_D12_CSR_Count	NBMISCIND:0x62			2-320
IOC_PCIE_D2_CNTL	NBMISCIND:0x51			2-23
IOC_PCIE_D2_CNTL	NBMISCIND:0x51			2-315
IOC_PCIE_D2_CSR_Count	NBMISCIND:0x50			2-23
IOC_PCIE_D2_CSR_Count	NBMISCIND:0x50			2-315
IOC_PCIE_D3_CNTL	NBMISCIND:0x53			2-24
IOC_PCIE_D3_CNTL	NBMISCIND:0x53			2-316
IOC_PCIE_D3_CSR_Count	NBMISCIND:0x52			2-24
IOC_PCIE_D3_CSR_Count	NBMISCIND:0x52			2-316
IOC_PCIE_D4_CNTL	NBMISCIND:0x55			2-24
IOC_PCIE_D4_CNTL	NBMISCIND:0x55			2-316
IOC_PCIE_D4_CSR_Count	NBMISCIND:0x54			2-24
IOC_PCIE_D4_CSR_Count	NBMISCIND:0x54			2-316
IOC_PCIE_D5_CNTL	NBMISCIND:0x57			2-25
IOC_PCIE_D5_CNTL	NBMISCIND:0x57			2-317
IOC_PCIE_D5_CSR_Count	NBMISCIND:0x56			2-25
IOC_PCIE_D5_CSR_Count	NBMISCIND:0x56			2-317
IOC_PCIE_D6_CNTL	NBMISCIND:0x59			2-25
IOC_PCIE_D6_CNTL	NBMISCIND:0x59			2-317

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
IOC_PCIE_D6_CSR_Count	NBMISCIND:0x58			2-25
IOC_PCIE_D6_CSR_Count	NBMISCIND:0x58			2-317
IOC_PCIE_D7_CNTL	NBMISCIND:0x5B			2-26
IOC_PCIE_D7_CNTL	NBMISCIND:0x5B			2-318
IOC_PCIE_D7_CSR_Count	NBMISCIND:0x5A			2-26
IOC_PCIE_D7_CSR_Count	NBMISCIND:0x5A			2-318
IOC_PCIE_D9_CNTL	NBMISCIND:0x5D			2-26
IOC_PCIE_D9_CNTL	NBMISCIND:0x5D			2-318
IOC_PCIE_D9_CSR_Count	NBMISCIND:0x5C			2-26
IOC_PCIE_D9_CSR_Count	NBMISCIND:0x5C			2-318
IOCIsocMapAddr_HI	NBMISCIND:0xF			2-304
IOCIsocMapAddr_LO	NBMISCIND:0xE			2-304
K8_FB_LOCATION	NBMCIND:0x11			2-231
LATENCY	AudioPcie:0xD	GpuF0Pcie:0xD	GpuF1Pcie:0xD	2-80
LINK_CAP	AudioPcie:0x64	GpuF0Pcie:0x64	GpuF1Pcie:0x64	2-87
LINK_CAP2	AudioPcie:0x84	GpuF0Pcie:0x84	GpuF1Pcie:0x84	2-90
LINK_CNTL	AudioPcie:0x68	GpuF0Pcie:0x68	GpuF1Pcie:0x68	2-88
LINK_CNTL2	AudioPcie:0x88	GpuF0Pcie:0x88	GpuF1Pcie:0x88	2-90
Link_State_Control_0	HTIUNBIND:0x15			2-381
Link_State_Control_1	HTIUNBIND:0x16			2-382
Link_State_Control_2	HTIUNBIND:0x17			2-382
Link_State_Control_3	HTIUNBIND:0x18			2-382
Link_State_Control_4	HTIUNBIND:0x19			2-382
Link_State_Control_5	HTIUNBIND:0x1A			2-383
Link_State_Control_6	HTIUNBIND:0x1B			2-383
Link_State_Control_7	HTIUNBIND:0x1C			2-383
LINK_STATUS	AudioPcie:0x6A	GpuF0Pcie:0x6A	GpuF1Pcie:0x6A	2-89
LINK_STATUS2	AudioPcie:0x8A	GpuF0Pcie:0x8A	GpuF1Pcie:0x8A	2-90
LMM1	HTIUNBIND:0x70			2-400
LMM2	HTIUNBIND:0x71			2-401
LMM3	HTIUNBIND:0x72			2-401
LMM4	HTIUNBIND:0x73			2-401
LMM5	HTIUNBIND:0x74			2-402
LMM6	HTIUNBIND:0x75			2-402
LMM7	HTIUNBIND:0x76			2-402
LS_History0	HTIUNBIND:0x40			2-393
LS_History1	HTIUNBIND:0x41			2-393
LS_History2	HTIUNBIND:0x42			2-394
LS_History3	HTIUNBIND:0x43			2-394
LS_History4	HTIUNBIND:0x44			2-394
LS_History5	HTIUNBIND:0x45			2-394
LVTMA_BL_MOD_CNTL	GpuF0MMReg:0x7F94			2-219
LVTMA_DATA_SYNCHRONIZATION	GpuF0MMReg:0x7F98			2-218
LVTMA_LOAD_DETECT	GpuF0MMReg:0x7F08			2-220
LVTMA_MACRO_CONTROL	GpuF0MMReg:0x7F0C			2-221

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
LVTMA_PREEMPHASIS_CONTROL	GpuF0MMReg:0x7F1C			2-222
LVTMA_PWRSEQ_CNTL	GpuF0MMReg:0x7F80			2-218
LVTMA_PWRSEQ_DELAY1	GpuF0MMReg:0x7F8C			2-218
LVTMA_PWRSEQ_DELAY2	GpuF0MMReg:0x7F90			2-218
LVTMA_PWRSEQ_REF_DIV	GpuF0MMReg:0x7F88			2-218
LVTMA_PWRSEQ_STATE	GpuF0MMReg:0x7F84			2-219
LVTMA_REG_TEST_OUTPUT	GpuF0MMReg:0x7F10			2-222
LVTMA_TRANSMITTER_ADJUST	GpuF0MMReg:0x7F18			2-222
LVTMA_TRANSMITTER_CONTROL	GpuF0MMReg:0x7F00			2-221
LVTMA_TRANSMITTER_DEBUG	GpuF0MMReg:0x7F14			2-222
LVTMA_TRANSMITTER_ENABLE	GpuF0MMReg:0x7F04			2-220
MAX_LATENCY	AudioPcie:0x3F	GpuF0Pcie:0x3F	GpuF1Pcie:0x3F	2-83
MC_ACMD_DLL_CNTRL_A	clkconfig:0x88			2-68
MC_ACMD_DLL_CNTRL_B	clkconfig:0x89			2-69
MC_BIST_CNTL0	NBMCIND:0x5C			2-252
MC_BIST_CNTL1	NBMCIND:0x5D			2-252
MC_BIST_MISMATCH_H	NBMCIND:0x5F			2-253
MC_BIST_MISMATCH_L	NBMCIND:0x5E			2-253
MC_BIST_PATTERN0H	NBMCIND:0x61			2-253
MC_BIST_PATTERN0L	NBMCIND:0x60			2-253
MC_BIST_PATTERN1H	NBMCIND:0x63			2-254
MC_BIST_PATTERN1L	NBMCIND:0x62			2-254
MC_BIST_PATTERN2H	NBMCIND:0x65			2-254
MC_BIST_PATTERN2L	NBMCIND:0x64			2-254
MC_BIST_PATTERN3H	NBMCIND:0x67			2-254
MC_BIST_PATTERN3L	NBMCIND:0x66			2-254
MC_BIST_PATTERN4H	NBMCIND:0x69			2-255
MC_BIST_PATTERN4L	NBMCIND:0x68			2-254
MC_BIST_PATTERN5H	NBMCIND:0x6B			2-255
MC_BIST_PATTERN5L	NBMCIND:0x6A			2-255
MC_BIST_PATTERN6H	NBMCIND:0x6D			2-255
MC_BIST_PATTERN6L	NBMCIND:0x6C			2-255
MC_BIST_PATTERN7H	NBMCIND:0x6F			2-255
MC_BIST_PATTERN7L	NBMCIND:0x6E			2-255
MC_CLK_CNTRL	clkconfig:0x58			2-65
MC_CLK_DATA	clkconfig:0x64			2-66
MC_CLK_INDEX	clkconfig:0x60			2-66
MC_CREDITS_CONTROL	NBMCIND:0x15			2-237
MC_DATA_DLL_CNTRL_A	clkconfig:0x80			2-68
MC_DEBUG	NBMCIND:0x4F			2-251
MC_FB_LOCATION	NBMCIND:0x10			2-231
MC_GENERAL_PURPOSE	NBMCIND:0x1			2-224
MC_GENERAL_PURPOSE_2	NBMCIND:0x2			2-225
MC_GENERAL_PURPOSE_3	NBMCIND:0x3			2-225

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
MC_HTIU_GFX_RD_URGENT_CONTROL	NBMCIND:0x23			2-241
MC_HTIU_GFX_WR_URGENT_CONTROL	NBMCIND:0x24			2-241
MC_HTIU_ISOC_URGENT_CONTROL	NBMCIND:0x25			2-241
MC_IMP_CTRL_CNTL	NBMCIND:0x4			2-226
MC_IMP_CTRL_REF	NBMCIND:0x5			2-226
MC_ISOC_ARB_CNTL	NBMCIND:0x17			2-238
MC_ISOC_ARB_CNTL2	NBMCIND:0x18			2-238
MC_ISOC_BW_LIM_CNTL	NBMCIND:0x1B			2-239
MC_ISOC_BW_LIM_MAX	NBMCIND:0x1A			2-238
MC_ISOC_BW_LIM_WINDOW	NBMCIND:0x19			2-238
MC_ISOC_CONTROL	NBMCIND:0x16			2-237
MC_LATENCY_COUNT_CNTL	NBMCIND:0x1C			2-239
MC_MCLK_CONTROL	NBMCIND:0xC			2-230
MC_MISC_UMA_CNTL	NBMCIND:0x12			2-232
MC_MPLL_CONTROL	NBMCIND:0x6			2-227
MC_MPLL_CONTROL2	NBMCIND:0x7			2-227
MC_MPLL_CONTROL3	NBMCIND:0x8			2-228
MC_MPLL_DIV_CONTROL	NBMCIND:0xB			2-229
MC_MPLL_FREQ_CONTROL	NBMCIND:0x9			2-228
MC_MPLL_SEQ_CONTROL	NBMCIND:0xA			2-229
MC_SYSTEM_STATUS	NBMCIND:0x0			2-223
MC_UMA_ADDRESS_SWIZZLE_0	NBMCIND:0x13			2-232
MC_UMA_ADDRESS_SWIZZLE_1	NBMCIND:0x14			2-235
MCA_DLL_MASTER_0	NBMCIND:0xD8			2-296
MCA_DLL_MASTER_1	NBMCIND:0xD9			2-296
MCA_DLL_SLAVE_RD_0	NBMCIND:0xE0			2-297
MCA_DLL_SLAVE_RD_1	NBMCIND:0xE1			2-297
MCA_DLL_SLAVE_WR_0	NBMCIND:0xE8			2-297
MCA_DLL_SLAVE_WR_1	NBMCIND:0xE9			2-297
MCA_DQ_DQS_READ_BACK	NBMCIND:0xC6			2-284
MCA_DQS_CLK_READ_BACK	NBMCIND:0xC7			2-284
MCA_DRIVING	NBMCIND:0xB4			2-271
MCA_GENERAL_PURPOSE	NBMCIND:0xC3			2-281
MCA_GENERAL_PURPOSE_2	NBMCIND:0xC4			2-282
MCA_IN_TIMING_DQS_3210	NBMCIND:0xB2			2-270
MCA_IN_TIMING_DQS_3210_PM	NBMCIND:0xD0			2-293
MCA_MEMORY_INIT_EMRS	NBMCIND:0xA1			2-256
MCA_MEMORY_INIT_EMRS_PM	NBMCIND:0xC9			2-286
MCA_MEMORY_INIT_EMRS2	NBMCIND:0xA2			2-257
MCA_MEMORY_INIT_EMRS2_PM	NBMCIND:0xCA			2-287
MCA_MEMORY_INIT_EMRS3	NBMCIND:0xA3			2-258
MCA_MEMORY_INIT_EMRS3_PM	NBMCIND:0xCB			2-288
MCA_MEMORY_INIT_MRS	NBMCIND:0xA0			2-256

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
MCA_MEMORY_INIT_MRS_PM	NBMCIND:0xC8			2-285
MCA_MEMORY_INIT_SEQUENCE_1	NBMCIND:0xA4			2-259
MCA_MEMORY_INIT_SEQUENCE_2	NBMCIND:0xA5			2-260
MCA_MEMORY_INIT_SEQUENCE_3	NBMCIND:0xA6			2-261
MCA_MEMORY_INIT_SEQUENCE_4	NBMCIND:0xA7			2-262
MCA_MEMORY_TYPE	NBMCIND:0xAC			2-267
MCA_MX1X2X_DQ	NBMCIND:0xD6			2-295
MCA_MX1X2X_DQS	NBMCIND:0xD7			2-295
MCA_OCD_CONTROL	NBMCIND:0xC5			2-284
MCA_OUT_TIMING	NBMCIND:0xB5			2-273
MCA_OUT_TIMING_DQ	NBMCIND:0xB6			2-275
MCA_OUT_TIMING_DQ_PM	NBMCIND:0xD2			2-294
MCA_OUT_TIMING_DQS	NBMCIND:0xB7			2-275
MCA_OUT_TIMING_DQS_PM	NBMCIND:0xD3			2-294
MCA_PREBUF_SLEW_N	NBMCIND:0xC1			2-280
MCA_PREBUF_SLEW_P	NBMCIND:0xC2			2-281
MCA_RECEIVING	NBMCIND:0xB1			2-269
MCA_RESERVED_0	NBMCIND:0xF0			2-298
MCA_RESERVED_1	NBMCIND:0xF1			2-298
MCA_RESERVED_2	NBMCIND:0xF2			2-298
MCA_RESERVED_3	NBMCIND:0xF3			2-298
MCA_RESERVED_4	NBMCIND:0xF4			2-298
MCA_RESERVED_5	NBMCIND:0xF5			2-298
MCA_RESERVED_6	NBMCIND:0xF6			2-298
MCA_RESERVED_7	NBMCIND:0xF7			2-299
MCA_SEQ_CONTROL	NBMCIND:0xB0			2-267
MCA_STRENGTH_N	NBMCIND:0xB8			2-276
MCA_STRENGTH_P	NBMCIND:0xB9			2-276
MCA_STRENGTH_READ_BACK_N	NBMCIND:0xBB			2-279
MCA_STRENGTH_READ_BACK_P	NBMCIND:0xBC			2-279
MCA_STRENGTH_STEP	NBMCIND:0xBA			2-277
MCA_TIMING_PARAMETERS_1	NBMCIND:0xA8			2-263
MCA_TIMING_PARAMETERS_1_PM	NBMCIND:0xCC			2-289
MCA_TIMING_PARAMETERS_2	NBMCIND:0xA9			2-264
MCA_TIMING_PARAMETERS_2_PM	NBMCIND:0xCD			2-290
MCA_TIMING_PARAMETERS_3	NBMCIND:0xAA			2-264
MCA_TIMING_PARAMETERS_3_PM	NBMCIND:0xCE			2-290
MCA_TIMING_PARAMETERS_4	NBMCIND:0xAB			2-266

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
MCA_TIMING_PARAMETERS_4_PM	NBMCIND:0xCF			2-292
MCB_LATENCY_COUNT_EVENT_BIF	NBMCIND:0x1E			2-240
MCB_LATENCY_COUNT_EVENT_SP	NBMCIND:0x1D			2-240
MCB_LATENCY_COUNT_EVENT_UMA	NBMCIND:0x1F			2-240
MCD_LATENCY_COUNT_EVENT_BIF	NBMCIND:0x21			2-240
MCD_LATENCY_COUNT_EVENT_SP	NBMCIND:0x20			2-240
MCD_LATENCY_COUNT_EVENT_UMA	NBMCIND:0x22			2-241
MCIF_CONTROL	GpuF0MMReg:0x6CB8			2-205
MIN_GRANT	AudioPcie:0x3E	GpuF0Pcie:0x3E	GpuF1Pcie:0x3E	2-83
MM_CFGREGS_CNTL	GpuF0MMReg:0x544C			2-100
MM_DATA	GpuF0MMReg:0x4	GpuIOReg:0x4		2-100
MM_INDEX	GpuF0MMReg:0x0	GpuIOReg:0x0		2-100
MSI_CAP_LIST	AudioPcie:0xA0	GpuF0Pcie:0xA0	GpuF1Pcie:0xA0	2-91
MSI_MSG_ADDR_HI	AudioPcie:0xA8	GpuF0Pcie:0xA8	GpuF1Pcie:0xA8	2-91
MSI_MSG_ADDR_LO	AudioPcie:0xA4	GpuF0Pcie:0xA4	GpuF1Pcie:0xA4	2-91
MSI_MSG_CNTL	AudioPcie:0xA2	GpuF0Pcie:0xA2	GpuF1Pcie:0xA2	2-91
MSI_MSG_DATA	AudioPcie:0xA8	GpuF0Pcie:0xA8	GpuF1Pcie:0xA8	2-92
MSI_MSG_DATA_64	AudioPcie:0xAC	GpuF0Pcie:0xAC	GpuF1Pcie:0xAC	2-92
NB_ADAPTER_ID	nbconfig:0x2C			2-6
NB_ADAPTER_ID_W	nbconfig:0x50			2-8
NB_APIC_P2P_CNTL	NBMISCIND:0x3D			2-312
NB_APIC_P2P_RANGE_0	NBMISCIND:0x3E			2-313
NB_APIC_P2P_RANGE_1	NBMISCIND:0x3F			2-313
NB_BAR1_RCRB	nbconfig:0x14			2-5
NB_BAR2_PM2	nbconfig:0x18			2-5
NB_BAR3_PCIEXP_MMCFG	nbconfig:0x1C			2-5
NB_BAR3_UPPER_PCIEXP_MMCFG	nbconfig:0x20			2-6
NB_BASE_CODE	nbconfig:0xB			2-3
NB_BIF_SPARE	NBMISCIND:0x1E			2-305
NB_BIST	nbconfig:0xF			2-4
NB_BROADCAST_BASE_HI	NBMISCIND:0x3B			2-312
NB_BROADCAST_BASE_LO	NBMISCIND:0x3A			2-312
NB_BROADCAST_CNTL	NBMISCIND:0x3C			2-312
NB_BUS_NUM_CNTL	NBMISCIND:0x11			2-304
NB_CACHE_LINE	nbconfig:0xC			2-3
NB_CAPABILITIES_PTR	nbconfig:0x34			2-6
NB_CFG_STAT	nbconfig:0x88			2-30
NB_CNTL	NBMISCIND:0x0			2-300
NB_COMMAND	nbconfig:0x4			2-1
NB_DEVICE_ID	nbconfig:0x2			2-1

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
NB_EXSMRAM	nbconfig:0x6A			2-17
NB_FDHC	nbconfig:0x68			2-16
NB_GC_STRAPS	nbconfig:0x8C			2-30
NB_HEADER	nbconfig:0xE			2-4
NB_HT_ARB_I	HTIUNBIND:0x36			2-393
NB_HT_ARB_II	HTIUNBIND:0x37			2-393
NB_HT_CLK_CNTL_RECEIVER_COMP_CNTL	HTIUNBIND:0x0			2-20
NB_HT_CLK_CNTL_RECEIVER_COMP_CNTL	HTIUNBIND:0x0			2-387
NB_HT_CLMC_I	HTIUNBIND:0x34			2-392
NB_HT_CLMC_II	HTIUNBIND:0x35			2-392
NB_HT_ENUMERATION_SCRATCHPAD	nbconfig:0xD8			2-23
NB_HT_ERROR_RETRY_CAPABILITY	nbconfig:0x40			2-8
NB_HT_ERROR_RETRY_CONTROL_STATUS	nbconfig:0x44			2-9
NB_HT_ERROR_RETRY_COUNT	nbconfig:0x48			2-9
NB_HT_LINK_COMMAND	nbconfig:0xC4			2-20
NB_HT_LINK_CONF_CNTL	nbconfig:0xC8			2-21
NB_HT_LINK_END	nbconfig:0xCC			2-22
NB_HT_LINK_FREQ_CAP_A	nbconfig:0xD0			2-22
NB_HT_LINK_FREQ_CAP_B	nbconfig:0xD4			2-22
NB_HT_MEMORY_BASE_UPPER	nbconfig:0xDC			2-23
NB_HT_TRANS_COMP_CNTL	HTIUNBIND:0x1			2-19
NB_HT_TRANS_COMP_CNTL	HTIUNBIND:0x1			2-388
NB_HT3_BIST_CONTROL	nbconfig:0xC0			2-16
NB_HT3_CAPABILITY	nbconfig:0x9C			2-9
NB_HT3_GLOBAL_LINK_TRAIN	nbconfig:0xA0			2-10
NB_HT3_LINK_RECEIVER_CONF_0	nbconfig:0xA8			2-12
NB_HT3_LINK_RECEIVER_CONF_I	nbconfig:0xB8			2-15
NB_HT3_LINK_TRAINING_0	nbconfig:0xAC			2-13
NB_HT3_LINK_TRAINING_1	nbconfig:0xBC			2-15
NB_HT3_LINK_TRANSMITTER_CONF_0	nbconfig:0xA4			2-11
NB_HT3_LINK_TRANSMITTER_CONF_1	nbconfig:0xB4			2-14
NB_HT3_Power_management_Capability	nbconfig:0xF8			2-4
NB_HT3_Power_management_data_port	nbconfig:0xFC			2-4
NB_HT3_RESERVED	nbconfig:0xB0			2-14
NB_HTIU_CFG	HTIUNBIND:0x32			2-389
NB_HTIU_SPARE	HTIUNBIND:0x2D			2-403
NB_INTERRUPT_PIN	NBMISCIND:0x1F			2-306
NB_IOC_CFG_CNTL	nbconfig:0x7C			2-19

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
NB_IOC_DEBUG	NBMISCIND:0x1			2-300
NB_LATENCY	nbconfig:0xD			2-4
NB_LOWER_TOP_OF_DRAM2	HTIUNBIND:0x30			2-388
NB_MC_IND_DATA	nbconfig:0x74			2-32
NB_MC_IND_INDEX	nbconfig:0x70			2-32
NB_MEM_CH_CNTL0	NBMCIND:0xD			2-230
NB_MEM_CH_CNTL1	NBMCIND:0xE			2-231
NB_MEM_CH_CNTL2	NBMCIND:0xF			2-231
NB_MMIOBASE	NBMISCIND:0x17			2-305
NB_MMIOLIMIT	NBMISCIND:0x18			2-305
NB_PCI_ARB	nbconfig:0x84			2-28
NB_PCI_CTRL	nbconfig:0x4C			2-6
NB_PCIE_ADV_ERR_CAP_CNTL	pcieConfigDev[12:2]:0x168			2-54
NB_PCIE_ADV_ERR_RPT_ENH_CAP_LIST	pcieConfigDev[12:2]:0x150			2-52
NB_PCIE_BASE_CLASS	pcieConfigDev[12:2]:0xB			2-35
NB_PCIE_BIST	pcieConfigDev[12:2]:0xF			2-36
NB_PCIE_CACHE_LINE	pcieConfigDev[12:2]:0xC			2-35
NB_PCIE_CAP	pcieConfigDev[12:2]:0x5A			2-40
NB_PCIE_CAP_LIST	pcieConfigDev[12:2]:0x58			2-40
NB_PCIE_CAP_PTR	pcieConfigDev[12:2]:0x34			2-38
NB_PCIE_COMMAND	pcieConfigDev[12:2]:0x4			2-34
NB_PCIE_CORR_ERR_MASK	pcieConfigDev[12:2]:0x164			2-54
NB_PCIE_CORR_ERR_STATUS	pcieConfigDev[12:2]:0x160			2-53
NB_PCIE_DEV_SERIAL_NUM_DW1	pcieConfigDev[12:2]:0x144			2-52
NB_PCIE_DEV_SERIAL_NUM_DW2	pcieConfigDev[12:2]:0x148			2-52
NB_PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST	pcieConfigDev[12:2]:0x140			2-52
NB_PCIE_DEVICE_CAP	pcieConfigDev[12:2]:0x5C			2-40
NB_PCIE_DEVICE_CAP2	pcieConfigDev[12:2]:0x7C			2-45
NB_PCIE_DEVICE_CNTL	pcieConfigDev[12:2]:0x60			2-41
NB_PCIE_DEVICE_CNTL2	pcieConfigDev[12:2]:0x80			2-45
NB_PCIE_DEVICE_ID	pcieConfigDev[12:2]:0x2			2-33
NB_PCIE_DEVICE_STATUS	pcieConfigDev[12:2]:0x62			2-41

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
NB_PCIE_DEVICE_STATUS2	pcieConfigDev[12:2]:0x82			2-45
NB_PCIE_ERR_SRC_ID	pcieConfigDev[12:2]:0x184			2-55
NB_PCIE_HDR_LOG0	pcieConfigDev[12:2]:0x16C			2-54
NB_PCIE_HDR_LOG1	pcieConfigDev[12:2]:0x170			2-54
NB_PCIE_HDR_LOG2	pcieConfigDev[12:2]:0x174			2-54
NB_PCIE_HDR_LOG3	pcieConfigDev[12:2]:0x178			2-55
NB_PCIE_HEADER	pcieConfigDev[12:2]:0xE			2-36
NB_PCIE_INTERRUPT_LINE	pcieConfigDev[12:2]:0x3C			2-39
NB_PCIE_INTERRUPT_PIN	pcieConfigDev[12:2]:0x3D			2-39
NB_PCIE_IO_BASE_LIMIT	pcieConfigDev[12:2]:0x1C			2-36
NB_PCIE_IO_BASE_LIMIT_HI	pcieConfigDev[12:2]:0x30			2-38
NB_PCIE_IRQ_BRIDGE_CNTL	pcieConfigDev[12:2]:0x3E			2-38
NB_PCIE_LATENCY	pcieConfigDev[12:2]:0xD			2-36
NB_PCIE_LINK_CAP	pcieConfigDev[12:2]:0x64			2-42
NB_PCIE_LINK_CAP2	pcieConfigDev[12:2]:0x84			2-45
NB_PCIE_LINK_CNTL	pcieConfigDev[12:2]:0x68			2-42
NB_PCIE_LINK_CNTL2	pcieConfigDev[12:2]:0x88			2-45
NB_PCIE_LINK_STATUS	pcieConfigDev[12:2]:0x6A			2-43
NB_PCIE_LINK_STATUS2	pcieConfigDev[12:2]:0x8A			2-46
NB_PCIE_MEM_BASE_LIMIT	pcieConfigDev[12:2]:0x20			2-37
NB_PCIE_MSI_CAP_LIST	pcieConfigDev[12:2]:0xA0			2-46
NB_PCIE_MSI_MAP_CAP_LIST	pcieConfigDev[12:2]:0xB8			2-48
NB_PCIE_MSI_MSG_ADDR_HI	pcieConfigDev[12:2]:0xA8			2-47
NB_PCIE_MSI_MSG_ADDR_LO	pcieConfigDev[12:2]:0xA4			2-47
NB_PCIE_MSI_MSG_CNTL	pcieConfigDev[12:2]:0xA2			2-47
NB_PCIE_MSI_MSG_DATA	pcieConfigDev[12:2]:0xA8			2-48

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
NB_PCIE_MSI_MSG_DATA_64	pcieConfigDev[12:2]:0xAC			2-47
NB_PCIE_PMI_CAP	pcieConfigDev[12:2]:0x52			2-39
NB_PCIE_PMI_CAP_LIST	pcieConfigDev[12:2]:0x50			2-39
NB_PCIE_PMI_STATUS_CNTL	pcieConfigDev[12:2]:0x54			2-40
NB_PCIE_PORT_VC_CAP_REG1	pcieConfigDev[12:2]:0x114			2-49
NB_PCIE_PORT_VC_CAP_REG2	pcieConfigDev[12:2]:0x118			2-50
NB_PCIE_PORT_VC_CNTL	pcieConfigDev[12:2]:0x11C			2-50
NB_PCIE_PORT_VC_STATUS	pcieConfigDev[12:2]:0x11E			2-50
NB_PCIE_PREF_BASE_LIMIT	pcieConfigDev[12:2]:0x24			2-37
NB_PCIE_PREF_BASE_UPPER	pcieConfigDev[12:2]:0x28			2-38
NB_PCIE_PREF_LIMIT_UPPER	pcieConfigDev[12:2]:0x2C			2-38
NB_PCIE_PROG_INTERFACE	pcieConfigDev[12:2]:0x9			2-35
NB_PCIE_REVISION_ID	pcieConfigDev[12:2]:0x8			2-35
NB_PCIE_ROOT_CAP	pcieConfigDev[12:2]:0x76			2-44
NB_PCIE_ROOT_CNTL	pcieConfigDev[12:2]:0x74			2-44
NB_PCIE_ROOT_ERR_CMD	pcieConfigDev[12:2]:0x17C			2-55
NB_PCIE_ROOT_ERR_STATUS	pcieConfigDev[12:2]:0x180			2-55
NB_PCIE_ROOT_STATUS	pcieConfigDev[12:2]:0x78			2-44
NB_PCIE_SECONDARY_STATUS	pcieConfigDev[12:2]:0x1E			2-37
NB_PCIE_SLOT_CAP	pcieConfigDev[12:2]:0x6C			2-43
NB_PCIE_SLOT_CAP2	pcieConfigDev[12:2]:0x8C			2-46
NB_PCIE_SLOT_CNTL	pcieConfigDev[12:2]:0x70			2-43
NB_PCIE_SLOT_CNTL2	pcieConfigDev[12:2]:0x90			2-46
NB_PCIE_SLOT_STATUS	pcieConfigDev[12:2]:0x72			2-44
NB_PCIE_SLOT_STATUS2	pcieConfigDev[12:2]:0x92			2-46
NB_PCIE_SSID_CAP_LIST	pcieConfigDev[12:2]:0xB0			2-48
NB_PCIE_SSID_ID	pcieConfigDev[12:2]:0xB4			2-48

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
NB_PCIE_STATUS	pcieConfigDev[12:2]:0x6			2-34
NB_PCIE_SUB_BUS_NUMBER_LATENCY	pcieConfigDev[12:2]:0x18			2-36
NB_PCIE_SUB_CLASS	pcieConfigDev[12:2]:0xA			2-35
NB_PCIE_UNCORR_ERR_MASK	pcieConfigDev[12:2]:0x158			2-53
NB_PCIE_UNCORR_ERR_SEVERITY	pcieConfigDev[12:2]:0x15C			2-53
NB_PCIE_UNCORR_ERR_STATUS	pcieConfigDev[12:2]:0x154			2-52
NB_PCIE_VC_ENH_CAP_LIST	pcieConfigDev[12:2]:0x110			2-49
NB_PCIE_VC0_RESOURCE_CAP	pcieConfigDev[12:2]:0x120			2-50
NB_PCIE_VC0_RESOURCE_CNTL	pcieConfigDev[12:2]:0x124			2-50
NB_PCIE_VC0_RESOURCE_STATUS	pcieConfigDev[12:2]:0x12A			2-51
NB_PCIE_VC1_RESOURCE_CAP	pcieConfigDev[12:2]:0x12C			2-51
NB_PCIE_VC1_RESOURCE_CNTL	pcieConfigDev[12:2]:0x130			2-51
NB_PCIE_VC1_RESOURCE_STATUS	pcieConfigDev[12:2]:0x136			2-51
NB_PCIE_VENDOR_ID	pcieConfigDev[12:2]:0x0			2-33
NB_PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST	pcieConfigDev[12:2]:0x100			2-48
NB_PCIE_VENDOR_SPECIFIC_HDR	pcieConfigDev[12:2]:0x104			2-49
NB_PCIE_VENDOR_SPECIFIC1	pcieConfigDev[12:2]:0x108			2-49
NB_PCIE_VENDOR_SPECIFIC2	pcieConfigDev[12:2]:0x10C			2-49
NB_PERF_CNT_CTRL	nbconfig:0xF4			2-31
NB_PMCR	nbconfig:0x6B			2-18
NB_PROG_DEVICE_REMAP_0	NBMISCIND:0x20			2-306
NB_PROG_DEVICE_REMAP_1	NBMISCIND:0x21			2-306
NB_REGPROG_INF	nbconfig:0x9			2-3
NB_REVISION_ID	nbconfig:0x8			2-3
NB_SMRAM	nbconfig:0x69			2-17
NB_SPARE1	NBMISCIND:0x2			2-300
NB_STATUS	nbconfig:0x6			2-2
NB_STRAP_READ_BACK	nbconfig:0x6C			2-18
NB_STRAPS_READBACK_DATA	NBMISCIND:0x4			2-301
NB_STRAPS_READBACK_MUX	NBMISCIND:0x3			2-300
NB_SUB_CLASS	nbconfig:0xA			2-3
NB_TOM_PCI	NBMISCIND:0x16			2-305
NB_TOP_OF_DRAM_SLOT1	nbconfig:0x90			2-31

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
NB_UNITID_CLUMPING_CAPABILITY	nbconfig:0x54			2-8
NB_UNITID_CLUMPING_ENABLE	nbconfig:0x5C			2-8
NB_UNITID_CLUMPING_SUPPORT	nbconfig:0x58			2-8
NB_UPPER_TOP_OF_DRAM2	HTIUNBIND:0x31			2-388
NB_VENDOR_ID	nbconfig:0x0			2-1
NBCLK_IO_CONTROL	clkconfig:0xBC			2-71
OSC_CONTROL	clkconfig:0x40			2-64
PCIE_ADV_ERR_CAP_CNTL	AudioPcie:0x168	GpuF0Pcie:0x168	GpuF1Pcie:0x168	2-97
PCIE_ADV_ERR_RPT_ENH_CAP_LIST	AudioPcie:0x150	GpuF0Pcie:0x150	GpuF1Pcie:0x150	2-96
PCIE_B_P90_CNTL	PCIEIND:0xC3			2-349
PCIE_BUS_CNTL	PCIEIND:0x21			2-331
PCIE_CAC_DEVICE_CORRELATION	AudioPcie:0x194	GpuF0Pcie:0x194	GpuF1Pcie:0x194	2-98
PCIE_CAC_ENH_CAP_LIST	AudioPcie:0x190	GpuF0Pcie:0x190	GpuF1Pcie:0x190	2-98
PCIE_CAP	AudioPcie:0x5A	GpuF0Pcie:0x5A	GpuF1Pcie:0x5A	2-85
PCIE_CAP_LIST	AudioPcie:0x58	GpuF0Pcie:0x58	GpuF1Pcie:0x58	2-84
PCIE_CFG_CNTL	PCIEIND:0x3C			2-335
PCIE_CI_CNTL	PCIEIND:0x20			2-331
PCIE_CI_MST_C_RTR_TIMEOUT_CNTL	PCIEIND:0x16			2-329
PCIE_CI_MST_R_RTR_TIMEOUT_CNTL	PCIEIND:0x15			2-329
PCIE_CI_SLV_R_RTR_TIMEOUT_CNTL	PCIEIND:0x14			2-329
PCIE_CNTL	PCIEIND:0x10			2-327
PCIE_CNTL2	PCIEIND:0x1C			2-330
PCIE_CONFIG_CNTL	PCIEIND:0x11			2-327
PCIE_CORE_ARB	NBMISCIND:0x12			2-305
PCIE_CORR_ERR_MASK	AudioPcie:0x164	GpuF0Pcie:0x164	GpuF1Pcie:0x164	2-97
PCIE_CORR_ERR_STATUS	AudioPcie:0x160	GpuF0Pcie:0x160	GpuF1Pcie:0x160	2-97
PCIE_DEBUG_CNTL	PCIEIND:0x12			2-328
PCIE_DEV_SERIAL_NUM_DW1	AudioPcie:0x144	GpuF0Pcie:0x144	GpuF1Pcie:0x144	2-95
PCIE_DEV_SERIAL_NUM_DW2	AudioPcie:0x148	GpuF0Pcie:0x148	GpuF1Pcie:0x148	2-95
PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST	AudioPcie:0x140	GpuF0Pcie:0x140	GpuF1Pcie:0x140	2-95
PCIE_ERR_CNTL	PCIEIND_P:0x6A			2-362
PCIE_FC_CPL	PCIEIND_P:0x62			2-362
PCIE_FC_NP	PCIEIND_P:0x61			2-361
PCIE_FC_P	PCIEIND_P:0x60			2-361
PCIE_GFX_P2P_ARBITRER_CONTROL	NBMISCIND:0x49			2-324
PCIE_GFX_P2P_CONTROL	NBMISCIND:0x48			2-324
PCIE_HDR_LOG0	AudioPcie:0x16C	GpuF0Pcie:0x16C	GpuF1Pcie:0x16C	2-98
PCIE_HDR_LOG1	AudioPcie:0x170	GpuF0Pcie:0x170	GpuF1Pcie:0x170	2-98
PCIE_HDR_LOG2	AudioPcie:0x174	GpuF0Pcie:0x174	GpuF1Pcie:0x174	2-98

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
PCIE_HDR_LOG3	AudioPcie:0x178	GpuF0Pcie:0x178	GpuF1Pcie:0x178	2-98
PCIE_HW_DEBUG	PCIEIND:0x2			2-326
PCIE_I2C_DEBUG_BUS	PCIEIND:0x39			2-335
PCIE_I2C_REG_ADDR_EXPAND	PCIEIND:0x3A			2-335
PCIE_I2C_REG_DATA	PCIEIND:0x3B			2-335
PCIE_LC_BW_CHANGE_CNTL	PCIEIND_P:0xB2			2-367
PCIE_LC_CDR_CNTL	PCIEIND_P:0xB3			2-372
PCIE_LC_CNTL	PCIEIND_P:0xA0			2-364
PCIE_LC_CNTL2	PCIEIND_P:0xB1			2-365
PCIE_LC_CNTL3	PCIEIND_P:0xB5			2-366
PCIE_LC_LANE_CNTL	PCIEIND_P:0xB4			2-372
PCIE_LC_LINK_WIDTH_CNTL	PCIEIND_P:0xA2			2-369
PCIE_LC_N_FTS_CNTL	PCIEIND_P:0xA3			2-369
PCIE_LC_SPEED_CNTL	PCIEIND_P:0xA4			2-370
PCIE_LC_STATE0	PCIEIND_P:0xA5			2-372
PCIE_LC_STATE1	PCIEIND_P:0xA6			2-372
PCIE_LC_STATE10	PCIEIND:0x26			2-332
PCIE_LC_STATE11	PCIEIND:0x27			2-333
PCIE_LC_STATE2	PCIEIND_P:0xA7			2-372
PCIE_LC_STATE3	PCIEIND_P:0xA8			2-373
PCIE_LC_STATE4	PCIEIND_P:0xA9			2-373
PCIE_LC_STATE5	PCIEIND_P:0xAA			2-373
PCIE_LC_STATE6	PCIEIND:0x22			2-332
PCIE_LC_STATE7	PCIEIND:0x23			2-332
PCIE_LC_STATE8	PCIEIND:0x24			2-332
PCIE_LC_STATE9	PCIEIND:0x25			2-332
PCIE_LC_STATUS1	PCIEIND:0x28			2-333
PCIE_LC_STATUS2	PCIEIND:0x29			2-333
PCIE_LC_TRAINING_CNTL	PCIEIND_P:0xA1			2-367
PCIE_LINK_CFG	NBMISCIND:0x8			2-302
PCIE_NBCFG_REG10	NBMISCIND:0x28			2-309
PCIE_NBCFG_REG11	NBMISCIND:0x29			2-309
PCIE_NBCFG_REG12	NBMISCIND:0x2A			2-310
PCIE_NBCFG_REG13	NBMISCIND:0x2B			2-310
PCIE_NBCFG_REG14	NBMISCIND:0x2C			2-310
PCIE_NBCFG_REG15	NBMISCIND:0x2D			2-311
PCIE_NBCFG_REG16	NBMISCIND:0x2E			2-311
PCIE_NBCFG_REG17	NBMISCIND:0x2F			2-310
PCIE_NBCFG_REG2	NBMISCIND:0x32			2-307
PCIE_NBCFG_REG3	NBMISCIND:0x33			2-307
PCIE_NBCFG_REG4	NBMISCIND:0x34			2-307
PCIE_NBCFG_REG5	NBMISCIND:0x35			2-307
PCIE_NBCFG_REG6	NBMISCIND:0x36			2-307
PCIE_NBCFG_REG7	NBMISCIND:0x37			2-307
PCIE_NBCFG_REG8	NBMISCIND:0x38			2-307

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
PCIE_NBCFG_REG9	NBMISCIND:0x39			2-308
PCIE_NBCFG_REGA	NBMISCIND:0x22			2-308
PCIE_NBCFG_REGB	NBMISCIND:0x23			2-308
PCIE_NBCFG_REGC	NBMISCIND:0x24			2-308
PCIE_NBCFG_REGD	NBMISCIND:0x25			2-308
PCIE_NBCFG_REGE	NBMISCIND:0x26			2-308
PCIE_NBCFG_REGF	NBMISCIND:0x27			2-308
PCIE_P_BUF_STATUS	PCIEIND:0x41			2-337
PCIE_P_CNTL	PCIEIND:0x40			2-336
PCIE_P_DECODE_ERR_CNT_0	PCIEIND:0xF0			2-354
PCIE_P_DECODE_ERR_CNT_1	PCIEIND:0xF1			2-354
PCIE_P_DECODE_ERR_CNT_10	PCIEIND:0xFA			2-355
PCIE_P_DECODE_ERR_CNT_11	PCIEIND:0xFB			2-356
PCIE_P_DECODE_ERR_CNT_12	PCIEIND:0xFC			2-356
PCIE_P_DECODE_ERR_CNT_13	PCIEIND:0xFD			2-356
PCIE_P_DECODE_ERR_CNT_14	PCIEIND:0xFE			2-356
PCIE_P_DECODE_ERR_CNT_15	PCIEIND:0xFF			2-356
PCIE_P_DECODE_ERR_CNT_2	PCIEIND:0xF2			2-354
PCIE_P_DECODE_ERR_CNT_3	PCIEIND:0xF3			2-354
PCIE_P_DECODE_ERR_CNT_4	PCIEIND:0xF4			2-354
PCIE_P_DECODE_ERR_CNT_5	PCIEIND:0xF5			2-355
PCIE_P_DECODE_ERR_CNT_6	PCIEIND:0xF6			2-355
PCIE_P_DECODE_ERR_CNT_7	PCIEIND:0xF7			2-355
PCIE_P_DECODE_ERR_CNT_8	PCIEIND:0xF8			2-355
PCIE_P_DECODE_ERR_CNT_9	PCIEIND:0xF9			2-355
PCIE_P_DECODE_ERR_CNTL	PCIEIND:0xEF			2-354
PCIE_P_DECODER_STATUS	PCIEIND:0x42			2-338
PCIE_P_IMP_CNTL_STRENGTH	PCIEIND:0x60			2-344
PCIE_P_IMP_CNTL_UPDATE	PCIEIND:0x61			2-344
PCIE_P_MISC_DEBUG_STATUS	PCIEIND:0x43			2-339
PCIE_P_PAD_FORCE_DIS	PCIEIND:0x65			2-345
PCIE_P_PAD_FORCE_EN	PCIEIND:0x64			2-345
PCIE_P_PAD_MISC_CNTL	PCIEIND:0x63			2-345
PCIE_P_PLL_CNTL	PCIEIND:0x44			2-341
PCIE_P_PORT_LANE_STATUS	PCIEIND_P:0x50			2-361
PCIE_P_RCVR_DEBUG_CNTL	PCIEIND:0x45			2-341
PCIE_P_RXP_ERR_RETRAIN_CTL	PCIEIND:0x47			2-343
PCIE_P_STR_CNTL_UPDATE	PCIEIND:0x62			2-344
PCIE_P_SYMSYNC_CTL	PCIEIND:0x46			2-343
PCIE_P90_BRX_PRBS10_ER	PCIEIND:0xC7			2-350
PCIE_P90RX_PRBS10_CNTL	PCIEIND:0xC6			2-350
PCIE_PDNB_CNTL	NBMISCIND:0x7			2-301
PCIE_PERF_LATENCY_CNTL	PCIEIND:0x70			2-346
PCIE_PERF_LATENCY_COUNTER0	PCIEIND:0x77			2-347

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
PCIE_PERF_LATENCY_COUNTER1	PCIEIND:0x78			2-347
PCIE_PERF_LATENCY_MAX	PCIEIND:0x74			2-347
PCIE_PERF_LATENCY_REQ_ID	PCIEIND:0x71			2-346
PCIE_PERF_LATENCY_TAG	PCIEIND:0x72			2-347
PCIE_PERF_LATENCY_THRESHOLD	PCIEIND:0x73			2-347
PCIE_PERF_LATENCY_TIMER_HI	PCIEIND:0x76			2-347
PCIE_PERF_LATENCY_TIMER_LO	PCIEIND:0x75			2-347
PCIE_PERF_MAS_ACC_END_LO	PCIEIND:0xA1			2-348
PCIE_PERF_MAS_ACC_START_END_HI	PCIEIND:0xA2			2-348
PCIE_PERF_MAS_ACC_START_LO	PCIEIND:0xA0			2-348
PCIE_PERF_SLV_ACC_HI	PCIEIND:0xA4			2-348
PCIE_PERF_SLV_ACC_LO	PCIEIND:0xA3			2-348
PCIE_PI_RCVL0S_FTS_DET	PCIEIND:0x50			2-343
PCIE_PORT_DATA	pcieConfigDev[12:2]:0xE4			2-33
PCIE_PORT_INDEX	pcieConfigDev[12:2]:0xE0			2-33
PCIE_PORT_VC_CAP_REG1	AudioPcie:0x114	GpuF0Pcie:0x114	GpuF1Pcie:0x114	2-93
PCIE_PORT_VC_CAP_REG2	AudioPcie:0x118	GpuF0Pcie:0x118	GpuF1Pcie:0x118	2-93
PCIE_PORT_VC_CNTL	AudioPcie:0x11C	GpuF0Pcie:0x11C	GpuF1Pcie:0x11C	2-93
PCIE_PORT_VC_STATUS	AudioPcie:0x11E	GpuF0Pcie:0x11E	GpuF1Pcie:0x11E	2-93
PCIE_PRBS_CLR	PCIEIND:0xC8			2-350
PCIE_PRBS_ERRCNT_0	PCIEIND:0xD0			2-351
PCIE_PRBS_ERRCNT_1	PCIEIND:0xD1			2-352
PCIE_PRBS_ERRCNT_10	PCIEIND:0xDA			2-353
PCIE_PRBS_ERRCNT_11	PCIEIND:0xDB			2-353
PCIE_PRBS_ERRCNT_12	PCIEIND:0xDC			2-353
PCIE_PRBS_ERRCNT_13	PCIEIND:0xDD			2-353
PCIE_PRBS_ERRCNT_14	PCIEIND:0xDE			2-353
PCIE_PRBS_ERRCNT_15	PCIEIND:0xDF			2-354
PCIE_PRBS_ERRCNT_2	PCIEIND:0xD2			2-352
PCIE_PRBS_ERRCNT_3	PCIEIND:0xD3			2-352
PCIE_PRBS_ERRCNT_4	PCIEIND:0xD4			2-352
PCIE_PRBS_ERRCNT_5	PCIEIND:0xD5			2-352
PCIE_PRBS_ERRCNT_6	PCIEIND:0xD6			2-352
PCIE_PRBS_ERRCNT_7	PCIEIND:0xD7			2-352
PCIE_PRBS_ERRCNT_8	PCIEIND:0xD8			2-353
PCIE_PRBS_ERRCNT_9	PCIEIND:0xD9			2-353
PCIE_PRBS_FREERUN	PCIEIND:0xCB			2-350
PCIE_PRBS_HI_BITCNT	PCIEIND:0xCF			2-351
PCIE_PRBS_LO_BITCNT	PCIEIND:0xCE			2-351
PCIE_PRBS_MISC	PCIEIND:0xCC			2-351

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
PCIE_PRBS_STATUS1	PCIEIND:0xC9			2-350
PCIE_PRBS_STATUS2	PCIEIND:0xCA			2-350
PCIE_PRBS_USER_PATTERN	PCIEIND:0xCD			2-351
PCIE_REG_R_RTR_TIMEOUT_CNTL	PCIEIND:0x17			2-329
PCIE_RESERVED	PCIEIND:0x0			2-326
PCIE_RTR_CPL_TIMEOUT_STATUS	PCIEIND:0x13			2-328
PCIE_RX_CNTL	PCIEIND_P:0x70			2-362
PCIE_RX_CREDITS_ALLOCATED_CPL	PCIEIND_P:0x82			2-363
PCIE_RX_CREDITS_ALLOCATED_NP	PCIEIND_P:0x81			2-363
PCIE_RX_CREDITS_ALLOCATED_P	PCIEIND_P:0x80			2-363
PCIE_RX_CREDITS_RECEIVED_CPL	PCIEIND_P:0x85			2-364
PCIE_RX_CREDITS_RECEIVED_NP	PCIEIND_P:0x84			2-364
PCIE_RX_CREDITS_RECEIVED_P	PCIEIND_P:0x83			2-363
PCIE_RX_LAST_TLP0	PCIEIND:0x31			2-333
PCIE_RX_LAST_TLP1	PCIEIND:0x32			2-334
PCIE_RX_LAST_TLP2	PCIEIND:0x33			2-334
PCIE_RX_LAST_TLP3	PCIEIND:0x34			2-334
PCIE_RX_LASTACK_SEQNUM	PCIEIND_P:0x71			2-363
PCIE_RX_NUM_NACK	PCIEIND:0xE			2-326
PCIE_RX_NUM_NACK_GENERATED	PCIEIND:0xF			2-326
PCIE_RX_VENDOR_SPECIFIC	PCIEIND_P:0x72			2-363
PCIE_SCRATCH	PCIEIND:0x1			2-326
PCIE_STRAP_I2C_BD	PCIEIND:0xC4			2-349
PCIE_STRAP_MISC	PCIEIND:0xC0			2-348
PCIE_STRAP_MISC2	PCIEIND:0xC1			2-349
PCIE_STRAP_PI	PCIEIND:0xC2			2-349
PCIE_TX_ACK_LATENCY_LIMIT	PCIEIND_P:0x26			2-359
PCIE_TX_CNTL	PCIEIND_P:0x20			2-358
PCIE_TX_CREDITS_ADVT_CPL	PCIEIND_P:0x32			2-360
PCIE_TX_CREDITS_ADVT_NP	PCIEIND_P:0x31			2-360
PCIE_TX_CREDITS_ADVT_P	PCIEIND_P:0x30			2-360
PCIE_TX_CREDITS_INIT_CPL	PCIEIND_P:0x35			2-360
PCIE_TX_CREDITS_INIT_NP	PCIEIND_P:0x34			2-360
PCIE_TX_CREDITS_INIT_P	PCIEIND_P:0x33			2-360
PCIE_TX_CREDITS_STATUS	PCIEIND_P:0x36			2-361
PCIE_TX_LAST_TLP0	PCIEIND:0x35			2-334
PCIE_TX_LAST_TLP1	PCIEIND:0x36			2-334
PCIE_TX_LAST_TLP2	PCIEIND:0x37			2-334
PCIE_TX_LAST_TLP3	PCIEIND:0x38			2-334
PCIE_TX_REPLAY	PCIEIND_P:0x25			2-359

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
PCIE_TX_REQUEST_NUM_CNTL	PCIEIND_P:0x23			2-359
PCIE_TX_REQUESTER_ID	PCIEIND_P:0x21			2-358
PCIE_TX_SEQ	PCIEIND_P:0x24			2-359
PCIE_TX_SLVCPL_NS_TIMEOUT_CNTL	PCIEIND:0x19			2-330
PCIE_TX_SLVCPL_TIMEOUT_CNTL	PCIEIND:0x18			2-330
PCIE_TX_VENDOR_SPECIFIC	PCIEIND_P:0x22			2-359
PCIE_UNCORR_ERR_MASK	AudioPcie:0x158	GpuF0Pcie:0x158	GpuF1Pcie:0x158	2-96
PCIE_UNCORR_ERR_SEVERITY	AudioPcie:0x15C	GpuF0Pcie:0x15C	GpuF1Pcie:0x15C	2-97
PCIE_UNCORR_ERR_STATUS	AudioPcie:0x154	GpuF0Pcie:0x154	GpuF1Pcie:0x154	2-96
PCIE_VC_ENH_CAP_LIST	AudioPcie:0x110	GpuF0Pcie:0x110	GpuF1Pcie:0x110	2-93
PCIE_VC0_RESOURCE_CAP	AudioPcie:0x120	GpuF0Pcie:0x120	GpuF1Pcie:0x120	2-94
PCIE_VC0_RESOURCE_CNTL	AudioPcie:0x124	GpuF0Pcie:0x124	GpuF1Pcie:0x124	2-94
PCIE_VC0_RESOURCE_STATUS	AudioPcie:0x12A	GpuF0Pcie:0x12A	GpuF1Pcie:0x12A	2-94
PCIE_VC1_RESOURCE_CAP	AudioPcie:0x12C	GpuF0Pcie:0x12C	GpuF1Pcie:0x12C	2-94
PCIE_VC1_RESOURCE_CNTL	AudioPcie:0x130	GpuF0Pcie:0x130	GpuF1Pcie:0x130	2-95
PCIE_VC1_RESOURCE_STATUS	AudioPcie:0x136	GpuF0Pcie:0x136	GpuF1Pcie:0x136	2-95
PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST	AudioPcie:0x100	GpuF0Pcie:0x100	GpuF1Pcie:0x100	2-92
PCIE_VENDOR_SPECIFIC_HDR	AudioPcie:0x104	GpuF0Pcie:0x104	GpuF1Pcie:0x104	2-92
PCIE_VENDOR_SPECIFIC1	AudioPcie:0x108	GpuF0Pcie:0x108	GpuF1Pcie:0x108	2-92
PCIE_VENDOR_SPECIFIC2	AudioPcie:0x10C	GpuF0Pcie:0x10C	GpuF1Pcie:0x10C	2-92
PCIE_WPR_CNTL	PCIEIND:0x30			2-333
PCIEP_HW_DEBUG	PCIEIND_P:0x2			2-357
PCIEP_PORT_CNTL	PCIEIND_P:0x10			2-357
PCIEP_RESERVED	PCIEIND_P:0x0			2-356
PCIEP_SCRATCH	PCIEIND_P:0x1			2-356
PCIEP_STRAP_LC	PCIEIND_P:0xC0			2-373
PCIEP_STRAP_MISC	PCIEIND_P:0xC1			2-374
PLL_VOLTAGE_REG_CNTL	clkconfig:0x6C			2-66
PMI_CAP	AudioPcie:0x52	GpuF0Pcie:0x52	GpuF1Pcie:0x52	2-84
PMI_CAP	AudioPcie:0x52	GpuF0Pcie:0x52	GpuF1Pcie:0x52	2-99
PMI_CAP_LIST	AudioPcie:0x50	GpuF0Pcie:0x50	GpuF1Pcie:0x50	2-83
PMI_CAP_LIST	AudioPcie:0x50	GpuF0Pcie:0x50	GpuF1Pcie:0x50	2-99
PMI_STATUS_CNTL	AudioPcie:0x54	GpuF0Pcie:0x54	GpuF1Pcie:0x54	2-84
PMI_STATUS_CNTL	AudioPcie:0x54	GpuF0Pcie:0x54	GpuF1Pcie:0x54	2-99
PROG_INTERFACE	AudioPcie:0x9	GpuF0Pcie:0x9	GpuF1Pcie:0x9	2-80
Receiver_Control_0	HTIUNBIND:0x1D			2-384
Receiver_Control_1	HTIUNBIND:0x1E			2-385
Receiver_Control_2	HTIUNBIND:0x1F			2-385
Receiver_Control_3	HTIUNBIND:0x20			2-385
Receiver_Control_4	HTIUNBIND:0x33			2-392
REVISION_ID	AudioPcie:0x8	GpuF0Pcie:0x8	GpuF1Pcie:0x8	2-80
ROM_BASE_ADDR	AudioPcie:0x30	GpuF0Pcie:0x30	GpuF1Pcie:0x30	2-82
SCRATCH_4	NBMISCIND:0x74			2-323

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
SCRATCH_5	NBMISCIND:0x75			2-323
SCRATCH_6	NBMISCIND:0x76			2-323
SCRATCH_7	NBMISCIND:0x77			2-323
SCRATCH_8	NBMISCIND:0x78			2-323
SCRATCH_9	NBMISCIND:0x79			2-323
SCRATCH_CLKCFG	clkconfig:0x84			2-68
SCRATCH_NBCFG	nbconfig:0x78			2-18
SD1_CHROMA_MOD_CNTL	GpuF0MMReg:0x5EF0			2-213
SD1_CHROMA_OFFSET	GpuF0MMReg:0x5F90			2-217
SD1_COL_SC_DENOMIN	GpuF0MMReg:0x5EF4			2-213
SD1_COL_SC_INC	GpuF0MMReg:0x5EF8			2-213
SD1_COL_SC_INC_CORR	GpuF0MMReg:0x5EFC			2-214
SD1_COL_SC_PHASE_CNTL	GpuF0MMReg:0x5FD4			2-217
SD1_CRC_CNTL	GpuF0MMReg:0x5F1C			2-216
SD1_CRTC_HV_START	GpuF0MMReg:0x5F98			2-217
SD1_CRTC_TV_FRAMESTART_CNTL	GpuF0MMReg:0x5F9C			2-217
SD1_FORCE_DAC_DATA	GpuF0MMReg:0x5ECC			2-212
SD1_LUMA_BLANK_SETUP_LEVELS	GpuF0MMReg:0x5EA8			2-207
SD1_LUMA_COMB_FILT_CNTL1	GpuF0MMReg:0x5EB8			2-210
SD1_LUMA_COMB_FILT_CNTL2	GpuF0MMReg:0x5EBC			2-210
SD1_LUMA_COMB_FILT_CNTL3	GpuF0MMReg:0x5EC0			2-210
SD1_LUMA_COMB_FILT_CNTL4	GpuF0MMReg:0x5EC4			2-210
SD1_LUMA_FILT_CNTL	GpuF0MMReg:0x5EB4			2-208
SD1_LUMA_OFFSET_LIMIT	GpuF0MMReg:0x5F8C			2-217
SD1_LUMA_SYNC_TIP_LEVELS	GpuF0MMReg:0x5EB0			2-208
SD1_MAIN_CNTL2	GpuF0MMReg:0x5E00			2-206
SD1_RGB_OR_PBPR_BLANK_LEVEL	GpuF0MMReg:0x5EAC			2-208
SD1_SCM_COL_SC_DENOMIN	GpuF0MMReg:0x5F00			2-214
SD1_SCM_COL_SC_INC	GpuF0MMReg:0x5F04			2-214
SD1_SCM_COL_SC_INC_CORR	GpuF0MMReg:0x5F08			2-214
SD1_SCM_DB_DR_SCALE_FACTORS	GpuF0MMReg:0x5F10			2-215
SD1_SCM_MAX_DTO_SWING	GpuF0MMReg:0x5F18			2-216
SD1_SCM_MIN_DTO_SWING	GpuF0MMReg:0x5F14			2-215
SD1_SCM_MOD_CNTL	GpuF0MMReg:0x5F0C			2-215
SD1_SDTV0_DEBUG	GpuF0MMReg:0x5F28			2-216
SD1_U_AND_V_GAIN_SETTINGS	GpuF0MMReg:0x5EA4			2-207
SD1_U_V_BREAK_POINT_SETTINGS	GpuF0MMReg:0x5E9C			2-206
SD1_UPSAMPLE_MODE	GpuF0MMReg:0x5F94			2-217
SD1_VIDEO_PORT_SIG	GpuF0MMReg:0x5F20			2-216
SD1_VIDOUT_MUX_CNTL	GpuF0MMReg:0x5EC8			2-211
SD1_Y_AND_PASSTHRU_GAIN_SETTINGS	GpuF0MMReg:0x5EA0			2-207
SD1_Y_BREAK_POINT_SETTING	GpuF0MMReg:0x5E98			2-206

Table 2-1 All Registers Sorted by Name (Continued)

Name	Address	Secondary Address	Additional Address	Page
SEQ00	VGASEQIND:0x0			2-104
SEQ01	VGASEQIND:0x1			2-105
SEQ02	VGASEQIND:0x2			2-105
SEQ03	VGASEQIND:0x3			2-105
SEQ04	VGASEQIND:0x4			2-106
SEQ8_DATA	GpuF0MMReg:0x3C5	VGA_IO:0x3C5		2-106
SEQ8_IDX	GpuF0MMReg:0x3C4	VGA_IO:0x3C4		2-106
STATUS	AudioPcie:0x6	GpuF0Pcie:0x6	GpuF1Pcie:0x6	2-79
StrapsOutputMux_0	NBMISCIND:0x70			2-320
StrapsOutputMux_1	NBMISCIND:0x71			2-320
StrapsOutputMux_2	NBMISCIND:0x72			2-321
StrapsOutputMux_3	NBMISCIND:0x73			2-321
StrapsOutputMux_4	NBMISCIND:0x64			2-321
StrapsOutputMux_5	NBMISCIND:0x65			2-321
StrapsOutputMux_6	NBMISCIND:0x66			2-321
StrapsOutputMux_7	NBMISCIND:0x67			2-321
StrapsOutputMux_8	NBMISCIND:0x68			2-321
StrapsOutputMux_9	NBMISCIND:0x69			2-322
StrapsOutputMux_A	NBMISCIND:0x6A			2-322
StrapsOutputMux_B	NBMISCIND:0x6B			2-322
StrapsOutputMux_C	NBMISCIND:0x6C			2-322
StrapsOutputMux_D	NBMISCIND:0x6D			2-322
StrapsOutputMux_E	NBMISCIND:0x6E			2-322
StrapsOutputMux_F	NBMISCIND:0x6F			2-322
SUB_CLASS	AudioPcie:0xA	GpuF0Pcie:0xA	GpuF1Pcie:0xA	2-80
Transmiter_Control_0	HTIUNBIND:0x23			2-386
Transmiter_Control_1	HTIUNBIND:0x24			2-386
Transmiter_Control_2	HTIUNBIND:0x25			2-387
TX_B_P90PLL_IBias	HTIUNBIND:0x46			2-395
VENDOR_ID	AudioPcie:0x0	GpuF0Pcie:0x0	GpuF1Pcie:0x0	2-78

A.3 All Registers Sorted By Address

Table 2-2 All Registers Sorted by Address

Name	Address	Secondary Address	Additional Address	Page
APC_VENDOR_ID	apcconfig:0x0			2-56
APC_SUB_BUS_NUMBER_LATENCY	apcconfig:0x18			2-59
APC_AGP_PCI_IOBASE_LIMIT	apcconfig:0x1C			2-60
APC_AGP_PCI_STATUS	apcconfig:0x1E			2-60
APC_DEVICE_ID	apcconfig:0x2			2-56
APC_AGP_PCI_MEMORY_LIMIT_BASE	apcconfig:0x20			2-60
APC_AGP_PCI_PREFETCHABLE_LIMIT_BASE	apcconfig:0x24			2-61
APC_AGP_PCI_PREFETCHABLE_BASE_Upper	apcconfig:0x28			2-61
APC_AGP_PCI_PREFETCHABLE_LIMIT_Upper	apcconfig:0x2C			2-61
APC_CAPABILITIES_PTR	apcconfig:0x34			2-61
APC_COMMAND	apcconfig:0x4			2-56
APC_MISC_DEVICE_CTRL	apcconfig:0x40			2-62
APC_HT_MSI_CAP	apcconfig:0x44			2-62
APC_ADAPTER_ID_W	apcconfig:0x4C			2-62
APC_STATUS	apcconfig:0x6			2-57
APC_REVISION_ID	apcconfig:0x8			2-58
APC_REGPROG_INF	apcconfig:0x9			2-58
APC_SUB_CLASS	apcconfig:0xA			2-58
APC_BASE_CODE	apcconfig:0xB			2-58
APC_SSID_CAP_ID	apcconfig:0xB0			2-63
APC_SSID	apcconfig:0xB4			2-63
APC_CACHE_LINE	apcconfig:0xC			2-58
APC_LATENCY	apcconfig:0xD			2-59
APC_HEADER	apcconfig:0xE			2-59
APC_BIST	apcconfig:0xF			2-59
VENDOR_ID	AudioPcie:0x0	GpuF0Pcie:0x0	GpuF1Pcie:0x0	2-78
BASE_ADDR_1	AudioPcie:0x10	GpuF0Pcie:0x10	GpuF1Pcie:0x10	2-81
PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST	AudioPcie:0x100	GpuF0Pcie:0x100	GpuF1Pcie:0x100	2-92
PCIE_VENDOR_SPECIFIC_HDR	AudioPcie:0x104	GpuF0Pcie:0x104	GpuF1Pcie:0x104	2-92
PCIE_VENDOR_SPECIFIC1	AudioPcie:0x108	GpuF0Pcie:0x108	GpuF1Pcie:0x108	2-92
PCIE_VENDOR_SPECIFIC2	AudioPcie:0x10C	GpuF0Pcie:0x10C	GpuF1Pcie:0x10C	2-92
PCIE_VC_ENH_CAP_LIST	AudioPcie:0x110	GpuF0Pcie:0x110	GpuF1Pcie:0x110	2-93
PCIE_PORT_VC_CAP_REG1	AudioPcie:0x114	GpuF0Pcie:0x114	GpuF1Pcie:0x114	2-93
PCIE_PORT_VC_CAP_REG2	AudioPcie:0x118	GpuF0Pcie:0x118	GpuF1Pcie:0x118	2-93
PCIE_PORT_VC_CNTL	AudioPcie:0x11C	GpuF0Pcie:0x11C	GpuF1Pcie:0x11C	2-93
PCIE_PORT_VC_STATUS	AudioPcie:0x11E	GpuF0Pcie:0x11E	GpuF1Pcie:0x11E	2-93
PCIE_VC0_RESOURCE_CAP	AudioPcie:0x120	GpuF0Pcie:0x120	GpuF1Pcie:0x120	2-94
PCIE_VC0_RESOURCE_CNTL	AudioPcie:0x124	GpuF0Pcie:0x124	GpuF1Pcie:0x124	2-94
PCIE_VC0_RESOURCE_STATUS	AudioPcie:0x12A	GpuF0Pcie:0x12A	GpuF1Pcie:0x12A	2-94

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
PCIE_VC1_RESOURCE_CAP	AudioPcie:0x12C	GpuF0Pcie:0x12C	GpuF1Pcie:0x12C	2-94
PCIE_VC1_RESOURCE_CNTL	AudioPcie:0x130	GpuF0Pcie:0x130	GpuF1Pcie:0x130	2-95
PCIE_VC1_RESOURCE_STATUS	AudioPcie:0x136	GpuF0Pcie:0x136	GpuF1Pcie:0x136	2-95
BASE_ADDR_2	AudioPcie:0x14	GpuF0Pcie:0x14	GpuF1Pcie:0x14	2-81
PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST	AudioPcie:0x140	GpuF0Pcie:0x140	GpuF1Pcie:0x140	2-95
PCIE_DEV_SERIAL_NUM_DW1	AudioPcie:0x144	GpuF0Pcie:0x144	GpuF1Pcie:0x144	2-95
PCIE_DEV_SERIAL_NUM_DW2	AudioPcie:0x148	GpuF0Pcie:0x148	GpuF1Pcie:0x148	2-95
PCIE_ADV_ERR_RPT_ENH_CAP_LIST	AudioPcie:0x150	GpuF0Pcie:0x150	GpuF1Pcie:0x150	2-96
PCIE_UNCORR_ERR_STATUS	AudioPcie:0x154	GpuF0Pcie:0x154	GpuF1Pcie:0x154	2-96
PCIE_UNCORR_ERR_MASK	AudioPcie:0x158	GpuF0Pcie:0x158	GpuF1Pcie:0x158	2-96
PCIE_UNCORR_ERR_SEVERITY	AudioPcie:0x15C	GpuF0Pcie:0x15C	GpuF1Pcie:0x15C	2-97
PCIE_CORR_ERR_STATUS	AudioPcie:0x160	GpuF0Pcie:0x160	GpuF1Pcie:0x160	2-97
PCIE_CORR_ERR_MASK	AudioPcie:0x164	GpuF0Pcie:0x164	GpuF1Pcie:0x164	2-97
PCIE_ADV_ERR_CAP_CNTL	AudioPcie:0x168	GpuF0Pcie:0x168	GpuF1Pcie:0x168	2-97
PCIE_HDR_LOG0	AudioPcie:0x16C	GpuF0Pcie:0x16C	GpuF1Pcie:0x16C	2-98
PCIE_HDR_LOG1	AudioPcie:0x170	GpuF0Pcie:0x170	GpuF1Pcie:0x170	2-98
PCIE_HDR_LOG2	AudioPcie:0x174	GpuF0Pcie:0x174	GpuF1Pcie:0x174	2-98
PCIE_HDR_LOG3	AudioPcie:0x178	GpuF0Pcie:0x178	GpuF1Pcie:0x178	2-98
BASE_ADDR_3	AudioPcie:0x18	GpuF0Pcie:0x18	GpuF1Pcie:0x18	2-81
PCIE_CAC_ENH_CAP_LIST	AudioPcie:0x190	GpuF0Pcie:0x190	GpuF1Pcie:0x190	2-98
PCIE_CAC_DEVICE_CORRELATION	AudioPcie:0x194	GpuF0Pcie:0x194	GpuF1Pcie:0x194	2-98
BASE_ADDR_4	AudioPcie:0x1C	GpuF0Pcie:0x1C	GpuF1Pcie:0x1C	2-81
DEVICE_ID	AudioPcie:0x2	GpuF0Pcie:0x2	GpuF1Pcie:0x2	2-78
BASE_ADDR_5	AudioPcie:0x20	GpuF0Pcie:0x20	GpuF1Pcie:0x20	2-82
BASE_ADDR_6	AudioPcie:0x24	GpuF0Pcie:0x24	GpuF1Pcie:0x24	2-82
ADAPTER_ID	AudioPcie:0x2C	GpuF0Pcie:0x2C	GpuF1Pcie:0x2C	2-83
ROM_BASE_ADDR	AudioPcie:0x30	GpuF0Pcie:0x30	GpuF1Pcie:0x30	2-82
CAP_PTR	AudioPcie:0x34	GpuF0Pcie:0x34	GpuF1Pcie:0x34	2-82
INTERRUPT_LINE	AudioPcie:0x3C	GpuF0Pcie:0x3C	GpuF1Pcie:0x3C	2-82
INTERRUPT_PIN	AudioPcie:0x3D	GpuF0Pcie:0x3D	GpuF1Pcie:0x3D	2-82
MIN_GRANT	AudioPcie:0x3E	GpuF0Pcie:0x3E	GpuF1Pcie:0x3E	2-83
MAX_LATENCY	AudioPcie:0x3F	GpuF0Pcie:0x3F	GpuF1Pcie:0x3F	2-83
COMMAND	AudioPcie:0x4	GpuF0Pcie:0x4	GpuF1Pcie:0x4	2-78
ADAPTER_ID_W	AudioPcie:0x4C	GpuF0Pcie:0x4C	GpuF1Pcie:0x4C	2-83
PMI_CAP_LIST	AudioPcie:0x50	GpuF0Pcie:0x50	GpuF1Pcie:0x50	2-83
PMI_CAP_LIST	AudioPcie:0x50	GpuF0Pcie:0x50	GpuF1Pcie:0x50	2-99
PMI_CAP	AudioPcie:0x52	GpuF0Pcie:0x52	GpuF1Pcie:0x52	2-84
PMI_CAP	AudioPcie:0x52	GpuF0Pcie:0x52	GpuF1Pcie:0x52	2-99
PMI_STATUS_CNTL	AudioPcie:0x54	GpuF0Pcie:0x54	GpuF1Pcie:0x54	2-84
PMI_STATUS_CNTL	AudioPcie:0x54	GpuF0Pcie:0x54	GpuF1Pcie:0x54	2-99
PCIE_CAP_LIST	AudioPcie:0x58	GpuF0Pcie:0x58	GpuF1Pcie:0x58	2-84
PCIE_CAP	AudioPcie:0x5A	GpuF0Pcie:0x5A	GpuF1Pcie:0x5A	2-85
DEVICE_CAP	AudioPcie:0x5C	GpuF0Pcie:0x5C	GpuF1Pcie:0x5C	2-85

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
STATUS	AudioPcie:0x6	GpuF0Pcie:0x6	GpuF1Pcie:0x6	2-79
DEVICE_CNTL	AudioPcie:0x60	GpuF0Pcie:0x60	GpuF1Pcie:0x60	2-86
DEVICE_STATUS	AudioPcie:0x62	GpuF0Pcie:0x62	GpuF1Pcie:0x62	2-87
LINK_CAP	AudioPcie:0x64	GpuF0Pcie:0x64	GpuF1Pcie:0x64	2-87
LINK_CNTL	AudioPcie:0x68	GpuF0Pcie:0x68	GpuF1Pcie:0x68	2-88
LINK_STATUS	AudioPcie:0x6A	GpuF0Pcie:0x6A	GpuF1Pcie:0x6A	2-89
DEVICE_CAP2	AudioPcie:0x7C	GpuF0Pcie:0x7C	GpuF1Pcie:0x7C	2-89
REVISION_ID	AudioPcie:0x8	GpuF0Pcie:0x8	GpuF1Pcie:0x8	2-80
DEVICE_CNTL2	AudioPcie:0x80	GpuF0Pcie:0x80	GpuF1Pcie:0x80	2-89
DEVICE_STATUS2	AudioPcie:0x82	GpuF0Pcie:0x82	GpuF1Pcie:0x82	2-90
LINK_CAP2	AudioPcie:0x84	GpuF0Pcie:0x84	GpuF1Pcie:0x84	2-90
LINK_CNTL2	AudioPcie:0x88	GpuF0Pcie:0x88	GpuF1Pcie:0x88	2-90
LINK_STATUS2	AudioPcie:0x8A	GpuF0Pcie:0x8A	GpuF1Pcie:0x8A	2-90
PROG_INTERFACE	AudioPcie:0x9	GpuF0Pcie:0x9	GpuF1Pcie:0x9	2-80
SUB_CLASS	AudioPcie:0xA	GpuF0Pcie:0xA	GpuF1Pcie:0xA	2-80
MSI_CAP_LIST	AudioPcie:0xA0	GpuF0Pcie:0xA0	GpuF1Pcie:0xA0	2-91
MSI_MSG_CNTL	AudioPcie:0xA2	GpuF0Pcie:0xA2	GpuF1Pcie:0xA2	2-91
MSI_MSG_ADDR_LO	AudioPcie:0xA4	GpuF0Pcie:0xA4	GpuF1Pcie:0xA4	2-91
MSI_MSG_ADDR_HI	AudioPcie:0xA8	GpuF0Pcie:0xA8	GpuF1Pcie:0xA8	2-91
MSI_MSG_DATA	AudioPcie:0xA8	GpuF0Pcie:0xA8	GpuF1Pcie:0xA8	2-92
MSI_MSG_DATA_64	AudioPcie:0xAC	GpuF0Pcie:0xAC	GpuF1Pcie:0xAC	2-92
BASE_CLASS	AudioPcie:0xB	GpuF0Pcie:0xB	GpuF1Pcie:0xB	2-80
CACHE_LINE	AudioPcie:0xC	GpuF0Pcie:0xC	GpuF1Pcie:0xC	2-80
LATENCY	AudioPcie:0xD	GpuF0Pcie:0xD	GpuF1Pcie:0xD	2-80
HEADER	AudioPcie:0xE	GpuF0Pcie:0xE	GpuF1Pcie:0xE	2-81
BIST	AudioPcie:0xF	GpuF0Pcie:0xF	GpuF1Pcie:0xF	2-81
OSC_CONTROL	clkconfig:0x40			2-64
CPLL_CONTROL	clkconfig:0x44			2-65
CLK_TOP_PWM7_CNTL	clkconfig:0x48			2-73
clk_top_pwm4_ctrl	clkconfig:0x4C			2-73
clk_top_pwm5_ctrl	clkconfig:0x50			2-73
clk_top_pwm6_ctrl	clkconfig:0x54			2-73
MC_CLK_CNTRL	clkconfig:0x58			2-65
DELAY_SET_IOC_CCLK	clkconfig:0x5C			2-65
MC_CLK_INDEX	clkconfig:0x60			2-66
MC_CLK_DATA	clkconfig:0x64			2-66
CT_DISABLE_BIU	clkconfig:0x68			2-66
PLL_VOLTAGE_REG_CNTL	clkconfig:0x6C			2-66
CPLL_CONTROL3	clkconfig:0x70			2-67
GC_CLK_CNTRL	clkconfig:0x74			2-67
CG_MISC_INPUT_1	clkconfig:0x78			2-68
CG_MISC_INPUT_2	clkconfig:0x7C			2-68
MC_DATA_DLL_CNTRL_A	clkconfig:0x80			2-68
SCRATCH_CLKCFG	clkconfig:0x84			2-68
MC_ACMD_DLL_CNTRL_A	clkconfig:0x88			2-68
MC_ACMD_DLL_CNTRL_B	clkconfig:0x89			2-69

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
CLKGATE_DISABLE2	clkconfig:0x8C			2-69
CG_MISC_INPUT_3	clkconfig:0x90			2-69
CLKGATE_DISABLE	clkconfig:0x94			2-70
CPLL_CONTROL2	clkconfig:0x98			2-71
ILA_CLK_INDEX	clkconfig:0x9C			2-77
ILA_CLK_DATA	clkconfig:0xA0			2-77
clk_top_pwm1_ctrl	clkconfig:0xB0			2-75
clk_top_pwm2_ctrl	clkconfig:0xB4			2-75
clk_top_test_ctrl	clkconfig:0xB8			2-76
NBCLK_IO_CONTROL	clkconfig:0xBC			2-71
CLK_TOP_THERMAL_ALERT_INTR_EN	clkconfig:0xC0			2-72
CLK_TOP_THERMAL_ALERT_STATUS	clkconfig:0xC4			2-72
CLK_TOP_THERMAL_ALERT_WAIT_WINDOW	clkconfig:0xC8			2-72
clk_top_pwm3_ctrl	clkconfig:0xCC			2-72
clk_top_spare_pll	clkconfig:0xD0			2-74
CLK_CFG_HTPLL_CNTL	clkconfig:0xD4			2-74
GPIO_ctrl	clkconfig:0xDC			2-73
CLK_TOP_SPARE_A	clkconfig:0xE0			2-74
CLK_TOP_SPARE_B	clkconfig:0xE4			2-75
CLK_TOP_SPARE_C	clkconfig:0xE8			2-75
CLK_TOP_SPARE_D	clkconfig:0xEC			2-75
CLK_MISC_INDEX	clkconfig:0xF0			2-76
CLK_MISC_DATA	clkconfig:0xF4			2-76
CFG_CT_CLKGATE_HTIU	clkconfig:0xF8			2-76
clk_la_shift_reg_stage0	CLKMISCIND:0x0			2-406
clk_la_shift_reg_stage1	CLKMISCIND:0x1			2-406
clk_la_shift_reg_stage2	CLKMISCIND:0x2			2-406
clk_la_shift_reg_stage3	CLKMISCIND:0x3			2-406
clk_la_shift_reg_stage4	CLKMISCIND:0x4			2-406
clk_la_shift_reg_stage5	CLKMISCIND:0x5			2-406
clk_la_shift_reg_stage6	CLKMISCIND:0x6			2-407
clk_la_shift_reg_stage7	CLKMISCIND:0x7			2-407
clk_la_config	CLKMISCIND:0x8			2-407
clk_la_status	CLKMISCIND:0x9			2-407
MM_INDEX	GpuF0MMReg:0x0	GpuIOReg:0x0		2-100
CRTC8_IDX	GpuF0MMReg:0x3B4	GpuF0MMReg:0x3D4	VGA_IO:0x3B4 VGA_IO:0x3D4	2-106
CRTC8_DATA	GpuF0MMReg:0x3B5	GpuF0MMReg:0x3D5	VGA_IO:0x3B5 VGA_IO:0x3D5	2-106
GENFC_WT	GpuF0MMReg:0x3BA	GpuF0MMReg:0x3DA	VGA_IO:0x3BA VGA_IO:0x3DA	2-101
GENS1	GpuF0MMReg:0x3BA	GpuF0MMReg:0x3DA	VGA_IO:0x3BA VGA_IO:0x3DA	2-103
ATTRX	GpuF0MMReg:0x3C0	VGA_IO:0x3C0		2-116

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
ATTRDW	GpuF0MMReg:0x3C0	VGA_IO:0x3C0		2-116
ATTRDR	GpuF0MMReg:0x3C1	VGA_IO:0x3C1		2-116
GENMO_WT	GpuF0MMReg:0x3C2	VGA_IO:0x3C2		2-101
GENS0	GpuF0MMReg:0x3C2	VGA_IO:0x3C2		2-102
GENENB	GpuF0MMReg:0x3C3	VGA_IO:0x3C3		2-102
SEQ8_IDX	GpuF0MMReg:0x3C4	VGA_IO:0x3C4		2-106
SEQ8_DATA	GpuF0MMReg:0x3C5	VGA_IO:0x3C5		2-106
DAC_MASK	GpuF0MMReg:0x3C6	VGA_IO:0x3C6		2-104
DAC_R_INDEX	GpuF0MMReg:0x3C7	VGA_IO:0x3C7		2-104
DAC_W_INDEX	GpuF0MMReg:0x3C8	VGA_IO:0x3C8		2-104
DAC_DATA	GpuF0MMReg:0x3C9	VGA_IO:0x3C9		2-103
GENFC_RD	GpuF0MMReg:0x3CA	VGA_IO:0x3CA		2-101
GENMO_RD	GpuF0MMReg:0x3CC	VGA_IO:0x3CC		2-102
GRPH8_IDX	GpuF0MMReg:0x3CE	VGA_IO:0x3CE		2-114
GRPH8_DATA	GpuF0MMReg:0x3CF	VGA_IO:0x3CF		2-114
MM_DATA	GpuF0MMReg:0x4	GpuIOReg:0x4		2-100
MM_CFGREGS_CNTL	GpuF0MMReg:0x544C			2-100
SD1_MAIN_CNTL2	GpuF0MMReg:0x5E00			2-206
SD1_Y_BREAK_POINT_SETTING	GpuF0MMReg:0x5E98			2-206
SD1_U_V_BREAK_POINT_SETTINGS	GpuF0MMReg:0x5E9C			2-206
SD1_Y_AND_PASSTHRU_GAIN_SETTINGS	GpuF0MMReg:0x5EA0			2-207
SD1_U_AND_V_GAIN_SETTINGS	GpuF0MMReg:0x5EA4			2-207
SD1_LUMA_BLANK_SETUP_LEVELS	GpuF0MMReg:0x5EA8			2-207
SD1_RGB_OR_PBPR_BLANK_LEVEL	GpuF0MMReg:0x5EAC			2-208
SD1_LUMA_SYNC_TIP_LEVELS	GpuF0MMReg:0x5EB0			2-208
SD1_LUMA_FILT_CNTL	GpuF0MMReg:0x5EB4			2-208
SD1_LUMA_COMB_FILT_CNTL1	GpuF0MMReg:0x5EB8			2-210
SD1_LUMA_COMB_FILT_CNTL2	GpuF0MMReg:0x5EBC			2-210
SD1_LUMA_COMB_FILT_CNTL3	GpuF0MMReg:0x5EC0			2-210
SD1_LUMA_COMB_FILT_CNTL4	GpuF0MMReg:0x5EC4			2-210
SD1_VIDOUT_MUX_CNTL	GpuF0MMReg:0x5EC8			2-211
SD1_FORCE_DAC_DATA	GpuF0MMReg:0x5ECC			2-212
SD1_CHROMA_MOD_CNTL	GpuF0MMReg:0x5EF0			2-213
SD1_COL_SC_DENOMIN	GpuF0MMReg:0x5EF4			2-213
SD1_COL_SC_INC	GpuF0MMReg:0x5EF8			2-213
SD1_COL_SC_INC_CORR	GpuF0MMReg:0x5EFC			2-214
SD1_SCM_COL_SC_DENOMIN	GpuF0MMReg:0x5F00			2-214
SD1_SCM_COL_SC_INC	GpuF0MMReg:0x5F04			2-214
SD1_SCM_COL_SC_INC_CORR	GpuF0MMReg:0x5F08			2-214
SD1_SCM_MOD_CNTL	GpuF0MMReg:0x5F0C			2-215
SD1_SCM_DB_DR_SCALE_FACTORS	GpuF0MMReg:0x5F10			2-215
SD1_SCM_MIN_DTO_SWING	GpuF0MMReg:0x5F14			2-215
SD1_SCM_MAX_DTO_SWING	GpuF0MMReg:0x5F18			2-216

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
SD1_CRC_CNTL	GpuF0MMReg:0x5F1C			2-216
SD1_VIDEO_PORT_SIG	GpuF0MMReg:0x5F20			2-216
SD1_SDTV0_DEBUG	GpuF0MMReg:0x5F28			2-216
SD1_LUMA_OFFSET_LIMIT	GpuF0MMReg:0x5F8C			2-217
SD1_CHROMA_OFFSET	GpuF0MMReg:0x5F90			2-217
SD1_UPSAMPLE_MODE	GpuF0MMReg:0x5F94			2-217
SD1_CRTC_HV_START	GpuF0MMReg:0x5F98			2-217
SD1_CRTC_TV_FRAMESTART_CNTL	GpuF0MMReg:0x5F9C			2-217
SD1_COL_SC_PHASE_CNTL	GpuF0MMReg:0x5FD4			2-217
D1CRTC_MVP_CONTROL1	GpuF0MMReg:0x6038			2-154
D1CRTC_MVP_CONTROL2	GpuF0MMReg:0x603C			2-155
D1CRTC_MVP_FIFO_CONTROL	GpuF0MMReg:0x6040			2-156
D1CRTC_MVP_FIFO_STATUS	GpuF0MMReg:0x6044			2-156
D1CRTC_MVP_SLAVE_STATUS	GpuF0MMReg:0x6048			2-156
D1CRTC_MVP_INBAND_CNTL_CAP	GpuF0MMReg:0x604C			2-156
D1CRTC_MVP_INBAND_CNTL_INSERT	GpuF0MMReg:0x6050			2-157
D1CRTC_MVP_INBAND_CNTL_INSERT_TIMER	GpuF0MMReg:0x6054			2-157
D1CRTC_MVP_BLACK_KEYER	GpuF0MMReg:0x6058			2-157
D1CRTC_MVP_STATUS	GpuF0MMReg:0x605C			2-157
D1GRPH_ENABLE	GpuF0MMReg:0x6100			2-122
D1GRPH_CONTROL	GpuF0MMReg:0x6104			2-122
D1GRPH_LUT_SEL	GpuF0MMReg:0x6108			2-124
D1GRPH_SWAP_CNTL	GpuF0MMReg:0x610C			2-124
D1GRPH_PRIMARY_SURFACE_ADDRESS	GpuF0MMReg:0x6110			2-125
D1GRPH_SECONDARY_SURFACE_ADDRESS	GpuF0MMReg:0x6118			2-125
D1GRPH_PITCH	GpuF0MMReg:0x6120			2-125
D1GRPH_SURFACE_OFFSET_X	GpuF0MMReg:0x6124			2-125
D1GRPH_SURFACE_OFFSET_Y	GpuF0MMReg:0x6128			2-126
D1GRPH_X_START	GpuF0MMReg:0x612C			2-126
D1GRPH_Y_START	GpuF0MMReg:0x6130			2-126
D1GRPH_X_END	GpuF0MMReg:0x6134			2-126
D1GRPH_Y_END	GpuF0MMReg:0x6138			2-126
D1COLOR_SPACE_CONVERT	GpuF0MMReg:0x613C			2-147
D1OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	GpuF0MMReg:0x6140			2-143
D1GRPH_UPDATE	GpuF0MMReg:0x6144			2-127
D1GRPH_FLIP_CONTROL	GpuF0MMReg:0x6148			2-128
D1GRPH_SURFACE_ADDRESS_INUSE	GpuF0MMReg:0x614C			2-128
D1GRPH_DFQ_CONTROL	GpuF0MMReg:0x6150			2-144
D1GRPH_DFQ_STATUS	GpuF0MMReg:0x6154			2-144
D1GRPH_INTERRUPT_STATUS	GpuF0MMReg:0x6158			2-144

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
D1GRPH_INTERRUPT_CONTROL	GpuF0MMReg:0x615C			2-144
D1OVL_ENABLE	GpuF0MMReg:0x6180			2-128
D1OVL_CONTROL1	GpuF0MMReg:0x6184			2-129
D1OVL_CONTROL2	GpuF0MMReg:0x6188			2-130
D1OVL_SWAP_CNTL	GpuF0MMReg:0x618C			2-130
D1OVL_SURFACE_ADDRESS	GpuF0MMReg:0x6190			2-130
D1OVL_PITCH	GpuF0MMReg:0x6198			2-131
D1OVL_SURFACE_OFFSET_X	GpuF0MMReg:0x619C			2-131
D1OVL_SURFACE_OFFSET_Y	GpuF0MMReg:0x61A0			2-131
D1OVL_START	GpuF0MMReg:0x61A4			2-131
D1OVL_END	GpuF0MMReg:0x61A8			2-131
D1OVL_UPDATE	GpuF0MMReg:0x61AC			2-132
D1OVL_SURFACE_ADDRESS_IN USE	GpuF0MMReg:0x61B0			2-132
D1OVL_DFQ_CONTROL	GpuF0MMReg:0x61B4			2-133
D1OVL_DFQ_STATUS	GpuF0MMReg:0x61B8			2-133
D1OVL_MATRIX_TRANSFORM_E N	GpuF0MMReg:0x6200			2-133
D1OVL_MATRIX_COEF_1_1	GpuF0MMReg:0x6204			2-133
D1OVL_MATRIX_COEF_1_2	GpuF0MMReg:0x6208			2-134
D1OVL_MATRIX_COEF_1_3	GpuF0MMReg:0x620C			2-134
D1OVL_MATRIX_COEF_1_4	GpuF0MMReg:0x6210			2-134
D1OVL_MATRIX_COEF_2_1	GpuF0MMReg:0x6214			2-134
D1OVL_MATRIX_COEF_2_2	GpuF0MMReg:0x6218			2-134
D1OVL_MATRIX_COEF_2_3	GpuF0MMReg:0x621C			2-135
D1OVL_MATRIX_COEF_2_4	GpuF0MMReg:0x6220			2-135
D1OVL_MATRIX_COEF_3_1	GpuF0MMReg:0x6224			2-135
D1OVL_MATRIX_COEF_3_2	GpuF0MMReg:0x6228			2-135
D1OVL_MATRIX_COEF_3_3	GpuF0MMReg:0x622C			2-135
D1OVL_MATRIX_COEF_3_4	GpuF0MMReg:0x6230			2-136
D1OVL_PWL_TRANSFORM_EN	GpuF0MMReg:0x6280			2-136
D1OVL_PWL_0TOF	GpuF0MMReg:0x6284			2-136
D1OVL_PWL_10TO1F	GpuF0MMReg:0x6288			2-136
D1OVL_PWL_20TO3F	GpuF0MMReg:0x628C			2-136
D1OVL_PWL_40TO7F	GpuF0MMReg:0x6290			2-137
D1OVL_PWL_80TOBF	GpuF0MMReg:0x6294			2-137
D1OVL_PWL_C0TOFF	GpuF0MMReg:0x6298			2-137
D1OVL_PWL_100TO13F	GpuF0MMReg:0x629C			2-137
D1OVL_PWL_140TO17F	GpuF0MMReg:0x62A0			2-137
D1OVL_PWL_180TO1BF	GpuF0MMReg:0x62A4			2-138
D1OVL_PWL_1C0TO1FF	GpuF0MMReg:0x62A8			2-138
D1OVL_PWL_200TO23F	GpuF0MMReg:0x62AC			2-138
D1OVL_PWL_240TO27F	GpuF0MMReg:0x62B0			2-138
D1OVL_PWL_280TO2BF	GpuF0MMReg:0x62B4			2-138
D1OVL_PWL_2C0TO2FF	GpuF0MMReg:0x62B8			2-139
D1OVL_PWL_300TO33F	GpuF0MMReg:0x62BC			2-139
D1OVL_PWL_340TO37F	GpuF0MMReg:0x62C0			2-139

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
D1OVL_PWL_380TO3BF	GpuF0MMReg:0x62C4			2-139
D1OVL_PWL_3C0TO3FF	GpuF0MMReg:0x62C8			2-139
D1OVL_KEY_CONTROL	GpuF0MMReg:0x6300			2-140
D1GRPH_ALPHA	GpuF0MMReg:0x6304			2-140
D1OVL_ALPHA	GpuF0MMReg:0x6308			2-140
D1OVL_ALPHA_CONTROL	GpuF0MMReg:0x630C			2-141
D1GRPH_KEY_RANGE_RED	GpuF0MMReg:0x6310			2-141
D1GRPH_KEY_RANGE_GREEN	GpuF0MMReg:0x6314			2-141
D1GRPH_KEY_RANGE_BLUE	GpuF0MMReg:0x6318			2-142
D1GRPH_KEY_RANGE_ALPHA	GpuF0MMReg:0x631C			2-142
D1OVL_KEY_RANGE_RED_CR	GpuF0MMReg:0x6320			2-142
D1OVL_KEY_RANGE_GREEN_Y	GpuF0MMReg:0x6324			2-142
D1OVL_KEY_RANGE_BLUE_CB	GpuF0MMReg:0x6328			2-143
D1OVL_KEY_ALPHA	GpuF0MMReg:0x632C			2-143
D1GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL	GpuF0MMReg:0x6380			2-145
D1COLOR_MATRIX_COEF_1_1	GpuF0MMReg:0x6384			2-145
D1COLOR_MATRIX_COEF_1_2	GpuF0MMReg:0x6388			2-145
D1COLOR_MATRIX_COEF_1_3	GpuF0MMReg:0x638C			2-145
D1COLOR_MATRIX_COEF_1_4	GpuF0MMReg:0x6390			2-145
D1COLOR_MATRIX_COEF_2_1	GpuF0MMReg:0x6394			2-146
D1COLOR_MATRIX_COEF_2_2	GpuF0MMReg:0x6398			2-146
D1COLOR_MATRIX_COEF_2_3	GpuF0MMReg:0x639C			2-146
D1COLOR_MATRIX_COEF_2_4	GpuF0MMReg:0x63A0			2-146
D1COLOR_MATRIX_COEF_3_1	GpuF0MMReg:0x63A4			2-146
D1COLOR_MATRIX_COEF_3_2	GpuF0MMReg:0x63A8			2-147
D1COLOR_MATRIX_COEF_3_3	GpuF0MMReg:0x63AC			2-147
D1COLOR_MATRIX_COEF_3_4	GpuF0MMReg:0x63B0			2-147
D1CUR_CONTROL	GpuF0MMReg:0x6400			2-149
D1CUR_SURFACE_ADDRESS	GpuF0MMReg:0x6408			2-150
D1CUR_SIZE	GpuF0MMReg:0x6410			2-150
D1CUR_POSITION	GpuF0MMReg:0x6414			2-150
D1CUR_HOT_SPOT	GpuF0MMReg:0x6418			2-150
D1CUR_COLOR1	GpuF0MMReg:0x641C			2-150
D1CUR_COLOR2	GpuF0MMReg:0x6420			2-151
D1CUR_UPDATE	GpuF0MMReg:0x6424			2-151
D1ICON_CONTROL	GpuF0MMReg:0x6440			2-152
D1ICON_SURFACE_ADDRESS	GpuF0MMReg:0x6448			2-152
D1ICON_SIZE	GpuF0MMReg:0x6450			2-152
D1ICON_START_POSITION	GpuF0MMReg:0x6454			2-152
D1ICON_COLOR1	GpuF0MMReg:0x6458			2-153
D1ICON_COLOR2	GpuF0MMReg:0x645C			2-153
D1ICON_UPDATE	GpuF0MMReg:0x6460			2-153
DC_LUT_RW_SELECT	GpuF0MMReg:0x6480			2-193
DC_LUT_RW_MODE	GpuF0MMReg:0x6484			2-193
DC_LUT_RW_INDEX	GpuF0MMReg:0x6488			2-193

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
DC_LUT_SEQ_COLOR	GpuF0MMReg:0x648C			2-193
DC_LUT_PWL_DATA	GpuF0MMReg:0x6490			2-194
DC_LUT_30_COLOR	GpuF0MMReg:0x6494			2-194
DC_LUT_READ_PIPE_SELECT	GpuF0MMReg:0x6498			2-194
DC_LUT_WRITE_EN_MASK	GpuF0MMReg:0x649C			2-194
DC_LUT_AUTOFILL	GpuF0MMReg:0x64A0			2-195
DC_LUTA_CONTROL	GpuF0MMReg:0x64C0			2-195
DC_LUTA_BLACK_OFFSET_BLUE	GpuF0MMReg:0x64C4			2-197
DC_LUTA_BLACK_OFFSET_GREEN	GpuF0MMReg:0x64C8			2-197
DC_LUTA_BLACK_OFFSET_RED	GpuF0MMReg:0x64CC			2-197
DC_LUTA_WHITE_OFFSET_BLUE	GpuF0MMReg:0x64D0			2-197
DC_LUTA_WHITE_OFFSET_GREEN	GpuF0MMReg:0x64D4			2-197
DC_LUTA_WHITE_OFFSET_RED	GpuF0MMReg:0x64D8			2-197
D1OVL_RT_SKEWCOMMAND	GpuF0MMReg:0x6500			2-148
D1OVL_RT_SKEWCONTROL	GpuF0MMReg:0x6504			2-148
D1OVL_RT_BAND_POSITION	GpuF0MMReg:0x6508			2-148
D1OVL_RT_PROCEED_COND	GpuF0MMReg:0x650C			2-148
D1OVL_RT_STAT	GpuF0MMReg:0x6510			2-149
D1_MVP_AFR_FLIP_MODE	GpuF0MMReg:0x6514			2-154
D1_MVP_AFR_FLIP_FIFO_CNTL	GpuF0MMReg:0x6518			2-154
D1_MVP_FLIP_LINE_NUM_INSERT	GpuF0MMReg:0x651C			2-154
D2_MVP_AFR_FLIP_MODE	GpuF0MMReg:0x65E8			2-192
D2_MVP_AFR_FLIP_FIFO_CNTL	GpuF0MMReg:0x65EC			2-192
D2_MVP_FLIP_LINE_NUM_INSERT	GpuF0MMReg:0x65F0			2-192
DC_MVP_LB_CONTROL	GpuF0MMReg:0x65F4			2-205
D2CRTC_MVP_INBAND_CNTL_INSERT	GpuF0MMReg:0x6838			2-158
D2CRTC_MVP_INBAND_CNTL_INSERT_TIMER	GpuF0MMReg:0x683C			2-158
D1CRTC_MVP_CRC_CNTL	GpuF0MMReg:0x6840			2-158
D1CRTC_MVP_CRC_RESULT	GpuF0MMReg:0x6844			2-158
D1CRTC_MVP_CRC2_CNTL	GpuF0MMReg:0x6848			2-158
D1CRTC_MVP_CRC2_RESULT	GpuF0MMReg:0x684C			2-159
D1CRTC_MVP_CONTROL3	GpuF0MMReg:0x6850			2-159
D1CRTC_MVP_RECEIVE_CNT_CNTL1	GpuF0MMReg:0x6854			2-159
D1CRTC_MVP_RECEIVE_CNT_CNTL2	GpuF0MMReg:0x6858			2-159
D2GRPH_ENABLE	GpuF0MMReg:0x6900			2-160
D2GRPH_CONTROL	GpuF0MMReg:0x6904			2-160
D2GRPH_LUT_SEL	GpuF0MMReg:0x6908			2-162
D2GRPH_SWAP_CNTL	GpuF0MMReg:0x690C			2-162

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
D2GRPH_PRIMARY_SURFACE_ADDRESS	GpuF0MMReg:0x6910			2-163
D2GRPH_SECONDARY_SURFACE_ADDRESS	GpuF0MMReg:0x6918			2-163
D2GRPH_PITCH	GpuF0MMReg:0x6920			2-163
D2GRPH_SURFACE_OFFSET_X	GpuF0MMReg:0x6924			2-163
D2GRPH_SURFACE_OFFSET_Y	GpuF0MMReg:0x6928			2-163
D2GRPH_X_START	GpuF0MMReg:0x692C			2-164
D2GRPH_Y_START	GpuF0MMReg:0x6930			2-164
D2GRPH_X_END	GpuF0MMReg:0x6934			2-164
D2GRPH_Y_END	GpuF0MMReg:0x6938			2-164
D2COLOR_SPACE_CONVERT	GpuF0MMReg:0x693C			2-185
D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	GpuF0MMReg:0x6940			2-174
D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	GpuF0MMReg:0x6940			2-182
D2GRPH_UPDATE	GpuF0MMReg:0x6944			2-165
D2GRPH_FLIP_CONTROL	GpuF0MMReg:0x6948			2-166
D2GRPH_SURFACE_ADDRESS_INUSE	GpuF0MMReg:0x694C			2-166
D2OVL_MATRIX_TRANSFORM_EN	GpuF0MMReg:0x6A00			2-171
D2OVL_MATRIX_COEF_1_1	GpuF0MMReg:0x6A04			2-171
D2OVL_MATRIX_COEF_1_2	GpuF0MMReg:0x6A08			2-172
D2OVL_MATRIX_COEF_1_3	GpuF0MMReg:0x6A0C			2-172
D2OVL_MATRIX_COEF_1_4	GpuF0MMReg:0x6A10			2-172
D2OVL_MATRIX_COEF_2_1	GpuF0MMReg:0x6A14			2-172
D2OVL_MATRIX_COEF_2_2	GpuF0MMReg:0x6A18			2-172
D2OVL_MATRIX_COEF_2_3	GpuF0MMReg:0x6A1C			2-173
D2OVL_MATRIX_COEF_2_4	GpuF0MMReg:0x6A20			2-173
D2OVL_MATRIX_COEF_3_1	GpuF0MMReg:0x6A24			2-173
D2OVL_MATRIX_COEF_3_2	GpuF0MMReg:0x6A28			2-173
D2OVL_MATRIX_COEF_3_3	GpuF0MMReg:0x6A2C			2-173
D2OVL_MATRIX_COEF_3_4	GpuF0MMReg:0x6A30			2-174
D2OVL_PWL_TRANSFORM_EN	GpuF0MMReg:0x6A80			2-174
D2OVL_PWL_0TOF	GpuF0MMReg:0x6A84			2-174
D2OVL_PWL_10TO1F	GpuF0MMReg:0x6A88			2-174
D2OVL_PWL_20TO3F	GpuF0MMReg:0x6A8C			2-175
D2OVL_PWL_40TO7F	GpuF0MMReg:0x6A90			2-175
D2OVL_PWL_80TOBF	GpuF0MMReg:0x6A94			2-175
D2OVL_PWL_C0TOFF	GpuF0MMReg:0x6A98			2-175
D2OVL_PWL_100TO13F	GpuF0MMReg:0x6A9C			2-175
D2OVL_PWL_140TO17F	GpuF0MMReg:0x6AA0			2-176
D2OVL_PWL_180TO1BF	GpuF0MMReg:0x6AA4			2-176
D2OVL_PWL_1C0TO1FF	GpuF0MMReg:0x6AA8			2-176
D2OVL_PWL_200TO23F	GpuF0MMReg:0x6AAC			2-176
D2OVL_PWL_240TO27F	GpuF0MMReg:0x6AB0			2-176

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
D2OVL_PWL_280TO2BF	GpuF0MMReg:0x6AB4			2-177
D2OVL_PWL_2C0TO2FF	GpuF0MMReg:0x6AB8			2-177
D2OVL_PWL_300TO33F	GpuF0MMReg:0x6ABC			2-177
D2OVL_PWL_340TO37F	GpuF0MMReg:0x6AC0			2-177
D2OVL_PWL_380TO3BF	GpuF0MMReg:0x6AC4			2-177
D2OVL_PWL_3C0TO3FF	GpuF0MMReg:0x6AC8			2-178
D2OVL_KEY_CONTROL	GpuF0MMReg:0x6B00			2-178
D2GRPH_ALPHA	GpuF0MMReg:0x6B04			2-179
D2OVL_ALPHA	GpuF0MMReg:0x6B08			2-179
D2OVL_ALPHA_CONTROL	GpuF0MMReg:0x6B0C			2-179
D2GRPH_KEY_RANGE_RED	GpuF0MMReg:0x6B10			2-180
D2GRPH_KEY_RANGE_GREEN	GpuF0MMReg:0x6B14			2-180
D2GRPH_KEY_RANGE_BLUE	GpuF0MMReg:0x6B18			2-180
D2GRPH_KEY_RANGE_ALPHA	GpuF0MMReg:0x6B1C			2-180
D2OVL_KEY_RANGE_RED_CR	GpuF0MMReg:0x6B20			2-181
D2OVL_KEY_RANGE_GREEN_Y	GpuF0MMReg:0x6B24			2-181
D2OVL_KEY_RANGE_BLUE_CB	GpuF0MMReg:0x6B28			2-181
D2OVL_KEY_ALPHA	GpuF0MMReg:0x6B2C			2-181
D2GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL	GpuF0MMReg:0x6B80			2-182
D2COLOR_MATRIX_COEF_1_1	GpuF0MMReg:0x6B84			2-182
D2COLOR_MATRIX_COEF_1_2	GpuF0MMReg:0x6B88			2-182
D2COLOR_MATRIX_COEF_1_3	GpuF0MMReg:0x6B8C			2-182
D2COLOR_MATRIX_COEF_1_4	GpuF0MMReg:0x6B90			2-183
D2COLOR_MATRIX_COEF_2_1	GpuF0MMReg:0x6B94			2-183
D2COLOR_MATRIX_COEF_2_2	GpuF0MMReg:0x6B98			2-183
D2COLOR_MATRIX_COEF_2_3	GpuF0MMReg:0x6B9C			2-183
D2COLOR_MATRIX_COEF_2_4	GpuF0MMReg:0x6BA0			2-184
D2COLOR_MATRIX_COEF_3_1	GpuF0MMReg:0x6BA4			2-184
D2COLOR_MATRIX_COEF_3_2	GpuF0MMReg:0x6BA8			2-184
D2COLOR_MATRIX_COEF_3_3	GpuF0MMReg:0x6BAC			2-184
D2COLOR_MATRIX_COEF_3_4	GpuF0MMReg:0x6BB0			2-185
D2CUR_CONTROL	GpuF0MMReg:0x6C00			2-187
D2CUR_SURFACE_ADDRESS	GpuF0MMReg:0x6C08			2-188
D2CUR_SIZE	GpuF0MMReg:0x6C10			2-188
D2CUR_POSITION	GpuF0MMReg:0x6C14			2-188
D2CUR_HOT_SPOT	GpuF0MMReg:0x6C18			2-188
D2CUR_COLOR1	GpuF0MMReg:0x6C1C			2-188
D2CUR_COLOR2	GpuF0MMReg:0x6C20			2-189
D2CUR_UPDATE	GpuF0MMReg:0x6C24			2-189
D2ICON_CONTROL	GpuF0MMReg:0x6C40			2-190
D2ICON_SURFACE_ADDRESS	GpuF0MMReg:0x6C48			2-190
D2ICON_SIZE	GpuF0MMReg:0x6C50			2-190
D2ICON_START_POSITION	GpuF0MMReg:0x6C54			2-190
D2ICON_COLOR1	GpuF0MMReg:0x6C58			2-191
D2ICON_COLOR2	GpuF0MMReg:0x6C5C			2-191

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
D2ICON_UPDATE	GpuF0MMReg:0x6C60			2-191
DCP_CRC_CONTROL	GpuF0MMReg:0x6C80			2-200
DCP_CRC_MASK	GpuF0MMReg:0x6C84			2-201
DCP_CRC_P0_CURRENT	GpuF0MMReg:0x6C88			2-201
DCP_CRC_P1_CURRENT	GpuF0MMReg:0x6C8C			2-201
DCP_CRC_P0_LAST	GpuF0MMReg:0x6C90			2-201
DCP_CRC_P1_LAST	GpuF0MMReg:0x6C94			2-201
DCP_TILING_CONFIG	GpuF0MMReg:0x6CA0			2-202
DCP_MULTI_CHIP_CNTL	GpuF0MMReg:0x6CA4			2-203
DMIF_CONTROL	GpuF0MMReg:0x6CB0			2-204
DMIF_STATUS	GpuF0MMReg:0x6CB4			2-204
MCIF_CONTROL	GpuF0MMReg:0x6CB8			2-205
DCP_LB_DATA_GAP_BETWEEN_CHUNK	GpuF0MMReg:0x6CBC			2-202
DC_LUTB_CONTROL	GpuF0MMReg:0x6CC0			2-198
DC_LUTB_BLACK_OFFSET_BLUE	GpuF0MMReg:0x6CC4			2-199
DC_LUTB_BLACK_OFFSET_GREEN	GpuF0MMReg:0x6CC8			2-199
DC_LUTB_BLACK_OFFSET_RED	GpuF0MMReg:0x6CCC			2-200
DC_LUTB_WHITE_OFFSET_BLUE	GpuF0MMReg:0x6CD0			2-200
DC_LUTB_WHITE_OFFSET_GREEN	GpuF0MMReg:0x6CD4			2-200
DC_LUTB_WHITE_OFFSET_RED	GpuF0MMReg:0x6CD8			2-200
D2OVL_RT_SKEWCOMMAND	GpuF0MMReg:0x6D00			2-185
D2OVL_RT_SKEWCONTROL	GpuF0MMReg:0x6D04			2-186
D2OVL_RT_BAND_POSITION	GpuF0MMReg:0x6D08			2-186
D2OVL_RT_PROCEED_COND	GpuF0MMReg:0x6D0C			2-186
D2OVL_RT_STAT	GpuF0MMReg:0x6D10			2-186
DAC_CONTROL	GpuF0MMReg:0x7058	GpuF0MMReg:0x7158		2-103
LVTMA_TRANSMITTER_CONTROL	GpuF0MMReg:0x7F00			2-221
LVTMA_TRANSMITTER_ENABLE	GpuF0MMReg:0x7F04			2-220
LVTMA_LOAD_DETECT	GpuF0MMReg:0x7F08			2-220
LVTMA_MACRO_CONTROL	GpuF0MMReg:0x7F0C			2-221
LVTMA_REG_TEST_OUTPUT	GpuF0MMReg:0x7F10			2-222
LVTMA_TRANSMITTER_DEBUG	GpuF0MMReg:0x7F14			2-222
LVTMA_TRANSMITTER_ADJUST	GpuF0MMReg:0x7F18			2-222
LVTMA_PREEMPHASIS_CONTROL	GpuF0MMReg:0x7F1C			2-222
LVTMA_PWRSEQ_CNTL	GpuF0MMReg:0x7F80			2-218
LVTMA_PWRSEQ_STATE	GpuF0MMReg:0x7F84			2-219
LVTMA_PWRSEQ_REF_DIV	GpuF0MMReg:0x7F88			2-218
LVTMA_PWRSEQ_DELAY1	GpuF0MMReg:0x7F8C			2-218
LVTMA_PWRSEQ_DELAY2	GpuF0MMReg:0x7F90			2-218
LVTMA_BL_MOD_CNTL	GpuF0MMReg:0x7F94			2-219

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
LVTMA_DATA_SYNCHRONIZATION	GpuF0MMReg:0x7F98			2-218
D2OVL_ENABLE	GpuF0MMReg\:0x6980			2-167
D2OVL_CONTROL1	GpuF0MMReg\:0x6984			2-167
D2OVL_CONTROL2	GpuF0MMReg\:0x6988			2-168
D2OVL_SWAP_CNTL	GpuF0MMReg\:0x698C			2-168
D2OVL_SURFACE_ADDRESS	GpuF0MMReg\:0x6990			2-168
D2OVL_PITCH	GpuF0MMReg\:0x6998			2-169
D2OVL_SURFACE_OFFSET_X	GpuF0MMReg\:0x699C			2-169
D2OVL_SURFACE_OFFSET_Y	GpuF0MMReg\:0x69A0			2-169
D2OVL_START	GpuF0MMReg\:0x69A4			2-169
D2OVL_END	GpuF0MMReg\:0x69A8			2-169
D2OVL_UPDATE	GpuF0MMReg\:0x69AC			2-170
D2OVL_SURFACE_ADDRESS_INUSE	GpuF0MMReg\:0x69B0			2-170
D2OVL_DFQ_CONTROL	GpuF0MMReg\:0x69B4			2-171
D2OVL_DFQ_STATUS	GpuF0MMReg\:0x69B8			2-171
NB_HT_CLK_CNTL_RECEIVER_COMP_CNTL	HTIUNBIND:0x0			2-20
NB_HT_CLK_CNTL_RECEIVER_COMP_CNTL	HTIUNBIND:0x0			2-387
NB_HT_TRANS_COMP_CNTL	HTIUNBIND:0x1			2-19
NB_HT_TRANS_COMP_CNTL	HTIUNBIND:0x1			2-388
HTIU_UPSTREAM_CONFIG_9	HTIUNBIND:0x10			2-379
HTIU_UPSTREAM_CONFIG_10	HTIUNBIND:0x11			2-379
HTIU_UPSTREAM_CONFIG_11	HTIUNBIND:0x12			2-379
HTIU_UPSTREAM_CONFIG_12	HTIUNBIND:0x13			2-379
HTIU_UPSTREAM_CONFIG_19	HTIUNBIND:0x14			2-380
Link_State_Control_0	HTIUNBIND:0x15			2-381
Link_State_Control_1	HTIUNBIND:0x16			2-382
Link_State_Control_2	HTIUNBIND:0x17			2-382
Link_State_Control_3	HTIUNBIND:0x18			2-382
Link_State_Control_4	HTIUNBIND:0x19			2-382
Link_State_Control_5	HTIUNBIND:0x1A			2-383
Link_State_Control_6	HTIUNBIND:0x1B			2-383
Link_State_Control_7	HTIUNBIND:0x1C			2-383
Receiver_Control_0	HTIUNBIND:0x1D			2-384
Receiver_Control_1	HTIUNBIND:0x1E			2-385
Receiver_Control_2	HTIUNBIND:0x1F			2-385
Receiver_Control_3	HTIUNBIND:0x20			2-385
HT_BIST_Extended_Control_0	HTIUNBIND:0x21			2-385
HT_BIST_Extended_Control_1	HTIUNBIND:0x22			2-385
Transmiter_Control_0	HTIUNBIND:0x23			2-386
Transmiter_Control_1	HTIUNBIND:0x24			2-386
Transmiter_Control_2	HTIUNBIND:0x25			2-387
HT3PHY_CNTL_1	HTIUNBIND:0x26			2-389
HT3PHY_CNTL_2	HTIUNBIND:0x27			2-389

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
HT3PHY_CNTL_3	HTIUNBIND:0x28			2-390
HT3PHY_CNTL_4	HTIUNBIND:0x29			2-390
HT3PHY_CNTL_5	HTIUNBIND:0x2A			2-391
HT3PHY_CNTL_6	HTIUNBIND:0x2B			2-391
HT3PHY_CNTL_7	HTIUNBIND:0x2C			2-391
NB_HTIU_SPARE	HTIUNBIND:0x2D			2-403
NB_LOWER_TOP_OF_DRAM2	HTIUNBIND:0x30			2-388
NB_UPPER_TOP_OF_DRAM2	HTIUNBIND:0x31			2-388
NB_HTIU_CFG	HTIUNBIND:0x32			2-389
Receiver_Control_4	HTIUNBIND:0x33			2-392
NB_HT_CLMC_I	HTIUNBIND:0x34			2-392
NB_HT_CLMC_II	HTIUNBIND:0x35			2-392
NB_HT_ARB_I	HTIUNBIND:0x36			2-393
NB_HT_ARB_II	HTIUNBIND:0x37			2-393
LS_History0	HTIUNBIND:0x40			2-393
LS_History1	HTIUNBIND:0x41			2-393
LS_History2	HTIUNBIND:0x42			2-394
LS_History3	HTIUNBIND:0x43			2-394
LS_History4	HTIUNBIND:0x44			2-394
LS_History5	HTIUNBIND:0x45			2-394
TX_B_P90PLL_IBias	HTIUNBIND:0x46			2-395
HT3PHY_CNTL_8	HTIUNBIND:0x47			2-403
HT3PHY_CNTL_9	HTIUNBIND:0x48			2-403
HT3PHY_CNTL_10	HTIUNBIND:0x49			2-404
HT3PHY_CNTL_11	HTIUNBIND:0x4A			2-404
HT3PHY_CNTL_12	HTIUNBIND:0x4B			2-405
HT3PHY_CNTL_13	HTIUNBIND:0x4C			2-405
HT3PHY_CNTL_14	HTIUNBIND:0x4D			2-405
HTIU_DEBUG	HTIUNBIND:0x5			2-375
CLMC_I	HTIUNBIND:0x50			2-395
CLMC_ReadBack	HTIUNBIND:0x51			2-395
CLMC_CONTROL_I	HTIUNBIND:0x52			2-395
CLMC_CONTROL_II	HTIUNBIND:0x53			2-395
CLMC_CONTROL_III	HTIUNBIND:0x54			2-396
CLMC_LMM_St1	HTIUNBIND:0x55			2-396
CLMC_LMM_St2	HTIUNBIND:0x56			2-396
CLMC_LMM_St3	HTIUNBIND:0x57			2-396
CLMC_LMM_St4	HTIUNBIND:0x58			2-396
CLMC_LMM_St5	HTIUNBIND:0x59			2-396
CLMC_LMM_St6	HTIUNBIND:0x5A			2-397
CLMC_BWESTM_I	HTIUNBIND:0x5B			2-397
CLMC_BWESTM_ClientBw1	HTIUNBIND:0x5C			2-397
CLMC_BWESTM_ClientBw2	HTIUNBIND:0x5D			2-397
CLMC_BWESTM_ClientBw3	HTIUNBIND:0x5E			2-397
CLMC_BWESTM_ClientBw4	HTIUNBIND:0x5F			2-398

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
HTIU_DOWNSTREAM_CONFIG	HTIUNBIND:0x6			2-375
CLMC_BWESTM_ClientBw5	HTIUNBIND:0x60			2-398
CLMC_BWESTM_ClientBw6	HTIUNBIND:0x61			2-398
CLMC_BWESTM_ClientBw7	HTIUNBIND:0x62			2-398
CLMC_BWESTM_ClientBw8	HTIUNBIND:0x63			2-398
CLMC_BWESTM_ClientBw9	HTIUNBIND:0x64			2-398
CLMC_BWESTM_BwRange1	HTIUNBIND:0x65			2-399
CLMC_BWESTM_BwRange2	HTIUNBIND:0x66			2-399
CLMC_BWESTM_BwRange3	HTIUNBIND:0x67			2-399
CLMC_BWESTM_Timer1	HTIUNBIND:0x68			2-399
CLMC_BWESTM_Timer2	HTIUNBIND:0x69			2-399
CLMC_BWESTM_Timer3	HTIUNBIND:0x6A			2-399
CLMC_CONTROL_IV	HTIUNBIND:0x6B			2-400
CLMC_CONTROL_V	HTIUNBIND:0x6C			2-400
CLMC_CONTROL_VI	HTIUNBIND:0x6D			2-400
HTIU_UPSTREAM_CONFIG_0	HTIUNBIND:0x7			2-376
LMM1	HTIUNBIND:0x70			2-400
LMM2	HTIUNBIND:0x71			2-401
LMM3	HTIUNBIND:0x72			2-401
LMM4	HTIUNBIND:0x73			2-401
LMM5	HTIUNBIND:0x74			2-402
LMM6	HTIUNBIND:0x75			2-402
LMM7	HTIUNBIND:0x76			2-402
HTIU_UPSTREAM_CONFIG_13	HTIUNBIND:0x77			2-379
HTIU_UPSTREAM_CONFIG_1	HTIUNBIND:0x8			2-377
HTIU_UPSTREAM_CONFIG_2	HTIUNBIND:0x9			2-377
HTIU_UPSTREAM_CONFIG_3	HTIUNBIND:0xA			2-377
HTIU_UPSTREAM_CONFIG_4	HTIUNBIND:0xB			2-378
HTIU_UPSTREAM_CONFIG_5	HTIUNBIND:0xC			2-378
HTIU_UPSTREAM_CONFIG_6	HTIUNBIND:0xD			2-378
HTIU_UPSTREAM_CONFIG_7	HTIUNBIND:0xE			2-378
HTIU_UPSTREAM_CONFIG_8	HTIUNBIND:0xF			2-378
NB_VENDOR_ID	nbconfig:0x0			2-1
NB_BAR1_RCRB	nbconfig:0x14			2-5
NB_BAR2_PM2	nbconfig:0x18			2-5
NB_BAR3_PCIEXP_MMCFG	nbconfig:0x1C			2-5
NB_DEVICE_ID	nbconfig:0x2			2-1
NB_BAR3_UPPER_PCIEXP_MMCFG	nbconfig:0x20			2-6
NB_ADAPTER_ID	nbconfig:0x2C			2-6
NB_CAPABILITIES_PTR	nbconfig:0x34			2-6
NB_COMMAND	nbconfig:0x4			2-1
NB_HT_ERROR_RETRY_CAPABILITY	nbconfig:0x40			2-8
NB_HT_ERROR_RETRY_CONTROL_STATUS	nbconfig:0x44			2-9
NB_HT_ERROR_RETRY_COUNT	nbconfig:0x48			2-9

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
NB_PCI_CTRL	nbconfig:0x4C			2-6
NB_ADAPTER_ID_W	nbconfig:0x50			2-8
NB_UNITID_CLUMPING_CAPABILITY	nbconfig:0x54			2-8
NB_UNITID_CLUMPING_SUPPORT	nbconfig:0x58			2-8
NB_UNITID_CLUMPING_ENABLE	nbconfig:0x5C			2-8
NB_STATUS	nbconfig:0x6			2-2
NB_FDHC	nbconfig:0x68			2-16
NB_SMRAM	nbconfig:0x69			2-17
NB_EXSMRAM	nbconfig:0x6A			2-17
NB_PMCR	nbconfig:0x6B			2-18
NB_STRAP_READ_BACK	nbconfig:0x6C			2-18
NB_MC_IND_INDEX	nbconfig:0x70			2-32
NB_MC_IND_DATA	nbconfig:0x74			2-32
SCRATCH_NBCFG	nbconfig:0x78			2-18
NB_IOC_CFG_CNTL	nbconfig:0x7C			2-19
NB_REVISION_ID	nbconfig:0x8			2-3
NB_PCI_ARB	nbconfig:0x84			2-28
NB_CFG_STAT	nbconfig:0x88			2-30
NB_GC_STRAPS	nbconfig:0x8C			2-30
NB_REGPROG_INF	nbconfig:0x9			2-3
NB_TOP_OF_DRAM_SLOT1	nbconfig:0x90			2-31
NB_HT3_CAPABILITY	nbconfig:0x9C			2-9
NB_SUB_CLASS	nbconfig:0xA			2-3
NB_HT3_GLOBAL_LINK_TRAIN	nbconfig:0xA0			2-10
NB_HT3_LINK_TRANSMITTER_CONF_0	nbconfig:0xA4			2-11
NB_HT3_LINK_RECEIVER_CONF_0	nbconfig:0xA8			2-12
NB_HT3_LINK_TRAINING_0	nbconfig:0xAC			2-13
NB_BASE_CODE	nbconfig:0xB			2-3
NB_HT3_RESERVED	nbconfig:0xB0			2-14
NB_HT3_LINK_TRANSMITTER_CONF_1	nbconfig:0xB4			2-14
NB_HT3_LINK_RECEIVER_CONF_1	nbconfig:0xB8			2-15
NB_HT3_LINK_TRAINING_1	nbconfig:0xBC			2-15
NB_CACHE_LINE	nbconfig:0xC			2-3
NB_HT3_BIST_CONTROL	nbconfig:0xC0			2-16
NB_HT_LINK_COMMAND	nbconfig:0xC4			2-20
NB_HT_LINK_CONF_CNTL	nbconfig:0xC8			2-21
NB_HT_LINK_END	nbconfig:0xCC			2-22
NB_LATENCY	nbconfig:0xD			2-4
NB_HT_LINK_FREQ_CAP_A	nbconfig:0xD0			2-22
NB_HT_LINK_FREQ_CAP_B	nbconfig:0xD4			2-22

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
NB_HT_ENUMERATION_SCRATCHPAD	nbconfig:0xD8			2-23
NB_HT_MEMORY_BASE_UPPER	nbconfig:0xDC			2-23
NB_HEADER	nbconfig:0xE			2-4
NB_BIST	nbconfig:0xF			2-4
NB_PERF_CNT_CTRL	nbconfig:0xF4			2-31
NB_HT3_Power_management_Capability	nbconfig:0xF8			2-4
NB_HT3_Power_management_data_port	nbconfig:0xFC			2-4
MC_SYSTEM_STATUS	NBMCIND:0x0			2-223
MC_GENERAL_PURPOSE	NBMCIND:0x1			2-224
MC_FB_LOCATION	NBMCIND:0x10			2-231
K8_FB_LOCATION	NBMCIND:0x11			2-231
MC_MISC_UMA_CNTL	NBMCIND:0x12			2-232
MC_UMA_ADDRESS_SWIZZLE_0	NBMCIND:0x13			2-232
MC_UMA_ADDRESS_SWIZZLE_1	NBMCIND:0x14			2-235
MC_CREDITS_CONTROL	NBMCIND:0x15			2-237
MC_ISOC_CONTROL	NBMCIND:0x16			2-237
MC_ISOC_ARB_CNTL	NBMCIND:0x17			2-238
MC_ISOC_ARB_CNTL2	NBMCIND:0x18			2-238
MC_ISOC_BW_LIM_WINDOW	NBMCIND:0x19			2-238
MC_ISOC_BW_LIM_MAX	NBMCIND:0x1A			2-238
MC_ISOC_BW_LIM_CNTL	NBMCIND:0x1B			2-239
MC_LATENCY_COUNT_CNTL	NBMCIND:0x1C			2-239
MCB_LATENCY_COUNT_EVENT_SP	NBMCIND:0x1D			2-240
MCB_LATENCY_COUNT_EVENT_BIF	NBMCIND:0x1E			2-240
MCB_LATENCY_COUNT_EVENT_UMA	NBMCIND:0x1F			2-240
MC_GENERAL_PURPOSE_2	NBMCIND:0x2			2-225
MCD_LATENCY_COUNT_EVENT_SP	NBMCIND:0x20			2-240
MCD_LATENCY_COUNT_EVENT_BIF	NBMCIND:0x21			2-240
MCD_LATENCY_COUNT_EVENT_UMA	NBMCIND:0x22			2-241
MC_HTIU_GFX_RD_URGENT_CONTROL	NBMCIND:0x23			2-241
MC_HTIU_GFX_WR_URGENT_CONTROL	NBMCIND:0x24			2-241
MC_HTIU_ISOC_URGENT_CONTROL	NBMCIND:0x25			2-241
HT_CLMC_I	NBMCIND:0x29			2-242
HT_CLMC_II	NBMCIND:0x2A			2-242
HT_ARB_I	NBMCIND:0x2B			2-242
HT_ARB_II	NBMCIND:0x2C			2-243
HT_FORCE_I	NBMCIND:0x2D			2-243
HT_FORCE_II	NBMCIND:0x2E			2-243

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
HT_FORCE_III	NBMCIND:0x2F			2-243
MC_GENERAL_PURPOSE_3	NBMCIND:0x3			2-225
CPU_DRAM0_CS0_BASE	NBMCIND:0x30			2-243
CPU_DRAM0_CS1_BASE	NBMCIND:0x31			2-243
CPU_DRAM0_CS2_BASE	NBMCIND:0x32			2-244
CPU_DRAM0_CS3_BASE	NBMCIND:0x33			2-244
CPU_DRAM0_CS4_BASE	NBMCIND:0x34			2-244
CPU_DRAM0_CS5_BASE	NBMCIND:0x35			2-244
CPU_DRAM0_CS6_BASE	NBMCIND:0x36			2-244
CPU_DRAM0_CS7_BASE	NBMCIND:0x37			2-244
CPU_DRAM0_CS01_MASK	NBMCIND:0x38			2-245
CPU_DRAM0_CS23_MASK	NBMCIND:0x39			2-245
CPU_DRAM0_CS45_MASK	NBMCIND:0x3A			2-245
CPU_DRAM0_CS67_MASK	NBMCIND:0x3B			2-245
CPU_DRAM0_BANK_ADDR_MAPPING	NBMCIND:0x3C			2-246
CPU_DRAM1_CS0_BASE	NBMCIND:0x3D			2-247
CPU_DRAM1_CS1_BASE	NBMCIND:0x3E			2-247
CPU_DRAM1_CS2_BASE	NBMCIND:0x3F			2-247
MC_IMP_CTRL_CNTL	NBMCIND:0x4			2-226
CPU_DRAM1_CS3_BASE	NBMCIND:0x40			2-248
CPU_DRAM1_CS4_BASE	NBMCIND:0x41			2-248
CPU_DRAM1_CS5_BASE	NBMCIND:0x42			2-248
CPU_DRAM1_CS6_BASE	NBMCIND:0x43			2-248
CPU_DRAM1_CS7_BASE	NBMCIND:0x44			2-248
CPU_DRAM1_CS01_MASK	NBMCIND:0x45			2-249
CPU_DRAM1_CS23_MASK	NBMCIND:0x46			2-249
CPU_DRAM1_CS45_MASK	NBMCIND:0x47			2-249
CPU_DRAM1_CS67_MASK	NBMCIND:0x48			2-249
CPU_DRAM1_BANK_ADDR_MAPPING	NBMCIND:0x49			2-249
CPU_DRAM_CNTL_SELECT_LO	NBMCIND:0x4A			2-251
CPU_DRAM_CNTL_SELECT_HI	NBMCIND:0x4B			2-251
CPU_DRAM_BASE_SYSTEM_ADDRESS	NBMCIND:0x4C			2-251
CPU_DRAM_HOLE_ADDRESS	NBMCIND:0x4D			2-251
CPU_DRAM_LIMIT_SYSTEM_ADDRESS	NBMCIND:0x4E			2-251
MC_DEBUG	NBMCIND:0x4F			2-251
MC_IMP_CTRL_REF	NBMCIND:0x5			2-226
MC_BIST_CNTL0	NBMCIND:0x5C			2-252
MC_BIST_CNTL1	NBMCIND:0x5D			2-252
MC_BIST_MISMATCH_L	NBMCIND:0x5E			2-253
MC_BIST_MISMATCH_H	NBMCIND:0x5F			2-253
MC_MPLL_CONTROL	NBMCIND:0x6			2-227
MC_BIST_PATTERN0L	NBMCIND:0x60			2-253
MC_BIST_PATTERN0H	NBMCIND:0x61			2-253

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
MC_BIST_PATTERN1L	NBMCIND:0x62			2-254
MC_BIST_PATTERN1H	NBMCIND:0x63			2-254
MC_BIST_PATTERN2L	NBMCIND:0x64			2-254
MC_BIST_PATTERN2H	NBMCIND:0x65			2-254
MC_BIST_PATTERN3L	NBMCIND:0x66			2-254
MC_BIST_PATTERN3H	NBMCIND:0x67			2-254
MC_BIST_PATTERN4L	NBMCIND:0x68			2-254
MC_BIST_PATTERN4H	NBMCIND:0x69			2-255
MC_BIST_PATTERN5L	NBMCIND:0x6A			2-255
MC_BIST_PATTERN5H	NBMCIND:0x6B			2-255
MC_BIST_PATTERN6L	NBMCIND:0x6C			2-255
MC_BIST_PATTERN6H	NBMCIND:0x6D			2-255
MC_BIST_PATTERN7L	NBMCIND:0x6E			2-255
MC_BIST_PATTERN7H	NBMCIND:0x6F			2-255
MC_MPLL_CONTROL2	NBMCIND:0x7			2-227
MC_MPLL_CONTROL3	NBMCIND:0x8			2-228
MC_MPLL_FREQ_CONTROL	NBMCIND:0x9			2-228
MC_MPLL_SEQ_CONTROL	NBMCIND:0xA			2-229
MCA_MEMORY_INIT_MRS	NBMCIND:0xA0			2-256
MCA_MEMORY_INIT_EMRS	NBMCIND:0xA1			2-256
MCA_MEMORY_INIT_EMRS2	NBMCIND:0xA2			2-257
MCA_MEMORY_INIT_EMRS3	NBMCIND:0xA3			2-258
MCA_MEMORY_INIT_SEQUENCE_1	NBMCIND:0xA4			2-259
MCA_MEMORY_INIT_SEQUENCE_2	NBMCIND:0xA5			2-260
MCA_MEMORY_INIT_SEQUENCE_3	NBMCIND:0xA6			2-261
MCA_MEMORY_INIT_SEQUENCE_4	NBMCIND:0xA7			2-262
MCA_TIMING_PARAMETERS_1	NBMCIND:0xA8			2-263
MCA_TIMING_PARAMETERS_2	NBMCIND:0xA9			2-264
MCA_TIMING_PARAMETERS_3	NBMCIND:0xAA			2-264
MCA_TIMING_PARAMETERS_4	NBMCIND:0xAB			2-266
MCA_MEMORY_TYPE	NBMCIND:0xAC			2-267
MC_MPLL_DIV_CONTROL	NBMCIND:0xB			2-229
MCA_SEQ_CONTROL	NBMCIND:0xB0			2-267
MCA_RECEIVING	NBMCIND:0xB1			2-269
MCA_IN_TIMING_DQS_3210	NBMCIND:0xB2			2-270
MCA_DRIVING	NBMCIND:0xB4			2-271
MCA_OUT_TIMING	NBMCIND:0xB5			2-273
MCA_OUT_TIMING_DQ	NBMCIND:0xB6			2-275
MCA_OUT_TIMING_DQS	NBMCIND:0xB7			2-275
MCA_STRENGTH_N	NBMCIND:0xB8			2-276
MCA_STRENGTH_P	NBMCIND:0xB9			2-276
MCA_STRENGTH_STEP	NBMCIND:0xBA			2-277
MCA_STRENGTH_READ_BACK_N	NBMCIND:0xBB			2-279

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
MCA_STRENGTH_READ_BACK_P	NBMCIND:0xBC			2-279
MC_MCLK_CONTROL	NBMCIND:0xC			2-230
MCA_PREBUF_SLEW_N	NBMCIND:0xC1			2-280
MCA_PREBUF_SLEW_P	NBMCIND:0xC2			2-281
MCA_GENERAL_PURPOSE	NBMCIND:0xC3			2-281
MCA_GENERAL_PURPOSE_2	NBMCIND:0xC4			2-282
MCA_OCD_CONTROL	NBMCIND:0xC5			2-284
MCA_DQ_DQS_READ_BACK	NBMCIND:0xC6			2-284
MCA_DQS_CLK_READ_BACK	NBMCIND:0xC7			2-284
MCA_MEMORY_INIT_MRS_PM	NBMCIND:0xC8			2-285
MCA_MEMORY_INIT_EMRS_PM	NBMCIND:0xC9			2-286
MCA_MEMORY_INIT_EMRS2_PM	NBMCIND:0xCA			2-287
MCA_MEMORY_INIT_EMRS3_PM	NBMCIND:0xCB			2-288
MCA_TIMING_PARAMETERS_1_PM	NBMCIND:0xCC			2-289
MCA_TIMING_PARAMETERS_2_PM	NBMCIND:0xCD			2-290
MCA_TIMING_PARAMETERS_3_PM	NBMCIND:0xCE			2-290
MCA_TIMING_PARAMETERS_4_PM	NBMCIND:0xCF			2-292
NB_MEM_CH_CNTL0	NBMCIND:0xD			2-230
MCA_IN_TIMING_DQS_3210_PM	NBMCIND:0xD0			2-293
MCA_OUT_TIMING_DQ_PM	NBMCIND:0xD2			2-294
MCA_OUT_TIMING_DQS_PM	NBMCIND:0xD3			2-294
MCA_MX1X2X_DQ	NBMCIND:0xD6			2-295
MCA_MX1X2X_DQS	NBMCIND:0xD7			2-295
MCA_DLL_MASTER_0	NBMCIND:0xD8			2-296
MCA_DLL_MASTER_1	NBMCIND:0xD9			2-296
NB_MEM_CH_CNTL1	NBMCIND:0xE			2-231
MCA_DLL_SLAVE_RD_0	NBMCIND:0xE0			2-297
MCA_DLL_SLAVE_RD_1	NBMCIND:0xE1			2-297
MCA_DLL_SLAVE_WR_0	NBMCIND:0xE8			2-297
MCA_DLL_SLAVE_WR_1	NBMCIND:0xE9			2-297
NB_MEM_CH_CNTL2	NBMCIND:0xF			2-231
MCA_RESERVED_0	NBMCIND:0xF0			2-298
MCA_RESERVED_1	NBMCIND:0xF1			2-298
MCA_RESERVED_2	NBMCIND:0xF2			2-298
MCA_RESERVED_3	NBMCIND:0xF3			2-298
MCA_RESERVED_4	NBMCIND:0xF4			2-298
MCA_RESERVED_5	NBMCIND:0xF5			2-298
MCA_RESERVED_6	NBMCIND:0xF6			2-298
MCA_RESERVED_7	NBMCIND:0xF7			2-299
NB_CNTL	NBMISCIND:0x0			2-300
NB_IOC_DEBUG	NBMISCIND:0x1			2-300
DFT_CNTL2	NBMISCIND:0x10			2-304
NB_BUS_NUM_CNTL	NBMISCIND:0x11			2-304

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
PCIE_CORE_ARB	NBMISCIND:0x12			2-305
NB_TOM_PCI	NBMISCIND:0x16			2-305
NB_MMIOBASE	NBMISCIND:0x17			2-305
NB_MMIOLIMIT	NBMISCIND:0x18			2-305
DFT_CNTL4	NBMISCIND:0x1D			2-324
NB_BIF_SPARE	NBMISCIND:0x1E			2-305
NB_INTERRUPT_PIN	NBMISCIND:0x1F			2-306
NB_SPARE1	NBMISCIND:0x2			2-300
NB_PROG_DEVICE_REMAP_0	NBMISCIND:0x20			2-306
NB_PROG_DEVICE_REMAP_1	NBMISCIND:0x21			2-306
PCIE_NBCFG_REGA	NBMISCIND:0x22			2-308
PCIE_NBCFG_REGB	NBMISCIND:0x23			2-308
PCIE_NBCFG_REGC	NBMISCIND:0x24			2-308
PCIE_NBCFG_REGD	NBMISCIND:0x25			2-308
PCIE_NBCFG_REGE	NBMISCIND:0x26			2-308
PCIE_NBCFG_REGF	NBMISCIND:0x27			2-308
PCIE_NBCFG_REG10	NBMISCIND:0x28			2-309
PCIE_NBCFG_REG11	NBMISCIND:0x29			2-309
PCIE_NBCFG_REG12	NBMISCIND:0x2A			2-310
PCIE_NBCFG_REG13	NBMISCIND:0x2B			2-310
PCIE_NBCFG_REG14	NBMISCIND:0x2C			2-310
PCIE_NBCFG_REG15	NBMISCIND:0x2D			2-311
PCIE_NBCFG_REG16	NBMISCIND:0x2E			2-311
PCIE_NBCFG_REG17	NBMISCIND:0x2F			2-310
NB_STRAPS_READBACK_MUX	NBMISCIND:0x3			2-300
IOC_LAT_PERF_CNTR_CNTL	NBMISCIND:0x30			2-306
IOC_LAT_PERF_CNTR_OUT	NBMISCIND:0x31			2-306
PCIE_NBCFG_REG2	NBMISCIND:0x32			2-307
PCIE_NBCFG_REG3	NBMISCIND:0x33			2-307
PCIE_NBCFG_REG4	NBMISCIND:0x34			2-307
PCIE_NBCFG_REG5	NBMISCIND:0x35			2-307
PCIE_NBCFG_REG6	NBMISCIND:0x36			2-307
PCIE_NBCFG_REG7	NBMISCIND:0x37			2-307
PCIE_NBCFG_REG8	NBMISCIND:0x38			2-307
PCIE_NBCFG_REG9	NBMISCIND:0x39			2-308
NB_BROADCAST_BASE_LO	NBMISCIND:0x3A			2-312
NB_BROADCAST_BASE_HI	NBMISCIND:0x3B			2-312
NB_BROADCAST_CNTL	NBMISCIND:0x3C			2-312
NB_APIC_P2P_CNTL	NBMISCIND:0x3D			2-312
NB_APIC_P2P_RANGE_0	NBMISCIND:0x3E			2-313
NB_APIC_P2P_RANGE_1	NBMISCIND:0x3F			2-313
NB_STRAPS_READBACK_DATA	NBMISCIND:0x4			2-301
GPIO_PAD	NBMISCIND:0x40			2-313
GPIO_PAD_CNTL_PU_PD	NBMISCIND:0x41			2-314
GPIO_PAD_SCHMEM_OE	NBMISCIND:0x42			2-314
GPIO_PAD_SP_SN	NBMISCIND:0x43			2-315

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
DFT_VIP_IO_GPIO	NBMISCIND:0x44			2-315
DFT_VIP_IO_GPIO_OR	NBMISCIND:0x45			2-315
IOC_JTAG_CNTL	NBMISCIND:0x47			2-324
PCIE_GFX_P2P_CONTROL	NBMISCIND:0x48			2-324
PCIE_GFX_P2P_ARBITRER_CONTROL	NBMISCIND:0x49			2-324
GPIO_SDVO_HPD	NBMISCIND:0x4A			2-325
DFT_CNTL0	NBMISCIND:0x5			2-301
IOC_PCIE_D2_CSR_Count	NBMISCIND:0x50			2-23
IOC_PCIE_D2_CSR_Count	NBMISCIND:0x50			2-315
IOC_PCIE_D2_CNTL	NBMISCIND:0x51			2-23
IOC_PCIE_D2_CNTL	NBMISCIND:0x51			2-315
IOC_PCIE_D3_CSR_Count	NBMISCIND:0x52			2-24
IOC_PCIE_D3_CSR_Count	NBMISCIND:0x52			2-316
IOC_PCIE_D3_CNTL	NBMISCIND:0x53			2-24
IOC_PCIE_D3_CNTL	NBMISCIND:0x53			2-316
IOC_PCIE_D4_CSR_Count	NBMISCIND:0x54			2-24
IOC_PCIE_D4_CSR_Count	NBMISCIND:0x54			2-316
IOC_PCIE_D4_CNTL	NBMISCIND:0x55			2-24
IOC_PCIE_D4_CNTL	NBMISCIND:0x55			2-316
IOC_PCIE_D5_CSR_Count	NBMISCIND:0x56			2-25
IOC_PCIE_D5_CSR_Count	NBMISCIND:0x56			2-317
IOC_PCIE_D5_CNTL	NBMISCIND:0x57			2-25
IOC_PCIE_D5_CNTL	NBMISCIND:0x57			2-317
IOC_PCIE_D6_CSR_Count	NBMISCIND:0x58			2-25
IOC_PCIE_D6_CSR_Count	NBMISCIND:0x58			2-317
IOC_PCIE_D6_CNTL	NBMISCIND:0x59			2-25
IOC_PCIE_D6_CNTL	NBMISCIND:0x59			2-317
IOC_PCIE_D7_CSR_Count	NBMISCIND:0x5A			2-26
IOC_PCIE_D7_CSR_Count	NBMISCIND:0x5A			2-318
IOC_PCIE_D7_CNTL	NBMISCIND:0x5B			2-26
IOC_PCIE_D7_CNTL	NBMISCIND:0x5B			2-318
IOC_PCIE_D9_CSR_Count	NBMISCIND:0x5C			2-26
IOC_PCIE_D9_CSR_Count	NBMISCIND:0x5C			2-318
IOC_PCIE_D9_CNTL	NBMISCIND:0x5D			2-26
IOC_PCIE_D9_CNTL	NBMISCIND:0x5D			2-318
IOC_PCIE_D10_CSR_Count	NBMISCIND:0x5E			2-27
IOC_PCIE_D10_CSR_Count	NBMISCIND:0x5E			2-319
IOC_PCIE_D10_CNTL	NBMISCIND:0x5F			2-27
IOC_PCIE_D10_CNTL	NBMISCIND:0x5F			2-319
DFT_CNTL1	NBMISCIND:0x6			2-301
IOC_PCIE_D11_CSR_Count	NBMISCIND:0x60			2-27
IOC_PCIE_D11_CSR_Count	NBMISCIND:0x60			2-319
IOC_PCIE_D11_CNTL	NBMISCIND:0x61			2-27
IOC_PCIE_D11_CNTL	NBMISCIND:0x61			2-319
IOC_PCIE_D12_CSR_Count	NBMISCIND:0x62			2-28

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
IOC_PCIE_D12_CSR_Count	NBMISCIND:0x62			2-320
IOC_PCIE_D12_CNTL	NBMISCIND:0x63			2-28
IOC_PCIE_D12_CNTL	NBMISCIND:0x63			2-320
StrapsOutputMux_4	NBMISCIND:0x64			2-321
StrapsOutputMux_5	NBMISCIND:0x65			2-321
StrapsOutputMux_6	NBMISCIND:0x66			2-321
StrapsOutputMux_7	NBMISCIND:0x67			2-321
StrapsOutputMux_8	NBMISCIND:0x68			2-321
StrapsOutputMux_9	NBMISCIND:0x69			2-322
StrapsOutputMux_A	NBMISCIND:0x6A			2-322
StrapsOutputMux_B	NBMISCIND:0x6B			2-322
StrapsOutputMux_C	NBMISCIND:0x6C			2-322
StrapsOutputMux_D	NBMISCIND:0x6D			2-322
StrapsOutputMux_E	NBMISCIND:0x6E			2-322
StrapsOutputMux_F	NBMISCIND:0x6F			2-322
PCIE_PDNB_CNTL	NBMISCIND:0x7			2-301
StrapsOutputMux_0	NBMISCIND:0x70			2-320
StrapsOutputMux_1	NBMISCIND:0x71			2-320
StrapsOutputMux_2	NBMISCIND:0x72			2-321
StrapsOutputMux_3	NBMISCIND:0x73			2-321
SCRATCH_4	NBMISCIND:0x74			2-323
SCRATCH_5	NBMISCIND:0x75			2-323
SCRATCH_6	NBMISCIND:0x76			2-323
SCRATCH_7	NBMISCIND:0x77			2-323
SCRATCH_8	NBMISCIND:0x78			2-323
SCRATCH_9	NBMISCIND:0x79			2-323
DFT_CNTL3	NBMISCIND:0x7B			2-323
PCIE_LINK_CFG	NBMISCIND:0x8			2-302
IOC_DMA_ARBITER	NBMISCIND:0x9			2-303
IOC_PCIE_CSR_Count	NBMISCIND:0xA			2-303
IOC_PCIE_CNTL	NBMISCIND:0xB			2-303
IOC_P2P_CNTL	NBMISCIND:0xC			2-304
IOCIsocMapAddr_LO	NBMISCIND:0xE			2-304
IOCIsocMapAddr_HI	NBMISCIND:0xF			2-304
NB_PCIE_VENDOR_ID	pcieConfigDev[12:2]:0x0			2-33
NB_PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST	pcieConfigDev[12:2]:0x100			2-48
NB_PCIE_VENDOR_SPECIFIC_HDR	pcieConfigDev[12:2]:0x104			2-49
NB_PCIE_VENDOR_SPECIFIC1	pcieConfigDev[12:2]:0x108			2-49
NB_PCIE_VENDOR_SPECIFIC2	pcieConfigDev[12:2]:0x10C			2-49
NB_PCIE_VC_ENH_CAP_LIST	pcieConfigDev[12:2]:0x110			2-49
NB_PCIE_PORT_VC_CAP_REG1	pcieConfigDev[12:2]:0x114			2-49
NB_PCIE_PORT_VC_CAP_REG2	pcieConfigDev[12:2]:0x118			2-50
NB_PCIE_PORT_VC_CNTL	pcieConfigDev[12:2]:0x11C			2-50
NB_PCIE_PORT_VC_STATUS	pcieConfigDev[12:2]:0x11E			2-50
NB_PCIE_VC0_RESOURCE_CAP	pcieConfigDev[12:2]:0x120			2-50

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
NB_PCIE_VC0_RESOURCE_CNTL	pcieConfigDev[12:2]:0x124			2-50
NB_PCIE_VC0_RESOURCE_STATUS	pcieConfigDev[12:2]:0x12A			2-51
NB_PCIE_VC1_RESOURCE_CAP	pcieConfigDev[12:2]:0x12C			2-51
NB_PCIE_VC1_RESOURCE_CNTL	pcieConfigDev[12:2]:0x130			2-51
NB_PCIE_VC1_RESOURCE_STATUS	pcieConfigDev[12:2]:0x136			2-51
NB_PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST	pcieConfigDev[12:2]:0x140			2-52
NB_PCIE_DEV_SERIAL_NUM_DW1	pcieConfigDev[12:2]:0x144			2-52
NB_PCIE_DEV_SERIAL_NUM_DW2	pcieConfigDev[12:2]:0x148			2-52
NB_PCIE_ADV_ERR_RPT_ENH_CAP_LIST	pcieConfigDev[12:2]:0x150			2-52
NB_PCIE_UNCORR_ERR_STATUS	pcieConfigDev[12:2]:0x154			2-52
NB_PCIE_UNCORR_ERR_MASK	pcieConfigDev[12:2]:0x158			2-53
NB_PCIE_UNCORR_ERR_SEVERITY	pcieConfigDev[12:2]:0x15C			2-53
NB_PCIE_CORR_ERR_STATUS	pcieConfigDev[12:2]:0x160			2-53
NB_PCIE_CORR_ERR_MASK	pcieConfigDev[12:2]:0x164			2-54
NB_PCIE_ADV_ERR_CAP_CNTL	pcieConfigDev[12:2]:0x168			2-54
NB_PCIE_HDR_LOG0	pcieConfigDev[12:2]:0x16C			2-54
NB_PCIE_HDR_LOG1	pcieConfigDev[12:2]:0x170			2-54
NB_PCIE_HDR_LOG2	pcieConfigDev[12:2]:0x174			2-54
NB_PCIE_HDR_LOG3	pcieConfigDev[12:2]:0x178			2-55
NB_PCIE_ROOT_ERR_CMD	pcieConfigDev[12:2]:0x17C			2-55
NB_PCIE_SUB_BUS_NUMBER_LATENCY	pcieConfigDev[12:2]:0x18			2-36
NB_PCIE_ROOT_ERR_STATUS	pcieConfigDev[12:2]:0x180			2-55
NB_PCIE_ERR_SRC_ID	pcieConfigDev[12:2]:0x184			2-55
NB_PCIE_IO_BASE_LIMIT	pcieConfigDev[12:2]:0x1C			2-36
NB_PCIE_SECONDARY_STATUS	pcieConfigDev[12:2]:0x1E			2-37
NB_PCIE_DEVICE_ID	pcieConfigDev[12:2]:0x2			2-33
NB_PCIE_MEM_BASE_LIMIT	pcieConfigDev[12:2]:0x20			2-37
NB_PCIE_PREF_BASE_LIMIT	pcieConfigDev[12:2]:0x24			2-37
NB_PCIE_PREF_BASE_UPPER	pcieConfigDev[12:2]:0x28			2-38
NB_PCIE_PREF_LIMIT_UPPER	pcieConfigDev[12:2]:0x2C			2-38
NB_PCIE_IO_BASE_LIMIT_HI	pcieConfigDev[12:2]:0x30			2-38
NB_PCIE_CAP_PTR	pcieConfigDev[12:2]:0x34			2-38
NB_PCIE_INTERRUPT_LINE	pcieConfigDev[12:2]:0x3C			2-39
NB_PCIE_INTERRUPT_PIN	pcieConfigDev[12:2]:0x3D			2-39
NB_PCIE_IRQ_BRIDGE_CNTL	pcieConfigDev[12:2]:0x3E			2-38
NB_PCIE_COMMAND	pcieConfigDev[12:2]:0x4			2-34
NB_PCIE_PMI_CAP_LIST	pcieConfigDev[12:2]:0x50			2-39
NB_PCIE_PMI_CAP	pcieConfigDev[12:2]:0x52			2-39
NB_PCIE_PMI_STATUS_CNTL	pcieConfigDev[12:2]:0x54			2-40
NB_PCIE_CAP_LIST	pcieConfigDev[12:2]:0x58			2-40

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
NB_PCIE_CAP	pcieConfigDev[12:2]:0x5A			2-40
NB_PCIE_DEVICE_CAP	pcieConfigDev[12:2]:0x5C			2-40
NB_PCIE_STATUS	pcieConfigDev[12:2]:0x6			2-34
NB_PCIE_DEVICE_CNTL	pcieConfigDev[12:2]:0x60			2-41
NB_PCIE_DEVICE_STATUS	pcieConfigDev[12:2]:0x62			2-41
NB_PCIE_LINK_CAP	pcieConfigDev[12:2]:0x64			2-42
NB_PCIE_LINK_CNTL	pcieConfigDev[12:2]:0x68			2-42
NB_PCIE_LINK_STATUS	pcieConfigDev[12:2]:0x6A			2-43
NB_PCIE_SLOT_CAP	pcieConfigDev[12:2]:0x6C			2-43
NB_PCIE_SLOT_CNTL	pcieConfigDev[12:2]:0x70			2-43
NB_PCIE_SLOT_STATUS	pcieConfigDev[12:2]:0x72			2-44
NB_PCIE_ROOT_CNTL	pcieConfigDev[12:2]:0x74			2-44
NB_PCIE_ROOT_CAP	pcieConfigDev[12:2]:0x76			2-44
NB_PCIE_ROOT_STATUS	pcieConfigDev[12:2]:0x78			2-44
NB_PCIE_DEVICE_CAP2	pcieConfigDev[12:2]:0x7C			2-45
NB_PCIE_REVISION_ID	pcieConfigDev[12:2]:0x8			2-35
NB_PCIE_DEVICE_CNTL2	pcieConfigDev[12:2]:0x80			2-45
NB_PCIE_DEVICE_STATUS2	pcieConfigDev[12:2]:0x82			2-45
NB_PCIE_LINK_CAP2	pcieConfigDev[12:2]:0x84			2-45
NB_PCIE_LINK_CNTL2	pcieConfigDev[12:2]:0x88			2-45
NB_PCIE_LINK_STATUS2	pcieConfigDev[12:2]:0x8A			2-46
NB_PCIE_SLOT_CAP2	pcieConfigDev[12:2]:0x8C			2-46
NB_PCIE_PROG_INTERFACE	pcieConfigDev[12:2]:0x9			2-35
NB_PCIE_SLOT_CNTL2	pcieConfigDev[12:2]:0x90			2-46
NB_PCIE_SLOT_STATUS2	pcieConfigDev[12:2]:0x92			2-46
NB_PCIE_SUB_CLASS	pcieConfigDev[12:2]:0xA			2-35
NB_PCIE_MSI_CAP_LIST	pcieConfigDev[12:2]:0xA0			2-46
NB_PCIE_MSI_MSG_CNTL	pcieConfigDev[12:2]:0xA2			2-47
NB_PCIE_MSI_MSG_ADDR_LO	pcieConfigDev[12:2]:0xA4			2-47
NB_PCIE_MSI_MSG_ADDR_HI	pcieConfigDev[12:2]:0xA8			2-47
NB_PCIE_MSI_MSG_DATA	pcieConfigDev[12:2]:0xA8			2-48
NB_PCIE_MSI_MSG_DATA_64	pcieConfigDev[12:2]:0xAC			2-47
NB_PCIE_BASE_CLASS	pcieConfigDev[12:2]:0xB			2-35
NB_PCIE_SSID_CAP_LIST	pcieConfigDev[12:2]:0xB0			2-48
NB_PCIE_SSID_ID	pcieConfigDev[12:2]:0xB4			2-48
NB_PCIE_MSI_MAP_CAP_LIST	pcieConfigDev[12:2]:0xB8			2-48
NB_PCIE_CACHE_LINE	pcieConfigDev[12:2]:0xC			2-35
NB_PCIE_LATENCY	pcieConfigDev[12:2]:0xD			2-36
NB_PCIE_HEADER	pcieConfigDev[12:2]:0xE			2-36
PCIE_PORT_INDEX	pcieConfigDev[12:2]:0xE0			2-33
PCIE_PORT_DATA	pcieConfigDev[12:2]:0xE4			2-33
NB_PCIE_BIST	pcieConfigDev[12:2]:0xF			2-36
PCIE_RESERVED	PCIEIND:0x0			2-326
PCIE_SCRATCH	PCIEIND:0x1			2-326
PCIE_CNTL	PCIEIND:0x10			2-327
PCIE_CONFIG_CNTL	PCIEIND:0x11			2-327

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
PCIE_DEBUG_CNTL	PCIEIND:0x12			2-328
PCIE_RTR_CPL_TIMEOUT_STATUS	PCIEIND:0x13			2-328
PCIE_CI_SLV_R_RTR_TIMEOUT_CNTL	PCIEIND:0x14			2-329
PCIE_CI_MST_R_RTR_TIMEOUT_CNTL	PCIEIND:0x15			2-329
PCIE_CI_MST_C_RTR_TIMEOUT_CNTL	PCIEIND:0x16			2-329
PCIE_REG_R_RTR_TIMEOUT_CNTL	PCIEIND:0x17			2-329
PCIE_TX_SLVCPL_TIMEOUT_CNTL	PCIEIND:0x18			2-330
PCIE_TX_SLVCPL_NS_TIMEOUT_CNTL	PCIEIND:0x19			2-330
PCIE_CNTL2	PCIEIND:0x1C			2-330
PCIE_HW_DEBUG	PCIEIND:0x2			2-326
PCIE_CI_CNTL	PCIEIND:0x20			2-331
PCIE_BUS_CNTL	PCIEIND:0x21			2-331
PCIE_LC_STATE6	PCIEIND:0x22			2-332
PCIE_LC_STATE7	PCIEIND:0x23			2-332
PCIE_LC_STATE8	PCIEIND:0x24			2-332
PCIE_LC_STATE9	PCIEIND:0x25			2-332
PCIE_LC_STATE10	PCIEIND:0x26			2-332
PCIE_LC_STATE11	PCIEIND:0x27			2-333
PCIE_LC_STATUS1	PCIEIND:0x28			2-333
PCIE_LC_STATUS2	PCIEIND:0x29			2-333
PCIE_WPR_CNTL	PCIEIND:0x30			2-333
PCIE_RX_LAST_TLP0	PCIEIND:0x31			2-333
PCIE_RX_LAST_TLP1	PCIEIND:0x32			2-334
PCIE_RX_LAST_TLP2	PCIEIND:0x33			2-334
PCIE_RX_LAST_TLP3	PCIEIND:0x34			2-334
PCIE_TX_LAST_TLP0	PCIEIND:0x35			2-334
PCIE_TX_LAST_TLP1	PCIEIND:0x36			2-334
PCIE_TX_LAST_TLP2	PCIEIND:0x37			2-334
PCIE_TX_LAST_TLP3	PCIEIND:0x38			2-334
PCIE_I2C_DEBUG_BUS	PCIEIND:0x39			2-335
PCIE_I2C_REG_ADDR_EXPAND	PCIEIND:0x3A			2-335
PCIE_I2C_REG_DATA	PCIEIND:0x3B			2-335
PCIE_CFG_CNTL	PCIEIND:0x3C			2-335
PCIE_P_CNTL	PCIEIND:0x40			2-336
PCIE_P_BUF_STATUS	PCIEIND:0x41			2-337
PCIE_P_DECODER_STATUS	PCIEIND:0x42			2-338
PCIE_P_MISC_DEBUG_STATUS	PCIEIND:0x43			2-339
PCIE_P_PLL_CNTL	PCIEIND:0x44			2-341
PCIE_P_RCVR_DEBUG_CNTL	PCIEIND:0x45			2-341
PCIE_P_SYMSYNC_CTL	PCIEIND:0x46			2-343

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
PCIE_P_RXP_ERR_RETRAIN_CTL	PCIEIND:0x47			2-343
PCIE_PI_RCVL0S_FTS_DET	PCIEIND:0x50			2-343
PCIE_P_IMP_CNTL_STRENGTH	PCIEIND:0x60			2-344
PCIE_P_IMP_CNTL_UPDATE	PCIEIND:0x61			2-344
PCIE_P_STR_CNTL_UPDATE	PCIEIND:0x62			2-344
PCIE_P_PAD_MISC_CNTL	PCIEIND:0x63			2-345
PCIE_P_PAD_FORCE_EN	PCIEIND:0x64			2-345
PCIE_P_PAD_FORCE_DIS	PCIEIND:0x65			2-345
PCIE_PERF_LATENCY_CNTL	PCIEIND:0x70			2-346
PCIE_PERF_LATENCY_REQ_ID	PCIEIND:0x71			2-346
PCIE_PERF_LATENCY_TAG	PCIEIND:0x72			2-347
PCIE_PERF_LATENCY_THRESHOLD	PCIEIND:0x73			2-347
PCIE_PERF_LATENCY_MAX	PCIEIND:0x74			2-347
PCIE_PERF_LATENCY_TIMER_LO	PCIEIND:0x75			2-347
PCIE_PERF_LATENCY_TIMER_HI	PCIEIND:0x76			2-347
PCIE_PERF_LATENCY_COUNTER0	PCIEIND:0x77			2-347
PCIE_PERF_LATENCY_COUNTER1	PCIEIND:0x78			2-347
PCIE_PERF_MAS_ACC_START_LO	PCIEIND:0xA0			2-348
PCIE_PERF_MAS_ACC_END_LO	PCIEIND:0xA1			2-348
PCIE_PERF_MAS_ACC_START_END_HI	PCIEIND:0xA2			2-348
PCIE_PERF_SLV_ACC_LO	PCIEIND:0xA3			2-348
PCIE_PERF_SLV_ACC_HI	PCIEIND:0xA4			2-348
PCIE_STRAP_MISC	PCIEIND:0xC0			2-348
PCIE_STRAP_MISC2	PCIEIND:0xC1			2-349
PCIE_STRAP_PI	PCIEIND:0xC2			2-349
PCIE_B_P90_CNTL	PCIEIND:0xC3			2-349
PCIE_STRAP_I2C_BD	PCIEIND:0xC4			2-349
PCIE_P90RX_PRBS10_CNTL	PCIEIND:0xC6			2-350
PCIE_P90_BRX_PRBS10_ER	PCIEIND:0xC7			2-350
PCIE_PRBS_CLR	PCIEIND:0xC8			2-350
PCIE_PRBS_STATUS1	PCIEIND:0xC9			2-350
PCIE_PRBS_STATUS2	PCIEIND:0xCA			2-350
PCIE_PRBS_FREERUN	PCIEIND:0xCB			2-350
PCIE_PRBS_MISC	PCIEIND:0xCC			2-351
PCIE_PRBS_USER_PATTERN	PCIEIND:0xCD			2-351
PCIE_PRBS_LO_BITCNT	PCIEIND:0xCE			2-351
PCIE_PRBS_HI_BITCNT	PCIEIND:0xCF			2-351
PCIE_PRBS_ERRCNT_0	PCIEIND:0xD0			2-351
PCIE_PRBS_ERRCNT_1	PCIEIND:0xD1			2-352
PCIE_PRBS_ERRCNT_2	PCIEIND:0xD2			2-352
PCIE_PRBS_ERRCNT_3	PCIEIND:0xD3			2-352

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
PCIE_PRBS_ERRCNT_4	PCIEIND:0xD4			2-352
PCIE_PRBS_ERRCNT_5	PCIEIND:0xD5			2-352
PCIE_PRBS_ERRCNT_6	PCIEIND:0xD6			2-352
PCIE_PRBS_ERRCNT_7	PCIEIND:0xD7			2-352
PCIE_PRBS_ERRCNT_8	PCIEIND:0xD8			2-353
PCIE_PRBS_ERRCNT_9	PCIEIND:0xD9			2-353
PCIE_PRBS_ERRCNT_10	PCIEIND:0xDA			2-353
PCIE_PRBS_ERRCNT_11	PCIEIND:0xDB			2-353
PCIE_PRBS_ERRCNT_12	PCIEIND:0xDC			2-353
PCIE_PRBS_ERRCNT_13	PCIEIND:0xDD			2-353
PCIE_PRBS_ERRCNT_14	PCIEIND:0xDE			2-353
PCIE_PRBS_ERRCNT_15	PCIEIND:0xDF			2-354
PCIE_RX_NUM_NACK	PCIEIND:0xE			2-326
PCIE_P_DECODE_ERR_CNTL	PCIEIND:0xEF			2-354
PCIE_RX_NUM_NACK_GENERATED	PCIEIND:0xF			2-326
PCIE_P_DECODE_ERR_CNT_0	PCIEIND:0xF0			2-354
PCIE_P_DECODE_ERR_CNT_1	PCIEIND:0xF1			2-354
PCIE_P_DECODE_ERR_CNT_2	PCIEIND:0xF2			2-354
PCIE_P_DECODE_ERR_CNT_3	PCIEIND:0xF3			2-354
PCIE_P_DECODE_ERR_CNT_4	PCIEIND:0xF4			2-354
PCIE_P_DECODE_ERR_CNT_5	PCIEIND:0xF5			2-355
PCIE_P_DECODE_ERR_CNT_6	PCIEIND:0xF6			2-355
PCIE_P_DECODE_ERR_CNT_7	PCIEIND:0xF7			2-355
PCIE_P_DECODE_ERR_CNT_8	PCIEIND:0xF8			2-355
PCIE_P_DECODE_ERR_CNT_9	PCIEIND:0xF9			2-355
PCIE_P_DECODE_ERR_CNT_10	PCIEIND:0xFA			2-355
PCIE_P_DECODE_ERR_CNT_11	PCIEIND:0xFB			2-356
PCIE_P_DECODE_ERR_CNT_12	PCIEIND:0xFC			2-356
PCIE_P_DECODE_ERR_CNT_13	PCIEIND:0xFD			2-356
PCIE_P_DECODE_ERR_CNT_14	PCIEIND:0xFE			2-356
PCIE_P_DECODE_ERR_CNT_15	PCIEIND:0xFF			2-356
PCIEP_RESERVED	PCIEIND_P:0x0			2-356
PCIEP_SCRATCH	PCIEIND_P:0x1			2-356
PCIEP_PORT_CNTL	PCIEIND_P:0x10			2-357
PCIEP_HW_DEBUG	PCIEIND_P:0x2			2-357
PCIE_TX_CNTL	PCIEIND_P:0x20			2-358
PCIE_TX_REQUESTER_ID	PCIEIND_P:0x21			2-358
PCIE_TX_VENDOR_SPECIFIC	PCIEIND_P:0x22			2-359
PCIE_TX_REQUEST_NUM_CNTL	PCIEIND_P:0x23			2-359
PCIE_TX_SEQ	PCIEIND_P:0x24			2-359
PCIE_TX_REPLAY	PCIEIND_P:0x25			2-359
PCIE_TX_ACK_LATENCY_LIMIT	PCIEIND_P:0x26			2-359
PCIE_TX_CREDITS_ADVT_P	PCIEIND_P:0x30			2-360
PCIE_TX_CREDITS_ADVT_NP	PCIEIND_P:0x31			2-360
PCIE_TX_CREDITS_ADVT_CPL	PCIEIND_P:0x32			2-360

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
PCIE_TX_CREDITS_INIT_P	PCIEIND_P:0x33			2-360
PCIE_TX_CREDITS_INIT_NP	PCIEIND_P:0x34			2-360
PCIE_TX_CREDITS_INIT_CPL	PCIEIND_P:0x35			2-360
PCIE_TX_CREDITS_STATUS	PCIEIND_P:0x36			2-361
PCIE_P_PORT_LANE_STATUS	PCIEIND_P:0x50			2-361
PCIE_FC_P	PCIEIND_P:0x60			2-361
PCIE_FC_NP	PCIEIND_P:0x61			2-361
PCIE_FC_CPL	PCIEIND_P:0x62			2-362
PCIE_ERR_CNTL	PCIEIND_P:0x6A			2-362
PCIE_RX_CNTL	PCIEIND_P:0x70			2-362
PCIE_RX_LASTACK_SEQNUM	PCIEIND_P:0x71			2-363
PCIE_RX_VENDOR_SPECIFIC	PCIEIND_P:0x72			2-363
PCIE_RX_CREDITS_ALLOCATED_P	PCIEIND_P:0x80			2-363
PCIE_RX_CREDITS_ALLOCATED_NP	PCIEIND_P:0x81			2-363
PCIE_RX_CREDITS_ALLOCATED_CPL	PCIEIND_P:0x82			2-363
PCIE_RX_CREDITS_RECEIVED_P	PCIEIND_P:0x83			2-363
PCIE_RX_CREDITS_RECEIVED_NP	PCIEIND_P:0x84			2-364
PCIE_RX_CREDITS_RECEIVED_CPL	PCIEIND_P:0x85			2-364
PCIE_LC_CNTL	PCIEIND_P:0xA0			2-364
PCIE_LC_TRAINING_CNTL	PCIEIND_P:0xA1			2-367
PCIE_LC_LINK_WIDTH_CNTL	PCIEIND_P:0xA2			2-369
PCIE_LC_N_FTS_CNTL	PCIEIND_P:0xA3			2-369
PCIE_LC_SPEED_CNTL	PCIEIND_P:0xA4			2-370
PCIE_LC_STATE0	PCIEIND_P:0xA5			2-372
PCIE_LC_STATE1	PCIEIND_P:0xA6			2-372
PCIE_LC_STATE2	PCIEIND_P:0xA7			2-372
PCIE_LC_STATE3	PCIEIND_P:0xA8			2-373
PCIE_LC_STATE4	PCIEIND_P:0xA9			2-373
PCIE_LC_STATE5	PCIEIND_P:0xAA			2-373
PCIE_LC_CNTL2	PCIEIND_P:0xB1			2-365
PCIE_LC_BW_CHANGE_CNTL	PCIEIND_P:0xB2			2-367
PCIE_LC_CDR_CNTL	PCIEIND_P:0xB3			2-372
PCIE_LC_LANE_CNTL	PCIEIND_P:0xB4			2-372
PCIE_LC_CNTL3	PCIEIND_P:0xB5			2-366
PCIEP_STRAP_LC	PCIEIND_P:0xC0			2-373
PCIEP_STRAP_MISC	PCIEIND_P:0xC1			2-374
ATTR00	VGAATTRIND:0x0			2-116
ATTR01	VGAATTRIND:0x1			2-116
ATTR10	VGAATTRIND:0x10			2-120
ATTR11	VGAATTRIND:0x11			2-120
ATTR12	VGAATTRIND:0x12			2-120
ATTR13	VGAATTRIND:0x13			2-121

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
ATTR14	VGAATTRIND:0x14			2-121
ATTR02	VGAATTRIND:0x2			2-117
ATTR03	VGAATTRIND:0x3			2-117
ATTR04	VGAATTRIND:0x4			2-117
ATTR05	VGAATTRIND:0x5			2-117
ATTR06	VGAATTRIND:0x6			2-117
ATTR07	VGAATTRIND:0x7			2-118
ATTR08	VGAATTRIND:0x8			2-118
ATTR09	VGAATTRIND:0x9			2-118
ATTR0A	VGAATTRIND:0xA			2-118
ATTR0B	VGAATTRIND:0xB			2-118
ATTR0C	VGAATTRIND:0xC			2-119
ATTR0D	VGAATTRIND:0xD			2-119
ATTR0E	VGAATTRIND:0xE			2-119
ATTR0F	VGAATTRIND:0xF			2-119
CRT00	VGACRTIND:0x0			2-107
CRT01	VGACRTIND:0x1			2-107
CRT10	VGACRTIND:0x10			2-111
CRT11	VGACRTIND:0x11			2-111
CRT12	VGACRTIND:0x12			2-111
CRT13	VGACRTIND:0x13			2-112
CRT14	VGACRTIND:0x14			2-112
CRT15	VGACRTIND:0x15			2-112
CRT16	VGACRTIND:0x16			2-112
CRT17	VGACRTIND:0x17			2-113
CRT18	VGACRTIND:0x18			2-113
CRT1E	VGACRTIND:0x1E			2-113
CRT1F	VGACRTIND:0x1F			2-113
CRT02	VGACRTIND:0x2			2-107
CRT22	VGACRTIND:0x22			2-113
CRT03	VGACRTIND:0x3			2-107
CRT04	VGACRTIND:0x4			2-107
CRT05	VGACRTIND:0x5			2-108
CRT06	VGACRTIND:0x6			2-108
CRT07	VGACRTIND:0x7			2-108
CRT08	VGACRTIND:0x8			2-109
CRT09	VGACRTIND:0x9			2-109
CRT0A	VGACRTIND:0xA			2-109
CRT0B	VGACRTIND:0xB			2-110
CRT0C	VGACRTIND:0xC			2-110
CRT0D	VGACRTIND:0xD			2-110
CRT0E	VGACRTIND:0xE			2-110
CRT0F	VGACRTIND:0xF			2-111
GRA00	VGAGRPHIND:0x0			2-114
GRA01	VGAGRPHIND:0x1			2-114

Table 2-2 All Registers Sorted by Address (Continued)

Name	Address	Secondary Address	Additional Address	Page
GRA02	VGAGRPHIND:0x2			2-114
GRA03	VGAGRPHIND:0x3			2-114
GRA04	VGAGRPHIND:0x4			2-115
GRA05	VGAGRPHIND:0x5			2-115
GRA06	VGAGRPHIND:0x6			2-115
GRA07	VGAGRPHIND:0x7			2-115
GRA08	VGAGRPHIND:0x8			2-115
SEQ00	VGASEQIND:0x0			2-104
SEQ01	VGASEQIND:0x1			2-105
SEQ02	VGASEQIND:0x2			2-105
SEQ03	VGASEQIND:0x3			2-105
SEQ04	VGASEQIND:0x4			2-106

Appendix B
Revision History

B.1 Rev 1.01 (August 2009)

- PDF: 43451_rs780_rrg_pub_1.01
- Modified cover title.
- Added marketing names to the variants in section 1.1
- Removed extraneous/unused registers (section 2.9.31 Miscellaneous Display Clock Control Registers and section 2.12 Miscellaneous Memory Mapped Registers).

B.2 Rev 1.00 (July 2009)

- PDF: 43451_rs780_rrg_pub_1.00
- First public release based on OEM release rev 1.07.

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