82C451

Integrated VGA
Graphics Controller

Data Sheet

July 1990

P   R   E   L   I   M   I   N   A   R   Y

CHIPS

82C451
Integrated VGA
Graphics Controller

- Fully Compatible with IBM™ VGA at hardware, register, and BIOS level

- Enhanced backward compatibility with EGA, CGA, Hercules™, and MDA without using NMIs

- Dual Bus Architecture, Integrated Interface to EISA/ISA (PC/AT) and MCA bus (CHIPS/250 and CHIPS/280)

- Single Chip Solution

- Highly integrated design resulting in lower chip count. Total of 15 chips required for a VGA implementation including memory

- Small, low-cost package: 144-pin flat pack

- Supports 8 and 16 bit CPU interface

- Supports Digital and Analog Monitors

- Supports maximum resolution of 800x600 16 colors and 132 Column Text Mode

- External palette DAC support for up to 16 million colors

- Pinout compatible to 82C452 Super VGA. Same board design can use both parts

- Full complement of applications software drivers available from Chips and Technologies
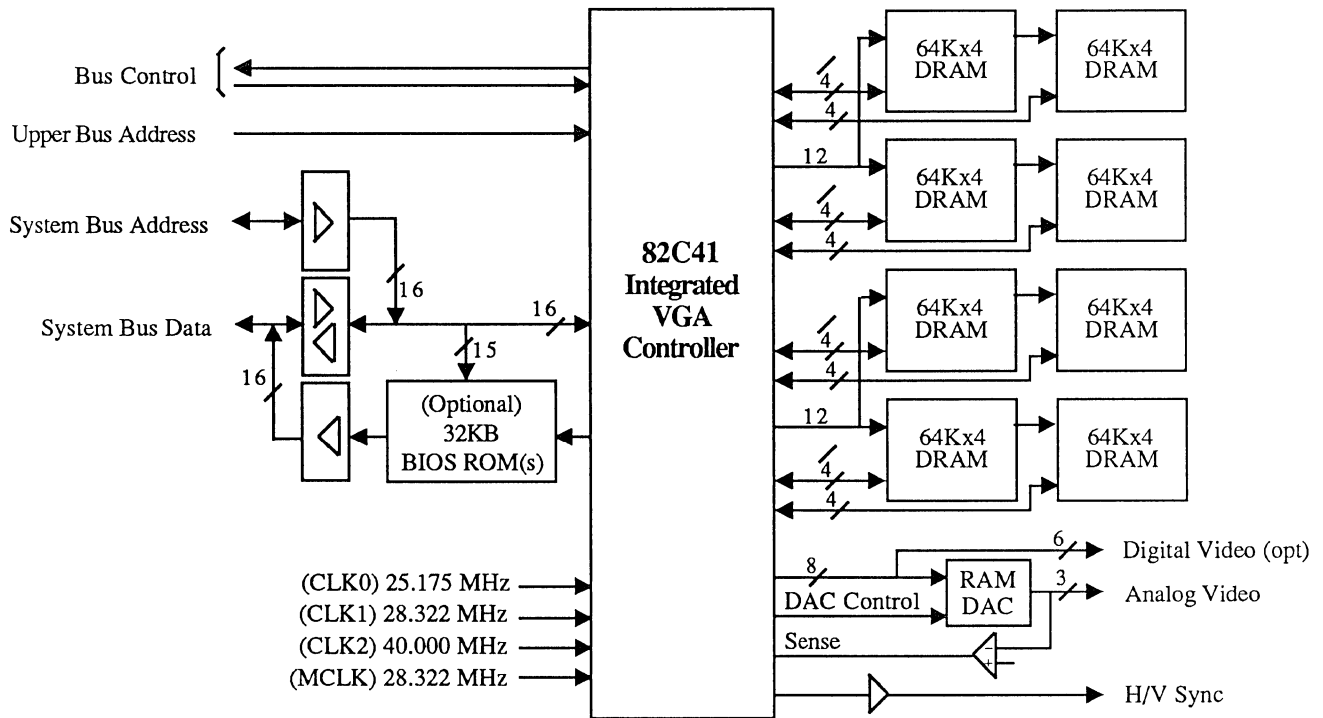
82C451 System Diagram

Revision History

Revision	Date	By	Comment
2.1	6/28/90	ST	Revised Data Sheet Initial Release

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Introduction

The 82C451 is a VGA™ controller of the CHIPS 45x product family. It is fully 100% compatible to IBM™'s VGA standard at the Gate, hardware, register, and BIOS level. It also offers enhanced backward compatibility; to EGA™, CGA™, Hercules™ and MDA™ standards without using NMIs.

The 82C451 VGA supports up to 800x600 16 colors resolution and 132 Column Text Mode.

EXTENSION REGISTERS

The capabilities of the 82C451 beyond the standard VGA are controlled via a set of 'extension' registers. All functionality of these extension registers is disabled on reset. Before the extension registers can be written to, they must be enabled by two sets of control bits (disabled on reset). None of the unused bits in the regular VGA registers are used for extensions.

CPU INTERFACE

The 82C451 provides a strap option to select operation in either EISA/ISA (PC/AT) bus or MCA (Micro Channel) bus systems. All control signals for both interface types are integrated onto the single VGA chip.

The 82C451 supports both 8-bit and 16-bit CPU interfaces to I/O, display memory, and/or BIOS ROM.

BIOS ROM INTERFACE

In EISA/ISA (PC/AT) Bus systems, the 82C451 supports an 8-bit BIOS with one external BIOS ROM chip. The ROM address is internally decoded and the transceivers are enabled directly by the 82C451. The 82C451 implements a ROM chip select (ROMCS/) pin to enable the ROM.

A 16-bit BIOS ROM could be implemented with the 82C451 using two BIOS ROM chips, an external PAL, and a 74LS244 buffer. However, a higher-performance and lower-cost video system will result from implementation of an 8-bit BIOS ROM which is copied into system RAM by the system BIOS on startup.

For motherboard EISA/ISA-bus implementations, the video BIOS may alternately be incorporated directly into the system BIOS. In Micro Channel-based systems, the video BIOS is always included in the system BIOS.

CONFIGURATION SWITCHES

The 82C451 supports up to 7 external DIP switches. These switches are multiplexed on input pins BHE/, RFSH/ (EISA/ISA) or DISA/ (MCA), AEN (EISA/ISA) or MIO/ (MCA), A16, A17, A18, and ADDHI. Two buffers (LS244s) are required to support this feature. The DIP switch state is read into an internal CPU accessible register when the command strobe (IORD/ or CMD/) is low.

MULTIPLE VGAs

It is possible to support up to sixteen 82C451s in one system. Each 82C451 must have a unique number assigned to it through the above mentioned DIP switches. All 82C451s occupy the same memory and I/O address space. However, only one 82C451 responds to CPU accesses at a time. The currently active 82C451 is selected by writing an ID number for that 82C451 into the internal Extended Enable Register for all 82C451s. Only the 82C451 which has the same number on its DIP switches will respond to further CPU accesses.

DISPLAY MEMORY INTERFACE

The 82C451 supports up to 256 Kbytes of display memory using 8 64kx4 DRAM chips. DRAMs are organized as 4 planes. Each plane is 64K bytes and is implemented using 2 64kx4 chips.

Implementing an 82C451 Video Subsystem with 256K Bytes results in a cost-efficient system which can support all VGA-standard modes as well as 800x600 mode and 132 Column Text Mode.

CLOCK SELECTION

The 82C451 provides separate inputs for dotclock selections 0, 1, and 2 (called CLK0, CLK1, and CLK2) which are normally selected by Misc Output Register bits 2 and 3. By default, CLK0 and CLK1 are inputs which must be connected to 25.175 MHz and 28.322 MHz for implementation of standard VGA capabilities. A 40MHz clock can be connected to CLK2 to support 800x600 and 132 Column Text modes. MCLK in 82C451 is used for internal I/O sequencing. 28.322 MHz clock can be connected to MCLK. DRAM timings are generated by the display clock being used. The 82C451 internally selects between these inputs and no additional circuitry is required.

GENERAL PURPOSE OUTPUTS

The 82C451 supports two general purpose output pins. In the 82C451, the TRAP/ and ERMEN/, pins can be defined to serve the respective functions or can individually be 3-stated, forced low or forced high through the General Purpose Output registers. The 82C451 general purpose outputs are defined further in following sections.

FEATURE CONTROL BITS

As in IBM's VGA, the 82C451 provides 2 inputs and outputs for the feature connector. The contents of bits 0 and 1 of the Feature Control Register are output on the FCOUT0/ and FCOUT1/ pins. The state of input pins FCIN0 and FCIN1 can be read by the CPU at bits 5 and 6 of the Input Status Register 0.

EXTERNAL COLOR PALETTE

The 82C451 supports the programming of an external color palette DAC (RAMDAC™) by decoding the CPU addresses and generating the READ and WRITE signals for the external palette.

Inmos™, Brooktree™-style RAMDACs or compatible RAM DACs may be used. The 82C451 normally decodes 3C6-3C9 port addresses for the RAMDAC, but may be configured to additionally decode 83C6-83C9 port addresses for the Brooktree RAMDAC extension registers.

Normally, each RAMDAC analog output provides 6-bit resolution (64 shades of color on each of the analog R, G, and B outputs). If 8-bit-per-color mode is desired for the DAC (e.g., if using Inmos IMSG178 or Brooktree BT478 RAMDACs which provide 256 shades of color on each RGB output), the DAC 6/8-bit mode pin may be controlled via logic external to the 82C451.

PACKAGE

The 82C451 is available in a 144-pin plastic flat pack (PFP). Complete descriptions of all 82C451 pins are included in this document. The pins are separated into the following logical groups for discussion: Bus Interface, Display memory, Video, Clock, Power, and Ground.

82C451 Pin Usage Summary

Bus Interface:	40
Display Memory:	54
Video:	19
Clock:	4
Power:	8
Ground:	12
No Connect	7
Total:	144

VIDEO SUBSYSTEM CHIP COUNT

Using the 82C451, a complete VGA-compatible 16-bit video subsystem for motherboard applications can be built with 15 ICs, including display memory, as shown in the following bill of materials table:

Qty	Chip type
1	82C451 VGA Chip
1	BT475 or BT477 RAMDAC
2	74LS245 Transceiver
2	74LS244 Buffer
1	74LS125 Buffer
8	64Kx4
15	Total

Additional components required are 25.175, 28.322, and 40.000 MHz oscillators, 15-pin video connector, and various resistors and capacitors.

For add-in EISA/ISA-bus boards, two additional 27256 (32Kx8) BIOS ROMs and two LS244 buffers are required.

If Inmos RAMDACs or Brooktree 471/476 RAM-DACs are used, then an additional LM339 comparator, LM334 Current reference, and 1N4148 diode are required (the BT475 and BT477 RAMDACs shown in the bill of materials table above incorporate the comparator and reference functions on-chip). The RAMDAC speed requirements should be compatible with the highest dotclock frequency used.

To implement digital monitor support, the additional components required would be a 16.257 MHz oscillator, 6-position dipswitch, two TTL multiplexer ICs, and a 9-pin connector.

82C451 Pinouts

Pin diagram for the 82C451 Integrated VGA.

Left side pins (top to bottom):

Pin	Name
109	VCC
110	Reserved
111	Reserved
112	TRAP/ (GPOUT1)
113	IRQ [IRQ/]
114	RESET
115	M2D0
116	M3D0
117	GND
118	M2D1
119	M3D1
120	M2D2
121	M3D2
122	M2D3
123	M3D3
124	M2D4
125	M3D4
126	VCC
127	GND
128	M2D5
129	M3D5
130	M2D6
131	M3D6
132	M2D7
133	M3D7
134	CAS0/
135	CAS1/
136	CAS2/
137	CAS3/
138	GND
139	WE/
140	ERMEN/ (GPOUT0)
141	BA0
142	M0D0
143	AA0
144	M1D0

Right side pins (top to bottom):

Pin	Name
72	BHE/ (SW4)
71	AEN (SW6) [MIO/]
70	MEMR/ [S1/]
69	MEMW/ [S0/]
68	IORD/ [CMD/]
67	ADREN/
66	GND
65	RDLO/
64	RDHI/
63	AD0
62	AD1
61	AD2
60	AD3
59	AD4
58	AD5
57	AD6
56	AD7
55	GND
54	VCC
53	AD8
52	AD9
51	AD10
50	AD11
49	AD12
48	AD13
47	AD14
46	AD15
45	GND
44	A16 (SW1)
43	A17 (SW2)
42	A18 (SW3)
41	ADDHI (SW5)
40	FCIN1
39	FCIN0
38	Reserved
37	VCC

Top side pins (left to right, 108 to 73):

Pin	Name
108	SENSE
107	FCOUT1/
106	FCOUT0/ (CLKIN)
105	CLK0 (CLKSEL0)
104	CLK1 (CLKSEL1)
103	CLK2
102	GND
101	MCLK
100	PALRD/
99	PALWR/
98	VSYNC
97	HSYNC
96	BLANK/ (DE)
95	P7
94	P6
93	P5
92	PCLK
91	GND
90	VCC
89	P4
88	P3
87	P2
86	P1
85	P0
84	Reserved
83	Reserved
82	PTMC [MCA/]
81	GND
80	RFSH/ [DISA/]
79	IOWR/ [SETUP/]
78	IOCS16/ [VGAREQ/]
77	MEN16/ [DS16/]
76	ROMCS/ [POSID/]
75	WR46E8/ [CSFB/]
74	RDY
73	VCC

(SW7)

Bottom side pins (left to right, 1 to 36):

Pin	Name
1	VCC
2	BA1
3	M0D1
4	AA1
5	M1D1
6	BA2
7	M0D2
8	AA2
9	GND
10	M1D2
11	BA3
12	M0D3
13	AA3
14	M1D3
15	BA4
16	M0D4
17	Reserved
18	VCC
19	GND
20	RAS/
21	AA4
22	M1D4
23	BA5
24	M0D5
25	AA5
26	M1D5
27	BA6
28	M0D6
29	AA6
30	GND
31	M1D6
32	BA7
33	M0D7
34	AA7
35	M1D7
36	Reserved

82C451 Integrated VGA

Note:
Pin names shown indicate EISA/ISA bus connections
Pin names in brackets [...] indicate MCA bus connections
Pin names in parenthese (...) indicate alternate function

82C451 Pinouts

82C451 PIN DESCRIPTIONS

Pin #	Pin Name		Type	Active	Description
41	ADDHI	(SW5)	In	High	Multiplexed memory address enable and auxiliary data bus. High order memory address enable (decoded A19-A23) when ADREN/ is low. This bit is read into bit 4 of the Internal Switch Register (XR01) when the Switch Register is accessed by the CPU and ADREN/ is high. Address latched internally. Defines the current memory address as a valid address for 82C451. Ignored for I/O cycles.
42	A18	(SW3)	In	High	Multiplexed upper address and auxiliary data bus. High order address when ADREN/ is low. These bits are read into bits 0-2 of the Internal Switch Register (XR01) when the Switch Register is accessed by the CPU and ADREN/ is high. In the MCA bus, address and status are latched internally on the leading edge of CMD/.
43	A17	(SW2)	In	High	
44	A16	(SW1)	In	High	
46	AD15		I/O	High	System upper multiplexed address and data bus. Address when ADREN/ is low and data when ADREN/ is high. In the MCA bus, the address is latched internally on the leading edge of CMD/.
47	AD14		I/O	High	
48	AD13		I/O	High	
49	AD12		I/O	High	
50	AD11		I/O	High	
51	AD10		I/O	High	
52	AD9		I/O	High	
53	AD8		I/O	High	
56	AD7		I/O	High	System lower multiplexed address and data bus. Address when ADREN/ is low and data when ADREN/ is high. In the MCA bus, address is latched internally on the leading edge of CMD/.
57	AD6		I/O	High	
58	AD5		I/O	High	
59	AD4		I/O	High	
60	AD3		I/O	High	
61	AD2		I/O	High	
62	AD1		I/O	High	
63	AD0		I/O	High	
67	ADREN/		Out	Low	Controls multiplexing of external address/data multiplexers. 0=Enable address, 1=Enable Data.
64	RDHI/		Out	Low	Data transceiver direction controls. Control direction of external data transceivers for the AD bus. 0: read from 82C451, 1: write to 82C451. Enable for the transceiver is externally generated by inverting ADREN/.
65	RDLO/		Out	Low	
72	BHE/	(SW4)	In	Low	Multiplexed Byte High Enable and auxiliary data bit. BHE/ when ADREN/ is low. BHE/ low indicates that the high order byte at the current word address is being accessed. This bit is read into bit 3 of Internal Switch Register (XR01) when the Switch register is accessed by the CPU and CMD/ (or I/O or memory strobe) is low. Status latched internally on falling edge of CMD/ (or I/O or memory strobe).

Note: Pin names in brackets [...] indicate MCA bus functionality if different from EISA/ISA (PC/AT) bus

82C451 PIN DESCRIPTIONS   System Bus Interface

Pin #	Pin Name		Type	Active	Description
114	RESET		In	High	Reset. Connect directly to the bus reset signal.
68	IORD/	[CMD/]	In	Low	In EISA/ISA interface, indicates I/O Read Cycle. In MCA interface, indicates beginning of a command part of a bus cycle. Driven off CMD/ on MCA, VGACMD/ on CHIPS/250.
79	IOWR/	[SETUP/]	In	Low	In EISA/ISA interface, indicates I/O Write Cycle. In MCA interface, indicates that the configuration register at 100-107 should be enabled. All other memory and I/O functions are disabled.
70	MEMR/	[S1/]	In	Low	In EISA/ISA interface, indicates Memory Read cycle. In MCA interface, indicates Status 1.
69	MEMW/	[S0/]	In	Low	In EISA/ISA interface, indicates Memory Write cycle. In MCA interface, indicates Status 0.

					S1/	S0/	Operation
					0	0	Undefined
					0	1	Read
					1	0	Write
					1	1	Undefined

Pin #	Pin Name		Type	Active	Description
71	AEN	[MIO/] (SW6)	In	Both	In EISA/ISA interface, defines valid I/O address: 0 = valid I/O address, 1 = Invalid I/O address (latched internally). In MCA interface, indicates memory or I/O cycle: 1 = memory, 0 = I/O. Latched internally. When ADREN/ is high, this bit is read into bit 5 of the Internal Switch register (XR01) when the Switch register is accessed by the CPU.
80	RFSH/	[ISA/] (SW7)	In	Low	This low pin is an active low signal which disables memory and I/O cycles in both PC and MCA systems (when this pin is low, display memory and I/O registers are not accessible). In PC bus systems, this pin is connected to the bus refresh pin (low indicates a memory refresh cycle to which the 82C451 should not respond). In MCA systems, this pin is connected to the VGA DISABLE/ signal). When ADREN/ is high, this bit is read into bit 6 of Internal Switch Register (XR01) when the Switch Register is accessed by the CPU.
82	PTMC	[MCA/]	In	Both	Indicates the type of CPU interface: 0 = MCA, 1 = EISA/ISA (PC).

Note: Pin names in brackets [...] indicate MCA bus functionality if different from EISA/ISA (PC/AT) bus.

Pin #	Pin Name		Type	Active	Description
74	RDY		Out	High	Ready. Driven low to indicate that current cycle should be extended with wait states. Driven high at end of cycle to indicate 'ready' then 3-stated.
113	IRQ	[IRQ/]	Out	Both	Frame Interrupt Output. Interrupt polarity is programmable. Set when interrupt on VSYNC is enabled. Cleared by reprogramming register 11h in the CRT Controller. (EISA/ISA-Bus interrupts are active high, MCA bus interrupts are active low). See also XR14 bit-7.
78	IOCS16/	[VGAREQ/]	Out	Low	In PC-Bus interface systems, this output is an active low signal indicating a valid 16-bit I/O cycle. In MCA interface systems, this output is an active low signal indicating that a FAST cycle can be executed (this can be disabled through a register).
77	MEN16/	[DS16/]	Out	Low	Indicates 16-bit memory cycle in PC-Bus interface systems. Indicates 16-bit memory and I/O cycles in MCA interface systems. In PC Bus interface systems this signal is a DC level which is low when 16-bit interface is enabled and high when 16-bit interface is disabled.
75	WR46E8/	[CSFB/]	Out	Low	In PC-BUS interface systems, active low for I/O writes to port 46E8h. In MCA Interface systems, indicates any valid access to 82C451.
112	TRAP/	(GPOUT1)	Out	Low	Indicates trap condition requiring special CPU assistance. Can be redefined as a general purpose output pin.
100	PALRD/		Out	Low	Connected to the Read input of the Palette DAC (G176, BT471, or compatible). Asserted when the 82C451 is enabled and an I/O Read occurs from addresses 3C6h, 3C8h, or 3C9h (or 83C6h-83C9h if enabled). (The 82C451 responds directly for accesses to 3C7h).
99	PALWR/		Out	Low	Connected to the Write input of the Palette DAC (G176, BT471, or compatible). Asserted when the 82C451 is enabled and an I/O Write occurs to addresses 3C6-3C9h (or 83C6h-83C9h if enabled).
76	ROMCS/	[POSID/]	Out	Low	Indicates access to ROM space in PC-Bus interface systems. Indicates access to POS ID registers (address 100, 101, and SETUP/ low) in MCA interface systems.

Note: Pin names in brackets [...] indicate MCA bus functionality if different from EISA/ISA (PC/AT) bus.

82C451 PIN DESCRIPTIONS

Pin #	Pin Name		Type	Active	Description
36	Reserved		-	-	(AA8 82C452 Super-VGA)
34	AA7		Out	High	DRAM address bus for planes 0-1.
29	AA6		Out	High	
25	AA5		Out	High	
21	AA4		Out	High	
13	AA3		Out	High	
8	AA2		Out	High	
4	AA1		Out	High	
143	AA0		Out	High	
38	Reserved		-	-	(BA8 in 82C452 Super-VGA)
32	BA7		Out	High	DRAM address bus for planes 2-3.
27	BA6		Out	High	
23	BA5		Out	High	
15	BA4		Out	High	
11	BA3		Out	High	
6	BA2		Out	High	
2	BA1		Out	High	
141	BA0		Out	High	
139	WE/		Out	Low	Write enable for all memory banks/planes
20	RAS/		Out	Low	Row address strobe for memory bank 0
17	Reserved		-	-	(RAS2/ in 82C452 Super-VGA
134	CAS0/		Out	Low	Column address strobes for memory planes 0-3.
135	CAS1/		Out	Low	
136	CAS2/		Out	Low	
137	CAS3/		Out	Low	
140	ERMEN/	(GPOUT0)	Out	Low	Indicates CRT memory cycle (High) or CPU memory cycle (low). Can be redefined as a general purpose output pin.

82C451 PIN DESCRIPTIONS

Display Memory Interface

Pin #	Pin Name	Type	Active	Description
33	M0D7	I/O	High	DRAM address bus for planes 0
28	M0D6	I/O	High	
24	M0D5	I/O	High	
16	M0D4	I/O	High	
12	M0D3	I/O	High	
7	M0D2	I/O	High	
3	M0D1	I/O	High	
142	M0D0	I/O	High	
35	M1D7	I/O	High	DRAM data bus for plane 1
31	M1D6	I/O	High	
26	M1D5	I/O	High	
22	M1D4	I/O	High	
14	M1D3	I/O	High	
10	M1D2	I/O	High	
5	M1D1	I/O	High	
144	M1D0	I/O	High	
132	M2D7	I/O	High	
130	M2D6	I/O	High	DRAM data bus for plane 2
128	M2D5	I/O	High	
124	M2D4	I/O	High	
122	M2D3	I/O	High	
120	M2D2	I/O	High	
118	M2D1	I/O	High	
115	M2D0	I/O	High	
133	M3D7	I/O	High	DRAM data bus for plane 3
131	M3D6	I/O	High	
129	M3D5	I/O	High	
125	M3D4	I/O	High	
123	M3D3	I/O	High	
121	M3D2	I/O	High	
119	M3D1	I/O	High	
116	M3D0	I/O	High	

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Pin #	Pin Name		Type	Active	Description
95	P7		Out	High	8-bit video pixel output
94	P6		Out	High	
93	P5		Out	High	
89	P4		Out	High	
88	P3		Out	High	
87	P2		Out	High	
86	P1		Out	High	
85	P0		Out	High	
92	PCLK		Out	High	Video Pixel Clock. Video data is synchronized to this clock.
96	BLANK/	(DE)	Out	Both	Blanking signal (active low) for external palette DAC. May be redefined under software control as active high DE (Display Enable).
97	HSYNC		Out	Both	Horizontal and vertical sync signals for the CRT (polarity is programmable).
98	VSYNC		Out	Both	
110	Reserved		-	-	These pins should be pulled high through 10K resistors.
111	Reserved		-	-	
108	SENSE		In	High	Input pin normally used for reading monitor sense. Normally connected to the outputs of an LM339 comparator on the analog RGB outputs. The state of this pin may read as bit-4 of Input Status Register 0 (port 3C2h).
84	Reserved		-	-	These pins should be left unconnected.
83	Reserved		-	-	

82C451 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
39	FCIN0	In	High	These two pins may be read as bits 5 (FCIN0) and 6
40	FCIN1	In	High	(FCIN1) of Input Status Register 0 (port 3C2h).
106	FCOUT0/	Out	Low	These two pins indicate the inverse of bits 0 and 1 of the
107	FCOUT1/	Out	Low	Feature Control Register (which may be written at port 3BA/3DAh and read at 3CAh).
105	CLK0	In	High	CLK0, CLK1, and CLK2 are 3 clock inputs. One of
104	CLK1	In	High	the three is selected as the input dotclock per Miscella-
103	CLK2	In	High	neous Output Register (3C2h) bits 2 and 3.
101	MCLK	In	High	Memory Clock. Used for internal I/O Sequencing. This clock should not be more than 30 MHz. In 82C452 this clock is used for generating memory timings.
1	VCC	VCC	--	Power
18	VCC	VCC	--	
37	VCC	VCC	--	
54	VCC	VCC	--	
73	VCC	VCC	--	
90	VCC	VCC	--	
109	VCC	VCC	--	
126	VCC	VCC	--	
9	GND	GND	--	Ground
19	GND	GND	--	
30	GND	GND	--	
45	GND	GND	--	
55	GND	GND	--	
66	GND	GND	--	
81	GND	GND	--	
91	GND	GND	--	
102	GND	GND	--	
117	GND	GND	--	
127	GND	GND	--	
138	GND	GND	--	

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82C451 REGISTER SUMMARY - CGA, MDA, AND HERCULES MODES

Register	Register Name	Bits	Access	I/O Port - MGA	I/O Port - CGA	Comment
STAT	Display Status	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W	3BB (ignored)	3DB (ignored)	no light pen
SLPEN	Set Light Pen Flip Flop	0	W	3B9 (ignored)	3DC (ignored)	no light pen
MODE	CGA/MDA/Hercules Mode Control	7	RW	3B8	3D8	
COLOR	CGA Color Select	6	RW	n/a	3D9	
CONFIG	Hercules Configuration	2	W	3BF	n/a	
			R	3B6-3B7 index 14	n/a	XR14
RX, R0-11	'6845' Registers	0-8	RW	3B4-3B5	3D4-3D5	
XRX, XR0-7F	Extension Registers	0-8	RW	3B6-3B7	3D6-3D7	if port 103 bit-7=1

82C451 REGISTER SUMMARY - EGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
MISC	Miscellaneous Output	7	W	3C2	3C2	
FC	Feature Control	3	W	3BA	3DA	
FEAT	Feature Read (Input Status 0)	4	R	3C2	3C2	
STAT	Display Status (Input Status 1)	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W	3BB (ignored)	3DB (ignored)	no light pen
SLPEN	Set Light Pen Flip Flop	0	W	3BC (ignored)	3DC (ignored)	no light pen
SRX, SR0-4	Sequencer	0-8	RW	3C4-3C5	3C4-3C5	
CRX, CR0-18	CRT Controller	0-8	RW	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	RW	3CE-3CF	3CE-3CF	
ARX, AR0-13	Attributes Controller	0-8	RW	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	RW	3B6-3B7	3D6-3D7	if port 103 bit-7=1

82C451 REGISTER SUMMARY - VGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Reg Type	Comment
POSIDL	POS ID LSB	8	R	100 (Setup Only)	100 (Setup Only)	VGA	External
POSIDH	POS ID MSB	8	R	101 (Setup Only)	101 (Setup Only)	VGA	External
SLEEP	Video Subsystem Sleep Control	1	RW	102 (Setup Only)	102 (Setup Only)	VGA	
XENA	Extended Enable	7	RW	103 (Setup Only)	103 (Setup Only)	VGA	
GLOBID	Global ID (0A5h)	8	R	104 (Setup Only)	104 (Setup Only)	VGA	
MISC	Miscellaneous Output	7	W	3C2	3C2	VGA	
			R	3CC	3CC	VGA	
FC	Feature Control	3	W	3BA	3DA	VGA	
			R	3CA	3CA	VGA	
FEAT	Feature Read (Input Status 0)	4	R	3C2	3C2	VGA	
STAT	Display Status (Input Status 1)	6	R	3BA	3DA	VGA	
CLPEN	Clear Light Pen Flip Flop	0	W	3BB (ignored)	3DB (ignored)	n/a	no lpen
SLPEN	Set Light Pen Flip Flop	0	W	3BC (ignored)	3DC (ignored)	n/a	no lpen
VSE	Video Subsystem Enable	1	RW	3C3 if MCA	3C3 if MCA	Motherboard	
46E8	Setup / Disable Control	2	W	46E8 if EISA/ISA	46E8 if EISA/ISA	VGA	
DACMASK	Color Palette Pixel Mask	8	RW	3C6, 83C6	3C6, 83C6	DAC	
DACSTATE	Color Palette State	2	R	3C7, 83C7	3C7, 83C7	VGA	
DACRX	Color Palette Read-Mode Index	8	W	3C7, 83C7	3C7, 83C7	DAC	
DACWX	Color Palette Write-Mode Index	8	RW	3C8, 83C8	3C8, 83C8	DAC	
DACDATA	Color Palette Registers 0-FF	3x6 or 3x8	RW	3C9, 83C9	3C9, 83C9	DAC	
SRX, SR0-7	Sequencer	0-8	RW	3C4-3C5	3C4-3C5	VGA	
CRX, CR0-3F	CRT Controller	0-8	RW	3B4-3B5	3D4-3D5	VGA	
GRX, GR0-8	Graphics Controller	0-8	RW	3CE-3CF	3CE-3CF	VGA	
ARX, AR0-14	Attributes Controller	0-8	RW	3C0-3C1	3C0-3C1	VGA	
XRX, XR0-7F	Extension Registers	0-8	RW	3B6-3B7	3D6-3D7	VGA	103 bit7=1

82C451 REGISTER SUMMARY - INDEXED REGISTERS (EGA / VGA)

Register	Register Name	Bits	Register Type	Access (VGA)	Access (EGA)	I/O Port
SRX	Sequencer Index	3	VGA/EGA	RW	RW	3C4
SR0	Reset	2	VGA/EGA	RW	RW	3C5
SR1	Clocking Mode	6	VGA/EGA	RW	RW	3C5
SR2	Plane Mask	4	VGA/EGA	RW	RW	3C5
SR3	Character Map Select	6	VGA/EGA	RW	RW	3C5
SR4	Memory Mode	3	VGA/EGA	RW	RW	3C5
SR7	Reset Horizontal Character Counter	0	VGA	W	n/a	3C5
CRX	CRTC Index	6	VGA/EGA	RW	RW	3B4 Mono, 3D4 Color
CR0	Horizontal Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR1	Horizontal Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR2	Horizontal Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR3	Horizontal Blanking End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR4	Horizontal Retrace Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR5	Horizontal Retrace End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR6	Vertical Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR7	Overflow	5	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR8	Preset Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR9	Character Cell Height	5+3	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRA	Cursor Start	5+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRB	Cursor End	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRC	Start Address High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRD	Start Address Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRE	Cursor Location High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRF	Cursor Location Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
LPENH	Light Pen High	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
LPENL	Light Pen Low	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
CR10	Vertical Retrace Start	8	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR11	Vertical Retrace End	4+4	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR12	Vertical Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR13	Offset	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR14	Underline Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR15	Vertical Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR16	Vertical Blanking End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR17	CRT Mode Control	7	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR18	Line Compare	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR22	Graphics Controller Data Latches	8	VGA	R	n/a	3B5 Mono, 3D5 Color
CR24	Attribute Controller Index/Data Latch	1	VGA	R	n/a	3B5 Mono, 3D5 Color
CR3x	Clear Vertical Display Enable FF	0	VGA	W	n/a	3B5 Mono, 3D5 Color
GRX	Graphics Controller Index	4	VGA/EGA	RW	RW	3CE
GR0	Set/Reset	4	VGA/EGA	RW	RW	3CF
GR1	Enable Set/Reset	4	VGA/EGA	RW	RW	3CF
GR2	Color Compare	4	VGA/EGA	RW	RW	3CF
GR3	Data Rotate	5	VGA/EGA	RW	RW	3CF
GR4	Read Map Select	2	VGA/EGA	RW	RW	3CF
GR5	Mode	6	VGA/EGA	RW	RW	3CF
GR6	Miscellaneous	4	VGA/EGA	RW	RW	3CF
GR7	Color Don't Care	4	VGA/EGA	RW	RW	3CF
GR8	Bit Mask	8	VGA/EGA	RW	RW	3CF
ARX	Attribute Controller Index	6	VGA/EGA	RW	RW	3C0 (3C1)
AR0-F	Internal Palette Regs 0-15	6	VGA/EGA	RW	RW	3C0 (3C1)
AR10	Mode Control	7	VGA/EGA	RW	RW	3C0 (3C1)
AR11	Overscan Color	6	VGA/EGA	RW	RW	3C0 (3C1)
AR12	Color Plane Enable	6	VGA/EGA	RW	RW	3C0 (3C1)
AR13	Horizontal Pixel Panning	4	VGA/EGA	RW	RW	3C0 (3C1)
AR14	Color Select	4	VGA	RW	n/a	3C0 (3C1)

82C451 EXTENSION REGISTER SUMMARY: 00-2F

Chips' 45x Product Family

Reg	Register Name	Bits	Access	Port	Reset	450	451	452	455	456
XRX	Extension Index Register	7	R/W	3B6/3D6	0 x x x x x x x	✓	✓	✓	✓	✓
XR00	Chip Version	8	R/O	3B7/3D7	0 1 0 0 r r r r	✓	✓	✓	✓	✓
XR01	DIP Switch	8	R/O	3B7/3D7	d d d d d d d d	✓	✓	✓	✓	✓
XR02	CPU Interface	8	R/W	3B7/3D7	R R R R R R R R	✓	✓	✓	✓	✓
XR03	ROM Interface	1		3B7/3D7	0 0 0 0 0 0 0 R	.	✓	✓	.	.
XR04	Memory Mapping	2	R/W	3B7/3D7	0 0 R 0 0 0 0 R	✓	✓	✓	✓	✓
XR05	Sequencer Control	6	R/W	3B7/3D7	R R 0 R R R R 0	.	.	✓	.	.
XR06	DRAM Interface	8	R/W	3B7/3D7	0 1 0 0 1 0 1 0	.	.	✓	.	.
XR07	-reserved-	–	–	3B7/3D7	0 0 0 0 0 R R R	.	.	.	.	.
XR08	General Purpose Output Select B	4	R/W	3B7/3D7	0 0 0 0 R R R R	.	✓	✓	✓	✓
XR09	General Purpose Output Select A	4	R/W	3B7/3D7	0 0 0 0 R R R R	.	✓	✓	✓	✓
XR0A	Cursor Address Top	2	R/W	3B7/3D7	0 0 0 0 R R R R	.	.	✓	.	.
XR0B	CPU Paging	3	R/W	3B7/3D7	0 0 0 0 0 R R R	✓	.	✓	✓	✓
XR0C	Start Address Top	2	R/W	3B7/3D7	0 0 0 0 0 0 R R	✓	.	✓	.	.
XR0D	Auxiliary Offset	2	R/W	3B7/3D7	0 0 0 0 0 0 R R	✓	✓	✓	✓	✓
XR0E	Text Mode	2	R/W	3B7/3D7	0 0 0 0 R R 0 0	✓	.	✓	.	.
XR0F	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR10	Single/Low Map Register	6	R/W	3B7/3D7	0 0 x x x x x x	✓	.	✓	.	.
XR11	High Map Register	6	R/W	3B7/3D7	0 0 x x x x x x	✓	.	✓	.	.
XR12	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR13	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR14	Emulation Mode	8	R/W	3B7/3D7	R R R R h h R R	✓	✓	✓	✓	✓
XR15	Write Protect	7	R/W	3B7/3D7	R R R R R R R R	✓	✓	✓	✓	✓
XR16	Trap Enable	6	R/W	3B7/3D7	0 0 R R R R R R	.	✓	✓	✓	✓
XR17	Trap Status	6	R/W	3B7/3D7		.	✓	✓	✓	✓
XR18	Alternate H Display End	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR19	Alt H Retr Start/Half-line Comp	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR1A	Alternate H Retrace End	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR1B	Alternate H Total	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR1C	Alternate H Blank Start	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR1D	Alternate H Blank End	8	R/W	3B7/3D7	R x x x x x x x	✓	✓	✓	✓	✓
XR1E	Alternate Offset	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR1F	(Virtual EGA Switch Register)	–	–	3B7/3D7	0 0 0 0 x x x x	✓	.	.	.	.
XR20	Sliding Unit Delay / (453 Interface)	2	R/W	3B7/3D7	0 0 0 0 0 0 R R	.	.	✓	.	.
XR21	Sliding Hold A	8	R/W	3B7/3D7	x x x x x x x x	.	.	✓	.	.
XR22	Sliding Hold B	8	R/W	3B7/3D7	x x x x x x x x	.	.	✓	.	.
XR23	Sliding Hold C / (Wr Bit Mask Ctrl)	8	R/W	3B7/3D7	x x x x x x x x	.	.	✓	.	.
XR24	Sliding Hold D / (Wr Bit Mask Pattern)	8	R/W	3B7/3D7		.	.	✓	.	.
XR25	(453 Pin Definition)	–	–	3B7/3D7		.	.	.	.	.
XR26	(453 Configuration)	–	–	3B7/3D7		.	.	.	.	.
XR27	Force Sync State	6	R/W	3B7/3D7	0 0 x x x x x x	.	.	✓	.	.
XR28	Video Interface	3	R/W	3B7/3D7	0 0 0 0 0 R R R	✓	✓	✓	✓	✓
XR29	Function Control	6	R/W	3B7/3D7	0 0 x x x x x x	.	.	✓	.	.
XR2A	Frame Interrupt Count	4	R/W	3B7/3D7	0 0 0 0 R R R R	.	.	✓	.	.
XR2B	Default Video	8	R/W	3B7/3D7	R R R R R R R R	✓	✓	✓	✓	✓
XR2C	Delay Horizontal High	4		3B7/3D7	0 0 0 0 x x x x	.	.	✓	.	.
XR2D	Delay Horizontal Low	8		3B7/3D7	x x x x x x x x	.	.	✓	.	.
XR2E	Delay Vertical High	4		3B7/3D7	0 0 0 0 R R R R	.	.	✓	.	.
XR2F	Delay Vertical Low	8		3B7/3D7	x x x x x x x x	.	.	✓	.	.

Reset Codes:
x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits

0 = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
R = Reset to 0 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 451 = Integrated VGA, 452 = Super VGA, 455 & 456 VGAs drive both 450 = 1 Megabit VGA, 452 = VRAM VGA CRT and Flat Panel displays (Plasma, EL, and LCD).

82C451 EXTENSION REGISTER SUMMARY: 30-5F

Reg	Register Name	Bits	Access	Port	Reset	Chips' 45x Product Family				
						450	451	452	455	456
XR30	Graphics Cursor Start Address High	8	RW	3B7/3D7	R R R R R R R R	.	.	✓	.	.
XR31	Graphics Cursor Start Address Low	8	RW	3B7/3D7	R R R R R R R R	.	.	✓	.	.
XR32	Graphics Cursor End Address	8	RW	3B7/3D7	R R R R R R R R	.	.	✓	.	.
XR33	Graphics Cursor X Position High	5	RW	3B7/3D7	x 0 0 R R R R R	.	.	✓	.	.
XR34	Graphics Cursor X Position Low	8	RW	3B7/3D7	R R R R R R R R	.	.	✓	.	.
XR35	Graphics Cursor Y Position High	4	RW	3B7/3D7	0 0 0 0 R R R R	.	.	✓	.	.
XR36	Graphics Cursor Y Position Low	8	RW	3B7/3D7	R R R R R R R R	.	.	✓	.	.
XR37	Graphics Cursor Mode	5	RW	3B7/3D7	0 0 0 x x x x x	.	.	✓	.	.
XR38	Graphics Cursor Mask	8	RW	3B7/3D7	x x x x x x x x	.	.	✓	.	.
XR39	Graphics Cursor Color 0	8	RW	3B7/3D7	x x x x x x x x	.	.	✓	.	.
XR3A	Graphics Cursor Color 1	8	RW	3B7/3D7	x x x x x x x x	.	.	✓	.	.
XR3B	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR3C	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR3D	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR3E	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR3F	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR40	(I/O Flag)	–	–	3B7/3D7		.	.	.	.	.
XR41	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR42	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR43	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR44	(Scratch Register 0)	–	–	3B7/3D7		.	.	.	.	.
XR45	(Scratch Register 1 / FG Color)	–	–	3B7/3D7		.	.	.	.	.
XR46	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR47	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR48	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR49	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR4A	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR4B	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR4C	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR4D	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR4E	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR4F	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR50	(Panel Format)	–	–	3B7/3D7		.	.	.	✓	✓
XR51	(Display Type)	–	–	3B7/3D7		.	.	.	✓	✓
XR52	(Panel Size)	–	–	3B7/3D7		.	.	.	✓	✓
XR53	(Override)	–	–	3B7/3D7		.	.	.	✓	✓
XR54	(Alternate Misc Output)	–	–	3B7/3D7		.	.	.	✓	✓
XR55	(Text Mode 350_A Compensation)	–	–	3B7/3D7		.	.	.	✓	✓
XR56	(Text Mode 350_B Compensation)	–	–	3B7/3D7		.	.	✓	✓	✓
XR57	(Text Mode 400 Compensation)	–	–	3B7/3D7		.	.	.	✓	✓
XR58	(Graphics Mode 350 Compensation)	–	–	3B7/3D7		.	.	.	✓	✓
XR59	(Graphics Mode 400 Compensation)	–	–	3B7/3D7		.	.	.	✓	✓
XR5A	(Flat Panel Vertical Display Start 400)	–	–	3B7/3D7		.	.	.	✓	✓
XR5B	(Flat Panel Vertical Display End 400)	–	–	3B7/3D7		.	.	.	✓	✓
XR5C	(Weight Control Clock A)	–	–	3B7/3D7		.	.	.	✓	✓
XR5D	(Weight Control Clock B)	–	–	3B7/3D7		.	.	.	✓	✓
XR5E	(ACDCLK Control)	–	–	3B7/3D7		.	.	.	✓	✓
XR5F	(Power Down Mode Refresh)	–	–	3B7/3D7		.	.	.	✓	✓

82C451 EXTENSION REGISTER SUMMARY: 60-7F

Chips' 45x Product Family

Reg	Register Name	Bits	Access	Port	Reset	450	451	452	455	456
XR60	*(Blink Rate Control)*	–	–	3B7/3D7		.	.	.	✓	✓
XR61	*(Text Color Mapping Control)*	–	–	3B7/3D7		.	.	.	✓	✓
XR62	*(Text Color Shift Parameter)*	–	–	3B7/3D7		.	.	.	✓	✓
XR63	*(Graphics Color Mapping Control)*	–	–	3B7/3D7		.	.	.	✓	✓
XR64	*(Alternate Vertical Total)*	–	–	3B7/3D7		.	.	.	✓	✓
XR65	*(Alternate Overflow)*	–	–	3B7/3D7		.	.	.	✓	✓
XR66	*(Alternate Vertical Sync Start)*	–	–	3B7/3D7		.	.	.	✓	✓
XR67	*(Alternate Vertical Sync End)*	–	–	3B7/3D7		.	.	.	✓	✓
XR68	*(Alternate Vertical Display Enable End)*	–	–	3B7/3D7		.	.	.	✓	✓
XR69	*(Flat Panel Vertical Display Start 350)*	–	–	3B7/3D7		.	.	.	✓	✓
XR6A	*(Flat Panel Vertical Display End 350)*	–	–	3B7/3D7		.	.	.	✓	✓
XR6B	*(Flat Panel Vertical Overflow 2)*	–	–	3B7/3D7		.	.	.	✓	✓
XR6C	*(Weight Control Clock C)*	–	–	3B7/3D7		.	.	.	✓	✓
XR6D	*(External Palette Control)*	–	–	3B7/3D7		.	.	.	.	✓
XR6E	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR6F	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR70	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR71	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR72	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR73	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR74	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR75	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR76	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR77	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR78	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR79	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR7A	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR7B	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR7C	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR7D	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR7E	**CGA/Hercules Color Select**	6	R/O	3B7/3D7	0 0 x x x x x x	✓	✓	✓	✓	✓
XR7F	**Diagnostic**	7	R/W	3B7/3D7	R R x x x x R R	✓	✓	✓	✓	✓

82C451 Registers

GLOBAL CONTROL (SETUP) REGISTERS

The Setup Control Register is used to enable or disable the VGA. It is also used to place the VGA in normal or setup mode. This register is used only in the PC-bus interface. In the MCA Bus interface these functions are performed by the DISA/ and SETUP/ pins respectively.

The Global and Extension Enable Registers are accessible only during Setup mode. The Global ID Register contains the ID number that identifies the 82C451 as a Chips & Technologies product.

Note: In setup mode in the IBM VGA, the Global Setup Register (defined as port address 102) actually occupies the *entire I/O space*. Only the lower 3 bits are used to decode and select this register. To avoid bus conflicts with other peripherals, reads should only be performed at the 10xh port addresses while in setup mode. To eliminate potential compatibility problems in widely varying PC systems, the 82C451 decodes the Global Setup register at I/O port 102h only.

GENERAL CONTROL REGISTERS

Two Input Status Registers read the SENSE pin, pending CRT interrupt, display enable/HSYNC output, and vertical retrace/video output. The Feature Control Register selects the VSYNC function while the Miscellaneous Output Register controls I/O address select, clock selection, access to video RAM, memory page, and video SYNC polarity.

CGA / HERCULES REGISTERS

CGA Mode and Color Select registers are provided on-chip for emulation of CGA modes. Hercules Mode and Configuration registers are provided on-chip for emulation of Hercules mode.

SEQUENCER REGISTERS

The Sequencer Index Register contains a 3-bit index to the Sequencer Data Registers. The Reset Register forces an asynchronous or synchronous reset of the sequencer. The Sequencer Clocking Mode Register controls master clocking functions, video enable/disable and selects either an 8 or 9 dot character clock. A Plane/Map Mask Register enables the color plane and write protect. The Character Font Select Register handles video intensity and character generation and controls the display memory plane through the character generator select. The Sequencer Memory Mode Register handles all memory, giving access by the CPU to 4/16/32KBytes, Odd/Even addresses (planes) and writing of data to display memory.

CRT CONTROLLER REGISTERS

The CRT Controller Index Register contains a 6-bit index to the CRT Controller Registers. Twenty eight registers perform all display functions for modes: horizontal and vertical blanking and sync, panning and scrolling, cursor size and location, light pen, and underline.

GRAPHICS CONTROLLER REGISTERS

The Graphics Controller Index Register contains a 4-bit index to the Graphics Controller Registers. The Set/Reset Register controls the format of the CPU data to display memory. It also works with the Enable Set/Reset Register. Reducing 32 bits of display data to 8 bits of CPU data is accomplished by the Color Compare Register. Data Rotate Registers specify the CPU data bits to be rotated and subjected to logical operations. The Read Map Select Register reduces memory data for the CPU in the four plane (16 color) graphics mode. The Graphics Mode Register controls the write, read, and shift register modes. The Miscellaneous Register handles graphics/text, chaining of odd/even planes, and display memory mapping. Additional registers include Color Don't Care and Bit Mask.

ATTRIBUTE CONTROLLER AND EXTERNAL COLOR PALETTE REGISTERS

The Attribute Controller Index Register contains a 5-bit index to the Attribute Controller Registers. A 6th bit is used to enable the video. The Attribute Controller Registers handle internal color lookup table mapping, text/graphics mode, overscan color, and color plane enable. The horizontal Pixel Panning and Pixel Padding Registers control pixel attributes on screen. External color palette registers handle CPU reads and writes to I/O address range 3C6h-3C9h. Some of the registers are located external to the 82C451 in the external color palette. Inmos IMSG176 (Brooktree BT471/476) compatible registers are documented in this manual.

EXTENSION REGISTERS

The 82C451 defines a set of extension registers which are addressed with the 7-bit Extension Register Index. The I/O port address (3Bx/3Dxh) and Read/Write access to the extension registers are controlled by the Extension Enable Register (103h).

The extension registers handle a variety of interfacing, compatibility, and display functions as discussed below. They are grouped into the following logical groups for discussion purposes:

1. Miscellaneous Registers include the 82C451 Version number, Dip Switch, CPU interface, paging control, memory mode control, and diagnostic functions.

2. General Purpose Registers handle video blanking and the video default color.

3. Backwards Compatibility Registers control Hercules, MDA, and CGA emulation modes. Write Protect functions are provided to increase flexibility in providing backwards compatibility.

4. Alternate Horizontal and Vertical Registers handle all horizontal and vertical timing, including sync, blank and offset. These are used for backwards compatibility.

Note: The state of most of the Standard VGA Registers is undefined at reset. All registers specific to the 82C451 (Extension Registers) are summarized in the Extension Register Table.

82C451 Global Control (Setup) Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
–	Setup Control	–	W	46E8h (PC-Bus only)	–	23
–	Global Enable	–	RW	102h & Setup mode	–	23
–	Extension Enable	–	RW	103h & Setup mode	–	24
–	Global ID	–	R	104h & Setup mode	–	24

SETUP CONTROL REGISTER
Write only at I/O Address 46E8h
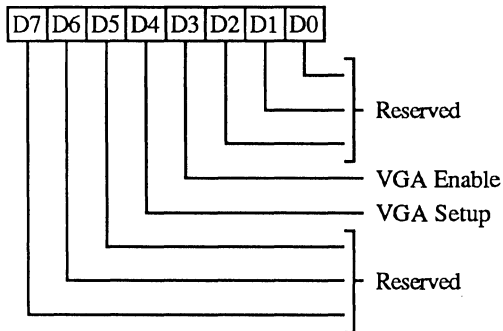
This register is used with the PC-Bus Interface only. It is cleared by RESET. In the MCA interface, the Setup mode and VGA Disable are controlled through the SETUP/ and DISA/ pins, respectively.

2-0 Reserved (0)

3 VGA Enable

    0: VGA is disabled
    1: VGA is enabled

4 Setup Mode

    0: VGA is in Normal Mode
    1: VGA is in Setup Mode

7-5 Reserved (0)

GLOBAL ENABLE REGISTER
Read/Write at I/O Address 102h
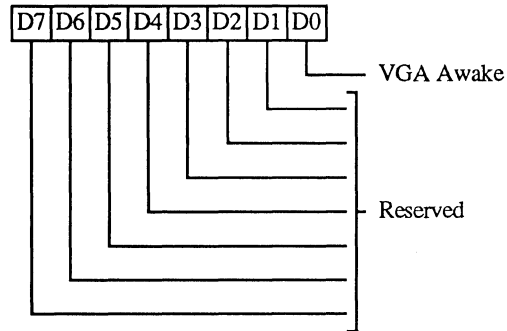
This register is only accessible in Setup Mode. It is cleared by RESET.

0 VGA Awake

    0: VGA is in sleep mode
    1: VGA is awake

7-1 Reserved (0)

EXTENSION ENABLE REGISTER
Read/Write at I/O Address 103h

Multiple VGA ID

Reserved

Extension Registers
Address Select

Extension Registers
Access Enable

This register is only accessible in Setup Mode. It is cleared by RESET.

4-0 Multiple VGA ID. The ID number of the currently active VGA when multiple VGA feature is enabled.

D4	D3	D2	D1	D0	Comment
0	0	0	0	0	1 82C451, no DIP switch to be compared against
0	0	0	0	1	1 82C451, no DIP switch to be compared against
0	0	0	1	x	2 82C451, 1 DIP switch to be compared against
0	0	1	x	x	4 82C451, 2 DIP switch to be compared against
0	1	x	x	x	8 82C451, 3 DIP switch to be compared against
1	x	x	x	x	16 82C451, 4 DIP switch to be compared against

5 Reserved (0)

6 Address for Extension Registers

0: Extension registers at I/O Address 3D6/3D7h
1: Extension registers at I/O Address 3B6/3B7h.

7 Extension Registers Access Enable. This bit controls access to the extension registers at 3D6/7 or 3B6/7. It also allows access to all CGA, MDA and Hercules registers in non-emulation mode.

0: Disable Access
1: Enable Access

The CRT Controller and CGA/Hercules Registers are dependent on this bit and the emulation mode as follows:

Bit 7	Emulation Mode	CRTC Address	CGA/Hercus Registers 3B8,3BF, 3D8, 3D9
0	VGA	3x4/5 only	not accessible
0	CGA	3D0/1,3D2/3 3D4/5,3D6/70	3D8,3D9 accessible
0	Hercules	3B0/1,3B2/3 3B4/5,3B6/7	3B8,3BF accessible
1	any	3x4/5 only	all accessible

GLOBAL ID REGISTER
Read only at I/O Address 104h
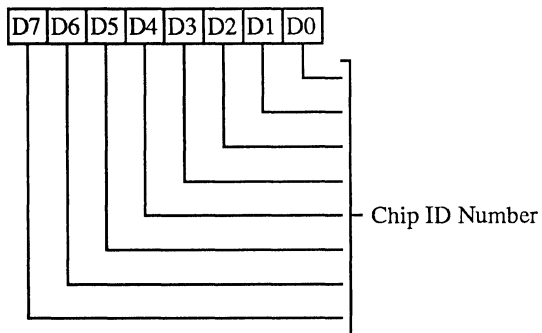
Chip ID Number

This register is only accessible in Setup Mode.

7-0 These bits contain the ID number (0A5h). This identifies the chip as a Chips and Technologies product.

82C451 General Control & Status Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ST00	Input Status 0	–	R	3C2h	–	25
ST01	Input Status 1	–	R	3BAh/3DAh	–	25
FCR	Feature Control	–	W	3BAh/3DAh	5	26
			R	3CAh		
MSR	Miscellaneous Output	–	W	3C2h	5	26
			R	3CCh		

INPUT STATUS REGISTER 0 (ST00)
Read only at I/O Address at 3C2h

- Reserved
- Switch Sense
- FCIN0
- FCIN1
- CRT Interrupt Pending
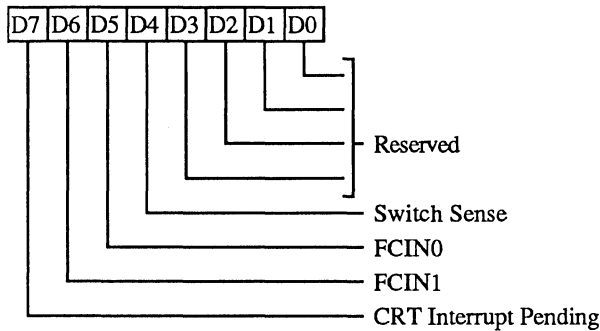
3-0   Reserved (0)

4   Switch Sense. This bit returns the Status of the SENSE pin.

6-5   These bits indicate the status of FCIN1 and FCIN0 input pins.

7   CRT Interrupt Pending

    0: Indicates no CRT interrupt is pending
    1: Indicates a CRT interrupt is waiting to be serviced

INPUT STATUS REGISTER 1 (ST01)
Read only at I/O Address 3BAh/3DAh

- DE/Hsync Output
- Reserved
- Vertical Retrace/Video
- Video Feedback
- Reserved
- Vsync Output
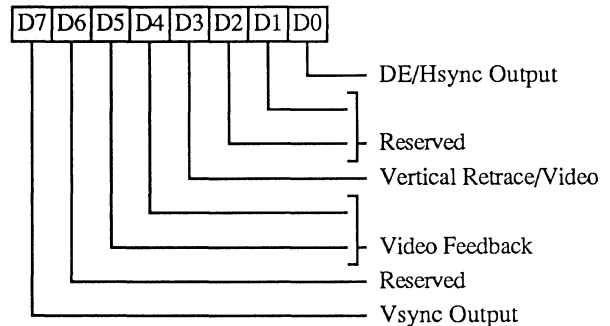
0   Display Enable/HSYNC Output. The functionality of this bit is controlled by the Emulation Mode register (XR14 D4).

    0: Indicates DE or HSYNC <u>inactive</u>
    1: Indicates DE or HSYNC <u>active</u>

2-1   Reserved (0)

3   Vertical Retrace/Video. The functionality of this bit is controlled by the Emulation Mode register (XR14 D5).

    0: Indicates VSYNC or video <u>inactive</u>
    1: Indicates VSYNC or video <u>active</u>

5-4   Video Feedback 1,0. These are diagnostic video bits which are selected via the Color Plane Enable Register.

6   Reserved (0)

7   Vsync Output. The functionality of this bit is controlled by the Emulation Mode register (XR14 D6). It reflects the active status of the VSYNC output: 0=inactive, 1=active.

FEATURE CONTROL REGISTER (FCR)
Write at I/O Address 3BAh/3DAh
Read at I/O Address 3CAh
Group 5 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- Feature Control
- Reserved
- Vsync Control
- Reserved
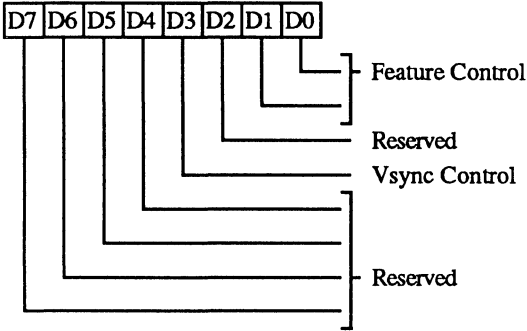
1-0 These two bits are inverted and output on the FCOUT1 and FCOUT0 pins.

2 Reserved (0)

3 Vsync Control   This bit is cleared by RESET.

    0: VSync output on the VSYNC pin
    1: Logical 'OR' of VSync and
       Display Enable output
       on the VSYNC pin

7-4 Reserved (0)

MISCELLANEOUS OUTPUT REGISTER (MSR)
Write at I/O Address 3C2h
Read at I/O Address 3CCh
Group 5 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- I/O Address Select
- RAM Enable
- Clock Select
- Reserved
- Page Select
- Hsync Polarity
- Vsync Polarity
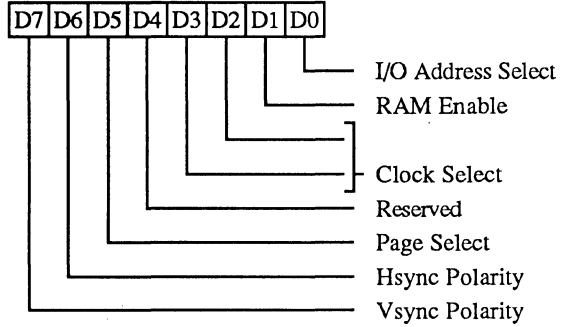
This register is cleared by RESET.

0 I/O Address Select. This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01).

    0: Select 3Bxh I/O address
    1: Select 3Dxh I/O address

1 Enable RAM

    0: Prevent CPU access to display memory.
    1: Allow CPU access to display memory.

3-2 Clock Select. These bits select the dot clock source for the CRT interface:

32	Clock Source Selected
00	CLK0
01	CLK1
10	CLK2
11	Not Used

4 Reserved (0)

5 Page Select. In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64K byte page in display memory for CPU access: 1=select lower page; 0=select upper page.

6 CRT Hsync Polarity. 0=pos, 1=neg

7 CRT Vsync Polarity. 0=pos, 1=neg

(Blank pin polarity can be controlled via the Video Interface Register)

82C451 CGA / Hercules Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
MODE	CGA/Hercules Mode	–	RW	3D8h	–	27
COLOR	CGA Color Select	–	RW	3D9h	–	28
HCFG	Hercules Configuration	–	RW	3BFh	–	29

CGA / HERCULES MODE CONTROL REGISTER (MODE)
Read/Write at I/O Address 3B8h/3D8h
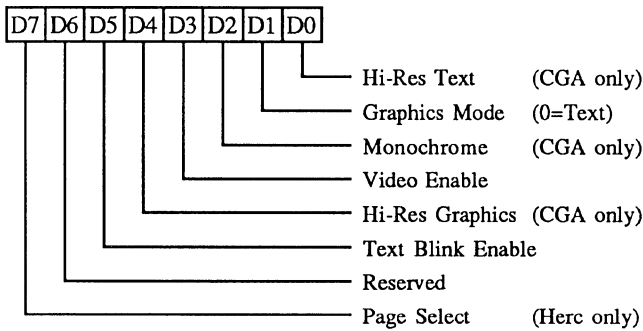
This register is effective only in CGA and Hercules modes. It is accessible if CGA or Hercules emulation mode is selected or the extension registers are enabled. If the extension registers are enabled, the address is determined by the address select in the Miscellaneous Outputs register. Otherwise the address is determined by the emulation mode. It is cleared by RESET.

0   CGA 80/40 Column Text Mode
   0:   Select 40 column CGA text mode
   1:   Select 80 column CGA text mode

1   CGA/Hercules Graphics/Text Mode
   0:   Select text mode
   1:   Select graphics mode

2   CGA Mono/Color Mode
   0:   Select CGA color mode
   1:   Select CGA monochrome mode

3   CGA/Hercules Video Enable
   0:   Blank the screen
   1:   Enable video output

4   CGA High Resolution Mode
   0:   Select 320x200 graphics mode
   1:   Select 640x200 graphics mode

5   CGA/Hercules Text Blink Enable
   0:   Disable character blink attribute (blink attribute bit-7 used to control background intensity)
   1:   Enable character blink attribute

6   Reserved (0)

7   Hercules Page Select
   0:   Select the lower part of memory (starting address B0000h) in Hercules Graphics Mode
   1:   Select the upper part of the memory (starting address B8000h) in Hercules Graphics Mode

CGA COLOR SELECT REGISTER
Read/Write at I/O Address 3D9h


```
D7 D6 D5 D4 D3 D2 D1 D0
```
Color bit-0 (Blue)
Color bit-1 (Green)
Color bit-2 (Red)
Color bit-3 (Intensity)
Intensity Enable
Color Set Select
Reserved
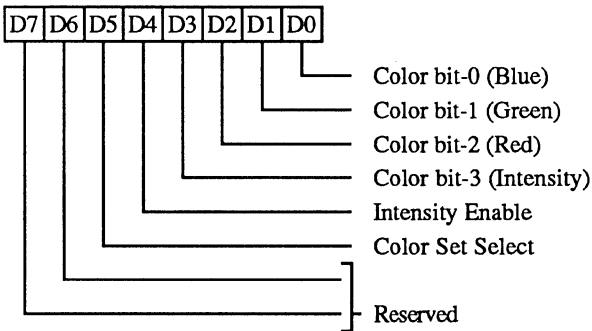
This register is effective only in CGA modes. It is accessible if CGA emulation mode is selected or the extension registers are enabled. This register may also be read or written as an Extension Register (XR7E). It is cleared by RESET. In Hercules Graphics mode, this register should be accessed at 7Eh. A value of 0Fh in 7Eh will work for the Hercules Graphics mode.

3-0   Color

320x200 4-color: Background Color (color when the pixel value is 0)

The foreground colors (colors when the pixel value is 1-3) are determined by bit-5 of this register.

640x200 2-color: Foreground Color (color when the pixel value is 1)

The background color (color when the pixel value is 0) is black.

4   Intensity Enable

Text Mode: Enables intensified background colors

320x200 4-color: Enables intensified colors 0-3

640x200 2-color: Don't care

5   Color Set Select. This bit selects one of two available CGA color palettes to be used in 320x200 graphics mode (it is ignored in all other modes) according to the following table:

Pixel Value	Color Set 0	Color Set 1
0 0	Color per bits 0-3	Color per bits 0-3
0 1	Green	Cyan
1 0	Red	Magenta
1 1	Brown	White

7-6   Reserved (0)

HERCULES CONFIGURATION REGISTER (HCFG)
Write only at I/O Address 3BFh
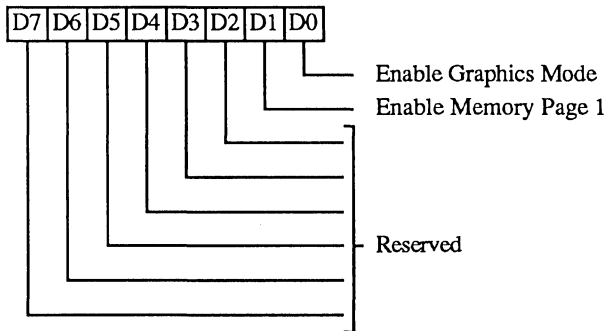
This register is effective only in Hercules mode. It is accessible in Hercules emulation mode or if the extension registers are enabled. It may be read back through XR14 D3 & D2. It is cleared by RESET.

0   Enable Graphics Mode

> 0: Lock the 82C451 in Hercules text mode. In this mode, the CPU has access only to memory address range B0000h-B7FFFh.
>
> 1: Permit entry to Hercules Graphics mode.

1   Enable Memory Page 1

> 0: Prevent setting of the Page Select bit (bit 7 of the Hercules Mode Control Register). This function also restricts memory usage to addresses B0000h-B7FFFh.
>
> 1: The Page Select bit can be set and the upper part of display memory (addresses B8000h - BFFFFh) is available.

7-2   Reserved (0)

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82C451 Sequencer Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SRX	Sequencer Index	–	RW	3C4h	1	31
SR00	Reset	00h	RW	3C5h	1	31
SR01	Clocking Mode	01h	RW	3C5h	1	32
SR02	Plane/Map Mask	02h	RW	3C5h	1	32
SR03	Character Font	03h	RW	3C5h	1	33
SR04	Memory Mode	04h	RW	3C5h	1	34
SR07	Horizontal Character Counter Reset	07h	W	3C5h	–	34

SEQUENCER INDEX REGISTER (SRX)
Read/Write at I/O Address 3C4h
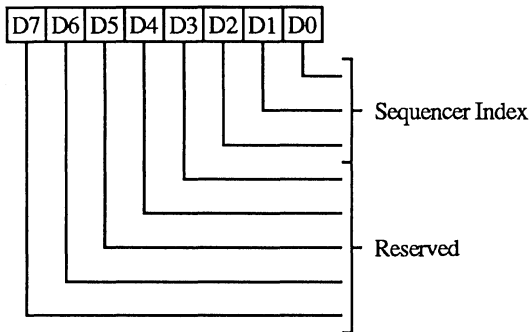
This register is cleared by RESET.

2-0   These bits contain a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7.

7-3   Reserved (0)

SEQUENCER RESET REGISTER (SR00)
Read/Write at I/O Address 3C5h
Index 00h
Group 1 Protection
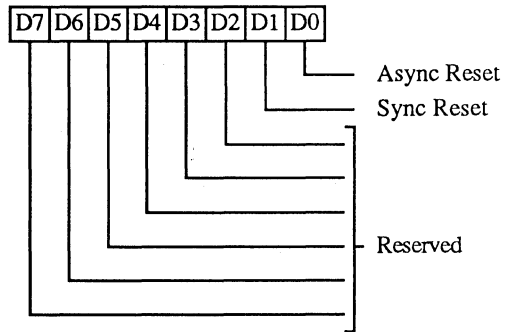
0   Asynchronous Reset

   0: Force asynchronous reset
   1: Normal operation

   Display memory data will be corrupted if this bit is set to zero.

1   Synchronous Reset

   0: Force synchronous reset
   1: Normal operation

   Display memory data is not corrupted if this bit is set to zero for a short period of time (a few tens of microseconds).

7-2   Reserved (0)

SEQUENCER CLOCKING MODE REGISTER (SR01)
Read/Write at I/O Address 3C5h
Index 01h
Group 1 Protection

D7 D6 D5 D4 D3 D2 D1 D0
- 8/9 Dot Clocks
- Reserved
- Shift Load
- Input Clock Divide
- Shift 4
- Screen Off
- Reserved
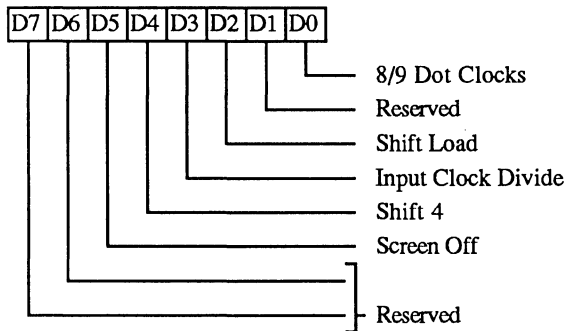
0 **8/9 Dot Clocks.** This bit determines whether a character clock is 8 or 9 dot clocks long.

    0: Select 9 dots/character clock
    1: Select 8 dots/character clock

1 Reserved (0)

2 Shift Load

    0: Load video data shift registers <u>every</u> character clock.
    1: Load video data shift registers <u>every other</u> character clock.

Bit-4 of this register must be 0 for this bit to be effective.

3 Input Clock Divide

    0: Sequencer master clock output on the PCLK pin (used for 640 (720) pixel modes).
    1: Master clock divided by 2 output on the PCLK pin (used for 320 (360) pixel modes).

4 Shift 4

    0: Load video shift registers every 1 or 2 character clocks (depending on bit-2 of this register).
    1: Load shift registers every 4th character clock.

5 Screen Off

    0: Normal Operation.
    1: Disable video output and assign all display memory bandwidth for CPU accesses.

7-6 Reserved (0)

SEQUENCER PLANE/MAP MASK REGISTER (SR02)
Read/Write at I/O Address 3C5h
Index 02h
Group 1 Protection

D7 D6 D5 D4 D3 D2 D1 D0
- Color Plane Enable
- Reserved
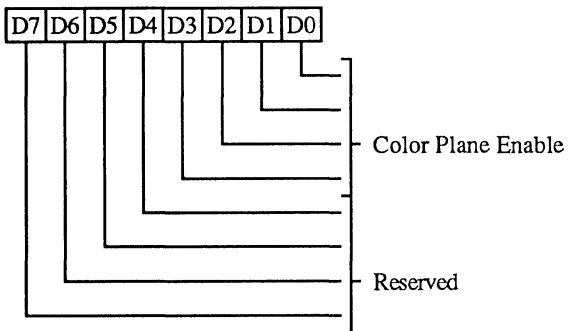
3-0 Color Plane Enable

    0: Write protect corresponding color plane.
    1: Allow write to corresponding color plane.

In Odd/Even and Quad modes, these bits still control access to the corresponding color plane.

7-4 Reserved (0)

CHARACTER FONT SELECT REGISTER (SR03)
Read/Write at I/O Address 3C5h
Index 03h
Group 1 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- Font Select B bit-1
- Font Select B bit-2
- Font Select A bit-1
- Font Select A bit-2
- Font Select B bit-0
- Font Select A bit-0
- Reserved
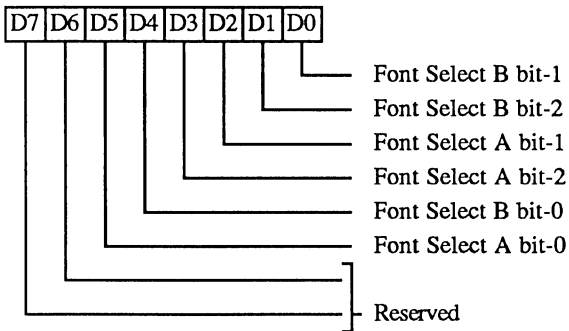
In text modes, bit-3 of the video data's attribute byte normally controls the foreground intensity. This bit may be redefined to control switching between character sets. This latter function is enabled whenever there is a difference in the values of the Character Font Select A and the Character Font Select B bits. If the two values are the same, the character select function is disabled and attribute bit-3 controls the foreground intensity.

SR04 bit-1 must be 1 for the character font select function to be active. Otherwise, only character fonts 0 and 4 are available.

1-0 High order bits of Character Generator Select B

3-2 High order bits of Character Generator Select A

4 Low order bit of Character Generator Select B

5 Low order bit of Character Generator Select A

7-6 Reserved (0)

The following table shows the display memory plane selected by the Character Generator Select A and B bits.

Code	Character Generator Table Location
0	First 8K of Plane 2
1	Second 8K of Plane 2
2	Third 8K of Plane 2
3	Fourth 8K of Plane 2
4	Fifth 8K of Plane 2
5	Sixth 8K of Plane 2
6	Seventh 8K of Plane 2
7	Eighth 8K of Plane 2

where 'code' is:

Character Generator Select A (bits 3, 2, 5) when bit-3 of the the attribute byte is one.

Character Generator Select B (bits 1, 0, 4) when bit-3 of the attribute byte is zero.

SEQUENCER MEMORY MODE REGISTER (SR04)
Read/Write at I/O Address 3C5h
Index 04h
Group 1 Protection
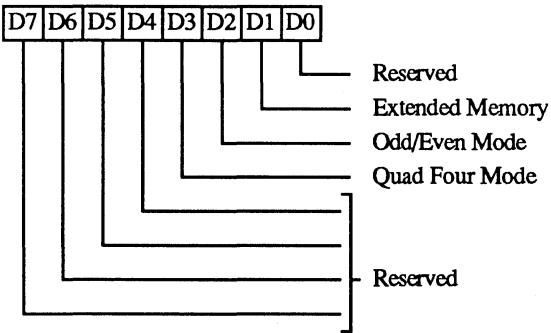
0 Reserved (0)

1 Extended Memory

0: Restrict CPU access to 4/16/32 Kbytes

1: Allow complete access to memory

This bit should normally be 1.

2 Odd/Even Mode

0: CPU accesses to Odd/Even addresses are directed to corresponding odd/even planes

1: All planes are accessed simultaneously (IRGB color)

Bit-3 of this register must be 0 for this bit to be effective. This bit affects only CPU <u>write</u> accesses to display memory.

3 Quad Four Mode

0: CPU addresses are mapped to display memory as defined by bit-2 of this register

1: CPU addresses are mapped to display memory modulo 4. The two low order CPU address bits select the display memory plane.

This bit affects both CPU reads and writes to display memory.

7-4 Reserved (0)

SEQUENCER HORIZONTAL CHARACTER COUNTER RESET (SR07)
Read/Write at I/O Address 3C5h
Index 07h
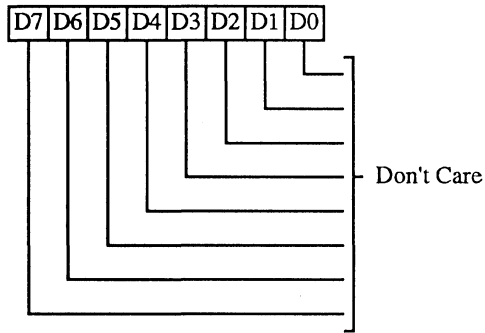
Writing to SR07 with any data will cause the horizontal character counter to be held reset (character counter output = 0) until a write to any other sequencer register with any data value. The write to any index in the range 0-6 clears the latch that is holding the reset condition on the character counter.

The vertical line counter is clocked by a signal derived from horizontal display enable (which does not occur if the horizontal counter is held reset). Therefore, if the write to SR07 occurs during vertical retrace, the horizontal and vertical counters will both be set to zero. A write to any other sequencer register may then be used to start both counters with reasonable synchronization to an external event via software control.

This is a standard VGA register which was not documented by IBM.

82C451 CRT Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
CRX	CRTC Index	–	RW	3B4h/3D4h	–	36
CR00	Horizontal Total	00h	RW	3B5h/3D5h	0	36
CR01	Horizontal Display Enable End	01h	RW	3B5h/3D5h	0	36
CR02	Horizontal Blank Start	02h	RW	3B5h/3D5h	0	37
CR03	Horizontal Blank End	03h	RW	3B5h/3D5h	0	37
CR04	Horizontal Sync Start	04h	RW	3B5h/3D5h	0	38
CR05	Horizontal Sync End	05h	RW	3B5h/3D5h	0	38
CR06	Vertical Total	06h	RW	3B5h/3D5h	0	39
CR07	Overflow	07h	RW	3B5h/3D5h	0/3	39
CR08	Preset Row Scan	08h	RW	3B5h/3D5h	3	40
CR09	Maximum Scan Line	09h	RW	3B5h/3D5h	2/4	40
CR0A	Cursor Start Scan Line	0Ah	RW	3B5h/3D5h	2	41
CR0B	Cursor End Scan Line	0Bh	RW	3B5h/3D5h	2	41
CR0C	Start Address High	0Ch	RW	3B5h/3D5h	–	42
CR0D	Start Address Low	0Dh	RW	3B5h/3D5h	–	42
CR0E	Cursor Location High	0Eh	RW	3B5h/3D5h	–	42
CR0F	Cursor Location Low	0Fh	RW	3B5h/3D5h	–	42
CR10	Vertical Sync Start (See Note 2)	10h	W or RW	3B5h/3D5h	4	43
CR11	Vertical Sync End (See Note 2)	11h	W or RW	3B5h/3D5h	3/4	43
CR10	Lightpen High (See Note 2)	10h	R	3B5h/3D5h	–	43
CR11	Lightpen Low (See Note 2)	11h	R	3B5h/3D5h	–	43
CR12	Vertical Display Enable End	12h	RW	3B5h/3D5h	4	44
CR13	Offset	13h	RW	3B5h/3D5h	3	44
CR14	Underline Row	14h	RW	3B5h/3D5h	3	44
CR15	Vertical Blank Start	15h	RW	3B5h/3D5h	4	45
CR16	Vertical Blank End	16h	RW	3B5h/3D5h	4	45
CR17	CRT Mode Control	17h	RW	3B5h/3D5h	3/4	46
CR18	Line Compare	18h	RW	3B5h/3D5h	3	47
CR22	Memory Data Latches	22h	R	3B5h/3D5h	–	48
CR24	Attribute Controller Toggle	24h	R	3B5h/3D5h	–	48
CR3X	Clear Vertical Display Enable	3xh	W	3B5h/3D5h	–	48

Note 1: When MDA or Hercules emulation is enabled, the CRTC I/O address should be set to 3B0h-3B7h by setting the I/O address select bit in the Miscellaneous Output register (3C2h/3CCh bit-0) to zero. When CGA emulation is enabled, the CRTC I/O address should be set to 3D0h-3D7h by setting Misc Output Register bit-0 to 1.

Note 2: In both the EGA and VGA, the light pen registers are at index locations conflicting with the vertical sync registers. This would normally prevent reads and writes from occurring at the same index. Since the light pen registers are not normally useful, the VGA provides software control (CR03 D7) of whether the vertical sync or light pen registers are readable at indices 10-11.

CRTC INDEX REGISTER (CRX)
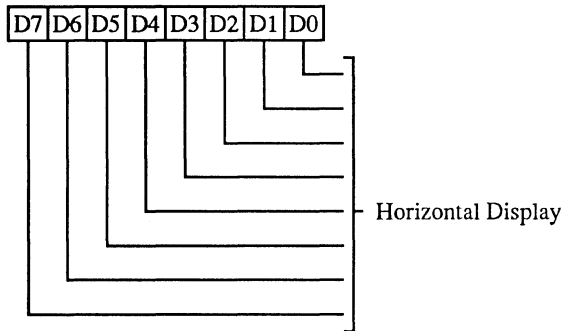*Read/Write at I/O Address 3B4h/3D4h*
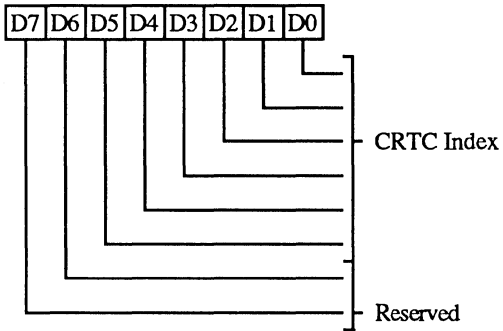
5-0   CRTC data register index

7-6   Reserved (0)

HORIZONTAL TOTAL REGISTER (CR00)
Read/Write at I/O Address 3B5h/3D5h
Index 00h
Group 0 protection

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.
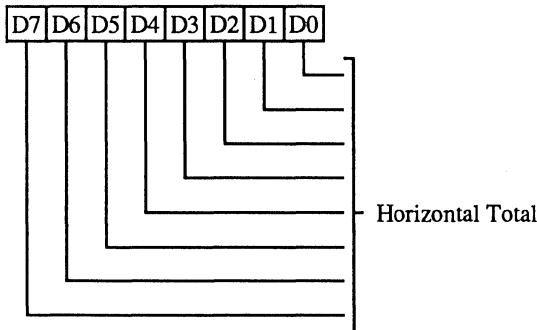
7-0   Horizontal Total. Total number of character clocks per line = contents of this register + 5. This register determines the horizontal sweep rate.

HORIZONTAL DISPLAY ENABLE END REGISTER (CR01)
Read/Write at I/O Address 3B5h/3D5h
Index 01h
Group 0 protection

This register is used for all VGA and EGA modes on CRTs. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0   Number of Characters displayed per scan line - 1.

HORIZONTAL BLANK START REGISTER (CR02)
Read/Write at I/O Address 3B5h/3D5h
Index 02h
Group 0 protection
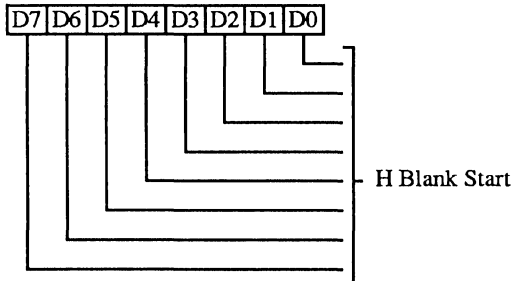
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

— H Blank Start

HORIZONTAL BLANK END REGISTER (CR03)
Read/Write at I/O Address 3B5h/3D5h
Index 03h
Group 0 protection
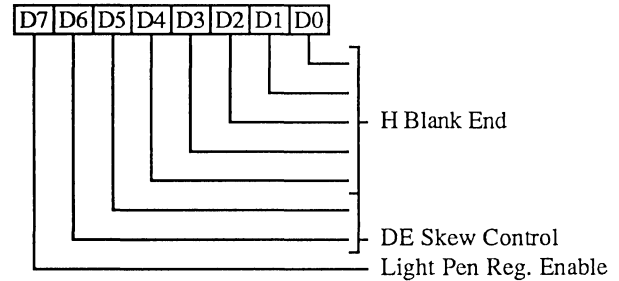
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

— H Blank End
— DE Skew Control
— Light Pen Reg. Enable

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 These bits specify the beginning of horizontal blank in terms of character clocks from the beginning of the display scan. The period between Horizontal Display Enable End and Horizontal Blank Start is the right side border on screen.

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0 These are the lower 5 bits of the character clock count used to define the end of horizontal blank. The interval between the end of horizontal blank and the beginning of the display (a count of 0) is the left side border on the screen. The horizontal blanking width, W, is: Value in Start Blanking Register + W = 6-bit value. Lower 5 bits programmed in this register, 6th bit programmed in bit 7 of CR05.

6-5 Display Enable Skew Control: Defines the number of character clocks that the Display Enable signal is delayed to compensate for internal pipeline delays.

7 Light Pen Reg. Enable: Must be 1 for normal operation; when this bit is 0, CRTC registers CR10 and CR11 function as lightpen readback registers.

HORIZONTAL SYNC START
REGISTER (CR04)
Read/Write at I/O Address 3B5h/3D5h
Index 04h
Group 0 protection
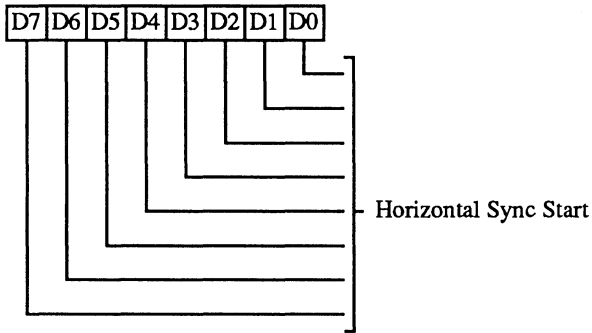
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Horizontal Sync Start

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0   These bits specify the beginning of HSYNC in terms of Character clocks from the beginning of the display scan. These bits also determine display centering on the screen.

HORIZONTAL SYNC END
REGISTER (CR05)
Read/Write at I/O Address 3B5h/3D5h
Index 05h
Group 0 protection
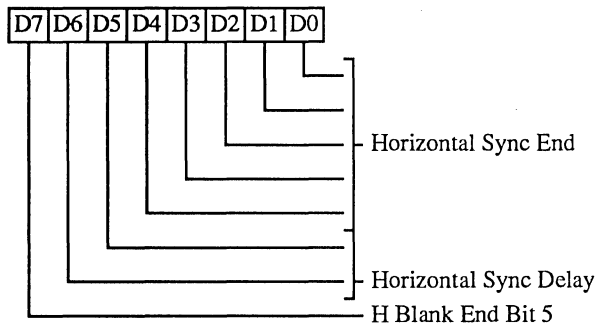
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Horizontal Sync End

Horizontal Sync Delay
H Blank End Bit 5

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0   HSYNC End. Lower 5 bits of the character clock count which specifies the end of Horizontal Sync. The horizontal sync width, W, is: Value in Start Retrace Register + W = 5-bit value to be programmed in this register.

6-5   Horizontal Sync Delay. These bits specify the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.

7   Horizontal Blank End Bit 5. Sixth bit of the Horizontal Blank End Register (CR03).

VERTICAL TOTAL REGISTER (CR06)
Read/Write at I/O Address 3B5h/3D5h
Index 06h
Group 0 protection
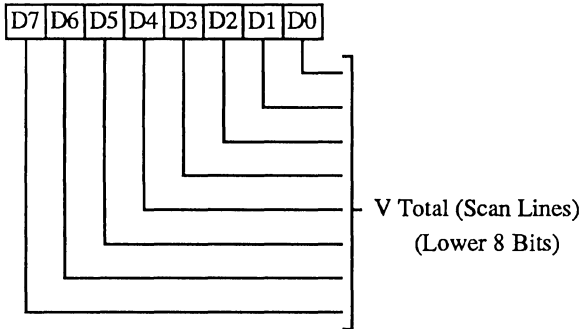
V Total (Scan Lines)
(Lower 8 Bits)

This register is used in all modes.

7-0 These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow Register. The Vertical Total value specifies the total number of scan lines (horizontal retrace periods) per frame.
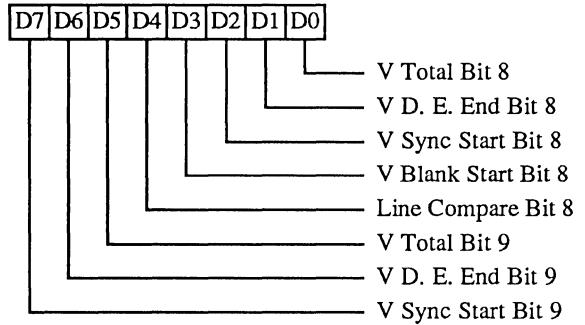
Programmed Count = Actual Count − 2

OVERFLOW REGISTER (CR07)
Read/Write at I/O Address 3B5h/3D5h
Index 07h
Group 0 protection on bits 0-3 and bits 5-7
Group 3 protection on bit 4

V Total Bit 8
V D. E. End Bit 8
V Sync Start Bit 8
V Blank Start Bit 8
Line Compare Bit 8
V Total Bit 9
V D. E. End Bit 9
V Sync Start Bit 9

This register is used in all modes.

0 Vertical Total Bit 8

1 Vertical Display Enable End Bit 8

2 Vertical Sync Start Bit 8

3 Vertical Blank Start Bit 8

4 Line Compare Bit 8

5 Vertical Total Bit 9

6 Vertical Display Enable End Bit 9

7 Vertical Sync Start Bit 9

PRESET ROW SCAN REGISTER (CR08)
Read/Write at I/O Address 3B5h/3D5h
Index 08h
Group 3 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- Start Row Scan Count
- Byte Panning Control
- Reserved
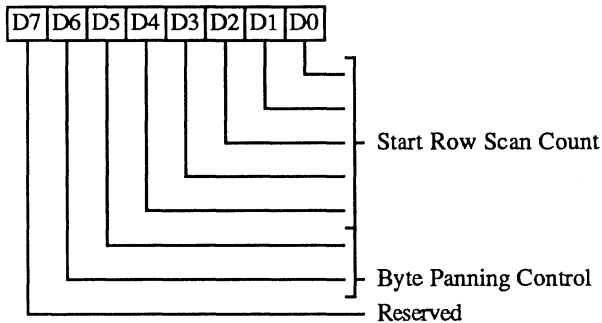
4-0 These bits specify the starting row scan count after each vertical retrace. Every horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count during active display. This register is used for soft scrolling in text modes.

6-5 Byte Panning Control. These bits specify the lower order bits for the display start address. They are used for horizontal panning in Odd/Even and Quad modes.

7 Reserved (0)

MAXIMUM SCAN LINE REGISTER (CR09)
Read/Write at I/O Address 3B5h/3D5h
Index 09h
Group 2 protection on bits 0-4
Group 4 Protection on bit 5-7

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- Scan Lines Per Row
- V Blank Start Bit 9
- Line Compare Bit 9
- Double Scan
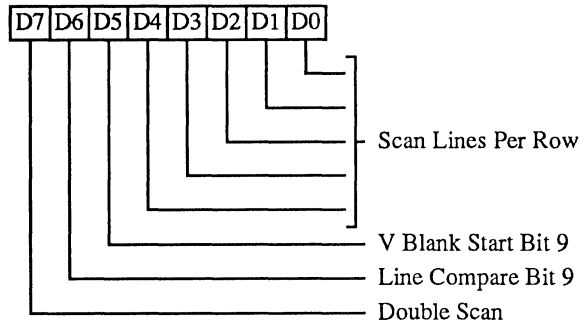
4-0 These bits specify the number of scan lines in a row: Number of scan lines per row = value + 1.

5 Bit 9 of the Vertical Blank Start register

6 Bit 9 of the Line Compare register

7 Double Scan

　　0: Normal Operation
　　1: Enable scan line doubling

The vertical parameters in the CRT Controller (even for a split screen) are not affected, only the CRTC row scan counter (bits 0-4 of this register) and display memory addressing screen refresh are affected.

CURSOR START SCAN LINE
REGISTER (CR0A)
Read/Write at I/O Address 3B5h/3D5h
Index 0Ah
Group 2 Protection
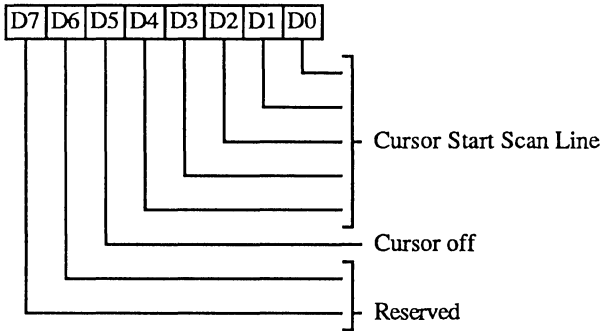
4-0   These bits specify the scan line of the character row where the cursor display begins.

5   Cursor Off

        0: Text Cursor On
        1: Text Cursor Off

7-6   Reserved (0)

CURSOR END SCAN LINE
REGISTER (CR0B)
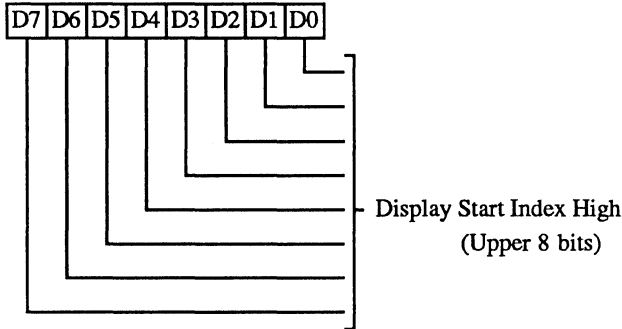*Read/Write at I/O Address 3B5h/3D5h*
Index 0Bh
Group 2 protection
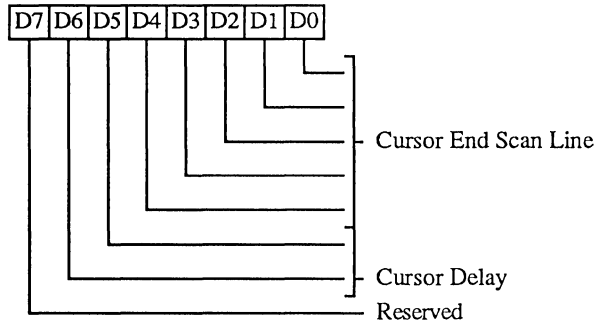
4-0   These bits specify the scan line of a character row where the cursor display ends: Last scan line for the block cursor = Value + 1.

6-5   These bits define the number of character clocks that the cursor is delayed to compensate for internal pipeline delay.

7   Reserved (0)

Note: If the Cursor Start Line is greater than the Cursor End Line, then no cursor is generated.

START INDEX HIGH REGISTER (CR0C)
Read/Write at I/O Address 3B5h/3D5h
Index 0Ch

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Display Start Index High
(Upper 8 bits)

7-0   Upper 8 bits of display start address. In CGA/MDA/Hercules modes, this register wraps around at the 16, 32, and 64 K byte boundaries respectively.

CURSOR LOCATION HIGH REGISTER (CR0E)
Read/Write at I/O Address 3B5h/3D5h
Index 0Eh

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Text Cursor Mem. Index
(Upper 8 bits)
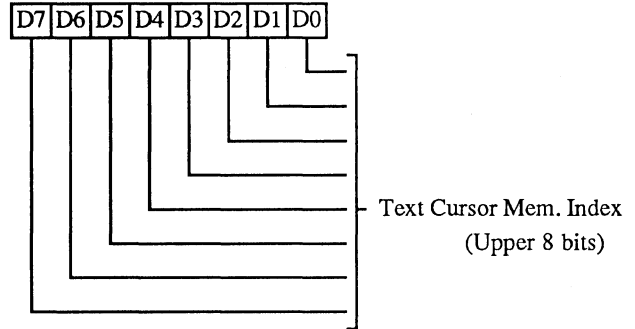
7-0   Upper 8 bits of the memory address where the text cursor is active. In CGA/MDA/Hercules modes, this register wraps around at 16, 32, and 64 K byte boundaries respectively.

START INDEX LOW REGISTER (CR0D)
Read/Write at I/O Address 3B5h/3D5h
Index 0Dh

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Display Start Index Low
(Lower 8 bits)
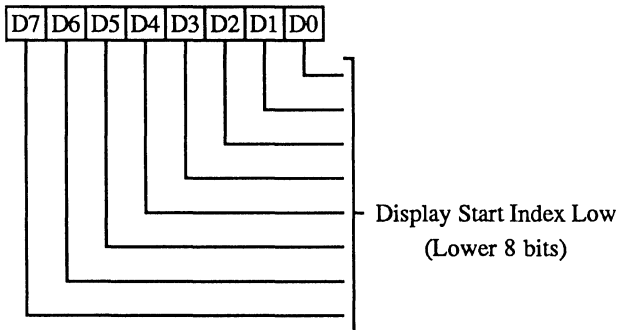
7-0   Lower 8 bits of the display start address. The display start address points to the memory address corresponding to the top left corner of the screen.

CURSOR LOCATION LOW REGISTER (CR0F)
Read/Write at I/O Address 3B5h/3D5h
Index 0Fh

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Text Cursor Mem. Index
(Lower 8 bits)
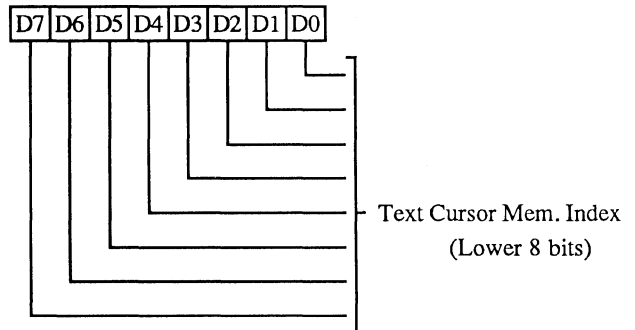
7-0   Lower 8 bits of the memory address where the text cursor is active. In CGA/MDA/Hercules modes, this register wraps around at 16, 32, and 64 K byte boundaries respectively.

LIGHTPEN HIGH REGISTER (CR10)
Read only at I/O Address 3B5h/3D5h
Index 10h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.
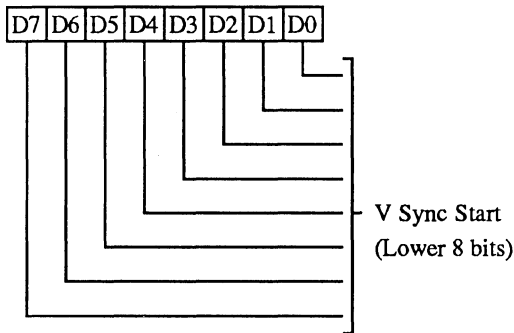
LIGHTPEN LOW REGISTER (CR11)
Read only at I/O Address 3B5h/3D5h
Index 11h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

VERTICAL SYNC START REGISTER (CR10)
Read/Write at I/O Address 3B5h/3D5h
Index 10h
Group 4 Protection

V Sync Start
(Lower 8 bits)

This register is used in all modes. This register is not readable in (Line Compare bit-9) MDA/Hercules emulation or when CR03 D7=1.

7-0 The eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRTC Overflow Register. They define the scan line position at which Vertical Sync becomes active.

VERTICAL SYNC END REGISTER (CR11)
Read/Write at I/O Address 3B5h/3D5h
Index 11h
Group 3 Protection for bits 4 and 5
Group 4 Protection for bits 0-3, 6 and 7

V Sync End
V Interrupt Clear
V Interrupt Enable
Select Refresh Type
Protect CRTC (Group 0)
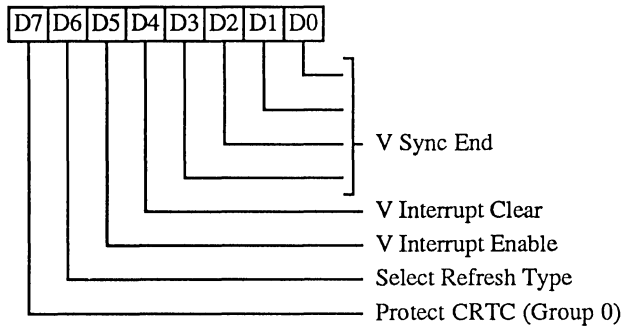
This register is used in all modes. This register is not readable in MDA/Hercules emulation or when CR03 D7=1.

3-0 Vertical Sync End. Lower 4 bits of the scan line count that defines the end of vertical sync. The vertical sync width, W, is: Value in vertical sync start register + W= 4-bit value to be programmed in this register.

4 Vertical Interrupt Clear. 0=Clear vertical interrupt generated on the IRQ output; 1=Normal operation. This bit is cleared by RESET.

5 Vertical Interrupt Enable. 0: Enable vertical interrupt; 1: Disable vertical interrupt. This bit is cleared by RESET.

6 Select Refresh Type:

   0: 3 refresh cycles per scan line
   1: 5 refresh cycles per scan line

7 Group Protect 0. This bit is logically ORed with XR15 D6 to determine the protection for group 0 registers. This bit is cleared by RESET.

   0: Enable writes to CR00-CR07
   1: Disable writes to CR00-CR07

CR07 D4 (Line Compare bit-8) is not affected by this bit.

VERTICAL DISPLAY ENABLE END REGISTER (CR12)
Read/Write at I/O Address 3B5h/3D5h
Index 12h
Group 4 protection

D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0

V Display Enable End
(Lower 8 bits)
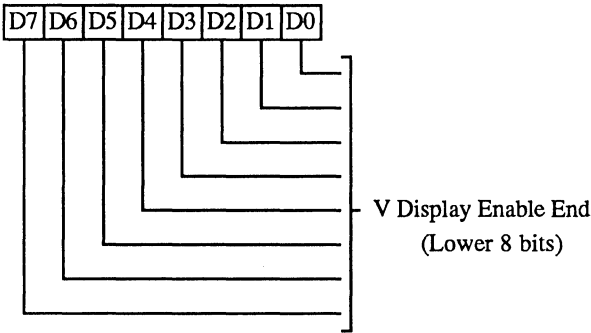
7-0 These are the eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow register. The actual count = Contents of this register + 1.

OFFSET REGISTER (CR13)
Read/Write at I/O Address 3B5h/3D5h
Index 13h
Group 3 protection

D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0

Display Buffer Width
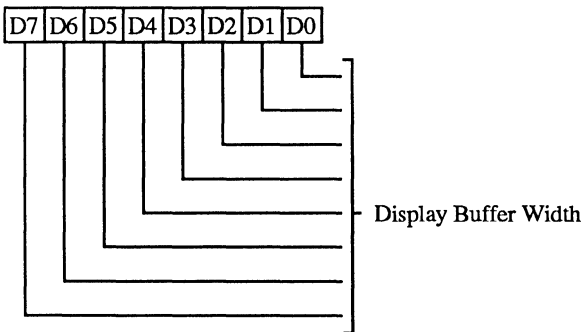
7-0 Display Buffer Width. The byte starting address of the next display row = Byte Start Address for current row + K* (CR13 where K = 2 in byte mode, K = 4 in word mode. Byte, word and double word mode is selected by bit-6 of CR17 and bit-6 of CR14. A less significant bit than bit-0 of this register is defined in the Auxiliary Offset register (XR0D). This allows finer resolution of the bit map width. Byte, word and doubleword mode affects the translation of the 'logical' display memory address to the 'physical' display memory address.

UNDERLINE LOCATION REGISTER (CR14)
Read/Write at I/O Address 3B5h/3D5h
Index 14h
Group 3 protection

D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0

Underline Position

Count by 4
Double word Mode
Reserved
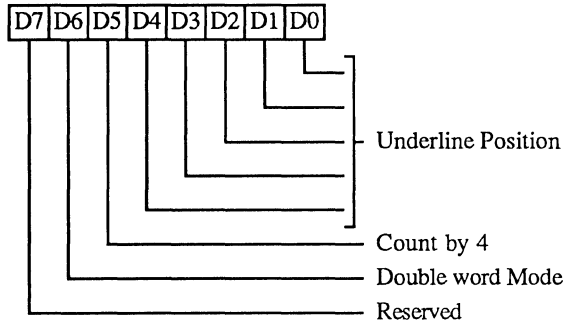
4-0 These bits specify the underline's scan line position within a character row. Value = Actual scan line number - 1.

5 Count by 4 for Double word Mode. 0: Frame Buffer Address is incremented by 1 or 2; 1: Frame Buffer Address is incremented by 4 or 2. See CR17 D3 for further details.

6 Double word Mode. 0: Frame Buffer Address is byte or word address; 1: Frame Buffer Address is doubleword address. Used in conjunction with CR17 D6 to select the display memory addressing mode.

7 Reserved (0)

VERTICAL BLANK START
REGISTER (CR15)
Read/Write at I/O Address 3B5h/3D5h
Index 15h
*Group 4 protection*
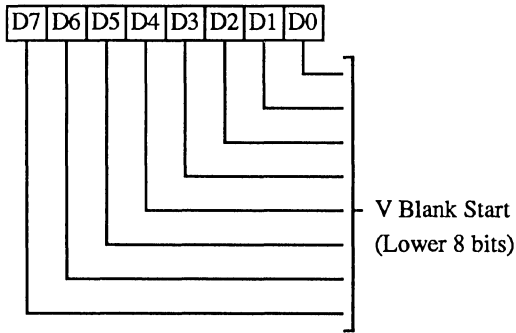
V Blank Start
(Lower 8 bits)

This register is used in all modes.

7-0 These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers respectively. Together these 10 bits define the scan line position where vertical blank begins. The interval between the end of the vertical display and the beginning of vertical blank is the bottom border on the screen.

VERTICAL BLANK END
REGISTER (CR16)
Read/Write at I/O Address 3B5h/3D5h
Index 16h
Group 4 protection

V Blank End
(Lower 8 bits)
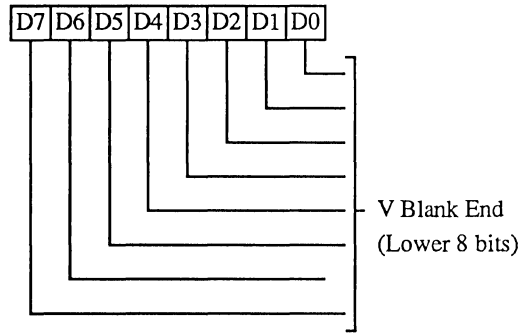
This register is used in all modes.

7-0 End Vertical Blank. These are the 8 low order bits of the scan line count which specifies the end of Vertical Blank. The vertical blank width, W, is: Value in Start Blanking Register - 1 + W= 8 bit value to be programmed in the register.
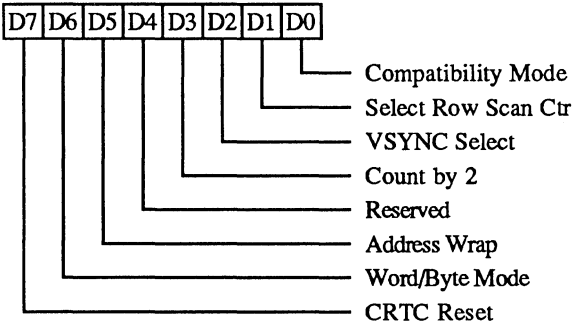
CRT MODE CONTROL REGISTER (CR17)
Read/Write at I/O Address 3B5h/3D5h
Index 17h
Group 3 Protection for bits 0,1 and 3-7
Group 4 Protection for bit 2.

D7	D6	D5	D4	D3	D2	D1	D0

- Compatibility Mode
- Select Row Scan Ctr
- VSYNC Select
- Count by 2
- Reserved
- Address Wrap
- Word/Byte Mode
- CRTC Reset

0 Compatibility Mode Support. This bit allows compatibility with the IBM CGA two-bank graphics mode. 0: The character row scan line counter bit 0 is substituted for memory address bit 13 during active display time; 1: normal operation, no substitution takes place.

1 Select Row Scan Counter. This bit allows compatibility with Hercules graphics and with any other 4-bank graphics system. 0: Substitute character row scan line counter bit 1 for memory address bit 14 during active display time; 1: normal operation, no substitution takes place.

2 Vertical Sync Select. This bit controls the vertical resolution of the CRT Controller by permitting selection of the clock rate input to the vertical counters. When set to 1, the vertical counters are clocked by the horizontal retrace clock divided by 2.

3 Count By Two

    0: Memory address counter is incremented every character clock
    1: Memory address counter is incremented every two character clocks, used in conjunction with bit 5 of 0Fh.

Note: This bit is used in conjunction with CR14 D5. The net effect is as follows:

CR14 D5	CR17 D3	Increment Addressing Every
0	0	1 CCLK
0	1	2 CCLK
1	0	4 CCLK
1	1	2 CCLK

Note: In Hercules graphics and Hi-res CGA modes, the address increments every two clocks.

4 Reserved (0)

5 Address Wrap (effective only in word mode.)

    0: Wrap display memory address at 16 Kbytes. This is used in IBM CGA mode.
    1: Normal operation (extended mode).

6 Word Mode or Byte Mode. 0: Word Mode is selected. In this mode the display memory address counter bits are shifted down by one, causing the most-significant bit of the counter to appear on the least-significant bit of the display memory address output; 1: Select byte mode.

Note: This bit is used in conjunction with CR14D6 to select byte, word, or double word memory addressing as follows:

CR14 D6	CR17 D6	Addressing Mode
0	0	Word Mode
0	1	Byte Mode
1	0	Double Word Mode
1	1	Double Word Mode

Display memory addresses are affected as shown in the table on the following page.

7 Hardware Reset (This bit is cleared by RESET)

    0: Force HSYNC and VSYNC to be inactive. No other registers or outputs affected.
    1: Normal Operation.

Display memory addresses are affected by CR17 D6 as shown in the table below:

Logical Memory Address	Physical Memory Address		
	Byte Mode	Word Mode	Double Word Mode
MA00	A00	Note 1	Note 2
MA01	A01	A00	Note 3
MA02	A02	A01	A00
MA03	A03	A02	A01
MA04	A04	A03	A02
MA05	A05	A04	A03
MA06	A06	A05	A04
MA07	A07	A06	A05
MA08	A08	A07	A06
MA09	A09	A08	A07
MA10	A10	A09	A08
MA11	A11	A10	A09
MA12	A12	A11	A10
MA13	A13	A12	A11
MA14	A14	A13	A12
MA15	A15	A14	A13

Note 1 = A13 * NOT CR17 D5 + A15 * CR17 D5
Note 2 = A12 x or (A14 * XR04 D2)
Note 3 = A13 x or (A15 * XR04 D2)

LINE COMPARE
REGISTER (CR18)
Read/Write at I/O Address 3B5h/3D5h
Index 18h
Group 3 protection

Line Compare Target
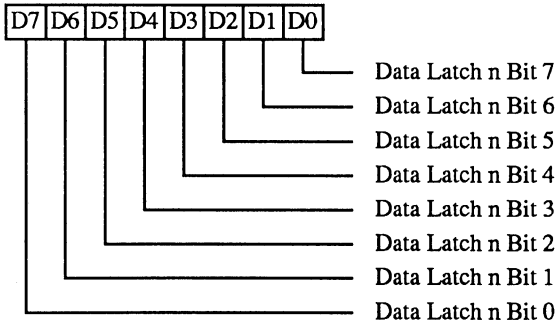(Lower 8 bits)
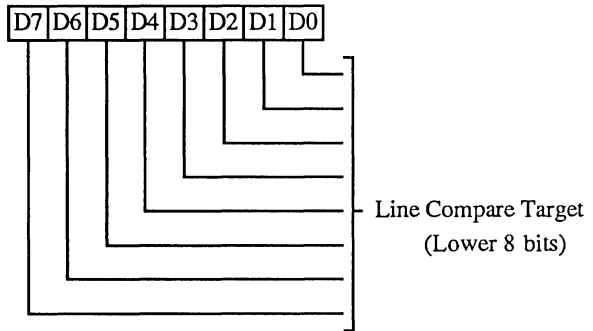
7-0 These are the low order 8 bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers, respectively. This register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address counter is cleared to 0. The display memory address counter then sequentially addresses the display memory starting at address 0. Each subsequent row address is generated by the addition of the Offset Register contents. This register is not affected by the double scanning bit (CR09 D7).

MEMORY DATA LATCH
REGISTER (CR22)
Read only at I/O Address 3B5h/3D5h
Index 22h

D7	D6	D5	D4	D3	D2	D1	D0

Data Latch n Bit 7
Data Latch n Bit 6
Data Latch n Bit 5
Data Latch n Bit 4
Data Latch n Bit 3
Data Latch n Bit 2
Data Latch n Bit 1
Data Latch n Bit 0

This register may be used to read the state of Graphics Controller Memory Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (GR04 D0 & D1) and is in the range 0-3.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

ATTRIBUTE CONTROLLER TOGGLE
REGISTER (CR24)
Read only at I/O Address 3B5h/3D5h
Index 24h

D7	D6	D5	D4	D3	D2	D1	D0

Index (0) / Data (1)
Reserved
Palette Address Source

Attribute
Controller
Index
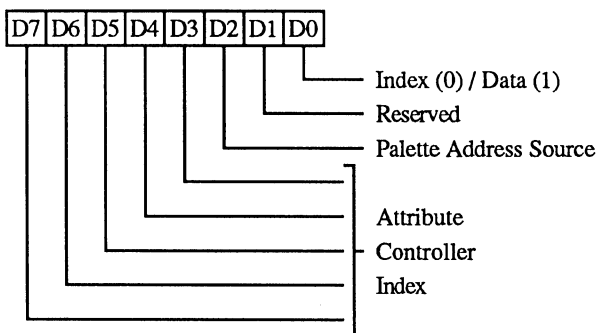
This register may be used to read back the state of the attribute controller index/data latch.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

CLEAR VERTICAL
DISPLAY ENABLE FFh (CR3X)
Write only at I/O Address 3B5h/3D5h
Index 3xh

D7	D6	D5	D4	D3	D2	D1	D0

Clear Vert Disp Ena FF

Ignored
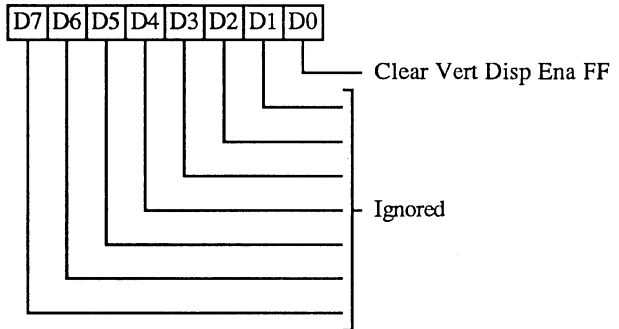
Writing odd data values to CRTC index 30-3Fh causes the vertical display enable flip-flop to be cleared. The flip-flop is automatically set by reaching vertical total. The effect of this is to force a longer vertical retrace period. There are two side effects of terminating vertical display enable early: first, the screen blanks early for one frame causing a minor visual disturbance and second, the sequencer gives more display memory cycles to the CPU because vertical display is not enabled.

Reads from this register are not decoded and will return indeterminate data.

This is a standard VGA register which was not documented by IBM.

Write Protect Register Grouping For CRT Registers

Register Number	Group 0	Group 2	Group 3	Group 4	Unprotected
CR00	Yes	-	-	-	-
CR01	-	Yes	-	-	-
CR02	Yes	-	-	-	-
CR03	Yes	-	-	-	-
CR04	Yes	-	-	-	-
CR05	Yes	-	-	-	-
CR06	Yes	-	-	-	-
CR07	Bits 0-3, 5-7		Bit 4	-	-
CR08	-	-	Yes	-	-
CR09	-	Bits 0-4	-	Bits 5-7	-
CR0A	-	Yes	-	-	-
CR0B	-	Yes	-	-	-
CR0C	-	-	-	-	Yes
CR0D	-	-	-	-	Yes
CR0E	-	-	-	-	Yes
CR0F	-	-	-	-	Yes
CR10	-	-	-	Yes	-
CR11	-	-	Bits 4-5	0-3,6	-
CR12	-	-	Yes	-	-
CR13	-	-	Yes	-	-
CR14	-	-	Yes	-	-
CR15	-	-	-	Yes	-
CR16	-	-	-	Yes	-
CR17	-	-	0,1,3-7	Bit 2	-
CR18	-	-	Yes	-	-

NOTE: All the registers at address 3Cx fall under group 1.

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82C451 Graphics Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
GRX	Graphics Index	–	RW	3CEh	1	51
GR00	Set/Reset	00h	RW	3CFh	1	51
GR01	Enable Set/Reset	01h	RW	3CFh	1	52
GR02	Color Compare	02h	RW	3CFh	1	52
GR03	Data Rotate	03h	RW	3CFh	1	53
GR04	Read Map Select	04h	RW	3CFh	1	53
GR05	Graphics mode	05h	RW	3CFh	1	54
GR06	Miscellaneous	06h	RW	3CFh	1	56
GR07	Color Don't Care	07h	RW	3CFh	1	56
GR08	Bit Mask	08h	RW	3CFh	1	57

GRAPHICS CONTROLLER INDEX REGISTER (GRX)
Read/Write at I/O Address 3CEh
Group 1 Protection

Index to Graphics Controller Data Registers
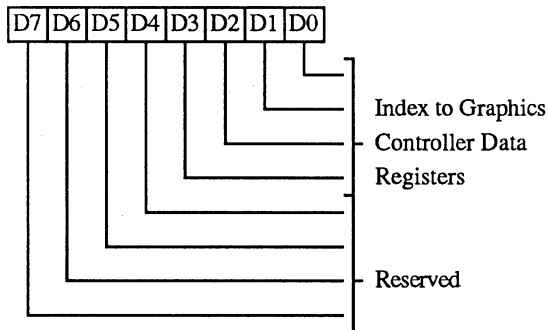
Reserved

3-0 4-bit index to Graphics Controller registers.

7-4 Reserved (0)

SET/RESET REGISTER (GR00)
Read/Write at I/O Address 3CFh
Index 00h
Group 1 Protection

Set/Reset Bit 0
Set/Reset Bit 1
Set/Reset Bit 2
Set/Reset Bit 3

Reserved
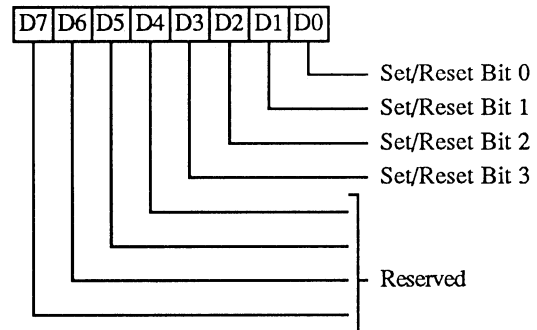
The SET/RESET and ENABLE SET/RESET registers are used to 'expand' 8 bits of CPU data to 32 bits of display memory.
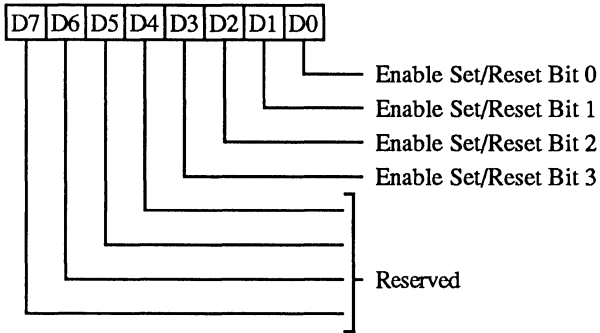
3-0 When the Graphics Mode register selects Write Mode 0, all 8 bits of each display memory plane are set as specified in the corresponding bit in this register. The Enable Set/Rest register (GR01) allows selection of some of the source of data to be written to individual planes. In Write Mode 3 (see GR05), these bits determine the color value.

7-4 Reserved (0)

ENABLE SET/RESET REGISTER (GR01)
Read/Write at I/O Address 3CFh
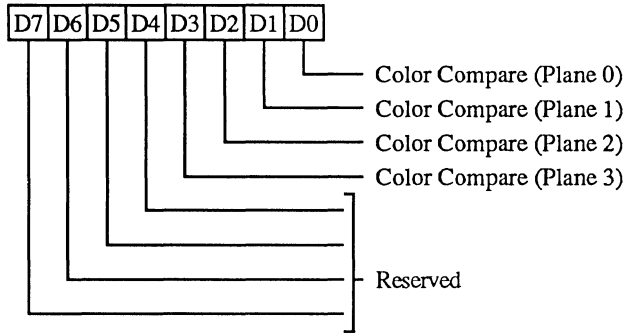*Index 01h*
Group 1 Protection

```
D7 D6 D5 D4 D3 D2 D1 D0
                     └─── Enable Set/Reset Bit 0
                  └────── Enable Set/Reset Bit 1
               └───────── Enable Set/Reset Bit 2
            └──────────── Enable Set/Reset Bit 3

                     ┐
                     ├─ Reserved
                     ┘
```

3-0 This register works in conjunction with the Set/Reset register (GR00). The Graphics Mode register must be programmed to Write Mode 0 in order for this register to have any effect.

    0: The corresponding plane is written with the data from the CPU data bus

    1: The corresponding plane is set to 0 or 1 as specified in the Set/Reset Register

7-4 Reserved (0)

COLOR COMPARE REGISTER (GR02)
Read/Write at I/O Address 3CFh
Index 02h
Group 1 Protection

```
D7 D6 D5 D4 D3 D2 D1 D0
                     └─── Color Compare (Plane 0)
                  └────── Color Compare (Plane 1)
               └───────── Color Compare (Plane 2)
            └──────────── Color Compare (Plane 3)

                     ┐
                     ├─ Reserved
                     ┘
```

3-0 This register is used to 'reduce' 32 bits of memory data to 8 bits for the CPU in 4-plane graphics mode. These bits provide a reference color value to compare to data read from display memory planes 0-3. The Color Don't Care register (GR07) is used to affect the result. This register is active only if the Graphics Mode register (GR05) is set to Read Mode 1. A match between the memory data and the Color Compare register (GR02) (for the bits specified in the Color Don't Care register) causes a logical 1 to be placed on the CPU data bus for the corresponding data bit, a mis-match returns a logical 0.
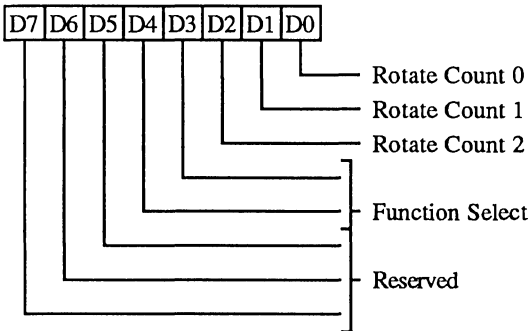
7-4 Reserved (0)

DATA ROTATE REGISTER (GR03)
Read/Write at I/O Address 3CFh
Index 03h
Group 1 Protection

2-0 These bits specify the number of bits to rotate to the right the data being written by the CPU. The CPU data bits are first rotated, then subjected to the logical operation as specified in the Function Select bit field. The rotate function is active only if the Graphics Mode register is programmed for Write Mode 0.

4-3 These Function Select bits specify the logical function performed on the contents of the processor latches (loaded on a previous CPU read cycle) before the data is written to display memory. These bits operate as follows:

Bit 4	Bit 3	Result
0	0	No change to the Data, Latches are updated;
0	1	Logical 'AND' between Data and latched data;
1	0	Logical 'OR' between Data and latched data;
1	1	Logical 'XOR' between Data and latched data.

7-5 Reserved (0)

READ MAP SELECT REGISTER (GR04)
Read/Write at I/O Address 3CFh
Index 04h
Group 1 Protection
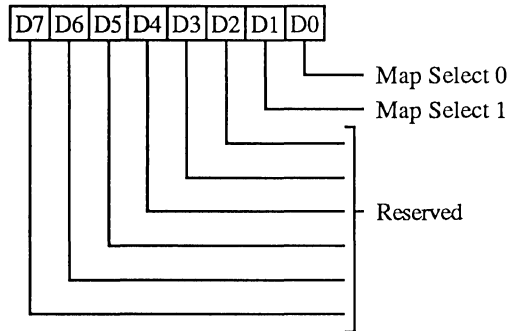
1-0 This register is also used to 'reduce' 32 bits of memory data to 8 bits for the CPU in the 4-plane graphics mode. These bits select the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even mode, bit-0 is ignored. In Quad mode, bits 0 and 1 are both ignored.

The four memory maps are selected as follows:

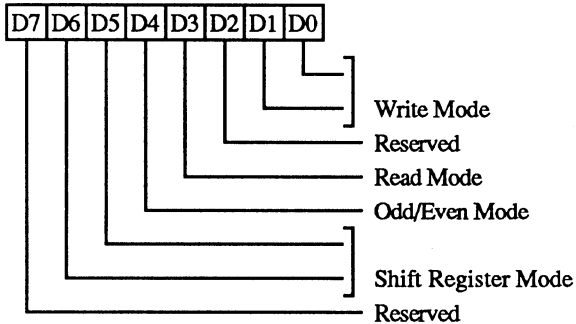| Bit 1	Bit 0	Map Selected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

7-2 Reserved (0)

GRAPHICS MODE REGISTER (GR05)
Read/Write at I/O Address 3CFh
Index 05h
Group 1 Protection

1-0 These bits specify the Write Mode as follows: (For 16-bit writes, the operation is repeated on the lower and upper bytes of CPU data).

D1	D0	Write Mode
0	0	**Write mode 0.** Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.
0	1	**Write mode 1.** Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.
1	0	**Write mode 2.** The CPU data bus data is treated as the color value for the addressed byte in planes 0-3. All eight pixels in the addressed byte are modified unless protected by the Bit Mask register setting. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the

processor latches. The Set/Reset and Enable Set/Reset registers are ignored. The Function Select bits in the Data Rotate register are used.

| 1 | 1 | **Write mode 3.** The CPU data is rotated then logically ANDed with the contents of the Bit Mask register (GR08) and then treated as the addressed data's bit mask, while the contents of the Set/Reset register is treated as the color value. |

A '0' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the corresponding pixel in the processor latches.

A '1' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the color value specified in the Set/Reset register.

The Enable Set/Reset register is ignored. The Data Rotate is used. This write mode can be used to fill an area with a single color and pattern.

2 Reserved (0)

3 This bit specifies the Read Mode as follows:

0: The CPU reads data from one of the planes as selected in the Read Map Select register.

1: The CPU reads the 8-bit result of the logical comparison between all eight pixels in the four display planes and the contents of the Color Compare and Color Don't Care registers. The CPU reads a logical 1 if a match occurs for each pixel and logical 0 if a mis-match occurs. In 16-bit read cycles, this operation is repeated on the lower and upper bytes.

4   Odd/Even Mode:

      0:   All CPU addresses sequentially access all planes

      1:   Even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for IBM CGA-compatible memory organization

6-5   Shift Register Mode. These two bits select the data shift pattern used when passing data from the four memory planes through the four video shift registers. If the data bits in the memory planes (0-3) are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7 respectively, then the data in the serial shift registers is shifted out as follows:

65	Last Bit Shifted Out			Shift Direction →				1st Bit Shifted Out	Output to:
00:	M0D0	M0D1	M0D2	M0D3	M0D4	M0D5	M0D6	M0D7	Bit0
	M1D0	M1D1	M1D2	M1D3	M1D4	M1D5	M1D6	M1D7	Bit1
	M2D0	M2D1	M2D2	M2D3	M2D4	M2D5	M2D6	M2D7	Bit2
	M3D0	M3D1	M3D2	M3D3	M3D4	M3D5	M3D6	M3D7	Bit3
01:	M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	Bit0
	M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	Bit1
	M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	Bit2
	M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	Bit3
1x:	M3D0	M3D4	M2D0	M2D4	M1D0	M1D4	M0D0	M0D4	Bit0
	M3D1	M3D5	M2D1	M2D5	M1D1	M1D5	M0D1	M0D5	Bit1
	M3D2	M2D2	M3D6	M2D6	M1D3	M1D6	M0D2	M0D6	Bit2
	M3D3	M3D7	M2D3	M2D7	M1D3	M1D7	M0D3	M0D7	Bit3

Note: If the Shift Register is not loaded every character clock (see SR01 D2 & D4) then the four 8-bit shift registers are effectively 'chained' with the output of shift register 1 becoming the input to shift register 0 and so on. This allows one to have a large monochrome (or 4 color) bit map and display one portion thereof.
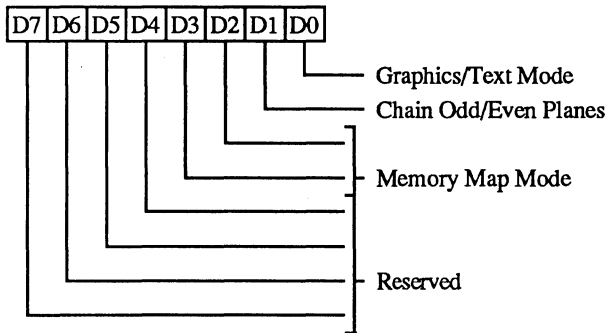
7   Reserved (0)

MISCELLANEOUS REGISTER (GR06)
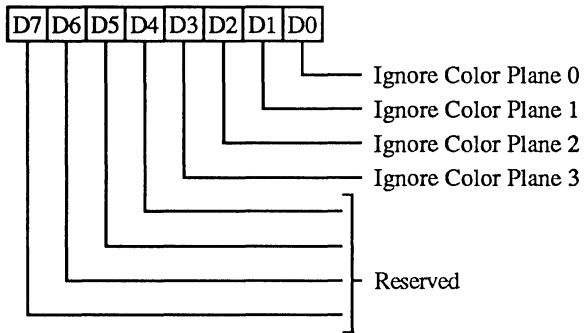*Read/Write at I/O Address 3CFh*
Index 06h
Group 1 Protection

D7 D6 D5 D4 D3 D2 D1 D0
— Graphics/Text Mode
— Chain Odd/Even Planes
— Memory Map Mode
— Reserved

0 Graphics/Text Mode

   0: Text Mode
   1: Graphics mode

1 Chain Odd/Even Planes. This mode can be used to double the address space into display memory.

   0: A0 not replaced
   1: CPU address bit A0 is replaced by a higher order address bit. The state of A0 determines which memory plane is to be selected:

      A0 = 0: select planes 0 and 2
      A0 = 1: select planes 1 and 3

3-2 Memory Map mode. These bits control the mapping of the display memory into the CPU address space as follows (also used in extended modes):

Bit 3	Bit 2	CPU Address
0	0	A0000h-BFFFFh
0	1	A0000h-AFFFFh
1	0	B0000h-B7FFFh
1	1	B8000h-BFFFFh

7-4 Reserved (0)

COLOR DON'T CARE REGISTER (GR07)
Read/Write at I/O Address 3CFh
Index 07h
Group 1 Protection

D7 D6 D5 D4 D3 D2 D1 D0
— Ignore Color Plane 0
— Ignore Color Plane 1
— Ignore Color Plane 2
— Ignore Color Plane 3
— Reserved

3-0 Ignore Color Plane (0-3)

   0: This causes the corresponding bit of the Color Compare register to be a don't care during a comparison.
   1: The corresponding bit of the Color Compare register is enabled for color comparison. This register is active in Read Mode 1 only.

7-4 Reserved (0)

BIT MASK REGISTER (GR08)
Read/Write at I/O Address 3CFh
Index 08h
Group 1 Protection

0=Immune to change
1=Change permitted
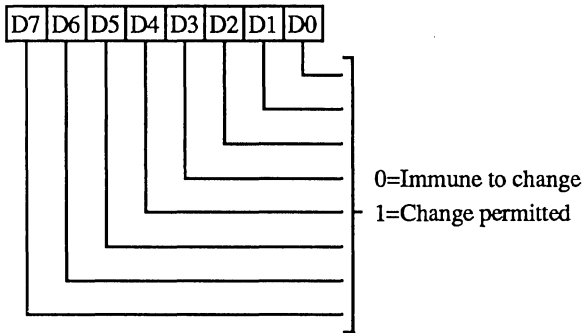
7-0 This bit mask is applicable to any data written by the CPU, including that subject to a rotate, logical function (AND, OR, XOR), Set/Reset, and No Change. In order to execute a proper read-modify-write cycle into displayed memory, each byte must first be read (and latched by the VGA), the Bit Mask register set, and the new data then written. The bit mask applies to all four planes simultaneously.

0: The corresponding bit in each of the four memory planes is written from the corresponding bit in the latches.

1: Unrestricted manipulation of the corresponding data bit in each of the four memory planes is permitted.

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82C451 Attribute Controller
and Color Palette Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ARX	Attribute Index (for 3C0/3C1h)	–	RW	3C0h	1	59
AR00-AR0F	Internal Color Palette Data	00-0Fh	RW	3C0h/3C1h	1	60
AR10	Mode Control	10h	RW	3C0h/3C1h	1	60
AR11	Overscan Color	11h	RW	3C0h/3C1h	1	61
AR12	Color Plane Enable	12h	RW	3C0h/3C1h	1	61
AR13	Horizontal Pixel Panning	13h	RW	3C0h/3C1h	1	62
AR14	Pixel Pad	14h	RW	3C0h/3C1h	1	62
DACMASK	External Color Palette Pixel Mask	–	RW	3C6h	6	63
DACSTATE	DAC State	–	R	3C7h	–	63
DACRX	External Color Palette Read-Mode Index	–	W	3C7h	6	64
DACX	External Color Palette Index (for 3C9h)	–	RW	3C8h	6	64
DACDATA	External Color Palette Data	00-FFh	RW	3C9h	6	64

In regular VGA mode, all Attribute Controller registers are located at the same byte address (3C0h) in the CPU I/O space. An internal flip-flop controls the selection of either the Attribute Index or Data Registers. To select the Index Register, an I/O Read is executed to address 3BAh/3DAh to clear this flip-flop. After the Index Register has been loaded by an I/O Write to address 3C0h, this flip-flop toggles, and the Data Register is ready to be accessed. Every I/O Write to address 3C0h toggles this flip-flop. The flip-flop does not have any effect on the reading of the Attribute Controller registers. The Attribute Controller index register is always read back at address 3C0h, the data register is always read back at address 3C1h.

In one of the extended modes (See "CPU Interface Register"), the Attribute Controller Index register is located at address 3C0h and the Attribute Controller Data register is located at address 3C1h (to allow word I/O accesses). In another extended mode, the Attribute Controller can be both read and written at either 3C0h or 3C1h (EGA compatible mode).

ATTRIBUTE INDEX
REGISTER (ARX)
Read/Write at I/O Address 3C0h
Group 1 Protection
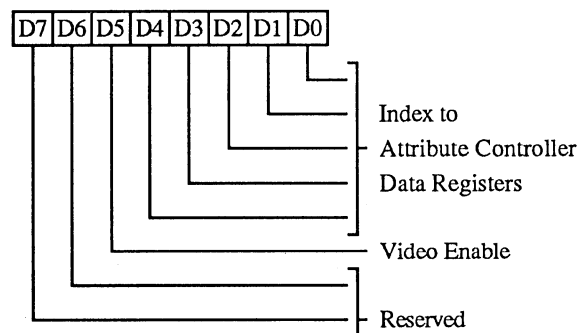
4-0 These bits point to one of the internal registers of the Attribute Controller
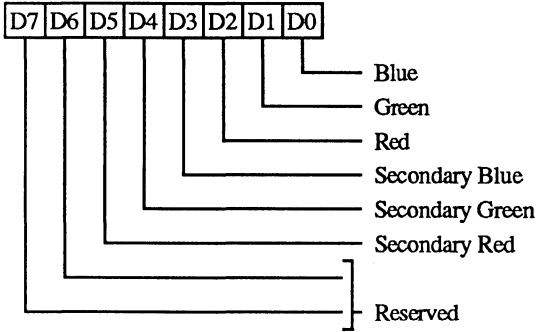
5 Enable Video:

　　0: Disables the video, allowing the Attribute Controller color registers to be accessed by the CPU.
　　1: Enables the video and causes the Attribute Controller Color registers (AR00-AR0F) to be inaccessible by the CPU.

7-6 Reserved (0)

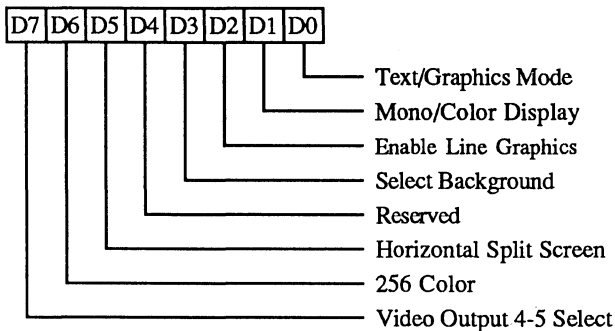## ATTRIBUTE CONTROLLER COLOR PALETTE DATA REGISTERS (AR00-AR0F)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 00-0Fh
Group 1 Protection

D7 D6 D5 D4 D3 D2 D1 D0
- Blue
- Green
- Red
- Secondary Blue
- Secondary Green
- Secondary Red
- Reserved

5-0 These bits are the color value in the respective palette register as pointed to by the index register.

7-6 Reserved (0)

ATTRIBUTE CONTROLLER MODE CONTROL REGISTER (AR10)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 10h
Group 1 Protection

D7 D6 D5 D4 D3 D2 D1 D0
- Text/Graphics Mode
- Mono/Color Display
- Enable Line Graphics
- Select Background
- Reserved
- Horizontal Split Screen
- 256 Color
- Video Output 4-5 Select

0 Text/Graphics Mode

    0: Select text mode
    1: Select graphics mode

1 Monochrome/Color Display

    0: Select color display attributes
    1: Select mono display attributes

2 Enable Line Graphics Character Codes. This bit is dependent on bit 0 of the Override register.

    0: Make the ninth pixel appear the same as the background.
    1: For special line graphics character codes (0C0h-0DFh), make the ninth pixel identical to the eighth pixel of the character. For other characters, the ninth pixel is the same as the background.

3 Enable Blink/Select Background Intensity. The blinking counter is clocked by the VSYNC signal. The Blink frequency is defined in the Blink Rate Control Register (XR60).

    0: Disable Blinking and enable text mode background intensity.
    1: Enable the blink attribute in text and graphics modes.

4 Reserved (0)

5 Split Screen Horizontal Panning Mode

    0: Scroll both screens horizontally as specified in the Pixel Panning register.
    1: Scroll horizontally only the top screen as specified in the Pixel panning register.

6 256 Color Output Assembler

    0: 6-bits of video (translated from 4-bits by the internal color palette) are output every dot clock.
    1: Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot clock (256 color mode).

7 Video Output 5-4 Select

    0: Video bits 4 and 5 are generated by the internal Attribute Controller color palette registers.
    1: Video bits 4 and 5 are the same as bits 0 and 1 in the Pixel Pad register (AR14).

OVERSCAN COLOR REGISTER (AR11)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 11H
Group 1 Protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```
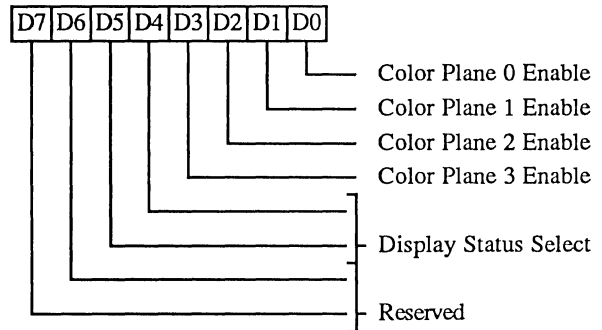— Overscan Color
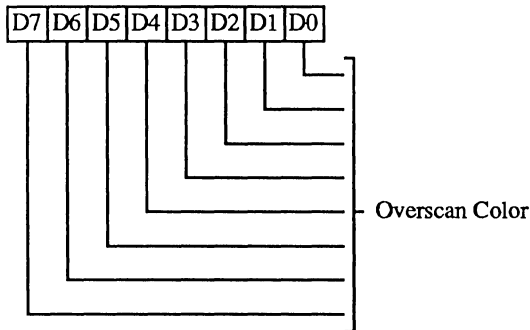
7-0 Overscan Color. These 8 bits define the overscan (border) color value. For monochrome displays, these bits should be zero.

The border color is displayed in the interval after Display Enable End and before Blank Start (end of display area; i.e. right side and bottom of screen) and between Blank End and Display Enable Start (beginning of display area; i.e. left side and top of screen).

COLOR PLANE ENABLE REGISTER (AR12)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 12h
Group 1 Protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```
— Color Plane 0 Enable
— Color Plane 1 Enable
— Color Plane 2 Enable
— Color Plane 3 Enable
— Display Status Select
— Reserved

3-0 Color Plane (0-3) Enable

0: Force the corresponding color plane pixel bit to 0 before it addresses the color palette.
1: Enable the plane data bit of the corresponding color plane to pass.

5-4 Display Status Select. Select two of the eight color outputs to be read back in the Input Status Register 1 (port 3BAh or 3DAh). The output color combinations available on the status bits are as follows:

| | | Status Register 1 | |
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

7-6 Reserved (0)

ATTRIBUTE CONTROLLER HORIZONTAL PIXEL PANNING REGISTER (AR13)
Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
*Index 13h*
Group 1 Protection
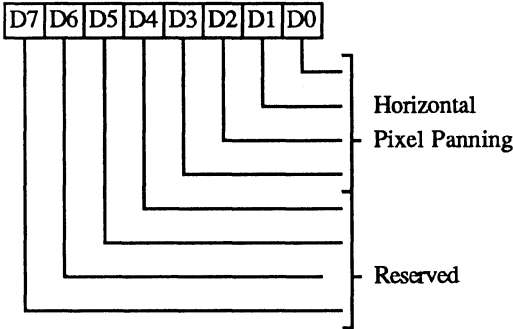
3-0 Horizontal Pixel Panning. These bits select the number of pixels to shift the display horizontally to the left. Pixel panning is available in both text and graphics modes. In 9 pixels/character text mode, the output can be shifted a maximum of 9 pixels. In 8 pixels/character text mode and all graphics modes a maximum shift of 8 pixels is possible. In 256-color mode (output assembler AR10 D6 = 1), bit 0 of this register must be 0 which results in only 4 panning positions per display byte. In Shift Load 2 and Shift Load 4 modes, register CR08 provides single pixel resolution for panning. Panning is controlled as follows:

	Number of Pixels Shifted		
AR13	**9-dot mode**	**8-dot mode**	**256-color mode**
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7-4 Reserved (0)

ATTRIBUTE CONTROLLER PIXEL PAD REGISTER (AR14)
Read at I/O Address 3C1h
*Write At I/O Address 3C0/1h*
Index 14h
Group 1 Protection
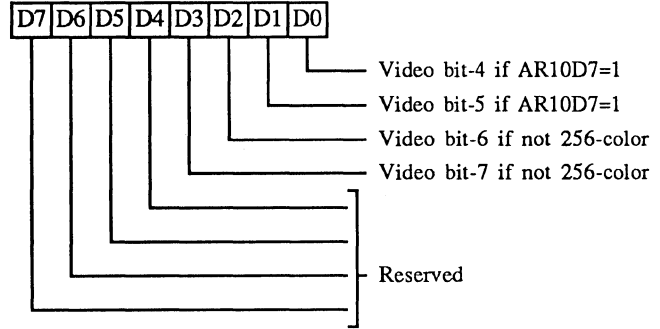
1-0 These bits are output as video bits 5 and 4 when AR10 D7 = 1. They are disabled in 256 color mode.

3-2 These bits are output as video bits 7 and 6 in all modes except 256-color mode.

7-4 Reserved (0)

EXTERNAL COLOR PALETTE PIXEL MASK REGISTER (DACMASK)
Read/Write at I/O Address 3C6h
Group 6 Protection

- Pixel Mask Bit-0
- Pixel Mask Bit-1
- Pixel Mask Bit-2
- Pixel Mask Bit-3
- Pixel Mask Bit-4
- Pixel Mask Bit-5
- Pixel Mask Bit-6
- Pixel Mask Bit-7
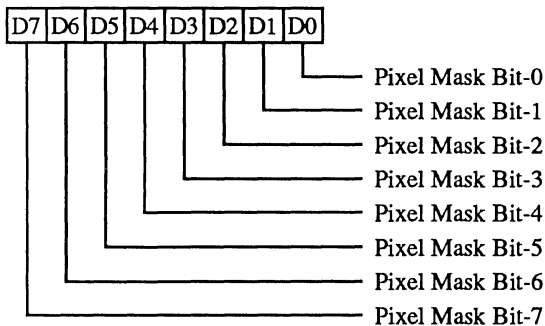
The contents of this register are logically ANDed with the 8 bits of video data coming into the external color palette. Zero bits in this register therefore cause the corresponding address input to the external color palette to be zero. For example, if this register is programmed with 7, only external color palette registers 0-7 would be accessible; video output bits 3-7 would be ignored and all color values would map into the lower 8 locations in the color palette.

This register is physically located in the external color palette chip (used for displaying analog data to the CRT). Reads from this I/O location cause the PALRD/ pin to be asserted. Writes to this I/O location cause the PALWR/ pin to be asserted. The functionality of this port is determined by the external palette chip.

EXTERNAL COLOR PALETTE STATE REGISTER (DACSTATE)
Read only at I/O Address 3C7h

- Palette State 0
- Palette State 1
- Reserved
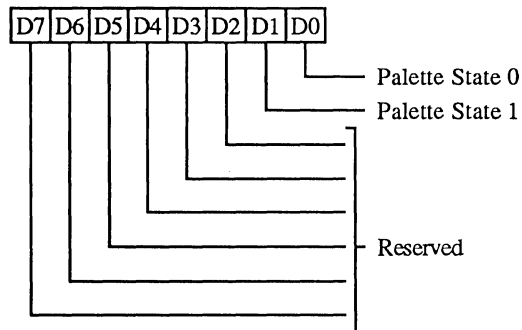
1-0   Status bits indicate the I/O address of the last CPU write to the external DAC/Color Palette:

00: The last write was to 3C8h (write mode).
11: The last write was to 3C7h (read mode).

7-2   Reserved (0)

To allow saving and restoring the state of the video subsystem, this register is required since the external color palette chip automatically increments its index register differently depending on whether the index is written at 3C7h or 3C8h.
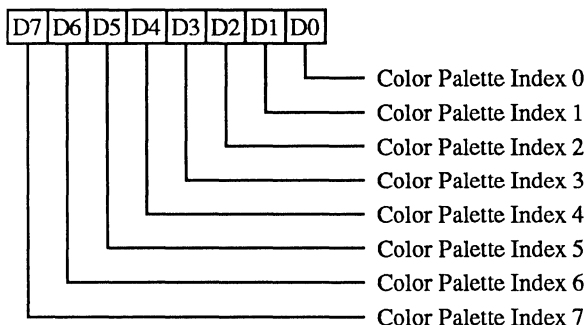
This register is physically located in the 82C451 chip (PALRD/ is *not* asserted for reads from this I/O address).

EXTERNAL COLOR PALETTE
READ-MODE INDEX REGISTER (DACRX)
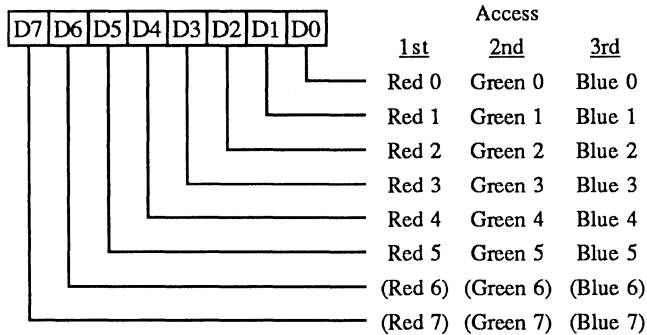*Write only at I/O Address 3C7h*
Group 6 Protection

EXTERNAL COLOR PALETTE
INDEX REGISTER (DACX)
Read/Write at I/O Address 3C8h
Group 6 Protection

D7	D6	D5	D4	D3	D2	D1	D0

- Color Palette Index 0
- Color Palette Index 1
- Color Palette Index 2
- Color Palette Index 3
- Color Palette Index 4
- Color Palette Index 5
- Color Palette Index 6
- Color Palette Index 7

EXTERNAL COLOR PALETTE
DATA REGISTERS (DACDATA 00-FF)
Read/Write at I/O Address 3C9h
Index 00h-FFh
Group 6 Protection

D7	D6	D5	D4	D3	D2	D1	D0

| | Access | |
1st	2nd	3rd
Red 0	Green 0	Blue 0
Red 1	Green 1	Blue 1
Red 2	Green 2	Blue 2
Red 3	Green 3	Blue 3
Red 4	Green 4	Blue 4
Red 5	Green 5	Blue 5
(Red 6)	(Green 6)	(Blue 6)
(Red 7)	(Green 7)	(Blue 7)

The color palette index and data registers are physically located in the external color palette chip. The index register is used to point to one of 256 data registers. Each data register is either 18 or 24 bits in length depending on the type of palette chip used (6 or 8 bits each for red, green, and blue), so the data values must be read as a sequence of 3 bytes. After writing the index register (3C7h or 3C8h), data values may be read from or written to the color palette data register port (3C9h) in sequence: first red, then green, then blue, then repeat for the next

location if desired (the index is incremented automatically by the palette chip).

The index may be written at 3C7h and may be read or written at 3C8h. When the index value is written to either port, it is written to both the index register and a 'save' register internal to the color palette chip. The save register (not the index register) is used internally by the palette chip to point at the current data register. When the index value is written to 3C7h (**read mode**), it is written to both the index register and the save register, then the index register is automatically incremented. When the index value is written to 3C8h (**write mode**), the automatic incrementing of the index register does not occur.

After the third of the three sequential data reads from (or writes to) 3C9h is completed, the save and index registers are both automatically incremented by the palette chip. This allows the entire palette (or any subset) to be read (written) by writing the index of the first color in the set, then sequentially reading (writing) the values for each color, without having to reload the index every three bytes.

The state of the RGB sequence is not saved; the user must access each three bytes in an uninterruptable sequence (or be assured that interrupt service routines will not access the palette index or data registers). When the index register is written (at either port), the RGB sequence is restarted. Data value reads and writes may be intermixed; either reads or writes increment the palette chip internal RGB sequence counter.

The palette chip internal save register always contains a value one less than the readable index value if the last index write was to the 'read mode' port. The 82C451 therefore saves the state of which port (3C7h or 3C8h) was last written and returns that information on reads from 3C7h (PALRD/ is only asserted on reads from 3C8h and not on reads from 3C7h). Writes to 3C7h or 3C8h cause the PALWR/ pin to be asserted.

The functionality of the index and data ports is determined by the external palette chip.
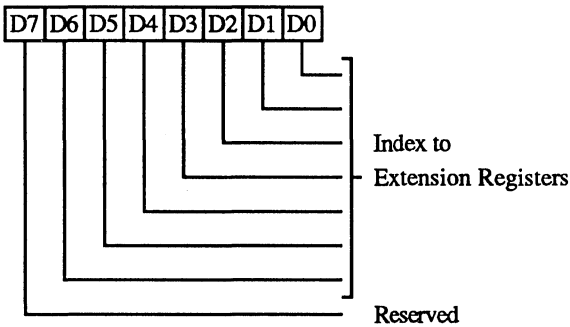
82C451 Extension Registers

Register Mnemonic	Register Group	Register Name	Index	I/O Access	Address	State After Reset	Page
XRX	–	Extension Index	--	RW	3B6h / 3D6h	- x x x x x x x	66
XR00	Misc	Chip Version	00h	R	3B7h / 3D7h	0 0 0 1 r r r r	66
XR01	Misc	DIP Switch	01h	R	3B7h / 3D7h	- d d d d d d d	66
XR02	Misc	CPU Interface	02h	RW	3B7h / 3D7h	x x 0 0 0 0 0 0	67
XR03	Misc	ROM Decode	03h	RW	3B7h / 3D7h	- - - - - - - 0	67
XR04	Misc	Memory Mode	04h	RW	3B7h / 3D7h	- - - - - 0 - -	68
XR7F	Misc	Diagnostic	7Fh	RW	3B7h / 3D7h	x x 0 0 0 0 0 0	77
XR0B	Mapping	CPU Paging	0Bh	RW	3B7h / 3D7h	- - - - - 0 0	70
XR08	General	General Purpose Output Select B	08h	RW	3B7h / 3D7h	- - - - - 0 0	69
XR09	General	General Purpose Output Select A	09h	RW	3B7h / 3D7h	- - - - - 0 0	69
XR0D	General	Auxiliary Offset	0Dh	RW	3B7h / 3D7h	- - - - - 0 0	77
XR28	General	Video Interface	28h	RW	3B7h / 3D7h	- - - - 0 0 1 0	76
XR2B	General	Default Video	2Bh	RW	3B7h / 3D7h	0 0 0 0 0 0 0 0	76
XR14	Compatibility	Emulation Mode	14h	RW	3B7h / 3D7h	0 0 0 0 x x 0 0	71
XR15	Compatibility	Write Protect	15h	RW	3B7h / 3D7h	- 0 0 0 0 0 0 0	72
XR16	Compatibility	Trap Enable	16h	RW	3B7h / 3D7h	- - 0 0 0 0 0 0	73
XR17	Compatibility	Trap Status	17h	RW	3B7h / 3D7h	- - 0 0 0 0 0 0	73
XR7E	Compatibility	CGA Color Select	7Eh	RW	3B7h / 3D7h	- - x x x x x x	77
XR18	Alternate	Alternate H Display End	18h	RW	3B7h / 3D7h	x x x x x x x x	74
XR19	Alternate	Alternate H Sync Start	19h	RW	3B7h / 3D7h	x x x x x x x x	74
XR1A	Alternate	Alternate H Sync End	1Ah	RW	3B7h / 3D7h	- - - x x x x x	74
XR1B	Alternate	Alternate H Total	1Bh	RW	3B7h / 3D7h	x x x x x x x x	74
XR1C	Alternate	Alternate H Blank Start or End	1Ch	RW	3B7h / 3D7h	x x x x x x x x	75
XR1D	Alternate	Alternate H Blank End or Start	1Dh	RW	3B7h / 3D7h	x x x x x x x x	75
XR1E	Alternate	Alternate Offset	1Eh	RW	3B7h / 3D7h	x x x x x x x x	75

Reset Codes:
x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits

0 = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
R = Reset to 0 by falling edge of RESET

EXTENSION INDEX REGISTER (XRX)
Read/Write at I/O Address 3B6h/3D6h
Index Xh

```
D7 D6 D5 D4 D3 D2 D1 D0
```

Index to
Extension Registers

Reserved

6-0 Index value used to access the extension registers.

7 Reserved (0)

DIP SWITCH REGISTER (XR01)
Read only at I/O Address 3B7h/3D7h
Index 01h

```
D7 D6 D5 D4 D3 D2 D1 D0
```

DIP Switches Status
(read only)
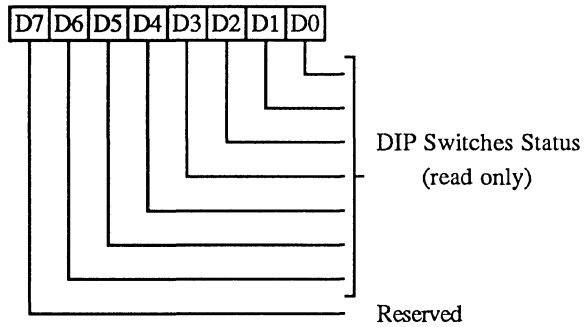
Reserved

6-0 These bits give the state of the DIP switches which are multiplexed with address/data/control signals on pins RFSH/, AEN, ADDHI, BHE/ and A18-A16.

7 Reserved (0)

This register is not related to the EGA Dip Switches.

CHIPS VERSION REGISTER (XR00)
Read only at I/O Address 3B7h/3D7h
Index 00h

```
D7 D6 D5 D4 D3 D2 D1 D0
```
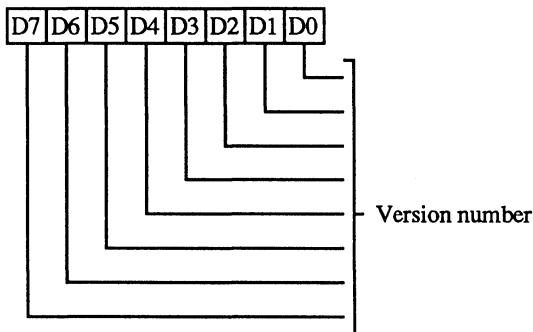
Version number

7-0 This register contains the version number for the 82C451. Values start at 01h and are incremented for every silicon step. The current production silicon (Rev C) reads 04h in this register.

CPU INTERFACE REGISTER (XR02)
Read/Write at I/O Address 3B7h/3D7h
Index 02h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```
                        16-bit Memory
                        Access Enable
                        Reserved
                        Fast Cycles
                        Attribute Controller
                        Mapping
                        I/O Address Decoding
                        Palette Interface
                        Attribute FF Status (R/O)
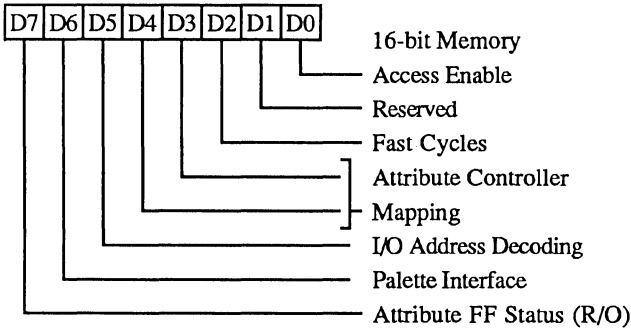
0   16-bit Memory Access Enable

   0: Disabled
   1: Enabled

1   Reserved (0)

2   Fast Cycles Enable. Default is disabled (0) on Reset. The Fast option works only with a 16-bit MCA interface (bit-0 =1 and input signal pin PTMC = Low).

4-3   Attribute Controller Mapping

   00: Write Index at 3C0h and Data at 3C0h (8-bit access only). (Default on Reset; VGA type mapping).
   01: Write Index at 3C0h and Data at 3C1h (8 or 16-bit access), the attribute flip-flop is always reset in this mode (16-bit mapping).
   10: Write Index and Data at 3C0h/3C1h (8-bit access only EGA type mapping).
   11: Reserved (0)

5   I/O Address Decoding. This bit affects 3B4/5h, 3D4/5h, 3C0-2h, 3C4/5h, 3CE/Fh, 3BAh, 3BFh and 3D8h.

   0: Decode all 16 bits of I/O address (Default on Reset).
   1: Decode only the lower 10 bits.

6   Palette Interface

   0: Decode only address 3C6-3C9h (Selected on Reset).
   1: Activate Palette at 3C6-3C9h and 83C6-83C9h.

7   Attribute Flip-flop Status (read only)

   0: Index
   1: Data

ROM DECODE REGISTER (XR03)
Read/Write at I/O Address 3B7h/3D7h
Index 03h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```
                        ROM Enable
                        Reserved
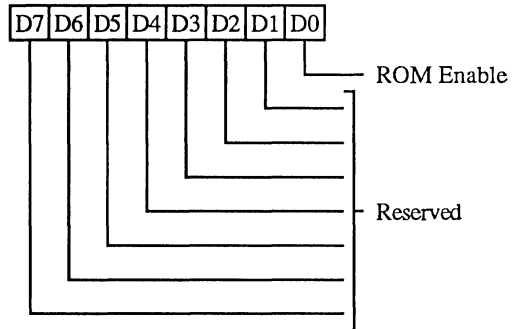
0   ROM Decode Enable

   0: ROM space decode enabled. On reset ROM decode enabled with EISA/ISA-Bus interface, disabled with MCA interface. ROMCS/ active (low) for CPU reads to C0000h-C7FFFh.
   1: ROM space decode disabled.

7-1   Reserved (0)

MEMORY MODE REGISTER (XR04)
Read/Write at I/O Address 3B7h/3D7h
Index 04h
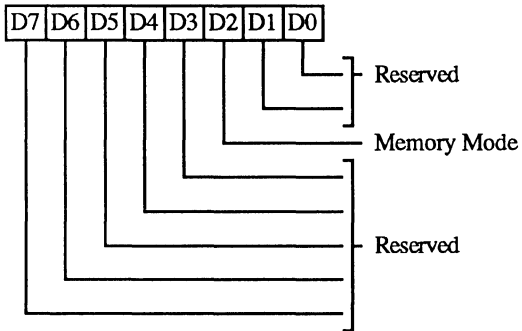
1-0 Reserved(0)

2 Memory Mode

    0: Select VGA Compatibilty Mode.
    1: Select the extended 'Quad Mode'. In this mode, the display memory is mapped in the CPU address space as 4 pages of 64 Kbytes each(or 2 pages of 128 Kbytes each).The paging is controlled through the extended CPU Paging Register(XR0Bh).
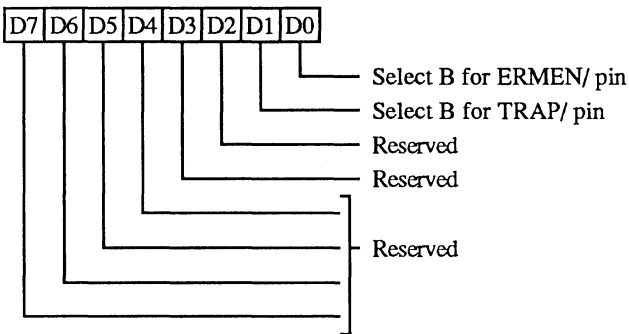
7-3 Reserved (0)

General Purpose Output Select Registers

These two 2 bit registers allow the CPU to define the functions of TRAP/ and ERMEN/ pins. These pins can be defined to work in its normal mode or they can be defined as general purpose outputs. Each pin is controlled by 2 bits defined in the General Purpose Output Select A and General Purpose Output Select B Registers.

Select Bits		Pin Function
B	**A**	
0	0	Normal Function of pin
0	1	3-State
1	0	Force low
1	1	Force high

GENERAL PURPOSE OUTPUT SELECT B REGISTER (XR08)
I/O Address 3B7h/3D7h
Index 08h

D7	D6	D5	D4	D3	D2	D1	D0

- Select B for ERMEN/ pin
- Select B for TRAP/ pin
- Reserved
- Reserved
- Reserved

Select bit B determines if the pin should be a general purpose output or perform its normal function.

0   Select bit B for ERMEN/ pin

1   Select bit B for TRAP/ pin

7-2   Reserved (0)

GENERAL PURPOSE OUTPUT SELECT A REGISTER (XR09)
I/O Address 3B7h/3D7h
Index 09h

D7	D6	D5	D4	D3	D2	D1	D0

- Select A for ERMEN/ pin
- Select A for TRAP/ pin
- Reserved
- Reserved
- Reserved
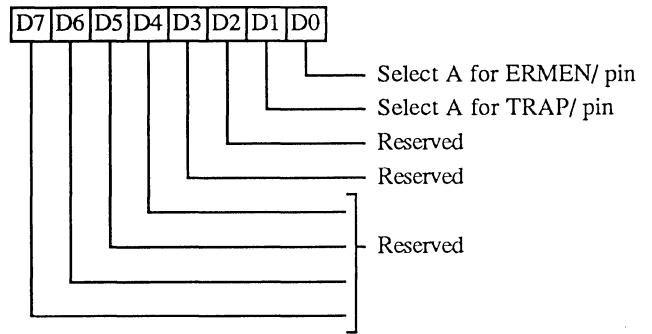
Select bit A determines if the pin should be a general purpose output or perform its normal function.

0   Select bit A for ERMEN/ pin

1   Select bit A for TRAP/ pin

7-2   Reserved (0)

CPU PAGING REGISTER (XR0B)
Read/Write at I/O Address 3B7h/3D7h
Index 0Bh
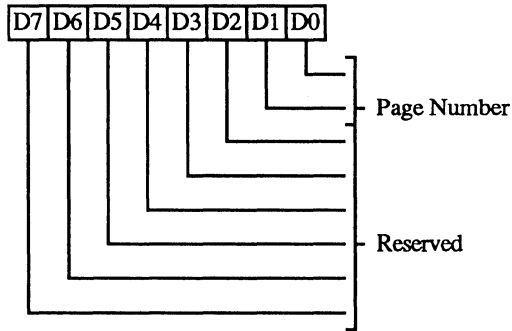
1-0 Page Number

Defines the portion of display memory to be mapped into CPU address space. This 2-bit page number allows the user to access all of 256 Kbytes of display memory in mode 13h. Used in conjunction with bits -D2,D3 of GR06.

7-2 Reserved(0)

AUXILIARY OFFSET REGISTER (XR0D)
Read/Write at I/O Address 3B7h/3D7h
Index 0Dh
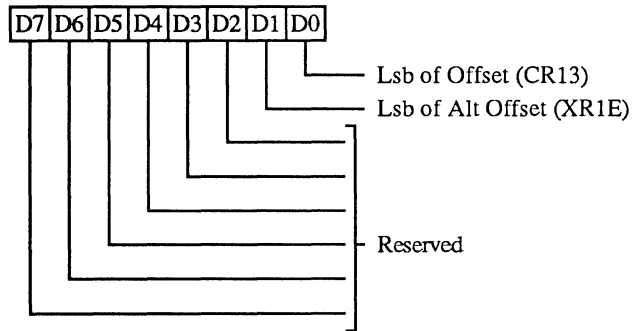
0 This bit provides finer granularity to the Offset when the word and double word modes are used. This bit is used with the regular Offset register (CR13).

1 This bit provides finer granularity to the Offset when the Odd/Even and Quad modes are used. This bit is used with the alternate Offset register (XR1E).

7-2 Reserved (0)

EMULATION MODE REGISTER (XR14)
Read/Write at I/O Address 3B7h/3D7h
Index 14h

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- Emulation Mode
- Herc Config (read only)
- DE Status Mode
- V Retrace Status Mode
- Vsync Status Mode
- Interrupt Polarity
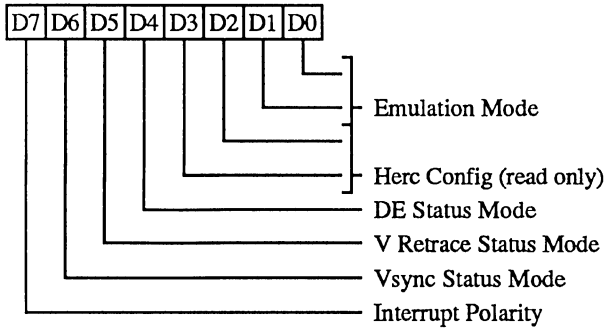
1-0 Emulation Mode

10	Mode
00:	VGA/EGA
01:	CGA
10:	MDA
11:	MDA / Hercules

3-2 Hercules Configuration Register (3BFh) readback (read only).

4 Display Enable Status Mode

    0: Select <u>Display Enable</u> status to appear at bit 0 of Input Status register 1 (I/O Address 3xAh in CGA and VGA modes).

    1: Select <u>Hsync</u> status to appear at bit 0 of Input Status register 1 (I/O Address 3xAh in MDA and Hercules modes).

5 Vertical Retrace Status Mode

    0: Select <u>Vertical Retrace status</u> to appear at bit 3 of Input Status register 1 (I/O Address 3xAh in CGA and VGA modes).

    1: Select <u>Video</u> to appear at bit 3 of Input Status register 1 (I/O Address 3xAh in MDA and Hercules modes).

6 Vsync Status Mode

    0: Enable Vsync status to appear at bit 7 of Input Status register 1 (I/O Address 3xAh in MDA and Hercules modes).

    1: Prevent Vsync status from appearing at bit 7 of Input Status register 1 (I/O Address 3xAh in CGA and VGA modes).

7 Interrupt Output Function

This bit controls the function of the IRQ/ output in both MCA-bus and PC-bus.

Interrupt State	XR14 D7=0 PC Bus	XR14 D7=0 MCA Bus	XR14 D7=1
Disabled	3-state	3-state	3-state
Enabled, Inactive	3-state	3-state	Low
Enabled, Active	3-state	Low	High

WRITE PROTECT REGISTER (XR15)
Read/Write at I/O Address 3B7h/3D7h
Index 15h

This register controls write protection for various groups of registers as shown. 0 = unprotected, 1= protected.

0 Write Protect Group 1 Registers:

Sequencer (SR00-SR04)
Graphics Controller (GR00-GR08)
Attribute Controller (AR00-AR14)

1 Write Protect Group 2 Registers:

Cursor Size register (CR09) bits 0-4
Character Height regs (CR0A, CR0B)

2 Write Protect Group 3 Registers:

CRT Controller CR07 bit-4
CRT Controller CR08
CRT Controller CR11 bits 4 and 5
CRT Controller CR13 and CR14
CRT Controller CR17 bits 0,1 & 3-7
CRT Controller CR18

(Split screen, smooth scroll, & CRTC Mode)

3 Write Protect Group 4 Registers:

CRT Controller CR09 bits 5-7
CRT Controller CR10
CRT Controller CR11 bits 0-3 & 6
CRT Controller CR12, CR15, CR16
CRT Controller CR17 bit-2

4 Write Protect Group 5 Registers:

Miscellaneous Output (3C2h)
Feature Control (3BA/3DAh)

5 Write Protect Group 6. (I/O Addresses 3C6-3C9h). The PALRD/ and PALWR/ output signals are disabled and the 82C451 DAC state register is write protected.

6 Write Protect Group 0. Auxiliary Write Protect for CRT Controller registers CR00-CR07 except CR07 D4. This bit is logically ORed with CR11 D7.

7 Reserved (0)

TRAP ENABLE REGISTER (XR16)
Read/Write at I/O Address 3B7h/3D7h
Index 16h

```
D7 D6 D5 D4 D3 D2 D1 D0
                        Trap on access to:
                     └─ 3B4/3B5h
                  └──── 3B8/3BFh
               └─────── 3Cxh
            └────────── 3D4/3D5h
         └───────────── 3D8/3D9h
      └──────────────── CR00-0B and CR10-18
  └─┘
      ├─ Reserved
```
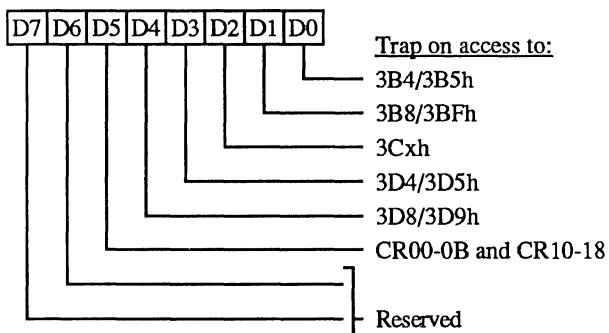
Trap Enable bits:

0   Generate Trap on Access to I/O Addresses 3B4h or 3B5h.

1   Generate Trap on Access to I/O Addresses 3B8h or 3BFh.

2   Generate Trap on Access to I/O Addresses 3Cxh.

3   Generate Trap on Access to I/O Addresses 3D4h or 3D5h.

4   Generate Trap on Access to I/O Addresses 3D8h or 3D9h.

5   Generate Trap on Access to registers CR0B and CR10 through CR18.

7-6   Reserved (0)

For all bits:

0:    Disable trap
1:    Enable trap

This register is cleared (0) on reset.

TRAP STATUS REGISTER (XR17)
Read/Clear at I/O Address 3B7h/3D7h
Index 17h

```
D7 D6 D5 D4 D3 D2 D1 D0
                        Trap occurred at:
                     └─ 3B4/3B5h
                  └──── 3B8/3BFh
               └─────── 3Cxh
            └────────── 3D4/3D5h
         └───────────── 3D8/3D9h
      └──────────────── CR00-0B or CR10-18
  └─┘
      ├─ Reserved
```
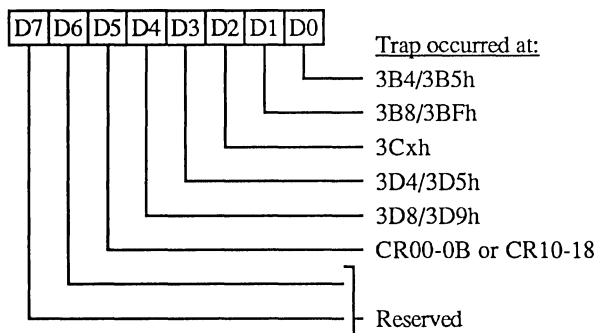
Trap Status bits:

0   Trap occurred on access to I/O Address 3B4h or 3B5h.

1   Trap occurred on access to I/O Address 3B8h or 3BFh.

2   Trap occurred on access to I/O Address 3Cxh.

3   Trap occurred on access to I/O Address 3D4h or 3D5h.

4   Trap occurred on access to I/O Address 3D8h or 3D9h.

5   Trap occurred on access to CRT Controller registers CR00 through CR0B and CR10 through CR18.

7-6   Reserved (0)

For all bits:

0:    No access occurred
1:    Access occurred

Any or all bits in this register may be cleared by writing a one (1) to the desired bit location.

ALTERNATE HORIZONTAL DISPLAY ENABLE END (XR18)
Read/Write at I/O Address 3B7h/3D7h
Index 18h

D7 D6 D5 D4 D3 D2 D1 D0

— Alternate H Display End
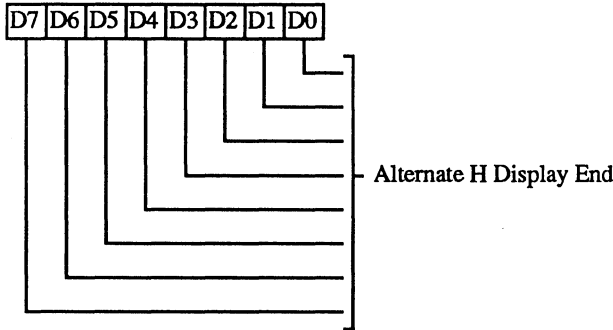
This register is used in CRT low resolution CGA modes, Hercules graphics mode.

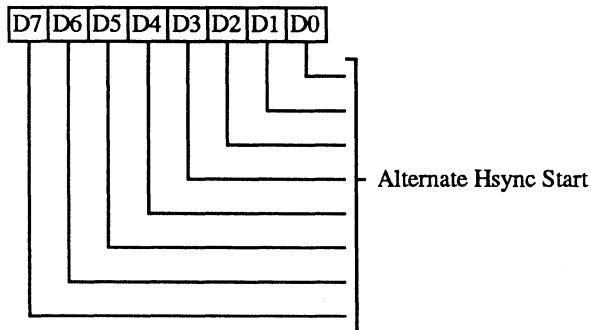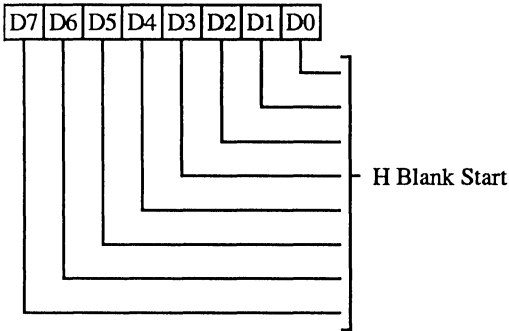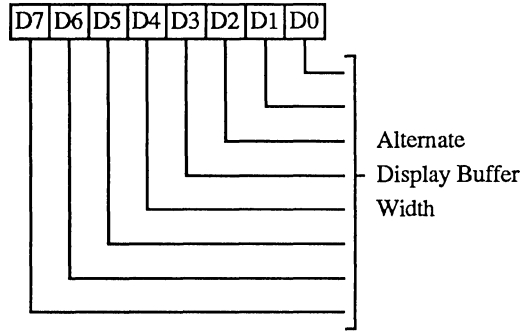**7-0** Alternate Horizontal Display Enable End. See CR01 for description.

ALTERNATE HORIZONTAL SYNC END (XR1A)
Read/Write at I/O Address 3B7h/3D7h
Index 1Ah
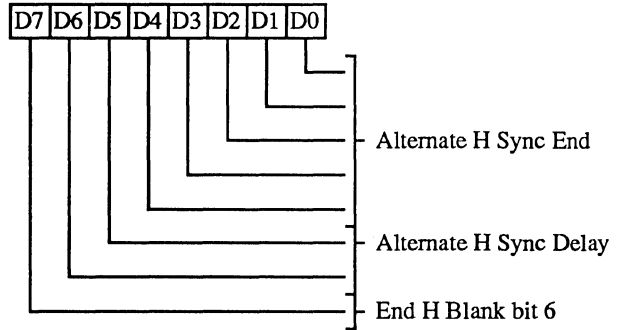
D7 D6 D5 D4 D3 D2 D1 D0

— Alternate H Sync End

— Alternate H Sync Delay

— End H Blank bit 6

This register is used in CRT low resolution CGA modes, Hercules graphics modes.

4-0 Alternate Horizontal Sync End. See CR05 for description.

6-5 Alternate Horizontal Sync Delay. See CR05 for description.

7 End Horizontal Blank bit 6. Sixth bit of the Alternate Horizontal Blanking Register.

ALTERNATE HORIZONTAL SYNC START (XR19)
Read/Write at I/O Address 3B7h/3D7h
Index 19h

D7 D6 D5 D4 D3 D2 D1 D0

— Alternate Hsync Start

This register is used in CRT low resolution CGA modes, Hercules graphics modes.

7-0 Alternate Horizontal Sync Start. See CR04 for description.

ALTERNATE HORIZONTAL TOTAL (XR1B)
Read/Write at I/O Address 3B7h/3D7h
Index 1Bh
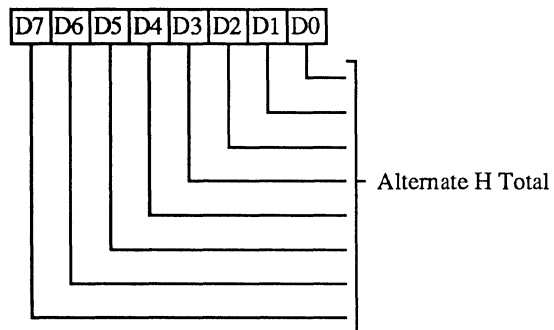
D7 D6 D5 D4 D3 D2 D1 D0

— Alternate H Total

This register is used in CRT low resolution CGA modes, Hercules graphics modes.

7-0 Alternate Horizontal Total. See CR00 for description.

ALTERNATE HORIZONTAL BLANK START (XR1C)
Read/Write at I/O Address 3B7h/3D7h
Index 1Ch

```
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
```
H Blank Start

This register is used in CRT low resolution CGA modes and Hercules graphics modes.

7-0   Alternate Horizontal Blank Start. See CR02 for description.

ALTERNATE HORIZONTAL BLANK END (XR1D)
Read/Write at I/O Address 3B7h/3D7h
Index 1Dh
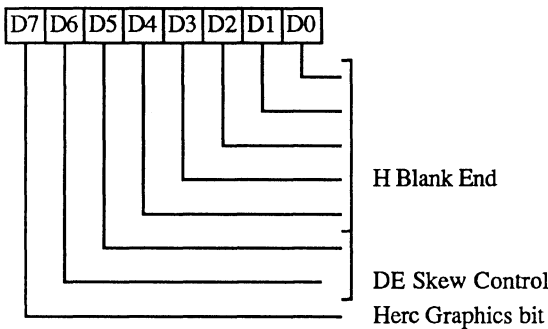
```
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
```
H Blank End

DE Skew Control
Herc Graphics bit

This register is used in CRT low resolution CGA modes and Hercules graphics modes.

4-0   Alternate Horizontal Blank End. See CR03 for description.

6-5   Display Enable Skew Control. See CR03 for description.

7   Herc Graphics bit.

   0: For IBM VGA compatible operation.
   1: Enhances split screen functionality. Also this bit should be set to '1' for Hercules Graphics mode (720 x348 line mode).

ALTERNATE OFFSET (XR1E)
Read/Write at I/O Address 3B7h/3D7h
Index 1Eh

```
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
```
Alternate
Display Buffer
Width

This register is used in low resolution CGA modes and Hercules graphics modes.

7-0   Alternate Offset. See CR13 for description.

VIDEO INTERFACE REGISTER (XR28)
Read/Write at I/O Address 3B7h/3D7h
Index 28h
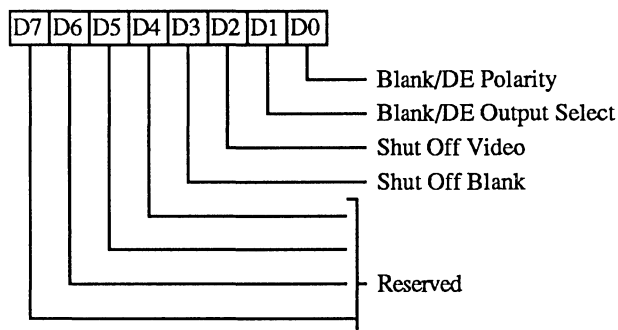
0   BLANK/Display Enable Polarity

    0: Negative
    1: Positive

1   Blank / Display Enable Select

    0: BLANK/ pin outputs BLANK/
    1: BLANK/ pin outputs DE

The signal polarity selected by bit 0 is applicable for either selection

2   Shut off Video

    0: Video not forced to Default Video Register during blank time.
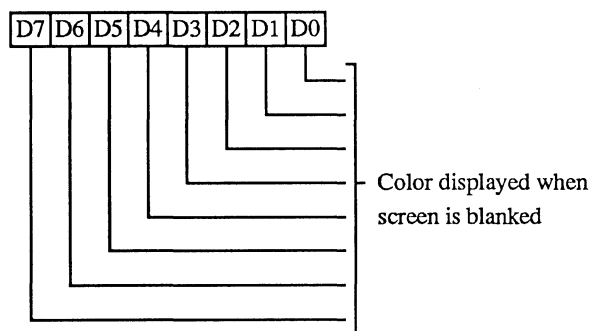   1: Video forced to default video when the screen is blanked.

3   Shut Off Blank

    0: The BLANK/ output is not forced to be active when the screen is blanked (using bit 5 of the Sequencer Clocking Mode register SR01).
    1: The BLANK/ output is forced active when the screen is blanked (Bit 5 of SR01).

7-4 Reserved (0)

DEFAULT VIDEO REGISTER (XR2B)
Read/Write at I/O Address 3B7h/3D7h
Index 2Bh

7-0 Color to be displayed when the screen is forced to blank state (using bit 5 of SR1).

CGA COLOR SELECT (XR7E)
Read/Write at I/O Address 3B7h/3D7h
Index 7Eh

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- Color bit-0 (Blue)
- Color bit-1 (Green)
- Color bit-2 (Red)
- Color bit-3 (Intensity)
- Intensity Enable
- Color Set Select
- Reserved (0)
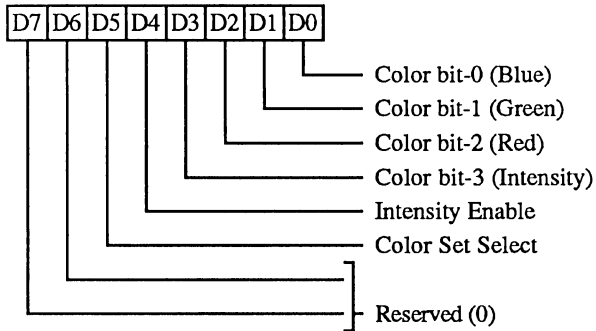
This register is a copy of the CGA color select register 3D9h. Writes to this register will change the copy at 3D9h. It is effective in CGA emulation mode. The copy at 3D9h is visible only in CGA emulation mode. The copy at XR7F is always visible.

DIAGNOSTIC (XR7F)
Read/Write at I/O Address 3B7h/3D7h
Index 7Fh

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- 3-state Control
- Test Function
- Reserved (0)
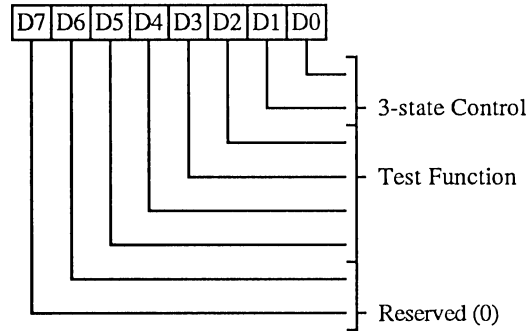
Diagnostic Register (I/O Address 3D7h; Address Pointer: 7Fh). Read - Write Register.

0   3-State Control bit 0: 0: Normal Outputs; 1: 3-state output pins PALRD/, PALWR/, WR46E8/, HSYNC, VSYNC, RDLO/, RDHI/, ROMCS/, IRQ.

1   3-state Control bit 1; 1: 3-state output pins WE/, RAS/, CAS0/, CAS1/, CAS2/, CAS3/, AA0-7 and BA0-7.

6-2   Test Function Pins. These bits are used for internal testing of the chip. They should be 0 for normal operation.

7   Reserved (0)

Functional Description

CPU INTERFACE - PC (EISA/ISA) BUS

The 82C451 supports both PC (EISA/ISA or Industry Standard Architecture) and MCA (Microchannel: PS/2™ or CHIPS/2™) interface configurations. The interface type is selected by strapping the PTMC pin high (ISA bus) or low (MCA bus).

The 82C451 supports both 8-bit and 16-bit CPU interface configurations. The 16-bit interface can be independently enabled/disabled for memory cycles through the CPU Interface Register 16 bit I/O operation is dependent on the state of BHE/. In 16 bit AT slot 82C451 always supports 16 bit I/O operation and in 8 bit slot, 8 bit I/O cycles are

supported. On reset, the chip is configured for 8-bit accesses for memory and I/O cycles. The 16-bit interface for I/O cycles is restricted to index/data pairs of registers. This includes the Sequencer (3C4h), Graphics Controller (3CEh), CRT Controller (3B4h/3D4h), extended registers (3D6/3D7h) and the Attribute Controller (3C0h). There is an independent control for 16-bit interface to the Attribute Controller. All other I/O addresses (color palette, Miscellaneous Output and Status) are always treated as 8-bit ports; DS16/ (IOCS16/) is never asserted for these ports.

When the 16-bit interface is chosen, the 82C451 will always assert DS16/ (MEMCS16/ or IOCS16/) after
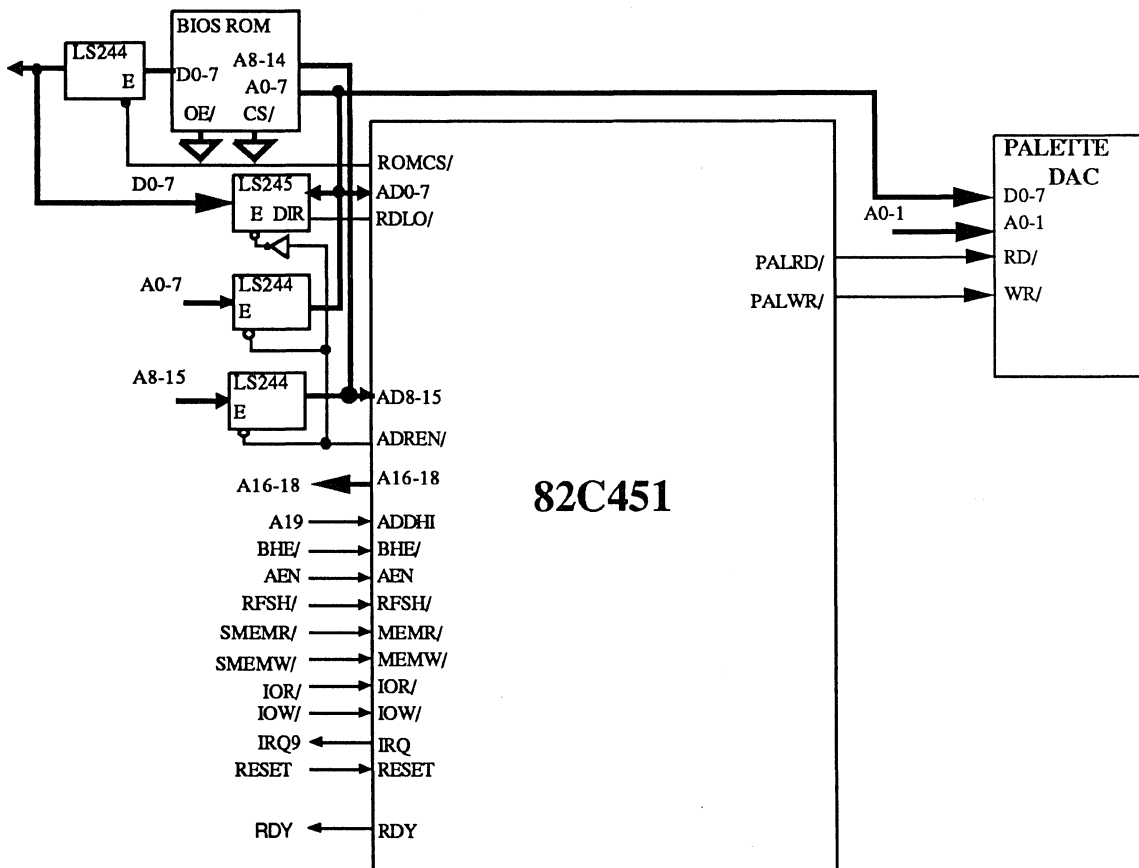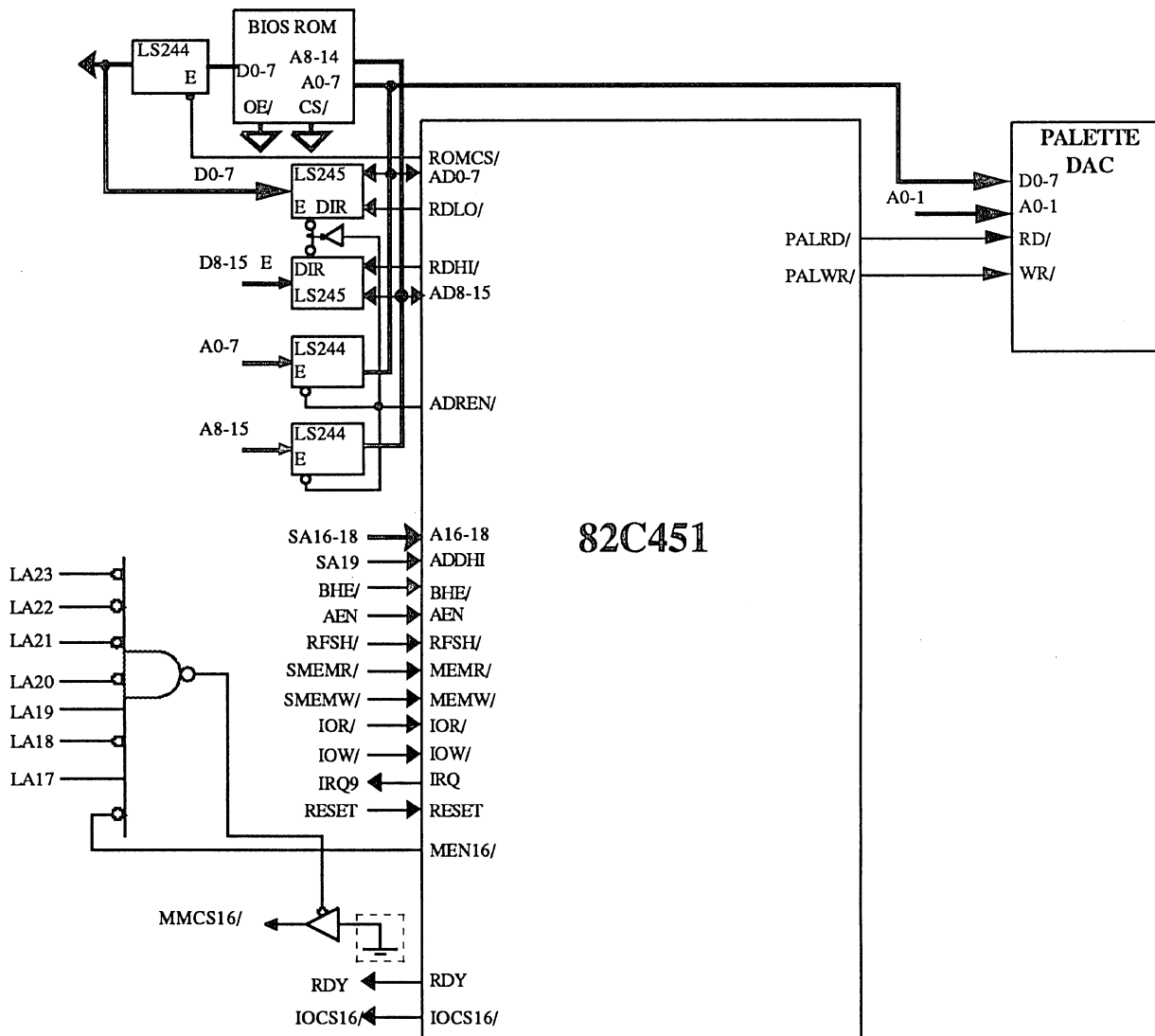

Block Diagram – 8-Bit EISA/ISA Bus Interface

a valid memory or I/O address is recognized. Depending on the state of A0 and BHE/, either an 8-bit or 16-bit cycle will actually be executed. This ensures that even for software-directed 8-bit accesses, faster non-converted cycles will be executed by the system logic. If both A0 and BHE/ are high, then a byte transfer will be executed from the lower data bus to the odd byte (default 8-bit transfer mode); connecting BHE/ to Vcc results in forcing 8 bit transfers. Regardless of the 8-bit cycle being directed to odd or even address, only one half of the data bus will respond. In case of read cycles, only one half of the data bus will be driven.

8-Bit EISA/ISA Interface

The PTMC pin should be strapped high to enable the EISA/ISA bus interface.

To use an 8-bit CPU interface, an external 8-bit multiplexer is required. This can be implemented using one buffer (LS244) for the lower 8 bits of the address bus and one transceiver (LS245) for the data bus. Address bus bits 8-15 are connected directly to the 82C451. The control and direction signals for the multiplexer are provided by the 82C451.

Since the EISA/ISA bus supports only 1 MB of

Block Diagram – 16-Bit EISA/ISA Bus Interface (8-Bit BIOS ROM)

memory, the high address pin ADDHI is connected to A19.

The RDY line on the EISA/ISA Bus can be driven directly by the 82C451. Depending on the load on the bus, it may be desirable to buffer this signal using a 3-state buffer.

An EISA/ISA bus implementation of the 82C451 also requires a BIOS ROM. The 82C451 supports a 32 KByte ROM BIOS. To interface a BIOS ROM, addresses 0C0000-0C7fffh are decoded and the ROMCS/ pin is pulled low for these addresses. When the ROM is being accessed, the 82C451 always keeps the external multiplexer in the address state. The ROM address pins can therefore be connected to the 82C451 multiplexed address/data bus. An additional buffer (LS244) is needed to buffer the ROM data onto the EISA/ISA data bus.

The enable for this buffer is the ROMCS/ pin out of the 82C451.

In order to support the ROM paging scheme as done in IBM™'s VGA add in card for the EISA/ISA-bus, the 82C451 decodes I/O writes to the Paging Control Register (46E8h). External hardware must latch data bits 0-2 at this time and use the latched data bits to translate the ROM address. In this case, the ROMCS/ pin out of the 82C451 must be qualified by the external hardware to enable the buffer for the appropriate ROM addresses.

Like the IBM VGA add in card for the EISA/ISA bus, the 82C451 supports both a setup mode and an enable/disable mode. This is controlled by bits 3 and 4 of I/O port 46E8h. All hardware to implement this is included inside 82C451.

Note:
This diagram shows the 16 bit bios interface in detail. Refer to previous diagram for 16 bit interface to the 82C451.
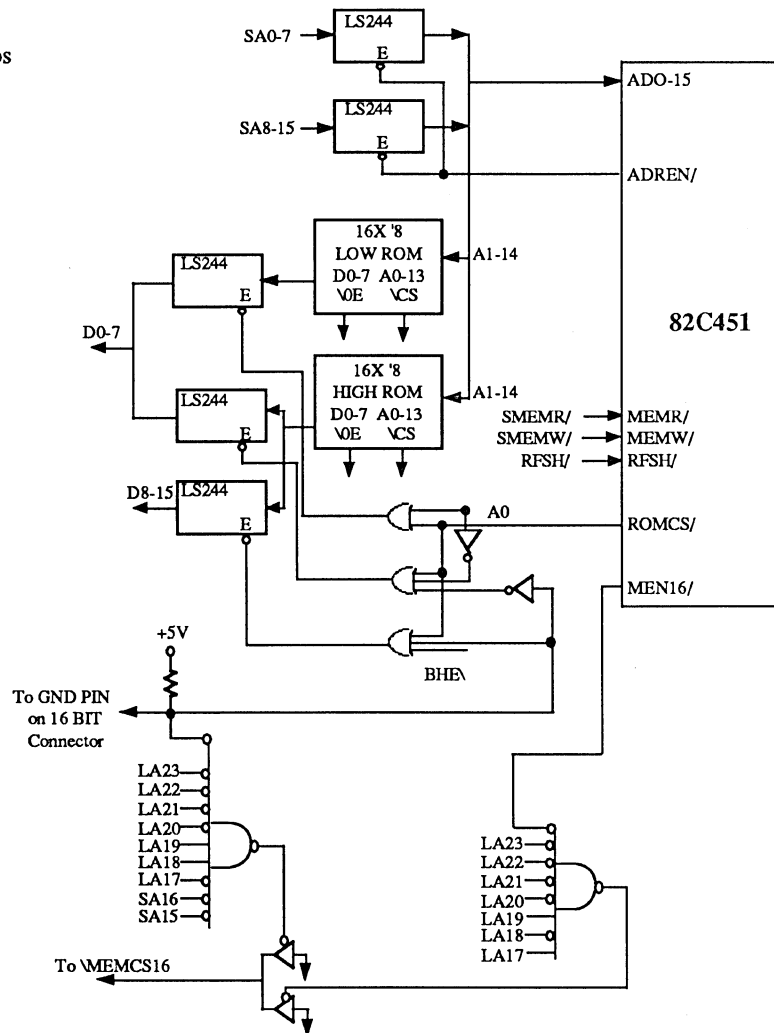
Block Diagram – 16-Bit EISA/ISA Bus Interface (16-Bit BIOS ROM)

16-Bit EISA/ISA Interface

The 16-bit interface supports 16-bit accesses to display memory and to the index/data pairs of I/O registers. The stand-alone registers and BIOS ROM are still accessed as 8-bit devices. A 16-bit BIOS interface can be supported. This is explained later in this section. Also, 16-bit accesses to display memory assume that the 82C451 controls the entire 0A0000-0Bffffh address space. This requires that the 82C451 be the only active video card in the system.

The PTMC pin is strapped high to enable the EISA/ISA bus interface.

The external 16-bit multiplexer can be implemented using two buffers (LS244s) for the address bus and two transceivers (LS245s) for the data bus. The control and direction signals for the multiplexer are provided by the 82C451.

Since the 82C451 resides only in the first megabyte of the CPU address space, the MEMR/ and MEMW/ pins are connected to the SMEMR/ and SMEMW/ signals on the EISA/ISA bus. The high address pin ADDHI is connected to A19. The 82C451 provides a pin called MEN16/ to support the 16-bit interface. This pin is low when the 16-bit memory interface is enabled and high when the 16-bit interface is disabled. This pin is controlled by bit-0 of the CPU Interface Register in the extended address space. MEMCS16/ should be generated externally by decoding LA17 - LA23. MEN16/ can be used in the external decoding.

Pulling MEMCS16/ or IOCS16/ low causes the system logic to generate 235ns (min.) memory cycle (MEMR/ and MEMW/) and 175ns (min.) I/O cycles (IORD/ and IOWR/). If these pins are not pulled low then all the command signals will be low for a minimum of 540ns.

A 16-bit I/O interface is supported. IOCS16/ is pulled low whenever the address pins A0-15 match a valid 16-bit I/O address and AEN is low. It is possible for this pin to be pulled low for memory accesses. Pulling IOCS16/ active for memory accesses has no effect.

The RDY and IOCS16/ lines on the EISA/ISA bus can be driven directly by the 82C451. Depending on the load on the bus, it may be desirable to also buffer these signals using a tristate buffer. The BIOS interface is similar to the 8-bit EISA/ISA bus interface. The ROM paging scheme is also similar to the 8-bit EISA/ISA bus interface as explained in the 8-bit EISA/ISA interface section.

The 82C451 also supports a 16-bit BIOS interface. Note that extreme care should be taken to decode A15 - A23. In the PC/AT bus, addresses A15 and A16 are not available in the unlatched form. Care should be taken to guarantee the MEMCS16/ timing to meet the system specification. This requires fast decoding of the addresses to generate the MEMCS16/ back to the system logic.

There are two ways to implement the 16 bit BIOS interface. 32K bytes of BIOS data can be split into two 16K x 8 ROMS. External control logic can steer the proper data byte on low or high data bus. This scheme is shown on the previous page. Another option is to use two 32k x 8 ROMS for low and high data bytes. In this scheme, BIOS does not have to be split. Both the ROMS are identified. This is shown on the following page.

Like the IBM VGA card for the EISA/ISA bus, the 82C451 supports both a setup mode and an enable/disable mode. This is controlled by bits 3 and 4 of I/O port 46E8h. All hardware to implement this logic is included inside the 82C451.

RDY is generated after a valid address and status (S0/, S1/ or MEMR/, MEMW/) is seen. In the EISA/ISA bus interface, RDY will always be low until after the data is available to the CPU. In the MCA case, RDY can go high before data is available.
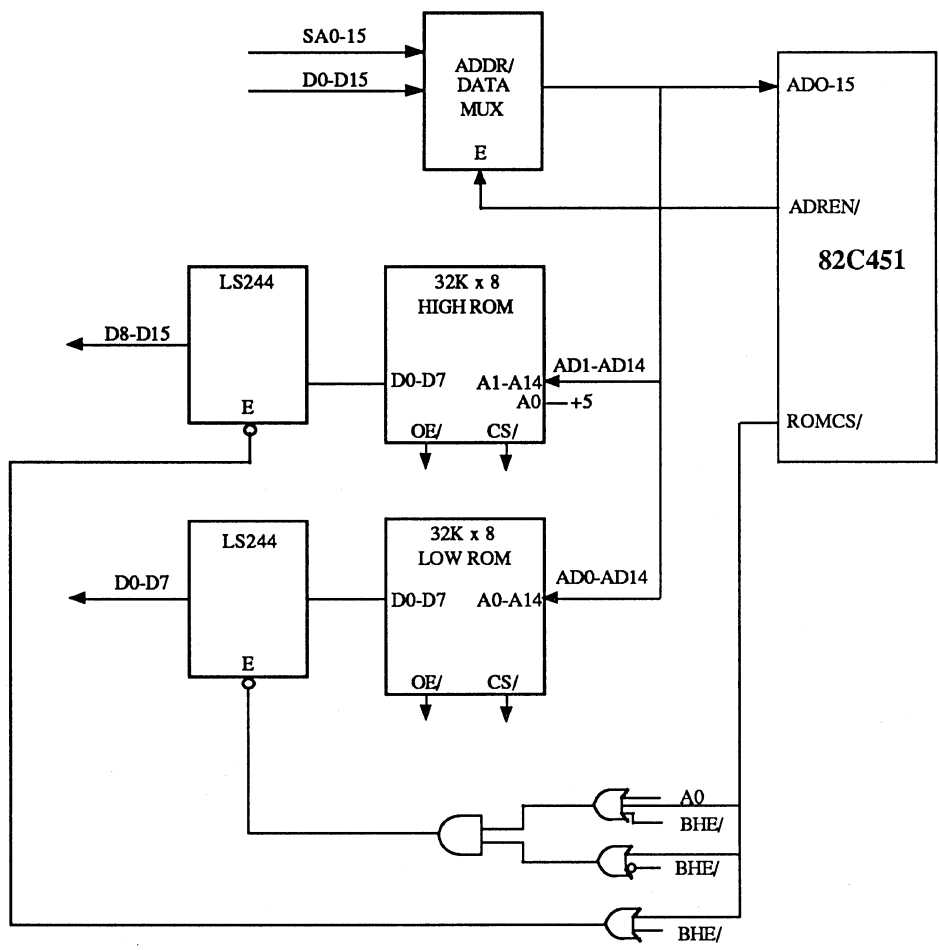
Block Diagram - 16 bit BIOS ROM (32k x 8 ROMs)
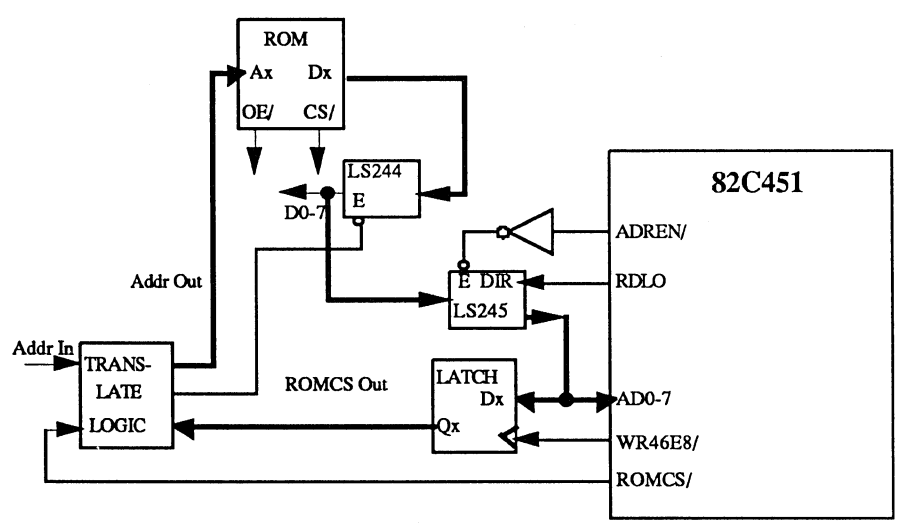
Block Diagram – ROM Paging

CPU INTERFACE - MCA BUS

The 82C451 supports the MCA interface when the strap pin (PTMC) is pulled low. The 82C451 has a multiplexed address and data bus. To use a 16-bit CPU interface, an external 16-bit multiplexer is required. This multiplexer can be implemented using two buffers (LS244s) on the address bus and two tranceivers (LS245s) on the data bus. The control and direction signals for the external multiplexer are provided by the 82C451. The multiplexer control signal (ADREN/) is tied to the enable inputs of the buffers and is inverted and connected to the enable inputs of the transceivers. The direction of the transceivers is controlled by the RDLO/ and RDHI/ outputs from 82C451. Unless otherwise specified, the 82C451 always drives the transceivers away from the external bus.

The circuit diagram for the interface is shown in the figure on the following page.

The CPU interface for the 82C451 is optimized for the CHIPS/250 and /280 Chipsets. The 82C451 also supports fast cycles with the Chipsets™. Using the VGAREQ/ signal, the 82C451 can request the /250 or /280 Chipsets to execute the current cycle at the fastest rate - 0 WS (200ns) at 10 MHz and 1 WS (187.5ns) at 16 MHz. The FAST VGA cycle gives additional boost to the system performance.

Since the 82C451 resides only in the first megabyte of CPU address space, the high address pin ADDHI is connected to decoded address A19-A23 (A31 on 80386 based systems). This signal is directly available in the CHIPS/250 and /280 Chipsets. All the address pins on 82C451 are connected (through the multiplexer) to the unlatched address lines in the system (MCA address bus). The 82C451 latches all the addresses internally.

The 82C451 generates DS16/, RDY, and CSFB/ by decoding ADDHI, A0-18, and MIO/ as a valid memory or I/O address in the current display memory & I/O address space. These pins directly correspond to the DS16/, RDY and CSFB/ pins on the MCA. Although not necessary, it may be desirable for ESD protection to buffer these signals using 3-state buffers.

The RESET, S0/, S1/, MIO/ signals on the MCA can directly drive the corresponding pins on 82C451. The CMD/ signal on the MCA must be qualified with RFSH/ and then connected to the CMD/ pin on 82C451. The CHIPS/250 and /280 Chipsets provide a qualified command signal called VGACMD/.

In an MCA implementation, the 82C451 can be disabled by pulling the DISA/ pin low. This pin is typically controlled by bit-0 of port 3C3. CHIPS/250 and /280 Chipsets provide bit-0 of port 3C3 on the VGAENAB signal. The 82C451 can also be put in the setup mode by pulling SETUP/ pin low. This is typically done using bit-5 of port 94h. Again, the CHIPS/250 and /280 Chipsets provide this bit on a signal called VGASETUP/.

The standard IBM MCA implementation of VGA does not have a POS ID number. However, the 82C451 does support an external optional POS ID number. On I/O accesses to ports 100h and 101h during the setup mode, the POSID/ pin out of 82C451 is pulled low. External hardware can use this pin to gate the contents of an external POS ID number register on the CPU data bus (see figure below).
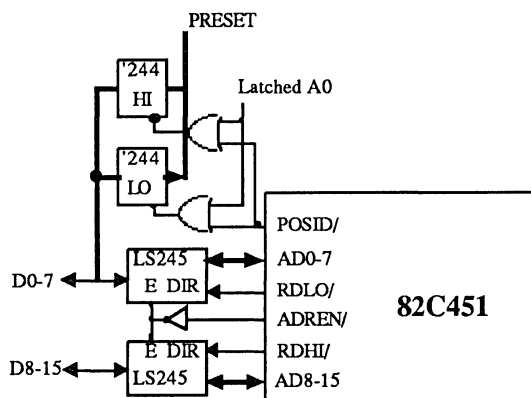
Block Diagram – POS ID Interface
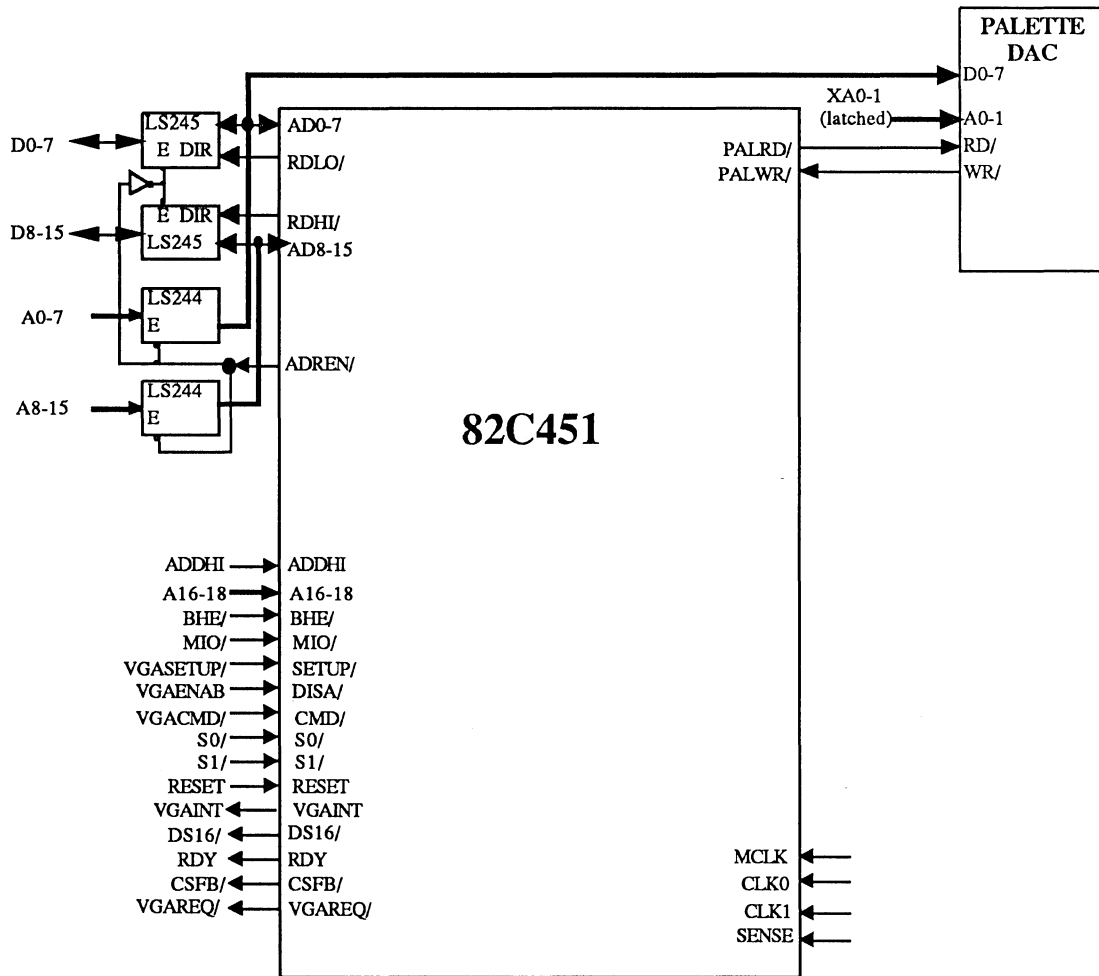
Block Diagram – 16-bit MCA Interface

SETUP AND ENABLE MODES

Setup Mode

The 82C451 supports a setup mode. In this mode, only the configuration registers in the 82C451 are accessible. In the MCA interface, the setup mode is invoked when the SETUP/ pin is low. Typically, this pin is controlled by bit-5 of port 94h and is implemented in the system logic. In the PC-bus interface, setup mode is invoked by writing a '1' to bit-4 of port 46E8h. This port is incorporated inside the 82C451.

Enable Mode

The 82C451 should be enabled for normal operation. With the MCA interface, the 82C451 disappears from the CPU memory and I/O space if the DISA/ input pin is low. This pin is controlled by bit-0 of port 3C3h. In the PC bus interface, bit-3 of port 46E8 = 0 disables the 82C451; 46E8 bit-3 = 1 enables the 82C451. For normal operation, the VGA should be programmed as follows:

MCA Bus Interface

A. Bit-0 of port 3C3h must be 1; This will cause the DISA/ pin to be high, and

B. The 82C451 should be put in setup mode (bit-5 of port 94h = 1 causing SETUP/ pin to go low); bit-0 of port xx2h = 1 then the 82C451 will be put back in normal mode (bit-5 of port 94h = 0)

PC Bus Interface

A. Bit-3 of port 46E8h must be 1, and

B. The 82C451 should be put in setup mode (bit-4 of port 46e8h = 1); and bit-0 of port xx2 = 1 then the 82C451 will be put back in normal mode (bit-4 of port 46e8h = 0).

ENABLING EXTENDED REGISTERS

The 82C451 has extended registers to support the extra functionality of the chips. All functionality of the extended registers in the 82C451 are disabled on reset. The extended registers can be enabled by two sets of control bits (disabled on reset). No new bits are defined nor are any of the unused bits used in the regular VGA registers.

Two separate registers are accessed to enable the extended functionality of the 82C451. The read/write accesses to the extended registers are controlled by the enable control bits. The functionality of the registers is always enabled (disabled on reset). The two registers are defined as follows:

A. Global Enable Register. This register can be accessed at I/O address xx2 (octal) in setup mode. Bit-0 of this register determines if the VGA is in sleep mode or awake mode.

B. Extended Enable Register. This register can be accessed at I/O address 103H in the setup mode. This register defines:

- If the extended registers are enabled (bit-7)
- If the Multiple VGA ID feature is to be enabled and if so, then the ID number of the currently active VGA (bits 0-4)

These registers are described in detail in the register description.

DIP SWITCH INTERFACE

The 82C451 supports up to 7 external DIP switches (see figures below). In the Microchannel interface, these switches are multiplexed on input pins BHE/, DISA/, MIO/, A16, A17, A18, and ADDHI. Two buffers (LS244s) are required to support this feature. The DIP switch state is read into an internal CPU accessible register when CMD/ is low.

In the PC BUS interface, these switches are multiplexed on input pins BHE/, AEN, RFSH/, A16, A17, A18, and ADDHI. Two Buffers (LS244s) are required to support this feature. The DIP switch state is read into an internal CPU accessible register when IORD/ is low.

MULTIPLE VGAs

It is possible to support up to sixteen 82C451s in one system. Each 82C451 must have a unique number assigned to it through the above mentioned DIP switches. All 82C451s occupy the same memory and I/O address space. However, only one 82C451 responds to CPU accesses at a time. The currently active 82C451 is selected by writing an ID number for that 82C451 into the internal Extended Enable Register for all 82C451s. Only the 82C451 which has the same number on its DIP switches will respond to further CPU accesses.
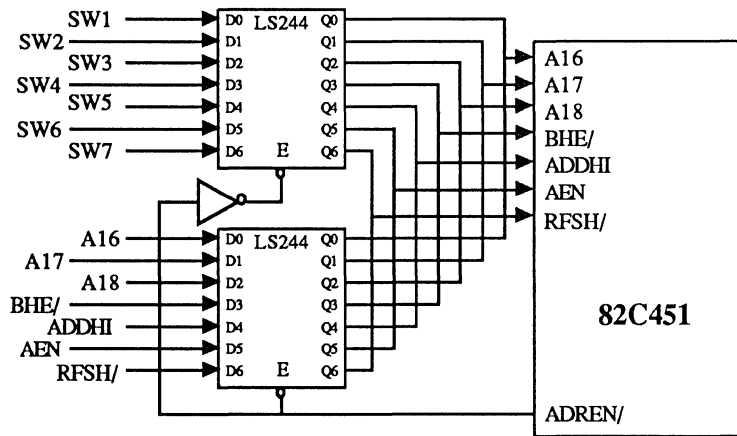
Block Diagram – DIP Switch Interface (EISA/ISA Bus)
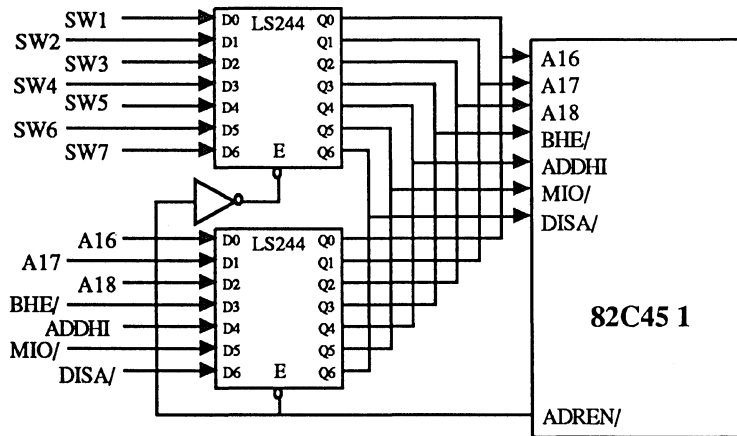
Block Diagram – DIP Switch Interface (MCA Bus)
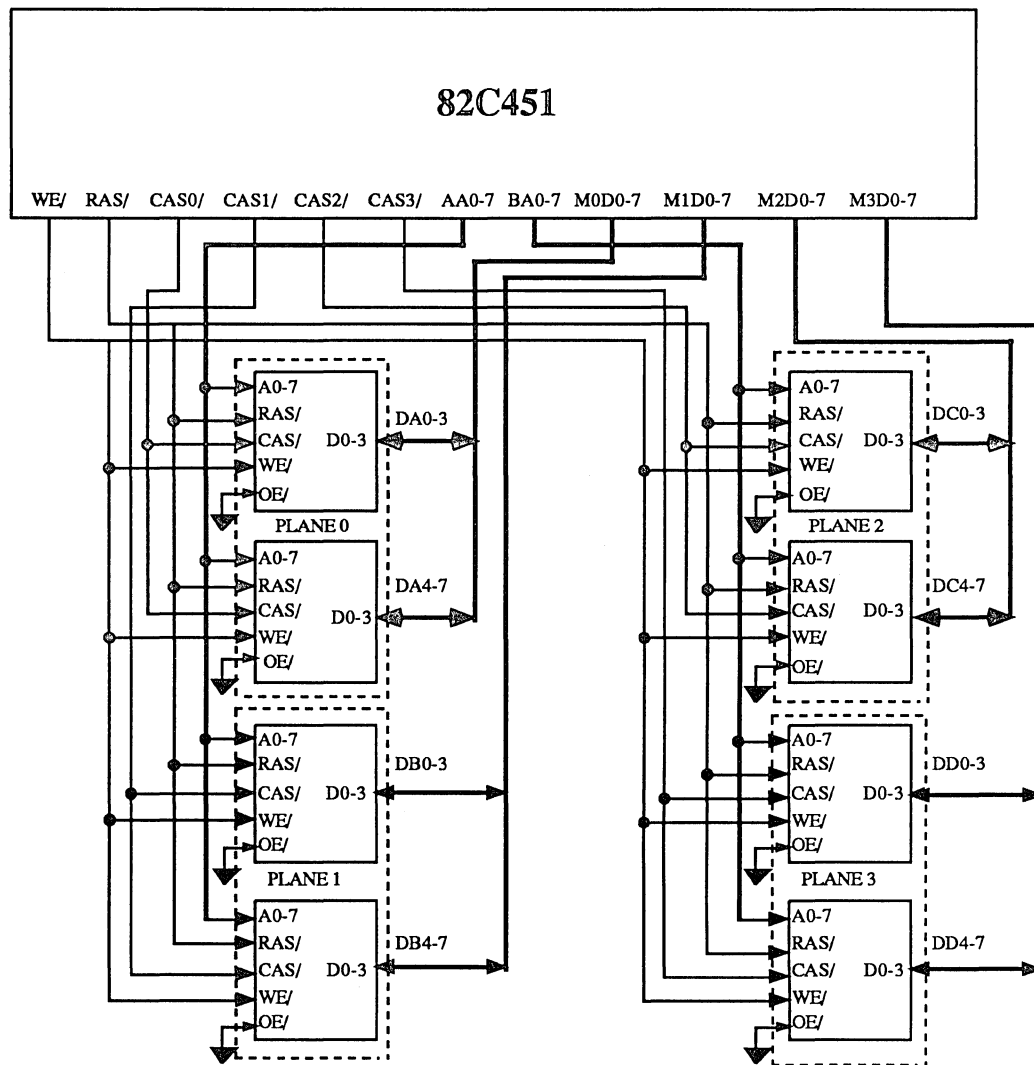
DISPLAY MEMORY INTERFACE

The DRAMs are organized as 4 planes. There are 4 bidirectional 8 bit data buses, one for each of the 4 planes. There are two 8 bit multiplexed address buses for planes 0, 1 and planes 2, 3, respectively. There is a common WE/ line for all 4 planes. To selectively write only to some memory planes, the 82C451 has four CAS/ lines, one for each plane. The DRAM data bus direction is indirectly controlled by RAS/, CAS/ and WE/ (the OE/ pins on the DRAMS are grounded). Proper damping resistors are required between the control pins on the 82C451 and the DRAM inputs.

The typical loading on the DRAM interface lines is:

RAS	8 devices
CAS	2 devices
WE	8 devices
Addr	4 devices
Data	2 devices

The 82C451 supports early write cycles into the DRAMs. The 82C451 supports 256 KB of display memory as follows:

8 Devices 64K x 4   256 KB

Block Diagram – DRAM Interface for 256 KBytes

The display memory interface consists of the following pins:

1	RAS
4	CAS
1	WE
18	Address (two sets of 9 pins)
32	Data (4 sets of 8 pins)

The display memory control signals are derived from the display clock being used.

DISPLAY MODES AND RESOLUTION

82C451 supports all the standard VGA modes. It can also support 800x600 16 Colors Graphics and 132 Column Text Modes. Higher resolution modes such as 960x720 four color and 1280x960 monochrome modes can be supported with external hardware. This is shown in the figures on the following pages.

VIDEO INTERFACE

The 82C451 supports both digital and analog video interfaces. It has all the necessary logic built in to support the external palette interface. It generates the RD/ and WR/ signals for the external palette by decoding CPU I/O addresses 3C6 - 3C9h as valid palette addresses.

It is also possible to program the 82C451 to decode addresses 83C6 - 83C9h. This allows the use of a palette/DAC like a Brooktree® Bt471 which has additional overlay registers and therefore needs more addressability.

SCREEN BLANKING

The 82C451 support screen blanking by writing to a control register (as in IBM's VGA). During this time, all memory cycles are available to the CPU. Unlike the IBM VGA, the video output can be programmed to be forced to a predefined color (default video) whenever the BLANK/ pin is asserted. When BLANK/ is asserted, the video outputs are forced to the default color exactly at the same time (dot clock).
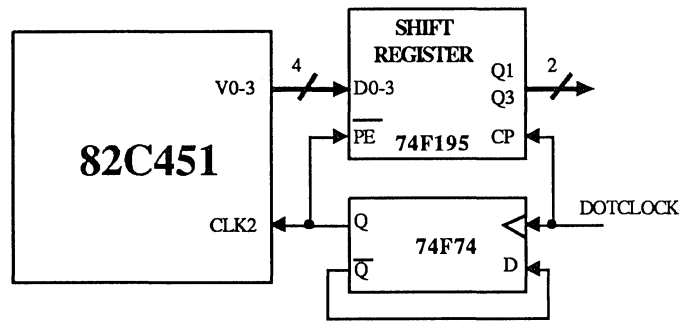
CLOCK INTERFACES

82C451 has 3 clock inputs and 1 memory clock input. MCLK in 82C451 is used for internal I/O sequencing. In 82C452 DRAM timings are derived from MCLK. For a minimum system configuration 82C451 can support up to 3 display clocks. This configuration will support up to 800x600 16 color mode. 82C451 can also be interfaced to an external clock chip. The following pages shows different clock schemes for 82C451.

MONITOR TYPE DETECTION

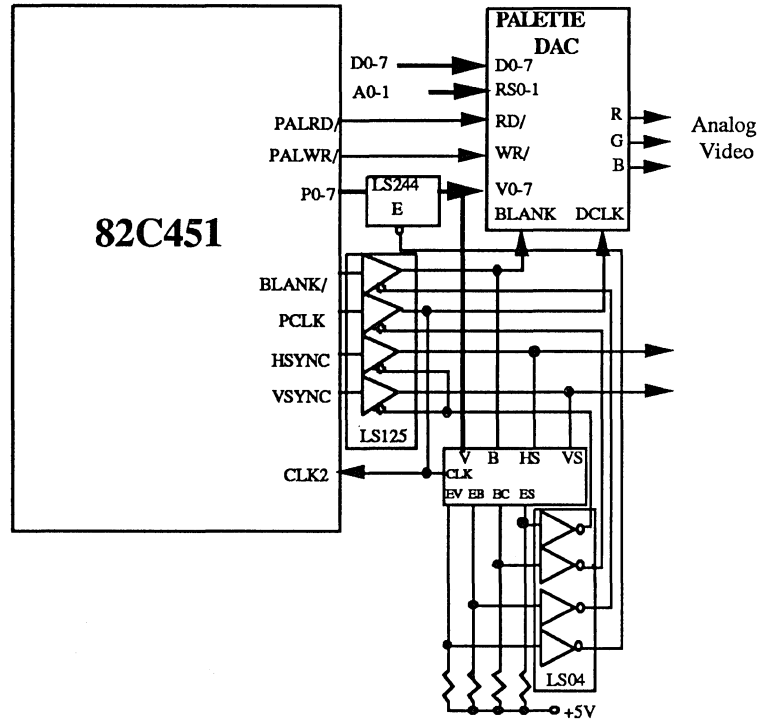82C451 also supports IBM compatible monitor detection scheme. Refer to the figure on the following page.
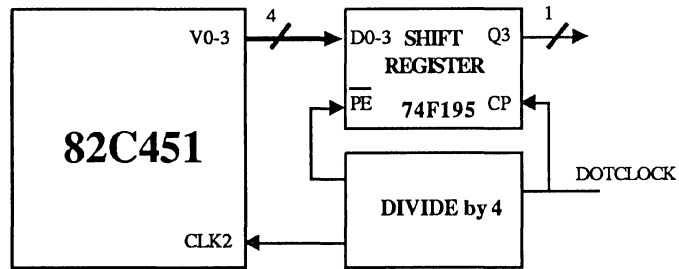
Block Diagram – Ultra High Resolution Monochrome Video Interface

Block Diagram –Super High Resolution (4 Color) Video Interface

Block Diagram – Inmos Palette DAC (IMSG176/178)
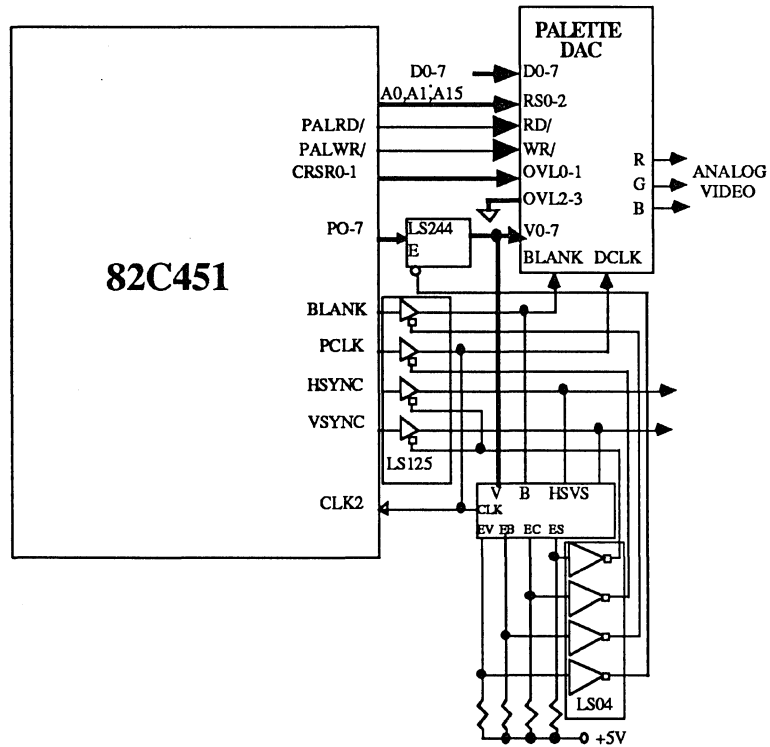
Block Diagram – Brooktree Palette DAC (BT47x)
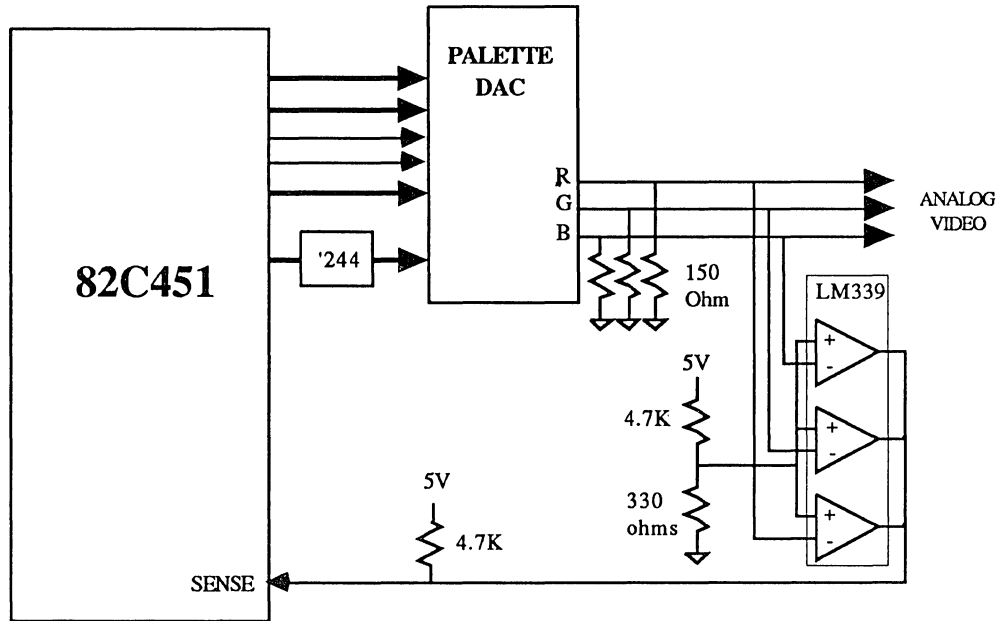
Block Diagram – Monitor Type Detection

Block Diagram – Clock Interface - Minimum

Block Diagram – Clock Interface - Digital Monitor Support

WR3C2 = !IOW & !AEN & A9 & A8 & A7 & A6 & !A5 & !A4 & !A3 & !A2 & A1 & !A0

Block Diagram – Clock Interface - Clock Chip

Compatibility

The 82C451 is compatible with the VGA, EGA, Hercules, CGA and MDA display standards. In general, application software written for one of these standards can be run on a 82C451-based system if a monitor with a resolution equal to or greater than that display standard is used.
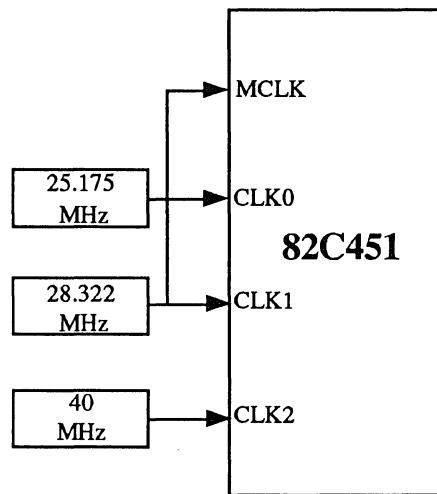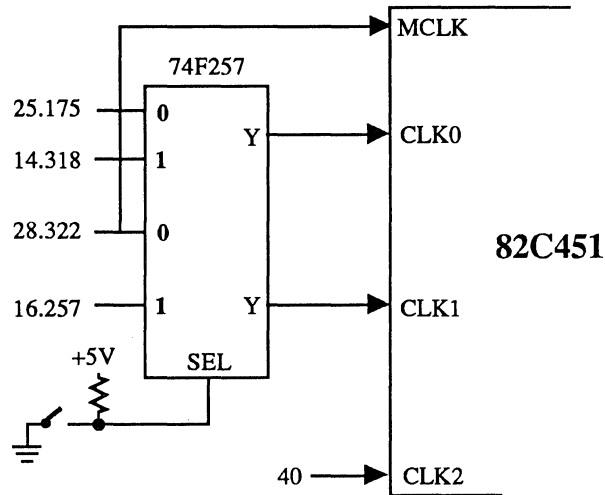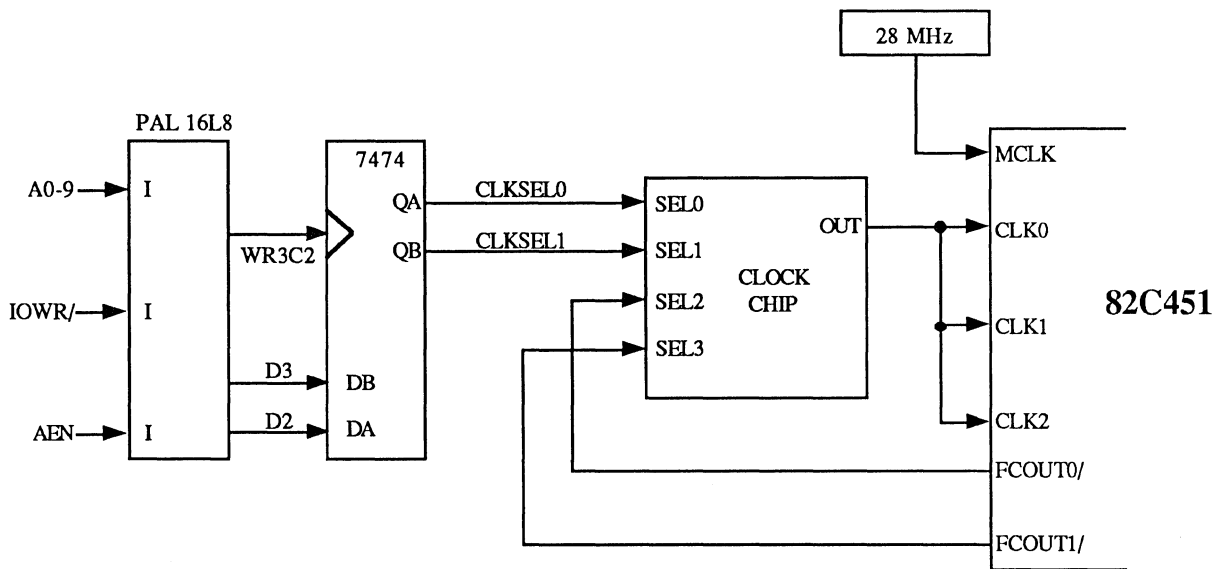
The 82C451 provides several features which aid in the implementation of a display system compatible with these standards. These features are as follows:

• Write protection of internal registers using a Write Protect Register (one of the Backward Compatibility registers). This ensures that writes to internal registers initiated by applications software do not corrupt register values, enabling user to run software written for previous graphics standards.

• Two sets of display parameter registers are supplied. The 82C451 automatically selects the set to be used based on the current display mode and the type of display in use.

Certain assumptions are made regarding the VGA and backward compatibility:

• No NMI or any other interrupts have to be used. It is possible to generate NMI traps if required to support auto emulation.

• On power up the chip is always in VGA mode.

• There is no separate EGA mode. EGA mode is considered to be a special case of VGA mode. Special bits are provided to Write Protect some EGA specific registers. Software that uses the EGA in standard modes will work with the 82C451.

• In an implementation the display (CRT) is known and fixed.

• A software program can be executed to switch the chip into and out of CGA or Hercules modes. The software utility is consistent with the exact display being used. The BIOS for the 82C451 available from Chips & Technologies includes software to program the 82C451 in the VGA, EGA, CGA, MDA and Hercules modes.

• CGA/MDA/Hercules software can run on any monitor (EGA, Multisync™ or PS/2).

• When in CGA or Hercules mode, all VGA/EGA registers are unavailable.

• EGA, CGA, MDA and Hercules modes will definitely function in the standard defined modes.

VGA REGISTER WRITE PROTECTION

To use the write protect features:

A. Initialize the CRT controller or alternate registers to generate sync signals for the display in use.

B. Write protect the CRT controller or alternate registers using the Write Protect Register.

C. Permit the applications software to write CRT or alternate registers as if a particular display was in use. The 82C451 will operate as if a standard I/O write took place but will not permit protected registers to be altered.

ALTERNATE REGISTER SETS

The 82C451 supplies two sets of Display Parameter Registers. These are summarized in the table below. To make use of these two sets:

1. Program one set for text mode and the other set for graphics mode.

2. Write protect both sets of registers using the Write Protect Register to prevent the application software from corrupting them.

The contents of the internal mode registers are interpreted automatically and either the text or graphics set of CRTC or alternate registers is selected accordingly to generate the correct display. Since the display memory format in text and graphics is identical, switching between these modes does not require CPU or application software intervention.

Display Parameter Registers used in CGA and Hercules modes:

Emulation	Mode	H Reg Set	V Reg Set
CGA	320x200	Alternate	Regular
CGA	640x200	Regular	Regular
Hercules	Text	Regular	Regular
Hercules	Graphics	Alternate	Regular

The BIOS supplied by Chips & Technologies can be used to initialize both sets of registers.

COMPATIBILITY MODE PROGRAMMING

To enable backward compatibility, the chip is programmed as follows:

VGA Mode

A. Program the 82C451 exactly analogous to IBM's VGA. Disable the additional bits in the new registers.

B. Select VGA mode (default).

EGA Mode

A. Program the 82C451 exactly analogous to IBM's VGA. Disable the additional bits in the new registers.

B. Write protect Group 4 registers. Also protect the external palette, clock select register, internal palette (if desired) and all CRT sync registers.

C. Force all 10th bits of vertical counters (including line compare) to 0.

D. Select the EGA type frame interrupt. This is controlled with bit-7 of Emulation Mode Register.

CGA Mode

A. Program the regular CRT registers for the 640 pixels horizontal mode. The horizontal sync rate must be consistent with the monitor used. Program the Alternate Horizontal Register for 320 pixels horizontal mode.

B. The vertical resolution can be 200 or 400 lines. The vertical sync rate must be consistent with the monitor used.

C. Load the font in the memory .

D. Pre-program all registers in Sequencer, Attribute Controller and Graphics Controller as in Mode 2.

E. Set the sync polarity as required for 200 or 400 lines.

F. Enable Double Scanning (if required by the monitor).

G. Program the CGA Mode Control Register (3D8h) and Color Palette Register (3D9h) as required. These registers are implemented in hardware.

H. Write Protect Group 1, Group 3, and Group 4 registers.

I. Select CGA mode.

The 82C451 will automatically respond to 320/640 pixels/line and text/graphics mode as defined in the CGA Mode Control Register (3D8h). In 40 column

CGA modes, the alternate CRTC registers are used.

MDA Mode

A. Program the regular CRT registers in the 720 pixels horizontal mode with 9 pixels/character. The horizontal sync rate must be consistent with the monitor used.

B. The vertical resolution must be 350 lines. The vertical sync rate must be consistent with the monitor used.

C. Load the font in memory .

D. Pre-program all registers in Sequencer, Attribute Controller and Graphics Controller as in Mode 7.

E. Set the sync polarity as required for 350 lines.

F. Write Protect Group 1, Group 3, and Group 4 registers.

G. Select MDA mode.

H. Hercules Control Registers do not work in this mode.

HERCULES Mode

A. Program the regular CRT registers for 720 pixels horizontal mode with 9 dots/character. Program the alternate registers for 720 pixels with 8 dots/character. The clock divide parameter must be set to divide by 8 (not 9).

B. The vertical resolution must be 350 lines. The vertical sync rate must be consistent with the monitor used. The vertical display end must be programmed to 350 Lines (Text Mode). In Graphics mode, 2 lines will automatically be subtracted. The Vertical Sync and Blank parameters must be programmed greater than 350 lines.

C. Load the font in the memory.

D. Pre-program all registers in the Sequencer, Attribute Controller, and Graphics Controller as in Mode 7. The 8/9 divide bit in the sequencer must be set to divide by 8.

E. Set the sync polarity as required for 350 lines.

F. Program the Display Mode Control Register (3B8h) and Hercules Configuration Register (3BFh) as required. These registers are implemented in hardware.

G. Write Protect Group 1, Group 2, and Group 3 registers.

H. Select Hercules mode.

The 82C451 will automatically respond to text, half graphics and full graphics modes as defined in the Mode Control Registers (3B8h and 3BFh). The regular CRT Offset Register is used in Hercules text mode. In Hercules graphics mode, the offset is defined in the Alternate Offset and Auxiliary Offset Registers. The Alternate Horizontal Registers are used in the Hercules Graphics mode.

When Emulation is enabled and the extended registers are disabled, bits 1 and 2 of the CRTC Register addresses are ignored (Similar to CGA and Hercules). The CRTC Registers occupy addresses 3B0h - 3B7h (3D0h - 3D7h).

AUTO EMULATION TRAPS

The 82C451 also supports trap generation for auto emulation purposes. The traps can be enabled on various conditions as defined in the Trap Enable Register. Traps are generated for I/O Write cycles only.

LIGHT PEN REGISTERS

In the CGA and Hercules modes, the contents of the Display Address counter is saved at the end of the frame before being reset. The saved value can be read in the CRT Controller Register space 10h and 11h. This allows simulating the Light Pen Hit technique to detect text/graphics modes on the CGA/Hercules cards.

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82C451 Electrical Specifications

82C451 ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Max	Units
P_D	Power Dissipation	–	1	W
V_{CC}	Supply Voltage	–0.5	7	V
V_I	Input Voltage	–0.5	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	85	°C
T_{STG}	Storage Temperature	–40	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

82C451 NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
T_A	Ambient Temperature	0	55	°C

82C451 DC CHARACTERISTICS (Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Max	Units
I_{CC1}	Power Supply Current	@28.332 MHz CLK, 0°C, 5.25V	–	150	mA
I_{IL}	Input Leakage Current		–100	+10	uA
I_{OZ}	Output Leakage Current	High Impedance	–10	+10	uA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA (RDY,IRQ,TRAP/,VGAREQ/,RAS/,WE/)	–	0.45	V
	(@4.75V)	I_{OL} = 4 mA (all others)	–	0.45	V
V_{OH}	Output High Voltage	I_{OL} = –8 mA (RDY,IRQ,TRAP/,VGAREQ/,RAS/,WE/)	2.4	–	V
	(@4.75V)	I_{OH} = –4 mA (all others)	2.4	–	V

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

82C451 AC TIMING CHARACTERISTICS - CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_C	CLK Period (40 MHz)		25		–	nS
T_{CH}	CLK High Time		$0.45T_C$	–	$0.55T_C$	nS
T_{CL}	CLK Low Time		$0.45T_C$	–	$0.55T_C$	nS
T_M	MCLK Period	25-30 Mhz	33	–	40	nS
T_{MH}	MCLK High Time		$0.45T_M$	–	$0.55T_M$	nS
T_{ML}	MCLK Low Time		$0.45T_M$	–	$0.55T_M$	nS
T_{RF}	Clock Rise / Fall		–	–	$0.05T_C$	nS
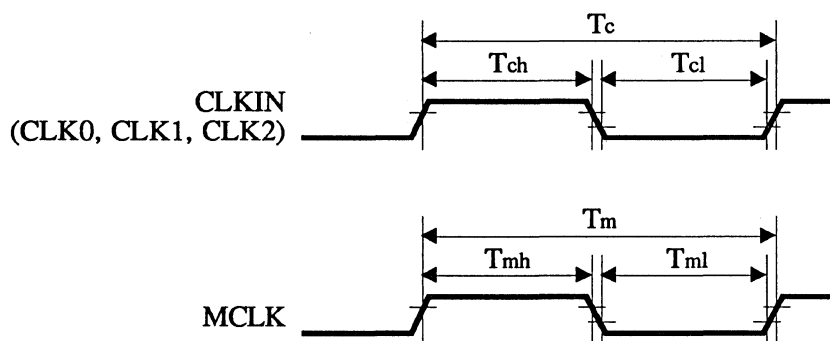
82C451 Clock Timing

82C451 AC TIMING CHARACTERISTICS - RESET TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{RST}	RESET Pulse Width		64 T_C	–	–	nS

Note: In CLKIN/2 mode, T_{RST} must be 128 Tc minimum

82C451 AC TIMING CHARACTERISTICS - AD BUS MULTIPLEXER TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{dnh}	Strobe falling to ADREN/ rising		–	–	15	nS
T_{dnl}	Strobe rising to ADREN/ falling		–	–	15	nS
T_{rdl}	ADREN/ rising to RDLO/ and/or RDHI/ falling		–	–	20	nS
T_{rdh}	ADREN/ falling to RDLO/ and/or RDHI/ rising		–	–	20	nS
T_{dd}	ADREN/ rising to write data valid		–	–	20	nS

Strobe (CMD/ for MCA; IORD/,
IOWR/, MEMR/, or MEMW/ for ISA)

CMD/

ADREN/

T_{dnh} T_{dnl}

RDLO/, RDHI/

T_{rdl} T_{rdh}

Data (Write)

T_{dd}
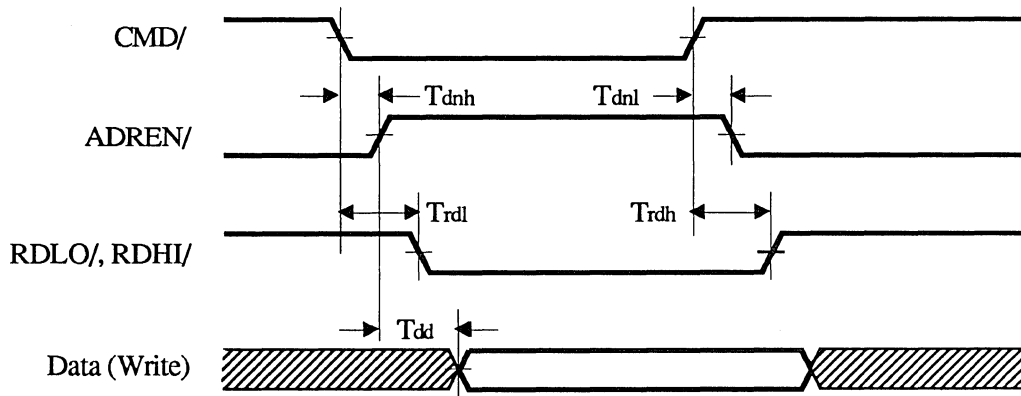
82C451 AD Bus Multiplexer Timing

82C451 AC TIMING CHARACTERISTICS - ISA BUS TIMING

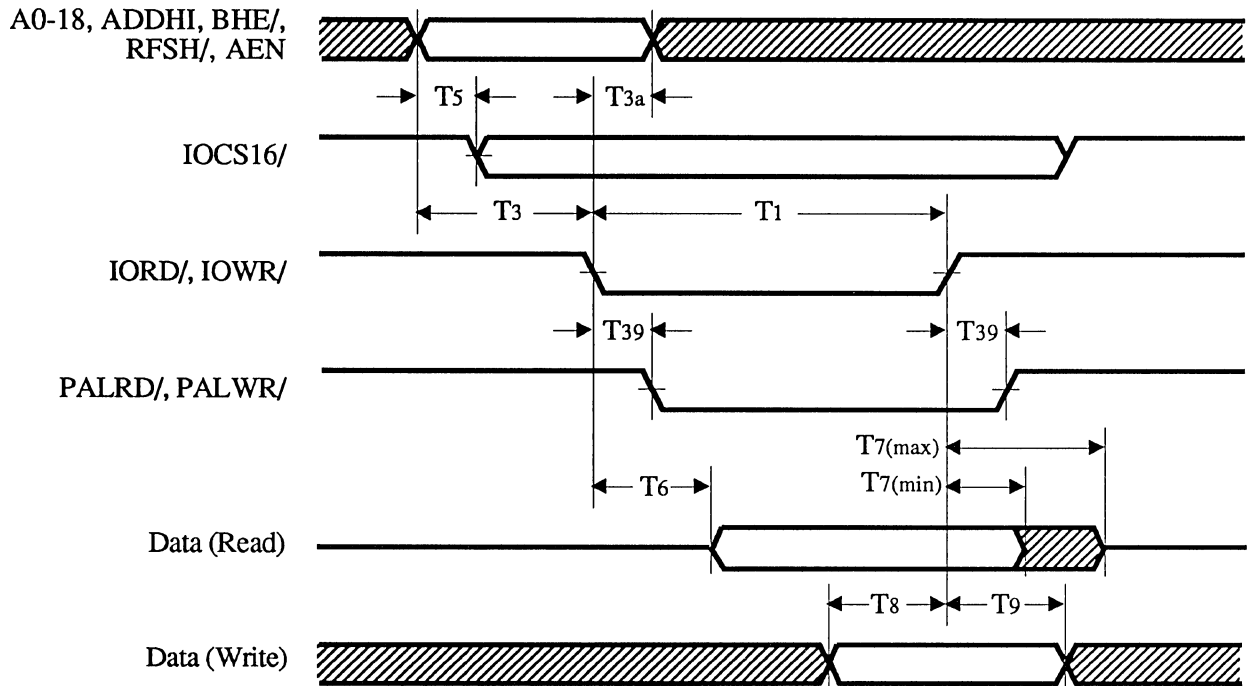| Symbol	Parameter	Notes	Min	Typ	Max	Units
T1	IORD/, IOWR/ Pulse Width		175	–	–	nS
T2	MEMR/, MEMW/ Pulse Width		175	–	–	nS
T3	Address setup to Read/Write		30	–	–	nS
T3a	Address hold from Read/Write Signal		20	–	–	nS
T4	MEMR/, MEMW/ hold from RDY (Memory)		0	–	–	nS
T5	IOCS16/ Delay from valid address		–	–	35	nS
T6	I/O Read Data delay from IORD/		–	–	50	nS
T7	I/O Read Data hold from IORD/		5	–	40	nS
T8	I/O Write Data setup to IOWR/		40	–	–	nS
T9	I/O Write Data hold from IOWR/		10	–	–	nS
T10	Memory Read Data hold from MEMR/		5	–	40	nS
T11	Memory Write Data hold from MEMW/		0	–	–	nS
T12	MEMR/, MEMW/ to RDY Low delay		–	–	30	nS
T13	Memory Read Data setup to RDY		25	–	–	nS
T14	Memory Write Data setup to RDY		40	–	–	nS
T15	RDY width		7Tc	–	128Tc	nS
T39	PALRD/, PALWR/ delay from Read/Write		–	–	25	nS

CHIPS®

A0-18, ADDHI, BHE/,
RFSH/, AEN

T5   T3a

IOCS16/

T3   T1

IORD/, IOWR/

T39   T39

PALRD/, PALWR/

T7(max)
T7(min)

T6

Data (Read)

T8   T9

Data (Write)

ISA Bus I/O Cycle Timing

A0-18, ADDHI, BHE/,
RFSH/, AEN

T3   T3a

T2

MEMR/, MEMW/

T12   T15   T4

RDY

T10 (max)

T10 (min)

T13

Data (Read)

T14   T11

Data (Write)
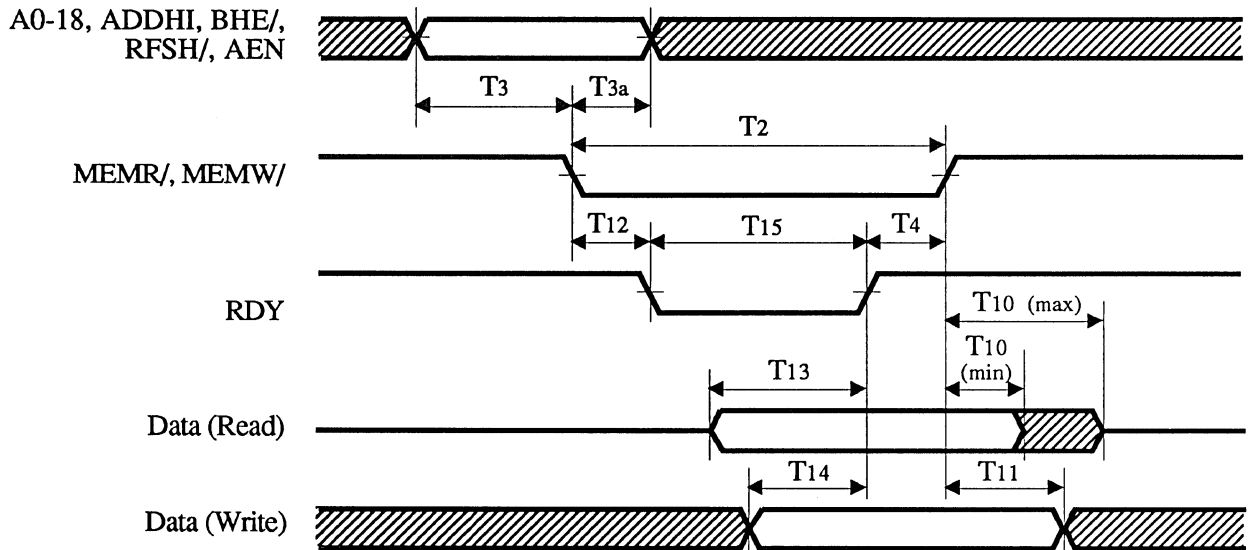
ISA Bus Memory Cycle Timing

82C451 AC TIMING CHARACTERISTICS - MCA BUS TIMING

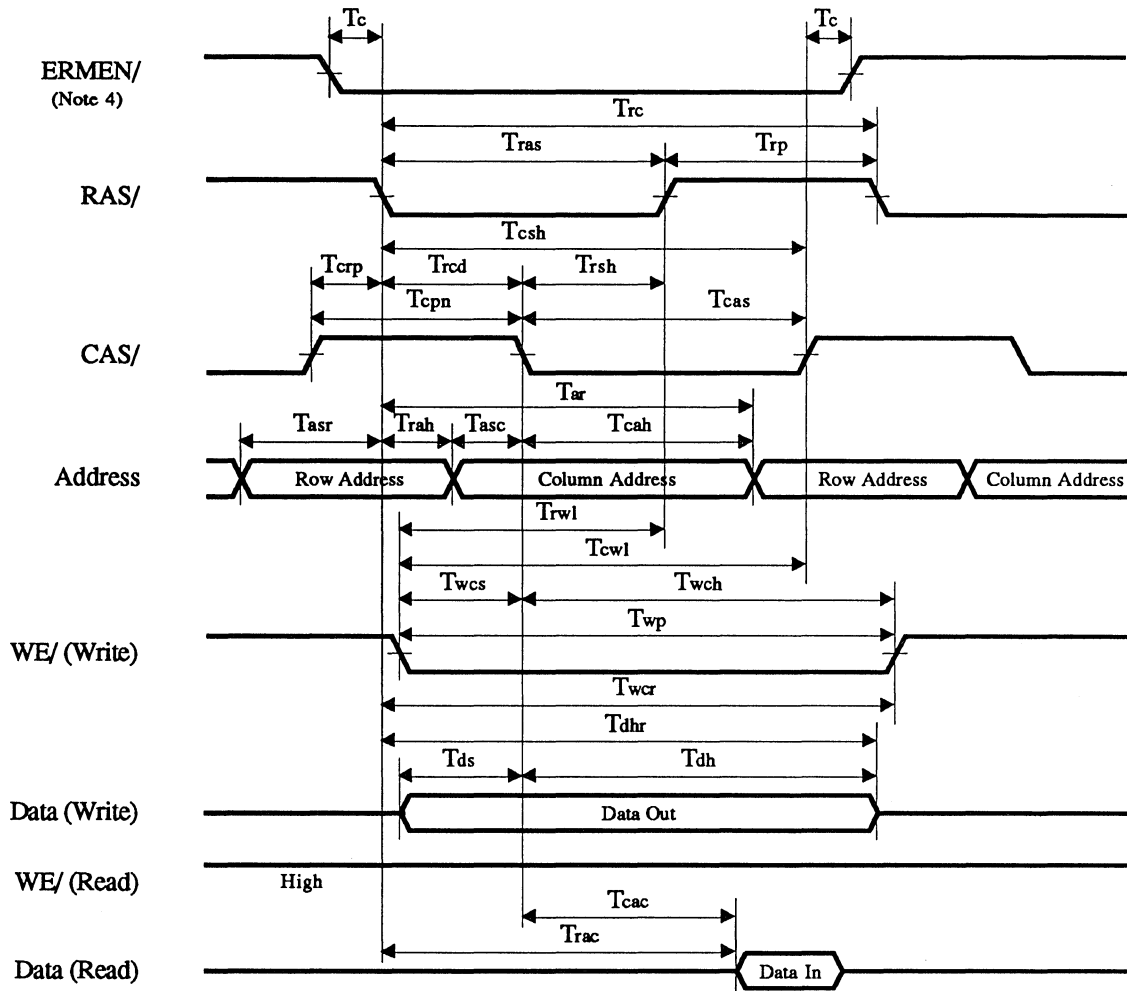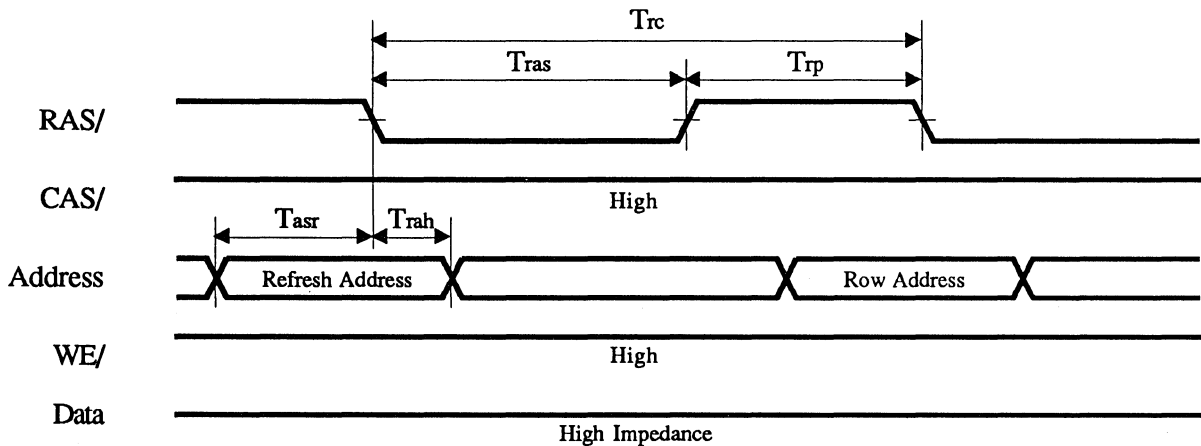| Symbol	Parameter	Notes	Min	Typ	Max	Units
T16	Status hold from CMD/		20	–	–	nS
T17	Status active from address valid		0	–	–	nS
T18	BHE/ Setup to CMD/		30	–	–	nS
T19	BHE/ hold from CMD/		20	–	–	nS
T19A	Address hold from CMD/		25	–	–	nS
T20	CMD/ active from Status		30	–	–	nS
T21	CMD/ from address valid		80	–	–	nS
T22	CMD/ Pulse Width		80	–	–	nS
T23	CMD/ inactive to next CMD/		80	–	–	nS
T24	Write data setup to CMD/		5	–	–	nS
T25	Write data hold from CMD/		10	–	–	nS
T26	Read data valid from CMD/		–	–	50	nS
T27	Read data hold from CMD/		0	–	40	nS
T28	Status to Read data valid		–	–	125	nS
T29	DS16/ active from address valid		–	–	30	nS
T30	DS16/ inactive from Status		5	–	25	nS
T31	CSFB/ active from address valid		–	–	30	nS
T32	CSFB/ inactive from Status		5	–	25	nS
T33	VGAREQ/ active from address valid		–	–	30	nS
T34	VGAREQ/ inactive from Status		5	–	25	nS
T35	RDY active from CMD/ high		65	–	–	nS
T36	Read data from RDY active (high)		–	–	50	nS
T37	RDY inactive (low) from Status		–	–	25	nS
T39	PALRD/, PALWR/ delay from CMD/		–	–	25	nS
Tmc	VGA Cycle Time		160	–	–	nS
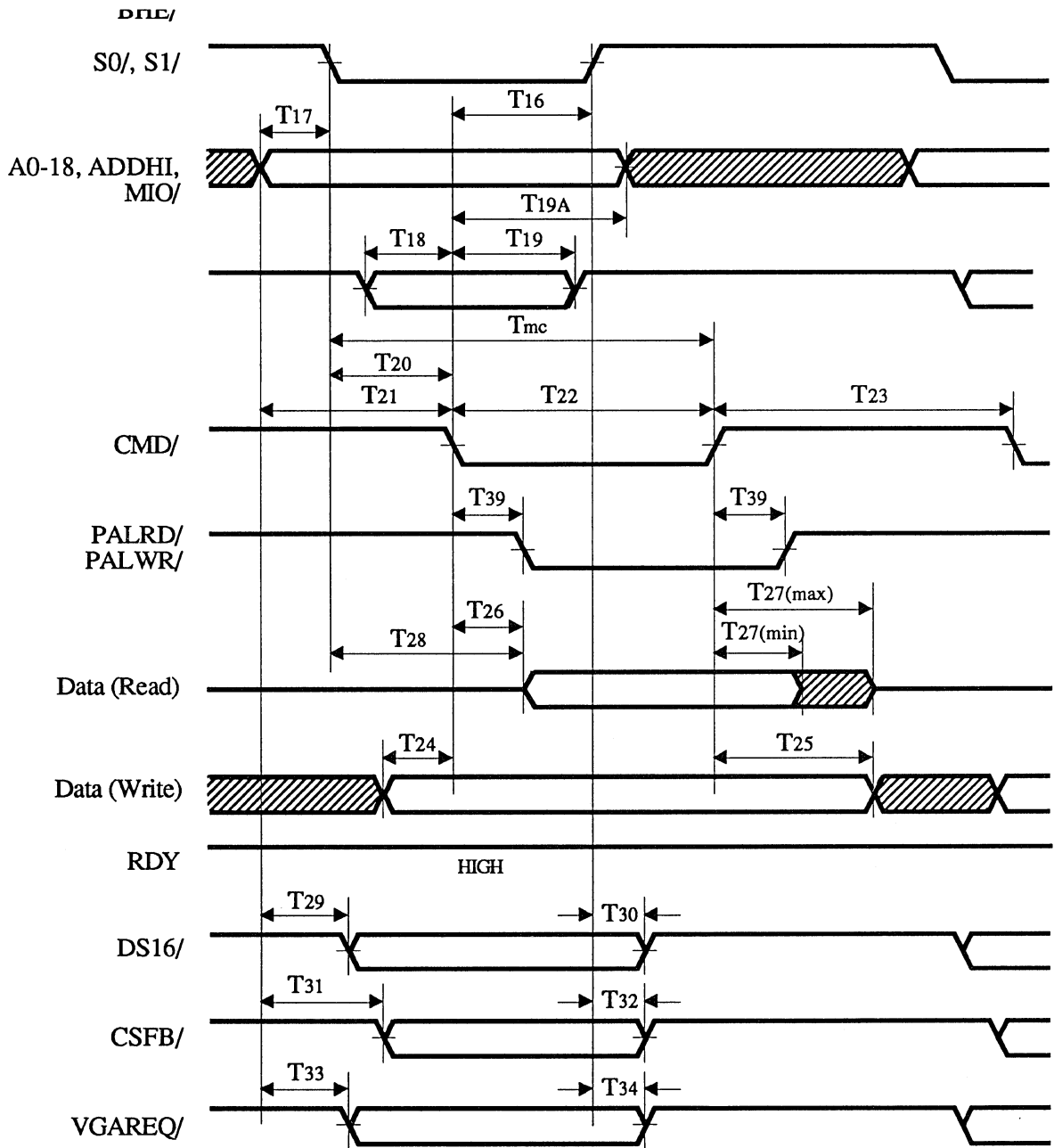
MCA Bus I/O Cycle Timing
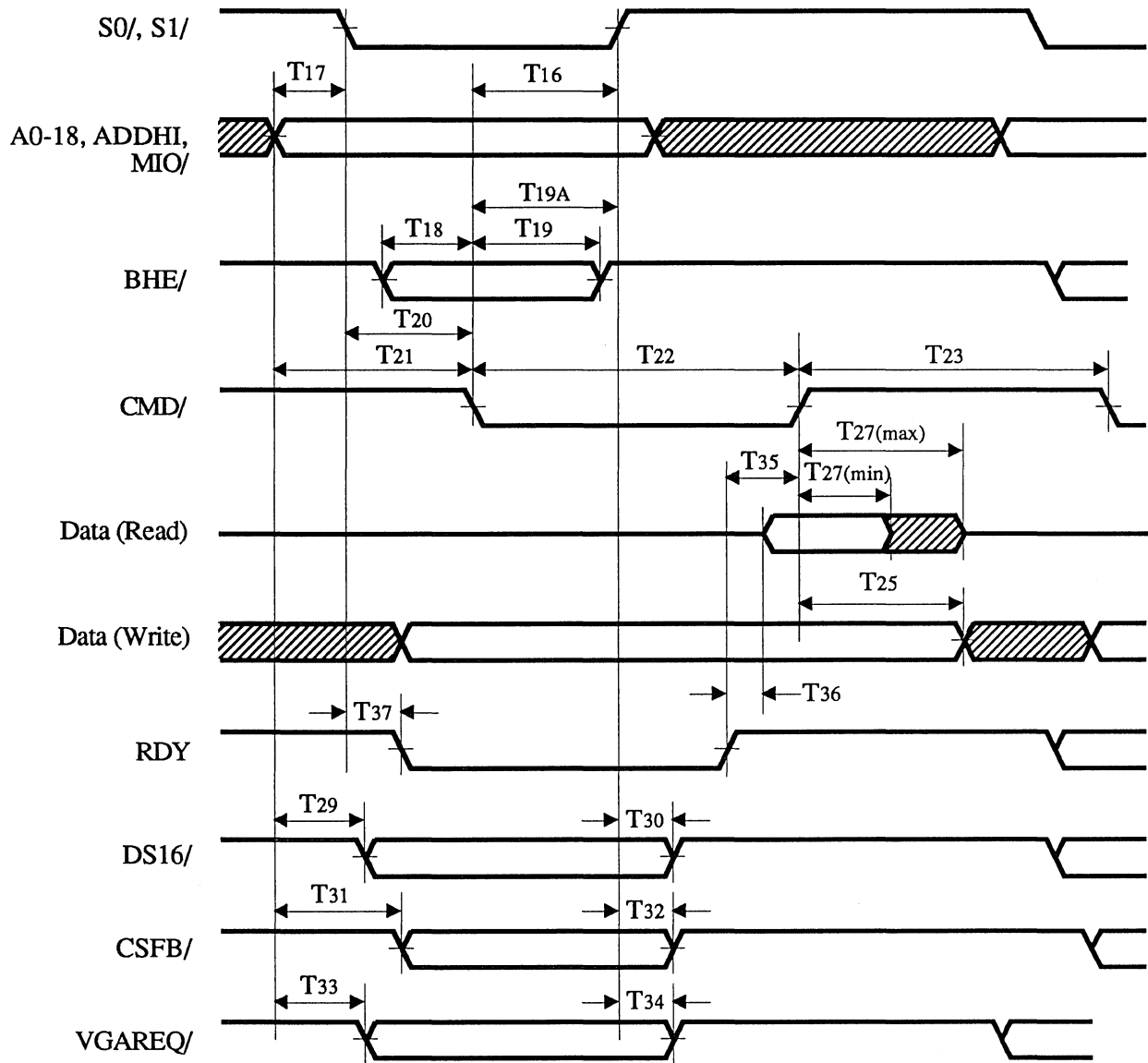
MCA Bus Memory Cycle Timing

82C451 AC TIMING CHARACTERISTICS - DRAM TIMING

Symbol	Parameter	8 Dot Mode Min	Max	9 Dot Mode Min	Max	Units
Trc	Read/Write Cycle Time	7Tc	–	8Tc	–	nS
Tras	RAS/ Pulse Width	4Tc	–	4Tc	–	nS
Tar	Column Address Hold from RAS/	5Tc	–	5Tc	–	nS
Trp	RAS/ Precharge	3Tc	–	4Tc	–	nS
Tcrp	CAS/ to RAS/ precharge	Tc-2	–	2Tc-2	–	nS
Tcsh	CAS/ Hold from RAS/	6Tc-3.5	–	6Tc-3.5	–	nS
Trcd	RAS/ to CAS/ delay	2Tc-1	–	2Tc-1	–	nS
Trsh	RAS/ Hold from CAS/	2Tc	–	2Tc	–	nS
Tcpn	CAS/ Precharge	3Tc	–	4Tc	–	nS
Tcas	CAS/ Pulse Width	4Tc-4.5	–	4Tc-4.5	–	nS
Tasr	Row Address Setup to RAS/	2Tc-18	–	3Tc-18	–	nS
Tasc	Column Address Setup to CAS/	Tc-10	–	Tc-10	–	nS
Trah	Row Address Hold from RAS/	Tc	–	Tc	–	nS
Tcah	Column Address Hold from CAS/	3Tc	–	3Tc	–	nS
Tcac	Data Access Time from CAS/	–	3Tc	–	3Tc	nS
Trac	Data Access Time from RAS/	–	5Tc	–	5Tc	nS
Trcs	Read CMD/ Setup time	2Tc-6	–	2Tc-6	–	nS
Trrh	Read Hold Time from RAS/	3Tc	–	4Tc	–	nS
Trch	Read Hold Time from CAS/	Tc	–	2Tc	–	nS
Twp	WE/ Pulse Width	7Tc-2.5	–	8Tc-2.5	–	nS
Tds	Write Data Setup to CAS/	2Tc-5	–	2Tc-5	–	nS
Tdh	Write Data Hold from CAS/	5Tc	–	6Tc	–	nS
Tdhr	Write Data Hold from RAS/	7Tc	–	8Tc	–	nS
Twch	WE/ Hold from CAS/	5Tc	–	6Tc	–	nS
Twcs	WE/ Setup to CAS/	2Tc-8	–	2Tc-8	–	nS
Trwl	WE/ Lead to RAS/	4Tc-12	–	4Tc-12	–	nS
Tcwl	WE/ Lead to CAS/	6Tc-11	–	6Tc-11	–	nS
Twcr	WE/ Hold from RAS/	7Tc	–	8Tc	–	nS

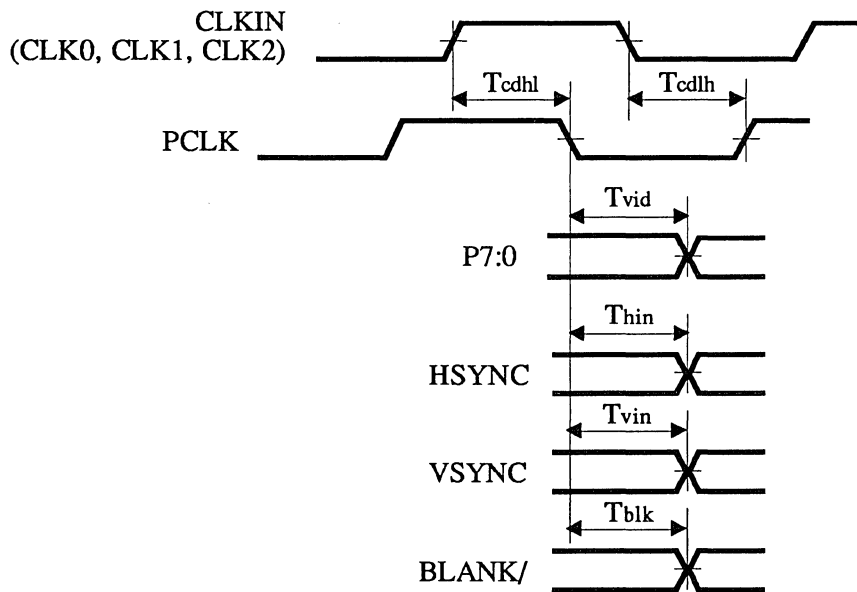**DRAM Read / Write Cycle Timing**

DRAM Refresh Cycle Timing

NOTE: *ERMEN is active (Low) only during CPU memory cycles*

82C451 AC TIMING CHARACTERISTICS - VIDEO TIMING

Symbol	Parameter	Min	Typ	Max	Units
Tcdhl	CLKIN Rise to PCLK Fall Delay	7	–	11.5	nS
Tcdlh	CLKIN Fall to PCLK Rise Delay	6	–	11	nS
Thin	HSYNC delay from PCLK falling edge	14	–	26	nS
Tvin	VSYNC delay from PCLK falling edge	10	–	22	nS
Tblk	BLANK/ delay from PCLK falling edge	3	–	6	nS
Tvid	Video delay from PCLK falling edge	1	–	7	nS

CLKIN
(CLK0, CLK1, CLK2)

Tcdhl   Tcdlh

PCLK

Tvid

P7:0

Thin

HSYNC

Tvin

VSYNC

Tblk

BLANK/

82C451 Video Timing

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82C451 Mechanical Specifications

CHIPS®

144-Pin
Plastic Flat Pack

82C451

Lead Pitch
0.65 (0.0256)

Lead Width
0.30 ±0.10
(0.012 ±0.004)

Lead Length
See Note 2

Pin 1

See Note 1

Footprint 31.6 (1.244)
32.4 (1.276)

Footprint $\frac{31.6 \ (1.244)}{32.4 \ (1.276)}$

Lead Length
See Note 2

DIMENSIONS:
mm (in)

Clearance
$\frac{0.30 \ (0.012)}{0.60 \ (0.024)}$

Max Height
4.4 (0.173)

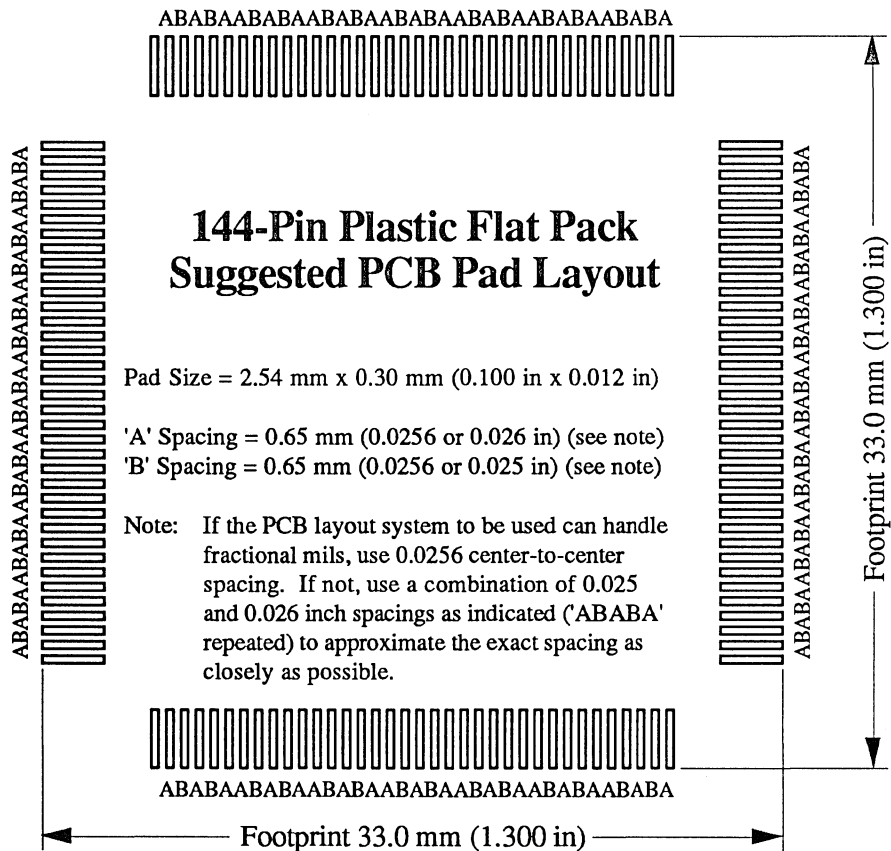Seating Plane
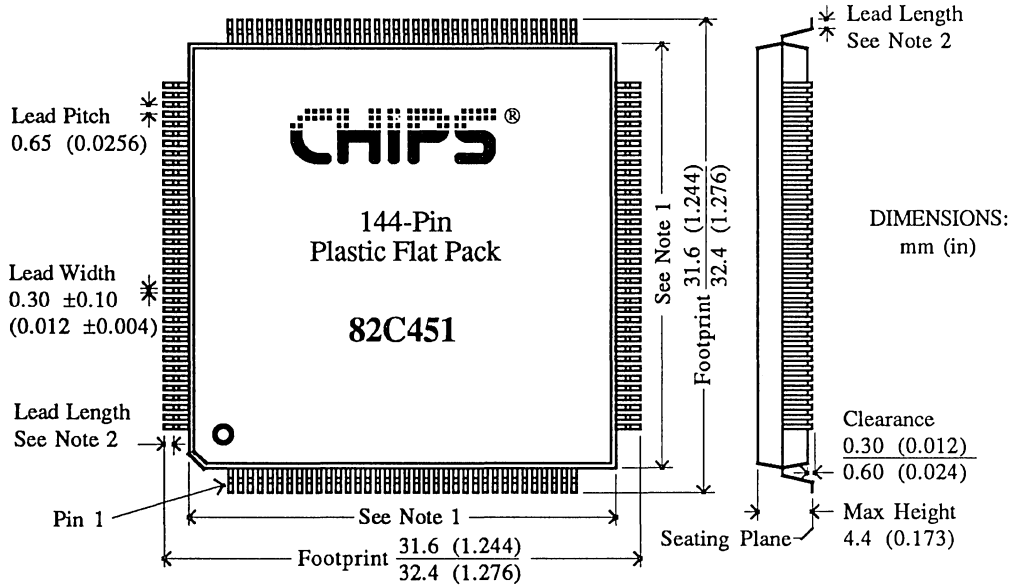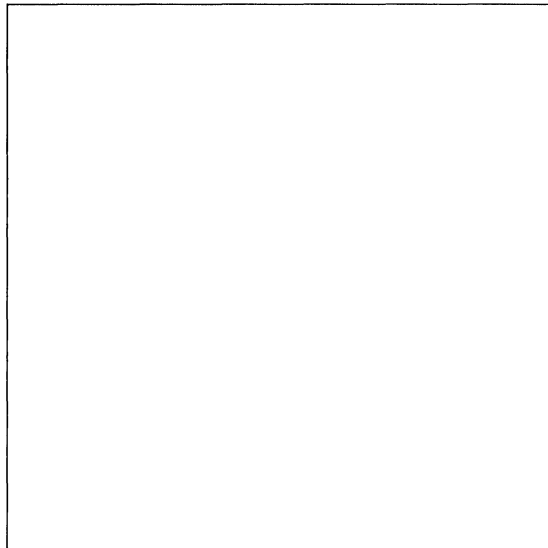
Note 1: Package Body Size = 28 ±0.2 (1.102 ±0.008)
Note 2: Lead Length = 0.8 ±0.2 (0.031 ±0.008)

82C451 Suggested PCB Pad Layout

ABABAABABAABABAABABAABABAABABAABABA

ABABAABABAABABAABABAABABAABABAABABA

144-Pin Plastic Flat Pack
Suggested PCB Pad Layout

Pad Size = 2.54 mm x 0.30 mm (0.100 in x 0.012 in)

'A' Spacing = 0.65 mm (0.0256 or 0.026 in) (see note)
'B' Spacing = 0.65 mm (0.0256 or 0.025 in) (see note)

Note: If the PCB layout system to be used can handle
fractional mils, use 0.0256 center-to-center
spacing. If not, use a combination of 0.025
and 0.026 inch spacings as indicated ('ABABA'
repeated) to approximate the exact spacing as
closely as possible.

ABABAABABAABABAABABAABABAABABAABABA

Footprint 33.0 mm (1.300 in)

Footprint 33.0 mm (1.300 in)