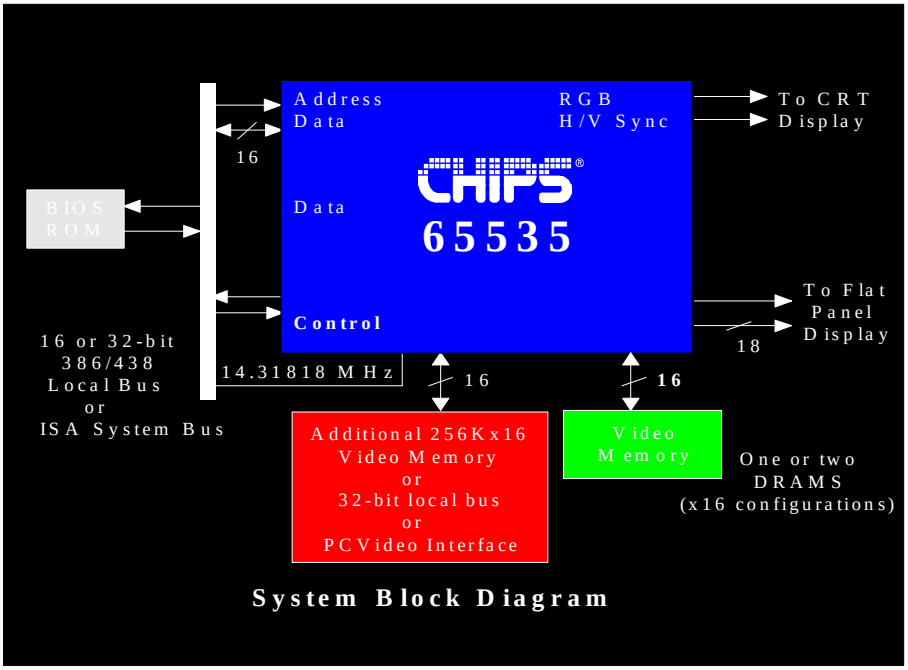
65535

High Performance Flat Panel / CRT VGA Controller

- Highly integrated design (flat panel/ CRT controller, RAMDAC, clock synthesizer, non-multiplexed bus direct panel drive)
- Integrated interface for Multiple Bus Architecture
  - Local bus (32-bit or 16-bit 386sx) including VL-Bus compatibility
  - EISA/ISA (PC/AT) Bus
- Flexible display memory configurations:
  - One 256Kx16 DRAM (512K)
  - Two 256Kx16 DRAMs (1MB)
  - Four 256Kx4 DRAMs (512K)
- VGA flat panel subsystem with color STN-DD. Simultaneous Display capability can be implemented with single 256Kx16 DRAM
- Programmable Linear Acceleration video memory addressing feature provides ability to "linearly map" video memory thus overcoming paging and I/O bottlenecks. High performance Linear Acceleration drivers are available for popular application programs such as Windows.
- Interface to CHIPS PC Video 69001A (82C9001A) and 69003/4 Video Windowing Controllers to display "live" video or specialized video overlay on flat panel displays.
- Supports LCD, EL and Plasma panels to 1280x1024 resolution
- Supports non-interlaced CRT monitors with resolutions up to 1024x256 colors
- Hi-color display capability (16-bits per pixel) with on-chip palette on flat panels and CRT monitors up to 640x480 resolution
- Direct interface to color and monochrome dual panel/dual drive (DD) and single panel/single drive (SS) panels (supports 8,9,12,15 and 18-bit data interfaces)
- Advanced Power Management features minimize power consumption during:
  - Normal operation
  - Standby (sleep) modes
  - Panel-off, Power-saving Mode
- Flexible on-board Activity timer facilitates ordered shutdown of the display system with optional backlight shutdown or 65535 entering low-power panel-off mode with flat panel powered down
- Power Sequencing control outputs regulate application of Bias voltage, +5V to the panel and +12V to the inverter for Backlight Operation
- Mixed 3.3V/5.0V +/-10% operation
- High performance resulting from zero wait-state writes (write buffer) and minimum wait-state read (internal Asynchronous FIFO design)
- SMARTMAP™ intelligent color-to-gray-scale conversion enhances text legibility
- Text enhancement feature improves white text contrast on flat panel displays
- Fully compatible with IBM® VGA and enhanced backward compatibility with EGA, CGA, Hercules™, and MDA without using NMIs
- EIAJ-standard 160-pin plastic flat pack
- Chip pinouts optimized for PCB layout



System Block Diagram

Product Overview

The 65535 High Performance, True Color VGA Flat Panel/CRT Controller provides a low-power, minimum chip-count graphics solution for high performance, full-features notebook and pen-based portable PCs. The 65535 requires only a single 256Kx16 DRAM to complete a VGA subsystem display with a color STN-DD panel and 34-bit local bus. This two chip implementation requires less than 2 square inches (1290 sq mm) of board space. As an option, the 65535 supports a second 256Kx16 DRAM which may be used as additional display memory to support CRT resolutions up to 1024x768 with 256 colors or 640x480 SX/DX, 486 'S' Series, and 386DX local bus, 16-bit 386SX local bus, and EISA/ISA buses. The 65535 employs separate address and data buses and direct flat panel drive capability, so that no external buffers are required.

High Performance Features

The 65535 employs a number of performance enhancement techniques, including direct 32-bit local bus, CPU, 32-bit memory interface capability, and integrated write buffer and linear memory addressing supported driver technology. CHIPS' software driver scores significantly higher than those obtainable with competing solutions based on a similar architecture.

Display Support

The 65535 supports a wide variety of monochrome and color Single-Panel, Single-Drive (S/S) and Dual-Panel, Dual Drive (D/D) passive STN and Single-Panel, Single Drive active matrix TFT/MIM LCDs. On CRT displays, the 65535 supports up to 1024x768 with 256 colors, 640x480 with 64K colors. With D/D-LCDs, the 65535 uses the upper portion of display memory as the frame buffer during simultaneous CRT/LCD display or LCD-only operation with a single 256x16 DRAM.

The 65535 provides many features to enhance flat panel display quality including multiple RGB color to gray scale reduction techniques, fast vertical centering, line replication or stretching, blank line insertion, tall font selection and text intensity enhancement. The CHIPS' proprietary polynomial-based Frame Rate Control(FRC) and dithering algorithm is programmable, producing optimum gray scales for a given panel model and reducing flicker without increasing the vertical refresh rate.

Power Management

The dedicated power pins for the 65535's interlogic, clock interface, bus interface, color palette, memory interface, and flat panel interface provide full 5.0V, 3.3V or "mixed" 3.3V and 5.0V operation in any combination. Both self-refresh and slow refresh (32KHz) type DRAMs are supported.

Two power saving-modes are supported by the 65535. In 'Panel-Off' mode, the 65535 turns of the flat panel, initiates a panel power sequence, and optionally turns off the palette. The 65535 'Standby' mode provides additional power savings by suspending all video activities allowing the input clocks to be shut off. The 'Standby' mode may be activated either through register programming or a hardware powerdown pin.

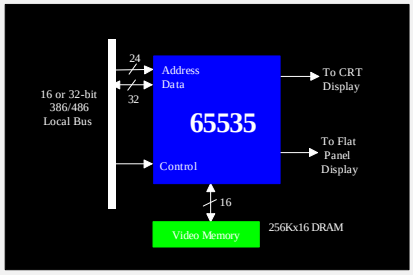
The 65535's programmable activity timer provides for powerdown of the backlight only on entering 'Panel-Off' mode independent of system BIOS. The 65535 provides an activity indicator output indicating any I/O or memory request to the VGA to facilitate external powerdown circuitry.

Software Support

The 65535 is fully compatible with the IBM VGA graphics standard register, gate and BIOS levels while providing full backwards compatibility with the EGA, CGA, MDA and Hercules graphics standards without using NMIs. CHIPS and third -party vendors supply VGA-compatible BIOS, end-user utilities, and extended mode software drivers for common application programs such as Windows, AutoCAD, WordPerfect, etc. CHIPS' drivers for Microsoft Windows provide the highest available performance in a controller of this architecture while offering visual enhancements specific for portable applications.

INTEGRATED 32-BIT LOCAL BUS SUPPORT

The 65535 provides lowest chip count solution for 32-bit local bus implementations. A complete high performance local bus graphics sub-system for the Intel 'S' series or other 32-bit CPU requires only the 65535 and a single 256Kx 16 DRAM. No external clock chips, buffers, glue logic, or ASICs are required for the 65535 local bus sub-system.



This unique configuration supports 32-bit local bus, linear acceleration, single-scan and dual-scan passive color and active matrix color LCDs, and simultaneous display.

Publication No.: PO27.3
Stock No: 067027-003
Revision: 1.0
Date: 7/31/95

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65535

High Performance
Flat Panel / CRT
VGA Controllers

Data Sheet

March 1994

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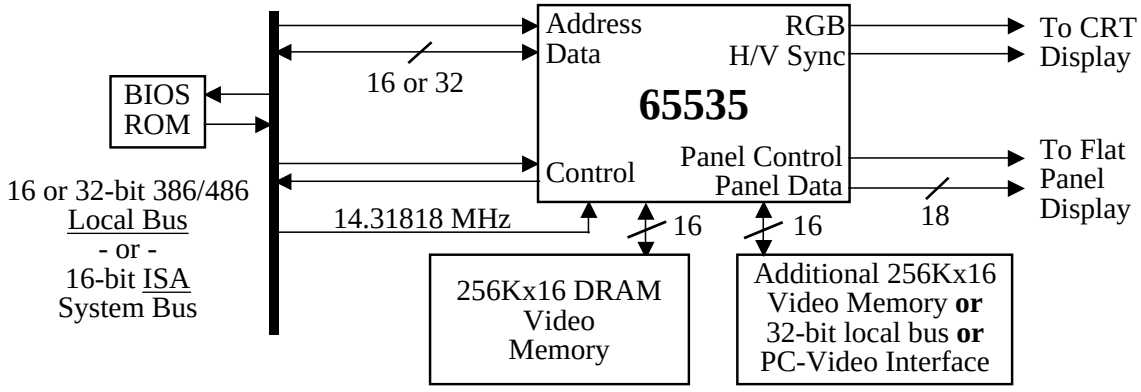
65535
High Performance
Flat Panel / CRT VGA Controller

- Highly Integrated Design (Flat Panel/CRT Controller, RAMDAC, Clock Synthesizer, non-multiplexed bus, direct panel drive)
- Integrated Interface for Multiple Bus Architectures
  - Local Bus (32-bit 386/486 or 16-bit 386SX) (including VL-Bus compatibility)
  - EISA/ISA (PC/AT) Bus
- Flexible display memory configurations:
  - One 256Kx16 DRAM (512KB)
  - Two 256Kx16 DRAMs (1MB)
  - Four 256Kx4 DRAMs (512KB)
- VGA Flat Panel subsystem with Color STN-DD Simultaneous Display capability can be implemented with single 256Kx16 DRAM
- Programmable Linear Acceleration video memory addressing feature provides ability to "linearly map" video memory thus overcoming paging and I/O bottlenecks. High performance Linear Acceleration drivers are available for popular application programs such as Windows.
- Interface to CHIPS' PC Video 69001A (82C9001A) and 69003/4 Video Windowing Controllers to display "live" video or specialized video overlay on Flat Panel displays
- Supports LCD, Electro Luminescent (EL), and Gas Plasma panels to 1280 x 1024 resolution
- Supports non-interlaced CRT monitors with resolutions up to 1024 x 768, 256 colors
- Hi-color display capability (16 bits per pixel) with on-chip palette on Flat Panels and CRT monitors up to 640x480 resolution
- Direct interface to Color and Monochrome Dual Panel / Dual Drive (DD) and Single Panel / Single Drive (SS) panels (supports 8, 9, 12, 15, and 18-bit data interfaces)
- Advanced Power Management features minimize power consumption during:
  - Normal Operation
  - Standby (Sleep) Modes
  - Panel-Off Power-Saving Mode
- Flexible on-board Activity Timer facilitates ordered shut-down of the display system with optional backlight shutdown or 65535 entering low power Panel-off mode with Flat Panel powered down
- Mixed 3.3V / 5.0V ±10% Operation
- Power Sequencing control outputs regulate application of Bias voltage, +5V to the Panel and +12V to the inverter for Backlight operation
- High Performance resulting from Zero Wait-State writes (write buffer) and minimum Wait-State reads (internal Asynchronous FIFO design)
- SMARTMAP™ intelligent Color-to-Gray-Scale Conversion enhances text legibility
- Text Enhancement feature improves white text contrast on Flat Panel displays
- Fully Compatible with IBM™ VGA and Enhanced Backward Compatibility with EGA, CGA, Hercules™, & MDA without using NMIs
- EIAJ-standard 160-pin Plastic Flat Pack
- Chip Pinouts optimized for PCB Layout



System Diagram

Revision History

Revision	Date	By	Comment
0.1	12/92	SV/JS	Internal Review - Rough Draft
0.2	2/93	BD/AT	Revised Introduction Section
0.3	5/93	DH/JS	Added VGA Registers, Programming, Panel Timing, Application Schematics, Panel Interfaces, and Electrical Specifications
1.0	6/93	DH	Official Release
2.0	3/94	JS/BB/DH	Removed references to 24bpp True-Color support from features list & intro Moved Standby Mode Signal Status tables from Intro. to Pin Description Fixed typo in configuration pin table (AA0 & AA1 in 1.0 Data Sheet pg 23) Added CRT Power Management section to intro (DPMS support) Updated Supported Video Modes table Changed pin name: pin 104 AA4 (CFG4) (EV#) Changed bus config pin names: BRDY# to LRDY# & BLAST# to GND Made same changes in Pin Descriptions section Removed PI & MC pin descriptions (no longer supported) All 'Reserved' notation changed to 'Reserved (0)' in Registers section Changed M2D6 to M3D6 and M3D2 to M2D2 in GR05 Changed Config Register XR01 (assigned CFG4; other misc changes made) Added XR03, XR29, and XR73 register definitions Added bit descriptions to Software Flags Registers 0 & 2 (XR0F & XR44) Changed Panel Format Register 2 (XR4F) to match 65540 Data Sheet Changed name of XR53 to 'Panel Format Register 3' to match 65540 Edited Panel Power Sequencing Delay Register (XR5B) Fixed definitions of XR5C bit-0 and XR05 bits 1-2 Added XR0B bit-3 definition Added 'Functional Description' section Added 'Panel Timing' section Fixed programming parameters for some panels Changed Bus Interface Application Schematics - ADDHI, LRDY#, BLAST#, & RDYRTN# connections Removed PI & MC bus interface schematics Changed Panel/CRT Output Application Schematic - Added VESA Display Data Channel (DDC) connections - Changed RSET Value from 383 to 270 ohms - Fixed typo on connector pin J3-40 Fixed typos in PC-Video Interface Application Schematic Updated Panel Interface Schematics & added worksheet parameter tables Fixed Monochrome SS 8-bit panel interface schematics Modified Timing Section Operating & standby current specifications added Local Bus section rewritten ALE Timing added to ISA PI & MC Bus timing removed Clock Timing modified Parameters added to RESET timing Changed RESET timing in Electrical Specifications

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Introduction

The 65535 VGA Flat Panel / CRT controller provides a low-power, minimal chip-count graphics solution for high performance, full-featured notebook and pen-based portable PCs. Through the innovative frame-buffer design, a single 256Kx16 DRAM chip is the only additional component required to implement a complete flat panel graphics subsystem which supports simultaneous flat panel / CRT operation with all panel types including dual scan color STN-DD panels. A complete a VGA sub-system can be implemented in less than 2 square inches (1290 sq mm). As an option, the 65535 supports an additional 256Kx16 DRAM, which may be used as additional display memory to support CRT resolutions up to 1024x768 with 256 colors and up to 640x480 with 64K colors (16bpp "high color" modes). The 65535 can directly interface to the 32-bit 486DX/SX and 386DX local bus, 16-bit 386SX local bus, and EISA/ISA buses. The 65535 employs separate address and data buses and direct flat panel drive capability, so that no external buffers are required.

The 65535 employs a number of performance enhancement techniques, including direct 32-bit local bus CPU or 32-bit memory interface capability, an integrated write buffer and FIFO, and linear addressable display memory.

The 65535 supports a wide variety of monochrome and color Single-Panel, Single-Drive (S/S) and Dual-Panel, Dual-Drive (D/D) passive STN-DD and active-matrix TFT / MIM LCDs, EL and plasma panels. The 65535 supports monochrome panels with resolutions up to 1280x1024 16 gray scales or 1024x768 64 gray scales. The 65535 produces up to 226,981 colors on passive STN-DD LCDs, up to 185,193 colors on 512-color active-matrix LCDs, and up to 1,771,561 colors on 4,096-color active-matrix LCDs:

9-bit '512-Color'	12-bit '4096-Color'	Dither	FRC
512 (8^3)	4096 (16^3)	No	No
3,375 (15^3)	29,791 (31^3)†	No	Yes
24,389 (29^3)	226,981 (61^3)	Yes	No
185,193 (57^3)	1,771,561 (121^3)†	Yes	Yes

† New capability in 65535, not available in 65530

The 65535 supports 4,096-color active matrix panels with resolutions up to 1280x1024 16 colors and 1024x768 256 colors. In addition, the 65535 simultaneously displays 64K colors at 640x480 resolution on 18-bit "high color" active-matrix LCDs. The 65535 provides a variety of programmable features to optimize display quality, such as Vertical and Horizontal Compensation, SMARTMAP™, Text Enhancement, three selectable color to gray scale reduction techniques, and a polynomial FRC gray scale algorithm, which reduces flicker on fast response "mouse quick" LCDs without diminishing gray scale linearity.

The 65535 employs a variety of advanced power management features to reduce power consumption of the display subsystem and extend battery life. The 65535's internal logic, memory interface, bus interface and flat panel interface can be independently configured to operate at either 3.3V or 5.0V. The 65535 is optimized for minimum power consumption during normal operation and two power-savings modes – Panel Off and Standby. During Panel Off, the 65535 turns off the flat panel, and the VGA sub-system remains active. The palette may also be automatically shut off during Panel Off mode to further reduce power consumption. During Standby, the 65535's CPU interface is inactive, and the 65535 internal logic is powered down. During Standby mode, the 65535 suspends all CPU, memory and display activities. In this mode, the 65535 places the DRAM in the self-refresh mode of operation, and the 65535's reference clock input can be shut off. The 65535 also supports a programmable activity timer which monitors VGA activity. After all display activity ceases, the timer will automatically shut the panel down by either disabling the backlight or putting the 65535 into Panel Off mode.

The 65535 is fully compatible with the VGA graphics standard at the register, gate, and BIOS levels. The 65535 provides full backwards compatibility with the EGA, CGA, MDA and Hercules graphics standards without using NMIs. CHIPS' and third-party vendors supply fully VGA-compatible BIOS, end-user utilities and drivers for common application programs (e.g., Windows, OS/2, Word Perfect, Lotus, etc.). CHIPS' drivers for Windows include a Big Cursor (to increase the cursor's legibility on monochrome flat panels) and a panning/scrolling driver (to increase performance).

MINIMUM CHIP COUNT / BOARD SPACE

The 65535 provides a minimum chip count/board space, yet highly flexible VGA sub-system. The 65535 integrates a high-performance VGA flat panel/CRT controller, industry-standard RAMDAC, clock synthesizer, monitor sense circuitry and an activity timer in a 160-pin plastic flat pack package. In its minimum configuration, the 65535 requires only a single 256Kx16 DRAM, such that a complete VGA sub-system for motherboard applications can be implemented with just two ICs. This configuration consumes less than 2 square inches (1290 sq mm) of board space and is capable of supporting simultaneous flat panel/CRT display requirements while directly interfacing to a 32-bit local bus. As an option, a second memory chip may be implemented to increase performance (via a 32-bit data path to display memory) and support graphics modes which require more than 512 KBytes of display memory. No external buffers or glue logic are required for the 65535's bus interface, memory interface or panel interface. The 65535 employs separate address and data buses with sufficient drive capability, such that the bus can be driven directly. The 65535 also provides up to 18 bits of panel data with sufficient drive capability such that virtually all flat panels can be driven directly.

DISPLAY MEMORY INTERFACE

The 65535 supports multiple display memory configurations, providing the OEM with the flexibility to use the same VGA controller in several designs with differing cost, power consumption and performance criteria. The 65535 supports the following display memory configurations:

- One 256Kx16 DRAM (512 KBytes)
- Two 256Kx16 DRAMs (1 MBytes)
- Four 256Kx4 DRAMs (512 KBytes)

Implementing the 65535 with a single 256Kx16 DRAM results in a cost-efficient, minimum-chip-count / board-space display sub-system. In this configuration, the 65535 supports standard and SuperVGA resolution modes on a flat panel or external CRT monitor. (Alternatively, four 256Kx4 DRAMs may be used for display memory).

Performance is significantly improved when the 65535 is configured with a 32-bit data path to display memory, which is accomplished by using two 256Kx16 DRAMs. Two 256Kx16 DRAMs support all standard, Super, and Extended VGA resolutions up to 1024x768 8bpp (256 colors) as well as 16bpp "High-Color" up to 640x480.

The table below summarizes the various display memory options and corresponding CRT and flat panel display capabilities.

Display memory control signals are derived from the integrated clock synthesizer's memory clock. The 65535 serves as a DRAM controller for the system's display memory. It handles DRAM refresh, fetches data from display memory for display refresh, interfaces the CPU to display memory, and supplies all necessary DRAM control signals.

The 65535 supports 'two-CAS / one-WE' DRAMs and 'one-CAS / two-WE' 256Kx16 DRAMs. The 65535 supports the self-refresh features of 256Kx16 DRAMs and certain 256Kx4 DRAMs during STANDBY mode, enabling the 65535 to be powered down completely during suspend/resume operation.

Memory Configuration	CRT Resolution	Simultaneous Display	PC Video / Overlay Support
(1) 256Kx16 DRAM (512 KBytes)	640x400 8bpp 640x480 8bpp 800x600 8bpp 1024x768 4bpp	Yes	Yes
(2) 256Kx16 DRAMs (1 MBytes)	640x480 16bpp 1024x768 8bpp 1280x1024 4bpp	Yes	No

Supported Display Memory Options & Display Resolutions

CPU BUS INTERFACE

The 65535 provides a direct interface to:

- 32-bit 486DX/SX and 386DX local bus
- 16-bit 386SX local bus
- EISA/ISA (PC/AT) bus

Strap options allow the user to configure the chip for the type of interface desired. Control signals for all interface types are integrated on chip. All operations necessary to ensure proper operation in these various environments are handled in a fashion transparent to the CPU. These include internal decoding of all memory and I/O addresses, bus width translations, and generation of necessary control signals.

HIGH PERFORMANCE FEATURES

The 65535 includes a number of performance-enhancement techniques including:

- Direct 32-bit local bus CPU support
- 32-bit memory interface with 16-bit local bus
- Integrated write buffer and FIFO
- Linearly addressable display memory

The 65535's 32-bit and 16-bit local bus operation provides significantly higher performance than the slower ISA bus. A 32-bit memory interface limits the CPU data bus to 16-bits. An optional 32-bit interface to display memory provides additional bandwidth for demanding configurations such as high speed local bus or simultaneous display with dual drive panels. When using an ISA-bus configuration, the 65535's write buffer enables zero wait-state cycle operation. The 65535's internal asynchronous FIFO design provides minimum wait-state reads and fast display updates.

The 65535's linearly addressable display memory allows display memory to be accessed in any area of upper memory up to 1 MByte in size. Software drivers optimized for linearly addressable memory improve video performance as much as 80%. These drivers are available from your local CHIPS sales office.

PC VIDEO / OVERLAY SUPPORT

The 65535 allows 18 bits of external RGB video data to be input and merged with the internal VGA data stream. The 65535 supports two forms of video windowing: (i) color key input and (ii) X-Y window keying. See extension registers XR3A to XR3F for description of the 65535 color keying feature. The X-Y window key input is an alternate function on pin 79 and can be used to position the live video window coordinates. The 65535 can be used in conjunction with Chips and Technologies, Inc. PC-Video products to provide portable multi-media solutions.

CPU Configuration	Memory Configuration	Simultaneous Display	PC Video/ Overlay Support
16-bit EISA/ISA (PC/AT) bus 16-bit 386SX VL bus	16-bit or 32-bit	Yes	Yes for 16-bit memory bus No for 32-bit memory bus
32-bit 486SX VL bus 32-bit 486DX VL bus 32-bit 386DX VL bus	16-bit only	Yes	No

Supported CPU / Bus Options

DISPLAY INTERFACE

The 65535 is designed to support a wide range of flat panel and CRT displays of all different types and resolutions.

Flat Panel Displays

The 65535 supports all flat panel display technologies including plasma, electroluminescent (EL) and liquid crystal displays (LCD). LCD panel interfaces are provided for single panel-single drive (SS) and dual panel-dual drive (DD) configurations. A single panel sequences data similar to a CRT (i.e., sequentially from one area of video memory). In contrast, a dual panel requires video data to be provided alternating from two separate areas of video memory. In addition, a dual drive panel requires the data from the two areas to be provided to the panel simultaneously. Due to its integrated frame buffer and 18-data-line panel interface, the 65535 supports all panels directly. Support for LCD-DD panels does not require external hardware such as a frame buffer. Support for high-resolution, 'high color' flat panels also does not require additional components. The 65535 handles display data sequencing transparently to applications software, providing full compatibility on both CRT and flat panel displays.

9-bit '512-Color'	12-bit '4096-Color'	Dither	FRC
512 (8^3)	4096 (16^3)	No	No
3,375 (15^3)	29,791 (31^3)†	No	Yes
24,389 (29^3)	226,981 (61^3)	Yes	No
185,193 (57^3)	1,771,561 (121^3)†	Yes	Yes

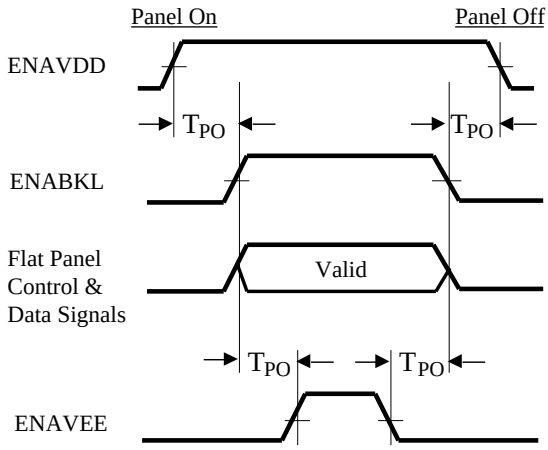
† New capability in 65535, not available in 65530

There is currently no standard interface for flat panel displays. Interface signals and timing requirements vary between panel technologies and suppliers. The 65535 provides register programmable features to allow interfacing to the widest possible range of flat panel displays. The 65535 provides a direct interface to panels from vendors such as Sharp, Sanyo, Epson, Seiko Instruments, Oki, Toshiba, Hitachi, Fujitsu, NEC, Matsushita/Panasonic and Planar.

PANEL POWER SEQUENCING

Flat panel displays are extremely sensitive to conditions where full biasing voltage VEE is applied to the liquid crystal material without enabling the control and data signals to the panel. This results in severe damage to the panel and may disable the panel permanently. The 65535 provides a simple and elegant method to sequence power to the flat panel display during various modes of operation to conserve power and provide safe operation to the flat panel. The 65535 provides three pins called ENAVEE, ENAVDD and ENABKL to regulate the LCD Bias Voltage (VEE), the driver electronics logic voltage (VDD), and the backlight voltage (BKL) to provide intelligent power sequencing to the panel. The timing diagram below illustrates the power sequencing cycle. In the 65535, the power on/off delay time (T_{PO}) is programmable (with a default of 32 mS).

The 65535 initiates a 'panel off' sequence if the STNDBY# input is asserted (low), or if XR52 bit-4 is set to a '1' putting the chip into Standby mode. The 65530 also initiates a 'panel off' sequence if the chip is programmed to enter 'panel off' mode (by setting extension register XR52 bit-3=1), or if the 'Display Type' is programmed to 'CRT' (extension register XR51 bit-2 transitions from '1' to '0'). The 65535 initiates a 'panel on' sequence if the STNDBY# input is high and the chip is programmed to 'panel on' (XR52 bit-3 transitions from a '1' to '0') and 'flat panel display' (XR51 bit-2 is set to '1').



Panel Power Sequencing

CRT Displays

The 65535 supports high resolution fixed frequency and variable frequency analog monitors in interlaced and non-interlaced modes of operation. Digital monitor support is also built in.

The 65535 supports resolutions up to 1024x768 256 colors or 640x480 65,536 colors in 1 MByte display memory configurations; 1024x768 16 colors or 640x480 256 colors are supported in 512 KByte display memory configurations. The following tables lists all 65535 CRT monitor video modes.

Supported Video Modes - VGA Standard

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	Max MCLK / DotClock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Video Memory	CRT
0+,1+	Text	16	40 x 25	9x16	360x400	56 / **28.322**	31.5	70	256 KB	A,B,C
			40 x 25	8x14	320x350	56 / 25.175	31.5	70	256 KB	A,B,C
			40 x 25	8x8	320x200	56 / 25.175	31.5	70	256 KB	A,B,C
2+,3+	Text	16	80 x 25	9x16	720x400	56 / **28.322**	31.5	70	256 KB	A,B,C
			80 x 25	8x14	640x350	56 / 25.175	31.5	70	256 KB	A,B,C
			80 x 25	8x8	640x200	56 / 25.175	31.5	70	256 KB	A,B,C
4	Graphics	4	40 x 25	8x8	320x200	56 / 25.175	31.5	70	256 KB	A,B,C
5	Graphics	4	40 x 25	8x8	320x200	56 / 25.175	31.5	70	256 KB	A,B,C
6	Graphics	2	80 x 25	8x8	640x200	56 / 25.175	31.5	70	256 KB	A,B,C
7+	Text	Mono	80 x 25	9x16	720x400	56 / **28.322**	31.5	70	256 KB	A,B,C
			80 x 25	9x14	720x350	56 / **28.322**	31.5	70	256 KB	A,B,C
			80 x 25	9x8	720x350	56 / **28.322**	31.5	70	256 KB	A,B,C
D	Planar	16	40 x 25	8x8	320x200	56 / 25.175	31.5	70	256 KB	A,B,C
E	Planar	16	80 x 25	8x8	640x200	56 / 25.175	31.5	70	256 KB	A,B,C
F	Planar	Mono	80 x 25	8x14	640x350	56 / 25.175	31.5	70	256 KB	A,B,C
10	Planar	16	80 x 25	8x14	640x350	56 / 25.175	31.5	70	256 KB	A,B,C
11	Planar	2	80 x 30	8x16	640x480	56 / 25.175	31.5	**60**	256 KB	A,B,C
12	Planar	16	80 x 30	8x16	640x480	56 / 25.175	31.5	**60**	256 KB	A,B,C
13	Packed Pixel	256	40 x 25	8x8	320x200	56 / 25.175	31.5	70	256 KB	A,B,C

Note: All of the above VGA standard modes are supported directly in the 65535 BIOS (both 32K and 40K BIOS versions).
All of the above VGA standard modes are supported at both 3.3V and 5V.
Max MCLK refers to the maximum clock rate required for proper mode operation.

CRT Codes:

A PS/2 fixed frequency analog CRT monitor or equivalent (31.5 / 35.5 KHz Horizontal Frequency Specification)

B Multi-Frequency CRT monitor (37.5 KHz Minimum Horizontal Frequency Specification) (NEC MultiSync 3D or equivalent)

C Multi-Frequency High-Performance CRT Monitor (48.5 KHz Min H Freq Specification) (Nanao Flexscan 9070s, MultiSync 5D, or equivalent)

Supported Video Modes - Extended Resolution

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	Max MCLK / DotClock (MHz) †	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Video Memory	CRT
20	4 bit Linear	16	80 x 30	8x16	640x480	56 / 25.175	31.5	60	512 KB	A,B,C
22	4 bit Linear	16	100 x 37	8x16	800x600	56 / 40.000	37.5	60	512 KB	B,C
24	4 bit Linear	16	128 x 48	8x16	1024x768	65 / 65.000	48.5	60	00000000	C
24 I						65 / 44.900	35.5	**43**		B,C
30	8 bit Linear	256	80 x 30	8x16	640x480	56 / 25.175	31.5	60	512 KB	A,B,C
32	8 bit Linear	256	100 x 37	8x16	800x600	65 / 40.000	37.5	60	512 KB	B,C
34	8 bit Linear	256	128 x 48	8x16	1024x768	65 / 65.000	48.5	60	1 MB	C
34 I						65 / 44.900	35.5	**43**		B,C
40	15bit Linear	32K	80 x 30	8x16	640x480	65 / 50.350	31.5	60	1 MB	A,B,C
41	16bit Linear	64K	80 x 30	8x16	640x480	65 / 50.350	31.5	60	1 MB	A,B,C
60	Text	16	132 x 25	8x16	1056x400	65 / 40.000	30.5	**68**	256 KB	A,B,C
61	Text	16	132 x 50	8x16	1056x400	65 / 40.000	30.5	**68**	256 KB	A,B,C
6A, 70	Planar	16	100 x 37	8x16	800x600	56 / 40.000	37.5	60	256 KB	B,C
72, 75	Planar	16	128 x 48	8x16	1024x768	65 / 65.000	48.5	60	512 KB	C
72, 75 I						65 / 44.900	35.5	**43**		B,C
78	Packed Pixel	16	80 x 25	8x16	640x400	56 / 25.175	31.5	**70**	256 KB	A,B,C
79	Packed Pixel	256	80 x 30	8x16	640x480	56 / 25.175	31.5	60	512 KB	A,B,C
7C	Packed Pixel	256	100 x 37	8x16	800x600	65 / 40.000	37.5	60	512 KB	B,C
7E	Packed Pixel	256	128 x 48	8x16	1024x768	65 / 65.000	48.5	60	1 MB	C
7E I						65 / 44.900	35.5	**43**		B,C

Note: Support for the modes in the above table is included directly in the BIOS (both 32K and 40K versions).
The 'I' in the mode # column indicates "Interlaced'.
Max MCLK refers to the maximum clock rate required for proper mode operation.

Supported Video Modes - High Refresh

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	Max MCLK / DotClock (MHz) †	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Video Memory	CRT
12*	Planar	16	80 x 30	8x16	640x480	56 / 31.500	37.5	75	256 KB	B,C
30	8 bit Linear	256	80 x 30	8x16	640x480	65 / 31.500	37.5	75	256 KB	C
79	Packed Pixel	256	80 x 30	8x16	640x480	65 / 31.500	37.5	75	512 KB	C
6A, 70	Planar	16	100 x 37	8x16	800x600	65 / 49.500	46.9	75	512 KB	C
32	8 bit Linear	256	100 x 37	8x16	800x600	65 / 49.500	46.9	75	1 MB	C
7C	Packed Pixel	256	100 x 37	8x16	800x600	65 / 49.500	46.9	75	1 MB	C

Note: Support for the modes in the above table is included in the 40K version of the BIOS.
Max MCLK refers to the maximum clock rate required for proper mode operation.

† Refer to Electrical Specifications section for maximum clock frequencies for 5V and 3.3V operation.

CRT Codes:

A PS/2 fixed frequency analog CRT monitor or equivalent (31.5 / 35.5 KHz Horizontal Frequency Specification)

B Multi-Frequency CRT monitor (37.5 KHz Minimum Horizontal Frequency Specification) (NEC MultiSync 3D or equivalent)

C Multi-Frequency High-Performance CRT Monitor (48.5 KHz Min H Freq Specification) (Nanao Flexscan 9070s, MultiSync 5D, or equivalent)

Simultaneous Flat Panel / CRT Display

The 65535 provides simultaneous display operation with Multi-Sync variable frequency or PS/2 fixed frequency CRT monitors and single panel-single drive LCDs (LCD-SS), dual panel-dual drive LCDs (LCD-DD), and plasma and EL panels (which employ single panel-single drive interfaces). Single drive panels sequence data in the same manner as CRTs, so the 65535 provides simultaneous CRT display with LCD-SS, Plasma, and EL panels by driving the panels with CRT timing. LCD-DD panels require video data alternating between two separate locations in memory. In addition, a dual drive panel requires data from both locations simultaneously. The 65535 provides simultaneous display with monchrome LCD-DD panels with a single 256Kx16 DRAM.

DISPLAY ENHANCEMENT FEATURES

Display quality is one of the most important features for the success of any flat panel-based system. The 65535 provides many features to enhance the flat panel display quality.

"TRUE-GRAY" Gray Scale Algorithm

A proprietary polynomial-based Frame Rate Control (FRC) and dithering algorithm in the 65535's hardware generates a maximum of 61 gray levels on monochrome panels. The FRC technique simulates a maximum of 16 gray levels on monochrome panels by turning the pixels on and off over several frames in time. The dithering technique increases the number of gray scales from 16 to 61 by altering the pattern of gray scales in adjacent pixels. The persistence (response time) of the pixels varies among panel manufacturers and models. By re-programming the polynomial (an 8-bit value in Extension Register XR6E) while viewing the display, the FRC algorithm can be adjusted to match the persistence of the particular panel without increasing the panel's vertical refresh rate. With this technique, the 65535 produces up to 61 flicker-free gray scales on the latest fast response "mouse quick" film compensated monochrome STN-DD LCDs. The alternate method of reducing flicker -- increasing the panel's vertical refresh rate -- has several drawbacks. As the vertical refresh rate increases, the panel's power consumption increases, ghosting (cross-talk) increases, and contrast decreases. CHIPS' polynomial FRC gray scale algorithm reduces flicker without increasing the vertical refresh rate.

RGB Color To Gray Scale Reduction

The 24 bits of color palette data from the VGA standard color lookup table (CLUT) are reduced to 6 bits for 64 gray scales via one of three selectable RGB color to gray scale reduction techniques:

1) NTSC Weighting: 5/16 Red 9/16 Green 2/16 Blue
2) Equal Weighting: 5/16 Red 6/16 Green 5/16 Blue
3) Green Only: 6 bits of Green only

NTSC is the most common weighting, which is used in television broadcasting. Equal weighting increases the weighting for Blue, which is useful for Applications such as Microsoft Windows 3.1 which often uses Blue for background colors. Green Only is useful for replicating on a flat panel the display of software optimized for IBM's monochrome monitors which use the six Green bits of palette data.

SmartMap™

SmartMap™ is a proprietary feature that can be invoked to intelligently map colors to gray levels in text mode. SmartMap™ improves the legibility of flat panel displays by solving a common problem:

Most application programs are optimized for color CRT monitors using multiple colors. For example, a word processor might use a blue background with white characters for normal text, underlined text could be displayed in green, italicized text in yellow, and so on. This variety of colors, which is quite distinct on a color CRT monitor, can be illegible on a monochrome flat panel display if the colors are mapped to adjacent gray scale values. In the example, underlined and italicized text would be illegible if yellow is mapped to gray scale 4, green to gray scale 6 with the blue background mapped to gray scale 5.

SmartMap™ compares and adjusts foreground and background gray scale values to produce adequate display contrast on flat panel displays. The minimum contrast value and the foreground / background gray scale adjustment values are programmed in the 65535's Extension Registers. This feature can be disabled if desired.

Text Enhancement

Text Enhancement is another feature of the 65535 that improves image quality on flat panel displays. When turned "on," the Text Enhancement feature displays Dim White as Bright White, thereby optimizing the contrast level on flat panels. Text Enhancement can be turned "on" and "off" by changing a bit in one of the Extension Registers.

Vertical & Horizontal Compensation

Vertical & Horizontal Compensation are programmable features that adjust the display to completely fill the flat panel display. Vertical Compensation increases the useable display area when running lower resolution software on a higher resolution panel. Unlike CRT monitors, flat panels have a fixed number of scan lines (e.g., 200, 400, 480 or 768 lines). Lower resolution software run on a higher resolution panel only partially fills the useable display area. For instance, 350-line EGA software displayed on a 480-line panel would leave 130 blank lines at the bottom of the display and 400-line VGA text or Mode 13 images would leave 80 blank lines at the bottom. The 65535 offers the following Vertical Compensation techniques to increase the useable screen area:

Vertical Centering displays text or graphics images in the center of the flat panel, with a border of unused area at the top and bottom of the display. Automatic Vertical Centering automatically adjusts the Display Start address such that the unused area at the top of the display equals the unused area at the bottom. Non-Automatic Vertical Centering enables the Display Start address to be set (via programming the Extension Registers) such that text or graphics images can be positioned anywhere on the display.

Line replication (referred to as "stretching") duplicates every Nth display line (where N is programmable), thus stretching text characters and graphic images an adjustable amount. The display can be stretched to completely fill the flat panel area. Double scanning, a form of line replication where every line is replicated, is useful for running 200 line software on a 400 line panel or 480 line software on a 1024 line panel.

Blank line insertion, inserts N lines (where N is programmable) between each line of text characters. Thus text can be evenly spaced to fill the entire panel display area without altering the height and shape of the text characters. Blank line insertion can be used in text mode only.

The 65535 implements the Tall Font™ scheme so that there are very few blank lines on the flat panel in text modes. For example, using 8x19 font would fill 475 lines on a 480 line panel in VGA mode 3. If extension register XR28 bit-7=0, lines 1, 9, 12 of the 16 line font are replicated to generate 8x19 font. If extension register XR28 Bit-7=1, line 0 is replicated twice and line 15 is replicated once. The Tall Font™ scheme is implemented in hardware thereby avoiding any compatibility issues.

Each of these Vertical Compensation techniques can be controlled by programming the Extension Registers. Each Vertical Compensation feature can be individually disabled, enabled and adjusted. A combination of Vertical Compensation features can be used by adjusting the features' priority order. For example, text mode vertical compensation consists of four priority order options:

- Double Scanning+Line Insertion, Double Scanning, Line Insertion
- Double Scanning+Line Insertion, Line Insertion, Double Scanning
- Double Scanning+Tall Fonts, Double Scanning, Tall Fonts
- Double Scanning+Tall Fonts, Tall Fonts, Double Scanning

Text and graphics modes offer two Line Replication priority order options:

- Double Scanning+ Line Replication, Double Scanning, Line Replication
- Double Scanning+ Line Replication, Line Replication, Double Scanning

Horizontal Compensation techniques include Horizontal Compression, Horizontal Centering, and Horizontal Doubling. Horizontal Compression will compress 9-dot text to 8-dots such that 720-dot text in Hercules modes will fit on a 640-dot panel. Automatic Horizontal Centering automatically centers the display on a larger resolution panel such that the unused area at the left of the display equals the unused area at the right. Non-Automatic Horizontal Centering enables the left border to be set (via programming the Horizontal Centering Extension Register) such that the image can be positioned anywhere on the display. Automatic Horizontal Doubling will automatically double the display in the horizontal direction when the horizontal display width is equal to or less than half of the horizontal panel size.

ADVANCED POWER MANAGEMENT

Normal Operating Mode

The 65535 is a full-custom, sub-micron CMOS integrated circuit optimized for low power consumption during normal operation. The 65535 provides CAS-before-RAS refresh cycles for the DRAM display memory. The 65535 provides "mixed" 3.3V and 5.0V operation by providing dedicated VCC pins for the 65535's internal logic, bus interface, memory interface, and display interface. If the 65535 internal logic operates at 3.3V then the memory interface, bus interface, and panel interface can independently operate at either 3.3V or 5.0V. Clock VCC must be the same as the VCC of the internal logic. The 65535 provides direct interface to 386DX/SX and 486DX/SX local bus which conserves power when 3.3V microprocessors are used. A flexible clock synthesizer is used to generate independent memory and video clocks. The 65535's performance-enhancement features minimize the memory clock frequency (and thus power consumption) required to achieve a given performance level. The 65535's proprietary gray scaling algorithm produces a flicker-free display with a minimum video clock and panel vertical refresh rate. (Note: the power consumption of the controller increases linearly with video clock frequency).

Mixed 3.3V and 5.0V Operation

The 65535 supports operation at either 5.0V ±10% or 3.3V ±0.3V. The 65535 also provides "mixed" 5V / 3.3V operation by providing dedicated Vcc pins for the 65535's internal logic, bus interface, memory interface, and display interface. Each dedicated Vcc can be either 5V or 3.3V, such that the 65535 internal logic operates at 3.3V and the various interfaces at either 3.3V or 5V. Clock Vcc must be the same as the Vcc of the internal logic. The following table shows the relationship between the Vcc inputs and the interface pins controlled by each VCC input. In "mixed" voltage mode, the reference VCC input on pin 132 must be 5V (can only be 3.3V if all other VCC inputs are 3.3V).

Vcc Pins	Interface	Pins Affected
62, 139	Internal Logic	–
118	Memory	100-131
19, 29	Bus	1-40, 133-153, 159
52	Display	47-76
132	Reference	–
86	Extra	78-99
157, 158	Clock †	155, 156
45	DAC	41,44,46

† Must be the same as the Vcc of the internal logic.

When switching from 5V to 3.3V (or vice versa), the clock frequency must be maintained. If switching voltage requires a clock change, the clock must be switched to a lower frequency before switching to a lower voltage. The maximum clock frequency rating for 3.3V operation is 56 MHz.

Power Sequencing During Mixed Voltage Operation

During a power up sequence, the internal logic and internal clock VCCs must be turned on before or at the same time as the rest of the VCCs. During a power down sequence, IVCC and CVCC must be the last VCCs to be turned off. The VCC inputs for the internal DAC, CPU bus and Display bus may be turned off while the VCC inputs to the internal logic remain turned on. In this mode of operation, the internal DAC, CPU bus, and display bus VCC pins are floating.

Panel Off Mode

In 'Panel Off' mode, the 65535 turns off the flat panel interface logic. The VGA sub-system remains active, such that the CPU can read/write display memory and I/O registers. The 65535's video clock can be reduced significantly, saving power. Panel Off mode is activated via software (by programming Extended Register XR52 bit-3=1).

Standby Mode

In 'Standby' mode, the 65535 suspends all CPU, memory and display activities. The 65535 places the DRAM in either slow refresh or self-refresh mode of operation, and the 65535's clock can be shut off. The VGA sub-system dissipates a minimum amount of power during Standby. Since the 65535 is a fully static device, the contents of the controller's registers and on-chip palette are maintained during Standby. Therefore, Standby mode provides fast Suspend / Resume modes. Standby mode may be activated by forcing the STNDBY# pin low or via software (by programming XR52 bit-4 = '1'). The state of all 65535 pins during Standby mode is summarized in tables in the pin description section.

CRT Power Management / DPMS

The 65535 supports the VESA DPMS (Display Power Management Signaling) protocol. This includes the ability to independently stop HSYNC and/or VSYNC and hold them at a static level to signal the CRT to enter various power-saving states. Additionally, the RAMDAC may be powered down and the clock frequencies lowered for further power savings.

CPU ACTIVITY INDICATOR / TIMER

The 65535 provides an output pin called ACTI (pin 75) to facilitate an orderly power down sequence. The ACTI output is an active high signal which is driven high every time a valid VGA memory read/write operation or VGA I/O read/write operation is executed by the CPU. This signal may be used by power management circuitry to put the 65535 in Panel Off or Standby power down modes. The 65535 may also evoke its own low power operation by using the activity timer which monitors the ACTI signal. The activity timer will either disable the backlight or evoke Panel Off mode after a specified time interval. This time interval is programmed in 30 second intervals via Extension Register XR5C.

FULL COMPATIBILITY

The 65535 is fully compatible with the IBM™ VGA standard at the hardware, register, and BIOS level. The 65535 also provides enhanced backward compatibility to EGA™, CGA™, Hercules™, and MDA™ standards without using NMIs. These controllers include a variety of features to provide compatibility on flat panel displays in addition to CRT monitors. Internal compensation techniques ensure that industry-standard software designed for different displays can be executed on the single flat panel used in an implementation. Mode initialization is supported at the BIOS and register levels, ensuring compatibility with all application software.

Write Protection

The 65535 has the ability to write protect most of the standard VGA registers. This feature is used to provide backwards compatibility with software written for older generation display types. The write protection is grouped into register sets and controlled by the Write Protect Register (XR15).

Extension Registers

The 65535 employs an "Extension" Register set to control its enhanced features. These Extension Registers provide control of the flat panel interface, flat panel timing, vertical compensation, SMARTMAP™, and Backwards Compatibility. These registers are always accessible as an index/data register set at port addresses 3D6-3D7h. None of the unused bits in the regular VGA registers are used for extensions.

Panel Interface Registers

The Flat Panel Interface characteristics are controlled by a subset of the Extension Registers. These Registers select the panel type, data formatting, panel configuration, panel size, clock selection and video polarity. Since the 65535 is designed to support a wide range of panel types and sizes, the control of these features is fully programmable. The video polarity of text and graphics modes is independently selectable to allow black text on a white background and still provide normal graphics images.

Alternate Panel Timing Registers

Flat panel displays usually require sync signal timing that is different from a CRT. To provide full compatibility with the IBM VGA standard, alternate timing registers are used to allow independent timing of the sync signals for flat panel displays. Unlike the values programmed into the standard CRT timing registers, the value programmed into the alternate timing registers is dependent on the panel type used and is independent of the display mode.

Context Switching

For support of multi-tasking, windowing, and context switching, the entire state of the 65535 (internal registers) is readable and writable. This feature is fully compatible with IBM's VGA. Additional registers are provided to allow read back of internal latches not readable in the IBM VGA.

RESET, SETUP, AND TEST MODES

Reset Mode

When this mode is activated by pulling the RESET pin high, the 65535 is forced to VGA-compatible mode and the CRT is selected as the active display. In addition, the 65535 is disabled; it must be enabled after deactivating the RESET pin by writing to the Global Enable Register (102h in Setup Mode for ISA bus configurations or to port 3C3h in Local Bus configurations). Access to all Extension Registers is always enabled after reset (at 3D6/3D7h). The RESET pin must be active for at least 64 clock cycles.

Setup Mode

In this mode, only the Global Enable register is accessible. In ISA bus configurations, setup mode is entered by writing a 1 to bit-4 of port 46E8h. This port is incorporated in the 65535. While in Setup mode, the video output is active if it was active prior to entering Setup mode and inactive if it was inactive prior to entering Setup mode. After power up, video BIOS can optionally disable the video 46E8 or 3C3 registers (via XR70) for compatibility in case other non-IBM-compatible peripheral devices use those ports.

Tri-State Mode

In this mode, all output pins of the 65535 chip may be disabled for testing of circuitry external to the chip. The 65535 will enter Tri-State mode if it sees a rising edge on XTALI during RESET with one of the display memory data pins pulled low (MAD0 pin 114). The 65535 will exit Tri-State mode with the enabling memory data pin (MAD0) high or RESET low.

ICT (In-Circuit Test) Mode

In this mode, all pins of the 65535 chip may be tested individually to determine if they are properly connected. The 65535 will enter ICT mode if it sees a rising edge on XTALI during RESET with one of the display memory data pins pulled low (a different pin from the one used to enable Tri-state mode: MAD1). In ICT mode, all digital signal pins become inputs which are part of a long path starting at ENAVDD (pin 48) and proceeding to lower pin numbers around the chip to pin 1 then to pin 160 and ending at VSYNC (pin 50). If all pins in the path are high, the VSYNC output will be high. If any pin is low, the VSYNC output will be low. Thus the chip can be checked in circuit to determine if all pins are connected properly by toggling all pins one at a time (XTALI last) and observing the effect on VSYNC. XTALI must be toggled last because rising edges on XTALI with either of the enabling memory data pins high or RESET low will exit ICT mode. As a side effect, ICT mode effectively Tri-States all pins except VSYNC.

Mode of Operation	RESET Pin	STNDBY# Pin	Display Memory Access	Video Output
Reset	High	xxx	-----	-----
Setup	-----	-----	No	Yes
Test	-----	-----	No	Yes
Standby	Low	Low	No	No
Panel Off	Low	High	Yes	No

Note: Combinations of pin levels not shown above are illegal and should not be used.

Reset / Setup / Test / Standby / Panel Off Mode Summary

CHIP ARCHITECTURE

The 65535 integrates six major internal modules:

Sequencer

The Sequencer generates all CPU and display memory timing. It controls CPU access of display memory by inserting cycles dedicated to CPU access. It also contains mask registers which can prevent writes to individual display memory planes.

CRT Controller

The CRT Controller generates all the sync and timing signals for the display and also generates the multiplexed row and column addresses used for both display refresh and CPU access of display memory.

Graphics Controller

The Graphics Controller interfaces the 8, 16, or 32-bit CPU data bus to the 32-bit internal data bus used by the four planes (Maps) of display memory. It also latches and supplies display memory data to the Attribute Controller for use in refreshing the screen image. For text modes this data is supplied in parallel form (character generator data and attribute code); for graphics modes it is converted to serial form (one bit from each of four bytes form a single pixel). The Graphics Controller can also perform any one of several types of logical operations on data while reading it from or writing it to display memory or the CPU data bus.

Attribute Controller

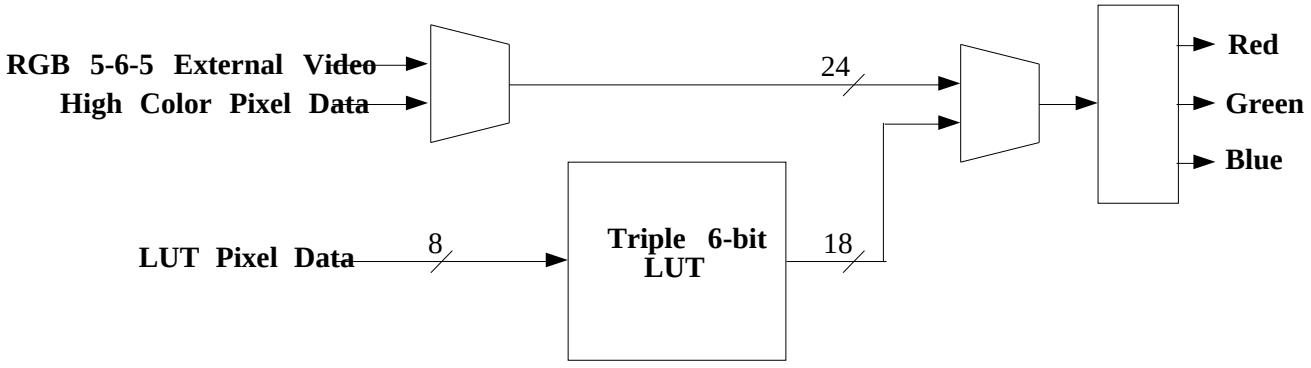
The Attribute Controller generates the 4-bit-wide video data stream used to refresh the display. This is created in text modes from a font pattern and an attribute code which pass through a parallel to serial conversion. In graphics modes, the display memory contains the 4-bit pixel data. In text and 16 color graphic modes the 4-bit pixel data acts as an index into a set of 16 internal color look-up registers which generate a 6-bit color value. Two additional bits of color data are added to provide an 8-bit address to the VGA color palette. In 256-color modes, two 4-bit values may be passed through the color look-up registers and assembled into one 8-bit video data value. In high-resolution 256-color modes, an 8-bit video data value may be provided directly, bypassing the attribute controller color lookup registers. Text and cursor blink, underline and horizontal scrolling are also the responsibility of the Attribute Controller.

VGA / Color Palette DAC

The 65535 integrates a VGA compatible triple 6-bit Color Lookup Table (sometimes referred to as a "CLUT" or just "LUT") and high speed 6/8-bit DACs. Additionally true color bypass modes are supported displaying color depths of up to 24bpp (8-red, 8-green, 8-blue). The palette DAC can switch between true color data and LUT data on a pixel by pixel basis. Thus, video overlays may be any arbitrary shape and can lie on any pixel boundary. The hardware cursor is also a true color bitmap which may overlay on any pixel boundary.

The internal palette DAC register I/O addresses and functionality are 100% compatible with the VGA standard. In all bus interfaces the palette DAC automatically controls accesses to its registers to avoid data overrun. This is handled by holding RDY in the ISA configuration and by delaying RDY# for VL-Bus and local bus interfaces.

Extended RAMDAC display modes are selected in the Palette Control Register (XR06). Two 16bpp formats are supported: 5-red, 5-green, 5-blue Targa format and 5-red, 6-green, 5-blue XGA format. The internal Palette / DAC may also be disabled via the Palette Control Register (XR06).



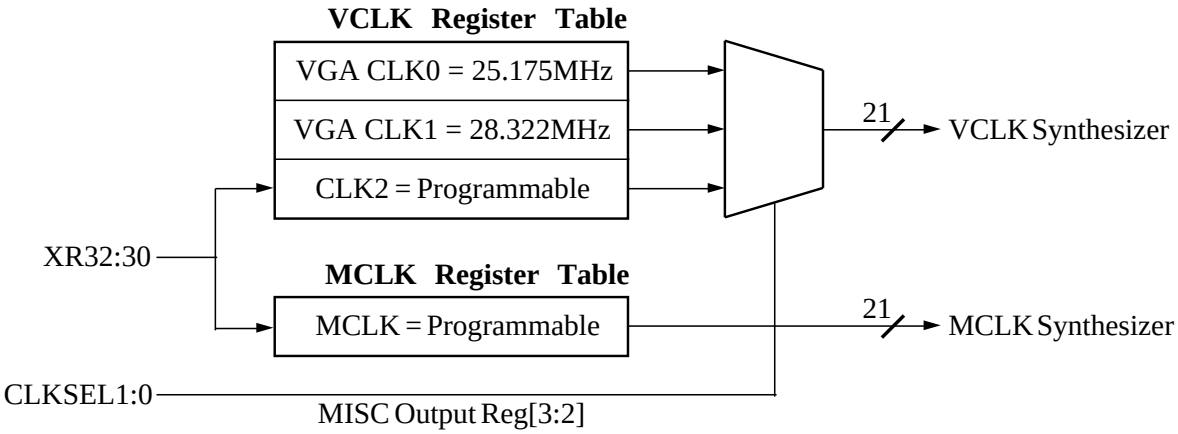
Color Palette / DAC Internal Block Diagram

Clock Synthesizer

An integrated dual clock synthesizer supports all pixel clock (VCLK) and memory clock (MCLK) frequencies which may be required by the 65535. A block diagram of the dual clock synthesizer section is shown in the figure below. Each clock synthesizer may be programmed to output frequencies ranging between 1MHz and the maximum specified operating frequency for that clock (refer to "Electrical Specifications" for 3.3V and 5V operation) in increments not exceeding 0.5%. The frequencies are generated by an 18-bit divisor word. This value contains divisor fields for the Phase Lock Loop (PLL), Voltage Controlled Oscillator (VCO) and Pre/Post Divide Control blocks. The divisor word for both synthesizers is programmable via the Clock Control Extension Registers (XR30:32).

VCLK always has three registers from which to select its frequency. This duplication is required for VGA compatibility. CLK0 and CLK1 are fixed at the VGA compatible frequencies 25.175MHz and 28.322MHz respectively. These values can not be changed unlike CLK2 which is fully programmable. The active VCLK register set is selected by the clock select bits in the VGA "Miscellaneous Output Register".

A more detailed description of the operation and programming of the clock synthesizer block is given in the Functional Description section of this document.



Clock Synthesizer Block Diagram

CONFIGURATION INPUTS

The 65535 can read up to twelve configuration bits. These signals are sampled on the memory address bus AA0-AA8 (CFG0-8) and on pins 38-40 (BCFG2-0) on the falling edge of RESET. The 65535 implements pull-up resistors on-chip on all configuration input pins.

65535 Pin #	Signal	Active	Functionality
100	LB#	Low	Bus Configuration
101	ISA#	Low	Bus Configuration
102	2X#	Low	2x CPU Clock Select
103	RC#	Low	ROMCS# is output
104	EC#	Low	Ext Clk Src Select
105	OS#	Low	External Osc Select
106	undefined	Low	Reserved
107	TS#	Low	Test Mode Disable
108	LV#	Low	Low Voltage Select

In the default configuration, the 65535 is set for Auto Select for the bus interface. However, if the user wishes to force a certain option, then a 4.7k ohm resistor may be used to pull-down the desired configuration pin:

ISA# (AA1) Pin 101	LB# (AA0) Pin 100	Functionality
Low	Low	Reserved
Low	High	ISA Bus
High	Low	Reserved
High	High	Autoselect

For autoselection, the state of the pins 38-40 during RESET determine the local bus type as follows:

BCFG2 Pin 40	BCFG1 Pin 39	BCFG0 Pin 38	Bus Functionality
Low	don't care	don't care	Reserved
High	Low	Low	386-32 bit
High	Low	High	386-16 bit
High	High	Low	486-32 bit
High	High	High	486-16 bit

AA2 determines the CPU clock rate for purposes of local bus implementation (0=2x CPU clock, 1=1x CPU clock). AA3, when forced low during RESET, enables ROMCS# (a decode for the C0000 address range) to be output on ZWS# (pin 38). AA4 determines whether the internal VCO is enabled or not (0=disabled, 1=enabled).

AA5, if forced to 0, indicates that a reference frequency of 14.414 MHz is forced on pin 155. AA6 and AA7 are reserved. AA8, when forced low, selects 3.3V level of operation for the internal logic and the clock core.

VIRTUAL SWITCH REGISTER

The 65535 implements a 'virtual switch register'. In 'EGA' mode, the sense bit of the Feature control register (3C2 bit 4) may be set up to read a selected bit from the 'virtual switch register' (an extension register set up by BIOS at initialization time) instead of reading the state of the SENSE pin (or internal comparator output). This reduces overall video subsystem chip count by eliminating the external multiplexers otherwise required on the sense pin to implement TTL monitor support.

LIGHT PEN REGISTERS

In the CGA and Hercules modes, the contents of the Display Address counter are saved at the end of the frame before being reset. The saved value can be read in the CRT Controller Register space at indices 10h and 11h. This allows simulation of a light pen hit in CGA and Hercules modes.

BIOS ROM INTERFACE

In typical ISA bus applications, the 65535 is placed on the motherboard and the video BIOS is integrated with the system BIOS (in Local Bus systems, the video BIOS is always included in the system BIOS). A separate signal (ROMCS#) can be generated on the ZWS# pin for ISA bus or may be created external to the 65535 for implementing a separate external ROM BIOS.

Typically, an 8-bit BIOS is implemented with one external ROM chip. A 16-bit dedicated video BIOS ROM could be implemented with the 65535 if required using two BIOS ROM chips, an external PAL, and a 74LS244 buffer. However, a higher-performance and lower-cost video system will result from implementation of the video BIOS as either an 8-bit dedicated video BIOS ROM or as part of the system BIOS and having the video BIOS be copied into system RAM by the system BIOS on startup.

Chips and Technologies, Inc. supplies a video BIOS that is optimized for the 65535 hardware. The BIOS supports the extended functions of the 65535, such as switching between the flat panel and the CRT, SMARTMAP™, Vertical Compensation, and palette load/save. The BIOS Modification Program (BMP) enables OEMs to tailor their feature set by programming the extended functions. CHIPS offers the BIOS as a standard production version, a customized version, or as source code.

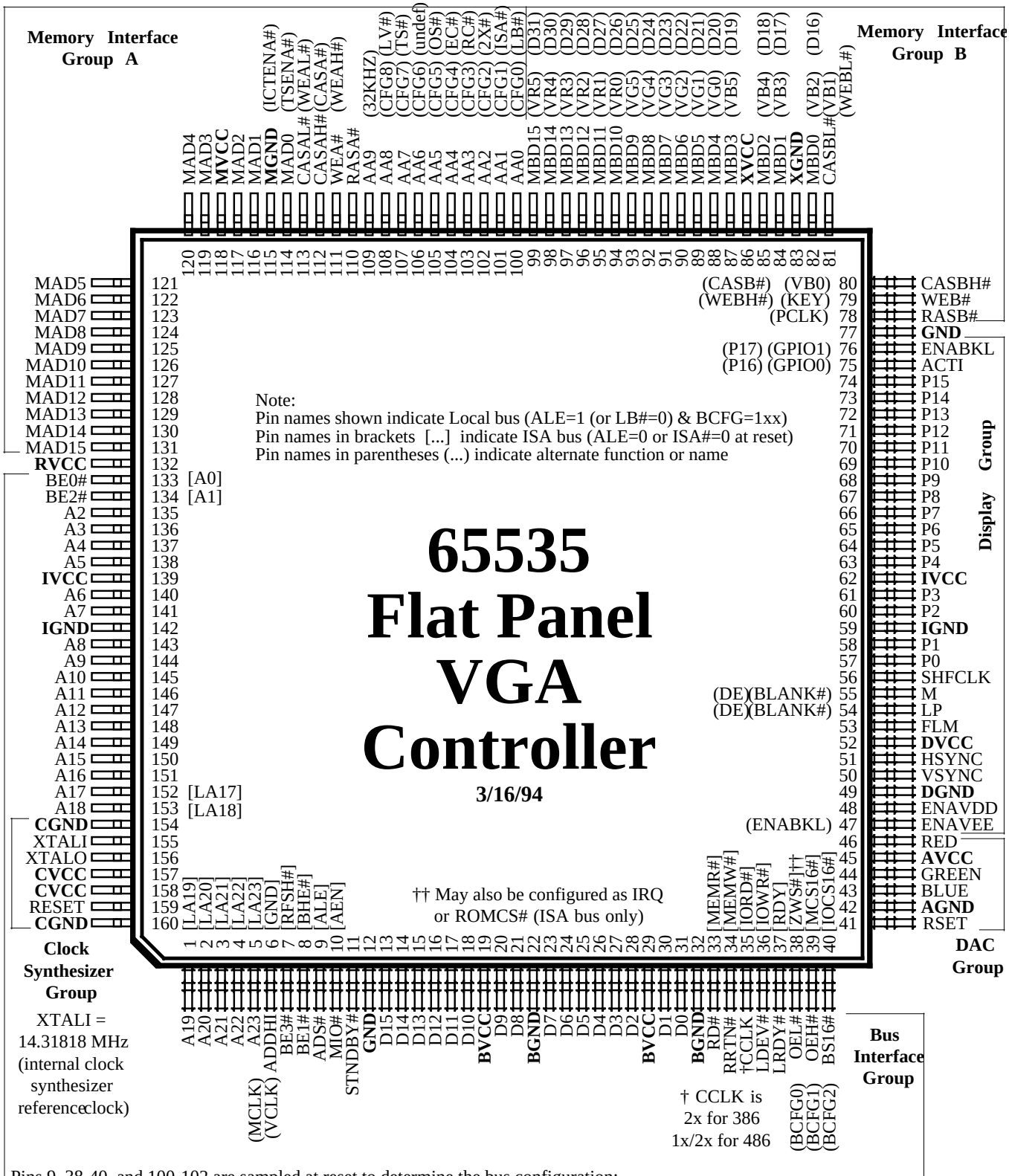
PACKAGE

The 65535 is available in a EIAJ-standard 160-pin plastic flat pack with a 28 x 28 mm body size and 0.65 mm (25.6 mil) lead pitch.

APPLICATION SCHEMATIC EXAMPLES

Eventually, this document will include application schematic examples of the following:

1. Bus Interface - 16-bit EISA/ISA Bus
   Bus Interface - 16-bit Micro Channel Bus
   Bus Interface - 16-bit x86 SL PI Bus
   Bus Interface - 16-bit 386SX/486SLC Local Bus
   Bus Interface - 16-bit 486 Local Bus
   Bus Interface - 32-bit 486 Local Bus
2. Memory Interface - 256Kx16 DRAMs (2C)
   Memory Interface - 256Kx16 DRAMs (2W)
   Memory Interface - 256Kx4 DRAMs
3. CRT / Panel Interface
   PC-Video Interface



Pins 9, 38-40, and 100-102 are sampled at reset to determine the bus configuration:

CFG1	CFG0	Bus Configuration	Local Bus Options				BCFG2	BCFG1	BCFG0		
			BCFG:	2	1	0	Pin 34 (1x)	Pin 34 (2x)	Pin 40	Pin 39	Pin 38	Pin 133	Pin 8
L	L	Reserved	386-32:	1	0	0	n/a	CPURST	BS16#	GND	GND	BE0#	BE1#
L	H	Force ISA	386-16:	1	0	1	n/a	CPURST	BVCC	GND	BVCC	BLE#	BHE#
H	L	Force LB	486-32:	1	1	0	RDYRTN#	CPURST	BS16#	BVCC	GND	BE0#	BE1#
H	H	Sample pin-9 to autoselect ISA/LB	486-16:	1	1	1	GND	CPURST	BS16#	OEH#	OEL#	BE0#	BE1#

Pin Name			Pin #	Dir	Drive
A2			135	In	—
A3			136	In	—
A4			137	In	—
A5			138	In	—
A6			140	In	—
A7			141	In	—
A8			143	In	—
A9			144	In	—
A10			145	In	—
A11			146	In	—
A12			147	In	—
A13			148	In	—
A14			149	In	—
A15			150	In	—
A16			151	In	—
A17	[LA17]		152	In	—
A18	[LA18]		153	In	—
A19	[LA19]		1	In	—
A20	[LA20]		2	In	—
A21	[LA21]		3	In	—
A22	[LA22]		4	In	—
A23	[LA23]		5	In	—
AA0	(CFG0)	(LB#)	100	I/O	4mA
AA1	(CFG1)	(ISA#)	101	I/O	4mA
AA2	(CFG2)	(2X#)	102	I/O	4mA
AA3	(CFG3)	(RC#)	103	I/O	4mA
AA4	(CFG4)	(EC#)	104	I/O	4mA
AA5	(CFG5)	(OS#)	105	I/O	4mA
AA6	(CFG6)	(reserved)	106	I/O	4mA
AA7	(CFG7)	(TS#)	107	I/O	4mA
AA8	(CFG8)	(LV#)	108	I/O	4mA
AA9	(32KHZ)		109	I/O	4mA
ADDHI			6	In	—
AGND			42	—	—
ADS#	[ALE]		9	In	—
AVCC			45	—	—
BE0#	[A0]		133	In	—
BE1#	[BHE#]		8	In	—
BE2#	[A1]		134	In	—
BE3#	[RFSH#]		7	In	—
BLUE			43	Out	—
BGND	(Bus)		22	—	—
BGND	(Bus)		32	—	—
BVCC	(Bus)		19	—	—
BVCC	(Bus)		29	—	—
BS16#	(BCFG2)	[IOCS16#]	40	Out	12mA
CASAH#	(CASA#)		112	Out	4mA
CASAL#	(WEAL#)		113	Out	4mA
CASBH#	(CASB#)	(VB0)	80	I/O	4mA
CASBL#	(WEBL#)	(VB1)	81	I/O	4mA
CGND	(Clock)		154	—	—
CGND	(Clock)		160	—	—
CVCC	(Clock)		157	—	—
CVCC	(Clock)		158	—	—

Pin Name			Pin #	Dir	Drive
D0			31	I/O	4mA
D1			30	I/O	4mA
D2			28	I/O	4mA
D3			27	I/O	4mA
D4			26	I/O	4mA
D5			25	I/O	4mA
D6			24	I/O	4mA
D7			23	I/O	4mA
D8			21	I/O	4mA
D9			20	I/O	4mA
D10			18	I/O	4mA
D11			17	I/O	4mA
D12			16	I/O	4mA
D13			15	I/O	4mA
D14			14	I/O	4mA
D15			13	I/O	4mA
DGND	(Display)		49	—	—
DVCC	(Display)		52	—	—
ENAVDD			48	Out	8mA
ENAVEE	(ENABKL)		47	Out	8mA
FLM			53	Out	8mA
GND			12	—	—
GND			77	—	—
GREEN			44	Out	—
HSYNC			51	Out	12mA
IGND	(Internal	Logic)	59	—	—
IGND	(Internal	Logic)	142	—	—
IVCC	(Internal	Logic)	62	—	—
IVCC	(Internal	Logic)	139	—	—
LCLK	[IORD#]		35	In	—
LDEV#	[IOWR#]		36	I/O	12mA
LRDY#	[RDY]		37	Out	12mA
LP	(BLANK#)	(DE)	54	Out	8mA
M	(BLANK#)	(DE)	55	Out	8mA
MAD0	(TSENA#)		114	I/O	2mA
MAD1	(ICTENA#)		116	I/O	2mA
MAD2			117	I/O	2mA
MAD3			119	I/O	2mA
MAD4			120	I/O	2mA
MAD5			121	I/O	2mA
MAD6			122	I/O	2mA
MAD7			123	I/O	2mA
MAD8			124	I/O	2mA
MAD9			125	I/O	2mA
MAD10			126	I/O	2mA
MAD11			127	I/O	2mA
MAD12			128	I/O	2mA
MAD13			129	I/O	2mA
MAD14			130	I/O	2mA
MAD15			131	I/O	2mA

Pin Name			Pin #	Dir	Drive
MBD0	(VB2)	(D16)	82	I/O	4mA
MBD1	(VB3)	(D17)	84	I/O	4mA
MBD2	(VB4)	(D18)	85	I/O	4mA
MBD3	(VB5)	(D19)	87	I/O	4mA
MBD4	(VG0)	(D20)	88	I/O	4mA
MBD5	(VG1)	(D21)	89	I/O	4mA
MBD6	(VG2)	(D22)	90	I/O	4mA
MBD7	(VG3)	(D23)	91	I/O	4mA
MBD8	(VG4)	(D24)	92	I/O	4mA
MBD9	(VG5)	(D25)	93	I/O	4mA
MBD10	(VR0)	(D26)	94	I/O	4mA
MBD11	(VR1)	(D27)	95	I/O	4mA
MBD12	(VR2)	(D28)	96	I/O	4mA
MBD13	(VR3)	(D29)	97	I/O	4mA
MBD14	(VR4)	(D30)	98	I/O	4mA
MBD15	(VR5)	(D31)	99	I/O	4mA
MGND	(Memory)		115	—	—
MIO#	[AEN]		10	In	—
MVCC	(Memory)		118	—	—
OEH#	(BCFG1)	[MCS16#]	39	Out	12mA
OEL#	(BCFG0)	[ZWS#]	38	Out	12mA
P0			57	Out	8mA
P1			58	Out	8mA
P2			60	Out	8mA
P3			61	Out	8mA
P4			63	Out	8mA
P5			64	Out	8mA
P6			65	Out	8mA
P7			66	Out	8mA
P8	(SHFCLKU)		67	Out	8mA
P9			68	Out	8mA
P10			69	Out	8mA
P11			70	Out	8mA
P12			71	Out	8mA
P13			72	Out	8mA
P14			73	Out	8mA
P15			74	Out	8mA
P16	(ACTI)	(GPIO0)	75	I/O	8mA
P17	(ENABKL)	(GPIO1)	76	I/O	8mA
RASA#			110	Out	4mA
RASB#	(PCLK)		78	Out	4mA
RD#	[MEMR#]		33	In	—
RED			46	Out	—
RESET			159	In	—
RRTN#	[MEMW#]		34	In	—
RSET			41	In	—
RVCC	(Reference)		132	—	—
SHFCLK	(CL2)	(SHFCLKL)	56	Out	8mA
STNDBY#			11	In	—
VSYNC			50	Out	12mA
WEA#	(WEAH#)		111	Out	4mA
WEB#	(WEBH#)	(KEY)	79	Out	4mA
XGND			83	—	—
XTALI			155	In	—
XTALO			156	Out	—
XVCC			86	—	—

PIN DESCRIPTIONS

System Bus Interface

Pin #	Pin Name			Type	Active	Description
31	D0			I/O	High	System Data Bus
30	D1			I/O	High	
28	D2			I/O	High	
27	D3			I/O	High	
26	D4			I/O	High	
25	D5			I/O	High	
24	D6			I/O	High	
23	D7			I/O	High	
21	D8			I/O	High	
20	D9			I/O	High	
18	D10			I/O	High	
17	D11			I/O	High	
16	D12			I/O	High	
15	D13			I/O	High	
14	D14			I/O	High	
13	D15			I/O	High	
133	BE0#	[A0]		In	Low	System Data Bus Byte Enables. For EISA/ISA bus, pin 7 is an active low input indicating a Refresh cycle (when low, display memory is not accessible).
8	BE1#	[BHE#]		In	Low	
134	BE2#	[A1]		In	Low	
7	BE3#	[RFSH#]			In	Low
135	A2			In	High	System Address Bus
136	A3			In	High	
137	A4			In	High	
138	A5			In	High	
140	A6			In	High	
141	A7			In	High	
143	A8			In	High	
144	A9			In	High	
145	A10			In	High	
146	A11			In	High	
147	A12			In	High	
148	A13			In	High	
149	A14			In	High	
150	A15			In	High	On the EISA/ISA bus A17-23 may be latched addresses LA17-23.
151	A16			In	High	
152	A17	[LA17]		In	High	
153	A18	[LA18]		In	High	ADDHI may be used to connect to LA24 or a decode of addresses higher than A23. See description of XR08.
1	A19	[LA19]		In	High	
2	A20	[LA20]		In	High	
3	A21	[LA21]		In	High	In external clock mode, ADDHI is used to input VCLK (XTALI is used to input MCLK); In clock test mode, ADDHI is used to output VCLK and A23 is used to output MCLK. See XR01 for more details.
4	A22	[LA22]		In	High	
5	A23	[LA23]	(MCLK)	I/O	High	
6	ADDHI		(VCLK)	I/O	High	

Note: Pin names indicate local bus configuration
Pin names in brackets [...] indicate ISA bus

PIN DESCRIPTIONS **System Bus Interface (continued)**

Pin #	Pin Name		Type	Active	Description
159	RESET		In	High	Reset. Connect directly to bus reset.
9	ADS#		In	Low	This pin is Address Strobe for local bus and Address Latch Enable for EISA/ISA Bus. It indicates the start of a bus cycle.
		[ALE]	In	High	
10	MIO#		In	Both	For local bus operation, this pin indicates memory or I/O cycle: 1 = memory, 0 = I/O. In EISA/ISA interfaces, it indicates a valid I/O address: 0 = valid I/O address, 1 = Invalid I/O address (latched internally).
		[AEN]	In	High	
33	RD#	[MEMR#]	In	Low	For local bus operation, this pin indicates a read (low) or write (high) bus cycle. In EISA/ISA bus, it indicates a Memory Read cycle.
34	RDYRTN#	[MEMW#]	In	Low	The expected input signal on this pin is determined by the Bus Configuration (BCFG) inputs:
or	CPURST		In	High	
or	GND		In	n/a	

BCFG 2	BCFG 1	BCFG 0	CFG 2	Selected Bus	Function of This Pin	Comment
0	x	x	x	Reserved	Undefined	–
1	0	x	1	Reserved	Undefined	–
1	0	0	0	386-32	CPURST	2x clock
1	0	1	0	386-16	CPURST	2x clock
1	1	0	0	486-32	CPURST	2x clock
1	1	1	0	486-16	CPURST	2x clock
1	1	0	1	486-32	RDYRTN#	VL-Bus
1	1	1	1	486-16	GND	–

In 486 32-bit 1x-clock local bus interfaces, this pin complies with the VL-Bus RDYRTN# signal. For 486 16-bit operation, this signal should be connected to ground. For 2x-clock local bus operation for all CPU types and data widths, this pin provides an input for the CPU Reset (CPURST) signal which is used by the 65535 to synchronize the clock. In the EISA/ISA bus, this pin is an input that indicates a Memory Write cycle.

Note: Pin names indicate local bus configuration
Pin names in brackets [...] indicate ISA bus

PIN DESCRIPTIONS **System Bus Interface (continued)**

Pin #	Pin Name		Type	Active	Description
35	CCLK		In	High	In local bus interfaces, this pin connects to the 1x or 2x CPU clock (the '2X#' configuration bit should be set accordingly) or to LCLK on the VL-Bus (always a 1x clock). The local bus interface is synchronous to rising edges. For EISA/ISA bus, this pin indicates an I/O Read Cycle.
		[IORD#]	In	Low	
40	BS16#	[IOCS16#]	Out	Low	In local bus interfaces, this pin should be connected to BS16#. In the EISA/ISA bus interface, this pin serves as the indicator for 16-bit I/O capability.
37	LRDY#		Out	Low	Ready. Driven low during local bus cycles to indicate the current cycle should be completed Driven low during EISA/ISA bus cycles to indicate the current cycle should be extended with wait states. This signal is driven high at the end of the cycle, then Tri-Stated.
		[RDY]	Out	High	
36	LDEV#		Out	Low	For local bus, this pin is an output which indicates decode of local bus display memory addresses. This pin is the I/O Write input for EISA/ISA bus.
		[IOWR#]	In	Low	
39	OEH#	[MCS16#]	Out	Low	In local bus systems, this pin is used to enable the transceivers on D31-16 system data lines for 16-bit 486 local bus operation. In EISA/ISA bus configurations, this pin isMemory Select 16.
38	OEL#	[ZWS#]	Out	Low	In local bus systems, this pin is used to enable the transceivers on D15-0 system data lines for 16-bit 486 local bus operation. In EISA/ISA bus configurations, this pin has three definitions: ZWS# (zero wait state out), IRQ (interrupt out), or ROMCS# (Video BIOS ROM enable). For selection between the various EISA/ISA bus options, refer to XR01 bit-3 (configuration bit-3) and XR72 bit-0.
		[IRQ]	Out	High	
		[ROMCS#]	Out	Low	

Note: Pin names indicate local bus configuration
Pin names in brackets [...] indicate ISA bus

PIN DESCRIPTIONS **Display Memory Interface**

Pin #	Pin Name		Type	Active	Description
100	AA0 (LB#)	(CFG0)	I/O	High	DRAM address bus.
101	AA1 (ISA#)	(CFG1)	I/O	High	
102	AA2 (2X#)	(CFG2)	I/O	High	The state of AA0-AA8 are latched on the falling edge of
103	AA3 (RC#)	(CFG3)	I/O	High	RESET in XR01 bits 0-7 and XR6C bit-1 respectively
104	AA4 (EC#)	(CFG4)	I/O	High	to determine various configuration options (refer to the
105	AA5 (OS#)	(CFG5)	I/O	High	extended register descriptions for complete configu-
106	AA6 (reserved)	(CFG6)	I/O	High	ration details). Note that the 2X# configuration pin
107	AA7 (TS#)	(CFG7)	I/O	High	should only be used in 16-bit local bus configurations.
108	AA8 (LV#)	(CFG8)	I/O	High	
109	AA9	(32KHZ)	I/O	High	AA9, alternately, becomes the clock input for refresh of non-self-refresh DRAMs.
110	RASA#		Out	Low	Row address strobe for DRAM A
78	RASB#	(PCLK)	Out	Low	Row address strobe for DRAM B
113	CASAL#	(WEAL#)	Out	Low	Column address strobe for the DRAM A lower byte
112	CASAH#	(CASA#)	Out	Low	Column address strobe for the DRAM A upper byte
81	CASBL# (VB1)	(WEBL#)	Out	Low	Column address strobe for the DRAM B lower byte
80	CASBH# (VB0)	(CASB#)	Out	Low	Column address strobe for the DRAM B upper byte
111	WEA#	(WEAH#)	Out	Low	Write enable for DRAM A
79	WEB# (KEY)	(WEBH#)	Out	Low	Write enable for DRAM B

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS **Display Memory Interface (continued)**

Pin #	PinName			Type	Active	Description
114	MAD0	(TSENA#)		I/O	High	Data bus for DRAM A (lower 512K of display memory)
116	MAD1	(ICTENA#)		I/O	High	
117	MAD2			I/O	High	
119	MAD3			I/O	High	
120	MAD4			I/O	High	
121	MAD5			I/O	High	
122	MAD6			I/O	High	
123	MAD7			I/O	High	
124	MAD8			I/O	High	
125	MAD9			I/O	High	
126	MAD10			I/O	High	
127	MAD11			I/O	High	
128	MAD12			I/O	High	
129	MAD13			I/O	High	
130	MAD14			I/O	High	
131	MAD15			I/O	High	
82	MBD0	(VB2)	(D16)	I/O	High	Memory data bus for DRAM B (upper 512KB)
84	MBD1	(VB3)	(D17)	I/O	High	
85	MBD2	(VB4)	(D18)	I/O	High	When a second DRAM is not used, this bus is also used
87	MBD3	(VB5)	(D19)	I/O	High	to input 16 bits of RGB data from an external PC-Video
88	MBD4	(VG0)	(D20)	I/O	High	subsystem. Alternately, these lines may be used to
89	MBD5	(VG1)	(D21)	I/O	High	interface to the system data bus D31-D16.
90	MBD6	(VG2)	(D22)	I/O	High	
91	MBD7	(VG3)	(D23)	I/O	High	
92	MBD8	(VG4)	(D24)	I/O	High	
93	MBD9	(VG5)	(D25)	I/O	High	
94	MBD10	(VR0)	(D26)	I/O	High	
95	MBD11	(VR1)	(D27)	I/O	High	
96	MBD12	(VR2)	(D28)	I/O	High	
97	MBD13	(VR3)	(D29)	I/O	High	
98	MBD14	(VR4)	(D30)	I/O	High	
99	MBD15	(VR5)	(D31)	I/O	High	

Note: Pin names in parentheses (...) indicate alternate functions: If ICTENA# is low with RESET high, a rising edge on XTALI will put the chip into 'In Circuit Test' mode. In ICT mode, all digital signal pins become inputs which are part of a long path starting at ENAVDD (pin 48) and proceeding to lower pin numbers around the chip to pin 1 then to pin 160 and ending at VSYNC (pin 50). If all pins in the path are high, the VSYNC output will be high. If any pin is low, the VSYNC output will be low. Thus the chip can be checked in circuit to determine if all pins are connected properly by toggling all pins one at a time and observing the effect on VSYNC. XTALI must be toggled last because rising edges on XTALI with ICTENA# high or RESET low will exit ICT mode. As a side effect, ICT mode effectively 3-states all pins except VSYNC.

If TSENA# is low with RESET high, a rising edge on XTALI will 3-state all pins. An XTALI rising edge without the enabling conditions exits 3-state.

PIN DESCRIPTIONS — Flat Panel Display Interface

Pin #	Pin Name	Type	Active	Description
57	P0	Out	High	8, 9, 12, or 18-bit flat panel data output. Refer to the table below for configurations for various panel types.
58	P1	Out	High	
60	P2	Out	High	
61	P3	Out	High	
63	P4	Out	High	
64	P5	Out	High	
65	P6	Out	High	
66	P7	Out	High	
67	P8 (SHFCLKU)	Out	High	
68	P9	Out	High	
69	P10	Out	High	
70	P11	Out	High	
71	P12	Out	High	
72	P13	Out	High	
73	P14	Out	High	
74	P15	Out	High	Pins 75 and 76 may also be configured as general purpose I/O pins. See the description of Extension Register XR72 for more information.
75	P16 (ACTI) (GPIO0)	Out	High	
76	P17 (ENABKL) (GPIO1)	Out	High	
53	FLM	Out	High	First Line Marker. Flat Panel equivalent of VSYNC.
54	LP (CL1)	Out	High	Latch Pulse. Flat Panel equivalent of HSYNC.
56	SHFCLK (CL2) (SHFCLKL)	Out	High	Shift Clock. Pixel clock for flat panel data.
55	M (DE)	Out	High	M Signal may also be configured as Display Enable (DE) for TFT Panels. See description of XR4F bit-6.
11	STNDBY#	In	Low	Standby Control Pin. Pulling this pin to ground places the 65535 in Standby Mode.
48	ENAVDD	Out	High	Power sequencing control for panel driver electronics voltage V_{DD}
47	ENAVEE	Out	High	Power sequencing control for panel LCD bias voltage V_{EE}

65535 Pin#	65535 PinName	Mono SS Panel	Mono DD 8-bit	Mono DD 16-bit	Color TFT 15-bit	Color TFT 18-bit	Color STN 8-bit	Color STN 16-bit	Color STN DD 8-bit	Color STN DD 16-bit
57	P0	P0	UD3	UD7	B0	B0	R1...	R1...	UR1...	UR1...
58	P1	P1	UD2	UD6	B1	B1	B1...	G1...	UG1...	UG1...
60	P2	P2	UD1	UD5	B2	B2	G2...	B1...	UB1...	UB1...
61	P3	P3	UD0	UD4	B3	B3	R3...	R2...	UR2...	UR2...
63	P4	P4	LD3	UD3	B4	B4	B3...	G2...	LR1...	LR1...
64	P5	P5	LD2	UD2	G0	B5	G4...	B2...	LG1...	LG1...
65	P6	P6	LD1	UD1	G1	G0	R5...	R3...	LB1...	LB1...
66	P7	P7	LD0	UD0	G2	G1	B5...	G3...	LR2...	LR2...
67	P8	–	–	LD7	G3	G2	**SHFCLKU**	B3...	–	UG2...
68	P9	–	–	LD6	G4	G3	–	R4...	–	UB2...
69	P10	–	–	LD5	R0	G4	–	G4...	–	UR3...
70	P11	–	–	LD4	R1	G5	–	B4...	–	UG3...
71	P12	–	–	LD3	R2	R0	–	R5...	–	LG2...
72	P13	–	–	LD2	R3	R1	–	G5...	–	LB2...
73	P14	–	–	LD1	R4	R2	–	B5...	–	LR3...
74	P15	–	–	LD0	–	R3	–	R6...	–	LG3...
75	ACTI	ACTI	ACTI	ACTI	ACTI	**R4**	ACTI	ACTI	ACTI	ACTI
76	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	**R5**	ENABKL	ENABKL	ENABKL	ENABKL
56	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	**SHFCLKL**	SHFCLK	SHFCLK	SHFCLK
Pixels per shift clk:		8	8	16	1	1	2-2/3	5-1/3	2-2/3	5-1/3

PIN DESCRIPTIONS — CRT Interface and Clock Synthesizer

Pin #	Pin Name	Type	Active	Description
51	HSYNC	Out	Both	CRT Horizontal Sync (polarity is programmable)
50	VSYNC	Out	Both	CRT Vertical Sync (polarity is programmable)
46	RED	Out	High	CRT analog video outputs from the internal color palette DAC.
44	GREEN	Out	High	
43	BLUE	Out	High	
41	RSET	In	n/a	Set point resistor for the internal color palette DAC.
155	XTALI	I/O	High	This pin serves as the series resonant crystal input.
156	XTALO	Out	High	This pin serves as the series resonant crystal output.

65535 Pin #	Signal Name	Signal Status	Signal Polarity
53	FLM	ForcedLow	XR54 bit 7
54	LP	ForcedLow	XR54 bit 6
56	SHFCLK	ForcedLow	N/A
55	M	ForcedLow	N/A
57	P0	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
58	P1	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
60	P2	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
61	P3	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
63	P4	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
64	P5	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
65	P6	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
66	P7	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
67	P8	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
68	P9	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
69	P10	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
70	P11	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
71	P12	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
72	P13	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
73	P14	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
74	P15	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
75	P16	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
76	P17	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)

Panel Output Signal Status During Standby Mode

		Signal Status		
65535 Pin #	Signal Name	Local Bus	PI Bus	ISA Bus
36	LDEV#	Driven High	Tri-Stated	N/A
37	LRDY#	Tri-Stated	Tri-Stated	Tri-Stated
38	OEL#	Driven	BVCC	Tri-Stated (see note 1)
39	OEH#	Driven	GND	Tri-Stated
40	BS16#	Tri-Stated	GND	Tri-Stated
156	XTALO	Driven (see note 2)	Driven (see note 2)	Driven (see note 2)
78	RASB#	Driven (see note 3)	Driven (see note 3)	Driven (see note 3)
79	WEB#	Driven (see note 4)	Driven (see note 4)	Driven (see note 4)
80	CASBH#	Driven (see note 4)	Driven (see note 4)	Driven (see note 4)
81	CASBL#	Driven (see note 4)	Driven (see note 4)	Driven (see note 4)

CPU, Memory, and Clock Output Signal Status During Standby Mode

Notes:
1 In ISA bus mode, OEL# can be configured to be ROMCS#. ROMCS# will be driven high during Standby Mode.
2 The XTALO pin will always be driven except when XR33 bit-2 is set to '1'.
3 RASB# will be driven when using 2 x16 DRAMs. or PC Video. This pin should be left disconnected for 32-bit VL bus operation.
4 These pins should be left disconnected when using a 32-bit VL bus or PC Video. These pins are driven when using a 32-bit memory bus.

PIN DESCRIPTIONS **Power and Ground**

Pin #	Pin Name		Type	Active	Description
62	IVCC		VCC	--	Power (Internal Logic). Either 5V or 3.3V ±10%
139	IVCC		VCC	--	
19	BVCC		VCC	--	Power (Bus Interface). Either 5V or 3.3V ±10%
29	BVCC		VCC	--	
52	DVCC		VCC	--	Power (Display Interface). Either 5V or 3.3V ±10%
118	MVCC		VCC	--	Power (Memory Interface). Either 5V or 3.3V ±10%
132	RVCC		VCC	--	Power (+5V reference for mixed 3.3V / 5V interface)
86	XVCC		VCC	--	Power. Either 5V or 3.3V ±10%
12	GND		GND	--	Ground
22	GND	(BGND)	GND	--	
32	GND	(BGND)	GND	--	
49	GND	(DGND)	GND	--	
59	GND	(IGND)	GND	--	
77	GND		GND	--	
83	GND	(XGND)	GND	--	
115	GND	(MGND)	GND	--	
142	GND	(IGND)	GND	--	
45	AVCC		VCC	--	Analog power and ground pins for noise isolation for the internal RAMDAC.
42	AGND		GND	--	
157	CVCC		VCC	--	Power and ground pins for noise isolation for the internal clock synthesizer. Must be the same as VCC for internal logic.
158	CVCC		VCC	--	
154	CGND		GND	--	
160	CGND		GND	--	

Note: Pin names in parentheses (...) indicate alternate functions

I/O Map

Port Address	Read	Write
102	Global Enable (ISA Bus Only)	Global Enable (ISA Bus Only)
3B0	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B1	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B2	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B3	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B4	CRTC Index	CRTC Index
3B5	CRTC Data	CRTC Data
3B6	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B7	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B8	Hercules Mode Register (MODE)	Hercules Mode Register (MODE)
3B9	--	Set Light Pen FF (ignored)
3BA	Status Register (STAT)	Feature Control Register (FCR)
3BB	--	Clear Light Pen FF (ignored)
3BC	Reserved for system parallel port	
3BD		
3BE		
3BF	Hercules Configuration Register (HCFG)	Hercules Configuration Register (HCFG)
3C0	Attribute Controller Index / Data	Attribute Controller Index / Data
3C1	Attribute Controller Index / Data	Attribute Controller Index / Data
3C2	Feature Read Register (FCR)	Miscellaneous Output Register (MSR)
3C3	Video Subsystem Enable (VSE) (LB Only)	Video Subsystem Enable (VSE) (LB Only)
3C4	Sequencer Index	Sequencer Index
3C5	Sequencer Data	Sequencer Data
3C6, 83C6	Color Palette Mask	Color Palette Mask
3C7, 83C7	Color Palette State	Color Palette Read Mode Index
3C8, 83C8	Color Palette Write Mode Index	Color Palette Write Mode Index
3C9, 83C9	Color Palette Data	Color Palette Data
3CA	Feature Read Register (FEAT)	--
3CB	--	--
3CC	Miscellaneous Output Register (MSR)	--
3CD	--	--
3CE	Graphics Controller Index	Graphics Controller Index
3CF	Graphics Controller Data	Graphics Controller Data
3D0	--	--
3D1	--	--
3D2	--	--
3D3	--	--
3D4	CRTC Index	CRTC Index
3D5	CRTC Data	CRTC Data
3D6	CHIPS™ Extensions Index	CHIPS™ Extensions Index
3D7	CHIPS™ Extensions Data	CHIPS™ Extensions Data
3D8	CGA Mode Register (MODE)	CGA Mode Register (MODE)
3D9	CGA Color Register (COLOR)	CGA Color Register (COLOR)
3DA	Status Register (STAT)	Feature Control Register (FCR)
3DB	--	Clear Light Pen FF (ignored)
3DC	--	Set Light Pen FF (ignored)
46E8	--	Setup Control (ISA Bus Only)

Mono Mode

Color Mode

REGISTER SUMMARY - CGA, MDA, AND HERCULES MODEs

Register	Register Name	Bits	Access	I/O Port - MDA/Herc	I/O Port - CGA	Comment
ST00 (STAT)	Display Status	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB(ignored)	3DB(ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9(ignored)	3DC(ignored)	ref only: no light pen
MODE	CGA/MDA/Hercules Mode Control	7	R/W	3B8	3D8	
COLOR	CGA Color Select	6	R/W	n/a	3D9	
HCFG	Hercules Configuration	2	W	3BF	n/a	
			R	3D6-3D7 index 14	n/a	XR14
RX, R0-11	'6845' Registers	0-8	R/W	3B4-3B5	3D4-3D5	
XRX, XR0-7F	Extension Registers	0-8	R/W	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - EGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
MSR	Miscellaneous Output	7	W	3C2	3C2	
FCR	Feature Control	3	W	3BA	3DA	
ST00 (FEAT)	Feature Read (Input Status 0)	4	R	3C2	3C2	
ST01 (STAT)	Display Status (Input Status 1)	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB(ignored)	3DB(ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9(ignored)	3DC(ignored)	ref only: no light pen
SRX, SR0-7	Sequencer	0-8	R/W	3C4-3C5	3C4-3C5	
CRX, CR0-3F	CRT Controller	0-8	R/W	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	R/W	3CE-3CF	3CE-3CF	
ARX, AR0-14	Attributes Controller	0-8	R/W	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	R/W	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - VGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
VSE	Video Subsystem Enable	1	R/W	3C3 if LB	3C3 if LB	Disabled by XR70 bit-6
SETUP	Setup Control	2	W	46E8 if ISA	46E8 if ISA	Disabled by XR70 bit-7
ENABLE	Global Enable	1	R/W	102 if ISA	102 if ISA	Setup Only
MSR	Miscellaneous Output	7	W	3C2	3C2	
			R	3CC	3CC	
FCR	Feature Control	3	W	3BA	3DA	
			R	3CA	3CA	
ST00 (FEAT)	Feature Read (Input Status 0)	4	R	3C2	3C2	
ST01 (STAT)	Display Status (Input Status 1)	6	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB(ignored)	3DB(ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9(ignored)	3DC(ignored)	ref only: no light pen
DACMASK	Color Palette Pixel Mask	8	R/W	3C6, 83C6	3C6, 83C6	
DACSTATE	Color Palette State	2	R	3C7, 83C7	3C7, 83C7	
DACRX	Color Palette Read-Mode Index	8	W	3C7, 83C7	3C7, 83C7	
DACWX	Color Palette Write-Mode Index	8	R/W	3C8, 83C8	3C8, 83C8	
DACDATA	Color Palette Data 0-FF	3x6 or 3x8	R/W	3C9, 83C9	3C9, 83C9	
SRX, SR0-7	Sequencer	0-8	R/W	3C4-3C5	3C4-3C5	
CRX, CR0-3F	CRT Controller	0-8	R/W	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	R/W	3CE-3CF	3CE-3CF	
ARX, AR0-14	Attributes Controller	0-8	R/W	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	R/W	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - INDEXED REGISTERS (VGA)

Register	Register Name	Bits	Register Type	Access (VGA)	Access (EGA)	I/O Port
SRX	Sequencer Index	3	VGA/EGA	R/W	R/W	3C4
SR0	Reset	2	VGA/EGA	R/W	R/W	3C5
SR1	Clocking Mode	6	VGA/EGA	R/W	R/W	3C5
SR2	Plane Mask	4	VGA/EGA	R/W	R/W	3C5
SR3	Character Map Select	6	VGA/EGA	R/W	R/W	3C5
SR4	Memory Mode	3	VGA/EGA	R/W	R/W	3C5
SR7	Reset Horizontal Character Counter	0	VGA	W	n/a	3C5
CRX	CRTC Index	6	VGA/EGA	R/W	R/W	3B4 Mono, 3D4 Color
CR0	Horizontal Total	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR1	Horizontal Display End	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR2	Horizontal Blanking Start	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR3	Horizontal Blanking End	5+2+1	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR4	Horizontal Retrace Start	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR5	Horizontal Retrace End	5+2+1	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR6	Vertical Total	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR7	Overflow	5	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR8	Preset Row Scan	5+2	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR9	Character Cell Height	5+3	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRA	Cursor Start	5+1	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRB	Cursor End	5+2	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRC	Start Address High	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRD	Start Address Low	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRE	Cursor Location High	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRF	Cursor Location Low	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
LPENH	Light Pen High	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
LPENL	Light Pen Low	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
CR10	Vertical Retrace Start	8	VGA/EGA	R/W	W	3B5 Mono, 3D5 Color
CR11	Vertical Retrace End	4+4	VGA/EGA	R/W	W	3B5 Mono, 3D5 Color
CR12	Vertical Display End	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR13	Offset	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR14	Underline Row Scan	5+2	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR15	Vertical Blanking Start	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR16	Vertical Blanking End	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR17	CRT Mode Control	7	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR18	Line Compare	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR22	Graphics Controller Data Latches	8	VGA	R	n/a	3B5 Mono, 3D5 Color
CR24	Attribute Controller Index/Data Latch	1	VGA	R	n/a	3B5 Mono, 3D5 Color
CR3x	Clear Vertical Display Enable FF	0	VGA	W	n/a	3B5 Mono, 3D5 Color
GRX	Graphics Controller Index	4	VGA/EGA	R/W	R/W	3CE
GR0	Set/Reset	4	VGA/EGA	R/W	R/W	3CF
GR1	Enable Set/Reset	4	VGA/EGA	R/W	R/W	3CF
GR2	Color Compare	4	VGA/EGA	R/W	R/W	3CF
GR3	Data Rotate	5	VGA/EGA	R/W	R/W	3CF
GR4	Read Map Select	2	VGA/EGA	R/W	R/W	3CF
GR5	Mode	6	VGA/EGA	R/W	R/W	3CF
GR6	Miscellaneous	4	VGA/EGA	R/W	R/W	3CF
GR7	Color Don't Care	4	VGA/EGA	R/W	R/W	3CF
GR8	Bit Mask	8	VGA/EGA	R/W	R/W	3CF
ARX	Attribute Controller Index	6	VGA/EGA	R/W	R/W	3C0 (3C1)
AR0-F	Internal Palette Regs 0-15	6	VGA/EGA	R/W	R/W	3C0 (3C1)
AR10	Mode Control	7	VGA/EGA	R/W	R/W	3C0 (3C1)
AR11	Overscan Color	6	VGA/EGA	R/W	R/W	3C0 (3C1)
AR12	Color Plane Enable	6	VGA/EGA	R/W	R/W	3C0 (3C1)
AR13	Horizontal Pixel Panning	4	VGA/EGA	R/W	R/W	3C0 (3C1)
AR14	Color Select	4	VGA	R/W	n/a	3C0 (3C1)

EXTENSION REGISTER SUMMARY: 00-2F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family					
						82C450	64300	65510	65530	65540	65545
XRX	**Extension Index Register**	7	R/W	3D6	- x x x x x x x	✓	✓	✓	✓	✓	✓
XR00	**Chip Version**	8	R/O	3D7	1 1 0 0 r r r r	✓	✓	✓	✓	✓	✓
XR01	**Configuration**	8	R/O	3D7	d d d d d d d d	✓	✓	✓	✓	✓	✓
XR02	**CPU Interface Control 1**	7	R/W	3D7	0 0 0 0 0 - 0 0	✓	✓	✓	✓	✓	✓
XR03	**CPU Interface Control 2** *(ROM Intfc)*	3	R/W	3D7	• • 0 0 • • 1 0	.	✓	.	.	✓	✓
XR04	**Memory Control 1**	5	R/W	3D7	- 0 0 - - 0 0 0	✓	✓	✓	✓	✓	✓
XR05	**Memory Control 2** *(Clock Control)*	6	R/W	3D7	• 0 • 0 0 0 0 0	.	✓	.	.	.	.
XR06	**Palette Control** *(DRAM Intfc)*	8	R/W	3D7	0 0 0 0 0 0 0 0	.	✓	✓	✓	✓	✓
XR07	-reserved- *(I/O Base)*	--	--	3D7		.	✓	.	.	.	.
XR08	**Linear Addressing Base** *(Linear Base L)*	5	R/W	3D7	x x x x x • • •	.	✓	.	.	.	.
XR09	-reserved- *(Linear Base H)*	--	--	3D7		.	✓	.	.	.	.
XR0A	-reserved- *(XRAM Mode)*	--	--	3D7		.	✓	.	.	.	.
XR0B	**CPU Paging**	5	R/W	3D7	- - - 0 0 0 0 0	✓	✓	✓	✓	✓	✓
XR0C	**Start Address Top**	2	R/W	3D7	- - - - - - 0 0	✓	✓	✓	✓	✓	✓
XR0D	**Auxiliary Offset**	2	R/W	3D7	- - - - - - 0 0	✓	✓	✓	✓	✓	✓
XR0E	**Text Mode Control**	2	R/W	3D7	- - - - 0 0 - -	✓	✓	✓	✓	✓	✓
XR0F	**Software Flags 0**	8	R/W	3D7	x x x x x x x x	.	✓	✓	✓	✓	✓
XR10	**Single/Low Map Register**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓
XR11	**High Map Register**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓
XR12	-reserved-	--	--	3D7		.	.	.	.	.	.
XR13	-reserved-	--	--	3D7		.	.	.	.	.	.
XR14	**Emulation Mode**	8	R/W	3D7	0 0 0 0 h h 0 0	✓	✓	✓	✓	✓	✓
XR15	**Write Protect**	8	R/W	3D7	0 0 0 0 0 0 0 0	✓	✓	✓	✓	✓	✓
XR16	**Vertical Overflow**	5	R/W	3D7	• 0 • 0 • 0 0 0	.	✓	.	.	.	.
XR17	**Horizontal Overflow**	7	R/W	3D7	• 0 0 0 0 0 0 0	.	✓	.	.	.	.
XR18	**Alternate HDisp End**	8	R/W	3D7	x x x x x x x x	✓	.	✓	✓	✓	✓
XR19	**Alternate HSync Start** *(Half-line)*	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓
XR1A	**Alternate HSync End**	8	R/W	3D7	x x x x x x x x	✓	.	✓	✓	✓	✓
XR1B	**Alternate HTotal**	8	R/W	3D7	x x x x x x x x	✓	.	✓	✓	✓	✓
XR1C	**Alternate H Blank Start / H Panel Size**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓
XR1D	**Alternate HBlank End**	8	R/W	3D7	0 x x x x x x x	✓	.	✓	✓	✓	✓
XR1E	**Alternate Offset**	8	R/W	3D7	x x x x x x x x	✓	.	✓	✓	✓	✓
XR1F	**Virtual EGA Switch Register**	5	R/W	3D7	0 - - - x x x x	✓	.	✓	✓	✓	✓
XR20	-reserved-	--	--	3D7		.	.	.	.	.	.
XR21	**Alt H Sync Start Ext Modes**	8	R/W	3D7	x x x x x x x x	.	.	.	✓	✓	✓
XR22	**Alt H Sync End Ext Modes**	8	R/W	3D7	x x x x x x x x	.	.	.	✓	✓	✓
XR23	**Alt H Total Ext**	8	R/W	3D7	x x x x x x x x	.	.	.	✓	✓	✓
XR24	**FP Alt Max Scanline**	5	R/W	3D7	• • • x x x x x	.	.	✓	✓	✓	✓
XR25	**FP Alt Gr H Virt Panel Size**	8	R/W	3D7	x x x x x x x x	.	.	.	✓	✓	✓
XR26	**Alt H Sync Start**	8	R/W	3D7	x x x x x x x x	.	.	.	.	.	.
XR27	-reserved-	--	--	3D7		.	.	.	.	.	.
XR28	**Video Interface**	5	R/W	3D7	0 0 0 0 - - 0 -	✓	✓	✓	✓	✓	✓
XR29	**Half Line Compare**	8	R/W	3D7	x x x x x x x x	.	.	.	.	✓	✓
XR2A	-reserved-	--	--	3D7		.	.	.	.	.	.
XR2B	**Software Flags 1**	8	R/W	3D7	0 0 0 0 0 0 0 0	✓	✓	✓	✓	✓	✓
XR2C	**FLM Delay**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR2D	**LP Delay**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR2E	**LP Delay**	8	R/W	3D7	x x x x x x x x	.	.	.	✓	✓	✓
XR2F	**LP Width**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
r = Chip revision # (starting from 0000)
– = Not implemented (always reads 0)
• = Reserved (read/write, reset to 0)
0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 82C450 & 64xxx VGAs drive CRTs only, 65xxx VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

EXTENSION REGISTER SUMMARY: 30-5F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family					
						82C450	64300	65510	65530	65540	65545
XR30	**Clock Divide Control**	4	R/W	3D7	• • • • x x x x	.	✓	.	.	✓	✓
XR31	**Clock M-Divisor**	7	R/W	3D7	• x x x x x x x	.	✓	.	.	✓	✓
XR32	**Clock N-Divisor**	7	R/W	3D7	• x x x x x x x	.	✓	.	.	✓	✓
XR33	**Clock Control**	4	R/W	3D7	• 0 0 0 • 0 • •	.	✓	.	.	✓	✓
XR34	-reserved-	--	--	3D7		.	.	.	.	.	.
XR35	-reserved-	--	--	3D7		.	.	.	.	.	.
XR36	-reserved-	--	--	3D7		.	.	.	.	.	.
XR37	-reserved-	--	--	3D7		.	.	.	.	.	.
XR38	-reserved-	--	--	3D7		.	.	.	.	.	.
XR39	-reserved-	--	--	3D7		.	.	.	.	.	.
XR3A	**Color Key 0**	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓	✓
XR3B	**Color Key 1**	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓	✓
XR3C	**Color Key 2**	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓	✓
XR3D	**Color Key Mask 0**	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓	✓
XR3E	**Color Key Mask 1**	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓	✓
XR3F	**Color Key Mask 2**	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓	✓
XR40	-reserved- *(BitBlt Config)*	--	--	3D7		.	✓	.	.	✓	✓
XR41	-reserved-	--	--	3D7		.	.	.	.	.	.
XR42	-reserved-	--	--	3D7		.	.	.	.	.	.
XR43	-reserved-	--	--	3D7		.	.	.	.	.	.
XR44	**Software Flag Register 2**	8	R/W	3D7	x x x x x x x x	.	✓	✓	✓	✓	✓
XR45	**Software Flag Register 3**	8	R/W	3D7	x x x x x x x x	.	.	.	.	✓	✓
XR46	-reserved-	--	--	3D7		.	.	.	.	.	.
XR47	-reserved-	--	--	3D7		.	.	.	.	.	.
XR48	-reserved-	--	--	3D7		.	.	.	.	.	.
XR49	-reserved-	--	--	3D7		.	.	.	.	.	.
XR4A	-reserved-	--	--	3D7		.	.	.	.	.	.
XR4B	-reserved-	--	--	3D7		.	.	.	.	.	.
XR4C	-reserved-	--	--	3D7		.	.	.	.	.	.
XR4D	-reserved-	--	--	3D7		.	.	.	.	.	.
XR4E	-reserved-	--	--	3D7		.	.	.	.	.	.
XR4F	**Panel Format 2**	5	R/W	3D7	x x • • • x x x	.	.	.	.	✓	✓
XR50	**Panel Format 1**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR51	**Display Type**	7	R/W	3D7	0 0 0 • 0 0 0 0	.	.	✓	✓	✓	✓
XR52	**Power Down Control** *(Refresh Ctrl)*	8	R/W	3D7	0 0 0 0 0 0 0 0	.	✓	✓	✓	✓	✓
XR53	**Panel Format 3**	7	R/W	3D7	• x x x x x x 0	.	.	✓	✓	✓	✓
XR54	**Panel Interface**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR55	**H Compensation**	6	R/W	3D7	x x x x • • x x	.	.	✓	✓	✓	✓
XR56	**H Centering**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR57	**V Compensation**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR58	**V Centering**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR59	**V Line Insertion**	7	R/W	3D7	x x x • x x x x	.	.	✓	✓	✓	✓
XR5A	**V Line Replication**	4	R/W	3D7	• • • • x x x x	.	.	✓	✓	✓	✓
XR5B	**Power Sequencing Delay**	8	R/W	3D7	0 1 1 1 0 0 0 1	.	.	✓	✓	✓	✓
XR5C	**Activity Indicator Control**	7	R/W	3D7	0 x • x x x x x	.	.	.	.	✓	✓
XR5D	**FP Diagnostic**	8	R/W	3D7	0 0 0 0 0 0 0 0	.	.	.	.	✓	✓
XR5E	**M(ACDCLK) Control**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR5F	**Power Down Mode Refresh**	8	R/W	3D7	x x x x x x x x	.	.	.	✓	✓	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
r = Chip revision # (starting from 0000)
– = Not implemented (always reads 0)
• = Reserved (read/write, reset to 0)
0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 82C450 & 64xxx VGAs drive CRTs only, 65xxx VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

EXTENSION REGISTER SUMMARY: 60-7F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family					
						82C450	64300	65510	65530	65540	65545
XR60	**Blink Rate Control**	8	R/W	3D7	1 0 0 0 0 0 1 1	.	✓	✓	✓	✓	✓
XR61	**SmartMap™ Control**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR62	**SmartMap™ Shift Parameter**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR63	**SmartMap™ Color Mapping Control**	8	R/W	3D7	x 1 x x x x x x	.	.	✓	✓	✓	✓
XR64	**FP Alternate Vertical Total**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR65	**FP Alternate Overflow**	6	R/W	3D7	x x x • • x x x	.	.	✓	✓	✓	✓
XR66	**FP Alternate Vertical Sync Start**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR67	**FP Alternate Vertical Sync End**	4	R/W	3D7	• • • • x x x x	.	.	✓	✓	✓	✓
XR68	**FP V Panel Size**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓	✓
XR69	-reserved-	--	--	3D7		.	.	.	.	.	.
XR6A	-reserved-	--	--	3D7		.	.	.	.	.	.
XR6B	-reserved-	--	--	3D7		.	.	.	.	.	.
XR6C	**Programmable Output Drive**	5	R/W	3D7	• • 0 0 0 0 d •	.	.	✓	✓	✓	✓
XR6D	-reserved-	--	--	3D7		.	.	.	.	.	.
XR6E	**Polynomial FRC Control**	8	R/W	3D7	1 0 1 1 1 1 0 1	.	.	✓	✓	✓	✓
XR6F	**Frame Buffer Control**	3	R/W	3D7	0 • • • • • 0 0	.	.	.	✓	✓	✓
XR70	**Setup / Disable Control**	1	R/W	3D7	0 - - - - - - -	✓	✓	✓	✓	✓	✓
XR71	-reserved- *(GPIO Control)*	--	--	3D7		.	✓	.	.	.	.
XR72	**External Device I/O** *(GPIO Data)*	8	R/W	3D7	0 0 0 0 0 0 0 0	.	✓	.	.	.	.
XR73	**DPMS Control** *(Misc Control)*	4	R/W	3D7	- - - - 0 0 0 0	.	✓	.	.	✓	✓
XR74	-reserved- *(Configuration 2)*	--	--	3D7		.	✓	.	.	.	.
XR75	-reserved- *(Software Flags 3)*	--	--	3D7		.	✓	.	.	.	.
XR76	-reserved-	--	--	3D7		.	.	.	.	.	.
XR77	-reserved-	--	--	3D7		.	.	.	.	.	.
XR78	-reserved-	--	--	3D7		.	.	.	.	.	.
XR79	-reserved-	--	--	3D7		.	.	.	.	.	.
XR7A	-reserved-	--	--	3D7		.	.	.	.	.	.
XR7B	-reserved-	--	--	3D7		.	.	.	.	.	.
XR7C	-reserved-	--	--	3D7		.	.	.	.	.	.
XR7D	**FP Compensation Diagnostic**	0	R/O	3D7	- - - - - - - -	.	✓	✓	✓	✓	✓
XR7E	**CGA/Hercules Color Select**	6	R/W	3D7	- - x x x x x x	✓	.	✓	✓	✓	✓
XR7F	**Diagnostic**	8	R/W	3D7	0 0 x x x x 0 0	✓	✓	✓	✓	✓	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
r = Chip revision # (starting from 0000)
– = Not implemented (always reads 0)
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Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 82C450 & 64xxx VGAs drive CRTs only, 65xxx VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

Registers

GLOBAL CONTROL (SETUP) REGISTERS

The Setup Control Register and Video Subsystem Enable registers are used to enable or disable the VGA. The Setup Control register is also used to place the VGA in normal or setup mode (the Global Enable Register is accessible only during Setup mode). The Setup Control register is used only in ISA bus interfaces; the Video Subsystem Enable register is used only in Local Bus configurations. The various internal 'disable' bits 'OR' together to provide multiple ways of disabling the chip; all 'disable' bits must be off to enable access to the chip. When the chip is 'disabled' in this fashion, only bus access is disabled; other functions remain operational (memory refresh, display refresh, etc).

Note: In setup mode in the IBM VGA, the Global Setup Register (defined as port address 102) actually occupies the *entire I/O space* . Only the lower 3 bits are used to decode and select this register. To avoid bus conflicts with other peripherals, reads should only be performed at the 10xh port addresses while in setup mode. To eliminate potential compatibility problems in widely varying PC systems, CHIPS' VGA Controllers decode the Global Setup register at I/O port 102h only.

GENERAL CONTROL REGISTERS

Two Input Status Registers read the internal comparator output (or the Virtual Switch Register), pending CRT interrupt, display enable / horizontal sync output, and vertical retrace / video output. The Feature Control Register selects the vertical sync function while the Miscellaneous Output Register controls I/O address select, clock selection, access to video RAM, memory page, and horizontal and vertical sync polarity.

CGA / HERCULES REGISTERS

CGA Mode and Color Select registers are provided on-chip for emulation of CGA modes. Hercules Mode and Configuration registers are provided on-chip for emulation of Hercules mode.

SEQUENCER REGISTERS

The Sequencer Index Register contains a 3-bit index to the Sequencer Data Registers. The Reset Register forces an asynchronous or synchronous reset of the sequencer. The Sequencer Clocking Mode Register controls master clocking functions, video enable/disable and selects either an 8 or 9 dot character clock. A Plane/Map Mask Register enables the color plane and write protect. The Character Font Select Register handles video intensity and character generation and controls the display memory plane through the character generator select. The Sequencer Memory Mode Register handles all memory, giving access by the CPU to 4 / 16 / 32 KBytes, Odd / Even addresses (planes) and writing of data to display memory.

CRT CONTROLLER REGISTERS

The CRT Controller Index Register contains a 6-bit index to the CRT Controller Registers. Twenty eight registers perform all display functions for modes: horizontal and vertical blanking and sync, panning and scrolling, cursor size and location, light pen, and underline.

GRAPHICS CONTROLLER REGISTERS

The Graphics Controller Index Register contains a 4-bit index to the Graphics Controller Registers. The Set/Reset Register controls the format of the CPU data to display memory. It also works with the Enable Set/Reset Register. Reducing 32 bits of display data to 8 bits of CPU data is accomplished by the Color Compare Register. Data Rotate Registers specify the CPU data bits to be rotated and subjected to logical operations. The Read Map Select Register reduces memory data for the CPU in the four plane (16 color) graphics mode. The Graphics Mode Register controls the write, read, and shift register modes. The Miscellaneous Register handles graphics/text, chaining of odd/even planes, and display memory mapping. Additional registers include Color Don't Care and Bit Mask.

ATTRIBUTE CONTROLLER AND COLOR PALETTE REGISTERS

The Attribute Controller Index Register contains a 5-bit index to the Attribute Controller Registers. A 6th bit is used to enable the video. The Attribute Controller Registers handle internal color lookup table mapping, text/graphics mode, overscan color, and color plane enable. The horizontal Pixel Panning and Pixel Padding Registers control pixel attributes on screen.

Color palette registers handle CPU reads and writes to I/O address range 3C6h-3C9h. Inmos IMSG176 (Brooktree BT471/476) compatible registers are documented in this manual.

EXTENSION REGISTERS

The 65535 defines a set of extension registers which are addressed with the 7-bit Extension Register Index. The I/O port address is fixed at 3D6-3D7h and read/write access is always enabled to improve software performance.

The extension registers handle a variety of interfacing, compatibility, and display functions as discussed below. They are grouped into the following logical groups for discussion purposes:

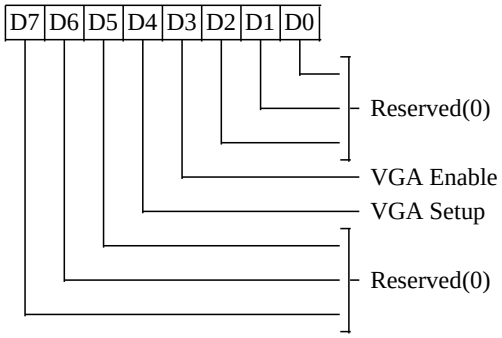
1. Miscellaneous Registers include the Version number, Dip Switch, CPU interface, paging control, memory mode control, and diagnostic functions.
2. General Purpose Registers handle video blanking and the video default color.
3. Backwards Compatibility Registers control Hercules, MDA, and CGA emulation modes. Write Protect functions are provided to increase flexibility in providing backwards compatibility.
4. Alternate Horizontal and Vertical Registers handle all horizontal and vertical timing, including sync, blank and offset. These are used for backwards compatibility.
5. Flat Panel Registers handle all internal logic specific to driving of flat panel displays.

Note: The state of most of the Standard VGA Registers is undefined at reset. All registers specific to the 65535 (Extension Registers) are summarized in the Extension Register Table.

Global Control (Setup) Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SETUP	Setup Control	–	W	46E8h (ISA bus only)	–	41
VSE	Video Subsystem Enable	–	W	3C3h (Local bus only)	–	41
ENAB	Global Enable	–	R/W	102h (Setup mode only)	–	42

SETUP CONTROL REGISTER (SETUP)
Write only at I/O Address 46E8h



This register is accessible in ISA bus configurations only. It is ignored completely in Local Bus configurations. It is also ignored if XR70 bit-7 is set to 1 (the default is 0).

This register is cleared by RESET.

2-0 Reserved (0)

3 VGA Enable

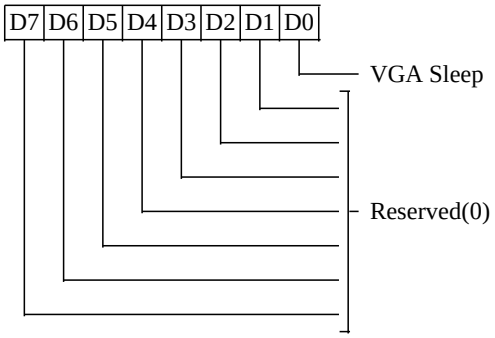
0 VGA is disabled
1 VGA is enabled

4 Setup Mode

0 VGA is in Normal Mode
1 VGA is in Setup Mode

7-5 Reserved (0)

VIDEO SUBSYSTEM ENABLE REGISTER (VSE)
Write Only at I/O Address 3C3h



This register is accessible in Local Bus configurations only. It is ignored in ISA bus configurations (register 46E8 is used in ISA bus configurations). Access to this register may be disabled by setting XR70 bit-7 to 1 (the default is 0).

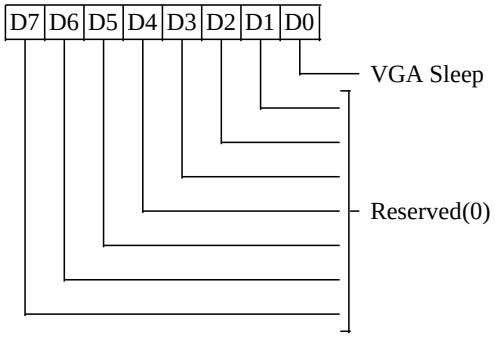
This register is cleared by RESET.

0 VGA Sleep

0 VGA is disabled
1 VGA is enabled

7-1 Reserved (0)

GLOBAL ENABLE REGISTER (ENAB)
Read/Write at I/O Address 102h



This register is only accessible in Setup Mode (enabled by register 46E8 in ISA bus configurations.

Bit-0 of this register is cleared by RESET in ISA bus configurations and set by RESET in Local Bus configurations.

0 VGA Sleep

0 VGA is disabled
1 VGA is enabled

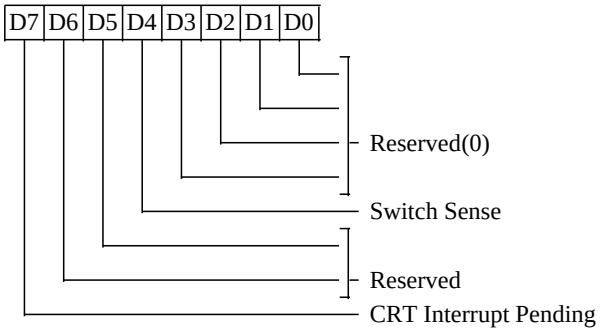
7-1 Reserved (0)

General Control & Status Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ST00	Input Status 0	–	R	3C2h	–	43
ST01	Input Status 1	–	R	3BAh/3DAh	–	43
FCR	Feature Control	–	W	3BAh/3DAh	5	44
			R	3CAh		
MSR	Miscellaneous Output	–	W	3C2h	5	44
			R	3CCh		

INPUT STATUS REGISTER 0 (ST00)

Read only at I/O Address at 3C2h



3-0 Reserved (0)

4 Switch Sense

This bit returns the Status of the SENSE pin or the Virtual Switch Register (XR1F) output if enabled by XR1F bit-7. XR1F bit-7 takes priority over the other settings if set.

6-5 Reserved

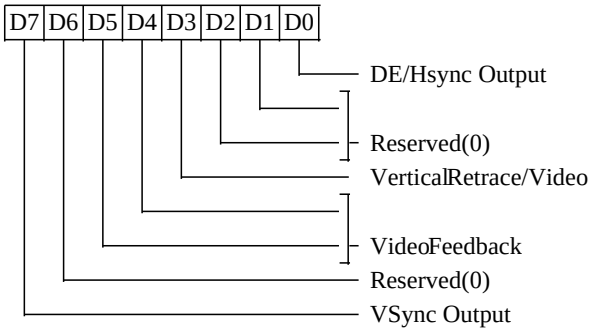
These bits read back 00 in PC and PI bus configurations and 11 in MC configuration.

7 CRT Interrupt Pending

0 Indicates no CRT interrupt is pending
1 Indicates a CRT interrupt is waiting to be serviced

INPUT STATUS REGISTER 1 (ST01)

Read only at I/O Address 3BAh/3DAh



0 Display Enable/HSYNC Output

The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-4).

0 Indicates DE or HSYNC inactive
1 Indicates DE or HSYNC active

2-1 Reserved (0)

3 Vertical Retrace/Video

The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-5).

0 Indicates VSYNC or video inactive
1 Indicates VSYNC or video active

5-4 Video Feedback 1, 0

These are diagnostic video bits which are selected via the Color Plane Enable Register.

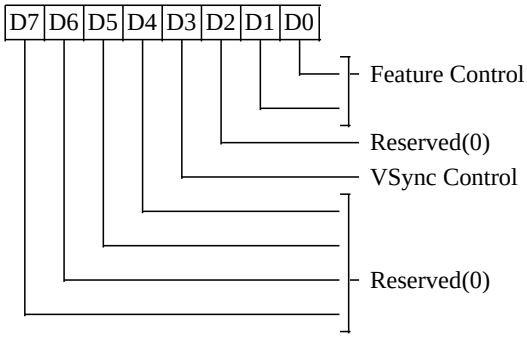
6 Reserved (0)

7 VSync Output

The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-6). It reflects the active status of the VSYNC output: 0=inactive, 1=active.

FEATURE CONTROL REGISTER (FCR)

Write at I/O Address 3BAh/3DAh
Read at I/O Address 3CAh
Group 5 Protection



1-0 Feature Control

These bits are used internal to the chip in conjunction with the Configuration Register (XR01). When enabled by XR01 bits 2-3 and Misc Output Register bits 3-2 = 10, these bits determine the pixel clock frequency typically as follows:

FCR1:0 = 00 = 40.000 MHz
FCR1:0 = 01 = 50.350 MHz
FCR1:0 = 10 = User defined
FCR1:0 = 11 = 44.900 MHz

This preserves compatibility with drivers developed for earlier generation Chips and Technologies VGA controllers.

2 Reserved (0)

3 Vsync Control

This bit is cleared by RESET.

0 VSync output on the VSYNC pin
1 Logical 'OR' of VSync and Display Enable output on the VSYNC pin

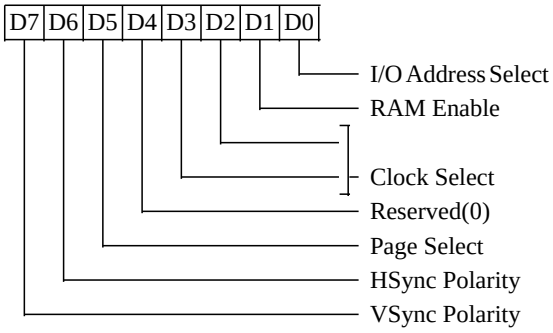
This capability is not typically very useful, but is provided for IBM compatibility.

7-4 Reserved (0)

CRT Display Sync Polarities				
V	H	Display	H Freq	V Freq
P	P	>480 Line	Variable	Variable
P	P	200 Line	15.7 KHz	60 Hz
N	P	350 Line	21.8 KHz	60 Hz
P	N	400 Line	31.5 KHz	70 Hz
N	N	480 Line	31.5 KHz	60 Hz

MISCELLANEOUS OUTPUT REGISTER (MSR)

Write at I/O Address 3C2h
Read at I/O Address 3CCh
Group 5 Protection



This register is cleared by RESET.

0 I/O Address Select
This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01).

0 Select 3Bxh I/O address
1 Select 3Dxh I/O address

1 RAM Enable

0 Prevent CPU access to display memory
1 Allow CPU access to display memory

3-2 Clock Select. These bits usually select the dot clock source for the CRT interface:

MSR3:2 = 00 = Select CLK0
MSR3:2 = 01 = Select CLK1
MSR3:2 = 10 = Select CLK2
MSR3:2 = 11 = Select CLK3

See extension register XR01 bits 2-3 (Configuration) and FCR bits 0-1 for variations of the above clock selection mapping. See also XR1F (Virtual Switch Register) for additional functionality potentially controlled by these bits.

4 Reserved (0)

5 Page Select. In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64 KByte page in display memory for CPU access: 0=select upper page; 1=select lower page.

6 CRT HSync Polarity. 0=pos, 1=neg

7 CRT VSync Polarity. 0=pos, 1=neg

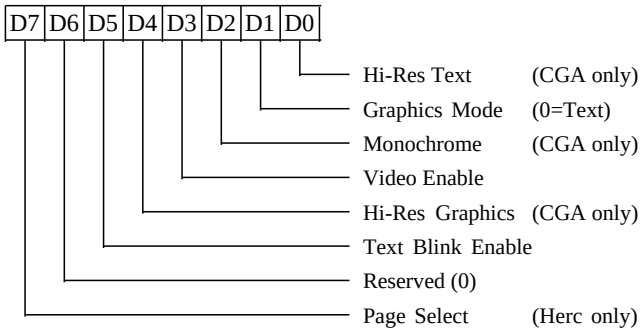
(Blank pin polarity can be controlled via the Video Interface Register, XR28). XR55 bits 6-7 are used to control H/V sync polarity instead of these bits if XR51 bit-2 = 1 (display type = flat panel).

CGA / Hercules Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
MODE	CGA/Hercules Mode	–	R/W	3D8h	–	45
COLOR	CGA Color Select	–	R/W	3D9h	–	46
HCFG	Hercules Configuration	–	R/W	3BFh	–	46

CGA / HERCULES MODE CONTROL REGISTER (MODE)

Read/Write at I/O Address 3B8h/3D8h



This register is effective only in CGA and Hercules modes. It is accessible if CGA or Hercules emulation mode is selected or the extension registers are enabled. If the extension registers are enabled, the address is determined by the address select in the Miscellaneous Outputs register. Otherwise the address is determined by the emulation mode. It is cleared by RESET.

0 CGA 80/40 Column Text Mode
- 0 Select 40 column CGA text mode
- 1 Select 80 column CGA text mode

1 CGA/Hercules Graphics/Text Mode
- 0 Select text mode
- 1 Select graphics mode

2 CGA Mono/Color Mode
- 0 Select CGA color mode
- 1 Select CGA monochrome mode

3 CGA/Hercules Video Enable
- 0 Blank the screen
- 1 Enable video output

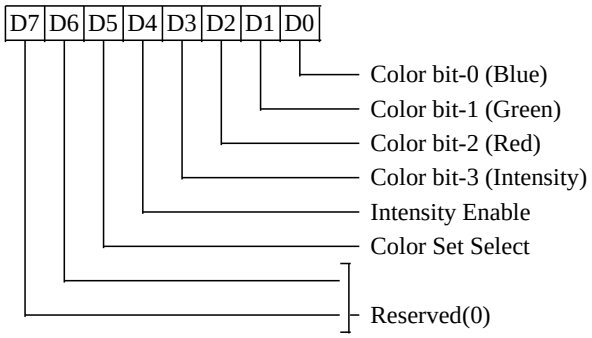
4 CGA High Resolution Mode
- 0 Select 320x200 graphics mode
- 1 Select 640x200 graphics mode

5 CGA/Hercules Text Blink Enable
- 0 Disable character blink attribute (blink attribute bit-7 used to control background intensity)
- 1 Enable character blink attribute

6 Reserved (0)

7 Hercules Page Select
- 0 Select the lower part of memory (starting address B0000h) in Hercules Graphics Mode
- 1 Select the upper part of the memory (starting address B8000h) in Hercules Graphics Mode

CGA COLOR SELECT REGISTER (COLOR)
Read/Write at I/O Address 3D9h



This register is effective only in CGA modes. It is accessible if CGA emulation mode is selected or the extension registers are enabled. This register may also be read or written as an Extension Register (XR7E). It is cleared by RESET.

3-0 Color

320x200 4-color: Background Color (color when the pixel value is 0)

The foreground colors (colors when the pixel value is 1-3) are determined by bit-5 of this register.

640x200 2-color:
Foreground Color (color when the pixel value is 1)

The background color (color when the pixel value is 0) is black.

4 Intensity Enable

TextMode:	Enables intensified background colors
320x200 4-color:	Enables intensified colors 0-3
640x200 2-color:	Don't care

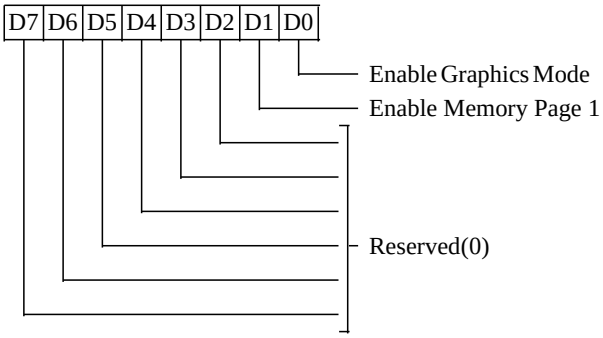
5 Color Set Select

This bit selects one of two available CGA color palettes to be used in 320x200 graphics mode (it is ignored in all other modes) according to the following table:

Pixel Value	Color Set 0	Color Set 1
0 0	Color per bits 0-3	Color per bits 0-3
0 1	Green	Cyan
1 0	Red	Magenta
1 1	Brown	White

7-6 Reserved (0)

HERCULES CONFIGURATION REGISTER (HCFG)
Write only at I/O Address 3BFh



This register is effective only in Hercules mode. It is accessible in Hercules emulation mode or if the extension registers are enabled. It may be read back through XR14 bits 2 & 3. It is cleared by RESET.

0 Enable Graphics Mode

0 Lock the chip in Hercules text mode. In this mode, the CPU has access only to memory address range B0000h-B7FFFh (in text mode the same area of display memory wraps around 8 times within this range such that B0000 accesses the same display memory location as B1000, B2000, etc.).
1 Permit entry to Hercules Graphics mode

1 Enable Memory Page 1

0 Prevent setting of the Page Select bit (bit 7 of the Hercules Mode Control Register). This function also restricts memory usage to addresses B0000h-B7FFFh.
1 The Page Select bit can be set and the upper part of display memory (addresses B8000h - BFFFFh) is available.

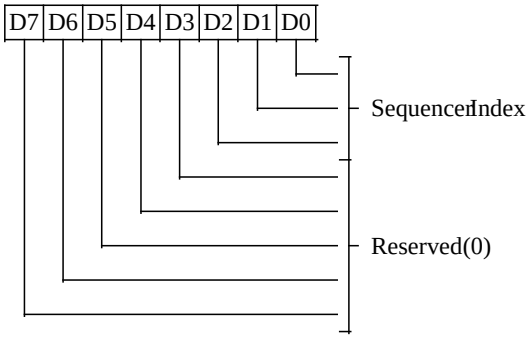
7-2 Reserved (0)

Sequencer Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SRX	Sequencer Index	–	R/W	3C4h	1	47
SR00	Reset	00h	R/W	3C5h	1	47
SR01	Clocking Mode	01h	R/W	3C5h	1	48
SR02	Plane/Map Mask	02h	R/W	3C5h	1	48
SR03	Character Font	03h	R/W	3C5h	1	49
SR04	Memory Mode	04h	R/W	3C5h	1	50
SR07	Horizontal Character Counter Reset	07h	W	3C5h	–	50

SEQUENCER INDEX REGISTER (SRX)

Read/Write at I/O Address 3C4h



This register is cleared by reset.

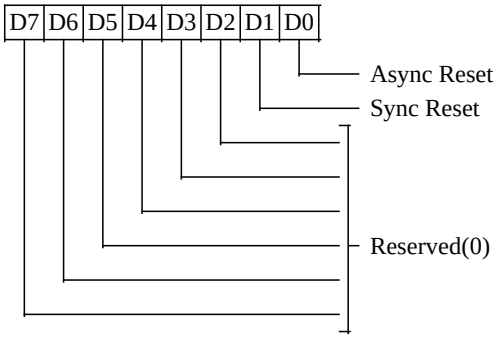
2-0 Sequencer Index

These bits contain a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7.

7-3 Reserved (0)

SEQUENCER RESET REGISTER (SR00)

Read/Write at I/O Address 3C5h
Index 00h
Group 1 Protection



0 Asynchronous Reset

0 Force asynchronous reset
1 Normal operation

Display memory data will be corrupted if this bit is set to zero.

1 Synchronous Reset

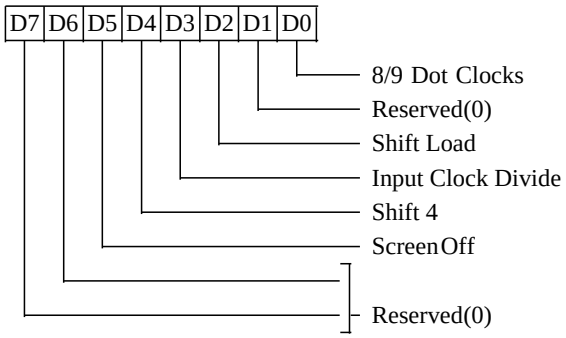
0 Force synchronous reset
1 Normal operation

Display memory data is not corrupted if this bit is set to zero for a short period of time (a few tenths of a microsecond).

7-2 Reserved (0)

SEQUENCER CLOCKING MODE REGISTER (SR01)

Read/Write at I/O Address 3C5h
Index 01h
Group 1 Protection



0 8/9 Dot Clocks

This bit determines whether a character clock is 8 or 9 dot clocks long.

0 Select 9 dots/character clock
1 Select 8 dots/character clock

1 Reserved (0)

2 Shift Load

0 Load video data shift registers every character clock
1 Load video data shift registers every other character clock

Bit-4 of this register must be 0 for this bit to be effective.

3 Input Clock Divide

0 Sequencer master clock output on the PCLK pin (used for 640 (720) pixel modes)
1 Master clock divided by 2 output on the PCLK pin (used for 320 (360) pixel modes)

4 Shift 4

0 Load video shift registers every 1 or 2 character clocks (depending on bit-2 of this register)
1 Load shift registers every 4th character clock.

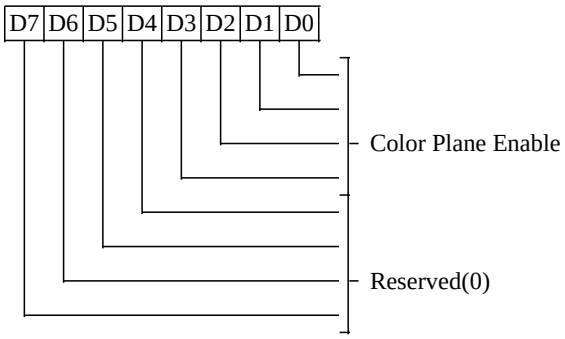
5 Screen Off

0 Normal Operation
1 Disable video output and assign all display memory bandwidth for CPU accesses

7-6 Reserved (0)

SEQUENCER PLANE/MAP MASK REGISTER (SR02)

Read/Write at I/O Address 3C5h
Index 02h
Group 1 Protection



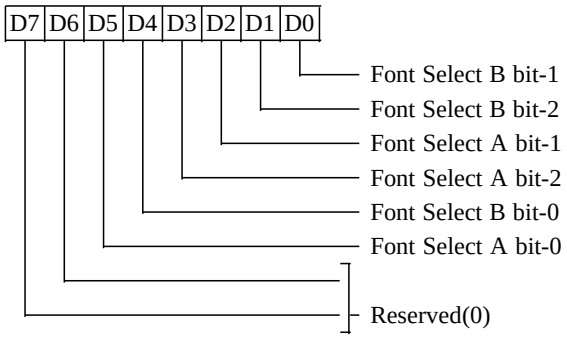
3-0 Color Plane Enable

0 Write protect corresponding color plane
1 Allow write to corresponding color plane.

In Odd/Even and Quad modes, these bits still control access to the corresponding color plane.

7-4 Reserved (0)

CHARACTER FONT SELECT REGISTER (SR03)
Read/Write at I/O Address 3C5h
Index 03h
Group 1 Protection



In text modes, bit-3 of the video data's attribute byte normally controls the foreground intensity. This bit may be redefined to control switching between character sets. This latter function is enabled whenever there is a difference in the values of the Character Font Select A and the Character Font Select B bits. If the two values are the same, the character select function is disabled and attribute bit-3 controls the foreground intensity.

SR04 bit-1 must be 1 for the character font select function to be active. Otherwise, only character fonts 0 and 4 are available.

1-0 High order bits of Character Generator Select B

3-2 High order bits of Character Generator Select A

4 Low order bit of Character Generator Select B

5 Low order bit of Character Generator Select A

7-6 Reserved (0)

The following table shows the display memory plane selected by the Character Generator Select A and B bits.

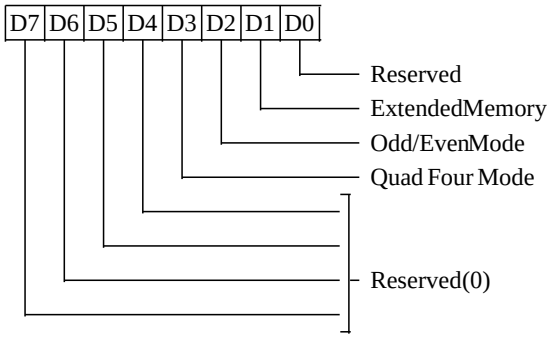
Code	Character Generator Table Location
0	First 8K of Plane 2
1	Second 8K of Plane 2
2	Third 8K of Plane 2
3	Fourth 8K of Plane 2
4	Fifth 8K of Plane 2
5	Sixth 8K of Plane 2
6	Seventh 8K of Plane 2
7	Eighth 8K of Plane 2

where 'code' is:

Character Generator Select A (bits 3, 2, 5) when bit-3 of the the attribute byte is one.

Character Generator Select B (bits 1, 0, 4) when bit-3 of the attribute byte is zero.

SEQUENCER MEMORY MODE REGISTER (SR04)
Read/Write at I/O Address 3C5h
Index 04h
Group 1 Protection



0 Reserved (0)

1 Extended Memory

0 Restrict CPU access to 4/16/32 K Bytes
1 Allow complete access to memory

This bit should normally be 1.

2 Odd/Even Mode

0 CPU accesses to Odd/Even addresses are directed to corresponding odd/even planes
1 All planes are accessed simultaneously (IRGB color)

Bit-3 of this register must be 0 for this bit to be effective. This bit affects only CPU write accesses to display memory.

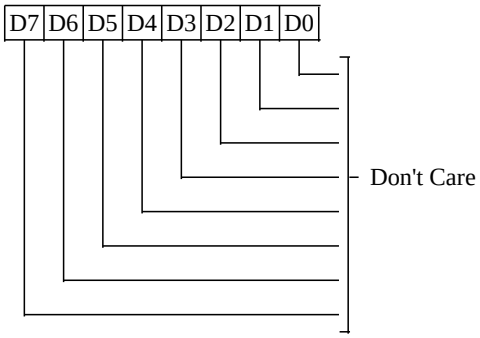
3 Quad Four Mode

0 CPU addresses are mapped to display memory as defined by bit-2 of this register
1 CPU addresses are mapped to display memory modulo 4. The two low order CPU address bits select the display memory plane.

This bit affects both CPU reads and writes to display memory.

7-4 Reserved (0)

SEQUENCER HORIZONTAL CHARACTER COUNTER RESET (SR07)
Read/Write at I/O Address 3C5h
Index 07h



Writing to SR07 with any data will cause the horizontal character counter to be held reset (character counter output = 0) until a write to any other sequencer register with any data value. The write to any index in the range 0-6 clears the latch that is holding the reset condition on the character counter.

The vertical line counter is clocked by a signal derived from horizontal display enable (which does not occur if the horizontal counter is held reset). Therefore, if the write to SR07 occurs during vertical retrace, the horizontal and vertical counters will both be set to zero. A write to any other sequencer register may then be used to start both counters with reasonable synchronization to an external event via software control.

This is a standard VGA register which was not documented by IBM.

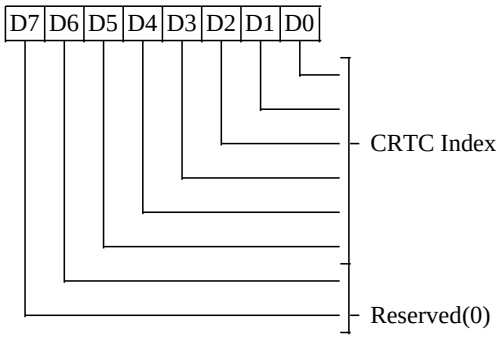
CRT Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
CRX	CRTC Index	–	R/W	3B4h/3D4h	–	52
CR00	Horizontal Total	00h	R/W	3B5h/3D5h	0	52
CR01	Horizontal Display Enable End	01h	R/W	3B5h/3D5h	0	52
CR02	Horizontal Blank Start	02h	R/W	3B5h/3D5h	0	53
CR03	Horizontal Blank End	03h	R/W	3B5h/3D5h	0	53
CR04	Horizontal Sync Start	04h	R/W	3B5h/3D5h	0	54
CR05	Horizontal Sync End	05h	R/W	3B5h/3D5h	0	54
CR06	Vertical Total	06h	R/W	3B5h/3D5h	0	55
CR07	Overflow	07h	R/W	3B5h/3D5h	0/3	55
CR08	Preset Row Scan	08h	R/W	3B5h/3D5h	3	56
CR09	Maximum Scan Line	09h	R/W	3B5h/3D5h	2/4	56
CR0A	Cursor Start Scan Line	0Ah	R/W	3B5h/3D5h	2	57
CR0B	Cursor End Scan Line	0Bh	R/W	3B5h/3D5h	2	57
CR0C	Start Address High	0Ch	R/W	3B5h/3D5h	–	58
CR0D	Start Address Low	0Dh	R/W	3B5h/3D5h	–	58
CR0E	Cursor Location High	0Eh	R/W	3B5h/3D5h	–	58
CR0F	Cursor Location Low	0Fh	R/W	3B5h/3D5h	–	58
CR10	Vertical Sync Start (See Note 2)	10h	W or R/W	3B5h/3D5h	4	59
CR11	Vertical Sync End (See Note 2)	11h	W or R/W	3B5h/3D5h	3/4	59
CR10	Lightpen High (See Note 2)	10h	R	3B5h/3D5h	–	59
CR11	Lightpen Low (See Note 2)	11h	R	3B5h/3D5h	–	59
CR12	Vertical Display Enable End	12h	R/W	3B5h/3D5h	4	60
CR13	Offset	13h	R/W	3B5h/3D5h	3	60
CR14	Underline Row	14h	R/W	3B5h/3D5h	3	60
CR15	Vertical Blank Start	15h	R/W	3B5h/3D5h	4	61
CR16	Vertical Blank End	16h	R/W	3B5h/3D5h	4	61
CR17	CRT Mode Control	17h	R/W	3B5h/3D5h	3/4	62
CR18	Line Compare	18h	R/W	3B5h/3D5h	3	63
CR22	Memory Data Latches	22h	R	3B5h/3D5h	–	64
CR24	Attribute Controller Toggle	24h	R	3B5h/3D5h	–	64

Note 1: When MDA or Hercules emulation is enabled, the CRTC I/O address should be set to 3B0h-3B7h by setting the I/O address select bit in the Miscellaneous Output register (3C2h/3CCh bit-0) to zero. When CGA emulation is enabled, the CRTC I/O address should be set to 3D0h-3D7h by setting Misc Output Register bit-0 to 1.

Note 2: In the EGA, all CRTC registers except the cursor (CR0C-CR0F) and light pen (CR10 and CR11) registers are write-only (i.e., no read back). In both the EGA and VGA, the light pen registers are at index locations conflicting with the vertical sync registers. This would normally prevent reads and writes from occurring at the same index. Since the light pen registers are not normally useful, the VGA provides software control (CR03 bit-7) of whether the vertical sync or light pen registers are readable at indices 10-11.

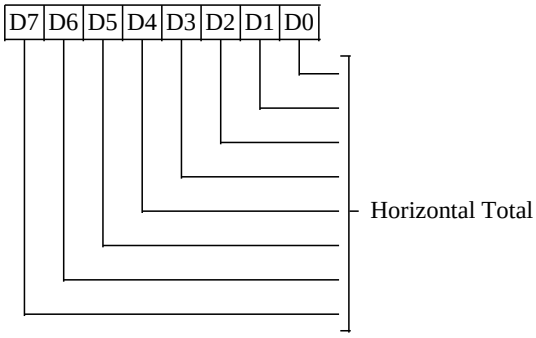
CRTC INDEX REGISTER (CRX)
Read/Write at I/O Address 3B4h/3D4h



5-0 CRTC Data Register Index

7-6 Reserved (0)

HORIZONTAL TOTAL REGISTER (CR00)
Read/Write at I/O Address 3B5h/3D5h
Index 00h
Group 0 Protection

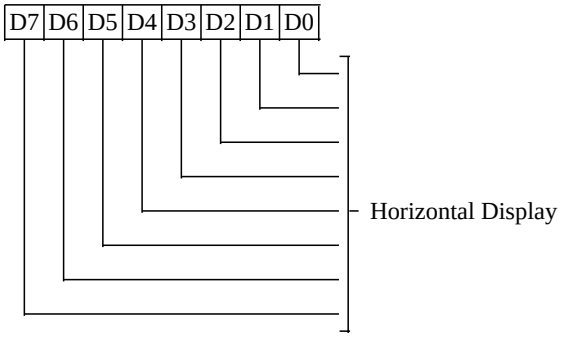


This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Total

Total number of character clocks per line = contents of this register + 5. This register determines the horizontal sweep rate.

HORIZONTAL DISPLAY ENABLE END REGISTER (CR01)
Read/Write at I/O Address 3B5h/3D5h
Index 01h
Group 0 Protection

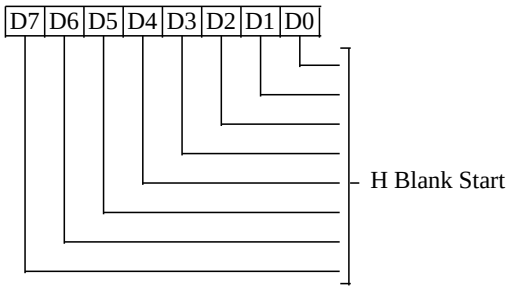


This register is used for all VGA and EGA modes on CRTs. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Display

Number of Characters displayed per scan line – 1.

HORIZONTAL BLANK START REGISTER (CR02)
Read/Write at I/O Address 3B5h/3D5h
Index 02h
Group 0 Protection

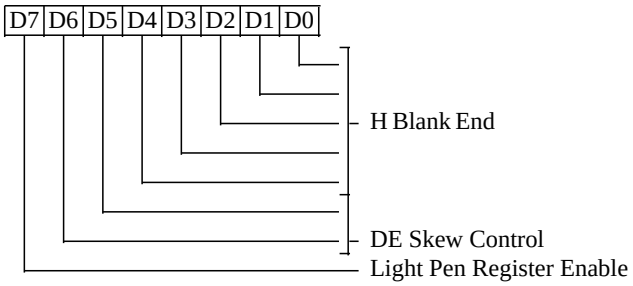


This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Blank Start

These bits specify the beginning of horizontal blank in terms of character clocks from the beginning of the display scan. The period between Horizontal Display Enable End and Horizontal Blank Start is the right side border on screen.

HORIZONTAL BLANK END REGISTER (CR03)
Read/Write at I/O Address 3B5h/3D5h
Index 03h
Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0 Horizontal Blank End

These are the lower 5 bits of the character clock count used to define the end of horizontal blank. The interval between the end of horizontal blank and the beginning of the display (a count of 0) is the left side border on the screen. If the horizontal blank width desired is W clocks, the 5-bit value programmed in this register = [contents of CR02 + W] and 1Fh. The most significant bit is programmed in CR05 bit-7. This bit = [(CR02 + W) and 20h]/20h.

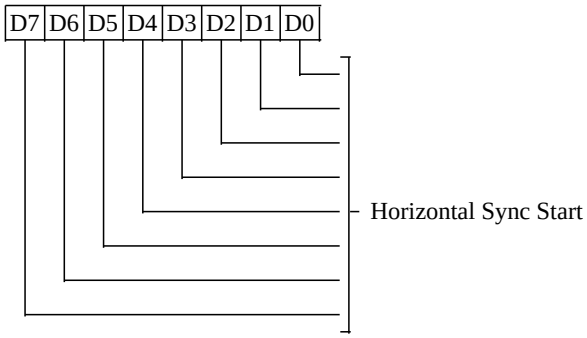
6-5 Display Enable Skew Control

Defines the number of character clocks that the Display Enable signal is delayed to compensate for internal pipeline delays.

7 Light Pen Register Enable

This bit must be 1 for normal operation; when this bit is 0, CRTC registers CR10 and CR11 function as lightpen readback registers.

HORIZONTAL SYNC START REGISTER (CR04)
Read/Write at I/O Address 3B5h/3D5h
Index 04h
Group 0 Protection

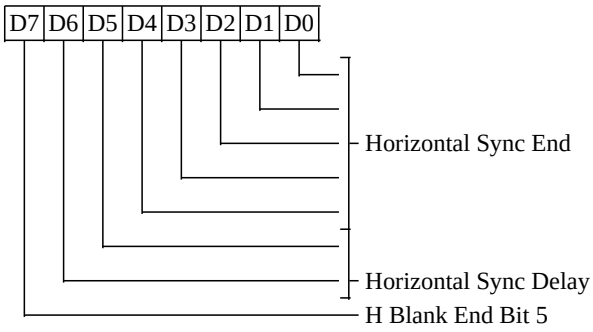


This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Sync Start

These bits specify the beginning of Hsync in terms of Character clocks from the beginning of the display scan. These bits also determine display centering on the screen.

HORIZONTAL SYNC END REGISTER (CR05)
Read/Write at I/O Address 3B5h/3D5h
Index 05h
Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0 Horizontal Sync End

Lower 5 bits of the character clock count which specifies the end of Horizontal Sync. If the horizontal sync width desired is N clocks, then these bits = (N + contents of CR04) and 1Fh.

6-5 Horizontal Sync Delay

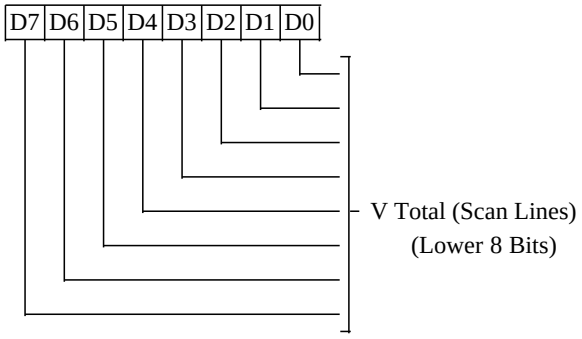
These bits specify the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.

7 Horizontal Blank End Bit 5

This bit is the sixth bit of the Horizontal Blank End Register (CR03).

VERTICAL TOTAL REGISTER (CR06)

Read/Write at I/O Address 3B5h/3D5h
Index 06h
Group 0 Protection



This register is used in all modes.

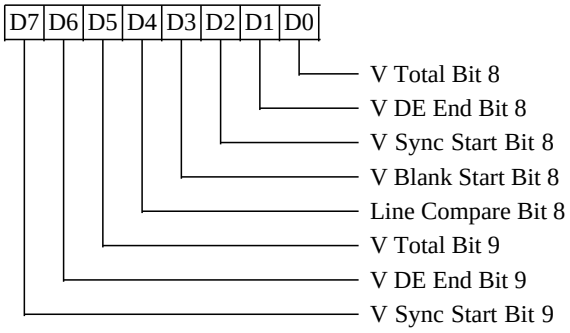
7-0 Vertical Total

These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow Register. The Vertical Total value specifies the total number of scan lines (horizontal retrace periods) per frame.

Programmed Count = Actual Count – 2

OVERFLOW REGISTER (CR07)

Read/Write at I/O Address 3B5h/3D5h
Index 07h
Group 0 Protection on bits 0-3 and bits 5-7
Group 3 Protection on bit 4



This register is used in all modes.

0 Vertical Total Bit 8

1 Vertical Display Enable End Bit 8

2 Vertical Sync Start Bit 8

3 Vertical Blank Start Bit 8

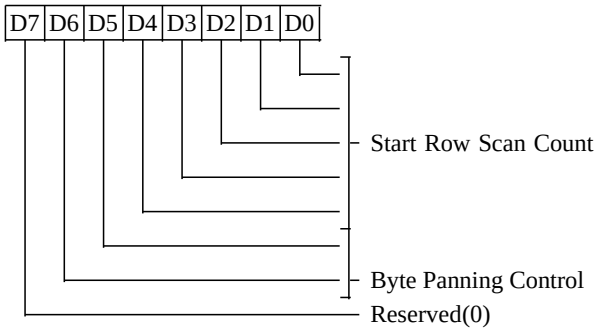
4 Line Compare Bit 8

5 Vertical Total Bit 9

6 Vertical Display Enable End Bit 9

7 Vertical Sync Start Bit 9

PRESET ROW SCAN REGISTER (CR08)
Read/Write at I/O Address 3B5h/3D5h
Index 08h
Group 3 Protection



4-0 Start Row Scan Count

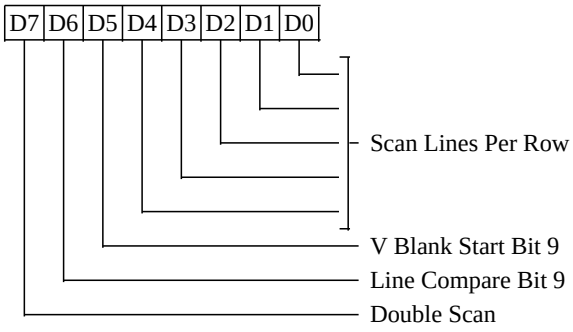
These bits specify the starting row scan count after each vertical retrace. Every horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count during active display. This register is used for soft scrolling in text modes.

6-5 Byte Panning Control

These bits specify the lower order bits for the display start address. They are used for horizontal panning in Odd/Even and Quad modes.

7 Reserved (0)

MAXIMUM SCAN LINE REGISTER (CR09)
Read/Write at I/O Address 3B5h/3D5h
Index 09h
Group 2 Protection on bits 0-4
Group 4 Protection on bits 5-7



4-0 Scan Lines Per Row

These bits specify the number of scan lines in a row:

Programmed Value = Actual Value – 1

5 Vertical Blank Start Register Bit 9

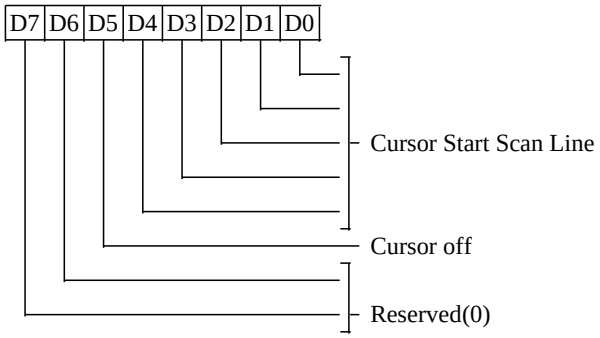
6 Line Compare Register Bit 9

7 Double Scan

0 NormalOperation
1 Enable scan line doubling

The vertical parameters in the CRT Controller (even for a split screen) are not affected, only the CRTC row scan counter (bits 0-4 of this register) and display memory addressing screen refresh are affected.

CURSOR START SCAN LINE REGISTER (CR0A)
Read/Write at I/O Address 3B5h/3D5h
Index 0Ah
Group 2 Protection



4-0 Cursor Start Scan Line

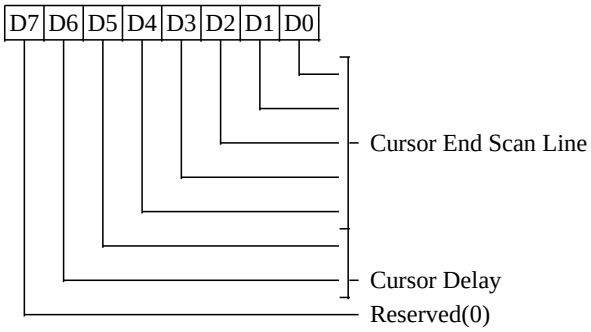
These bits specify the scan line of the character row where the cursor display begins.

5 Cursor Off

0 Text Cursor On
1 Text Cursor Off

7-6 Reserved (0)

CURSOR END SCAN LINE REGISTER (CR0B)
Read/Write at I/O Address 3B5h/3D5h
Index 0Bh
Group 2 Protection



4-0 Cursor End Scan Line

These bits specify the scan line of a character row where the cursor display ends (i.e., last scan line for the block cursor):

Programmed Value = Actual Value + 1

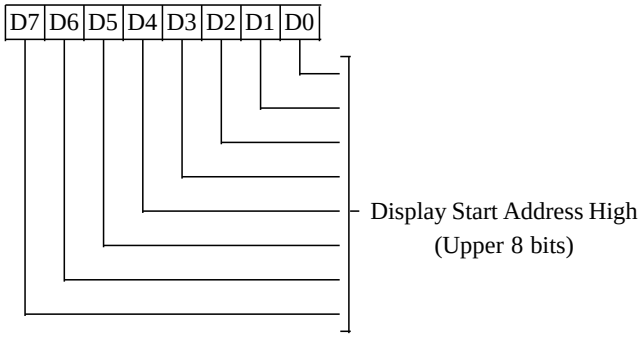
6-5 Cursor Delay

These bits define the number of character clocks that the cursor is delayed to compensate for internal pipeline delay.

7 Reserved (0)

Note: If the Cursor Start Line is greater than the Cursor End Line, then no cursor is generated.

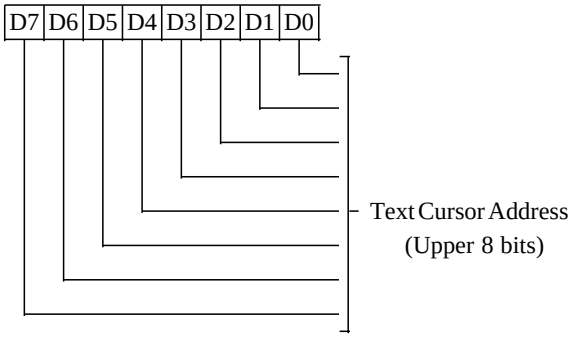
START ADDRESS HIGH REGISTER (CR0C)
Read/Write at I/O Address 3B5h/3D5h
Index 0Ch



7-0 Display Start Address High

This register contains the upper 8 bits of the display start address. In CGA / MDA / Hercules modes, this register wraps around at the 16K, 32K, and 64Kbyte boundaries respectively.

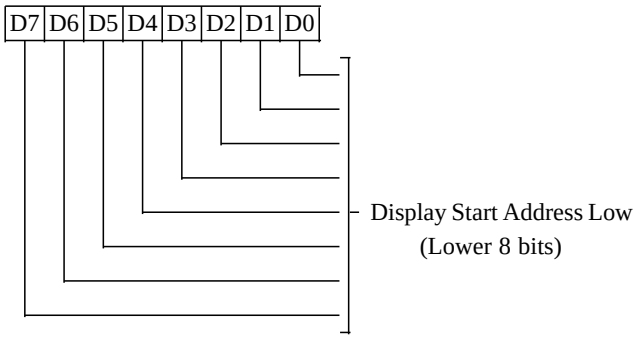
CURSOR LOCATION HIGH REGISTER (CR0E)
Read/Write at I/O Address 3B5h/3D5h
Index 0Eh



7-0 Text Cursor Location High

This register contains the upper 8 bits of the memory address where the text cursor is active. In CGA / MDA / Hercules modes, this register wraps around at 16K, 32K, and 64Kbyte boundaries respectively.

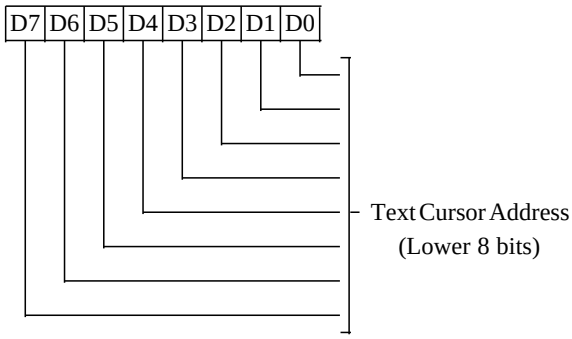
START ADDRESS LOW REGISTER (CR0D)
Read/Write at I/O Address 3B5h/3D5h
Index 0Dh



7-0 Display Start Address Low

This register contains the lower 8 bits of the display start address. The display start address points to the memory address corresponding to the top left corner of the screen.

CURSOR LOCATION LOW REGISTER (CR0F)
Read/Write at I/O Address 3B5h/3D5h
Index 0Fh



7-0 Text Cursor Location Low

This register contains the lower 8 bits of the memory address where the text cursor is active. In CGA / MDA / Hercules modes, this register wraps around at 16K, 32K, and 64Kbyte boundaries respectively.

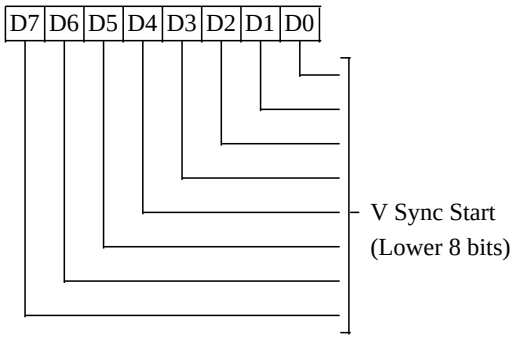
LIGHTPEN HIGH REGISTER (CR10)
Read only at I/O Address 3B5h/3D5h
Index 10h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

LIGHTPEN LOW REGISTER (CR11)
Read only at I/O Address 3B5h/3D5h
Index 11h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

VERTICAL SYNC START REGISTER (CR10)
Read/Write at I/O Address 3B5h/3D5h
Index 10h
Group 4 Protection

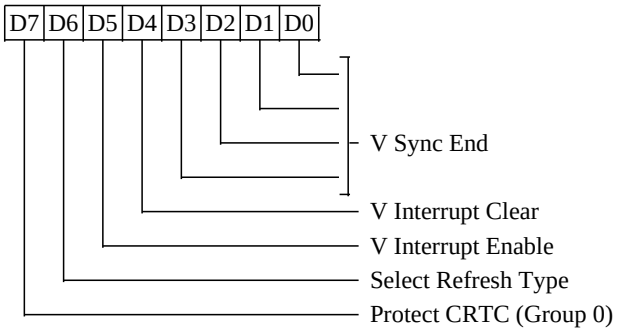


This register is used in all modes. This register is not readable in (Line Compare bit-9) MDA/Hercules emulation or when CR03 bit-7=1.

7-0 Vertical Sync Start

The eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRTC Overflow Register. They define the scan line position at which Vertical Sync becomes active.

VERTICAL SYNC END REGISTER (CR11)
Read/Write at I/O Address 3B5h/3D5h
Index 11h
Group 3 Protection for bits 4 and 5
Group 4 Protection for bits 0-3, 6, and 7



This register is used in all modes. This register is not readable in MDA/Hercules emulation or when CR03 bit-7=1.

3-0 Vertical Sync End

The lower 4 bits of the scan line count that defines the end of vertical sync. If the vertical sync width desired is N lines, then bits 3-0 of this register = (CR10 + N) AND 0Fh.

4 Vertical Interrupt Clear

0=Clear vertical interrupt generated on the IRQ output; 1=Normal operation. This bit is cleared by RESET.

5 Vertical Interrupt Enable

0 Enable vertical interrupt (default)
1 Disable vertical interrupt

This bit is cleared by RESET.

6 Select Refresh Type

0 3 refresh cycles per scan line
1 5 refresh cycles per scan line

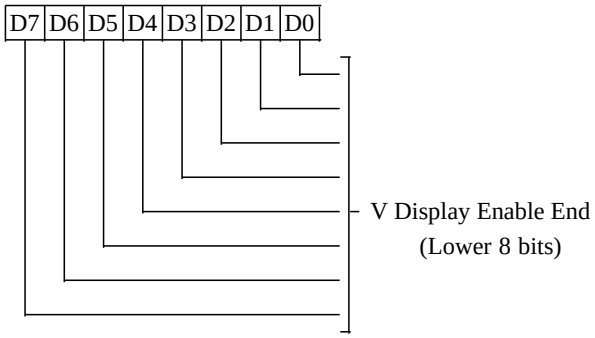
7 Group Protect 0

This bit is logically ORed with XR15 bit-6 to determine the protection for group 0 registers. This bit is cleared by RESET.

0 Enable writes to CR00-CR07
1 Disable writes to CR00-CR07

CR07 bit-4 (Line Compare bit-9) is not affected by this bit.

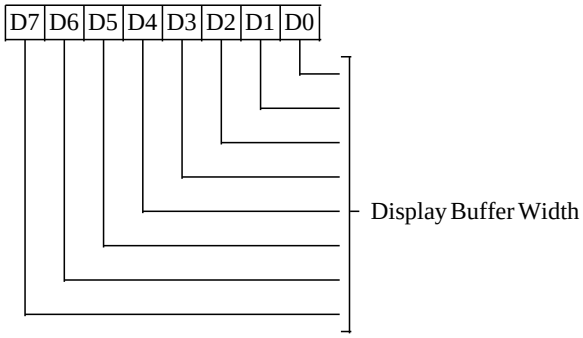
VERTICAL DISPLAY ENABLE END REGISTER (CR12)
Read/Write at I/O Address 3B5h/3D5h
Index 12h
Group 4 Protection



7-0 Vertical Display Enable End

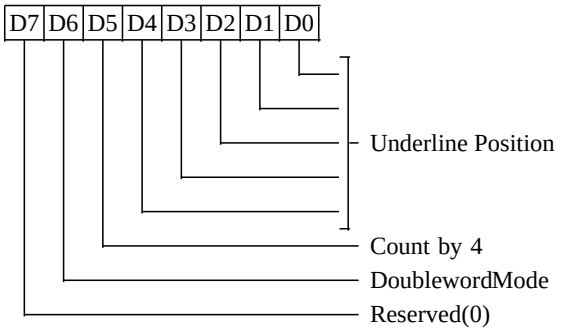
These are the eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow register. The actual count = Contents of this register + 1.

OFFSET REGISTER (CR13)
Read/Write at I/O Address 3B5h/3D5h
Index 13h
Group 3 Protection



7-0 Display Buffer Width. The byte starting address of the next display row = Byte Start Address for current row + K* (CR13 + Z/2), where Z = bit defined in XR0D, K = 2 in byte mode, and K = 4 in word mode. Byte, word and double word mode is selected by bit-6 of CR17 and bit-6 of CR14. A less significant bit than bit-0 of this register is defined in the Auxiliary Offset register (XR0D). This allows finer resolution of the bit map width. Byte, word and doubleword mode affects the translation of the 'logical' display memory address to the 'physical' display memory address.

UNDERLINE LOCATION REGISTER (CR14)
Read/Write at I/O Address 3B5h/3D5h
Index 14h
Group 3 Protection



4-0 Underline Position

These bits specify the underline's scan line position within a character row.

Programmed Value = Actual scan line number – 1

5 Count by 4 for Doubleword Mode

0 Frame Buffer Address is incremented by 1 or 2
1 Frame Buffer Address is incremented by 4 or 2

See CR17 bit-3 for further details.

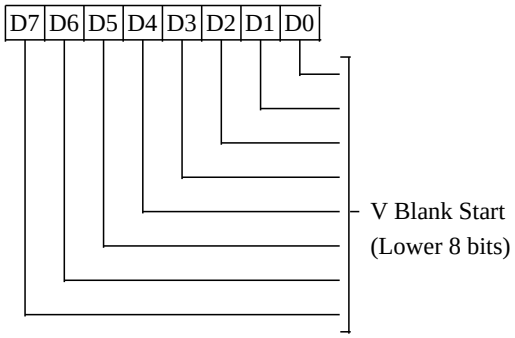
6 Doubleword Mode

0 Frame Buffer Address is byte or word address
1 Frame Buffer Address is doubleword address

This bit is used in conjunction with CR17 bit-6 to select the display memory addressing mode.

7 Reserved (0)

VERTICAL BLANK START REGISTER (CR15)
Read/Write at I/O Address 3B5h/3D5h
Index 15h
Group 4 Protection

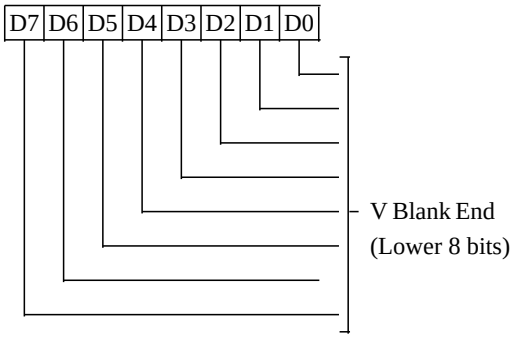


This register is used in all modes.

7-0 Vertical Blank Start

These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers respectively. Together these 10 bits define the scan line position where vertical blank begins. The interval between the end of the vertical display and the beginning of vertical blank is the bottom border on the screen.

VERTICAL BLANK END REGISTER (CR16)
Read/Write at I/O Address 3B5h/3D5h
Index 16h
Group 4 Protection



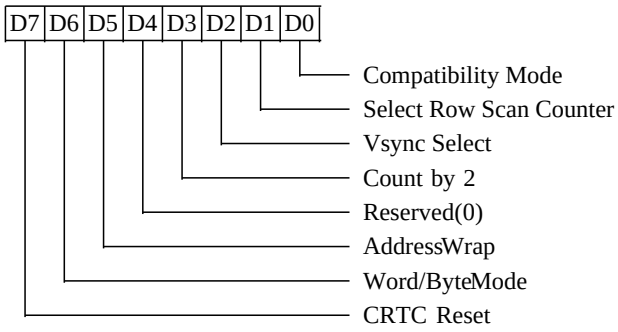
This register is used in all modes.

7-0 Vertical Blank End

These are the 8 low order bits of the scan line count which specifies the end of Vertical Blank. If the vertical blank width desired is Z lines these bits = (Vertical Blank Start + Z) and 0FFh.

CRT MODE CONTROL REGISTER (CR17)

Read/Write at I/O Address 3B5h/3D5h
Index 17h
Group 3 Protection for bits 0, 1, and 3-7
Group 4 Protection for bit 2



0 Compatibility Mode Support

This bit allows compatibility with the IBM CGA two-bank graphics mode.

0 Character row scan line counter bit 0 is substituted for memory address bit 13 during active display time
1 Normal operation, no substitution takes place

1 Select Row Scan Counter

This bit allows compatibility with Hercules graphics and with any other 4-bank graphics system.

0 Character row scan line counter bit 1 is substituted for memory address bit 14 during active display time
1 Normal operation, no substitution takes place

2 Vertical Sync Select

This bit controls the vertical resolution of the CRT Controller by permitting selection of the clock rate input to the vertical counters. When set to 1, the vertical counters are clocked by the horizontal retrace clock divided by 2.

3 Count By Two

0 Memory address counter is incremented every character clock
1 Memory address counter is incremented every two character clocks, used in conjunction with bit 5 of 0Fh.

Note: This bit is used in conjunction with CR14 bit-5. The net effect is as follows:

CR14 Bit-5	CR17 Bit-3	Increment Addressing Every
0	0	1 CCLK
0	1	2 CCLK
1	0	4 CCLK
1	1	2 CCLK

Note: In Hercules graphics and Hi-res CGA modes, address increments every two clocks.

4 Reserved (0)

5 Address Wrap (effective only in word mode)

0 Wrap display memory address at 16 Kbytes. Used in IBM CGA mode.
1 Normal operation (extended mode).

6 Word Mode or Byte Mode

0 Select Word Mode. In this mode the display memory address counter bits are shifted down by one, causing the most-significant bit of the counter to appear on the least-significant bit of the display memory address output
1 Select byte mode

Note: This bit is used in conjunction with CR14 bit-6 to select byte, word, or double word memory addressing as follows:

CR14 Bit-6	CR17 Bit-6	Addressing Mode
0	0	Word Mode
0	1	Byte Mode
1	0	Double Word Mode
1	1	Double Word Mode

Display memory addresses are affected as shown in the table on the following page.

7 CRTC Reset

0 Force HSYNC and VSYNC inactive. No other registers or outputs affected.
1 Normal Operation

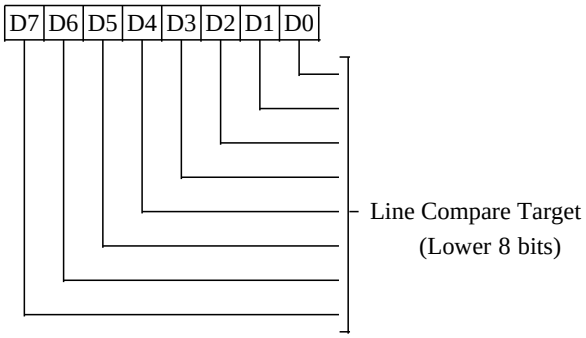
This bit is cleared by RESET.

Display memory addresses are affected by CR17 bit 6 as shown in the table below:

Logical Memory Address	Physical Memory Address Byte Mode	Word Mode	Double Word Mode
MA00	A00	Note 1	Note 2
MA01	A01	A00	Note 3
MA02	A02	A01	A00
MA03	A03	A02	A01
MA04	A04	A03	A02
MA05	A05	A04	A03
MA06	A06	A05	A04
MA07	A07	A06	A05
MA08	A08	A07	A06
MA09	A09	A08	A07
MA10	A10	A09	A08
MA11	A11	A10	A09
MA12	A12	A11	A10
MA13	A13	A12	A11
MA14	A14	A13	A12
MA15	A15	A14	A13

Note 1 = A13 * NOT CR17 bit 5
+ A15 * CR17 bit 5
Note 2 = A12 xor (A14 * XR04 bit 2)
Note 3 = A13 xor (A15 * XR04 bit 2)

LINE COMPARE REGISTER (CR18)
Read/Write at I/O Address 3B5h/3D5h
Index 18h
Group 3 Protection

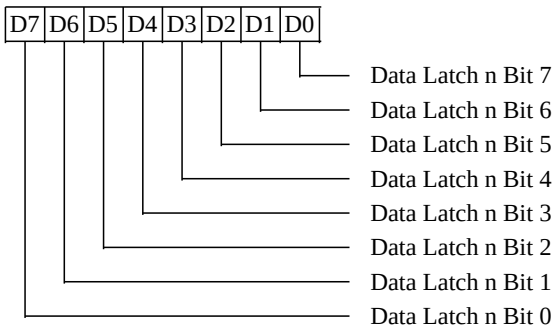


7-0 Line Compare Target

These are the low order 8 bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers, respectively. This register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address counter is cleared to 0. The display memory address counter then sequentially addresses the display memory starting at address 0. Each subsequent row address is generated by the addition of the Offset Register contents. This register is not affected by the double scanning bit (CR09 bit 7).

MEMORY DATA LATCH REGISTER (CR22)

Read only at I/O Address 3B5h/3D5h
Index 22h



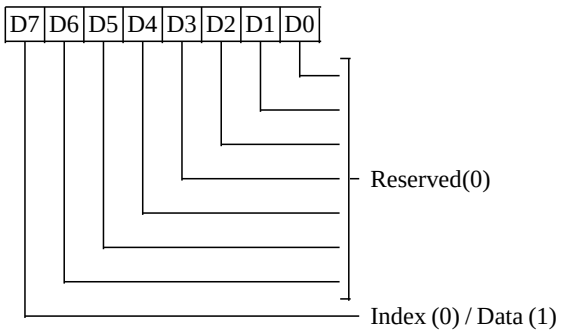
This register may be used to read the state of Graphics Controller Memory Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (GR04 bits 0–1) and is in the range 0–3.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

ATTRIBUTE CONTROLLER TOGGLE REGISTER (CR24)

Read only at I/O Address 3B5h/3D5h
Index 24h



6-0 Reserved (0)

7 Index/Data

This bit may be used to read back the state of the attribute controller index/data latch. This latch indicates whether the next write to the attribute controller at 3C0h will be to the register index pointer or to an indexed register.

0 Next write is to the index
1 Next write is to an indexed register

Writes to this register are not decoded and will be ignored.

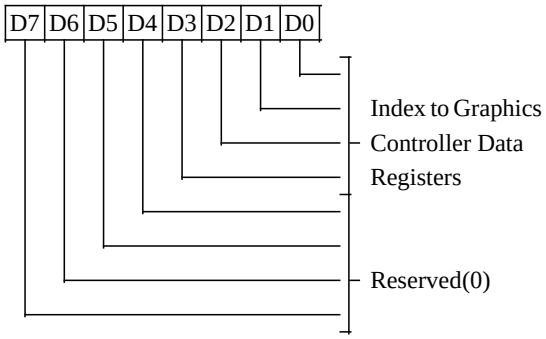
This is a standard VGA register which was not documented by IBM.

Graphics Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
GRX	Graphics Index	–	R/W	3CEh	1	65
GR00	Set/Reset	00h	R/W	3CFh	1	65
GR01	EnableSet/Reset	01h	R/W	3CFh	1	66
GR02	Color Compare	02h	R/W	3CFh	1	66
GR03	DataRotate	03h	R/W	3CFh	1	67
GR04	Read Map Select	04h	R/W	3CFh	1	67
GR05	Graphics mode	05h	R/W	3CFh	1	68
GR06	Miscellaneous	06h	R/W	3CFh	1	70
GR07	Color Don't Care	07h	R/W	3CFh	1	70
GR08	Bit Mask	08h	R/W	3CFh	1	71

GRAPHICS CONTROLLER INDEX REGISTER (GRX)

Write only at I/O Address 3CEh
Group 1 Protection

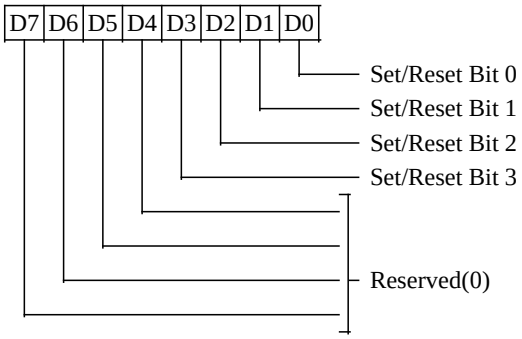


3-0 4-bit Index to Graphics Controller Registers

7-4 Reserved (0)

SET/RESET REGISTER (GR00)

Read/Write at I/O Address 3CFh
Index 00h
Group 1 Protection



The SET/RESET and ENABLE SET/RESET registers are used to 'expand' 8 bits of CPU data to 32 bits of display memory.

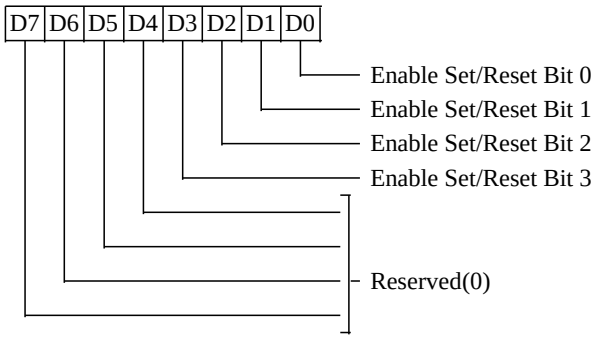
3-0 Set / Reset Planes 3-0

When the Graphics Mode register selects Write Mode 0, all 8 bits of each display memory plane are set as specified in the corresponding bit in this register. The Enable Set/Reset register (GR01) allows selection of some of the source of data to be written to individual planes. In Write Mode 3 (see GR05), these bits determine the color value.

7-4 Reserved (0)

ENABLE SET/RESET REGISTER (GR01)

Read/Write at I/O Address 3CFh
Index 01h
Group 1 Protection



3-0 Enable Set / Reset Planes 3-0

This register works in conjunction with the Set/Reset register (GR00). The Graphics Mode register must be programmed to Write Mode 0 in order for this register to have any effect.

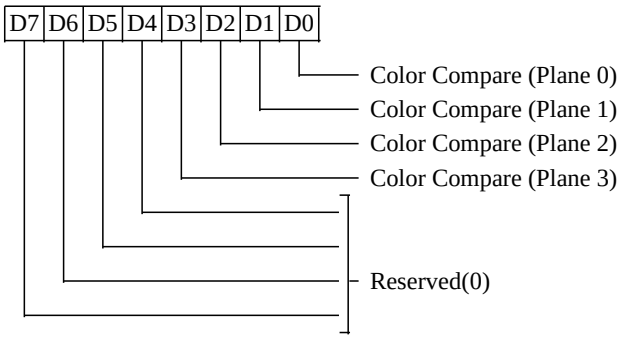
0 The corresponding plane is written with the data from the CPU data bus

1 The corresponding plane is set to 0 or 1 as specified in the Set/Reset Register

7-4 Reserved (0)

COLOR COMPARE REGISTER (GR02)

Read/Write at I/O Address 3CFh
Index 02h
Group 1 Protection



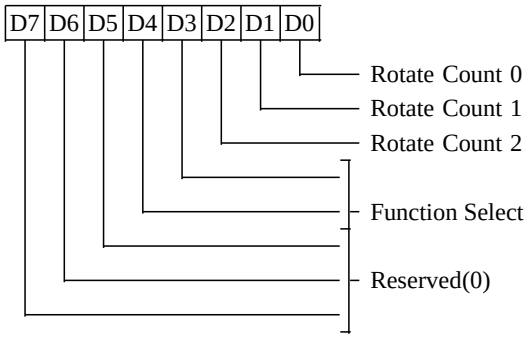
3-0 Color Compare Planes 3-0

This register is used to 'reduce' 32 bits of memory data to 8 bits for the CPU in 4-plane graphics mode. These bits provide a reference color value to compare to data read from display memory planes 0-3. The Color Don't Care register (GR07) is used to affect the result. This register is active only if the Graphics Mode register (GR05) is set to Read Mode 1. A match between the memory data and the Color Compare register (GR02) (for the bits specified in the Color Don't Care register) causes a logical 1 to be placed on the CPU data bus for the corresponding data bit; a mis-match returns a logical 0.

7-4 Reserved (0)

DATA ROTATE REGISTER (GR03)

Read/Write at I/O Address 3CFh
Index 03h
Group 1 Protection



2-0 Data Rotate Count

These bits specify the number of bits to rotate to the right the data being written by the CPU. The CPU data bits are first rotated, then subjected to the logical operation as specified in the Function Select bit field. The rotate function is active only if the Graphics Mode register is programmed for Write Mode 0.

4-3 Function Select

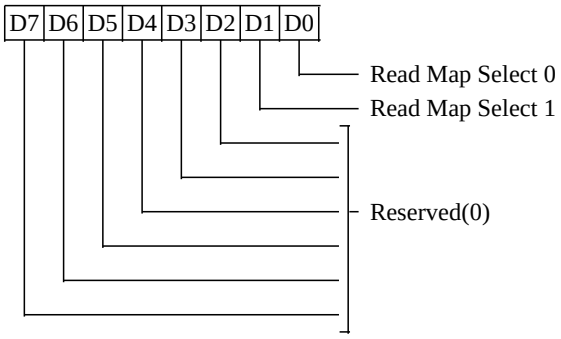
These Function Select bits specify the logical function performed on the contents of the processor latches (loaded on a previous CPU read cycle) before the data is written to display memory. These bits operate as follows:

Bit 4	Bit 3	Result
0	0	No change to the Data
0	1	Logical 'AND' between Data and latched data
1	0	Logical 'OR' between Data and latched data
1	1	Logical 'XOR' between Data and latched data

7-5 Reserved (0)

READ MAP SELECT REGISTER (GR04)

Read/Write at I/O Address 3CFh
Index 04h
Group 1 Protection



1-0 Read Map Select

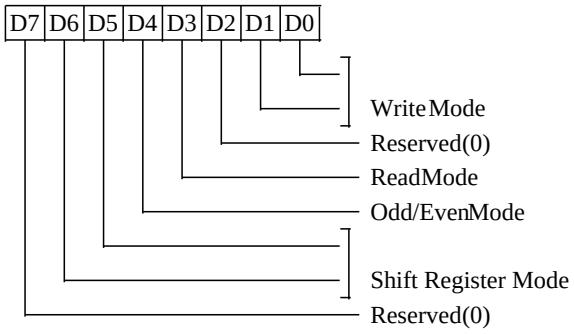
This register is also used to 'reduce' 32 bits of memory data to 8 bits for the CPU in the 4-plane graphics mode. These bits select the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even mode, bit-0 is ignored. In Quad mode, bits 0 and 1 are both ignored.

The four memory maps are selected as follows:

Bit 1	Bit 0	MapSelected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

7-2 Reserved (0)

GRAPHICS MODE REGISTER (GR05)
Read/Write at I/O Address 3CFh
Index 05h
Group 1 Protection



1-0 Write Mode

For 16-bit writes, the operation is repeated on the lower and upper bytes of CPU data.

1	0	Write Mode
0	0	**Write mode 0**. Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.
0	1	**Write mode 1**. Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.
1	0	**Write mode 2**. The CPU data bus data is treated as the color value for the addressed byte in planes 0-3. All eight pixels in the addressed byte are modified unless protected by the Bit Mask register setting. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset and Enable Set/Reset registers are ignored. The Function Select bits in the Data Rotate register are used.
1	1	**Write mode 3**. The CPU data is rotated then logically ANDed with the contents of the Bit Mask register (GR08) and then treated as the addressed data's bit mask, while the contents of the Set/Reset register is treated as the color value. A '0' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the corresponding pixel in the processor latches. A '1' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the color value specified in the Set/Reset register. The Enable Set/Reset register is ignored. The Data Rotate is used. This write mode can be used to fill an area with a single color and pattern.

2 Reserved (0)

3 Read Mode

0 The CPU reads data from one of the planes as selected in the Read Map Select register.

1 The CPU reads the 8-bit result of the logical comparison between all eight pixels in the four display planes and the contents of the Color Compare and Color Don't Care registers. The CPU reads a logical 1 if a match occurs for each pixel and logical 0 if a mis-match occurs. In 16-bit read cycles, this operation is repeated on the lower and upper bytes.

(Continued on following page)

4 Odd/Even Mode

0 All CPU addresses sequentially access all planes

1 Even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for compatibility with the IBM CGA memory organization.

6-5 Shift Register Mode

These two bits select the data shift pattern used when passing data from the four memory planes through the four video shift registers. If data bits 0-7 in memory planes 0-3 are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7 respectively, then the data in the serial shift registers is shifted out as follows:

65	Last Bit Shifted Out			Shift Direction →				1st Bit Shifted Out	Output to:
00:	M0D0	M0D1	M0D2	M0D3	M0D4	M0D5	M0D6	M0D7	Bit 0
	M1D0	M1D1	M1D2	M1D3	M1D4	M1D5	M1D6	M1D7	Bit 1
	M2D0	M2D1	M2D2	M2D3	M2D4	M2D5	M2D6	M2D7	Bit 2
	M3D0	M3D1	M3D2	M3D3	M3D4	M3D5	M3D6	M3D7	Bit 3
01:	M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	Bit 0
	M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	Bit 1
	M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	Bit 2
	M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	Bit 3
1x:	M3D0	M3D4	M2D0	M2D4	M1D0	M1D4	M0D0	M0D4	Bit 0
	M3D1	M3D5	M2D1	M2D5	M1D1	M1D5	M0D1	M0D5	Bit 1
	M3D2	M3D6	M2D2	M2D6	M1D2	M1D6	M0D2	M0D6	Bit 2
	M3D3	M3D7	M2D3	M2D7	M1D3	M1D7	M0D3	M0D7	Bit 3

Note: If the Shift Register is not loaded every character clock (see SR01 bits 2&4) then the four 8-bit shift registers are effectively 'chained' with the output of shift register 1 becoming the input to shift register 0 and so on. This allows one to have a large monochrome (or 4 color) bit map and display one portion thereof.

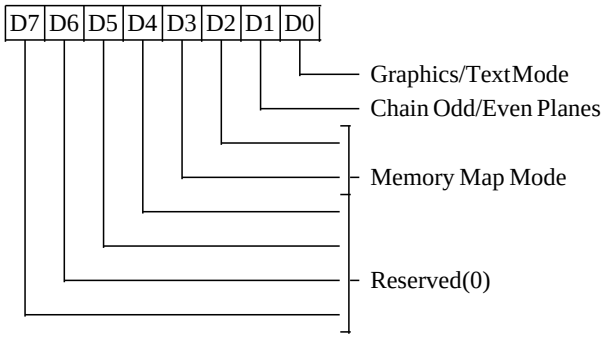
Note: If XR28 bit-4 is set (8-bit video path), GR05 bit-6 must be set to 0:

0x and XR28 bit-4=1:					
	M3D0	M2D0	M1D0	M0D0	Bit 0
	M3D1	M2D1	M1D1	M0D1	Bit 1
	M3D2	M2D2	M1D2	M0D2	Bit 2
	M3D3	M2D3	M1D3	M0D3	Bit 3
	M3D4	M2D4	M1D4	M0D4	Bit 4
	M3D5	M2D5	M1D5	M0D5	Bit 5
	M3D6	M2D6	M1D6	M0D6	Bit 6
	M3D7	M2D7	M1D7	M0D7	Bit 7

7 Reserved (0)

MISCELLANEOUS REGISTER (GR06)

Read/Write at I/O Address 3CFh
Index 06h
Group 1 Protection



0 Graphics/Text Mode

0 TextMode
1 Graphics mode

1 Chain Odd/Even Planes

This mode can be used to double the address space into display memory.

1 CPU address bit A0 is replaced by a higher order address bit. The state of A0 determines which memory plane is to be selected:

A0 = 0: select planes 0 and 2
A0 = 1: select planes 1 and 3

0 A0 not replaced

3-2 Memory Map Mode

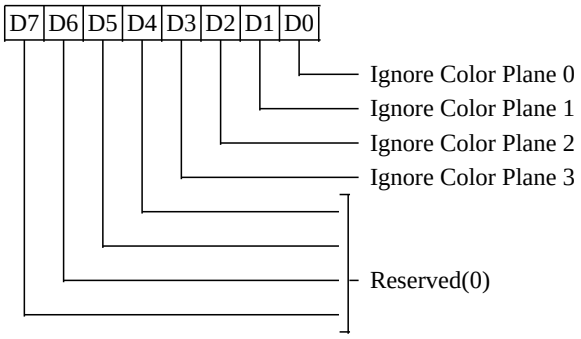
These bits control the mapping of the display memory into the CPU address space as follows (also used in extended modes):

Bit 3	Bit 2	CPU Address
0	0	A0000h-BFFFFh
0	1	A0000h-AFFFFh
1	0	B0000h-B7FFFh
1	1	B8000h-BFFFFh

7-4 Reserved (0)

COLOR DON'T CARE REGISTER (GR07)

Read/Write at I/O Address 3CFh
Index 07h
Group 1 Protection



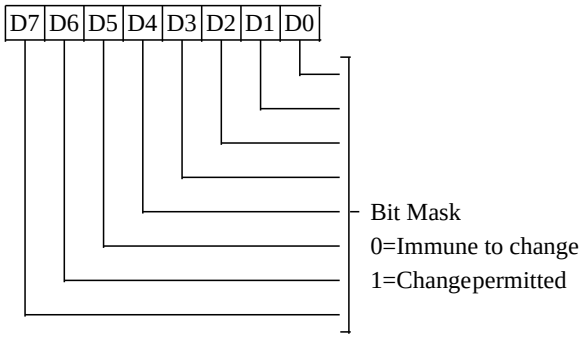
3-0 Ignore Color Plane (3-0)

0 This causes the corresponding bit of the Color Compare register to be a don't care during a comparison.

1 The corresponding bit of the Color Compare register is enabled for color comparison. This register is active in Read Mode 1 only.

7-4 Reserved (0)

BIT MASK REGISTER (GR08)
Read/Write at I/O Address 3CFh
Index 08h
Group 1 Protection



7-0 Bit Mask

This bit mask is applicable to any data written by the CPU, including that subject to a rotate, logical function (AND, OR, XOR), Set/Reset, and No Change. In order to execute a proper read-modify-write cycle into displayed memory, each byte must first be read (and latched by the VGA), the Bit Mask register set, and the new data then written. The bit mask applies to all four planes simultaneously.

0 The corresponding bit in each of the four memory planes is written from the corresponding bit in the latches

1 Unrestricted manipulation of the corresponding data bit in each of the four memory planes is permitted

Attribute Controller and VGA Color Palette Registers

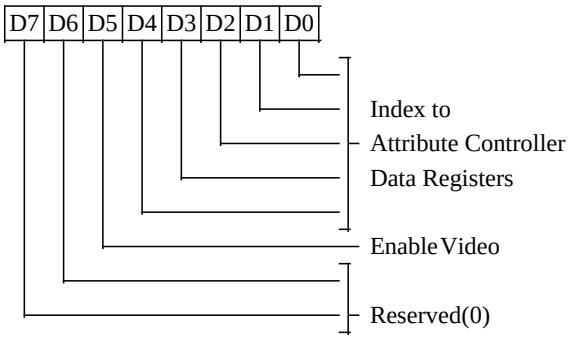
Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ARX	Attribute Index (for 3C0/3C1h)	–	R/W	3C0h	1	73
AR00-AR0F	Attribute Controller Color Data	00-0Fh	R/W	3C0h/3C1h	1	74
AR10	Mode Control	10h	R/W	3C0h/3C1h	1	74
AR11	Overscan Color	11h	R/W	3C0h/3C1h	1	75
AR12	Color Plane Enable	12h	R/W	3C0h/3C1h	1	75
AR13	Horizontal Pixel Panning	13h	R/W	3C0h/3C1h	1	76
AR14	Pixel Pad	14h	R/W	3C0h/3C1h	1	76
DACMASK	Color Palette Pixel Mask	–	R/W	3C6h	6	77
DACSTATE	Color Palette State	–	R	3C7h	–	77
DACRX	Color Palette Read-Mode Index	–	W	3C7h	6	78
DACX	Color Palette Index (for 3C9h)	–	R/W	3C8h	6	78
DACDATA	Color Palette Data	00-FFh	R/W	3C9h	6	78

In regular VGA mode, all Attribute Controller registers are located at the same byte address (3C0h) in the CPU I/O space. An internal flip-flop controls the selection of either the Attribute Index or Data Registers. To select the Index Register, an I/O Read is executed to address 3BAh/3DAh to clear this flip-flop. After the Index Register has been loaded by an I/O Write to address 3C0h, this flip-flop toggles, and the Data Register is ready to be accessed. Every I/O Write to address 3C0h toggles this flip-flop. The flip-flop does not have any effect on the reading of the Attribute Controller registers. The Attribute Controller index register is always read back at address 3C0h, the data register is always read back at address 3C1h.

In one of the extended modes (See "CPU Interface Register"), the Attribute Controller Index register is located at address 3C0h and the Attribute Controller Data register is located at address 3C1h (to allow word I/O accesses). In another extended mode, the Attribute Controller can be both read and written at either 3C0h or 3C1h (EGA compatible mode).

The VGA color palette logic is used to further modify the video color output following the attribute controller color registers. The color palette logic is contained on-chip, however an external color palette chip may still be used by disabling the internal color palette (see XR06). DAC logic is provided on-chip (or in the external 'RAMDAC' chip if used) to convert the final video output of the color palette to analog RGB outputs for use in driving a CRT display.

ATTRIBUTE INDEX REGISTER (ARX)
Read/Write at I/O Address 3C0h
Group 1 Protection



4-0 Attribute Controller Index

These bits point to one of the internal registers of the Attribute Controller.

5 Enable Video

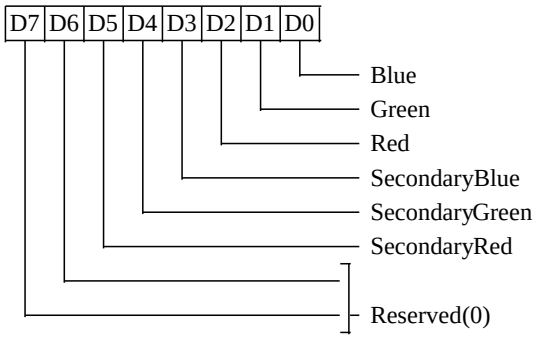
0 Disable video, allowing the Attribute Controller Color registers to be accessed by the CPU

1 Enable video, causing the Attribute Controller Color registers (AR00-AR0F) to be inaccessible to the CPU

7-6 Reserved (0)

ATTRIBUTE CONTROLLER COLOR REGISTERS (AR00-AR0F)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 00-0Fh
Group 1 Protection or XR63 bit-6



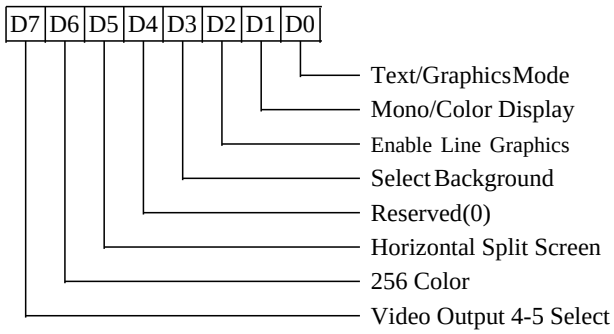
5-0 Color Value

These bits are the color value in the respective attribute controller color register as pointed to by the attribute index register.

7-6 Reserved (0)

ATTRIBUTE CONTROLLER MODE CONTROL REGISTER (AR10)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 10h
Group 1 Protection



0 Text/Graphics Mode

0 Select text mode
1 Select graphics mode

1 Monochrome/Color Display

0 Select color display attributes
1 Select mono display attributes

2 Enable Line Graphics Character Codes

This bit is dependent on bit 0 of the Override register.

0 Make the ninth pixel appear the same as the background

1 For special line graphics character codes (0C0h-0DFh), make the ninth pixel identical to the eighth pixel of the character. For other characters, the ninth pixel is the same as the background.

3 Enable Blink/Select Background Intensity

The blinking counter is clocked by the VSYNC signal. The Blink frequency is defined in the Blink Rate Control Register (XR60).

0 Disable Blinking and enable text mode background intensity

1 Enable the blink attribute in text and graphics modes.

4 Reserved (0)

5 Split Screen Horizontal Panning Mode

0 Scroll both screens horizontally as specified in the Pixel Panning register

1 Scroll horizontally only the top screen as specified in the Pixel panning register

6 256 Color Output Assembler

0 6-bits of video (translated from 4-bits by the internal color palette) are output every dot clock

1 Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot clock (256 color mode).

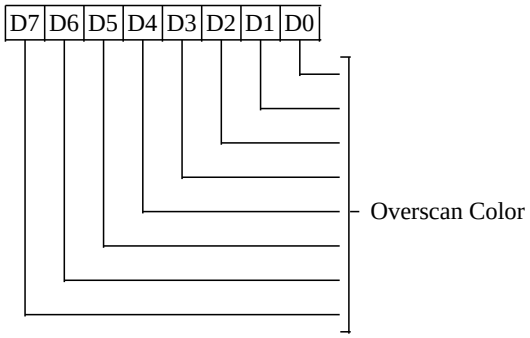
7 Video Output 5-4 Select

0 Video bits 4 and 5 are generated by the internal Attribute Controller color paletteregisters

1 Video bits 4 and 5 are the same as bits 0 and 1 in the Pixel Pad register (AR14)

OVERSCAN COLOR REGISTER (AR11)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 11H
Group 1 Protection



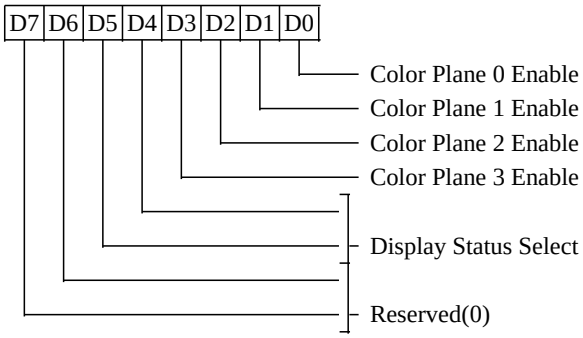
7-0 Overscan Color

These 8 bits define the overscan (border) color value. For monochrome displays, these bits should be zero.

The border color is displayed in the interval after Display Enable End and before Blank Start (end of display area; i.e. right side and bottom of screen) and between Blank End and Display Enable Start (beginning of display area; i.e. left side and top of screen).

COLOR PLANE ENABLE REGISTER (AR12)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 12h
Group 1 Protection



3-0 Color Plane (3-0) Enable

0 Force the corresponding color plane pixel bit to 0 before it addresses the colorpalette

1 Enable the plane data bit of the corresponding color plane to pass

5-4 Display Status Select

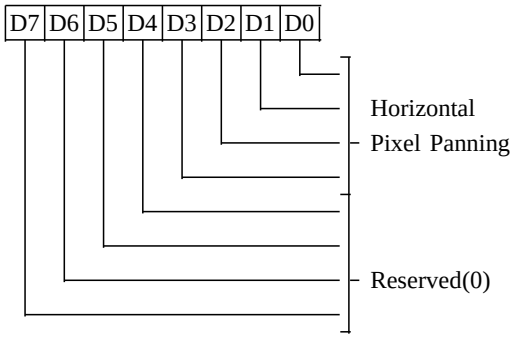
These bits select two of the eight color outputs to be read back in the Input Status Register 1 (port 3BAh or 3DAh). The output color combinations available on the status bits are as follows:

		Status Register 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

7-6 Reserved (0)

ATTRIBUTE CONTROLLER HORIZONTAL PIXEL PANNING REGISTER (AR13)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 13h
Group 1 Protection



3-0 Horizontal Pixel Panning

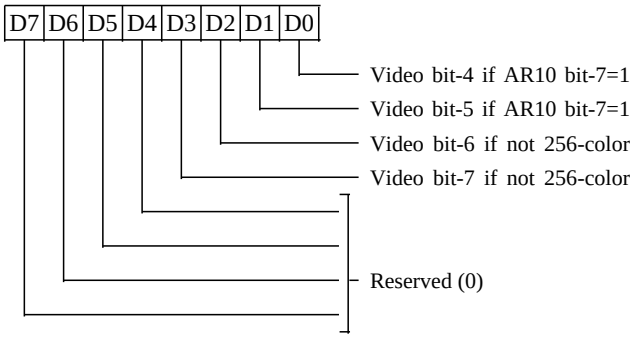
These bits select the number of pixels to shift the display horizontally to the left. Pixel panning is available in both text and graphics modes. In 9 pixel/character text mode, the output can be shifted a maximum of 9 pixels. In 8 pixel/character text mode and all graphics modes a maximum shift of 8 pixels is possible. In 256-color mode (output assembler AR10 bit-6 = 1), bit 0 of this register must be 0 which results in only 4 panning positions per display byte. In Shift Load 2 and Shift Load 4 modes, register CR08 provides single pixel resolution for panning. Panning is controlled as follows:

	Number of Pixels Shifted		
AR13	9-dot mode	8-dot mode	256-color mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7-4 Reserved (0)

ATTRIBUTE CONTROLLER PIXEL PAD REGISTER (AR14)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 14h
Group 1 Protection



1-0 Video Bits 5-4

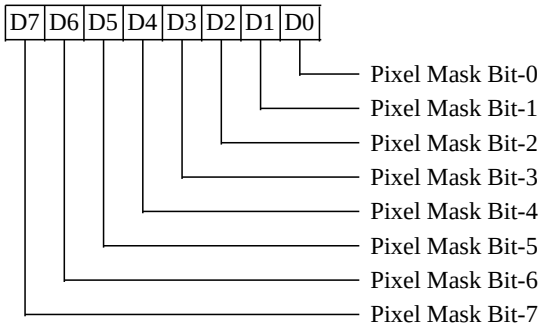
These bits are output as video bits 5 and 4 when AR10 bit-7 = 1. They are disabled in the 256 color mode.

3-2 Video Bits 7-6

These bits are output as video bits 7 and 6 in all modes except 256-color mode.

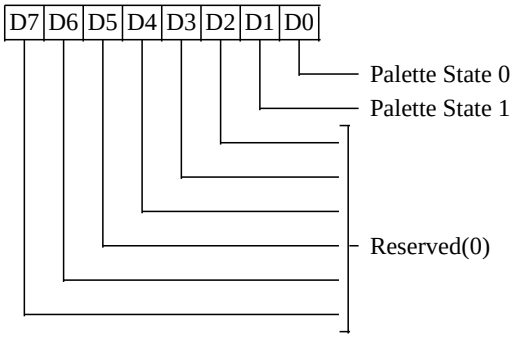
7-4 Reserved (0)

COLOR PALETTE
PIXEL MASK REGISTER (DACMASK)
Read/Write at I/O Address 3C6h
Group 6 Protection



The contents of this register are logically ANDed with the 8 bits of video data coming into the color palette. Zero bits in this register therefore cause the corresponding address input to the color palette to be zero. For example, if this register is programmed with 7, only color palette registers 0-7 would be accessible; video output bits 3-7 would be ignored and all color values would map into the lower 8 locations in the color palette.

COLOR PALETTE
STATE REGISTER (DACSTATE)
Read only at I/O Address 3C7h



1-0 Palette State 1-0

Status bits indicate the I/O address of the last CPU write to the Color Palette:

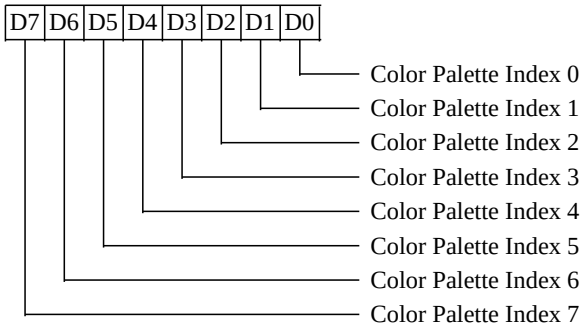
- 00 The last write was to 3C8h (write mode)
- 11 The last write was to 3C7h (read mode)

7-2 Reserved (0)

To allow saving and restoring the state of the video subsystem, this register is required since the color palette index register is automatically incremented differently depending on whether the index is written at 3C7h or 3C8h.

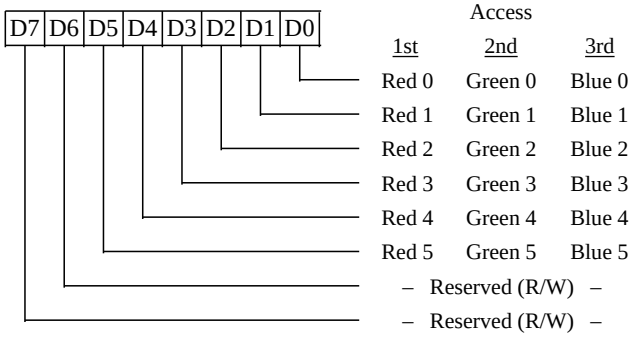
COLOR PALETTE
READ-MODE INDEX REGISTER (DACRX)
Write only at I/O Address 3C7h
Group 6 Protection

COLOR PALETTE
INDEX REGISTER (DACX)
Read/Write at I/O Address 3C8h
Group 6 Protection



There is only one palette index register. There are two ports used to access it (3C7h and 3C8h), however, and the action taken by the chip is different depending on which port is used for the access. The nature of this difference is in the auto-incrementation of the index register. Refer to the explanation at right under the Palette Data Register for additional details.

COLOR PALETTE
DATA REGISTERS (DACDATA 00-FF)
Read/Write at I/O Address 3C9h
Index 00h-FFh
Group 6 Protection



The palette index register points to one of 256 data registers. Each data register is 18 bits in length (6 bits each for red, green, and blue), so data values must be read as a sequence of 3 bytes. After writing the index register (3C7h or 3C8h), data values may be read from or written to the palette data port (3C9h) in sequence: first red, then green, then blue, then repeat for the next location if desired (the index is incremented automatically by the palette logic).

The index may be written at 3C7h and read or written at 3C8h. When the index value is written to either port, it is written to both the index register and a 'save' register. The save register (not the index register) is used by the palette logic to point to the current data register. When the index value is written to 3C7h (**read mode**), it is written to both index and save registers, then the index register is automaticallyincremented. When the index value is written to 3C8h (**write mode**), the automatic incrementing of the index register does not occur.

After the third of the three sequential data reads from (or writes to) 3C9h is completed, the save and index registers are both automatically incremented by the palette logic. This allows the entire palette (or any subset) to be read (written) by writing the index of the first color in the set, then sequentially reading (writing) values for each color, without having to reload the index every three bytes.

The state of the RGB sequence is not saved; the user must access each three bytes in an uninterruptible sequence (or be assured that interrupt service will not access the palette index or data registers). When the index register is written (at either port), the RGB sequence is restarted. Data reads and writes may be intermixed; either reads or writes increment the palette logic's RGB sequence counter.

The palette's save register always contains a value one less than the readable index value if the last index write was to the 'read mode' port. The state is saved for which port (3C7h or 3C8h) was last written and that information is returned on reads from 3C7h.

Extension Registers

Register Mnemonic	Register Group	Extension Register Name	Index	I/O Access	Address	State After Reset	Page
XRX	--	Extension Index	--	R/W	3D6h	- x x x x x x x	81
XR00	Misc	Chip Version	00h	RO	3D7h	1 1 0 0 r r r r	81
XR01	Misc	Configuration	01h	RO	3D7h	d d d d d d d d	82
XR02	Misc	CPU Interface Control 1	02h	R/W	3D7h	0 0 0 0 0 - 0 0	83
XR03	Misc	CPU Interface Control 2	03h	R/W	3D7h	• • 0 0 • • 1 0	83
XR04	Misc	Memory Control 1	04h	R/W	3D7h	- 0 0 - - 0 0 0	84
XR05	Misc	Memory Control 2	05h	R/W	3D7h	• 0 • 0 0 0 0 0	84
XR06	Misc	Palette Control	06h	R/W	3D7h	0 0 0 0 0 0 0 0	85
XR0E	Misc	Text Mode Control	0Eh	R/W	3D7h	- - - - 0 0 - -	87
XR28	Misc	Video Interface	28h	R/W	3D7h	0 0 0 0 - - 0 -	98
XR29	Misc	Half-Line Compare	29h	R/W	3D7h	x x x x x x x x	98
XR70	Misc	Setup / Disable Control	70h	R/W	3D7h	0 - - - - - - -	130
XR72	Misc	External Device I/O	72h	R/W	3D7h	0 0 0 0 0 0 0 0	131
XR73	Misc	DPMS Control	73h	R/W	3D7h	- - - - 0 0 0 0	132
XR7F	Misc	Diagnostic	7Fh	R/W	3D7h	0 0 x x x x 0 0	133
XR08	Mapping	Linear Addressing Base	08h	R/W	3D7h	x x x x x • • •	85
XR0B	Mapping	CPU Paging	0Bh	R/W	3D7h	- - 0 0 - 0 0 0	86
XR0C	Mapping	Start Address Top	0Ch	R/W	3D7h	- - - - - - x x	86
XR10	Mapping	Single/Low Map	10h	R/W	3D7h	x x x x x x x x	89
XR11	Mapping	High Map	11h	R/W	3D7h	x x x x x x x x	89
XR0F	Software Flags	Software Flags 0	0Fh	R/W	3D7h	x x x x x x x x	88
XR2B	Software Flags	Software Flags 1	2Bh	R/W	3D7h	0 0 0 0 0 0 0 0	99
XR44	Software Flags	Software Flags 2	44h	R/W	3D7h	x x x x x x x x	108
XR45	Software Flags	Software Flags 3	45h	R/W	3D7h	x x x x x x x x	108
XR14	Compatibility	Emulation Mode	14h	R/W	3D7h	0 0 0 0 h h 0 0	90
XR15	Compatibility	Write Protect	15h	R/W	3D7h	0 0 0 0 0 0 0 0	91
XR1F	Compatibility	Virtual EGA Switch	1Fh	R/W	3D7h	0 - - - x x x x	96
XR7E	Compatibility	CGA/Hercules Color Select	7Eh	R/W	3D7h	- - x x x x x x	133
XR30	Clock	Clock Divide Control	30h	R/W	3D7h	• • • • x x x x	102
XR31	Clock	Clock M-Divisor	31h	R/W	3D7h	• x x x x x x x	102
XR32	Clock	Clock N-Divisor	32h	R/W	3D7h	• x x x x x x x	103
XR33	Clock	Clock Control	33h	R/W	3D7h	• 0 0 0 • 0 • •	104
XR3A	MultiMedia	Color Key 0	3Ah	R/W	3D7h	x x x x x x x x	105
XR3B	MultiMedia	Color Key 1	3Bh	R/W	3D7h	x x x x x x x x	105
XR3C	MultiMedia	Color Key 2	3Ch	R/W	3D7h	x x x x x x x x	106
XR3D	MultiMedia	Color Key Mask 0	3Dh	R/W	3D7h	x x x x x x x x	106
XR3E	MultiMedia	Color Key Mask 1	3Eh	R/W	3D7h	x x x x x x x x	107
XR3F	MultiMedia	Color Key Mask 2	3Fh	R/W	3D7h	x x x x x x x x	107

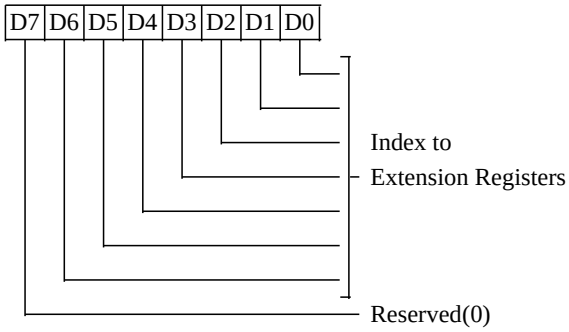
Reset Codes:
x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
r = Chip revision # (starting from 0000)
– = Not implemented (always reads 0)
• = Reserved (read/write, reset to 0)
0/1 = Reset to 0 or 1 by falling edge of RESET

Extension Registers

Register Mnemonic	Register Group	Extension Register Name	Index	I/O Access	Address	State After Reset	Page
XR0D	Alternate	Auxiliary Offset	0Dh	R/W	3D7h	- - - - - - x x	87
XR16	Alternate	Vertical Overflow	16h	R/W	3D7h	• 0 • 0 • 0 0 0	92
XR17	Alternate	Horizontal Overflow	17h	R/W	3D7h	• 0 0 0 0 0 0 0	92
XR18	Alternate	Alternate Horizontal Display End	18h	R/W	3D7h	x x x x x x x x	93
XR19	Alternate	Alternate H Sync Start	19h	R/W	3D7h	x x x x x x x x	93
XR1A	Alternate	Alternate Horizontal Sync End	1Ah	R/W	3D7h	x x x x x x x x	94
XR1B	Alternate	Alternate Horizontal Total	1Bh	R/W	3D7h	x x x x x x x x	94
XR1C	Alternate	Alternate H Blank Start / H Panel Size	1Ch	R/W	3D7h	x x x x x x x x	95
XR1D	Alternate	Alternate Horizontal Blank End	1Dh	R/W	3D7h	0 x x x x x x x	95
XR1E	Alternate	Alternate Offset	1Eh	R/W	3D7h	x x x x x x x x	96
XR24	Alternate	Alternate Maximum Scan Line	24h	R/W	3D7h	• • • x x x x x	97
XR25	Alternate	Alternate Text Mode H Virtual Panel Size	25h	R/W	3D7h	x x x x x x x x	97
XR26	Alternate	Alternate Horizontal Sync Start Register	26h	R/W	3D7h	x x x x x x x x	97
XR64	Alternate	Alternate Vertical Total	64h	R/W	3D7h	x x x x x x x x	126
XR65	Alternate	Alternate Overflow	65h	R/W	3D7h	x x x • • x x x	126
XR66	Alternate	Alternate Vertical Sync Start	66h	R/W	3D7h	x x x x x x x x	127
XR67	Alternate	Alternate Vertical Sync End	67h	R/W	3D7h	• • • • x x x x	127
XR2C	Flat Panel	FLM Delay	2Ch	R/W	3D7h	x x x x x x x x	99
XR2D	Flat Panel	LP Delay (Comp Disabled)	2Dh	R/W	3D7h	x x x x x x x x	100
XR2E	Flat Panel	LP Delay (Comp Enabled)	2Eh	R/W	3D7h	x x x x x x x x	100
XR2F	Flat Panel	LP Width	2Fh	R/W	3D7h	x x x x x x x x	101
XR4F	Flat Panel	Panel Format Register 2	4Fh	R/W	3D7h	x x • • • x x x	109
XR50	Flat Panel	Panel Format Register 1	50h	R/W	3D7h	x x x x x x x x	110
XR51	Flat Panel	Display Type	51h	R/W	3D7h	0 0 0 • 0 0 0 0	111
XR52	Flat Panel	Power Down Control	52h	R/W	3D7h	0 0 0 0 0 0 0 0	112
XR53	Flat Panel	Panel Format Register 3	53h	R/W	3D7h	• 0 0 0 0 0 x 0	113
XR54	Flat Panel	Panel Interface	54h	R/W	3D7h	x x x x x x x x	114
XR55	Flat Panel	Horizontal Compensation	55h	R/W	3D7h	x x x • • x x x	115
XR56	Flat Panel	Horizontal Centering	56h	R/W	3D7h	x x x x x x x x	116
XR57	Flat Panel	Vertical Compensation	57h	R/W	3D7h	x x x x x x x x	117
XR58	Flat Panel	Vertical Centering	58h	R/W	3D7h	x x x x x x x x	118
XR59	Flat Panel	Vertical Line Insertion	59h	R/W	3D7h	x x x • x x x x	118
XR5A	Flat Panel	Vertical Line Replication	5Ah	R/W	3D7h	• • • • x x x x	119
XR5B	Flat Panel	Panel Power Sequencing Delay	5Bh	R/W	3D7h	1 0 0 0 0 0 0 1	119
XR5C	Flat Panel	Activity Timer Control	5Ch	R/W	3D7h	0 x • x x x x x	120
XR5D	Flat Panel	FP Diagnostic	5Dh	R/W	3D7h	0 0 0 0 0 0 0 0	121
XR5E	Flat Panel	M (ACDCLK) Control	5Eh	R/W	3D7h	x x x x x x x x	122
XR5F	Flat Panel	Power Down Mode Refresh	5Fh	R/W	3D7h	x x x x x x x x	122
XR60	Flat Panel	Blink Rate Control	60h	R/W	3D7h	1 0 0 0 0 0 1 1	123
XR61	Flat Panel	SmartMap™ Control	61h	R/W	3D7h	x x x x x x x x	124
XR62	Flat Panel	SmartMap™ Shift Parameter	62h	R/W	3D7h	x x x x x x x x	125
XR63	Flat Panel	SmartMap™ Color Mapping Control	63h	R/W	3D7h	x 1 x x x x x x	125
XR68	Flat Panel	Vertical Panel Size	68h	R/W	3D7h	x x x x x x x x	128
XR6C	Flat Panel	Programmable Output Drive	6Ch	R/W	3D7h	• • 0 0 0 0 d •	128
XR6E	Flat Panel	Polynomial FRC Control	6Eh	R/W	3D7h	1 0 1 1 1 1 0 1	129
XR6F	Flat Panel	Frame Buffer Control	6Fh	R/W	3D7h	0 • • • • • 0 0	129

Reset Codes:
x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
r = Chip revision # (starting from 0000)
– = Not implemented (always reads 0)
• = Reserved (read/write, reset to 0)
0/1 = Reset to 0 or 1 by falling edge of RESET

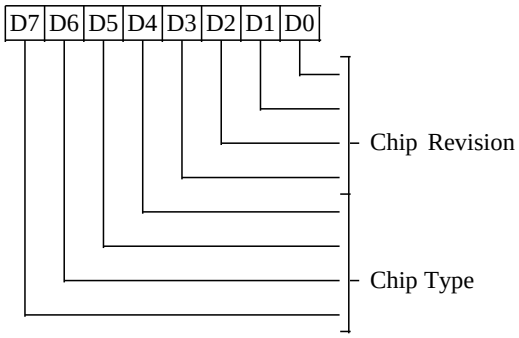
EXTENSION INDEX REGISTER (XRX)
Read/Write at I/O Address 3D6h



6-0 Index value used to access the extension registers

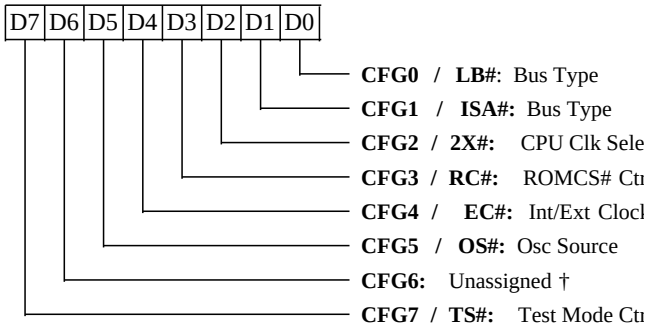
7 Reserved (0)

CHIPS VERSION REGISTER (XR00)
Read only at I/O Address 3D7h
Index 00h



7-0 **Chip Version** - Chip Versions start at C0h and are incremented for every silicon step.

CONFIGURATION REGISTER (XR01)
Read only at I/O Address 3D7h
Index 01h



These bits latch the state of memory address bus A (AA bus) bits 0-7 on the falling edge of RESET. The state of bits 0-7 after RESET effect chip internal logic as indicated below. During RESET, internal pullups are enabled for AA[7:0] and hence the status of these bits will be high if no external pull-down resistors are present on these pins.

This register is not related to the Virtual EGA Switch register (XR1F).

1-0 CFG1:0 - CPU Bus Type

00 Reserved
01 ISA bus
10 Force Local bus. The state of IOCS16#, MCS16#, and ZWS# pins during RESET determines the bus type as follows:

BCFG2 Pin 40 IOCS16#	BCFG1 Pin 39 MCS16#	BCFG0 Pin 38 ZWS#	Bus Type	CCLK
L	x	x	Reserved	–
H	L	L	386-32	2x
H	L	H	386-16	2x
H	H	L	486-32	1x/2x
H	H	H	486-16	1x/2x

11 Autoselect. If ALE is low at RESET, then ISA bus is selected otherwise Local bus is selected per BFG2-0 as shown in the table above.

Internal pull-ups are enabled on the IOCS16#, MCS16#, and ZWS# pins when RESET is active. When RESET goes low, the IOCS16# pin is tri-stated for local buses and the MCS16# and ZWS# pins are Tri-Stated for local buses except 486-16. When CCLK = 2x, pipeline mode is detected automatically, and when CCLK = 1x, pipeline mode is disabled. When the 486 Local Bus interface is selected (BCFG2-0=110 or 111) and XR01[2]=0, the functions of RDY (pin 37) and MEMW# (pin 34) are redefined as:

BCFG 2 1 0	XR01[2] LB Clk Select	Pin 34 MEMW#	Pin 37 RDY
1 1 0	0	CPURST	LRDY#
1 1 1	0	CPURST	LRDY#

2 CFG2 - Local Bus CPU Clock Select

0 2x CPU Clock is input to the 65535 on the CCLK pin
1 1x CPU Clock is input to the 65535 on CCLK pin

This bit is meaningful for 386 / 486 local bus only and is ignored for other buses.

3 CFG3 - ROMCS# / ZWS# Select †

0 ROMCS# output on ZWS# (pin 38)
1 ZWS# output on ZWS# pin (pin 38)

This bit is meaningful for ISA bus only. It is ignored for other buses (pin 38 has other defined functions). Note that pin 38 can also be defined as an IRQ output (over-riding the setting of this bit) via XR72 bit-0.

4 CFG4 - Internal / External Clock Select

0 External Clock Chip (pin 6 ADDHI = VCLK in, pin 155 XTALI = MCLK in, & GPIO0-1=CLKSEL0-1 out)
1 Internal Clock Synthesis (pin 6 functions as ADDHI)

5 CFG5 - Oscillator Source Select

0 External Clock drives XTALI pin 155
1 Series resonant Crystal connected to XTALI and XTALO (pins 155-156)

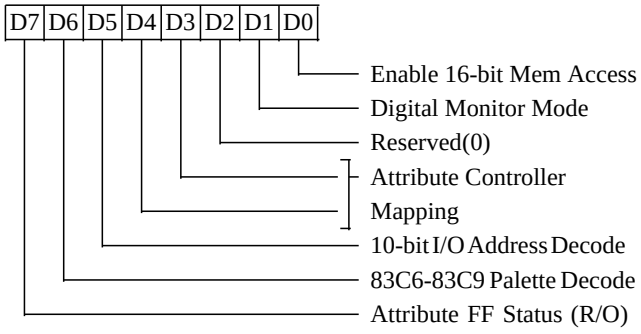
6 CFG 6 - Unassigned †

7 CFG7 - Clock Core Test Mode Control

0 Enable clock core test mode. Output MCLK on A23 (pin 5) and VCLK on ADDHI (pin 6)
1 Disable clock core test mode

† CHIPS' BIOS supports a feature which allows 'hardware' selection of one of four panels via a 2-bit code presented on CFG3 and CFG6. This feature is usable in local bus mode only since CFG3 has a defined hardware function in ISA bus mode.

CPU INTERFACE CTRL REGISTER 1 (XR02)
Read/Write at I/O Address 3D7h
Index 02h



0 8 / 16-bit CPU Memory Access
- 0 8-bit CPU memory access (default)
- 1 16-bit CPU memory access

1 Digital Monitor Clock Mode
- 0 Normal (clk 0-1=25,28 MHz) (default)
- 1 Digital Monitor (clk 0-1=14,16MHz) 14MHz = 56MHz ÷ 4 or 28MHz ÷ 2 16MHz = 50MHz ÷ 3

2 Reserved (0)

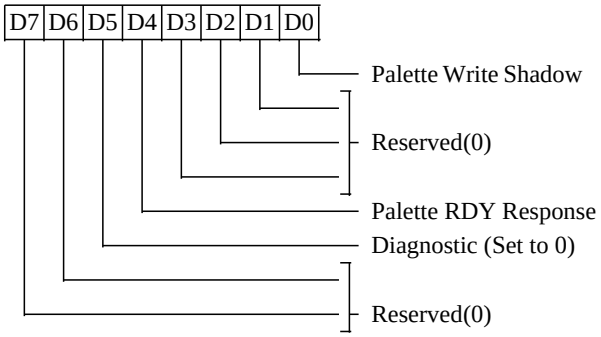
4-3 Attribute Controller Mapping
- 00 Write Index and Data at 3C0h. (8-bit access only) (default - VGA mapping)
- 01 Write Index at 3C0h and Data at 3C1h (8-bit or 16-bit access). Attribute flip-flop (bit-7) is always reset in this mode (16-bit mapping)
- 10 Write Index and Data at 3C0h/3C1h (8-bit access only) (EGA mapping)
- 11 Reserved

5 I/O Address Decoding
- 0 Decode all 16 bits of I/O address (default)
- 1 Decode only lower 10 bits of I/O address. This affects the following addresses: 3B4h, 3B5h, 3B8h, 3BAh, 3BFh, 3C0h, 3C1h, 3C2h, 3C4h, 3C5h, 3CEh, 3CFh, 3D4h, 3D5h, 3D8h, 3D9h, and 3DAh.

6 Palette Address Decoding
- 0 External palette registers can be accessed only at 3C6h-3C9h (default)
- 1 External palette registers can be accessed at both 3C6h-3C9h and 83C6h-83C9h (for Brooktree-type palette chips)

7 Attribute Flip-Flop Status (read only)
0 = Index, 1 = Data

CPU INTERFACE CTRL REGISTER 2 (XR03)
Read/Write at I/O Address 3D7h
Index 03h



0 Palette Write Shadow
- 0 Chip responds normally to Palette Write accesses (LDEV# is returned for VL-Bus accesses)
- 1 Palette write commands are executed internally but the chip does not respond externally (LDEV# is not returned for VL-Bus accesses). This conforms to VL-Bus "Palette Shadowing" requirements as it forces the access to be passed on to the ISA bus where add-in cards may be shadowing the VGA color palette data. This bit should normally be set to 1.

3-1 Reserved (0)

4 ISA Bus Palette Access RDY Response
- 0 Hold off the CPU using RDY for palette accesses (read or write to 3C6-3C9h).
- 1 Do not hold off the CPU using RDY for palette accesses (read or write to 3C6-3C9h)

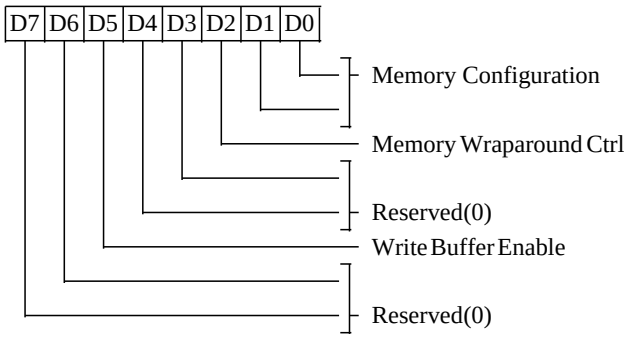
The internal RAMDAC has a minimum specification for time between accesses. A faster CPU is more likely to violate this specification, so it is normally required to add delay between accesses in software. This bit may be set to 0 to effectively create a CPU-transparent delay, however this is not compatible with some systems: some systems ignore RDY for palette accesses, so for those systems, this bit must be set to 1.

5 Diagnostic (R/W but should be set to 0)

7-6 Reserved (0)

MEMORY CONTROL REGISTER 1 (XR04)

Read/Write at I/O Address 3D7h
Index 04h



1-0 Memory Configuration

00 32-bit memory data path. Memory data bus is on MAD15-0 & MBD15-0.
01 16-bit data path. The memory data bus is on MAD15-0.
10 Reserved
11 Reserved

2 Memory Wraparound Control

This bit enables bits 16-17 of the CRT Controller address counter (default = 0 on reset).

0 Disable CRTC addr counter bits 16-17
1 Enable CRTC addr counter bits 16-17

4-3 Reserved (0)

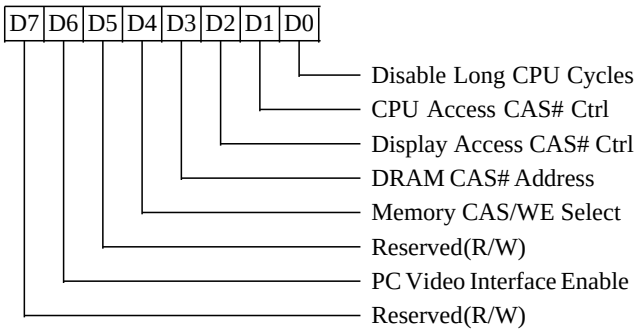
5 CPU Memory Write Buffer

0 Disable CPU memory write buffer (default)
1 Enable CPU memory write buffer

7-6 Reserved (0)

Memory Control Register 2 (XR05)

Read/Write at I/O Address 3D7h
Index 05h



0 Disable Long CPU Cycles

0 Enable long CPU cycles to put as many CPU cycles as possible into one RAS cycle (default)
1 Disable long CPU cycles

1 CPU Memory Access CAS# Cycle Control
2 Display Memory Access CAS# Cycle Cntrl

Bit-1 affects CPU accesses to display memory. Bit-2 affects accesses to display memory initiated by the 65535 for display refresh. Both bits are defined as follows:

0 3-MCLK CAS# cycle (2 low, 1 high) for all read or write accesses (default)
1 4-MCLK CAS# cycle (3 low, 1 high) for all read accesses and for the first CAS# cycle of page-mode write accesses (following cycles are 2L/1H)

These bits may be set to create looser memory timing (e.g., for 3.3V operation, to allow use of cheaper DRAMs, etc.).

3 DRAM CAS# Address for Display Memory

0 9-bit CAS address symmetric DRAM
1 8-bit CAS address asymmetric DRAM

4 CAS#/WE# Select for Display Memory

0 2CAS# / 1WE# DRAM used (default)
1 1CAS# / 2WE# DRAM used

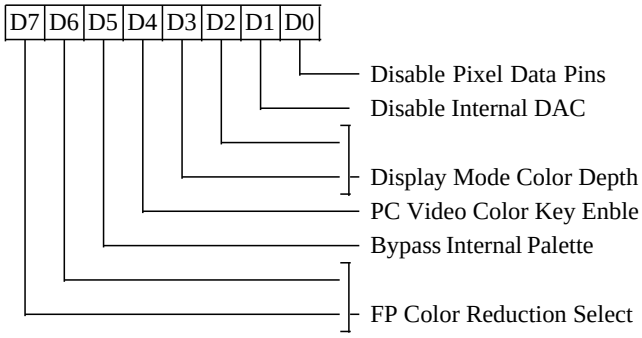
5 Reserved (R/W)

6 PC Video Interface Enable

0 Disable PC Video Interface (default)
1 Enable PC Video interface on memory group B pins (MBD15-0). 16-bit memory interface should be programmed (XR04[1-0]=01) and 16-bit CPU interface should be used in local bus configurations.

7 Reserved (R/W)

PALETTE CONTROL REGISTER (XR06)
Read/Write at I/O Address 3D7h
Index 06h



0 Disable Pixel Data Pins

0 Pixel data (P17:0) pins will output flat panel pixel data (default on Reset).
1 P7:0 will output CRT pixel data and other pixel data lines (P17:8) will output internal signals for diagnostic purpose.

1 Disable Internal DAC

This bit affects the DAC analog outputs.

0 Enable internal DAC (default on Reset). DAC analog outputs (R, G, B) will be active and HSYNC and VSYNC signals are driven (Default on reset).
1 Disable internal DAC. The DAC analog outputs (R, G, B) will be 3-stated. Setting this bit forces power down of the internal DAC. HSYNC and VSYNC are forced inactive if XR5D[6] is 0 and will be driven if XR5D[6] is 1.

3-2 Display Mode Color Depth

00 4 or 8 bits-per-pixel (default on reset)
01 16 bpp (5-5-5) (Sierra compatible)
10 24 bpp (true color)
11 16 bpp (5-6-5) (XGA compatible)

4 PC Video Color Key Enable

0 Disable PC Video Overlay (default on reset)
1 Enable PC Video Overlay on color key

5 Bypass Internal VGA Palette

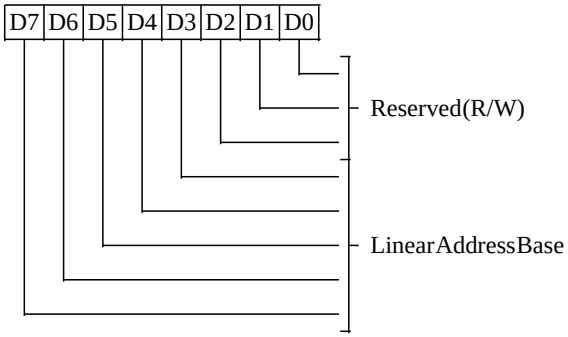
0 Use internal VGA palette (Default on reset).
1 Bypass internal VGA palette which will be powered down if DAC is disabled.

7-6 Color Reduction Select

These bits are effective in flat panel mode. These bits select the algorithm used to reduce 24-bit or 18-bit color data to 8-bit or 6-bit color data for monochrome panels.

00 NTSC weighting algorithm (default on reset)
01 Equivalent weighting algorithm
10 Green only
11 Color (no reduction). This setting should be used when driving color panels.

LINEAR ADDRESSING BASE REGISTER (XR08)
Read/Write at I/O Address 3B7h/3D7h
Index 08h



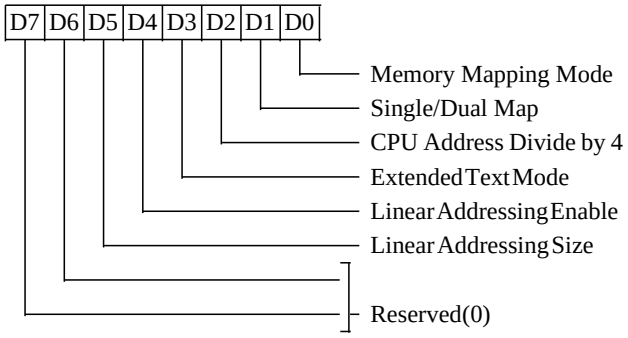
2-0 Reserved (R/W)

7-3 Linear Address Base

If linear addressing is enabled (XR0B[4]=1), these 5 bits are compared to ADDHI, A[23:20] to determine the base address of the 1 MB of linear display memory. For example, if the video memory is to be placed at 12Mb address, this register should be programmed to '01100'. If XR01[4]=0, ADDHI is ignored; if XR01[7]=0, ADDHI and A23 are ignored.

CPU PAGING REGISTER (XR0B)

Read/Write at I/O Address 3D7h
Index 0Bh



0 Memory Mapping Mode

0 Normal Mode (VGA compatible) (default on Reset)
1 Extended Mode (mapping for > 256 KByte memory configurations)

1 CPU Single/Dual Mapping

0 CPU uses only a single map to access the extended video memory space (default on Reset)
1 CPU uses two maps to access the extended video memory space. The base addresses for the two maps are defined in the Low Map Register (XR10) and High Map Register (XR11).

2 CPU Address Divide by 4

0 Disable divide by 4 for CPU addresses (default on Reset)
1 Enable divide by 4 for CPU addresses. This allows the video memory to be accessed sequentially in mode 13. In addition, all video memory is available in mode 13 by setting this bit.

3 Extended Text Mode

Set to enable text font 'scrambling' in plane 2. Setting this bit improves text performance in single DRAM configurations. This bit should be set in single DRAM configurations only.

4 Linear Addressing Enable

0 Standard VGA (A0000 - BFFFF) memory space decoded on-chip using A17-19 (default on Reset)
1 Linear Addressing Enabled. The video memory size for linear addressing is determined by XR0B[5].

5 Linearly Addressable Memory Size

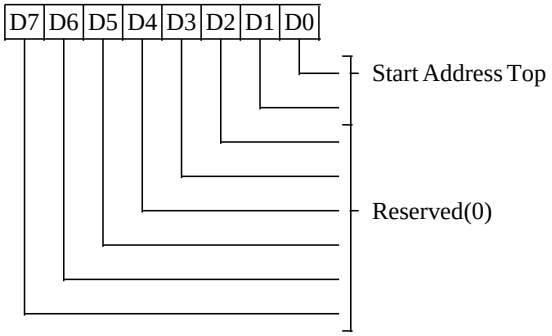
This bit controls the size of the linearly addressable video memory and the decodes for the linear address base are controlled by XR08[7:3].

0 The linearly addressable video memory size is 512 KBytes (default on reset).
1 The linearly addressable video memory size is 1 MByte.

7-6 Reserved (0)

START ADDRESS TOP REGISTER (XR0C)

Read/Write at I/O Address 3D7h
Index 0Ch



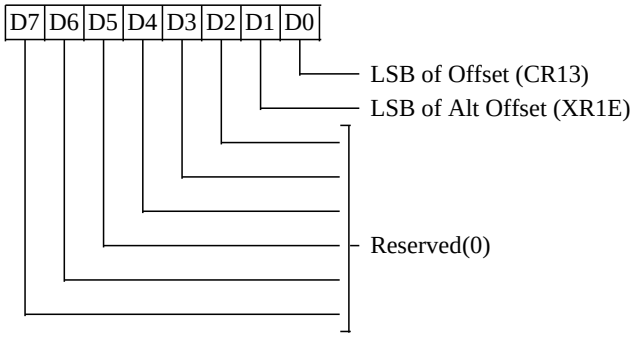
1-0 Start Address Top

These bits defines the high order bits for the Display Start Address when 512 KBytes or more of memory is used (see XR04 bits 1–0).

7-2 Reserved (0)

AUXILIARY OFFSET REGISTER (XR0D)

Read/Write at I/O Address 3D7h
Index 0Dh



0 Offset Register LSB

This bit provides finer granularity to the display memory address offset when word and doubleword modes are used. This bit is used with the regular Offset register (CR13).

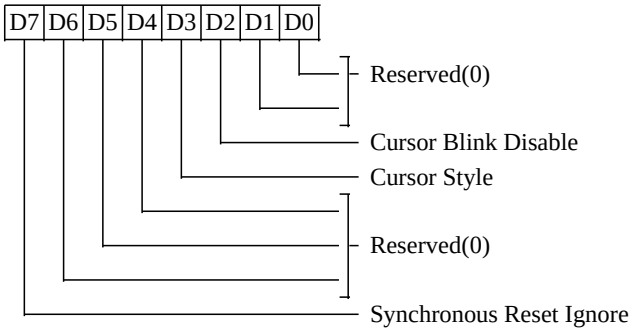
1 Alternate Offset Register LSB

This bit provides finer granularity to the display memory address offset when word and doubleword modes are used. This bit is used with the Alternate Offset register (XR1E).

7-2 Reserved (0)

TEXT MODE CONTROL REGISTER (XR0E)

Read/Write at I/O Address 3D7h
Index 0Eh



This register is effective for both CRT and flat panel text modes.

1-0 Reserved (0)

2 Cursor Mode

0 Blinking (default on Reset).
1 Non-blinking

3 Cursor Style

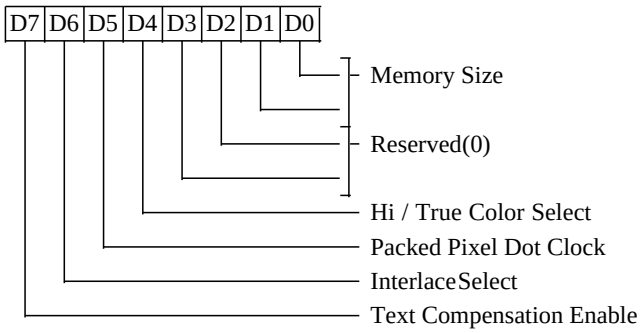
0 Replace (default on Reset)
1 Exclusive-Or

6-4 Reserved (0)

7 Synchronous Reset Ignore

When this bit is set, the chip will ignore SR00 bit-1 (Synchronous Reset) and will remain in normal operation. Synchronous Reset is a holdover from the original VGA which is no longer required. VGA software, however, performs Synchronous Resets frequently, creating the possibility for display memory corruption if the chip is left in the Synchronous Reset state for too long. The 65535 display memory sequencer does not need to be periodically reset, so this bit is provided to prevent potential display memory corruption problems. For absolute VGA compatibility, this bit may be set to 0.

SOFTWARE FLAGS REGISTER 0 (XR0F)
Read/Write at I/O Address 3D7h
Index 0Fh



This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software. For reference, the functions of the bits of this register are currently defined as follows:

1-0 Memory Size

00 256KB
01 512KB
1x 1MB

2-3 Reserved (0)

4 Hi Color / True Color

0 Current mode is not hi-/true-color mode
1 Current mode is hi-color / true-color mode

5 Packed-Pixel Mode Dot Clock

0 Use default dot clock in packed-pixel modes
1 Use 40MHz dot clock in packed-pixel modes

This bit is used for high resolution panels in panel mode only.

6 Interlace Select

0 Set mode 24h, 34h, 72h/75h or 7Eh interlaced
1 Set mode 24h, 34h, 72h/75h or 7Eh non-interlaced

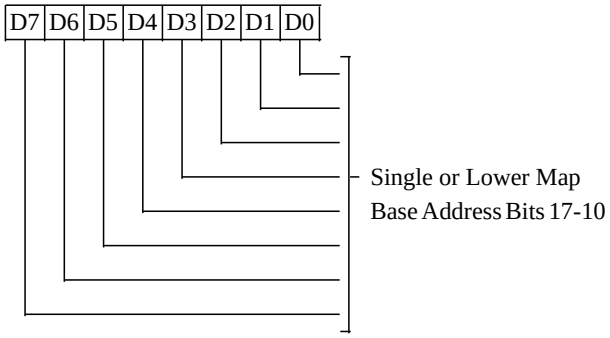
7 Text Compensation Enable / Disable

0 Tall font disabled
1 Tall font enabled

See also XR2B, XR44, XR45 for definition of other software flags registers.

SINGLE/LOW MAP REGISTER (XR10)

Read/Write at I/O Address 3D7h
Index 10h



This register effects CPU memory address mapping.

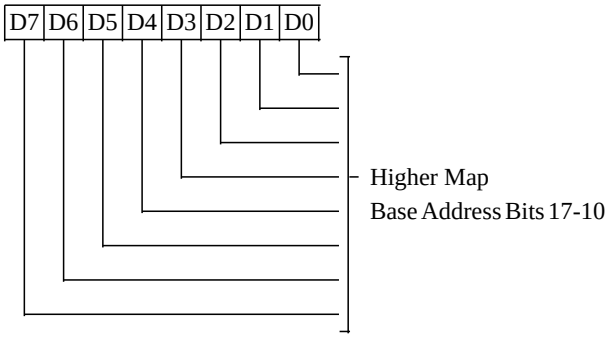
7-0 Single / Low Map Base Address Bits 17-10

These bits define the base address in single map mode (XR0B bit-1 = 0), or the lower map base address in dual map mode (XR0B bit-1 = 1). The memory map starts on a 1K boundary in planar modes and on a 4K boundary in packed pixel modes. In case of dual mapping, this register controls the CPU window into display memory based on the contents of GR06 bits 3-2 as follows:

GR06 Bits 3-2	Low Map	
00	A0000-AFFFF	
01	A0000-A7FFF	
10	B0000-B7FFF	Single mapping only
11	B8000-BFFFF	Single mapping only

HIGH MAP REGISTER (XR11)

Read/Write at I/O Address 3D7h
Index 11h



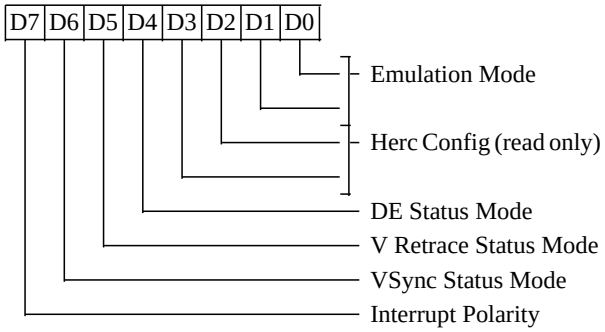
This register effects CPU memory address mapping.

7-0 High Map Base Address Bits 17-10

These bits define the Higher Map base address in dual map modes (XR0B bit-1=1). The memory map starts on a 1K boundary in planar modes and on a 4K boundary in packed pixel modes. This register controls the CPU window into display memory based on the contents of GR06 bits 3-2 as follows:

GR06 bits 3-2	High Map
00	B0000-BFFFF
01	A8000-AFFFF
10	Don't care
11	Don't care

EMULATION MODE REGISTER (XR14)
Read/Write at I/O Address 3D7h
Index 14h



1-0 Emulation Mode

00 VGA mode (default on Reset)
01 CGA mode
10 MDA/Herculesmode
11 EGA mode

3-2 Hercules Configuration Register (3BFh) readback (read only)

4 Display Enable Status Mode

0 Select Display Enable status to appear at bit 0 of Input Status register 1 (I/O Address 3BAh/3DAh) (default on reset). Normally used for CGA, EGA, and VGA modes.

1 Select HSync status to appear at bit 0 of Input Status register 1 (I/O Address 3BAh/3DAh). Normally used for MDA / Hercules mode.

5 Vertical Retrace Status Mode

0 Select VerticalRetrace status to appear at bit 3 of Input Status register 1 (I/O Address 3BAh/3DAh) (default on Reset). Normally used for CGA, EGA, and VGA modes.
1 Select Video to appear at bit 3 of Input Status register 1 (I/O Address 3BAh/3DAh). Normally used for MDA / Hercules mode.

6 VSync Status Mode

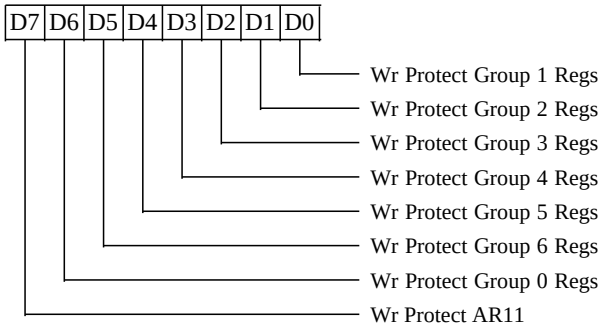
0 Prevent VSync status from appearing at bit 7 of Input Status Register 1 (I/O Address 3BAh/3DAh). Normally used for CGA, EGA, and VGA modes.
1 Enable VSync status to appear as bit-7 of Input Status Register 1 (I/O Address 3BAh/3DAh). Normally used for MDA/Hercules mode.

7 Interrupt Output Function

This bit controls the function of the interrupt output pin (IRQ):

Interrupt State	bit-7=0 PC Bus	bit-7=0 MC Bus	bit-7=1 Either Bus
Disabled	3-state	3-state	3-state
Enabled, Inactive	3-state	3-state	Low
Enabled, Active	3-state	Low	High

WRITE PROTECT REGISTER (XR15)
Read/Write at I/O Address 3D7h
Index 15h



This register controls write protection for various groups of registers as shown. 0 = unprotected (default on Reset), 1= protected.

0 Write Protect Group 1 Registers

This bit affects the Sequencer registers (SR00-04), Graphics Controller registers (GR00-08), and Attribute Controller registers (AR00-14).

Note that AR11 is also protected by bit-7 which is ORed with this bit.

1 Write Protect Group 2 Registers

This bit affects CR09 bits 0-4, CR0A, and CR0B.

2 Write Protect Group 3 Registers

This bit affects CR07 bit-4, CR08, CR11 bits 5-4, CR13, CR14, CR17 bits 0-1 and bits 3-7, and CR18.

3 Write Protect Group 4 Registers

This bit affects CR09 bits 5-7, CR10, CR11 bits 0-3 and bits 6-7, CR12, CR15, CR16, and CR17 bit-2.

4 Write Protect Group 5 Registers

This bit affects the Miscellaneous Output register (3C2h) and the Feature Control register(3BAh/3DAh).

5 Write Protect Group 6 Registers

This bit affects the VGA Color Palette registers (3C6h-3C9h). If this bit is set, all color palette registers are write protected.

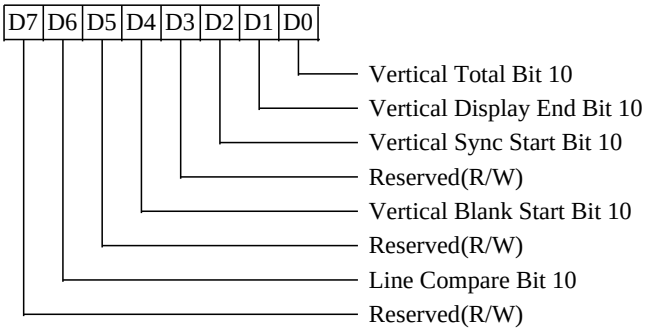
6 Write Protect Group 0 Registers

This bit affects CR0-7 (except CR07 bit-4). This bit is logically ORed with CR11 bit-7.

7 Write Protect AR11

This bit is ORed with bit-0, therefore writing to AR11 is possible only if both bit-0 and bit-7 are 0. This feature is used for write protection of the overscan color. This is important in order to keep application software from changing the border color while still permitting the attribute controller to be changed for the addressable portion of the display. Overscan is an ergonomics requirement in some systems and this bit will ensure software compatibility.

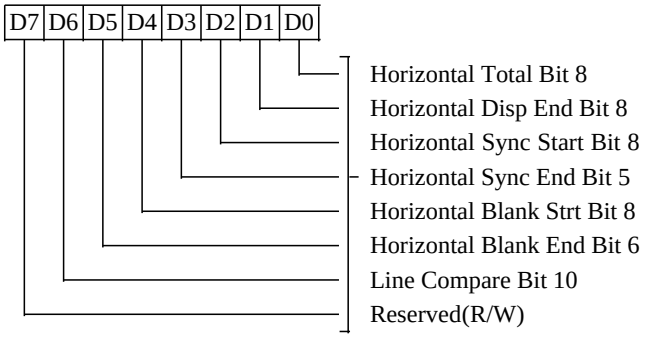
VERTICAL OVERFLOW REGISTER (XR16)
Read/Write at I/O Address 3D7h
Index 16h



This register is used for both normal and alternate vertical parameters.

0 Vertical Total Bit-10
1 Vertical Display End Bit-10
2 Vertical Sync Start Bit-10
3 Reserved (R/W)
4 Vertical Blank Start Bit-10
5 Reserved (R/W)
6 Line Compare Bit-10
7 Reserved (R/W)

HORIZONTAL OVERFLOW REGISTER (XR17)
Read/Write at I/O Address 3D7h
Index 17h

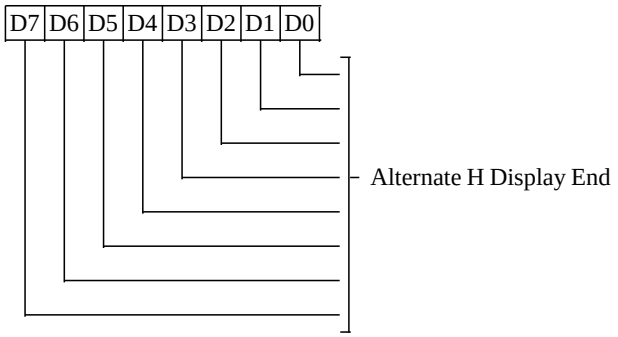


This register is used for both normal and alternate horizontal parameters.

0 Horizontal Total Bit-8
1 Horizontal Display End Bit-8
2 Horizontal Sync Start Bit-8
3 Horizontal Sync End Bit-5
4 Horizontal Blank Start Bit-8
5 Horizontal Blank End Bit-6
6 Line Compare Bit-10
7 Reserved (R/W)

ALTERNATE HORIZONTAL DISPLAY END REGISTER (XR18)

Read/Write at I/O Address 3D7h
Index 18h



This register is used in flat panel and CRT CGA text and graphics modes, and Hercules graphics mode.

7-0 Alternate Horizontal Display End

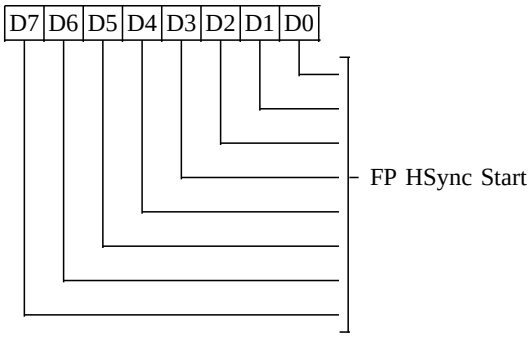
This register specifies the number of characters displayed per scan line, similar to CR01.

Programmed Value = Actual Value – 1

Note: This register is used in emulation modes only. It is not used in CRT or flat panel VGA modes.

FP HSYNC START REGISTER (XR19)

Read/Write at I/O Address 3D7h
Index 19h



This register is used in all flat panel modes with horizontal compression disabled, to set the horizontal sync start. This register is also used in CRT CGA text and graphics modes, and Hercules graphics mode.

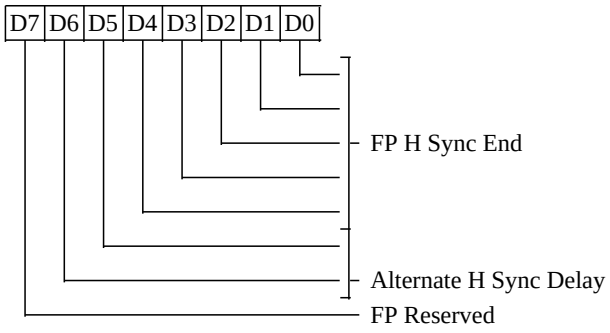
7-0 FP Alternate Horizontal Sync Start

These bits specify the beginning of the HSync in terms of character clocks from the beginning of the display scan. Similar to CR04.

Programmed Value = Actual Value – 1

FP HORIZONTAL SYNC END REGISTER (XR1A)

Read/Write at I/O Address 3D7h
Index 1Ah



This register is used in all flat panel modes with horizontal compression disabled, CRT CGA text and graphics modes, and Hercules graphics mode.

4-0 Alternate Horizontal Sync End

Lower 5 bits of the character clock count which specifies the end of horizontal sync. Similar to CR05. If the horizontal sync width desired is N clocks, then programmed value is:

(N + Contents of XR19) ANDed with 01F Hex

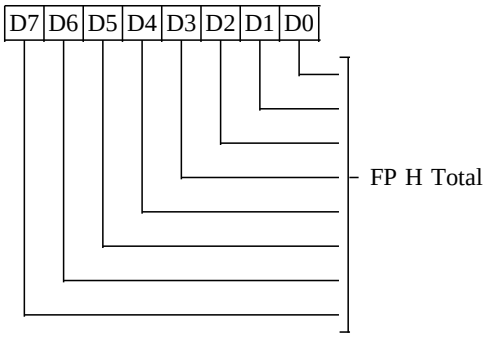
6-5 CRT Alternate Horizontal Sync Delay

See CR05 for description

7 FP Reserved

FP HORIZONTAL TOTAL REGISTER (XR1B)

Read/Write at I/O Address 3D7h
Index 1Bh



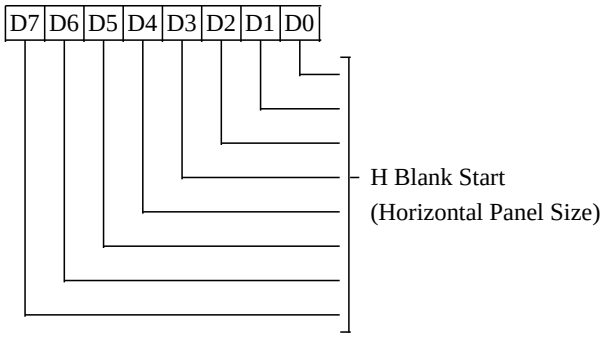
This register is used in all flat panel modes with horizontal compression disabled, CRT CGA text and graphics modes, and Hercules graphics mode.

7-0 Alternate Horizontal Total

This register contents are the total number of character clocks per line. Similar to CR00.

Programmed Value = Actual Value – 5

ALTERNATE HORIZONTAL BLANK START / HORIZONTAL PANEL SIZE REGISTER (XR1C)
Read/Write at I/O Address 3D7h
Index 1Ch



The value in this register is the Horizontal Panel Size in all Flat Panel Modes. In CRT mode, it is used for CGA text and graphics and Hercules graphics modes.

7-0 FP Horizontal Panel Size

Horizontal panel size is programmed in terms of number of 8-bit (graphics/text) or 9-bit (text) characters. For double drive flat panels the actual horizontal panel size must be a multiple of two character clocks.

Programmed Value = Actual Value – 1

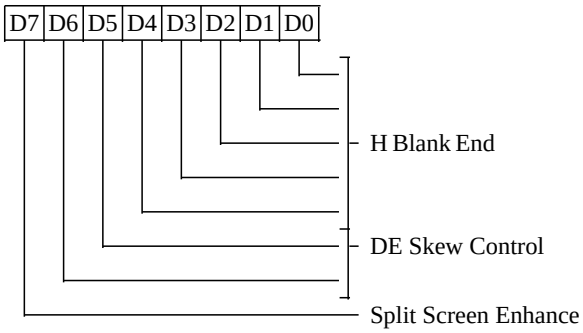
or

7-0 CRT Alternate Horizontal Blank Start

See CR02 for description

Programmed Value = Actual Value – 1

ALTERNATE HORIZONTAL BLANK END REGISTER (XR1D)
Read/Write at I/O Address 3D7h
Index 1Dh



Bits 0-6 of this register are used in CRT CGA text and graphics modes and CRT Hercules graphics mode. Bit 7 of this register is used for all CRT and flat panel modes.

4-0 CRT Alternate Horizontal Blank Start

See CR03 for description

6-5 CRT Alternate Display Enable Skew Control

See CR03 for description

7 Line Compare Fix

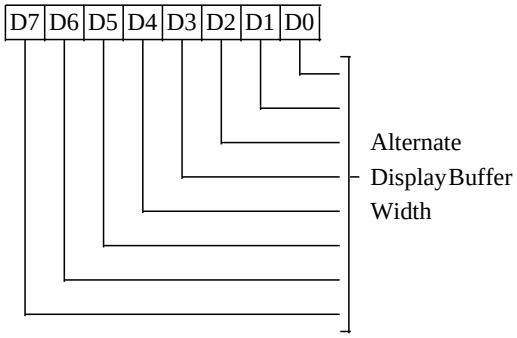
This bit affects all CRT and FP text modes. This bit is 0 on reset.

0 Internal Line Compare (split screen) flag is not delayed so that the Vertical Row Counter is reset too early which in text mode causes the first scanline of the first character row following split screen to be skipped (not displayed). This is IBM VGA compatible.

1 Internal Line Compare (split screen) flag is delayed so that the Vertical Row Counter is reset properly which in text mode causes the first scanline of the first character row following split screen to be displayed.

Note: This register is used in emulation modes only. It is not used in CRT or flat panel VGA modes.

ALTERNATE OFFSET REGISTER (XR1E)
Read/Write at I/O Address 3D7h
Index 1Eh



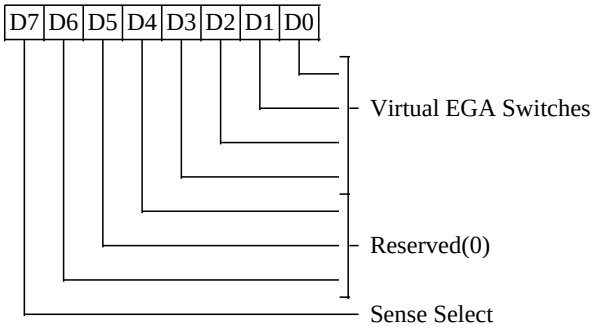
This register is used in all flat panel modes, CRT CGA text and graphics modes and Hercules graphics mode.

7-0 Alternate Offset

See CR13 for description

Programmed Value = Actual Value – 1

VIRTUAL EGA SWITCH REGISTER (XR1F)
Read/Write at I/O Address 3D7h
Index 1Fh



3-0 Virtual Switch Register

If bit-7 is '1', then one of these four bits is read back in Input Status Register 0 (3C2h) bit 4. The selected bit is determined by Miscellaneous Output Register (3C2h) bits 3-2 as follows:

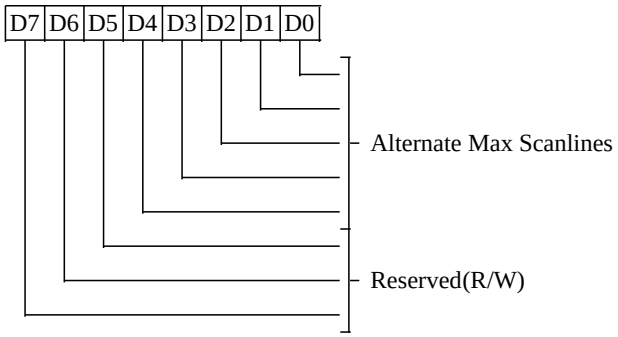
Misc 3-2	XR1F Bit Selected
00	bit-3
01	bit-2
10	bit-1
11	bit-0

6-4 Reserved (0)

7 Sense Select

0 Select the SENSE pin for readback in Input Status Register 0 bit-4 (default on Reset).
1 Select one of bits 3-0 for readback in Input Status Register 0 bit-4.

ALTERNATE MAXIMUM SCANLINE REGISTER (XR24)
Read/Write at I/O Address 3D7h
Index 24h



This register is used in flat panel text mode when TallFont is enabled during vertical compensation.

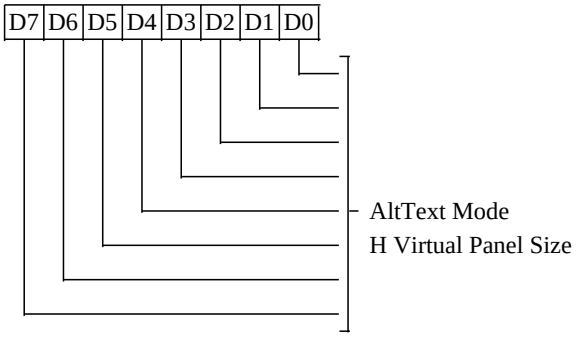
4-0 Alternate Maximum Scanlines (AMS)

Programmed Value = number of scanlines minus one per character row of TallFont

Double scanned lines, inserted lines, and replicated lines are not counted.

7-5 Reserved (R/W)

FP ALTERNATE TEXT MODE HORIZONTAL VIRTUAL PANEL SIZE REGISTER (XR25)
Read/Write at I/O Address 3D7h
Index 25h

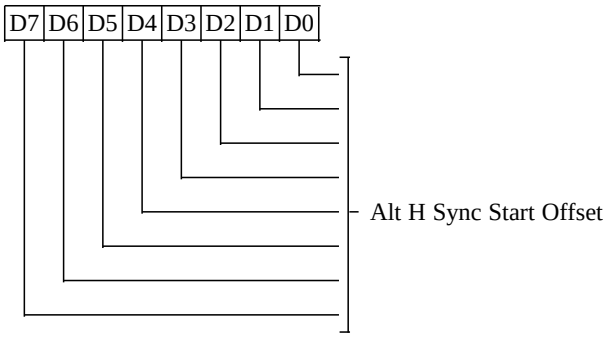


This register is used in flat panel 9-dot text modes.

7-0 FP Alternate Text Mode Horizontal Virtual Panel Size

Programmed Value = 9/8 [XR1C + 1] – 1

ALTERNATE HORIZONTAL SYNC START OFFSET REGISTER (XR26)
Read/Write at I/O Address 3D7h
Index 26h



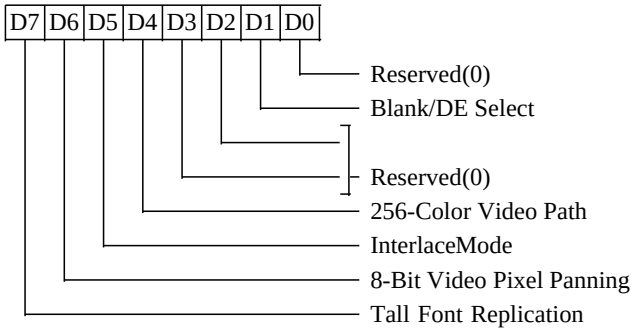
This register is used in flat panel mode.

7-0 Horizontal Sync Start Offset

This value is added to CR04 (Horizontal Sync Start) when XR02 bit 2 is set to '1'.

VIDEO INTERFACE REGISTER (XR28)

Read/Write at I/O Address 3D7h
Index 28h



0 Reserved (0)

1 Blank / Display Enable Select

This bit is effective in CRT mode only. In flat panel mode, XR54 bit-1 controls BLANK# pin functionality.

0 BLANK# controls color palette output (default)
1 Display Enable controls palette output

3-2 Reserved (0)

4 256-Color Video Path

This bit is effective for both CRT and flat panel in 256-color modes other than mode 13 (i.e., Super VGA modes).

0 4-bit video data path (default on reset)
1 8-bit video data path (horizontal pixel panning is controlled by bit-6)

Note: GR05 bit-5 must be 0 if this bit is set

5 Interlace Video

This bit is effective only for CRT graphics mode; it should be programmed to 0 for flat panel. In interlace mode XR29 holds the half-line positioning of VSync for odd frames.

0 Non-interlaced video (default on reset)
1 Interlacedvideo

6 8-Bit Video Pixel Panning

This bit is effective for both CRT and flat panel when the 8-bit video data path is selected (bit-4 = 1).

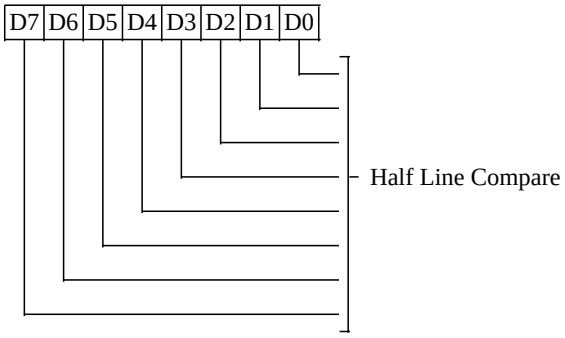
0 AR13 bits 2-1 used to control pixel panning (default on Reset)
1 AR13 bits 2-0 used to control pixel panning

7 Tall Font Replication

0 Lines 1, 9 and 12 replicated once
1 Line 0 replicated twice & line 15 once

HALF LINE COMPARE REGISTER (XR29)

Read/Write at I/O Address 3D7h
Index 29h



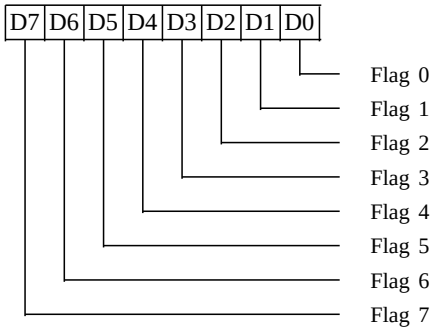
In Interlaced mode CRT operation, this register is used to generate the Half Line Compare Signal.

7-0 CRT Half-Line Value

In CRT interlaced video mode this value is used to generate the 'half-line compare' signal that controls the positioning of the VSync for odd frames.

SOFTWARE FLAGS REGISTER 1 (XR2B)

Read/Write at I/O Address 3D7h
Index 2Bh



This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software. For reference, the functions of the bits of this register are currently defined as follows:

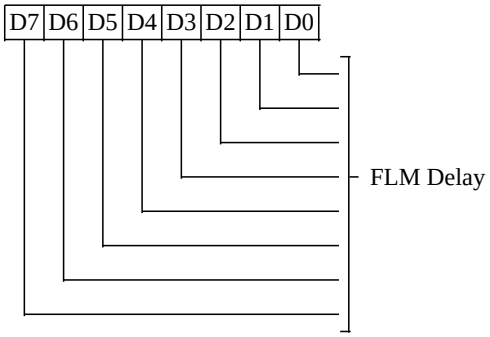
7-0 Display Mode

These bits are used by the BIOS to store the current display mode number.

See also XR0F, XR44, XR45 for definition of other software flags registers.

FLM DELAY REGISTER (XR2C)

Read/Write at I/O Address 3D7h
Index 2Ch

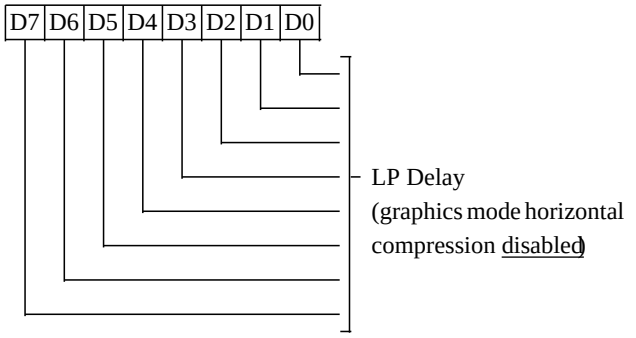


This register is used only in flat panel mode when XR2F bit-7=0. The First Line Marker (FLM) signal is generated from an internal FP VSync active edge with a delay specified by this register. The FLM pulse width is always one line for SS panels and two lines for DD panels.

7-0 FLM Delay (VDelay)

These bits define the number of HSyncs between the internal VSync and the rising edge of FLM.

LP DELAY REGISTER (CMPR OFF) (XR2D)
Read/Write at I/O Address 3D7h
Index 2Dh



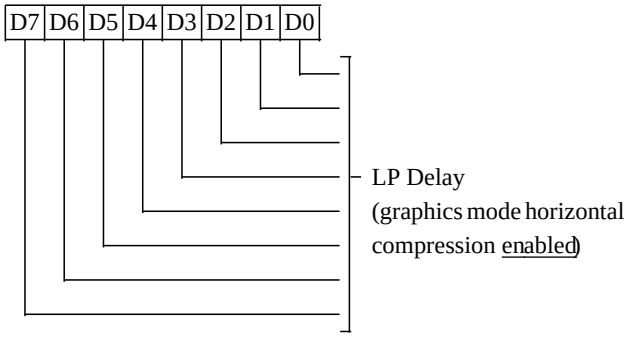
This register is used only in flat panel mode when XR2F bit-6 = 0 and graphics mode horizontal compression is disabled. The LP output is generated from the FP Blank inactive edge with a delay specified by XR2F bit-5 and the value in this register. The LP pulse width is specified in register XR2F.

7-0 LP Delay (HDelay)

These bits define the number of character clocks between the FP Blank inactive edge and the rising edge of the LP output in flat panel mode with graphics mode horizontal compression disabled. The msb (bit 8) of this parameter is XR2F bit-5.

Programmed Value = Actual Value – 1

LP DELAY REGISTER (CMPR ON) (XR2E)
Read/Write at I/O Address 3D7h
Index 2Eh



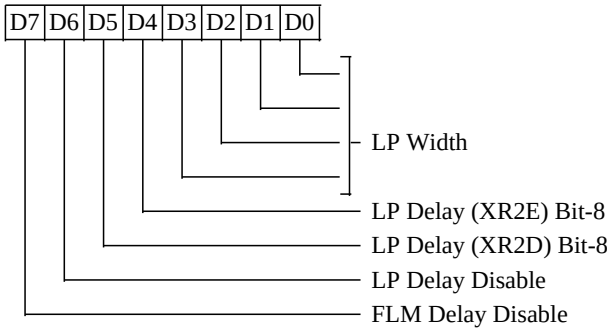
This register is used only in flat panel mode when XR2F bit-6 = 0 and 9-dot text mode is used. The LP output is generated from the FP Blank inactive edge with a delay specified by XR2F bit-4 and the value in this register. The LP pulse width is specified in register XR2F.

7-0 LP Delay (HDelay)

These bits define the number of character clocks between the FP Blank inactive edge and the rising edge of the LP output in flat panel 9-dot text modes. The msb (bit 8) of this parameter is XR2F bit-4.

Programmed Value = Actual Value – 1

LP WIDTH REGISTER (XR2F)
Read/Write at I/O Address 3D7h
Index 2Fh



This register is used only in flat panel mode. This register together with XR2D or XR2E defines the LP output pulse in flat panel mode.

3-0 LP Width

These bits define the width of LP output pulse in terms of number of character (8-dot only) clocks in flat panel mode.

Programmed Value = Actual Value – 1

4 LP Delay (XR2E) Bit-8

This bit is the msb of the LP Delay parameter for 9-dot text modes.

5 LP Delay (XR2D) Bit-8

This bit is the msb of the LP Delay parameter for graphics mode with horizontal compression disabled.

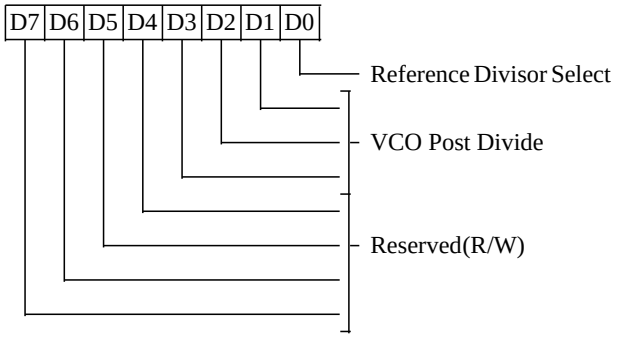
6 LP Delay Disable

0 LP Delay Enable: XR2D and XR2F bit-5 (or XR2E and XR2F bit-4) are used to delay the LP active edge with respect to the FP Blank inactive edge.
1 LP Delay Disable: the LP active edge will coincide with the FP Blank inactive edge.

7 FLM Delay Disable

0 FLM Delay Enable: XR2C is used to delay the external FLM active edge with respect to the internal FLM active edge.
1 FLM Delay Disable: the external FLM active edge will coincide with the internal FLM active edge.

CLOCK DIVIDE CONTROL REGISTER 0 (XR30)
Read/Write at I/O Address 3D7h
Index 30h



The three clock data registers (XR30-XR32) are programmed with the loop parameters to be loaded into the clock synthesizer. The Memory and Video clock VCO's both have programmable registers. Which of the VCO's is currently selected for programming is determined by the Clock Register Program Pointer (XR33[5]).

The data written to this register is calculated based on the reference frequency, the desired output frequency, and characteristic VCO constraints as described in the Functional Description.

Data is written to registers XR30, and XR31 followed by a write to XR32. The completion of the write to XR32 causes data from all three registers is transferred to the VCO register file simultaneously. This prevents wild fluctuations in the VCO output during intermediate stages of a clock programming sequence.

0 Reference Divisor Select

Selects the reference pre-scale factor:

0 Divide by 4
1 Divide by 1

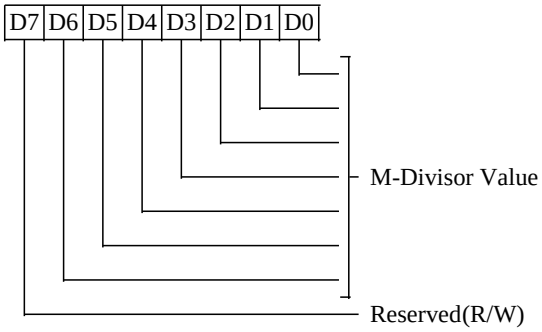
3–1 Post Divisor Select

Selects the post-divide factor:

000 Divide by 1
001 Divide by 2
010 Divide by 4
011 Divide by 8
100 Divide by 16
101 Divide by 32
110 Divide by 64
111 Divide by 128

7–4 Reserved (R/W)

CLOCK M-DIVISOR REGISTER (XR31)
Read/Write at I/O Address 3D7h
Index 31h



The three clock data registers (XR30-XR32) are programmed with the loop parameters to be loaded into the clock synthesizer. The Memory and Video clock VCO's both have programmable registers. Which of the VCO's is currently selected for programming is determined by the Clock Register Program Pointer (XR33[5]).

The data written to this register is calculated based on the reference frequency, the desired output frequency, and characteristic VCO constraints as described in the Functional Description.

Data is written to registers XR30, and XR31 followed by a write to XR32. The completion of the write to XR32 causes data from all three registers is transferred to the VCO register file simultaneously. This prevents wild fluctuations in the VCO output during intermediate stages of a clock programming sequence.

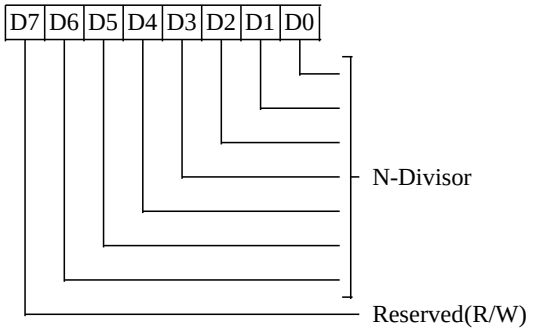
6–0 VCO M-Divisor

M-Divisor value calculated for the desired output frequency.

7 Reserved (R/W)

CLOCK N-DIVISOR REGISTER (XR32)

Read/Write at I/O Address 3D7h
Index 32h



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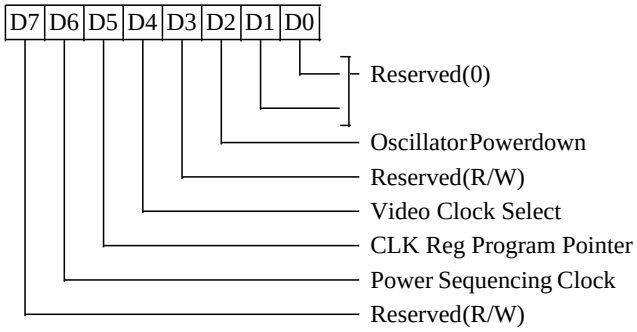
6–0 VCO N-Divisor

N-Divisor value calculated for the desired output frequency.

7 Reserved (R/W)

CLOCK CONTROL REGISTER (XR33)

Read/Write at I/O Address 3D7h
Index 33h



1-0 Reserved (0)

These bits are reserved for future use and must be programmed to 0 for proper operation.

2 Oscillator Powerdown

0 OSC Enabled (default on reset)
1 OSC Disabled

This bit is effective if XR01[5] = 1 and XR33[6] = 1.

3 Reserved (R/W)

4 Video Clock Select

0 Use VCLK as Video Clock Source

XR01[4] = 1 (internal clock source): use the output of the internal VCLK VCO as the video clock

XR01[4] = 0 (external clock source†): use the XTALI input pin (external video clock input) as the video clock

1 Use MCLK as Video Clock Source

XR01[4] = 1 (internal clock source): use the output of the internal MCLK VCO divided by 2 as the video clock

XR01[4] = 0 (external clock source†): use the ADDHI input pin (external memory clock input) divided by 2 as the video clock

5 Clock Register Program Pointer

This bit determines which VCO is being programmed. Following a write to XR32 the data contained in XR32:30 is synchronously transferred to the appropriate VCO counter latch.

0 VCLK VCO selected
1 MCLK VCO selected

6 Power Sequencing Reference Clock

If XR01[4]=0 (external clock source†):

0 Use AA9 pin as 32 KHz clock input for panel power sequencing and slow refresh clock (default on reset). Asymmetric DRAM option (XR05[3]=1) should not be enabled.
1 Use the MCLK divided by 1536 as the reference clock for panel power sequencing. For 56 MHz memory clock, panel power sequencing would be 36.5 KHz.

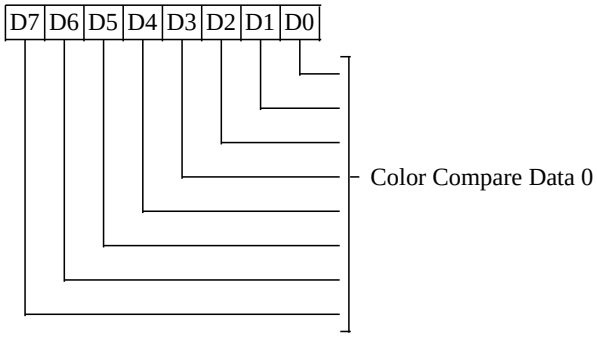
If XR01[4]=1 (internal clock source):

0 Use the XTALI input pin (or the oscillator on the XTALI & XTALO pins) divided by 384 as the panel power sequencing reference clock and slow refresh clock. For an input clock of 14.414 MHz, panel power sequencing clock would be 37.5 KHz (default on reset).
1 Use AA9 pin as 32 KHz clock input for panel power sequencing reference clock and slow refresh clock. Asymmetric DRAM option (XR05[3]=1) should not be enabled in this case.

7 Reserved (R/W)

† For the external clock option, GPIO0-1 are used to output clock selects 0 and 1, the ADDHI pin is used to input the memory clock, and the XTALI pin is used to input the video clock.

COLOR KEY REGISTER 0 (XR3A)
Read/Write at I/O Address 3D7h
Index 3Ah

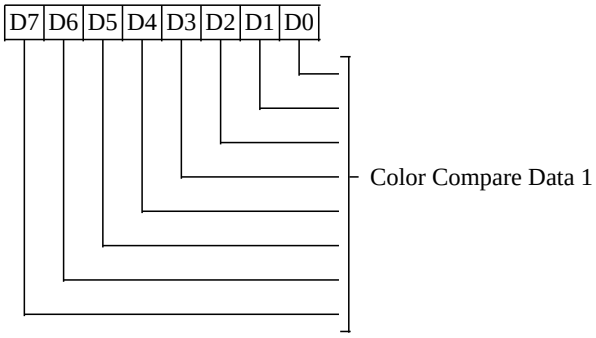


7-0 Color Compare Data 0

These bits are compared to the least significant 8 bits of the background video stream. If a match occurs on all enabled bits (see Color Compare Mask Register XR3D) and the key is enabled (XR06[4]), external video is sent to the screen. External video is input on the MBD15:0, CASBH# and CASBL# pins. The logical masking and compare operations are described in the functional description.

The color comparison occurs before the RAMDAC. In 4BPP and 8BPP modes using palette LUT data, the LUT index is used in the comparison, not the 18BPP LUT data.

COLOR KEY REGISTER 1 (XR3B)
Read/Write at I/O Address 3D7h
Index 3Bh

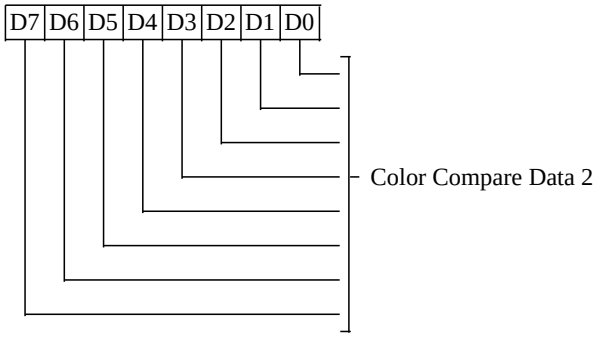


7-0 Color Compare Data 1

These bits are compared to bits 15:8 of the background video stream. If a match occurs on all enabled bits (see Color Compare Mask Register XR3D) and the key is enabled (XR06[4]), external video is sent to the screen. External video is input on the MBD15:0, CASBH# and CASBL# pins. The logical masking and compare operations are described in the functional description. This register should be masked from participating in the comparison in 4BPP and 8BPP modes. This is accomplished by setting Color Mask Register 1 (XR3E) = 0FFh.

COLOR KEY REGISTER 2 (XR3C)

Read/Write at I/O Address 3D7h
Index 3Ch

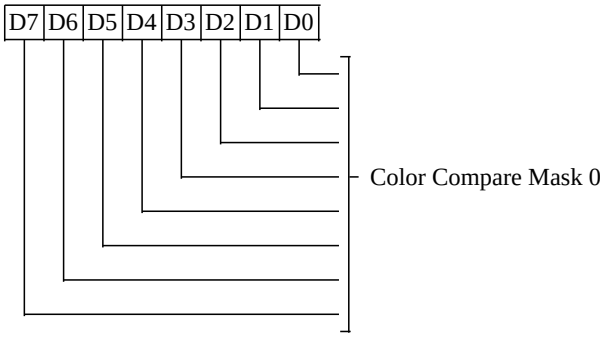


7-0 Color Compare Data 2

These bits are compared to bits 23:16 of the background video stream. If a match occurs on all enabled bits (see Color Compare Mask Register XR3D) and the key is enabled (XR06[4]), external video is sent to the screen. External video is input on the MBD15:0, CASBL# and CASBH# pins. The logical masking and compare operations are described in the functional description. This register should be masked from participating in the comparison in 4BPP, 8BPP and 16BPP modes. It should only be used in 24BPP modes. This is accomplished by setting Color Mask Register 2 (XR3F) = 0FFh.

COLOR KEY MASK REGISTER 0 (XR3D)

Read/Write at I/O Address 3D7h
Index 3Dh

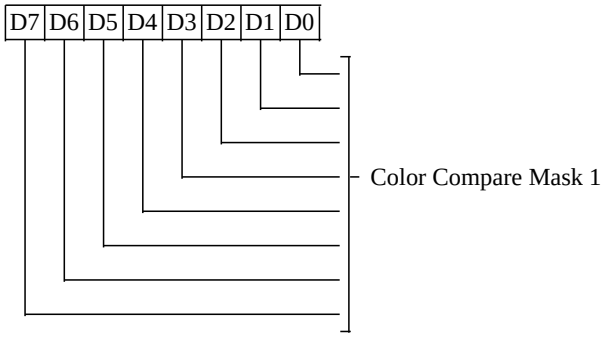


7-0 Color Compare Mask 0

This register is used to select which bits of the background video data stream are used in the comparison with the Color Compare Data 23:0. This register controls bits 7:0.

0 Data does participate in compare operation
1 Data does not participate in compare operation (masked)

COLOR KEY MASK REGISTER 1 (XR3E)
Read/Write at I/O Address 3D7h
Index 3Eh

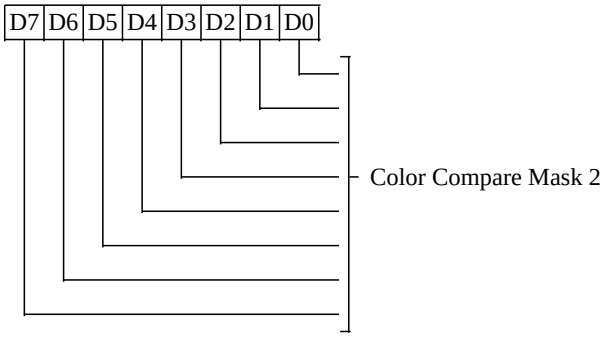


7-0 Color Compare Mask 1

This register is used to select which bits of the background video data stream are used in the comparison with the Color Compare Data 23:0. This register controls bits 7:0.

0 Data does participate in compare operation
1 Data does not participate in compare operation (masked)

COLOR KEY MASK REGISTER 2 (XR3F)
Read/Write at I/O Address 3D7h
Index 3Fh



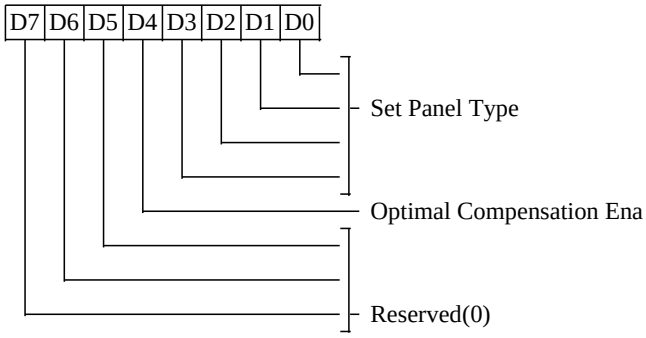
7-0 Color Compare Mask 2

This register is used to select which bits of the background video data stream are used in the comparison with the Color Compare Data 23:0. This register controls bits 7:0.

0 Data does participate in compare operation
1 Data does not participate in compare operation (masked)

SOFTWARE FLAGS REGISTER 2 (XR44)

Read/Write at I/O Address 3D7h
Index 44h



This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software. For reference, the functions of the bits of this register are currently defined as follows:

3-0 Set Panel Type (40K BIOS Only)

00	Panel #1
01	Panel #2
02	Panel #3
03	Panel #4
04	Panel #5
05	Panel #6
06	Panel #7
07	Panel #8
08-0F	Reserved

4 Optimal Compensation Enable

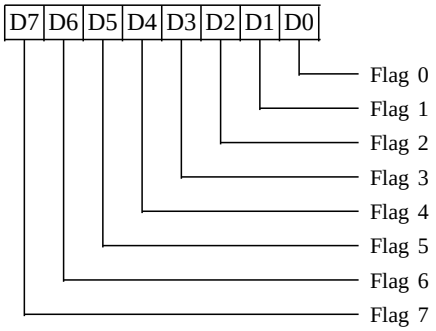
0	Disable optimal compensation
1	Enable optimal compensation

7-5 Reserved (0)

See also XR0F, XR2B, XR45 for definition of other software flags registers.

SOFTWARE FLAGS REGISTER 3 (XR45)

Read/Write at I/O Address 3D7h
Index 45h

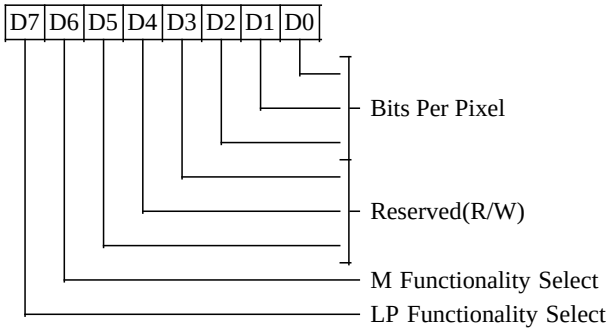


This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software. For reference, the functions of the bits of this register are currently defined as follows:

7-0 Flags (Reserved)

See also XR0F, XR2B, XR44 for definition of other software flags registers.

PANEL FORMAT REGISTER 2 (XR4F)
Read/Write at I/O Address 3D7h
Index 4Fh



This register is used only in flat panel mode.

2-0 Bits Per Pixel Selection

The value in this field, along with the dither and FRC settings, determines gray / color levels produced:

No FRC

	# of msbs Used to Generate Gray / Color Levels	Gray / Color Levels without Dithering	Gray / Color Levels with Dithering
001	1	2	5
010	2	4	13
011	3	8	13
100	4	16	61
101	5	32	125
110	6	64	253
111	8	256	n/a

2-Frame FRC
(Color TFT or Monochrome Panels)

	# of msbs Used to Generate Gray / Color Levels	Gray / Color Levels without Dithering	Gray / Color Levels with Dithering
010	1	3	9
011	2	7	25
100	3	15	57
101	4	31	125

16-Frame FRC
(Color or Monochrome STN Panels)

	# of msbs Used to Generate Gray / Color Levels	Gray / Color Levels without Dithering	Gray / Color Levels with Dithering
001	1	2	5
010	2	4	13
011	3	8	29
100	4	16	61

The setting programmed into this field determines how many most-significant color-bits / pixel are used to generate flat panel video data. In general, 8 bits of monochrome data or 8 bits/color of RGB color data enter the flat panel logic for every dot clock. Not all of these bits, however, are used to generate output colors / gray scales, depending on the type of panel used, graphics / text mode, and the gray-scaling algorithm chosen (the actual number of bits used is indicated in the table above). If the VGA palette is used then a maximum of 6 bits/pixel (bits 7-2) (setting '110') should be used. If the VGA palette is bypassed then a maximum of 8 bits/pixel (bits 7-0) (setting '111) may be used. With 2-frame and 16-frame FRC, settings not listed in the tables above are undefined. Also note that settings which achieve higher gray / color levels may not necessarily produce acceptable display quality on some (or any) currently available panels. This document contains recommended settings for various popular panels that Chips and Technologies has found to produce acceptable results with those panels. Customers may modify these settings to achieve a better match with their requirements.

3-5 Reserved (R/W)

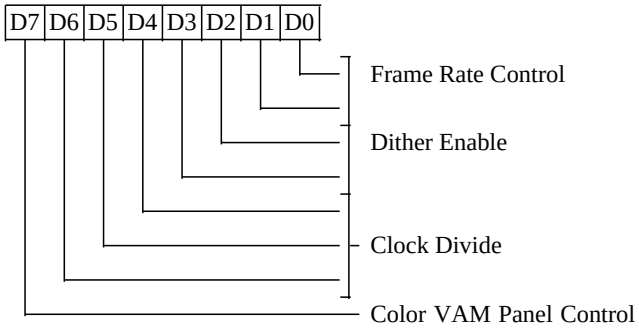
6 M Pin Select

0 M signal goes to the M pin (default on reset)
1 FP Display Enable (FP Blank#) signal goes to the M pin. Polarity is controlled by XR54[0].

7 LP Pin Select

0 FP HSync (LP) signal goes to the LP pin. Polarity is controlled by XR54[6] (default on reset).
1 FP Display Enable (FP Blank#) signal goes to the LP pin. Polarity is controlled by XR54[0].

PANEL FORMAT REGISTER 1 (XR50)
Read/Write at I/O Address 3D7h
Index 50h



This register is used only in flat panel mode.

1-0 Frame Rate Control (FRC)

FRC is gray scale simulation on a frame by frame basis to generate gray scales on on monochrome flat panels that do not support gray levels internally.

00 No FRC. This setting is used for panels which can generate gray scales internally.
01 16-frame FRC. One to four bits/pixel output to the panel are possible and therefore this setting is used only with panels which do not support internal gray scaling. This setting is used to simulate 16 gray levels per pixel. The bits per pixel are specified by XR4F[2-0] and the valid values are 010, 011, 100 and 101.
10 2-frame FRC. One to four bits/pixel output to the panel are possible and therefore this setting can also be used with panels that support internal gray scaling. Number of input bits used (specified in XR4F[2-0]) are one more than the number of output bits and therefore, the valid values for XR4F[2-0] are 010,011,100 or 101.
11 Reserved

3-2 Dither Enable

00 Disabledithering
01 Enable dithering for 256-color modes (AR10 bit-6 = 1 or XR28 bit 4 = 1)
10 Enable dithering for all modes
11 Reserved

6-4 Clock Divide (CD)

These bits specify the frequency ratio between the dot clock and the flat panel shift clock (SHFCLK) signal.

000 Shift Clock Freq = Dot Clock Freq. This setting is used to output 1 pixel per shift clock with a maximum of 8 bpp (bits/pixel) for single drive monochrome panels. For double drive color panels, this setting is used to output 2-2/3 4-bit pack pixels. FRC and dithering may be enabled.

001 Shift Clk Freq = 1/2 Dot Clock Freq. This setting is used to output 2 pixels per shift clock with a maximum of 8 bits/pixel for single drive monochrome panels and 4 bpp for single drive color panels. For double drive color panels, this setting is used to output 5-1/3 4-bit pack pixels. FRC and dithering can be enabled.

010 Shift Clk Freq = 1/4 Dot Clock Freq. This setting is used to output 4 pixels per shift clock with a maximum of 4 bpp for single drive mono panels and 2 bits/pixel for single drive color panels. For double drive monochrome panels, this setting is used to output 8 pixels per shift clock with 1 bit/pixel. FRC and dithering can be enabled.

011 Shift Clk Freq = 1/8 Dot Clock Freq. This setting is used to output 8 pixels per shift clock with a maximum of 2 bpp for single drive mono panels and 1 bit/pixel for single drive color panels. For double drive mono panels, this setting is also used to output 16 pixels per shift clock with 1 bit/pixel. FRC and dithering can be enabled.

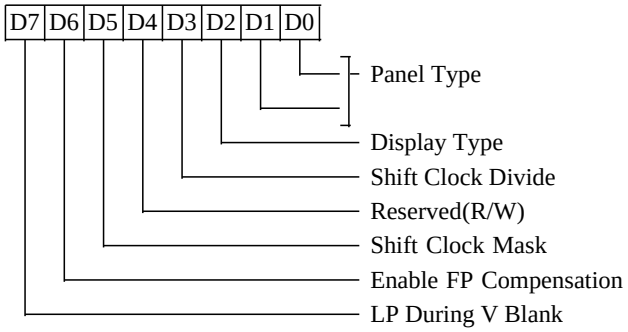
100 Shift Clk Freq = 1/16 Dot Clock Freq. This setting is used to output 16 pixels per shift clock with maximum of 1 bit/pixel for single drive monochrome panels. Dithering can also be enabled.

7 Color VAM Panel Control

This bit is effective only when color Voltage Amplitude Modulation (VAM) panel is used.

0 15-bit color VAM panel interface
1 18-bit color VAM panel interface

DISPLAY TYPE REGISTER (XR51)
Read/Write at I/O Address 3D7h
Index 51h



1-0 Panel Type (PT)

These bits are effective for flat panel only.

00 Single Panel Single Drive (SS)
01 Reserved
10 Reserved
11 Dual Panel Double Drive (DD)

2 Display Type (DT)

This bit is effective for CRT and flat panel. This bit also controls the BLANK# pin.

0 CRT display (default on Reset)
BLANK# pin outputs CRT Blank
1 FP (Flat Panel) display
BLANK# pin outputs FP Blank

3 Shift Clock Divide

This bit is effective for flat panel only.

0 Shift Clock to Dot Clock relationship expressed by XR50[6-4].
1 In this mode, the Shift Clock is further divided by 2 and different video data is valid on the rising and falling edges of Shift Clock.

4 Reserved (R/W)

5 Shift Clock Mask (SM)

This bit is effective for flat panel only.

0 Allow shift clock output to toggle outside the display enable interval
1 Force the shift clock output low outside the display enable interval

6 Enable FP Compensation (EFCP)

This bit is effective for flat panel only. It enables flat panel horizontal and vertical compensation depending on panel size, current display mode, and contents of the compensation registers.

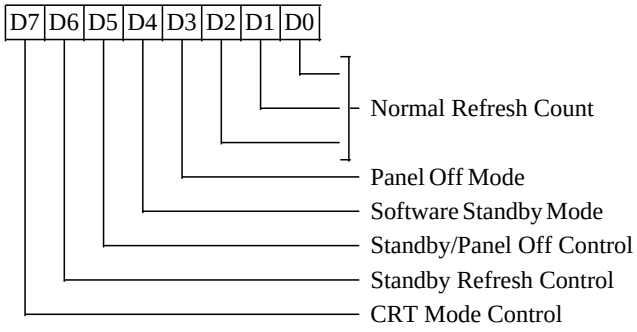
0 Disable FP compensation
1 Enable FP compensation

7 LP During Vertical Blank

This bit should be set only for SS panels which require FP HSync (LP) to be active during vertical blank time when XR54 bit-1 = 0 (e.g., Plasma / EL panels). This bit should be reset when using non-SS panels or when XR54 bit-1 = 1.

0 FP HSync (LP) is generated from internal FP Blank inactive edge
1 FP HSync (LP) is generated from internal FP Horizontal Blank inactive edge

POWER DOWN CONTROL REGISTER (XR52)
Read/Write at I/O Address 3D7h
Index 52h



2-0 Normal Refresh Count

These bits specify the number of memory refresh cycles to be performed per scanline. A minimum value of 1 should be programmed in this register.

3 Panel Off Mode

This bit provides a software alternative to enter Panel Off mode. Note that Panel Off mode will be effective in both CRT and flat panel modes of operation.

0 Normal mode (default on reset)
1 Panel Off mode

In Panel Off mode, the CRT / FP display memory interface is inactive but CPU interface and display memory refresh are still active. The internal RAMDAC is also inactive.

4 Software STANDBY Mode

This bit provides an alternative way to enter the Standby mode. When this bit is set, the 65535 enters Standby mode. To exit Standby mode, when this bit is set, STNDBY# pin must be asserted and then reasserted. This bit will also be reset when STNDBY# pin goes active (low).

0 Normal Mode (default on reset)
1 Standby Mode

5 Standby and Panel Off Control

This bit is effective in Flat Panel Mode during Standby and Panel Off modes (XR52[3] = 1 or XR52[4] = 1 or STNDBY# pin 11 active (low)).

0 Video data and/or flat panel control signals are driven inactive (default on reset).
1 Video data and flat panel control signals pins are tri-stated with a weak internal pull-down.

Note: XR61 bit-7 controls the inactive level for video data in text mode; XR63 bit-7 controls the inactive level for video data in graphics mode:

0 = low when inactive
1 = high when inactive

Note: This bit does not affect HSYNC and VSYNC pins. In Standby and Panel Off modes, HSYNC and VSYNC will be driven low.

6 Standby Refresh Control

This bit is effective only in Standby mode (STNDBY# pin low). Standby mode is effective for both CRT and flat panel modes. In Standby mode, CPU interface to display memory and internal registers is inactive. The CRT / FP display memory interface, video data and timing signals, and internal RAMDAC are inactive (all CRT and flat panel video control and data pins are 3-stated). Display memory refresh is controlled by this bit.

0 Self-Refresh DRAM support.
1 Display memory refresh frequency is derived from XR33 bit-6. This bit indicates whether the internal RCLK or the external 32 KHz is used for slow refresh.

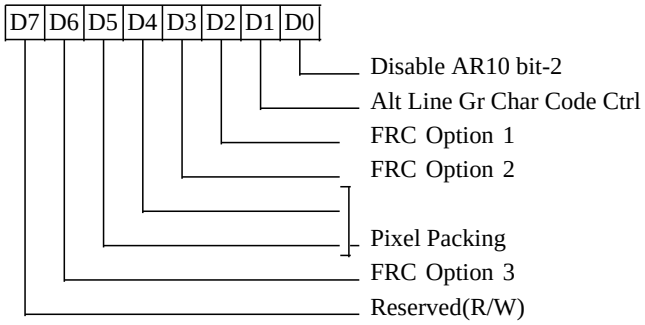
7 CRT Mode Control

This bit is effective in CRT mode only (non-simultaneous CRT and flat panel) (XR51 bit-2 = 0).

0 Video data and flat panel control signals are 3-stated with weak internal pull-down (default on reset).
1 Video data and flat panel control signals are inactive.

PANEL FORMAT REGISTER 3 (XR53)

Read/Write at I/O Address 3D7h
Index 53h



0 Disable AR10 Bit-2

0 Use AR10 bit-2 for Line Graphics control (default on Reset).
1 Use XR53 bit-1 instead of AR10 bit-2 for Line Graphics control

1 Alternate Line Graphics Character Control

This bit is effective only if bit-0 = 1.

0 Ninth pixel of line graphics character is set to the background color
1 Ninth pixel of line graphics character is identical to the eighth pixel

2 FRC Option 1

3 FRC Option 2

5-4 Pixel Packing

These bits should be programmed only when color STN panels are used. These bits should be programmed to 00 for monochrome panels or TFT color panels.

00 3-bit Pack. XR50 bits 5-4 can be 00, 01, or 10.
01 4-bit Pack. XR50 bits 5-4 can be 00 or 01. If a DD panel is used, XR50 bits 5-4 should be set 00.
10 Reserved
11 Extended 4-bit Pack. XR50 bits 5-4 must be programmed to 01.

These bits are effective only for Color STN panels when FRC is enabled.

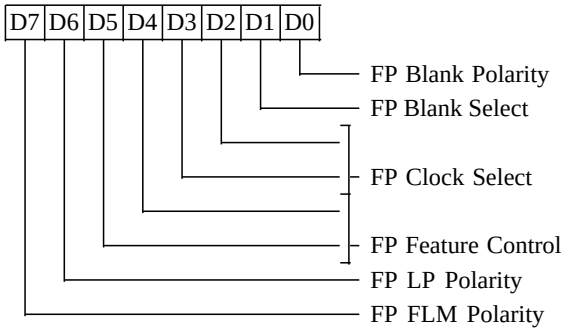
6 FRC Option 3

This bit affects 2-frame FRC

0 FRC data changes every frame
1 FRC data changes every other frame

7 Reserved (R/W)

PANEL INTERFACE REGISTER (XR54)
Read/Write at I/O Address 3D7h
Index 54h



This register is used only in flat panel modes.

0 FP Blank Polarity

This bit controls the polarity of the BLANK# pin in flat panel mode. In CRT mode, XR28 bit-0 controls polarity of the BLANK# pin.

0 Positive polarity
1 Negative polarity

1 FP Blank Select

This bit controls the BLANK# pin output in flat panel mode. In CRT mode, XR28 bit-1 controls the BLANK# output. This bit also affects operation of the flat panel video logic, generation of the FP HSync (LP) pulse signals, and masking of the Shift Clock.

0 The BLANK# pin outputs both FP Vertical and Horizontal Blank. In 480-line DD panels, this option will generate exactly 240 FP HSync (LP) pulses.
1 The BLANK# pin outputs only FP Horizontal Blank. During FP Vertical Blank, the flat panel video logic will be active, the FP HSync (LP) pulse will be generated, and Shift Clock can not be masked. Note however that Shift Clock can still be masked during FP Horizontal Blank.

Note: The signal polarity selected by bit-0 is applicable for either selection.

3-2 FP Clock Select Bits 1-0

Select flat panel dot clock source. These bits are used instead of Miscellaneous Output Register (MSR) bits 3-2 in flat panel mode. See description of MSR bits 3-2.

5-4 FP Feature Control Bits 1-0

Select flat panel dot clock source. These bits are used instead of Feature Control Register (FCR) bits 1-0 in flat panel mode. See description of FCR bits 1-0.

6 FP HSync (LP) Polarity

This bit controls the polarity of the flat panel HSync (LP) pin.

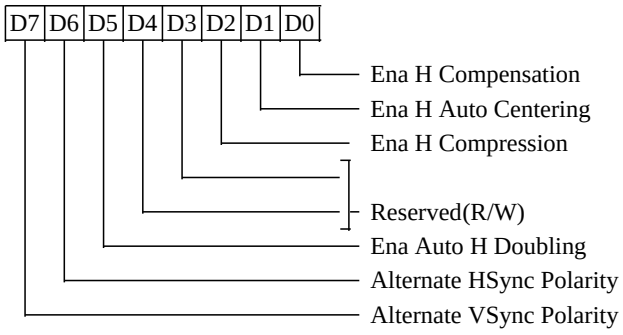
0 Positive polarity
1 Negative polarity

7 FP VSync (FLM) Polarity

This bit controls the polarity of the flat panel VSync (FLM) pin.

0 Positive polarity
1 Negative polarity

HORIZONTAL COMPENSATION REGISTER (XR55)
Read/Write at I/O Address 3D7h
Index 55h



This register is used only in flat panel modes when flat panel compensation is enabled (XR51 bit-6 = 1).

0 Enable Horizontal Compensation (EHCP)

0 Disable horizontal compensation
1 Enable horizontal compensation

1 Enable Automatic Horizontal Centering (EAHC) (effective only if bit-0 is 1)

0 Enable non-automatic horizontal centering. The Horizontal Centering Register is used to specify the left border. If no centering is desired then the Horizontal Centering Register can be programmed to 0.
1 Enable automatic horizontal centering. Horizontal left and right borders will be computed automatically.

2 Enable Text Mode Horizontal Compression (ETHC) (this bit is effective only if bit-0 is 1 in flat panel text mode). Setting this bit will turn on text mode horizontal compression regardless of horizontal display width or horizontal panel size.

0 Text mode horizontal compression off
1 Text mode horizontal compression on. 8-dot text mode is forced when 9-dot text mode is specified (SR01 bit-0 = 0 or Hercules text).

Note: This bit affects the horizontal pixel panning logic. When text mode horizontal compression is active, programming 9-bit panning will result in 8-bit panning.

4-3 Reserved (R/W)

5 Enable Automatic Horizontal Doubling (EAHD) (this bit is effective if bit-0 is 1)

0 Disable Automatic Horizontal Doubling. Horizontal doubling will only be performed for flat panels when SR01 bit-3 = 1 in any emulation mode or when 3B8/3D8 bit-0 & 3B8/3D8 bit-4 = 0 in CGA emulation.
1 Enable Automatic Horizontal Doubling. Horizontal doubling will be performed for flat panels when SR01 bit-3 = 1 in any emulation mode or when 3B8/3D8 bit-0 & 3B8/3D8 bit-4 = 0 in CGA emulation or when the Horizontal Display width (CR01) is equal to or less than half of the Horizontal Panel Size (XR18).

6 Alternate CRT HSync Polarity

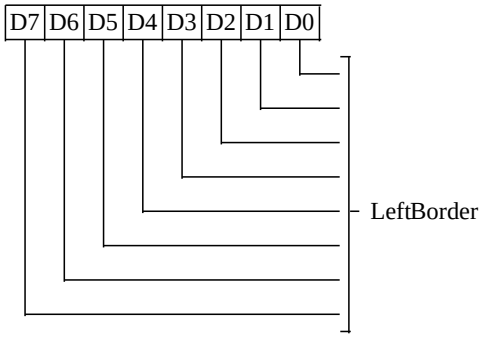
0 Positive
1 Negative

7 Alternate CRT VSync Polarity

0 Positive
1 Negative

Note: bits 6 and 7 above are used in flat panel mode (XR51 bit-2 = 1) instead of MSR bits 6 and 7). This is primarily used for simultaneous CRT / Flat Panel display.

HORIZONTAL CENTERING REGISTER (XR56)
Read/Write at I/O Address 3D7h
Index 56h

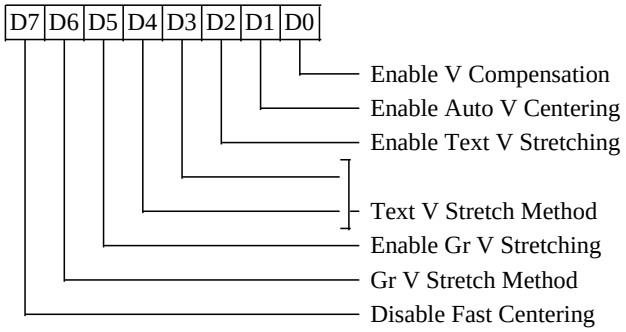


This register is used only in flat panel modes when non-automatic horizontal centering is enabled.

7-0 Horizontal Left Border (HLB)

Programmed Value (in character clocks)
= Width of Left Border – 1

VERTICAL COMPENSATION REGISTER (XR57)
Read/Write at I/O Address 3D7h
Index 57h



This register is used only in flat panel modes when flat panel compensation is enabled.

0 Enable Vertical Compensation (EVCP)

0 Disable vertical compensation
1 Enable vertical compensation

1 Enable Automatic Vertical Centering (EAVC)

This bit is effective only if bit-0 is 1.

0 Enable non-automatic vertical centering. The Vertical Centering Register is used to specify the top border. If no centering is desired then the Vertical Centering Register can be programmed to 0.
1 Enable automatic vertical centering. Vertical top and bottom borders will be computed automatically.

2 Enable Text Mode Vertical Stretching (ETVS)

This bit is effective only if bit-0 is 1.

0 Disable text mode vertical stretching; graphics mode vertical stretching is used if enabled.
1 Enable text mode vertical stretching

4-3 Text Mode Vertical Stretching (TVS1-0)

These bits are effective if bits 2 and 0 are 1.

00 Double Scanning (DS) and Line Insertion (LI) with the following priority: DS+LI, DS, LI.
01 Double Scanning (DS) and Line Insertion (LI) with the following priority: DS+LI, LI, DS.
10 Double Scanning (DS) and TallFont (TF) with the following priority: DS+TF, DS, TF.
11 Double Scanning (DS) and TallFont (TF) with the following priority: DS+TF, TF, DS.

5 Enable Vertical Stretching (EVS)

This bit is effective only if bit-0 is 1.

0 Disable vertical stretching
1 Enable vertical stretching

6 Vertical Stretching (VS)

Vertical Stretching can be enabled in both text and graphics modes. This bit is effective only if bits 5 and 0 are 1.

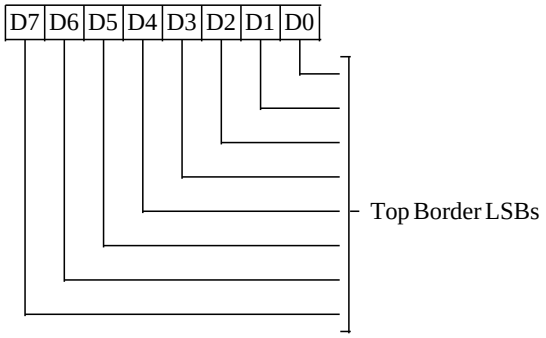
0 Double Scanning (DS) and Line Replication (LR) with the following priority: DS+LR, DS, LR.
1 Double Scanning (DS) and Line Replication (LR) with the following priority: DS+LR, LR, DS.

7 Disable Fast Centering

This bit is effective only if XR58[1-0] = 11.

0 Enable Fast Centering
1 Disable Fast Centering

VERTICAL CENTERING REGISTER (XR58)
Read/Write at I/O Address 3D7h
Index 58h



This register is used only in flat panel modes when non-automatic vertical centering is enabled.

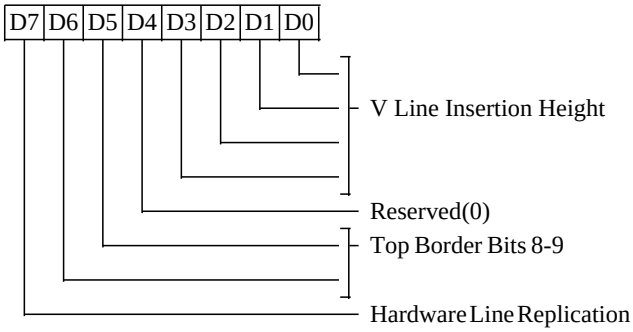
7-0 Vertical Top Border LSBs (VTB7-0)

Programmed value:

Top Border Height (in scan lines) – 1

This register contains the eight least significant bits of the programmed value of the Vertical Top Border (VTB). The two most significant bits are in the Vertical Line Insertion Register (XR59).

VERTICAL LINE INSERTION REGISTER (XR59)
Read/Write at I/O Address 3D7h
Index 59h



This register is used only in flat panel text mode when vertical line insertion is enabled.

3-0 Vertical Line Insertion Height (VLIH3-0)

Programmed Value:

Number of Insertion Lines – 1

The value programmed in this register - 1 is the number of lines to be inserted between the rows. Insertion lines are never double scanned even if double scanning is enabled. Insertion lines use the background color.

4 Reserved (0)

6-5 Vertical Top Border MSBs (VTB9-8)

This register contains the two most significant bits of the programmed value of the Vertical Top Border (VTB). The eight least significant bits are in the Vertical Centering Register (XR58).

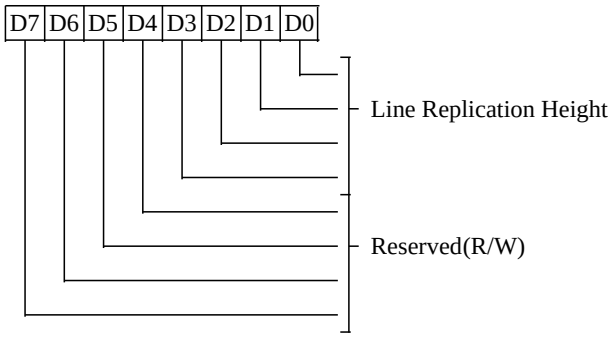
7 Hardware Line Replication

This bit is effective in text mode when Line Replication is selected (XR57[2] = 1). Hardware line replication, when enabled, replicates lines to display a 19-line character from a 16-line font as specified in XR28 bit-7.

0 Normal text mode line replication
1 Hardware line replication is enabled

VERTICAL LINE REPLICATION REGISTER (XR5A)

Read/Write at I/O Address 3D7h
Index 5Ah



This register is used only in flat panel text or graphics modes when vertical line replication is enabled.

3-0 Vertical Line Replication Height (VLRH)

Programmed Value = Number of Lines Between Replicated Lines – 1

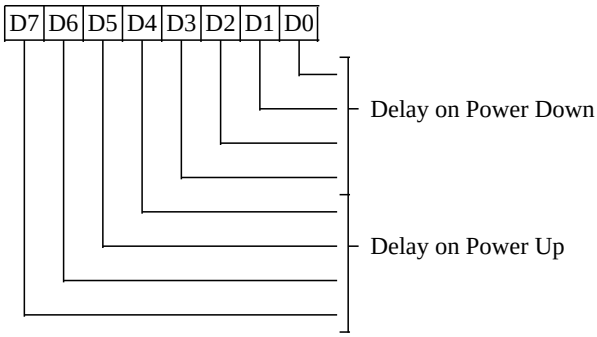
Double scanned lines are also counted.

In other words, if this field is programmed with '7', every 8th line will be replicated.

7-4 Reserved (R/W)

PANEL POWER SEQUENCING DELAY REGISTER (XR5B)

Read/Write at I/O Address 3D7h
Index 5Bh

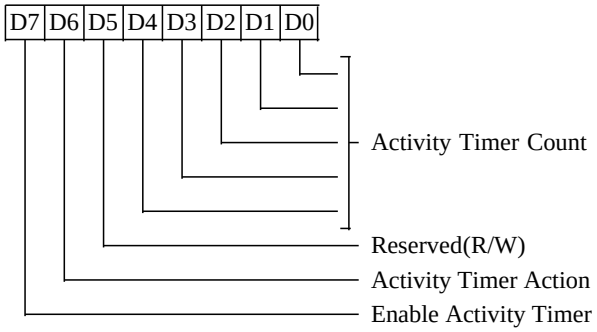


This register is used only in flat panel modes. The generation of the clock for panel power sequencing logic is controlled by XR33[6]. The delay intervals below assume a 37.5 KHz clock generated by the interal clock synthesizer. If the 32KHZ input is used, the delay intervals should be scaled accordingly.

3-0 Programmable value of panel power-sequencing during power down. This value can be programmed up to 459 milliseconds in increments of 29 milliseconds. A value of 0 is not valid.

7-4 Programmable value of panel power sequencing during power up. This value can be programmed up to 54 milliseconds in increments of 3.4 milliseconds. A value of 0 is not valid.

ACTIVITY TIMER CONTROL REGISTER (XR5C)
Read/Write at I/O Address 3D7h
Index 5Ch



This register is used to control the Activity timer functionality. The activity timer uses the same clock as power sequencing which is controlled by XR33[6]. The delay intervals below assume a 35.7 KHz clock, if an external 32 KHz input is used, the delay is scaled accordingly.

4-0 Activity Timer Count

For a 35.7 KHz clock the counter granularity is approximately 25.6 seconds. The minimum programmed value of 1 results in 25.6 second delay and the maximum count of 32 results in a delay of 13.7 minutes. If the clock input on AA9 is other than 32 KHz, the delay should be scaled accordingly.

5 Reserved (R/W)

6 Activity Timer Action

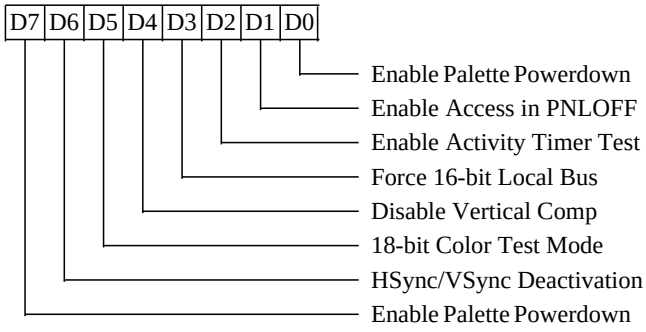
0 When the activity timer count is reached, the ENABKL pin is deactivated (driven low to turn the backlight off)
1 When the activity timer count is reached, Panel Off mode is entered.

7 Enable Activity Timer

0 Disable activity timer (default on reset)
1 Enable activity timer

FP DIAGNOSTIC REGISTER (XR5D)

Read/Write at I/O Address 3D7h
Index 5Dh



0 Enable VGA Palette Powerdown in Panel Off Mode.

0 Disable VGA Palette powerdown in Panel Off Mode (default on reset)
1 Enable VGA Palette powerdown in Panel Off mode

1 Enable CPU Access to VGA Palette in Panel Off Mode.

This bit is effective when bit 0=1 or bit 7=1.

0 Disable CPU access to VGA Palette in Panel Off Mode (default on reset)
1 Enable CPU access to VGA Palette in Panel Off Mode

2 Enable Activity Timer Test

0 Disable Activity Timer test mode (default on reset)
1 Enable Activity Timer test mode

3 Force 16-Bit Local Bus

This bit is effective when 32-bit local bus and 16-bit memory interface are used during font load.

0 Do not force 16-bit local bus when loading font (default on reset)
1 Force 16-bit local bus when loading font

4 Disable Vertical Compensation

0 Vertical compensation can be enabled in all cases (default on reset)
1 Disable vertical compensation if Vertical Display Enable End equals Vertical Panel Size.

5 18-bit Color TFT Test Mode

0 Disable 18-bit color TFT test mode (default on reset)
1 Enable 18-bit color TFT test mode

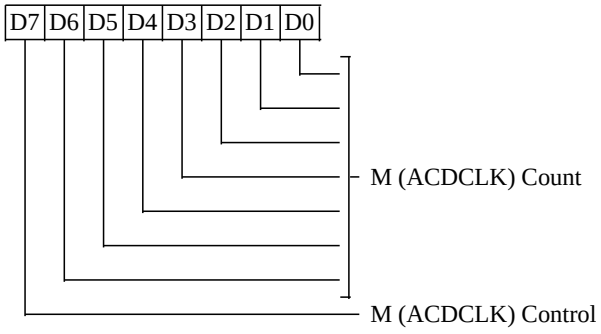
6 Prevent HSYNC and VSYNC Deactivation

0 Allow HSYNC and VSYNC to be deactivated when XR06[1] = 1 (default on reset)
1 Prevents HSYNC and VSYNC from being deactivated when XR06[1] = 1.

7 Enable VGA Palette Powerdown in VGA Palette Bypass Mode

0 Disable VGA palette powerdown when XR06[5]=1
1 Enable VGA palette powerdown when XR06[5]=1 and XR06[1]=1

M (ACDCLK) CONTROL REGISTER (XR5E)
Read/Write at I/O Address 3D7h
Index 5Eh



This register is used only in flat panel mode.

6-0 M (ACDCLK) Count (ACDCNT)

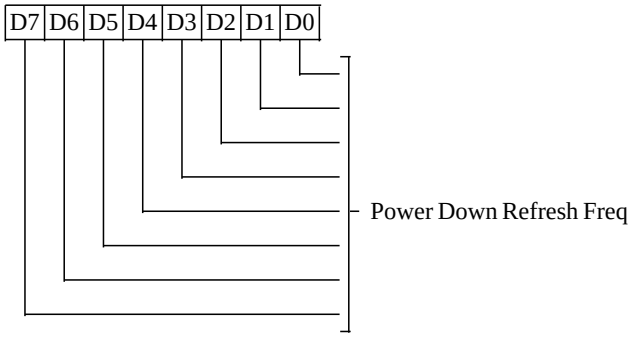
These bits define the number of HSyncs between adjacent phase changes on the M (ACDCLK) output. These bits are effective only when bit 7 = 0 and contents of this register are grater than 2.

Programmed Value = Actual Value – 2

7 M (ACDCLK) Control

0 The M (ACDCLK) phase changes depending on bits 0-6 of this register
1 The M (ACDCLK) phase changes every frame if frame accelerator is not used. If frame accelerator is used, the M (ACDCLK) phase changes every other frame.

POWER DOWN REFRESH REGISTER (XR5F)
Read/Write at I/O Address 3D7h
Index 5Fh



7-0 Power Down Refresh Frequency

These bits define the frequency of memory refresh cycles in power down (standby) mode (STNDBY# pin low). CAS-Before-RAS (CBR) refresh cycles are performed.

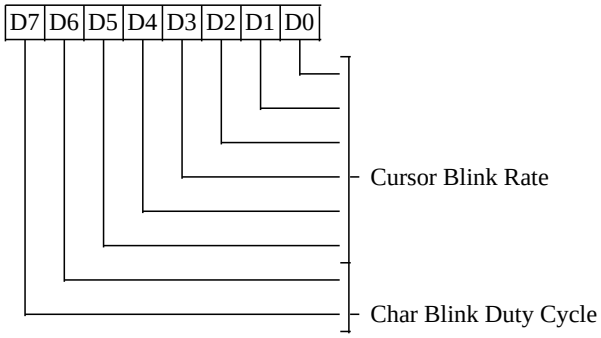
If XR52 bit-6 = 1, the interval between two refresh cycles is determined by bits 0-3 of this register per the table below. Bits 4-7 of this register are reserved for future use in this mode (and should be programmed to 0).

3 2 1 0	Approximate Refresh Interval
0 0 0 0	16 usec / cycle
0 0 0 1	47 usec / cycle
0 0 1 0	63 usec / cycle
0 0 1 1	78 usec / cycle
0 1 0 0	94 usec / cycle
0 1 0 1	109 usec / cycle
0 1 1 0	125 usec / cycle
0 1 1 1	141 usec / cycle
1 0 0 0	156 usec / cycle

These refresh intervals assume a 32 KHz clock. If the internal clock is used, the refresh interval is scaled accordingly.

If XR52 bit-6 = 0, a value of 0 causes no refresh to be performed. Self-Refresh DRAMs should be used in this case.

BLINK RATE CONTROL REGISTER (XR60)
Read/Write at I/O Address 3D7h
Index 60h



This register is used in all modes.

5-0 Cursor Blink Rate

These bits specify the cursor blink period in terms of number of VSyncs (50% duty cycle). In text mode, the character blink period and duty cycle is controlled by bits 7-6 of this register. These bits default to 000011 (decimal 3) on reset which corresponds to eight VSyncs per cursor blink period per the following formula (four VSyncs on and four VSyncs off):

Programmed Value = (Actual Value) / 2 – 1

Note: In graphics mode, the pixel blink period is fixed at 32 VSyncs per cursor blink period with 50% duty cycle (16 on and 16 off).

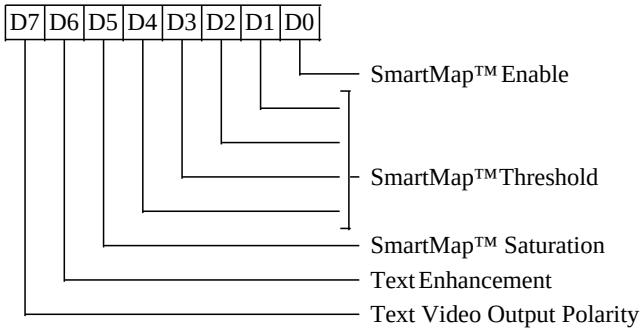
7-6 Character Blink Duty Cycle

These bits specify the character blink (also called 'attribute blink') duty cycle in text mode.

7	6	Character Blink Duty Cycle	
0	0	50%	
0	1	25%	
1	0	50%	(default on Reset)
1	1	75%	

For setting 00, the character blink period is equal to the cursor blink period. For all other settings, the character blink period is twice the cursor blink period (character blink is twice as slow as cursor blink).

SMARTMAP™ CONTROL REGISTER (XR61)
Read/Write at I/O Address 3D7h
Index 61h



This register is used in flat panel text mode only.

0 SmartMap™ Enable

0 Disable SmartMap™, use color lookup table and use internal RAMDAC palette if enabled (XR06 bit-2 = 1).

1 Enable SmartMap™, bypass both color lookup table and internal RAMDAC palette in flat panel text mode. Although color lookup table is bypassed, translation of 4 bits/pixel data to 6 bits/pixel data is still performed depending on AR10 bit-1 (monochrome / color display) as follows:

Output	AR10 bit-1 = 0	AR10 bit-1 = 1
Out0	In0	In0
Out1	In1	In1
Out2	In2	In2
Out3	In3	In0+In1+In2+In3
Out4	In3	In3
Out5	In3	In3

Note: This bit does not affect CRT text / graphics mode or flat panel graphics mode; i.e.: the color lookup table is always used, and similarly the internal RAMDAC palette is used if enabled.

4-1 SmartMap™ Threshold

These bits are used only in flat panel text mode when SmartMap™ is enabled (bit-0 = 1). They define the minimum difference between the foreground and background colors. If the difference is less than this threshold, the colors are separated by adding and subtracting the shift values (XR62) to the foreground and background colors. However, if the foreground and background color values are the same, then the color values are not adjusted.

5 SmartMap™ Saturation

This bit is used only in flat panel text mode when SmartMap™ is enabled (bit-0 = 1). It selects the clamping level after the color addition/subtraction.

0 The color result is clamped to the maximum and minimum values (0Fh and 00h respectively)

1 The color result is computed modulo 16 (no clamping)

6 Text Enhancement

This bit is used only in flat panel text mode.

0 Normal text
1 Text attribute 07h and 0Fh are reversed to maximize the brightness of the normal DOS prompt

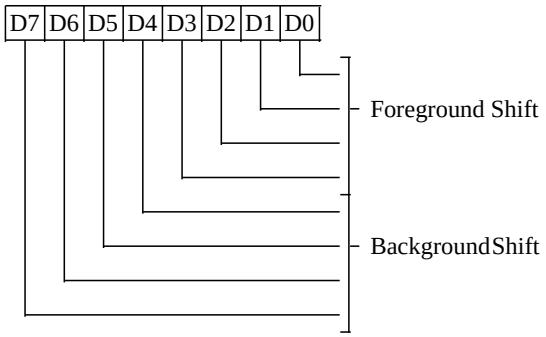
7 Text Video Output Polarity (TVP)

This bit is effective for flat panel text mode only.

0 Normal polarity
1 Inverted polarity

Note: Graphics video output polarity is controlled by XR63 bit-7 (GVP).

SMARTMAP™ SHIFT PARAMETER REGISTER (XR62)
Read/Write at I/O Address 3D7h
Index 62h



This register is used in flat panel text mode when SmartMap™ is enabled (XR61 bit-0 = 1).

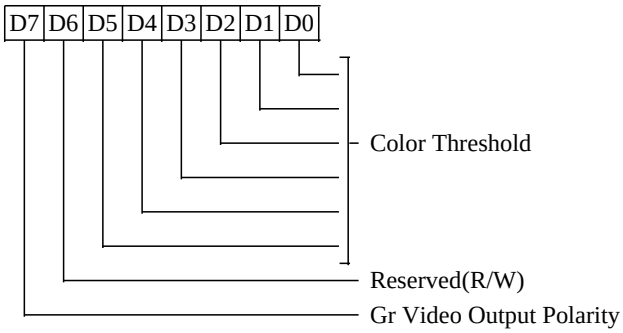
3-0 Foreground Shift

These bits define the number of levels that the foreground color is shifted when the foreground and background colors are closer than the SmartMap™ Threshold (XR61 bits 1-4). If the foreground color is "greater" than the background color, then this field is added to the foreground color. If the foreground color is "smaller" than the background color, then this field is subtracted from the foreground color.

7-4 Background Shift

These bits define the number of levels that the background color is shifted when the foreground and background colors are closer than the SmartMap™ Threshold (XR61 bits 1-4). If the background color is "greater" than the foreground color, then this field is added to the background color. If the background color is "smaller" than the foreground color, then this field is subtracted from the background color.

SMARTMAP™ COLOR MAPPING CONTROL REGISTER (XR63)
Read/Write at I/O Address 3D7h
Index 63h



5-0 Color Threshold

These bits are effective for monochrome (XR51 bit-5 = 1) single/double drive flat panel with 1 bit/pixel (XR50 bits 4-5 = 11) without FRC (XR50 bits 0-1 = 11). They specify the color threshold used to reduce 6-bit video to 1-bit video color. Color values equal to or greater than the threshold are mapped to 1 and color values less than the threshold are mapped to 0.

6 Reserved (R/W)

Reset defaults this bit to 1.

7 Graphics Video Output Polarity (GVP)

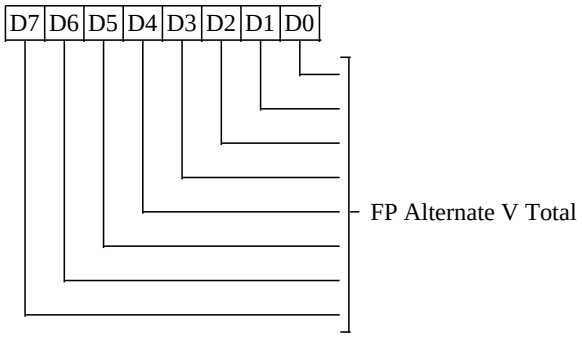
This bit is effective for CRT and flat panel graphics mode only.

0 Normal polarity
1 Inverted polarity

Note: Text video output polarity is controlled by XR61 bit-7 (TVP).

FP ALTERNATE VERTICAL TOTAL REGISTER (XR64)

Read/Write at I/O Address 3D7h
Index 64h



This register is used in all flat panel modes.

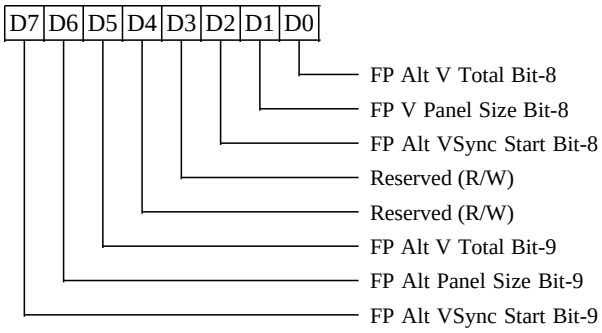
7-0 FP Alternate Vertical Total

The contents of this register are 8 low order bits of a 10-bit value. Bits 9 and 10 are defined in XR65. The vertical total value specifies the total number of scan lines per frame. Similar to CR06.

Programmed Value = Actual Value – 2

FP ALTERNATE OVERFLOW REGISTER (XR65)

Read/Write at I/O Address 3D7h
Index 65h



This register is used in all flat panel modes.

0 FP Alternate Vertical Total Bit-8

1 FP Vertical Panel Size Bit-8

2 FP Alternate Vertical Sync Start Bit-8

3 Reserved (R/W)

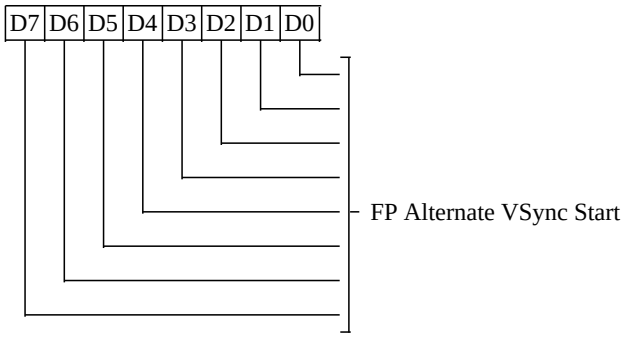
4 Reserved (R/W)

5 FP Alternate Vertical Total Bit-9

6 FP Vertical Panel Size Bit-9

7 FP Alternate Vertical Sync Start Bit-9

FP ALTERNATE VERTICAL SYNC START REGISTER (XR66)
Read/Write at I/O Address 3D7h
Index 66h



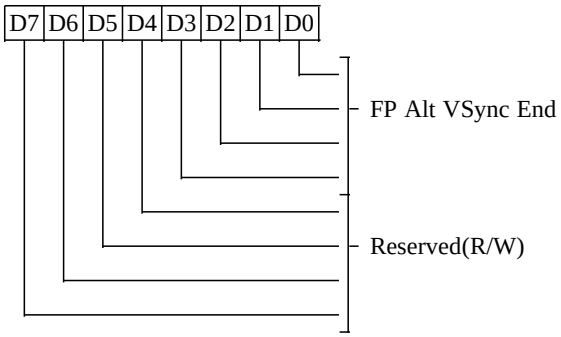
This register is used in all flat panel modes.

7-0 FP Alternate Vertical Sync Start

The contents of this register are the 8 low order bits of a 10-bit value. Bits 9 and 10 are defined in XR65. This value defines the scan line position at which vertical sync becomes active. Similar to CR10.

Programmed Value = Actual Value – 1

FP ALTERNATE VERTICAL SYNC END REGISTER (XR67)
Read/Write at I/O Address 3D7h
Index 67h



This register is used in all flat panel modes.

3-0 FP Alternate Vertical Sync End

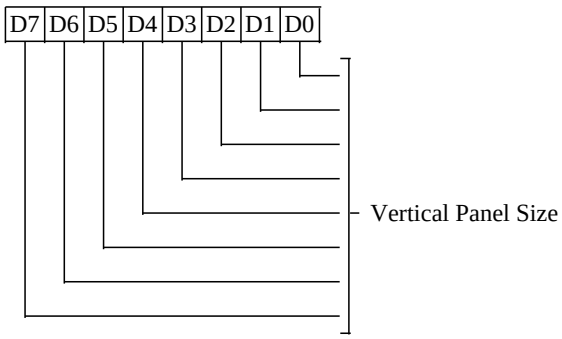
The lower 4 bits of the scan line count that defines the end of vertical sync. Similar to CR11. If the vertical sync width desired is N lines, the programmed value is:

(contents of XR66 + N) ANDed with 0FH

7-4 Reserved (R/W)

VERTICAL PANEL SIZE REGISTER (XR68)

Read/Write at I/O Address 3D7h
Index 68h



This register is used in all flat panel modes.

7-0 Vertical Panel Size

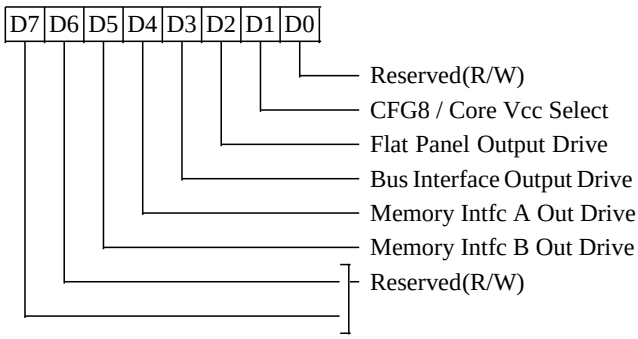
The contents of this register define the number of scan lines per frame.

Programmed Value = Actual Value – 1

Panel size bits 8-9 are defined in overflow register XR65.

PROGRAMMABLE OUTPUT DRIVE REGISTER (XR6C)

Read/Write at I/O Address 3D7h
Index 6Ch



This register is used to control the output drive of the bus, video, and memory interface pins.

0 Reserved (R/W)

1 CFG8 - Core Vcc Selection

This bit determines pad input threshold. On the falling edge of RESET, this bit will latch the state of AA8 pin (CFG8).

0 VCC for internal logic is 3.3V
1 VCC for internal logic is 5V (Default)

2 Flat Panel Interface Output Drive Select

0 Lower drive (Default)
1 Higher drive (doubles the rated output drive)

3 Bus Interface Output Drive Select

0 Higher drive (Default) (doubles the rated drive)
1 Lower drive

4 Memory Interface A Output Drive Select

This bit affect memory interface group A control pins: RASA#, CASAH#, CASAL#, and WEA#.

0 Lower drive (Default)
1 Higher drive (doubles the rated output drive)

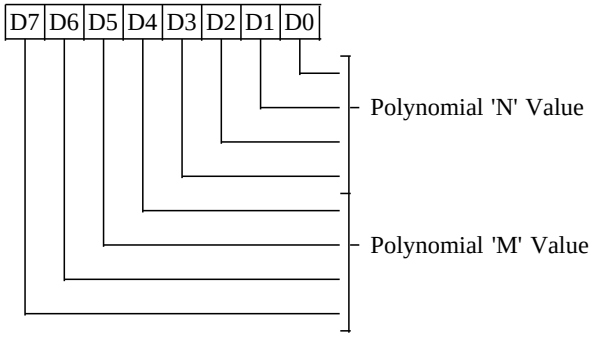
5 Memory Interface B Output Drive Select

This bit affect memory interface group A pins: RASB#, CASBH#, CASBL#, WEB#, and MBD15:0

0 Lower drive (Default)
1 Higher drive (doubles the rated output drive)

7-6 Reserved (R/W)

POLYNOMIAL FRC CONTROL REGISTER (XR6E)
Read/Write at I/O Address 3D7h
Index 6Eh



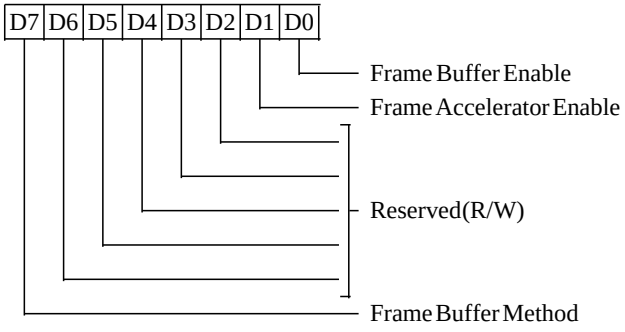
This register is effective in flat panel mode when polynomial FRC is enabled (see XR50 bits 0-1). It is used to control the FRC polynomial counters. The values in the counters determine the offset in rows and columns of the FRC count. These values are usually determined by trial and error.

3-0 Polynomial 'N' value

7-4 Polynomial 'M' value

This register defaults to '10111101' on RESET.

FRAME BUFFER CONTROL REGISTER (XR6F)
Read/Write at I/O Address 3D7h
Index 6Fh



This register is effective in flat panel mode only.

0 Frame Buffer Enable

This bit is used to enable the external frame buffer. Frame buffering and frame acceleration are required for simultaneous CRT and DD/DS panel operation. In case of simultaneous CRT and plasma or SS panels, the frame buffer is not used therefore thsese bits should be set to 0. The frame buffer with acceleration is always required to drive LCD DD panels.

0 Disable frame buffer (default)
1 Enable frame buffer

1 Frame Accelerator Enable

This bit should always be set to 1 for DD flat panels. This bit should be programmed to 0 when XR6F[0] = 0 or for non-DD panels.

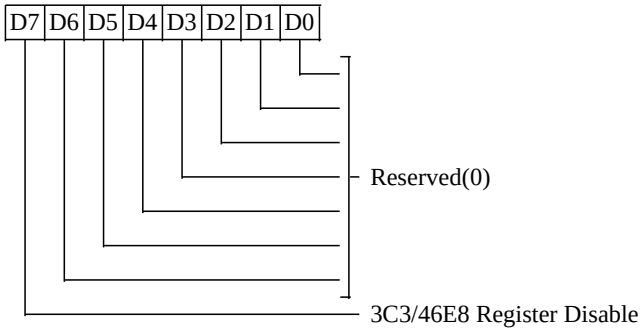
0 Disable frame accelerator (default)
1 Enable frame accelerator

6-2 Reserved (R/W)

7 Frame Buffer Method

0 Frame buffer is stored in upper portion of display memory
1 Reserved

SETUP / DISABLE CONTROL REGISTER (XR70)
Read/Write at I/O Address 3D7h
Index 70h



6-0 Reserved (0)

7 3C3 / 46E8 Register Disable

0 In the MC and PI bus, port 3C3h works as defined to provide control of VGA disable. In the ISA bus, port 46E8h works as defined to provide control of VGA setup and disable modes (setup and disable functions are not provided on pins).

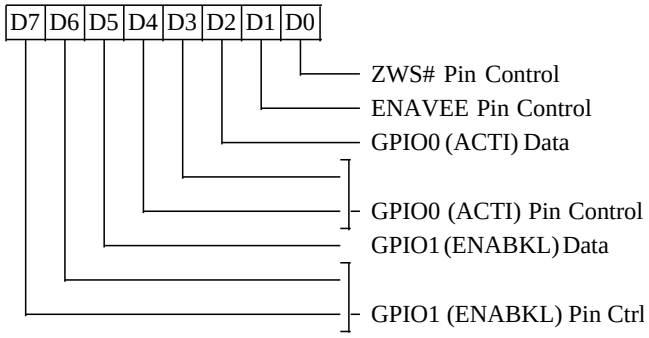
1 In the MC and PI bus, writes to I/O port 3C3 have no effect. In the ISA bus, writes to I/O port 46E8h have no effect (the VGA remains enabled and will not go into setup mode).

Note: Writes to register 46E8 are only effective in ISA bus configurations (46E8 is ignored in MC and PI bus configurations independent of the state of this bit). Writes to 3C3 are only effective in MC and PI bus configurations (3C3 is ignored in ISA bus configurations independent of the state of this bit).

Reads from ports 3C3 and 46E8h have no effect independent of the programming of this register (both 3C3 and 46E8h are write-only registers).

This register is cleared by reset.

EXTERNAL DEVICE I/O REGISTER (XR72)
Read/Write at I/O Address 3D7h
Index 72h



0 ZWS# Pin Control

This bit is effective when XR01[3]=1.

0 Pin 38 is used as ZWS# (Zero Wait State) for ISA bus or POS# for Micro Channel bus (default on reset).
1 Pin 38 is used as IRQ for ISA or Micro Channel bus.

1 ENAVEE Pin Control

0 Pin 47 is used as Enable VEE (ENAVEE) output (default on reset)
1 Pin 47 is used as Enable Backlight (ENABKL) output

2 GPIO0 (ACTI) Data

This bit always reads back the state of the ACTI pin (pin 75). When ACTI is configured as general purpose output (XR72[4-3]=11) this bit determines the data output on ACTI pin.

4-3 GPIO0 (ACTI) Pin Control

This bit is effective only when XR01[4]=1 and XR50[7]=0.

00 Pin 75 is ACTI output (default on reset)
01 Reserved
10 Pin 75 is general purpose input 0 (GPIO0)
11 Pin 75 is general purpose output 0 (GPIO0)

5 GPIO1 (ENABKL) Data

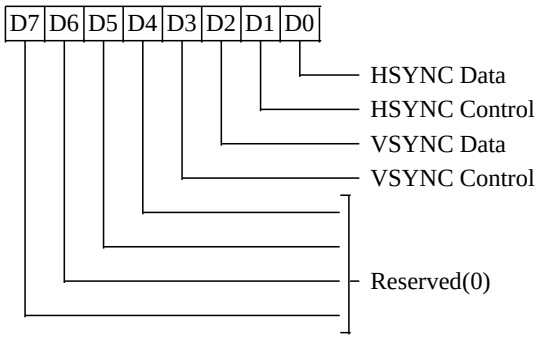
This bit always reads back the status of the ENABKL pin (pin 76). When ENABKL is configured as general purpose output (XR72[7-6]=11), this bit determines the data output on the ENABKL pin.

7-6 GPIO1 (ENABKL) Pin Control

This bit is effective only when XR01[4]=1 and XR50[7]=0.

00 Pin 76 is used to output ENABKL (enable backlight) (default on reset)
01 Reserved
10 Pin 76 is general purpose input 1 (GPIO1)
11 Pin 76 is general purpose output 1 (GPIO1)

DPMS CONTROL REGISTER (XR73)
Read/Write at I/O Address 3D7h
Index 73h



This register is provided to allow the controller to independently shut down either or both of the HSYNC and VSYNC outputs. This capability allows the controller to signal a CRT monitor to enter power-saving states per the VESA DPMS (Display Power Management Signaling) Standard. The DPMS states are:

H	V	Power Management State
Active	Active	Normal Operation
Inactive	Active	Standby (Quick Recovery) Opt
Active	Inactive	Suspend (Max Power Savings)
Inactive	Inactive	Off (Autorecovery is optional)

0 HSYNC Data

If XR73 bit-1 (bit-1 of this register) is programmed to 1, the state of this bit will be output on HSYNC (pin 51).

1 HSYNC Control

Determines whether bit-0 of this register or internal CRTC horizontal sync information is output on HSYNC (pin 51).

0 CRTC HSYNC is output (Default)
1 XR73[0] is output

2 VSYNC Data

If XR73 bit-3 (bit-3 of this register) is programmed to 1, the state of this bit will be output on VSYNC (pin 50).

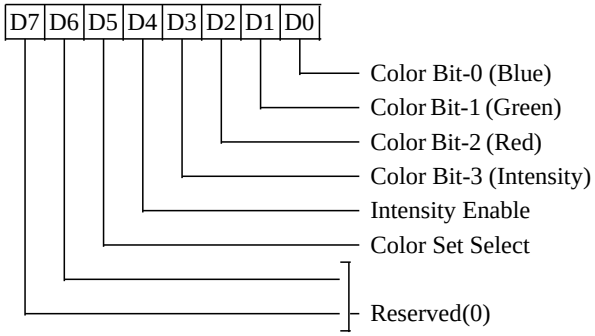
3 VSYNC Control

Determines whether bit-2 of this register or internal CRTC vertical sync information is output on VSYNC (pin 50).

0 CRTC VSYNC is output (Default)
1 XR73[2] is output

7-4 Reserved (0)

CGA/HERCULES COLOR SELECT REGISTER (XR7E)
Read/Write at I/O Address 3D7h
Index 7Eh

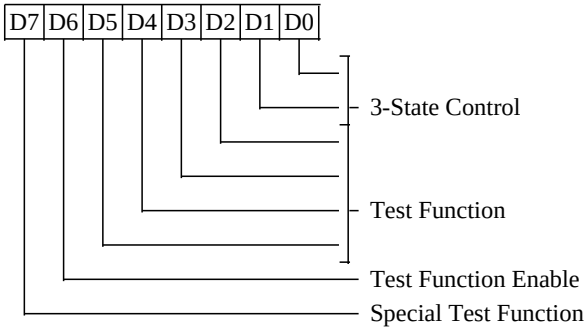


This I/O address is mapped to the same register as I/O address 3D9h. This alternate mapping effectively provides a color select register for Hercules mode. Writes to this register will change the copy at 3D9h. The copy at 3D9h is visible only in CGA emulation. The copy at XR7E is always visible.

5-0 See Register 3D9

7-6 Reserved (0)

DIAGNOSTIC REGISTER (XR7F)
Read/Write at I/O Address 3D7h
Index 7Fh



0 3-State Control Bit 0

0 Normal outputs (default on Reset)
1 3-state output pins: HSYNC, VSYNC, FLM, LP, M (ACDCLK), P15-0, SHFCLK, ACTI, ENABKL, ENAVDD, and ENAVEE.

1 3-State Control Bit 1

0 Normal outputs (default on Reset)
1 3-state output pins: RASA#, RASB#, CASAL#, CASAH#, CASBL#, CASBH#, WEA#, WEB#, and AA0-9.

5-2 Test Function

These bits are used for internal testing of the chip when bit-6 = 1.

6 Test Function Enable

This bit enables bits 5-2 for internal testing.

0 Disable test function bits (default)
1 Enable test function bits

7 Special Test Function

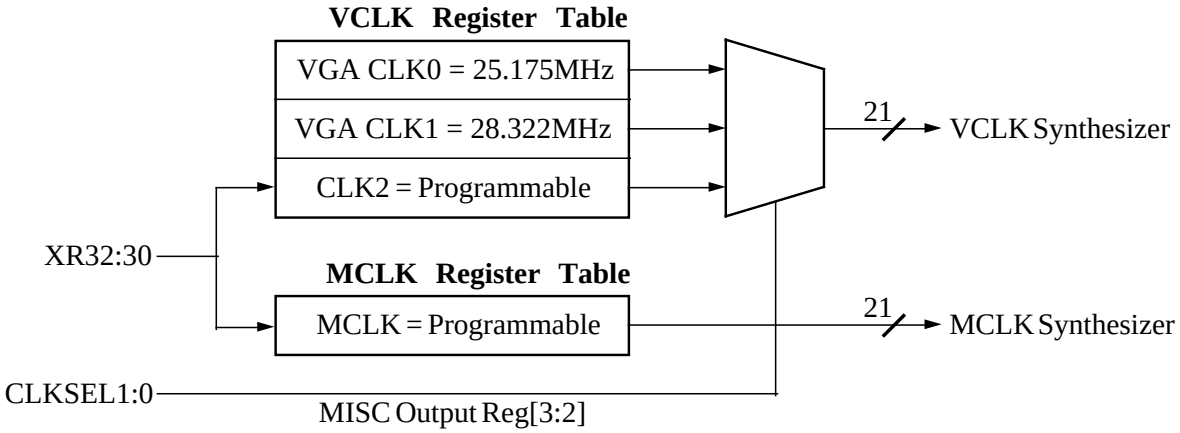
This bit is used for internal testing and should be set to 0 (default to 0 on reset) for normal operation.

Clock Synthesizer

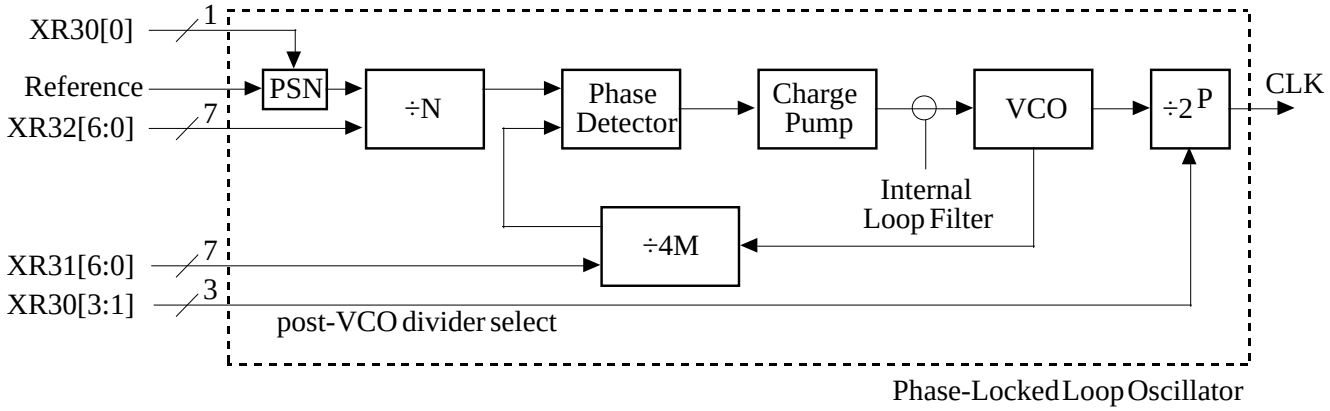
An integrated clock synthesizer supports all required pixel clock (VCLK) and memory clock (MCLK) frequencies. Each of the two phase lock loops may be programmed to output frequencies ranging between 1MHz and the maximum specified operating frequency for that clock in increments not exceeding 0.5%. The frequencies are generated by an 18-bit divisor word. This value contains fields for the Phase Lock Loop (PLL), Voltage Controlled Oscillator (VCO) and Pre/Post Divide Control blocks. The divisor word for both synthesizers is programmable via Clock Control Registers XR30-32.

MCLK Operation

Normal operational frequencies for MCLK are between 50MHz and 68MHz. Refer to the Electrical Specifications for maximum frequencies at 3.3V and 5V (the maximum frequency at 3.3V will be slightly lower). Normal MCLK operational frequencies are defined by the display memory sequencer parameters described in the Memory Timing section. The frequency selected is also dependent upon the AC characteristics of the display memories connected to the 65535. A typical match is between industry standard 70ns access memories and a 65MHz MCLK. The MCLK output defaults to 60MHz on reset and is fully programmable. This initial value is conservative enough not to violate slow DRAM parameters but not so slow as to cause a system timeout on CPU accesses. The MCLK frequency must always equal or exceed the host clock (CCLK) frequency.



Clock Synthesizer Register Structure



Clock Synthesizer PLL Block Diagram

VCLK Operation

The VCLK output typically ranges between 19MHz and 65MHz. VCLK has a table of three frequencies from which to select a frequency. This is required for VGA compatibility. CLK0 and CLK1 are fixed at the VGA compatible frequencies of 25.175MHz and 28.322MHz respectively. These values can not be changed unlike CLK2 which is fully programmable. The active frequency is chosen by clock select bits MSR[3:2].

Programming the Clock Synthesizer

The desired output frequency is defined by an 18-bit value programmed in XR30-32. The 65535 has two programmable clock synthesizers; one for memory (MCLK) and one for video (VCLK). They are both programmed by writing the divisor values to XR30-32. The clock to be programmed is selected by the Clock Register Program Pointer XR33[5]. The output frequency of each of the clock synthesizers is based on the reference frequency (FREF) and the 4 programmed fields:

Field	# Bits	
Prescale N (PSN)	**XR30[0]**	**(÷1 or ÷4)**
M counter (M')	**XR31[6:0]**	**(M' = M - 2)**
N counter (N')	**XR32[6:0]**	**(N' = N - 2)**
Post Divisor (P)	**XR30[3:1]**	**($\div 2^P$; $0 \le P \le 5$)**

$$F_{OUT} = \frac{F_{REF} * 4 * M}{PSN * N * 2^P}$$

The frequency of the Voltage Controlled Oscillator (FVCO) is determined by these fields as follows:

$$F_{VCO} = \frac{F_{REF} * 4 * M}{PSN * N}$$

where FREF = Reference frequency (between 4 MHz - 20 MHz; typically 14.31818 MHz)

Note: If a reference frequency other than 14.31818 MHz is used, then the frequencies loaded on RESET will not be correct.

P	Post Divisor
000	1
001	2
010	4
011	8
100	16
101	3

Programming Constraints

There are five primary programming constraints the programmer must be aware of:

$$4 \text{ MHz} \le F_{REF} \le 20 \text{ MHz}$$

$$150 \text{ KHz} \le F_{REF}/(PSN * N) \le 2 \text{ MHz}$$

$$48 \text{ MHz} < F_{VCO} \le 220 \text{ MHz}$$

$$3 \le M \le 127$$

$$3 \le N \le 127$$

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation.

The value of FVCO must remain between 48 MHz and 220 MHz inclusive. Therefore, for output frequencies below 48 MHz, FVCO must be brought into range by using the post-VCO Divisor.

To avoid crosstalk between the VCO's, the VCO frequencies should not be within 0.5% of each other nor should their harmonics be within 0.5% of the other's fundamental frequency.

The 65535 clock synthesizers will seek the new frequency as soon as it is loaded following a write to XR32. Any change in the post-divisor will take affect immediately. There is a possibility that the output may glitch during this transition of post divide values. Because of this, the programmer may wish to hold the post-divisor value constant across a range of frequencies (eg. changing MCLK from the reset value of 50MHz to 65MHz). There is also the consideration of changing from a low frequency VCO value with a post-divide ÷1 (eg. 50MHz) to a high frequency ÷4 (eg. 220MHz). Although the beginning and ending frequencies are close together, the intermediate frequencies may cause the 65535 to fail in some environments. In this example there will be a short-lived time frame during which the output frequency will be in the neighborhood of 12.5MHz. The bus interface may not function correctly if the MCLK frequency falls below a certain value. Register and memory accesses which are synchronized to MCLK may be so slow as to violate bus timing and cause a watchdog timer error. Programmers should time-out the system (CPU) for approximately 10ms after writing XR32 before accessing the VGA again. This will ensure that accesses do not occur to the VGA while the clocks are in an indeterminate state.

Note: On reset the MCLK is initialized to a 60MHz output with a post divisor = 2 (FVCO = 120MHz).

Programming Example

The following is an example of the calculations which are performed:

Derive the proper programming word for a 25.175 MHz output frequency using a 14.31818 MHz reference frequency:

Since 25.175 MHz < 48 MHz, double it to 50.350 MHz to get FVCO in its valid range. Set the post divide field (P) to 001.

Prescaling PSN = 4

The result:

FVCO = 50.350 = (14.31818 x 4 x M/4 x N)

M/N = 3.51655

Several choices for M and N are available:

M	N	FVCO	Error
109	31	50.344	-0.00300
102	29	50.360	+0.00500

Choose (M, N) = (109,31) for best accuracy.

Prescaling PSN = 1

The result:

FVCO = 50.350 = (14.31818 x 4 x M/1 x N)

M/N = 0.879127

M	N	FVCO	Error
80	91	50.349	-0.00050

FREF/(PSN x N) = 157.3KHz

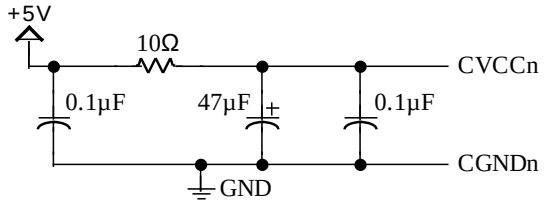
Therefore M/N = 80/91 with PSN = 1 is even better than with PSN = 4.

XR30 = 0000010b (02h)
XR31 = 80 - 2 = 78 (4Eh)
XR32 = 91 - 2 = 89 (59h)

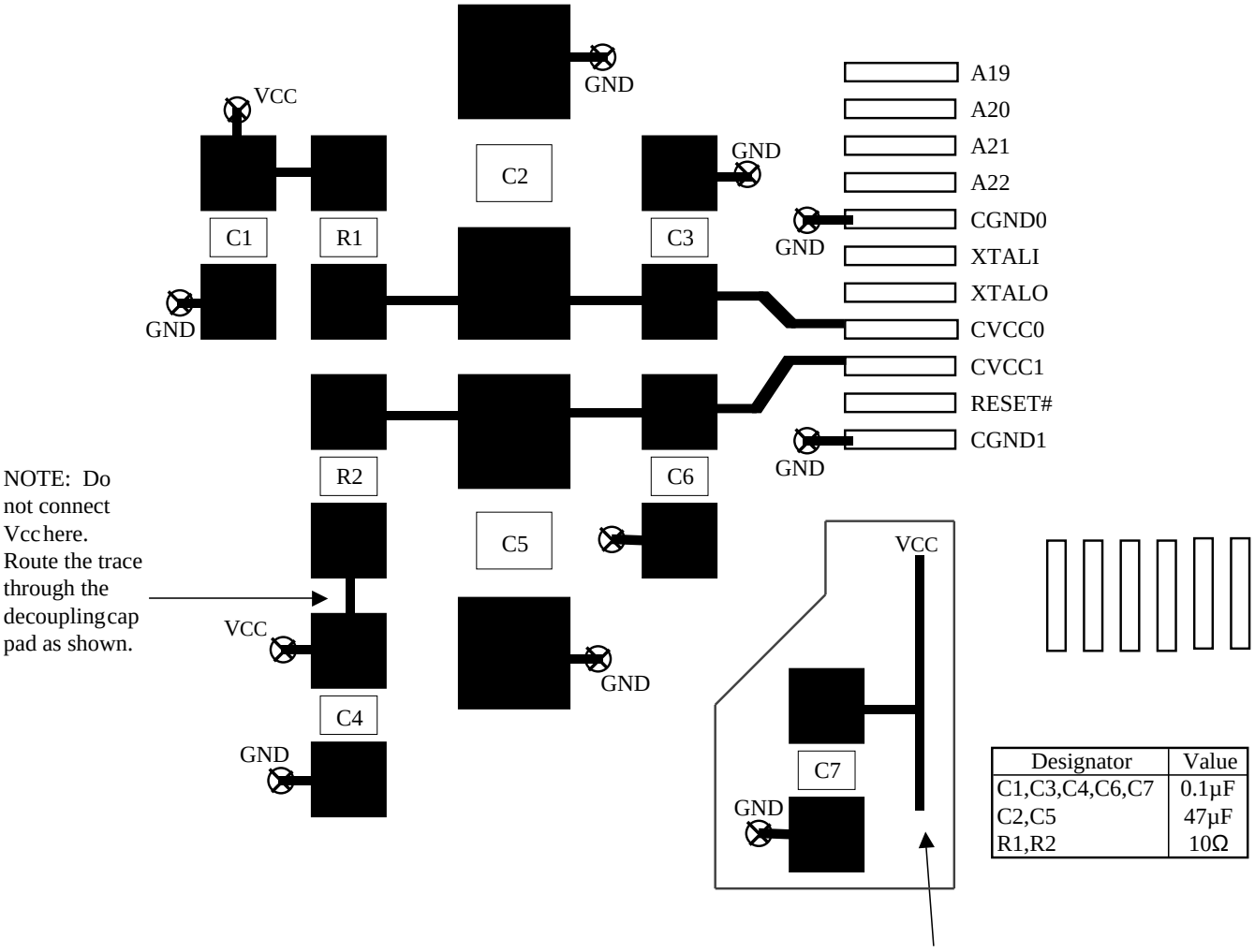
Clock Synthesizer PCB Layout Considerations

Clock synthesizers, like most analog components, must be isolated from the digital noise which exists on a PCB power plane. Care must be taken not to route any high frequency digital signals in close proximity to the analog sections. Inside the 65535, the clocks are physically located in the lower left corner of the chip surrounded by low frequency input and output pins. This helps minimize both internally and externally coupled noise.

The memory clock and video clock power pins on the 65535 each require similar RC filtering to isolate the synthesizers from the VCC plane and from each other. The filter circuit for each CVCCn / CGNDn pair is shown in the figure to the right:



The suggested method for layout assumes a multi-layer board including VCC and GND planes. All ground connections should be made as close to the pin / component as possible. The CVCC trace should route from the 65535 **through the pads** of the filter components. The trace should NOT be connected to the filter components by a stub. All components (particularly the initial 0.1µF capacitor) should be placed as close as possible to the 65535.



Designator	Value
C1,C3,C4,C6,C7	0.1µF
C2,C5	47µF
R1,R2	10Ω

Always pass the Vcc trace through the decoupling cap pad. Do not leave a stub as shown here.

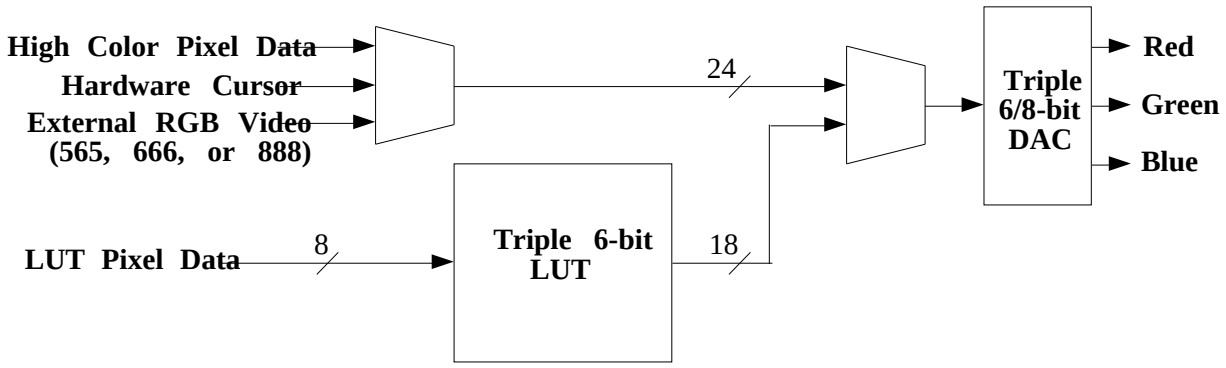
VGA Color Palette DAC

The 65535 integrates a VGA compatible triple 6-bit lookup table (LUT) and high speed 6/8-bit DACs. Additionally the internal color palette DAC supports true-color bypass modes displaying color depths up to 24bpp (8-8-8). The palette DAC can switch between true-color data and LUT data on a pixel by pixel basis. Thus, video overlays may be any arbitrary shape and can lie on any pixel boundary. The hardware cursor is also a true-color bitmap which may overlay both video and graphics on any pixel boundary.

The internal palette DAC register I/O addresses and functionality are 100% compatible with the VGA standard. In all bus interfaces the palette DAC automatically controls accesses to its registers to avoid data overrun. This is accomplished by holding RDY in the ISA configuration and by delaying LRDY# for VL-Bus and direct processor interfaces.

For compatibility with the VL-Bus Specification the 65535 may be disabled from responding to palette writes (although it will perform them) so that an adapter card on a slow (ISA) bus which is shadowing the palette LUT may see the access. The 65535 always responds to palette read accesses so it is still possible for the shadowing adapter to become out of phase with the internal modulo-3 RGB pointer. It is presumed that this will not be a problem with well-behaved software.

Extended display modes may be selected in the Palette Control Register (XR06). Two 16bpp formats are supported: 5-5-5 Targa format and 5-6-5 XGA format.



VGA Color Palette DAC Data Flow

Flat Panel Timing

Overview

A number of extension registers in the 65535 control the panel interface, including the functions of the interface pins and the timing sequences produced for compatibility with various types of panels. Some key registers of interest for panel interfacing are:

XR06 Color Reduction Select
XR1C H Panel Size (# of characters – 1)
XR68 V Panel Size (# of scan lines – 1) bits 0-7
(XR65[1]=Vsize bit-8, XR65[6]=bit-9)

XR4F Panel Format 2 (Bits/pixel,M/LP function)
XR50 Panel Format 1 (FRC,dither,clkdiv,VAM)
XR51 Display Type (Panel type, clk/LP control)
XR53 Panel Format 3 (FRC opt, pixel packing)
XR54 Panel Interface (FLM/LP Control)
XR5E M (ACDCLK) Control
XR6F Frame Buffer Control

This section summarizes the function of the various fields of the above registers as they pertain to panel interfacing. Detailed timing diagrams are shown for output of data and control sequences to a variety of panel types. The 65535 highly configurable controllers can interface to virtually all existing monochrome LCD, EL, and Plasma panels and all color LCD STN and TFT panels. The panel types supported are:

Single panel-Single drive (SS) Monochrome
1 pixel/clock, 8 bits/pixel
2 pixels/clock, 8 bits/pixel
4 pixels/clock, 4 bits/pixel
8 pixels/clock, 2 bit/pixel
16 pixels/clock, 1 bit/pixel

Dual panel-Double drive (DD) Monochrome
8 pixels/clock, 1 bit/pixel
16 pixels/clock, 1 bit/pixel

Single panel-Single drive (SS) Color TFT
1 pixel/clock, 15 bit/pixel 5-5-5 RGB
1 pixel/clock, 18 bit/pixel 6-6-6 RGB

Single panel-Single drive (SS) Color STN
2 2/3 pixels/clock, 3 bit/pixel 1-1-1 RGB
5 1/3 pixels/clock, 3 bit/pixel 1-1-1 RGB

Dual panel-Double drive (DD) Color STN
2 2/3 pixels/clock, 3 bit/pixel 1-1-1 RGB
5 1/3 pixels/clock, 3 bit/pixel 1-1-1 RGB

Panel Size

The horizontal panel size register (XR1C) is an 8-bit register programmed with panel width (minus one) in units of 8-pixel characters (e.g., a 640x480 panel is 80 'characters' wide so XR1C would be programmed with 79 decimal). The vertical panel size register is programmed with the panel height (minus one) in scan lines (independent of single or dual panel type). The programmed value is 10 bits in size with the 8 lsbs in XR68 and the overflow in XR65 bits 1 and 6. The maximum panel resolution supported is 2048x1024.

Panel Type

The panel type (PT) is determined by XR51 bits 1-0:

00 Single panel-Single drive (SS)
11 Dual panel-Double drive (DD)

For DD panels, XR6F bit-0 (Frame Buffer Enable) and/or bit-1 (Frame Accelerator Enable) must also be set (either external or embedded may be used).

TFT Panel Data Width

XR50 bit-7 controls output width for TFT panels:

0 15-bit color TFT panel interface (555 RGB)
1 18-bit color TFT panel interface (666 RGB)

Color Reduction Select

XR06 bits 7-6 determines color versus monochrome output: 11 selects color, all others select monochrome (they select the algorithm used to reduce 18-bit color data to 8-bit or 6-bit data for monochrome panels).

00 NTSC Weighting
01 Equivalent Weighting
10 Green Only Weighting
11 Color (no reduction)

Display Quality Settings

Frame Rate Control (FRC)

The 65535 provides 2 and 16 level FRC to generate multiple gray / color levels. FRC selection is determined by XR50 bits 1-0:

00 No FRC
01 16-frame FRC (color or mono STN panels)
10 2-frame FRC (color TFT or mono panels)

Three options are provided for FRC control:

FRC option 1 (XR53[2]) (always set to 1)
FRC option 2 (XR53[3]) (always set to 1)
FRC option 3 (XR53[6]) (for 2-frame FRC only):

0 FRC data changes every frame
1 FRC data changes every other frame

A setting of 0 typically results in better display quality, but panels with an internal 'M' signal typically recommend this bit be set to 1 for longer panel life.

XR6E is also provided for FRC polynomial control. The values of the 'm' and 'n' parameters are typically set by trial and error (recommended settings are given elsewhere in this manuals for selected panels as derived by Chips and Technologies).

Dither

The 65535 also provides Dither capability to generate multiple gray / color levels. Dither selection is determined by XR50 bits 3-2:

00 No Dither
01 Enable Dither for 256-color modes only
10 Enable Dither for all modes

M Signal Timing

Register XR5E (M/ACDCLK Control) is provided to control the timing of the M (sometimes called ACDCLK) signal. XR5E bit-7 selects between two types of timing control:

0 Use XR5E bits 0-6 to determine M signal timing (bits 0-6 are programmed with the number of HSYNCs between phase changes minus 2)
1 M phase changes every frame if the frame buffer is used, otherwise the phase changes every other frame

XR4F bit-6 controls the M pin output. If set, the M pin will output flat panel BLANK# / Display Enable (DE) instead of the normal M signal (and XR5E will be ignored).

Gray / Color Levels

Gray / color levels are selected via XR4F bits 2-0 (somewhat misleadingly called 'Bits Per Pixel'):

No FRC

	# of msbs Used to Generate Gray/Color Levels	Gray / Color Levels	Gray / Color Levels with Dithering
001	1	2	5
010	2	4	13
011	3	8	13
100	4	16	61
101	5	32	125
110	6	64	253
111	8	256	n/a

2-Frame FRC
(Color TFT or Monochrome Panels)

	# of msbs Used to Generate Gray/Color Levels	Gray / Color Levels	Gray / Color Levels with Dithering
010	1	3	9
011	2	7	25
100	3	15	57
101	4	32	125

16-Frame FRC
(Color or Monochrome STN Panels)

	# of msbs Used to Generate Gray/Color Levels	Gray / Color Levels	Gray / Color Levels with Dithering
001	1	2	5
010	2	4	13
011	3	8	29
100	4	16	61

The setting programmed into XR4F bits 0-2 above determines how many most-significant color-bits / pixel are used to generate flat panel video data. In general, 8 bits of monochrome data or 8 bits/color of RGB color data enter the flat panel logic for every dot clock. Not all of these bits, however, are used to generate output colors / gray scales, depending on the type of panel used, graphics / text mode, and the gray-scaling algorithm chosen (the actual number of bits used is indicated in the table above). Also note that settings which achieve higher gray / color levels may not necessarily produce acceptable display quality on some (or any) currently available panels. This document contains recommended settings for various popular panels that have been found to produce acceptable results with those panels. Customers may modify these settings to achieve a better match with their requirements.

Pixels Per Shift Clock

The 65535 can be programmed to output 1, 2, 4, 8, or 16 pixels per shift clock. This is achieved by programming the frequency ratio between the dot clock and the shift clock. The shift clock divide (CD) is set by XR50 bits 6-4. For monochrome panels, the valid settings are:

	Shift Clock	Pixels Per Shift Clock without Frame Acceleration	Pixels Per Shift Clock with Frame Acceleration
000	Dot clk	1	2
001	Dclk / 2	2	4
010	Dclk / 4	4	8
011	Dclk / 8	8	16
100	Dclk / 16	16	n/a

Pixels Per Shift Clock	8-Bit Panel Interface	Valid Outputs (8-bit)	16-Bit Panel Interface	Valid Outputs (16-bit)
1	8bpp	P8-15	8bpp	P8-15
2	4bpp	P8-15 (8-11 1st)	8bpp	P0-15
4	2bpp	P8-15 (8-9 1st)	4bpp	P0-15
8	1bpp	P1,3,5,... (1 1st)	2bpp	P0-15
16	n/a	n/a	1bpp	P0-15

The pixel on the lowest numbered output pin is always the first pixel output (the pixel shown first on the left side of the screen). For example, for 8 pixels per clock, 1bpp on an 8-bit interface, P1 is the first pixel, P3 is the second, etc. For 16 pixels per clock, 1bpp on a 16-bit interface, P0 is the first pixel, P1 is the second, etc. For 4 pixels per clock, 2bpp on an 8-bit interface, P8-9 is the first pixel, P10-11 is the second, etc. Data output mappings for SS panels for more than 1bit/pixel are shown in more detail below:

	18bit Color	18bit Color	15bit Color	15bit Color	8bit Mono	16bit Mono	16bit Mono	16bit Mono
Pix/clk:	1	2	1	2	1	2	4	8
CD:	000	001	000	001	000	001	010	011
P0	B2n	B5n	B3n	B6n	–	G0n	G4n	G6n
P1	B3n	B6n	B4n	B7n	–	G1n	G5n	G7n
P2	B4n	B7n	B5n	B5n+1	–	G2n	G4n+1	G6n+1
P3	B5n	B5n+1	B6n	B6n+1	–	G3n	G5n+1	G7n+1
P4	B6n	B6n+1	B7n	B7n+1	G0n†	G0n+1	G4n+2	G6n+2
P5	B7n	B7n+1	G3n	G6n	G1n†	G1n+1	G5n+2	G7n+2
P6	G2n	G5n	G4n	G7n	G2n†	G2n+1	G4n+3	G6n+3
P7	G3n	G6n	G5n	G5n+1	G3n†	G3n+1	G5n+3	G7n+3
P8	G4n	G7n	G6n	G6n+1	G0n	G4n	G6n	G6n+4
P9	G5n	G5n+1	G7n	G7n+1	G1n	G5n	G7n	G7n+4
P10	G6n	G6n+1	R3n	R6n	G2n	G6n	G6n+1	G6n+5
P11	G7n	G7n+1	R4n	R7n	G3n	G7n	G7n+1	G7n+5
P12	R2n	R5n	R5n	R5n+1	G4n	G4n+1	G6n+2	G6n+6
P13	R3n	R6n	R6n	R6n+1	G5n	G5n+1	G7n+2	G7n+6
P14	R4n	R7n	R7n	R7n+1	G6n	G6n+1	G6n+3	G6n+7
P15	R5n	R5n+1	–	–	G7n	G7n+1	G7n+3	G7n+7
P16	R6n	R6n+1	–	–	–	–	–	–
P17	R7n	R7n+1	–	–	–	–	–	–

† For information only, not recommended for panel connections

The number of bits per pixel is determined as follows:

1bpp: Bits/Pixel=000 or 001 or
16-Frame FRC or
2-Frame FRC with Bits/Pixel=010

2bpp: Not 1bpp and CD=011 (8 Pixels/Clock)

4bpp: Not 1bpp and CD=010 (4 Pixels/Clock)

8bpp: Not 1bpp and CD=001 (2 Pixels/Clock) or
Not 1bpp and CD=000 (1 Pixels/Clock)

Valid Color TFT panel shift clock divide settings are:

	Pixels per Shift Clock	TFT Output Width	TFT Output Format	"B0-n" Panel Outputs	"G0-n" Panel Outputs	"R0-n" Panel Outputs
000	1	15	5-5-5	P0-4	P5-9	P10-14
		18	6-6-6	P0-5	P6-11	P12-17

For Color STN, valid shift clock divide settings are:

	Pixels Per Clock without FrameAcceleration SS or DD Panels	Pixels Per Clock with FrameAcceleration DD Panels Only
000	1	2
001	2	4
010	4	n/a

For Color STN data, pixel output sequences are controlled by the 'Color STN Pixel Packing' bits (XR53[5-4]) described on the following page (packing may be selected as '3-Bit Pack', '4-Bit Pack', or 'Extended 4-Bit Pack' sometimes referred to in this document as 3bP, 4bP, and X4bP). All cases in the above table can use 3-Bit Pack or 4-Bit Pack. Extended 4-Bit Pack is only used for the single case of 2 pixels per shift clock without frame acceleration. Pixel Packing is not used for EL/Plasma, Monochrome DD, or Color TFT panels so the pixel packing bits should be set to 00 for all panels except color STN.

Shift Clock Divide

The above clock divide ('CD') bits (XR50 bits 6-4) affect both shift clock and data out. XR51[3] (Shift Clock Divide or SD) may be set so that only the shift clock (and not the video data) is further divided by two beyond the setting of XR50 bits 6-4. This has the effect of causing a new pixel to be output on every clock edge (i.e., both rising and falling) instead of just every falling clock edge (the first pixel output on every scan line will be on the rising edge).

Extended 4-Bit Pack for Color STN panels requires the SD bit (XR51[3]) to be set to 1. In all other cases in the Color STN table above, either setting may be used.

Color STN Pixel Packing (Pixel Output Order)

For color STN panels, pixel packing must be selected via XR53 bits 5-4:

	Packing	CD Settings Allowable
00	3-Bit Pack	SS: 000, 001, or 010 DD: 000, 001 (010 w/o FA)
01	4-Bit Pack	SS: 000, 001, or 010 DD: 000, 001 (010 w/o FA)
11	Ext'd 4-Bit Pack	SS: 001 (8bit panels only)

These settings are valid for color STN panels only (these bits must be set to 00 for monochrome and color TFT panels).

Pixel output order for 3-Bit Pack STN-SS panels without frame acceleration:

	CD=000 (1p/clk) ShfClk Edge				CD=001 (2p/clk) Shift Clock Edge				CD=010 (4p/clk) Shift Clock Edge			
	1st	2nd	3rd	4th	1st	2nd	3rd	4th	1st	2nd	3rd	4th
P0	–	–	–					...				...
P1	R1	R2	R3	...	R1	R3	R5	...	R1	R5	R9	...
P2	G1	G2	G3	...	G1	G3	G5	...	G1	G5	G9	...
P3	B1	B2	B3	...	B1	B3	B5	...	B1	B5	B9	...
P4	–	–	–		–	–	–		–	–	–	
P5	–	–	–		R2	R4	R6	...	R2	R6	R10	...
P6	–	–	–		G2	G4	G6	...	G2	G6	G10	...
P7	–	–	–		B2	B4	B6	...	B2	B6	B10	...
P8	–	–	–		–	–	–					...
P9	–	–	–		–	–	–		R3	R7	R11	...
P10	–	–	–		–	–	–		G3	G7	G11	...
P11	–	–	–		–	–	–		B3	B7	B11	...
P12	–	–	–		–	–	–		–	–	–	
P13	–	–	–		–	–	–		R4	R8	R12	...
P14	–	–	–		–	–	–		G4	G8	G12	...
P15	–	–	–		–	–	–		B4	B8	B12	...

	4b Pack, CD=001 Shift Clock Edge				Ext'd 4b Pack, CD=001 Shift Clock Edge						
	1st	2nd	3rd	4th	1st	2nd	3rd	4th	5th	6th	7th
P0	R1	B3	G6	...	R1	G1	G6	B6	B11	R12	...
P1	G1	R4	B6	...	B1	R2	R7	G7	G12	B12	...
P2	B1	G4	R7	...	G2	B2	B7	R8	R13	G13	...
P3	R2	B4	G7	...	R3	G3	G8	B8	B13	R14	...
P4	G2	R5	B7	...	B3	R4	R9	G9	G14	B14	...
P5	B2	G5	R8	...	G4	B4	B9	R10	R15	G15	...
P6	R3	B5	G8	...	R5	G5	G10	B10	B15	R16	...
P7	G3	R6	B8	...	B5	R6	R11	G11	G16	B16	...

The pixel sequence for 3-bit Pack repeats with either 1, 2, or 4 pixels every shift clock edge depending on the setting of the clock divide (CD) field. The pixel sequence for 4-bit Pack repeats with 8 pixels every 3 shift clock edges. The sequence for Extended 4-Bit Pack repeats with 16 pixels every 6 shift clock edges. Extended 4-bit Pack is used only for 8-bit color STN-SS panels. It is not used for color STN DD panels or for 16-bit color STN interfaces.

Pixel output order for 4-Bit Pack 8-bit STN DD panels:

	Shift Clock Edge			
	1st	2nd	3rd	4th
Upper:				
P0	R1	G2	B3	...
P1	G1	B2	R4	...
P2	B1	R3	G4	...
P3	R2	G3	B4	...
Lower:				
P4	R1	G2	B3	...
P5	G1	B2	R4	...
P6	B1	R3	G4	...
P7	R2	G3	B4	...

The pixel sequence repeats with 8 pixels (4 for each of the upper and lower panels) every 3 shift clock edges. Clock divide must be set to 000 with Frame Acceleration and 001 without Frame Acceleration.

Pixel output order for 16-bit STN panels (4bit Pack):

	STN-SS Panels Shift Clock Edge				STN-DD Panels Shift Clock Edge			
	1st	2nd	3rd	4th	1st	2nd	3rd	4th
P0	R1	G6	B11	...	Upper:			
P1	G1	B6	R12	...	P0	R1	B3	G6 ...
P2	B1	R7	G12	...	P1	G1	R4	B6 ...
P3	R2	G7	B12	...	P2	B1	G4	R7 ...
P4	G2	B7	R13	...	P3	R2	B4	G7 ...
P5	B2	R8	G13	...	P8	G2	R5	B7 ...
P6	R3	G8	B13	...	P9	B2	G5	R8 ...
P7	G3	B8	R14	...	P10	R3	B5	G8 ...
P8	B3	R9	G14	...	P11	G3	R6	B8 ...
P9	R4	G9	B14	...	Lower:			
P10	G4	B9	R15	...	P4	R1	B3	G6 ...
P11	B4	R10	G15	...	P5	G1	R4	B6 ...
P12	R5	G10	B15	...	P6	B1	G4	R7 ...
P13	G5	B10	R16	...	P7	R2	B4	G7 ...
P14	B5	R11	G16	...	P12	G2	R5	B7 ...
P15	R6	G11	B16	...	P13	B2	G5	R8 ...
					P14	R3	B5	G8 ...
					P15	G3	R6	B8 ...

For STN-SS panels the pixel sequence repeats with 16 pixels every 3 shift clock edges (5-1/3 pixels per shift clock edge). Clock divide must be set to 010.

For STN-DD panels the pixel sequence repeats with 16 pixels (8 for each of the upper and lower panels) every 3 shift clock edges (2-2/3 pixels per shift clock edge per panel). Clock divide must be set to 001 with Frame Acceleration and 010 without Frame Acceleration.

Output Signal Timing

LP Signal Timing

LP output polarity is controlled by XR54[6] (0=positive, 1=negative). Setting XR4F bit-7, however, causes the LP pin to output flat panel BLANK# / DE instead of the normal LP signal (and all other LP timing control parameters will be ignored). Some panels (e.g., Plasma and EL) require LP to be active during vertical blank time. XR51[7] may be set to enable this. Otherwise LP pulses are not generated during vertical blank.

FLM Output Signal Timing

FLM signal output polarity is controlled by XR54[7] (0=positive, 1=negative).

BLANK# / DE Output Signal Timing

The polarity of the BLANK# / DE output (if selected for output on M, LP, or FLM as indicated above) may be controlled by XR54[0] (0=positive, 1=negative). XR54[1] selects whether BLANK# / DE outputs both H and V (0) or just H (1). XR51[2] selects whether BLANK# / DE is generated from CRT Blank or Flat Panel Blank.

SHFCLK Output Signal Timing

XR51[5] (Shift Clock Mask or SM) may be set to force the shift clock output low outside the display enable interval.

Pixel Timing Diagrams

Pixel output timing sequences are shown for the following panel configurations:

1) **SS Monochrome Plasma / EL**

Single Panel-Single Drive (Panel Type = 00)
Plasma/EL Panel
2 pixels/shift clock, 4 bits/pixel (CD = 001)

2) **DD Monochrome LCD**

Dual Panel-Double Drive (Panel Type = 11)
Monochrome LCD Panel
8 pixels/shiftclk, 1bit/pixel, CD = 011
(010 with FB)
16 pixels/shiftclk, 1bit/pixel, CD = 100
(011 with FB)

3) **SS Color TFT LCD**

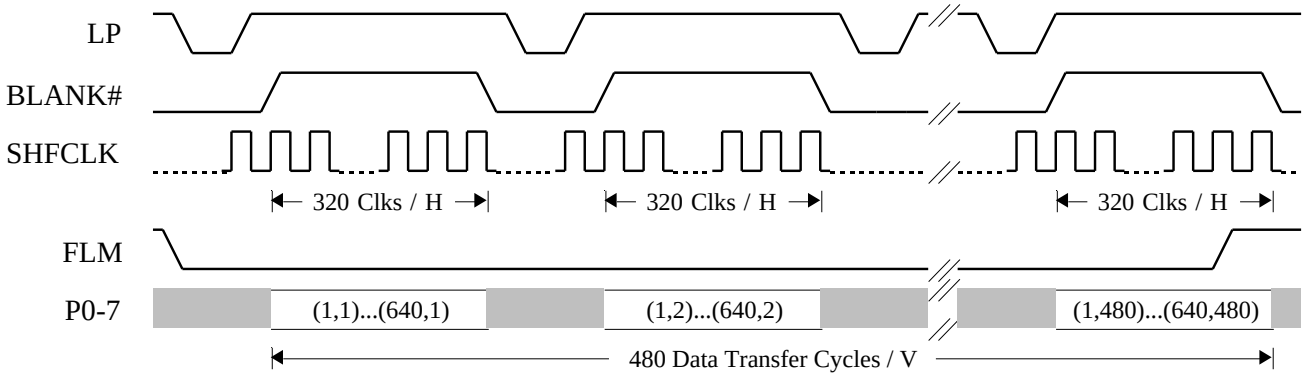
Single Panel-Single Drive (Panel Type = 00)
Color TFT LCD Panel
4/5/6 bits/color/pixel (12/16/18 bits total)
1 pixel/shift clock, 15-bit 5-5-5 RGB, CD=000
1 pixel/shift clock, 18-bit 6-6-6 RGB, CD=000

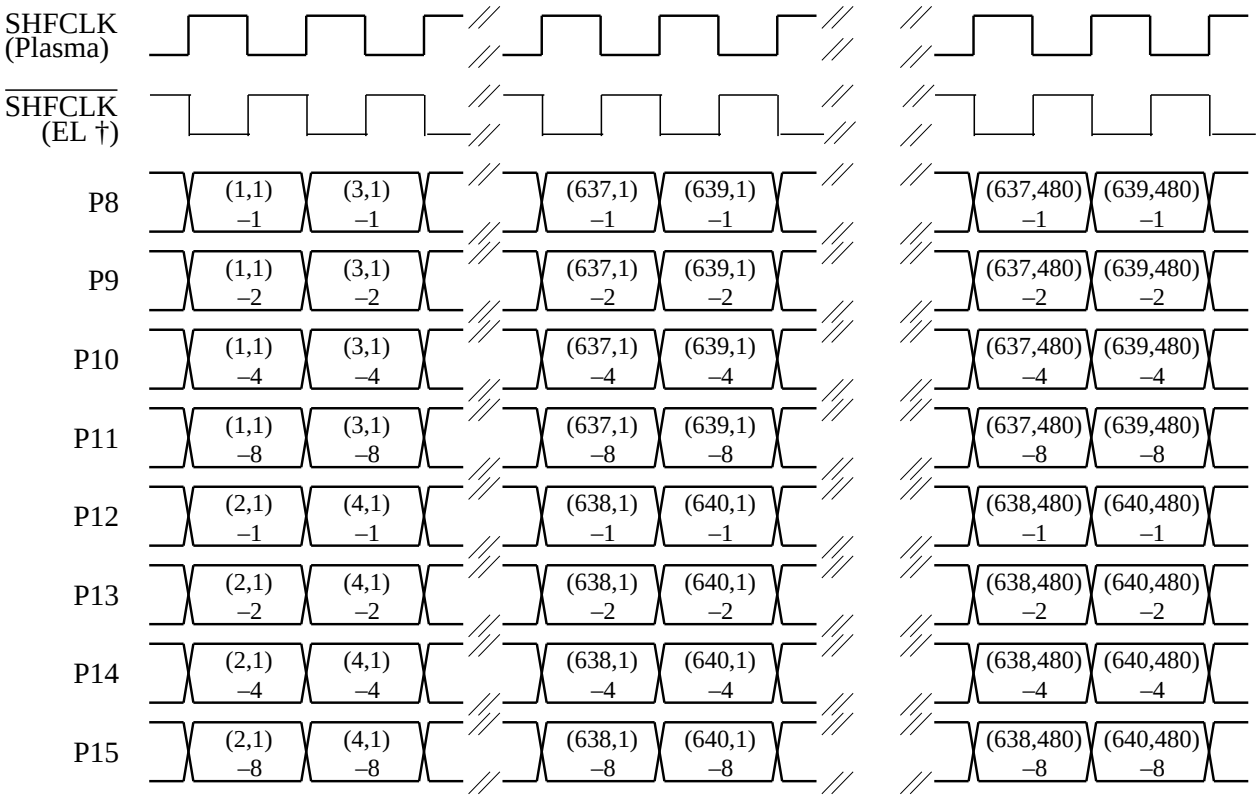
4) **SS Color STN LCD**

Single Panel-Single Drive (Panel Type = 00)
Color STN LCD Panel
1 bit/color/pixel (3 bits total) 1-1-1 RGB
1 pixel/shiftclk (3bit), CD=000
2 pixels/shiftclk (6bit), CD=001
2-2/3 pixels/shift clock (8bit), CD=010
5-1/3 pixels/shift clock (8bit), CD=010, SD=1
5-1/3 pixels/shift clock (16bit), CD=010

5) **DD Color STN LCD**

Dual Panel-Dual Drive (Panel Type = 11)
Color STN LCD Panel
All timings = 1 bit/color/pixel (3 bits total) RGB
2-2/3 pixels/shift clock (8-bit), CD=001
5-1/3 pixels/shift clock (16-bit), CD=010

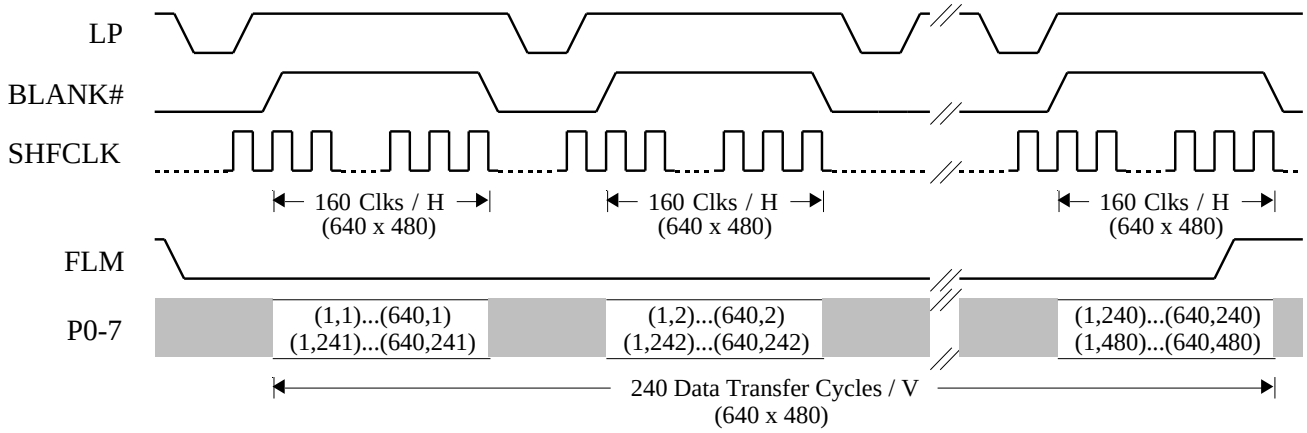




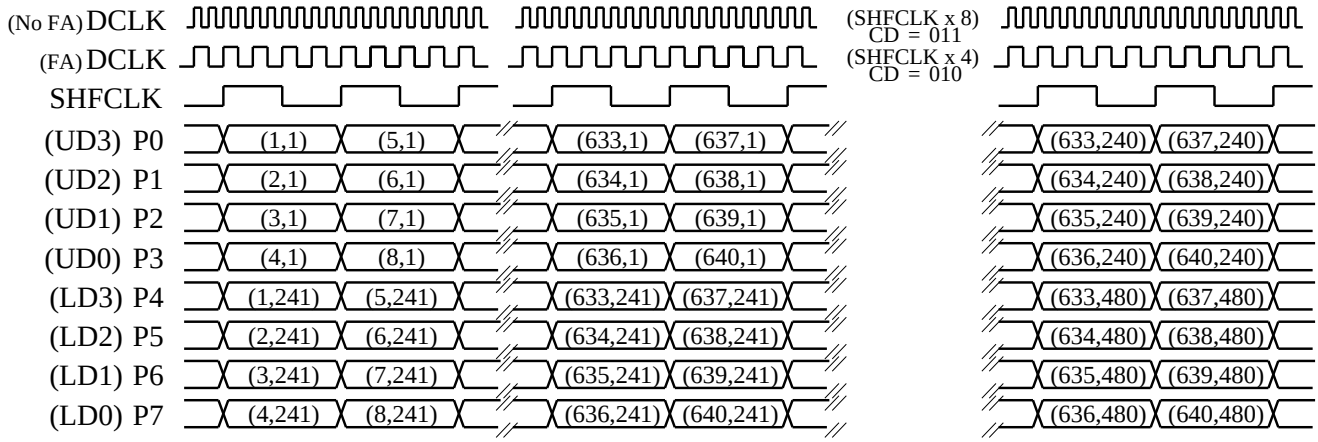
† EL panels use the rising edge of SHFCLK to clock in panel data, so the SHFCLK output from the 65535 must be inverted prior to driving the panel

Panel Timing - Monochrome 16-Gray-Level EL / Plasma 8-Bit Interface

Panel Output Timing - 640 x 480 Monochrome DD 8-Bit (1 Bit / Pixel, 8 Pixels / Shift Clock)



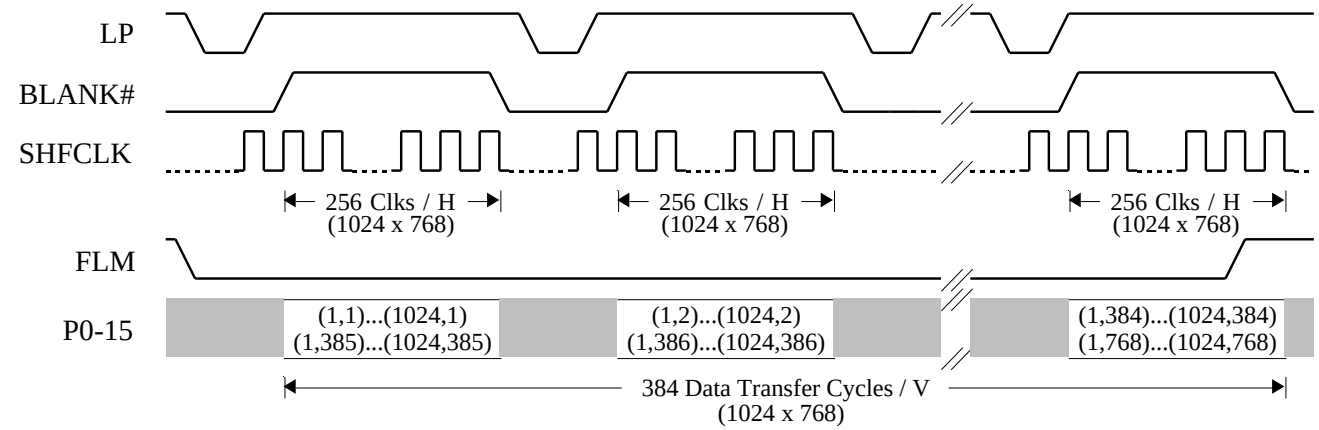
Panel Output Pixel Order - 640 x 480



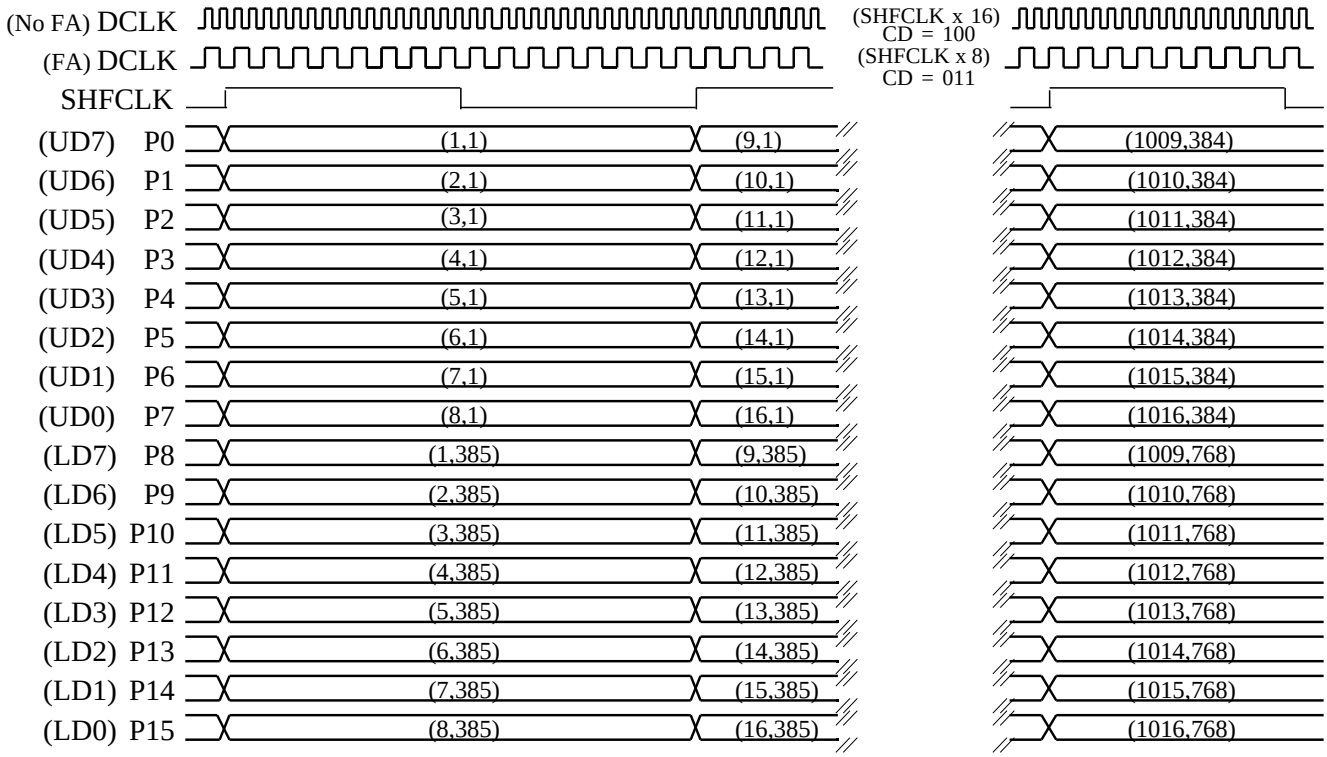
FA = Frame Accelerator (Imbedded or External)

Panel Timing - Monochrome LCD DD 8-Bit Interface

Panel Output Timing - 1024 x 768 Monochrome DD 16-Bit (1 Bit / Pixel, 16 Pixels / Shift Clock)

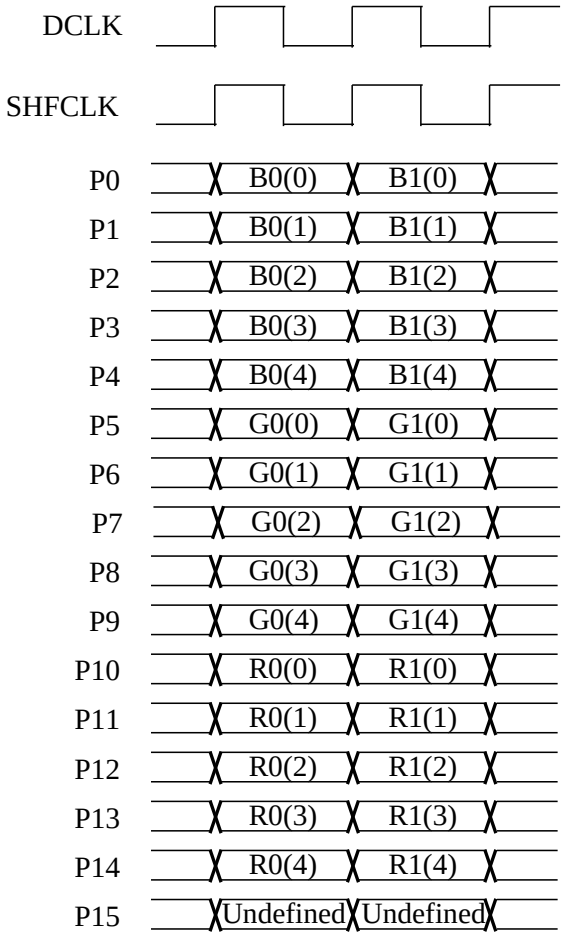


Pixel Output Pixel Order - 1024 x 768



FA = Frame Accelerator (Embedded or External)

Panel Timing - Monochrome LCD DD 16-Bit Interface

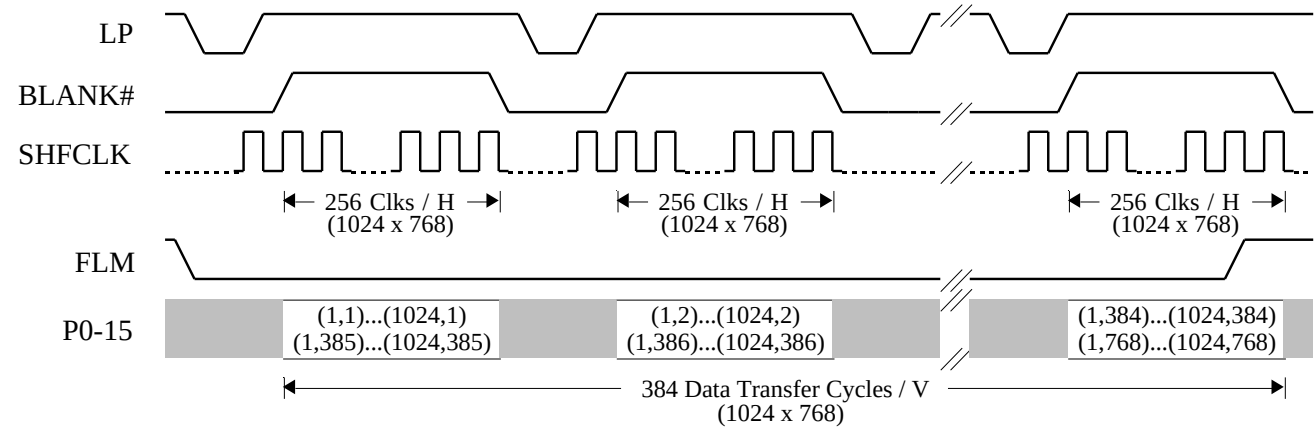


CD:	000 (1 Pixel / Clock)
FRC:	10 (2 Frame)
Bits / Pixel:	110 (6 bits/pixel)
Pixel Format:	5-5-5 RGB
DataWidth:	15-Bit †

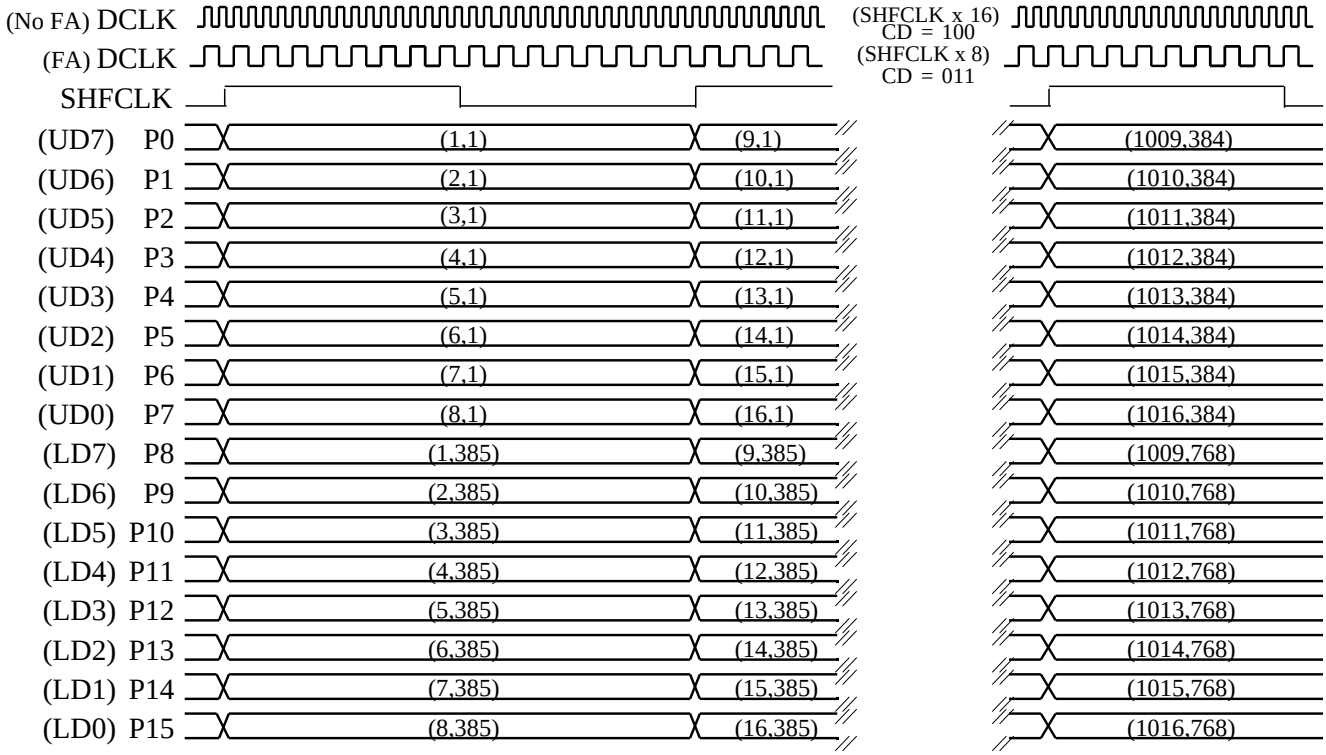
† Panels with 9 or 12-bit data interfaces would use this setting and only connect to the msbs of each color

Panel Timing - Color LCD TFT 9 / 12 / 15-Bit Interface

Panel Output Timing - 1024 x 768 Monochrome DD 16-Bit (1 Bit / Pixel, 16 Pixels / Shift Clock)

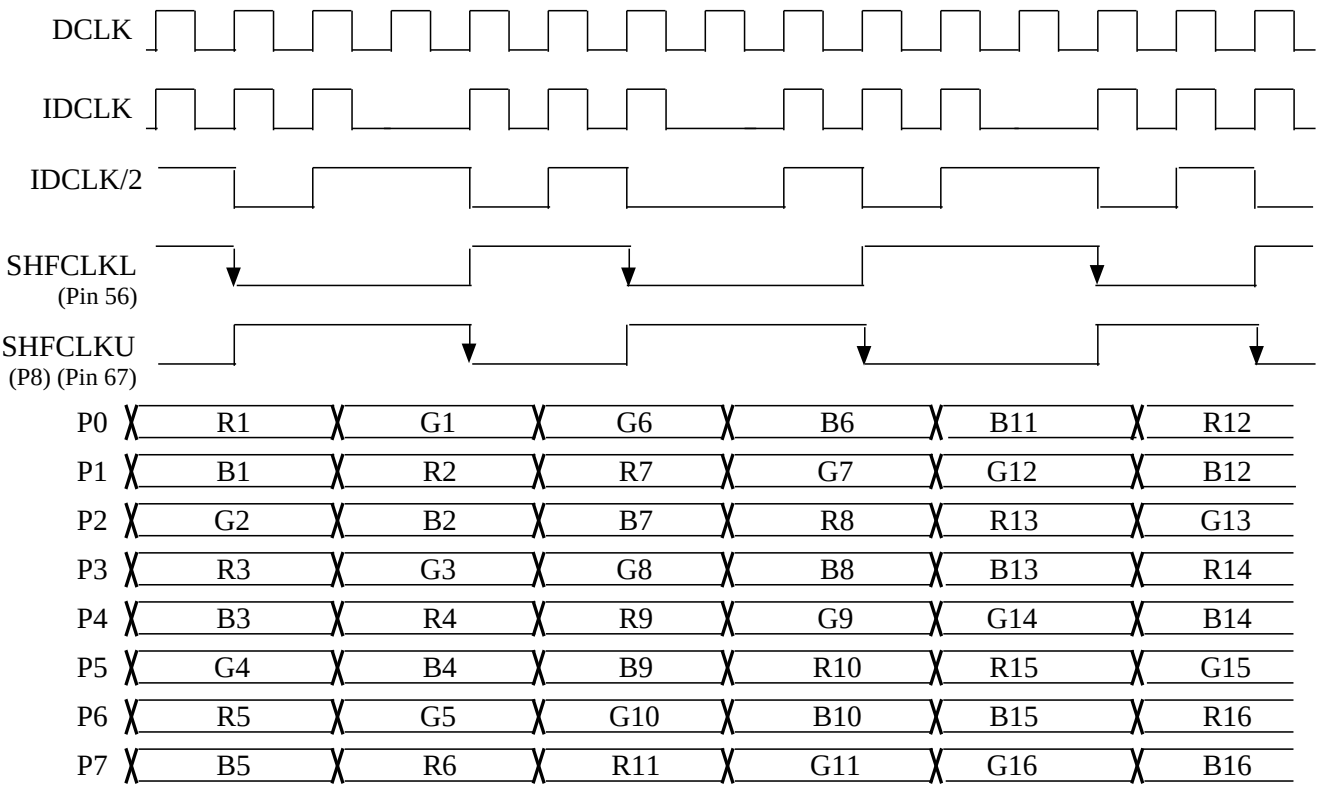


Pixel Output Pixel Order - 1024 x 768



FA = Frame Accelerator (Embedded or External)

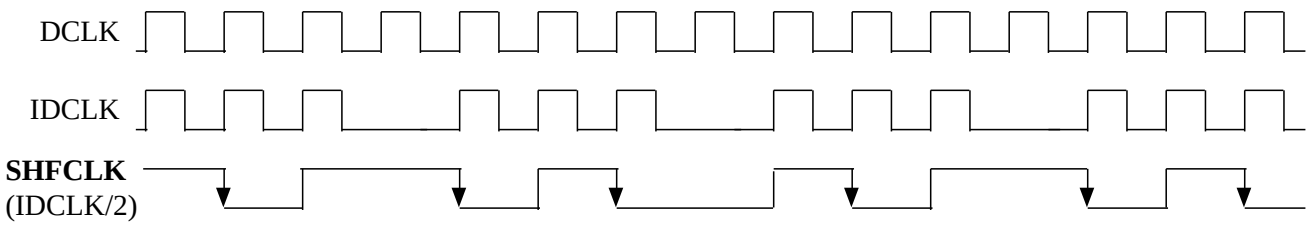
Panel Timing - Color LCD TFT 18-Bit Interface



PT:	00 (SS Panel)
CD:	010 (5-1/3 Pixels / Clock)
FRC:	01 (16-Frame)
Pixel Packing:	11 (Extended 4-Bit Pack)
Bits / Pixel:	100 (4 bits / pixel)
Frame Buffer / Acceleration:	Disabled / Disabled

16 Pixels are transferred every 16 dot clocks (6 shift clock edges)

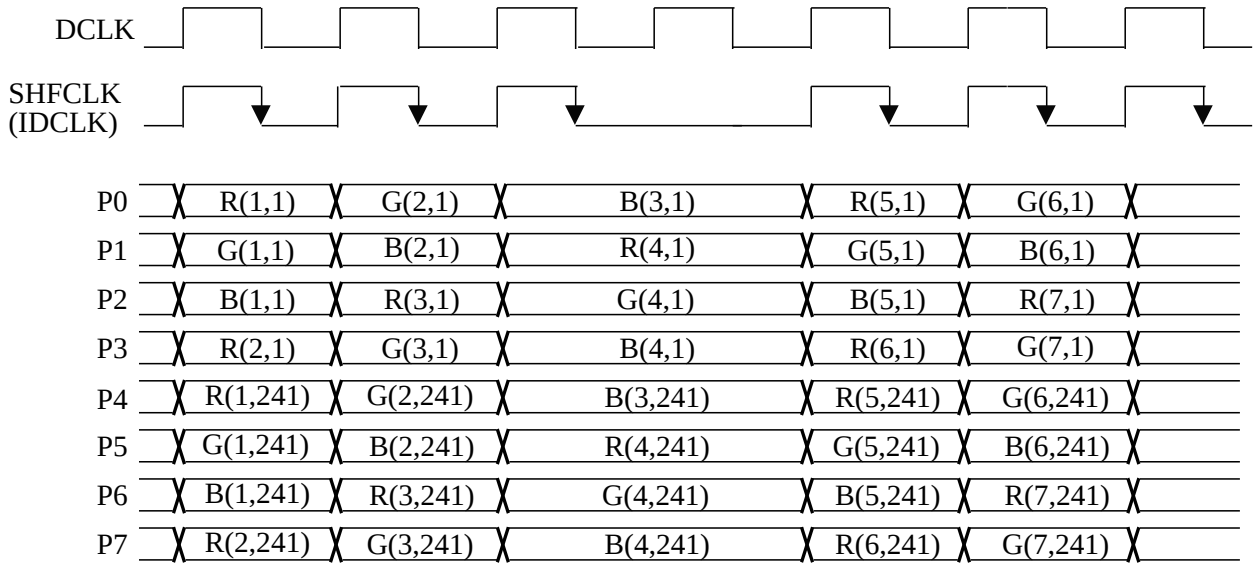
Panel Timing - Color LCD STN 8-Bit (Extended 4-Bit Pack) Interface



P0	R1	G6	B11	R17	G22	B27
P1	G1	B6	R12	G17	B22	R28
P2	B1	R7	G12	B17	R23	G28
P3	R2	G7	B12	R18	G23	B28
P4	G2	B7	R13	G18	B23	R29
P5	B2	R8	G13	B18	R24	G29
P6	R3	G8	B13	R19	G24	B29
P7	G3	B8	R14	G19	B24	R30
P8	B3	R9	G14	B19	R25	G30
P9	R4	G9	B14	R20	G25	B30
P10	G4	B9	R15	G20	B25	R31
P11	B4	R10	G15	B20	R26	G31
P12	R5	G10	B15	R21	G26	B31
P13	G5	B10	R16	G21	B26	R32
P14	B5	R11	G16	B21	R27	G32
P15	R6	G11	B16	R22	G27	B32

PT:	00 (SS Panel)
CD:	010 (5-1/3 Pixels / Clock)
FRC:	01 (16-Frame)
Pixel Packing:	01 (4-Bit Pack)
Bits / Pixel:	100 (4 bits / pixel)
Frame Buffer / Acceleration:	Disabled / Disabled

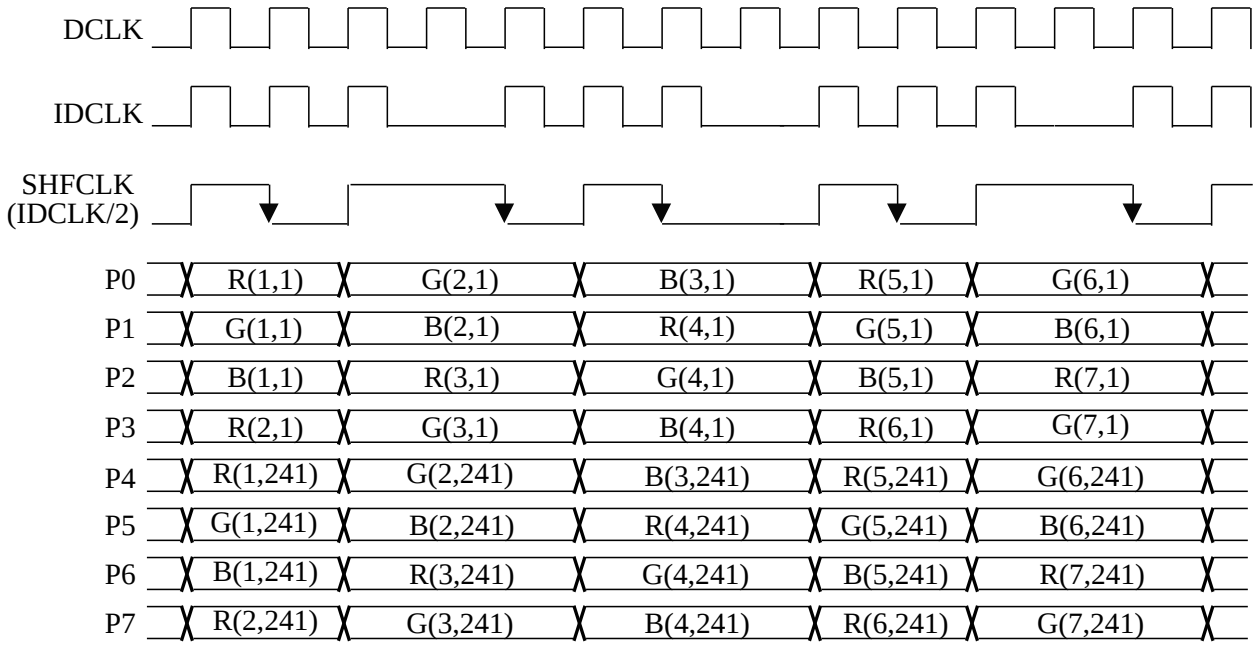
Panel Pixel Timing - Color LCD STN 16-Bit (4-Bit Pack) Interface



PT:	11 (DD Panel)
CD:	000 (2-2/3 Pixels / Clock)
FRC:	01 (16-Frame)
Bits / Pixel:	100 (4 bits/pixel)
Pixel Packing:	01 (4-Bit Pack)
Frame Buffer/Acceleration:	Enabled/Enabled

8 Pixels (4 each for the upper and lower panels) are transferred every 4 Dot Clocks (3 Shift Clock Edges)

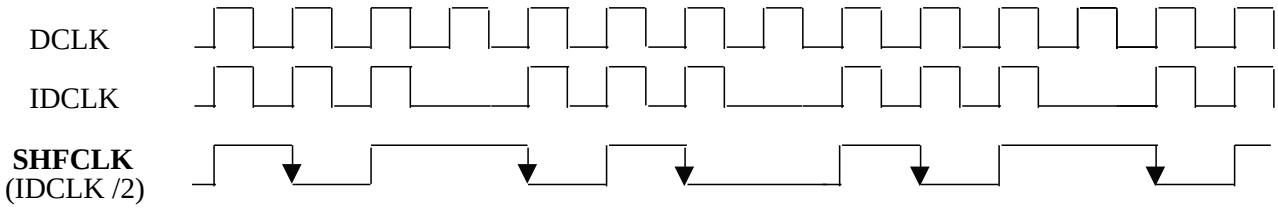
Panel Pixel Timing - Color LCD STN-DD 8-Bit (4-Bit Pack) Interface - With Frame Acceleration



PT:	11 (DD Panel)
CD:	010 (2-2/3 Pixels / Clock)
FRC:	01 (16-Frame)
Bits / Pixel:	100 (4 bits/pixel)
Pixel Packing:	01 (4-Bit Pack)
Frame Buffer/Acceleration:	Enabled/Disabled

8 Pixels (4 each for the upper and lower panels) are transferred every 8 Dot Clocks (3 Shift Clock Edges)

Panel Pixel Timing - Color LCD STN-DD 8-Bit (4-Bit Pack) Interface - Without Frame Acceleration

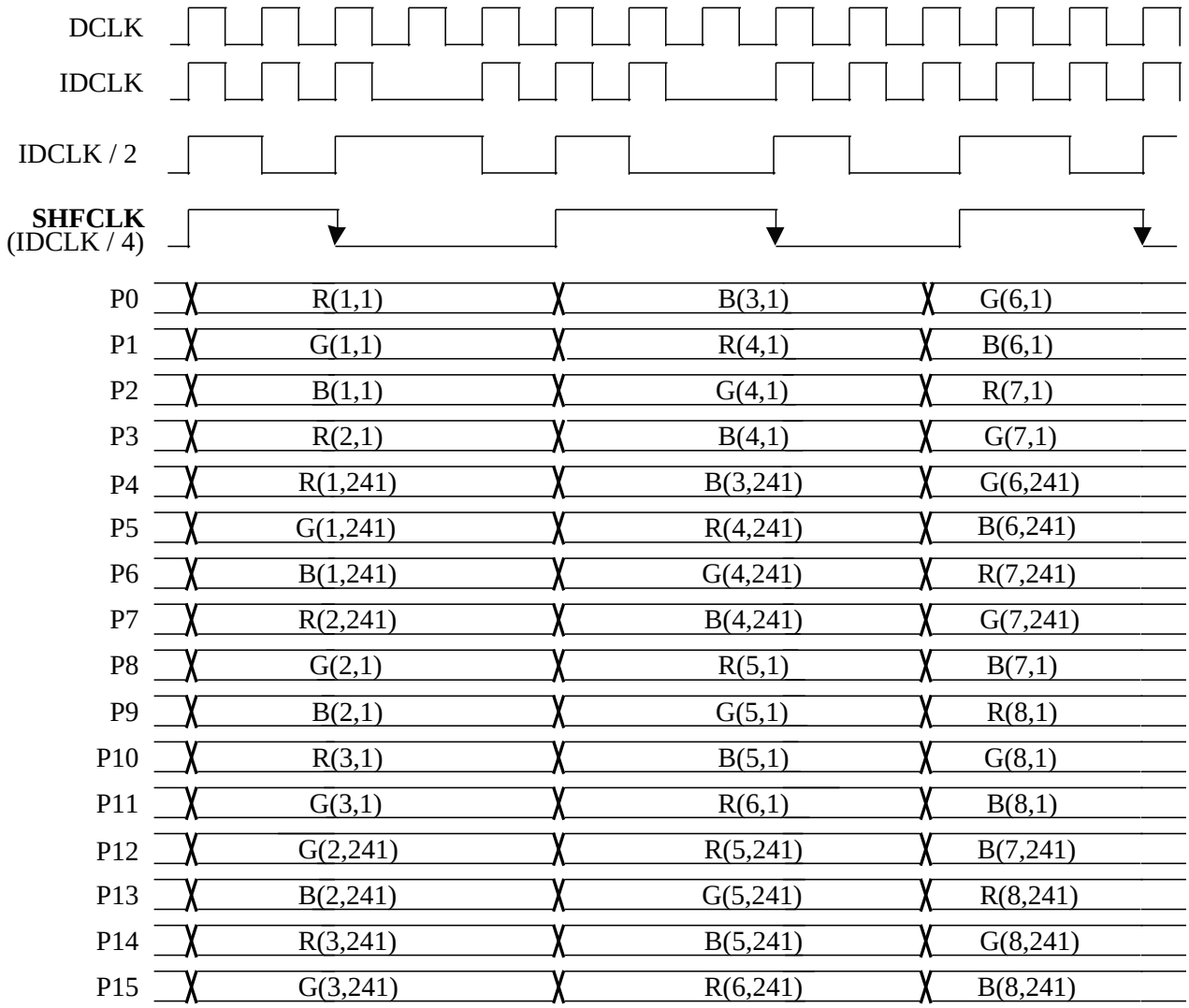


P0	R(1,1)	B(3,1)	G(6,1)	R(9,1)	B(11,1)
P1	G(1,1)	R(4,1)	B(6,1)	G(9,1)	R(12,1)
P2	B(1,1)	G(4,1)	R(7,1)	B(9,1)	G(12,1)
P3	R(2,1)	B(4,1)	G(7,1)	R(10,1)	B(12,1)
P4	R(1,241)	B(3,241)	G(6,241)	R(9,241)	B(11,241)
P5	G(1,241)	R(4,241)	B(6,241)	G(9,241)	R(12,241)
P6	B(1,241)	G(4,241)	R(7,241)	B(9,241)	G(12,241)
P7	R(2,241)	B(4,241)	G(7,241)	R(10,241)	B(12,241)
P8	G(2,1)	R(5,1)	B(7,1)	G(10,1)	R(13,1)
P9	B(2,1)	G(5,1)	R(8,1)	B(10,1)	G(13,1)
P10	R(3,1)	B(5,1)	G(8,1)	R(11,1)	B(13,1)
P11	G(3,1)	R(6,1)	B(8,1)	G(11,1)	R(14,1)
P12	G(2,241)	R(5,241)	B(7,241)	G(10,241)	R(13,241)
P13	B(2,241)	G(5,241)	R(8,241)	B(10,241)	G(13,241)
P14	R(3,241)	B(5,241)	G(8,241)	R(11,241)	B(13,241)
P15	G(3,241)	R(6,241)	B(8,241)	G(11,241)	R(14,241)

PT:	11 (DD Panel)
CD:	010 (5-1/3 Pixels / Clock)
FRC:	01 (16-Frame)
Pixel Packing:	01 (4-Bit Pack)
Bits / Pixel:	100 (4 bits / pixel)
Frame Buffer / Acceleration:	Enabled / Enabled

16 Pixels (8 each for the upper and lower panels) are transferred every 8 Dot Clocks (3 Shift Clock Edges)

Panel Pixel Timing - Color LCD STN-DD 16-Bit (4-Bit Pack) Interface - With Frame Acceleration



PT:	11 (DD Panel)
CD:	010 (5-1/3 Pixels / Clock)
FRC:	01 (16-Frame)
Pixel Packing:	01 (4-Bit Pack)
Bits / Pixel:	100 (4 bits / pixel)
Frame Buffer/Acceleration:	Enabled/Disabled

16 Pixels (8 each for the upper and lower panels) are transferred every 16 Dot Clocks (3 Shift Clock Edges)

Panel Pixel Timing - Color LCD STN-DD 16-Bit (4-Bit Pack) Interface - Without Frame Acceleration

Programming and Parameters

GENERAL PROGRAMMING HINTS

The values presented in this section make certain assumptions about the operating environment. The flat panel clock ('dot clock') is assumed to be generated by the internal clock synthesizer. The values programmed into the SmartMap™ control registers (XR61 and XR62) give a threshold of 3 with foreground and background shift of 3 but SmartMap™ is turned off. To enable it, set XR61 bit-0 = 1. The 65535 provide programmability of the gray scaling algorithm by adjusting 'm' and 'n' polynomial values in extended register 6E.

The horizontal parameter values presented here are the minimum required for each panel type. For high resolution panels, these parameters may be changed to suit the panel size. The horizontal values equal the number of characters clocks output per line. In dual drive panels this value includes both panels. Therefore, the horizontal values are double those expected.

Due to pipelining of the horizontal counters, certain sync or blank values may result in no display. Generally, the horizontal blank start must equal the display end and the blank end must equal the horizontal total. The horizontal sync start and end values have a wide range of acceptable values. The 65535 also has the versatility to program an LP delay to aid in interfacing to panels with a wide variety of timing requirements.

In order to program the 65535 for simultaneous display, two FLM signals are required. The first shorter FLM will match the normal FLM frequency as the data is displayed on the first half of the CRT display data. The second FLM will be longer to allow for the CRT blank time. The FLM delay is programmed in XR2C and should be equal to the CRT blank time + 1.

For flat panel types and sizes not presented here, start with the parameters for a panel that most closely resembles the target panel. Adjust the flat panel configuration registers as needed and adjust the horizontal and vertical parameters as needed. Adaption to a non-standard panel is usually a trial and error process.

These parameters are recommended by Chips and Technologies, Inc. for the 65535. They have been tested on several different flat panel displays. Customers should feel free to test other register values to improve the screen appearance or to customize the 65535 for other flat panel displays.

EXTENSION REGISTER VALUES

The 65535 controller can be programmed for a wide variety of flat panels, compensation techniques and backwards compatibility. The following pages provide the following 65535 Extension Register Value tables:

Table	Extension Registers	Display Type Description	Panels
#1	Minimum	Parameters for Initial Boot (Analog CRT VGA Mode)	
#2	Additional	Parameters for Emulation Modes	
#3	Additional	640x480 Monochrome LCD-DD (Panel Mode Only)	Epson EG-9005F-LS Citizen G6481L-FF Sharp LM64P80 Sanyo LCM-6494-24NTK Hitachi LMG5364XUFC
#4	Additional	640x480 Monochrome LCD-DD (Simultaneous Mode Display)	
#5	Additional	640x480 Color TFT LCD (Panel Mode Only)	HitachiTX26D02VC2AA Sharp LQ9D011 Toshiba LTM-09C015-1
#6	Additional	640x480 Color TFT LCD (Simultaneous Mode Display)	
#7	Additional	640x480 Color STN-SS LCD - 4-Bit Pack..... (Panel Only & Simultaneous Mode Display)	Sanyo LM-CK53-22NEZ Sanyo LCM5327-24NAK Sanyo LCM5330
#8	Additional	640x480 Color STN-SS LCD - Extended 4-Bit Pack.....	Sharp LM64C031
#9	Additional	640x480 Color STN-DD LCD - 8-Bit Interface..... (Panel Mode Only)	Kyocera KCL6448 DSTT Hitachi LMG9720XUFC
#10	Additional	640x480 Color STN-DD LCD - 16-Bit Interface ..... (Panel & Simultaneous Mode Display)	Sharp LM64C08P Sanyo LCM5331-22NTK Hitachi LMG9721XUFC Toshiba TLX-8062S-C3X Optrex DMF-50351NC-FW
#11	Additional	640x480 16 Internal Gray Scale Plasma	Matsushita S804
#12	Additional	640x480 16 Internal Gray Scale EL	Sharp LJ64ZU50

Table #1 specifies the minimum Extension Register values required for the 65535 to boot to VGA mode on an analog CRT monitor.

Table #2 specifies the additional Extension Register values required for emulation of EGA, CGA, MDA and Hercules backwards compatibility modes. The registers in Table #2 should be used in conjunction with the registers specified in Table #1. For registers listed in both tables, use the values in Table #2 (shown in bold text).

Tables #3-12 specify the additional Extension Register values required to support various panels. The registers in Tables #3-12 should be used in conjunction with the registers specified in Table #1 (and optionally Table #2). For registers listed in more than one table, use the values in Tables #3-12 (shown in bold text).

Table #1 - Parameters for Initial Boot

Initial Boot-Up Extension Register Values for VGA Display on an Analog CRT Monitor

Register	Value (Hex)	Register Name	Comments
XR02	01	CPU Interface Control 1	
XR04	A1	Memory Control 1	Note 1
XR05	00	Memory Control 2	
XR06	00	Palette Control	
XR0B	00	CPU Paging	
XR08	00	Linear Addressing Base	
XR0C	00	Start Address Top	
XR0D	00	Auxiliary Offset	
XR0E	80	Text Mode Control	
XR0F	10	Software Flags 0	Note 2
XR10	00	Single/Low Map	
XR11	00	High Map	
XR51	63	Display Type	
XR14	00	Emulation Mode	
XR15	00	Write Protect	
XR16	00	Vertical Overflow	
XR17	00	Horizontal Overflow	
XR1E	00	Alternate Offset	
XR1F	00	Virtual EGA Switch	
XR24	12	Alternate Max Scanline	
XR25	59	Horizontal Virtual Panel Size	
XR28	80	Video Interface	
XR29	4C	Half Line Compare	
XR2B	00	Software Flags 1	Note 2
XR33	20	Clock Control	
XR30	03	Clock Divide Control	
XR31	6B	Clock M-Divisor	
XR32	3C	Clock N-Divisor	
XR33	00	Clock Control	
XR30	03	Clock Divide Control	
XR31	4E	Clock M-Divisor	
XR32	59	Clock N-Divisor	
XR44	10	Software Flags 2	Note 2
XR45	00	Software Flags 3	Note 2
XR52	40	Power Down Control	
XR53	00	Panel Format 3	
XR54	32	Panel Interface	
XR5F	06	Power Down Mode Refresh	
XR60	88	Blink Rate Control	
XR61	2E	SmartMap™ Control	
XR62	07	SmartMap™ Shift Parameter	
XR63	41	SmartMap™ Color Mapping Control	
XR70	80	Setup / Disable Control	
XR72	24	External Device I/O	

Note: 1) Memory Control Register 1 is automatically re-programmed with the proper display memory configuration by the BIOS
2) The Software Flag Registers are used by the BIOS and should not be re-programmed

Table #2 - Parameters for Emulation Modes

Extension Register Values for CRT-Only, Panel-Only, & Simultaneous CRT / Panel Display

Register	Value (Hex)	Register Name	Comments
XR14	**00**	**Emulation Mode**	**EGA Emulation**
XR15	**18**	**Write Protect**	**EGA Emulation**

Register	Value (Hex)	Register Name	Comments
XR14	**01**	**Emulation Mode**	**CGA Emulation**
XR15	**0D**	**Write Protect**	**CGA Emulation**
XR18	27	Alternate Horizontal Display Enable End	CGA Emulation
XR19	2B	Alternate Horizontal Retrace Start	CGA Emulation
XR1A	A0	Alternate Horizontal Retrace End	CGA Emulation
XR1B	2D	Alternate Horizontal Total	CGA Emulation
XR1C	28	Alternate Horizontal Blanking Start	CGA Emulation
XR1D	10	Alternate Horizontal Blanking End	CGA Emulation
XR1E	**14**	**Alternate Offset**	**CGA Emulation**
XR7E	**30**	**CGA / Hercules Color Select**	**CGA Emulation**

Register	Value (Hex)	Register Name	Comments
XR14	**52**	**Emulation Mode**	**MDA Emulation**
XR15	**0D**	**Write Protect**	**MDA Emulation**
XR7E	**0F**	**CGA / Hercules Color Select**	**MDA Emulation**

Register	Value (Hex)	Register Name	Comments
XR0D	**02**	**Auxiliary Offset**	**Hercules Emulation**
XR14	**52**	**Emulation Mode**	**Hercules Emulation**
XR15	**0D**	**Write Protect**	**Hercules Emulation**
XR18	59	Alternate Horizontal Display Enable End	Hercules Emulation
XR19	60	Alternate Horizontal Retrace Start	Hercules Emulation
XR1A	8F	Alternate Horizontal Retrace End	Hercules Emulation
XR1B	6E	Alternate Horizontal Total	Hercules Emulation
XR1C	5C	Alternate Horizontal Blanking Start	Hercules Emulation
XR1D	31	Alternate Horizontal Blanking End	Hercules Emulation
XR1E	**16**	**Alternate Offset**	**Hercules Emulation**
XR7E	**0F**	**CGA / Hercules Color Select**	**Hercules Emulation**

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #3 - Parameters for 640x480 Monochrome LCD-DD Panels (Panel Mode Only)

Extension Register Values for Epson EG9005F-LS
Citizen G6481L-FF
Sharp LM64P80
Sanyo LCM-6494-24NTK
Hitachi LMG5364XUFC

Register	Value (Hex)	Register Name	Comments
XR06	**02**	**Palette Control**	**Disable Internal DAC**
XR19	57	Alternate Horizontal Sync Start	
XR1A	19	Alternate Horizontal Sync End	
XR1B	59	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	04	FLM Delay	
XR2D	50	LP Delay (CP disabled)	
XR2E	50	LP Delay (CP enabled)	
XR2F	00	LP Width	
XR4F	44	Panel Format 2	
XR50	25	Panel Format 1	
XR51	**67**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Panel Format 3**	
XR54	3A	Panel Interface	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	E4	Alternate Vertical Total	
XR65	07	Alternate Overflow	
XR66	E0	Alternate Vertical Sync Start	
XR67	01	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	26	Polynomial FRC Control Register	Optimize for best display quality
XR6F	1B	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #4 - Parameters for 640x480 Monochrome LCD-DD Panels (Simultaneous Mode Display)

Extension Register Values for Epson EG9005F-LS
Citizen G6481L-FF
Sharp LM64P80
Sanyo LCM-6494-24NTK
Hitachi LMG5364XUFC

Register	Value (Hex)	Register Name	Comments
XR19	55	Alternate Horizontal Sync Start	
XR1A	00	Alternate Horizontal Sync End	
XR1B	5F	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	21	FLM Delay	
XR2D	50	LP Delay (CP disabled)	
XR2E	50	LP Delay (CP enabled)	
XR2F	00	LP Width	
XR4F	44	Panel Format 2	
XR50	25	Panel Format 1	
XR51	**67**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Panel Format 3**	
XR54	3A	Panel Interface	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	0B	Alternate Vertical Total	
XR65	26	Alternate Overflow	
XR66	EA	Alternate Vertical Sync Start	
XR67	0C	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	26	Polynomial FRC Control Register	Optimize For LCD
XR6F	1B	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #5 - Parameters for 640x480 Color TFT Panels (Panel Mode Only)

Extension Register Values for HitachiTX26D02VC2AA
Sharp LQ9D011 (set to accommodate the DE signal)
ToshibaLTM-09C015-1

Register	Value (Hex)	Register Name	Comments
XR06	**C2**	**Palette Control**	**Color Reduction**
XR19	56	Alternate Horizontal Sync Start	
XR1A	13	Alternate Horizontal Sync End	
XR1B	5F	AlternateHorizontalTotal	
XR1C	4F	Horizontal Panel Size	
XR2C	04	FLMDelay	
XR2D	4F	LP Delay (CP disabled)	
XR2E	4F	LP Delay (CP enabled)	
XR2F	0F	LP Width	
XR4F	44	Panel Format 1	
XR50	02	Panel Format 2	
XR51	**C4**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Panel Format 3**	
XR54	**FA**	**Panel Interface**	**Set to F9 for Toshiba color panels**
XR55	E5	HorizontalCompensation	
XR56	00	HorizontalCentering	
XR57	1B	VerticalCompensation	
XR58	00	VerticalCentering	
XR59	84	VerticalLineInsertion	
XR5A	00	VerticalLineReplication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	01	AlternateVerticalTotal	
XR65	26	AlternateOverflow	
XR66	DF	Alternate Vertical Sync Start	
XR67	0C	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	ProgrammableOutputDrive	
XR6E	BD	Polynomial FRC Control	Optimize for best display quality
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #6 - Parameters for 640x480 Color TFT Panels (Simultaneous Mode Display)

Extension Register Values for HitachiTX26D02VC2AA
Sharp LQ9D011 (set to accommodate the DE signal)
ToshibaLTM-09C015-1

Register	Value (Hex)	Register Name	Comments
XR06	**C0**	**Palette Control**	**Color Reduction**
XR19	55	Alternate Horizontal Sync Start	
XR1A	00	Alternate Horizontal Sync End	
XR1B	5F	AlternateHorizontalTotal	
XR1C	4F	Horizontal Panel Size	
XR2C	00	FLMDelay	
XR2D	4F	LP Delay (CP disabled)	
XR2E	4F	LP Delay (CP enabled)	
XR2F	0F	LP Width	
XR4F	44	Panel Format 2	
XR50	02	Panel Format 1	
XR51	**C4**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Panel Format 3**	
XR54	**FA**	**Panel Interface**	**Set to F9 for Toshiba color panels**
XR55	E5	HorizontalCompensation	
XR56	00	HorizontalCentering	
XR57	1B	VerticalCompensation	
XR58	00	VerticalCentering	
XR59	84	Vertical Line Insertion	
XR5A	00	VerticalLineReplication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	0C	AlternateVerticalTotal	
XR65	26	AlternateOverflow	
XR66	EA	Alternate Vertical Sync Start	
XR67	0C	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	ProgrammableOutputDrive	
XR6E	BD	Polynomial FRC Control	Optimize for best display quality
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #7 - Parameters for 640x480 Color STN-SS Panels with 16-Bit Interface (4-Bit Pack) (Panel-Only and Simultaneous Display)

Extension Register Values for Sanyo LM-CK53-22NEZ
Sanyo LCM5327-24NAK
Sanyo LCM5330

Register	Value (Hex)	Register Name	Comments
XR06	**C2**	**Palette Control**	**C0 in simultaneous mode**
XR19	56	Alternate Horizontal Sync Start	55 in simultaneous mode
XR1A	19	Alternate Horizontal Sync End	00 in simultaneous mode
XR1B	59	Alternate Horizontal Total	5F in simultaneous mode
XR1C	4F	Horizontal Panel Size	
XR2C	04	FLM Delay	22 in simultaneous mode
XR2D	59	LP Delay (CP disabled)	62 in simultaneous mode
XR2E	59	LP Delay (CP enabled)	62 in simultaneous mode
XR2F	03	LP Width	00 in simultaneous mode
XR4F	44	Panel Format 1	
XR50	25	Panel Format 2	
XR51	C4	Display Type	
XR52	**41**	**Power Down Control**	**44 in simultaneous mode**
XR53	**1C**	**Panel Format 3**	
XR54	32	Panel Interface	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	23 in simultaneous mode
XR58	00	Vertical Centering	
XR59	8F	Vertical Line Insertion	8F in simultaneous mode
XR5A	00	Vertical Line Replication	04 in simultaneous mode
XR5B	81	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	22	M (ACDCLK) Control	22 in simultaneous mode
XR64	E4	Alternate Vertical Total	0B in simultaneous mode
XR65	07	Alternate Overflow	26 in simultaneous mode
XR66	E1	Alternate Vertical Sync Start	EA in simultaneous mode
XR67	02	Alternate Vertical Sync End	0C in simultaneous mode
XR68	DF	Vertical Panel Size	DF in simultaneous mode
XR6C	02	Programmable Output Drive	
XR6E	61	Polynomial FRC Control	Optimize for best display quality
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #8 - Parameters for 640x480 Color STN-SS Panels with 8-Bit Interface (Extended 4 Bit Pack) (Panel-Only and Simultaneous Display)

Extension Register Values for Sharp LM64C031

Register	Value (Hex)	Register Name	Comments
XR06	**C2**	**Palette Control**	**C0 simultaneous mode**
XR19	54	Alternate Horizontal Sync Start	55 simultaneous mode
XR1A	00	Alternate Horizontal Sync End	
XR1B	5F	Alternate Horizontal Total	5F simultaneous mode
XR1C	4F	Horizontal Panel Size	
XR2C	0C	FLM Delay	
XR2D	4F	LP Delay (CP disabled)	
XR2E	4F	LP Delay (CP enabled)	
XR2F	00	LP Width	
XR4F	44	Panel Format 2	
XR50	15	Panel Format 1	
XR51	**6C**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**3C**	**Panel Format 3**	
XR54	**3A**	**Panel Interface**	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	ED	Alternate Vertical Total	15 simultaneous mode
XR65	07	Alternate Overflow	26 simultaneous mode
XR66	E1	Alternate Vertical Sync Start	EA simultaneous mode
XR67	02	Alternate Vertical Sync End	0C simultaneous mode
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	BD	Polynomial FRC Control	Optimize for best display quality
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #9 - Parameters for 640x480 Color STN-DD LCD Panels with 8-Bit Interface without Frame Acceleration (Panel Mode Only)

Extension Register Values for Kyocera KCL6448 DSTT
Hitachi LMG9720XUFC

Register	Value (Hex)	Register Name	Comments
XR06	**C2**	**Palette Control**	
XR19	56	Alternate Horizontal Sync Start	
XR1A	13	Alternate Horizontal Sync End	
XR1B	5F	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	03	FLM Delay	
XR2D	B9	LP Delay (CP disabled)	
XR2E	B9	LP Delay (CP enabled)	
XR2F	00	LP Width	
XR4F	44	Panel Format 2	
XR50	15	Panel Format 1	
XR51	**67**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**1C**	**Panel Format 3**	
XR54	**32**	**Panel Interface**	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	1F	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	F4	Alternate Vertical Total	
XR65	07	Alternate Overflow	
XR66	F3	Alternate Vertical Sync Start	
XR67	01	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	33	Polynomial FRC Control	Optimize for best display quality
XR6F	1B	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #10 - Parameters for 640x480 Color STN-DD Panels with 16-Bit Interface with Frame Acceleration (Panel-Only and Simultaneous Mode Display)

Extension Register Values for Sharp LM64C08P
Sanyo LCM5331-22NTK
Hitachi LMG9721XUFC
Toshiba TLX-8062S-C3X
Optrex DMF-50351NC-FW

Register	Value (Hex)	Register Name	Comments
XR06	**C2**	**Palette Control**	
XR19	57	Alternate Horizontal Sync Start	
XR1A	19	Alternate Horizontal Sync End	
XR1B	59	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	15	FLM Delay	22 for no frame acceleration
XR2D	50	LP Delay (CP disabled)	9E for no frame acceleration
XR2E	50	LP Delay (CP enabled)	
XR2F	00	LP Width	
XR4F	04	Panel Format 1	
XR50	25	Panel Format 2	35 for no frame acceleration
XR51	**67**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**1C**	**Panel Format 3**	
XR54	**3A**	**Panel Interface**	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	1F	Vertical Line Replication	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR64	0B	Alternate Vertical Total	
XR65	07	Alternate Overflow	
XR66	EA	Alternate Vertical Sync Start	
XR67	0C	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	33	Polynomial FRC Control	Optimize for best display quality.
XR6F	1B	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #11 - Parameters for 640x480 Plasma Panels with 16 Internal Gray Levels

Extension Register Values for Matsushita S804

Register	Value (Hex)	Register Name	Comments
XR19	60	Alternate Horizontal Sync Start	
XR1A	00	Alternate Horizontal Sync End	
XR1B	60	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	04	FLM Delay	
XR2D	62	LP Delay (CP disabled)	
XR2E	6D	LP Delay (CP enabled)	
XR2F	08	LP Width	
XR4F	04	Panel Format 1	
XR50	17	Panel Format 2	
XR51	**C4**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Panel Format 3**	
XR54	**39**	**Panel Interface**	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	0D	Alternate Vertical Total	
XR65	26	Alternate Overflow	
XR66	E8	Alternate Vertical Sync Start	
XR67	0A	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	0D	Polynomial FRC Control	Optimize for best display quality
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #12 - Parameters for 640x480 EL Panels with 16 Internal Gray Levels

Extension Register Values for Sharp LJ64ZU50

Register	Value (Hex)	Register Name	Comments
XR19	52	Alternate Horizontal Sync Start	
XR1A	15	Alternate Horizontal Sync End	
XR1B	54	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	0C	FLM Delay	
XR2D	4F	LP Delay (CP disabled)	
XR2E	4E	LP Delay (CP enabled)	
XR2F	81	LP Width	
XR4F	04	Panel Format 1	
XR50	17	Panel Format 2	
XR51	**44**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Panel Format 3**	
XR54	**F9**	**Panel Interface**	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	F0	Alternate Vertical Total	
XR65	07	Alternate Overflow	
XR66	E5	Alternate Vertical Sync Start	
XR67	05	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Ouput Drive	
XR6E	9D	Polynomial FRC Control	Optimize for best display quality
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Application Schematic Examples

This section includes schematic examples showing various 65535 interfaces. The schematics are divided into into three main groups for discussion:

1) **System Bus Interface**
   - ISA (PC/AT) Bus (16-bit)
   - 486SLC / 386SX Local Bus (16-bit)
   - 486 16-Bit Local Bus (VL Bus compatible) (16-bit expanded to 32-bit)
   - 486 32-Bit Local Bus (VL Bus compatible) (32-bit)

2) **Display Memory Interface**
   - One or Two or 256Kx16 DRAMs (2-CAS)
   - One or Two or 256Kx16 DRAMs (2-WE)
   - Four or Eight or 256Kx4 DRAMs

3) **CRT/Panel/Video Interface**
   - CRT / Panel Interface
   - PC-VideoInterface

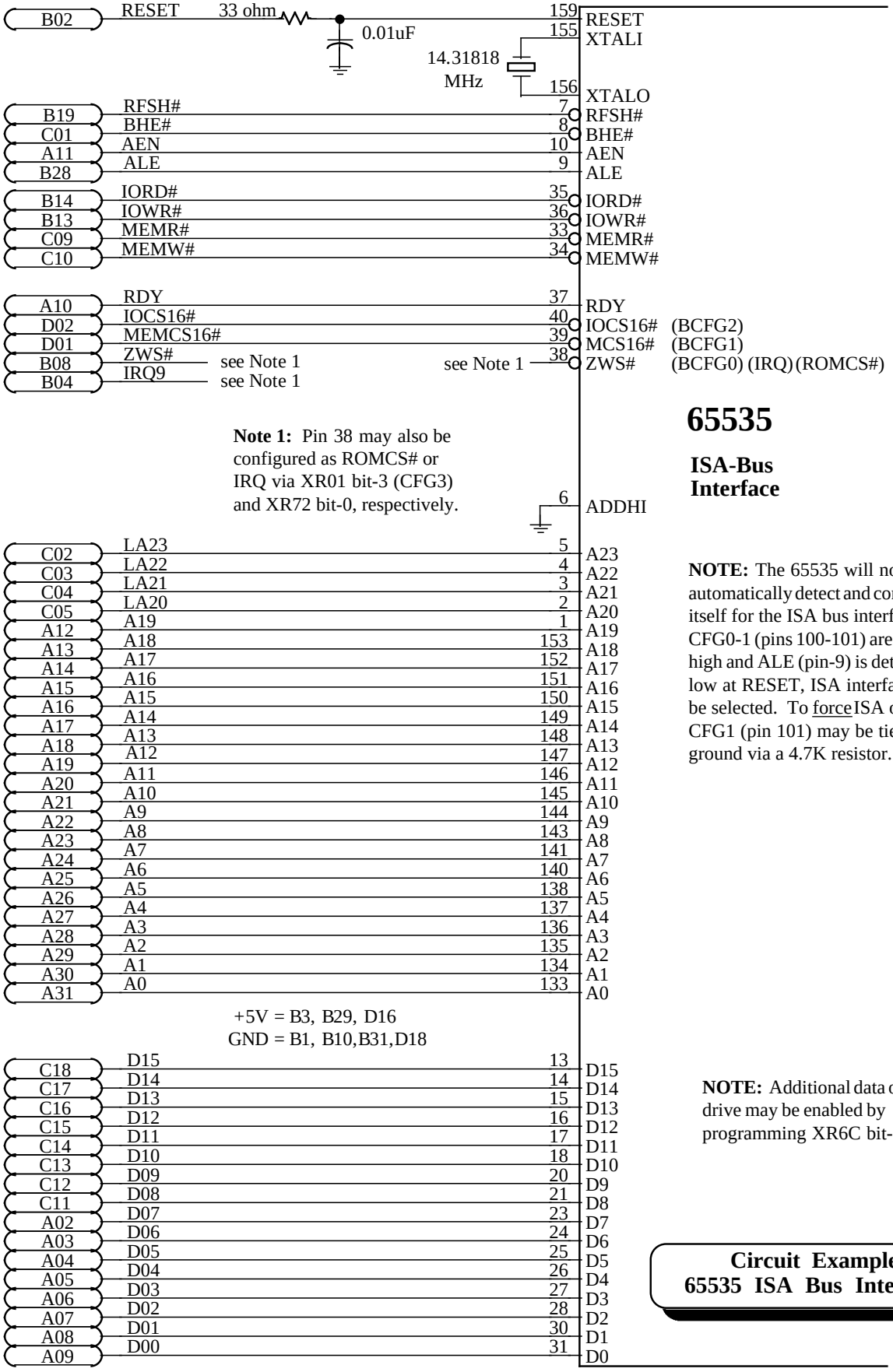
To design a system around the 65535, one schematic page would be selected from each of the groups above.

Selection of a bus interface for the VGA controller is generally dictated by the type of bus and CPU available in the system. If performance is a concern, however, and a 386 or 486 CPU is being used, a local bus interface should be considered and/or linear addressing support should be implemented. Linear addressing improves performance in GUI environments such as Windows™ by allowing the software used to access display memory (typically the Windows Driver) to be more efficient. If a 32-bit display memory interface is desired, the system bus interface can be only 16-bits (the same pins are used for the upper memory data bus or the upper system data bus). In this case, 486 local bus interfacing requires 4 external octal transceivers since, unlike the 386, the 486 CPU lacks the ability to do bus translation for 16-bit cycles. The 65535 provides all transceiver control signals, so no other external logic is required. 386 16-bit local bus interfacing does not require the external transceivers. Interfacing to ISA bus is always 16 bits, requires no external logic, and allows the use of either 16-bit or 32-bit display memory interfacing. Clock connections are shown as part of the bus interface diagrams. A 14.31818 MHz reference crystal is shown, although if a clean source of 14.31818 MHz is available in the system, it may be input on XTALI and the crystal would then not be required.

Generally, 256Kx16 DRAMs would be used for display memory, although, if desired, the memory interface may be designed to use 256Kx4's instead. Interface schematics are included for both DRAM sizes. 256Kx16 DRAMs come in two types: one write enable (WE#) with two CAS# inputs (one for the high byte and one for the low byte) or one CAS# input with two write enables (one for the high byte and one for the low byte). Either variety of DRAM may be used with the 65535 (default is to the 2-CAS variety with a programming option in the 65535 to change the memory control outputs for compatibility with either type). CHIPS' BIOS is able to detect which type is connected and program the 65535 accordingly. The diagrams included in this section show interfaces to both types; it is also possible to lay out a PCB to allow either type to be used (not shown).

An interface diagram is included showing connections to a standard CRT display. Panel interfaces, however, are not as standardized (generally every panel interface is different). To show how to interface to a wide variety of commonly available panels, the interface diagram in this section shows the connections used on CHIPS' Development Kit PC Board from the 65535 chip to connectors defined by CHIPS on that board. In the following section of this document, a number of examples are given showing connections from those DK board connectors to a number of typical panels. These connectors are used to simplify evaluation of the 65535 with various panels; a real system would not typically use the connectors shown, but would interface directly to the connector(s) used by the panel manufacturer. A second interface diagram is also included showing how to interface the 65535 to CHIPS' PC-Video products to provide live video overlay capability. Again, CHIPS' Development Kit PCB connector pinouts are used as an example, since there is a wide variety of possible configurations.

If internal logic is to be operated at 3.3V, CFG8 must be connected to ground via a 4.7K resistor.



Note 1: Pin 38 may also be configured as ROMCS# or IRQ via XR01 bit-3 (CFG3) and XR72 bit-0, respectively.

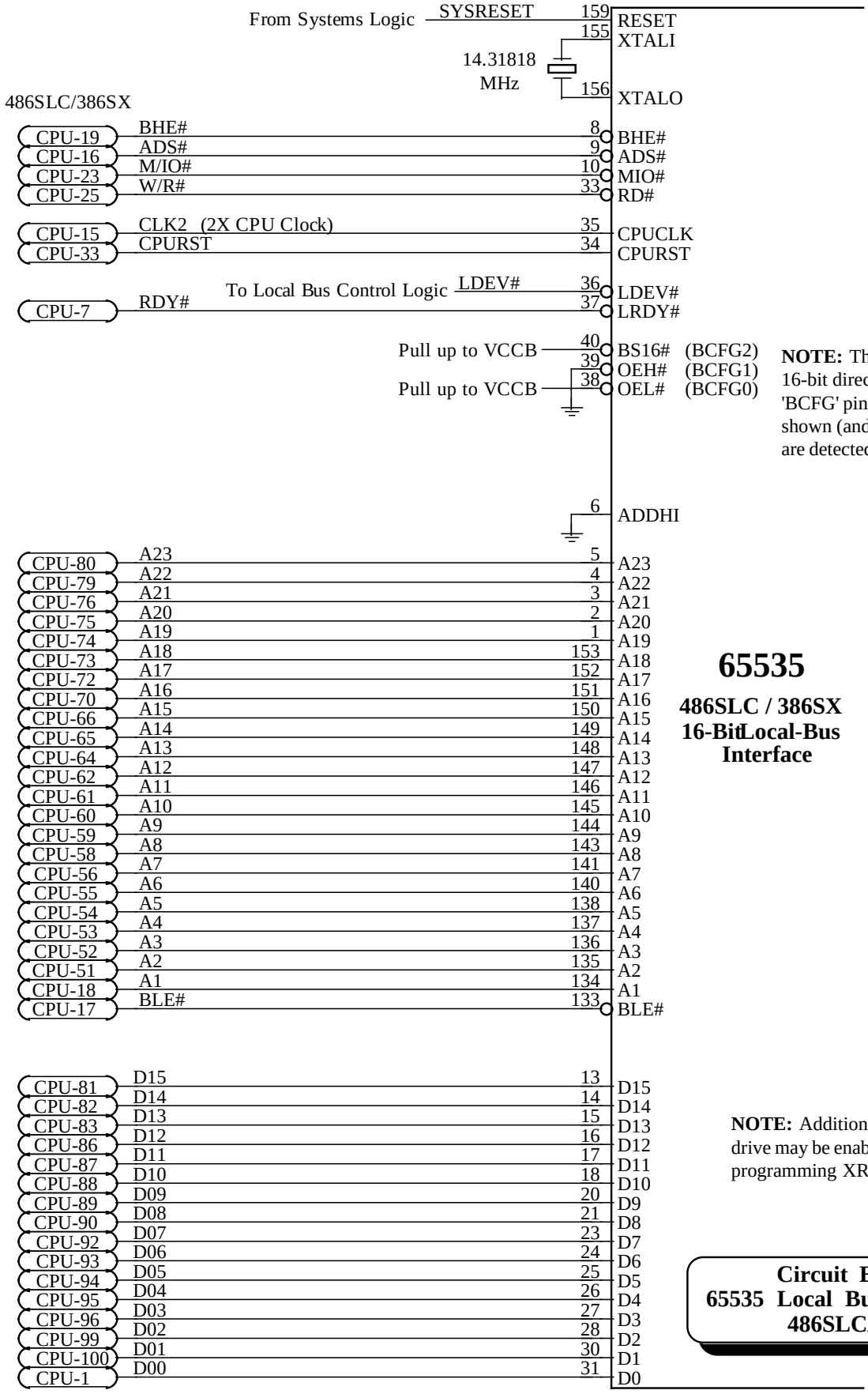
65535

ISA-Bus Interface

NOTE: The 65535 will normally automatically detect and configure itself for the ISA bus interface: if CFG0-1 (pins 100-101) are detected high and ALE (pin-9) is detected low at RESET, ISA interface will be selected. To force ISA operation, CFG1 (pin 101) may be tied to ground via a 4.7K resistor.

NOTE: Additional data output drive may be enabled by programming XR6C bit-3 = 0.

Circuit Example
65535 ISA Bus Interface



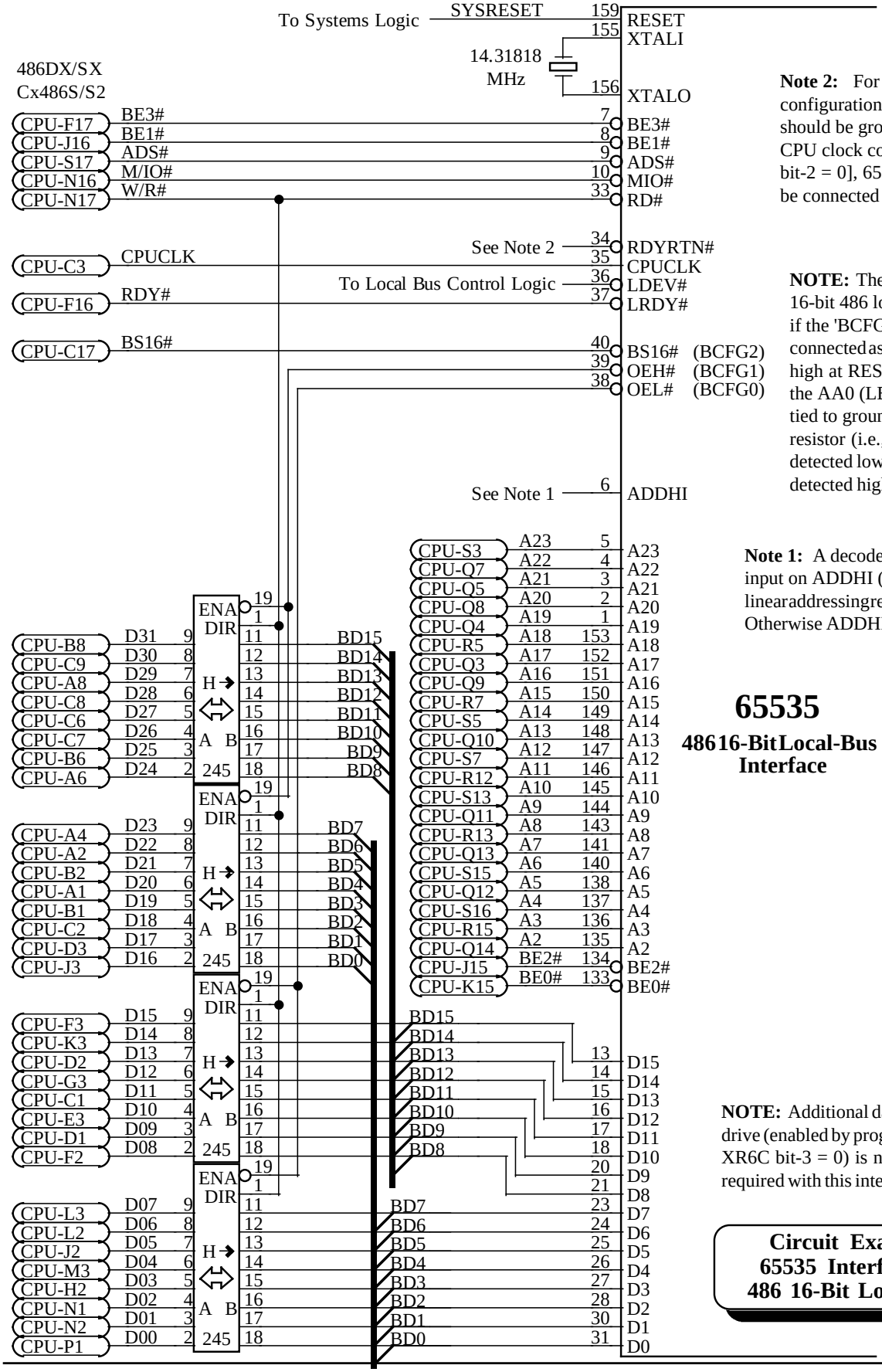
NOTE: The 65535 will select the 16-bit direct CPU interface if the 'BCFG' pins are connected as shown (and the AA0 and AA1 pins are detected high at RESET).

65535

486SLC / 386SX 16-Bit Local-Bus Interface

NOTE: Additional data output drive may be enabled by programming XR6C bit-3 = 0.

Circuit Example
65535 Local Bus Interface to 486SLC/386SX



Note 2: For normal 1x clock configuration, 65535 pin-34 should be grounded. For 2x CPU clock configuration [XR01 bit-2 = 0], 65535 pin-34 should be connected to CPURST#.

NOTE: The 65535 will select 16-bit 486 local bus operation if the 'BCFG' pins are connected as shown and detected high at RESET. In addition, the AA0 (LB#) pin must be tied to ground via a 4.7K resistor (i.e., AA0 must be detected low and AA1 must be detected high at RESET).

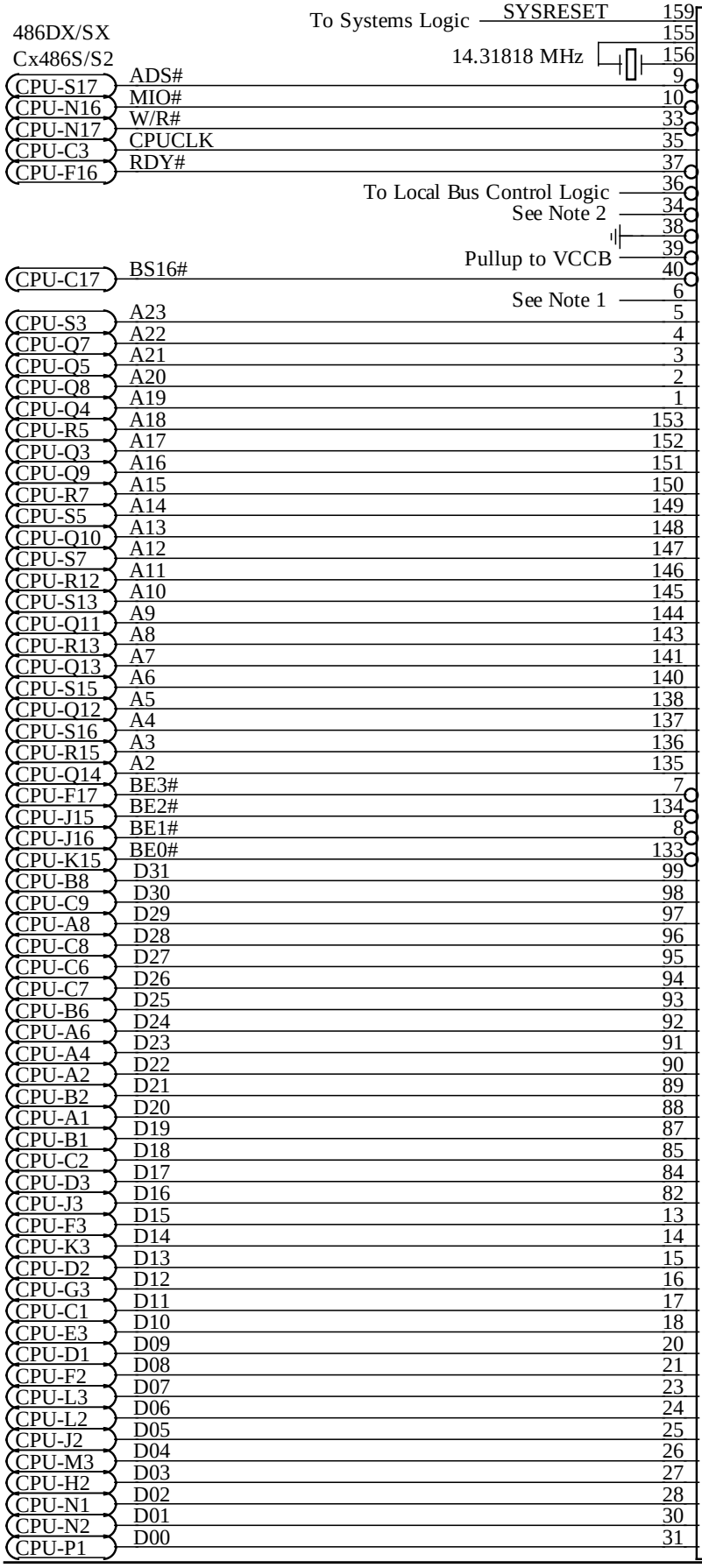
Note 1: A decode of A31-24 may be input on ADDHI (pin-6) to meet linear addressing requirements. Otherwise ADDHI must be grounded.

65535

486 16-Bit Local-Bus Interface

NOTE: Additional data output drive (enabled by programming XR6C bit-3 = 0) is not normally required with this interface.

Circuit Example
65535 Interface to
486 16-Bit Local Bus



NOTE: To select the 486 32-bit configuration, BCFG0 should be pulled to ground via a resistor and BCFG1 and 2 should be pulled to VCC via a resistor. To select auto configuration the AA0 and AA1 (ISA#) pins must both be left open. To force Local-bus pinout operation, the AA0 (LB#) pin must be tied to ground via a 4.7K resistor.

65535

486 32-Bit Local-Bus Interface

Note 1: A decode of A31-24 may be input on ADDHI (pin-6) to meet linear addressing requirements. Otherwise ADDHI must be grounded.

NOTE 2: For 1x clock configuration, RDYRTN# (pin-34) should be grounded. For 2x CPU clock configuration, RDYRTN# (pin 34) should be connected to CPURST#.

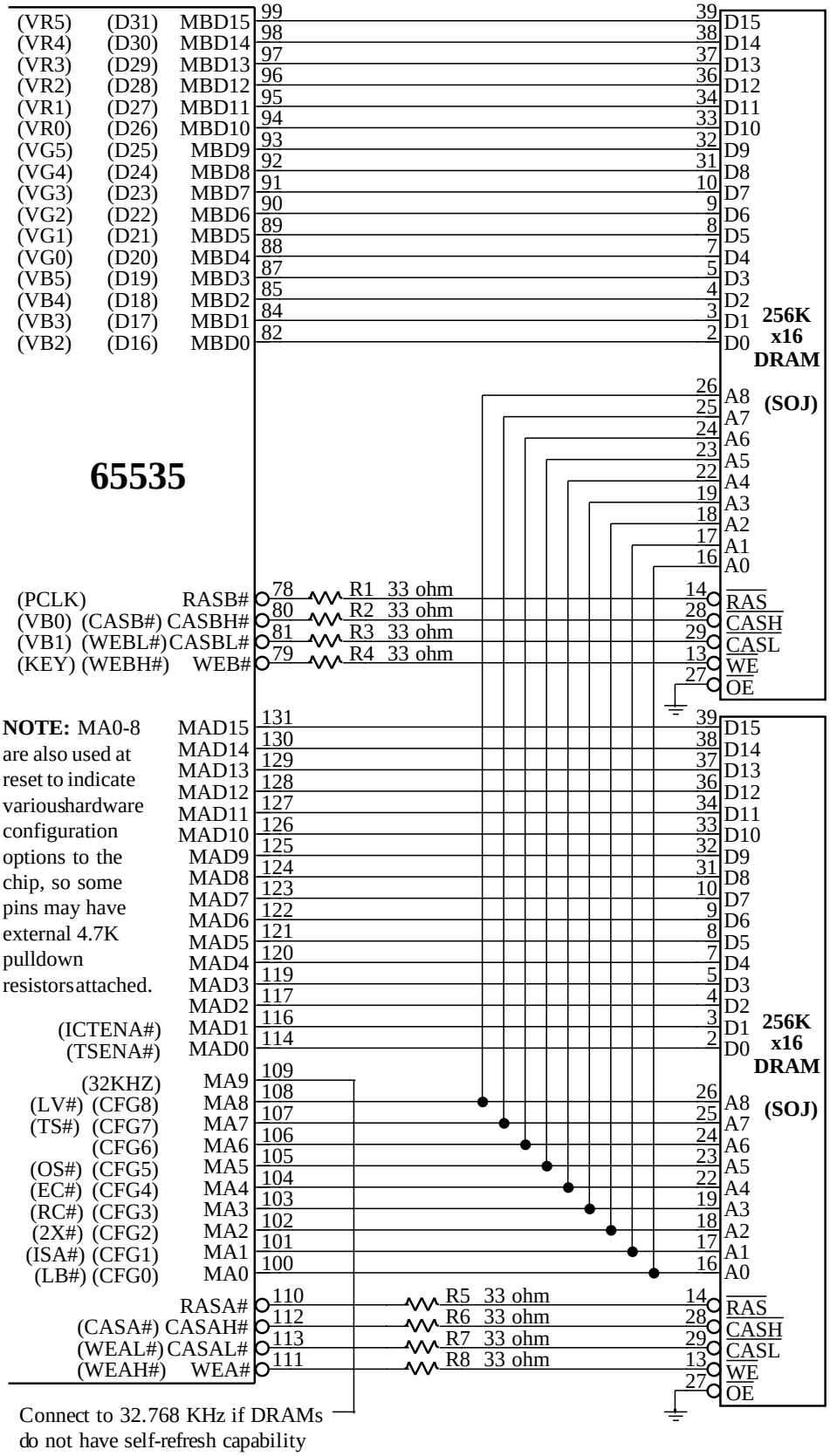
Per VL-Bus Spec:

LRDY# = Asychronous Ready
RDYRTN# = Sychronous Ready

NOTE: Only one 256Kx16 DRAM and no PC-Video is allowed with this bus configuration.

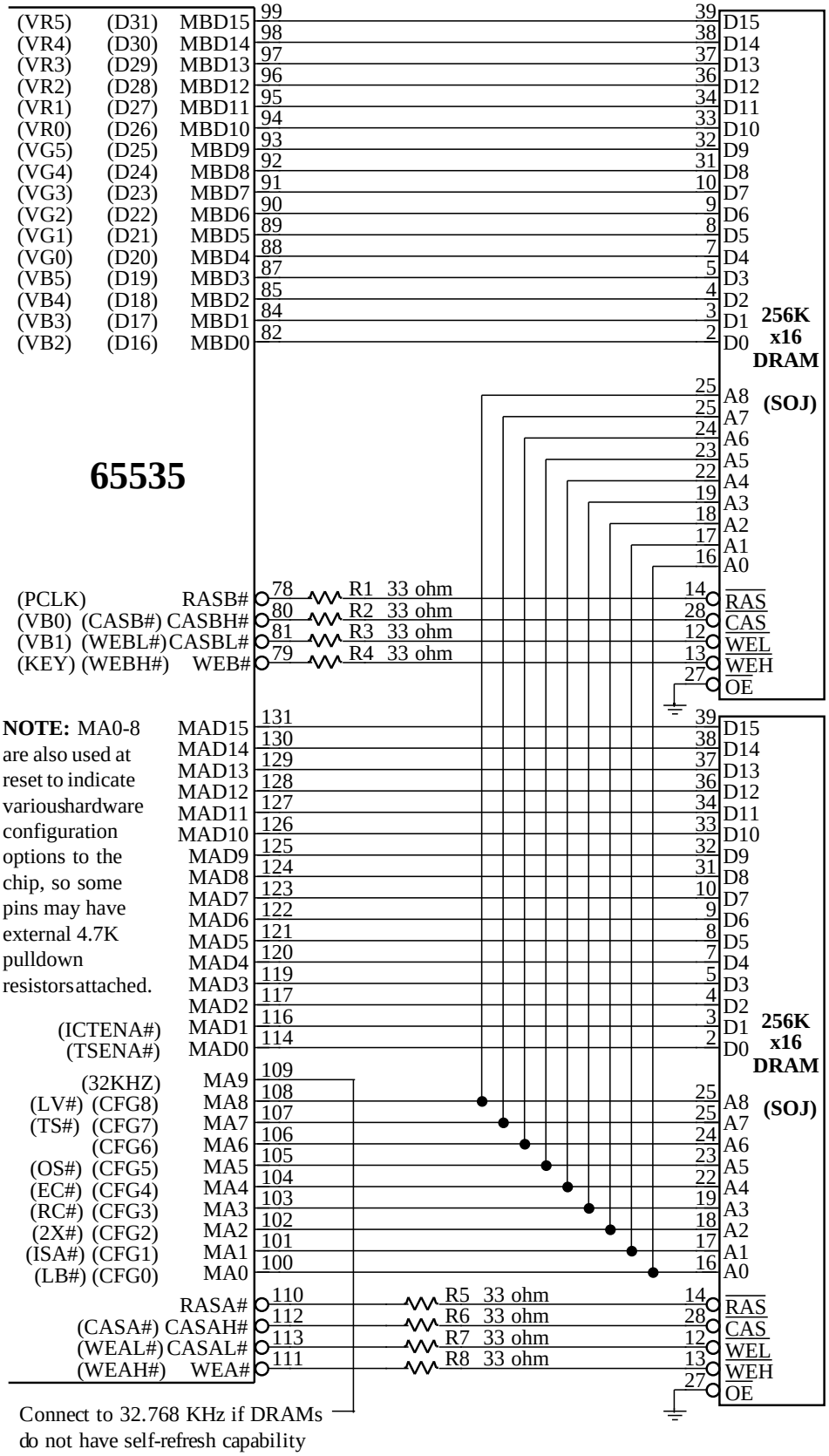
NOTE: Additional data output drive may be enabled by programming XR6C bit 3=0.

Circuit Example 65535 Interface to 486 32-Bit Local Bus



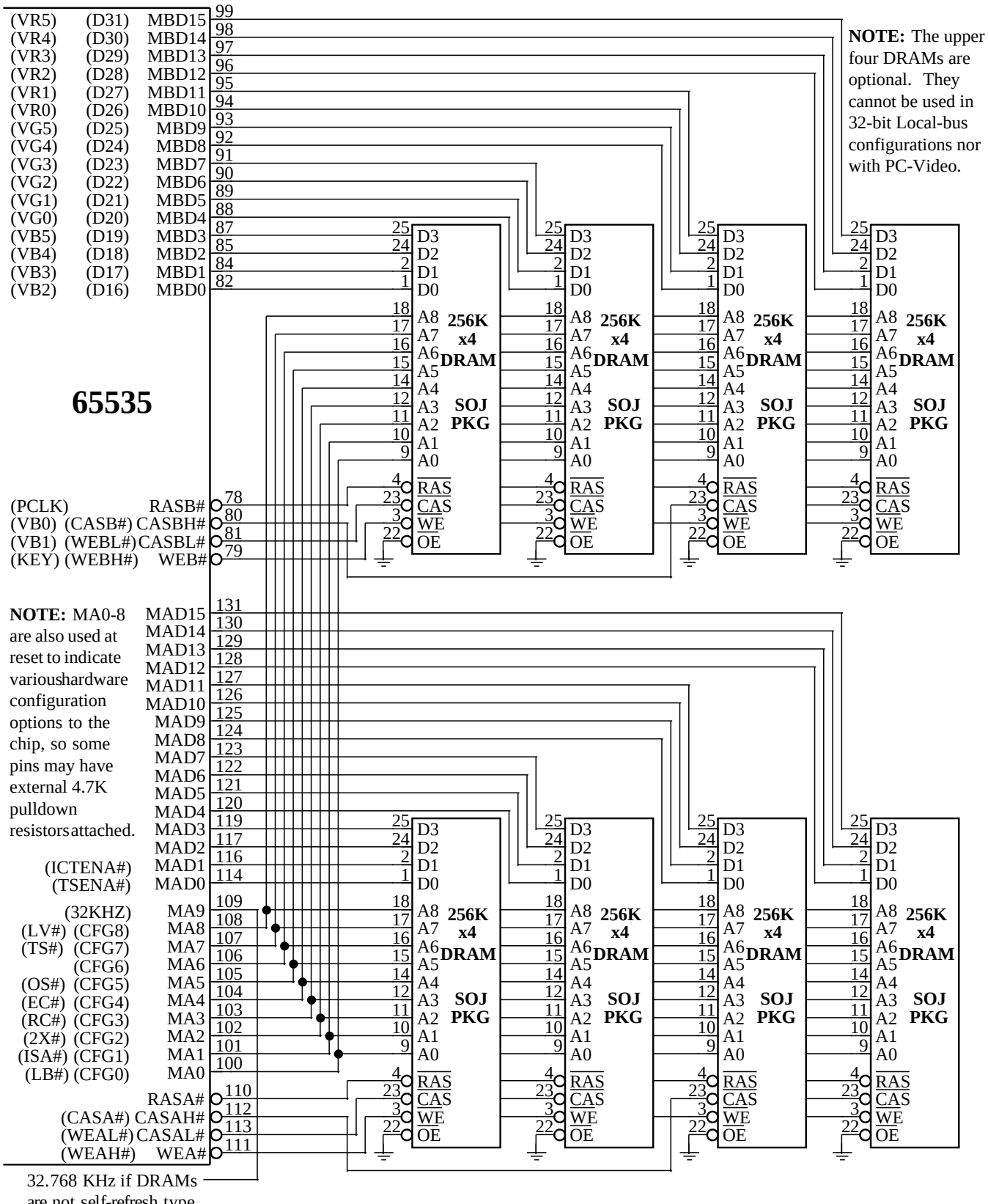
NOTE: The upper DRAM is optional. It cannot be used in 32-bit Local-bus configurations nor with PC-Video.

65535
Display Memory Circuit
One or Two
256Kx16 DRAMs
(Two-CAS)



NOTE: The upper DRAM is optional. It cannot be used in 32-bit Local-bus configurations nor with PC-Video.

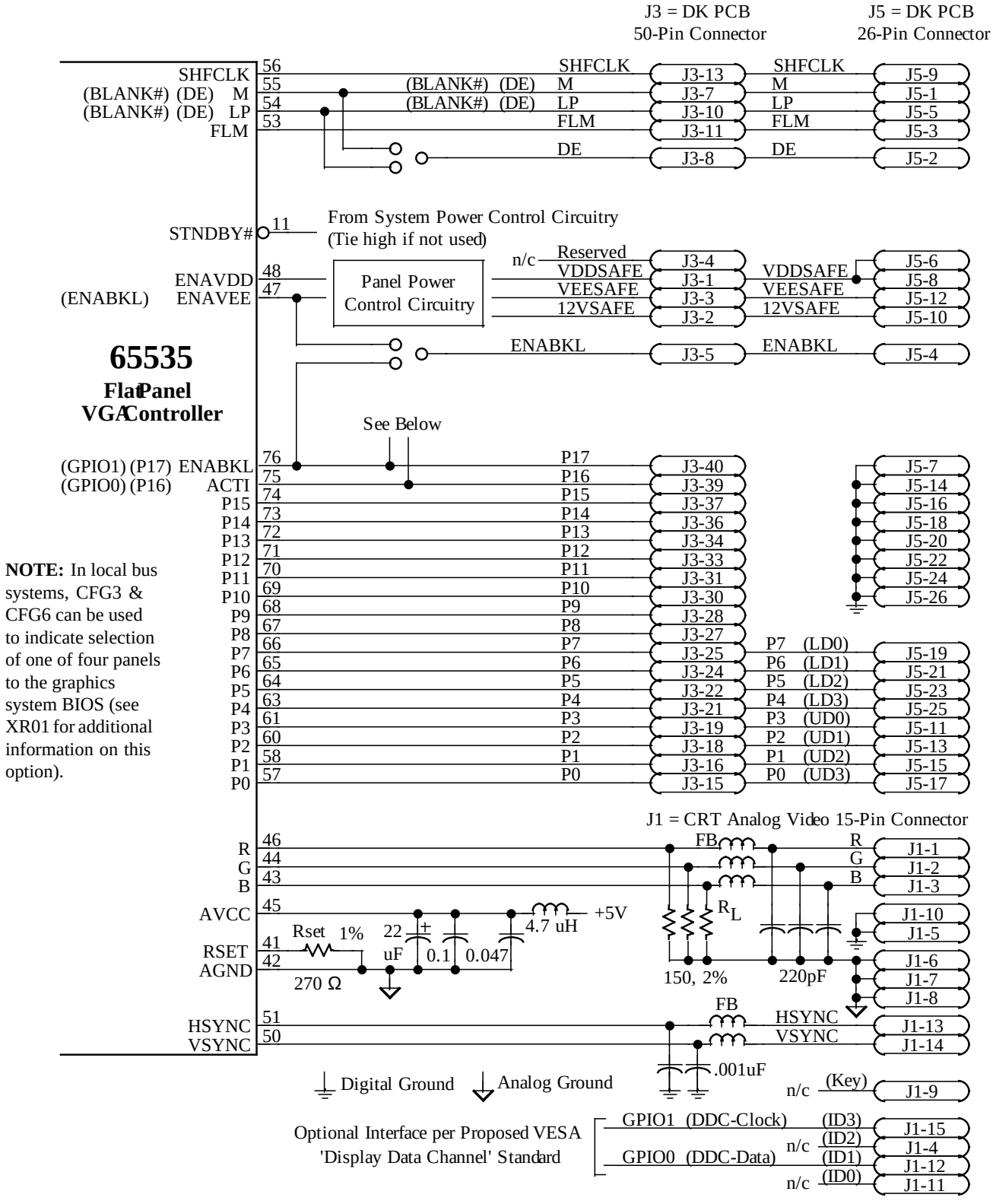
65535
Display Memory Circuit
One or Two
256Kx16 DRAMs
(Two-WE)



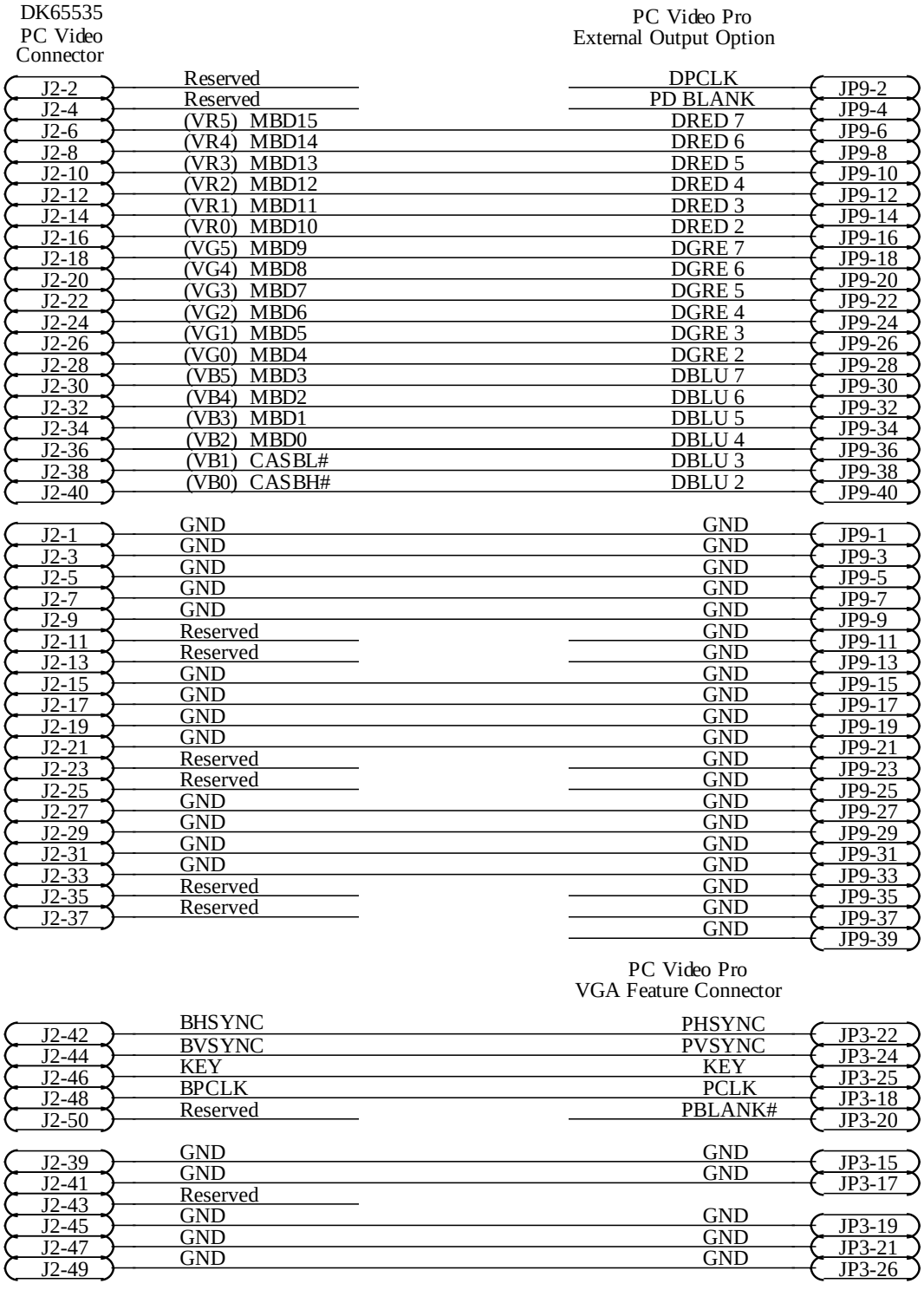
NOTE: The upper four DRAMs are optional. They cannot be used in 32-bit Local-bus configurations nor with PC-Video.

NOTE: MA0-8 are also used at reset to indicate various hardware configuration options to the chip, so some pins may have external 4.7K pulldown resistors attached.

65535 Display Memory Circuit - Four or Eight 256Kx4 DRAMs



65535 CRT/Panel Interface Circuit



65535 Interface to PC-Video

Panel Interface Examples

This section includes schematic examples showing how to connect the 65535 to various flat panel displays.

Plasma / EL Panels

	Mfr	Part Number	Panel Resolution	Panel Technology	Panel Drive	Panel Interface	Panel Data Transfer	Panel Gray Levels	Page
1)	Matsushita	S804	640x480	Plasma	SS	8-bit	2 Pixels/Clk	16	183
2)	Sharp	LJ64ZU50	640x480	EL	SS	8-bit	2 Pixels/Clk	16	184

Monochrome LCD Panels

	Mfr	Part Number	Panel Resolution	Panel Technology	Panel Drive	Panel Interface	Panel Data Transfer	Panel Gray Levels	Page
3)	Epson	EG-9005F-LS	640x480	LCD	DD	8-bit	8 Pixels/Clk	2	185
4)	Citizen	G6481L-FF	640x480	LCD	DD	8-bit	8 Pixels/Clk	2	186
5)	Sharp	LM64P80	640x480	LCD	DD	8-bit	8 Pixels/Clk	2	187
6)	Sanyo	LCM-6494-24NTK	640x480	LCD	DD	8-bit	8 Pixels/Clk	2	188
7)	Hitachi	LMG5364XUFC	640x480	LCD	DD	8-bit	8 Pixels/Clk	2	189
8)	Sanyo	LCM-5491-24NAK	1024x768	LCD	DD	16-bit	16 Pixels/Clk	2	190
9)	Epson	ECM-A9071	1024x768	LCD	DD	16-bit	16 Pixels/Clk	2	191
10)	Hitachi	LMG9060ZZFC	1024x768	LCD	DD	16-bit	16 Pixels/Clk	2	192
11)	Hitachi	LMG9100ZZFC	1280x1024	LCD	DD	16-bit	16 Pixels/Clk	2	193

Active Color Panels

	Mfr	Part Number	Panel Resolution	Panel Technology	Panel Drive	Panel Interface	Panel Data Transfer	Panel Colors	Page
10)	Hitachi	TM26D50VC2AA	640x480	TFT LCD	SS	9-bit	1 Pixel/Clk	512	198
11)	Sharp	LQ9D011	640x480	TFT LCD	SS	9-bit	1 Pixel/Clk	512	199
12)	Toshiba	LTM-09C015-1	640x480	TFT LCD	SS	9-bit	1 Pixel/Clk	512	200
13)	Sharp	LQ10D311	640x480	TFT LCD	SS	18-bit	1 Pixel/Clk	256K	201

Passive Color Panels

	Mfr	Part Number	Panel Resolution	Panel Technology	Panel Drive	Panel Interface	Panel Data Transfer	Panel Colors	Page
14)	Sharp	LM64C031	640x480	STN LCD	SS	8-bit	2-2/3 Pixels/Clk	8	202
15)	Sanyo	LM-CK53-22NEZ	640x480	STN LCD	SS	16-bit	5-1/3 Pixels/Clk	8	203
16)	Sanyo	LCM5327-24NAK	640x480	STN LCD	SS	16-bit	5-1/3 Pixels/Clk	8	204
17)	Kyocera	KCL6448	640x480	STN LCD	DD	8-bit	2-2/3 Pixels/Clk	8	205
18)	Hitachi	LMG9720XUFC	640x480	STN LCD	DD	8-bit	2-2/3 Pixels/Clk	8	206
19)	Sharp	LM64C08P	640x480	STN LCD	DD	16-bit	5-1/3 Pixels/Clk	8	207
20)	Sanyo	LCM5331-22NTK	640x480	STN LCD	DD	16-bit	5-1/3 Pixels/Clk	8	208
21)	Hitachi	LMG9721XUFC	640x480	STN LCD	DD	16-bit	5-1/3 Pixels/Clk	8	209
22)	Toshiba	TLX-8062S-C3X	640x480	STN LCD	DD	16-bit	5-1/3 Pixels/Clk	8	210
23)	Optrex	DMF-50351NC-FW	640x480	STN LCD	DD	16-bit	5-1/3 Pixels/Clk	8	211

Glossary:

SS = Single Panel Single Scan
DD = Dual Panel Dual Scan
TFT = Thin Film Transistor ('Active Matrix')
STN = Super Twist Nematic ('Passive Matrix')

Flat Panel Interface Examples

65535 Pin#	65535 Pin Name	DK65535 26-Pin Connector	DK65535 50-Pin Connector	Mono SS 8-bit	Mono DD 8-bit	Mono DD 16-bit	Color TFT 15-bit	Color TFT 18-bit	Color STN 8-bit	Color STN 16-bit	Color STNDD 8-bit	Color STNDD 16-bit
	Pixels Transferred Per Shift Clock:			8	8	16	1	1	2-2/3	5-1/3	2-2/3	5-1/3
57	P0	17	15	–	UD3	UD7	B0	B0	R1...	R1...	UR1...	UR1...
58	P1	15	16	–	UD2	UD6	B1	B1	B1...	G1...	UG1...	UG1...
60	P2	13	18	–	UD1	UD5	B2	B2	G2...	B1...	UB1...	UB1...
61	P3	11	19	–	UD0	UD4	B3	B3	R3...	R2...	UR2...	UR2...
63	P4	25	21	–	LD3	UD3	B4	B4	B3...	G2...	LR1...	LR1...
64	P5	23	22	–	LD2	UD2	G0	B5	G4...	B2...	LG1...	LG1...
65	P6	21	24	–	LD1	UD1	G1	G0	R5...	R3...	LB1...	LB1...
66	P7	19	25	–	LD0	UD0	G2	G1	B5...	G3...	LR2...	LR2...
67	P8	–	27	P0	–	LD7	G3	G2	**SHFCLKU**	B3...	–	UG2...
68	P9	–	28	P1	–	LD6	G4	G3	–	R4...	–	UB2...
69	P10	–	30	P2	–	LD5	**R0** †	G4	–	G4...	–	UR3...
70	P11	–	31	P3	–	LD4	**R1** †	G5	–	B4...	–	UG3...
71	P12	–	33	P4	–	LD3	**R2** †	R0	–	R5...	–	LG2...
72	P13	–	34	P5	–	LD2	**R3** †	R1	–	G5...	–	LB2...
73	P14	–	36	P6	–	LD1	**R4** †	R2	–	B5...	–	LR3...
74	P15	–	37	P7	–	LD0	**–** †	R3	–	R6...	–	LG3...
75	P16	–	39	–	–	–	–	R4	–	–	–	–
76	P17	–	40	–	–	–	–	R5	–	–	–	–
75	ACTI	–	–	ACTI	ACTI	ACTI	ACTI	–	ACTI	ACTI	ACTI	ACTI
47 or 76	ENABKL	4	5	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL
56	SHFCLK	9	13	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	**SHFCLKL**	SHFCLK	SHFCLK	SHFCLK
55	M	1	7	M	M	M	M	M	M	M	M	M
54	LP	5	10	LP	LP	LP	LP	LP	LP	LP	LP	LP
53	FLM	3	11	FLM	FLM	FLM	FLM	FLM	FLM	FLM	FLM	FLM
54 or 55	DE	2	8	DE	DE	DE	DE	DE	DE	DE	DE	DE
–	VDDSAFE	6, 8	1	–	–	–	–	–	–	–	–	–
–	+12VSAFE	10	2	–	–	–	–	–	–	–	–	–
–	VEESAFE	12	3	–	–	–	–	–	–	–	–	–
–	GND	7,14,16	6,9,12,14,	–	–	–	–	–	–	–	–	–
		18,20,22	17,20,23,26									
		24, 26	29,32,35,38,									
			41,44,47,50									

† **6554x** provides **16-bit** TFT output (5-6-5)
65535 provides **15-bit** TFT output (5-5-5)

J 5

M	1	2	DE
FLM	3	4	ENABKL
LP	5	6	**VDDSAFE (+5V)**
GND	7	8	**VDDSAFE (+5V)**
SHFCLK	9	10	**+12 VSAFE**
UD0	11	12	**VEESAFE**
UD1	13	14	GND
UD2	15	16	GND
UD3	17	18	GND
LD0	19	20	GND
LD1	21	22	GND
LD2	23	24	GND
LD3	25	26	GND

(-12V TO -45V) or (+12V TO +45V)

DevelopmentBoard Panel Connectors

J 3

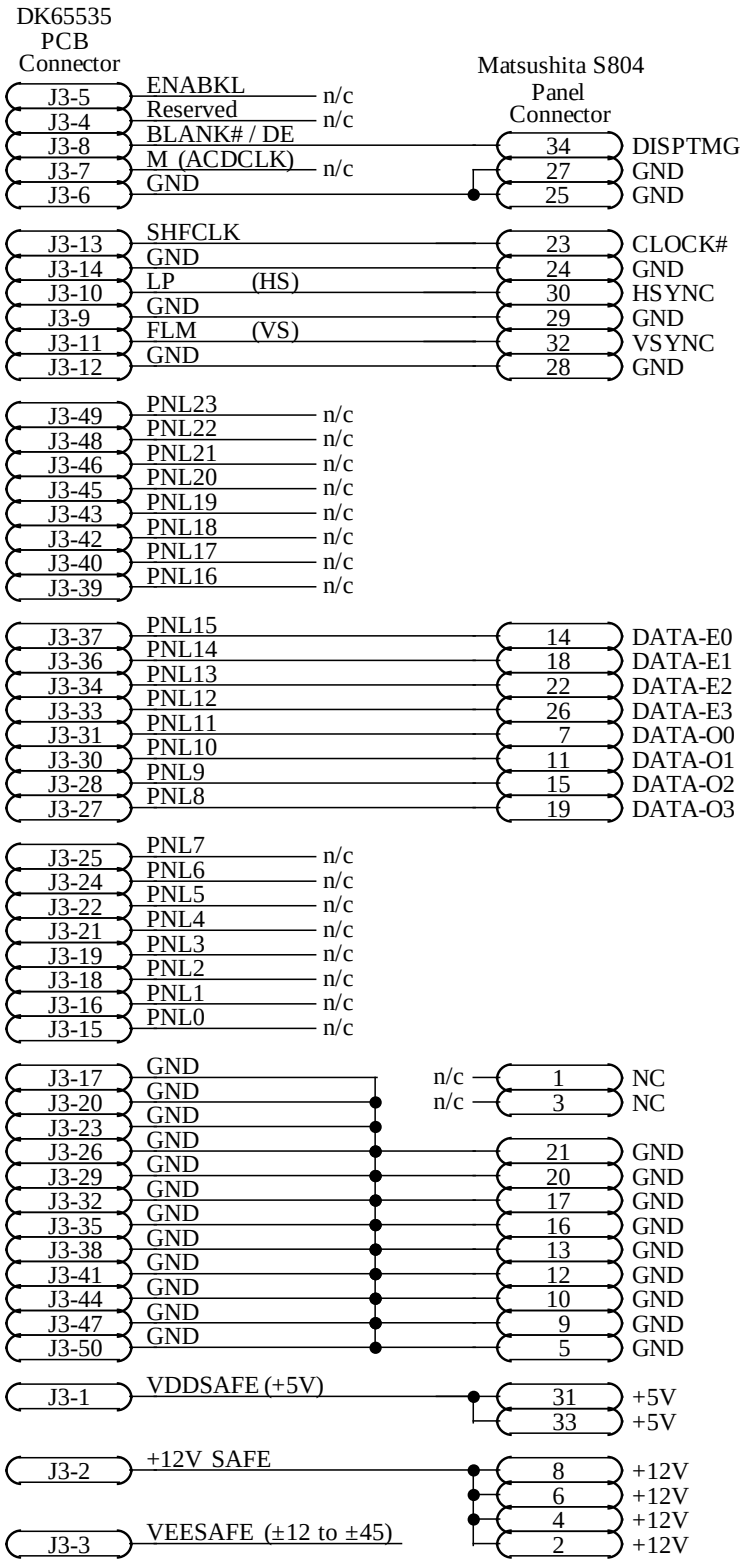
[+5V] VDDSAFE	1	2	**+12 VSAFE**
VEESAFE	3	4	Reserved
ENABKL	5	6	GND
M	7	8	DE
GND	9	10	LP
FLM	11	12	GND
SHFCLK	13	14	GND
P0	15	16	P1
GND	17	18	P2
P3	19	20	GND
P4	21	22	P5
GND	23	24	P6
P7	25	26	GND
P8	27	28	P9
GND	29	30	P10
P11	31	32	GND
P12	33	34	P13
GND	35	36	P14
P15	37	38	GND
P16	39	40	P17
GND	41	42	NC {P18}
{P19} NC	43	44	GND
{P20} NC	45	46	NC {P21}
GND	47	48	NC {P22}
{P23} NC	49	50	GND

{ P18-P23 } *FOR FUTURE USE*

J 2

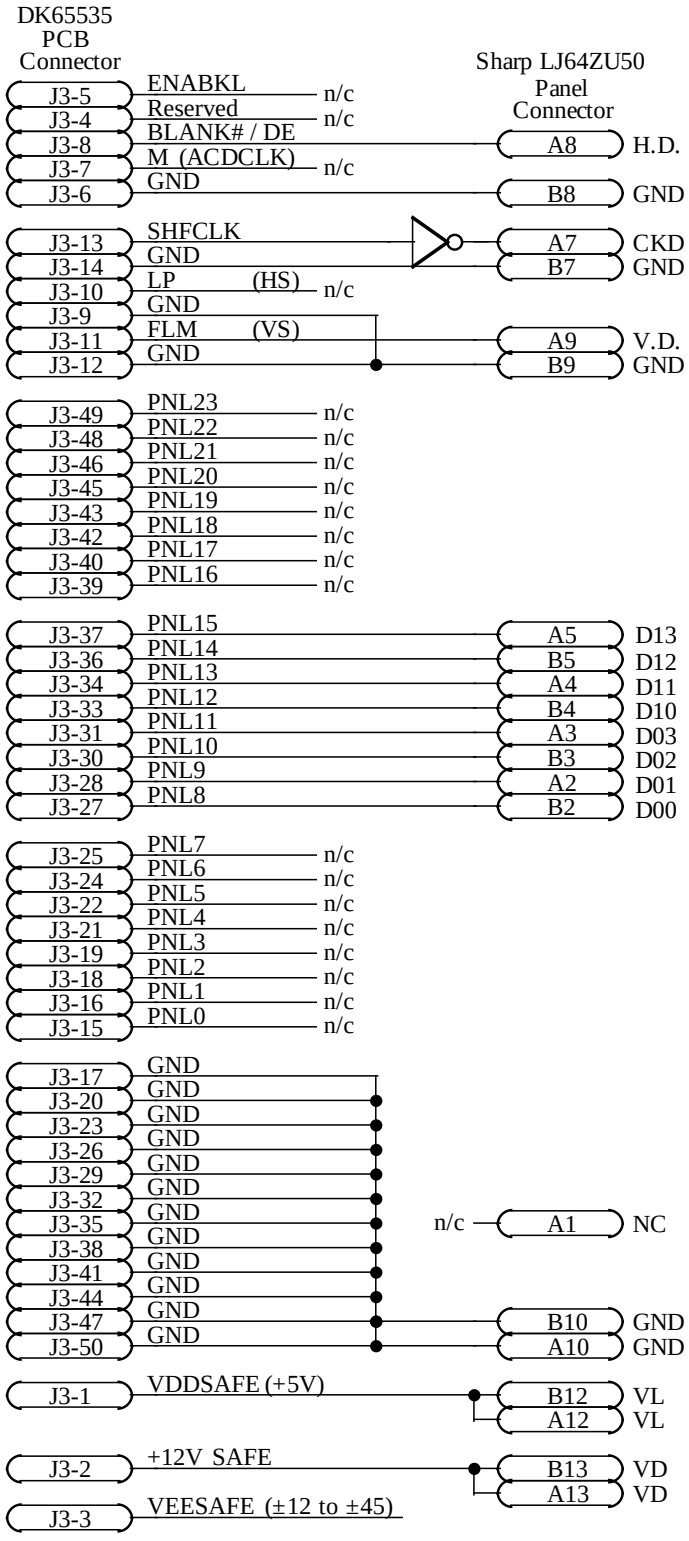
GND	1	2	[DPCLK]
GND	3	4	[BLANK#]
GND	5	6	**VR5**
GND	7	8	**VR4**
GND	9	10	**VR3**
[Reserved]	11	12	**VR2**
[Reserved]	13	14	**VR1**
GND	15	16	**VR0**
GND	17	18	**VG5**
GND	19	20	**VG4**
GND	21	22	**VG3**
[Reserved]	23	24	**VG2**
[Reserved]	25	26	**VG1**
GND	27	28	**VG0**
GND	29	30	**VB5**
GND	31	32	**VB4**
GND	33	34	**VB3**
[Reserved]	35	36	**VB2**
[Reserved]	37	38	**VB1**
GND	39	40	**VB0**
GND	41	42	**HSYNC**
[Reserved]	43	44	**VSYNC**
GND	45	46	**KEY**
GND	47	48	**PCLK**
GND	49	50	[Reserved]

Development Board PC-Video Connector



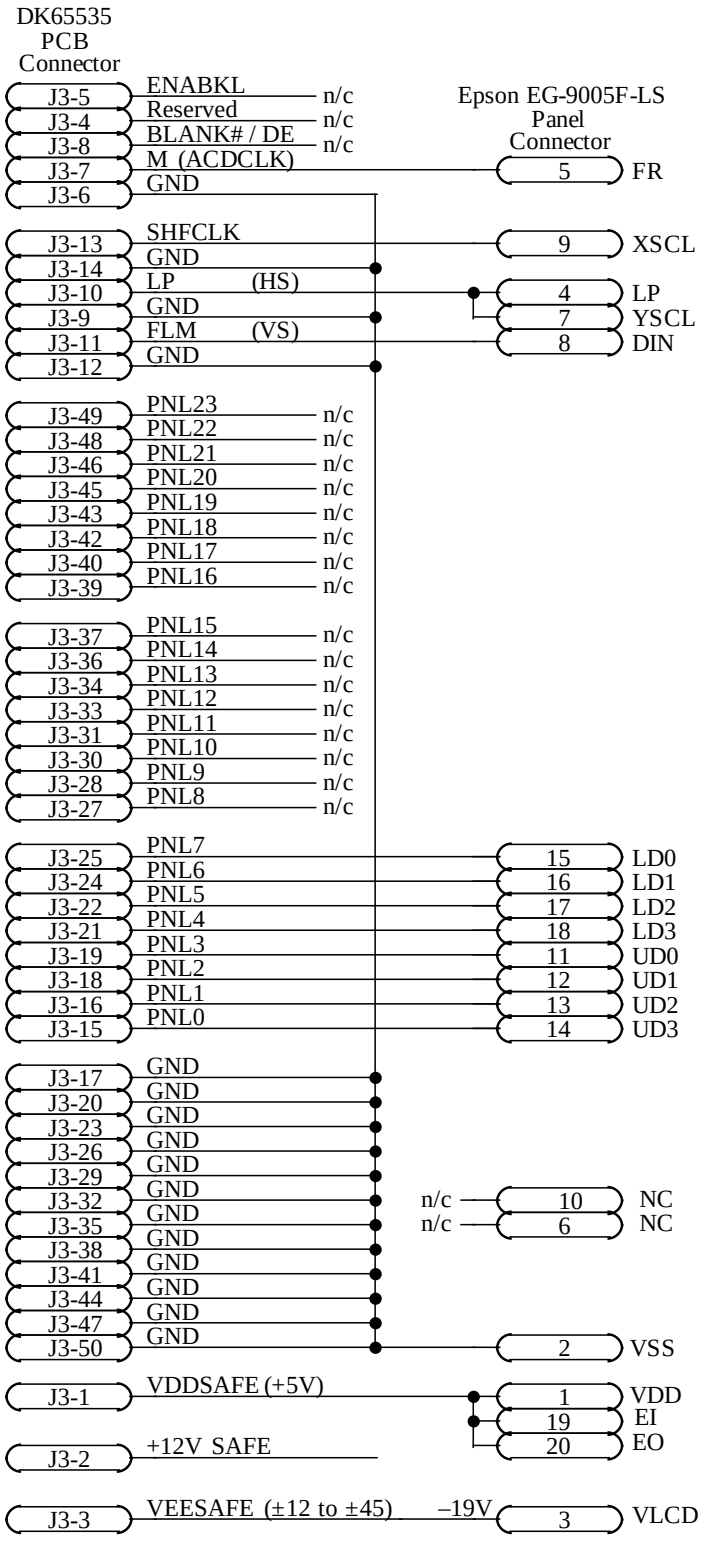
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]	00	
Clock Divide (CD)	XR50[6-4]	001	
Shiftclk Div (SD)	XR51[3]	0	
Gray/Color Levels	XR4F[2-0]	100	
TFT Data Width	XR50[7]	0	n/a
STN Pixel Packing	XR53[5-4]	00	n/a
Frame Accel Ena	XR6F[1]	0	Disabled
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]	0	
LP Delay Disable	XR2F[6]	0	
LP Delay (Hcomp disa)	XR2F/2D	062h	
LP Delay (Hcomp ena)	XR2F/2E	06Dh	
LP Pulse Width	XR2F[3-0]	8h	
LP Polarity	XR54[6]	0	
LP Blank	XR4F[7]	0	
LP Active during V	XR51[7]	1	
FLM Delay Disable	XR2F[7]	0	
FLM Delay	XR2C	04h	
FLM Polarity	XR54[7]	0	
Blank#/DE Polarity	XR54[0]	1	
Blank#/DE H-Only	XR54[1]	0	
Blank#/DE CRT/FP	XR51[2]	1	
Alt Hsync Start (CR04)	XR19	60h	
Alt Hsync End (CR05)	XR1A	00h	
Alt H Total (CR00)	XR1B	60h	
Alt V Total (CR06)	XR65/64	20Dh	
Alt Vsync Start (CR10)	XR65/66	1E8h	
Alt Vsync End (CR11)	XR67[3-0]	0Ah	
Alt Hsync Polarity	XR55[6]	1	
Alt Vsync Polarity	XR55[7]	1	
Display Quality Recommendations			
FRC	XR50[1-0]	11	
FRC Option 1	XR53[2]	1	Set to 1
FRC Option 2	XR53[3]	1	Set to 1
FRC Option 3	XR53[6]	0	
FRC Polynomial	XR6E[7-0]		n/a
Dither	XR50[3-2]	01	
M Phase Change	XR5E[7]		n/a
M Phase Change Count	XR5E[6-0]		n/a
Compensation Typical Settings			
H Compensation	XR55[0]	1	
V Compensation	XR57[0]	1	
Fast Centering Disable	XR57[7]	0	
H AutoCentering	XR55[1]	0	
V AutoCentering	XR57[1]	1	
H Centering	XR56	00h	
V Centering	XR59/58	000h	
H Text Compression	XR55[2]	1	
H AutoDoubling	XR55[5]	1	
V Text Stretching	XR57[2]	1	
V Text Stretch Mode	XR57[4-3]	11	
V Stretching	XR57[5]	0	
V Stretching Mode	XR57[6]	0	
V Line Insertion Height	XR59[3-0]	0Fh	
V H/W Line Replication	XR59[7]	0	
V Line Repl Height	XR5A[3-0]	0	

65535 Interface - Matsushita S804 (640x480 16-Gray Level Plasma Panel)



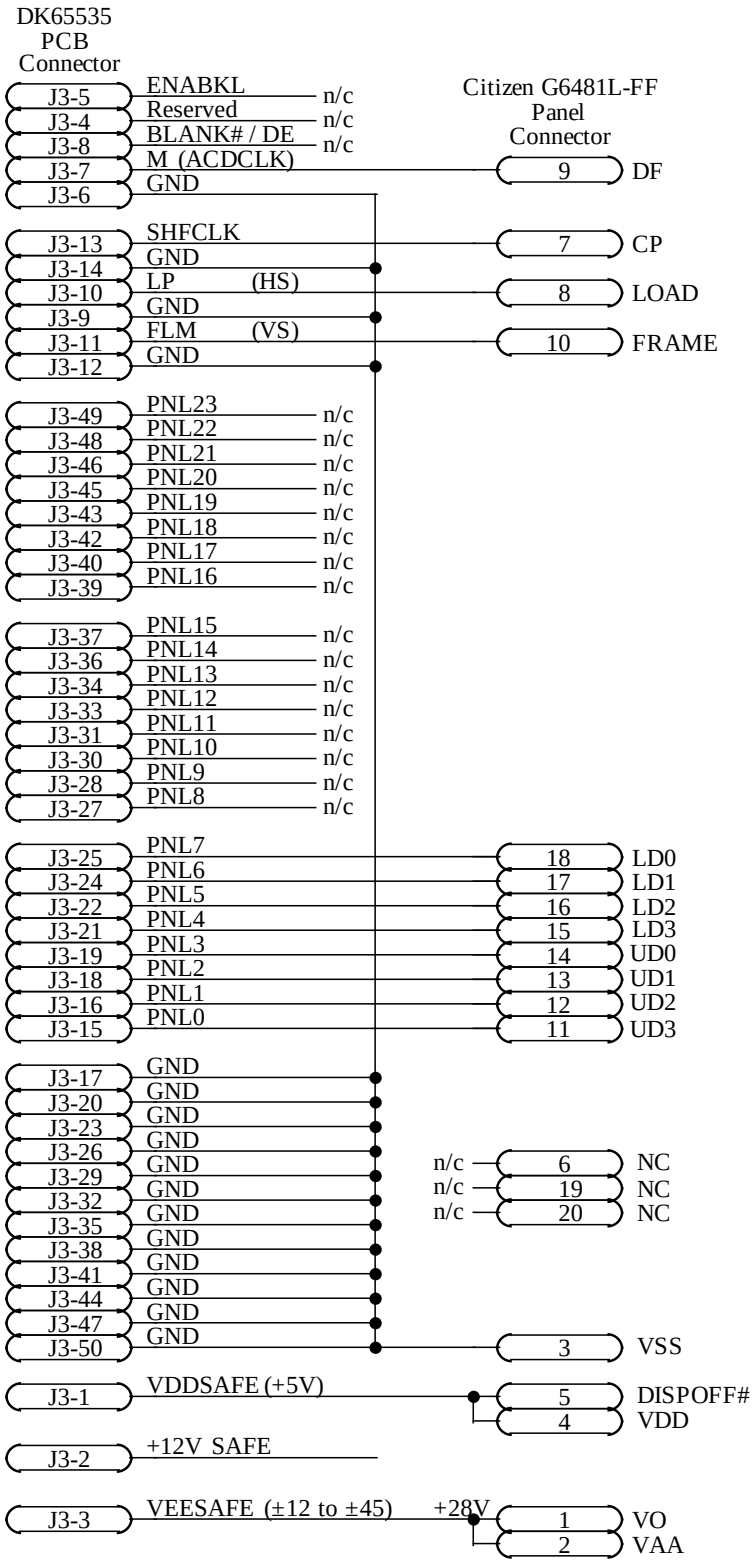
Programming	**Recommendations/Requirements**		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]	00	
Clock Divide (CD)	XR50[6-4]	001	
Shiftclk Div (SD)	XR51[3]	0	
Gray/Color Levels	XR4F[2-0]	100	
TFT Data Width	XR50[7]	0	n/a
STN Pixel Packing	XR53[5-4]	00	n/a
Frame Accel Ena	XR6F[1]	0	Disabled
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]	0	
LP Delay Disable	XR2F[6]	0	
LP Delay (Hcomp disa)	XR2F/2D	04Fh	
LP Delay (Hcomp ena)	XR2F/2E	04Eh	
LP Pulse Width	XR2F[3-0]	01h	
LP Polarity	XR54[6]	1	
LP Blank	XR4F[7]	0	
LP Active during V	XR51[7]	1	
FLM Delay Disable	XR2F[7]	1	
FLM Delay	XR2C	0Ch	
FLM Polarity	XR54[7]	1	
Blank#/DE Polarity	XR54[0]	1	
Blank#/DE H-Only	XR54[1]	0	
Blank#/DE CRT/FP	XR51[2]	1	
Alt Hsync Start (CR04)	XR19	52h	
Alt Hsync End (CR05)	XR1A	15h	
Alt H Total (CR00)	XR1B	54h	
Alt V Total (CR06)	XR65/64	1F0h	
Alt Vsync Start (CR10)	XR65/66	1E5h	
Alt Vsync End (CR11)	XR67[3-0]	0Eh	
Alt Hsync Polarity	XR55[6]	1	
Alt Vsync Polarity	XR55[7]	1	
Display Quality Recommendations			
FRC	XR50[1-0]	11	
FRC Option 1	XR53[2]	1	Set to 1
FRC Option 2	XR53[3]	1	Set to 1
FRC Option 3	XR53[6]	0	
FRC Polynomial	XR6E[7-0]		n/a
Dither	XR50[3-2]	01	
M Phase Change	XR5E[7]		n/a
M Phase Change Count	XR5E[6-0]		n/a
Compensation Typical Settings			
H Compensation	XR55[0]	1	
V Compensation	XR57[0]	1	
Fast Centering Disable	XR57[7]	0	
H AutoCentering	XR55[1]	0	
V AutoCentering	XR57[1]	0	
H Centering	XR56	00h	
V Centering	XR59/58	000h	
H Text Compression	XR55[2]	1	
H AutoDoubling	XR55[5]	1	
V Text Stretching	XR57[2]	0	
V Text Stretch Mode	XR57[4-3]	11	
V Stretching	XR57[5]	0	
V Stretching Mode	XR57[6]	0	
V Line Insertion Height	XR59[3-0]	0Fh	
V H/W Line Replication	XR59[7]	0	
V Line Repl Height	XR5A[3-0]	0	

65535 Interface - Sharp LJ64ZU50 (640x480 16-Gray Level EL Panel)



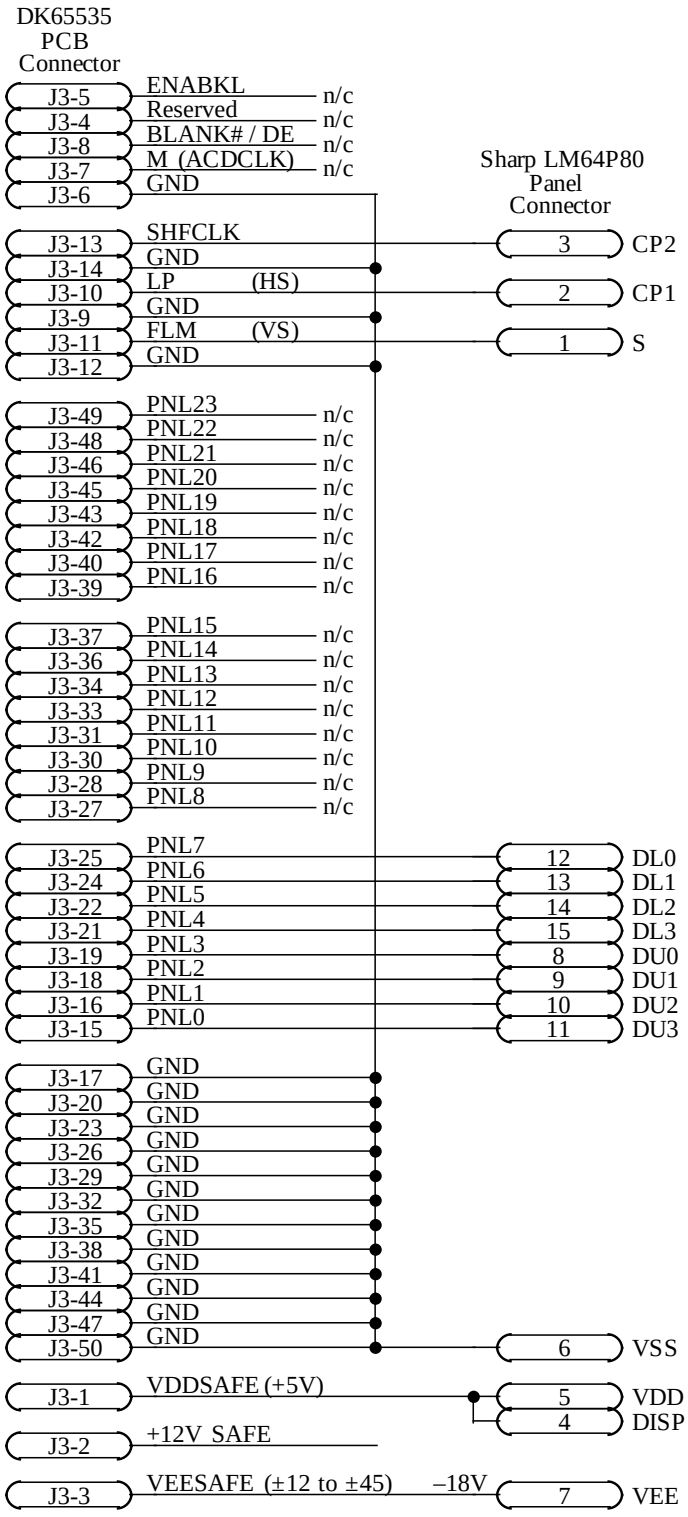
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Epson EG-9005F-LS (640x480 Monochrome LCD DD Panel)



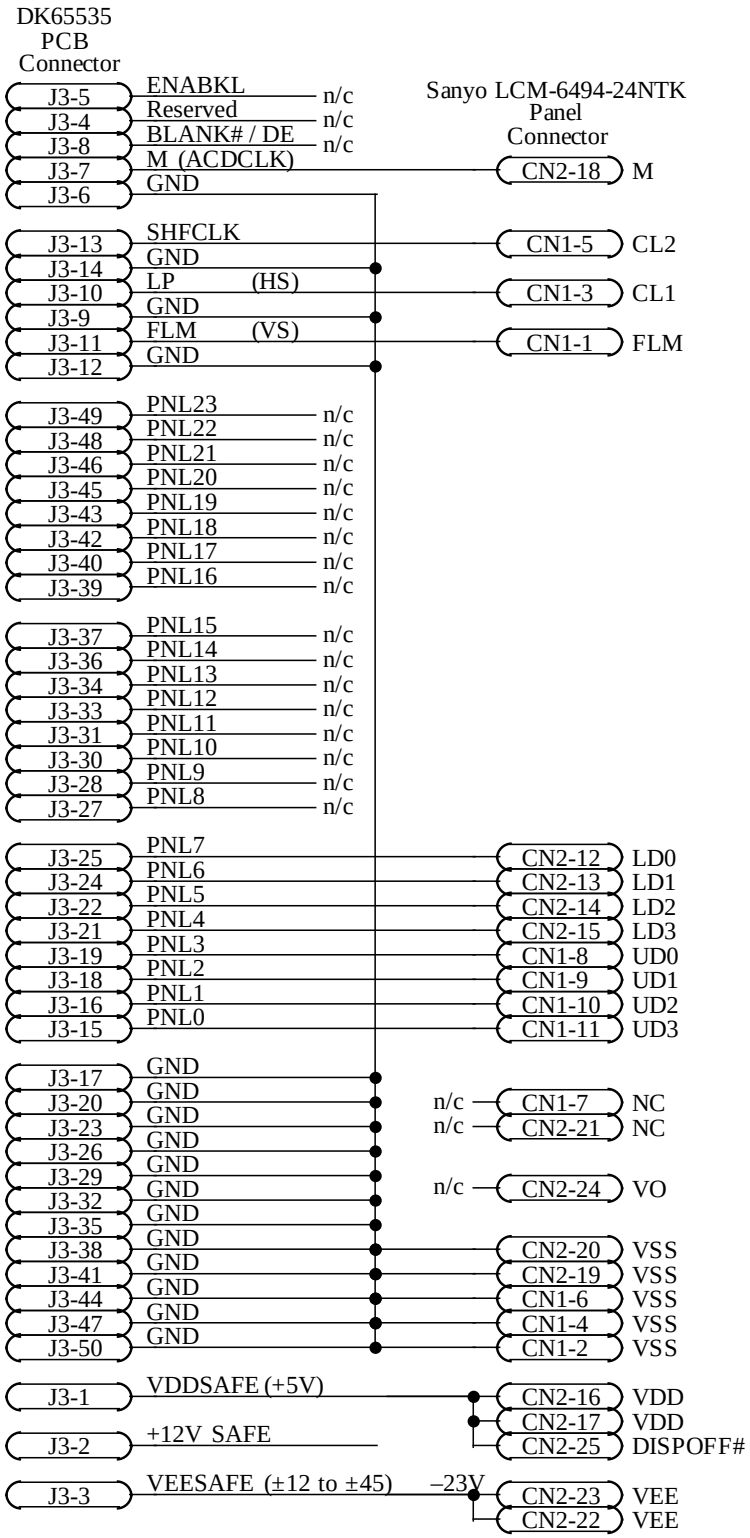
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Citizen G6481L-FF (640x480 Monochrome LCD DD Panel)



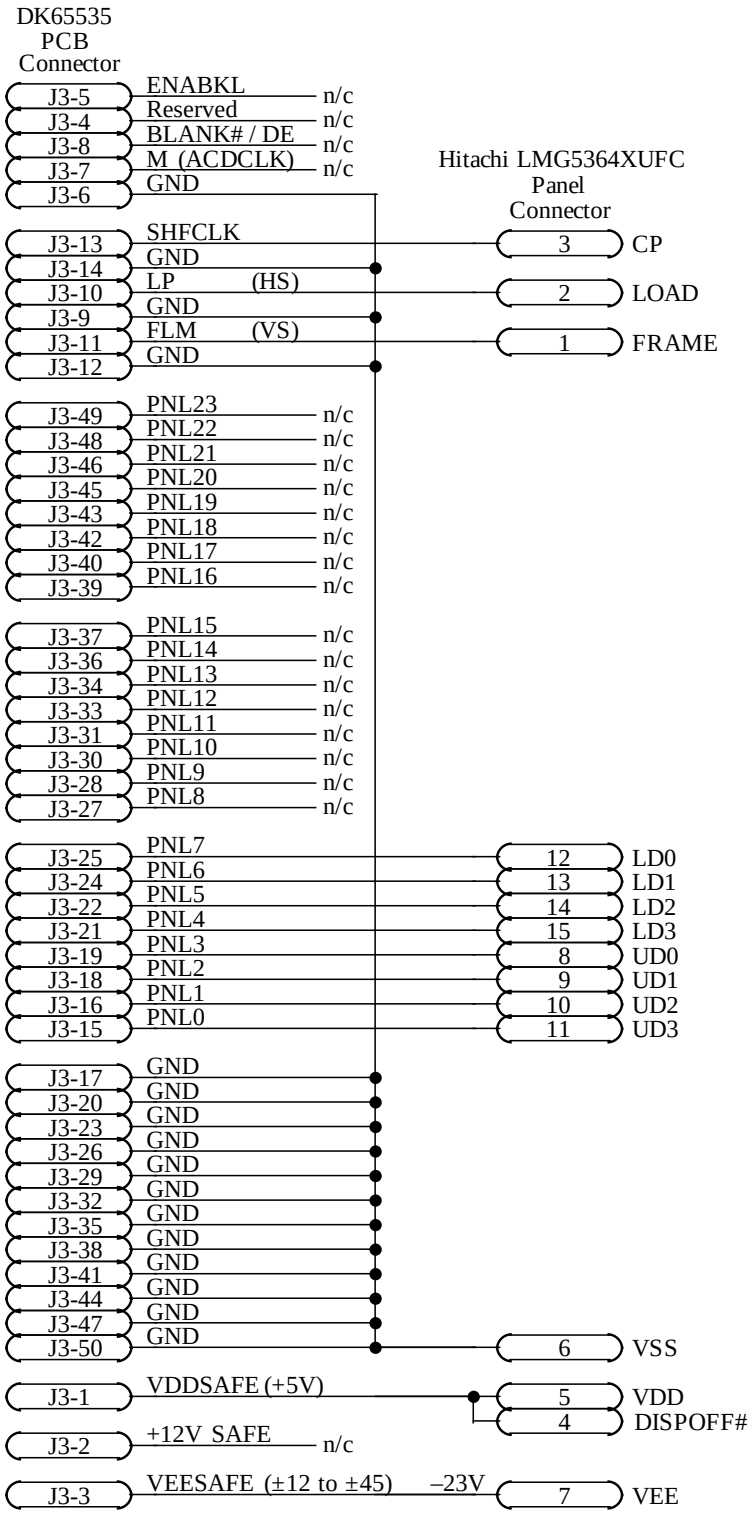
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]	11	DD
Clock Divide (CD)	XR50[6-4]	010	Dclk / 4
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]	100	16Level (61w/dith)
TFT Data Width	XR50[7]	0	n/a
STN Pixel Packing	XR53[5-4]	0	n/a
Frame Accel Ena	XR6F[1]	1	Enabled
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]	0	Enabled
LP Delay (Hcomp disa)	XR2F/2D	050h	
LP Delay (Hcomp ena)	XR2F/2E	050h	
LP Pulse Width	XR2F[3-0]	0h	
LP Polarity	XR54[6]		
LP Blank	XR4F[7]	0	
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]	0	Enabled
FLM Delay	XR2C	04h	4 lines
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19	57h	
Alt Hsync End (CR05)	XR1A	19h	
Alt H Total (CR00)	XR1B	59h	
Alt V Total (CR06)	XR65/64	1E4h	
Alt Vsync Start (CR10)	XR65/66	1E0h	
Alt Vsync End (CR11)	XR67[3-0]	1	
Alt Hsync Polarity	XR55[6]	1	Negative
Alt Vsync Polarity	XR55[7]	1	Negative
Display Quality Recommendations			
FRC	XR50[1-0]	01	16-Frame FRC
FRC Option 1	XR53[2]	1	Set to 1
FRC Option 2	XR53[3]	1	Set to 1
FRC Option 3	XR53[6]	0	n/a
FRC Polynomial	XR6E[7-0]	26h	
Dither	XR50[3-2]	01	256-color modes
M Phase Change	XR5E[7]	1	Every other frame
M Phase Change Count	XR5E[6-0]	00h	n/a
Compensation Typical Settings			
H Compensation	XR55[0]	1	Enabled
V Compensation	XR57[0]	1	Enabled
Fast Centering Disable	XR57[7]	0	Enabled
H AutoCentering	XR55[1]	0	Disabled
V AutoCentering	XR57[1]	1	Enabled
H Centering	XR56	00h	No left border
V Centering	XR59/58	000h	No top border
H Text Compression	XR55[2]	1	Enabled
H AutoDoubling	XR55[5]	1	Enabled
V Text Stretching	XR57[2]	0	Disabled
V Text Stretch Mode	XR57[4-3]	11	DS+TF,TF,DS
V Stretching	XR57[5]	0	Disabled
V Stretching Mode	XR57[6]	0	n/a
V Line Insertion Height	XR59[3-0]	0Fh	16 – 1
V H/W Line Replication	XR59[7]	0	Disabled
V Line Repl Height	XR5A[3-0]	0	n/a

65535 Interface - Sharp LM64P80 (640x480 Monochrome LCD DD Panel)



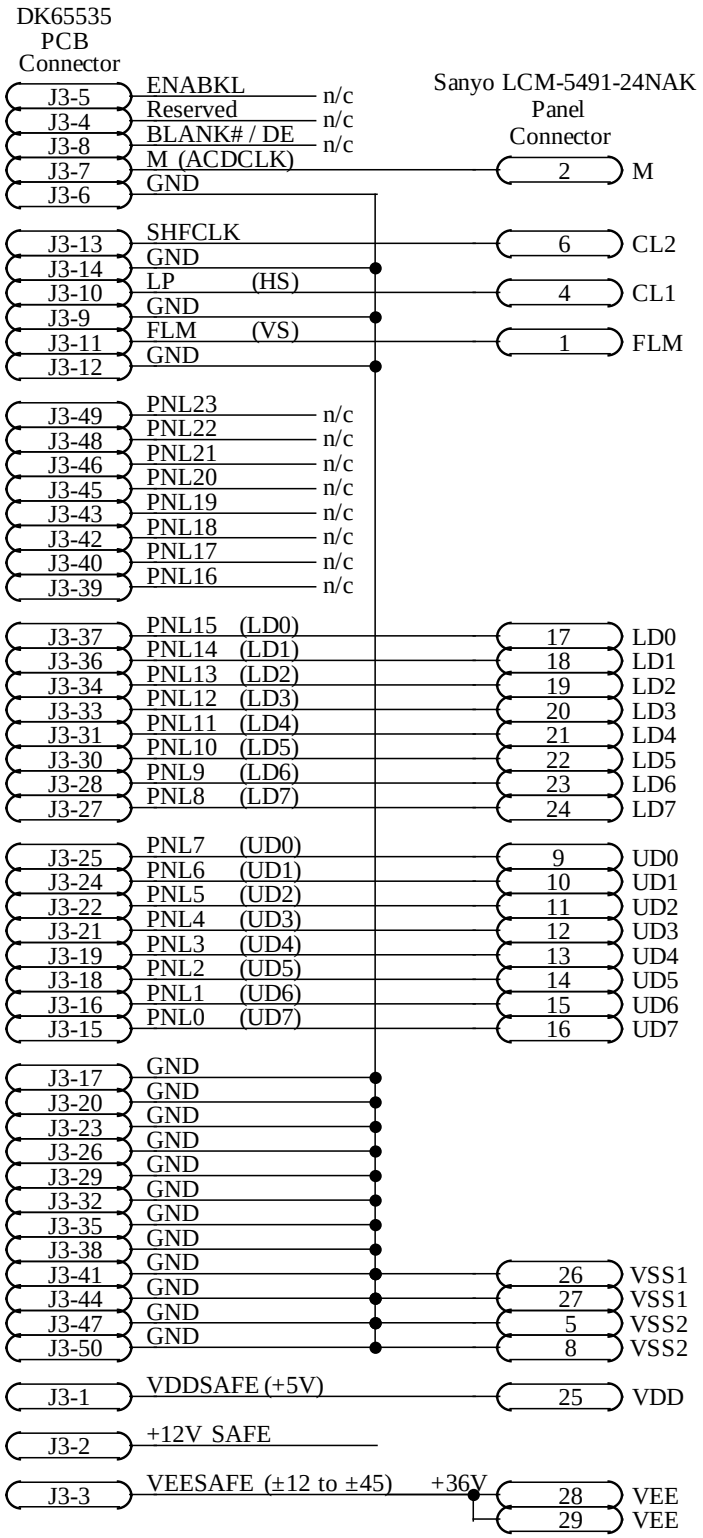
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Sanyo LCM-6494-24NTK (640x480 Monochrome LCD DD Panel)



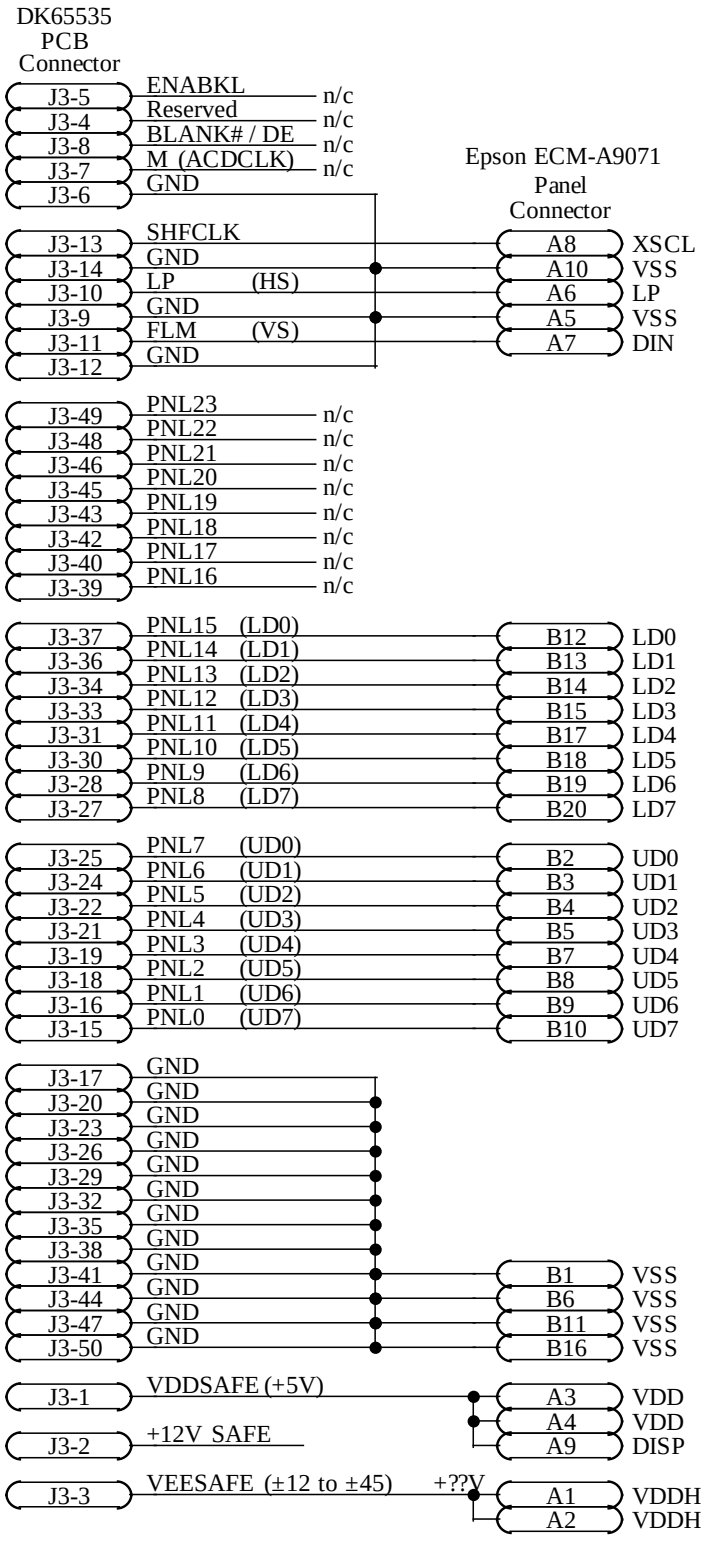
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Hitachi LMG5364XUFC (640x480 Monochrome LCD DD Panel)



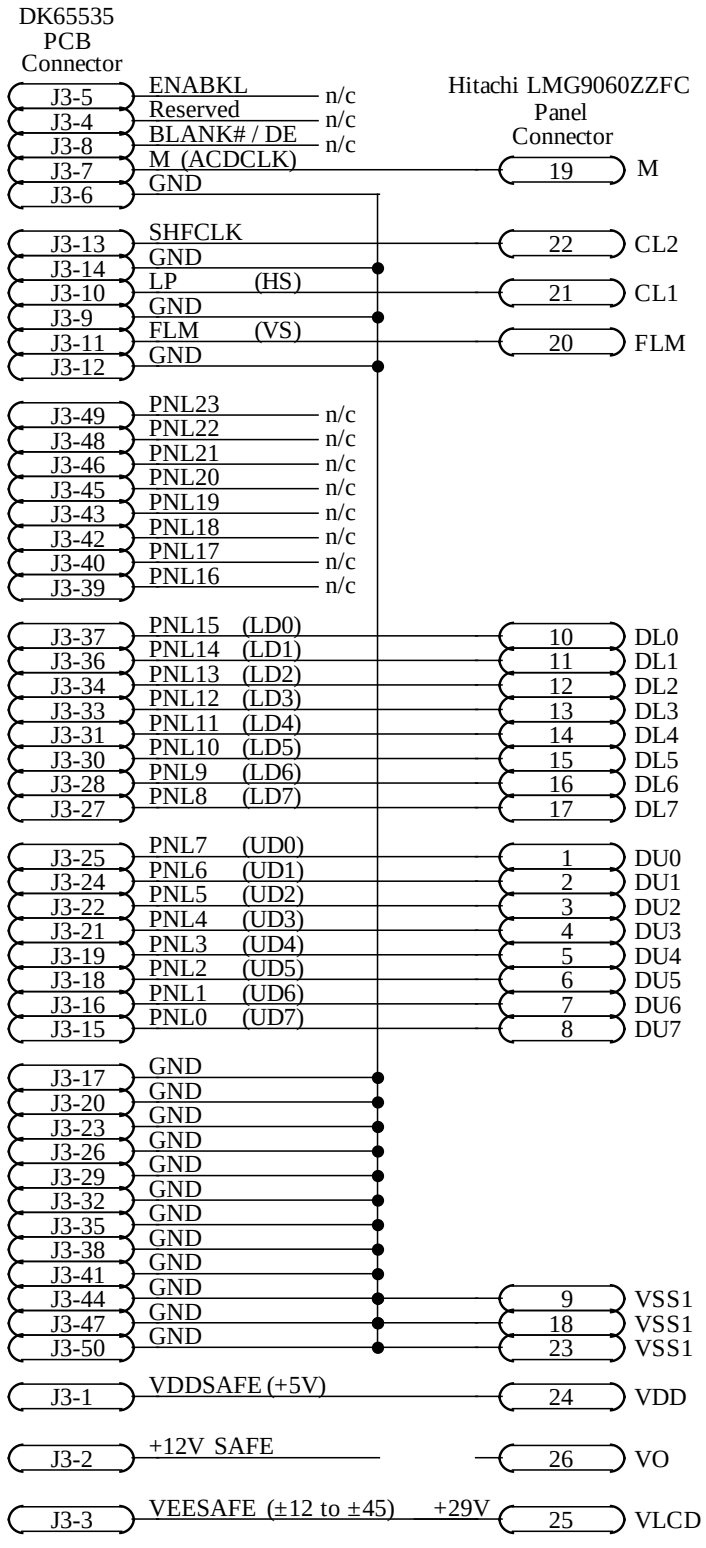
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	7Fh	(1024 / 8) – 1
Panel Height	XR65/68	2FFh	768 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Sanyo LCM-5491-24NAK (1024x768 LCD DD Panel)



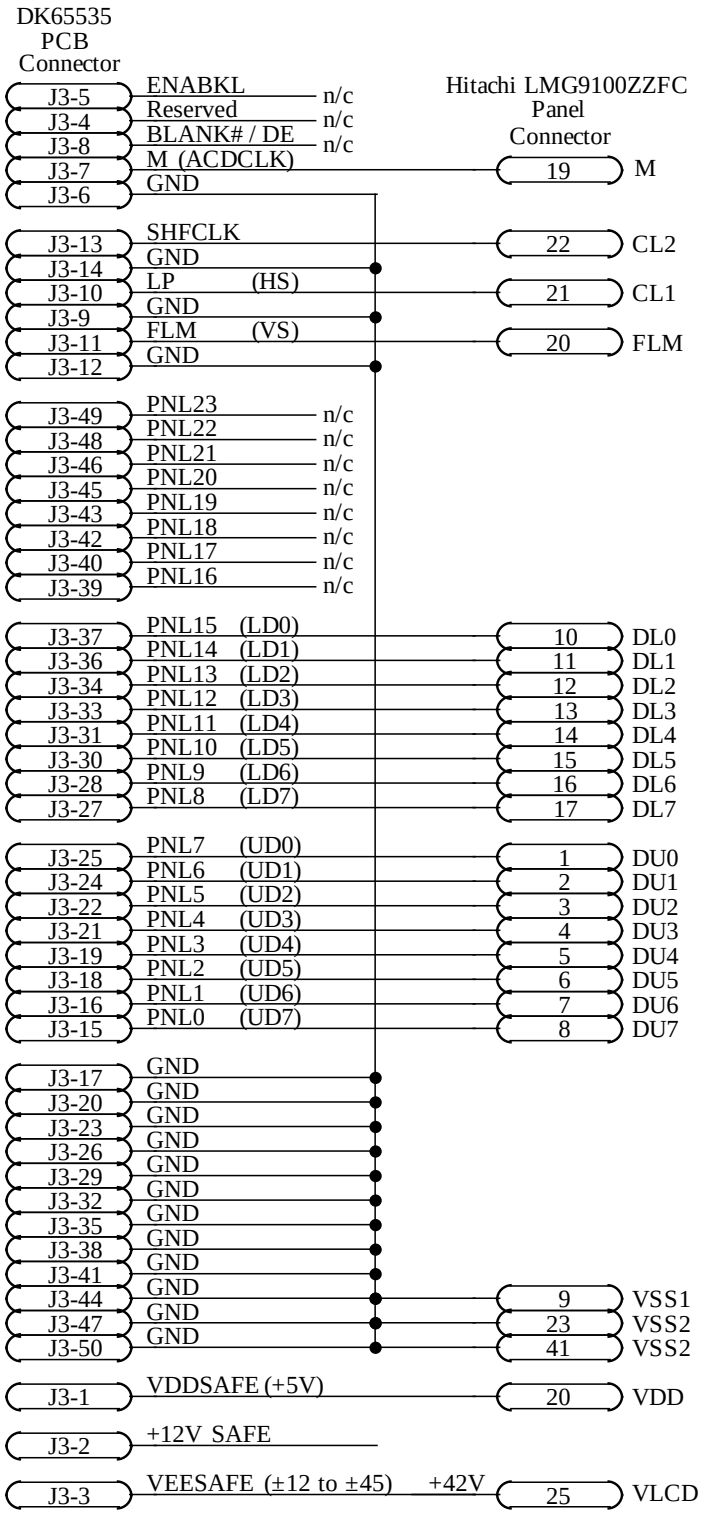
Programming	**Recommendations/Requirements**		
Parameter	Register	Value	Comment
Panel Width	XR1C	7Fh	(1024 / 8) – 1
Panel Height	XR65/68	2FFh	768 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Epson A9071 (1024x768 LCD DD Panel)



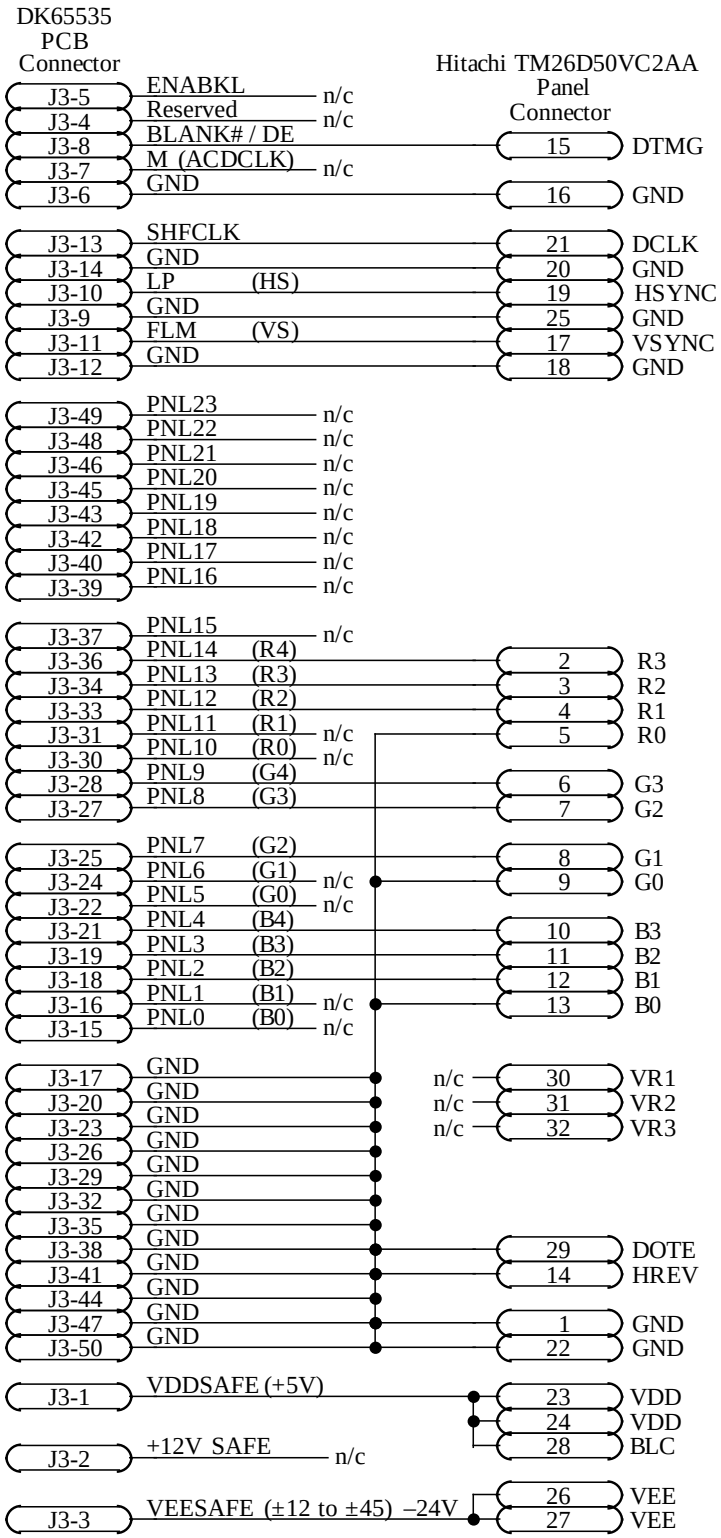
Programming	**Recommendations/Requirements**		
Parameter	Register	Value	Comment
Panel Width	XR1C	7Fh	(1024 / 8) – 1
Panel Height	XR65/68	2FFh	768 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Hitachi LMG9060ZZFC (1024x768 LCD DD Panel)



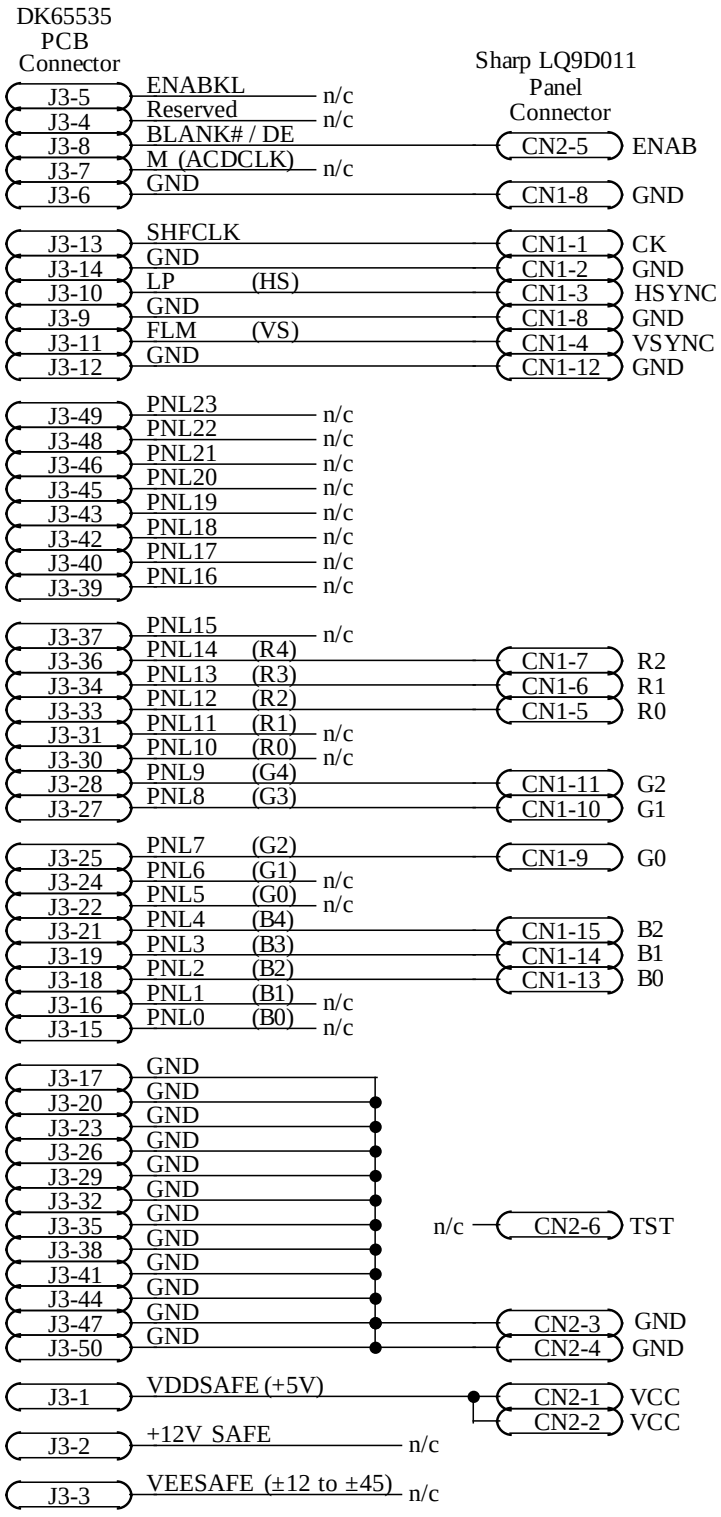
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	7Fh	(1024 / 8) – 1
Panel Height	XR65/68	2FFh	768 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Hitachi LMG9100ZZFC (1280x1024 LCD DD Panel)



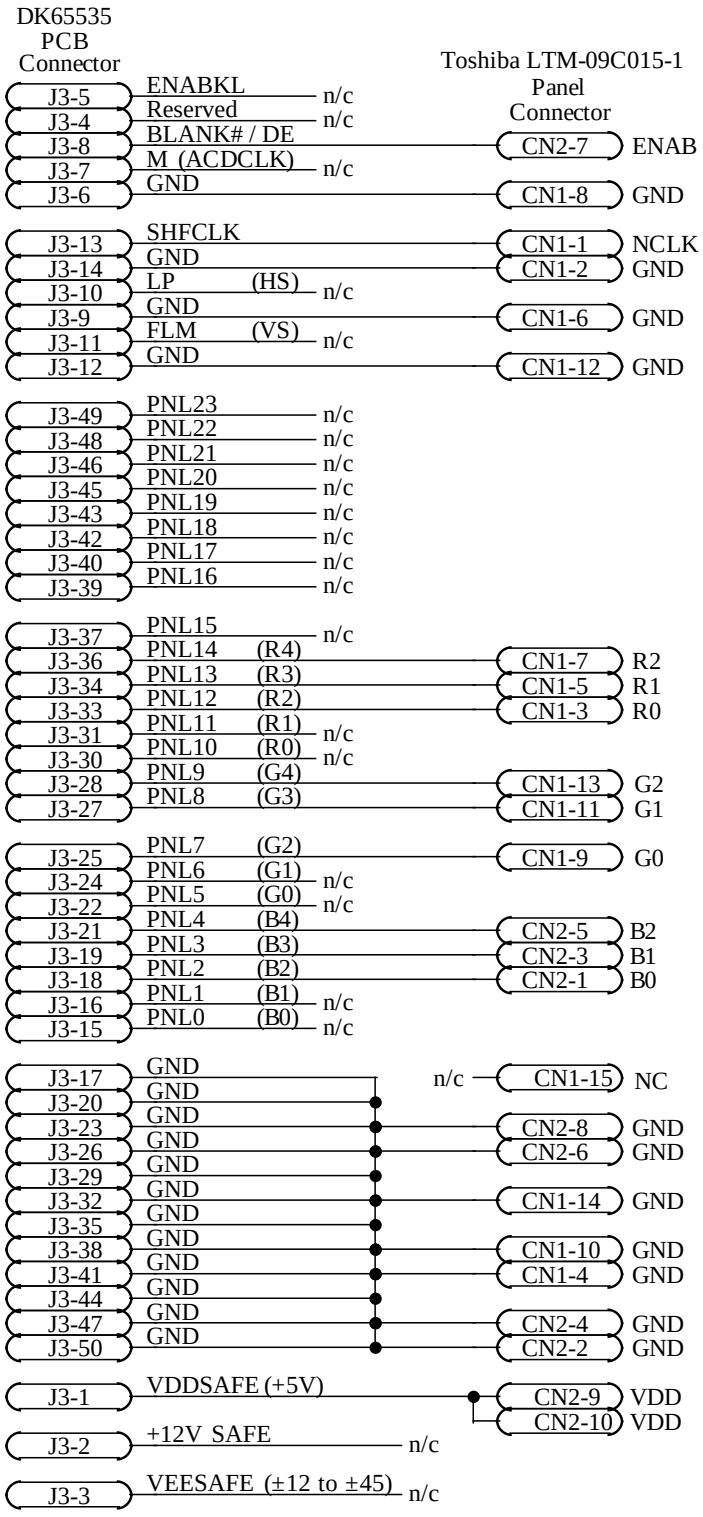
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]	00	
Clock Divide (CD)	XR50[6-4]	000	
Shiftclk Div (SD)	XR51[3]	0	
Gray/Color Levels	XR4F[2-0]	100	
TFT Data Width	XR50[7]	0	n/a
STN Pixel Packing	XR53[5-4]	00	n/a
Frame Accel Ena	XR6F[1]	0	Disabled
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]	0	
LP Delay Disable	XR2F[6]	0	
LP Delay (Hcomp disa)	XR2F/2D	04Fh	
LP Delay (Hcomp ena)	XR2F/2E	04Fh	
LP Pulse Width	XR2F[3-0]	0Fh	
LP Polarity	XR54[6]	1	
LP Blank	XR4F[7]	0	
LP Active during V	XR51[7]	1	
FLM Delay Disable	XR2F[7]	0	
FLM Delay	XR2C	04h	
FLM Polarity	XR54[7]	1	
Blank#/DE Polarity	XR54[0]	1	
Blank#/DE H-Only	XR54[1]	1	
Blank#/DE CRT/FP	XR51[2]	1	
Alt Hsync Start (CR04)	XR19	56h	
Alt Hsync End (CR05)	XR1A	13h	
Alt H Total (CR00)	XR1B	5Fh	
Alt V Total (CR06)	XR65/64	201h	
Alt Vsync Start (CR10)	XR65/66	1DFh	
Alt Vsync End (CR11)	XR67[3-0]	5h	
Alt Hsync Polarity	XR55[6]	1	
Alt Vsync Polarity	XR55[7]	1	
Display Quality Recommendations			
FRC	XR50[1-0]	10	
FRC Option 1	XR53[2]	1	Set to 1
FRC Option 2	XR53[3]	1	Set to 1
FRC Option 3	XR53[6]	0	
FRC Polynomial	XR6E[7-0]		n/a
Dither	XR50[3-2]	01	
M Phase Change	XR5E[7]		n/a
M Phase Change Count	XR5E[6-0]		n/a
Compensation Typical Settings			
H Compensation	XR55[0]	1	
V Compensation	XR57[0]	1	
Fast Centering Disable	XR57[7]	0	
H AutoCentering	XR55[1]	0	
V AutoCentering	XR57[1]	0	
H Centering	XR56	00h	
V Centering	XR59/58	000h	
H Text Compression	XR55[2]	1	
H AutoDoubling	XR55[5]	1	
V Text Stretching	XR57[2]	1	
V Text Stretch Mode	XR57[4-3]	11	
V Stretching	XR57[5]	0	
V Stretching Mode	XR57[6]	0	
V Line Insertion Height	XR59[3-0]	0Fh	
V H/W Line Replication	XR59[7]	0	
V Line Repl Height	XR5A[3-0]	0	

65535 Interface - Hitachi TM26D50VC2AA (640x480 512-Color TFT LCD Panel)



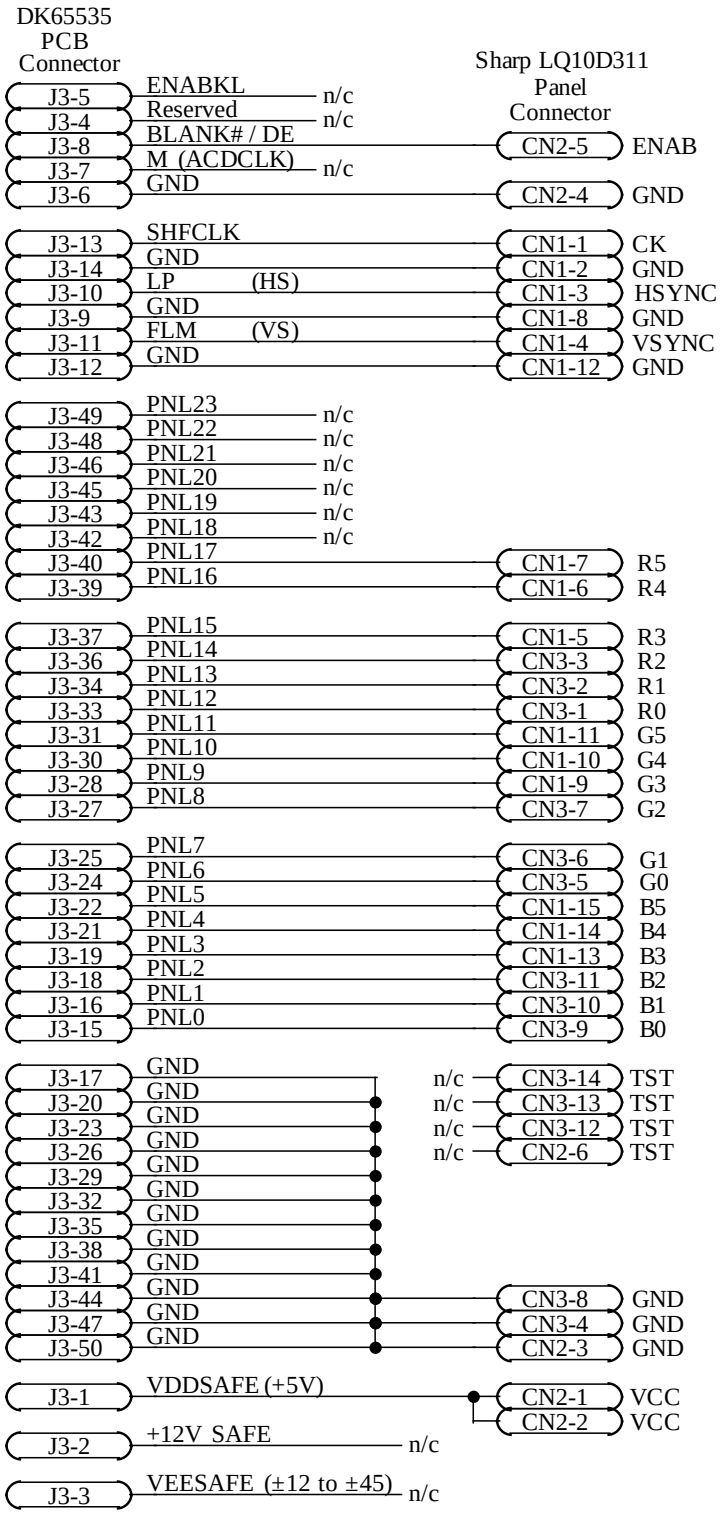
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]	00	
Clock Divide (CD)	XR50[6-4]	000	
Shiftclk Div (SD)	XR51[3]	0	
Gray/Color Levels	XR4F[2-0]	100	
TFT Data Width	XR50[7]	0	n/a
STN Pixel Packing	XR53[5-4]	00	n/a
Frame Accel Ena	XR6F[1]	0	Disabled
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]	0	
LP Delay Disable	XR2F[6]	0	
LP Delay (Hcomp disa)	XR2F/2D	04Fh	
LP Delay (Hcomp ena)	XR2F/2E	04Fh	
LP Pulse Width	XR2F[3-0]	0Fh	
LP Polarity	XR54[6]	1	
LP Blank	XR4F[7]	0	
LP Active during V	XR51[7]	1	
FLM Delay Disable	XR2F[7]	0	
FLM Delay	XR2C	04h	
FLM Polarity	XR54[7]	1	
Blank#/DE Polarity	XR54[0]	1	
Blank#/DE H-Only	XR54[1]	1	
Blank#/DE CRT/FP	XR51[2]	1	
Alt Hsync Start (CR04)	XR19	56h	
Alt Hsync End (CR05)	XR1A	13h	
Alt H Total (CR00)	XR1B	5Fh	
Alt V Total (CR06)	XR65/64	201h	
Alt Vsync Start (CR10)	XR65/66	1DFh	
Alt Vsync End (CR11)	XR67[3-0]	5h	
Alt Hsync Polarity	XR55[6]	1	
Alt Vsync Polarity	XR55[7]	1	
Display Quality Recommendations			
FRC	XR50[1-0]	10	
FRC Option 1	XR53[2]	1	Set to 1
FRC Option 2	XR53[3]	1	Set to 1
FRC Option 3	XR53[6]	0	
FRC Polynomial	XR6E[7-0]		n/a
Dither	XR50[3-2]	01	
M Phase Change	XR5E[7]		n/a
M Phase Change Count	XR5E[6-0]		n/a
Compensation Typical Settings			
H Compensation	XR55[0]	1	
V Compensation	XR57[0]	1	
Fast Centering Disable	XR57[7]	0	
H AutoCentering	XR55[1]	0	
V AutoCentering	XR57[1]	0	
H Centering	XR56	00h	
V Centering	XR59/58	000h	
H Text Compression	XR55[2]	1	
H AutoDoubling	XR55[5]	1	
V Text Stretching	XR57[2]	1	
V Text Stretch Mode	XR57[4-3]	11	
V Stretching	XR57[5]	0	
V Stretching Mode	XR57[6]	0	
V Line Insertion Height	XR59[3-0]	0Fh	
V H/W Line Replication	XR59[7]	0	
V Line Repl Height	XR5A[3-0]	0	

65535 Interface - Sharp LQ9D011 (640x480 512-Color TFT LCD Panel)



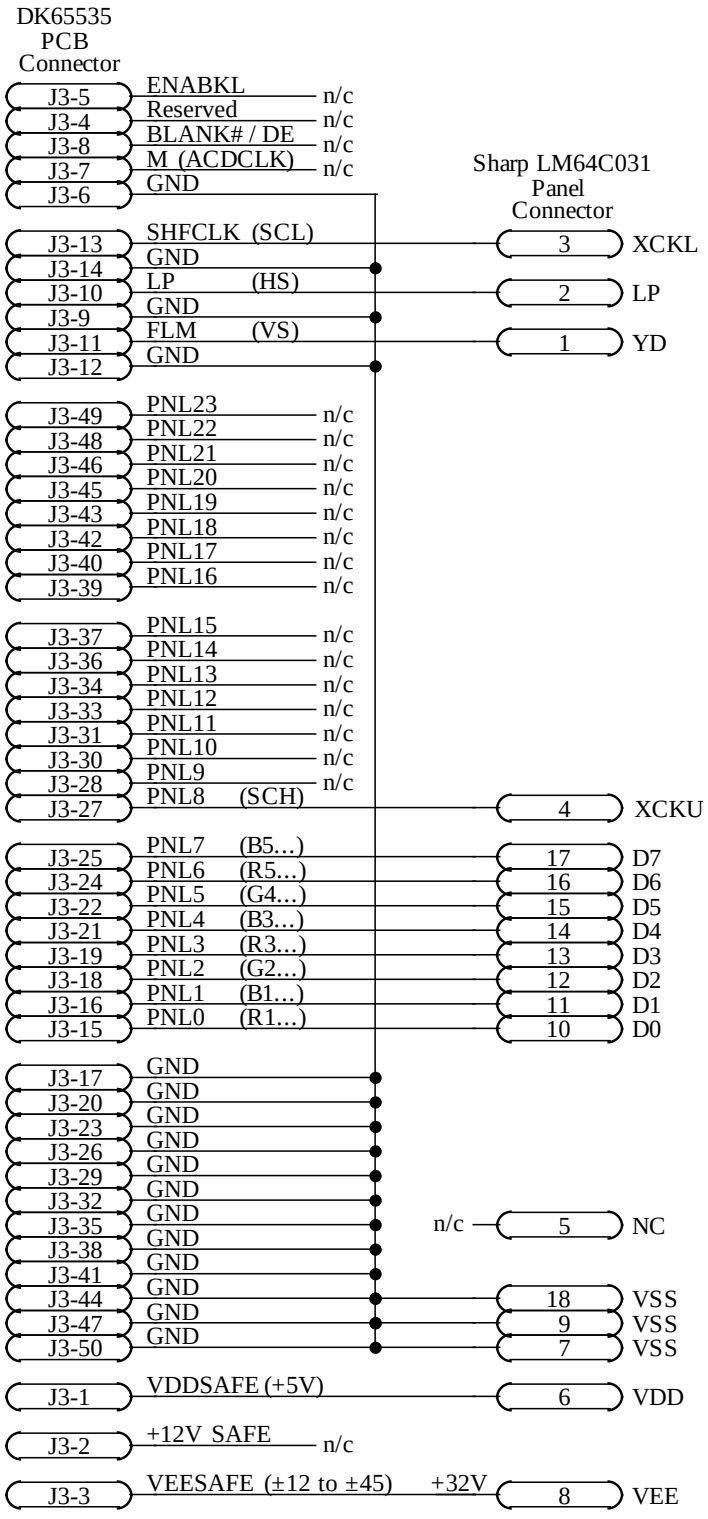
Programming	**Recommendations/Requirements**		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]	00	
Clock Divide (CD)	XR50[6-4]	000	
Shiftclk Div (SD)	XR51[3]	0	
Gray/Color Levels	XR4F[2-0]	100	
TFT Data Width	XR50[7]	0	n/a
STN Pixel Packing	XR53[5-4]	00	n/a
Frame Accel Ena	XR6F[1]	0	Disabled
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]	0	
LP Delay Disable	XR2F[6]	0	
LP Delay (Hcomp disa)	XR2F/2D	04Fh	
LP Delay (Hcomp ena)	XR2F/2E	04Fh	
LP Pulse Width	XR2F[3-0]	0Fh	
LP Polarity	XR54[6]	1	
LP Blank	XR4F[7]	0	
LP Active during V	XR51[7]	1	
FLM Delay Disable	XR2F[7]	0	
FLM Delay	XR2C	04h	
FLM Polarity	XR54[7]	1	
Blank#/DE Polarity	XR54[0]	1	
Blank#/DE H-Only	XR54[1]	0	Reqd for this panel
Blank#/DE CRT/FP	XR51[2]	1	
Alt Hsync Start (CR04)	XR19	56h	
Alt Hsync End (CR05)	XR1A	13h	
Alt H Total (CR00)	XR1B	5Fh	
Alt V Total (CR06)	XR65/64	201h	
Alt Vsync Start (CR10)	XR65/66	1DFh	
Alt Vsync End (CR11)	XR67[3-0]	5h	
Alt Hsync Polarity	XR55[6]	1	
Alt Vsync Polarity	XR55[7]	1	
Display Quality Recommendations			
FRC	XR50[1-0]	10	
FRC Option 1	XR53[2]	1	Set to 1
FRC Option 2	XR53[3]	1	Set to 1
FRC Option 3	XR53[6]	0	
FRC Polynomial	XR6E[7-0]		n/a
Dither	XR50[3-2]	01	
M Phase Change	XR5E[7]		n/a
M Phase Change Count	XR5E[6-0]		n/a
Compensation Typical Settings			
H Compensation	XR55[0]	1	
V Compensation	XR57[0]	1	
Fast Centering Disable	XR57[7]	0	
H AutoCentering	XR55[1]	0	
V AutoCentering	XR57[1]	0	
H Centering	XR56	00h	
V Centering	XR59/58	000h	
H Text Compression	XR55[2]	1	
H AutoDoubling	XR55[5]	1	
V Text Stretching	XR57[2]	1	
V Text Stretch Mode	XR57[4-3]	11	
V Stretching	XR57[5]	0	
V Stretching Mode	XR57[6]	0	
V Line Insertion Height	XR59[3-0]	0Fh	
V H/W Line Replication	XR59[7]	0	
V Line Repl Height	XR5A[3-0]	0	

65535 Interface - Toshiba LTM-09C015-1 (640x480 512-Color TFT LCD Panel)



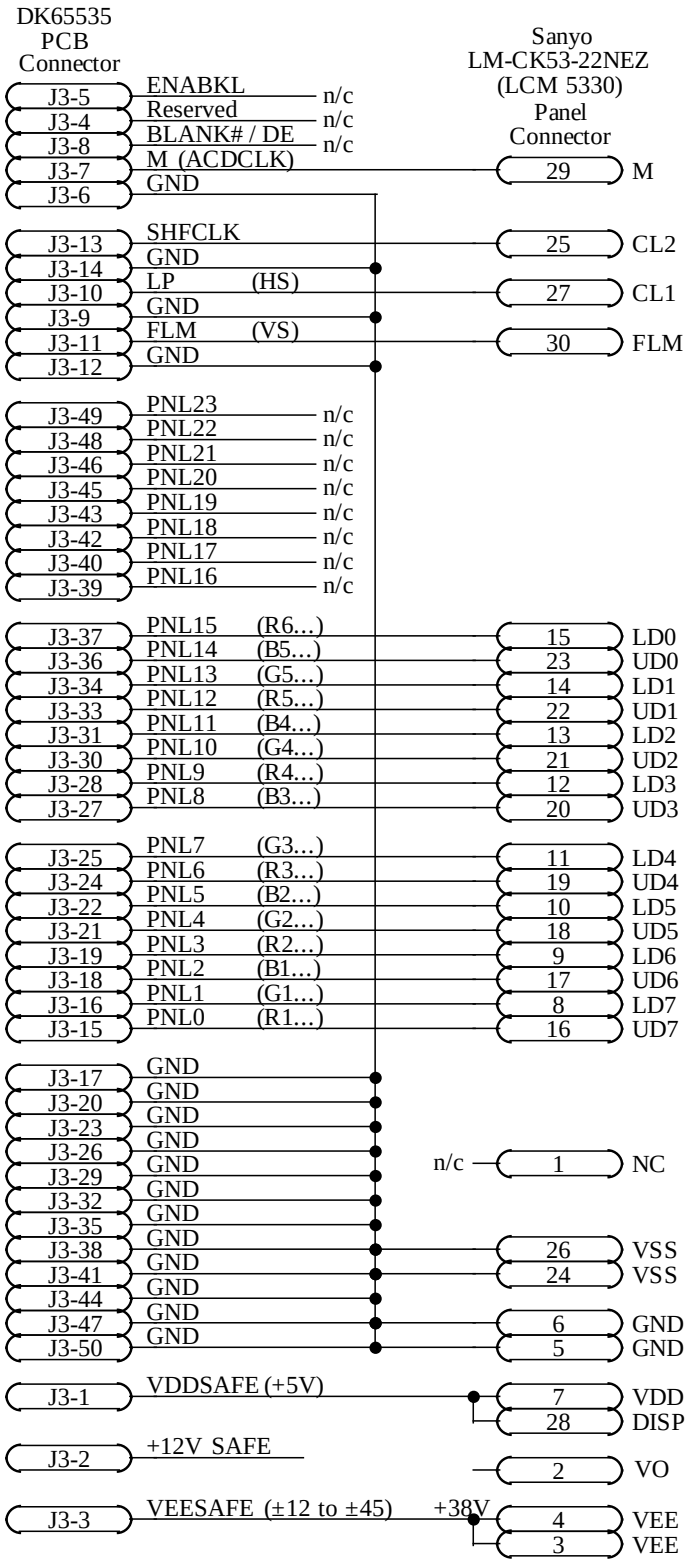
Programming	**Recommendations/Requirements**		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Sharp LQ10D311 (640x480 256K-Color TFT LCD Panel)



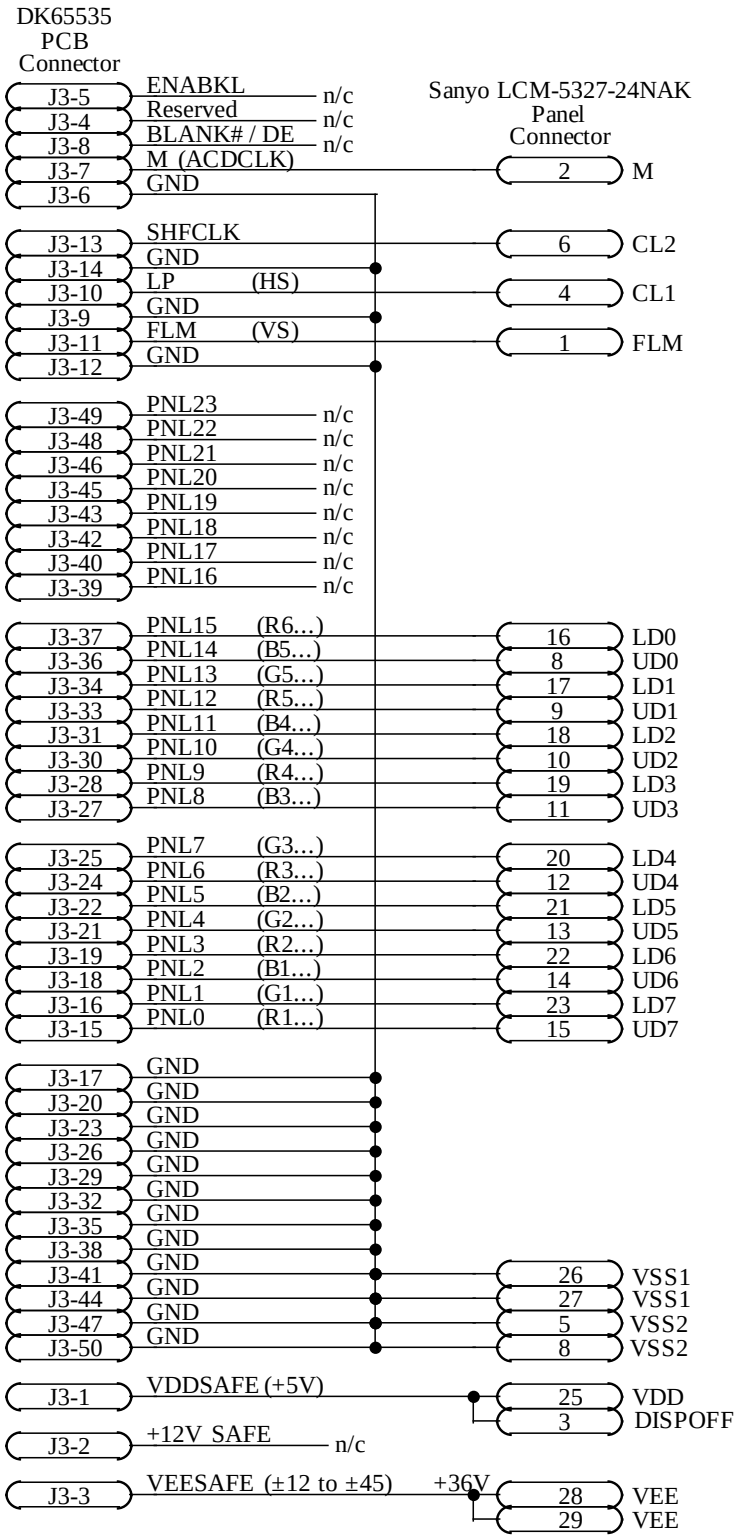
Programming	**Recommendations/Requirements**		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Sharp LM64C031 (640x480 Color STN LCD Panel)



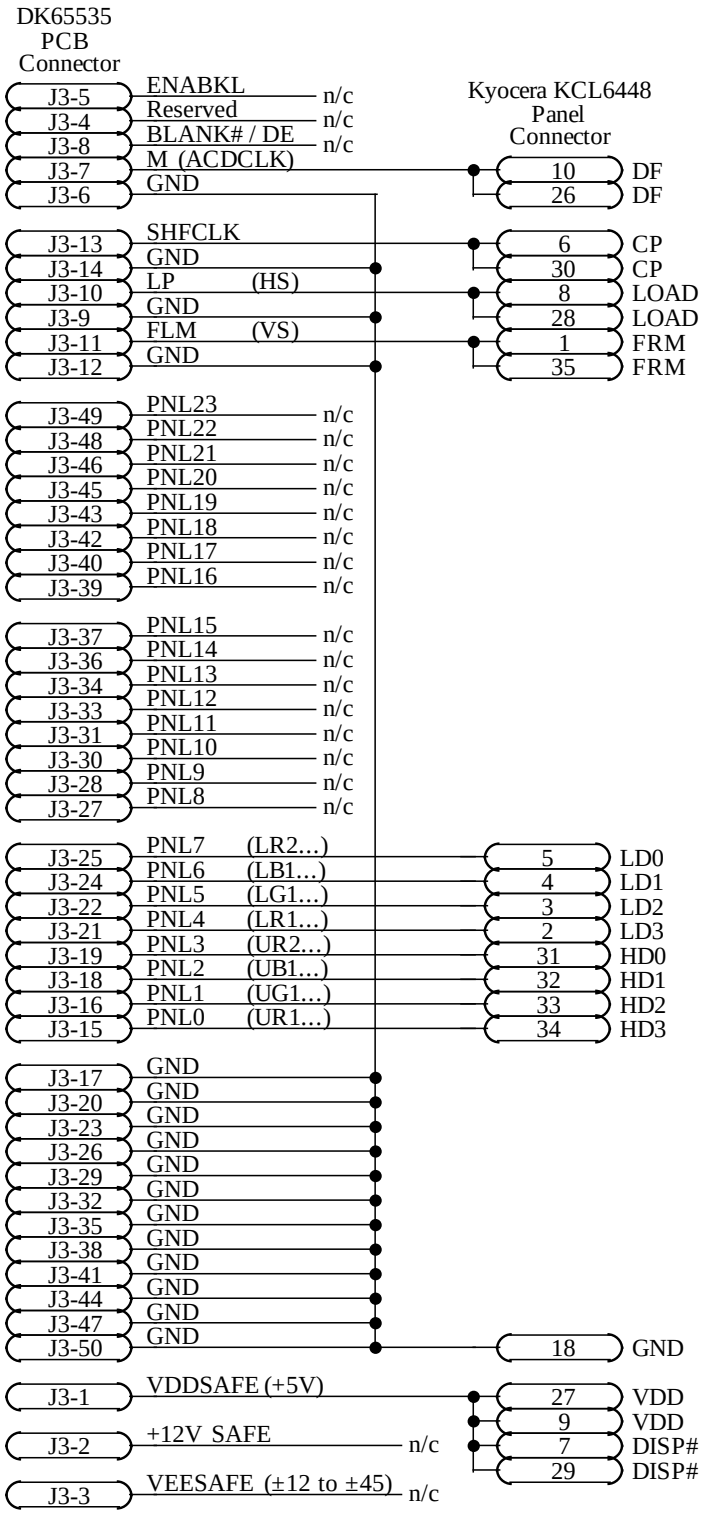
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Sanyo LM-CK53-22NEZ (LCM 5330) (640x480 Color STN LCD Panel)



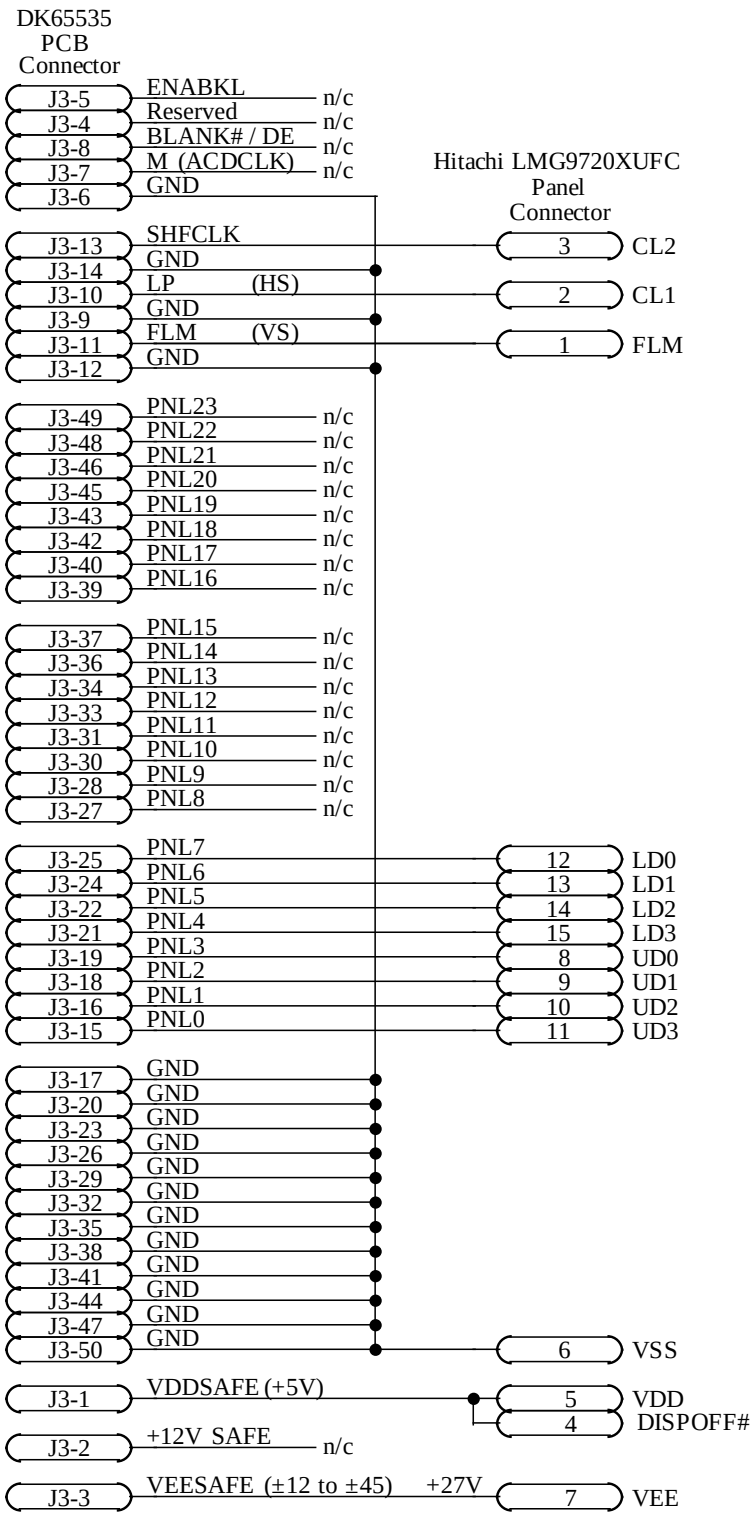
Programming	**Recommendations/Requirements**		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Sanyo LCM5327-24NAK (640x480 Color STN LCD Panel)



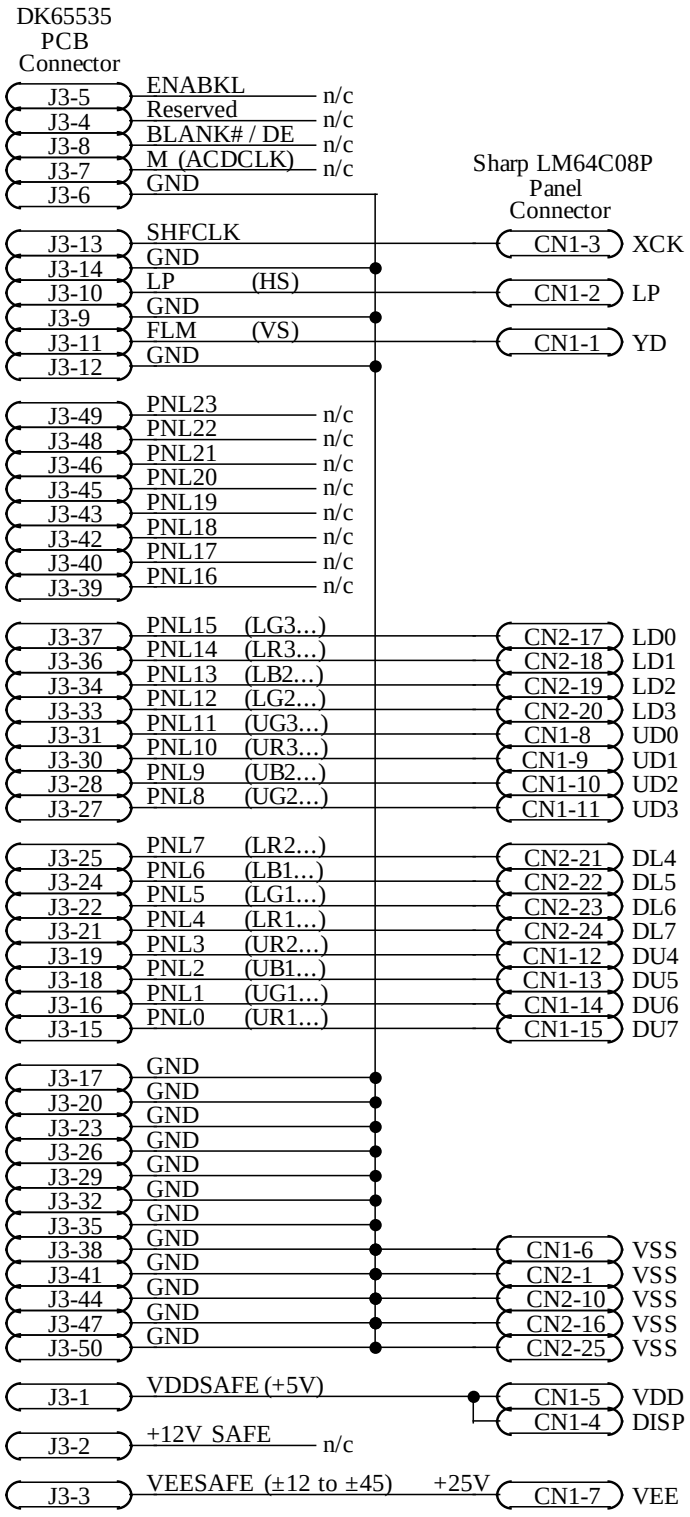
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Kyocera KCL6448 (640x480 Color STN-DD LCD Panel)



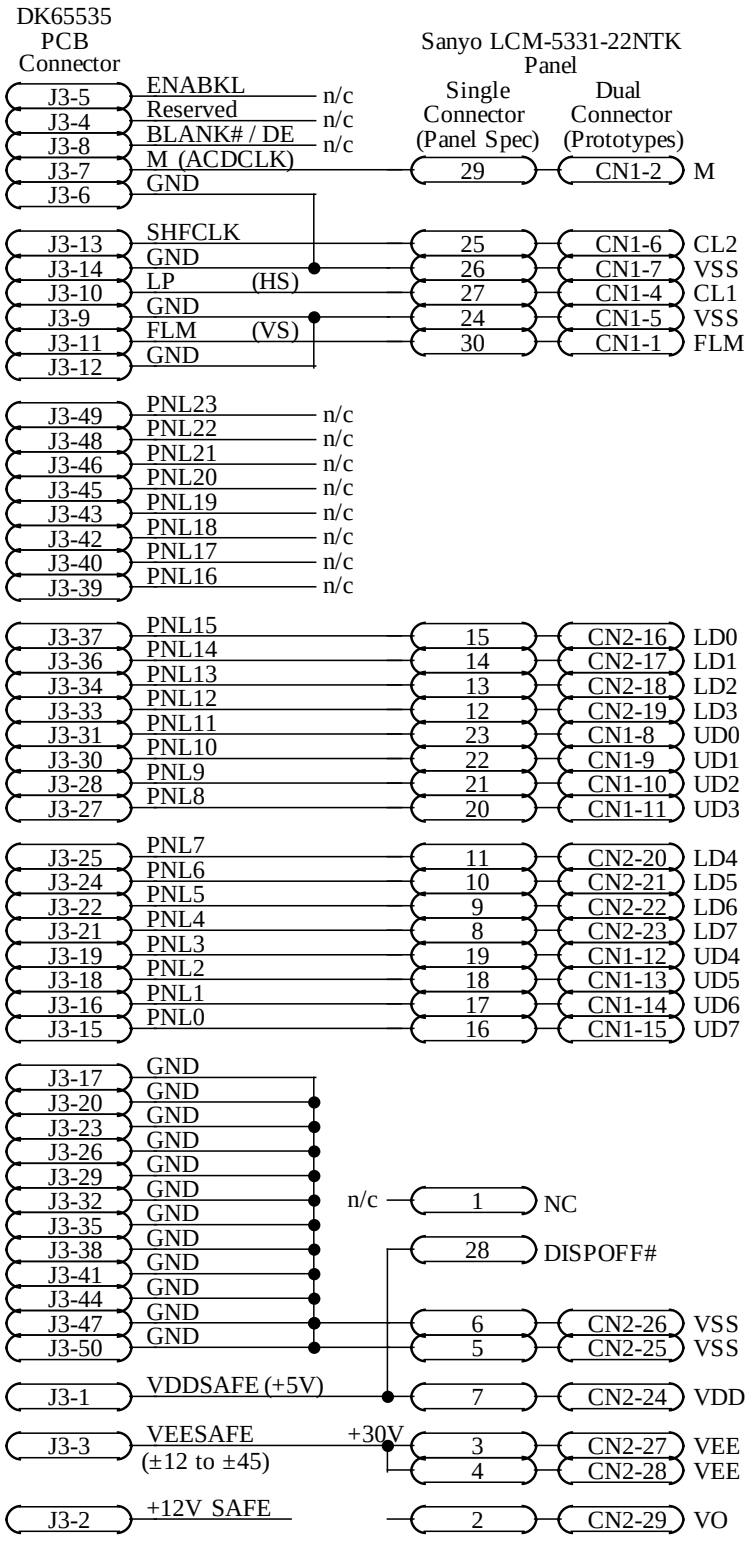
Programming	**Recommendations/Requirements**		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Hitachi LMG9720XUFC (640x480 Color STN-DD LCD Panel)



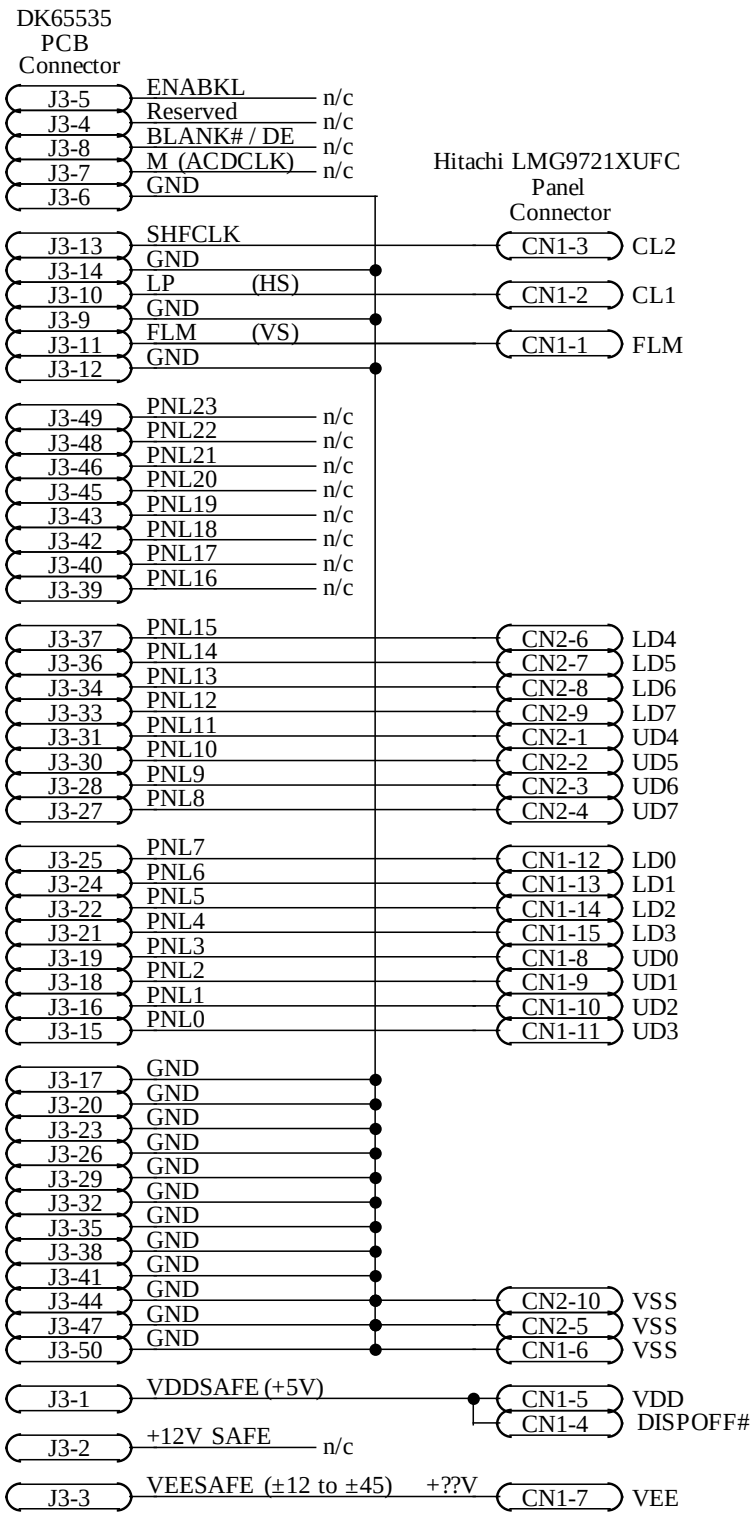
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]	0BAh	** Important **
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Sharp LM64C08P (640x480 Color STN-DD LCD Panel)



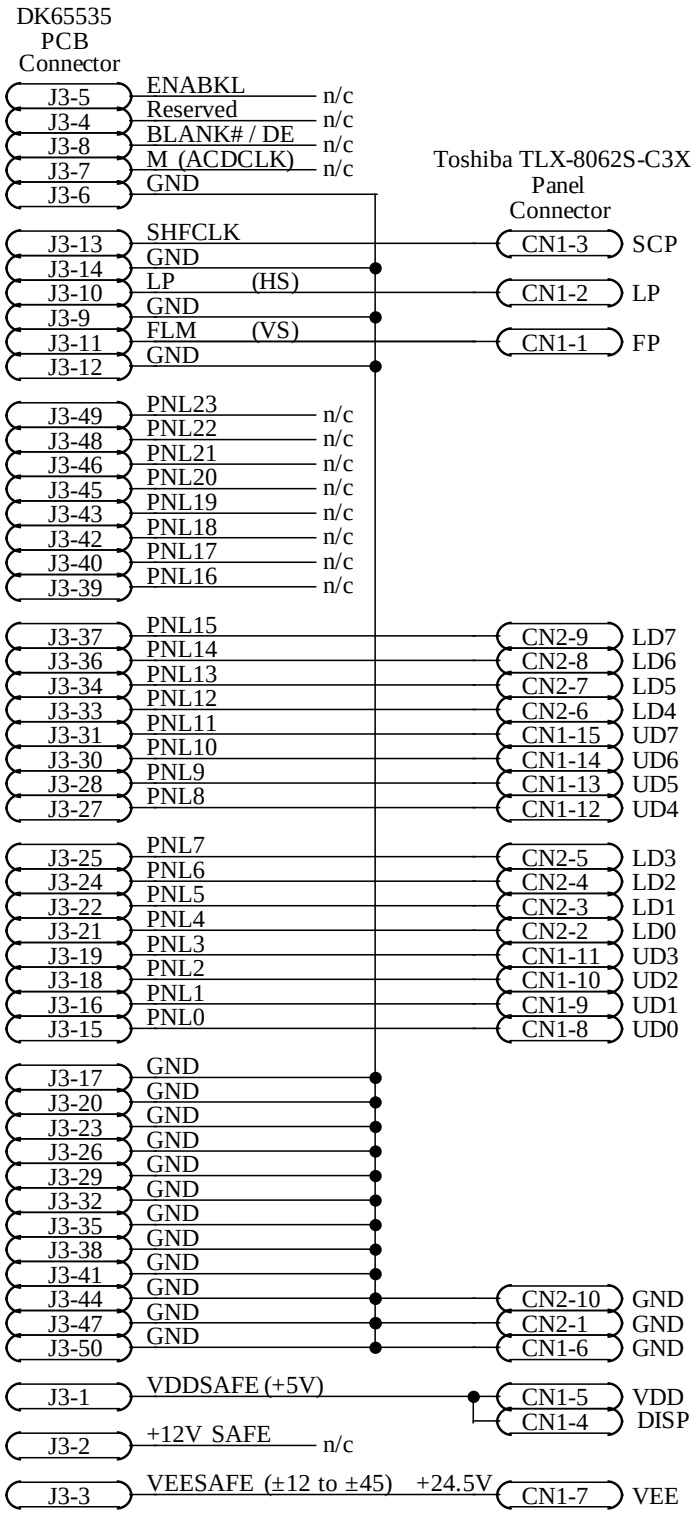
Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Sanyo LCM-5331-22NTK (640x480 Color STN-DD LCD Panel)



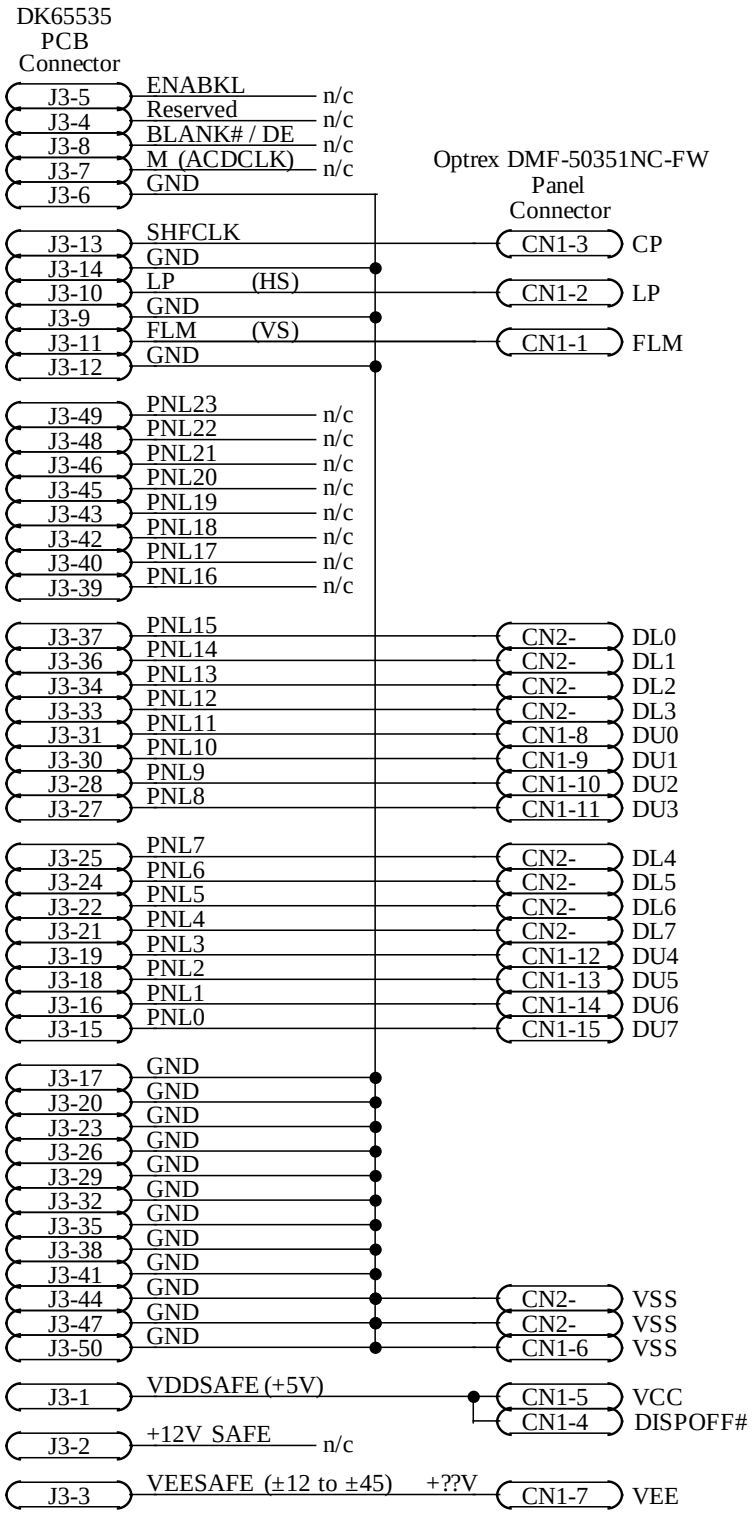
Programming	**Recommendations/Requirements**		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Hitachi LMG9721XUFC (640x480 Color STN-DD LCD Panel)



Programming	**Recommendations/Requirements**		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Toshiba TLX-8062S-C3X (640x480 Color STN-DD LCD Panel)



Programming	Recommendations/Requirements		
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (Hcomp disa)	XR2F/2D		
LP Delay (Hcomp ena)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

65535 Interface - Optrex DMF-50351NC-FW (640x480 Color STN-DD LCD Panel)

Electrical Specifications

65535 ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	1	W
V_{CC}	Supply Voltage	–0.5	–	7.0	V
V_I	Input Voltage	–0.5	–	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	–	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	–	85	°C
T_{STG}	Storage Temperature	–40	–	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

65535 NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage **(5V ± 10%)**	4.5	5	5.5	V
V_{CC}	Supply Voltage **(3.3V ± 10%)**	3	3.3	3.6	V
T_A	Ambient Temperature	0	–	70	°C
T_C	Case Temperature	0	–	100	°C

65535 DAC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
V_O	Output Voltage	$I_O \leq 10$ mA	1.5	–	–	V
I_O	Output Current	$V_O \leq 1V$ @ 37.5Ω Load	21	–	–	mA
	Full Scale Error		–	–	±5	%
	DAC to DAC Correlation		–	1.27	–	%
	DAC Linearity		±2	–	–	LSB
	Full Scale Settling Time		–	–	28	nS
	Rise Time	10% to 90%	–	–	6	nS
	Glitch Energy		–	–	200	pVsec
	Comparator Sensitivity		–	50	–	mV

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz.
Electrical specifications contained herein are preliminary and subject to change without notice.

65535 DC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
I_{CCDE}	Power Supply Current	0°C, **5.5V**, 65 MHz MCLK, DAC Enabled	–	120	200	mA
I_{CCDO}	Power Supply Current	0°C, **5.5V** , 65 MHz MCLK, DAC Disabled	–	70	150	mA
I_{CCDO}	Power Supply Current	0°C, **3.3V** , 56 MHz MCLK, DAC Disabled	–	50	130	mA
I_{CCS}	Power Supply Current	0°C, **5.5V** , Standby - Slow Refresh	–	–	1	mA
I_{IL}	Input Leakage Current		–100	–	+100	uA
I_{OZ}	Output Leakage Current	High Impedance	–100	–	+100	uA
V_{IL}	Input Low Voltage	All input pins	–0.5	–	0.8	V
V_{IH}	Input High Voltage	All input pins except clocks	2.0	–	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	Under max load per table below **(5V)**	–	–	0.5	V
V_{OL}	Output Low Voltage	Under max load per table below **(3.3V)**	–	–	0.5	V
V_{OH}	Output High Voltage	Under max load per table below **(5V)**	V_{CC}–0.5	–	–	V
V_{OH}	Output High Voltage	Under max load per table below **(3.3V)**	2.4	–	–	V

65535 DC DRIVE CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Output Pins	DC Test Conditions	Min	Units
I_{OL}	Output Low Drive	HSYNC, VSYNC, BS16#, LDEV#, LRDY#	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	12	mA
		FLM, LP, M	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	8	mA
		OEL#, 0EH#, ENAVEE, ENAVDD	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	8	mA
		P0-17, PCLK, SHFCLK, D0-15	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	8	mA
		RASA#, CASAH#, CASAL#, WEA#, MBD0-15	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	4	mA
		RASB#, CASBH#, CASBL#, WEB#, AA9-0	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	4	mA
		All Other Outputs	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	2	mA
I_{OH}	Output High Drive	HSYNC, VSYNC, BS16#, LDEV#, LRDY#	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	12	mA
		FLM, LP, M	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	8	mA
		OEL#, OEH#, ENAVEE, ENAVDD	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	8	mA
		P0-17, PCLK, SHFCLK, D0-15	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	8	mA
		RASA#, CASAH#, CASAL#, WEA#, MBD0-15	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		RASB#, CASBH#, CASBL#, WEB#, AA9-0	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		All Other Outputs	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	2	mA

65535 AC TEST CONDITIONS

(Under Normal Operating Conditions Unless Noted Otherwise)

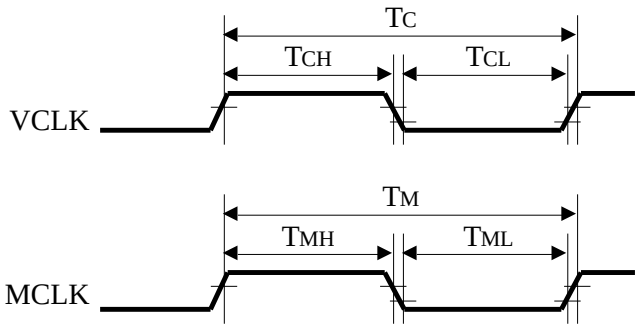
Output Pins	Output Low Voltage	Output High Voltage	Capacitive Load
D0-15, RDY, IRQ, ZWS#, BS16#, HSYNC, VSYNC	V_{OL}	2.4V	85pF
P0-7, PCLK, SHFCLK, ENAVEE#, ENAVDD#, FLM, LP, M	V_{OL}	2.4V	85pF
All Other 4mA Output Pads	V_{OL}	2.4V	85pF
All Other 2mA Output Pads	V_{OL}	2.4V	40pF

Note: STNDBY# power measurement was taken using Slow Refresh DRAMs with a 32 KHz clock input.

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65535 AC TIMING CHRACTERISTICS - CLOCK GENERATOR

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_C	VCLK Period, **(5V)**	68 MHz	14.7	–	–	nS
T_C	VCLK Period, **(3.3V)**	56 MHz	17.6	–	–	nS
T_{CH}	VCLK High Time		$0.45T_C$	–	$0.55T_C$	nS
T_{CL}	VCLK Low Time		$0.45T_C$	–	$0.55T_C$	nS
T_M	MCLK Period **(5V)**	68 MHz	14.7	–	–	nS
T_M	MCLK Period **(3.3V)**	56 MHz	17.6	–	–	nS
T_{MH}	MCLK High Time		$0.45T_M$	–	$0.55T_M$	nS
T_{ML}	MCLK Low Time		$0.45T_M$	–	$0.55T_M$	nS
T_{RF}	Clock Rise / Fall		–	–	5	nS
–	MCLK Frequency for 100 ns DRAMs **(5V)**		–	50.350	–	MHz
–	MCLK Frequency for 80 ns DRAMs **(5V)**		–	56.644	–	MHz
–	MCLK Frequency for 70 ns DRAMs **(5V)**		–	65	–	MHz



Clock Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

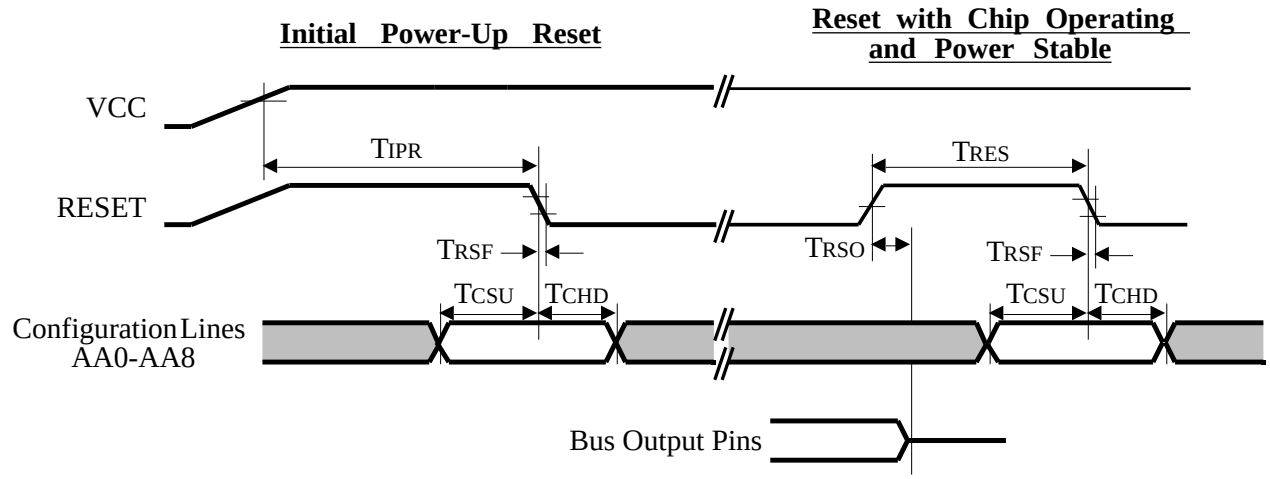
65535 AC TIMING CHARACTERISTICS - RESET

Symbol	Parameter	Notes	Min	Max	Units
T_{IPR}	Reset Active Time from Power Stable	See Note 1	5	–	**mS**
T_{RES}	Reset Active Time with Power Stable	See Note 2	2	–	**mS**
T_{RSF}	Reset Fall Time	Reset rise time is non-critical	–	20	nS
T_{RSO}	Reset Active to Output Float Delay		–	40	nS
T_{CSU}	Configuration Setup Time	See Note 3	20	–	nS
T_{CHD}	Configuration Hold Time		5	–	nS

Note 1: This parameter includes time for internal voltage stabilization of all sections of the chip, startup and stabilization of the internal clock synthesizer, and setting of all internal logic to a known state.

Note 2: This parameter includes time for the internal clock synthesizer to reset to its default frequency and time to set all internal logic to a known state. It assumes power is stable and the internal clock synthesizer is already operating at some stable frequency.

Note 3: Setup time to latch the state of the configuration bits reliably into XR01 and XR6C is specified by this parameter. Changes in some configuration bits may take longer to stabilize inside the chip (such as internal clock synthesizer-related bits 4 and 5). It is therefore recommended that configuration bit setup time be TRES (2mS) to insure that the chip is in a completely stable state when RESET goes inactive.

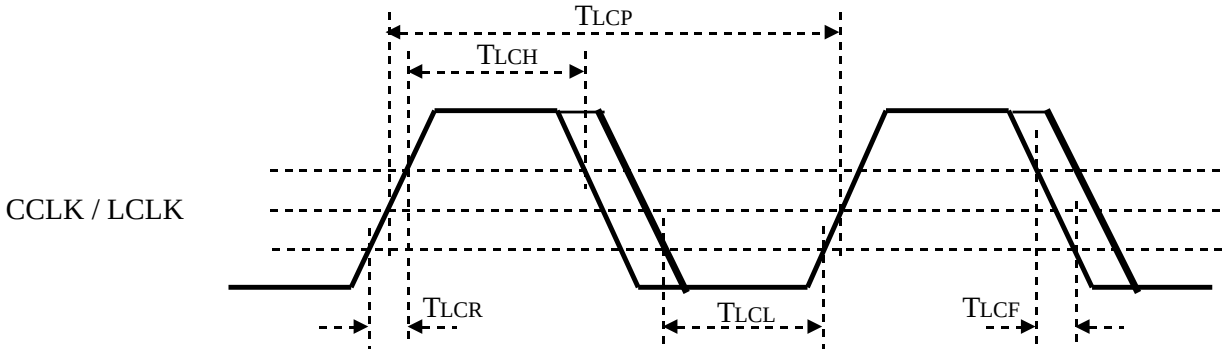


Reset Timing

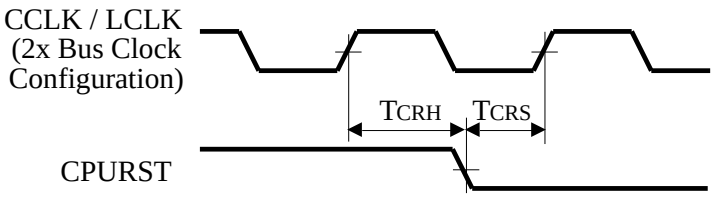
Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65535 AC TIMING CHARACTERISTICS - LOCAL BUS CLOCK (33 MHz)

Symbol	Parameter	Notes	C_L Max	Min	Max	Units
T_{LCP}	Local Bus Clock Period **(33MHz)**	0.1% stability at 2.0V / 0.8V	50pF	30	30	nS
T_{LCH}	Local Bus Clock High Time		50pF	12	–	nS
T_{LCL}	Local Bus Clock Low Time		50pF	12	–	nS
T_{LCR}	Local Bus Clock Rise Time		50pF	–	3	nS
T_{LCF}	Local Bus Clock Fall Time		50pF	–	3	nS
—	Local Bus Clock Slew Rate		–	1	4	**V / nS**
T_{CRS}	CPU Reset Setup Time to Local Bus Clock	For 2x Clock Sync	50pF	2	–	nS
T_{CRH}	CPU Reset Hold Time from Local Bus Clock	For 2x Clock Sync	50pF	5	–	nS



Local Bus Clock Timing

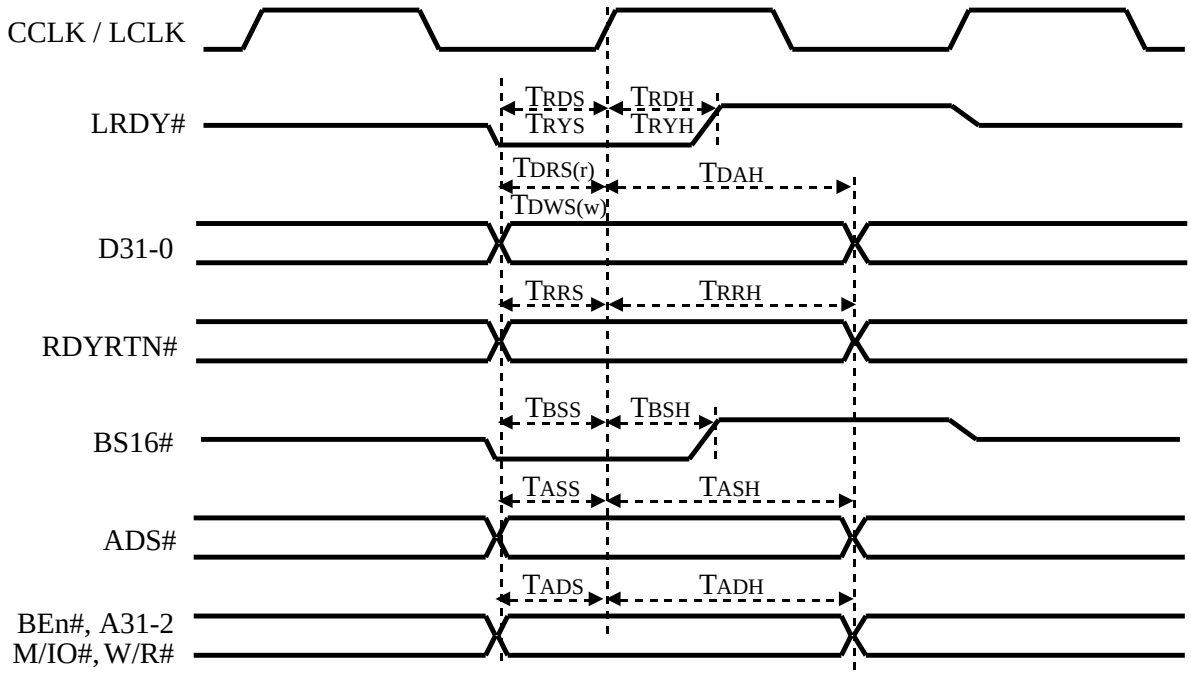


Local Bus '2x' Clock Synchronization Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65535 AC TIMING CHARACTERISTICS - LOCAL BUS INPUT SETUP & HOLD (33 MHz)

Symbol	Parameter	Notes	C_L Max	Min	Max	Units
T_{ADS}	Setup Time - A2-31,BEn#,M/IO#,W/R#		125pF	7	–	nS
T_{ASS}	Setup Time - ADS#		125pF	7	–	nS
T_{DRS}	Setup Time - D0-31 Read		125pF	5	–	nS
T_{DWS}	Setup Time - D0-31 Write		125pF	7	–	nS
T_{BSS}	Setup Time - BS16#		100pF	7	–	nS
T_{RDS}	Setup Time - LRDY#		100pF	5	–	nS
T_{RYS}	Setup Time - LRDY# tied to RDYRTN#		175pF	5	–	nS
T_{RRS}	Setup Time - RDYRTN#		100pF	5	–	nS
T_{ADH}	Hold Time - A2-31,BEn#,M/IO#,W/R#		125pF	2	–	nS
T_{ASH}	Hold Time - ADS#		125pF	2	–	nS
T_{DAH}	Hold Time - D0-31		125pF	2	–	nS
T_{BSH}	Hold Time - BS16#		100pF	2	–	nS
T_{RDH}	Hold Time - LRDY#		100pF	2	–	nS
T_{RYH}	Hold Time - LRDY# tied to RDYRTN#		175pF	2	–	nS
T_{RRH}	Hold Time - RDYRTN#		100pF	2	–	nS

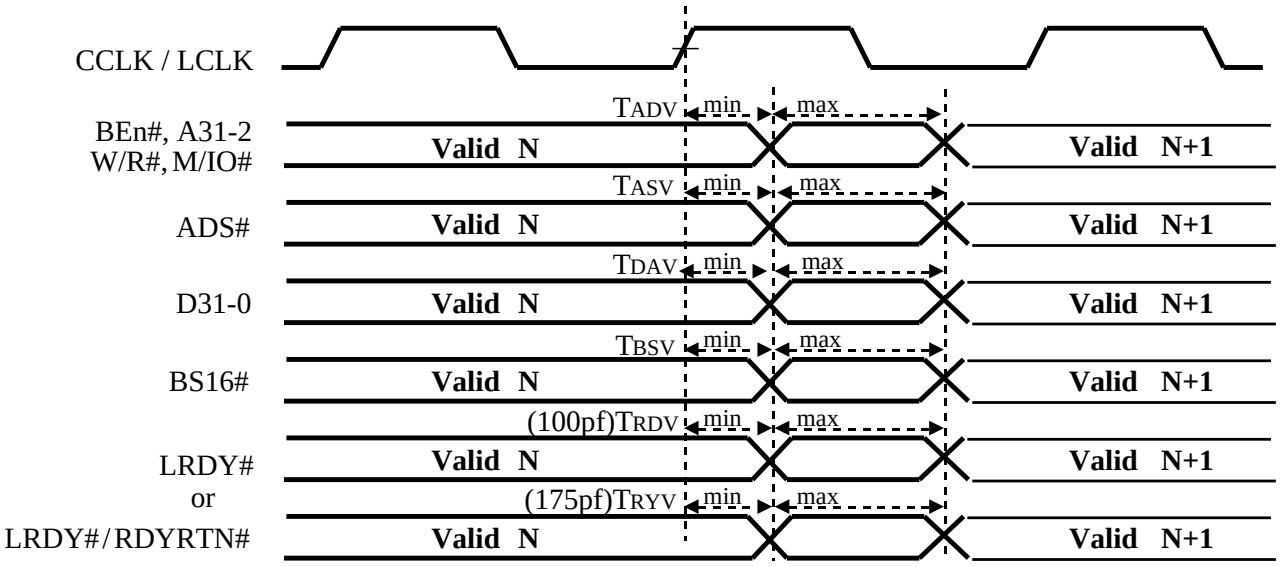


Local Bus Input Setup & Hold Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65535 AC TIMING CHARACTERISTICS - LOCAL BUS OUTPUT VALID (33 MHz)

Symbol	Parameter	Notes	C_L Max	Min	Max	Units
T_{ADV}	Bus Clock to Output Valid - A2-31,BEn#,M/IO#,W/R#		125pF	3	18	nS
T_{ASV}	Bus Clock to Output Valid - ADS#		125pF	3	18	nS
T_{DAV}	Bus Clock to Output Valid - D0-31		125pF	3	18	nS
T_{BSV}	Bus Clock to Output Valid - BS16#		100pF	3	18	nS
T_{RDV}	Bus Clock to Output Valid - LRDY#		100pF	3	14	nS
T_{RYV}	Bus Clock to Output Valid - LRDY# (connected to RDYRTN#)		175pF	3	17	nS

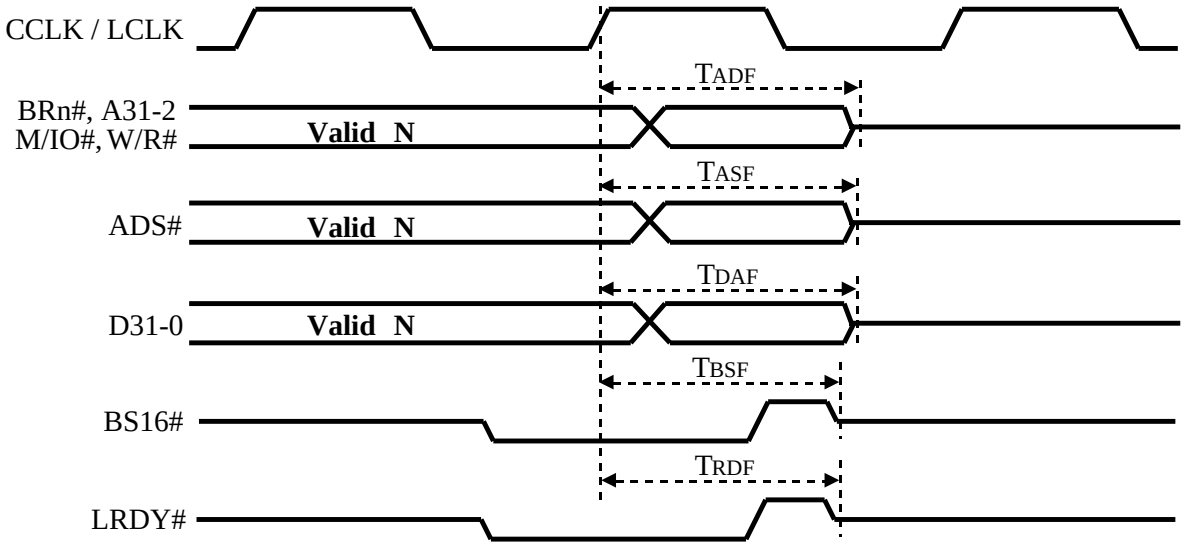


Local Bus Output Valid Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65535 AC TIMING CHARACTERISTICS - LOCAL BUS FLOAT DELAY (33MHZ)

Symbol	Parameter	Notes	C_L Max	Min	Max	Units
T_{ADF}	Float Delay - A2-31, BEn#, M/IO#, W/R#		125pF	–	20	nS
T_{ASF}	Float Delay - ADS#		125pF	–	20	nS
T_{DAF}	Float Delay - D0-31		125pF	–	20	nS
T_{BSF}	Float Delay - BS16#	Driven high before floating	100pF	–	30	nS
T_{RDF}	Float Delay - LRDY#	Driven high before floating	100pF	–	30	nS
	Float Delay - LRDY# connected to RDYRTN#		175pF	–	30	nS

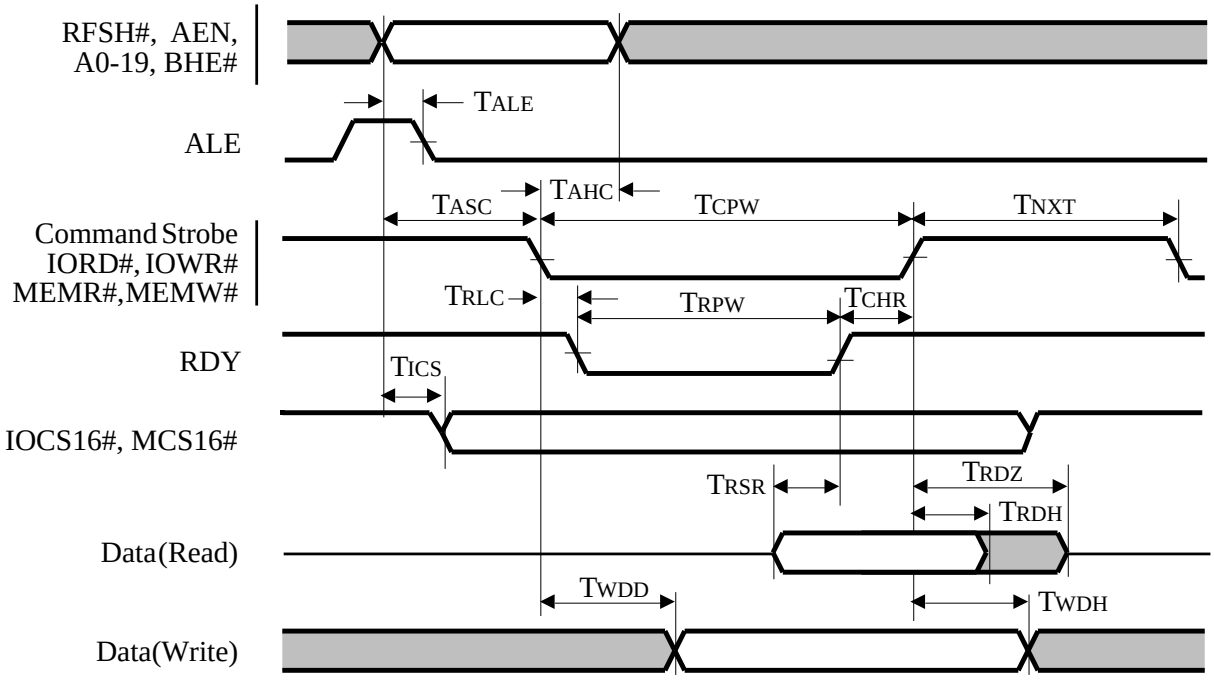


Local Bus Output Float Delay Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65535 AC TIMING CHARACTERISTICS - ISA BUS

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CPW}	Command Strobe Pulse Width		6Tm	–	–	nS
T_{CHR}	Command Strobe Hold from Ready		0	–	–	nS
T_{NXT}	Command Strobe Inactive to Next Strobe		3Tm	–	–	nS
T_{ALE}	Address Setup to ALE Inactive		29	–	–	nS
T_{ASC}	Address Setup to Command Strobe		30	–	–	nS
T_{ICS}	Address to IOCS16# & MEMCS16# Delay		–	–	2Tm	nS
T_{RSR}	Read Data Setup to Ready	Mem Accesses Only	25	–	–	nS
T_{RPW}	RDY Pulse Width	Mem Accesses Only	0	–	100Tm	nS
T_{AHC}	Address Hold to Command Strobe		20	–	–	nS
T_{RDH}	Read Data Hold from Command Strobe		10	–	–	nS
T_{RDZ}	Read Data Tri-Stated from Command Strobe		–	–	30	nS
T_{WDD}	Write Data Delay from Command Strobe		–	–	20	nS
T_{WDH}	Write Data Hold from Command Strobe		10	–	–	nS
T_{RLC}	RDY Low Delay from Command Strobe **(+5V)**	Mem Accesses Only	–	–	40	nS
T_{RLC}	RDY Low Delay from Command Strobe **(+3.3V)**	Mem Accesses Only	–	–	55	nS



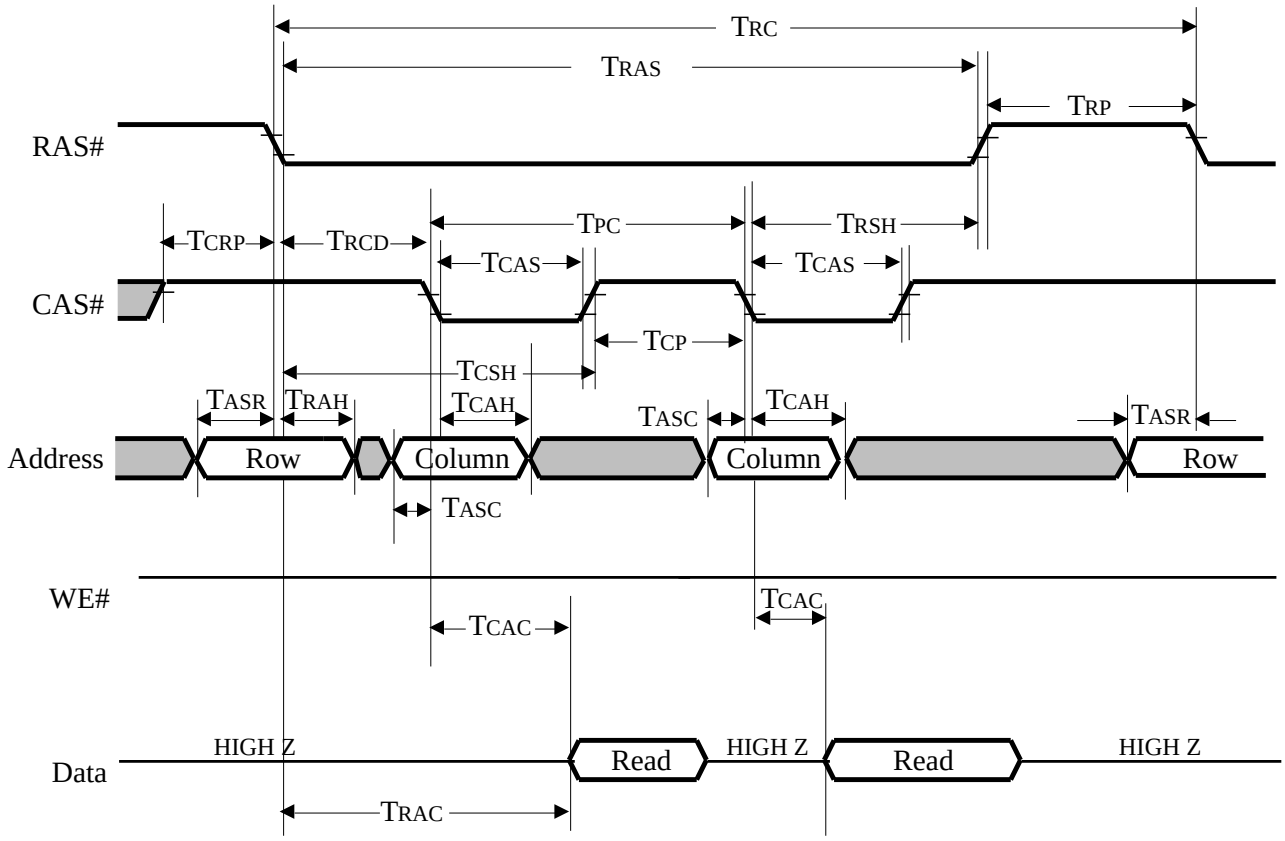
ISA Bus Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65535 AC TIMING CHARACTERISTICS - DRAM READ / WRITE

Symbol	Parameter	Notes	Min	Max	Units
T_{RC}	Read/Write Cycle Time		12Tm – 5	–	nS
T_{RAS}	RAS# Pulse Width		8Tm – 5	–	nS
T_{RP}	RAS# Precharge		4Tm – 3	–	nS
T_{CRP}	CAS# to RAS# Precharge		4Tm – 5	–	nS
T_{CSH}	CAS# Hold from RAS#		5Tm – 2	–	nS
T_{RCD}	RAS# to CAS# Delay		3Tm – 5	–	nS
T_{RSH}	RAS# Hold from CAS#		2Tm – 5	–	nS
T_{CP}	CAS# Precharge		Tm – 5	–	nS
T_{CAS}	CAS# Pulse Width		2Tm – 5	–	nS
T_{ASR}	Row Address Setup to RAS#		Tm – 5	–	nS
T_{ASC}	Column Address Setup to CAS#		2Tm – 8	–	nS
T_{RAH}	Row Address Hold from RAS#		Tm – 2	–	nS
T_{CAH}	Column Address Hold from CAS#		Tm – 2	–	nS
T_{CAC}	Data Access Time from CAS#	XR05[2-1]=0 (3MCLK CAS Cycle)	–	2Tm – 5	nS
		XR05[2-1]=1 (4MCLK CAS Cycle)	–	3Tm – 5	nS
T_{RAC}	Data Access Time from RAS#	XR05[2-1]=0 (3MCLK CAS Cycle)	–	5Tm – 2	nS
		XR05[2-1]=1 (4MCLK CAS Cycle)	–	6Tm – 2	nS
T_{DS}	Write Data Setup to CAS#		Tm – 5	–	nS
T_{DH}	Write Data Hold from CAS#		Tm – 5	–	nS
T_{PC}	CAS Cycle Time		3Tm – 1	–	nS
T_{WS}	WE# Setup to CAS#		1Tm – 5	–	nS
T_{WP}	WE# Hold from CAS#		2Tm – 5	–	nS

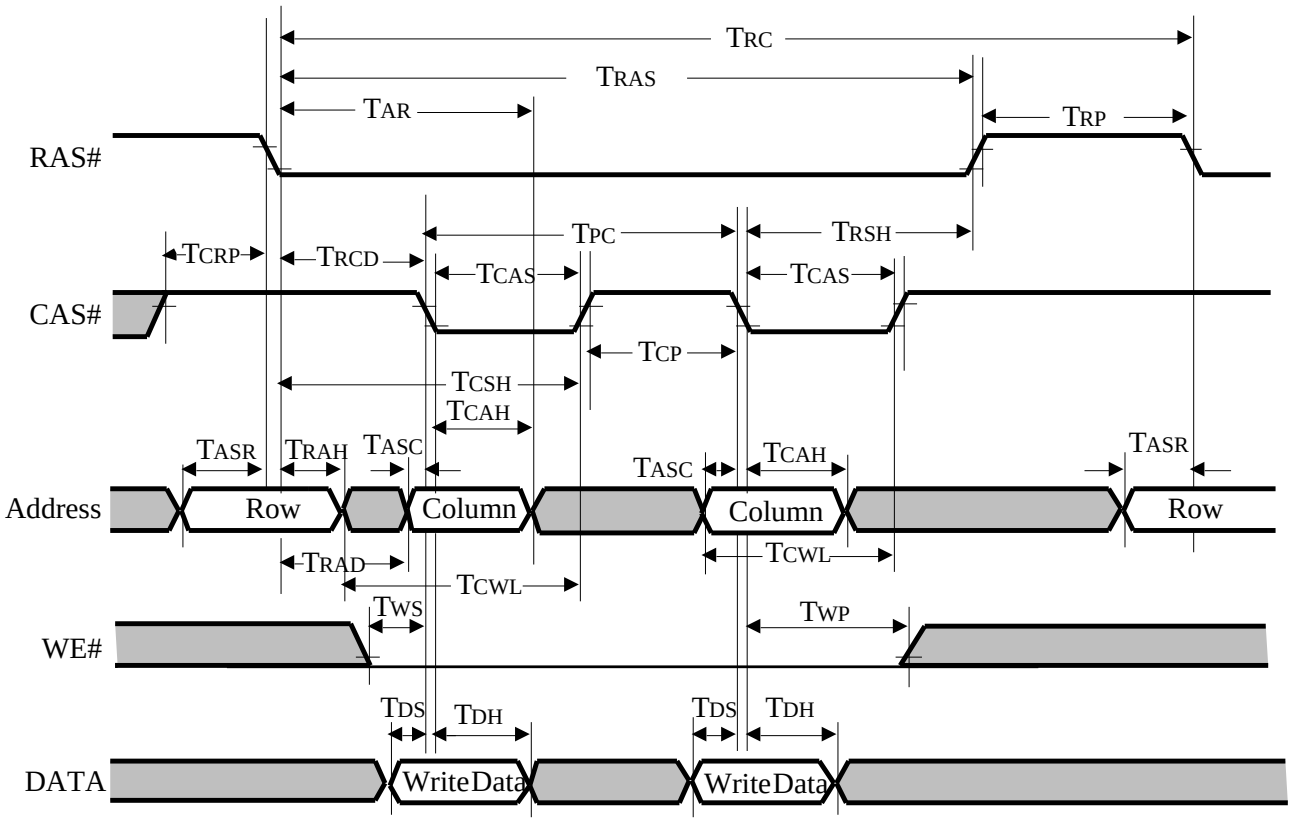
Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.



DRAM Page Mode Read Cycle Timing

Note: The above diagram represents a typical page mode read cycle. The number of actual CAS cycles may vary.

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.



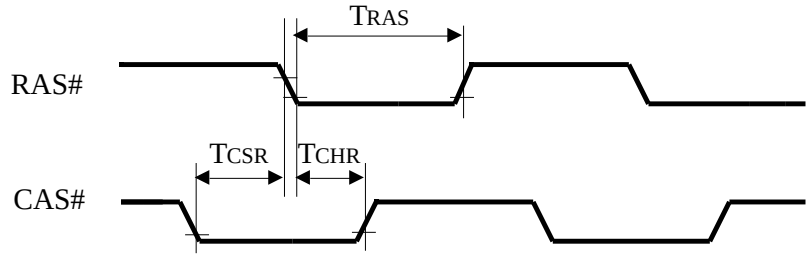
DRAM Page Mode Write Cycle Timing

Note: The above diagram represents a typical page mode read cycle. The number of actual CAS cycles may vary.

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65535 AC TIMING CHARACTERISTICS - REFRESH

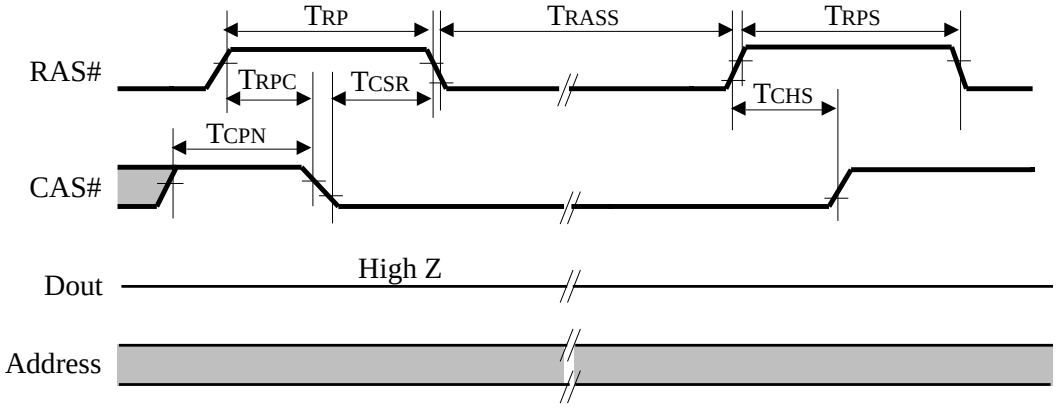
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CHR}	RAS# to CAS# Delay	Tm = 15.4 @ 65 MHz	5Tm – 5	–	5Tm + 5	nS
T_{CSR}	CAS# to RAS# Delay		Tm – 5	–	Tm + 5	nS
T_{RAS}	RAS# Pulse Width	5Tm = 89 ns (56 MHz) or 77 ns (65 MHz)	5Tm – 5	–	5Tm + 5	nS



CAS-Before-RAS (CBR) DRAM Refresh Cycle Timing

65535 AC TIMING CHARACTERISTICS - SELF REFRESH

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{RASS}	RAS# Pulse Width for Self-Refresh		100	–	–	µS
T_{RP}	RAS# Precharge		4Tm – 3	–	–	nS
T_{RPC}	RAS# to CAS# Delay		3Tm – 5	–	–	nS
T_{CHS}	CAS# Hold Time		0	–	–	nS
T_{CPN}	CAS# Precharge		Tm – 5	–	–	nS
T_{RPS}	RAS# Precharge for Self-Refresh		10Tm	–	–	nS



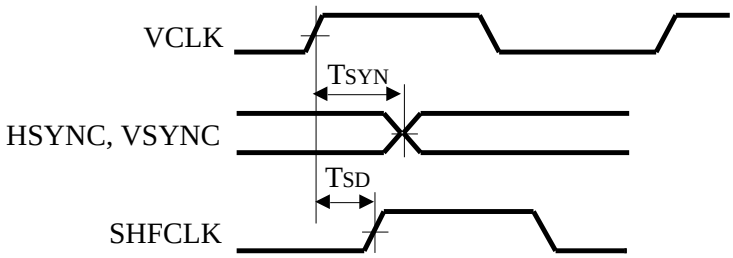
'Self-Refresh DRAM' Refresh Cycle Timing

Note: Upon exiting self-refresh mode, the 65535 will perform a complete set of CBR refresh cycles before resuming normal DRAM activity. The duration of the burst refresh will equal the panel power sequencing delay, programmed in XR5B bits 7-4.

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65535 AC TIMING CHARACTERISTICS - CRT OUTPUT

Symbol	Parameter		Min	Max	Units
T_{SYN}	HSYNC, VSYNC Delay from VCLK In **(5.0V)**	External Clock Option	–	50	nS
T_{SYN}	HSYNC, VSYNC Delay from VCLK In **(3.3V)**	External Clock Option	–	80	nS
T_{SD}	VCLK In to SHFCLK Delay **(5.0V)**	External Clock Option	–	30	nS
T_{SD}	VCLK In to SHFCLK Delay **(3.3V)**	External Clock Option	–	50	nS

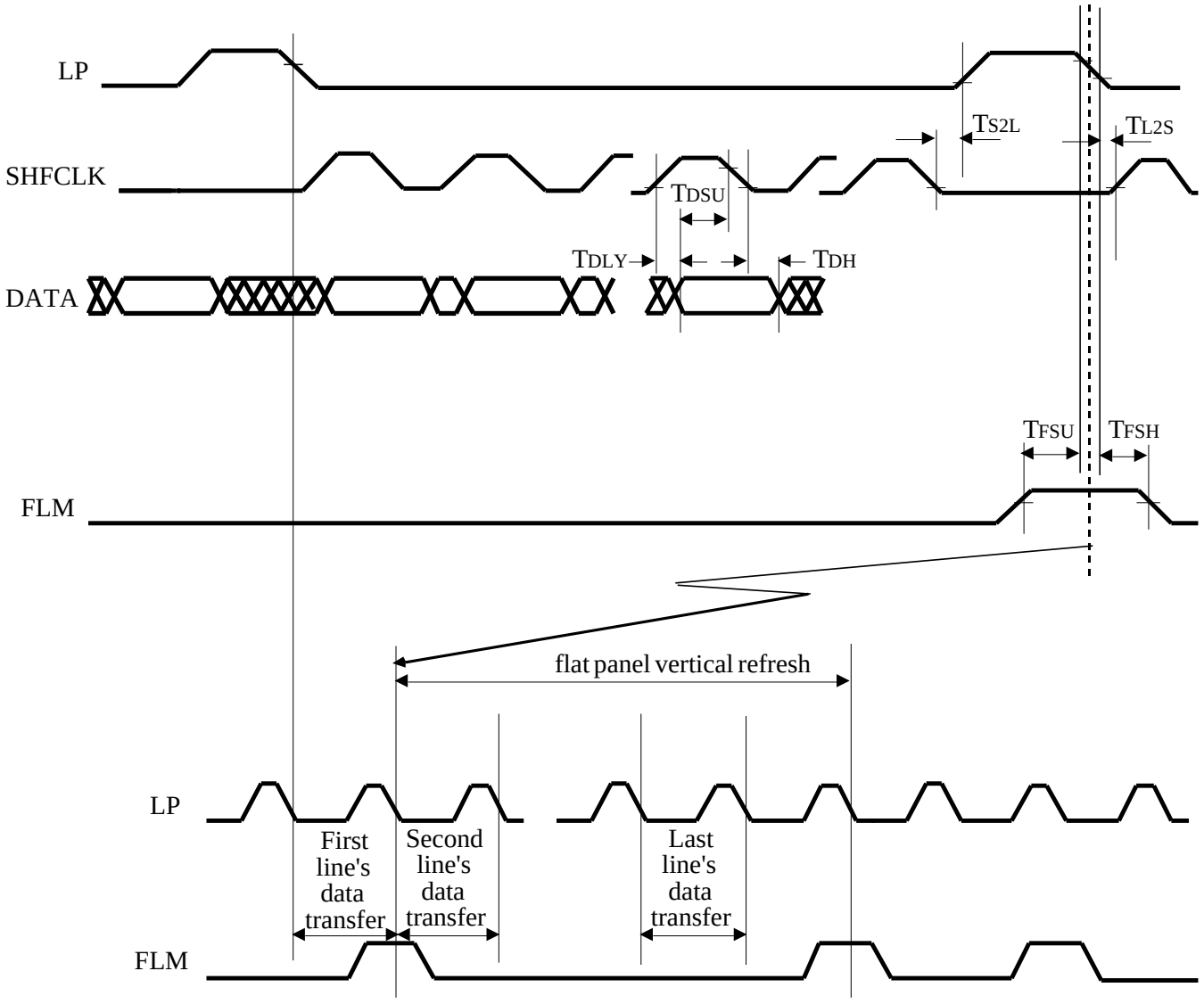


CRT Output Signal Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65535 AC TIMING CHARACTERISTICS - PANEL OUTPUT

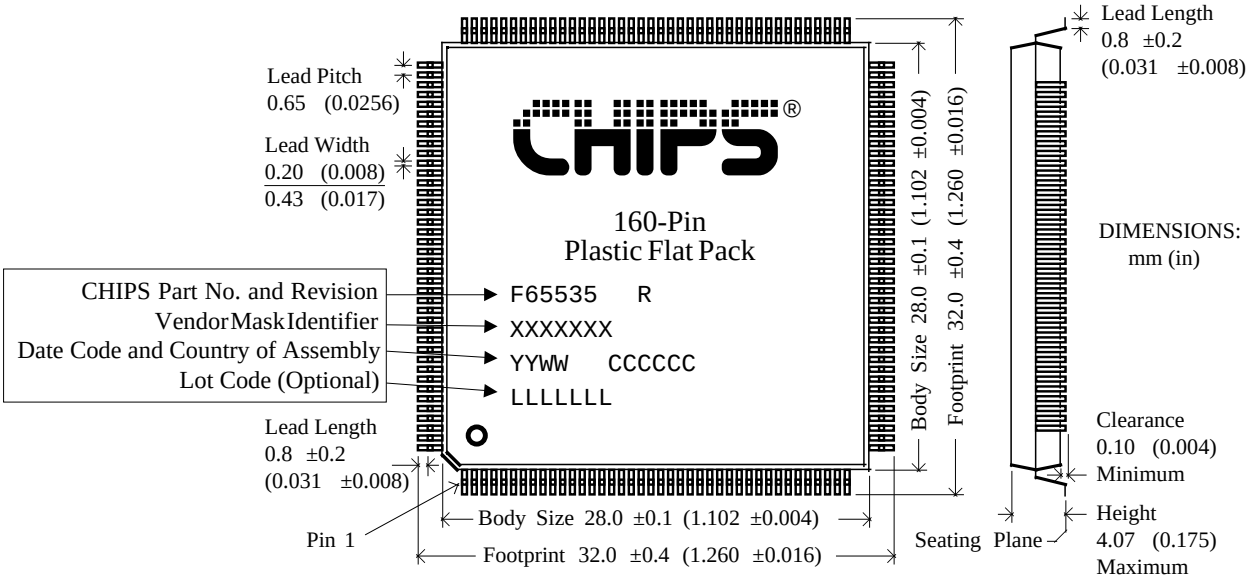
Symbol	Parameter		Min	Max	Units
T_{DSU}	Panel Data Setup to SHFCLK		5	–	nS
T_{DH}	Panel Data Hold to SHFCLK		10	–	nS
T_{DLY}	Panel Data Delay from SHFCLK		10	–	nS
T_{L2S}	SHFCLK Allowance Time from LP		Tc	–	nS
T_{S2L}	LP Allowance Time from SHFCLK		Tc	–	nS
T_{FSU}	FLM Setup Time		8 Tc	–	nS
T_{FSH}	FLM Hold Time		8 Tc	–	nS



Panel Output Signal Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 65MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

Mechanical Specifications



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Title: 65535 Data Sheet

Publication No.: DS165.1
Stock No.: 010165-002
Revision No.: 2.0