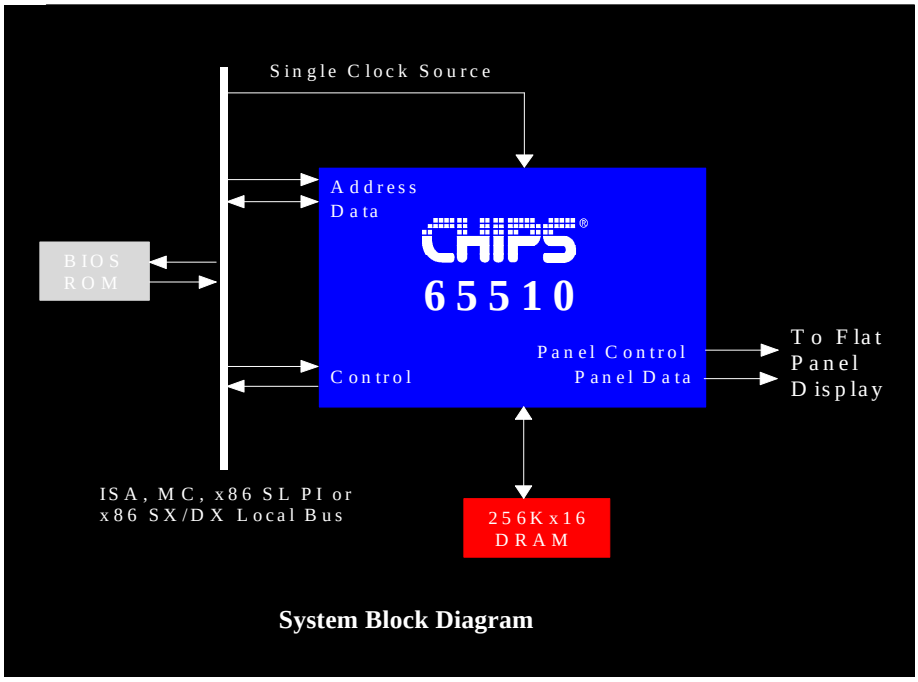
65510

Flat Panel VGA Controller

- Highly integrated solution and small form factor flat panel controller solution
  - Integrated 256x18 palette
  - Direct support for Dual or Single Scan panel
  - Separate address and data buses
  - Single clock source
  - 100-pin package
- Single 256Kx16 DRAM provides two-chip VGA subsystem
- Memory options are (1) 256Kx16 DRAM or (4) 256Kx4 DRAMs
- Mixed 3.3V/5.0V panel, bus and memory interface capability for low power operation
- Advanced power management features minimize power consumption during panel operation
- Dedicated input pin supports minimum power operation in Suspend and Resume modes
- Register programmable 4mA or 8mA drive on all bus data line (D0-15) and panel control and data signals
- Multiple Bus Interface support for
  - High-speed x86 SL PI Bus
  - High-speed x86 SX/DX Local Bus
  - EISA/ISA (PC/AT) Bus
  - Micro Channel (MC) Bus
- High performance Linear Acceleration™ drivers for Windows™ acceleration
- Supports Dual Panel/Dual Drive (D/D) and Single Panel/Single Drive (S/S) LCD, Plasma and El Panels
- Generates 64 gray levels of Monochrome panels
- Single clock source with rate multiplier function to generate a wide range of clock frequencies
- Optional "clock doubler" functionality
- Programmable vertical compensation techniques increase usable display area
- Intelligent SMARTMAP™ color to gray scale conversion
- Fully compatible with IBM® VGA
- High performance resulting from buffered writes (Write Buffer) and fast screen updates (internal asynchronous 16-level FIFO)
- Text Enhancement feature improves contrast of text on flat panel displays
- Three software selectable RGB color to gray scale reduction techniques
- Full backwards compatibility with EGA, CGA, MDA and Hercules graphics standards
- Chip pinouts optimized for PCB layout
- Programmable polynomial based Frame Rage Control gray scale algorithm supports fast response "mouse quick" displays by reducing flicker without increasing panel vertical refresh rate
- 16-bit display memory operations



System Block Diagram

Product Overview

The 65510 VGA flat panel controller provides a very low power consumption, minimum chip-count, minimum-board space, low-cost graphics solution for inexpensive notebook, sub-notebook, handheld and pen-based portable PCs and word processors. The 65510 only requires a single 256Kx16 DRAM and single clock input, such that a complete VGA subsystem can be implemented with just two ICs.

The 65510 employs a variety of advanced power management features to reduce power consumption of the display subsystem and extend battery life. The 65510's internal logic, memory interface, bus interface and flat panel interface can be independently configured to operate at either 3.3V or 5V. The 65510 is optimized for minimum power consumption during normal operation and two power-saving modes - Panel Off and Standby.

The 65510 supports a wide variety of monochrome Single-Panel / Single Drive (SS) and Dual-Panel / Dual Drive (DD) STN LCDs, TFT LCDs EL and plasma panels with up to 64 gray scales at 640x480 resolution or 16 gray scales at 800x600 resolution. The 65510 provides a variety of programmable features to optimize display quality, such as Vertical and Horizontal Compensation, SMART-MAP™ Text Enhancement, three selectable color-to-gray scale reduction techniques and a polynomial FRC grayscale algorithm, which reduces flicker on fast-response "mouse quick" LCD's without increasing the LCD's vertical refresh rate. The 65510 includes a number of performance-enhancement techniques, which provide good performance at low clock frequencies (resulting in low power consumption). The 65510's x86 SL PI and x86 DX/SX local bus operation provides high performance in 256-color modes. The 65510's internal asynchronous FIFO design provides minimum wait-state reads and fast display updates. The 65510's linearly addressable video memory allows the CPU to linearly address the 512 KBytes of video memory, enabling the use of high-performance 32-bit software drivers (called Linear Acceleration).

The 65510 is fully compatible with the VGA graphics standard at the register, gate, and BIOS levels. The 65510 provides full backwards compatibility with the EGA, CGA, MDA and Hercules graphics standards without using NMIs. CHIPS' and third-party vendors supply fully VGA-compatible BIOS's, end-user utilities and drivers for common application programs (e.g., Windows, OS/2, WordPerfect, Lotus, etc.). CHIPS' drivers for Windows include a Big Cursor (to increase the cursor's legibility on monochrome flat panels) and 32-bit Linear Acceleration and panning/scrolling drivers (to increase performance).

For more information contact your local sales representative.

MINIMUM CHIP COUNT / BOARD SPACE

The 65510 provides a minimum chip count / board space, low-cost VGA sub-system. The 65510 integrates a versatile VGA flat panel controller and 256x18 VGA palette in a 100-pin plastic flat pack package. The 65510 requires a single 256Kx16 DRAM and single clock input, such that a complete VGA sub-system for motherboard applications can be implemented with just two ICs:

Qty	Chip Type
1	65510 Controller
1	256Kx16 DRAM
2	Total

No external buffers or glue logic are required for the 65510's bus interface, memory interface, or panel interface.

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65510

Flat Panel VGA Controller

Data Sheet

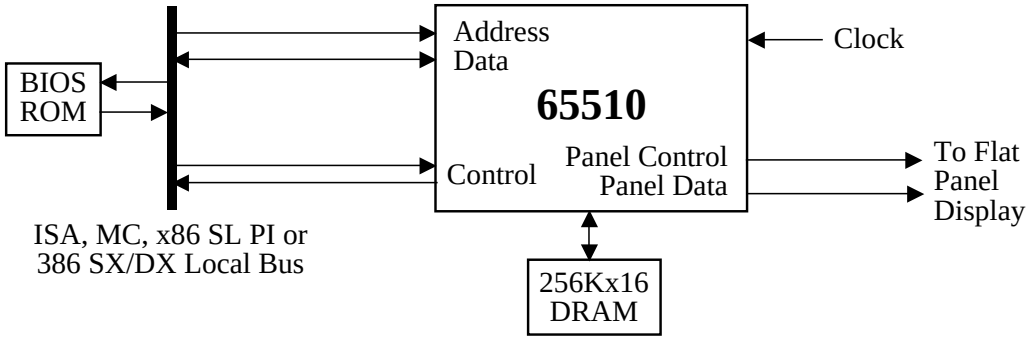
December 1992

P R E L I M I N A R Y

CHIPS®

65510
Flat Panel VGA Controller

- Highly integrated Flat Panel controller
  - Separate Address and Data buses
  - Direct support for Dual or Single Scan panels
  - Single clock source
  - 100-pin package
- Single 256Kx16 DRAM provides two-chip VGA subsystem
- Innovative clock "doubling" functionality
- Memory options are (1) 256Kx16 DRAM or (4) 256Kx4 DRAMs
- 3.3V/5V memory interface for low power normal mode of operation
- 3.3V/5V panel and bus interfaces to support a variety of panels and buses
- Register-programmable 4mA or 8mA drive on bus data lines D0-15 and panel interface signals
- Advanced power management features minimize power consumption during normal operation
- Dedicated input pin supports minimum power operation in Suspend and Resume modes (less than 500µA)
- Integrated Multiple Bus Interface
  - High-speed x86 SL PI Bus
  - EISA/ISA (PC/AT) Bus
  - Micro Channel (MC) Bus
  - High Speed 386 SX/DX Local Bus
- High performance resulting from buffered writes (Write Buffer) and fast screen updates (internal asynchronous 16-level FIFO)
- 16-bit display memory operations
- CPU activity indicated for orderly power down procedure
- Generates 64 gray levels on Monochrome Panels
- Supports 640x480, x400, x200 Dual Panel/Dual Drive (D/D) and Single Panel/Single Drive (S/S) LCD, Plasma, and EL Panels
- Single clock source with rate multiplier function to generate a wide range of dot clock frequencies for low power operation
- Programmable polynomial based Frame Rate Control gray scale algorithm supports fast response "mouse quick" displays by reducing flicker without increasing panel vertical refresh rate
- Programmable vertical compensation techniques maximize display area
- Intelligent SMARTMAP™ color to gray scale conversion
- Text Enhancement feature improves contrast of text on flat panel displays
- Three software selectable RGB color to gray scale reduction techniques
- Linearly Addressable Video Memory enables utilization of high performance 32-bit software drivers
- Fully Compatible with IBM™ VGA
- Full backwards compatability with EGA, CGA, MDA, and Hercules graphics standards
- Small low-cost package: EIAJ-standard 100-pin plastic flat pack available in thin 20 mil lead pitch or standard 25 mil lead pitch packages
- Chip pinouts optimized for PCB layout



System Diagram

Revision History

Revision	Date	By	Comment
0.1	??	DH	Internal Review - Rough Draft
0.2	3/92	ST	Internal Review - Added Pinouts and Mechanical Specifications
0.3	3/92	SV	First Release - Added std package specs and correct pinouts
0.4	4/92	ST	Internal Review - Modified Register Section
0.41	5/92	SV	Advance Product Information NDA Required Release
0.5	6/92	SV/DH	Added Electrical Specification and Application Schematic Sections
0.6	8/92	DH/SV/JS	Fixed 256Kx16 DRAM Pinouts in Application Schematics Fixed various extension register bit definition Added 'Future' note to TQFP package diagrams Fixed miscellaneous typographical errors Added Micro Channel Bus Interface Application Schematics Added "Register-Programmable-Output-Drive" feature Clarified TQFP package as "Future' availability Added clarifying notes to lead pitch in mechanical specs Changed thickness specification for TQFP package
0.7	10/92	SV	Updated Introduction Section Corrected DRAM Interfacing Updated Extended Register XR28 Changed pinout to reflect Activity Indicator Pin Removed 3V-Out/5V-In protection description Added Panel Interface and Panel Pixel Timing Section

Table of Contents

List of Figures and Tables

Introduction

The 65510 VGA flat panel controller provides a very low power consumption, minimum-chip-count/board-space, low-cost graphics solution for inexpensive notebook, sub-notebook, hand-held, and pen-based portable PCs and word processors. The 65510 requires only a single 256Kx16 DRAM and single clock input, such that a complete VGA subsystem can be implemented with just two ICs. The 65510 employs separate address and data buses and direct flat panel drive capability, so that no external transceivers or buffers are required.

The 65510 employs a variety of advanced power management features to reduce power consumption of the display subsystem and extend battery life. The 65510's internal logic, memory interface, bus interface, and flat panel interface can be independently configured to operate at either 3.3V or 5V. The 65510 is optimized for minimum power consumption during normal operation and two power-saving modes -- Panel Off and Standby.

The 65510 supports a wide variety of monochrome Single-Panel, Singe-Drive (SS) and Dual-Panel, Dual-Drive (DD) STN LCDs, TFT LCDs, EL and plasma panels with up to 64 gray scales at 640x480 resolution. The 65510 provides a variety of programmable features to optimize display quality, such as Vertical and Horizontal Compensation, SMARTMAP™, Text Enhancement, three selectable color to gray scale reduction techniques, and a polynomial FRC gray scale algorithm, which reduces flicker on fast response "mouse quick" LCDs without increasing the LCD's vertical refresh rate.

The 65510 is fully compatible with the VGA graphics standard at the register, gate, and BIOS levels. The 65510 provides full backwards compatibility with the EGA, CGA, MDA, and Hercules graphics standards without using NMIs. CHIPS' and third-party vendors supply fully VGA-compatible BIOS's, end-user utilities, and drivers for common application programs (e.g., Windows, OS/2, Word Perfect, Lotus, etc.). CHIPS' drivers for Windows include a Big Cursor (to increase the cursor's legibility on monochrome flat panels), a panning/scrolling driver (to increase performance), and a high performance 32-bit linear addressing driver for the 640x480x256 color mode.

MINIMUM CHIP COUNT / BOARD SPACE

The 65510 provides a minimum chip count/board space, low-cost VGA sub-system. The 65510 integrates a versatile VGA flat panel controller and 256x18 VGA palette in a 100-pin plastic flat pack. The 65510 requires a single 256Kx16 DRAM and single clock input, such that a complete VGA sub-system for motherboard applications can be implemented with just two ICs. No external buffers or glue logic are required for the 65510's bus interface, memory interface, or panel interface. The 65510 employs separate address and data buses; the data bus has 4/8 mA drive capability so that the bus can be driven directly. The 65510 also provides a direct interface to the flat panel with 4/8 mA drive capability on the flat panel outputs.

Display Memory Interface

The 65510 utilizes a single 256Kx16 DRAM for video memory, resulting in a minimum chip count/board space VGA sub-system (alternately, four 256Kx4 DRAMs may be used for video memory). The 65510 serves as a DRAM controller for the system's video memory. It handles DRAM refresh, fetches data from display memory as required to refresh the flat panel, interfaces the CPU to display memory, and supplies all necessary DRAM control signals. Display memory control signals are derived from the CLKIN clock input.

The 65510 supports either 2CAS/-1WE/ DRAMs or 1CAS/-2WE/ DRAMs. PCB designs may be set up to accommodate either DRAM type; the 65510 may be programmed to output control signals appropriate to the DRAM installed.

Clock Selection

The 65510 requires only a single clock input on the CLKIN pin. This fixed frequency clock input provides the memory clock. The 65510's on-chip rate multiplier internally divides the memory clock to generate a fully programmable dot clock, such that a wide variety of flat panel shift clock and vertical refresh rates can be generated.

Clock Doubling

The 65510 provides the functionality to double the input clock (CLKIN input) of 14.31818MHz to internally generate MCLK and DCLK. Rate multiplier functionality is available to divide the doubled input clock frequency to generate a variety of dot clocks.

The clock "doubling" feature may be enabled by connecting MA4 to ground with a pull-down resistor of 1.5K ohms at reset. This feature is especially useful for low-power/high-integration applications where a single clock source is used for the entire system.

MIXED VOLTAGE OPERATION

The 65510 provides three power planes: Internal logic and memory power, bus power, and display power. The internal logic and memory power plane is represented by pins 38 and 88 (VCCM) on F65510, the bus power plane by pin 13 (VCCB) on F65510 and the display power plane by pin 63 (VCCD) on F65510. The 65510 provides "mixed" voltage operation where the different power planes may each be run at 3.3V or 5V. The following table shows the VCC pin and the corresponding pins covered:

VCC Pin on F65510	Power Plane	Pins Covered
38, 88	Internal Logic and Memory	66 - 96
13	Bus	1-49 98-100
63	Display	50-65

ADVANCED POWER MANAGEMENT

Normal Operating Mode

The 65510 is a full-custom, sub-micron CMOS integrated circuit optimized for low power consumption during normal operation. The 65510 provides CAS-before-RAS refresh cycles for the DRAM video memory. The 65510 provides "mixed" 3.3 V and 5.0 V operation by providing dedicated VCC pins for the 65510's internal logic, bus interface, and flat panel interface. Each dedicated VCC can be either 3.3 V or 5.0 V, such that the 65510 internal logic and the memory interface can operate at 3.3 V and the bus interface and panel interface can independently operate at either 3.3 V or 5.0 V. A minimum, yet flexible, clock architecture is used to save power -- a single, fixed-frequency clock input provides the 65510's memory clock, and the 65510's internal rate multiplier function provides a programmable dot clock based on the memory clock. The 65510's performance-enhancement features minimize the memory clock frequency (and thus power consumption) required to achieve a certain performance level. The 65510's proprietary gray scaling algorithm produces a flicker-free display with a minimum dot clock and panel vertical refresh rate. (Note: the power consumption of the controller, video memory and flat panel all increase linearly with dot clock frequency and panel vertical refresh rate). In order to minimize power consumption by minimizing the internal logic, the 65510 supports only monochrome LCD, EL, and plasma flat panels.

Panel Off

In the Panel Off mode of operation, the 65510 turns off the flat panel, and generates panel power sequencing. The VGA sub-system remains active, such that the CPU can read/write video memory and I/O registers. The 65510's dot clock can be reduced significantly, saving power. Panel Off mode is activated by programming Extended Register XR52 bit-3. XR52 bit-5 provides the option of either tri-stating all the video interface signals or forcing them into an inactive state as shown in the table below:

T65510 PIN#	F65510 PIN#	SIGNAL NAME	SIGNAL STATUS	
			XR52 Bit 5 = 0	XR52 Bit 5 = 1
51	53	FLM	Inactive - driven low	Tristated (Weak Pull-up)
50	52	LP	Inactive - driven low	Tristated (Weak Pull-up)
62	64	SHFCLK	Inactive - driven low	Tristated (Weak Pull-up)
63	65	ACDCLK	Inactive - driven low	Tristated (Weak Pull-up)
53	55	P0	Inactive - driven low	Tristated (Weak Pull-up)
54	56	P1	Inactive - driven low	Tristated (Weak Pull-up)
55	57	P2	Inactive - driven low	Tristated (Weak Pull-up)
56	58	P3	Inactive - driven low	Tristated (Weak Pull-up)
57	59	P4	Inactive - driven low	Tristated (Weak Pull-up)
58	60	P5	Inactive - driven low	Tristated (Weak Pull-up)
59	61	P6	Inactive - driven low	Tristated (Weak Pull-up)
60	62	P7	Inactive - driven low	Tristated (Weak Pull-up)

Standby Mode

In the Standby mode of operation, the 65510 suspends all CPU, memory, and display activites. The 65510 places the DRAM in its self-refresh mode of operation, and the 65510's clock input can be shut off after a delay of 64µs from STNDBY/ going low. The VGA sub-system dissipates minimum power during Standby mode. Since the 65510 is a fully static device, the contents of the controller's registers and on-chip palette are maintained during Standby. Therefore, Standby mode provides fast Suspend/Resume modes. Standby mode is activated when the STNDBY/ pin is forced low. The status of the video interface signals during standby is shown in the table below:

T65510 PIN#	F65510 PIN#	SIGNAL NAME	SIGNAL STATUS
51	53	FLM	Inactive - driven low
50	52	LP	Inactive - driven low
62	64	SHFCLK	Inactive - driven low
63	65	ACDCLK	Inactive - driven low
53	55	P0	Inactive - driven low
54	56	P1	Inactive - driven low
55	57	P2	Inactive - driven low
56	58	P3	Inactive - driven low
57	59	P4	Inactive - driven low
58	60	P5	Inactive - driven low
59	61	P6	Inactive - driven low
60	62	P7	Inactive - driven low

CPU BUS INTERFACE

The 65510 provides a direct interface to the 386 DX/SX local bus, x86 SL PI ("Peripheral Interface") bus, MC (MicroChannel) bus and EISA/ISA (PC/AT) bus. Strap options allow the user to configure the chip for the type of interface desired. Control signals for all interface types are integrated on chip. The 65510's linearly addressable video memory allows the CPU to linearly address the 512 KBytes of video memory, enabling the use of high-performance 32-bit software drivers.

PROGRAMMABLE OUTPUT DRIVE

The 65510 provides register programmable functionality to double the output drive on all the output pins. Refer to the pin list tables for the T65510 (TQFP) and F65510 (PQFP) for drive specifications. Extension register 6C (XR6C), the programmable output drive register, bits 2-4 provide selection of normal drive or "doubled" drive on the panel interface outputs, bus interface output and memory interface outputs respectively. For example, memory address lines MA0-MA8 have 2mA drive and the output drive can be doubled to 4mA by setting XR6C bit-4 to 1.

CPU ACTIVITY INDICATOR

In the ISA bus configuration, the 65510 provides an output pin called ACTIND (pin 49 on F65510) to facilitate an orderly powerdown sequence. The ACTIND output is an active high signal which is driven high every time a valid VGA memory read/write operation or VGA I/O read/write operation is executed by the CPU. This signal may be used by the power management circuitry to put the 65510 in PNLOFF or STANDBY power down modes. The ACTIND output (pin 49 on F65510) may be configured to be the ERMEN/ output in the ISA Bus configuration. When the CPU executes a memory read or write cycle in text mode, ERMEN/ goes low two MCLK cycles prior to the fall of RAS/ and stays active until RAS/ is asserted. ERMEN/ is driven high in graphics modes and during all display refresh accesses. The ACTIND pin may be configured to be ERMEN/ by setting XR28 bit-3.

HIGH PERFORMANCE FEATURES

The 65510 includes a number of performance-enhancement techniques, which provide good performance at low clock frequencies (resulting in low power consumption). The 65510's x86 SL PI and 386 DX/SX local bus operation provide significantly higher performance than the slower ISA bus. The 65510's 8-bit internal data path provides high performance in 256-color modes. The 65510's internal asynchronous FIFO design provides minimum wait-state reads and fast display updates. The 65510's linearly addressable video memory allows the CPU to linearly address the 512 KBytes of video memory, enabling the use of high-performance 32-bit software drivers.

DISPLAY ENHANCEMENT FEATURES

Display quality is one of the most important features for the success of any flat panel-based system. The 65510 provides many features to enhance the flat panel display quality.

Superior Display Quality

The 65510 produces up to 64 flicker-free gray scales on monochrome or grayscale panels. Because most application software is written for

color CRT monitors, the 65510 provides several proprietary features to maximize display quality on monochrome flat panels. Via its Extension Registers, the 65510 provides the flexibility to interface to a wide range of flat panels and provide full compatibility transparently to application software.

RGB Color To Gray Scale Reduction

The 18 bits of color palette data from the VGA standard color lookup table (CLUT) are reduced to 6 bits for 64 gray scales via one of three selectable RGB color to gray scales reduction techniques:

1) NTSC Weighting: 5/16 Red 9/16 Green 2/16 Blue
2) Equal Weighting: 5/16 Red 6/16 Green 5/16 Blue
3) Green Only: 6 bits of Green only

NTSC is the most common weighting, which is used in television broadcasting. Equal weighting increases the weighting for Blue, which is important for applications such as Microsoft Windows 3.x which often uses Blue for background colors. Green Only is useful for replicating on a flat panel the display of software optimized for IBM's monochrome monitors which use the six Green bits of palette data.

Gray Scale Algorithm

A proprietary polynomial-based Frame Rate Control (FRC) and dithering algorithm in the 65510's hardware generates 64 gray levels on monochrome panels. The FRC technique simulates 16 gray levels on monochrome panels by turning the pixels on and off over several frames in time. The dithering technique increases the number of gray scales from 16 to 64 by altering the pattern of gray scales in adjacent pixels. By programming the polynomial (an 8-bit value in Extension Register XR6E), the FRC algorithm may be adjusted to reduce flicker without increasing the panel's vertical refresh rate. The persistence (response time) of the pixels varies among panel manufacturers and models. By re-programming the polynomial by trial-and-error while viewing the display, the FRC algorithm can be adjusted to match the persistence of the particular panel. With this technique, the 65510 produces 64 flicker-free gray scales on the latest fast response "mouse quick" film compensated monochrome STN LCDs. The alternate method of reducing flicker -- increasing the panel's vertical refresh rate -- has several drawbacks. As the vertical refresh rate increases, the panel's power consumption increases, ghosting (cross-talk) increases, and contrast decreases.

Vertical & Horizontal Compensation

Vertical & Horizontal Compensation are programmable features that adjust the display to completely fill the flat panel display. Vertical Compensation increases the usable display area when running lower resolution software on a higher resolution panel. Unlike CRT monitors, flat panels have a fixed number of scan lines (e.g., 200, 400, or 480). Lower resolution software run on a higher resolution panel only partially fills the usable display area. For instance, 350-line EGA software displayed on a 480-line panel would leave 130 blank lines at the bottom of the display, and 400-line VGA text or Mode 13 images would leave 80 blank lines at the bottom. The 65510 offers the following Vertical Compensation techniques to increase the useable screen area:

Vertical Centering displays text or graphics images in the center of the flat panel, with a border of unused area at the top and bottom of the display. Automatic Vertical Centering automatically adjusts the Display Start address such that the unused area at the top of the display equals the unused area at the bottom. Non-Automatic Vertical Centering enables the Display Start address to be set (via programming the Extension Registers) such that text or graphics images can be positioned anywhere on the display.

Line replication (referred to as "stretching") duplicates every Nth display line (where N is programmable), thus stretching text characters and graphic images an adjustable amount. The display can be stretched to completely fill the flat panel area. Double scanning, a form of line replication where every line is replicated, is useful for running 200 line software on a 400 line panel.

Blank line insertion, inserts N blank lines (where N is programmable) between each line of text characters. Thus text can be evenly spaced to fill the entire panel display area without altering the height and shape of the text characters. Blank line insertion can be used in text mode only.

Tall Fonts™ uses a non-VGA standard font such that text fills almost all lines on the flat panel and all lines of text are the same size. For example, an 8x19 font would fill 475 lines on a 480-line panel.

Each of these Vertical Compensation techniques can be controlled by programming the Extension Registers. Each Vertical Compensation feature can be individually disabled, enabled and adjusted. A combination of Vertical Compensation features can be used by adjusting the features' priority order.

For example, text mode vertical compensation consists of four priority order options:

- Double Scanning+Line Insertion, Double Scanning, Line Insertion
- Double Scanning+Line Insertion, Line Insertion, Double Scanning
- Double Scanning+Tall Fonts, Double Scanning, Tall Fonts
- Double Scanning+Tall Fonts, Tall Fonts, Double Scanning

Text and graphics modes offer two Line Replication priority order options:

- Double Scanning+ Line Replication, Double Scanning, Line Replication
- Double Scanning+ Line Replication, Line Replication, Double Scanning

Horizontal Compensation techniques include Horizontal Compression, Horizontal Centering, and Horizontal Doubling. Horizontal Compression will compress 9-dot text to 8-dots such that 720-dot text in Hercules modes will fit on a 640-dot panel.

SmartMap™

SmartMap™ is a proprietary feature that can be invoked to intelligently map colors to gray levels in text mode. SmartMap™ improves the legibility of flat panel displays by solving a common problem.

Most application programs are optimized for color CRT monitors using multiple colors. For example, a word processor might use a blue background with white characters for normal text, underlined text could be displayed in green, italicized text in yellow, and so on. This variety of colors, which is quite distinct on a color CRT monitor, can be illegible on a monochrome flat panel display if the colors are mapped to adjacent grayscale values. In the example, underlined and italicized text would be illegible if yellow is mapped to grayscale 4, green to grayscale 6 with the blue background mapped to grayscale 5.

SmartMap™ compares and adjusts foreground and background grayscale values to produce adequate display contrast on flat panel displays. The minimum contrast value and the foreground / background grayscale adjustment values are programmed in the 65510's Extension Registers. This feature can be disabled if desired.

Text Enhancement

Text Enhancement is another feature of the 65510 that improves image quality on flat panel displays. Many applications, such as MS-DOS, use Dim White for normal text characters, which results in non-optimal contrast on flat panels. When turned "on," the Text Enhancement feature displays Dim White as Bright White, thereby optimizing the contrast level on flat panels. This feature inverts the functionality of the Intensity Bit for White only. Highlighted white, which is displayed as Bright White when Text Enhancement is "off," is shown as Dim White with Text Enhancement "on," thus maintaining a difference between normal and highlighted text. Text Enhancement can be turned "on" and "off" by changing a bit in one of the Extension Registers.

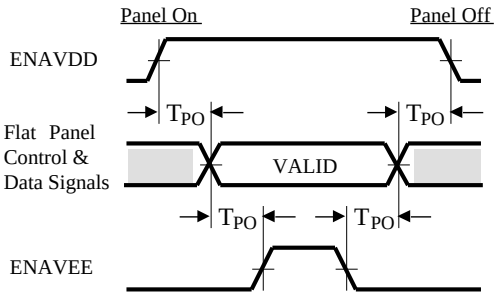
Inverse Video

Inverse video can be enabled in text modes only (normal video is displayed in graphics modes), in graphics modes only (normal video is displayed in text modes), or in both text and graphics modes.

PANEL POWER SEQUENCING

Flat panel displays are extremely sensitive to conditions where full biasing voltage VEE is applied to the liquid crystal material without enabling the control and data signals to the panel. This results in severe damage to the panel and may disable the panel permanently. The 65510 provides two pins called ENAVEE and ENAVDD to regulate the LCD Bias Voltage (VEE) and the driver electronics logic voltage (VDD), to provide intelligent power sequencing to the panel. The timing diagram below illustrates the power sequencing cycle.

The 65510 initiates a 'Panel Off' sequence if the PWRDN/ input is asserted low and the chip is programmed to enter 'panel off' mode (by setting extension register XR52 bit-3=1). The 65510 initiates a 'panel on' sequence if PWRDN/ input is high and the chip is programmed to 'panel on' (XR52 bit-3=0). The delay time (T_{PO}) may be adjusted via an extension register (XR5B).



Panel Power Sequencing

FULL COMPATIBILITY

The 65510 is fully compatible with the IBM™ VGA standard at the hardware, register, and BIOS level. The 65510 also provides enhanced backward compatibility to EGA™, CGA™, Hercules™, and MDA™ standards without using NMIs. This controller includes a variety of features to provide compatibility on flat panel displays. Internal compensation techniques ensure that industry-standard software designed for different displays can be executed on the flat panel. Mode initialization is supported at the BIOS and register levels, ensuring compatibility with all application software.

Write Protection

The 65510 has the ability to write protect most of the standard VGA registers. This feature is used to provide backwards compatibility with software written for older generation display types. The write protection is grouped into register sets and controlled by the Write Protect Register (XR15).

Extension Registers

The 65510 employs an "Extension" Register set to control its enhanced features. These Extension Registers provide control of the flat panel interface, flat panel timing, vertical compensation, SMARTMAP™, and Backwards Compatibility. These registers are always accessable as an index/data register set at port addresses 3D6-3D7h. None of the unused bits in the regular VGA registers are used for extensions.

Panel Interface Registers

The Flat Panel Interface characteristics are controlled by a subset of the Extension Registers. These Registers select the panel type, data formatting, panel configuration, panel size, clock selection and video polarity. Since the 65510 is designed to support a wide range of panel types and sizes, the control of these features is fully programmable. **The video polarity of text and graphics modes is independently selectable to allow black text on a white background and still provide normal graphics images.**

Alternate Panel Timing Registers

Flat panel displays usually require sync signal timing that is different from a CRT. To provide full compatibility with the IBM VGA standard, alternate timing registers are used to allow independent timing of the sync signals for flat panel displays. Unlike the values programmed into the standard CRT timing registers, the value programmed into the alternate timing registers is dependent on the panel type used and is independent of the display mode.

Context Switching

For support of multi-tasking, windowing, and context switching, the entire state of the 65510 (internal registers) is readable and writable. This feature is fully compatible with IBM's VGA. Additional registers are provided to allow read back of internal latches not readable in the IBM VGA.

RESET, SETUP, AND TEST MODES

Reset Mode

When this mode is activated by pulling the RESET pin high, the 65510 is forced to VGA-compatible mode and the 65510 is disabled; it must be enabled after deactivating the RESET pin by writing to the Global Enable Register (102h in Setup Mode for PC and MC bus configurations) or to port 3C3h in PI bus or Local Bus configurations). Access to all Extension Registers is always enabled after reset (at 3D6/3D7h). The RESET pin must be active for at least 64 clock cycles.

Setup Mode

In this mode, only the Global Enable register is accessible. In PC bus configurations, setup mode is entered by writing a 1 to bit-4 of port 46E8h. This port is incorporated in the 65510. While in Setup mode, the video output is active if it was active prior to entering Setup mode and inactive if it was inactive prior to entering Setup mode. In MC bus configurations, setup mode may be entered by activating the 65510 SETUP/ pin (typically connected to signals driven by bits in port 94h in MC bus systems). After power up, video BIOS can optionally disable the video 46E8 or 3C3 registers (via XR70) for compatibility in case other non-IBM-compatible peripheral devices use those ports.

Tri-State Mode

In this mode, all output pins of the 65510 chip may be disabled for testing of circuitry external to the chip. The 65510 will enter Tri-State mode if it sees a rising edge on CLK0 during RESET with MD0 and MD8 pins pulled low. The 65510 will exit Tri-State mode with either MD0 or MD8 pin pulled high or RESET low.

ICT (In-Circuit Test) Mode

In this mode, all pins of the 65510 chip may be tested individually to determine if they are properly connected. The 65510 will enter ICT mode if it sees a rising edge on CLKIN during RESET with the MD1 and MD9 pins pulled low. In the ICT mode, all digital signal pins become inputs and are part of a loop starting with P0, and ending with FLM. If all the pins in the path are set high, the FLM output is high. If any of the pins in the path are low, the output at FLM is low. Thus the chip can be checked out by toggling all the pins in the path one at a time (CLKIN last) and observing the effect on the output at FLM. CLKIN must be toggled last as a rising edge on CLKIN with MD1 and MD9 high or RESET low will exit ICT mode. In ICT mode, all pins except FLM are Tri-Stated.

Mode of Operation	RESET Pin	STNDBY/ Pin	Display Memory Access	Video Output
Reset	High	xxx	-----	-----
Setup	-----	-----	No	Yes
Test	-----	-----	No	Yes

Note: Combinations of pin levels not shown in the table above are illegal and should not be used.

CHIP ARCHITECTURE

The 65510 integrates five major internal modules:

Sequencer

The Sequencer generates all CPU and display memory timing. It controls CPU access of display memory by inserting cycles dedicated to CPU access. It also contains mask registers which can prevent writes to individual display memory planes.

CRT Controller

The CRT Controller generates all the sync and timing signals for the display and also generates the multiplexed row and column addresses used for both display refresh and CPU access of display memory.

Graphics Controller

The Graphics Controller interfaces the 8 or 16-bit CPU data bus to the 32-bit internal data bus used by the four planes (Maps) of display memory. It also latches and supplies display memory data to the Attribute Controller for use in refreshing the screen image. For text modes this data is supplied in parallel form (character generator data and attribute code); for graphics modes it is converted to serial form (one bit from each of four bytes form a single pixel). The Graphics Controller can also perform any one of several types of logical operations on data while reading it from or writing it to display memory or the CPU data bus.

Attribute Controller

The Attribute Controller generates the 4-bit-wide video data stream used to refresh the display. This is created in text modes from a font pattern and an attribute code which pass through a parallel to serial conversion. In graphics modes, the display memory contains the 4-bit pixel data. In text and 16 color graphic modes the 4-bit pixel data acts as an index into a set of 16 internal color look-up registers which generate a 6-bit color value. Two additional bits of color data are added to provide an 8-bit address to the VGA color palette. In 256-color modes, two 4-bit values may be passed through the color look-up registers and assembled into one 8-bit video data value. In high-resolution 256-color modes, an 8-bit video data value may be provided directly, bypassing the attribute controller color lookup registers. Text and cursor blink, underline and horizontal scrolling are also the responsibility of the Attribute Controller.

VGA Color Palette

For compatibility, the 65510 contains an internal 256x18 color palette compatible with industry-standard Inmos/Brooktree RAMDACs. All registers in the 03C6-03C9 I/O address range are included on-chip, including the pixel mask register and palette index registers. Since the 65510 does not include CRT support, the DACs normally associated with the RAMDAC are not included in this subsystem.

CONFIGURATION SWITCHES

The 65510 can read up to eight configuration bits. These signals are sampled on memory address bus bits MA0–MA7 on the falling edge of RESET. The 65510 has pull-ups on MA0-MA7 which are enabled during the RESET active period. The status of the configuration bits (MA0-MA7) is read into extension register XR01. The configuration bit may be forced to a zero by using a pull-down resistor value of 1.5K ohms on the appropriate configuration pin (MA0-MA7). The state of MA0 and MA1 on RESET determine EISA/ISA bus (default), MC bus, PI bus, or 386 SX CPU interface. The 65510 provides 4mA drive (default) on the data lines (D0-D15) to the bus which may be programmed to 8mA drive by enabling high drive option with extension register 6C. If higher drive is desired, transceivers may be used in the D0-D15 path and the 65510 provides VGARD signal to control the direction of the transceiver. VGARD may be generated instead of ENAVDD (pin 50 on F65510) by pulling MA3 low. The state of MA4 determines whether clock doubling is enabled. MA2 and MA5-7 are reserved for future use. All eight bits are latched into an extension register on RESET so software may determine the hardware configuration. Also, the reserved bits may optionally be used to read external switches or status bits. **Refer to the description of XR01 for details on the configuration options.**

LIGHT PEN REGISTERS

In the CGA and Hercules modes, the contents of the Display Address counter are saved at the end of the frame before being reset. The saved value can be read in the CRT Controller Register space at indices 10h and 11h. This allows simulation of a light pen hit in CGA and Hercules modes.

BIOS ROM INTERFACE

In typical ISA bus applications, the 65510 is placed on the motherboard and the video BIOS is

integrated with the system BIOS (in local bus, Micro Channel, and PI-bus-based systems, the video BIOS is always included in the system BIOS).

Chips and Technologies, Inc. supplies a video BIOS that is optimized for the 65510 hardware. The BIOS supports the extended functions of the 65510, such as SMARTMAP™, Vertical Compensation, and palette load/save. The BIOS Modification Program (BMP) enables OEMs to tailor their feature set by programming the extended functions. CHIPS offers the BIOS as a standard production version, a customized version, or as source code.

PACKAGE

The 65510 is available in a 100-pin plastic flat pack:

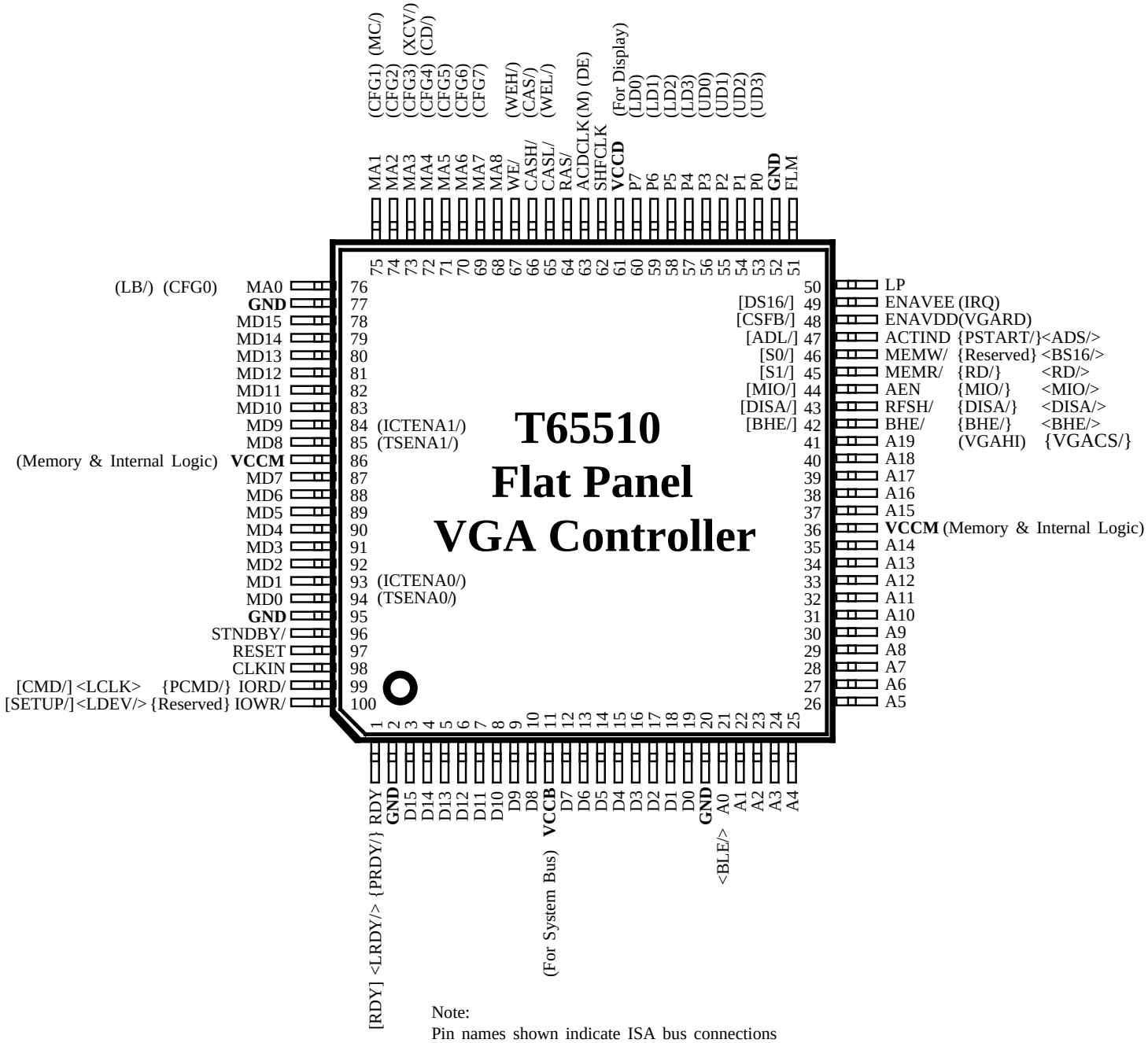
- F65510 - 20 x 14 mm QFP with 0.65 mm (25 mil) lead pitch

In the future, the 65510 will also be offered in a smaller, fine-lead-pitch package:

- T65510 - 14 x 14 mm QFP with 0.50 mm (20 mil) lead pitch

T65510 Pinout (Small QFP)

(Future)



Note:
Pin names shown indicate ISA bus connections
Pin names in brackets {...} indicate PI bus connections
Pin names in braces [...] indicate MC bus connections
Pin names in brackets <...> indicate Local bus connections
Pin names in parentheses (...) indicate alternate function

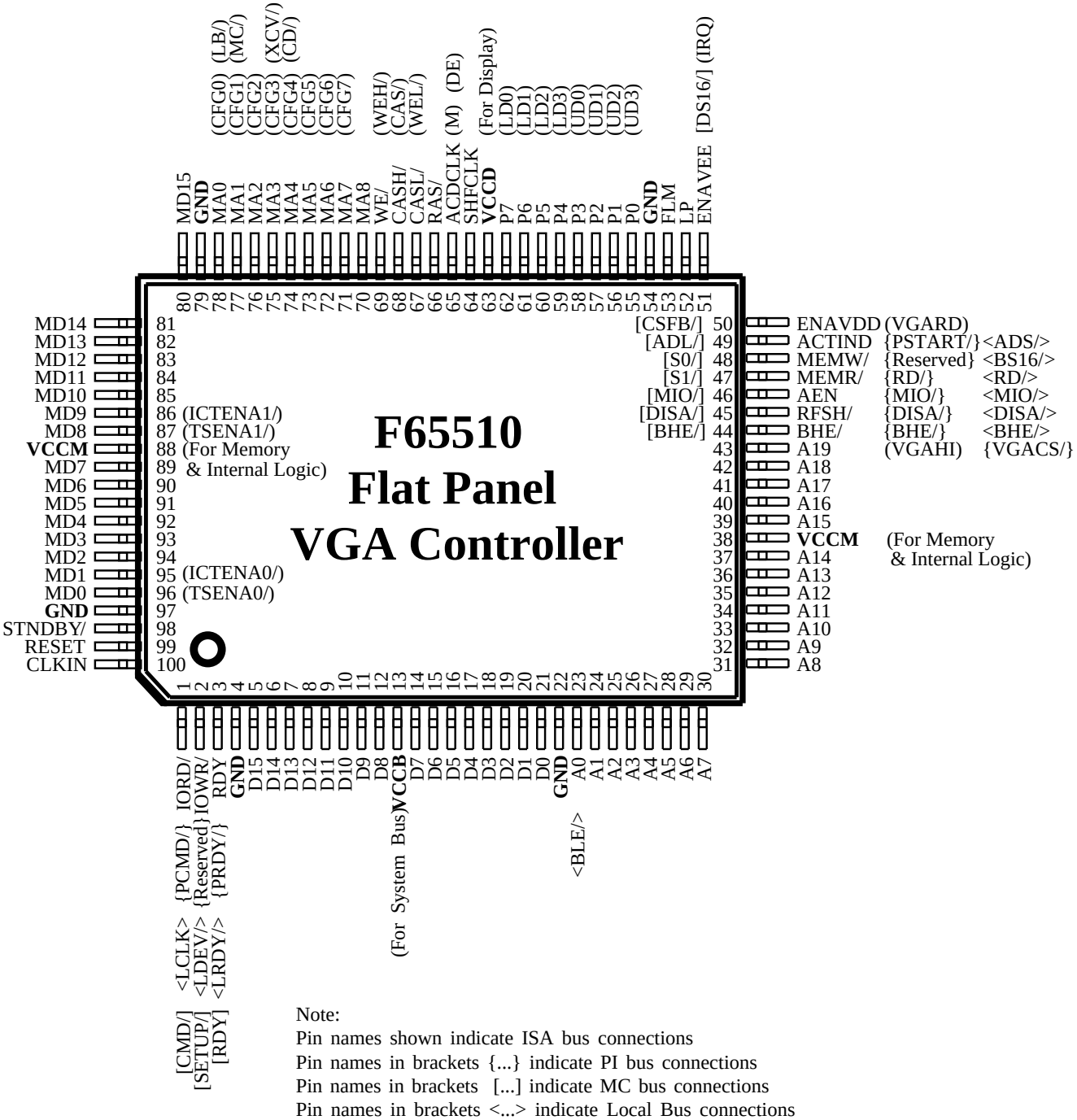
T65510 Pin List

Pin Name				Pin #	Dir	Drive
A00			<BLE/>	21	In	--
A01				22	In	--
A02				23	In	--
A03				24	In	--
A04				25	In	--
A05				26	In	--
A06				27	In	--
A07				28	In	--
A08				29	In	--
A09				30	In	--
A10				31	In	--
A11				32	In	--
A12				33	In	--
A13				34	In	--
A14				35	In	--
A15				37	In	--
A16				38	In	--
A17				39	In	--
A18				40	In	--
A19	(VGAHI)	{VGACS/}		41	In	--
ACDCLK	(M) (DE)			63	Out	4mA
ACTIND	[ADL/]	{PSTART/}	<ADS/>	47	I/O	2mA
AEN	[MIO/]	{MIO/}	<MIO/>	44	In	--
BHE/	[BHE/]	{BHE/}	<BHE/>	42	In	--
CASH/	(CAS/)			65	Out	4mA
CASL/	(WEL/)			66	Out	4mA
CLKIN				98	In	--
D00				19	I/O	4mA
D01				18	I/O	4mA
D02				17	I/O	4mA
D03				16	I/O	4mA
D04				15	I/O	4mA
D05				14	I/O	4mA
D06				13	I/O	4mA
D07				12	I/O	4mA
D08				10	I/O	4mA
D09				9	I/O	4mA
D10				8	I/O	4mA
D11				7	I/O	4mA
D12				6	I/O	4mA
D13				5	I/O	4mA
D14				4	I/O	4mA
D15				3	I/O	4mA
ENAVDD	[CSFB/]	(VGARD)		48	Out	4mA
ENAVEE	[DS16/]	(IRQ)		49	Out	8mA
FLM				51	Out	4mA
GND				2	--	--
GND				20	--	--
GND				52	--	--
GND				77	--	--
GND				95	--	--
IORD/	[CMD/]	{PCMD/}	<LCLK>	99	In	--
IOWR/	[SETUP/]	{Reserved	<LDEV/>	100	In	--
LP				50	Out	4mA
MA0	(CFG0)	(LB/)		76	I/O	2mA
MA1	(CFG1)	(MC/)		75	I/O	2mA
MA2	(CFG2)			74	I/O	2mA
MA3	(CFG3)	(XCV/)		73	I/O	2mA
MA4	(CFG4)	(CD/)		72	I/O	2mA
MA5	(CFG5)			71	I/O	2mA
MA6	(CFG6)			70	I/O	2mA
MA7	(CFG7)			69	I/O	2mA
MA8				68	I/O	2mA

Pin Name				Pin #	Dir	Drive
MD0	(TSENA0/)			94	I/O	2mA
MD1	(ICTENA0/)			93	I/O	2mA
MD2				92	I/O	2mA
MD3				91	I/O	2mA
MD4				90	I/O	2mA
MD5				89	I/O	2mA
MD6				88	I/O	2mA
MD7				87	I/O	2mA
MD8	(TSENA1/)			85	I/O	2mA
MD9	(ICTENA1/)			84	I/O	2mA
MD10				83	I/O	2mA
MD11				82	I/O	2mA
MD12				81	I/O	2mA
MD13				80	I/O	2mA
MD14				79	I/O	2mA
MD15				78	I/O	2mA
MEMR/	[S1/]	{RD/}	<RD/>	45	In	--
MEMW/	[S0/]	{Reserved	<BS16/>	46	In	--
P0	(UD3)			53	Out	4mA
P1	(UD2)			54	Out	4mA
P2	(UD1)			55	Out	4mA
P3	(UD0)			56	Out	4mA
P4	(LD3)			57	Out	4mA
P5	(LD2)			58	Out	4mA
P6	(LD1)			59	Out	4mA
P7	(LD0)			60	Out	4mA
RAS/				64	Out	4mA
RDY	[RDY]	{PRDY/}	<LRDY/>	1	Out	8mA
RESET				97	In	--
RFSH/	[DISA/]	{DISA/}	<DISA/>	43	In	--
SHFCLK				62	Out	4mA
STNDBY/				96	In	--
VCCB				11	--	--
VCCD				61	--	--
VCCM				36	--	--
VCCM				86	--	--
WE/	(WEH/)			67	Out	2mA

(1X/)				See MA2
(CAS/)				See CASL/
(CFG0-7)				See MA0-7
(ICTENA0/)				See MD1
(ICTENA1/)				See MD9
(LD3-LD0)				See P4-7
(LB/)				See MA0
(M)	(DE)			See ACDCLK
(MC/)				See MA1
(TSENA0/)				See MD0
(TSENA1/)				See MD8
(UD3-UD0)				See P0-3
(VGAHI)	{VGACS/}			See A19
(WEH/)				See CASH/
(WEL/)				See WE/
(XCV/)				See MA3
[ADL/]	{PSTART/}	<ADS/>		See ERMEN/
[BHE/]	{BHE/}	<BHE/>		See BHE/
		<BLE/>		See A0
[CMD/]	{PCMD/}	<LCLK>		See IORD/
[CSFB/]			(VGARD)	See ENAVDD
[DISA/]	{DISA/}	<DISA/>		See RFSH/
[DS16/]			(IRQ)	See ENAVEE
[MIO/]	{MIO/}	<MIO/>		See AEN
[RDY]	{PRDY/}	<LRDY/>		See RDY
[S0/]		<BS16/>		See MEMW/
[S1/]	{RD/}	<RD/>		See MEMR/
[SETUP/]		<LDEV/>		See IOWR/

F65510 Pinout (Standard QFP)



Note:
Pin names shown indicate ISA bus connections
Pin names in brackets {...} indicate PI bus connections
Pin names in brackets [...] indicate MC bus connections
Pin names in brackets <...> indicate Local Bus connections

F65510 Pin List

Pin Name				Pin #	Dir	Drive
A00			<BLE/>	23	In	--
A01				24	In	--
A02				25	In	--
A03				26	In	--
A04				27	In	--
A05				28	In	--
A06				29	In	--
A07				30	In	--
A08				31	In	--
A09				32	In	--
A10				33	In	--
A11				34	In	--
A12				35	In	--
A13				36	In	--
A14				37	In	--
A15				39	In	--
A16				40	In	--
A17				41	In	--
A18				42	In	--
A19	(VGAHI)	{VGACS/}		43	In	--
ACDCLK	(M) (DE)			65	Out	4mA
ACTIND	[ADL/]	{PSTART/}	<ADS/>	49	I/O	2mA
AEN	[MIO/]	{MIO/}	<MIO/>	46	In	--
BHE/	[BHE/]	{BHE/}	<BHE/>	44	In	--
CASH/	(CAS/)			67	Out	4mA
CASL/	(WEL/)			68	Out	4mA
CLKIN				100	In	--
D00				21	I/O	4mA
D01				20	I/O	4mA
D02				19	I/O	4mA
D03				18	I/O	4mA
D04				17	I/O	4mA
D05				16	I/O	4mA
D06				15	I/O	4mA
D07				14	I/O	4mA
D08				12	I/O	4mA
D09				11	I/O	4mA
D10				10	I/O	4mA
D11				9	I/O	4mA
D12				8	I/O	4mA
D13				7	I/O	4mA
D14				6	I/O	4mA
D15				5	I/O	4mA
ENAVDD	[CSFB/]		(VGARD)	50	Out	4mA
ENAVEE	[DS16/]		(IRQ)	51	Out	8mA
FLM				53	Out	4mA
GND				4	--	--
GND				22	--	--
GND				54	--	--
GND				79	--	--
GND				97	--	--
IORD/	[CMD/]	{PCMD/}	<LCLK>	1	In	--
IOWR/	[SETUP/]	{Reserved	<LDEV/>	2	In	--
LP				52	Out	4mA
MA0	(CFG0)	(LB/)		78	I/O	2mA
MA1	(CFG1)	(MC/)		77	I/O	2mA
MA2	(CFG2)			76	I/O	2mA
MA3	(CFG3)	(XCV/)		75	I/O	2mA
MA4	(CFG4)	(CD/)		74	I/O	2mA
MA5	(CFG5)			73	I/O	2mA
MA6	(CFG6)			72	I/O	2mA
MA7	(CFG7)			71	I/O	2mA
MA8				70	I/O	2mA

Pin Name				Pin #	Dir	Drive
MD0	(TSENA0/)			96	I/O	2mA
MD1	(ICTENA0/)			95	I/O	2mA
MD2				94	I/O	2mA
MD3				93	I/O	2mA
MD4				92	I/O	2mA
MD5				91	I/O	2mA
MD6				90	I/O	2mA
MD7				89	I/O	2mA
MD8	(TSENA1/)			87	I/O	2mA
MD9	(ICTENA1/)			86	I/O	2mA
MD10				85	I/O	2mA
MD11				84	I/O	2mA
MD12				83	I/O	2mA
MD13				82	I/O	2mA
MD14				81	I/O	2mA
MD15				80	I/O	2mA
MEMR/	[S1/]	{RD/}	<RD/>	47	In	--
MEMW/	[S0/]	{Reserved	<BS16/>	48	In	--
P0	(UD3)			55	Out	4mA
P1	(UD2)			56	Out	4mA
P2	(UD1)			57	Out	4mA
P3	(UD0)			58	Out	4mA
P4	(LD3)			59	Out	4mA
P5	(LD2)			60	Out	4mA
P6	(LD1)			61	Out	4mA
P7	(LD0)			62	Out	4mA
RAS/				66	Out	4mA
RDY	[RDY]	{PRDY/}	<LRDY/>	3	Out	8mA
RESET				99	In	--
RFSH/	[DISA/]	{DISA/}	<DISA/>	45	In	--
SHFCLK				64	Out	4mA
STNDBY/				98	In	--
VCCB				13	--	--
VCCD				63	--	--
VCCM				38	--	--
VCCM				88	--	--
WE/	(WEH/)			69	Out	2mA

(1X/)				See MA2
(CAS/)				See CASL/
(CFG0-7)				See MA0-7
(ICTENA0/)				See MD1
(ICTENA1/)				See MD9
(LD3-LD0)				See P4-7
(LB/)				See MA0
(M)	(DE)			See ACDCLK
(MC/)				See MA1
(TSENA0/)				See MD0
(TSENA1/)				See MD8
(UD3-UD0)				See P0-3
(VGAHI)	{VGACS/}			See A19
(WEH/)				See CASH/
(WEL/)				See WE/
(XCV/)				See MA3
[ADL/]	{PSTART/}	<ADS/>		See ERMEN/
[BHE/]	{BHE/}	<BHE/>		See BHE/
		<BLE/>		See A0
[CMD/]	{PCMD/}	<LCLK>		See IORD/
[CSFB/]			(VGARD)	See ENAVDD
[DISA/]	{DISA/}	<DISA/>		See RFSH/
[DS16/]			(IRQ)	See ENAVEE
[MIO/]	{MIO/}	<MIO/>		See AEN
[RDY]	{PRDY/}	<LRDY/>		See RDY
[S0/]		<BS16/>		See MEMW/
[S1/]	{RD/}	<RD/>		See MEMR/
[SETUP/]		<LDEV/>		See IOWR/

PIN DESCRIPTIONS

System Bus Interface

T Pin #	F Pin #	Pin Name		Type	Active	Description
						System Data Bus
19	21	D0		I/O	High	
18	20	D1		I/O	High	
17	19	D2		I/O	High	
16	18	D3		I/O	High	
15	17	D4		I/O	High	
14	16	D5		I/O	High	
13	15	D6		I/O	High	
12	14	D7		I/O	High	
10	12	D8		I/O	High	
9	11	D9		I/O	High	
8	10	D10		I/O	High	
7	9	D11		I/O	High	
6	8	D12		I/O	High	
5	7	D13		I/O	High	
4	6	D14		I/O	High	
3	5	D15		I/O	High	
						System Address Bus
21	23	A0	<BLE/>	In	High	
22	24	A1		In	High	
23	25	A2		In	High	
24	26	A3		In	High	
25	27	A4		In	High	
26	28	A5		In	High	
27	29	A6		In	High	
28	30	A7		In	High	
29	31	A8		In	High	
30	32	A9		In	High	
31	33	A10		In	High	
32	34	A11		In	High	
33	35	A12		In	High	
34	36	A13		In	High	
35	37	A14		In	High	
37	39	A15		In	High	
38	40	A16		In	High	
39	41	A17		In	High	
40	42	A18		In	High	
41	43	A19	(VGAHI)	In	High	When the Linear Addressing Register has a non-zero value, this input serves as an active high Chip Select for ISA/EISA bus operation (or active low Chip Select for PI bus) to access memory beyond the 1M address range (A0-18 are used to uniquely address each of the 512K bytes in display memory).
			{VGACS/}	In	Low	
97	99	RESET		In	High	Reset. Connect directly to ISA bus reset. Configuration inputs are sampled on the falling edge. Must be synchronous to LCLK in local bus interface mode. Typically, ISA bus reset is synchronized to the CPU clock by the core logic chipset.

Note: Pin names in parentheses (...) indicate alternate functions
Pin names in brackets [...] indicate MC bus functionality if different from EISA/ISA (PC/AT) bus
Pin names in braces {...} indicate PI bus functionality if different from EISA/ISA (PC/AT) bus
Pin names in brackets <...> indicate 386 SX/DX Local bus functionality if different from EISA/ISA bus

PIN DESCRIPTIONS **System Bus Interface (continued)**

T Pin #	F Pin #	Pin Name	Type	Active	Description
43	45	RFSH/ {DISA/} [DISA/] <DISA/>	In In In In	Low Low Low Low	This pin is an active low signal indicating a Refresh cycle for the EISA/ISA bus. In MC, PI, and Local bus systems, it is connected to the disable signal from system port 102h or tied high. When this pin is low, display memory is not accessible.
42	44	BHE/ {BHE/} [BHE/] <BHE/>	In In In In	Low Low Low Low	Byte High Enable. BHE/ low indicates the high order byte at the current word address is being accessed.
44	46	AEN {MIO/} [MIO/] <MIO/>	In In In In	High Both Both Both	In EISA/ISA interface, defines valid I/O address: 0 = valid I/O address, 1 = Invalid I/O address (latched internally). In MC, PI, and Local bus interfaces, indicates memory or I/O cycle: 1 = memory, 0 = I/O.
47	49	ACTIND {PSTART/} [ADL/] <ADS/>	Out In In In	High Low Low Low	CPU Activity Indicator (EISA/ISA Bus), Address Latch (MC Bus), Start (PI bus), or Address Strobe (Local Bus). Effectively indicates the start of a bus cycle in MC, PI, and Local Buses.
99	1	IORD/ {CMD/} [PCMD/] <LCLK>	In In In In	Low Low Low High	In EISA/ISA interface, indicates an I/O Read Cycle. In MC and PI bus interfaces, indicates the beginning of the command part of a bus cycle. Driven by CMD/ on the MC bus. This input is a 2x CPU Clock in Local Bus interface mode.
100	2	IOWR/ {Reserved} [SETUP/] <LDEV/>	In In In Out	Low Low Low Low	In EISA/ISA interface, indicates an I/O Write Cycle. In MC bus systems, indicates that all on-chip memory and I/O functions should be disabled. In Local bus, this pin is an output to indicate local bus cycle response.
45	47	MEMR/ {RD/} [S1/] <RD/>	In In In	Low Low Low	In the EISA/ISA bus, indicates a Memory Read cycle. In MC interface, indicates Status 1. In PI and Local bus, indicates read (low) or write (high) bus cycle.
46	48	MEMW/ {Reserved} [S0/] <BS16/>	In In In Out	Low Low Low Low	In EISA/ISA bus, indicates a Memory Write cycle. In MC, indicates Status 0. In PI, this input is ignored. In Local Bus, this pin is BS16/ (Bus Size 16-Bit). S1/ S0/ Operation 0 0 Undefined 0 1 Read 1 0 Write 1 1 Undefined
1	3	RDY {PRDY/} [RDY] <LRDY/>	Out Out Out Out	High Low High Low	Ready. Driven low during EISA/ISA/MC bus cycles to indicate that the current cycle should be extended with wait states. Driven low during PI/LB cycles to indicate the current cycle should be completed. This signal is driven high at the end of the cycle, then tristated.

Note: Pin names in parentheses (...) indicate alternate functions
Pin names in brackets [...] indicate MC bus functionality if different from EISA/ISA (PC/AT) bus
Pin names in braces {...} indicate PI bus functionality if different from EISA/ISA (PC/AT) bus
Pin names in brackets <...> indicate 386 SX/DX Local bus functionality if different from EISA/ISA bus

PIN DESCRIPTIONS — Display Memory Interface

T Pin #	F Pin #	Pin Name			Type	Active	Description
76	78	MA0	(CFG0)	(LB/)	Out	High	DRAM address bus
75	77	MA1	(CFG1)	(MC/)	Out	High	
74	76	MA2	(CFG2)		Out	High	
73	75	MA3	(CFG3)	(XCV/)	Out	High	
72	74	MA4	(CFG4)	(CD/)	Out	High	
71	73	MA5	(CFG5)		Out	High	
70	72	MA6	(CFG6)		Out	High	
69	71	MA7	(CFG7)		Out	High	XCV/ = 0: ENAVDD becomes VGARD
68	70	MA8			Out	High	CD/=0: Enable Clock Doubling
64	66	RAS/			Out	Low	Row address strobe
65	67	CASL/	(WEL/)		Out	Low	Column address strobe for lower byte
66	68	CASH/	(CAS/)		Out	Low	Column address strobe for upper byte
67	69	WE/	(WEH/)		Out	Low	Write enable
94	96	MD0	(TSENA0/)		I/O	High	DRAM data bus
93	95	MD1	(ICTENA0/)		I/O	High	
92	94	MD2			I/O	High	
91	93	MD3			I/O	High	
90	92	MD4			I/O	High	
89	91	MD5			I/O	High	
88	90	MD6			I/O	High	
87	89	MD7			I/O	High	
85	87	MD8	(TSENA1/)		I/O	High	
84	86	MD9	(ICTENA1/)		I/O	High	
83	85	MD10			I/O	High	
82	84	MD11			I/O	High	
81	83	MD12			I/O	High	
80	82	MD13			I/O	High	
79	81	MD14			I/O	High	
78	80	MD15			I/O	High	

MC/	LB/	System Bus Configuration
1	1	ISA Bus
1	0	Local Bus
0	1	Micro Channel
0	0	PI Bus

If ICTENA0/ and ICTENA1/ are low with RESET high, a rising edge on CLKIN will put the chip into In Circuit Test' mode. In ICT mode, all digital signal pins become inputs which are part of a long path starting at P0 (pin 55) and proceeding to higher pin numbers around the chip to pin 100 then to pin 1 and ending at FLM (pin 53). If all pins in the path are high, the FLM output will be high. If any pin is low, the FLM output will be low. Thus the chip can be checked in circuit to determine if all pins are connected properly by toggling all pins one at a time (CLKIN last) and observing the effect on FLM. CLKIN must be toggled last because rising edges on CLKIN with ICTENA0/ or 1/ high or RESET low will exit ICT mode. As a side effect, ICT mode effectively 3-states all pins except FLM.

If TSENA0/ and TSENA1/ are low with RESET high, a rising edge on CLKIN will 3-state all pins. A CLKIN rising edge without the enabling conditions exits 3-state.

Note: Pin names in parentheses (...) indicate alternate functions
Pin names in brackets [...] indicate MC bus functionality if different from EISA/ISA (PC/AT) bus
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Pin names in brackets <...> indicate 386 SX/DX Local bus functionality if different from EISA/ISA bus

PIN DESCRIPTIONS

Panel Interface

T Pin #	F Pin #	Pin Name		Type	Active	Description
60	62	P7	(LD0)	Out	High	8-bit flat panel data output
59	61	P6	(LD1)	Out	High	
58	60	P5	(LD2)	Out	High	
57	59	P4	(LD3)	Out	High	
56	58	P3	(UD0)	Out	High	
55	57	P2	(UD1)	Out	High	
54	56	P1	(UD2)	Out	High	
53	55	P0	(UD3)	Out	High	
51	53	FLM		Out	High	First Line Marker. Flat Panel equivalent of VSYNC.
50	52	LP		Out	High	Latch Pulse. Flat Panel equivalent of HSYNC.
62	64	SHFCLK		Out	High	Shift Clock. Pixel clock for panel data outputs.
63	65	ACDCLK		Out	High	ACD Clock or Display Enable signal for flat panels
		(M)		Out	High	
		(DE)		Out	High	
48	50	ENAVDD		Out	High	Panel Power Control (active high) or Card Select Feedback (active low) when configured for Micro Channel bus interface.
		(VGARD)		Out	High	
		[CSFB/]		Out	Low	
49	51	ENAVEE		Out	High	Panel Power Control (active high) or Data Select 16 (active low) when configured for Micro Channel bus interface. Except in Micro Channel, may optionally be configured as an output for vertical sync interrupts (selectable as either active high or active low).
		(IRQ)		Out	Both	
		[DS16/]		Out	Low	

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Pin names in brackets <...> indicate 386 SX/DX Local bus functionality if different from EISA/ISA bus

PIN DESCRIPTIONS **Clock, Power, and Ground**

T Pin #	F Pin #	Pin Name	Type	Active	Description
98	100	CLKIN	In	High	Single clock input serves as both memory clock (MCLK) and dot (pixel) clock (DCLK). This input is internally rate multiplied to generate a range of dot clock frequencies. This input may be 14.31818 MHz if the clock doubling (CD/) configuration bit is asserted low on RESET, otherwise this input is typically connected to the CPU clock (25-50 MHz).
96	98	STNDBY/	In	Low	Standby mode entry and exit pin
11	13	VCCB	Power	--	Power input (System Bus Interface)
36	38	VCCM	Power	--	Power input (Memory Interface & Internal Logic)
61	63	VCCD	Power	--	Power input (Display Interface)
86	88	VCCM	Power	--	Power input (Memory Interface & Internal Logic)
2	4	GND	Ground	--	Ground input
20	22	GND	Ground	--	Ground input
52	54	GND	Ground	--	Ground input
77	79	GND	Ground	--	Ground input
95	97	GND	Ground	--	Ground input

Note: Pin names in parentheses (...) indicate alternate functions
Pin names in brackets [...] indicate MC bus functionality if different from EISA/ISA (PC/AT) bus
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Pin names in brackets <...> indicate 386 SX/DX Local bus functionality if different from EISA/ISA bus

I/O Map

Port Address	Read	Write
102	Global Enable (ISA/MC)	Global Enable (ISA/MC)
3B0	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B1	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B2	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B3	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B4	CRTC Index	CRTC Index
3B5	CRTC Data	CRTC Data
3B6	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B7	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B8	Hercules Mode Register (MODE)	Hercules Mode Register (MODE)
3B9	--	Set Light Pen FF (ignored)
3BA	Status Register (STAT)	Feature Control Register (FCR)
3BB	--	Clear Light Pen FF (ignored)
3BC	Reserved for system parallel port	
3BD		
3BE		
3BF	Hercules Configuration Register (HCFG)	Hercules Configuration Register (HCFG)
3C0	Attribute Controller Index / Data	Attribute Controller Index / Data
3C1	Attribute Controller Index / Data	Attribute Controller Index / Data
3C2	Feature Read Register (FCR)	Miscellaneous Output Register (MSR)
3C3	Video Subsystem Enable (VSE)(MC/PI/LB)	Video Subsystem Enable (VSE)(MC/PI/LB)
3C4	Sequencer Index	Sequencer Index
3C5	Sequencer Data	Sequencer Data
3C6, 83C6	Color Palette Mask	Color Palette Mask
3C7, 83C7	Color Palette State	Color Palette Read Mode Index
3C8, 83C8	Color Palette Write Mode Index	Color Palette Write Mode Index
3C9, 83C9	Color Palette Data	Color Palette Data
3CA	Feature Read Register (FEAT)	--
3CB	--	--
3CC	Miscellaneous Output Register (MSR)	--
3CD	--	--
3CE	Graphics Controller Index	Graphics Controller Index
3CF	Graphics Controller Data	Graphics Controller Data
3D0	--	--
3D1	--	--
3D2	--	--
3D3	--	--
3D4	CRTC Index	CRTC Index
3D5	CRTC Data	CRTC Data
3D6	CHIPS™ Extensions Index	CHIPS™ Extensions Index
3D7	CHIPS™ Extensions Data	CHIPS™ Extensions Data
3D8	CGA Mode Register (MODE)	CGA Mode Register (MODE)
3D9	CGA Color Register (COLOR)	CGA Color Register (COLOR)
3DA	Status Register (STAT)	Feature Control Register (FCR)
3DB	--	Clear Light Pen FF (ignored)
3DC	--	Set Light Pen FF (ignored)
46E8	--	Setup Control (ISA bus only)

Mono Mode

Color Mode

REGISTER SUMMARY - CGA, MDA, AND HERCULES MODEs

Register	Register Name	Bits	Access	I/O Port - MDA/Herc	I/O Port - CGA	Comment
ST00 (STAT)	Display Status	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
MODE	CGA/MDA/Hercules Mode Control	7	RW	3B8	3D8	
COLOR	CGA Color Select	6	RW	n/a	3D9	
HCFG	Hercules Configuration	2	W	3BF	n/a	
			R	3D6-3D7 index 14	n/a	XR14
RX, R0-11	'6845' Registers	0-8	RW	3B4-3B5	3D4-3D5	
XRX, XR0-7F	Extension Registers	0-8	RW	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - EGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
MSR	Miscellaneous Output	7	W	3C2	3C2	
FCR	Feature Control	3	W	3BA	3DA	
ST00 (FEAT)	Feature Read (Input Status 0)	4	R	3C2	3C2	
ST01 (STAT)	Display Status (Input Status 1)	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
SRX, SR0-7	Sequencer	0-8	RW	3C4-3C5	3C4-3C5	
CRX, CR0-3F	CRT Controller	0-8	RW	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	RW	3CE-3CF	3CE-3CF	
ARX, AR0-14	Attributes Controller	0-8	RW	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	RW	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - VGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
VSE	Video Subsystem Enable	1	RW	3C3 if MC/PI/LB	3C3 if MC/PI/LB	Disabled by XR70 bit-6
SETUP	Setup Control	2	W	46E8 if ISA	46E8 if ISA	Disabled by XR70 bit-7
ENABLE	Global Enable	1	RW	102 if ISA/MC	102 if ISA/MC	Setup Only
MSR	Miscellaneous Output	7	W	3C2	3C2	
			R	3CC	3CC	
FCR	Feature Control	3	W	3BA	3DA	
			R	3CA	3CA	
ST00 (FEAT)	Feature Read (Input Status 0)	4	R	3C2	3C2	
ST01 (STAT)	Display Status (Input Status 1)	6	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
DACMASK	Color Palette Pixel Mask	8	RW	3C6, 83C6	3C6, 83C6	
DACSTATE	Color Palette State	2	R	3C7, 83C7	3C7, 83C7	
DACRX	Color Palette Read-Mode Index	8	W	3C7, 83C7	3C7, 83C7	
DACWX	Color Palette Write-Mode Index	8	RW	3C8, 83C8	3C8, 83C8	
DACDATA	Color Palette Data 0-FF	3x6 or 3x8	RW	3C9, 83C9	3C9, 83C9	
SRX, SR0-7	Sequencer	0-8	RW	3C4-3C5	3C4-3C5	
CRX, CR0-3F	CRT Controller	0-8	RW	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	RW	3CE-3CF	3CE-3CF	
ARX, AR0-14	Attributes Controller	0-8	RW	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	RW	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - INDEXED REGISTERS (VGA)

Register	Register Name	Bits	Register Type	Access (VGA)	Access (EGA)	I/O Port
SRX	Sequencer Index	3	VGA/EGA	RW	RW	3C4
SR0	Reset	2	VGA/EGA	RW	RW	3C5
SR1	Clocking Mode	6	VGA/EGA	RW	RW	3C5
SR2	Plane Mask	4	VGA/EGA	RW	RW	3C5
SR3	Character Map Select	6	VGA/EGA	RW	RW	3C5
SR4	Memory Mode	3	VGA/EGA	RW	RW	3C5
SR7	Reset Horizontal Character Counter	0	VGA	W	n/a	3C5
CRX	CRTC Index	6	VGA/EGA	RW	RW	3B4 Mono, 3D4 Color
CR0	Horizontal Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR1	Horizontal Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR2	Horizontal Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR3	Horizontal Blanking End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR4	Horizontal Retrace Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR5	Horizontal Retrace End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR6	Vertical Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR7	Overflow	5	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR8	Preset Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR9	Character Cell Height	5+3	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRA	Cursor Start	5+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRB	Cursor End	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRC	Start Address High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRD	Start Address Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRE	Cursor Location High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRF	Cursor Location Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
LPENH	Light Pen High	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
LPENL	Light Pen Low	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
CR10	Vertical Retrace Start	8	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR11	Vertical Retrace End	4+4	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR12	Vertical Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR13	Offset	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR14	Underline Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR15	Vertical Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR16	Vertical Blanking End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR17	CRT Mode Control	7	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR18	Line Compare	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR22	Graphics Controller Data Latches	8	VGA	R	n/a	3B5 Mono, 3D5 Color
CR24	Attribute Controller Index/Data Latc	1	VGA	R	n/a	3B5 Mono, 3D5 Color
CR3x	Clear Vertical Display Enable FF	0	VGA	W	n/a	3B5 Mono, 3D5 Color
GRX	Graphics Controller Index	4	VGA/EGA	RW	RW	3CE
GR0	Set/Reset	4	VGA/EGA	RW	RW	3CF
GR1	Enable Set/Reset	4	VGA/EGA	RW	RW	3CF
GR2	Color Compare	4	VGA/EGA	RW	RW	3CF
GR3	Data Rotate	5	VGA/EGA	RW	RW	3CF
GR4	Read Map Select	2	VGA/EGA	RW	RW	3CF
GR5	Mode	6	VGA/EGA	RW	RW	3CF
GR6	Miscellaneous	4	VGA/EGA	RW	RW	3CF
GR7	Color Don't Care	4	VGA/EGA	RW	RW	3CF
GR8	Bit Mask	8	VGA/EGA	RW	RW	3CF
ARX	Attribute Controller Index	6	VGA/EGA	RW	RW	3C0 (3C1)
AR0-F	Internal Palette Regs 0-15	6	VGA/EGA	RW	RW	3C0 (3C1)
AR10	Mode Control	7	VGA/EGA	RW	RW	3C0 (3C1)
AR11	Overscan Color	6	VGA/EGA	RW	RW	3C0 (3C1)
AR12	Color Plane Enable	6	VGA/EGA	RW	RW	3C0 (3C1)
AR13	Horizontal Pixel Panning	4	VGA/EGA	RW	RW	3C0 (3C1)
AR14	Color Select	4	VGA	RW	n/a	3C0 (3C1)

EXTENSION REGISTER SUMMARY: 00-2F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family								
						450	451	452	453	455	456	457	65520	65530
XRX	**Extension Index Register**	7	R/W	3B6/3D6	- x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR00	**Chip Version**	8	R/O	3B7/3D7	1 0 0 1 r r r r	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR01	**Configuration**	8	R/O	3B7/3D7	d d d d d d d d	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR02	**CPU Interface Control**	5	R/W	3B7/3D7	0 - 0 0 0 - 0 -	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR03	-reserved- *(ROM Interface)*	--	--	3B7/3D7		.	✓	✓	✓	.	.	✓	.	.
XR04	**Memory Control**	3	R/W	3B7/3D7	- - 0 0 - 0 - -	✓	✓	✓	.	✓	✓	✓	✓	✓
XR05	-reserved- *(Clock Control)*	--	--	3B7/3D7		.	.	✓	✓	.	.	✓	.	.
XR06	**Color Palette Control** *(DRAM Intfc)*	3	R/W	3B7/3D7	0 0 0 - - - - -	.	.	✓	.	.	.	.	✓	✓
XR07	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR08	-reserved- *(Gen Purp Output Select B)*	--	--	3B7/3D7		.	✓	✓	.	✓	✓	✓	.	.
XR09	-reserved- *(Gen Purp Output Select A)*	--	--	3B7/3D7		.	✓	✓	.	✓	✓	✓	.	.
XR0A	-reserved- *(Cursor Address Top)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR0B	**CPU Paging**	4	R/W	3B7/3D7	- - - 0 - 0 0 0	✓	.	✓	✓	✓	✓	✓	✓	✓
XR0C	**Start Address Top**	1	R/W	3B7/3D7	- - - - - - - 0	✓	.	✓	✓	.	.	.	✓	✓
XR0D	**Auxiliary Offset**	2	R/W	3B7/3D7	- - - - - - 0 0	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR0E	**Text Mode Control**	2	R/W	3B7/3D7	- - - - 0 0 - -	✓	.	✓	.	.	.	.	✓	✓
XR0F	**Software Flags 2**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	.	.	.	✓	✓
XR10	**Single/Low Map Register**	8	R/W	3B7/3D7	x x x x x x x x	✓	.	✓	✓	.	.	.	✓	✓
XR11	**High Map Register**	8	R/W	3B7/3D7	x x x x x x x x	✓	.	✓	✓	.	.	.	✓	✓
XR12	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR13	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR14	**Emulation Mode**	8	R/W	3B7/3D7	0 0 0 0 h h 0 0	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR15	**Write Protect**	8	R/W	3B7/3D7	0 0 0 0 0 0 0 0	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR16	-reserved- *(Trap Enable)*	--	--	3B7/3D7		.	✓	✓	✓	✓	✓	✓	.	.
XR17	-reserved- *(Trap Status)*	--	--	3B7/3D7		.	✓	✓	✓	✓	✓	✓	.	.
XR18	**Alternate H Disp End**	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR19	**Alternate H Sync Start / Half-line**	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1A	**Alternate H Sync End**	5	R/W	3B7/3D7	- - - x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1B	**Alternate H Total**	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1C	**Alternate H Blank Start / H Panel S**	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1D	**Alternate H Blank End**	2	R/W	3B7/3D7	- x x - - - - -	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1E	**Alternate Offset**	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1F	**Virtual EGA Switch Register**	5	R/W	3B7/3D7	0 - - - x x x x	✓	.	.	.	.	.	.	✓	✓
XR20	-reserved- *(453 Interface II)/(SUD)*	--	--	3B7/3D7		.	.	✓	✓	.	.	.	.	.
XR21	-reserved- *(Sliding Hold A)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR22	-reserved- *(Sliding Hold B)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR23	-reserved- *(SHC)/(WBM Ctrl)*	--	--	3B7/3D7		.	.	✓	✓	.	.	.	.	.
XR24	**FP AltMaxScanline** *(SHD)/(WBM Pat*	5	R/W	3B7/3D7	- - - x x x x x	.	.	✓	✓	.	.	.	✓	✓
XR25	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR26	-reserved- *(453 Config)*	--	--	3B7/3D7		.	.	.	✓	.	.	.	.	.
XR27	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR28	**Video Interface**	3	R/W	3B7/3D7	- 0 - 0 - 0 - -	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR29	-reserved- *(Function Control)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR2A	-reserved- *(Frame Intrpt Count)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR2B	**Default Video**	8	R/W	3B7/3D7	0 0 0 0 0 0 0 0	✓	✓	✓	.	✓	✓	✓	✓	✓
XR2C	**FP Vsync (FLM) Delay** *(Force H High*	8	R/W	3B7/3D7	x x x x x x x x	.	.	✓	.	.	.	.	✓	✓
XR2D	**FP Hsync (LP) Delay** *(Force H Low*	8	R/W	3B7/3D7	x x x x x x x x	.	.	✓	.	.	.	.	✓	✓
XR2E	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR2F	**FP Hsync (LP) Width** *(Force V Low)*	7	R/W	3B7/3D7	x x x - x x x x	.	.	✓	.	.	.	.	✓	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
– = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 450–453 VGAs drive CRTs only, 455–457 & 655x0 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

EXTENSION REGISTER SUMMARY: 30-5F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family								
						450	451	452	453	455	456	457	65520	65530
XR30	*(Graphics Cursor Start Address High)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR31	*(Graphics Cursor Start Address Low)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR32	*(Graphics Cursor End Address)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR33	*(Graphics Cursor X Position High)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR34	*(Graphics Cursor X Position Low)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR35	*(Graphics Cursor Y Position High)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR36	*(Graphics Cursor Y Position Low)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR37	*(Graphics Cursor Mode)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR38	*(Graphics Cursor Mask)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR39	*(Graphics Cursor Color 0)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR3A	*(Graphics Cursor Color 1)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR3B	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR3C	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR3D	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR3E	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR3F	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR40	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR41	-reserved- *(Virtual EGA Switch Reg)*	--	--	3B7/3D7		.	.	.	✓	.	.	.	.	.
XR42	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR43	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR44	**Software Flag Register**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	✓	.	.	.	✓	✓
XR45	-reserved- *(S/W Flag 2 / FG Color)*	--	--	3B7/3D7		.	.	.	✓	.	.	.	.	.
XR46	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR47	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR48	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR49	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR4A	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR4B	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR4C	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR4D	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR4E	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR4F	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR50	**Panel Format**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓	✓	✓
XR51	**Display Type**	7	R/W	3B7/3D7	x x x x - 0 x x	.	.	.	.	✓	✓	✓	✓	✓
XR52	**Power Down Control** *(Panel Size)*	6	R/W	3B7/3D7	0 - 0 - 0 0 0 0	.	.	.	.	✓	✓	✓	✓	✓
XR53	**Line Graphics Override**	3	R/W	3B7/3D7	- 0 - - x x - -	.	.	.	.	✓	✓	✓	✓	✓
XR54	**FP Interface** *(Alternate Misc Output)*	7	R/W	3B7/3D7	x x - x x x x x	.	.	.	.	✓	✓	✓	✓	✓
XR55	**H Compensation** *(Text 350_A Comp)*	5	R/W	3B7/3D7	- x x - - x x x	.	.	.	.	✓	✓	✓	✓	✓
XR56	**H Centering** *(Text 350_B Comp)*	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓	✓	✓
XR57	**V Compensation** *(Text 400 Comp)*	7	R/W	3B7/3D7	- x x x x x x x	.	.	.	.	✓	✓	✓	✓	✓
XR58	**V Centering** *(Graphics 350 Comp*	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓	✓	✓
XR59	**V Line Insertion** *(Graphics 400 Comp*	6	R/W	3B7/3D7	- x x - x x x x	.	.	.	.	✓	✓	✓	✓	✓
XR5A	**V Line Replication** *(FP VDisp St 400)*	4	R/W	3B7/3D7	- - - - x x x x	.	.	.	.	✓	✓	✓	✓	✓
XR5B	**Power Sequencing Delay** *(VD End 4(*	8	R/W	3B7/3D7	0 1 1 1 0 0 0 1	.	.	.	.	✓	✓	✓	.	✓
XR5C	-reserved- *(Weight Control Clock A)*	--	--	3B7/3D7		.	.	.	.	✓	✓	.	.	.
XR5D	-reserved- *(Weight Control Clock B)*	--	--	3B7/3D7		.	.	.	.	✓	✓	.	.	.
XR5E	**ACDCLK Control**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓	✓	✓
XR5F	-reserved- *(Power Down Mode Refresh)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓	✓	✓

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– = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 450–453 VGAs drive CRTs only, 455–457 & 655x0 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

EXTENSION REGISTER SUMMARY: 60-7F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family								
						450	451	452	453	455	456	457	65520	65530
XR60	**Blink Rate Control**	8	R/W	3B7/3D7	1 0 0 0 0 0 1 1	.	.	.	.	✓	✓	✓	✓	✓
XR61	**SmartMap™ Control**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	.	✓	✓
XR62	**SmartMap™ Shift Parameter**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	.	✓	✓
XR63	**SmartMap™ Color Mapping Contr**	7	R/W	3B7/3D7	x - x x x x x x	.	.	.	.	✓	✓	.	✓	✓
XR64	**FP Alternate Vertical Total**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓	✓	✓
XR65	**FP Alternate Overflow**	6	R/W	3B7/3D7	x x x - - x x x	.	.	.	.	✓	✓	✓	✓	✓
XR66	**FP Alternate Vertical Sync Start**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓	✓	✓
XR67	**FP Alternate Vertical Sync End**	4	R/W	3B7/3D7	- - - - x x x x	.	.	.	.	✓	✓	✓	✓	✓
XR68	**FP V Panel Size** *(FP Alt V DE End)*	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓	✓	✓
XR69	-reserved- *(FP V Display Start 350)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓	.	.
XR6A	-reserved- *(FP V Display End 350)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓	.	.
XR6B	-reserved- *(FP V Overflow 2)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓	.	.
XR6C	**Programmable Output Drive** *(Wclk*	4	R/W	3B7/3D7	- - - 0 0 0 - 0	.	.	.	.	✓	✓	.	.	✓
XR6D	-reserved- *(FRC Control)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	.	.
XR6E	**Polynomial FRC Control**	8	R/W	3B7/3D7	1 0 1 1 1 1 0 1	.	.	.	.	.	.	✓	✓	✓
XR6F	-reserved- *(Frame Buffer Control)*	--	--	3B7/3D7		.	.	.	.	.	.	.	✓	✓
XR70	**Setup / Disable Control**	1	R/W	3B7/3D7	0 - - - - - - -	✓	.	.	.	.	.	.	✓	✓
XR71	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR72	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR73	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR74	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR75	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR76	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR77	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR78	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR79	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR7A	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR7B	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.	.
XR7C	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.		
XR7D	**FP Compensation Diagnostic**	0	R/O	3B7/3D7	- - - - - - - -	.	.	.	.	.	.	.	✓	✓
XR7E	**CGA/Hercules Color Select**	6	R/W	3B7/3D7	- - x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR7F	**Diagnostic**	8	R/W	3B7/3D7	0 0 x x x x 0 0	✓	✓	✓	.	✓	✓	✓	✓	✓

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– = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
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Registers

GLOBAL CONTROL (SETUP) REGISTERS

The Setup Control Register and Video Subsystem Enable registers are used to enable or disable the VGA. The Setup Control register is also used to place the VGA in normal or setup mode (the Global Enable Register is accessible only during Setup mode). The Setup Control register is used only in ISA bus interfaces; the Video Subsystem Enable register is used only in MC, PI, and Local Bus configurations. In MC and PI Bus interfaces, disable and setup functions may also be performed by the DISA/ and SETUP/ pins respectively. The DISA/ pin and the various internal 'disable' bits 'OR' together to provide multiple ways of disabling the chip; all 'disable' bits must be off to enable access to the chip. When the chip is 'disabled' in this fashion, only bus access is disabled; other functions remain operational (memory refresh, display refresh, etc).

Note: In setup mode in the IBM VGA, the Global Setup Register (defined as port address 102) actually occupies the *entire I/O space* . Only the lower 3 bits are used to decode and select this register. To avoid bus conflicts with other peripherals, reads should only be performed at the 10xh port addresses while in setup mode. To eliminate potential compatibility problems in widely varying PC systems, the 65510 decodes the Global Setup register at I/O port 102h only.

GENERAL CONTROL REGISTERS

Two Input Status Registers read the SENSE pin (or Virtual Switch Register or internal comparator output instead), pending CRT interrupt, display enable / horizontal sync output, and vertical retrace / video output. The Feature Control Register selects the vertical sync function while the Miscellaneous Output Register controls I/O address select, clock selection, access to video RAM, memory page, and horizontal and vertical sync polarity.

CGA / HERCULES REGISTERS

CGA Mode and Color Select registers are provided on-chip for emulation of CGA modes. Hercules Mode and Configuration registers are provided on-chip for emulation of Hercules mode.

SEQUENCER REGISTERS

The Sequencer Index Register contains a 3-bit index to the Sequencer Data Registers. The Reset Register forces an asynchronous or synchronous reset of the sequencer. The Sequencer Clocking Mode Register controls master clocking functions, video enable/disable and selects either an 8 or 9 dot character clock. A Plane/Map Mask Register enables the color plane and write protect. The Character Font Select Register handles video intensity and character generation and controls the display memory plane through the character generator select. The Sequencer Memory Mode Register handles all memory, giving access by the CPU to 4 / 16 / 32 KBytes, Odd / Even addresses (planes) and writing of data to display memory.

CRT CONTROLLER REGISTERS

The CRT Controller Index Register contains a 6-bit index to the CRT Controller Registers. Twenty eight registers perform all display functions for modes: horizontal and vertical blanking and sync, panning and scrolling, cursor size and location, light pen, and underline.

GRAPHICS CONTROLLER REGISTERS

The Graphics Controller Index Register contains a 4-bit index to the Graphics Controller Registers. The Set/Reset Register controls the format of the CPU data to display memory. It also works with the Enable Set/Reset Register. Reducing 32 bits of display data to 8 bits of CPU data is accomplished by the Color Compare Register. Data Rotate Registers specify the CPU data bits to be rotated and subjected to logical operations. The Read Map Select Register reduces memory data for the CPU in the four plane (16 color) graphics mode. The Graphics Mode Register controls the write, read, and shift register modes. The Miscellaneous Register handles graphics/text, chaining of odd/even planes, and display memory mapping. Additional registers include Color Don't Care and Bit Mask.

ATTRIBUTE CONTROLLER AND COLOR PALETTE REGISTERS

The Attribute Controller Index Register contains a 5-bit index to the Attribute Controller Registers. A 6th

bit is used to enable the video. The Attribute Controller Registers handle internal color lookup table mapping, text/graphics mode, overscan color, and color plane enable. The horizontal Pixel Panning and Pixel Padding Registers control pixel attributes on screen.

Color palette registers handle CPU reads and writes to I/O address range 3C6h-3C9h. Inmos IMSG176 (Brooktree BT471/476) compatible registers are documented in this manual.

EXTENSION REGISTERS

The 65510 defines a set of extension registers which are addressed with the 7-bit Extension Register Index. The I/O port address is fixed at 3D6-3D7h and read/write access is always enabled to improve software performance.

The extension registers handle a variety of interfacing, compatibility, and display functions as discussed below. They are grouped into the following logical groups for discussion purposes:

1. Miscellaneous Registers include the Version number, Dip Switch, CPU interface, paging control, memory mode control, and diagnostic functions.
2. General Purpose Registers handle video blanking and the video default color.
3. Backwards Compatibility Registers control Hercules, MDA, and CGA emulation modes. Write Protect functions are provided to increase flexibility in providing backwards compatibility.
4. Alternate Horizontal and Vertical Registers handle all horizontal and vertical timing, including sync, blank and offset. These are used for backwards compatibility.
5. Flat Panel Registers handle all internal logic specific to driving of flat panel displays.

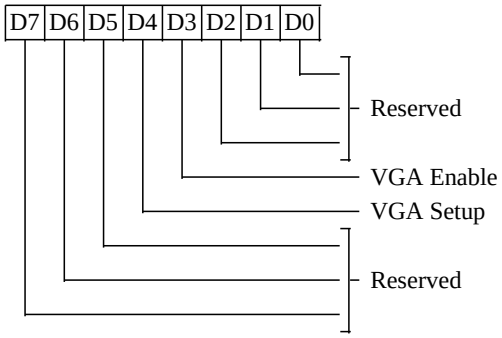
Note: The state of most of the Standard VGA Registers is undefined at reset. All registers specific to the 65510 (Extension Registers) are summarized in the Extension Register Table.

Global Control (Setup) Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SETUP	Setup Control	–	W	46E8h (ISA bus only)	–	33
VSE	Video Subsystem Enable	–	W	3C3h (MC/PI/LB bus only)	–	33
ENAB	Global Enable	–	RW	102h (Setup mode only)	–	34

SETUP CONTROL REGISTER (SETUP)

Write only at I/O Address 46E8h



This register is accessable in ISA (PC) bus configurations only. It is ignored completely in MC, PI, and Local Bus configurations. It is also ignored if XR70 bit-7 is set to 1 (the default is 0). In MC and PI bus configurations, Setup mode and VGA Disable are controlled through the SETUP/ and DISA/ pins, respectively and by register 3C3.

This register is cleared by RESET.

2-0 Reserved (0)

3 VGA Enable

0 VGA is disabled
1 VGA is enabled

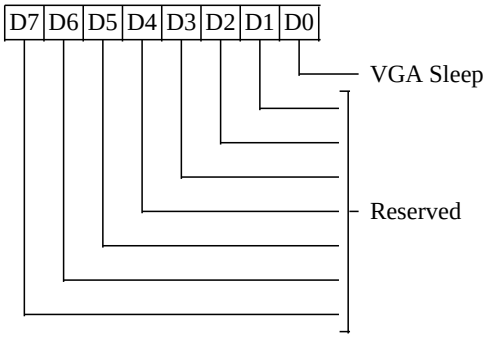
4 Setup Mode

0 VGA is in Normal Mode
1 VGA is in Setup Mode

7-5 Reserved (0)

VIDEO SUBSYSTEM ENABLE REGISTER (VSE)

Write Only at I/O Address 3C3h



This register is accessable in MC, PI, and Local Bus configurations only. It is ignored in ISA (PC) bus configurations (register 46E8 is used in ISA bus configurations). Access to this register may be disabled by setting XR70 bit-7 to 1 (the default is 0).

This register is cleared by RESET.

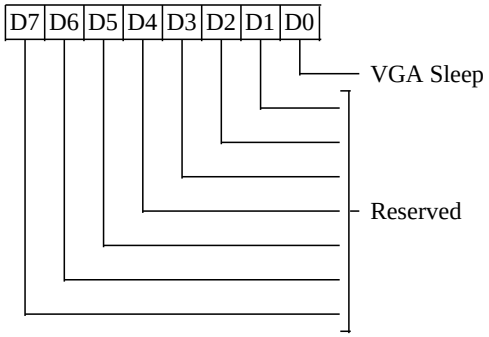
0 VGA Sleep

0 VGA is disabled
1 VGA is enabled

7-1 Reserved (0)

GLOBAL ENABLE REGISTER (ENAB)

Read/Write at I/O Address 102h



This register is only accessible in Setup Mode (enabled by register 46E8 in ISA bus configurations or by the SETUP/ pin in MC bus configurations).

Bit-0 of this register is cleared by RESET in ISA and MC bus configurations and set by RESET in PI and Local Bus configurations.

0 VGA Sleep

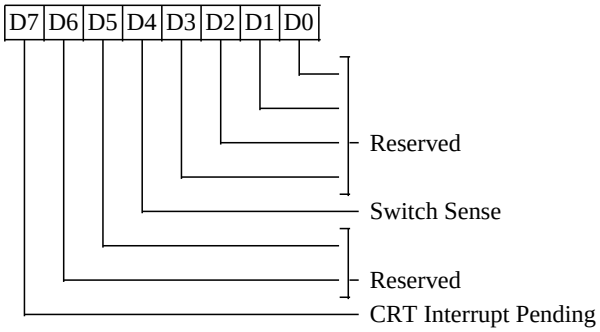
0 VGA is disabled
1 VGA is enabled

7-1 Reserved (0)

General Control & Status Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ST00	Input Status 0	–	R	3C2h	–	35
ST01	Input Status 1	–	R	3BAh/3DAh	–	35
FCR	Feature Control	–	W	3BAh/3DAh	5	36
			R	3CAh		
MSR	Miscellaneous Output	–	W	3C2h	5	36
			R	3CCh		

INPUT STATUS REGISTER 0 (ST00)
Read only at I/O Address at 3C2h



3-0 Reserved (0)

4 Switch Sense

This bit returns the Status of the SENSE pin or the Virtual Switch Register (XR1F) output if enabled by XR1F bit-7 or the output of the internal comparator if enabled by XR06 bit-4 (Sense Source). XR1F bit-7 takes priority over the other settings if set.

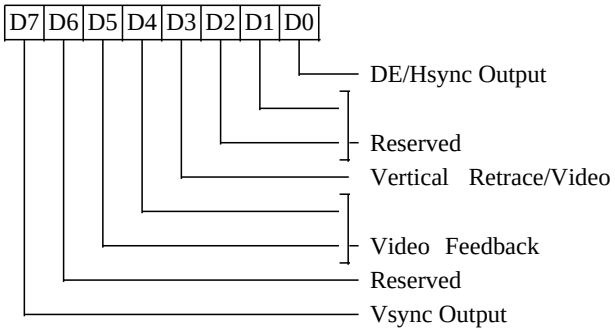
6-5 Reserved

These bits read back 00 in PC and PI bus configurations and 11 in MC configuration.

7 CRT Interrupt Pending

0 Indicates no CRT interrupt is pending
1 Indicates a CRT interrupt is waiting to be serviced

INPUT STATUS REGISTER 1 (ST01)
Read only at I/O Address 3BAh/3DAh



0 Display Enable/HSYNC Output

The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-4).

0 Indicates DE or HSYNC inactive
1 Indicates DE or HSYNC active

2-1 Reserved (0)

3 Vertical Retrace/Video

The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-5).

0 Indicates VSYNC or video inactive
1 Indicates VSYNC or video active

5-4 Video Feedback 1, 0

These are diagnostic video bits which are selected via the Color Plane Enable Register.

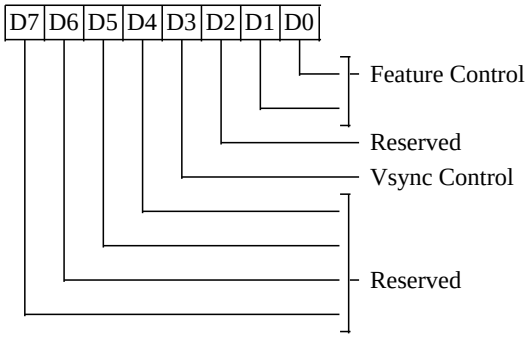
6 Reserved (0)

7 Vsync Output

The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-6). It reflects the active status of the VSYNC output: 0=inactive, 1=active.

FEATURE CONTROL REGISTER (FCR)

Write at I/O Address 3BAh/3DAh
Read at I/O Address 3CAh
Group 5 Protection



1-0 Feature Control

These bits are used internal to the chip in conjunction with the Configuration Register (XR01). When enabled by XR01 bits 2-3 and Misc Output Register bits 3-2 = 10, these bits determine the pixel clock frequency typically as follows:

FCR1:0 = 00 = 40.000 MHz
FCR1:0 = 01 = 50.350 MHz
FCR1:0 = 10 = User defined
FCR1:0 = 11 = 44.900 MHz

This preserves compatibility with drivers developed for earlier generation Chips and Technologies VGA controllers.

2 Reserved (0)

3 Vsync Control

This bit is cleared by RESET.

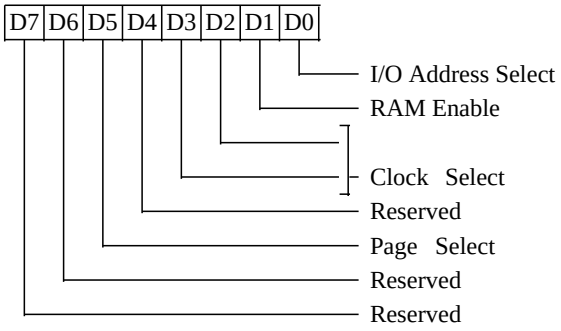
0 VSync output on the VSYNC pin
1 Logical 'OR' of VSync and Display Enable output on the VSYNC pin

This capability is not typically very useful, but is provided for IBM compatibility.

7-4 Reserved (0)

MISCELLANEOUS OUTPUT REGISTER (MSR)

Write at I/O Address 3C2h
Read at I/O Address 3CCh
Group 5 Protection



This register is cleared by RESET.

0 I/O Address Select . This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01).

0 Select 3Bxh I/O address
1 Select 3Dxh I/O address

1 RAM Enable

0 Prevent CPU access to display memory
1 Allow CPU access to display memory

3-2 Clock Select. These bits usually select the dot clock source for the CRT interface:

MSR3:2 = 00 = Select CLK0
MSR3:2 = 01 = Select CLK1
MSR3:2 = 10 = Select CLK2
MSR3:2 = 11 = Select CLK3

See extension register XR01 bits 2-3 (Configuration) and FCR bits 0-1 for variations of the above clock selection mapping. See also XR1F (Virtual Switch Register) for additional functionality potentially controlled by these bits.

4 Reserved (0)

5 Page Select. In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64 KByte page in display memory for CPU access: 0=select upper page; 1=select lower page.

6 Reserved (0)

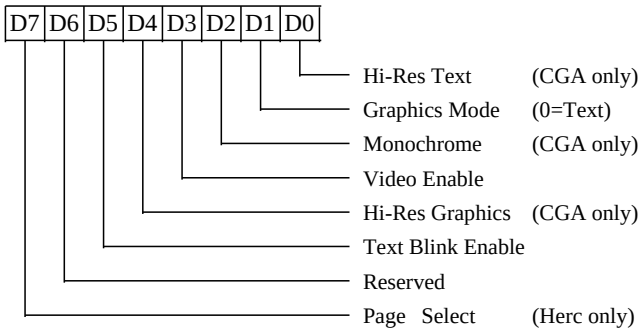
7 Reserved (0)

CGA / Hercules Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
MODE	CGA/Hercules Mode	–	RW	3D8h	–	37
COLOR	CGA Color Select	–	RW	3D9h	–	38
HCFG	Hercules Configuration	–	RW	3BFh	–	39

CGA / HERCULES MODE CONTROL REGISTER (MODE)

Read/Write at I/O Address 3B8h/3D8h



This register is effective only in CGA and Hercules modes. It is accessible if CGA or Hercules emulation mode is selected or the extension registers are enabled. If the extension registers are enabled, the address is determined by the address select in the Miscellaneous Outputs register. Otherwise the address is determined by the emulation mode. It is cleared by RESET.

0 CGA 80/40 Column Text Mode
- 0 Select 40 column CGA text mode
- 1 Select 80 column CGA text mode

1 CGA/Hercules Graphics/Text Mode
- 0 Select text mode
- 1 Select graphics mode

2 CGA Mono/Color Mode
- 0 Select CGA color mode
- 1 Select CGA monochrome mode

3 CGA/Hercules Video Enable
- 0 Blank the screen
- 1 Enable video output

4 CGA High Resolution Mode
- 0 Select 320x200 graphics mode
- 1 Select 640x200 graphics mode

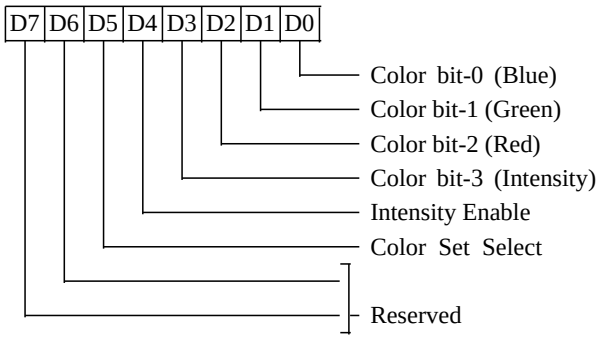
5 CGA/Hercules Text Blink Enable
- 0 Disable character blink attribute (blink attribute bit-7 used to control background intensity)
- 1 Enable character blink attribute

6 Reserved (0)

7 Hercules Page Select
- 0 Select the lower part of memory (starting address B0000h) in Hercules Graphics Mode
- 1 Select the upper part of the memory (starting address B8000h) in Hercules Graphics Mode

CGA COLOR SELECT REGISTER (COLOR)

Read/Write at I/O Address 3D9h



This register is effective only in CGA modes. It is accessible if CGA emulation mode is selected or the extension registers are enabled. This register may also be read or written as an Extension Register (XR7E). It is cleared by RESET.

3-0 Color

320x200 4-color: Background Color (color when the pixel value is 0)

The foreground colors (colors when the pixel value is 1-3) are determined by bit-5 of this register.

640x200 2-color: Foreground Color (color when the pixel value is 1)

The background color (color when the pixel value is 0) is black.

4 Intensity Enable

Text Mode: Enables intensified background colors

320x200 4-color: Enables intensified colors 0-3

640x200 2-color: Don't care

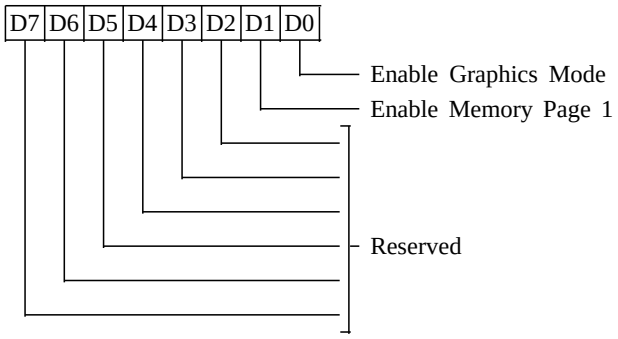
5 Color Set Select

This bit selects one of two available CGA color palettes to be used in 320x200 graphics mode (it is ignored in all other modes) according to the following table:

Pixel Value	Color Set 0	Color Set 1
0 0	Color per bits 0-3	Color per bits 0-3
0 1	Green	Cyan
1 0	Red	Magenta
1 1	Brown	White

7-6 Reserved (0)

HERCULES CONFIGURATION REGISTER (HCFG)
Write only at I/O Address 3BFh



This register is effective only in Hercules mode. It is accessible in Hercules emulation mode or if the extension registers are enabled. It may be read back through XR14 bits 2 & 3. It is cleared by RESET.

0 Enable Graphics Mode

0 Lock the chip in Hercules text mode. In this mode, the CPU has access only to memory address range B0000h-B7FFFh (in text mode the same area of display memory wraps around 8 times within this range such that B0000 accesses the same display memory location as B1000, B2000, etc.).

1 Permit entry to Hercules Graphics mode

1 Enable Memory Page 1

0 Prevent setting of the Page Select bit (bit 7 of the Hercules Mode Control Register). This function also restricts memory usage to addresses B0000h-B7FFFh.

1 The Page Select bit can be set and the upper part of display memory (addresses B8000h - BFFFFh) is available.

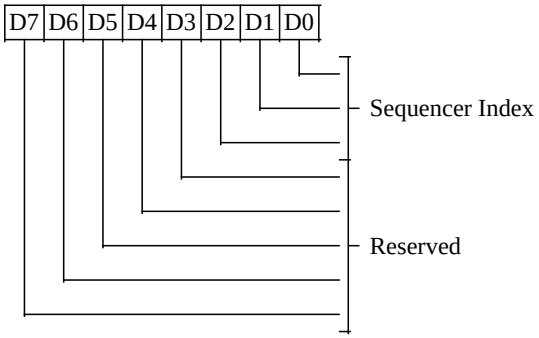
7-2 Reserved (0)

Sequencer Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SRX	Sequencer Index	–	RW	3C4h	1	41
SR00	Reset	00h	RW	3C5h	1	41
SR01	Clocking Mode	01h	RW	3C5h	1	42
SR02	Plane/Map Mask	02h	RW	3C5h	1	42
SR03	Character Font	03h	RW	3C5h	1	43
SR04	Memory Mode	04h	RW	3C5h	1	44
SR07	Horizontal Character Counter Reset	07h	W	3C5h	–	44

SEQUENCER INDEX REGISTER (SRX)

Read/Write at I/O Address 3C4h



This register is cleared by reset.

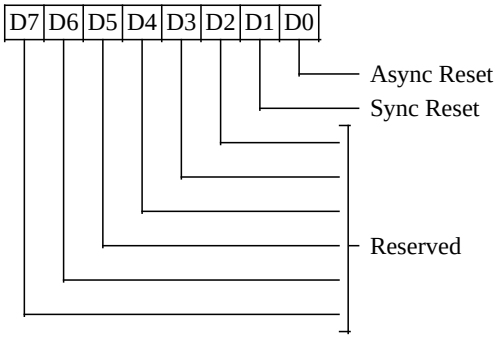
2-0 Sequencer Index

These bits contain a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7.

7-3 Reserved (0)

SEQUENCER RESET REGISTER (SR00)

Read/Write at I/O Address 3C5h
Index 00h
Group 1 Protection



0 Asynchronous Reset

0 Force asynchronous reset
1 Normal operation

Display memory data will be corrupted if this bit is set to zero.

1 Synchronous Reset

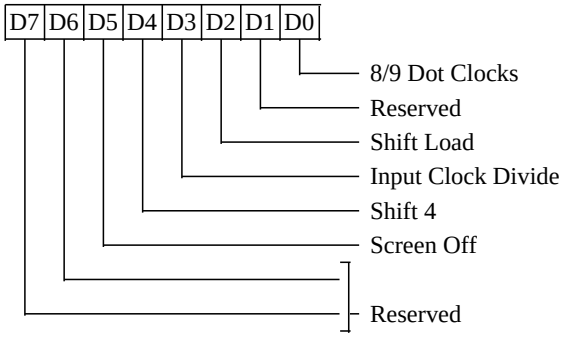
0 Force synchronous reset
1 Normal operation

Display memory data is not corrupted if this bit is set to zero for a short period of time (a few tens of microseconds).

7-2 Reserved (0)

SEQUENCER CLOCKING MODE REGISTER (SR01)

Read/Write at I/O Address 3C5h
Index 01h
Group 1 Protection



0 8/9 Dot Clocks

This bit determines whether a character clock is 8 or 9 dot clocks long.

0 Select 9 dots/character clock
1 Select 8 dots/character clock

1 Reserved (0)

2 Shift Load

0 Load video data shift registers every character clock
1 Load video data shift registers every other character clock

Bit-4 of this register must be 0 for this bit to be effective.

3 Input Clock Divide

0 Sequencer master clock output on the PCLK pin (used for 640 (720) pixel modes)
1 Master clock divided by 2 output on the PCLK pin (used for 320 (360) pixel modes)

4 Shift 4

0 Load video shift registers every 1 or 2 character clocks (depending on bit-2 of this register)
1 Load shift registers every 4th character clock.

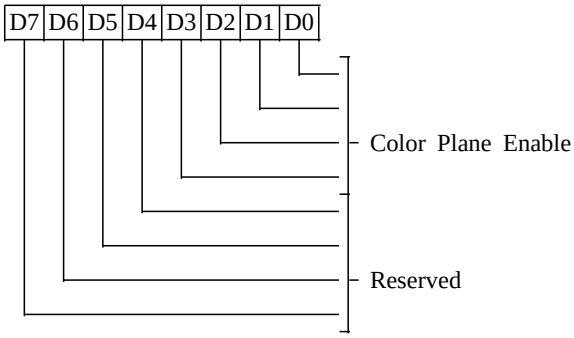
5 Screen Off

0 Normal Operation
1 Disable video output and assign all display memory bandwidth for CPU accesses

7-6 Reserved (0)

SEQUENCER PLANE/MAP MASK REGISTER (SR02)

Read/Write at I/O Address 3C5h
Index 02h
Group 1 Protection



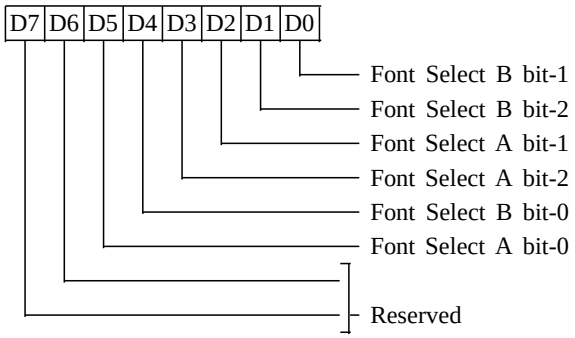
3-0 Color Plane Enable

0 Write protect corresponding color plane
1 Allow write to corresponding color plane.

In Odd/Even and Quad modes, these bits still control access to the corresponding color plane.

7-4 Reserved (0)

CHARACTER FONT SELECT REGISTER (SR03)
Read/Write at I/O Address 3C5h
Index 03h
Group 1 Protection



In text modes, bit-3 of the video data's attribute byte normally controls the foreground intensity. This bit may be redefined to control switching between character sets. This latter function is enabled whenever there is a difference in the values of the Character Font Select A and the Character Font Select B bits. If the two values are the same, the character select function is disabled and attribute bit-3 controls the foreground intensity.

SR04 bit-1 must be 1 for the character font select function to be active. Otherwise, only character fonts 0 and 4 are available.

1-0 High order bits of Character Generator Select B

3-2 High order bits of Character Generator Select A

4 Low order bit of Character Generator Select B

5 Low order bit of Character Generator Select A

7-6 Reserved (0)

The following table shows the display memory plane selected by the Character Generator Select A and B bits.

Code	Character Generator Table Location
0	First 8K of Plane 2
1	Second 8K of Plane 2
2	Third 8K of Plane 2
3	Fourth 8K of Plane 2
4	Fifth 8K of Plane 2
5	Sixth 8K of Plane 2
6	Seventh 8K of Plane 2
7	Eighth 8K of Plane 2

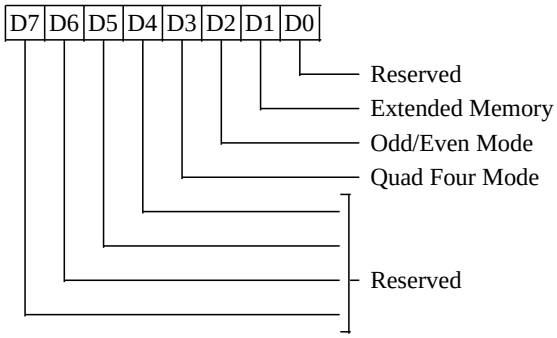
where 'code' is:

Character Generator Select A (bits 3, 2, 5) when bit-3 of the the attribute byte is one.

Character Generator Select B (bits 1, 0, 4) when bit-3 of the attribute byte is zero.

SEQUENCER MEMORY MODE REGISTER (SR04)

Read/Write at I/O Address 3C5h
Index 04h
Group 1 Protection



0 Reserved (0)

1 Extended Memory

0 Restrict CPU access to 4/16/32 Kbytes
1 Allow complete access to memory

This bit should normally be 1.

2 Odd/Even Mode

0 CPU accesses to Odd/Even addresses are directed to corresponding odd/even planes
1 All planes are accessed simultaneously (IRGB color)

Bit-3 of this register must be 0 for this bit to be effective. This bit affects only CPUwrite accesses to display memory.

3 Quad Four Mode

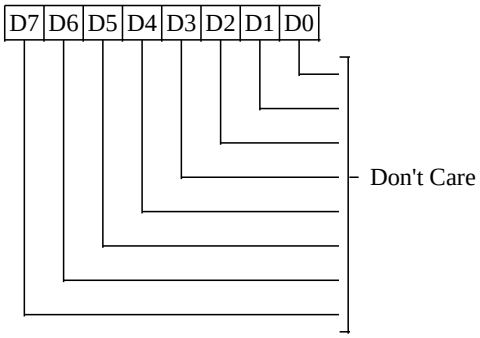
0 CPU addresses are mapped to display memory as defined by bit-2 of this register
1 CPU addresses are mapped to display memory modulo 4. The two low order CPU address bits select the display memory plane.

This bit affects both CPU reads and writes to display memory.

7-4 Reserved (0)

SEQUENCER HORIZONTAL CHARACTER COUNTER RESET (SR07)

Read/Write at I/O Address 3C5h
Index 07h



Writing to SR07 with any data will cause the horizontal character counter to be held reset (character counter output = 0) until a write to any other sequencer register with any data value. The write to any index in the range 0-6 clears the latch that is holding the reset condition on the character counter.

The vertical line counter is clocked by a signal derived from horizontal display enable (which does not occur if the horizontal counter is held reset). Therefore, if the write to SR07 occurs during vertical retrace, the horizontal and vertical counters will both be set to zero. A write to any other sequencer register may then be used to start both counters with reasonable synchronization to an external event via software control.

This is a standard VGA register which was not documented by IBM.

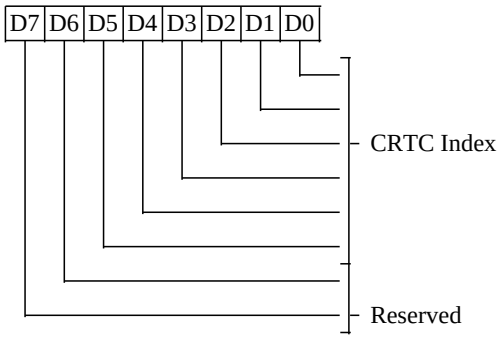
CRT Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
CRX	CRTC Index	–	RW	3B4h/3D4h	–	46
CR00	Horizontal Total	00h	RW	3B5h/3D5h	0	46
CR01	Horizontal Display Enable End	01h	RW	3B5h/3D5h	0	46
CR02	Horizontal Blank Start	02h	RW	3B5h/3D5h	0	47
CR03	Horizontal Blank End	03h	RW	3B5h/3D5h	0	47
CR04	Horizontal Sync Start	04h	RW	3B5h/3D5h	0	48
CR05	Horizontal Sync End	05h	RW	3B5h/3D5h	0	48
CR06	Vertical Total	06h	RW	3B5h/3D5h	0	49
CR07	Overflow	07h	RW	3B5h/3D5h	0/3	49
CR08	Preset Row Scan	08h	RW	3B5h/3D5h	3	50
CR09	Maximum Scan Line	09h	RW	3B5h/3D5h	2/4	50
CR0A	Cursor Start Scan Line	0Ah	RW	3B5h/3D5h	2	51
CR0B	Cursor End Scan Line	0Bh	RW	3B5h/3D5h	2	51
CR0C	Start Address High	0Ch	RW	3B5h/3D5h	–	52
CR0D	Start Address Low	0Dh	RW	3B5h/3D5h	–	52
CR0E	Cursor Location High	0Eh	RW	3B5h/3D5h	–	52
CR0F	Cursor Location Low	0Fh	RW	3B5h/3D5h	–	52
CR10	Vertical Sync Start (See Note 2)	10h	W or RW	3B5h/3D5h	4	53
CR11	Vertical Sync End (See Note 2)	11h	W or RW	3B5h/3D5h	3/4	53
CR10	Lightpen High (See Note 2)	10h	R	3B5h/3D5h	–	53
CR11	Lightpen Low (See Note 2)	11h	R	3B5h/3D5h	–	53
CR12	Vertical Display Enable End	12h	RW	3B5h/3D5h	4	54
CR13	Offset	13h	RW	3B5h/3D5h	3	54
CR14	Underline Row	14h	RW	3B5h/3D5h	3	54
CR15	Vertical Blank Start	15h	RW	3B5h/3D5h	4	55
CR16	Vertical Blank End	16h	RW	3B5h/3D5h	4	55
CR17	CRT Mode Control	17h	RW	3B5h/3D5h	3/4	56
CR18	Line Compare	18h	RW	3B5h/3D5h	3	57
CR22	Memory Data Latches	22h	R	3B5h/3D5h	–	58
CR24	Attribute Controller Toggle	24h	R	3B5h/3D5h	–	58
CR3x	Clear Vertical Display Enable	3xh	W	3B5h/3D5h	–	58

Note 1: When MDA or Hercules emulation is enabled, the CRTC I/O address should be set to 3B0h-3B7h by setting the I/O address select bit in the Miscellaneous Output register (3C2h/3CCh bit-0) to zero. When CGA emulation is enabled, the CRTC I/O address should be set to 3D0h-3D7h by setting Misc Output Register bit-0 to 1.

Note 2: In the EGA, all CRTC registers except the cursor (CR0C-CR0F) and light pen (CR10 and CR11) registers are write-only (i.e., no read back). In both the EGA and VGA, the light pen registers are at index locations conflicting with the vertical sync registers. This would normally prevent reads and writes from occurring at the same index. Since the light pen registers are not normally useful, the VGA provides software control (CR03 bit-7) of whether the vertical sync or light pen registers are readable at indices 10-11.

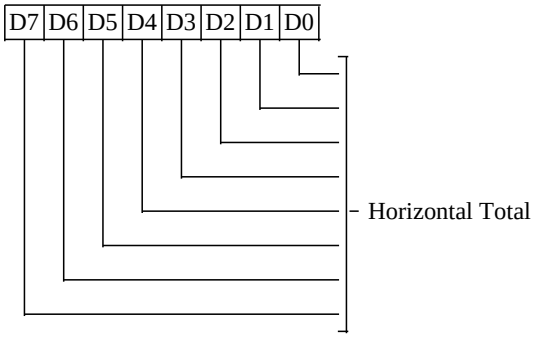
CRTC INDEX REGISTER (CRX)
Read/Write at I/O Address 3B4h/3D4h



5-0 CRTC data register index

7-6 Reserved (0)

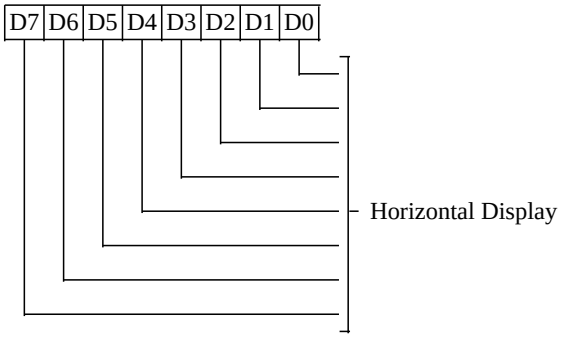
HORIZONTAL TOTAL REGISTER (CR00)
Read/Write at I/O Address 3B5h/3D5h
Index 00h
Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Total. Total number of character clocks per line = contents of this register + 5. This register determines the horizontal sweep rate.

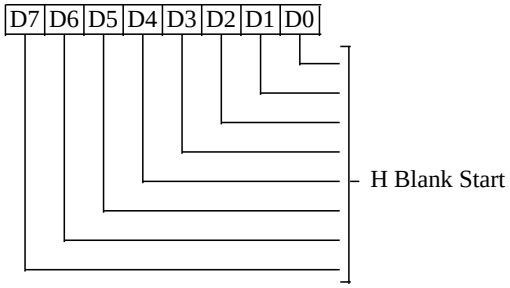
HORIZONTAL DISPLAY ENABLE END REGISTER (CR01)
Read/Write at I/O Address 3B5h/3D5h
Index 01h
Group 0 Protection



This register is used for all VGA and EGA modes on CRTs. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Number of Characters displayed per scan line - 1.

HORIZONTAL BLANK START REGISTER (CR02)
Read/Write at I/O Address 3B5h/3D5h
Index 02h
Group 0 Protection

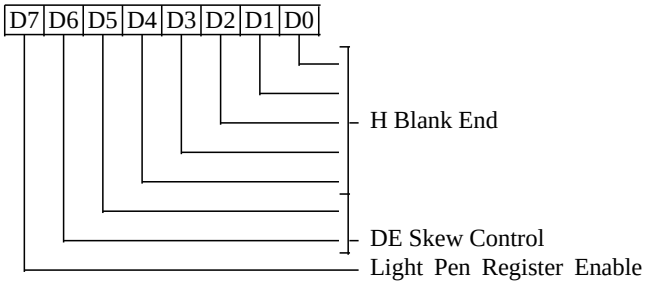


This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Blank Start

These bits specify the beginning of horizontal blank in terms of character clocks from the beginning of the display scan. The period between Horizontal Display Enable End and Horizontal Blank Start is the right side border on screen.

HORIZONTAL BLANK END REGISTER (CR03)
Read/Write at I/O Address 3B5h/3D5h
Index 03h
Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0 Horizontal Blank End

These are the lower 5 bits of the character clock count used to define the end of horizontal blank. The interval between the end of horizontal blank and the beginning of the display (a count of 0) is the left side border on the screen. If the horizontal blank width desired is W clocks, the 5-bit value programmed in this register = [contents of CR02 + W] and 1Fh. The most significant bit is programmed in CR05 bit-7. This bit = [(CR02 + W) and 20h]/20h.

6-5 Display Enable Skew Control

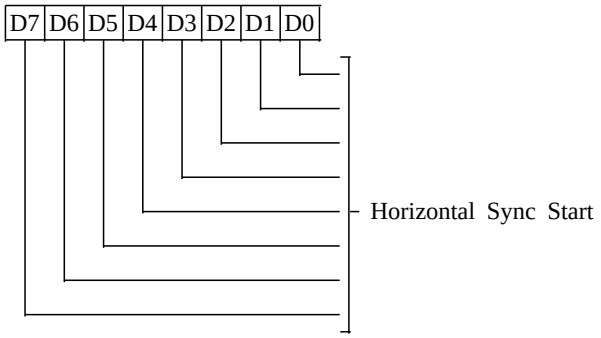
Defines the number of character clocks that the Display Enable signal is delayed to compensate for internal pipeline delays.

7 Light Pen Register Enable

This bit must be 1 for normal operation; when this bit is 0, CRTC registers CR10 and CR11 function as lightpen readback registers.

HORIZONTAL SYNC START REGISTER (CR04)

Read/Write at I/O Address 3B5h/3D5h
Index 04h
Group 0 Protection



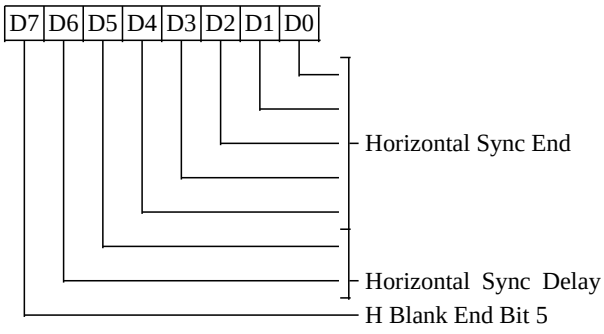
This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Sync Start

These bits specify the beginning of Hsync in terms of Character clocks from the beginning of the display scan. These bits also determine display centering on the screen.

HORIZONTAL SYNC END REGISTER (CR05)

Read/Write at I/O Address 3B5h/3D5h
Index 05h
Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0 Horizontal Sync End

Lower 5 bits of the character clock count which specifies the end of Horizontal Sync. If the horizontal sync width desired is N clocks, then these bits = (N + contents of CR04) and 1Fh.

6-5 Horizontal Sync Delay

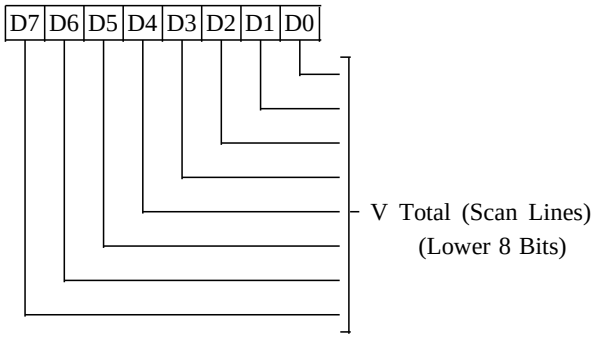
These bits specify the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.

7 Horizontal Blank End Bit 5

This bit is the sixth bit of the Horizontal Blank End Register (CR03).

VERTICAL TOTAL REGISTER (CR06)

Read/Write at I/O Address 3B5h/3D5h
Index 06h
Group 0 Protection



This register is used in all modes.

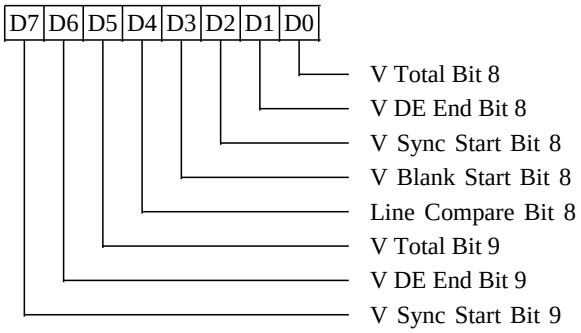
7-0 Vertical Total

These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow Register. The Vertical Total value specifies the total number of scan lines (horizontal retrace periods) per frame.

Programmed Count = Actual Count – 2

OVERFLOW REGISTER (CR07)

Read/Write at I/O Address 3B5h/3D5h
Index 07h
Group 0 Protection on bits 0-3 and bits 5-7
Group 3 Protection on bit 4



This register is used in all modes.

0 Vertical Total Bit 8

1 Vertical Display Enable End Bit 8

2 Vertical Sync Start Bit 8

3 Vertical Blank Start Bit 8

4 Line Compare Bit 8

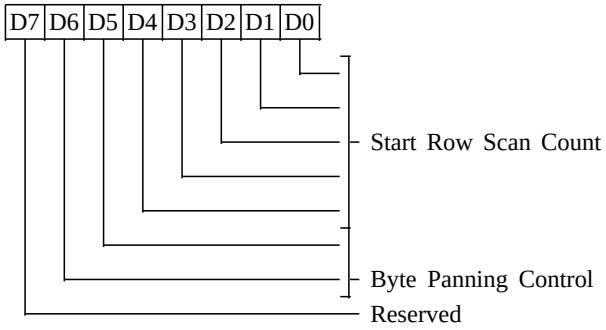
5 Vertical Total Bit 9

6 Vertical Display Enable End Bit 9

7 Vertical Sync Start Bit 9

PRESET ROW SCAN REGISTER (CR08)

Read/Write at I/O Address 3B5h/3D5h
Index 08h
Group 3 Protection



4-0 Start Row Scan Count

These bits specify the starting row scan count after each vertical retrace. Every horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count during active display. This register is used for soft scrolling in text modes.

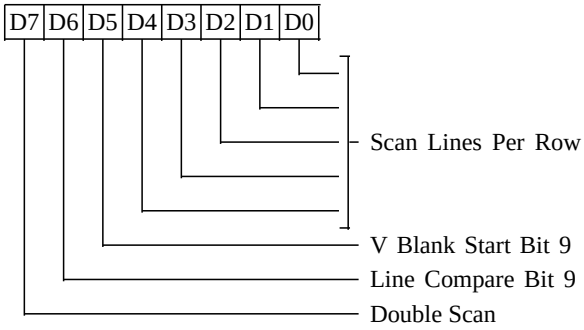
6-5 Byte Panning Control

These bits specify the lower order bits for the display start address. They are used for horizontal panning in Odd/Even and Quad modes.

7 Reserved (0)

MAXIMUM SCAN LINE REGISTER (CR09)

Read/Write at I/O Address 3B5h/3D5h
Index 09h
Group 2 Protection on bits 0-4
Group 4 Protection on bits 5-7



4-0 Scan Lines Per Row

These bits specify the number of scan lines in a row:

Programmed Value = Actual Value + 1

5 Vertical Blank Start Register Bit 9

6 Line Compare Register Bit 9

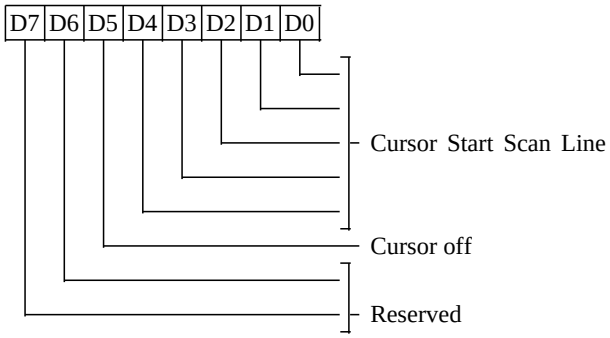
7 Double Scan

0 Normal Operation
1 Enable scan line doubling

The vertical parameters in the CRT Controller (even for a split screen) are not affected, only the CRTC row scan counter (bits 0-4 of this register) and display memory addressing screen refresh are affected.

CURSOR START SCAN LINE REGISTER (CR0A)

Read/Write at I/O Address 3B5h/3D5h
Index 0Ah
Group 2 Protection



4-0 Cursor Start Scan Line

These bits specify the scan line of the character row where the cursor display begins.

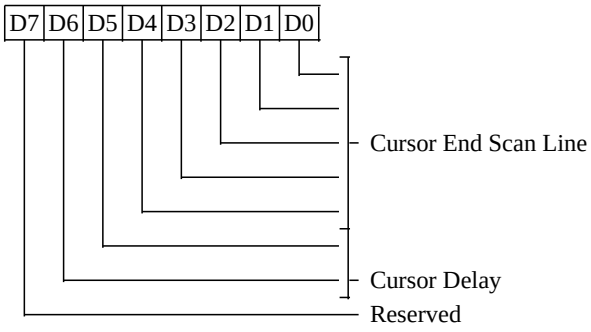
5 Cursor Off

0 Text Cursor On
1 Text Cursor Off

7-6 Reserved (0)

CURSOR END SCAN LINE REGISTER (CR0B)

Read/Write at I/O Address 3B5h/3D5h
Index 0Bh
Group 2 Protection



4-0 Cursor End Scan Line

These bits specify the scan line of a character row where the cursor display ends (i.e., last scan line for the block cursor):

Programmed Value = Actual Value + 1

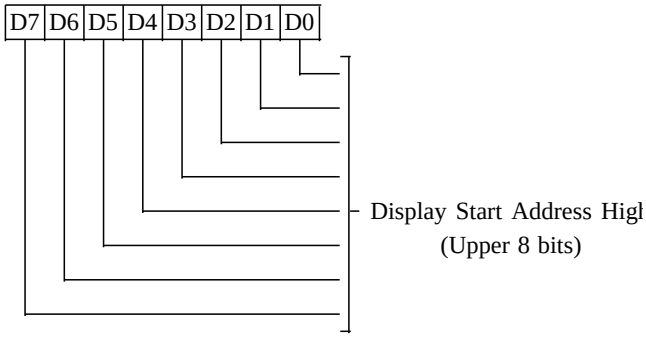
6-5 Cursor Delay

These bits define the number of character clocks that the cursor is delayed to compensate for internal pipeline delay.

7 Reserved (0)

Note: If the Cursor Start Line is greater than the Cursor End Line, then no cursor is generated.

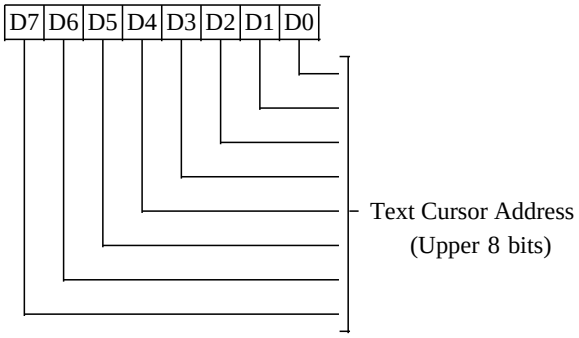
START ADDRESS HIGH REGISTER (CR0C)
Read/Write at I/O Address 3B5h/3D5h
Index 0Ch



7-0 Display Start Address High

This register contains the upper 8 bits of the display start address. In CGA / MDA / Hercules modes, this register wraps around at the 16K, 32K, and 64Kbyte boundaries respectively.

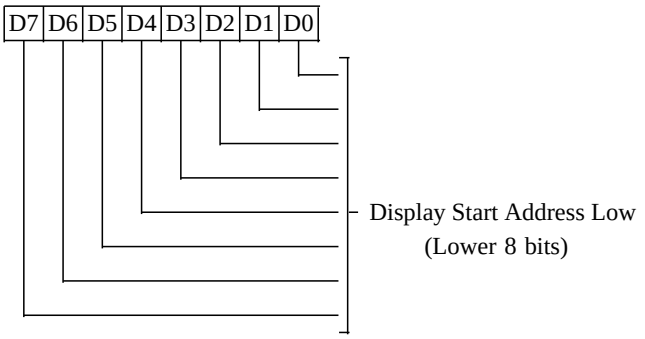
CURSOR LOCATION HIGH REGISTER (CR0E)
Read/Write at I/O Address 3B5h/3D5h
Index 0Eh



7-0 Cursor Location High

This register contains the upper 8 bits of the memory address where the text cursor is active. In CGA / MDA / Hercules modes, this register wraps around at 16K, 32K, and 64Kbyte boundaries respectively.

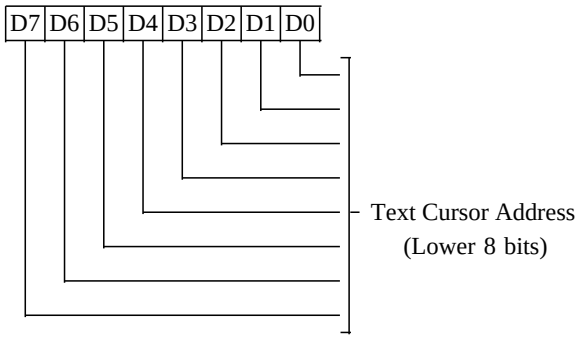
START ADDRESS LOW REGISTER (CR0D)
Read/Write at I/O Address 3B5h/3D5h
Index 0Dh



7-0 Display Start Address Low

This register contains the lower 8 bits of the display start address. The display start address points to the memory address corresponding to the top left corner of the screen.

CURSOR LOCATION LOW REGISTER (CR0F)
Read/Write at I/O Address 3B5h/3D5h
Index 0Fh



7-0 Cursor Location Low

This register contains the lower 8 bits of the memory address where the text cursor is active. In CGA / MDA / Hercules modes, this register wraps around at 16K, 32K, and 64Kbyte boundaries respectively.

LIGHTPEN HIGH REGISTER (CR10)

Read only at I/O Address 3B5h/3D5h
Index 10h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

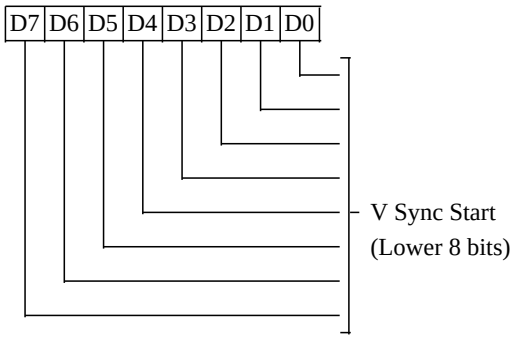
LIGHTPEN LOW REGISTER (CR11)

Read only at I/O Address 3B5h/3D5h
Index 11h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

VERTICAL SYNC START REGISTER (CR10)

Read/Write at I/O Address 3B5h/3D5h
Index 10h
Group 4 Protection



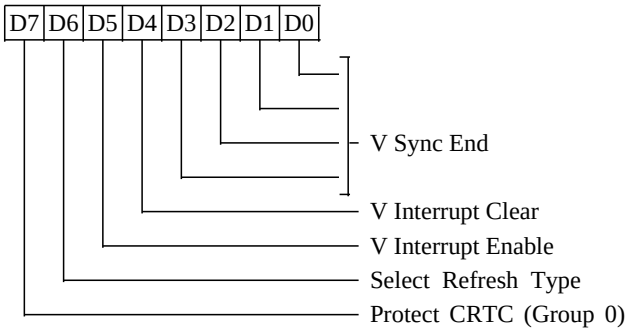
This register is used in all modes. This register is not readable in (Line Compare bit-9) MDA/Hercules emulation or when CR03 bit-7=1.

7-0 Vertical Sync Start

The eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRTC Overflow Register. They define the scan line position at which Vertical Sync becomes active.

VERTICAL SYNC END REGISTER (CR11)

Read/Write at I/O Address 3B5h/3D5h
Index 11h
Group 3 Protection for bits 4 and 5
Group 4 Protection for bits 0-3, 6, and 7



This register is used in all modes. This register is not readable in MDA/Hercules emulation or when CR03 bit-7=1.

3-0 Vertical Sync End

The lower 4 bits of the scan line count that defines the end of vertical sync. If the vertical sync width desired is N lines, then bits 3-0 of this register = (CR10 + N) AND 0Fh.

4 Vertical Interrupt Clear

0 Clear vertical interrupt generated on the IRQ output
1 Normal operation

This bit is cleared by RESET.

5 Vertical Interrupt Enable

0 Enable vertical interrupt (default)
1 Disable vertical interrupt

This bit is cleared by RESET.

6 Select Refresh Type

0 3 refresh cycles per scan line
1 5 refresh cycles per scan line

7 Group Protect 0

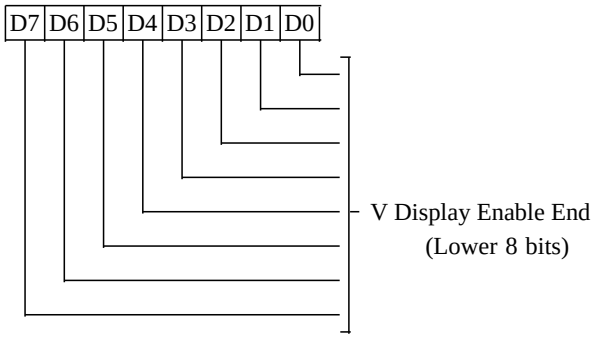
This bit is logically ORed with XR15 bit-6 to determine the protection for group 0 registers. This bit is cleared by RESET.

0 Enable writes to CR00-CR07
1 Disable writes to CR00-CR07

CR07 bit-4 (Line Compare bit-9) is not affected by this bit.

VERTICAL DISPLAY ENABLE END REGISTER (CR12)

Read/Write at I/O Address 3B5h/3D5h
Index 12h
Group 4 Protection

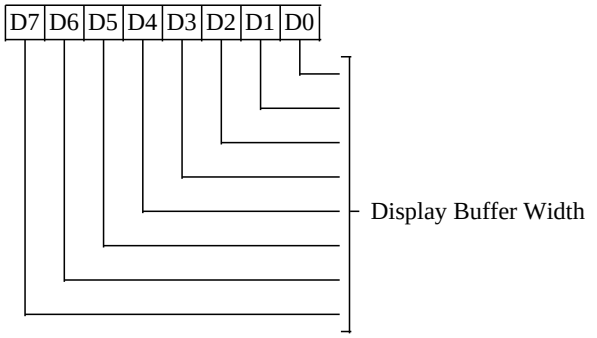


7-0 Vertical Display Enable End

These are the eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow register. The actual count = Contents of this register + 1.

OFFSET REGISTER (CR13)

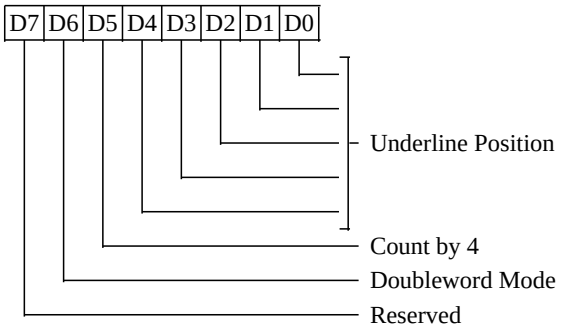
Read/Write at I/O Address 3B5h/3D5h
Index 13h
Group 3 Protection



7-0 Display Buffer Width. The byte starting address of the next display row = Byte Start Address for current row + K* (CR13 + Z/2), where Z = bit defined in XR0D, K = 2 in byte mode, and K = 4 in word mode. Byte, word and double word mode is selected by bit-6 of CR17 and bit-6 of CR14. A less significant bit than bit-0 of this register is defined in the Auxiliary Offset register (XR0D). This allows finer resolution of the bit map width. Byte, word and doubleword mode affects the translation of the 'logical' display memory address to the 'physical' display memory address.

UNDERLINE LOCATION REGISTER (CR14)

Read/Write at I/O Address 3B5h/3D5h
Index 14h
Group 3 Protection



4-0 Underline Position

These bits specify the underline's scan line position within a character row.

Programmed Value = Actual scan line number – 1

5 Count by 4 for Doubleword Mode

0 Frame Buffer Address is incremented by 1 or 2
1 Frame Buffer Address is incremented by 4 or 2

See CR17 bit-3 for further details.

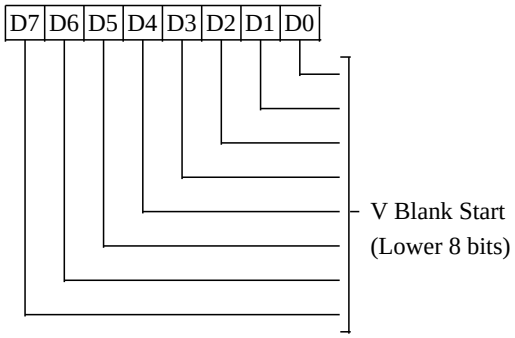
6 Doubleword Mode

0 Frame Buffer Address is byte or word address
1 Frame Buffer Address is doubleword address

This bit is used in conjunction with CR17 bit-6 to select the display memory addressing mode.

7 Reserved (0)

VERTICAL BLANK START REGISTER (CR15)
Read/Write at I/O Address 3B5h/3D5h
Index 15h
Group 4 Protection

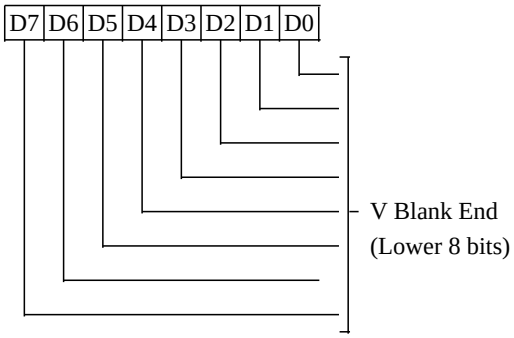


This register is used in all modes.

7-0 Vertical Blank Start

These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers respectively. Together these 10 bits define the scan line position where vertical blank begins. The interval between the end of the vertical display and the beginning of vertical blank is the bottom border on the screen.

VERTICAL BLANK END REGISTER (CR16)
Read/Write at I/O Address 3B5h/3D5h
Index 16h
Group 4 Protection



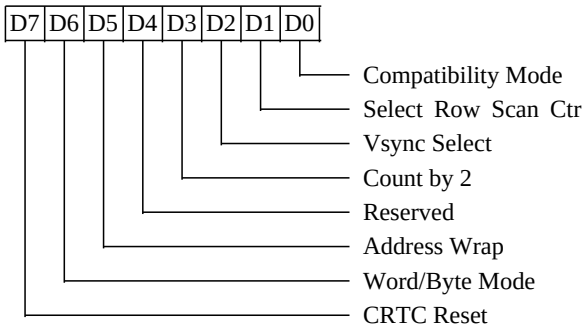
This register is used in all modes.

7-0 Vertical Blank End

These are the 8 low order bits of the scan line count which specifies the end of Vertical Blank. If the vertical blank width desired is Z lines these bits = (Vertical Blank Start + Z) and 0FFh.

CRT MODE CONTROL REGISTER (CR17)

Read/Write at I/O Address 3B5h/3D5h
Index 17h
Group 3 Protection for bits 0, 1, and 3-7
Group 4 Protection for bit 2



0 Compatibility Mode Support

This bit allows compatibility with the IBM CGA two-bank graphics mode.

0 Character row scan line counter bit 0 is substituted for memory address bit 13 during active display time
1 Normal operation, no substitution takes place

1 Select Row Scan Counter

This bit allows compatibility with Hercules graphics and with any other 4-bank graphics system.

0 Character row scan line counter bit 1 is substituted for memory address bit 14 during active display time
1 Normal operation, no substitution takes place

2 Vertical Sync Select

This bit controls the vertical resolution of the CRT Controller by permitting selection of the clock rate input to the vertical counters. When set to 1, the vertical counters are clocked by the horizontal retrace clock divided by 2.

3 Count By Two

0 Memory address counter is incremented every character clock
1 Memory address counter is incremented every two character clocks, used in conjunction with bit 5 of 0Fh.

Note: This bit is used in conjunction with CR14 bit-5. The net effect is as follows:

CR14 Bit-5	CR17 Bit-3	Increment Addressing Every
0	0	1 CCLK
0	1	2 CCLK
1	0	4 CCLK
1	1	2 CCLK

Note: In Hercules graphics and Hi-res CGA modes, address inrements every two clocks.

4 Reserved (0)

5 Address Wrap (effective only in word mode)

0 Wrap display memory address at 16 Kbytes. Used in IBM CGA mode.
1 Normal operation (extended mode).

6 Word Mode or Byte Mode

0 Select Word Mode. In this mode the display memory address counter bits are shifted down by one, causing the most-significant bit of the counter to appear on the least-significant bit of the display memory address output
1 Select byte mode

Note: This bit is used in conjunction with CR14 bit-6 to select byte, word, or double word memory addressing as follows:

CR14 Bit-6	CR17 Bit-6	Addressing Mode
0	0	Word Mode
0	1	Byte Mode
1	0	Double Word Mode
1	1	Double Word Mode

Display memory addresses are affected as shown in the table on the following page.

7 Hardware Reset

0 Force HSYNC and VSYNC inactive. No other registers or outputs affected.
1 Normal Operation

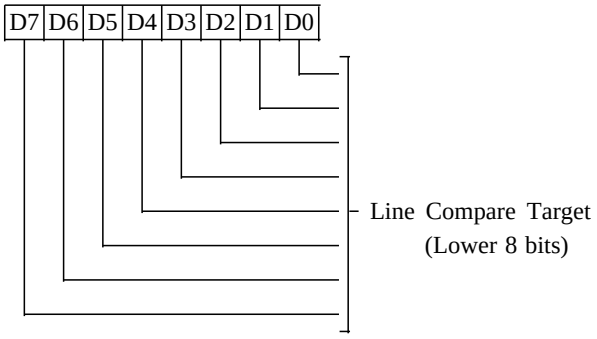
This bit is cleared by RESET.

Display memory addresses are affected by CR17 bit 6 as shown in the table below:

Logical Memory Address	Physical Memory Address Byte Mode	Word Mode	Double Word Mode
MA00	A00	Note 1	Note 2
MA01	A01	A00	Note 3
MA02	A02	A01	A00
MA03	A03	A02	A01
MA04	A04	A03	A02
MA05	A05	A04	A03
MA06	A06	A05	A04
MA07	A07	A06	A05
MA08	A08	A07	A06
MA09	A09	A08	A07
MA10	A10	A09	A08
MA11	A11	A10	A09
MA12	A12	A11	A10
MA13	A13	A12	A11
MA14	A14	A13	A12
MA15	A15	A14	A13

Note 1 = A13 * NOT CR17 bit 5
+ A15 * CR17 bit 5
Note 2 = A12 xor (A14 * XR04 bit 2)
Note 3 = A13 xor (A15 * XR04 bit 2)

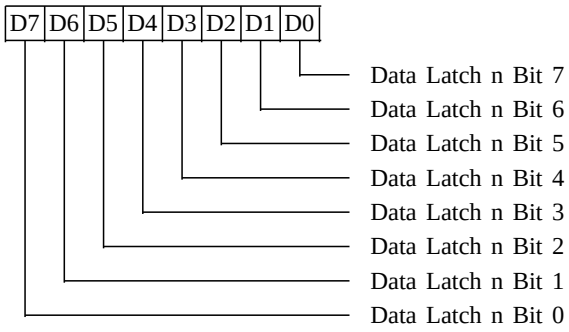
LINE COMPARE REGISTER (CR18)
Read/Write at I/O Address 3B5h/3D5h
Index 18h
Group 3 Protection



7-0 Line Compare Target

These are the low order 8 bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers, respectively. This register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address counter is cleared to 0. The display memory address counter then sequentially addresses the display memory starting at address 0. Each subsequent row address is generated by the addition of the Offset Register contents. This register is not affected by the double scanning bit (CR09 bit 7).

MEMORY DATA LATCH REGISTER (CR22)
Read only at I/O Address 3B5h/3D5h
Index 22h

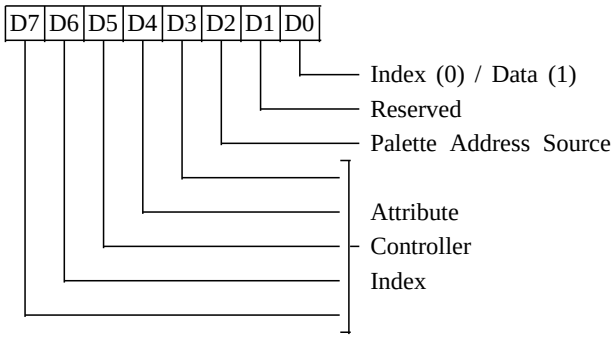


This register may be used to read the state of Graphics Controller Memory Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (GR04 bits 0–1) and is in the range 0–3.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

ATTRIBUTE CONTROLLER TOGGLE REGISTER (CR24)
Read only at I/O Address 3B5h/3D5h
Index 24h

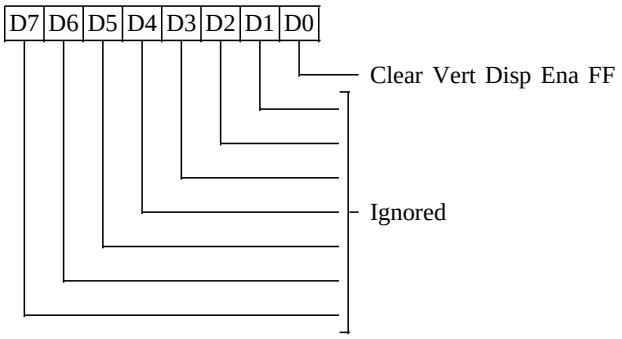


This register may be used to read back the state of the attribute controller index/data latch.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

CLEAR VERTICAL DISPLAY ENABLE FFh (CR3X)
Write only at I/O Address 3B5h/3D5h
Index 3xh



Writing odd data values to CRTC index 30-3Fh causes the vertical display enable flip-flop to be cleared. The flip-flop is automatically set by reaching vertical total. The effect of this is to force a longer vertical retrace period. There are two side effects of terminating vertical display enable early: first, the screen blanks early for one frame causing a minor visual disturbance and second, the sequencer gives more display memory cycles to the CPU because vertical display is not enabled.

Reads from this register are not decoded and will return indeterminate data.

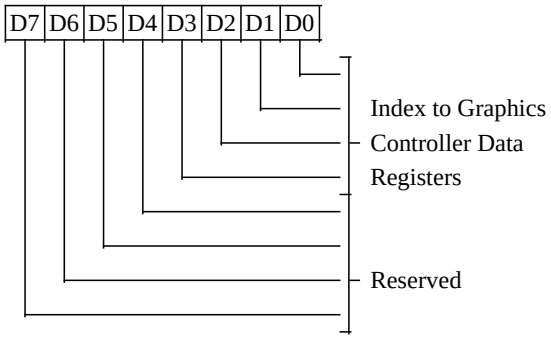
This is a standard VGA register which was not documented by IBM.

Graphics Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
GRX	Graphics Index	–	RW	3CEh	1	59
GR00	Set/Reset	00h	RW	3CFh	1	59
GR01	Enable Set/Reset	01h	RW	3CFh	1	60
GR02	Color Compare	02h	RW	3CFh	1	60
GR03	Data Rotate	03h	RW	3CFh	1	61
GR04	Read Map Select	04h	RW	3CFh	1	61
GR05	Graphics mode	05h	RW	3CFh	1	62
GR06	Miscellaneous	06h	RW	3CFh	1	64
GR07	Color Don't Care	07h	RW	3CFh	1	64
GR08	Bit Mask	08h	RW	3CFh	1	65

GRAPHICS CONTROLLER INDEX REGISTER (GRX)

Write only at I/O Address 3CEh
Group 1 Protection

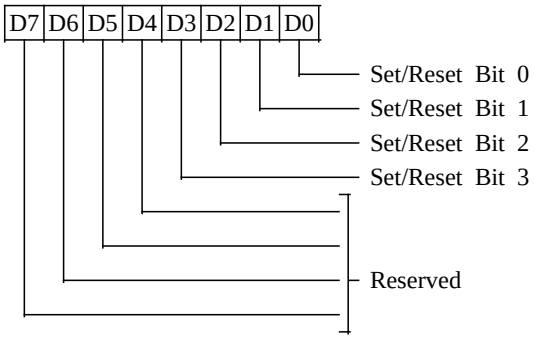


3-0 4-bit Index to Graphics Controller Registers

7-4 Reserved (0)

SET/RESET REGISTER (GR00)

Read/Write at I/O Address 3CFh
Index 00h
Group 1 Protection



The SET/RESET and ENABLE SET/RESET registers are used to 'expand' 8 bits of CPU data to 32 bits of display memory.

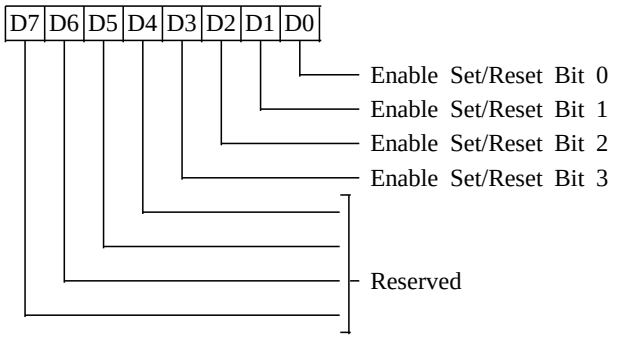
3-0 Set / Reset Planes 3-0

When the Graphics Mode register selects Write Mode 0, all 8 bits of each display memory plane are set as specified in the corresponding bit in this register. The Enable Set/Reset register (GR01) allows selection of some of the source of data to be written to individual planes. In Write Mode 3 (see GR05), these bits determine the color value.

7-4 Reserved (0)

ENABLE SET/RESET REGISTER (GR01)

Read/Write at I/O Address 3CFh
Index 01h
Group 1 Protection



3-0 Enable Set / Reset Planes 3-0

This register works in conjunction with the Set/Reset register (GR00). The Graphics Mode register must be programmed to Write Mode 0 in order for this register to have any effect.

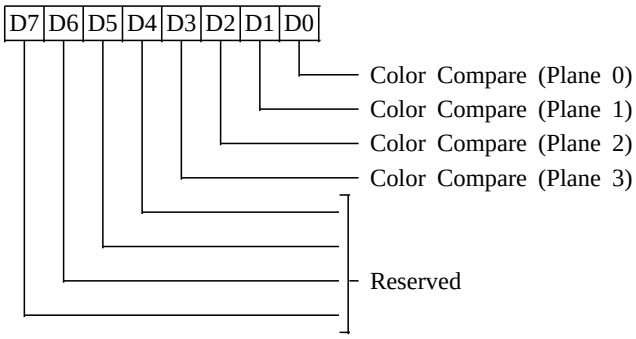
0 The corresponding plane is written with the data from the CPU data bus

1 The corresponding plane is set to 0 or 1 as specified in the Set/Reset Register

7-4 Reserved (0)

COLOR COMPARE REGISTER (GR02)

Read/Write at I/O Address 3CFh
Index 02h
Group 1 Protection



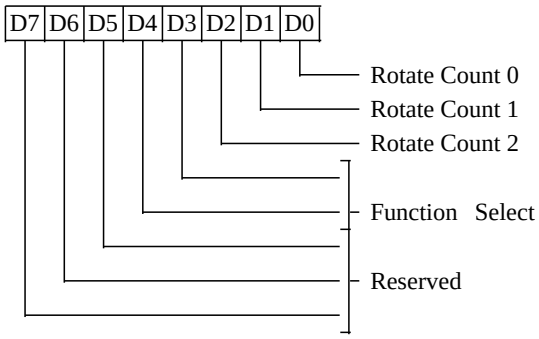
3-0 Color Compare Planes 3-0

This register is used to 'reduce' 32 bits of memory data to 8 bits for the CPU in 4-plane graphics mode. These bits provide a reference color value to compare to data read from display memory planes 0-3. The Color Don't Care register (GR07) is used to affect the result. This register is active only if the Graphics Mode register (GR05) is set to Read Mode 1. A match between the memory data and the Color Compare register (GR02) (for the bits specified in the Color Don't Care register) causes a logical 1 to be placed on the CPU data bus for the corresponding data bit; a mis-match returns a logical 0.

7-4 Reserved (0)

DATA ROTATE REGISTER (GR03)

Read/Write at I/O Address 3CFh
Index 03h
Group 1 Protection



2-0 Data Rotate Count

These bits specify the number of bits to rotate to the right the data being written by the CPU. The CPU data bits are first rotated, then subjected to the logical operation as specified in the Function Select bit field. The rotate function is active only if the Graphics Mode register is programmed for Write Mode 0.

4-3 Function Select

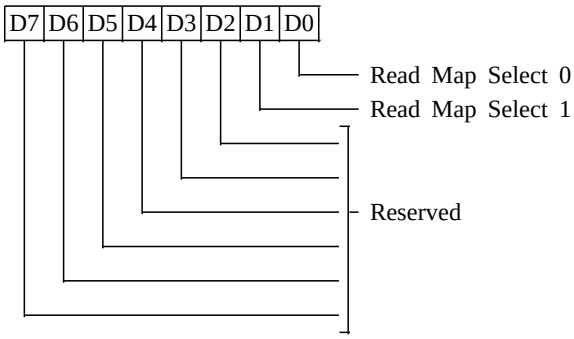
These Function Select bits specify the logical function performed on the contents of the processor latches (loaded on a previous CPU read cycle) before the data is written to display memory. These bits operate as follows:

Bit 4	Bit 3	Result
0	0	No change to the Data, Latches are updated
0	1	Logical 'AND' between Data and latched data
1	0	Logical 'OR' between Data and latched data
1	1	Logical 'XOR' between Data and latched data

7-5 Reserved (0)

READ MAP SELECT REGISTER (GR04)

Read/Write at I/O Address 3CFh
Index 04h
Group 1 Protection



1-0 Read Map Select

This register is also used to 'reduce' 32 bits of memory data to 8 bits for the CPU in the 4-plane graphics mode. These bits select the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even mode, bit-0 is ignored. In Quad mode, bits 0 and 1 are both ignored.

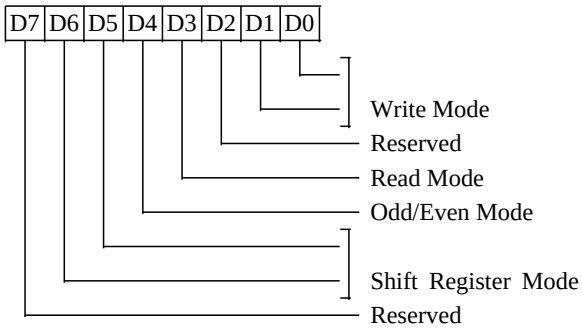
The four memory maps are selected as follows:

Bit 1	Bit 0	Map Selected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

7-2 Reserved (0)

GRAPHICS MODE REGISTER (GR05)

Read/Write at I/O Address 3CFh
Index 05h
Group 1 Protection



1-0 Write Mode

For 16-bit writes, the operation is repeated on the lower and upper bytes of CPU data.

1	0	Write Mode
0	0	**Write mode 0**. Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.
0	1	**Write mode 1**. Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.
1	0	**Write mode 2**. The CPU data bus data is treated as the color value for the addressed byte in planes 0-3. All eight pixels in the addressed byte are modified unless protected by the Bit Mask register setting. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset and Enable Set/Reset registers are ignored. The Function Select bits in the Data Rotate register are used.
1	1	**Write mode 3**. The CPU data is rotated then logically ANDed with the contents of the Bit Mask register (GR08) and then treated as the addressed data's bit mask, while the contents of the Set/Reset register is treated as the color value. A '0' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the corresponding pixel in the processor latches. A '1' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the color value specified in the Set/Reset register. The Enable Set/Reset register is ignored. The Data Rotate is used. This write mode can be used to fill an area with a single color and pattern.

2 Reserved (0)

3 Read Mode

0 The CPU reads data from one of the planes as selected in the Read Map Select register.

1 The CPU reads the 8-bit result of the logical comparison between all eight pixels in the four display planes and the contents of the Color Compare and Color Don't Care registers. The CPU reads a logical 1 if a match occurs for each pixel and logical 0 if a mis-match occurs. In 16-bit read cycles, this operation is repeated on the lower and upper bytes.

(Continued on following page)

4 Odd/Even Mode

0 All CPU addresses sequentially access all planes

1 Even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for compatibility with the IBM CGA memory organization.

6-5 Shift Register Mode

These two bits select the data shift pattern used when passing data from the four memory planes through the four video shift registers. If data bits 0-7 in memory planes 0-3 are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7 respectively, then the data in the serial shift registers is shifted out as follows:

65	Last Bit Shifted Out			Shift Direction →				1st Bit Shifted Out	Output to:
00:	M0D0	M0D1	M0D2	M0D3	M0D4	M0D5	M0D6	M0D7	Bit 0
	M1D0	M1D1	M1D2	M1D3	M1D4	M1D5	M1D6	M1D7	Bit 1
	M2D0	M2D1	M2D2	M2D3	M2D4	M2D5	M2D6	M2D7	Bit 2
	M3D0	M3D1	M3D2	M3D3	M3D4	M3D5	M3D6	M3D7	Bit 3
01:	M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	Bit 0
	M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	Bit 1
	M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	Bit 2
	M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	Bit 3
1x:	M3D0	M3D4	M2D0	M2D4	M1D0	M1D4	M0D0	M0D4	Bit 0
	M3D1	M3D5	M2D1	M2D5	M1D1	M1D5	M0D1	M0D5	Bit 1
	M3D2	M2D6	M3D2	M2D6	M1D2	M1D6	M0D2	M0D6	Bit 2
	M3D3	M3D7	M2D3	M2D7	M1D3	M1D7	M0D3	M0D7	Bit 3

Note: If the Shift Register is not loaded every character clock (see SR01 bits 2&4) then the four 8-bit shift registers are effectively 'chained' with the output of shift register 1 becoming the input to shift register 0 and so on. This allows one to have a large monochrome (or 4 color) bit map and display one portion thereof.

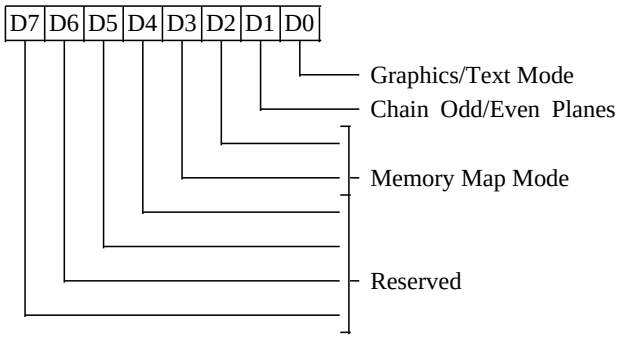
Note: If XR28 bit-4 is set (8-bit video path), GR05 bit-6 must be set to 0:

0x and XR28 bit-4=1:					
	M3D0	M2D0	M1D0	M0D0	Bit 0
	M3D1	M2D1	M1D1	M0D1	Bit 1
	M3D2	M2D2	M1D2	M0D2	Bit 2
	M3D3	M2D3	M1D3	M0D3	Bit 3
	M3D4	M2D4	M1D4	M0D4	Bit 4
	M3D5	M2D5	M1D5	M0D5	Bit 5
	M3D6	M2D6	M1D6	M0D6	Bit 6
	M3D7	M2D7	M1D7	M0D7	Bit 7

7 Reserved (0)

MISCELLANEOUS REGISTER (GR06)

Read/Write at I/O Address 3CFh
Index 06h
Group 1 Protection



0 Graphics/Text Mode

0 Text Mode
1 Graphics mode

1 Chain Odd/Even Planes

This mode can be used to double the address space into display memory.

1 CPU address bit A0 is replaced by a higher order address bit. The state of A0 determines which memory plane is to be selected:

A0 = 0: select planes 0 and 2
A0 = 1: select planes 1 and 3

0 A0 not replaced

3-2 Memory Map Mode

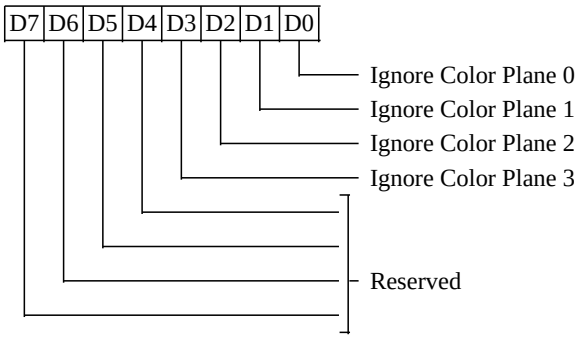
These bits control the mapping of the display memory into the CPU address space as follows (also used in extended modes):

Bit 3	Bit 2	CPU Address
0	0	A0000h-BFFFFh
0	1	A0000h-AFFFFh
1	0	B0000h-B7FFFh
1	1	B8000h-BFFFFh

7-4 Reserved (0)

COLOR DON'T CARE REGISTER (GR07)

Read/Write at I/O Address 3CFh
Index 07h
Group 1 Protection



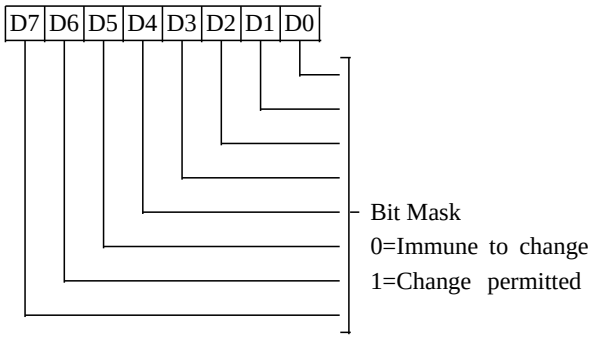
3-0 Ignore Color Plane (3-0)

0 This causes the corresponding bit of the Color Compare register to be a don't care during a comparison.

1 The corresponding bit of the Color Compare register is enabled for color comparison. This register is active in Read Mode 1 only.

7-4 Reserved (0)

BIT MASK REGISTER (GR08)
Read/Write at I/O Address 3CFh
Index 08h
Group 1 Protection



7-0 Bit Mask

This bit mask is applicable to any data written by the CPU, including that subject to a rotate, logical function (AND, OR, XOR), Set/Reset, and No Change. In order to execute a proper read-modify-write cycle into displayed memory, each byte must first be read (and latched by the VGA), the Bit Mask register set, and the new data then written. The bit mask applies to all four planes simultaneously.

0 The corresponding bit in each of the four memory planes is written from the corresponding bit in the latches

1 Unrestricted manipulation of the corresponding data bit in each of the four memory planes is permitted

Attribute Controller and VGA Color Palette Registers

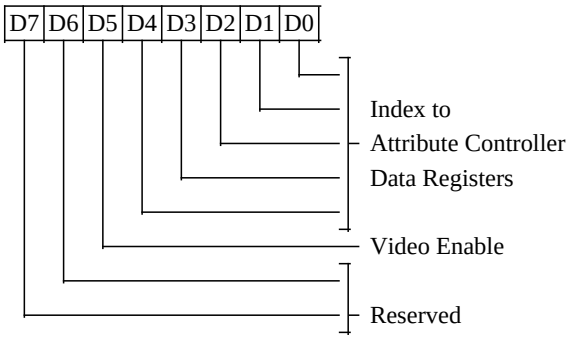
Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ARX	Attribute Index (for 3C0/3C1h)	–	RW	3C0h	1	67
AR00-AR0F	Attribute Controller Color Data	00-0Fh	RW	3C0h/3C1h	1	68
AR10	Mode Control	10h	RW	3C0h/3C1h	1	68
AR11	Overscan Color	11h	RW	3C0h/3C1h	1	69
AR12	Color Plane Enable	12h	RW	3C0h/3C1h	1	69
AR13	Horizontal Pixel Panning	13h	RW	3C0h/3C1h	1	70
AR14	Pixel Pad	14h	RW	3C0h/3C1h	1	70
DACMASK	Color Palette Pixel Mask	–	RW	3C6h	6	71
DACSTATE	Color Palette State	–	R	3C7h	–	71
DACRX	Color Palette Read-Mode Index	–	W	3C7h	6	72
DACX	Color Palette Index (for 3C9h)	–	RW	3C8h	6	72
DACDATA	Color Palette Data	00-FFh	RW	3C9h	6	72

In regular VGA mode, all Attribute Controller registers are located at the same byte address (3C0h) in the CPU I/O space. An internal flip-flop controls the selection of either the Attribute Index or Data Registers. To select the Index Register, an I/O Read is executed to address 3BAh/3DAh to clear this flip-flop. After the Index Register has been loaded by an I/O Write to address 3C0h, this flip-flop toggles, and the Data Register is ready to be accessed. Every I/O Write to address 3C0h toggles this flip-flop. The flip-flop does not have any effect on the reading of the Attribute Controller registers. The Attribute Controller index register is always read back at address 3C0h, the data register is always read back at address 3C1h.

In one of the extended modes (See "CPU Interface Register"), the Attribute Controller Index register is located at address 3C0h and the Attribute Controller Data register is located at address 3C1h (to allow word I/O accesses). In another extended mode, the Attribute Controller can be both read and written at either 3C0h or 3C1h (EGA compatible mode).

The VGA color palette logic is used to further modify the video color output following the attribute controller color registers. The color palette logic is contained on-chip, however an external color palette chip may still be used by disabling the internal color palette (see XR06). DAC logic is provided on-chip (or in the external 'RAMDAC' chip if used) to convert the final video output of the color palette to analog RGB outputs for use in driving a CRT display.

ATTRIBUTE INDEX REGISTER (ARX)
Read/Write at I/O Address 3C0h
Group 1 Protection



4-0 Attribute Controller Index

These bits point to one of the internal registers of the Attribute Controller.

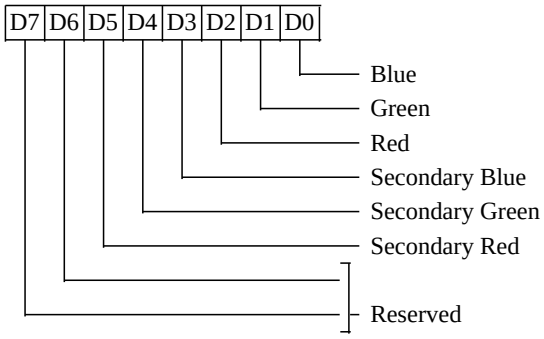
5 Enable Video

0 Disable video, allowing the Attribute Controller Color registers to be accessed by the CPU

1 Enable video, causing the Attribute Controller Color registers (AR00-AR0F) to be inaccessible to the CPU

7-6 Reserved (0)

ATTRIBUTE CONTROLLER COLOR REGISTERS (AR00-AR0F)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 00-0Fh
Group 1 Protection or XR63 bit-6

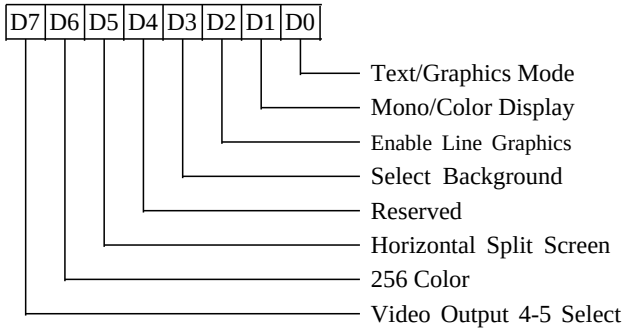


5-0 Color Value

These bits are the color value in the respective attribute controller color register as pointed to by the attribute index register.

7-6 Reserved (0)

ATTRIBUTE CONTROLLER MODE CONTROL REGISTER (AR10)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 10h
Group 1 Protection



0 Text/Graphics Mode

0 Select text mode
1 Select graphics mode

1 Monochrome/Color Display

0 Select color display attributes
1 Select mono display attributes

2 Enable Line Graphics Character Codes

This bit is dependent on bit 0 of the Override register.

0 Make the ninth pixel appear the same as the background

1 For special line graphics character codes (0C0h-0DFh), make the ninth pixel identical to the eighth pixel of the character. For other characters, the ninth pixel is the same as the background.

3 Enable Blink/Select Background Intensity

The blinking counter is clocked by the VSYNC signal. The Blink frequency is defined in the Blink Rate Control Register (XR60).

0 Disable Blinking and enable text mode background intensity

1 Enable the blink attribute in text and graphics modes.

4 Reserved (0)

5 Split Screen Horizontal Panning Mode

0 Scroll both screens horizontally as specified in the Pixel Panning register

1 Scroll horizontally only the top screen as specified in the Pixel panning register

6 256 Color Output Assembler

0 6-bits of video (translated from 4-bits by the internal color palette) are output every dot clock

1 Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot clock (256 color mode).

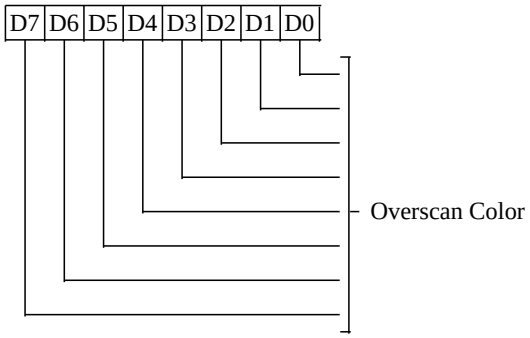
7 Video Output 5-4 Select

0 Video bits 4 and 5 are generated by the internal Attribute Controller color palette registers

1 Video bits 4 and 5 are the same as bits 0 and 1 in the Pixel Pad register (AR14)

OVERSCAN COLOR REGISTER (AR11)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 11H
Group 1 Protection



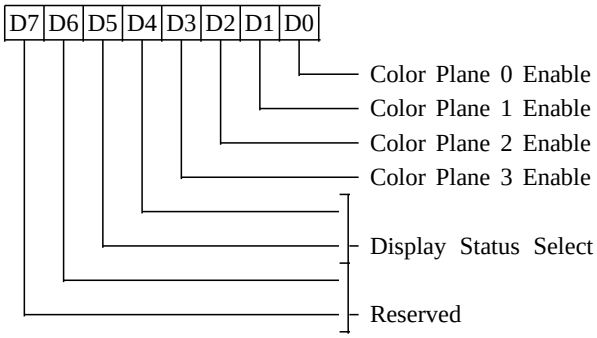
7-0 Overscan Color

These 8 bits define the overscan (border) color value. For monochrome displays, these bits should be zero.

The border color is displayed in the interval after Display Enable End and before Blank Start (end of display area; i.e. right side and bottom of screen) and between Blank End and Display Enable Start (beginning of display area; i.e. left side and top of screen).

COLOR PLANE ENABLE REGISTER (AR12)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 12h
Group 1 Protection



3-0 Color Plane (3-0) Enable

0 Force the corresponding color plane pixel bit to 0 before it addresses the color palette

1 Enable the plane data bit of the corresponding color plane to pass

5-4 Display Status Select

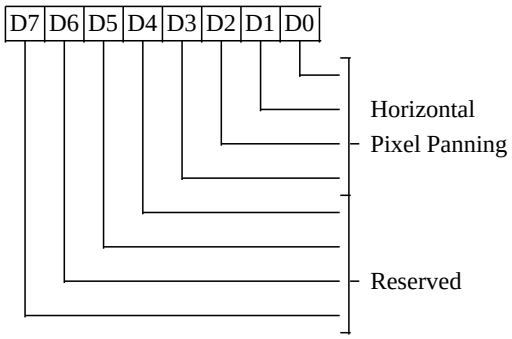
These bits select two of the eight color outputs to be read back in the Input Status Register 1 (port 3BAh or 3DAh). The output color combinations available on the status bits are as follows:

		Status Register 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

7-6 Reserved (0)

ATTRIBUTE CONTROLLER HORIZONTAL PIXEL PANNING REGISTER (AR13)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 13h
Group 1 Protection



3-0 Horizontal Pixel Panning

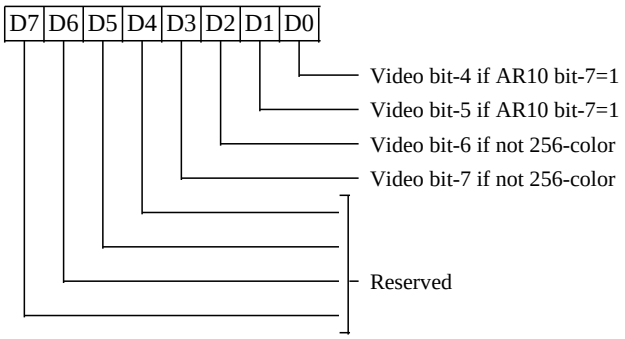
These bits select the number of pixels to shift the display horizontally to the left. Pixel panning is available in both text and graphics modes. In 9 pixel/character text mode, the output can be shifted a maximum of 9 pixels. In 8 pixel/character text mode and all graphics modes a maximum shift of 8 pixels is possible. In 256-color mode (output assembler AR10 bit-6 = 1), bit 0 of this register must be 0 which results in only 4 panning positions per display byte. In Shift Load 2 and Shift Load 4 modes, register CR08 provides single pixel resolution for panning. Panning is controlled as follows:

	Number of Pixels Shifted		
AR13	9-dot mode	8-dot mode	256-color mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7-4 Reserved (0)

ATTRIBUTE CONTROLLER PIXEL PAD REGISTER (AR14)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 14h
Group 1 Protection



1-0 Video Bits 5-4

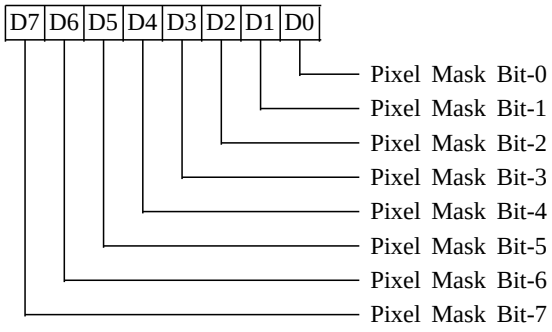
These bits are output as video bits 5 and 4 when AR10 bit-7 = 1. They are disabled in the 256 color mode.

3-2 Video Bits 7-6

These bits are output as video bits 7 and 6 in all modes except 256-color mode.

7-4 Reserved (0)

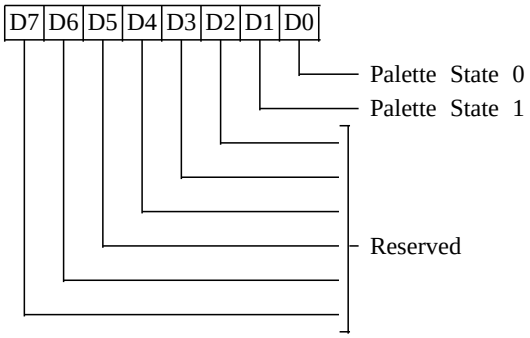
COLOR PALETTE
PIXEL MASK REGISTER (DACMASK)
Read/Write at I/O Address 3C6h
Group 6 Protection



The contents of this register are logically ANDed with the 8 bits of video data coming into the color palette. Zero bits in this register therefore cause the corresponding address input to the color palette to be zero. For example, if this register is programmed with 7, only color palette registers 0-7 would be accessible; video output bits 3-7 would be ignored and all color values would map into the lower 8 locations in the color palette.

This register is physically located on-chip (the chip will respond directly if the internal color palette is enabled). This register is also implemented in external color palette chips (RAMDACs) and the external copy will be used if an external RAMDAC is used instead (the on-chip mask register will be ignored if the internal color palette is disabled). Reads from this I/O location cause the PALRD/ pin to be asserted if the internal color palette is disabled. Writes to this I/O location cause the PALWR/ pin to be asserted if the internal color palette is disabled. If the internal color palette is disabled, the functionality of this port is therefore determined by the external palette chip.

COLOR PALETTE
STATE REGISTER (DACSTATE)
Read only at I/O Address 3C7h



1-0 Palette State 1-0

Status bits indicate the I/O address of the last CPU write to the Color Palette:

00 The last write was to 3C8h (write mode)

11 The last write was to 3C7h (read mode)

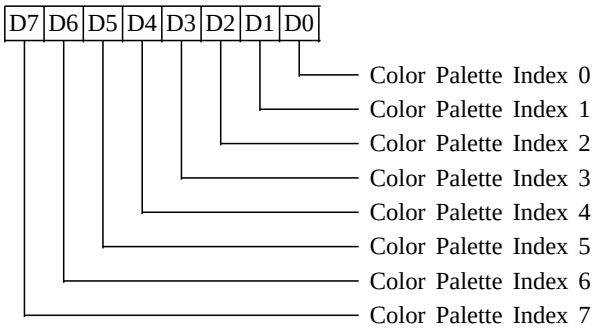
7-2 Reserved (0)

To allow saving and restoring the state of the video subsystem, this register is required since the color palette index register is automatically incremented differently depending on whether the index is written at 3C7h or 3C8h.

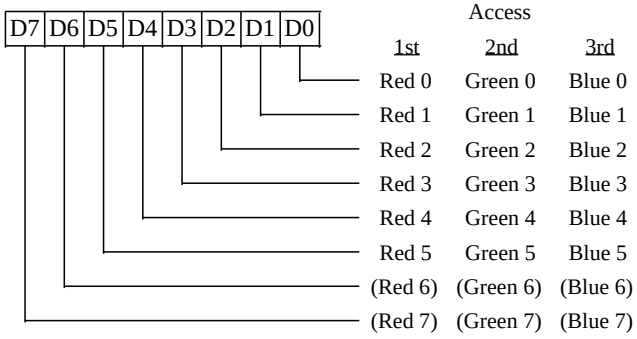
This register is physically located on-chip (PALRD/ is *not* asserted for reads from this I/O address independent of whether the internal palette is enabled or disabled).

COLOR PALETTE
READ-MODE INDEX REGISTER (DACRX)
Write only at I/O Address 3C7h
Group 6 Protection

COLOR PALETTE
INDEX REGISTER (DACX)
Read/Write at I/O Address 3C8h
Group 6 Protection



COLOR PALETTE
DATA REGISTERS (DACDATA 00-FF)
Read/Write at I/O Address 3C9h
Index 00h-FFh
Group 6 Protection



The color palette index and data registers are physically located on-chip and in the external color palette chip if one is used. Which set of registers is used depends on whether the on-chip color palette is enabled. If the on-chip palette is enabled, PALRD/ and PALWR/ are never active. If the on-chip color palette is disabled, PALRD/ and PALWR/ are active on I/O reads and writes respectively to enable the external palette chip.

In either case, the index register is used to point to one of 256 data registers. Each data register is either 18 or 24 bits in length depending on the type of palette chip used (6 or 8 bits each for red, green, and blue), so the data values must be read as a sequence of 3 bytes. After writing the index register (3C7h or 3C8h), data values may be read from or written to the color palette data register port (3C9h) in sequence: first red, then green, then blue, then repeat for the next location if desired (the index is incremented automatically by the palette logic).

The index may be written at 3C7h and may be read or written at 3C8h. When the index value is written to either port, it is written to both the index register and a 'save' register. The save register (not the index register) is used by the palette logic to point at the current data register. When the index value is written to 3C7h (**read mode**), it is written to both the index register and the save register, then the index register is automatically incremented. When the index value is written to 3C8h (**write mode**), the automatic incrementing of the index register does not occur.

After the third of the three sequential data reads from (or writes to) 3C9h is completed, the save and index registers are both automatically incremented by the palette logic. This allows the entire palette (or any subset) to be read (written) by writing the index of the first color in the set, then sequentially reading (writing) the values for each color, without having to reload the index every three bytes.

The state of the RGB sequence is not saved; the user must access each three bytes in an uninterruptable sequence (or be assured that interrupt service routines will not access the palette index or data registers). When the index register is written (at either port), the RGB sequence is restarted. Data value reads and writes may be intermixed; either reads or writes increment the palette logic's RGB sequence counter.

The palette's save register always contains a value one less than the readable index value if the last index write was to the 'read mode' port. The state is saved for which port (3C7h or 3C8h) was last written and that information is returned on reads from 3C7h (PALRD/ is only asserted on reads from 3C8h and not on reads from 3C7h if the internal palette is disabled). Writes to 3C7h or 3C8h cause the PALWR/ pin to be asserted if the on-chip palette is disabled.

If the on-chip color palette is disabled, the functionality of the index and data ports is determined by the external palette chip.

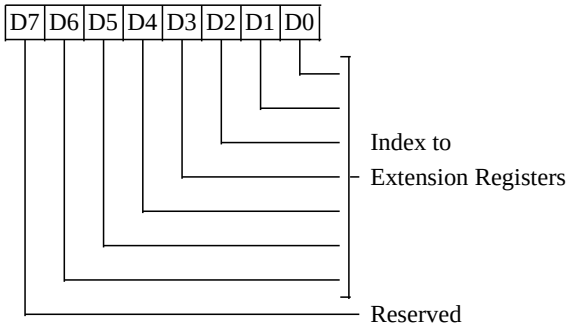
Extension Registers

Register Mnemonic	Register Group	Extension Register Name	Index	I/O Access	Address	State After Reset	Page
XRX	--	Extension Index	--	RW	3D6h	- x x x x x x x	74
XR00	Misc	Chip Version	00h	RO	3D7h	1 0 0 1 r r r r	74
XR01	Misc	Configuration	01h	RO	3D7h	d d d d d d d d	75
XR02	Misc	CPU Interface	02h	RW	3D7h	0 - 0 0 0 - 0 -	75
XR04	Misc	Memory Control	04h	RW	3D7h	- - 0 0 - 0 - -	76
XR06	Misc	Palette Control	06h	RW	3D7h	0 0 0 - - - - -	76
XR0D	Misc	Auxiliary Offset	0Dh	RW	3D7h	- - - - - - 0 0	78
XR0E	Misc	Text Mode Control	0Eh	RW	3D7h	- - - - 0 0 - -	78
XR0F	Misc	Software Flags 2	0Fh	R/W	3D7h	x x x x x x x x	78
XR28	Misc	Video Interface	28h	RW	3D7h	- 0 - 0 - 0 - -	87
XR2B	Misc	Default Video	2Bh	RW	3D7h	0 0 0 0 0 0 0 0	88
XR44	Misc	Software Flags	44h	RW	3D7h	x x x x x x x x	90
XR70	Misc	Setup / Disable Control	70h	RW	3D7h	0 - - - - - - -	106
XR7F	Misc	Diagnostic	7Fh	RW	3D7h	0 0 x x x x 0 0	107
XR0B	Mapping	CPU Paging	0Bh	RW	3D7h	- - - 0 - 0 0 0	77
XR0C	Mapping	Start Address Top	0Ch	RW	3D7h	- - - - - - - 0	77
XR10	Mapping	Single/Low Map	10h	RW	3D7h	x x x x x x x x	79
XR11	Mapping	High Map	11h	RW	3D7h	x x x x x x x x	79
XR14	Compatibility	Emulation Mode	14h	RW	3D7h	0 0 0 0 h h 0 0	80
XR15	Compatibility	Write Protect	15h	RW	3D7h	0 0 0 0 0 0 0 0	81
XR1F	Compatibility	Virtual EGA Switch	1Fh	RW	3D7h	0 - - - x x x x	85
XR7E	Compatibility	CGA/Hercules Color Select	7Eh	RW	3D7h	- - x x x x x x	107
XR18	Alternate	FP Horizontal Display End	18h	RW	3D7h	x x x x x x x x	82
XR19	Alternate	FP H Sync Start / Half Line Compare	19h	RW	3D7h	x x x x x x x x	82
XR1A	Alternate	FP Horizontal Sync End	1Ah	RW	3D7h	- - - x x x x x	83
XR1B	Alternate	FP Horizontal Total	1Bh	RW	3D7h	x x x x x x x x	83
XR1C	Alternate	FP H Blank Start / H Panel Size	1Ch	RW	3D7h	x x x x x x x x	84
XR1D	Alternate	FP Horizontal Blank End	1Dh	RW	3D7h	- x x - - - - -	84
XR1E	Alternate	FP Offset	1Eh	RW	3D7h	x x x x x x x x	85
XR24	Flat Panel	FP Maximum Scan Line	24h	RW	3D7h	- - - x x x x x	86
XR2C	Flat Panel	Vertical Sync (FLM) Delay	2Ch	RW	3D7h	x x x x x x x x	88
XR2D	Flat Panel	Horizontal Sync (LP) Delay	2Dh	RW	3D7h	x x x x x x x x	89
XR2F	Flat Panel	Horizontal Sync (LP) Width	2Fh	RW	3D7h	x x x - x x x x	89
XR50	Flat Panel	Panel Format	50h	RW	3D7h	x x x x x x x x	91
XR51	Flat Panel	Display Type	51h	RW	3D7h	x x x x - 0 x x	92
XR52	Flat Panel	Power Down Control	52h	RW	3D7h	0 - 0 - 0 0 0 0	93
XR53	Flat Panel	Line Graphics Override	53h	RW	3D7h	- 0 - - x x - -	93
XR54	Flat Panel	Panel Interface	54h	RW	3D7h	x x - x x x x x	94
XR55	Flat Panel	Horizontal Compensation	55h	RW	3D7h	- x x - - x x x	95
XR56	Flat Panel	Horizontal Centering	56h	RW	3D7h	x x x x x x x x	96
XR57	Flat Panel	Vertical Compensation	57h	RW	3D7h	- x x x x x x x	97
XR58	Flat Panel	Vertical Centering	58h	RW	3D7h	x x x x x x x x	98
XR59	Flat Panel	Vertical Line Insertion	59h	RW	3D7h	- x x - x x x x	98
XR5A	Flat Panel	Vertical Line Replication	5Ah	RW	3D7h	- - - - x x x x	99
XR5B	Flat Panel	Panel Power Sequencing Delay	5Bh	RW	3D7h	0 1 1 1 0 0 0 1	99
XR5E	Flat Panel	ACDCLK Control	5Eh	RW	3D7h	x x x x x x x x	100
XR60	Flat Panel	Blink Rate Control	60h	RW	3D7h	1 0 0 0 0 0 1 1	100
XR61	Flat Panel	SmartMap™ Control	61h	RW	3D7h	x x x x x x x x	101
XR62	Flat Panel	SmartMap™ Shift Parameter	62h	RW	3D7h	x x x x x x x x	102
XR63	Flat Panel	SmartMap™ Color Mapping Control	63h	RW	3D7h	x - x x x x x x	102
XR64	Flat Panel	FP Vertical Total	64h	RW	3D7h	x x x x x x x x	103
XR65	Flat Panel	FP Overflow	65h	RW	3D7h	x x x - - x x x	103
XR66	Flat Panel	FP Vertical Sync Start	66h	RW	3D7h	x x x x x x x x	104
XR67	Flat Panel	FP Vertical Sync End	67h	RW	3D7h	- - - - x x x x	104
XR68	Flat Panel	Vertical Panel Size	68h	RW	3D7h	x x x x x x x x	105
XR6C	Flat Panel	Programmable Output Drive	6Ch	RW	3D7h	- - - 0 0 0 - 0	105
XR6E	Flat Panel	Polynomial FRC Control	6Eh	RW	3D7h	1 0 1 1 1 1 0 1	105
XR7D	Flat Panel	Compensation Diagnostic	7Dh	RO	3D7h	- - - - - - - -	106

Reset Codes:
x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
– = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
0/1 = Reset to 0 or 1 by falling edge of RESET

EXTENSION INDEX REGISTER (XRX)

Read/Write at I/O Address 3B6h/3D6h

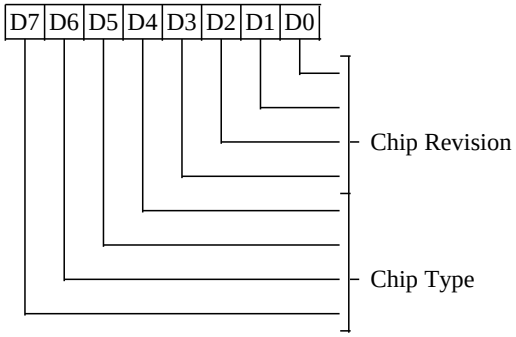


6-0 Index value used to access the extension registers

7 Reserved (0)

CHIPS VERSION REGISTER (XR00)

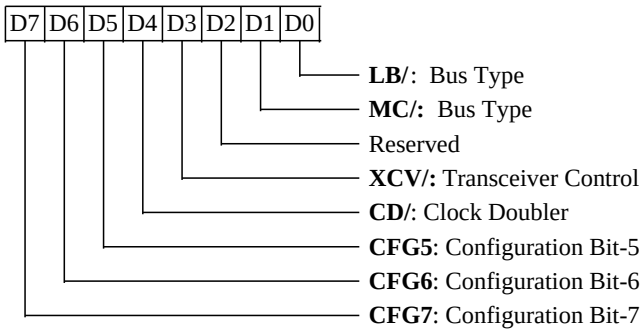
Read only at I/O Address 3B7h/3D7h
Index 00h



7-0 **Chip Version** - Chip Version starts at 90h and is incremented every silicon step.

CONFIGURATION REGISTER (XR01)

Read only at I/O Address 3B7h/3D7h
Index 01h



These bits latch the state of memory address bus (MA bus) bits 0-7 on the falling edge of RESET. The state of bits 0-4 after RESET effect chip internal logic as indicated below; bits 5-7 have no hardware effect on the chip. MA0-7 have on-chip high-value pullups which are enabled only at RESET.

This register is not related to the Virtual EGA Switch register (XR1F).

1-0 CPU Bus Type

00 PI bus
01 MC bus
10 Local Bus
11 ISA bus

2 Reserved

3 Transceiver Control

0 External Transceivers
(Pin 50 on F65510 is VGARD Output)
(Pin 48 on T65510 is VGARD Output)
1 No External Transceivers
(Pin 50 on F65510 is ENAVDD Output)
(Pin 48 on T65510 is ENAVDD Output)

4 Clock Doubler Control

0 Clock doubling enabled
(CLKIN = 14.318 MHz)
1 No Clock doubling
(CLKIN = 25-50 MHz)

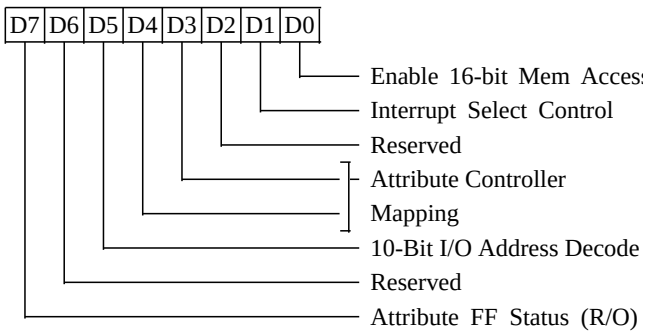
See also the explanation of the CLKIN input in the Pinouts section.

7-5 Configuration bits 7-5 (CFG7-5)

Latched from MA7-5 on the falling edge (end) of RESET and readable, but otherwise have no hardware effect. The 65510 has internal pull-ups on MA7-5 which are enabled only at RESET. The user may place external pull-downs on MA7-5 to use these bits as Reset configuration strap options.

CPU INTERFACE REGISTER (XR02)

Read/Write at I/O Address 3B7h/3D7h
Index 02h



0 8/16-bit CPU Memory Access

0 8-bit CPU memory access (default)
1 16-bit CPU memory access

1 Interrupt Select Control

0 Pin 49 (T65510) or Pin 51 (F65510) outputs ENAVEE Signal (default)
1 Pin 49 (T65510) or Pin 51 (F65510) outputs IRQ Signal

2 Reserved

4-3 Attribute Controller Mapping

00 Write Index and Data at 3C0h. (8-bit access only) (default - VGA mapping)
01 Write Index at 3C0h and Data at 3C1h (8-bit or 16-bit access). Attribute flip-flop (bit-7) is always reset in this mode (16-bit mapping)
10 Write Index and Data at 3C0h/3C1h (8-bit access only) (EGA mapping)
11 Reserved

5 I/O Address Decoding

0 Decode all 16 bits of I/O address (default)
1 Decode only lower 10 bits of I/O address. This affects the following addresses: 3B4h, 3B5h, 3B8h, 3BAh, 3BFh, 3C0h, 3C1h, 3C2h, 3C4h, 3C5h, 3CEh, 3CFh, 3D4h, 3D5h, 3D8h, 3D9h, and 3DAh.

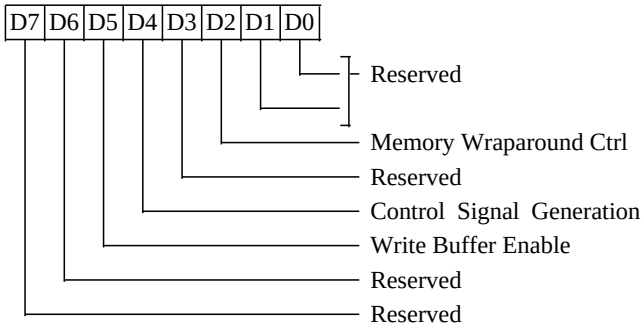
6 Reserved (*Must be programmed to 0*)

7 Attribute Flip-flop Status (read only)

0 = Index, 1 = Data

MEMORY CONTROL REGISTER (XR04)

Read/Write at I/O Address 3B7h/3D7h
Index 04h



1-0 Reserved ***(Must be programmed to 01)***

2 Memory Wraparound Control

This bit enables bit-16 of the CRT Controller address counter (default = 0 on reset).

0 Disable CRTC address counter bit-16
1 Enable CRTC address counter bit-16

3 Reserved ***(Must be programmed to 0)***

4 Control Signal Generation Select

0 2 CAS/, 1 WE/ 256Kx16 Memory Device
1 2 WE/, 1 CAS/ 256Kx16 Memory Device

5 CPU Memory Write Buffer

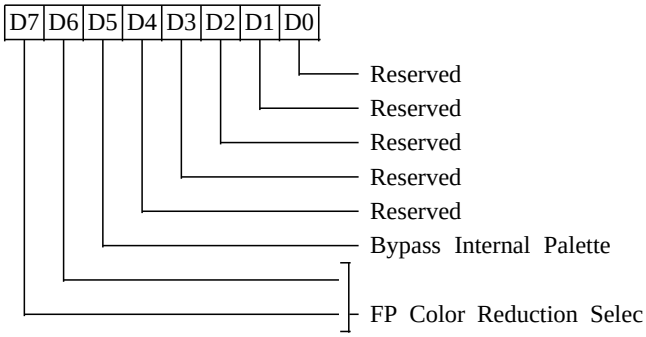
0 Disable CPU memory write buffer (default)
1 Enable CPU memory write buffer

6 Reserved

7 Reserved

PALETTE CONTROL REGISTER (XR06)

Read/Write at I/O Address 3B7h/3D7h
Index 06h



0 Reserved ***(Must be programmed to 0)***

1 Reserved ***(Must be programmed to 0)***

2 Reserved ***(Must be programmed to 0)***

3 Reserved ***(Must be programmed to 0)***

4 Reserved ***(Must be programmed to 1)***

5 Bypass Internal Palette (Test Mode only)

This is a test bit and should not be set. This feature is necessary for testing the FRC logic.

0 Use internal Palette. Internal palette output consists of 6 bits/pixel. Default on reset.
1 Bypass internal Palette. The input to the FRC logic consists of the least significant 6 bits of the 8-bit video data.

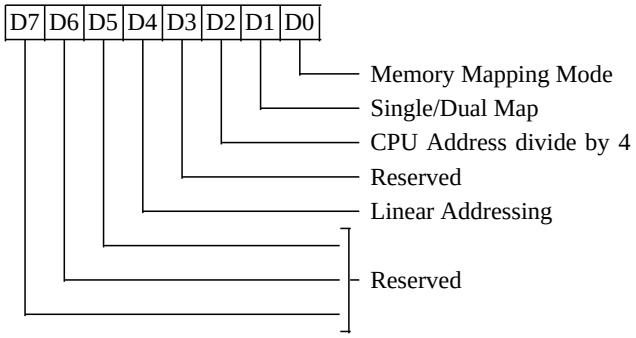
7-6 Color Reduction Select

These bits are effective in flat panel mode. These bits select the algorithm used to reduce 18-bit palette color data to 6-bit color data for monochrome panels.

00 NTSC weighting algorithm (default)
01 Equivalent weighting algorithm
10 Green only
11 Reserved

CPU PAGING REGISTER (XR0B)

Read/Write at I/O Address 3B7h/3D7h
Index 0Bh



0 Memory Mapping Mode

0 Normal Mode (VGA compatible) (default on Reset)
1 Extended Mode (mapping for > 256 KByte memory configurations)

1 CPU Single/Dual Mapping

0 CPU uses only a single map to access the extended video memory space (default on Reset)
1 CPU uses two maps to access the extended video memory space. The base addresses for the two maps are defined in the Low Map Register (XR10) and High Map Register (XR11).

2 CPU address Divide by 4

0 Disable divide by 4 for CPU addresses (default on Reset)
1 Enable divide by 4 for CPU addresses. This allows the video memory to be accessed sequentially in mode 13. In addition, all video memory is available in mode 13 by setting this bit.

3 Reserved

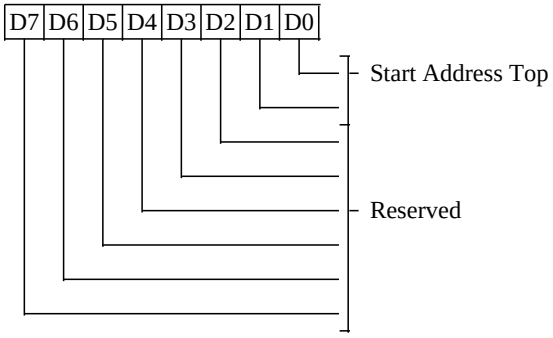
4 Linear Addressing

0 Standard VGA (A0000 - BFFFF) memory space decoded on-chip using A17-19 (default on Reset)
1 Linear Addressing (0.5 MB using A0-18)

7-5 Reserved (0)

START ADDRESS TOP REGISTER (XR0C)

Read/Write at I/O Address 3B7h/3D7h
Index 0Ch



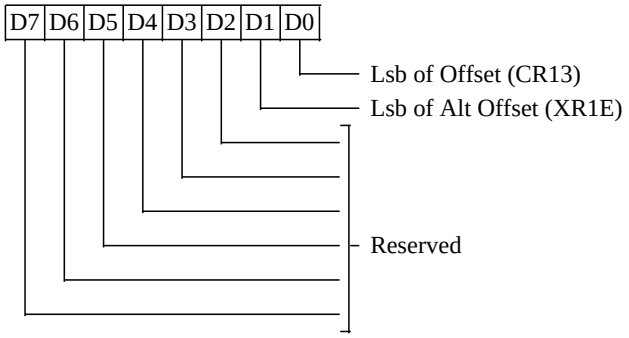
0 Start Address Top

This bit defines the high order bit for the Display Start Address when 512 KBytes of memory is used.

7-1 Reserved ***(Must be programmed to 0)***

AUXILIARY OFFSET REGISTER (XR0D)

Read/Write at I/O Address 3B7h/3D7h
Index 0Dh



0 Offset Register LSB

This bit provides finer granularity to the display memory address offset when word and doubleword modes are used. This bit is used with the regular Offset register (CR13).

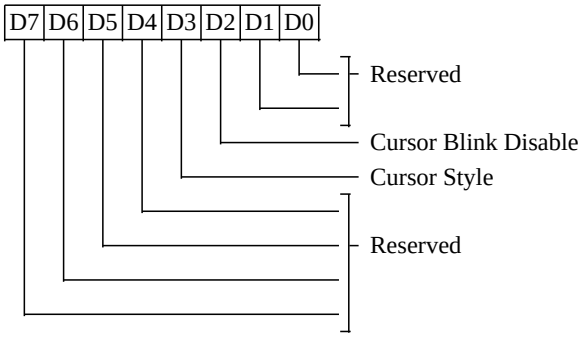
1 Alternate Offset Register LSB

This bit provides finer granularity to the display memory address offset when word and doubleword modes are used. This bit is used with the Alternate Offset register (XR1E).

7-2 Reserved (0)

TEXT MODE CONTROL REGISTER (XR0E)

Read/Write at I/O Address 3B7h/3D7h
Index 0Eh



This register is effective for all text modes.

1-0 Reserved (0)

2 Cursor Mode

0 Blinking (default on Reset).
1 Non-blinking

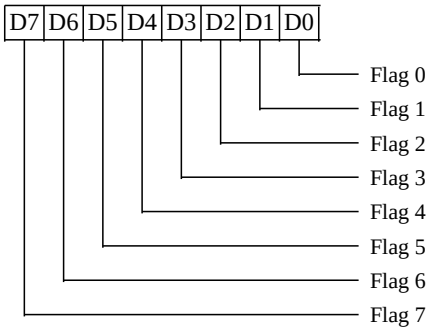
3 Cursor Style

0 Replace (default on Reset)
1 Exclusive-Or

7-4 Reserved (0)

SOFTWARE FLAGS REGISTER #2 (XR0F)

Read/Write at I/O Address 3B7h/3D7h
Index 0Fh



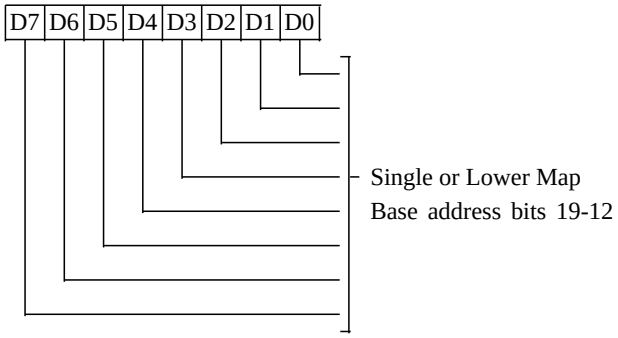
This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software.

7-0 Flags

(See also XR44)

SINGLE/LOW MAP REGISTER (XR10)

Read/Write at I/O Address 3B7h/3D7h
Index 10h



This register effects CPU memory address mapping.

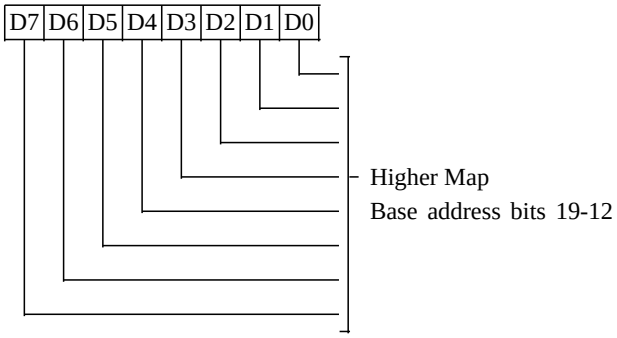
7-0 Single / Low Map Base Address Bits 17-10

These bits define the base address in single map mode (XR0B bit-1 = 0), or the lower map base address in dual map mode (XR0B bit-1 = 1). The memory map starts on a 1K boundary in planar modes and on a 4K boundary in packed pixel modes. In case of dual mapping, this register controls the CPU window into display memory based on the contents of GR06 bits 3-2 as follows:

GR06 Bits 3-2	Low Map		
00	A0000-AFFFF		
01	A0000-A7FFF		
10	B0000-B7FFF	Single	mapping only
11	B8000-BFFFF	Single	mapping only

HIGH MAP REGISTER (XR11)

Read/Write at I/O Address 3B7h/3D7h
Index 11h



This register effects CPU memory address mapping.

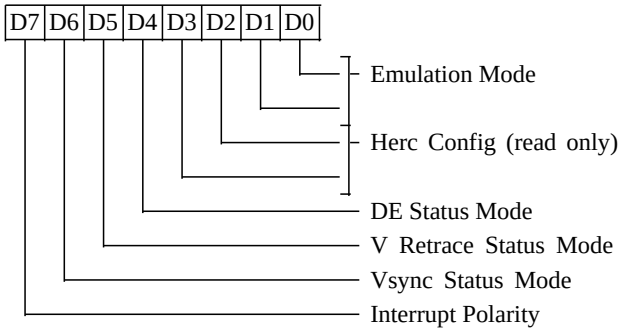
7-0 High Map Base Address Bits 17-10

These bits define the Higher Map base address in dual map modes (XR0B bit-1=1). The memory map starts on a 1K boundary in planar modes and on a 4K boundary in packed pixel modes. This register controls the CPU window into display memory based on the contents of GR06 bits 3-2 as follows:

GR06 bits 3-2	High Map
00	B0000-BFFFF
01	A8000-AFFFF
10	Don't care
11	Don't care

EMULATION MODE REGISTER (XR14)

Read/Write at I/O Address 3B7h/3D7h
Index 14h



1-0 Emulation Mode

00 VGA mode (default on Reset)
01 CGA mode
10 MDA/Hercules mode
11 EGA mode

3-2 Hercules Configuration Register (3BFh) readback (read only)

4 Display Enable Status Mode

0 Select Display Enable status to appear at bit 0 of Input Status register 1 (I/O Address 3BAh/3DAh) (default on reset). Normally used for CGA, EGA, and VGA modes.
1 Select Hsync status to appear at bit 0 of Input Status register 1 (I/O Address 3BAh/3DAh). Normally used for MDA / Hercules mode.

5 Vertical Retrace Status Mode

0 Select Vertical Retracestatus to appear at bit 3 of Input Status register 1 (I/O Address 3BAh/3DAh) (default on Reset). Normally used for CGA, EGA, and VGA modes.
1 Select Video to appear at bit 3 of Input Status register 1 (I/O Address 3BAh/3DAh). Normally used for MDA / Hercules mode.

6 VSync Status Mode

0 Prevent Vsync status from appearing at bit 7 of Input Status Register 1 (I/O Address 3BAh/3DAh). Normally used for CGA, EGA, and VGA modes.
1 Enable Vsync status to appear as bit-7 of Input Status Register 1 (I/O Address 3BAh/3DAh). Normally used for MDA/Hercules mode.

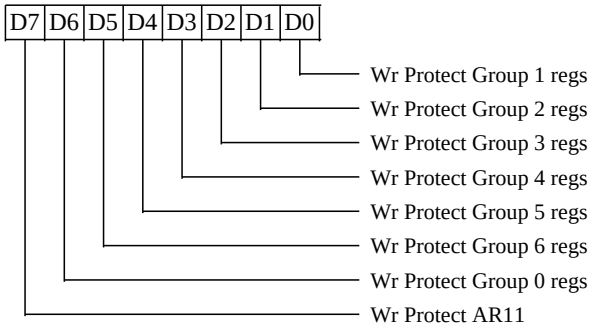
7 Interrupt Output Function

This bit controls the function of the interrupt output pin (IRQ):

	bit-7=0	bit-7=0	bit-7=1
Interrupt State	PC Bus	MC Bus	Either Bus
Disabled	3-state	3-state	3-state
Enabled, Inactive	3-state	3-state	Low
Enabled, Active	3-state	Low	High

WRITE PROTECT REGISTER (XR15)

Read/Write at I/O Address 3B7h/3D7h
Index 15h



This register controls write protection for various groups of registers as shown. 0 = unprotected (default on Reset), 1= protected.

0 Write Protect Group 1 Registers

This bit affects the Sequencer registers (SR00-04), Graphics Controller registers (GR00-08), and Attribute Controller registers (AR00-14).

Note that AR11 is also protected by bit-7 which is ORed with this bit.

1 Write Protect Group 2 Registers

This bit affects CR09 bits 0-4, CR0A, and CR0B.

2 Write Protect Group 3 Registers

This bit affects CR07 bit-4, CR08, CR11 bits 5-4, CR13, CR14, CR17 bits 0-1 and bits 3-7, and CR18.

3 Write Protect Group 4 Registers

This bit affects CR09 bits 5-7, CR10, CR11 bits 0-3 and bits 6-7, CR12, CR15, CR16, and CR17 bit-2.

4 Write Protect Group 5 Registers

This bit affects the Miscellaneous Output register (3C2h) and the Feature Control register (3BAh/3DAh).

5 Write Protect Group 6 Registers

This bit affects the RAMDAC registers (3C6h-3C9h). If this bit is set, PALRD/ and PALWR/ are disabled and all internal DAC registers are also write protected.

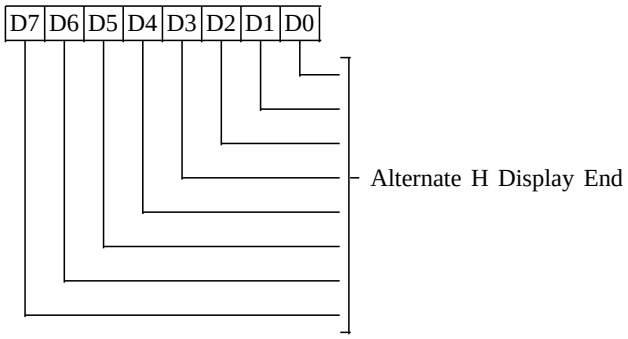
6 Write Protect Group 0 Registers

This bit affects CR0-7 (except CR07 bit-4). This bit is logically ORed with CR11 bit-7.

7 Write Protect AR11

This bit is ORed with bit-0, therefore writing to AR11 is possible only if both bit-0 and bit-7 are 0.

FP HORIZONTAL DISPLAY END REGISTER (XR18)
Read/Write at I/O Address 3B7h/3D7h
Index 18h



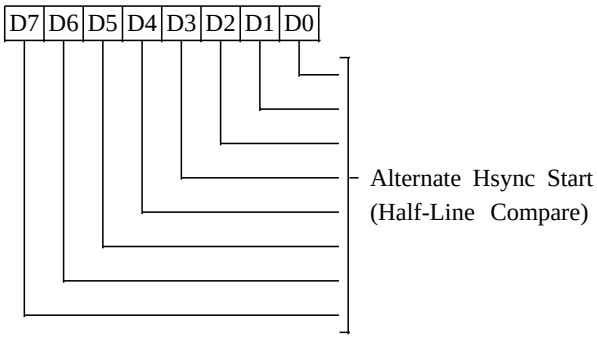
7-0 Horizontal Display End

This register specifies the number of characters displayed per scan line, similar to CR01.

Programmed Value = Actual Value – 1

Note: This register is used in emulation modes only.

FP HORIZONTAL SYNC START REGISTER (XR19)
Read/Write at I/O Address 3B7h/3D7h
Index 19h

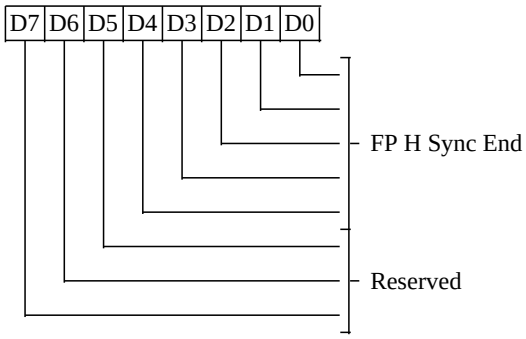


7-0 Horizontal Sync Start

These bits specifiy the begining of the Hsync in terms of character clocks from the begining of the display scan. Similar to CR04.

Programmed Value = Actual Value – 1

FP HORIZONTAL SYNC END REGISTER (XR1A)
Read/Write at I/O Address 3B7h/3D7h
Index 1Ah



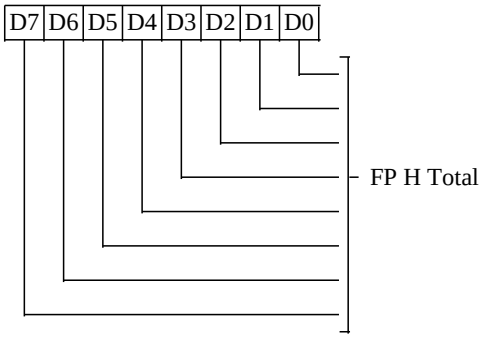
4-0 Horizontal Sync End

Lower 5 bits of the character clock count which specifies the end of horizontal sync. Similar to CR05. If the horizontal sync width desired is N clocks, then programmed value is:

(N + Contents of XR19) ANDed with 01Fh

7-5 Reserved (0)

FP HORIZONTAL TOTAL REGISTER (XR1B)
Read/Write at I/O Address 3B7h/3D7h
Index 1Bh

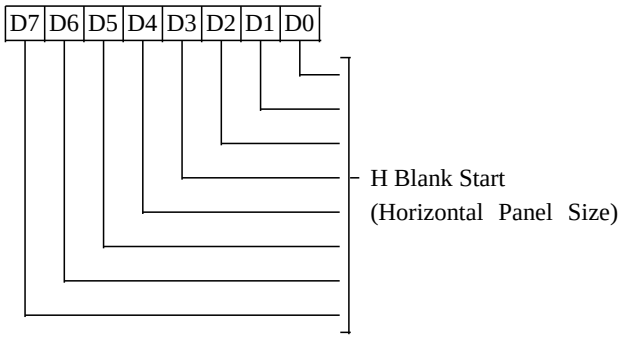


7-0 Horizontal Total

This register contents are the total number of character clocks per line. Similar to CR00.

Programmed Value = Actual Value – 5

FP HORIZONTAL BLANK START / HORIZONTAL PANEL SIZE REGISTER (XR1C)
Read/Write at I/O Address 3B7h/3D7h
Index 1Ch



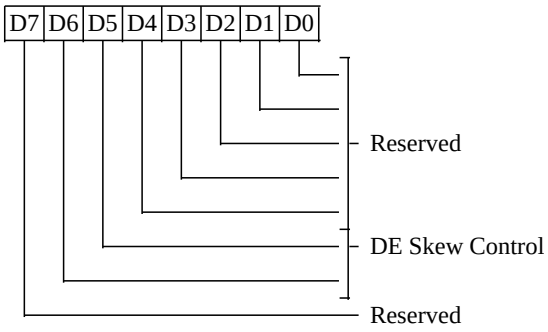
The value in this register is the Horizontal Panel Size in all Modes.

7-0 FP Horizontal Panel Size

Horizontal panel size is programmed in terms of number of 8-bit (graphics/text) or 9-bit (text) characters. For double drive flat panels the actual horizontal panel size must be a multiple of two character clocks.

Programmed Value = Actual Value – 1

FP HORIZONTAL BLANK END REGISTER (XR1D)
Read/Write at I/O Address 3B7h/3D7h
Index 1Dh



4-0 Reserved

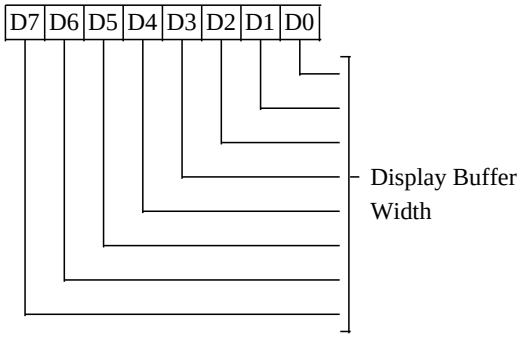
6-5 FP Display Enable Skew Control

Used in FP Hercules and CGA emulation modes. See CR03 for description.

7 Reserved

OFFSET REGISTER (XR1E)

Read/Write at I/O Address 3B7h/3D7h
Index 1Eh



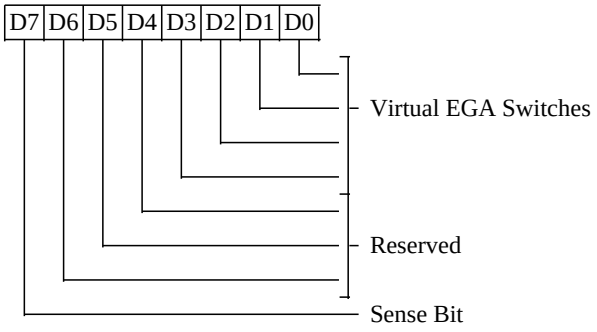
7-0 Offset Value

See CR13 for description

Programmed Value = Actual Value – 1

VIRTUAL EGA SWITCH REGISTER (XR1F)

Read/Write at I/O Address 3B7h/3D7h
Index 1Fh



3-0 Virtual Switch Register

If bit-7 is '1', then one of these four bits is read back in Input Status Register 0 (3C2h) bit 4. The selected bit is determined by Miscellaneous Output Register (3C2h) bits 3-2 as follows:

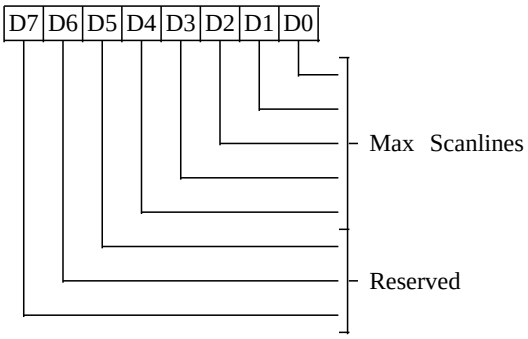
Misc 3-2	XR1F Bit Selected
00	bit-3
01	bit-2
10	bit-1
11	bit-0

6-4 Reserved (0)

7 Sense Bit

This bit always reads back as 0.

MAXIMUM
SCANLINE REGISTER (XR24)
Read/Write at I/O Address 3B7h/3D7h
Index 24h



This register is used in text modes when TallFont is enabled during vertical compensation.

4-0 Alternate Maximum Scanlines (AMS)

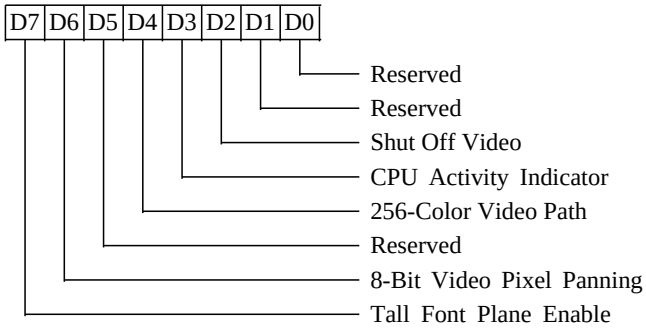
Programmed Value = number of scanlines minus one per character row of TallFont

Double scanned lines, inserted lines, and replicated lines are not counted.

7-5 Reserved (0)

VIDEO INTERFACE REGISTER (XR28)

Read/Write at I/O Address 3B7h/3D7h
Index 28h



0 Reserved

1 Reserved

2 Shut Off Video

This bit is effective in all flat panel modes during horizontal / vertical blank time. This bit should be set properly when using FP displays which look at video signals during blank time. It has no effect on displays that ignore video signals during blank time. This bit is also ignored when the screen is blanked (see XR2B for conditions when the screen is blanked).

0 When the screen is not blanked, video is forced to the border / overscan color (AR11) during blank time (default on Reset)
1 When the screen is not blanked, video is forced to default video (XR2B) during blank time.

Note: In flat panel mode, video is forced to the border / overscan color (AR11) or to default video (XR2B) before the internal palette and before the FRC logic.

3 CPU Activity Indicator

This bit controls the enabling of CPU activity indicator or ERMEN/ functionality on pin 49 (F65510) or pin 47 (T65510).

0 CPU Activity indicator is enabled on pin 49 (F65510) or pin 47 (T65510) (default).
1 ERMEN/ functionality is enabled on pin 49 (F65510) or pin 47 (T65510).

4 256-Color Video Path

This bit is effective for all flat panel packed pixel (256-color) Modes.

0 4-bit video data path (default on reset)
1 8-bit video data path (horizontal pixel panning is controlled by bit-6)

Note: GR05 bit-5 must be 0 if this bit is set

5 Reserved *(Must be Programmed to 0)*

6 8-Bit Video Pixel Panning

This bit is effective for flat panel operation when the 8-bit video data path is selected (XR28 bit-4 = 1).

0 AR13 bits 2-1 are used to control pixel panning (default on Reset)
1 AR13 bits 2-0 are used to control pixel panning

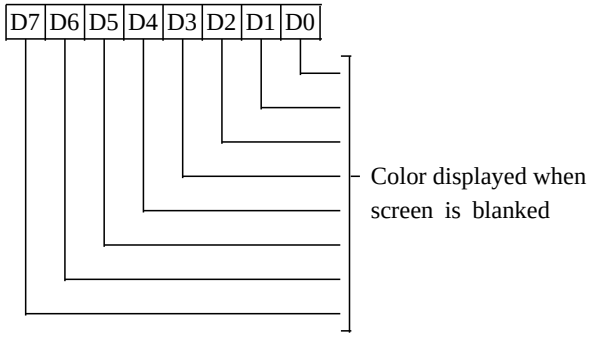
7 Tall Font Plane Enable

This bit is used to select the plane used to store tall fonts in text modes.

0 Tall Fonts are stored in plane 3 (default)
1 Tall Fonts are stored in plane 2

DEFAULT VIDEO REGISTER (XR2B)

Read/Write at I/O Address 3B7h/3D7h
Index 2Bh



This register affects all modes when the screen is not blanked and XR28 bit-2 = 1. This register effects flat panel operation when the screen is blanked independent of XR28 bit-2. Screen blank occurs when SR01 bit-5 is set in any emulation mode, or when bit-3 of the CGA / Hercules Mode Control Register (3B8h/3D8h) is reset in CGA / Hercules mode.

Note: For flat panel, video data output during screen blank is different than video data output during Panel Off power-saving mode. In Panel Off power-saving mode, video data is forced low or high or 3-stated (see XR52, XR61 bit-7, and XR63 bit-7). In Standby power saving mode, video data is 3-stated.

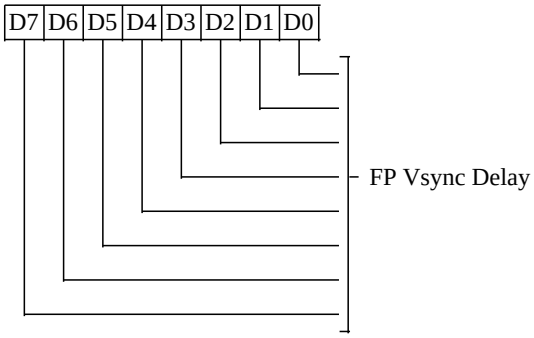
7-0 Default Video

When the screen is not blanked, these bits specify the color to be displayed during FP blank time when XR28 bit-2 = 1. When the screen is blanked, these bits specify the color to be displayed for both flat panel.

Note: In flat panel mode, video data is forced to default video before the internal RAMDAC palette and before the FRC logic.

FP VSYNC (FLM) DELAY REGISTER (XR2C)

Read/Write at I/O Address 3B7h/3D7h
Index 2Ch



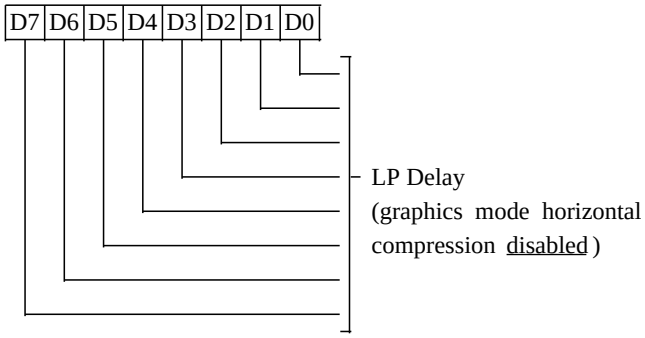
This register is used only when XR2F bit-7=0. The First Line Marker (FLM) signal is generated from an internal FP Vsync active edge with a delay specified by this register. The FLM pulse width is always one line for SS panels and two lines for DS/DD panels.

7-0 FP VSync Delay (VDelay)

These bits define the number of Hsyncs between the internal Vsync and the rising edge of FLM.

FP HSYNC (LP) DELAY REGISTER (XR2D)

Read/Write at I/O Address 3B7h/3D7h
Index 2Dh



This register is used only in flat panel mode when XR2F bit-6 = 0 and graphics mode horizontal compression is disabled. The LP output is generated from the FP Blank inactive edge with a delay specified by XR2F bit-5 and the value in this register. The LP pulse width is specified in register XR2F.

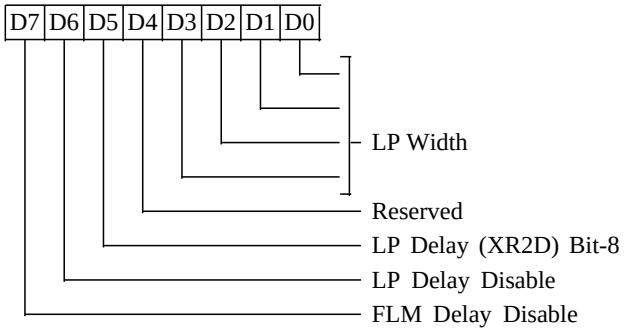
7-0 FP HSync (LP) Delay (HDelay)

These bits define the number of character clocks between the FP Blank inactive edge and the rising edge of the LP output in flat panel mode with graphics mode horizontal compression disabled. The msb (bit 8) of this parameter is XR2F bit-5.

Programmed Value = Actual Value – 1

FP HSYNC (LP) WIDTH REGISTER (XR2F)

Read/Write at I/O Address 3B7h/3D7h
Index 2Fh



This register together with XR2D defines the LP output pulse.

3-0 FP HSync (LP) Width (HWidth)

These bits define the width of LP output pulse in terms of number of character (8-dot only) clocks.

Programmed Value = Actual Value – 1

4 Reserved

5 FP HSync (LP) Delay (XR2D) Bit 8

This bit is the msb of the FP HSync (LP) Delay parameter for graphics mode with horizontal compression disabled.

6 FP HSync (LP) Delay Disable

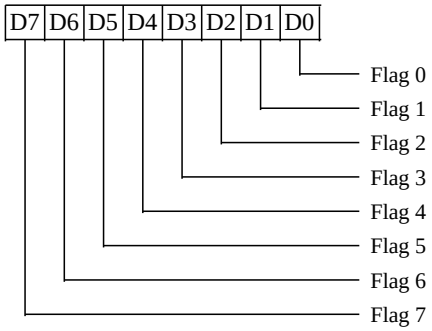
0 FP HSync (LP) Delay Enable: XR2D and XR2F bit-5 are used to delay the FP HSync (LP) active edge with respect to the FP Blank inactive edge.
1 FP HSync (LP) Delay Disable: FP HSync (LP) active edge will coincide with the FP Blank inactive edge.

7 FP VSync (FLM) Delay Disable

0 FP VSync (FLM) Delay Enable: XR2C is used to delay the external FP VSync (FLM) active edge with respect to the internal FP VSync active edge.
1 FP VSync (FLM) Delay Disable: the external FP VSync (FLM) active edge will coincide with the internal FP VSync (FLM) active edge.

SOFTWARE FLAGS REGISTER (XR44)

Read/Write at I/O Address 3B7h/3D7h
Index 44h

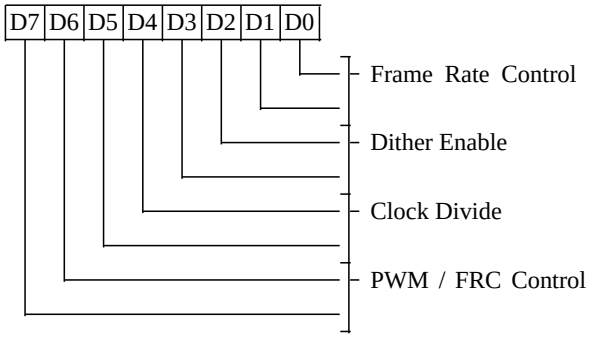


This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software.

7-0 Flags

(See also XR0F)

PANEL FORMAT REGISTER (XR50)
Read/Write at I/O Address 3B7h/3D7h
Index 50h



1-0 Frame Rate Control (FRC)

If bit-6 of this register is 0, these bits specify grayscale simulation on a frame by frame basis on monochrome flat panels that do not support gray levels internally.

00 8-frame FRC: 9-level grayscale simulation without dithering or 32-level grayscale simulation with dithering.
01 16-frame FRC: 16-level grayscale simulation with or without dithering.
10 4-frame FRC: 5-level grayscale simulation without dithering or 16-level grayscale simulation with dithering.
11 See description for bits 7-6.

3-2 Dither Enable

00 Disable dithering
01 Enable dithering only for 256-color mode (AR10 bit-6 = 1)
10 Enable dithering for all modes
11 Reserved

5-4 Clock Divide (CD)

These bits specify the frequency ratio between the dot clock and the flat panel shift clock (SHFCLK) signal.

00 Shift Clock Freq = Dot Clock Freq

This setting is used to output 1 pixel per shift clock with a maximum of 6 bpp (bits/pixel) for single drive monochrome panels. This setting cannot be used for double drive (DD) panels. FRC and Dithering can be enabled.

01 Shift Clk Freq = 1/2 Dot Clock Freq

This setting is used to output 2 pixels per shift clock with a maximum of 4 bpp (bits/pixel) for single drive monochrome panels. FRC and dithering can be enabled.

10 Shift Clk Freq = 1/4 Dot Clock Freq

This setting is used to output 4 pixels per shift clock with a maximum of 2 bpp for single drive mono panels. FRC and dithering can be enabled.

11 Shift Clk Freq = 1/8 Dot Clock Freq

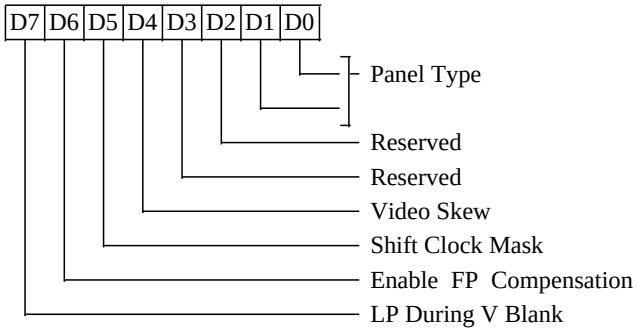
This setting is used to output 8 pixels per shift clock with a maximum of 1 bpp for single drive mono panels and is used to output 8 pixels per shift clock with 1 bpp for mono double drive (DD) panels. FRC and dithering can be enabled.

7-6 PWM / FRC Control

00 CD=00: 6 bpp PWM (dither bits 1,0)
CD=01: 4 bpp PWM (dither bits 1,0)
CD=10: 2 bpp PWM (dither bits 3,2)
CD=11: 1 bpp PWM (dither bits 5,4)
01 3 Bits/Pixel PWM (dither bits 2,1) use only CD=00 & 01 for mono panels
10 Reserved
11 Reserved

To use settings 01, 10, or 11 above, bits 1-0 of this register must be set to 11. In other words, if bits 1-0 are not 11 then bits 7-6 must be programmed to 00.

DISPLAY TYPE REGISTER (XR51)
Read/Write at I/O Address 3B7h/3D7h
Index 51h



1-0 Panel Type (PT)

00 Single Panel Single Drive (SS)
01 Reserved
10 Dual Panel Single Drive (DS)
11 Dual Panel Double Drive (DD)

2 Reserved *(Must be programmed to 1)*

3 Reserved *(Must be programmed to 0)*

4 Video Skew

This bit affects flat panel video.

0 No video data delay
1 Video data delayed by 1 shift clock

5 Shift Clock Mask (SM)

This bit controls shift clock operation.

0 Allow shift clock output to toggle outside the display enable interval
1 Force the shift clock output low outside the display enable interval

6 Enable FP Compensation (EFCP)

This bit enables flat panel horizontal and vertical compensation depending on panel size, current display mode, and contents of the compensation registers.

0 Disable FP compensation
1 Enable FP compensation

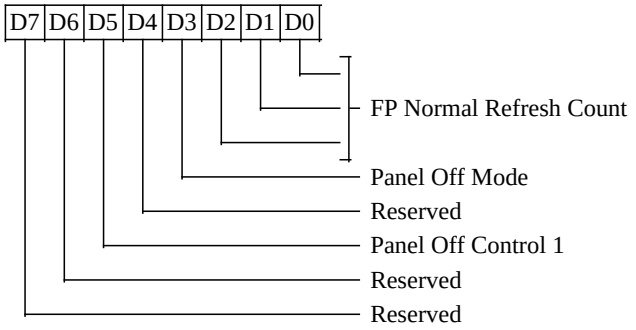
7 LP During Vertical Blank

This bit should be set only for SS panels which require FP Hsync (LP) to be active during vertical blank time when XR54 bit-1 = 0 (e.g., Plasma / EL panels). This bit should be reset when using non-SS panels or when XR54 bit-1 = 1.

0 FP Hsync (LP) is generated from internal FP Blank inactive edge
1 FP Hsync (LP) is generated from internal FP Horizontal Blank inactive edge

POWER DOWN CONTROL REGISTER (XR52)

Read/Write at I/O Address 3B7h/3D7h



2-0 FP Normal Refresh Count

These bits are effective for flat panel only. They specify the number of memory refresh cycles to be performed per scanline. A minimum value of 1 should be programmed in this register.

3 Panel Off Mode

This bit provides a software alternative to enter Panel Off mode.

0 Normal mode (default on reset)
1 Panel Off mode

In Panel Off mode, the FP display memory interface is inactive but CPU interface and display memory refresh are still active.

4 Reserved

5 Panel Off Control Bit

This bit is effective only in Panel Off mode (XR52 bit-3 = 1).

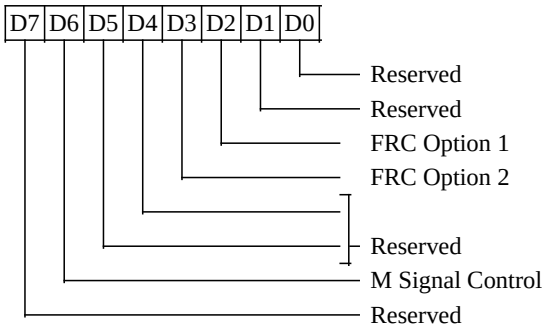
0 Video data (P0-P7) and flat panel timing and control signals (FLM, LP, DE, and SHFCLK) are driven.
1 Video data (P0-P7) and flat panel timing and control signals (FLM, LP, DE and SHFCLK) are Tri-Stated.

6 Reserved *(Must be programmed to 1)*

7 Reserved

FP FRC OPTION REGISTER (XR53)

Read/Write at I/O Address 3B7h/3D7h
Index 53h



0 Reserved

1 Reserved

2 FRC Option 1

3 FRC Option 2

5-4 Reserved

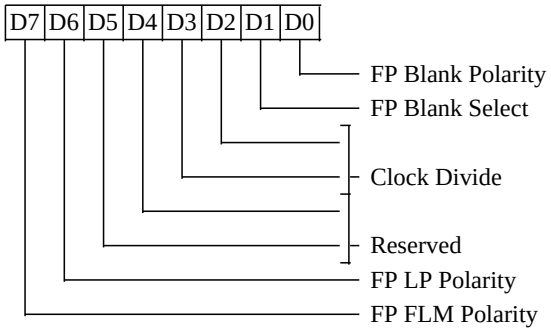
6 M Signal Control

This signal controls the output on pin 63 (T65510) or pin 65 (F65510), whether it is the M signal to the panel or BLANK/ signal to the panel

0 Pin 63 (T65510) or pin 65 (F65510) outputs M Signal (ACDCLK)
1 Pin 63 (T65510) or pin 65 (F65510) outputs BLANK/ signal

7 Reserved

FP INTERFACE REGISTER (XR54)
Read/Write at I/O Address 3B7h/3D7h
Index 54h



0 FP Blank Polarity

This bit controls the polarity of the BLANK/ pin in flat panel mode.

0 Positive polarity
1 Negative polarity

1 FP Blank Select

This bit controls the BLANK/ pin output in flat panel mode. This bit also affects operation of the flat panel video logic, generation of the FP HSync (LP) pulse signals, and masking of the Shift Clock.

0 The BLANK/ pin outputs both FP Vertical and Horizontal Blank. In 480-line DD panels, this option will generate exactly 240 FP HSync (LP) pulses.
1 The BLANK/ pin outputs only FP Horizontal Blank. During FP Vertical Blank, the flat panel video logic will be active, the FP HSync (LP) pulse will be generated, and Shift Clock can not be masked. Note however that Shift Clock can still be masked during FP Horizontal Blank.

Note: The signal polarity selected by bit-0 is applicable for either selection.

4-2 Clock Divider Select Bits

These bits control the internal Dot Clock generation from the CLKIN input. Bits 4-2 control the divide for CLKIN to generate the Dot Clock. The various divide schemes are shown below:

4 3 2	DCLK
0 0 0	CLKIN
0 0 1	15/16 (CLKIN)
0 1 0	14/16 (CLKIN)
0 1 1	13/16 (CLKIN)
1 0 0	12/16 (CLKIN)
1 0 1	11/16 (CLKIN)
1 1 0	10/16 (CLKIN)
1 1 1	9/16 (CLKIN)

5 Reserved

6 FP HSync (LP) Polarity

This bit controls the polarity of the flat panel HSync (LP) pin.

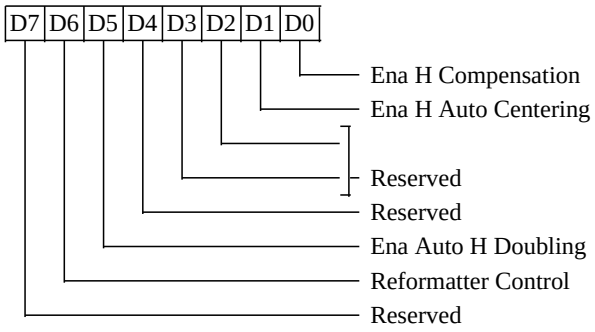
0 Positive polarity
1 Negative polarity

7 FP VSync (FLM) Polarity

This bit controls the polarity of the flat panel VSync (FLM) pin.

0 Positive polarity
1 Negative polarity

FP HORIZONTAL COMPENSATION REGISTER (XR55)
Read/Write at I/O Address 3B7h/3D7h
Index 55h



This register is used only when flat panel compensation is enabled (XR51 bit-6 = 1).

0 Enable Horizontal Compensation (EHCP)

0 Disable horizontal compensation
1 Enable horizontal compensation

1 Enable Automatic Horizontal Centering (EAHC) (effective only if bit-0 is 1)

0 Enable non-automatic horizontal centering. The Horizontal Centering Register is used to specify the left border. If no centering is desired then the Horizontal Centering Register can be programmed to 0.
1 Enable automatic horizontal centering. Horizontal left and right borders will be computed automatically.

2 Reserved *(Must be programmed to 1)*

When operating in 9-dot text modes, horizontal compensation must always be enabled (XR51 bit-6=1, XR55 bit-0=1).

3 Reserved

4 Reserved

5 Enable Automatic Horizontal Doubling (EAHD) (this bit is effective if bit-0 is 1)

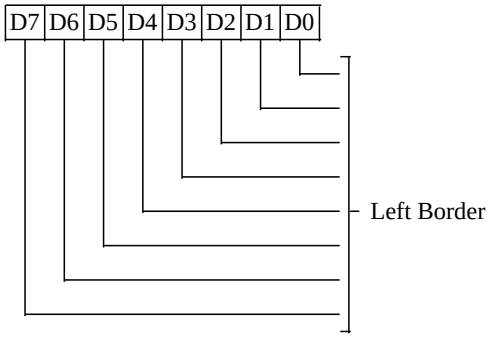
0 Disable Automatic Horizontal Doubling. Horizontal doubling will only be performed for flat panels when SR01 bit-3 = 1 in any emulation mode or when 3B8/3D8 bit-0 & 3B8/3D8 bit-4 = 0 in CGA emulation.
1 Enable Automatic Horizontal Doubling. Horizontal doubling will be performed for flat panels when SR01 bit-3 = 1 in any emulation mode or when 3B8/3D8 bit-0 & 3B8/3D8 bit-4 = 0 in CGA emulation or when the Horizontal Display width (CR01) is equal to or less than half of the Horizontal Panel Size (XR18).

6 Text Reformatter Control

This bit is typically set to 0. It is used for test purposes only.

7 Reserved

HORIZONTAL CENTERING REGISTER (XR56)
Read/Write at I/O Address 3B7h/3D7h

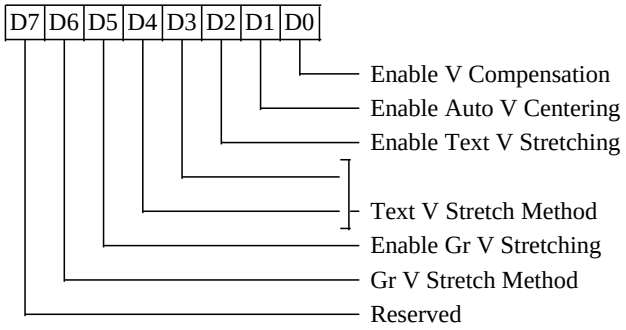


This register is used only when non-automatic horizontal centering is enabled.

7-0 Horizontal Left Border (HLB)

Programmed Value (in character clocks) = Width of Left Border – 1

VERTICAL COMPENSATION REGISTER (XR57)
Read/Write at I/O Address 3B7h/3D7h
Index 57h



This register is used only when flat panel compensation is enabled.

0 Enable Vertical Compensation (EVCP)

0 Disable vertical compensation
1 Enable vertical compensation

1 Enable Automatic Vertical Centering (EAVC)

This bit is effective only if bit-0 is 1.

0 Enable non-automatic vertical centering. The Vertical Centering Register is used to specify the top border. If no centering is desired then the Vertical Centering Register can be programmed to 0.
1 Enable automatic vertical centering. Vertical top and bottom borders will be computed automatically.

2 Enable Text Mode Vertical Stretching (ETVS)

This bit is effective only if bit-0 is 1.

0 Disable text mode vertical stretching; graphics mode vertical stretching is used if enabled.
1 Enable text mode vertical stretching

4-3 Text Mode Vertical Stretching (TVS1-0)

These bits are effective if bits 2 and 0 are 1.

00 Double Scanning (DS) and Line Insertion (LI) with the following priority: DS+LI, DS, LI.
01 Double Scanning (DS) and Line Insertion (LI) with the following priority: DS+LI, LI, DS.
10 Double Scanning (DS) and TallFont (TF) with the following priority: DS+TF, DS, TF.
11 Double Scanning (DS) and TallFont (TF) with the following priority: DS+TF, TF, DS.

5 Enable Vertical Stretching (EVS)

This bit is effective only if bit-0 is 1.

0 Disable vertical stretching
1 Enable vertical stretching

6 Vertical Stretching (VS)

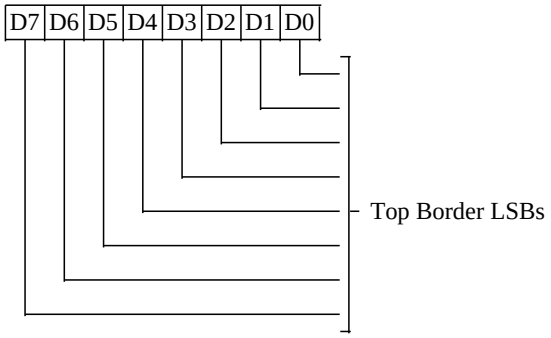
Vertical Stretching can be enabled in both text and graphics modes. This bit is effective only if bits 5 and 0 are 1.

0 Double Scanning (DS) and Line Replication (LR) with the following priority: DS+LR, DS, LR.
1 Double Scanning (DS) and Line Replication (LR) with the following priority: DS+LR, LR, DS.

7 Reserved (0)

VERTICAL CENTERING REGISTER (XR58)

Read/Write at I/O Address 3B7h/3D7h
Index 58h



This register is used only when non-automatic vertical centering is enabled.

7-0 Vertical Top Border LSBs (VTB7-0)

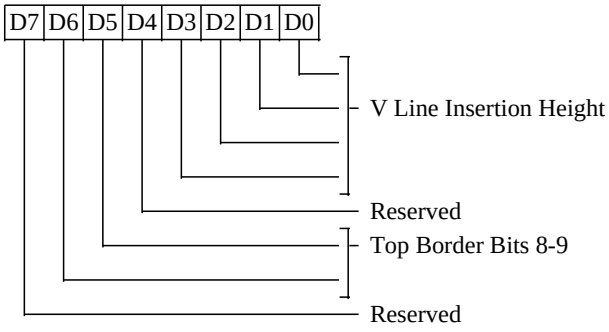
Programmed value:

Top Border Height (in scan lines) – 1

This register contains the eight least significant bits of the programmed value of the Vertical Top Border (VTB). The two most significant bits are in the Vertical Line Insertion Register (XR59).

VERTICAL LINE INSERTION REGISTER (XR59)

Read/Write at I/O Address 3B7h/3D7h



This register is used only in text mode when vertical line insertion is enabled.

3-0 Vertical Line Insertion Height (VLIH3-0)

Programmed Value:

Number of Insertion Lines – 1

The value promgrammed in this register - 1 is the number of lines to be inserted between the rows. Insertion lines are never double scanned even if double scanning is enabled. Insertion lines use the background color.

4 Reserved (0)

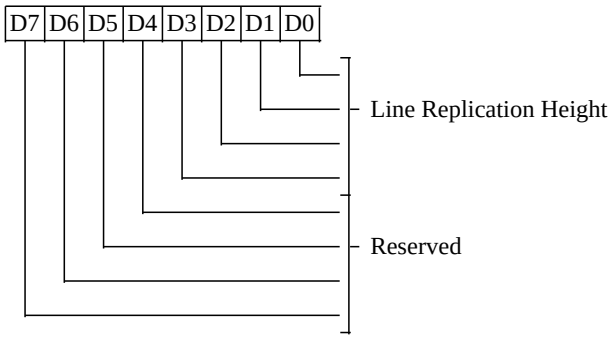
6-5 Vertical Top Border MSBs (VTB9-8)

This register contains the two most significant bits of the programmed value of the Vertical Top Border (VTB). The eight least significant bits are in the Vertical Centering Register (XR58).

7 Reserved (0)

VERTICAL LINE REPLICATION REGISTER (XR5A)

Read/Write at I/O Address 3B7h/3D7h
Index 5Ah



This register is used in text or graphics modes when vertical line replication is enabled.

3-0 Vertical Line Replication Height (VLRH)

Programmed Value = Number of Lines Between Replicated Lines – 1

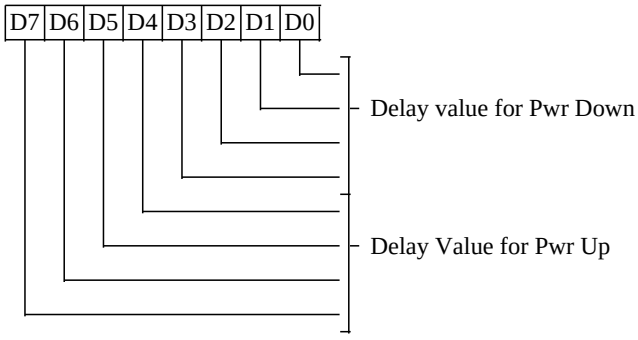
Double scanned lines are also counted.

In other words, if this field is programmed with '7', every 8th line will be replicated.

7-4 Reserved (0)

PANEL POWER SEQUENCING DELAY REGISTER (XR5B)

Read/Write at I/O Address 3B7h/3D7h
Index 5Bh



This register is used to generate programmable sequencing of the ENAVDD, Panel Data/Control and ENAVEE signals. This register defaults to a value of 81h on RESET.

3-0 Power-Down Delay

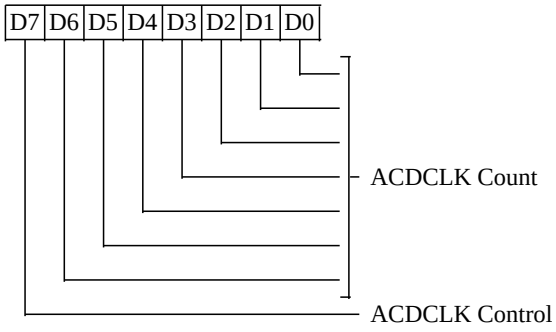
The value programmed determines the delay between each of the following events: ENAVEE going low, panel data/control signals becoming 3-state, and ENAVDD going low **during Power Down**. The delay is generated by dividing the CLKIN frequency by a divisor generated by programming this nibble. Each increment corresponds to a value of 2^{20} or 1,048,576. The maximum and minimum divisors are 2^{24} or 16,777,216 and 2^{20} or 1,048,576 respectively. For CLKIN of 33 MHz, minimum and maximum delays are 31.8 mS and 508.4 mS respectively.

7-4 Power-Up Delay

The value programmed determines the delay between each of the following events: ENAVDD going high, panel data/control signals becoming active, and ENAVEE signal going high **during Power Up**. The delay is generated by dividing the CLKIN frequency by a divisor generated by programming this nibble. Each increment corresponds to a value of 2^{17} or 131,072. The maximum and minimum divisors are 2^{21} or 2,097,152 and 2^{17} or 131,072 respectively. For CLKIN of 33 MHz, minimum & maximum delays are 3.971 mS and 63.5 mS respectively.

ACDCLK CONTROL REGISTER (XR5E)

Read/Write at I/O Address 3B7h/3D7h
Index 5Eh



This register is used to control the duty cycle of the ACDCLK (M) signal to the panel.

6-0 ACDCLK Count (ACDCNT)

These bits define the number of Hsyncs between adjacent phase changes on the ACDCLK output. These bits are effective only when bit 7 = 0 and contents of this register are grater than 2.

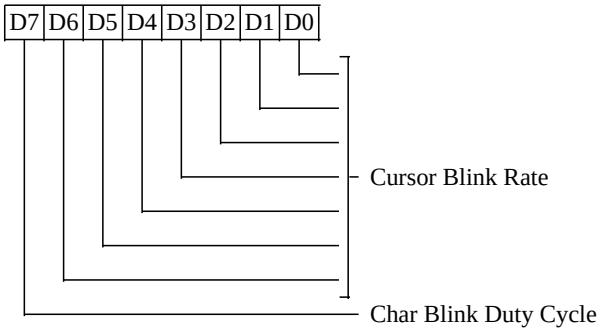
Programmed Value = Actual Value – 2

7 ACDCLK Control

0 The ACDCLK phase changes depending on bits 0-6 of this register
1 The ACDCLK phase changes every frame.

BLINK RATE CONTROL REGISTER (XR60)

Read/Write at I/O Address 3B7h/3D7h
Index 60h



This register is used in all modes.

5-0 Cursor Blink Rate

These bits specify the cursor blink period in terms of number of Vsyncs (50% duty cycle). In text mode, the character blink period and duty cycle is controlled by bits 7-6 of this register. These bits default to 000011 (decimal 3) on reset which corresponds to eight Vsyncs per cursor blink period per the following formula (four Vsyncs on and four Vsyncs off):

Programmed Value = (Actual Value) / 2 – 1

Note: In graphics mode, the pixel blink period is fixed at 32 Vsyncs per cursor blink period with 50% duty cycle (16 on and 16 off).

7-6 Character Blink Duty Cycle

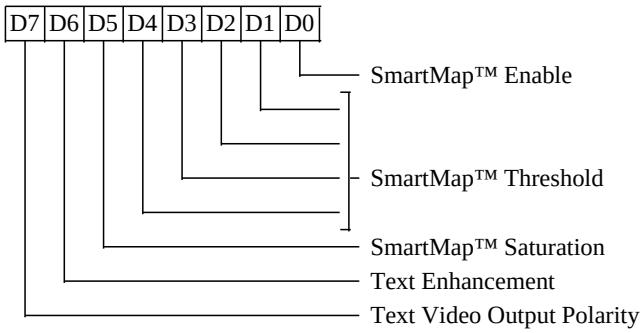
These bits specify the character blink (also called 'attribute blink') duty cycle in text mode.

7	6	Character Blink Duty Cycle	
0	0	50%	
0	1	25%	
1	0	50%	(default on Reset)
1	1	75%	

For setting 00, the character blink period is equal to the cursor blink period. For all other settings, the character blink period is twice the cursor blink period (character blink is twice as slow as cursor blink).

SMARTMAP™ CONTROL REGISTER (XR61)

Read/Write at I/O Address 3B7h/3D7h
Index 61h



This register is used in text modes only.

0 SmartMap Enable

0 Disable SmartMap, use color lookup table and use internal palette if enabled (XR06 bit-2 = 1).

1 Enable SmartMap, bypass both color lookup table and internal RAMDAC palette in flat panel text mode. Although color lookup table is bypassed, translation of 4 bits/pixel data to 6 bits/pixel data is still performed depending on AR10 bit-1 (monochrome / color display) as follows:

Output	AR10 bit-1 = 0	AR10 bit-1 = 1
Out0	In0	In0
Out1	In1	In1
Out2	In2	In2
Out3	In3	In0+In1+In2+In3
Out4	In3	In3
Out5	In3	In3

4-1 SmartMap Threshold

These bits are used only in flat panel text mode when SmartMap is enabled (bit-0 = 1). They define the minimum difference between the foreground and background colors. If the difference is less than this threshold, the colors are separated by adding and subtracting the shift values (XR62) to the foreground and background colors. However, if the foreground and background color values are the same, then the color values are not adjusted.

5 SmartMap Saturation

This bit is used only in flat panel text mode when SmartMap is enabled (bit-0 = 1). It selects the clamping level after the color addition/subtraction.

0 The color result is clamped to the maximum and minimum values (0Fh and 00h respectively)
1 The color result is computed modulo 16 (no clamping)

6 Text Enhancement

This bit is used only in flat panel text mode.

0 Normal text
1 Text attribute 07h and 0Fh are reversed to maximize the brightness of the normal DOS prompt

7 Text Video Output Polarity (TVP)

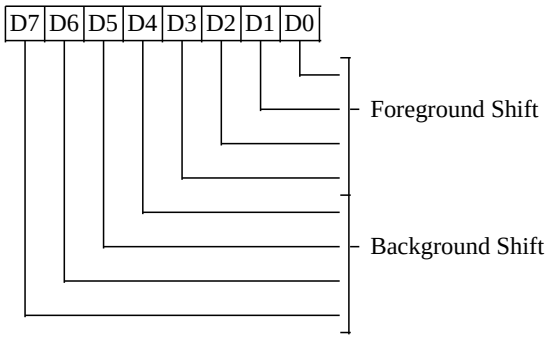
This bit is effective for flat panel text mode only.

0 Normal polarity
1 Inverted polarity

Note: Graphics video output polarity is controlled by XR63 bit-7 (GVP).

SMARTMAP™ SHIFT PARAMETER REGISTER (XR62)

Read/Write at I/O Address 3B7h/3D7h
Index 62h



This register is used in text mode when SmartMap is enabled (XR61 bit-0 = 1).

3-0 Foreground Shift

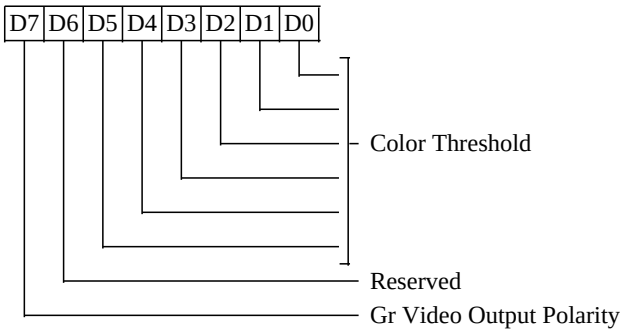
These bits define the number of levels that the foreground color is shifted when the foreground and background colors are closer than the SmartMap Threshold (XR61 bits 1-4). If the foreground color is "greater" than the background color, then this field is added to the foreground color. If the foreground color is "smaller" than the background color, then this field is subtracted from the foreground color.

7-4 Background Shift

These bits define the number of levels that the background color is shifted when the foreground and background colors are closer than the SmartMap Threshold (XR61 bits 1-4). If the background color is "greater" than the foreground color, then this field is added to the background color. If the background color is "smaller" than the foreground color, then this field is subtracted from the background color.

SMARTMAP™ COLOR MAPPING CONTROL REGISTER (XR63)

Read/Write at I/O Address 3B7h/3D7h
Index 63h



5-0 Color Threshold

These bits are effective for monochrome (XR51 bit-5 = 1) single/double drive flat panel with 1 bit/pixel (XR50 bits 4-5 = 11) without FRC (XR50 bits 0-1 = 11). They specify the color threshold used to reduce 6-bit video to 1-bit video color. Color values equal to or greater than the threshold are mapped to 1 and color values less than the threshold are mapped to 0.

6 Reserved

7 Graphics Video Output Polarity (GVP)

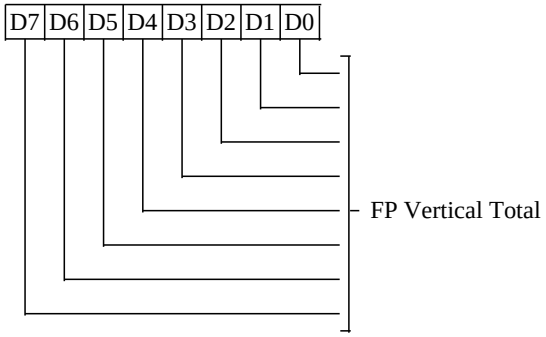
This bit is effective for flat panel graphics mode only.

0 Normal polarity
1 Inverted polarity

Note: Text video output polarity is controlled by XR61 bit-7 (TVP).

FP VERTICAL TOTAL REGISTER (XR64)

Read/Write at I/O Address 3B7h/3D7h
Index 64h



This register is used in all modes.

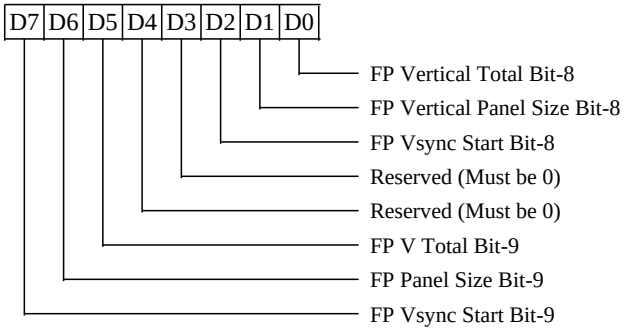
7-0 FP Alternate Vertical Total

The contents of this register are 8 low order bits of a 10-bit value. Bits 9 and 10 are defined in XR65. The vertical total value specifies the total number of scan lines per frame. Similar to CR06.

Programmed Value = Actual Value – 2

FP OVERFLOW REGISTER (XR65)

Read/Write at I/O Address 3B7h/3D7h
Index 65h



This register is used in all modes.

0 FP Alternate Vertical Total Bit-8

1 FP Vertical Panel Size Bit-8

2 FP Alternate Vertical Sync Start Bit-8

3 Reserved ***(Must be programmed to 0)***

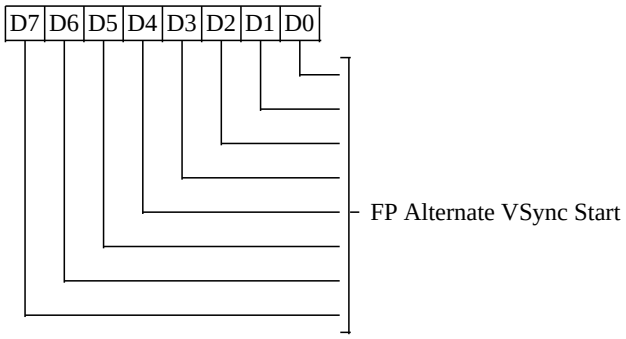
4 Reserved ***(Must be programmed to 0)***

5 FP Alternate Vertical Total Bit-9

6 FP Vertical Panel Size Bit-9

7 FP Alternate Vertical Sync Start Bit-9

FP VERTICAL SYNC START REGISTER (XR66)
Read/Write at I/O Address 3B7h/3D7h
Index 66h



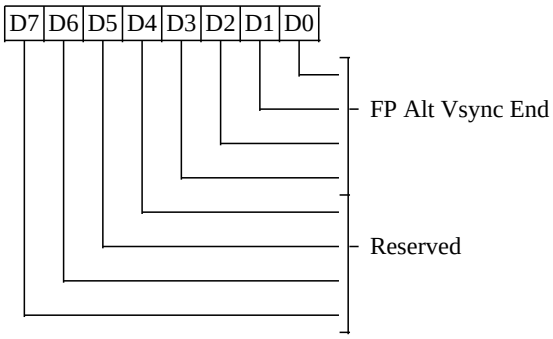
This register is used in all modes.

7-0 FP Alternate Vertical Sync Start

The contents of this register are the 8 low order bits of a 10-bit value. Bits 9 and 10 are defined in XR65. This value defines the scan line position at which vertical sync becomes active. Similar to CR10.

Programmed Value = Actual Value – 1

FP VERTICAL SYNC END REGISTER (XR67)
Read/Write at I/O Address 3B7h/3D7h
Index 67h



This register is used in all modes.

3-0 FP Alternate Vertical Sync End

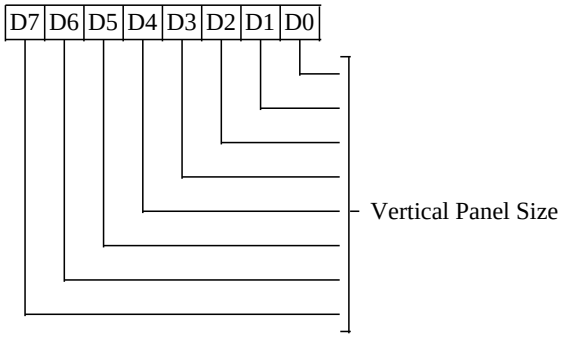
The lower 4 bits of the scan line count that defines the end of vertical sync. Similar to CR11. If the vertical sync width desired is N lines, the programmed value is:

(contents of XR66 + N) ANDed with 0FH

7-4 Reserved (0)

VERTICAL PANEL SIZE REGISTER (XR68)

Read/Write at I/O Address 3B7h/3D7h
Index 68h



This register is used in all modes.

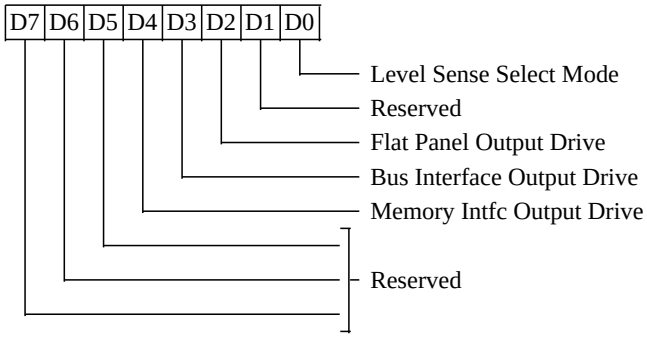
7-0 Vertical Panel Size

The contents of this register define the number of scan lines per frame.

Programmed Value = Actual Value – 1

PROGRAMMABLE OUTPUT DRIVE REGISTER (XR6C)

Read/Write at I/O Address 3B7h/3D7h
Index 6Ch



This register is used to control the output drive of the bus, video, and memory interface pins.

Please refer to the T65510 and F65510 pin list tables for normal drive values for all outputs.

0 Input Voltage Level Selection

0 V_{CC} for internal logic is 3.3V
1 V_{CC} for internal logic is 5V

1 Reserved

2 Flat Panel Interface Output Drive Select

0 Normal drive (Default)
1 2x Normal drive

3 Bus Interface Output Drive Select

0 Normal drive (Default)
1 2x Normal drive

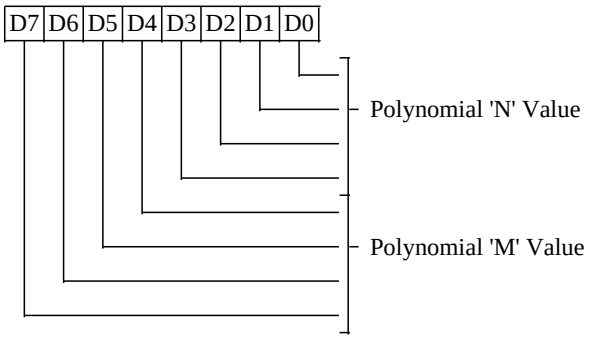
4 Memory Interface Output Drive Select

0 Normal drive (Default)
1 2x Normal drive

7-5 Reserved

POLYNOMIAL FRC CONTROL REGISTER (XR6E)

Read/Write at I/O Address 3B7h/3D7h
Index 6Eh



This register is effective in flat panel mode when polynomial FRC is enabled (see XR50 bits 0-1). It is used to control the FRC polynomial counters. The values in the counters determine the offset in rows and columns of the FRC count. These values are usually determined by trial and error.

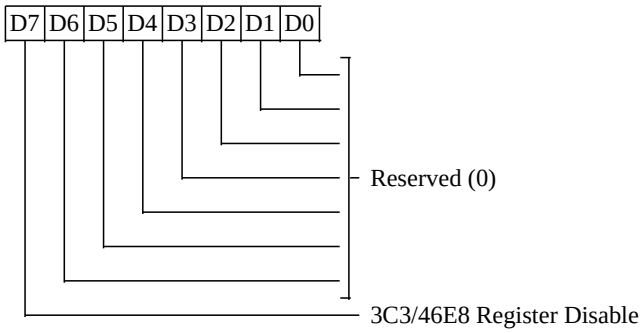
3-0 Polynomial 'N' value

7-4 Polynomial 'M' value

This register defaults to '10111101' on RESET.

SETUP / DISABLE CONTROL REGISTER (XR70)

Read/Write at I/O Address 3B7h/3D7h
Index 70h



6-0 Reserved (0)

7 3C3 / 46E8 Register Disable

0 In the MC and PI bus, port 3C3h works as defined to provide control of VGA disable (the DISA/ pin may also be used to disable the VGA). In the PC bus, port 46E8h works as defined to provide control of VGA disable and setup mode (DISA/ and SETUP/ functions are not provided on pins).

1 In the MC and PI bus, writes to I/O port 3C3 have no effect (the VGA can still be disabled via the DISA/ pin). In the PC bus, writes to I/O port 46E8h have no effect (the VGA remains enabled and will not go into setup mode).

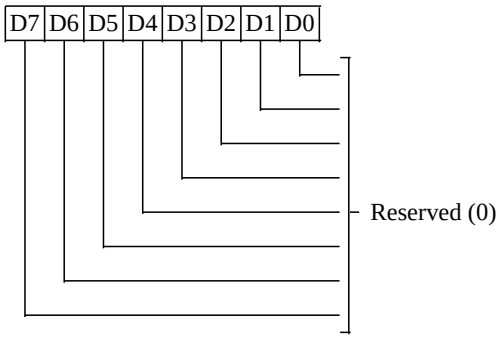
Note: Writes to register 46E8 are only effective in PC bus configurations (46E8 is ignored in MC and PI bus configurations independent of the state of this bit). Writes to 3C3 are only effective in MC and PI bus configurations (3C3 is ignored in PC bus configurations independent of the state of this bit).

Reads from ports 3C3 and 46E8h have no effect independent of the programming of this register (both 3C3 and 46E8h are write-only registers).

This register is cleared by RESET.

FP COMPENSATION DIAGNOSTIC REGISTER (XR7D)

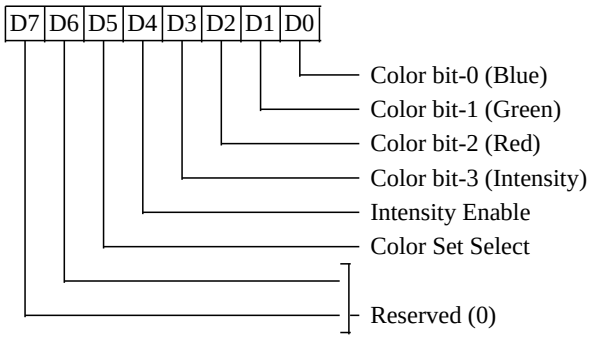
Read/Only at I/O Address 3B7h/3D7h
Index 7Dh



These bits are reserved for future use and currently all read back zero.

CGA / HERCULES COLOR SELECT REGISTER (XR7E)

Read/Write at I/O Address 3B7h/3D7h
Index 7Eh



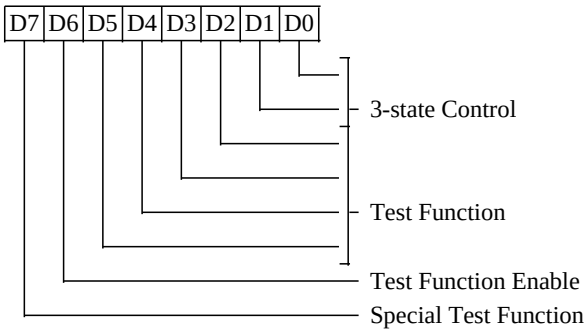
This I/O address is mapped to the same register as I/O address 3D9h. This alternate mapping effectively provides a color select register for Hercules mode. Writes to this register will change the copy at 3D9h. The copy at 3D9h is visible only in CGA emulation or when the extension registers are enabled. The copy at XR7E is visible when the extension registers are enabled.

5-0 See register 3D9

7-6 Reserved (0)

DIAGNOSTIC REGISTER (XR7F)

Read/Write at I/O Address 3B7h/3D7h
Index 7Fh



0 3-State Control Bit 0

0 Normal outputs (default on Reset)
1 3-state output pins: P7-0, FLM, LP, ACDCLK, SHFCLK, RDY, and BLANK/.

1 3-State Control Bit 1

0 Normal outputs (default on Reset)
1 3-state output pins: RAS/, CASL/, CASH/, WE/, and MA0-8.

5-2 Test Function

These bits are used for internal testing of the chip when bit-6 = 1.

6 Test Function Enable

This bit enables bits 5-2 for internal testing.

0 Disable test function bits (default)
1 Enable test function bits

7 Special Test Function

This bit is used for internal testing and should be set to 0 (default to 0 on reset) for normal operation.

Application Schematic Examples

This section includes schematic examples showing various 65510 interfaces. The schematics are broken down into three main groups for discussion:

1) **System Bus Interface**

• PC/AT Notebook	16-Bit	ISA Bus
• PC/Chip (F8680)	8-Bit	ISA Bus
• Micro Channel	16-Bit	MC Bus
• x86 SL	16-Bit	PI Bus
• 386 SX or 386 DX	16-Bit	Local Bus

2) **Display Memory Interface**

- One 256Kx16 DRAM (2 CAS/ or 2 WE/)
- Four 256Kx4 DRAMs

3) **Panel Interface**

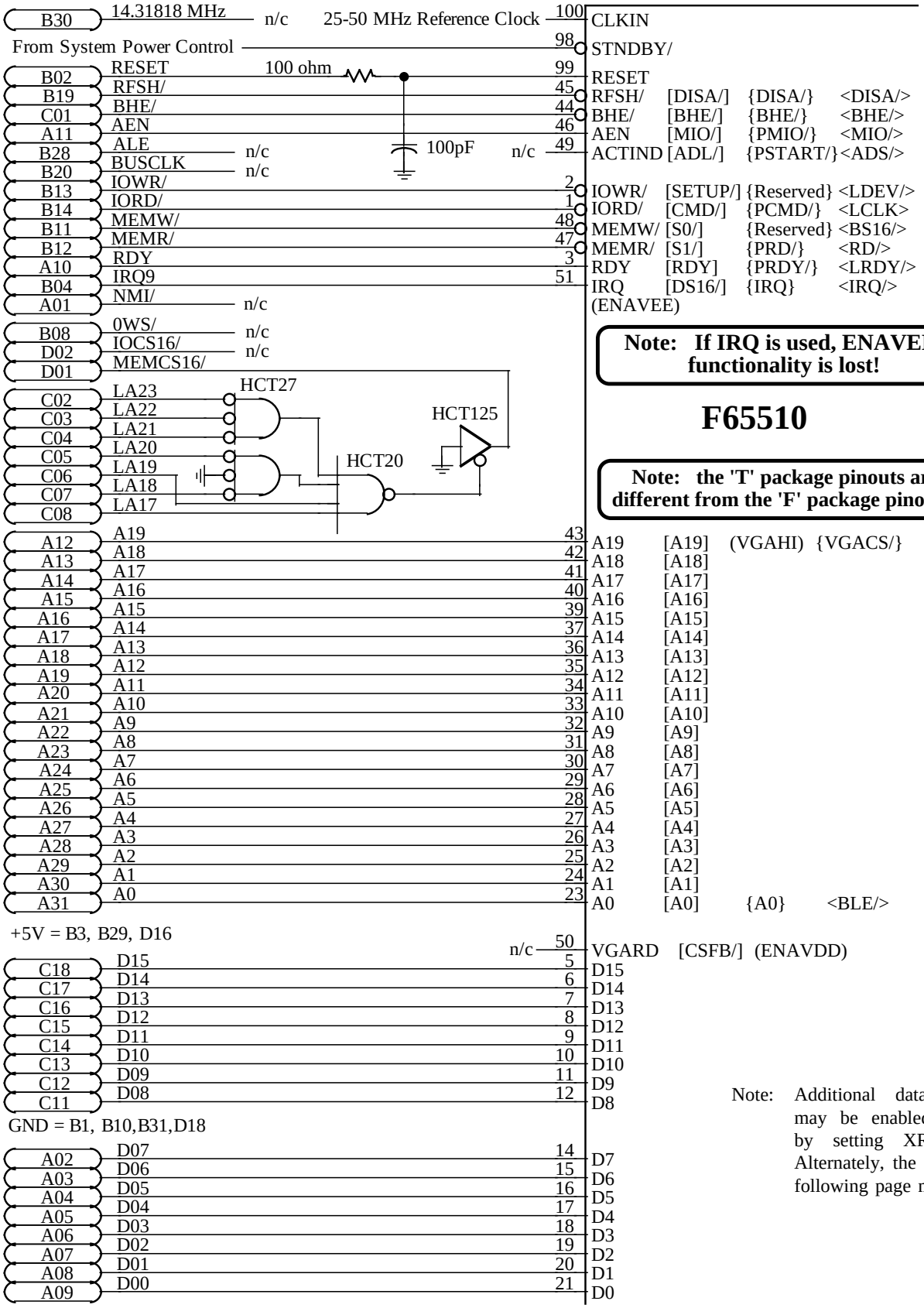
- F65510 Panel Interface

To design a system around the 65510, select one schematic page from each of the three groups above.

Selection of a bus interface for the VGA controller is generally dictated by the type of bus available in the system. If performance is a concern, however, and a 386 or 486 CPU is being used, a local bus interface should be used instead.

Selection of a memory interface depends on price and availability of the two sizes of DRAMs. Additional considerations are the amount of board space available (one 256Kx16 will generally require less board space) and power usage requirements (256Kx16 DRAMs have self-refresh capability so allow the 65510 and all clock inputs to be shut down during standby mode).

Note: The circuits in this section assume the use of the F65510 (rectangular 100-pin flat pack with 0.65 mm lead pitch). The pinouts of the T65510 (square 100-pin flat pack with 0.50 mm lead pitch) are different (the pinouts are rotated clockwise by two pins relative to the 'F' package pinouts).



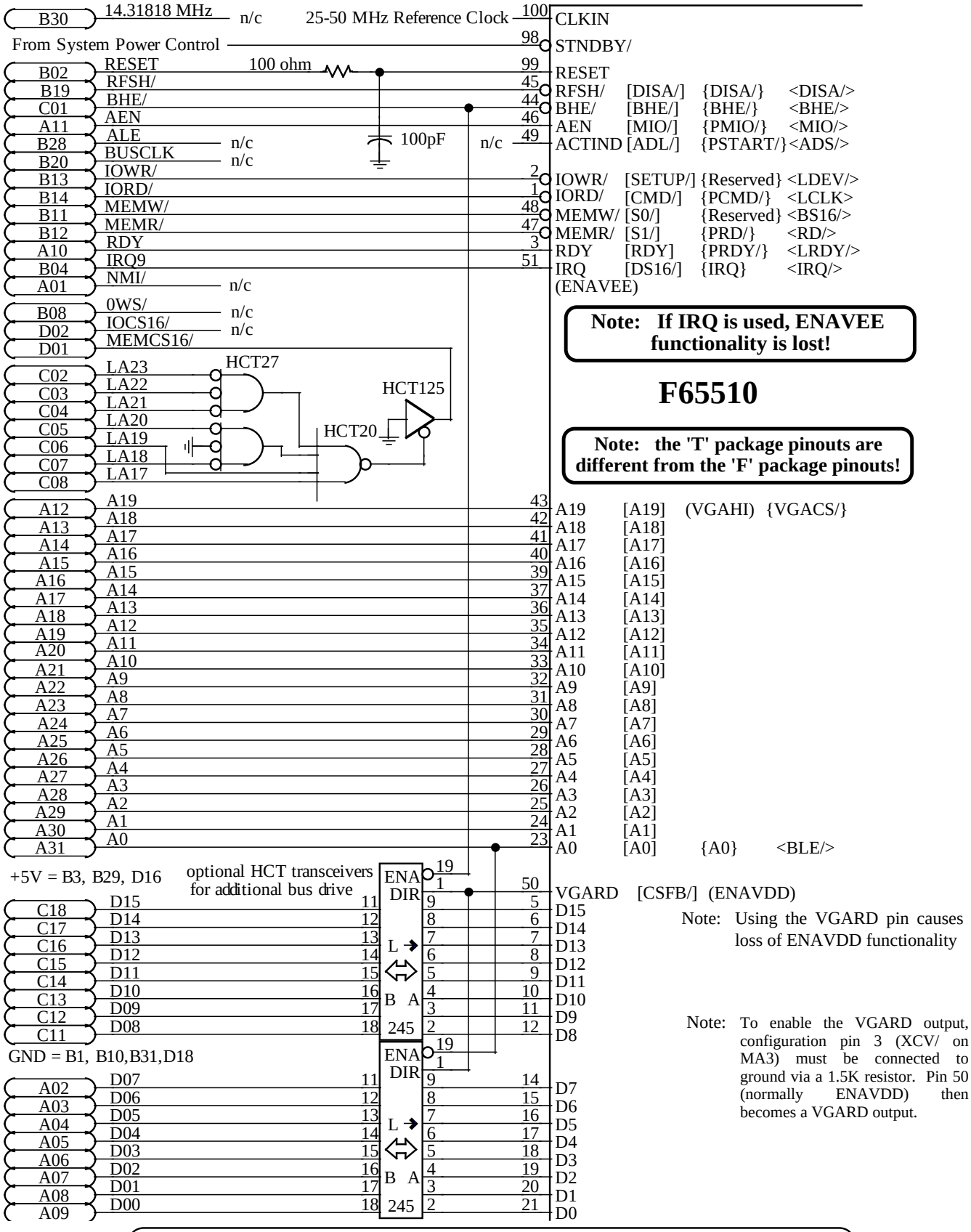
Note: If IRQ is used, ENAVEE functionality is lost!

F65510

Note: the 'T' package pinouts are different from the 'F' package pinouts!

Note: Additional data bus drive may be enabled if required by setting XR6C bit-3=1. Alternately, the circuit on the following page may be used.

Circuit Example - F65510 Interface to 16-Bit ISA Bus



Note: If IRQ is used, ENAVEE functionality is lost!

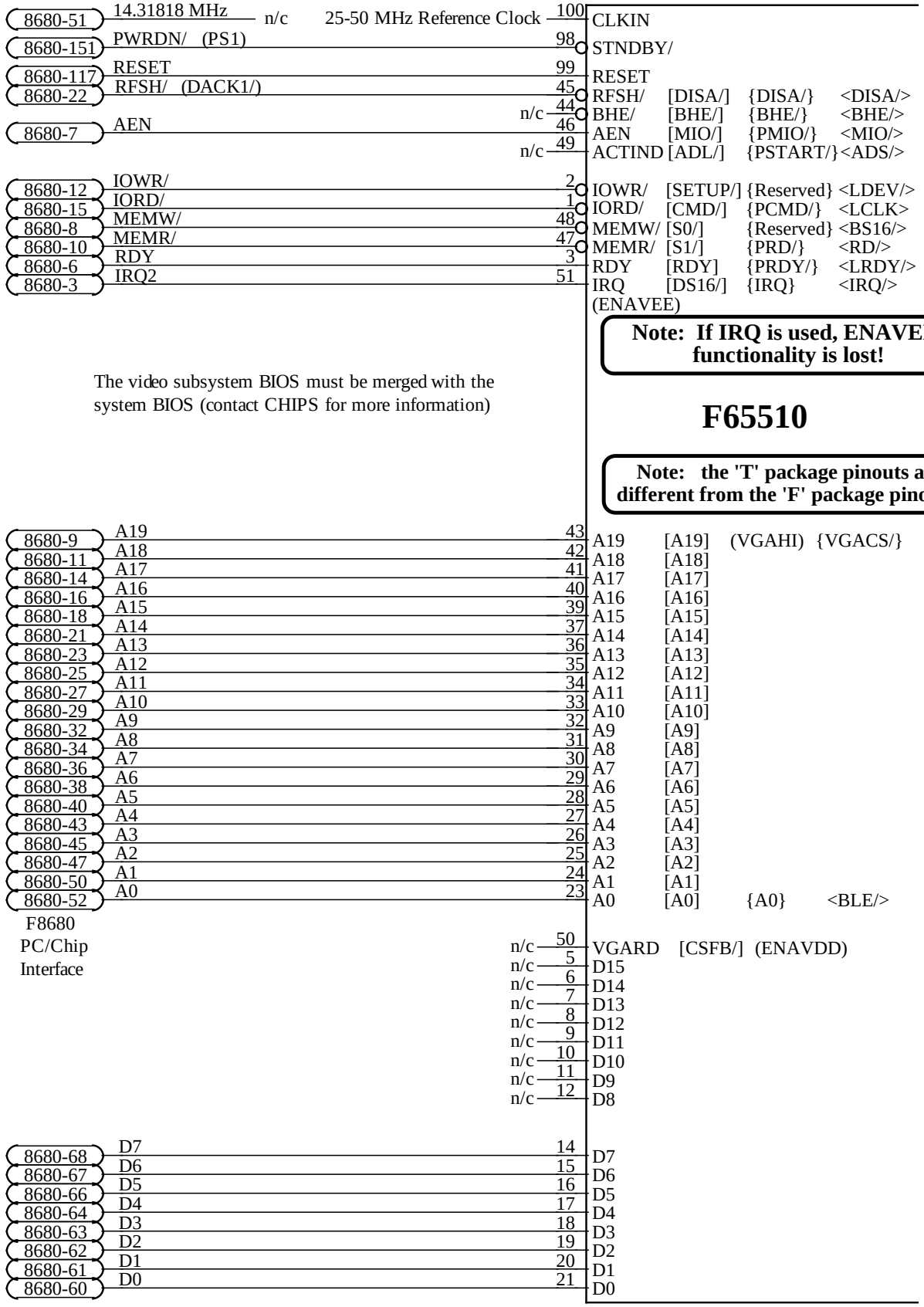
F65510

Note: the 'T' package pinouts are different from the 'F' package pinouts!

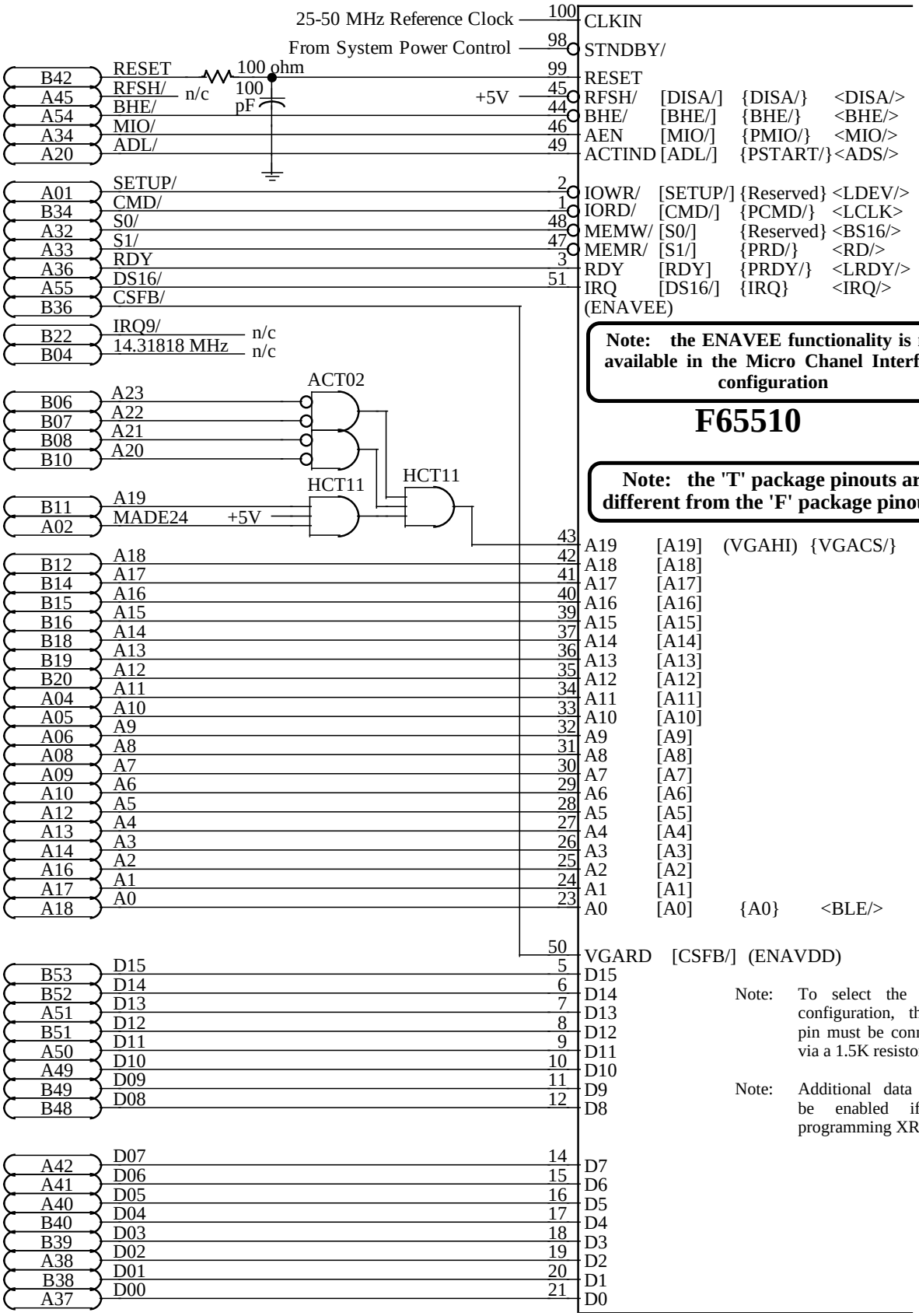
Note: Using the VGARD pin causes loss of ENAVDD functionality

Note: To enable the VGARD output, configuration pin 3 (XCV/ on MA3) must be connected to ground via a 1.5K resistor. Pin 50 (normally ENAVDD) then becomes a VGARD output.

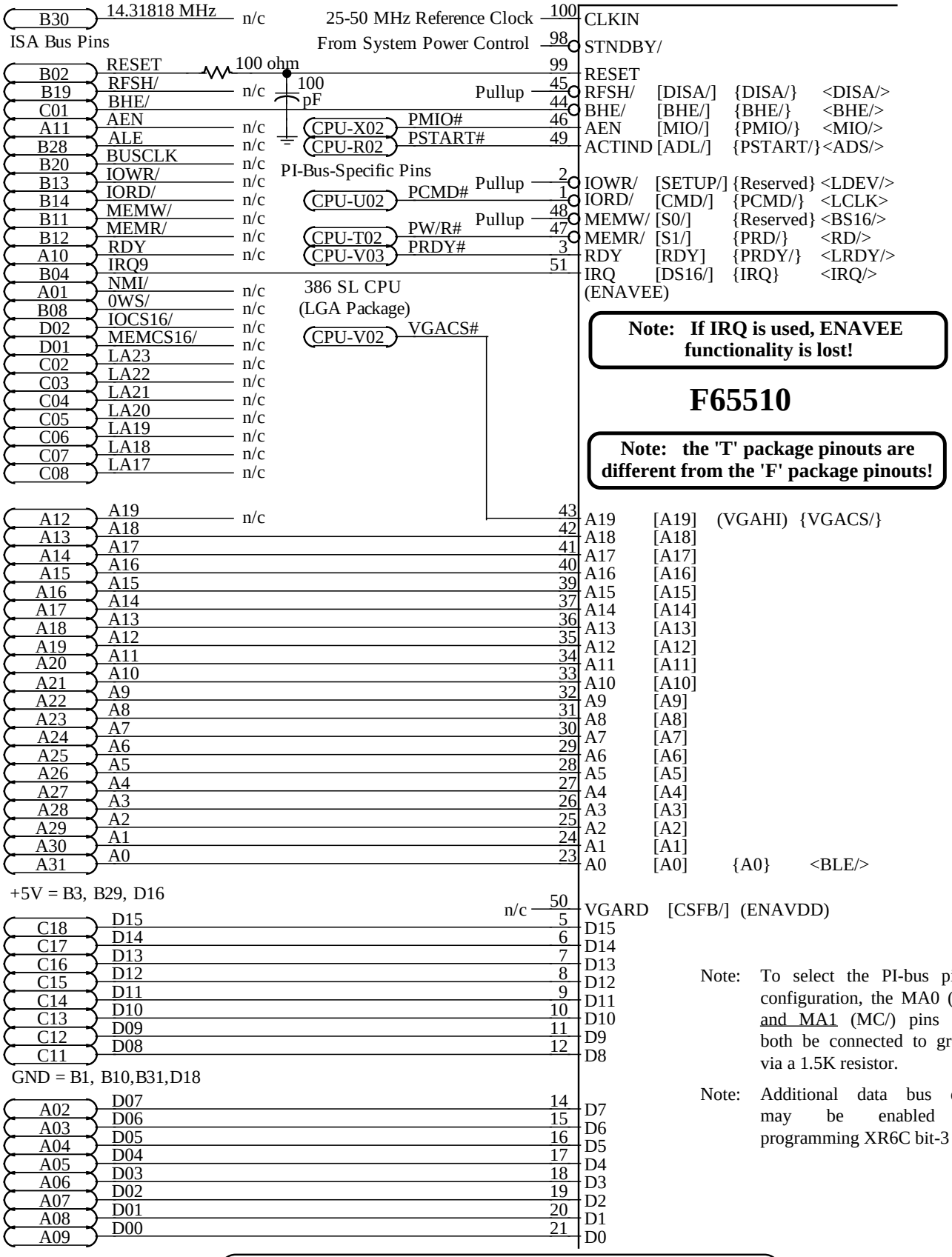
Circuit Example - 65510 Add-In Card ISA Bus (Extra Bus Drive Option)



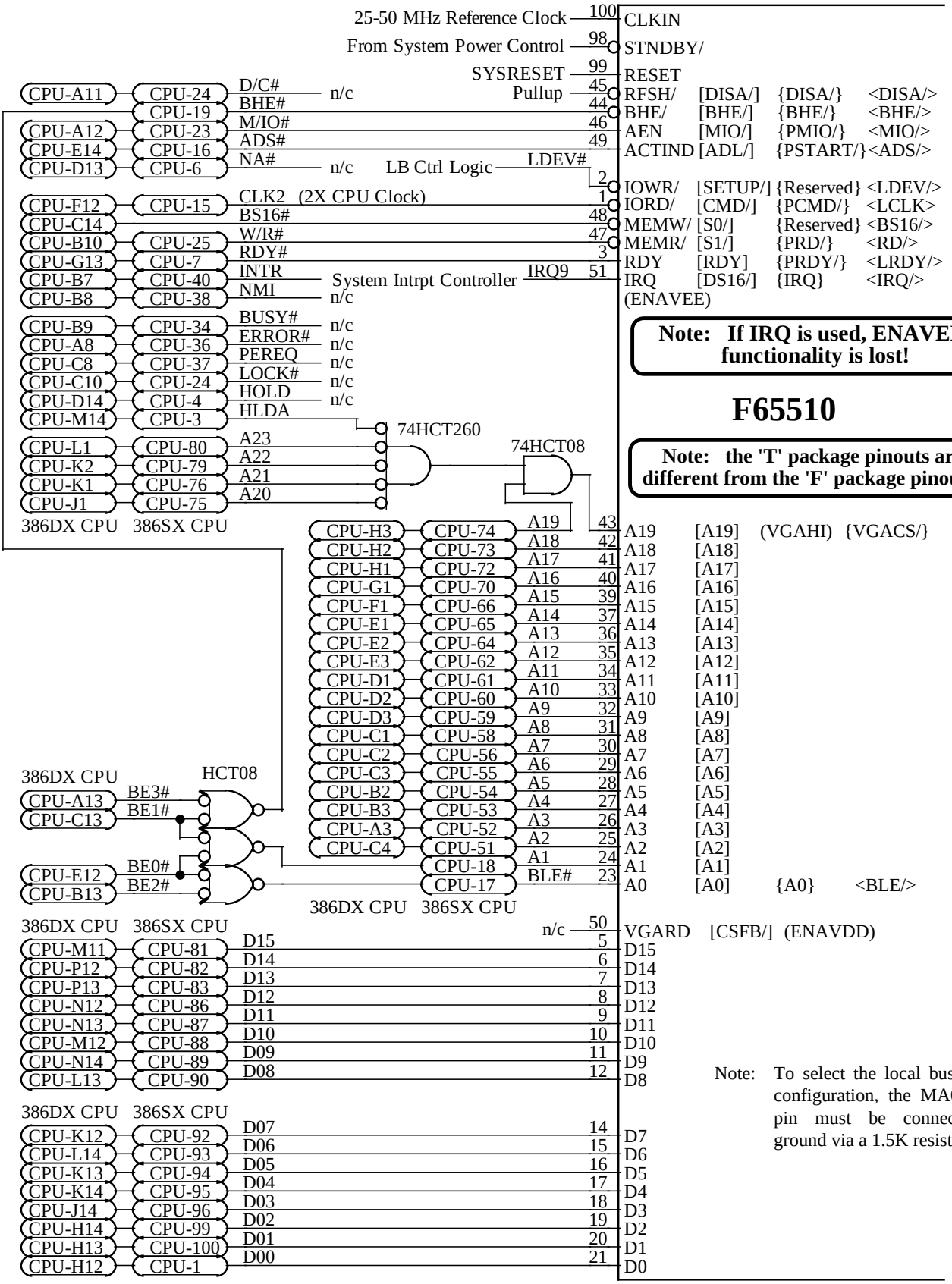
Circuit Example - 65510 Interface to PC/Chip (8-bit ISA Bus)



Circuit Example - 65510 Interface to Micro Channel Bus



Circuit Example - 65510 Interface to PI Bus (x86 SL)



Note: If IRQ is used, ENAVEE functionality is lost!

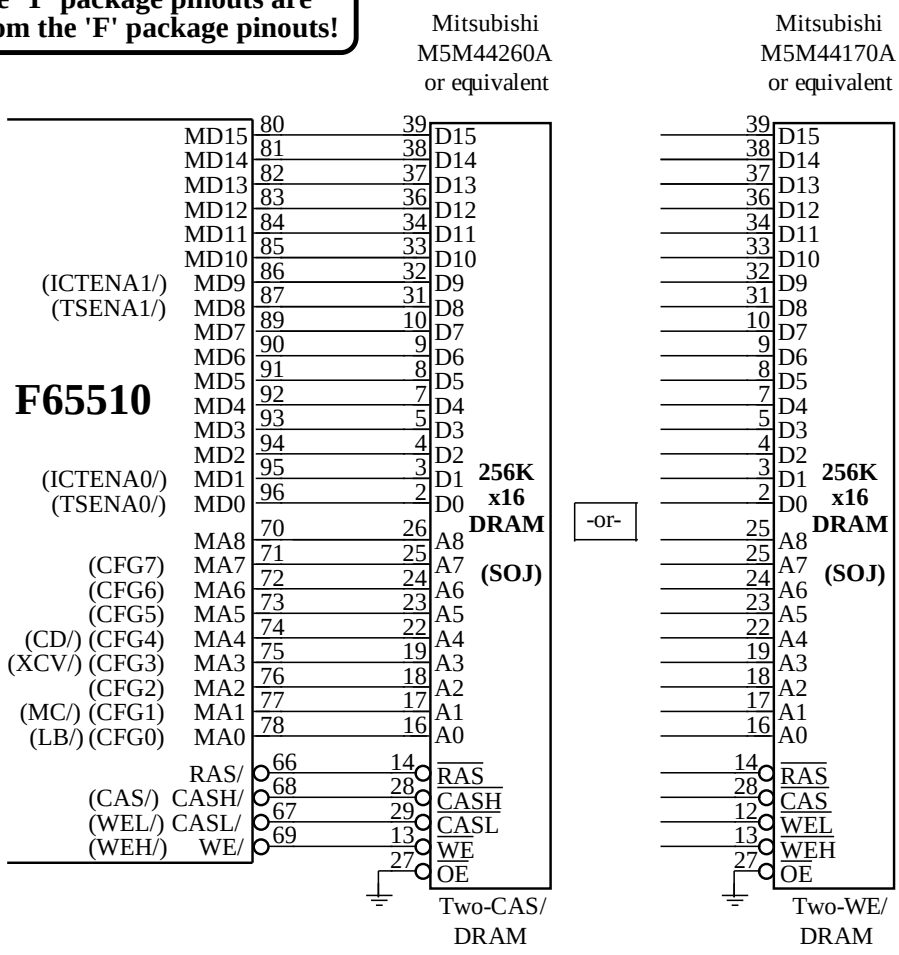
F65510

Note: the 'T' package pinouts are different from the 'F' package pinouts!

Note: To select the local bus pinout configuration, the MA0 (LB/) pin must be connected to ground via a 1.5K resistor.

Circuit Example - 65510 Interface to 386 SX/DX Local Bus

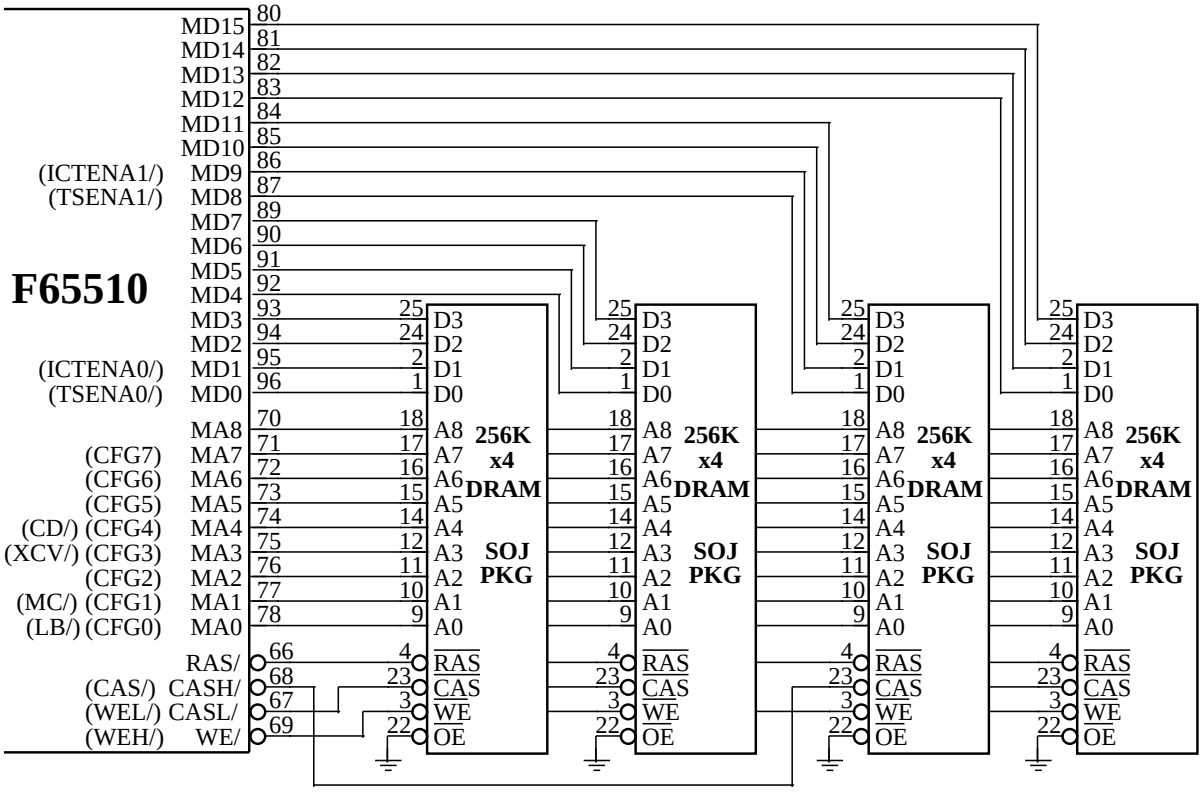
Note: the 'T' package pinouts are different from the 'F' package pinouts!



Circuit Example - 65510 Display Memory (One 256Kx16 DRAM)

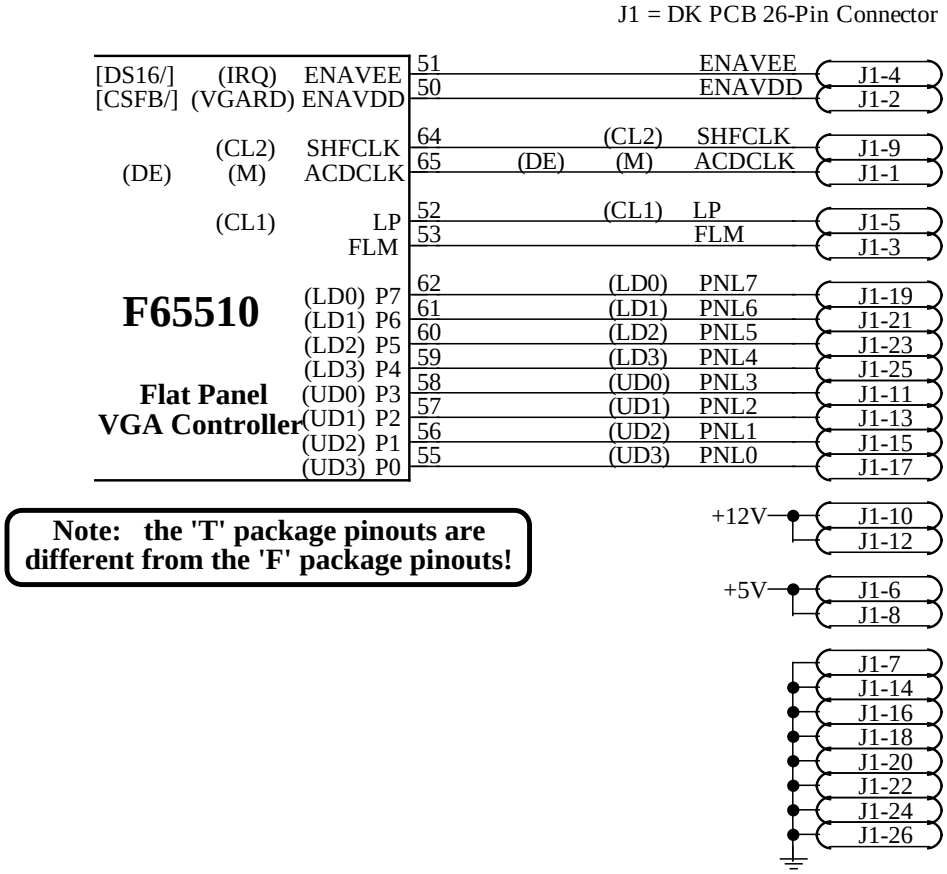
Note: 1.5K pulldown resistors may also be connected to selected MA (memory address) outputs above to select various configuration options.

Note: the 'T' package pinouts are different from the 'F' package pinouts!



Circuit Example - 65510 Display Memory (Four 256Kx4 DRAMs)

Note: 1.5K pulldown resistors may also be connected to selected MA (memory address) outputs above to select various configuration options.



Circuit Example - F65510 Panel Interface

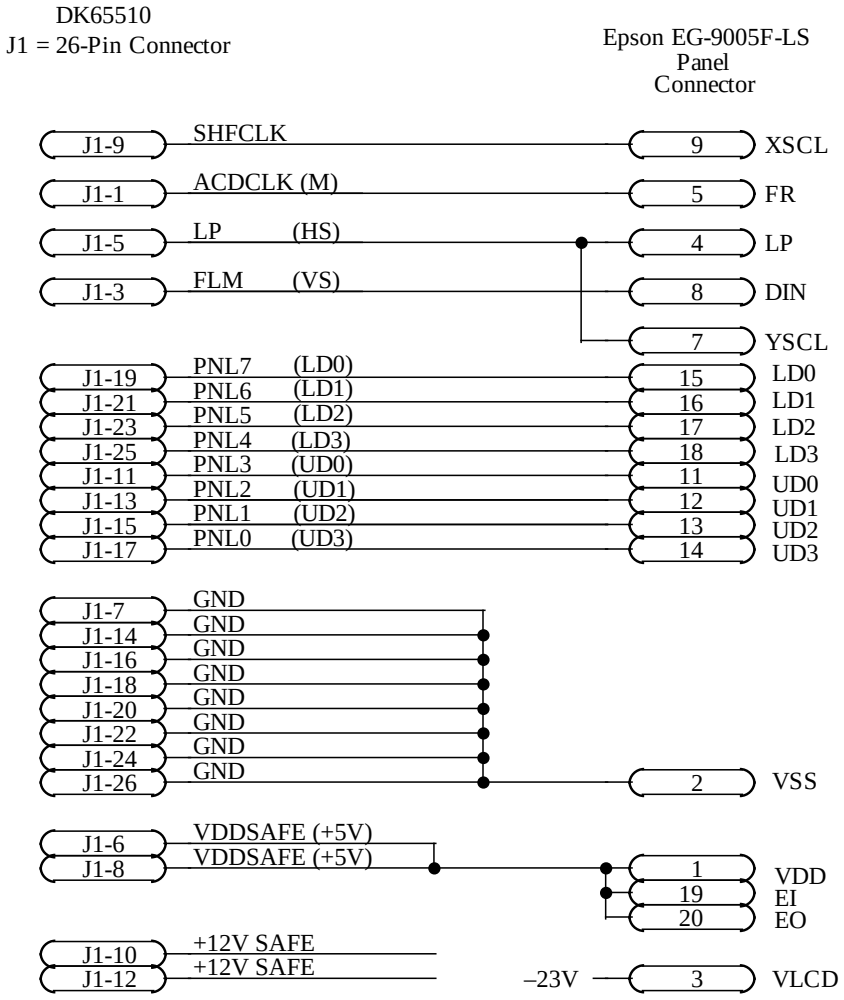
Note: Additional drive may be enabled for the panel output pins if required by programming XR6C bit-2 =1.

Flat Panel Interface Examples

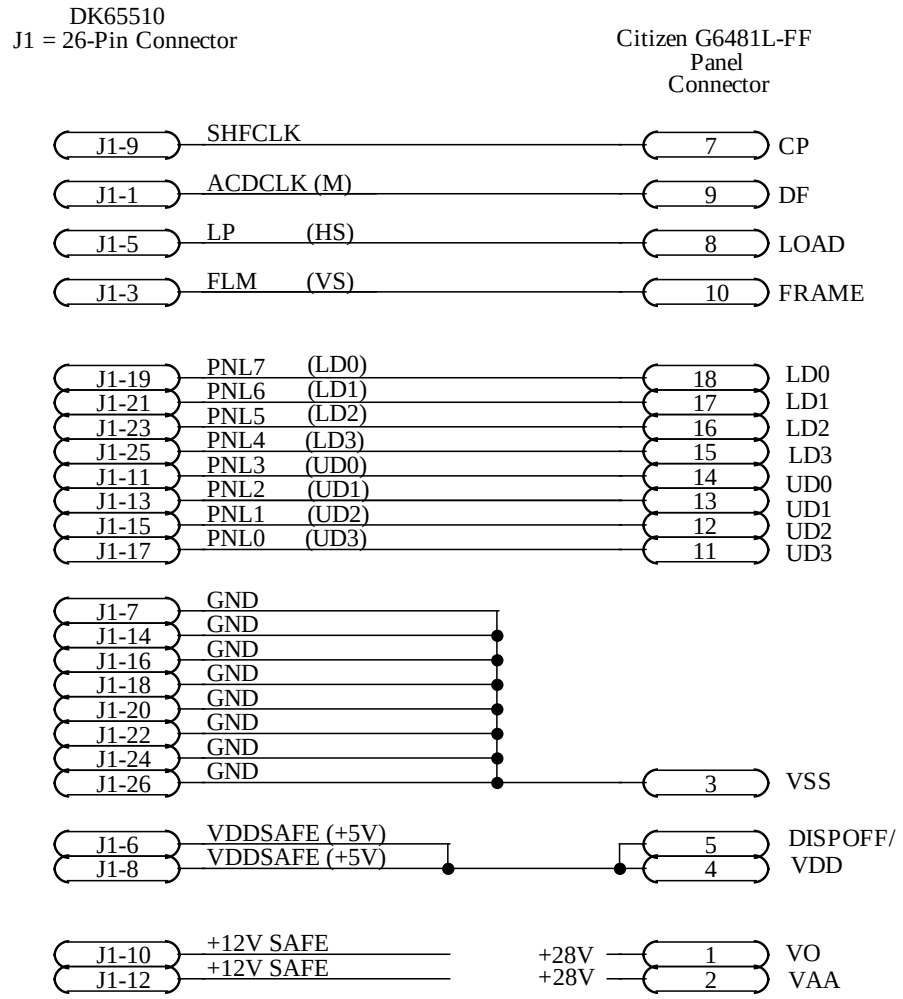
This section includes schematic examples showing how to connect the 65510 to various flat panel displays.

Monochrome Panels

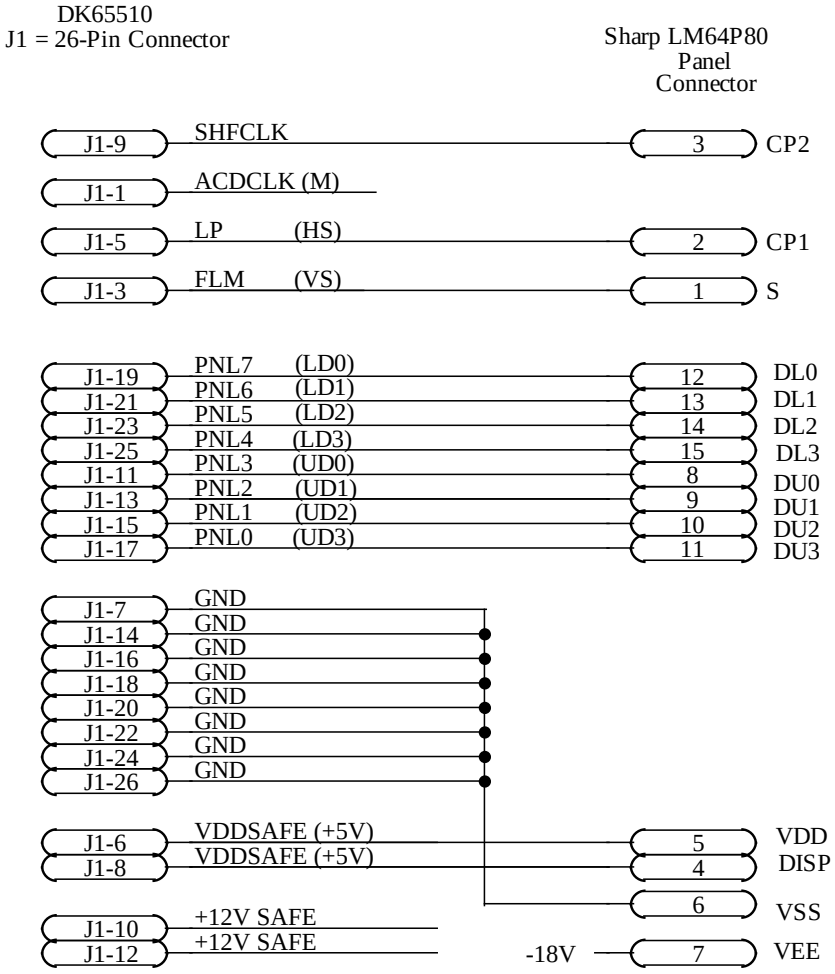
	Manufacturer	Part Number	Panel Resolution	Panel Technology	Panel Drive	Panel Interface	Panel Data Transfer	Panel Gray Levels
1)	Epson	EG-9005F-LS	640x480	LCD	DD	8-Bit	8 Pixels/Clk	2
2)	Citizen	G6481L-FF	640x480	LCD	DD	8-Bit	8 Pixels/Clk	2
3)	Sharp	LM64P80	640x480	LCD	DD	8-Bit	8 Pixels/Clk	2
4)	Sanyo	LCM-6494-24NAC	640x480	LCD	DD	8-Bit	8 Pixels/Clk	2
5)	Hitachi	LMG5162XUFC	640x480	LCD	DD	8-Bit	8 Pixels/Clk	2



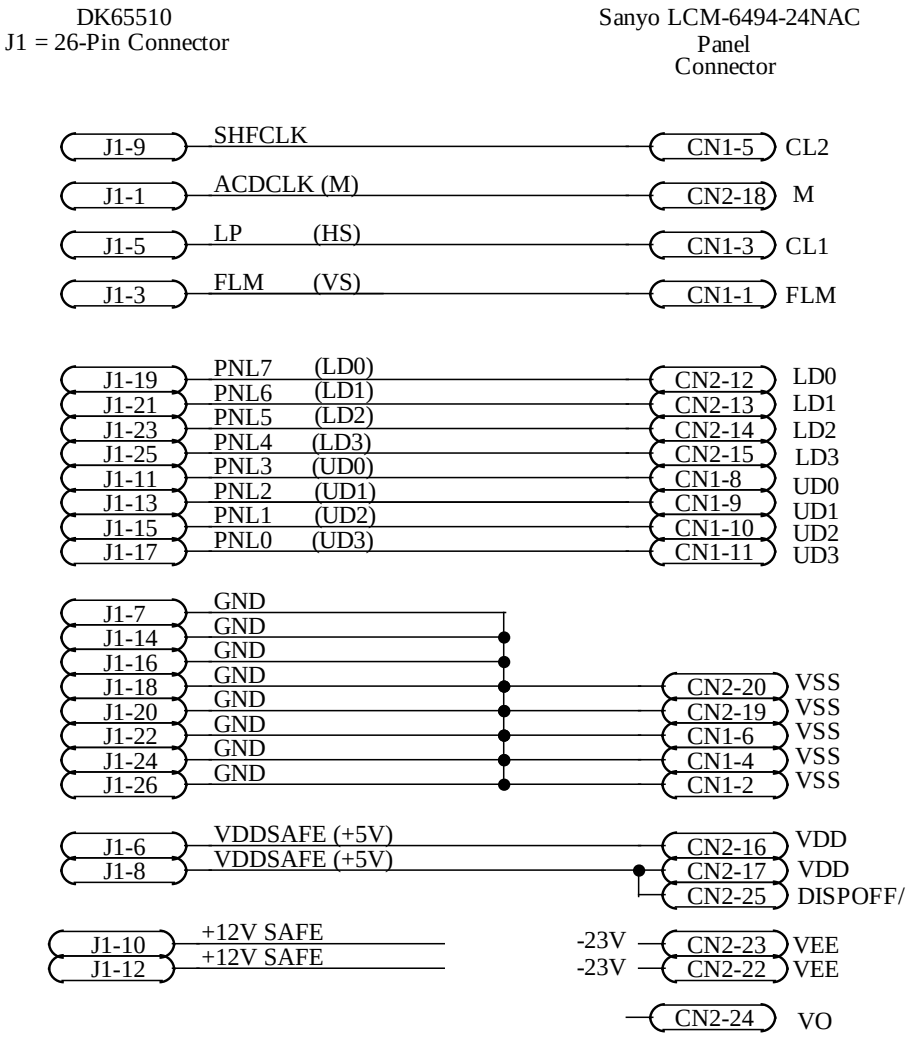
65510 Interface - Epson EG-9005F-LS (640x480 Monochrome LCD DD Panel)



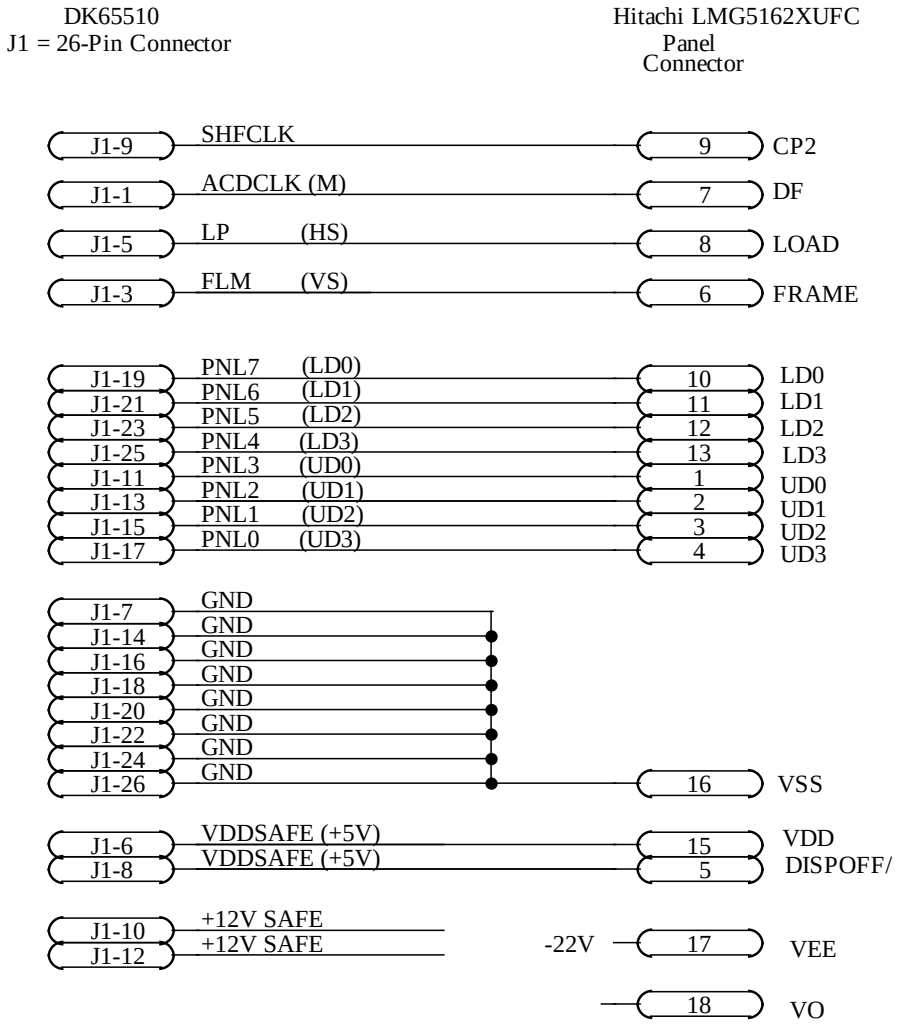
65510 Interface - Citizen G6481L-FF (640X480 Monochrome LCD-DD Panel)



65510 Interface - Sharp LM64P80 (640x480 Monochrome LCD DD Panel)



65510 Interface - Sanyo LCM-6494-24NAC (640x480 Monochrome LCD DD Panel)



65510 Interface - Hitachi LMG5162XUFC (640x480 Monochrome LCD DD Panel)

Flat Panel Timing

The 65510 is the most flexible flat panel graphics controller available, enabling the widest possible range of panel interfaces. This section includes timing diagrams for the following configurations:

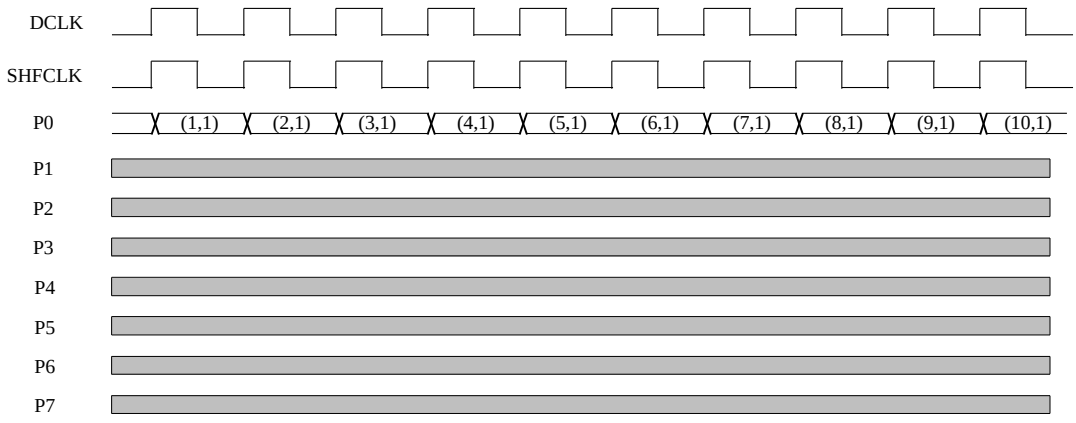
- Monochrome, Single Drive, 1 pixel/clock
- Monochrome, Single Drive, 2 pixels/clock
- Monochrome, Single Drive, 4 pixels/clock
- Monochrome, Single Drive, 8 pixels/clock
- Panel with 16 internal levels of gray, Single Drive, 1 pixel/clock, 4 bits/pixel
- Panel with 16 internal levels of gray, Single Drive, 2 pixels/clock, 4 bits/pixel
- Monochrome, Double Drive, 640x480, 8 pixels/clock

Extension register 50 (XR50) bits 5-4 define the clock divide (CD):

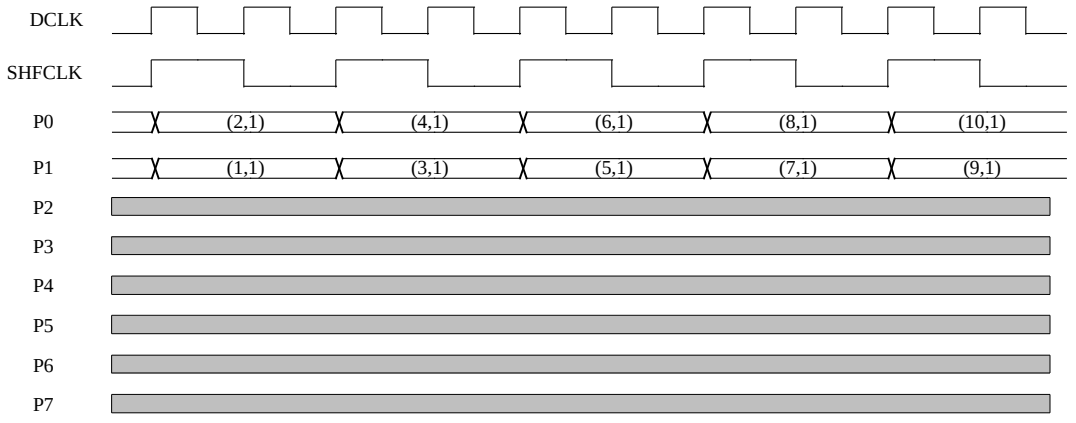
00 - Shift clock frequency = dot clock frequency
01 - Shift clock frequency = dot clock frequency/2
10 - Shift clock frequency = dot clock frequency/4
11 - Shift clock frequency = dot clock frequency/8

Extension Register 50 (XR50) bits 1-0 determine the FRC level used:

00 - 8-frame FRC
01 - 16-frame FRC
10 - 4-frame FRC



Monochorome, Single Drive, 1 pixel/clock, CD = 00, FRC = 00, 01, 10

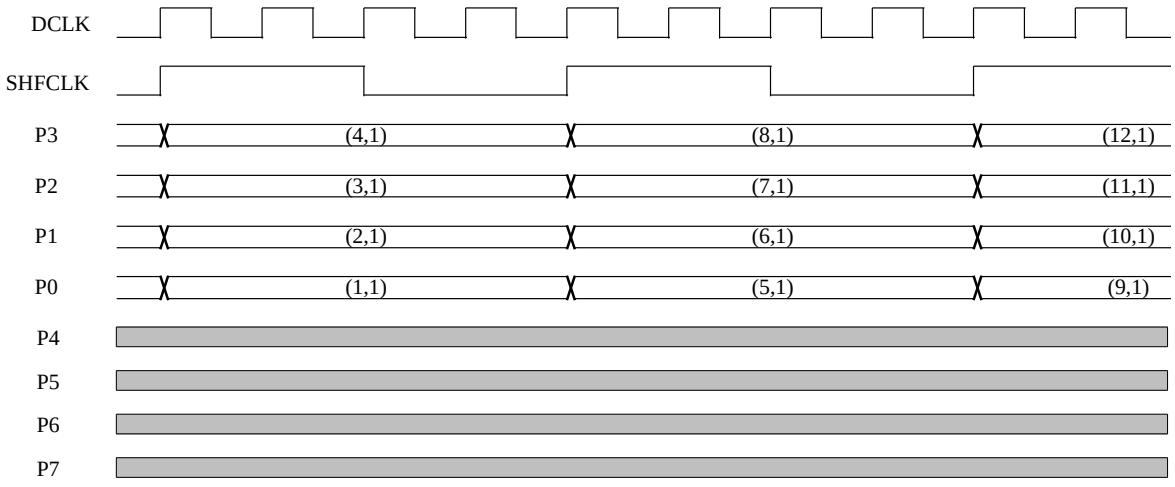


Monochrome, Single Drive, 2 pixels/clock, CD = 01, FRC = 00, 01, 10

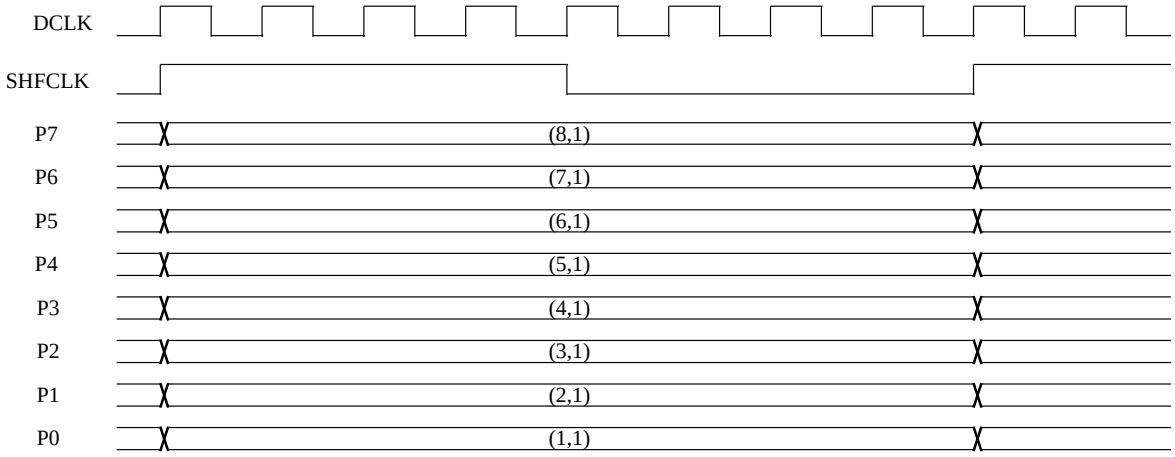
Panel Timing - Single Drive (1 & 2 Pixels / Clock)

These timing diagrams show the 65510 outputs to the flat panel for two scenarios:

1) One pixel per shift clock (where shift clock frequency = dot clock frequency) for monochrome panels with no internal gray-scale generation
2) Two pixels per shift clock (where shift clock frequency = dot clock frequency / 2) for monochrome panels with no internal gray-scale generation



Monochrome, Single Drive, 4 pixels/clock, CD = 10, FRC =00, 01, 10

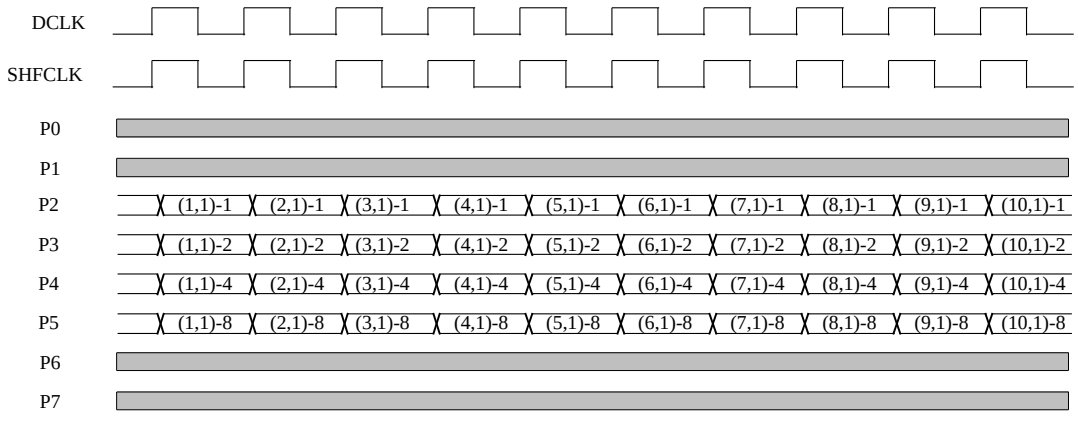


Monochrome, Single Drive, 8 pixels/clock, CD = 11, FRC = 00,01,10

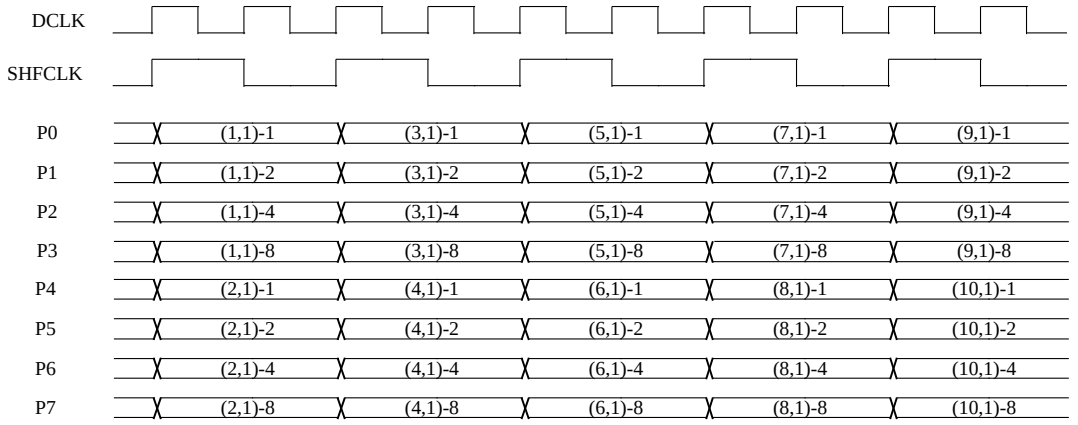
Panel Timing - Single Drive (4 & 8 Pixels / Clock)

These timing diagrams show the 65510 outputs to the flat panel for two scenarios:

1) Four pixels per shift clock (where shift clock frequency = dot clock frequency / 4) for monochrome panels with no internal gray-scale generation
2) Eight pixels per shift clock (where shift clock frequency = dot clock frequency / 8) for monochrome panels with no internal gray-scale generation



Monochrome, Single Drive, 1 pixel/clock, CD = 00, FRC = 11

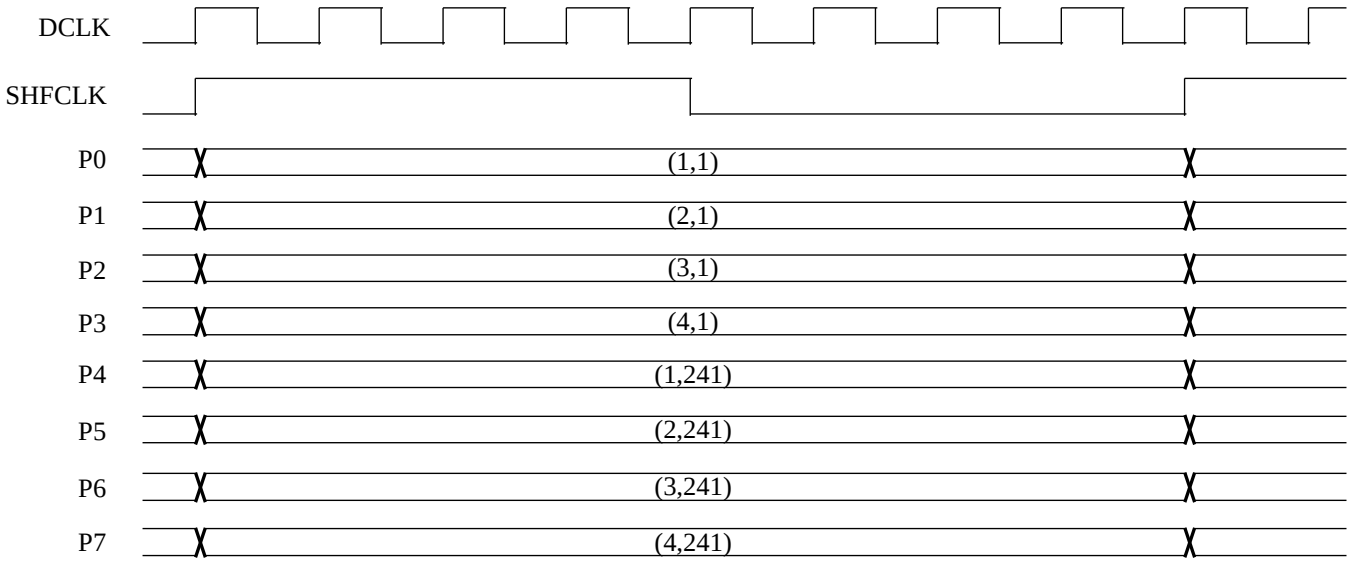


Monochrome, Single Drive, 2 pixels/clock, CD = 01, FRC = 11

Panel Timing - Single Drive (1 & 2 Pixels / Clock) 16 Gray Levels

These timing diagrams show the 65510 outputs for a monochrome flat panel display with 16 levels of internal gray scale generation. Two scenarios are presented:

1) One pixel per shift clock (where shift clock frequency = dot clock frequency)
2) Two pixels per shift clock (where shift clock frequency = dot clock frequency / 2)



Monochrome, Double Drive, 8 pixels/clock, CD = 11, FRC = 00, 01, 10

Panel Timing - 640x480 LCD DD

This timing diagram shows the 65510 outputs for a double drive monochrome panel with an eight pixels-per-shift-clock interface where the shift clock frequency equals the dot clock frequency divided by 8.

Flat Panel Pixel Timing

This section shows detailed timing diagrams for the 65510 outputting data and control sequences to a variety of panel types. The 65510 is a highly configurable controller which can interface to virtually all existing monochrome LCD, EL, and Plasma panels. The panel types supported are:

Dual panel-Double drive (DD)
- 8 pixels/clock, 1 bit/pixel

Dual panel-Single drive (DS)
- 1 pixel/clock, 6 bits/pixel
- 2 pixels/clock, 4 bits/pixel
- 4 pixels/clock, 2 bits/pixels
- 8 pixels/clock, 1 bit/pixel

Single panel-Single drive (SS)
- 1 pixel/clock, 6 bits/pixel
- 2 pixels/clock, 4 bits/pixel
- 4 pixels/clock, 2 bits/pixels
- 8 pixels/clock, 1 bit/pixel

The panel type (PT) is determined by XR51 bits 1-0:

00 Single panel-Single drive (SS)
10 Dual panel-Single drive (DS)
11 Dual panel-Double drive (DD)

The 65510 provide 4, 8 and 16 level Frame Rate Control (FRC) techniques to generate multiple gray levels on monochrome panels.

The FRC selected is determined by XR50 bits 1-0:

00 8-frame FRC
01 16-frame FRC
10 4-frame FRC

The 65510 can be programmed to output 1 pixel per shift clock, 2 pixels per shift clock, 4 pixels per shift clock or 8 pixels per shift clock. This is achieved by programming the frequency ratio between the dot clock and the shift clock.

The shift clock divide (CD) is set by XR50 bits 5-4:

00 shift clock = dot clock; 1 pixel/shift clock
01 shift clock = dot clock/2; 2 pixels/shift clock
10 shift clock = dot clock/4; 4 pixels/shift clock
11 shift clock = dot clock/8; 8 pixels/shift clock

Pixel output timings are shown for the following panel configurations:

1) Dual Panel-Double Drive 640x480
   Monochrome LCD Panel
   8 pixels/shift clock, 1bit/pixel

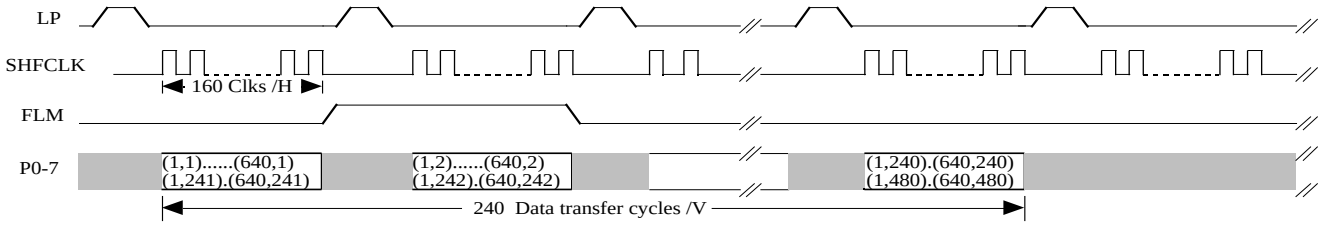
   CD = 10 (with Frame Accelerator)
   CD = 11 (without Frame Accelerator)
   FRC = 00, 01, 10, 11
   PT = 11

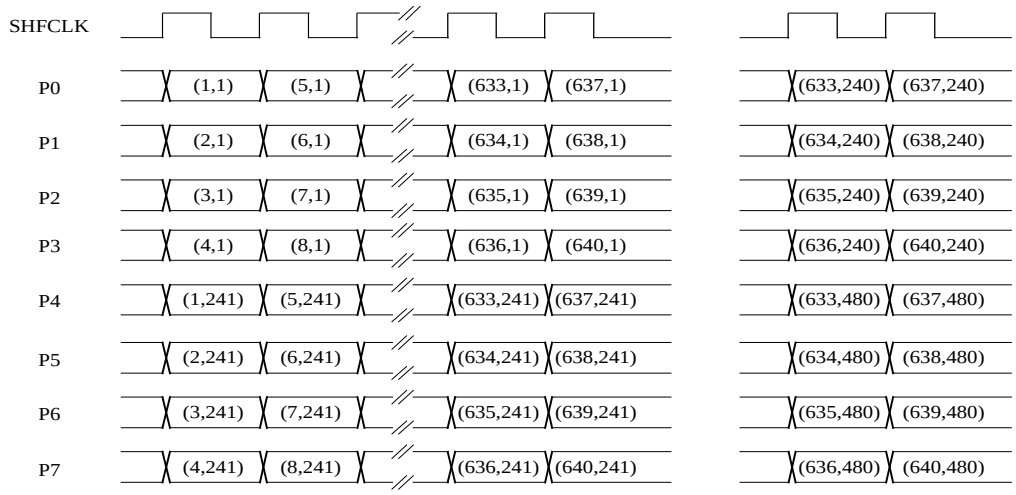
2) Dual Panel-Single Drive 640x480
   Monochrome LCD Panel
   4 pixels/shift clock, 2 bits/pixel

   CD = 10
   FRC = 00, 01, 10
   PT = 10

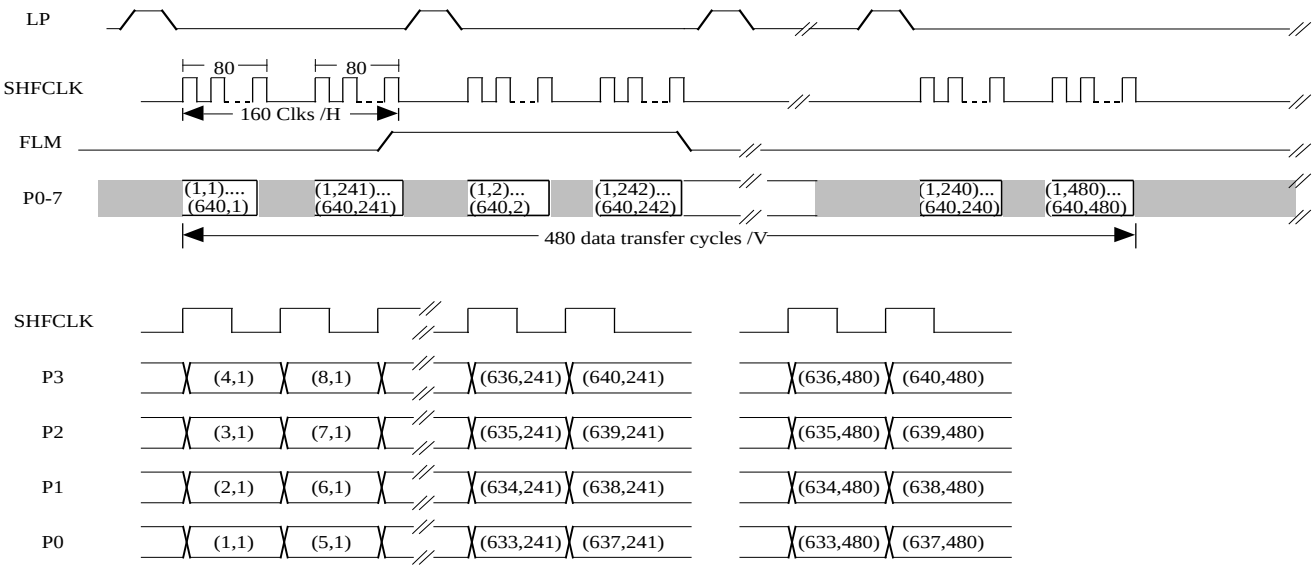
3) Single Panel-Single Drive Plasma/EL Panel
   2 Pixels/Shift Clock, 4 Bits/pixel Interface

   CD = 01
   FRC = 11
   PT = 00

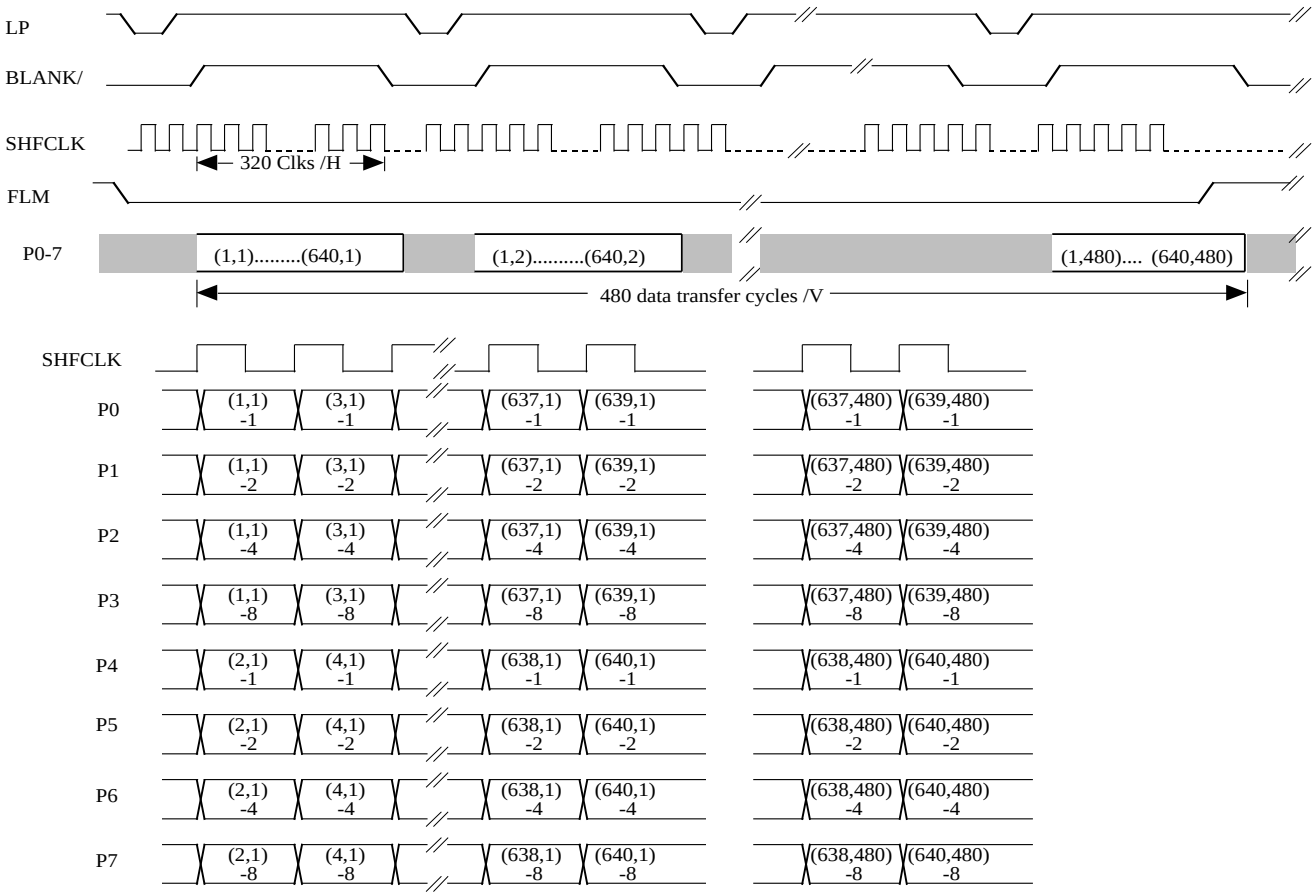




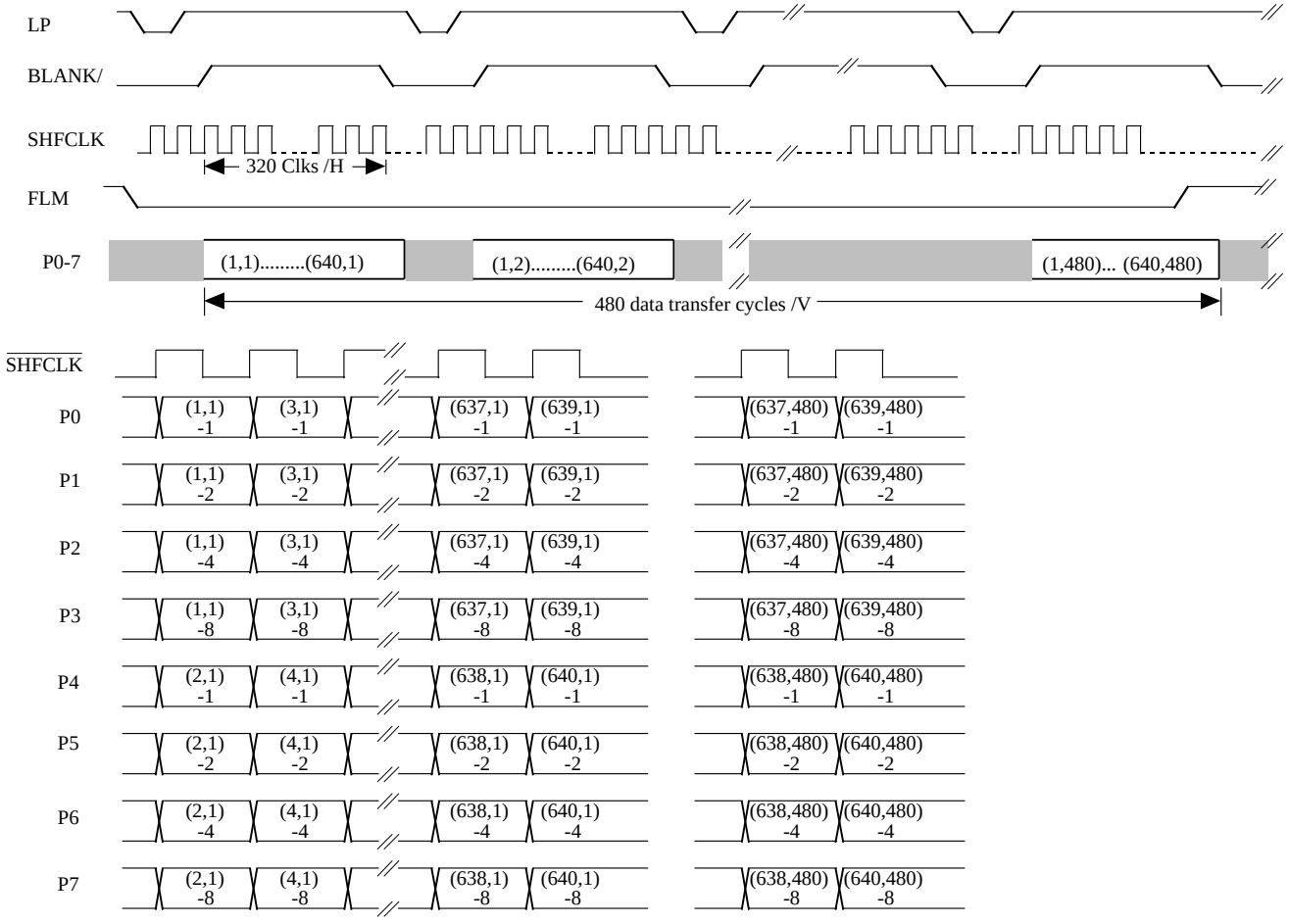
Panel Pixel Timing - LCD DD



Panel Pixel Timing - LCD DS 4-Bit Pack



Panel Pixel Timing - Plasma Panel with 2 Pixels/Shift Clock



Panel Pixel Timing - EL Panel with 2 Pixels/Shift Clock

Electrical Specifications

ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	1	W
V_{CC}	Supply Voltage	–0.5	–	7.0	V
V_I	Input Voltage	–0.5	–	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	–	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	–	85	° C
T_{STG}	Storage Temperature	–40	–	125	° C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage **(5V ±10%)**	4.5	5	5.5	V
V_{CC}	Supply Voltage **(3.3V ±10%)**	3.0	3.3	3.6	V
T_A	Ambient Temperature	0	–	70	° C

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

Electrical specifications contained herein are preliminary and subject to change without notice.

DC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
I_{CC}	Power Supply Current	0°C, **5.5V**, 50 MHz Clk	–	80	100	mA
I_{CC}	Power Supply Current	0°C, **3.3V**, 40 MHz Clk	–	50	60	mA
I_{CCS}	Power Supply Current	0°C, **5.5V**, Standby	–	300	800	µA
I_{CCS}	Power Supply Current	0°C, **3.3V**, Standby	–	180	500	µA
I_{IL}	Input Leakage Current		–100	–	+100	uA
I_{OZ}	Output Leakage Current	High Impedance	–100	–	+100	uA
V_{IL}	Input Low Voltage	All input pins	–0.5	–	0.8	V
V_{IH}	Input High Voltage	All input pins except CLKIN	2.0	–	V_{CC}+0.5	V
		CLKIN	2.8	–	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	Under max load per table below **(5V)**	–	–	0.45	V
V_{OL}	Output Low Voltage	Under max load per table below **(3.3V)**	–	–	0.5	V
V_{OH}	Output High Voltage	Under max load per table below **(5V)**	V_{CC}–0.5	–	–	V
V_{OH}	Output High Voltage	Under max load per table below **(3.3V)**	2.4	–	–	V

Note: The Icc specification for the 65510 comprises of the current drawn by the core and memory interface as well as the bus interface and display interface. The current drawn by the bus interface subsection is heavily dependant as the CPU activity to the video memory and I/O registers. The current drawn by the display interface is dependant on the load the panel presents and the refresh rates to the panel.

DC DRIVE CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Output Pins	DC Test Conditions	Min	Units
I_{OL}	Output Low Drive	RDY, ENAVEE, (IRQ)	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	8	mA
		P0-7, SHFCLK, D0-15	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	4	mA
		RAS/, CASL/, CASH/	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	4	mA
		ACDCLK, FLM, LP, ENAVDD	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	4	mA
		All other outputs	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	2	mA
I_{OH}	Output High Drive	RDY, ENAVEE, (IRQ)	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	8	mA
		P0-7, SHFCLK, D0-15	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		RAS/, CASL/, CASH/	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		ACDCLK, FLM, LP, ENAVDD	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		All other outputs	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	2	mA

AC TEST CONDITIONS

(Under Normal Operating Conditions Unless Noted Otherwise)

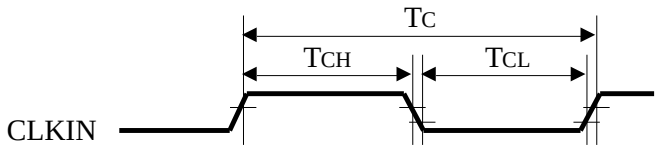
Output Pins	Output Low Voltage	Output High Voltage	Capacitive Load
D0-15, RDY	V_{OL}	3.0V	150pF
FLM, LP, ACDCLK, SHFCLK, ENAVDD, ENAVEE, P0-7,	V_{OL}	3.0V	150pF
All Others	V_{OL}	3.0V	25pF

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

Electrical specifications contained herein are preliminary and subject to change without notice.

AC TIMING CHARACTERISTICS - CLOCK TIMING

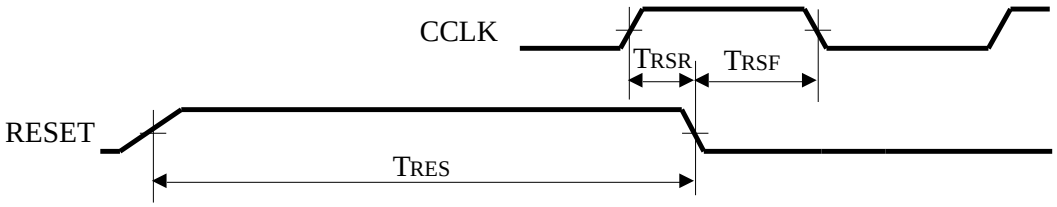
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_C	CLK Period	50.350 MHz, **(5V)**	20	–	–	nS
T_C	CLK Period	40 MHz, **(3.3V)**	25	–	–	nS
T_{CH}	CLK High Time		$0.4T_C$	–	$0.6T_C$	nS
T_{CL}	CLK Low Time		$0.4T_C$	–	$0.6T_C$	nS
T_{RF}	Clock Rise / Fall		–	–	5	nS



Clock Timing

AC TIMING CHARACTERISTICS - RESET TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
TRES	RESET Pulse Width		64TC	–	–	nS
TRSR	RESET Delay from CCLK rising edge	Local Bus only	4	–	–	nS
TRES	RESET Delay to CCLK falling edge	Local Bus only	13	–	–	nS



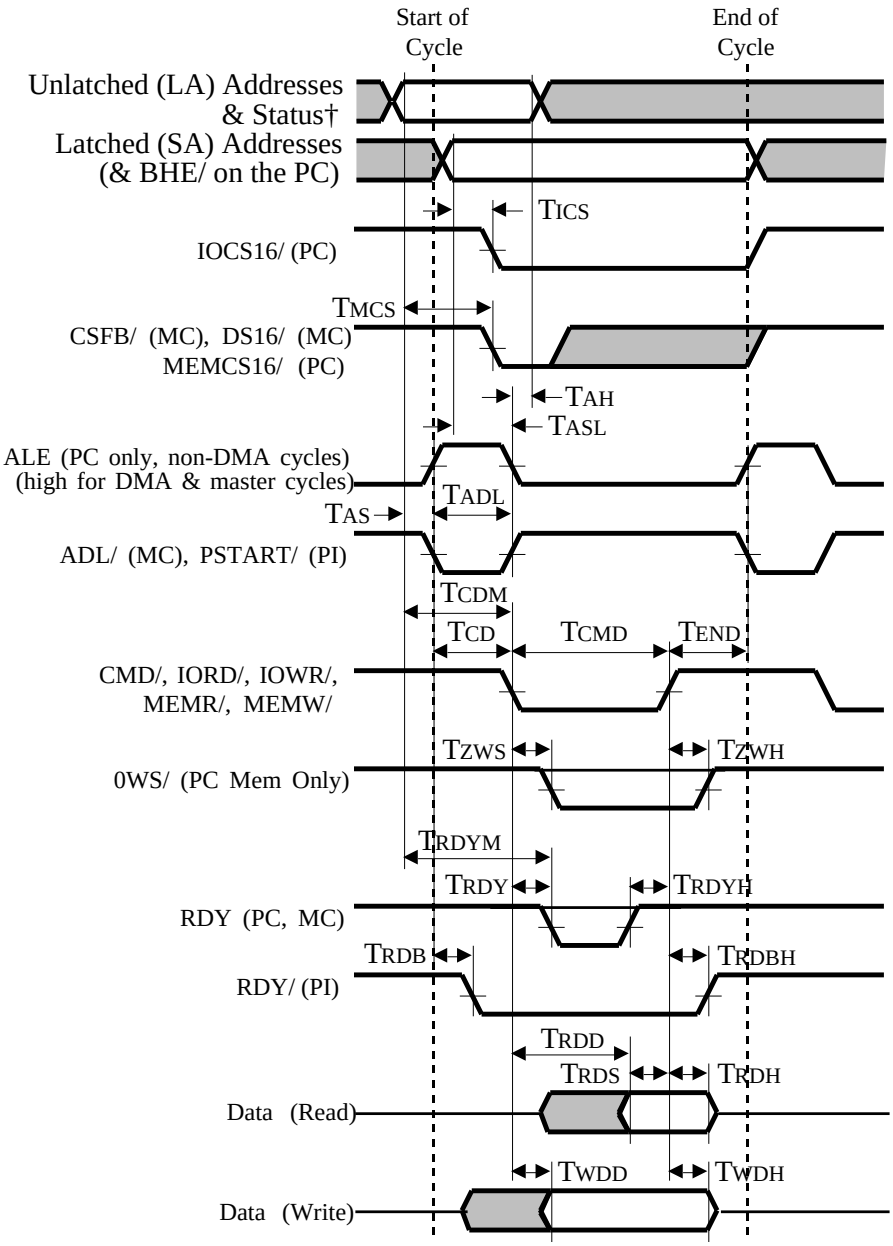
RESET Timing

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

FOR REFERENCE ONLY: BUS TIMING CHARACTERISTICS

Symbol	Parameter	8 MHz PC Bus	12.5 MHz MC Bus	20 MHz PI Bus	Units
TADL	Address Latch Pulse Width	50 min	40 min	50 min	nS
TCD	Delay from Start of Cycle to Command Strobe	50 min	40 min	50 min	nS
TCDM	Delay from Address Valid to Command Strobe	109 min	85 min	–	nS
TCMD	Command Strobe Pulse Width (Asynchronous Cycle)	176 min	90 min	70 min	nS
TCMD	Command Strobe Pulse Width (Synchronous Cycle)	176 min	90 min	40 min	nS
TEND	Delay from End of Command to Start of Next Cycle	50 min	40 min	0 min	nS
TAS	Address Setup to Start of Cycle	0 min	10 min	10 min	nS
TASL	Address Setup to Start of Command	29 min	–	–	nS
TAH	Address Hold from Start of Command	5 min	5 min	–5 min	nS
TRDD	Read Data Delay from Start of Command	187 max	60 max	–	nS
TRDS	Read Data Setup to End of Command	62 min	30 min	29 min	nS
TRDH	Read Data Hold from End of Command (Data Turnoff)	0 min	0 min	12 min	nS
		30 max	30 max	30 max	nS
TWDD	Write Data Delay from Start of Command	40 max	0 max	14 max	nS
TWDH	Write Data Hold from End of Command (Data Turnoff)	10 min	10 min	10 min	nS
		40 max	40 max	40 max	nS
TICS	Delay from Address to IOCS16/	90 max	–	–	nS
TMCS	Delay from Address to MEMCS16/, DS16/, CSFB/	66 max	55 max	–	nS
TZWS	Delay from Start of Command to Start of 0WS/ (16-bit)	40 max	–	–	nS
TZWS	Delay from Start of Command to Start of 0WS/ (8-bit)	1 min	–	–	SYSCLK
TZWH	Delay to End of 0WS/ from End of Command	30 max	–	–	nS
TRDY	Delay to Start of RDY from Start of Command	30 max	–	–	nS
TRDYM	Delay to Start of RDY from Address & Status Valid	–	30 max	–	nS
TRDYH	Delay from End of RDY to End of Command	1 SYSCLK	60 min	–	nS
TRDB	Delay from Start of Cycle to RDY/ Low (Sync)	–	–	28 max	nS
TRDB	Delay from Start of Cycle to RDY/ Low (Async)	–	–	92 min	nS
TRDBH	Delay from End of Command to RDY/ High	–	–	20 max	nS

Note: PC bus specifications correspond to an 8 MHz bus (SYSCLK period of 125nS) (12 MHz bus SYSCLK period would be 80nS)
MC bus specifications correspond to a 25MHz CPU (PS/2 Model 80)
PI bus specifications correspond to 20 MHz CPU; timing specifications scale with clock frequency for other CPU speeds
0WS/ is synchronous to SYSCLK in some systems and has other timing restrictions than shown above (esp. for 8-bit cycles)
Either 0WS/ or RDY may be asserted, but not both (PC Bus)
0WS/ is used for memory accesses only; it works for I/O writes in some systems but not for I/O reads
At the end of the cycle, RDY and 0WS/ should be driven high before being tri-stated
RDY in the MC bus should be generated based on address, status, and MIO/ only



† Status signals are: MIO/ (MC, PI), S0/ & S1/ (MC), AEN (PC-I/O), BHE/ (MC, PI), RD/ (PI), RFSH/ (PC-Me

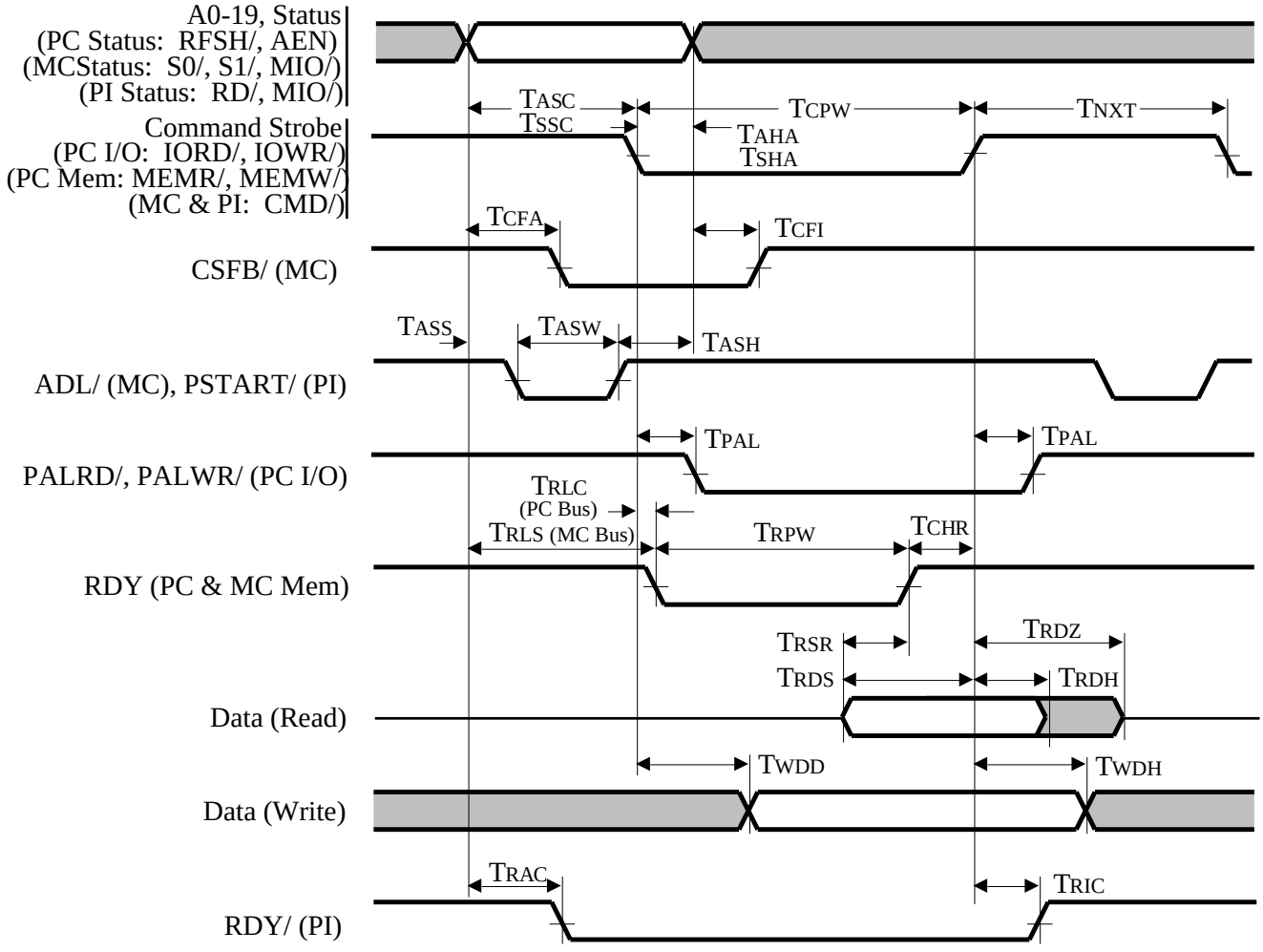
Note: Addresses must be latched on the leading edge of PSTART/ for the PI bus (addresses are not valid on the trailing edge)
Addresses should be latched on the trailing edge of ALE for the PC bus (addresses are not valid on the leading edge)
Addresses should be latched on the leading or trailing edge of ADL/ for the MC bus (addresses are valid on both edges)
Addresses may be latched on the leading edge of CMD/ instead on PC and MC bus (not PI!) if ALE or ADL/ are not used

PC / MC / PI Bus Timing Characteristics for Non-Bus-Master Peripheral Devices

AC TIMING CHARACTERISTICS - BUS TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CPW}	Command Strobe Pulse Width	PC Bus	120	–	–	nS
T_{CPW}	Command Strobe Pulse Width	MC & PI Bus	90	–	–	nS
T_{CHR}	Command Strobe Hold from Ready	Mem Accesses Only	0	–	–	nS
T_{NXT}	Command Strobe Inactive to Next Strobe		80	–	–	nS
T_{ASC}	Address Setup to Command Strobe **(5V)**		30	–	–	nS
T_{ASC}	Address Setup to Command Strobe **(3.3V)**		50	–	–	nS
T_{SSC}	Status Setup to Command Strobe **(5V)**		30	–	–	nS
T_{SSC}	Status Setup to Command Strobe **(3.3V)**		50	–	–	nS
T_{AHA}	Address Hold from Command Strobe		0	–	–	nS
T_{SHA}	Status Hold from Command Strobe		20	–	–	nS
T_{ASS}	Address Setup to Address Strobe	MC & PI Bus Only	10	–	–	nS
T_{ASW}	Address Strobe Width	MC & PI Bus Only	40	–	–	nS
T_{ASH}	Address Hold from Address Strobe	MC & PI Bus Only	10	–	–	nS
T_{RDS}	Read Data Setup to Command Strobe		30	–	–	nS
T_{RSR}	Read Data Setup to Ready	Mem Accesses Only	25	–	–	nS
T_{RDH}	Read Data Hold from Command Strobe		10	–	–	nS
T_{RDZ}	Read Data Tristated from Command Strobe **(5V)**		–	–	40	nS
T_{RDZ}	Read Data Tristated from Command Strobe **(3.3V)**		–	–	66	nS
T_{WDD}	Write Data Delay from Command Strobe		–	–	20	nS
T_{WDH}	Write Data Hold from Command Strobe		10	–	–	nS
T_{RLC}	RDY Low Delay from Command Strobe **(5V)**	PC Bus Mem Only	–	–	40	nS
T_{RLC}	RDY Low Delay from Command Strobe **(3.3V)**	PC Bus Mem Only	–	–	66	nS
T_{RLS}	RDY Low Delay from Status **(5V)**	MC Bus Mem Only	–	–	40	nS
T_{RLS}	RDY Low Delay from Status **(3.3V)**	MC Bus Mem Only	–	–	66	nS
T_{RPW}	RDY Pulse Width	Mem Accesses Only	0	–	128Tm	nS
T_{CFA}	CSFB/ Active from Address/Status Valid **(5V)**	MC Bus Only	–	–	40	nS
T_{CFA}	CSFB/ Active from Address/Status Valid **(3.3V)**	MC Bus Only	–	–	66	nS
T_{CFI}	CSFB/ Inactive from Address/Status Invalid **(5V)**	MC Bus Only	–	–	40	nS
T_{CFI}	CSFB/ Inactive from Address/Status Invalid **(3.3V)**	MC Bus Only	–	–	66	nS
T_{RAC}	RDY/ Active from Command Strobe	PI Bus Only	2Tm	–	–	nS
T_{RIC}	RDY/ Inactive from Command Strobe **(5V)**	PI Bus Only	–	–	40	nS
T_{RIC}	RDY/ Inactive from Command Strobe **(3.3V)**	PI Bus Only	–	–	66	nS

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

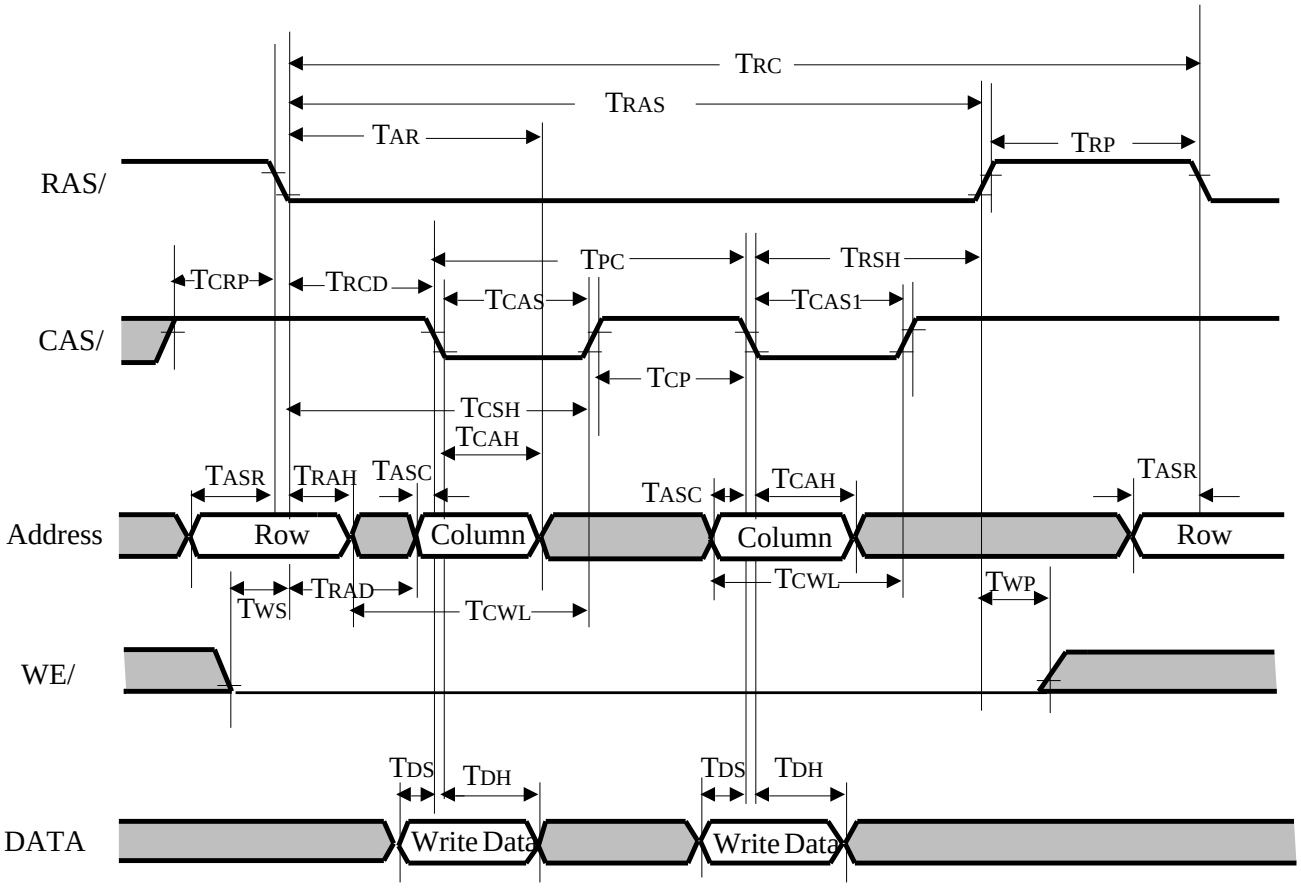


Bus Cycle Timing

AC TIMING CHARACTERISTICS - DRAM TIMING

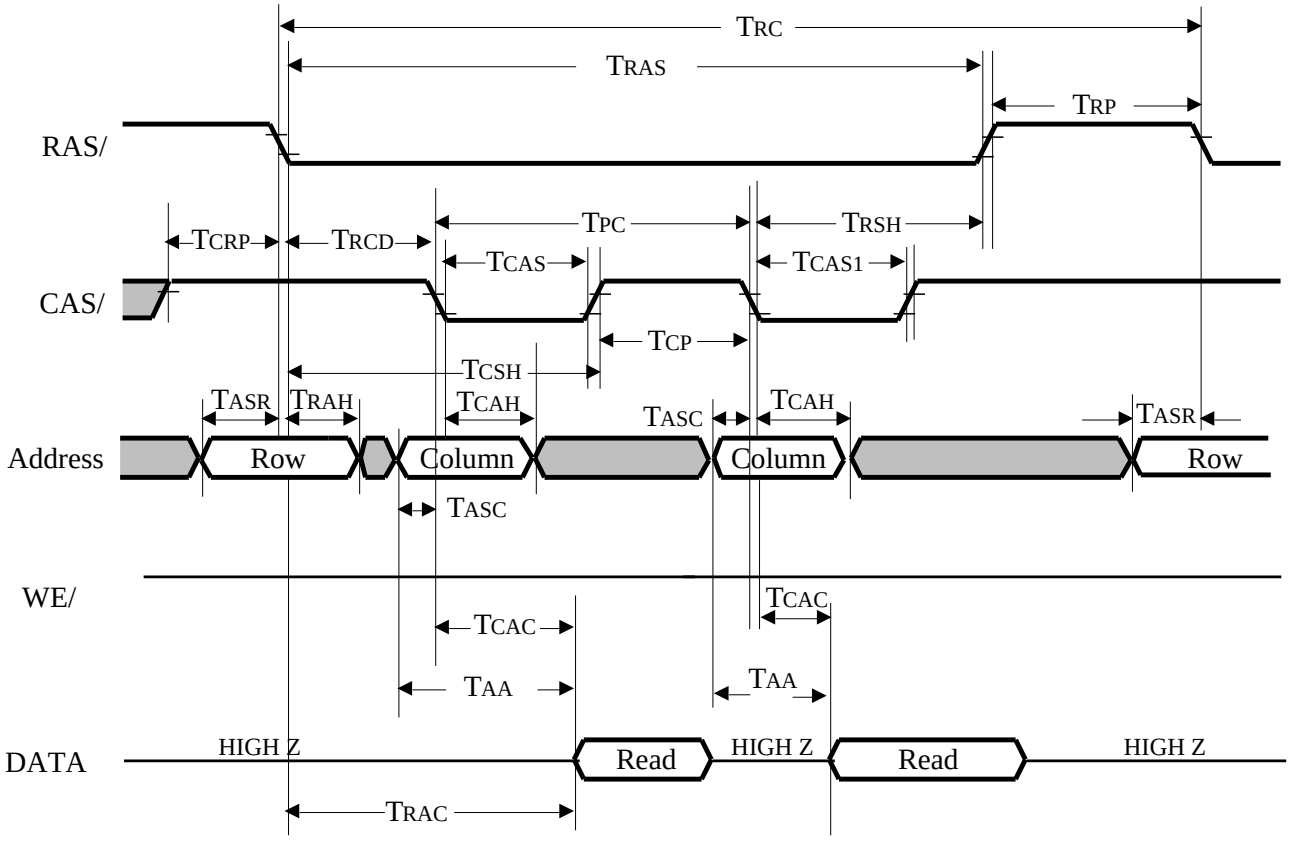
Symbol	Parameter	Min	Max	Units
T_{RC}	Read/Write Cycle Time	12Tm – 5	–	nS
T_{RAS}	RAS/ Pulse Width	8Tm – 5	–	nS
T_{RP}	RAS/ Precharge	4Tm	–	nS
T_{CRP}	CAS/ to RAS/ precharge	4Tm – 5	–	nS
TCSH	CAS/ Hold from RAS/	5Tm	–	nS
T_{RCD}	RAS/ to CAS/ delay	3Tm – 5	–	nS
T_{RSH}	RAS/ Hold from CAS/	2Tm – 5	–	nS
T_{CP}	CAS/ Precharge	Tm – 5	–	nS
T_{CAS}	CAS/ Pulse Width	3Tm – 5	–	nS
T_{CAS1}	CAS/ Pulse Width (Fast Page Cycle)	2Tm – 10	–	nS
T_{ASR}	Row Address Setup to RAS/	2Tm – 10	–	nS
TASC	Column Address Setup to CAS/	Tm – 10	–	nS
T_{RAH}	Row Address Hold from RAS/	Tm	–	nS
T_{CAH}	Column Address Hold from CAS/	Tm + 5	–	nS
T_{CAC}	Data Access Time from CAS/	–	2Tm – 5	nS
T_{RAC}	Data Access time from RAS/		5Tm	nS
T_{DS}	Write Data Setup to CAS/	Tm – 5	–	nS
T_{DH}	Write Data Hold from CAS/	2Tm – 5	–	nS
TPC	CAS Cycle Time	3Tm	–	nS
T_{WS}	WE/ Setup to RAS/	2Tm	–	nS
T_{WP}	WE/ Hold from RAS/	–	–	nS

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.



DRAM Page Mode Write Cycle Timing

Note: The above diagram represents a typical page mode write cycle.
The number of actual CAS cycles may vary between 0 and 4.

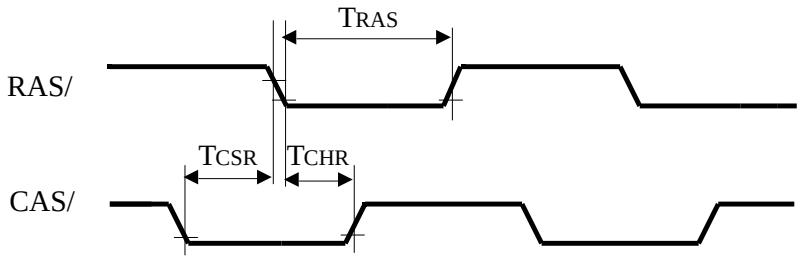


DRAM Page Mode Read Cycle Timing

Note: The above diagram represents a typical page mode read cycle. The number of actual CAS cycles may vary. The maximum number of CAS cycles allowed is 32 (when the FIFO is being filled).

AC TIMING CHARACTERISTICS - REFRESH TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CHR}	RAS to CAS delay	Tm = 17.7 @ 56 MHz	5Tm – 5	–	5Tm + 5	nS
T_{CSR}	CAS to RAS delay	5Tm = 88.3 ns (56 MHz) or 100 ns (50MHz)	Tm – 5	–	Tm + 5	nS
TRAS	RAS pulse width		5Tm – 5	–	5Tm + 5	nS

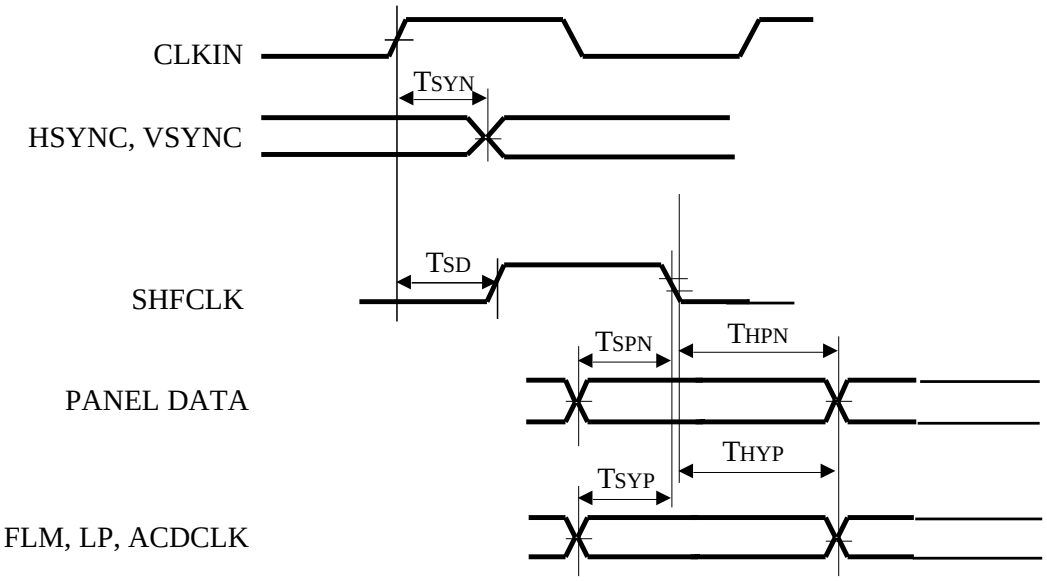


CAS-Before-RAS (CBR) DRAM Refresh Cycle Timing

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

AC TIMING CHARACTERISTICS - PANEL TIMING

Symbol	Parameter		Min	Max	Units
T_{SD}	CLKIN to SHFCLK delay **(5V)**		–	30	nS
T_{SD}	CLKIN to SHFCLK delay **(3.3V)**		–	50	nS
T_{SPN}	Panel data setup to SHFCLK		5	–	nS
T_{HPN}	Panel data hold to SHFCLK		10	–	nS
T_{SYP}	FLM, LP, ACDCLK setup to SHFCLK **(5V)**		5	–	nS
T_{SYP}	FLM, LP, ACDCLK setup to SHFCLK **(3.3V)**		8	–	nS
T_{HYP}	FLM, LP, ACDCLK hold to SHFCLK **(5V)**		10	–	nS
T_{HYP}	FLM, LP, ACDCLK hold to SHFCLK **(3.3V)**		16	–	nS

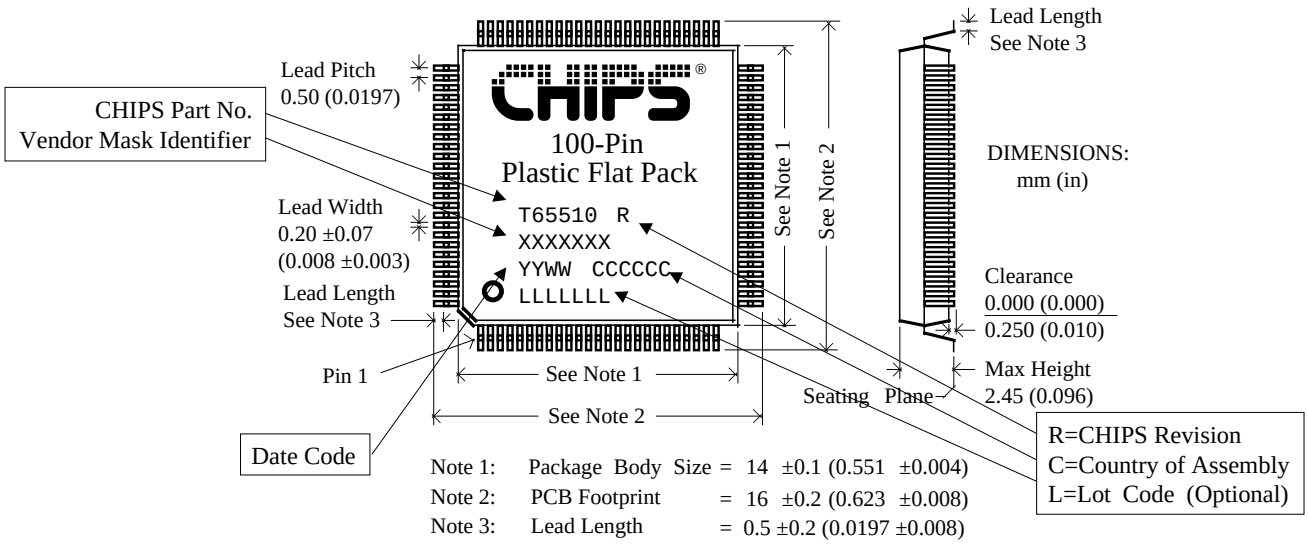


Flat Panel Video Data and Control Signal timing

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

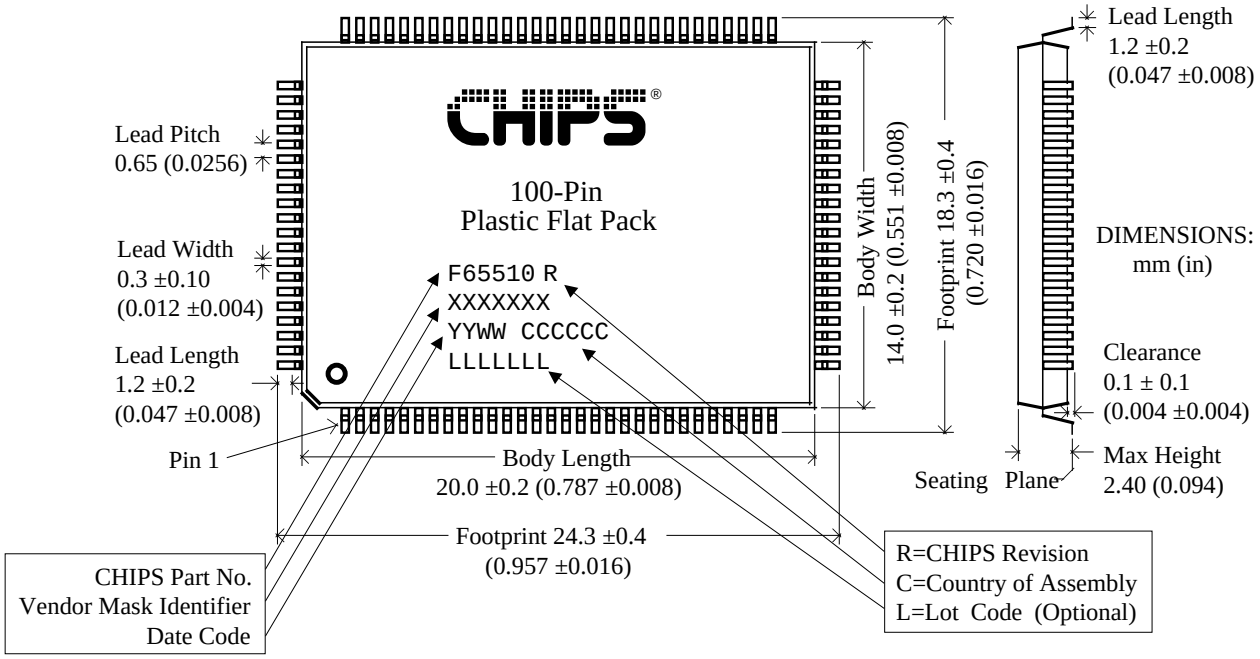
Mechanical Specifications - T65510 (20† mil Lead Pitch)

(Future)



† Actual lead pitch is 0.5mm (approximately 19.7mils) for the 'T' package

Mechanical Specifications - F65510 (25† mil Lead Pitch)



† Actual lead pitch is 0.65mm (approximately 25.6mils) for the 'F' package

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Data Sheet

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