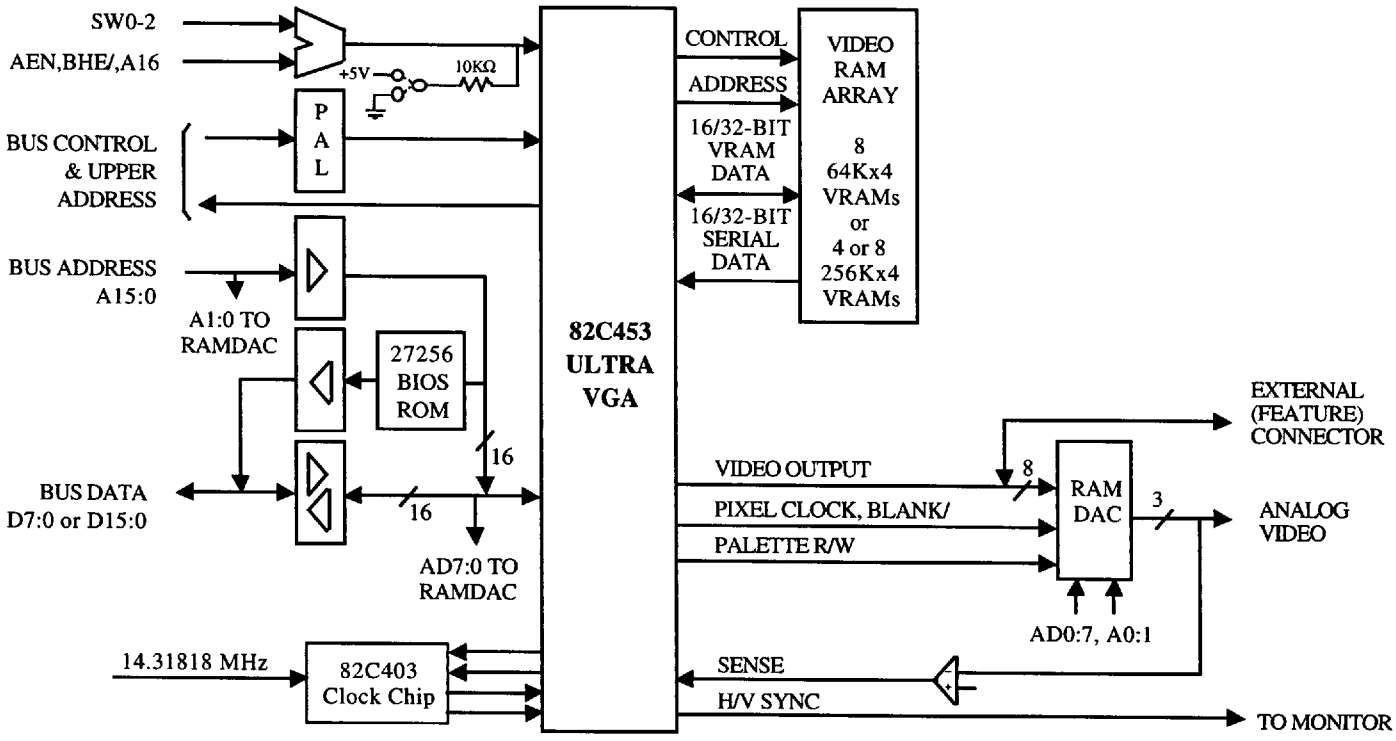
82C453
Ultra VGA
Graphics Controller

- High Performance VRAM VGA optimized for 800x600 and 1024x768, 16 and 256 color, display resolutions (interlaced/non-interlaced)
- 4 VRAMs (256Kx4) support all Super VGA modes up to 1024x768 with 16 colors including 800x600 with 256 colors at 72 Hz
- 8 VRAMs (256Kx4) support 1024x768, 256 colors out of 16 Million interlaced and non-interlaced mode
- Dedicated 32 bit serial port for CRT refresh and 32 bit parallel read/write port for display memory updates; eliminates memory bottleneck inherent with DRAM and multiplexed VRAM based VGAs
- Non-interlaced and interlaced (IBM 8514/8515) monitor support
- Single CPU bus cycle for Read-Modify-Write operation in VGA memory (patent pending)
- Packed Pixel Expansion Mode (patent pending) for rapid 256 color screen updates
- Enhanced support for virtualization (OS/2, UNIX, etc.)
- Full compatibility with IBM VGA at BIOS, register, and gate levels
- Full MDA, Hercules, CGA, and EGA compatibility without NMI
- Dual bus architecture. Integrated interface to EISA/ISA (PC/AT) and Micro Channel bus.
- 8514/A Adapter Interface (AI) compatible; allows use of large installed 8514/A AI applications base without special drivers
- Single 160-pin package saves PCB space
- Pinouts optimized for ease of PCB layout



82C453 System Diagram

Revision History

Revision	Date	By	Comment
0.6	8/90	ST	Initial Release
0.7	9/90	ST	Advance Product Information Initial Release
0.8	5/91	VS/AP	Added ISA Bus Interface (+5V changed to gnd symbol); MC Bus Interface (+5V changed to gnd symbol); AC Timing - ADREN/ changed to Strobe (2 plcs); Updated pinouts to reflect Rev 3 Silicon; Added 16-Bit EISA/ISA (8 & 16 Bit BIOS) to Functional Description; Deleted 2-Bank VRAM Address/Data Connection diagram; Added 4-VRAM Memory Timing diagrams; Updated Application Schematics.
0.9*	6/91	ST	Fixed Pin List; Updated Timing Specifications; Updated clock selection
1.0	7/91	DH	Final Data Sheet Release for Production 82C453 (fixed various typographical errors in rev 0.9)

* Internal Release Only

Table of Contents

List of Figures and Tables

Introduction

The 82C453 is the high-end VGA Controller of the CHIPS 45x product family. It is 100% compatible to IBM™'s VGA standard at the gate, hardware, register, and BIOS level. It also offers enhanced backward compatibility; to EGA™, CGA™, Hercules™ and MDA™ standards without using NMIs.

The 82C453 Ultra VGA offers high resolution and high performance. The 82C453 architecture is optimized to use dual port video RAMS (VRAMs). VRAM serial port is used for CRT refresh and VRAM Random read/write port is used for CPU access. The 82C453 supports up to 1 MByte of display memory and supports resolutions up to 1024x768 256 colors.

EXTENSION REGISTERS

The capabilities of the 82C453 beyond standard VGA are controlled via a set of 'extension' registers. All functionality of these extension registers is disabled on reset. Before the extension registers can be written to, they must be enabled by two sets of control bits (disabled on reset). None of the unused bits in the standard VGA registers are used for extensions.

CPU INTERFACE

The 82C453 supports both EISA/ISA and Micro Channel™ (MC) buses. The chip automatically configures itself for either the EISA/ISA or MC bus based on the status of configuration bit 0 on pin AEN/SW0. This bit is sampled at the end of the RESET cycle. All control signals for both interface types are integrated onto the single VGA chip.

The 82C453 supports both 8-bit and 16-bit CPU interfaces to I/O, display memory, and/or BIOS ROM.

BIOS ROM INTERFACE

In EISA/ISA (PC/AT) Bus systems, the 82C453 can support an 8-bit BIOS with one external BIOS ROM chip. The ROM Chip select (ROMCS) is generated externally for the ROM space (generally 0C0000-C7ffffh).

A 16-bit BIOS ROM can be implemented with the 82C453 using two BIOS ROM chips and external logic for generating ROMCS/ and MEMCS16/.

However, a higher-performance and lower-cost video system will result from implementation of an 8-bit BIOS ROM which is copied into system RAM by the system BIOS on startup.

For motherboard EISA/ISA-bus implementations, the video BIOS may alternately be incorporated directly into the system BIOS. In Micro Channel-based systems, the video BIOS is always included in the system BIOS.

CONFIGURATION SWITCHES

The 82C453 supports up to 3 external DIP switches. These switches are multiplexed on input pins A16/SW0, BHE/SW1 and A16/SW2. The DIP switch state is read into an internal CPU accessible register when the command strobe (IORD/ or CMD/) is low.

MULTIPLE VGAs

It is possible to support up to eight (4 in the Micro Channel bus) 82C453s in one system. Each 82C453 must have a unique number assigned to it through the above mentioned DIP switches. All 82C453s occupy the same memory and I/O address space. However, only one 82C453 responds to CPU accesses at a time. The currently active 82C453 is selected by writing an ID number for that 82C453 into the internal Extended Enable Register for all 82C453s. Only the 82C453 which has the same number on its DIP switches will respond to further CPU accesses.

DISPLAY MEMORY INTERFACE

The 82C453 supports three display memory configurations:

1) Eight 64Kx4 VRAM devices (256KBytes)
2) Eight 256Kx4 VRAM devices (1MByte)
3) Four 256Kx4 VRAM devices (512KBytes)

Implementing an 82C453 Video Subsystem with 256KBytes results in a cost-efficient system which can support all VGA-standard modes. Implementing 512KBytes or 1Mbyte allows support of higher-resolution modes such as 800x600x256-color and 1024x768x256-color modes. With 512KBytes of memory up to 1024x768 16 colors resolution can be supported. The four VRAM configuration is ideal for mother board designs where minimum PCB space is a priority.

CLOCK SELECTION

The 82C453 provides separate inputs for dotclock selections 0, 1, and 2 (called CLK0, CLK1 / CLKSEL0, and CLK2 / CLKSEL1) which are normally selected by Misc Output Register bits 2 and 3. Also, the 82C453 can be programmed to make CLK1 and CLK2 outputs and CLK0 the input clock. CLK1/CLKSEL0 and CLK2/CLKSEL1 can be used as select outputs for an external clock mux to select one of four clocks onto CLK0.

GENERAL PURPOSE OUTPUTS

The 82C453 supports one general purpose output pin in the EISA/ISA bus. No general purpose outputs are supported in the Micro Channel bus. The GPOUT pin can be 3-stated, forced low, or forced high through the Define Pins Register (XR25).

EXTERNAL COLOR PALETTE

The 82C453 supports the programming of an external color palette DAC (RAMDAC™) by decoding the CPU addresses and generating the READ and WRITE signals for the external palette.

Either Inmos™ or Brooktree™-style RAMDACs may be used. The 82C453 decodes 3C6-3C9 port addresses for the RAMDAC (and 83C6-83C9 port address if required).

Normally, each RAMDAC analog output provides 6-bit resolution (64 shades of color on each of the analog R, G, and B outputs). If 8-bit-per-color mode is desired for the DAC (e.g., if using Inmos IMSG178 or Brooktree BT478 RAMDACs which provide 256 shades of color on each RGB output), the DAC 6/8-bit mode pin may be controlled via logic external to the 82C453.

PACKAGE

The 82C453 is available in a 160-pin plastic flat pack (PFP). Complete descriptions of all 82C453 pins are included in this document. The pins are separated into the following logical groups for discussion: Bus Interface, Display memory, Video, Clock, Power, and Ground.

82C453 Pin Usage Summary

Bus Interface:	32
Display Memory:	92
Video:	14
Clock:	4
Power:	5
Ground:	13
Total:	160

VIDEO SUBSYSTEM CHIP COUNT

Using the 82C453, a complete VGA-compatible 16-bit video subsystem for motherboard applications can be built with 13 ICs, including display memory, as shown in the following bill of materials table:

Qty	Chip type
1	82C453 VGA Chip
1	82C403 Clock Chip
1	BT475 or BT477 RAMDAC
2	74LS245 Transceiver
2	74LS244 Buffer
1	74LS125 Buffer
1	PAL16L8
4	256Kx4 VRAMs
13	Total

Additional components required are a 14.31818 MHz crystal, 15-pin video connector, and various resistors and capacitors.

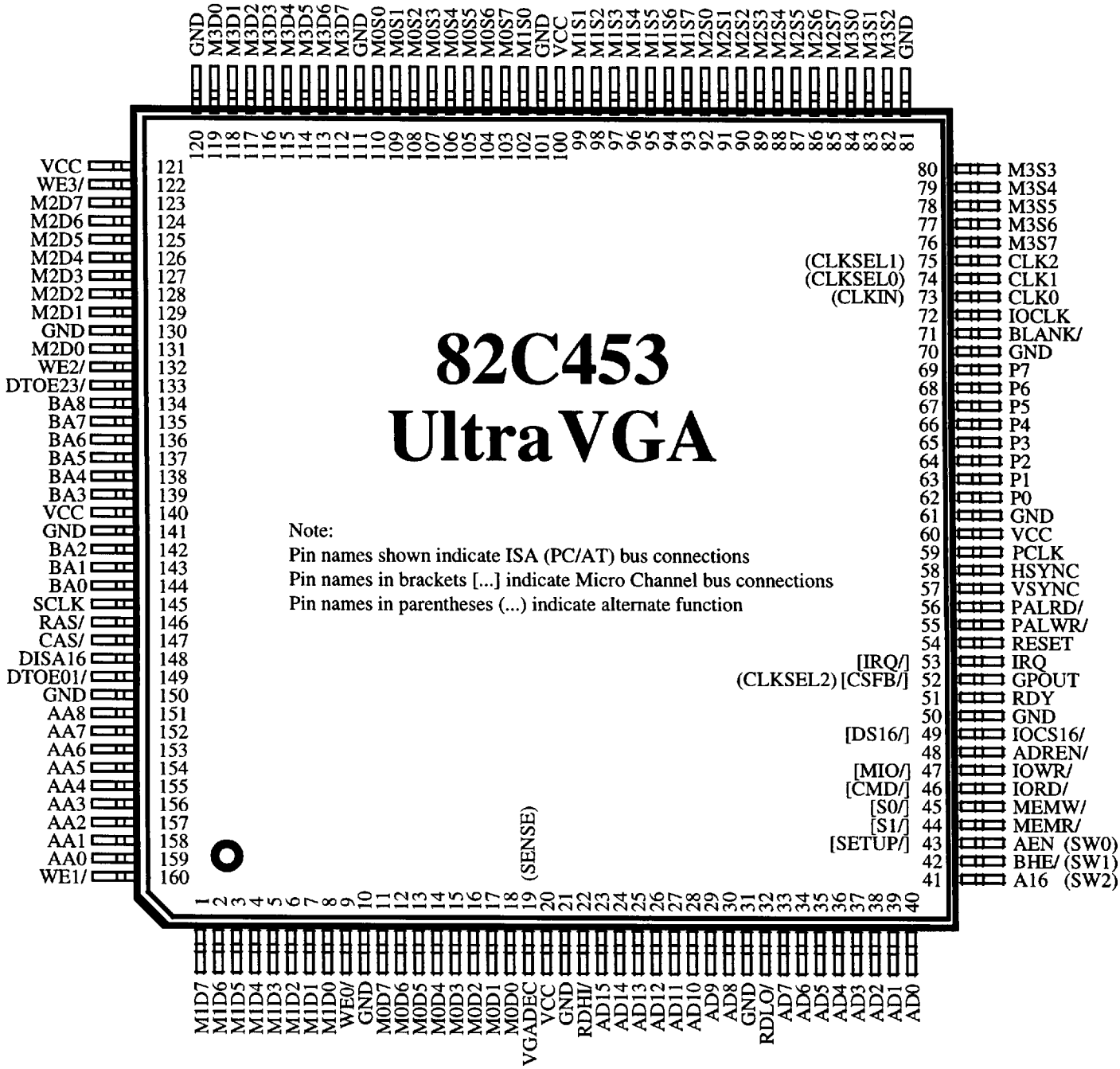
For add-in EISA/ISA-bus boards, one 27256 (32Kx8) BIOS ROM and one additional 74LS244 buffer are required.

The above configuration supports all standard VGA text and graphics modes, plus 640x480 and 800x600 256-color and 1024x768 interlaced and non-interlaced 16-color graphics. For 1024x768 256-color support four additional 256Kx4 VRAMs are required.

Chips and Technologies supplies a video clock synthesizer, the 82C403, which is optimized to interface to the 82C453 for support of all of the resolutions and modes listed above.

If Inmos RAMDACs or Brooktree 471/476 RAMDACs are used, then an additional LM339 comparator, LM334 Current reference, and 1N4148 diode are required (the BT475 and BT477 RAMDACs shown in the bill of materials table above incorporate the comparator and reference functions on-chip). The RAMDAC speed requirements should be compatible with the highest dotclock frequency used.

82C453 Pinouts



82C453 Pin List

Pin Name	Pin #
A16 (SW2)	41
AA0	159
AA1	158
AA2	157
AA3	156
AA4	155
AA5	154
AA6	153
AA7	152
AA8	151
AD0	40
AD1	39
AD2	38
AD3	37
AD4	36
AD5	35
AD6	34
AD7	33
AD8	30
AD9	29
AD10	28
AD11	27
AD12	26
AD13	25
AD14	24
AD15	23
ADREN/	48
AEN (SW0) [SETUP/]	43
BA0	144
BA1	143
BA2	142
BA3	139
BA4	138
BA5	137
BA6	136
BA7	135
BA8	134
BHE/ (SW1)	42
BLANK/	71
CAS/	147
CLK0 (CLKIN)	73
CLK1 (CLKSEL0)	74
CLK2 (CLKSEL1)	75
DISA16	148
DT0E01/	149
DTOE23/	133
GND	10
GND	21
GND	31
GND	50
GND	61
GND	70
GND	81
GND	101

Pin Name	Pin #
GND	111
GND	120
GND	130
GND	141
GND	150
GPOUT (CLKSEL2)	52
GPOUT [CSFB/]	52
HSYNC	58
IOCLK	72
IOCS16/ [DS16/]	49
IORD/ [CMD/]	46
IOWR/ [MIO/]	47
IRQ [IRQ/]	53
M0D0	18
M0D1	17
M0D2	16
M0D3	15
M0D4	14
M0D5	13
M0D6	12
M0D7	11
M0S0	110
M0S1	109
M0S2	108
M0S3	107
M0S4	106
M0S5	105
M0S6	104
M0S7	103
M1D0	8
M1D1	7
M1D2	6
M1D3	5
M1D4	4
M1D5	3
M1D6	2
M1D7	1
M1S0	102
M1S1	99
M1S2	98
M1S3	97
M1S4	96
M1S5	95
M1S6	94
M1S7	93
M2D0	131
M2D1	129
M2D2	128
M2D3	127
M2D4	126
M2D5	125
M2D6	124
M2D7	123
M2S0	92

Pin Name	Pin #
M2S1	91
M2S2	90
M2S3	89
M2S4	88
M2S5	87
M2S6	86
M2S7	85
M3D1	118
M3D2	117
M3D3	116
M3D4	115
M3D5	114
M3D6	113
M3D7	112
M3D0	119
M3S0	84
M3S1	83
M3S2	82
M3S3	80
M3S4	79
M3S5	78
M3S6	77
M3S7	76
MEMR/ [S1/]	44
MEMW/ [S0/]	45
P0	62
P1	63
P2	64
P3	65
P4	66
P5	67
P6	68
P7	69
PALRD/	56
PALWR/	55
PCLK	59
RAS/	146
RDHI/	22
RDLO/	32
RDY	51
RESET	54
SCLK	145
VCC	20
VCC	60
VCC	100
VCC	121
VCC	140
VGADEC (SENSE)	19
VSYNC	57
WE0/	9
WE1/	160
WE2/	132
WE3/	122

82C453 PIN DESCRIPTIONS

System Bus Interface

Pin #	Pin Name	Type	Active	Description
40	AD0	I/O	High	Multiplexed system address/data bus. Address when ADREN/ is low and data when ADREN/ is high. In the MC bus, the address is latched on the leading edge of CMD/.
39	AD1	I/O	High	
38	AD2	I/O	High	
37	AD3	I/O	High	
36	AD4	I/O	High	
35	AD5	I/O	High	
34	AD6	I/O	High	
33	AD7	I/O	High	
30	AD8	I/O	High	
29	AD9	I/O	High	
28	AD10	I/O	High	
27	AD11	I/O	High	
26	AD12	I/O	High	
25	AD13	I/O	High	
24	AD14	I/O	High	
23	AD15	I/O	High	
19	VGADEC (SENSE)	In	High	Multiplexed Memory address enable and SENSE input. When ADREN/ is low, this pin is the high order memory address enable (decoded A17-A23 qualified with the Refresh signal). In MC interface systems, VGADEC should also be qualified with MADE24 (1 indicates only 24 bits of address are being decoded) so that the 82C453 will not respond to any cycle unless MADE24 is high. When ADREN/ is high this pin is the SENSE input from the DAC output comparators (bit 4 of Input Status Register 0).
54	RESET	In	High	Bus Reset input. RESET = 1 resets the 82C453. RESET also puts all internal counters in a known state for chip test.
32	RDLO/	Out	Low	Direction controls for external data tranceivers for the AD bus: 0 = read from 82C453; 1 = write to 82C453. Enable for the AD Bus tranceivers is externally generated by inverting ADREN/.
22	RDHI/	Out	Low	
48	ADREN/	Out	Low	Address Enable. Used to enable address input buffers (typically LS244 or equivalent). Inverse used to enable data transceivers (typically LS245 or equivalent). 0 = Enable bus address onto AD15:0 1 = Enable bus data to/from AD15:0

Note: Pin names in brackets [...] indicate MC bus functionality if different from ISA (PC/AT) bus

82C453 PIN DESCRIPTIONS

System Bus Interface (continued)

Pin #	Pin Name		Type	Active	Description
41	A16	(SW2/CFG2)	In	High	Bus address 16. Also power-on auto-configuration bit-2 sampled on the falling edge of RESET (see VRAM configuration table below) and saved in Configuration Register (extension index 26h) bit-2. This pin may also be read into bit-2 of the Extended DIP-switch Register (ext. index 1) when ADREN/ is high.
42	BHE/	(SW1/CFG1)	In	Low	Byte High Enable for 16-bit interface. Low indicates that the high order byte at the current word address is being accessed. Along with A0, indicates which bytes are transferred over the bus (all byte steering is done internally): **BHE/ A0 Effect** 0 0 Both bytes on D15:0 0 1 High byte on D15:8 1 0 Low byte on D7:0 1 1 High byte on D7:0 (8-bit slot) The 82C453 configures itself to 8-bit or 16-bit bus slots. Also power-on auto-configuration bit-1 sampled on the falling edge of RESET and saved in Configuration Register (extension index 26h) bit-1: **CFG2 CFG1 VRAM Configuration** 0 1 4 1M VRAMs (512KB) 1 0 8 1M VRAMs (1MB) 1 1 8 256K VRAMs (256KB) This pin may also be read into bit-1 of the Extended DIP-switch Register (extension index 1).
43	AEN [SETUP/]	(SW0/CFG0)	In	Hi/Lo	ISA bus: defines valid I/O address: 0 = valid I/O address, 1 = Invalid I/O address (DMA cycle). If single-cycle DMA is used, memory addresses will be on the bus at the same time that IORD/ or IOWR/ is active. The 82C453 will not respond to IORD/ or IOWR/ while AEN=1. MC Bus: 0=Setup mode. The MC interface drives this pin to select the 82C453 during 'SETUP' mode (if low, the POS registers at 100-107h are accessable and all other 82C453 registers are not; if high, POS registers 100-107h are not accessable and all others are if the enable bit in register 102h was set). Also power-on configuration bit-0 sampled on the falling edge of RESET: 0=MC, 1=ISA. This pin may also be read into bit-0 of the Extended DIP-switch Register (extension index 1).

Note: MEMCS16/ must be driven by logic external to the 82C453. If the 82C453 sees BHE/ active, it assumes MEMCS16/ is being driven by external logic.

Note: BHE/ is located on the 16-bit bus extension in ISA systems, so should be connected to a 10K pullup to hold it inactive in case the card is installed in an 8-bit slot.

Note: Pin names in brackets [...] indicate MC bus functionality if different from ISA (PC/AT) bus

82C453 PIN DESCRIPTIONS

System Bus Interface (continued)

Pin #	Pin Name		Type	Active	Description
44	MEMR/	[S1/]	In	Low	In ISA (PC/AT) bus interface indicates a memory or ROM read cycle. In MC bus interface, indicates Status 1 (see table below).
45	MEMW/	[S0/]	In	Low	In ISA (PC/AT) bus, indicates a memory write cycle. In MC bus interface, indicates Status 0 (see table below).
46	IORD/	[CMD/]	In	Low	In ISA (PC/AT) bus interface, indicates an I/O Read cycle. In MC bus interface, indicates a command cycle (valid data on the bus). Driven by CMD/ from MC, VGACMD/ from CHIPS/250.
47	IOWR/	[MIO/]	In	Low	In ISA (PC/AT) bus interface, indicates an I/O Write cycle. In MC bus interface, indicates memory or I/O cycle: 1 = memory cycle, 0 = I/O cycle.
148	DISA16		Out	High	DISA16: The state of the pin is active high ('1') during text mode in 4-VRAM mode and when fonts are loaded in memory during 8-VRAM text mode. At other times, this pin is active low ('0'). This signal should be used externally to qualify MEMCS16/ to the ISA(PC/AT) bus. MEMCS16/ should be disabled when DISA16 is high ('1').

MIO/	S1/	S0/	Cycle Type
0	0	0	-reserved-
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	-reserved-
1	0	0	-reserved-
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	-reserved-

Note: Pin names in brackets [...] indicate MC bus functionality if different from ISA (PC/AT) bus

82C453 PIN DESCRIPTIONS

System Bus Interface (continued)

Pin #	Pin Name		Type	Active	Description
51	RDY		Tri-Out	High	Ready. Driven low to indicate the current cycle should be extended with wait states. Driven high at end of cycle to indicate 'ready' then tristated. This signal is normally high and is only driven low if the 82C453 cannot respond immediately to memory requests to insert the neccessary wait states.
49	IOCS16/	[DS16/]	Tri-Out	Low	In ISA bus interface, indicates 16-bit I/O cycle. In MC, indicates 16-bit Memory or I/O cycle. Asserted by the 82C453 to indicate that the chip is capable of transferring 16 bits over the bus at the requested address. In MC, DS16/ is active for all accesses except those to the RAMDAC.
53	IRQ	[IRQ/]	Tri-Out	Both	Vertical blank interrupt. In ISA bus, this pin is tristated when interrupts are not enabled, low when interrupts are enabled but no interrupt is pending, and high when interrupts are enabled and an interrupt is pending. In the MC bus, this pin functions as an active-low open-collector output. This pin is normally connected to IRQ9. IRQ9/ may be shared by multiple controllers on the MC bus; in the ISA bus, only one controller at a time may have IRQ9 enabled. This pin has high drive capability (IOL=12mA). While this is still not enough to meet the MC bus specification of 24mA, the board designer may still want to connect IRQ/ directly to the bus, eliminating the need for a 74LS125 driver.
52	GPOUT	[CSFB/] (CLKSEL2)	Tri-Out	Low	In the ISA bus, this pin is a general purpose output pin. The state of this pin can be controlled by bits 0 and 1 of the Define Pins Register (XR25). It is used as an additional clock select signal by the Chips BIOS. In the MC bus, this pin is called 'Card Select Feedback'; it indicates any valid access to the 82C453. It is an unlatched decode of A0:16, VGADEC, and MIO/. This pin has insufficient drive to connect to the MC bus directly (24 mA required) so is used as an enable for an external bus driver (74LS125 or equivalent).

Note: Pin names in brackets [...] indicate MC bus functionality if different from ISA (PC/AT) bus

82C453 PIN DESCRIPTIONS

Display Memory Interface

Pin #	Pin Name	Type	Active	Description
112	M3D7	I/O	High	VRAM Data Bus.
113	M3D6	I/O	High	
114	M3D5	I/O	High	The first digit in the signal name indicates the plane. The second indicates the bit position within the plane.
115	M3D4	I/O	High	
116	M3D3	I/O	High	In the 4-VRAM configuration, planes 1 and 3 (M1Dx and M3Dx) are left unconnected (see configuration bits 0-2).
117	M3D2	I/O	High	
118	M3D1	I/O	High	
119	M3D0	I/O	High	
123	M2D7	I/O	High	
124	M2D6	I/O	High	
125	M2D5	I/O	High	
126	M2D4	I/O	High	
127	M2D3	I/O	High	
128	M2D2	I/O	High	
129	M2D1	I/O	High	
131	M2D0	I/O	High	
1	M1D7	I/O	High	
2	M1D6	I/O	High	
3	M1D5	I/O	High	
4	M1D4	I/O	High	
5	M1D3	I/O	High	
6	M1D2	I/O	High	
7	M1D1	I/O	High	
8	M1D0	I/O	High	
11	M0D7	I/O	High	
12	M0D6	I/O	High	
13	M0D5	I/O	High	
14	M0D4	I/O	High	
15	M0D3	I/O	High	
16	M0D2	I/O	High	
17	M0D1	I/O	High	
18	M0D0	I/O	High	

82C453 PIN DESCRIPTIONS

Display Memory Interface (continued)

Pin #	Pin Name	Type	Active	Description
76	M3S7	In	High	VRAM Serial Data Bus. The first digit in the signal name indicates the plane. The second indicates the bit position within the plane. In the 4-VRAM configuration, planes 1 and 3 (M1Sx and M3Sx) are left unconnected (see configuration bits 0-2). Note that four 1Mb VRAMs provide 512KB of display memory and that 1024x768, 256-color mode requires 1MB total so that mode won't work in the 4-VRAM configuration.
77	M3S6	In	High	
78	M3S5	In	High	
79	M3S4	In	High	
80	M3S3	In	High	
82	M3S2	In	High	
83	M3S1	In	High	
84	M3S0	In	High	
85	M2S7	In	High	
86	M2S6	In	High	
87	M2S5	In	High	
88	M2S4	In	High	
89	M2S3	In	High	
90	M2S2	In	High	
91	M2S1	In	High	
92	M2S0	In	High	
93	M1S7	In	High	
94	M1S6	In	High	
95	M1S5	In	High	
96	M1S4	In	High	
97	M1S3	In	High	
98	M1S2	In	High	
99	M1S1	In	High	
102	M1S0	In	High	
103	M0S7	In	High	
104	M0S6	In	High	
105	M0S5	In	High	
106	M0S4	In	High	
107	M0S3	In	High	
108	M0S2	In	High	
109	M0S1	In	High	
110	M0S0	In	High	

82C453 PIN DESCRIPTIONS

Display Memory Interface (continued)

Pin #	Pin Name	Type	Active	Description
151	AA8	Tri-Out	High	VRAM Address bus A for connection to planes 0 and 1. With 64Kx4 VRAMs, AA8 is not required, so the pin is left unconnected.
152	AA7	Tri-Out	High	
153	AA6	Tri-Out	High	
154	AA5	Tri-Out	High	
155	AA4	Tri-Out	High	
156	AA3	Tri-Out	High	
157	AA2	Tri-Out	High	
158	AA1	Tri-Out	High	
159	AA0	Tri-Out	High	
134	BA8	Tri-Out	High	VRAM Address bus B for connection to planes 2 and 3. With 64Kx4 VRAMs, BA8 is not required, so the pin is left unconnected.
135	BA7	Tri-Out	High	
136	BA6	Tri-Out	High	
137	BA5	Tri-Out	High	
138	BA4	Tri-Out	High	
139	BA3	Tri-Out	High	
142	BA2	Tri-Out	High	
143	BA1	Tri-Out	High	
144	BA0	Tri-Out	High	
146	RAS/	Tri-Out	Low	VRAM Row Address Strobe for all planes and banks. A 50K internal pull-up keeps the VRAMs in a quiescent state during reset, or while exchanging control with another chip.
147	CAS/	Tri-Out	Low	VRAM Column Address Strobe for all planes.
122	WE3/	Tri-Out	Low	VRAM Write Enables for planes 3:0. WE1/ and WE3/ are not connected in the 4-VRAM configuration (see configuration bits 1-2).
132	WE2/	Tri-Out	Low	
160	WE1/	Tri-Out	Low	
9	WE0/	Tri-Out	Low	
149	DTOE01/	Tri-Out	Low	Data Transfer / Output Enables for VRAMs in planes 0-1 and 2-3, respectively.
133	DTOE23/	Tri-Out	Low	
145	SCLK	Tri-Out	High	VRAM Serial Clock for all VRAMs.

Note: The VRAM SOE/ input is normally grounded. The VRAM DSF pin, if present, is also grounded.

82C453 PIN DESCRIPTIONS

Video Interface

Pin #	Pin Name		Type	Active	Description
62	P0		Out	High	Video Pixel Data Out
63	P1		Out	High	
64	P2		Out	High	
65	P3		Out	High	
66	P4		Out	High	
67	P5		Out	High	
68	P6		Out	High	
69	P7		Out	High	
59	PCLK		Out	High	Video Pixel Clock Out
56	PALRD/		Out	Low	Connected to the Read input of the Palette DAC (IMSG176, BT471, or compatible). Asserted when the 82C453 is enabled and an I/O Read occurs from addresses 3C6h, 3C8h, 3C9h or (if enabled) 83C6h-83C9h. (The 82C453 responds directly for accesses to 3C7h).
55	PALWR/		Out	Low	Connected to the Write input of the Palette DAC (IMSG176, BT471, or compatible). Asserted when the 82C453 is enabled and an I/O Write occurs to addresses 3C6-3C9h or (if enabled) 83C6h-83C9h.
58	HSYNC		Out	Both	Horizontal and Vertical Sync signals for the monitor and Blanking signal for the external palette DAC. Sync polarities are programmable. The BLANK/ pin may be configured to output Display Enable (DE).
57	VSYNC		Out	Both	
71	BLANK/	(DE)	Out	Low	
72	IOCLK		In	High	I/O Clock. This clock is used for internal sequencing of I/O Registers. This clock can also be selected as display clock. IOCLK should be between 30-40 Mhz.
73	CLK0	(CLKIN)	In	High	CLK0-2 are three clock inputs to the chip.
74	CLK1	(CLKSEL0)	I/O	High	
75	CLK2	(CLKSEL1)	I/O	High	Alternately, CLK1 and CLK2 may be programmed (via bit 0 of XR05) as clock select outputs to externally select one of eight frequencies (CLKSEL2 is the inverse of FCOUT register bit 0):
52	GPOUT	(CLKSEL2) [CSFB/]	Out	High	

CLKSEL 2 1 0	82C403A Frequency Selected	Resolution
0 0 0	25.175 MHz	640x400 (8-dot text) & 640x480
0 0 1	28.322 MHz	720x400 (9-dot text)
0 1 0	36.000 MHz	800x600 (60Hz NI)
0 1 1	44.900 MHz	1024x768 (60Hz NI)
1 0 0	50.350 MHz	800x600 (72Hz NI)
1 0 1	75.000 MHz	1024x768 (72Hz NI)
1 1 0	40.000 MHz	132-column text
1 1 1	65.000 MHz	1024x768 (non-interlaced)

Note: The VRAM SOE/ input is normally grounded. The VRAM DSF pin, if present, is also grounded.

82C453 PIN DESCRIPTIONS

Power and Ground

Pin #	Pin Name	Type	Active	Description
20	VCC	P	-	Power Pins
60	VCC	P	-	
100	VCC	P	-	
121	VCC	P	-	
140	VCC	P	-	
10	GND	P	-	Ground Pins
21	GND	P	-	
31	GND	P	-	
50	GND	P	-	
61	GND	P	-	
70	GND	P	-	
81	GND	P	-	
101	GND	P	-	
111	GND	P	-	
120	GND	P	-	
130	GND	P	-	
141	GND	P	-	
150	GND	P	-	

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82C453 REGISTER SUMMARY - CGA, MDA, AND HERCULES MODES

Register	Register Name	Bits	Access	I/O Port - MGA	I/O Port - CGA	Comment
STAT	Display Status	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W	3BB (ignored)	3DB (ignored)	no light pen
SLPEN	Set Light Pen Flip Flop	0	W	3B9 (ignored)	3DC (ignored)	no light pen
MODE	CGA/MDA/Hercules Mode Control	7	RW	3B8	3D8	
COLOR	CGA Color Select	6	RW	n/a	3D9	
CONFIG	Hercules Configuration	2	W	3BF	n/a	
			R	3B6-3B7 index 14	n/a	XR14
RX, R0-11	'6845' Registers	0-8	RW	3B4-3B5	3D4-3D5	
XRX, XR0-7F	Extension Registers	0-8	RW	3B6-3B7	3D6-3D7	if port 103 bit-7=1

82C453 REGISTER SUMMARY - EGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
MISC	Miscellaneous Output	7	W	3C2	3C2	
FC	Feature Control	3	W	3BA	3DA	
FEAT	Feature Read (Input Status 0)	4	R	3C2	3C2	
STAT	Display Status (Input Status 1)	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W	3BB (ignored)	3DB (ignored)	no light pen
SLPEN	Set Light Pen Flip Flop	0	W	3BC (ignored)	3DC (ignored)	no light pen
SRX, SR0-4	Sequencer	0-8	RW	3C4-3C5	3C4-3C5	
CRX, CR0-18	CRT Controller	0-8	RW	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	RW	3CE-3CF	3CE-3CF	
ARX, AR0-13	Attributes Controller	0-8	RW	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	RW	3B6-3B7	3D6-3D7	if port 103 bit-7=1

82C453 REGISTER SUMMARY - VGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Reg Type	Comment
POSIDL	POS ID LSB	8	R	100 (Setup Only)	100 (Setup Only)	VGA	
POSIDH	POS ID MSB	8	R	101 (Setup Only)	101 (Setup Only)	VGA	
SLEEP	Video Subsystem Sleep Control	1	RW	102 (Setup Only)	102 (Setup Only)	VGA	
XENA	Extended Enable	7	RW	103 (Setup Only)	103 (Setup Only)	VGA	
GLOBID	Global ID (0A5h)	8	R	104 (Setup Only)	104 (Setup Only)	VGA	
MISC	Miscellaneous Output	7	W	3C2	3C2	VGA	
			R	3CC	3CC	VGA	
FC	Feature Control	3	W	3BA	3DA	VGA	
			R	3CA	3CA	VGA	
FEAT	Feature Read (Input Status 0)	4	R	3C2	3C2	VGA	
STAT	Display Status (Input Status 1)	6	R	3BA	3DA	VGA	
CLPEN	Clear Light Pen Flip Flop	0	W	3BB (ignored)	3DB (ignored)	n/a	no lpen
SLPEN	Set Light Pen Flip Flop	0	W	3BC (ignored)	3DC (ignored)	n/a	no lpen
VSE	Video Subsystem Enable	1	RW	3C3 if MC	3C3 if MC	Motherboard	
46E8	Setup / Disable Control	2	W	46E8 if ISA	46E8 if ISA	VGA	
DACMASK	Color Palette Pixel Mask	8	RW	3C6, 83C6	3C6, 83C6	DAC	
DACSTATE	Color Palette State	2	R	3C7, 83C7	3C7, 83C7	VGA	
DACRX	Color Palette Read-Mode Index	8	W	3C7, 83C7	3C7, 83C7	DAC	
DACWX	Color Palette Write-Mode Index	8	RW	3C8, 83C8	3C8, 83C8	DAC	
DACDATA	Color Palette Registers 0-FF	3x6 or 3x8	RW	3C9, 83C9	3C9, 83C9	DAC	
SRX, SR0-7	Sequencer	0-8	RW	3C4-3C5	3C4-3C5	VGA	
CRX, CR0-3F	CRT Controller	0-8	RW	3B4-3B5	3D4-3D5	VGA	
GRX, GR0-8	Graphics Controller	0-8	RW	3CE-3CF	3CE-3CF	VGA	
ARX, AR0-14	Attributes Controller	0-8	RW	3C0-3C1	3C0-3C1	VGA	
XRX, XR0-7F	Extension Registers	0-8	RW	3B6-3B7	3D6-3D7	VGA	103 bit7=1

82C453 REGISTER SUMMARY - INDEXED REGISTERS (EGA / VGA)

Register	Register Name	Bits	Register Type	Access (VGA)	Access (EGA)	I/O Port
SRX	Sequencer Index	3	VGA/EGA	RW	RW	3C4
SR0	Reset	2	VGA/EGA	RW	RW	3C5
SR1	Clocking Mode	6	VGA/EGA	RW	RW	3C5
SR2	Plane Mask	4	VGA/EGA	RW	RW	3C5
SR3	Character Map Select	6	VGA/EGA	RW	RW	3C5
SR4	Memory Mode	3	VGA/EGA	RW	RW	3C5
SR7	Reset Horizontal Character Counter	0	VGA	W	n/a	3C5
CRX	CRTC Index	6	VGA/EGA	RW	RW	3B4 Mono, 3D4 Color
CR0	Horizontal Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR1	Horizontal Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR2	Horizontal Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR3	Horizontal Blanking End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR4	Horizontal Retrace Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR5	Horizontal Retrace End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR6	Vertical Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR7	Overflow	5	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR8	Preset Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR9	Character Cell Height	5+3	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRA	Cursor Start	5+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRB	Cursor End	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRC	Start Address High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRD	Start Address Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRE	Cursor Location High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRF	Cursor Location Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
LPENH	Light Pen High	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
LPENL	Light Pen Low	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
CR10	Vertical Retrace Start	8	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR11	Vertical Retrace End	4+4	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR12	Vertical Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR13	Offset	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR14	Underline Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR15	Vertical Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR16	Vertical Blanking End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR17	CRT Mode Control	7	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR18	Line Compare	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR22	Graphics Controller Data Latches	8	VGA	R	n/a	3B5 Mono, 3D5 Color
CR24	Attribute Controller Index/Data Latch	1	VGA	R	n/a	3B5 Mono, 3D5 Color
CR3x	Clear Vertical Display Enable FF	0	VGA	W	n/a	3B5 Mono, 3D5 Color
GRX	Graphics Controller Index	4	VGA/EGA	RW	RW	3CE
GR0	Set/Reset	4	VGA/EGA	RW	RW	3CF
GR1	Enable Set/Reset	4	VGA/EGA	RW	RW	3CF
GR2	Color Compare	4	VGA/EGA	RW	RW	3CF
GR3	Data Rotate	5	VGA/EGA	RW	RW	3CF
GR4	Read Map Select	2	VGA/EGA	RW	RW	3CF
GR5	Mode	6	VGA/EGA	RW	RW	3CF
GR6	Miscellaneous	4	VGA/EGA	RW	RW	3CF
GR7	Color Don't Care	4	VGA/EGA	RW	RW	3CF
GR8	Bit Mask	8	VGA/EGA	RW	RW	3CF
ARX	Attribute Controller Index	6	VGA/EGA	RW	RW	3C0 (3C1)
AR0-F	Internal Palette Regs 0-15	6	VGA/EGA	RW	RW	3C0 (3C1)
AR10	Mode Control	7	VGA/EGA	RW	RW	3C0 (3C1)
AR11	Overscan Color	6	VGA/EGA	RW	RW	3C0 (3C1)
AR12	Color Plane Enable	6	VGA/EGA	RW	RW	3C0 (3C1)
AR13	Horizontal Pixel Panning	4	VGA/EGA	RW	RW	3C0 (3C1)
AR14	Color Select	4	VGA	RW	n/a	3C0 (3C1)

82C453 EXTENSION REGISTER SUMMARY: 00-2F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family 450	451	452	453	455	456	457
XRX	**Extension Index Register**	7	R/W	3B6/3D6	-xxxxxxx	✓	✓	✓	✓	✓	✓	✓
XR00	**Chip Version**	8	R/O	3B7/3D7	0011rrrr	✓	✓	✓	✓	✓	✓	✓
XR01	**DIP Switch**	3	R/O	3B7/3D7	-----ddd	✓	✓	✓	✓	✓	✓	✓
XR02	**CPU Interface**	8	R/W	3B7/3D7	00000000	✓	✓	✓	✓	✓	✓	✓
XR03	**Interface I**	5	R/W	3B7/3D7	00--00-0	.	✓	✓	✓	.	.	✓
XR04	*(Memory Control)*	--	--	3B7/3D7		✓	✓	✓	.	✓	✓	✓
XR05	**Sequencer Control**	5	R/W	3B7/3D7	0000---0	.	.	✓	✓	.	.	✓
XR06	*(DRAM Interface)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR07	-reserved-	--	--	3B7/3D7								
XR08	*(General Purpose Output Select B)*	--	--	3B7/3D7		.	✓	✓	.	✓	✓	✓
XR09	*(General Purpose Output Select A)*	--	--	3B7/3D7		.	✓	✓	.	✓	✓	✓
XR0A	*(Cursor Address Top)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR0B	**CPU Paging**	3	R/W	3B7/3D7	-----000	✓	.	✓	✓	✓	✓	✓
XR0C	**Start Address Top**	2	R/W	3B7/3D7	------00	✓	.	✓	✓	.	.	.
XR0D	**Auxiliary Offset**	2	R/W	3B7/3D7	------00	✓	✓	✓	✓	✓	✓	✓
XR0E	*(Text Mode)*	--	--	3B7/3D7		✓	.	✓	.	.	.	.
XR0F	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR10	**Single/Low Map Register**	8	R/W	3B7/3D7	xxxxxxxx	✓	.	✓	✓	.	.	.
XR11	**High Map Register**	8	R/W	3B7/3D7	xxxxxxxx	✓	.	✓	✓	.	.	.
XR12	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR13	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR14	**Emulation Mode**	8	R/W	3B7/3D7	0000hh00	✓	✓	✓	✓	✓	✓	✓
XR15	**Write Protect**	7	R/W	3B7/3D7	-0000000	✓	✓	✓	✓	✓	✓	✓
XR16	**Trap Enable**	6	R/W	3B7/3D7	--000000	.	✓	✓	✓	✓	✓	✓
XR17	**Trap Status**	6	R/W	3B7/3D7	--000000	.	✓	✓	✓	✓	✓	✓
XR18	**Alternate H Display End**	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	✓	✓	✓	✓
XR19	**Alt H Retrace Start / Halfline Comp**	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	✓	✓	✓	✓
XR1A	**Alternate H Retrace End**	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	✓	✓	✓	✓
XR1B	**Alternate H Total**	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	✓	✓	✓	✓
XR1C	**Alternate H Blank Start**	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	✓	✓	✓	✓
XR1D	**Alternate H Blank End**	8	R/W	3B7/3D7	0xxxxxxx	✓	✓	✓	✓	✓	✓	✓
XR1E	**Alternate Offset**	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	✓	✓	✓	✓
XR1F	*(Virtual EGA Switch Register)*	--	--	3B7/3D7		✓	.	.	.	.	.	.
XR20	*(Sliding Unit Delay)* / **Interface II**	2	R/W	3B7/3D7	----0-0-	.	.	✓	✓	.	.	.
XR21	*(Sliding Hold A)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR22	*(Sliding Hold B)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR23	*(Sliding Hold C)* / ***Wr Bit Mask Ctrl***	4	R/W	3B7/3D7	----0xx0	.	.	✓	✓	.	.	.
XR24	*(Sliding Hold D)* / ***Wr Bit Mask Pattern***	8	R/W	3B7/3D7	xxxxxxxx		.	✓	✓	.	.	.
XR25	**Pin Definition**	3	R/W	3B7/3D7	-----0x0	.	.	.	✓	.	.	.
XR26	**Configuration**	3	R/W	3B7/3D7	-----000	.	.	.	✓	.	.	.
XR27	*(Force Sync State)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR28	**Video Interface**	5	R/W	3B7/3D7	-----000	✓	✓	✓	✓	✓	✓	✓
XR29	*(Function Ctrl)* / **453 Halfline Compar**	8	R/W	3B7/3D7	xxxxxxxx	.	.	✓	✓	.	.	.
XR2A	*(Frame Interrupt Count)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR2B	*(Default Video)*	--	--	3B7/3D7		✓	✓	✓	.	✓	✓	✓
XR2C	*(Delay Horizontal High)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR2D	*(Delay Horizontal Low)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR2E	*(Delay Vertical High)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR2F	*(Delay Vertical Low)*	--	--	3B7/3D7		.	.	✓	.	.	.	.

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
– = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 450–453 VGAs drive CRTs only, 455–458 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

82C453 EXTENSION REGISTER SUMMARY: 30-5F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family 450	451	452	453	455	456	457
XR30	*(Graphics Cursor Start Address High)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR31	*(Graphics Cursor Start Address Low)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR32	*(Graphics Cursor End Address)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR33	*(Graphics Cursor X Position High)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR34	*(Graphics Cursor X Position Low)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR35	*(Graphics Cursor Y Position High)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR36	*(Graphics Cursor Y Position Low)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR37	*(Graphics Cursor Mode)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR38	*(Graphics Cursor Mask)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR39	*(Graphics Cursor Color 0)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR3A	*(Graphics Cursor Color 1)*	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR3B	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR3C	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR3D	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR3E	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR3F	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR40	*(I/O Flag)*	--	--	3B7/3D7		.	.	.	.	.	.	.
XR41	**EGA Switch Register**	5	RW	3B7/3D7	0---0000	.	.	.	✓	.	.	.
XR42	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR43	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR44	**Video Flag Register**	8	RW	3B7/3D7	00000000	.	.	.	✓	.	.	.
XR45	**Scratch Register 1 / FG Color**	8	RW	3B7/3D7	00000000	.	.	.	✓	.	.	.
XR46	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR47	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR48	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR49	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR4A	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR4B	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR4C	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR4D	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR4E	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR4F	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR50	*(Panel Format)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR51	*(Display Type)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR52	*(Panel Size)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR53	*(Override)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR54	*(Alternate Misc Output)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR55	*(Text Mode 350_A Compensation)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR56	*(Text Mode 350_B Compensation)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR57	*(Text Mode 400 Compensation)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR58	*(Graphics Mode 350 Compensation)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR59	*(Graphics Mode 400 Compensation)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR5A	*(Flat Panel Vertical Display Start 40(*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR5B	*(Flat Panel Vertical Display End 400)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR5C	*(Weight Control Clock A)*	--	--	3B7/3D7		.	.	.	.	✓	✓	.
XR5D	*(Weight Control Clock B)*	--	--	3B7/3D7		.	.	.	.	✓	✓	.
XR5E	*(ACDCLK Control)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR5F	*(Power Down Mode Refresh)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
– = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 450–453 VGAs drive CRTs only, 455–458 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

82C453 EXTENSION REGISTER SUMMARY: 60-7F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family 450	451	452	453	455	456	457
XR60	*(Blink Rate Control)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR61	*(Text Color Mapping Control)*	--	--	3B7/3D7		.	.	.	.	✓	✓	.
XR62	*(Text Color Shift Parameter)*	--	--	3B7/3D7		.	.	.	.	✓	✓	.
XR63	*(Graphics Color Mapping Control)*	--	--	3B7/3D7		.	.	.	.	✓	✓	.
XR64	*(Alternate Vertical Total)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR65	*(Alternate Overflow)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR66	*(Alternate Vertical Sync Start)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR67	*(Alternate Vertical Sync End)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR68	*(Alternate Vertical Display Enable En*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR69	*(Flat Panel Vertical Display Start 350)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR6A	*(Flat Panel Vertical Display End 350)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR6B	*(Flat Panel Vertical Overflow 2)*	--	--	3B7/3D7		.	.	.	.	✓	✓	✓
XR6C	*(Weight Control Clock C)*	--	--	3B7/3D7		.	.	.	.	✓	✓	.
XR6D	*(External Palette Control)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓
XR6E	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	✓
XR6F	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR70	*(46E8/3C3 Disable)*	--	--	3B7/3D7		.	.	.	.	.	.	.
XR71	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR72	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR73	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR74	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR75	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR76	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR77	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR78	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR79	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR7A	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR7B	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR7C	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR7D	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR7E	**CGA/Hercules Color Select**	6	R/O	3B7/3D7	--xxxxxx	✓	✓	✓	✓	✓	✓	✓
XR7F	**Diagnostic**	2	RW	3B7/3D7	------00	✓	✓	✓	✓	✓	✓	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
– = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 450–453 VGAs drive CRTs only, 455–458 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

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82C453 Registers

GLOBAL CONTROL (SETUP) REGISTERS

The Setup Control Register is used to enable or disable the VGA. It is also used to place the VGA in normal or setup mode. This register is used only in the PC-bus interface. In the MC Bus interface these functions are performed by the DISA/ and SETUP/ pins respectively.

The Global and Extension Enable Registers are accessible only during Setup mode. The Global ID Register contains the ID number that identifies the 82C453 as a Chips & Technologies product.

Note: In setup mode in the IBM VGA, the Global Setup Register (defined as port address 102) actually occupies the *entire I/O space*. Only the lower 3 bits are used to decode and select this register. To avoid bus conflicts with other peripherals, reads should only be performed at the 10xh port addresses while in setup mode. To eliminate potential compatibility problems in widely varying PC systems, the 82C453 decodes the Global Setup register at I/O port 102h only.

GENERAL CONTROL REGISTERS

Two Input Status Registers read the SENSE pin, pending CRT interrupt, display enable/HSYNC output, and vertical retrace/video output. The Feature Control Register selects the VSYNC function while the Miscellaneous Output Register controls I/O address select, clock selection, access to video RAM, memory page, and video SYNC polarity.

CGA / HERCULES REGISTERS

CGA Mode and Color Select registers are provided on-chip for emulation of CGA modes. Hercules Mode and Configuration registers are provided on-chip for emulation of Hercules mode.

SEQUENCER REGISTERS

The Sequencer Index Register contains a 3-bit index to the Sequencer Data Registers. The Reset Register forces an asynchronous or synchronous reset of the sequencer. The Sequencer Clocking Mode Register controls master clocking functions, video enable/disable and selects either an 8 or 9 dot character clock. A Plane/Map Mask Register enables the color plane and write protect. The Character Font Select Register handles video intensity and character generation and controls the display memory plane through the character generator select. The Sequencer Memory Mode Register handles all memory, giving access by the CPU to 4/16/32KBytes, Odd/Even addresses (planes) and writing of data to display memory.

CRT CONTROLLER REGISTERS

The CRT Controller Index Register contains a 6-bit index to the CRT Controller Registers. Twenty eight registers perform all display functions for modes: horizontal and vertical blanking and sync, panning and scrolling, cursor size and location, light pen, and underline.

GRAPHICS CONTROLLER REGISTERS

The Graphics Controller Index Register contains a 4-bit index to the Graphics Controller Registers. The Set/Reset Register controls the format of the CPU data to display memory. It also works with the Enable Set/Reset Register. Reducing 32 bits of display data to 8 bits of CPU data is accomplished by the Color Compare Register. Data Rotate Registers specify the CPU data bits to be rotated and subjected to logical operations. The Read Map Select Register reduces memory data for the CPU in the four plane (16 color) graphics mode. The Graphics Mode Register controls the write, read, and shift register modes. The Miscellaneous Register handles graphics/text, chaining of odd/even planes, and display memory mapping. Additional registers include Color Don't Care and Bit Mask.

ATTRIBUTE CONTROLLER AND EXTERNAL COLOR PALETTE REGISTERS

The Attribute Controller Index Register contains a 5-bit index to the Attribute Controller Registers. A 6th bit is used to enable the video. The Attribute Controller Registers handle internal color lookup table mapping, text/graphics mode, overscan color, and color plane enable. The horizontal Pixel Panning and Pixel Padding Registers control pixel attributes on screen. External color palette registers handle CPU reads and writes to I/O address range 3C6h-3C9h. Some of the registers are located external to the 82C453 in the external color palette. Inmos IMSG176 (Brooktree BT471/476) compatible registers are documented in this manual.

EXTENSION REGISTERS

The 82C453 defines a set of extension registers which are addressed with the 7-bit Extension Register Index. The I/O port address (3Bx/3Dxh) and Read/Write access to the extension registers are controlled by the Extension Enable Register (103h).

The extension registers handle a variety of interfacing, compatibility, and display functions as discussed below. They are grouped into the following logical groups for discussion purposes:

1. Miscellaneous Registers include the 82C453 Version number, Dip Switch, CPU interface, paging control, memory mode control, and diagnostic functions.
2. General Purpose Registers handle video blanking and the video default color.
3. Backwards Compatibility Registers control Hercules, MDA, and CGA emulation modes. Write Protect functions are provided to increase flexibility in providing backwards compatibility.
4. Alternate Horizontal and Vertical Registers handle all horizontal and vertical timing, including sync, blank and offset. These are used for backwards compatibility.

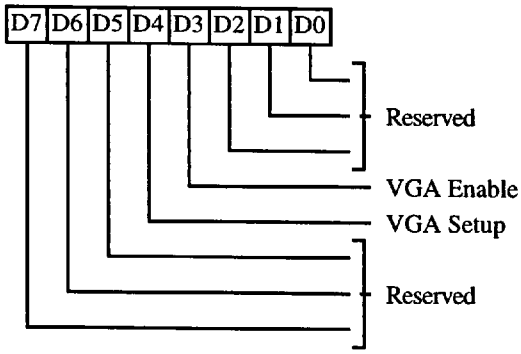
Note: The state of most of the Standard VGA Registers is undefined at reset. All registers specific to the 82C453 (Extension Registers) are summarized in the Extension Register Table.

82C453 Global Control (Setup) Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
–	Setup Control	–	W	46E8h (PC-Bus only)	–	27
–	Global Enable	–	RW	102h & Setup mode	–	27
–	Extension Enable	–	RW	103h & Setup mode	–	28
–	Global ID	–	R	104h & Setup mode	–	29
–	Video Subsystem Enable	–	RW	3C3h (MC Bus only)	–	29

SETUP CONTROL REGISTER

Write only at I/O Address 46E8h



This register is used with the PC-Bus Interface only. It is cleared by RESET. In the MC interface, the Setup mode and VGA Disable are controlled through the SETUP/ and DISA/ pins, respectively.

2-0 Reserved (0)

3 VGA Enable

- 0 VGA is disabled
- 1 VGA is enabled

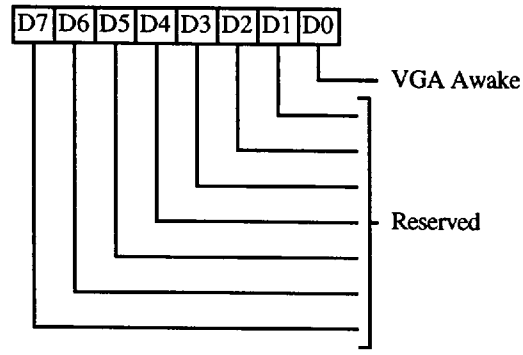
4 Setup Mode

- 0 VGA is in Normal Mode
- 1 VGA is in Setup Mode

7-5 Reserved (0)

GLOBAL ENABLE REGISTER

Read/Write at I/O Address 102h



This register is only accessible in Setup Mode. It is cleared by RESET.

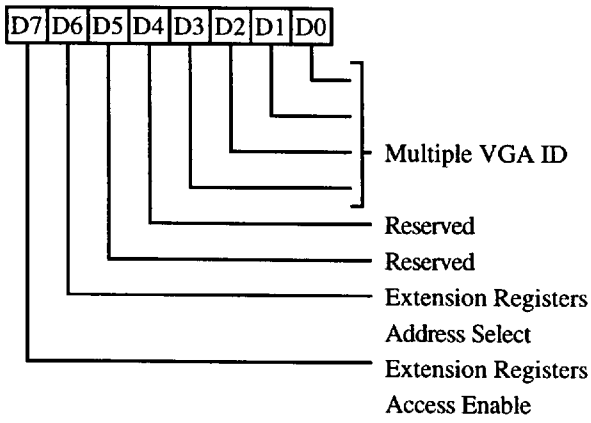
0 VGA Awake

- 0 VGA is in sleep mode
- 1 VGA is awake

7-1 Reserved (0)

EXTENSION ENABLE REGISTER

Read/Write at I/O Address 103h



This register is only accessible in Setup Mode. It is cleared by RESET.

3-0 Multiple VGA ID. The ID number of the currently active VGA when multiple VGA feature is enabled.

3	2	1	0	Comment
0	0	0	0	1 82C453, no DIP switch to be compared against
0	0	0	1	1 82C453, no DIP switch to be compared against
0	0	1	x	2 82C453s, 1 DIP switch to be compared against
0	1	x	x	4 82C453s, 2 DIP switches to be compared
1	x	x	x	8 82C453s, 3 DIP switches to be compared

5-4 Reserved (0)

6 Address for Extension Registers

- 0 Extension registers at I/O Address 3D6/3D7h
- 1 Extension registers at I/O Address 3B6/3B7

7 Extension Registers Access Enable. This bit controls access to the extension registers at 3D6/7 or 3B6/7. It also allows access to all CGA, MDA and Hercules registers in non-emulation mode.

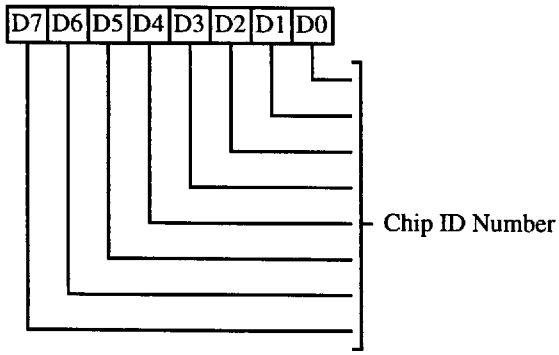
- 0 Disable Access
- 1 Enable Access

The CRT Controller and CGA/Hercules Registers are dependent on this bit and the emulation mode as follows:

CGA/Hercules Bit 7 Emulation Registers Mode	Address	CRTC 3B8,3BF, 3D8, 3D9
0 VGA	3x4/5 only	not accessible
0 CGA	3D0/1,3D2/3 3D4/5,3D6/70	3D8,3D9 accessible
0 Hercules	3B0/1,3B2/3 3B4/5,3B6/7	3B8,3BF accessible
1 any	3x4/5 only	all accessible

GLOBAL ID REGISTER

Read only at I/O Address 104h

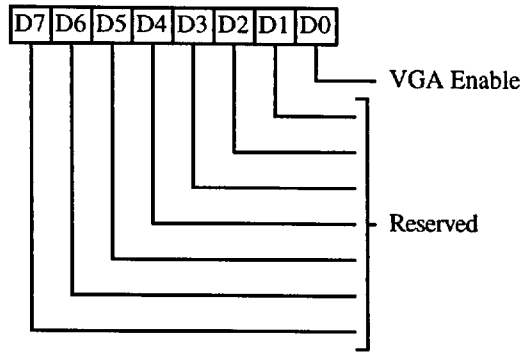


This register is only accessible in Setup Mode.

7-0 These bits contain the ID number (0A5h). This identifies the chip as a Chips and Technologies product.

VIDEO SUBSYSTEM ENABLE REGISTER

Read/Write at I/O Address 3C3h



This register is only accessible in MC Interface. It is cleared by RESET.

0 VGA Enable

- 0 VGA is disabled
- 1 VGA is enabled

7-1 Reserved (0)

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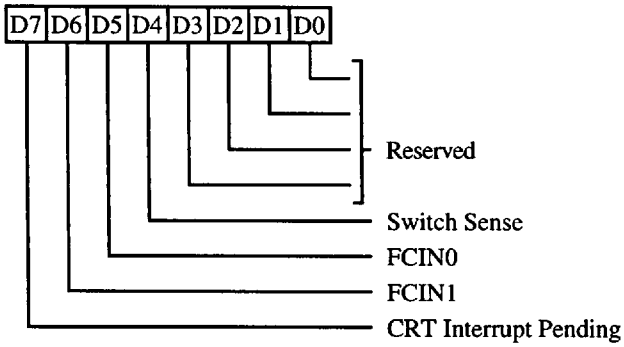
82C453 General Control & Status Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ST00	Input Status 0	–	R	3C2h	–	31
ST01	Input Status 1	–	R	3BAh/3DAh	–	31
FCR	Feature Control	–	W	3BAh/3DAh	5	32
			R	3CAh		
MSR	Miscellaneous Output	–	W	3C2h	5	32
			R	3CCh		

INPUT STATUS REGISTER 0 (ST00)

Read only at I/O Address at 3C2h



3-0 Reserved (0)

4 Switch Sense. This bit returns the Status of the SENSE pin.

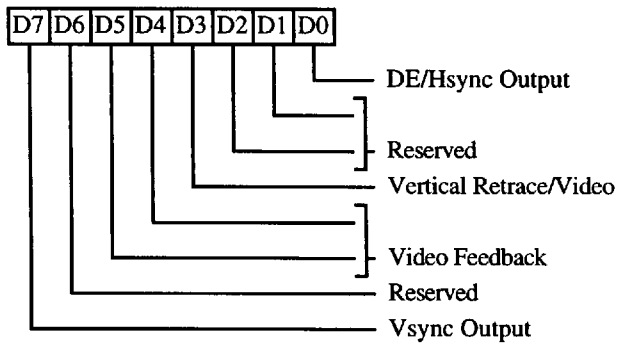
6-5 These bits indicate the status of FCIN0 and FCIN1 input pins.

7 CRT Interrupt Pending

- 0 Indicates no CRT interrupt is pending
- 1 Indicates a CRT interrupt is waiting to be serviced

INPUT STATUS REGISTER 1 (ST01)

Read only at I/O Address 3BAh/3DAh



0 Display Enable/HSYNC Output. The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-4).

- 0 Indicates DE or HSYNC inactive
- 1 Indicates DE or HSYNC active

2-1 Reserved (0)

3 Vertical Retrace/Video. The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-5).

- 0 Indicates VSYNC or video inactive
- 1 Indicates VSYNC or video active

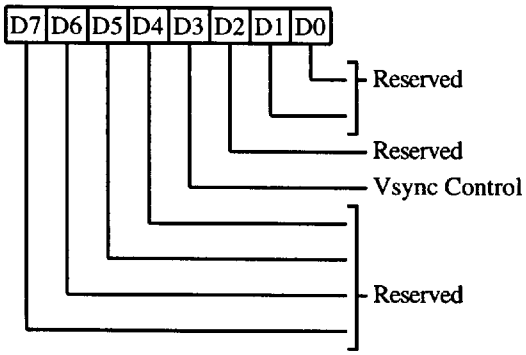
5-4 Video Feedback 1,0. These are diagnostic video bits which are selected via the Color Plane Enable Register.

6 Reserved (0)

7 Vsync Output. The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-6). It reflects the active status of the VSYNC output: 0=inactive, 1=active.

FEATURE CONTROL REGISTER (FCR)

Write at I/O Address 3BAh/3DAh
Read at I/O Address 3CAh
Group 5 Protection



0 This bit is inverted and output on the GPOUT pin.

2-1 Reserved (0)

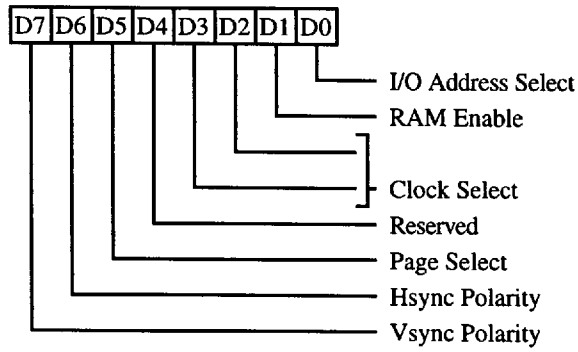
3 Vsync Control This bit is cleared by RESET.

0 VSync output on the VSYNC pin
1 Logical 'OR' of VSync and Display Enable output on the VSYNC pin

7-4 Reserved (0)

MISCELLANEOUS OUTPUT REGISTER (MSR)

Write at I/O Address 3C2h
Read at I/O Address 3CCh
Group 5 Protection



This register is cleared by RESET.

0 I/O Address Select. This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01).

0 Select 3Bxh I/O address
1 Select 3Dxh I/O address

1 Enable RAM.

0 Prevent CPU access to display memory
1 Allow CPU access to display memory

3-2 Clock Select. These bits select the dot clock source for the CRT interface:

32	Clock Source Selected
00	CLK0
01	CLK1
10	CLK2
11	CLK3

4 Reserved (0)

5 Page Select. In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64K byte page in display memory for CPU access: 1=select lower page; 0=select upper page.

6 CRT Hsync Polarity. 0=pos, 1=neg

7 CRT Vsync Polarity. 0=pos, 1=neg

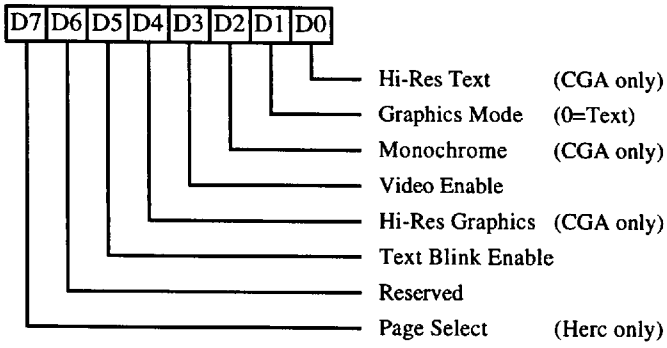
(Blank pin polarity can be controlled via the Video Interface Register)

82C453 CGA / Hercules Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
MODE	CGA/Hercules Mode	–	RW	3D8h	–	33
COLOR	CGA Color Select	–	RW	3D9h	–	34
HCFG	Hercules Configuration	–	RW	3BFh	–	35

CGA / HERCULES MODE CONTROL REGISTER (MODE)

Read/Write at I/O Address 3B8h/3D8h



This register is effective only in CGA and Hercules modes. It is accessible if CGA or Hercules emulation mode is selected or the extension registers are enabled. If the extension registers are enabled, the address is determined by the address select in the Miscellaneous Outputs register. Otherwise the address is determined by the emulation mode. It is cleared by RESET.

0 CGA 80/40 Column Text Mode
- 0 Select 40 column CGA text mode
- 1 Select 80 column CGA text mode

1 CGA/Hercules Graphics/Text Mode
- 0 Select text mode
- 1 Select graphics mode

2 CGA Mono/Color Mode
- 0 Select CGA color mode
- 1 Select CGA monochrome mode

3 CGA/Hercules Video Enable
- 0 Blank the screen
- 1 Enable video output

4 CGA High Resolution Mode
- 0 Select 320x200 graphics mode
- 1 Select 640x200 graphics mode

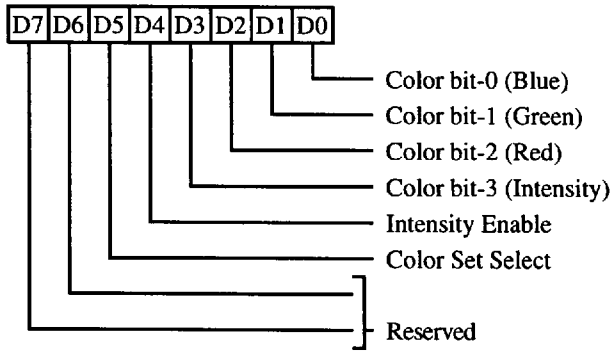
5 CGA/Hercules Text Blink Enable
- 0 Disable character blink attribute (blink attribute bit-7 used to control background intensity)
- 1 Enable character blink attribute

6 Reserved (0)

7 Hercules Page Select
- 0 Select the lower part of memory (starting address B0000h) in Hercules Graphics Mode
- 1 Select the upper part of the memory (starting address B8000h) in Hercules Graphics Mode

CGA COLOR SELECT REGISTER

Read/Write at I/O Address 3D9h



This register is effective only in CGA modes. It is accessible if CGA emulation mode is selected or the extension registers are enabled. This register may also be read or written as an Extension Register (XR7E). It is cleared by RESET. In Hercules Graphics mode, this register should be accessed at 7Eh. A value of OFh in 7Eh will work for the Hercules Graphics mode.

3-0 Color

320x200 4-color: Background Color (color when the pixel value is 0)

The foreground colors (colors when the pixel value is 1-3) are determined by bit-5 of this register.

640x200 2-color: Foreground Color (color when the pixel value is 1)

The background color (color when the pixel value is 0) is black.

4 Intensity Enable

Text Mode: Enables intensified background colors

320x200 4-color: Enables intensified colors 0-3

640x200 2-color: Don't care

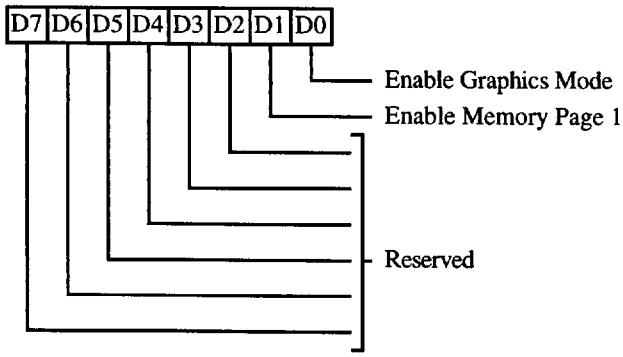
5 Color Set Select. This bit selects one of two available CGA color palettes to be used in 320x200 graphics mode (it is ignored in all other modes) according to the following table:

Pixel Value	Color Set 0	Color Set 1
0 0	Color per bits 0-3	Color per bits 0-3
0 1	Green	Cyan
1 0	Red	Magenta
1 1	Brown	White

7-6 Reserved (0)

HERCULES CONFIGURATION REGISTER (HCFG)

Write only at I/O Address 3BFh



This register is effective only in Hercules mode. It is accessible in Hercules emulation mode or if the extension registers are enabled. It may be read back through XR14D3&2. It is cleared by RESET.

0 Enable Graphics Mode

- 0 Lock the 82C453 in Hercules text mode. In this mode, the CPU has access only to memory address range B0000h-B7FFFh.
- 1 Permit entry to Hercules Graphics mode.

1 Enable Memory Page 1

- 0 Prevent setting of the Page Select bit (bit 7 of the Hercules Mode Control Register). This function also restricts memory usage to addresses B0000h-B7FFFh.
- 1 The Page Select bit can be set and the upper part of display memory (addresses B8000h - BFFFFh) is available.

7-2 Reserved (0)

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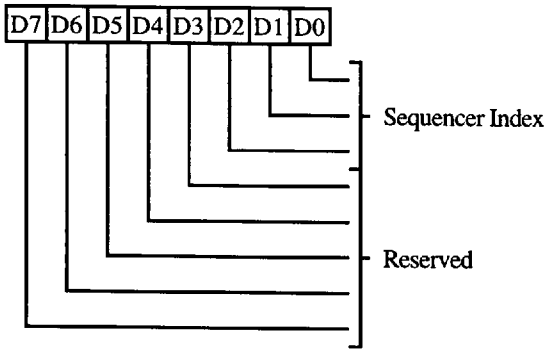
82C453 Sequencer Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SRX	Sequencer Index	–	RW	3C4h	1	37
SR00	Reset	00h	RW	3C5h	1	37
SR01	Clocking Mode	01h	RW	3C5h	1	38
SR02	Plane/Map Mask	02h	RW	3C5h	1	38
SR03	Character Font	03h	RW	3C5h	1	39
SR04	Memory Mode	04h	RW	3C5h	1	40
SR07	Horizontal Character Counter Reset	07h	W	3C5h	–	40

SEQUENCER INDEX REGISTER (SRX)

Read/Write at I/O Address 3C4h



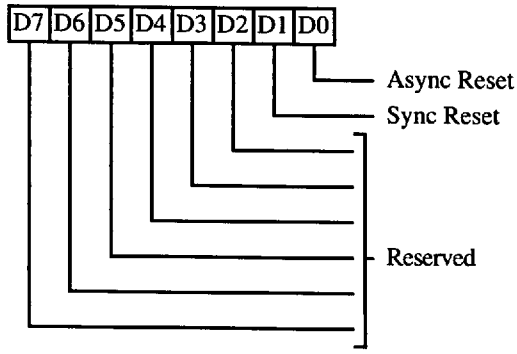
This register is cleared by RESET.

2-0 These bits contain a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7.

7-3 Reserved (0)

SEQUENCER RESET REGISTER (SR00)

Read/Write at I/O Address 3C5h
Index 00h
Group 1 Protection



0 Asynchronous Reset

0 Force asynchronous reset
1 Normal operation

Display memory data will be corrupted if this bit is set to zero.

1 Synchronous Reset

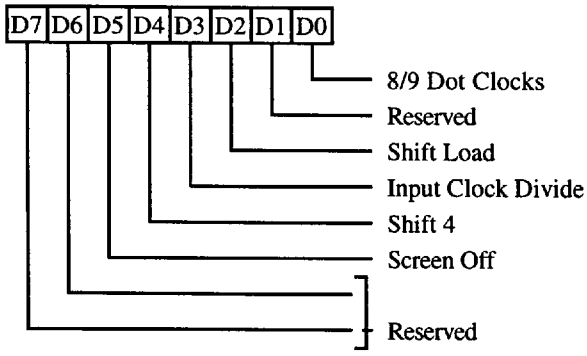
0 Force synchronous reset
1 Normal operation

Display memory data is not corrupted if this bit is set to zero for a short period of time (a few tens of microseconds).

7-2 Reserved (0)

SEQUENCER CLOCKING MODE REGISTER (SR01)

Read/Write at I/O Address 3C5h
Index 01h
Group 1 Protection



0 8/9 Dot Clocks. This bit determines whether a character clock is 8 or 9 dot clocks long.

- 0 Select 9 dots/character clock
- 1 Select 8 dots/character clock

1 Reserved (0)

2 Shift Load

- 0 Load video data shift registers every character clock
- 1 Load video data shift registers every other character clock

Bit-4 of this register must be 0 for this bit to be effective.

3 Input Clock Divide

- 0 Sequencer master clock output on the PCLK pin (used for 640 (720) pixel modes)
- 1 Master clock divided by 2 output on the PCLK pin (used for 320 (360) pixel modes)

4 Shift 4

- 0 Load video shift registers every 1 or 2 character clocks (depending on bit-2 of this register)
- 1 Load shift registers every 4th character clock.

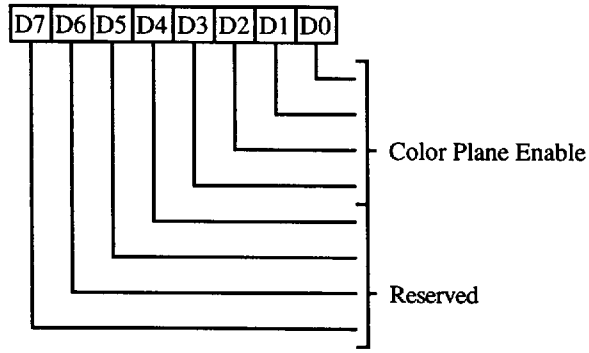
5 Screen Off

- 0 Normal Operation
- 1 Disable video output and assign all display memory bandwidth for CPU accesses

7-6 Reserved (0)

SEQUENCER PLANE/MAP MASK REGISTER (SR02)

Read/Write at I/O Address 3C5h
Index 02h
Group 1 Protection



3-0 Color Plane Enable

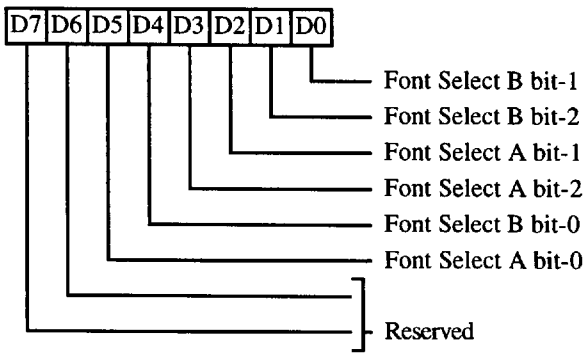
- 0 Write protect corresponding color plane
- 1 Allow write to corresponding color plane

In Odd/Even and Quad modes, these bits still control access to the corresponding color plane.

7-4 Reserved (0)

CHARACTER FONT SELECT REGISTER (SR03)

Read/Write at I/O Address 3C5h
Index 03h
Group 1 Protection



In text modes, bit-3 of the video data's attribute byte normally controls the foreground intensity. This bit may be redefined to control switching between character sets. This latter function is enabled whenever there is a difference in the values of the Character Font Select A and the Character Font Select B bits. If the two values are the same, the character select function is disabled and attribute bit-3 controls the foreground intensity.

SR04 bit-1 must be 1 for the character font select function to be active. Otherwise, only character fonts 0 and 4 are available.

1-0 High order bits of Character Generator Select B.

3-2 High order bits of Character Generator Select A.

4 Low order bit of Character Generator Select B.

5 Low order bit of Character Generator Select A.

7-6 Reserved (0)

The following table shows the display memory plane selected by the Character Generator Select A and B bits.

Code	Character Generator Table Location
0	First 8K of Plane 2
1	Second 8K of Plane 2
2	Third 8K of Plane 2
3	Fourth 8K of Plane 2
4	Fifth 8K of Plane 2
5	Sixth 8K of Plane 2
6	Seventh 8K of Plane 2
7	Eighth 8K of Plane 2

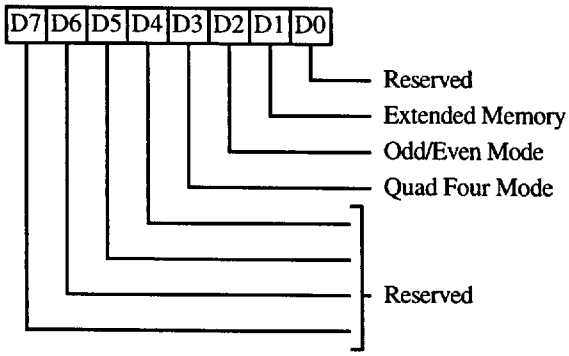
where 'code' is:

Character Generator Select A (bits 3, 2, 5) when bit-3 of the the attribute byte is one.

Character Generator Select B (bits 1, 0, 4) when bit-3 of the attribute byte is zero.

SEQUENCER MEMORY MODE REGISTER (SR04)

Read/Write at I/O Address 3C5h
Index 04h
Group 1 Protection



0 Reserved (0)

1 Extended Memory

- 0 Restrict CPU access to 4/16/32 Kbytes
- 1 Allow complete access to memory

This bit should normally be 1.

2 Odd/Even Mode

- 0 CPU accesses to Odd/Even addresses are directed to corresponding odd/even planes
- 1 All planes are accessed simultaneously (IRGB color)

Bit-3 of this register must be 0 for this bit to be effective. This bit affects only CPU write accesses to display memory.

3 Quad Four Mode

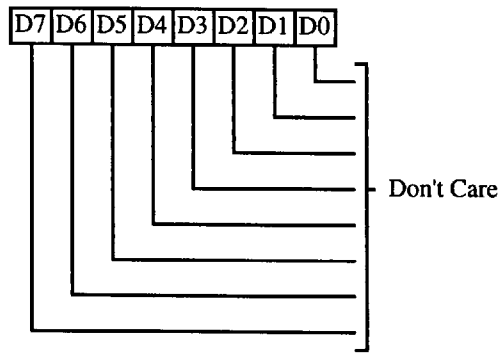
- 0 CPU addresses are mapped to display memory as defined by bit-2 of this register
- 1 CPU addresses are mapped to display memory modulo 4. The two low order CPU address bits select the display memory plane.

This bit affects both CPU reads and writes to display memory.

7-4 Reserved (0)

SEQUENCER HORIZONTAL CHARACTER COUNTER RESET REGISTER (SR07)

Read/Write at I/O Address 3C5h
Index 07h



Writing to SR07 with any data will cause the horizontal character counter to be held reset (character counter output = 0) until a write to any other sequencer register with any data value. The write to any index in the range 0-6 clears the latch that is holding the reset condition on the character counter.

The vertical line counter is clocked by a signal derived from horizontal display enable (which does not occur if the horizontal counter is held reset). Therefore, if the write to SR07 occurs during vertical retrace, the horizontal and vertical counters will both be set to zero. A write to any other sequencer register may then be used to start both counters with reasonable synchronization to an external event via software control.

This is a standard VGA register which was not documented by IBM.

82C453 CRT Controller Registers

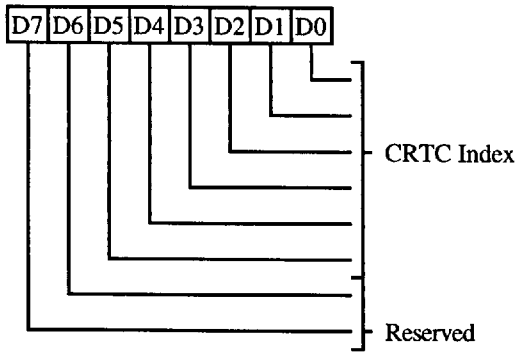
Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
CRX	CRTC Index	–	RW	3B4h/3D4h	–	42
CR00	Horizontal Total	00h	RW	3B5h/3D5h	0	42
CR01	Horizontal Display Enable End	01h	RW	3B5h/3D5h	0	42
CR02	Horizontal Blank Start	02h	RW	3B5h/3D5h	0	43
CR03	Horizontal Blank End	03h	RW	3B5h/3D5h	0	43
CR04	Horizontal Sync Start	04h	RW	3B5h/3D5h	0	44
CR05	Horizontal Sync End	05h	RW	3B5h/3D5h	0	44
CR06	Vertical Total	06h	RW	3B5h/3D5h	0	45
CR07	Overflow	07h	RW	3B5h/3D5h	0/3	45
CR08	Preset Row Scan	08h	RW	3B5h/3D5h	3	46
CR09	Maximum Scan Line	09h	RW	3B5h/3D5h	2/4	46
CR0A	Cursor Start Scan Line	0Ah	RW	3B5h/3D5h	2	47
CR0B	Cursor End Scan Line	0Bh	RW	3B5h/3D5h	2	47
CR0C	Start Address High	0Ch	RW	3B5h/3D5h	–	48
CR0D	Start Address Low	0Dh	RW	3B5h/3D5h	–	48
CR0E	Cursor Location High	0Eh	RW	3B5h/3D5h	–	48
CR0F	Cursor Location Low	0Fh	RW	3B5h/3D5h	–	48
CR10	Vertical Sync Start (See Note 2)	10h	W or RW	3B5h/3D5h	4	49
CR11	Vertical Sync End (See Note 2)	11h	W or RW	3B5h/3D5h	3/4	49
CR10	Lightpen High (See Note 2)	10h	R	3B5h/3D5h	–	49
CR11	Lightpen Low (See Note 2)	11h	R	3B5h/3D5h	–	49
CR12	Vertical Display Enable End	12h	RW	3B5h/3D5h	4	50
CR13	Offset	13h	RW	3B5h/3D5h	3	50
CR14	Underline Row	14h	RW	3B5h/3D5h	3	50
CR15	Vertical Blank Start	15h	RW	3B5h/3D5h	4	51
CR16	Vertical Blank End	16h	RW	3B5h/3D5h	4	51
CR17	CRT Mode Control	17h	RW	3B5h/3D5h	3/4	52
CR18	Line Compare	18h	RW	3B5h/3D5h	3	53
CR22	Memory Data Latches	22h	R	3B5h/3D5h	–	54
CR24	Attribute Controller Toggle	24h	R	3B5h/3D5h	–	54
CR3x	Clear Vertical Display Enable	3xh	W	3B5h/3D5h	–	54

Note 1: When MDA or Hercules emulation is enabled, the CRTC I/O address should be set to 3B0h-3B7h by setting the I/O address select bit in the Miscellaneous Output register (3C2h/3CCh bit-0) to zero. When CGA emulation is enabled, the CRTC I/O address should be set to 3D0h-3D7h by setting Misc Output Register bit-0 to 1.

Note 2: In both the EGA and VGA, the light pen registers are at index locations conflicting with the vertical sync registers. This would normally prevent reads and writes from occurring at the same index. Since the light pen registers are not normally useful, the VGA provides software control (CR03 bit-7) of whether the vertical sync or light pen registers are readable at indices 10-11.

CRTC INDEX REGISTER (CRX)

Read/Write at I/O Address 3B4h/3D4h

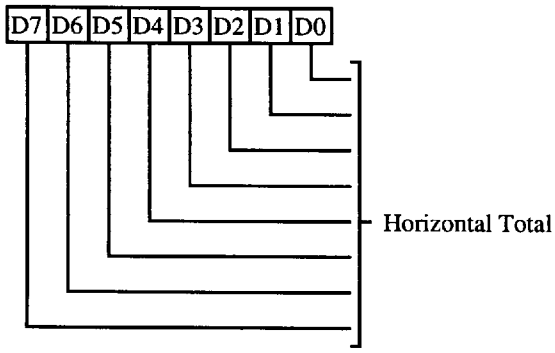


5-0 CRTC data register index

7-6 Reserved (0)

HORIZONTAL TOTAL REGISTER (CR00)

Read/Write at I/O Address 3B5h/3D5h
Index 00h
Group 0 Protection

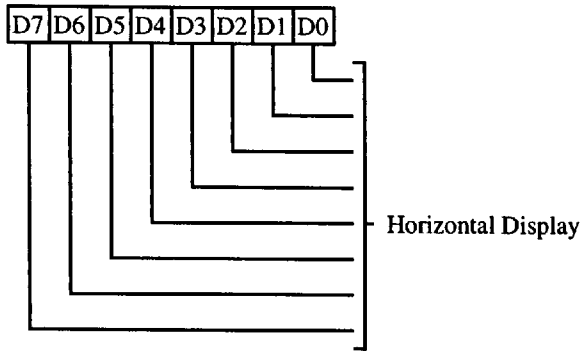


This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Total. Total number of character clocks per line = contents of this register + 5. This register determines the horizontal sweep rate.

HORIZONTAL DISPLAY ENABLE END REGISTER (CR01)

Read/Write at I/O Address 3B5h/3D5h
Index 01h
Group 0 Protection

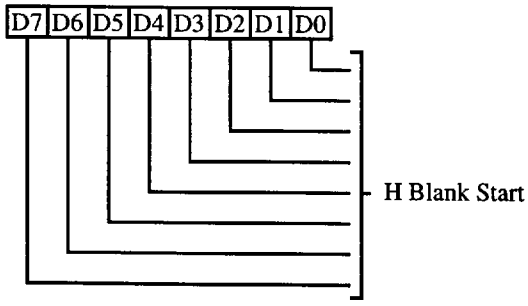


This register is used for all VGA and EGA modes on CRTs. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Number of Characters displayed per scan line - 1.

HORIZONTAL BLANK START REGISTER (CR02)

Read/Write at I/O Address 3B5h/3D5h
Index 02h
Group 0 Protection

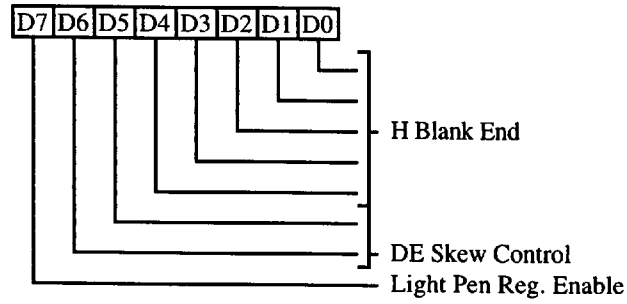


This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 These bits specify the beginning of horizontal blank in terms of character clocks from the beginning of the display scan. The period between Horizontal Display Enable End and Horizontal Blank Start is the right side border on screen.

HORIZONTAL BLANK END REGISTER (CR03)

Read/Write at I/O Address 3B5h/3D5h
Index 03h
Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

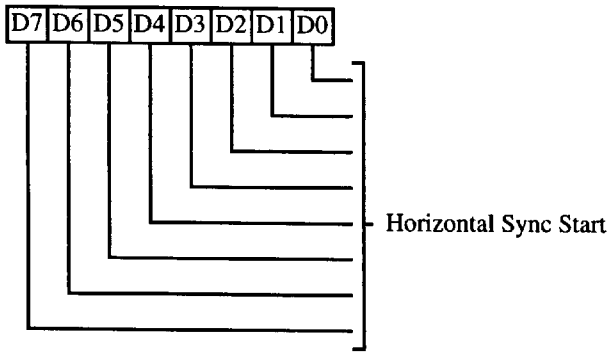
4-0 These are the lower 5 bits of the character clock count used to define the end of horizontal blank. The interval between the end of horizontal blank and the beginning of the display (a count of 0) is the left side border on the screen. The horizontal blanking width, W is: Value in Start Blanking Register + W = 6 bit Value. Lower 5 bits are programmed in this register. 6th bit is programmed in bit-7 of CR05.

6-5 Display Enable Skew Control: Defines the number of character clocks that the Display Enable signal is delayed to compensate for internal pipeline delays.

7 Light Pen Register Enable: Must be 1 for normal operation; when this bit is 0, CRTC registers CR10 and CR11 function as light-pen readback registers.

HORIZONTAL SYNC START REGISTER (CR04)

Read/Write at I/O Address 3B5h/3D5h
Index 04h
Group 0 Protection

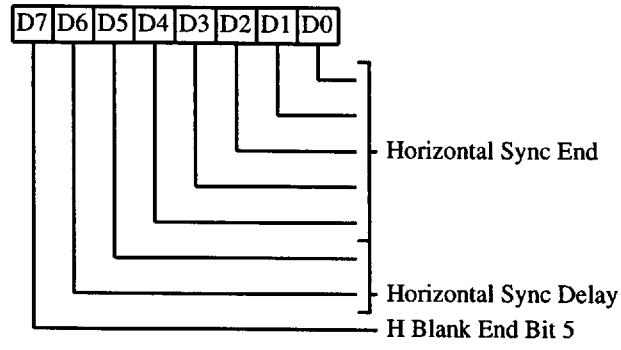


This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 These bits specify the beginning of Hsync in terms of Character clocks from the beginning of the display scan. These bits also determine display centering on the screen.

HORIZONTAL SYNC END REGISTER (CR05)

Read/Write at I/O Address 3B5h/3D5h
Index 05h
Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

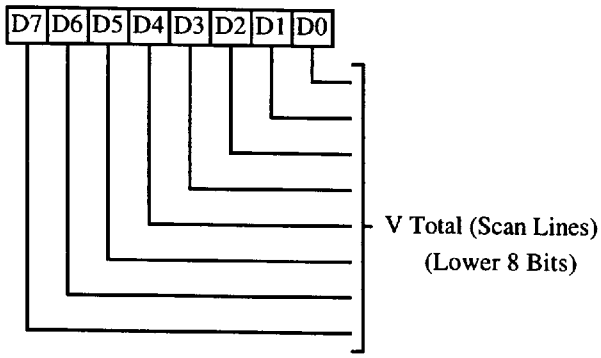
4-0 Hsync End. Lower 5 bits of the character clock count which specifies the end of Horizontal Sync. The horizontal sync width W, is: Value in Start Sync Register + W = 5 bit value to be programmed in this register.

6-5 Horizontal Sync Delay. These bits specify the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.

7 Horizontal Blank End Bit 5. Sixth bit of the Horizontal Blank End Register (CR03).

VERTICAL TOTAL REGISTER (CR06)

Read/Write at I/O Address 3B5h/3D5h
Index 06h
Group 0 Protection



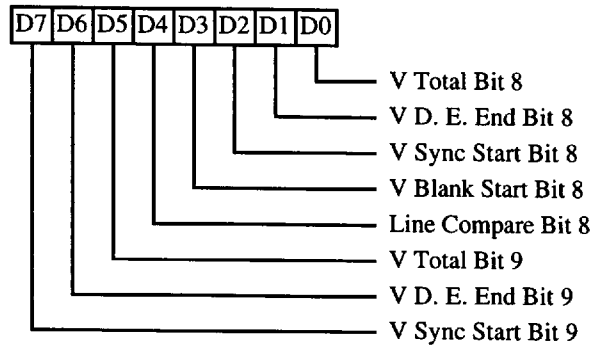
This register is used in all modes.

7-0 These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow Register. The Vertical Total value specifies the total number of scan lines (horizontal retrace periods) per frame.

Programmed Count = Actual Count - 2

OVERFLOW REGISTER (CR07)

Read/Write at I/O Address 3B5h/3D5h
Index 07h
Group 0 Protection on bits 0-3 and bits 5-7
Group 3 Protection on bit 4



This register is used in all modes.

0 Vertical Total Bit 8

1 Vertical Display Enable End Bit 8

2 Vertical Sync Start Bit 8

3 Vertical Blank Start Bit 8

4 Line Compare Bit 8

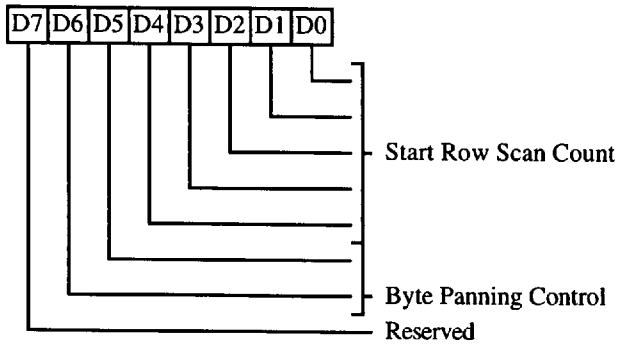
5 Vertical Total Bit 9

6 Vertical Display Enable End Bit 9

7 Vertical Sync Start Bit 9

PRESET ROW SCAN REGISTER (CR08)

Read/Write at I/O Address 3B5h/3D5h
Index 08h
Group 3 Protection



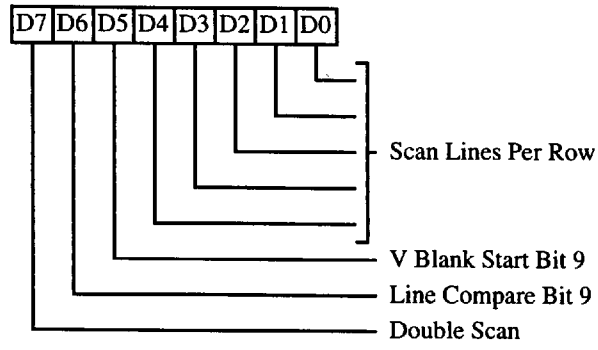
4-0 These bits specify the starting row scan count after each vertical retrace. Every horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count during active display. This register is used for soft scrolling in text modes.

6-5 Byte Panning Control. These bits specify the lower order bits for the display start address. They are used for horizontal panning in Odd/Even and Quad modes.

7 Reserved (0)

MAXIMUM SCAN LINE REGISTER (CR09)

Read/Write at I/O Address 3B5h/3D5h
Index 09h
Group 2 Protection on bits 0-4
Group 4 Protection on bits 5-7



4-0 These bits specify the number of scan lines in a row: Number of scan lines per row = value + 1.

5 Bit 9 of the Vertical Blank Start register

6 Bit 9 of the Line Compare register

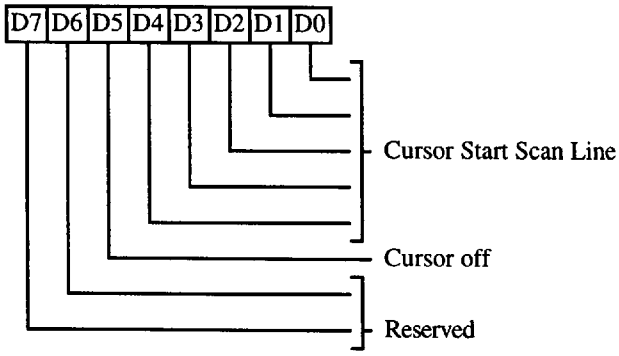
7 Double Scan

0 Normal Operation
1 Enable scan line doubling

The vertical parameters in the CRT Controller (even for a split screen) are not affected, only the CRTC row scan counter (bits 0-4 of this register) and display memory addressing screen refresh are affected.

CURSOR START SCAN LINE REGISTER (CR0A)

Read/Write at I/O Address 3B5h/3D5h
Index 0Ah
Group 2 Protection



4-0 These bits specify the scan line of the character row where the cursor display begins.

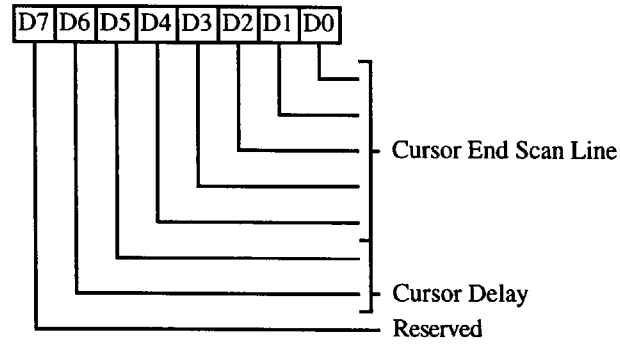
5 Cursor Off

0 Text Cursor On
1 Text Cursor Off

7-6 Reserved (0)

CURSOR END SCAN LINE REGISTER (CR0B)

Read/Write at I/O Address 3B5h/3D5h
Index 0Bh
Group 2 Protection



4-0 These bits specify the scan line of a character row where the cursor display ends: Last scan line for the block cursor = Value + 1.

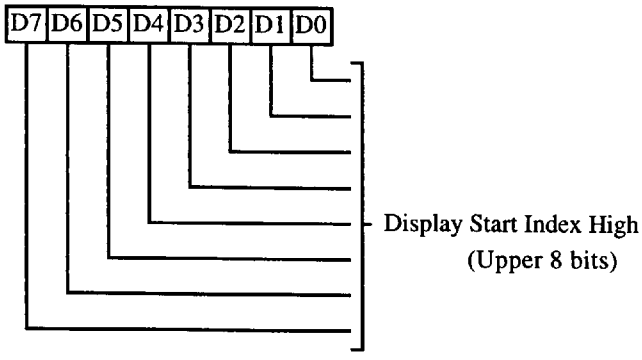
6-5 These bits define the number of character clocks that the cursor is delayed to compensate for internal pipeline delay.

7 Reserved (0)

Note: If the Cursor Start Line is greater than the Cursor End Line, then no cursor is generated.

START INDEX HIGH REGISTER (CR0C)

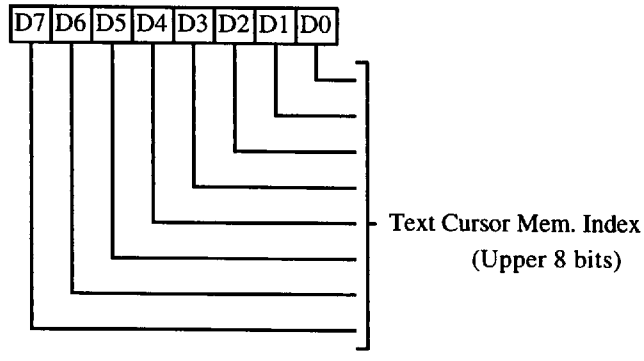
Read/Write at I/O Address 3B5h/3D5h
Index 0Ch



7-0 Upper 8 bits of display start address. In CGA / MDA / Hercules modes, this register wraps around at the 16, 32, and 64 KByte boundaries respectively.

CURSOR LOCATION HIGH REGISTER (CR0E)

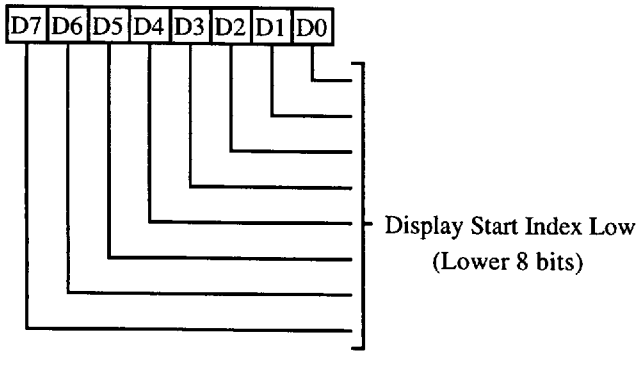
Read/Write at I/O Address 3B5h/3D5h
Index 0Eh



7-0 Upper 8 bits of the memory address where the text cursor is active. In CGA / MDA / Hercules modes, this register wraps around at 16, 32, and 64 KByte boundaries respectively.

START INDEX LOW REGISTER (CR0D)

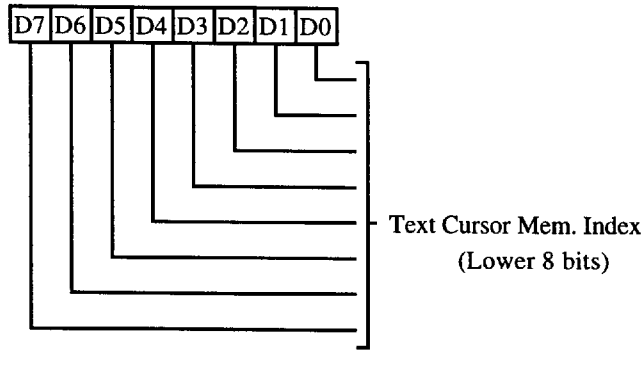
Read/Write at I/O Address 3B5h/3D5h
Index 0Dh



7-0 Lower 8 bits of the display start address. The display start address points to the memory address corresponding to the top left corner of the screen.

CURSOR LOCATION LOW REGISTER (CR0F)

Read/Write at I/O Address 3B5h/3D5h
Index 0Fh



7-0 Lower 8 bits of the memory address where the text cursor is active. In CGA / MDA / Hercules modes, this register wraps around at 16, 32, and 64 KByte boundaries respectively.

LIGHTPEN HIGH REGISTER (CR10)

Read only at I/O Address 3B5h/3D5h
Index 10h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

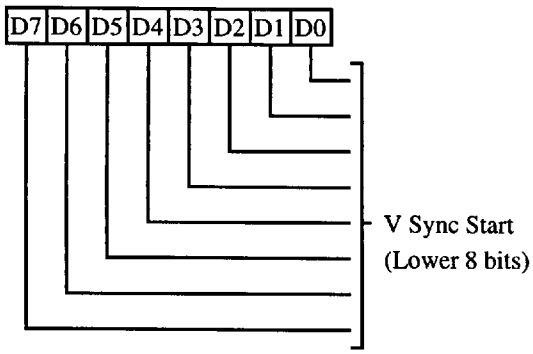
LIGHTPEN LOW REGISTER (CR11)

Read only at I/O Address 3B5h/3D5h
Index 11h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

VERTICAL SYNC START REGISTER (CR10)

Read/Write at I/O Address 3B5h/3D5h
Index 10h
Group 4 Protection

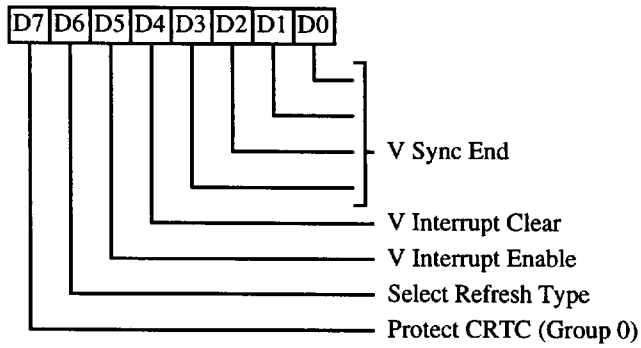


This register is used in all modes. This register is not readable in (Line Compare bit-9) MDA/Hercules emulation or when CR03 bit 7 = 1.

7-0 The eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRTC Overflow Register. They define the scan line position at which Vertical Sync becomes active.

VERTICAL SYNC END REGISTER (CR11)

Read/Write at I/O Address 3B5h/3D5h
Index 11h
Group 3 Protection for bits 4 and 5
Group 4 Protection for bits 0-3, 6 and 7



This register is used in all modes. This register is not readable in MDA/Hercules emulation or when CR03 bit 7 = 1.

3-0 Vertical Sync End

Lower 4 bits of the scan line count that defines the end of vertical sync. The Vertical sync width, W is: Value in Vertical Sync Start Register + W = 4 bit value to be programmed in this register.

4 Vertical Interrupt Clear

0 Clear vertical interrupt generated on the IRQ output
1 Normal operation. This bit is cleared by RESET.

5 Vertical Interrupt Enable

0 Enable vertical interrupt
1 Disable vertical interrupt. This bit is cleared by RESET.

6 Select Refresh Type

0 3 refresh cycles per scan line
1 5 refresh cycles per scan line

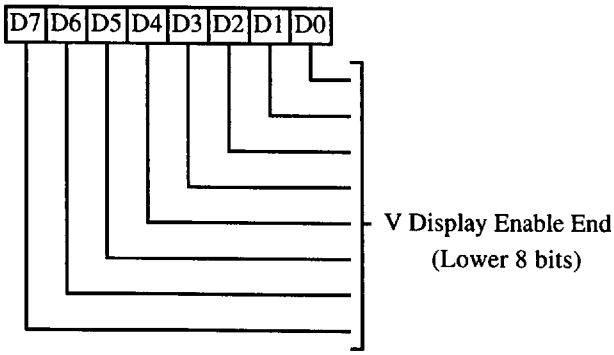
7 Group Protect 0. This bit is logically ORed with XR15 bit-6 to determine the protection for group 0 registers. This bit is cleared by RESET.

0 Enable writes to CR00-CR07
1 Disable writes to CR00-CR07

CR07 bit-4 (Line Compare bit-8) is not affected by this bit.

VERTICAL DISPLAY ENABLE END REGISTER (CR12)

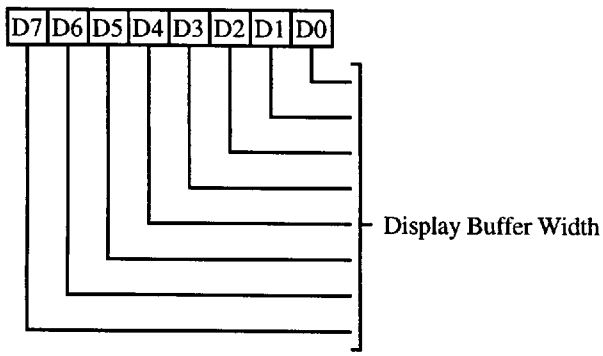
Read/Write at I/O Address 3B5h/3D5h
Index 12h
Group 4 Protection



7-0 These are the eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow register. The actual count = Contents of this register + 1.

OFFSET REGISTER (CR13)

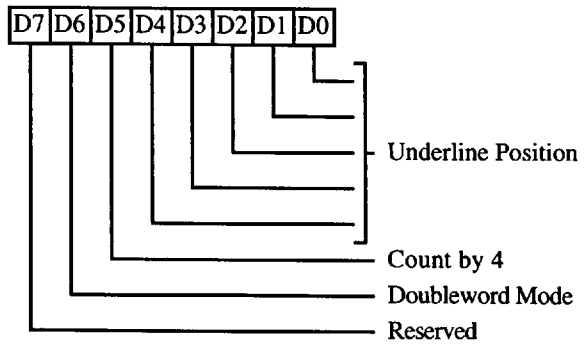
Read/Write at I/O Address 3B5h/3D5h
Index 13h
Group 3 Protection



7-0 Display Buffer Width. The byte starting address of the next display row = Byte Start Address for current row + K* (CR13 where K = 2 in byte mode, K = 4 in word mode. Byte, word and double word mode is selected by bit-6 of CR17 and bit-6 of CR14. A less significant bit than bit-0 of this register is defined in the Auxiliary Offset register (XR0D). This allows finer resolution of the bit map width. Byte, word and doubleword mode affects the translation of the 'logical' display memory address to the 'physical' display memory address.

UNDERLINE LOCATION REGISTER (CR14)

Read/Write at I/O Address 3B5h/3D5h
Index 14h
Group 3 Protection



4-0 These bits specify the underline's scan line position within a character row. Value = Actual scan line number - 1.

5 Count by 4 for Doubleword Mode.

- 0 Frame Buffer Address is incremented by 1 or 2
- 1 Frame Buffer Address is incremented by 4 or 2. See CR17 bit-3 for further details.

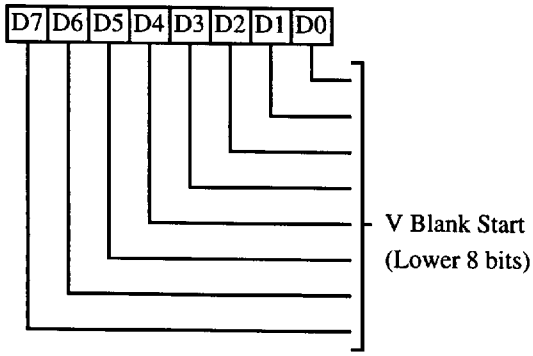
6 Doubleword Mode.

- 0 Frame Buffer Address is byte or word address
- 1 Frame Buffer Address is doubleword address. Used in conjunction with CR17 bit-6 to select the display memory addressing mode.

7 Reserved (0)

VERTICAL BLANK START REGISTER (CR15)

Read/Write at I/O Address 3B5h/3D5h
Index 15h
Group 4 Protection

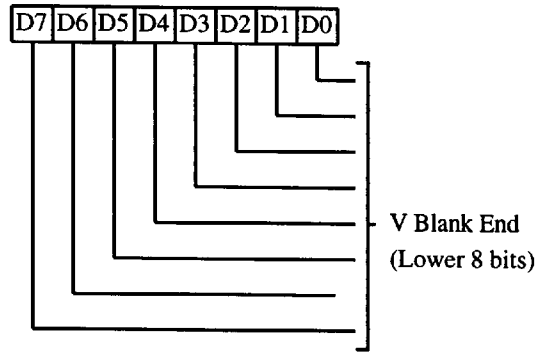


This register is used in all modes.

7-0 These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers respectively. Together these 10 bits define the scan line position where vertical blank begins. The interval between the end of the vertical display and the beginning of vertical blank is the bottom border on the screen.

VERTICAL BLANK END REGISTER (CR16)

Read/Write at I/O Address 3B5h/3D5h
Index 16h
Group 4 Protection

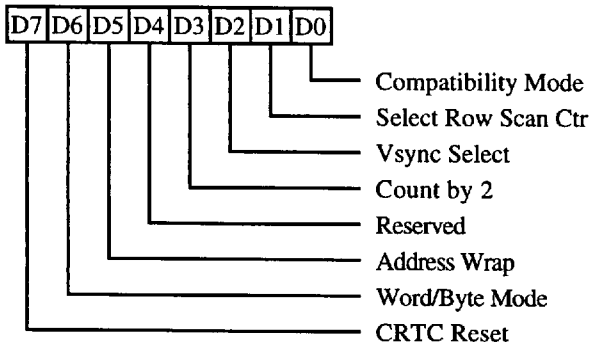


This register is used in all modes.

7-0 End Vertical Blank. These are the 8 low order bits of the scan line count which specifies the end of Vertical Blank. The vertical Blank Width, W, is: Value in Vertical Blank Start Register – 1 + W = 8-bit value to be programmed in this register.

CRT MODE CONTROL REGISTER (CR17)

Read/Write at I/O Address 3B5h/3D5h
Index 17h
Group 3 Protection for bits 0,1 and 3-7
Group 4 Protection for bit 2.



0 Compatibility Mode Support. This bit allows compatibility with the IBM CGA two-bank graphics mode.

- 0 The character row scan line counter bit 0 is substituted for memory address bit 13 during active display time
- 1 Normal operation, no substitution takes place.

1 Select Row Scan Counter. This bit allows compatibility with Hercules graphics and with any other 4-bank graphics system.

- 0 Substitute character row scan line counter bit 1 for memory address bit-14 during active display time
- 1 Normal operation, no substitution takes place

2 Vertical Sync Select. This bit controls the vertical resolution of the CRT Controller by permitting selection of the clock rate input to the vertical counters. When set to 1, the vertical counters are clocked by the horizontal retrace clock divided by 2.

3 Count By Two

- 0 Memory address counter is incremented every character clock
- 1 Memory address counter is incremented every two character clocks, used in conjunction with bit 5 of 0Fh.

Note: This bit is used in conjunction with CR14 bit-5. The net effect is as follows:

CR14 Bit-5	CR17 Bit-3	Increment Addressing Every
0	0	1 CCLK
0	1	2 CCLK
1	0	4 CCLK
1	1	2 CCLK

Note: In Hercules graphics and Hi-res CGA modes, the address inrements every two clocks.

4 Reserved (0)

5 Address Wrap (effective only in word mode.)

- 0 Wrap display memory address at 16 Kbytes. This is used in IBM CGA mode
- 1 Normal operation (extended mode)

6 Word Mode or Byte Mode.

- 0 Word Mode is selected. In this mode the display memory address counter bits are shifted down by one, causing the most-significant bit of the counter to appear on the least-significant bit of the display memory address output
- 1 Select byte mode.

Note: This bit is used in conjunction with CR14 bit-6 to select byte, word, or double word memory addressing as follows:

CR14 Bit-6	CR17 Bit-6	Addressing Mode
0	0	Word Mode
0	1	Byte Mode
1	0	Double Word Mode
1	1	Double Word Mode

Display memory addresses are affected as shown in the table on the following page.

7 Hardware Reset (This bit is cleared by RESET)

- 0 Force HSYNC and VSYNC to be inactive. No other registers or outputs affected.
- 1 Normal Operation.

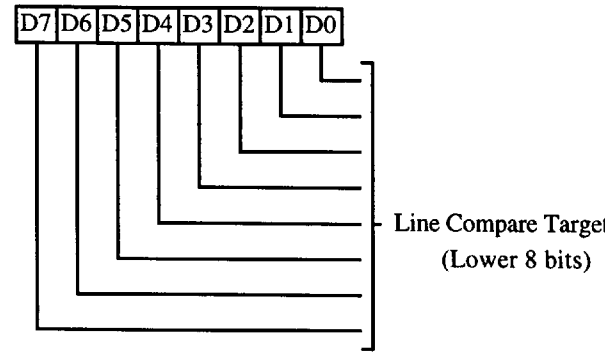
Display memory addresses are affected by CR17 bit-6 as shown in the table below:

Logical Memory Address	Physical Memory Address Byte Mode	Word Mode	Double Word Mode
MA00	A00	Note 1	Note 2
MA01	A01	A00	Note 3
MA02	A02	A01	A00
MA03	A03	A02	A01
MA04	A04	A03	A02
MA05	A05	A04	A03
MA06	A06	A05	A04
MA07	A07	A06	A05
MA08	A08	A07	A06
MA09	A09	A08	A07
MA10	A10	A09	A08
MA11	A11	A10	A09
MA12	A12	A11	A10
MA13	A13	A12	A11
MA14	A14	A13	A12
MA15	A15	A14	A13

Note 1 = A13 * NOT CR17 D5 + A15 * CR17 D5
Note 2 = A12
Note 3 = A13

LINE COMPARE REGISTER (CR18)

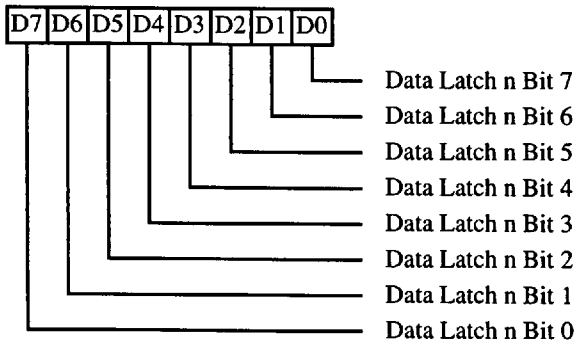
Read/Write at I/O Address 3B5h/3D5h
Index 18h
Group 3 Protection



7-0 These are the low order 8 bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers, respectively. This register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address counter is cleared to 0. The display memory address counter then sequentially addresses the display memory starting at address 0. Each subsequent row address is generated by the addition of the Offset Register contents. This register is not affected by the double scanning bit (CR09 bit-7).

MEMORY DATA LATCH REGISTER (CR22)

Read only at I/O Address 3B5h/3D5h
Index 22h



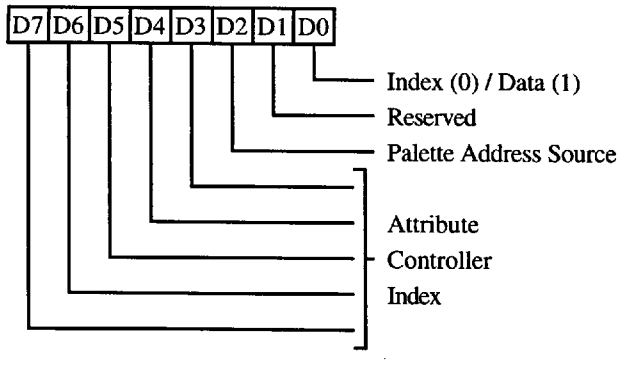
This register may be used to read the state of Graphics Controller Memory Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (GR04 bits 0&1) and is in the range 0-3.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

ATTRIBUTE CONTROLLER TOGGLE REGISTER (CR24)

Read only at I/O Address 3B5h/3D5h
Index 24h



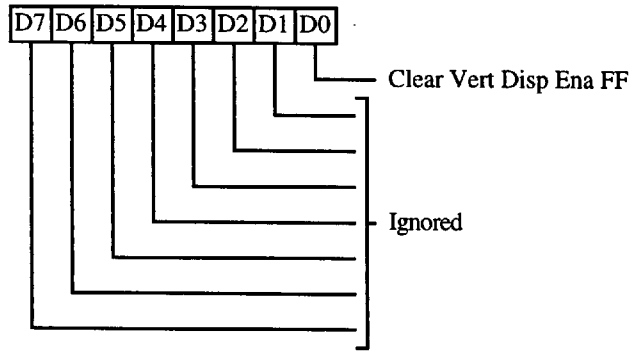
This register may be used to read back the state of the attribute controller index/data latch.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

CLEAR VERTICAL DISPLAY ENABLE FFh (CR3X)

Write only at I/O Address 3B5h/3D5h
Index 3xh



Writing odd data values to CRTC index 30-3Fh causes the vertical display enable flip-flop to be cleared. The flip-flop is automatically set by reaching vertical total. The effect of this is to force a longer vertical retrace period. There are two side effects of terminating vertical display enable early: first, the screen blanks early for one frame causing a minor visual disturbance and second, the sequencer gives more display memory cycles to the CPU because vertical display is not enabled.

Reads from this register are not decoded and will return indeterminate data.

This is a standard VGA register which was not documented by IBM.

Write Protect Register Grouping

Register Number	Group 0	Group 2	Group 3	Group 4	Unprotected
CR00	Yes	-	-	-	
CR01		Yes	-	-	-
CR02	Yes	-	-	-	
CR03	Yes	-	-	-	
CR04	Yes	-	-	-	-
CR05	Yes	-	-	-	-
CR06	Yes	-	-	-	-
CR07	Bits 0-3, 5-7		Bit 4	-	-
CR08	-	-	Yes	-	-
CR09	-	Bits 0-4	-	Bits 5-7	-
CR0A	-	Yes	-	-	-
CR0B	-	Yes	-	-	-
CR0C	-	-	-	-	Yes
CR0D	-	-	-	-	Yes
CR0E	-	-	-	-	Yes
CR0F	-	-	-	-	Yes
CR10	-	-	-	Yes	-
CR11	-	-	Bits 4-5	0-3,6	-
CR12	-	-	Yes	-	-
CR13	-	-	Yes	-	-
CR14	-	-	Yes	-	-
CR15	-	-	-	Yes	-
CR16	-	-	-	Yes	-
CR17	-	-	0,1,3-7	Bit 2	-
CR18	-	-	Yes	-	-

NOTE: All the registers at address 3Cx fall under group 1.

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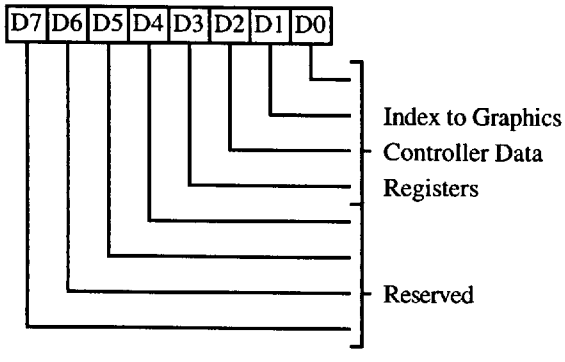
82C453 Graphics Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
GRX	Graphics Index	–	RW	3CEh	1	57
GR00	Set/Reset	00h	RW	3CFh	1	57
GR01	Enable Set/Reset	01h	RW	3CFh	1	58
GR02	Color Compare	02h	RW	3CFh	1	58
GR03	Data Rotate	03h	RW	3CFh	1	59
GR04	Read Map Select	04h	RW	3CFh	1	59
GR05	Graphics mode	05h	RW	3CFh	1	60
GR06	Miscellaneous	06h	RW	3CFh	1	62
GR07	Color Don't Care	07h	RW	3CFh	1	62
GR08	Bit Mask	08h	RW	3CFh	1	63

GRAPHICS CONTROLLER INDEX REGISTER (GRX)

Write only at I/O Address 3CEh
Group 1 Protection

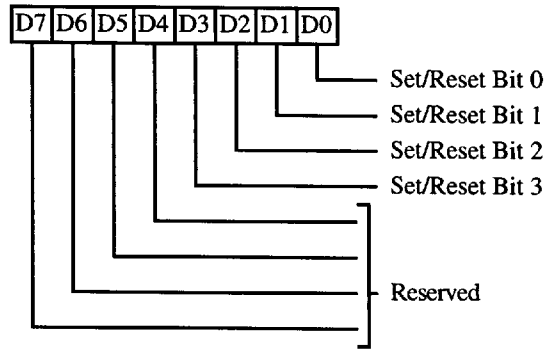


3-0 4-bit index to Graphics Controller registers

7-4 Reserved (0)

SET/RESET REGISTER (GR00)

Read/Write at I/O Address 3CFh
Index 00h
Group 1 Protection



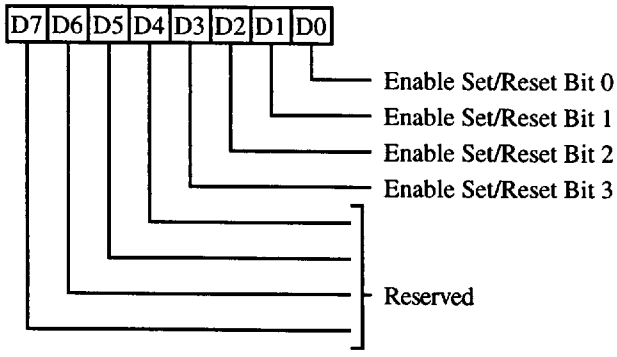
The SET/RESET and ENABLE SET/RESET registers are used to 'expand' 8 bits of CPU data to 32 bits of display memory.

3-0 When the Graphics Mode register selects Write Mode 0, all 8 bits of each display memory plane are set as specified in the corresponding bit in this register. The Enable Set/Rest register (GR01) allows selection of some of the source of data to be written to individual planes. In Write Mode 3 (see GR05), these bits determine the color value.

7-4 Reserved (0)

ENABLE SET/RESET REGISTER (GR01)

Read/Write at I/O Address 3CFh
Index 01h
Group 1 Protection



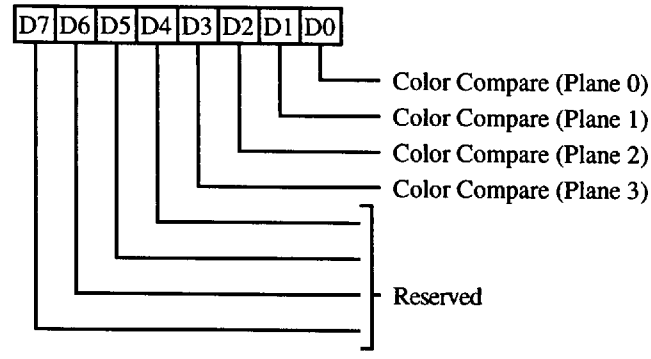
3-0 This register works in conjunction with the Set/Reset register (GR00). The Graphics Mode register must be programmed to Write Mode 0 in order for this register to have any effect.

0 The corresponding plane is written with the data from the CPU data bus
1 The corresponding plane is set to 0 or 1 as specified in the Set/Reset Register

7-4 Reserved (0)

COLOR COMPARE REGISTER (GR02)

Read/Write at I/O Address 3CFh
Index 02h
Group 1 Protection

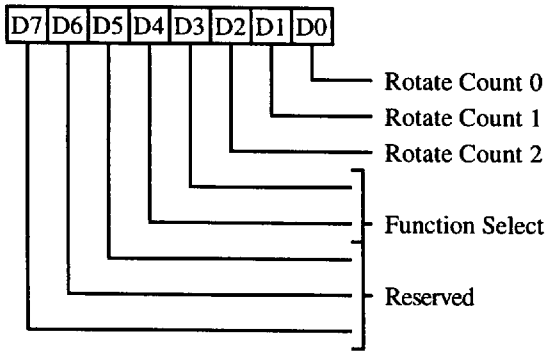


3-0 This register is used to 'reduce' 32 bits of memory data to 8 bits for the CPU in 4-plane graphics mode. These bits provide a reference color value to compare to data read from display memory planes 0-3. The Color Don't Care register (GR07) is used to affect the result. This register is active only if the Graphics Mode register (GR05) is set to Read Mode 1. A match between the memory data and the Color Compare register (GR02) (for the bits specified in the Color Don't Care register) causes a logical 1 to be placed on the CPU data bus for the corresponding data bit, a mis-match returns a logical 0.

7-4 Reserved (0)

DATA ROTATE REGISTER (GR03)

Read/Write at I/O Address 3CFh
Index 03h
Group 1 Protection



2-0 These bits specify the number of bits to rotate to the right the data being written by the CPU. The CPU data bits are first rotated, then subjected to the logical operation as specified in the Function Select bit field. The rotate function is active only if the Graphics Mode register is programmed for Write Mode 0.

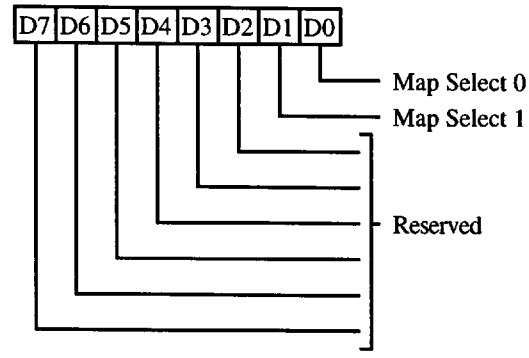
4-3 These Function Select bits specify the logical function performed on the contents of the processor latches (loaded on a previous CPU read cycle) before the data is written to display memory. These bits operate as follows:

Bit 4	Bit 3	Result
0	0	No change to the Data, Latches are updated;
0	1	Logical 'AND' between Data and latched data;
1	0	Logical 'OR' between Data and latched data;
1	1	Logical 'XOR' between Data and latched data.

7-5 Reserved (0)

READ MAP SELECT REGISTER (GR04)

Read/Write at I/O Address 3CFh
Index 04h
Group 1 Protection



1-0 This register is also used to 'reduce' 32 bits of memory data to 8 bits for the CPU in the 4-plane graphics mode. These bits select the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even mode, bit-0 is ignored. In Quad mode, bits 0 and 1 are both ignored.

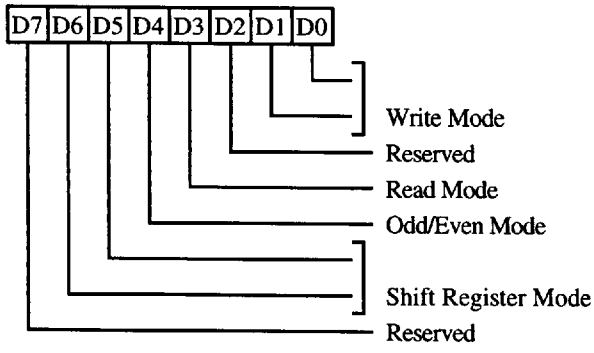
The four memory maps are selected as follows:

Bit 1	Bit 0	Map Selected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

7-2 Reserved (0)

GRAPHICS MODE REGISTER (GR05)

Read/Write at I/O Address 3CFh
Index 05h
Group 1 Protection



1-0 These bits specify the Write Mode as follows: (For 16-bit writes, the operation is repeated on the lower and upper bytes of CPU data).

1	0	Write Mode
0	0	**Write mode 0.** Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.
0	1	**Write mode 1.** Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.
1	0	**Write mode 2.** The CPU data bus data is treated as the color value for the addressed byte in planes 0-3. All eight pixels in the addressed byte are modified unless protected by the Bit Mask register setting. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset and Enable Set/Reset registers are ignored. The Function Select bits in the Data Rotate register are used.
1	1	**Write mode 3.** The CPU data is rotated then logically added with the contents of the Bit Mask register (GR08) and then treated as the addressed data's bit mask, while the contents of the Set/Reset register is treated as the color value. A '0' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the corresponding pixel in the processor latches. A '1' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the color value specified in the Set/Reset register. The Enable Set/Reset register is ignored. The Data Rotate is used. This write mode can be used to fill an area with a single color and pattern.

2 Reserved (0)

3 This bit specifies the Read Mode as follows:

0 The CPU reads data from one of the planes as selected in the Read Map Select register.

1 The CPU reads the 8-bit result of the logical comparison between all eight pixels in the four display planes and the contents of the Color Compare and Color Don't Care registers. The CPU reads a logical 1 if a match occurs for each pixel and logical 0 if a mis-match occurs. In 16-bit read cycles, this operation is repeated on the lower and upper bytes.

(Continued on following page)

4 Odd/Even Mode

0 All CPU addresses sequentially access all planes
1 Even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for IBM CGA-compatible memory organization.

6-5 Shift Register Mode. These two bits select the data shift pattern used when passing data from the four memory planes through the four video shift registers. If the data bits in the memory planes (0-3) are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7 respectively, then the data in the serial shift registers is shifted out as follows:

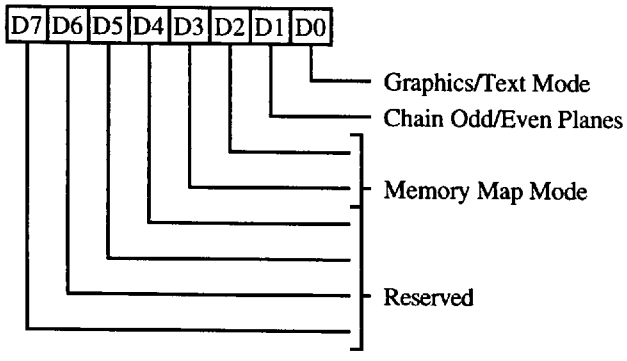
65	Last Bit Shifted Out			Shift Direction →				1st Bit Shifted Out	Output to:
00	M0D0	M0D1	M0D2	M0D3	M0D4	M0D5	M0D6	M0D7	Bit0
	M1D0	M1D1	M1D2	M1D3	M1D4	M1D5	M1D6	M1D7	Bit1
	M2D0	M2D1	M2D2	M2D3	M2D4	M2D5	M2D6	M2D7	Bit2
	M3D0	M3D1	M3D2	M3D3	M3D4	M3D5	M3D6	M3D7	Bit3
01	M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	Bit0
	M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	Bit1
	M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	Bit2
	M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	Bit3
1x	M3D0	M3D4	M2D0	M2D4	M1D0	M1D4	M0D0	M0D4	Bit0
	M3D1	M3D5	M2D1	M2D5	M1D1	M1D5	M0D1	M0D5	Bit1
	M3D2	M2D6	M3D2	M2D6	M1D2	M1D6	M0D2	M0D6	Bit2
	M3D3	M3D7	M2D3	M2D7	M1D3	M1D7	M0D3	M0D7	Bit3

Note: If the Shift Register is not loaded every character clock (see SR01 bits 2&4) then the four 8-bit shift registers are effectively 'chained' with the output of shift register 1 becoming the input to shift register 0 and so on. This allows one to have a large monochrome (or 4 color) bit map and display one portion thereof.

7 Reserved (0)

MISCELLANEOUS REGISTER (GR06)

Read/Write at I/O Address 3CFh
Index 06h
Group 1 Protection



0 Graphics/Text Mode

- 0 Text Mode
- 1 Graphics mode

1 Chain Odd/Even Planes. This mode can be used to double the address space into display memory.

- 1 CPU address bit A0 is replaced by a higher order address bit. The state of A0 determines which memory plane is to be selected:
  A0 = 0 select planes 0 and 2
  A0 = 1 select planes 1 and 3
- 0 A0 not replaced

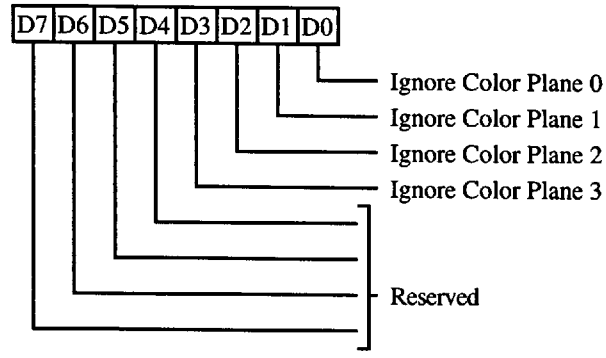
3-2 Memory Map mode. These bits control the mapping of the display memory into the CPU address space as follows (also used in extended modes):

Bit 3	Bit 2	CPU Address
0	0	A0000h-BFFFFh
0	1	A0000h-AFFFFh
1	0	B0000h-B7FFFh
1	1	B8000h-BFFFFh

7-4 Reserved (0)

COLOR DON'T CARE REGISTER (GR07)

Read/Write at I/O Address 3CFh
Index 07h
Group 1 Protection



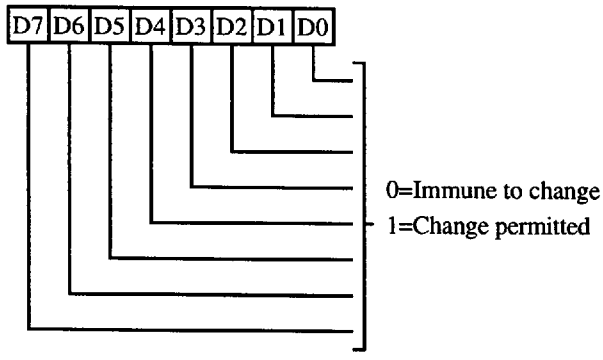
3-0 Ignore Color Plane (0-3)

- 0 This causes the corresponding bit of the Color Compare register to be a don't care during a comparison.
- 1 The corresponding bit of the Color Compare register is enabled for color comparison. This register is active in Read Mode 1 only.

7-4 Reserved (0)

BIT MASK REGISTER (GR08)

Read/Write at I/O Address 3CFh
Index 08h
Group 1 Protection



7-0 This bit mask is applicable to any data written by the CPU, including that subject to a rotate, logical function (AND, OR, XOR), Set/Reset, and No Change. In order to execute a proper read-modify-write cycle into displayed memory, each byte must first be read (and latched by the VGA), the Bit Mask register set, and the new data then written. The bit mask applies to all four planes simultaneously.

0 The corresponding bit in each of the four memory planes is written from the corresponding bit in the latches.

1 Unrestricted manipulation of the corresponding data bit in each of the four memory planes is permitted.

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82C453 Attribute Controller and Color Palette Registers

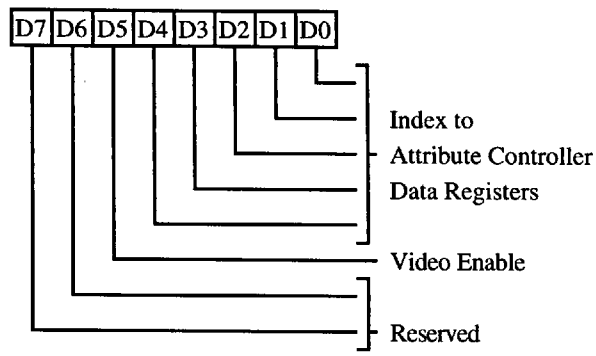
Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ARX	Attribute Index (for 3C0/3C1h)	–	RW	3C0h	1	65
AR00-AR0F	Internal Color Palette Data	00-0Fh	RW	3C0h/3C1h	1	66
AR10	Mode Control	10h	RW	3C0h/3C1h	1	66
AR11	Overscan Color	11h	RW	3C0h/3C1h	1	67
AR12	Color Plane Enable	12h	RW	3C0h/3C1h	1	67
AR13	Horizontal Pixel Panning	13h	RW	3C0h/3C1h	1	68
AR14	Pixel Pad	14h	RW	3C0h/3C1h	1	68
DACMASK	External Color Palette Pixel Mask	–	RW	3C6h	6	69
DACSTATE	DAC State	–	R	3C7h	–	69
DACRX	External Color Palette Read-Mode Index	–	W	3C7h	6	70
DACX	External Color Palette Index (for 3C9h)	–	RW	3C8h	6	70
DACDATA	External Color Palette Data	00-FFh	RW	3C9h	6	70

In regular VGA mode, all Attribute Controller registers are located at the same byte address (3C0h) in the CPU I/O space. An internal flip-flop controls the selection of either the Attribute Index or Data Registers. To select the Index Register, an I/O Read is executed to address 3BAh/3DAh to clear this flip-flop. After the Index Register has been loaded by an I/O Write to address 3C0h, this flip-flop toggles, and the Data Register is ready to be accessed. Every I/O Write to address 3C0h toggles this flip-flop. The flip-flop does not have any effect on the reading of the Attribute Controller registers. The Attribute Controller index register is always read back at address 3C0h, the data register is always read back at address 3C1h.

In one of the extended modes (See "CPU Interface Register"), the Attribute Controller Index register is located at address 3C0h and the Attribute Controller Data register is located at address 3C1h (to allow word I/O accesses). In another extended mode, the Attribute Controller can be both read and written at either 3C0h or 3C1h (EGA compatible mode).

ATTRIBUTE INDEX REGISTER (ARX)

Read/Write at I/O Address 3C0h
Group 1 Protection



4-0 These bits point to one of the internal registers of the Attribute Controller

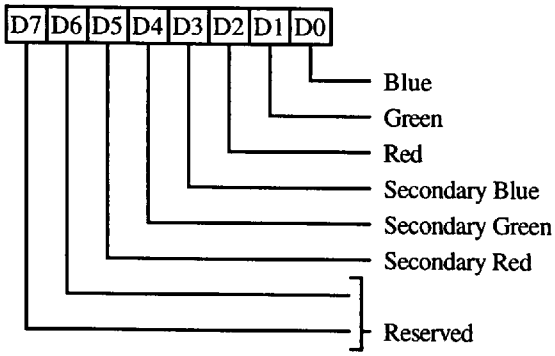
5 Enable Video:

- 0 Disables the video, allowing the Attribute Controller color registers to be accessed by the CPU
- 1 Enables the video and causes the Attribute Controller Color registers (AR00-AR0F) to be inaccessible by the CPU

7-6 Reserved (0)

ATTRIBUTE CONTROLLER COLOR PALETTE DATA REGISTERS (AR00-AR0F)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 00-0Fh
Group 1 Protection or XR63 D6

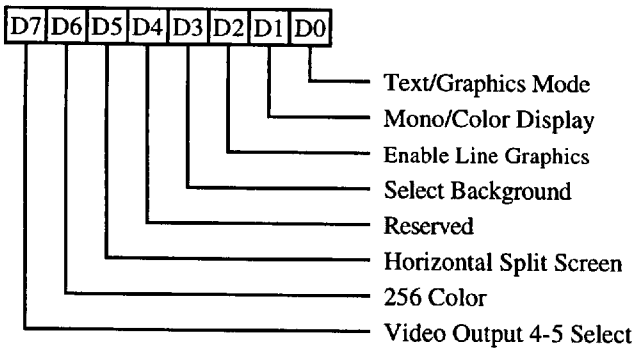


5-0 These bits are the color value in the respective palette register as pointed to by the index register.

7-6 Reserved (0)

ATTRIBUTE CONTROLLER MODE CONTROL REGISTER (AR10)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 10h
Group 1 Protection



0 Text/Graphics Mode
- 0 Select text mode
- 1 Select graphics mode

1 Monochrome/Color Display
- 0 Select color display attributes
- 1 Select mono display attributes

2 Enable Line Graphics Character Codes. This bit is dependent on bit 0 of the Override register.
- 0 Make the ninth pixel appear the same as the background
- 1 For special line graphics character codes (0C0h-0DFh), make the ninth pixel identical to the eighth pixel of the character. For other characters, the ninth pixel is the same as the background.

3 Enable Blink/Select Background Intensity. The blinking counter is clocked by the VSYNC signal.
- 0 Disable Blinking and enable text mode background intensity
- 1 Enable the blink attribute in text and graphics modes.

4 Reserved (0)

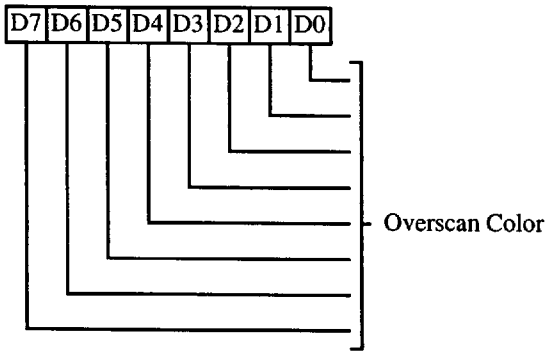
5 Split Screen Horizontal Panning Mode
- 0 Scroll both screens horizontally as specified in the Pixel Panning register
- 1 Scroll horizontally only the top screen as specified in the Pixel panning register

6 256 Color Output Assembler
- 0 6-bits of video (translated from 4-bits by the internal color palette) are output every dot clock
- 1 Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot clock (256 color mode).

7 Video Output 5-4 Select
- 0 Video bits 4 and 5 are generated by the internal Attribute Controller color palette registers
- 1 Video bits 4 and 5 are the same as bits 0 and 1 in the Pixel Pad register (AR14)

OVERSCAN COLOR REGISTER (AR11)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 11H
Group 1 Protection

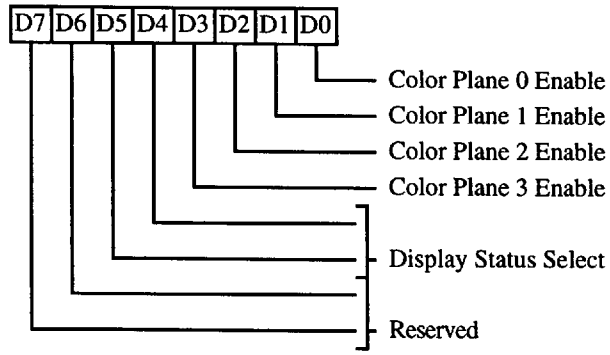


7-0 Overscan Color. These 8 bits define the overscan (border) color value. For monochrome displays, these bits should be zero.

The border color is displayed in the interval after Display Enable End and before Blank Start (end of display area; i.e. right side and bottom of screen) and between Blank End and Display Enable Start (beginning of display area; i.e. left side and top of screen).

COLOR PLANE ENABLE REGISTER (AR12)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 12h
Group 1 Protection



3-0 Color Plane (0-3) Enable

0 Force the corresponding color plane pixel bit to 0 before it addresses the color palette

1 Enable the plane data bit of the corresponding color plane to pass

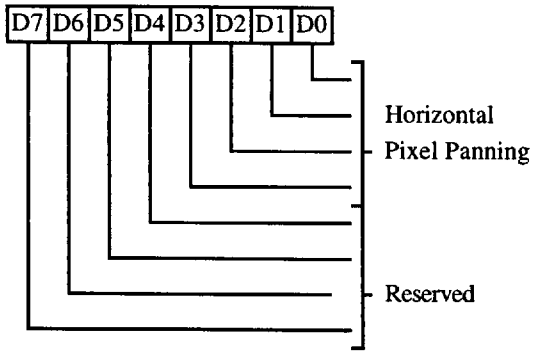
5-4 Display Status Select. Select two of the eight color outputs to be read back in the Input Status Register 1 (port 3BAh or 3DAh). The output color combinations available on the status bits are as follows:

		Status Register 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

7-6 Reserved (0)

ATTRIBUTE CONTROLLER HORIZONTAL PIXEL PANNING REGISTER (AR13)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 13h
Group 1 Protection



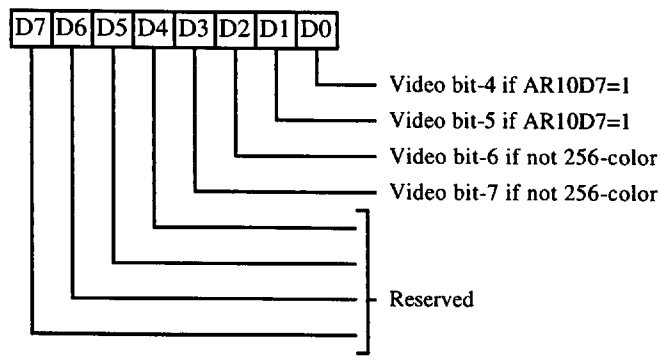
3-0 Horizontal Pixel Panning. These bits select the number of pixels to shift the display horizontally to the left. Pixel panning is available in both text and graphics modes. In 9 pixels/character text mode, the output can be shifted a maximum of 9 pixels. In 8 pixels/character text mode and all graphics modes a maximum shift of 8 pixels is possible. In 256-color mode (output assembler AR10 bit 6 = 1), bit 0 of this register must be 0 which results in only 4 panning positions per display byte. In Shift Load 2 and Shift Load 4 modes, register CR08 provides single pixel resolution for panning. Panning is controlled as follows:

	Number of Pixels Shifted		
AR13	**9-dot mode**	**8-dot mode**	**256-color mode**
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7-4 Reserved (0)

ATTRIBUTE CONTROLLER PIXEL PAD REGISTER (AR14)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 14h
Group 1 Protection



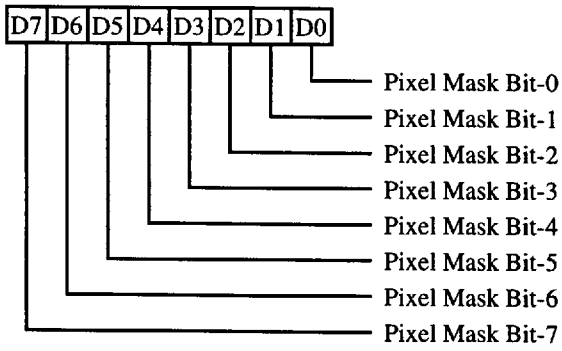
1-0 These bits are output as video bits 5 and 4 when AR10 bit 7 = 1. They are disabled in 256 color mode.

3-2 These bits are output as video bits 7 and 6 in all modes except 256-color mode.

7-4 Reserved (0)

EXTERNAL COLOR PALETTE PIXEL MASK REGISTER (DACMASK)

Read/Write at I/O Address 3C6h
Group 6 Protection

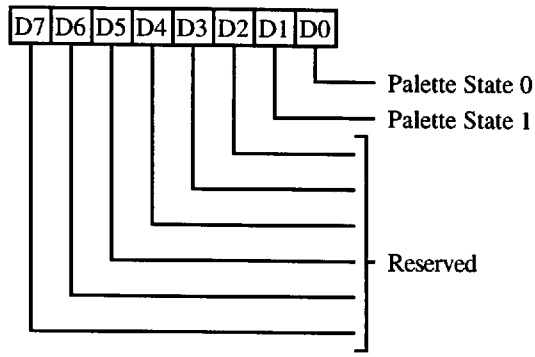


The contents of this register are logically ANDed with the 8 bits of video data coming into the external color palette. Zero bits in this register therefore cause the corresponding address input to the external color palette to be zero. For example, if this register is programmed with 7, only external color palette registers 0-7 would be accessible; video output bits 3-7 would be ignored and all color values would map into the lower 8 locations in the color palette.

This register is physically located in the external color palette chip (used for displaying analog data to the CRT). Reads from this I/O location cause the PALRD/ pin to be asserted. Writes to this I/O location cause the PALWR/ pin to be asserted. The functionality of this port is determined by the external palette chip.

EXTERNAL COLOR PALETTE STATE REGISTER (DACSTATE)

Read only at I/O Address 3C7h



1-0 Status bits indicate the I/O address of the last CPU write to the external DAC/Color Palette:

- 00 The last write was to 3C8h (write mode)
- 11 The last write was to 3C7h (read mode)

7-2 Reserved (0)

To allow saving and restoring the state of the video subsystem, this register is required since the external color palette chip automatically increments its index register differently depending on whether the index is written at 3C7h or 3C8h.

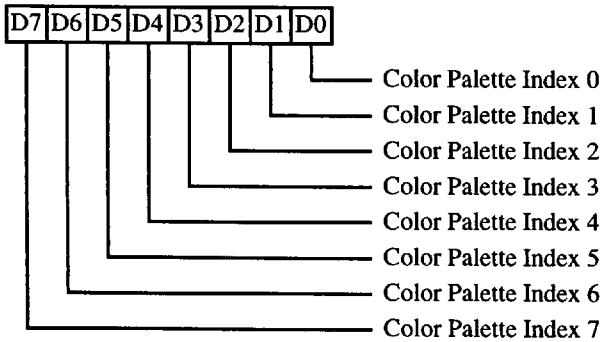
This register is physically located in the 82C453 chip (PALRD/ is *not* asserted for reads from this I/O address).

EXTERNAL COLOR PALETTE READ-MODE INDEX REGISTER (DACRX)

Write only at I/O Address 3C7h
Group 6 Protection

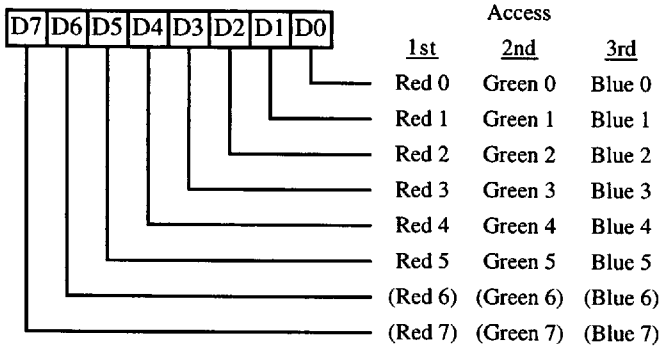
EXTERNAL COLOR PALETTE INDEX REGISTER (DACX)

Read/Write at I/O Address 3C8h
Group 6 Protection



EXTERNAL COLOR PALETTE DATA REGISTERS (DACDATA 00-FF)

Read/Write at I/O Address 3C9h
Index 00h-FFh
Group 6 Protection



The color palette index and data registers are physically located in the external color palette chip. The index register is used to point to one of 256 data registers. Each data register is either 18 or 24 bits in length depending on the type of palette chip used (6 or 8 bits each for red, green, and blue), so the data values must be read as a sequence of 3 bytes. After writing the index register (3C7h or 3C8h), data values may be read from or written to the color palette data register port (3C9h) in sequence: first red, then green, then blue, then repeat for the next location if desired (the index is incremented automatically by the palette chip).

The index may be written at 3C7h and may be read or written at 3C8h. When the index value is written to either port, it is written to both the index register and a 'save' register internal to the color palette chip. The save register (not the index register) is used internally by the palette chip to point at the current data register. When the index value is written to 3C7h (**read mode**), it is written to both the index register and the save register, then the index register is automaticallyincremented. When the index value is written to 3C8h (**write mode**), the automatic incrementing of the index register does not occur.

After the third of the three sequential data reads from (or writes to) 3C9h is completed, the save and index registers are both automatically incremented by the palette chip. This allows the entire palette (or any subset) to be read (written) by writing the index of the first color in the set, then sequentially reading (writing) the values for each color, without having to reload the index every three bytes.

The state of the RGB sequence is not saved; the user must access each three bytes in an un-interruptable sequence (or be assured that interrupt service routines will not access the palette index or data registers). When the index register is written (at either port), the RGB sequence is restarted. Data value reads and writes may be intermixed; either reads or writes increment the palette chip internal RGB sequence counter.

The palette chip internal save register always contains a value one less than the readable index value if the last index write was to the 'read mode' port. The 82C453 therefore saves the state of which port (3C7h or 3C8h) was last written and returns that information on reads from 3C7h (PALRD/ is only asserted on reads from 3C8h and not on reads from 3C7h). Writes to 3C7h or 3C8h cause the PALWR/ pin to be asserted.

The functionality of the index and data ports is determined by the external palette chip.

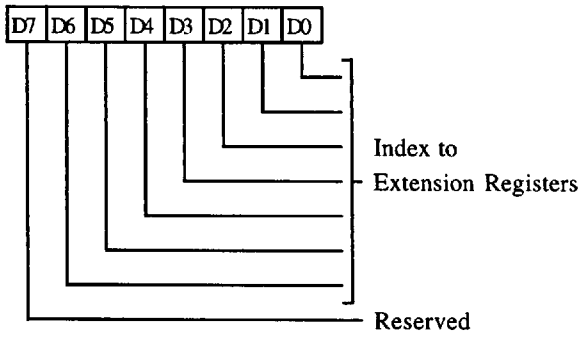
82C453 Extension Registers

Register Mnemonic	Register Group	Register Name	Index	I/O Access	Address	State After Reset	Page
XRX	–	Extension Index	–	RW	3B6h / 3D6h	-xxxxxxx	72
XR00	Misc	Chip Version	00h	R	3B7h / 3D7h	0011rrrr	72
XR01	Misc	DIP Switch	01h	R	3B7h / 3D7h	-----ddd	72
XR02	Misc	CPU Interface	02h	RW	3B7h / 3D7h	00000000	73
XR03	Misc	Interface Register I	03h	RW	3B7h / 3D7h	00--00-0	74
XR05	Misc	Sequencer Control	05h	RW	3B7h / 3D7h	0000---0	75
XR20	Misc	Interface Register II	20h	RW	3B7h / 3D7h	----0-0-	83
XR23	Misc	Write Bit Mask Control	23h	RW	3B7h / 3D7h	----0xx0	84
XR24	Misc	Write Bit Mask Pattern	24h	RW	3B7h / 3D7h	xxxxxxxx	84
XR25	Misc	Define Pins	25h	RW	3B7h / 3D7h	-----0x0	85
XR26	Misc	Configuration	26h	RW	3B7h / 3D7h	-----000	85
XR7F	Misc	Diagnostic	7Fh	RW	3B7h / 3D7h	------00	88
XR0B	Mapping	CPU Paging	0Bh	RW	3B7h / 3D7h	-----000	76
XR0C	Mapping	Start Address Top	0Ch	RW	3B7h / 3D7h	------00	76
XR10	Mapping	Single/Low Map	10h	RW	3B7h / 3D7h	xxxxxxxx	77
XR11	Mapping	High Map	11h	RW	3B7h / 3D7h	xxxxxxxx	77
XR14	Compatibility	Emulation Mode	14h	RW	3B7h / 3D7h	0000hh00	78
XR15	Compatibility	Write Protect	15h	RW	3B7h / 3D7h	-0000000	79
XR16	Compatibility	Trap Enable	16h	RW	3B7h / 3D7h	--000000	80
XR17	Compatibility	Trap Status	17h	RW	3B7h / 3D7h	--000000	80
XR7E	Compatibility	CGA Color Select	7Eh	RW	3B7h / 3D7h	--xxxxxx	87
XR0D	Alternate	Auxiliary Offset	0Dh	RW	3B7h / 3D7h	------00	76
XR18	Alternate	Alternate H Display End	18h	RW	3B7h / 3D7h	xxxxxxxx	81
XR19	Alternate	Alternate H Sync Start	19h	RW	3B7h / 3D7h	xxxxxxxx	81
XR1A	Alternate	Alternate H Sync End	1Ah	RW	3B7h / 3D7h	xxxxxxxx	81
XR1B	Alternate	Alternate H Total	1Bh	RW	3B7h / 3D7h	xxxxxxxx	81
XR1C	Alternate	Alternate H Blank Start	1Ch	RW	3B7h / 3D7h	xxxxxxxx	82
XR1D	Alternate	Alternate H Blank End	1Dh	RW	3B7h / 3D7h	0xxxxxxx	82
XR1E	Alternate	Alternate Offset	1Eh	RW	3B7h / 3D7h	xxxxxxxx	82
XR28	General	Video Interface	28h	RW	3B7h / 3D7h	--000-10	86
XR29	General	Half Line Compare	29h	RW	3B7h / 3D7h	xxxxxxxx	86
XR41	General	EGA Switch	41h	RW	3B7h / 3D7h	0---0000	87
XR44	General	Video Flags	44h	RW	3B7h / 3D7h	00000000	87
XR45	General	Scratch Register 1 / ForeGround Color	45h	RW	3B7h / 3D7h	00000000	87

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
– = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
0/1 = Reset to 0/1 by falling edge of RESET

EXTENSION INDEX REGISTER (XRX)

Read/Write at I/O Address 3B6h/3D6h
Index Xh

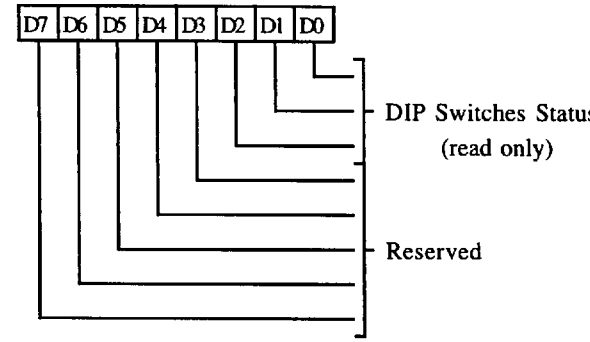


6-0 Index value used to access the extension registers

7 Reserved (0)

DIP SWITCH REGISTER (XR01)

Read only at I/O Address 3B7h/3D7h
Index 01h



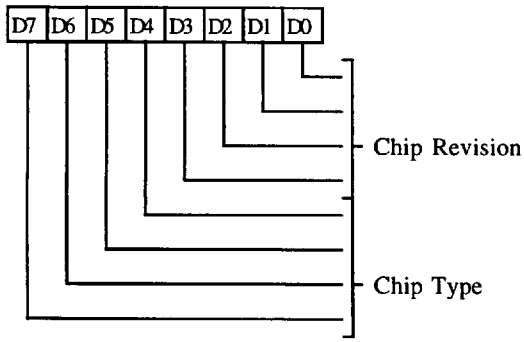
2-0 These bits give the state of the DIP switches which are multiplexed on pins A16-SW2, BHE/-SW1 and AEN-SW0.

7-3 Reserved (0)

This register is not related to the EGA Dip Switches.

CHIP VERSION REGISTER (XR00)

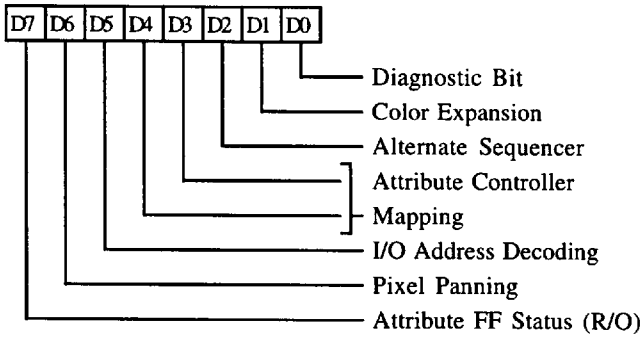
Read only at I/O Address 3B7h/3D7h
Index 00h



7-0 This register contains the version number for the 82C453. Values start at 30h and are incremented for every silicon step.

CPU INTERFACE REGISTER (XR02)

Read/Write at I/O Address 3B7h/3D7h
Index 02h



0 Diagnostic Bit. This bit is defined for test purposes only. This bit should be set to '0' for normal operation.

1 Packed Pixel Color Expansion

- 0 Select CPU rotated byte into Graphics Controller(default on Reset)
- 1 Select Scratch / Foreground Color Register (XR45) into Graphics Controller for Packed Pixel Color Expansion in packed pixel mode.

2 Alternate Sequencer Timing

- 0 Use normal RAS/CAS timing (7 clock cycles to one memory cycle).
- 1 Use alternate RAS/CAS timing (6 clock cycles to one memory cycle). Alternate timing should be used only when the sequencer clock is 25 MHz or below. This bit should be set when running 1024x768 interlaced mode for higher performance.

4-3 Attribute Controller Mapping

- 00 Write Index at 3C0h and Data at 3C0h (8-bit access only). (Default on Reset; VGA type mapping).
- 01 Write Index at 3C0h and Data at 3C1h (8 or 16-bit access), the attribute flip-flop is always reset in this mode (16-bit mapping)
- 10 Write Index and Data at 3C0h/3C1h (8-bit access only EGA type mapping).
- 11 Reserved (0)

5 I/O Address Decoding. This bit affects 3B4/5h, 3D4/5h, 3C0-2h, 3C4/5h, 3CE/Fh, 3BAh, 3BFh and 3D8h.

- 0 Decode all 16 bits of I/O address (Default on Reset)
- 1 Decode only the lower 10 bits.

6 Pixel Panning

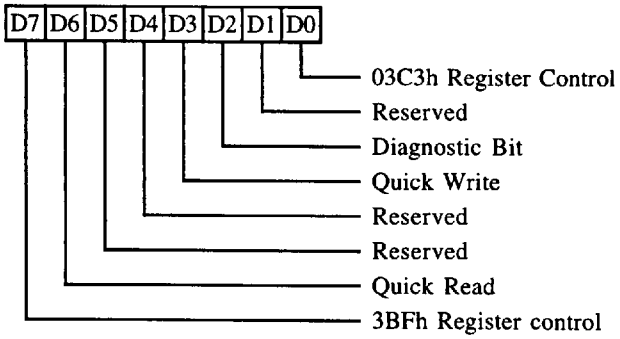
- 0 Use bits 1-0 of the Horizontal Pixel Panning Register (AR13) to control the Pixel Panning logic in the 8-bit video path.
- 1 Use bits 2-1 bits of the Horizontal Pixel Panning Register (AR13) to control the Pixel Panning logic in the 8-bit video path.

7 Attribute Flip-flop Status (read only)

- 0 Index
- 1 Data

INTERFACE REGISTER I (XR03)

Read/Write at I/O Address 3B7h/3D7h
Index 03h



0 3C3H Register Control. This bit is valid in MC interface only.

- 0 Write only access to 3C3H register on chip. Default on reset.
- 1 Allow both Read/Write access to 3C3h register on the chip.

1 Reserved

2 Diagnostic Bit. This bit is defined for test purposes only. This bit should be set to '0' for normal operation.

3 Quick Write

- 0 Normal CPU write cycle timing, default on reset.
- 1 Enable quick write feature on CPU write cycles. 82C453 completes a CPU Write Cycle quicker than a normal cycle by releasing Ready earlier. This feature should not be enabled when the dot clock is below 20 MHz.

4 Reserved (0)

5 Reserved (0)

6 Quick Read

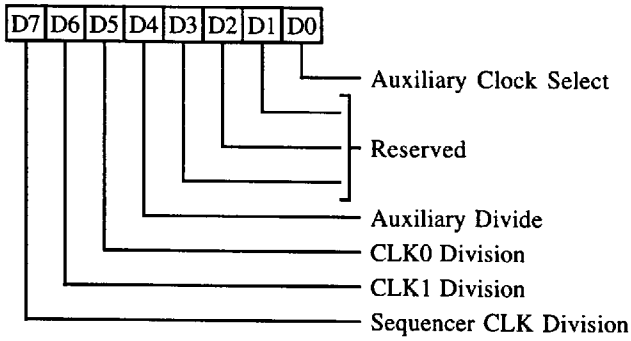
- 0 Normal CPU Read Cycle timing. Default on Reset.
- 1 Enable quick read feature on CPU write cycles. 82C453 completes a CPU Read Cycle quicker than a normal cycle by releasing ready (RDY) earlier. This feature should not be enabled when the dot clock is below 20 MHz.

7 3BFh Register Control

- 0 Disable reads to register 3BFH, default on reset
- 1 Enable reads to register 3BFh

SEQUENCER CONTROL REGISTER (XR05)

Read/Write at I/O Address 3B7h/3D7h
Index 05h



0 Auxiliary Clock Select

- 0 Select one of CLK0, CLK1/S0, CLK2/S1 as defined by the Misc. output register to be the display clock. Default on reset.
- 1 Redefine CLK0 as a common clock input and make CLK1/S0 and CLK2/S1 outputs to control an external clock select MUX. When this bit (0) is set to '1' CLK1/S0 and CLK2/S1 pins are driven by the Misc. Output Register bits 2 and 3.

3-1 Reserved

4 Auxiliary Divide. Divides the Display Clock selected by the Miscellaneous Output Register and bit 0 of this register by 2 or 3 before being used internally. The additional divide by two in the sequencer is still effective (SR1 bit 3).

- 0 Divide by 2
- 1 Divide by 3

5 CLK0 Division. This bit controls the division operation on CLK0 as specified bit 4 of this register.

- 0 No division on CLK0
- 1 Divide CLK0 as specified by bit 4 of this register

6 CLK1 division. This bit controls the division operation on CLK1 as specified by bit 4 of this register.

- 0 No division on CLK1
- 1 Divide CLK1 as specified by bit 4 of this register. When CLK0 is selected as common input, CLK1/S0 becomes an output. During this condition, bit 6 has no effect and when bit 5 is '1' all incoming clocks will be divided by 2 or 3 depending on the value of bit 4 of this register.

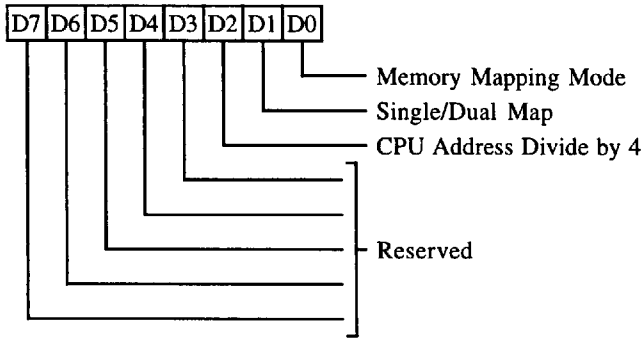
7 Sequencer Clock Division

- 0 Sequencer Clock same as video Clock, default on reset.
- 1 Sequencer Clock is video clock divided by two. This bit should be set for all video modes that use clock higher than 32 MHz for 120nS VRAM and higher than 36 MHz for 100 nS VRAM.

Note: Sequencer clock is used to derive the internal timing of the chip and memory timing.

CPU PAGING REGISTER (XR0B)

Read/Write at I/O Address 3B7h/3D7h
Index 0Bh



0 Memory Mapping Mode

- 0 Normal Mode (VGA Compatible).
- 1 Extended Mode, mapping for 512 KBytes or 1 MByte memory configuration.

1 Single/Dual Map

- 0 CPU uses only Low Map Register to translate the CPU addresses to access the extended video memory space.
- 1 CPU uses both the Low Map and High Map registers to translate the CPU addresses to access the extended video memory space.

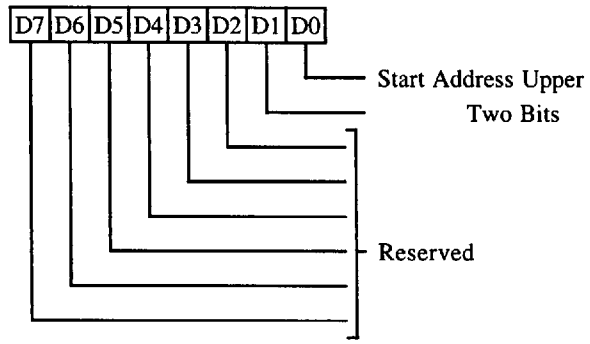
2 CPU Address Divide by 4

- 0 Disable CPU address divide by 4, normal mode.
- 1 Enable divide by 4 for CPU Addresses. This allows the video memory to be accessed sequentially in mode 13. Also all of the memory is available in mode 13 by setting this bit. Bit 0 of this register should be '1' for this bit to be effective.

7-3 Reserved (0)

START ADDRESS TOP (XR0C)

Read/Write at I/O Address 3B7h/3D7h
Index 0Ch

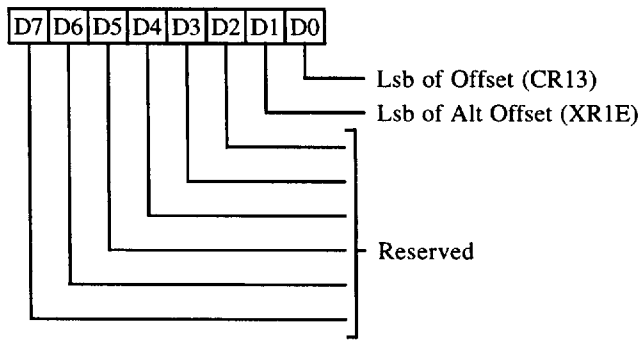


1-0 Start Address Upper two bits. Defines the 1 or 2 high order bits for the Display Start Address when 512 KB or 1 MB of memory is used. (Also see XR20 bit 1)

7-2 Reserved (0)

AUXILIARY OFFSET REGISTER (XR0D)

Read/Write at I/O Address 3B7h/3D7h
Index 0Dh



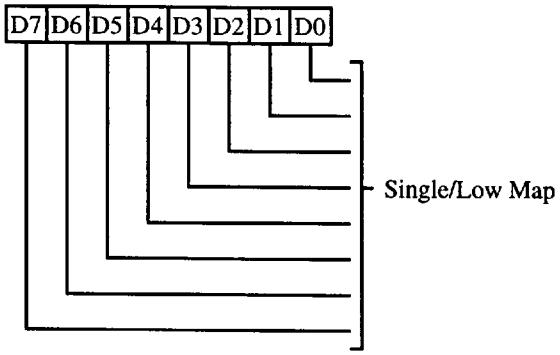
0 This bit provides finer granularity to the Offset when the chain (odd/even) and chain 4 modes are used. This bit is used with the regular offset register (CR13).

1 This bit provides finer granularity to the Offset when the chain Odd/Even and chain 4 modes are used. This bit is used with the alternate offset register (I/0 address 3D7h pointer 1Eh).

7-2 Reserved (0)

SINGLE/LOW MAP REGISTER (XR10)

Read/Write at I/O Address 3B7h/3D7h
Index 10h



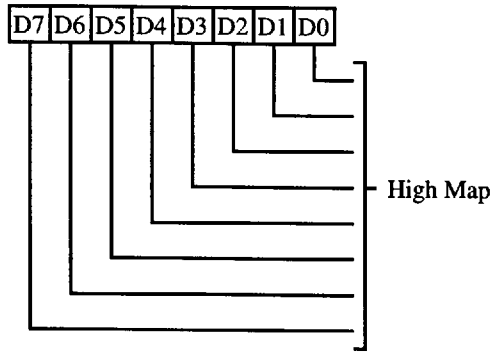
7-0 These eight bits define the Single or Lower Map (In dual map mode) base address bits 17-10 in planar modes and bits 19-12 in packed pixel modes. The map starts on 1K boundary for planar modes and 4K boundary for packed pixel modes. In case of Dual mapping this register controls the CPU window into the display memory based on the contents of GR6 as follows:

GR6	Low Map
0	0A0000-0Affffh
1	0A0000-0A7fffh
2	0B0000-0Bffffh
3	0B0000-0Bffffh

Note: Dual mapping is not allowed in the last two cases. In the last two instances the CPU uses single mapping.

HIGH MAP REGISTER (XR11)

Read/Write at I/O Address 3B7h/3D7h
Index 11h

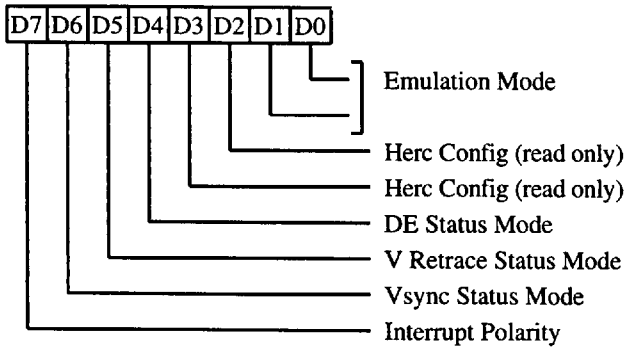


7-0 These eight bits define the Higher Map (In Dual Map Mode) base address bits 17-10 in planar modes and bits 19-12 in packed pixel modes. The Map starts on 1K boundary for planar modes and 4K boundary for packed pixel modes. This register maps the CPU window into display memory as follows:

GR6	High Map
0	0B0000-0Bffffh
1	0A8000-0Affffh
2	Don't care
3	Don't care

EMULATION MODE REGISTER (XR14)

Read/Write at I/O Address 3B7h/3D7h
Index 14h



1-0 Emulation Mode

- 00 VGA / EGA
- 01 CGA
- 10 MDA
- 11 MDA / Hercules

3-2 Hercules Configuration Register readback (read only).

4 Display Enable Status Mode

- 0 Select Display Enable status to appear at bit 0 of Input Status register 1 (I/O Address 3xAh in CGA and VGA modes).
- 1 Select HSYNC status to appear at bit 0 of Input Status register 1 (I/O Address 3xAh in MDA and Hercules modes).

5 Vertical Retrace Status Mode

- 0 Select Vertical Retrace status to appear at bit 3 of Input Status register 1(I/O Address 3xAh in CGA and VGA modes).
- 1 Select Video to appear at bit 3 of Input Status register 1(I/O Address 3xAh in MDA and Hercules modes).

6 VSYNC Status Mode

- 0 VSYNC status not enabled on bit-7 of input status register I (port 3xA) (CGA and VGA modes)
- 1 VSYNC status enabled on bit-7 of input status register I (port 3xA) (MDA and Hercules modes)

6 VSYNC Status Mode

- 0 Enable Vsync status to appear at bit 7 of Input Status register 1 (I/O Address 3xAh in MDA and Hercules modes)
- 1 Prevent Vsync status from appearing at bit 7 of Input Status register 1 (I/O Address 3xAh in CGA and VGA modes).

7 Interrupt Output Function

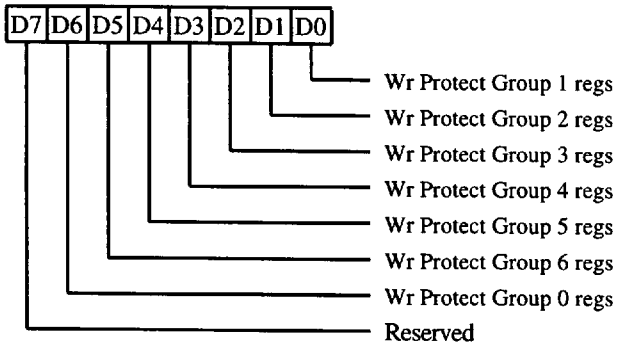
This bit controls the function of the IRQ/ output in both MC-bus and PC-bus.

Interrupt State	XR14 bit-7 = 0 PC Bus	XR14 bit-7 = 0 MC Bus	XR14 bit-7 = 1 PC Bus
Disabled	3-state	3-state	3-state
Enabled, Inactive	3-state	3-state	Low
Enabled, Active	3-state	Low	High

Note: Bit 7 should be set to '1' to enable the CRT interrupt function in the PC bus.

WRITE PROTECT REGISTER (XR15)

Read/Write at I/O Address 3B7h/3D7h
Index 15h



This register controls write protection for various groups of registers as shown. 0 = unprotected, 1= protected.

0 Write Protect Group 1 Registers:

Sequencer (SR00-SR04)
Graphics Controller (GR00-GR08)
Attribute Controller (AR00-AR14)

1 Write Protect Group 2 Registers:

Cursor Size register (CR09) bits 0-4
Character Height regs (CR0A, CR0B)

2 Write Protect Group 3 Registers:

CRT Controller CR07 bit-4
CRT Controller CR08
CRT Controller CR11 bits 4 and 5
CRT Controller CR13 and CR14
CRT Controller CR17 bits 0,1 & 3-7
CRT Controller CR18

(Split screen, smooth scroll, & CRTC Mode)

3 Write Protect Group 4 Registers:

CRT Controller CR09 bits 5-7
CRT Controller CR10
CRT Controller CR11 bits 0-3 & 6
CRT Controller CR12, CR15, CR16
CRT Controller CR17 bit-2

4 Write Protect Group 5 Registers:

Miscellaneous Output (3C2h)
Feature Control (3BA/3DAh)

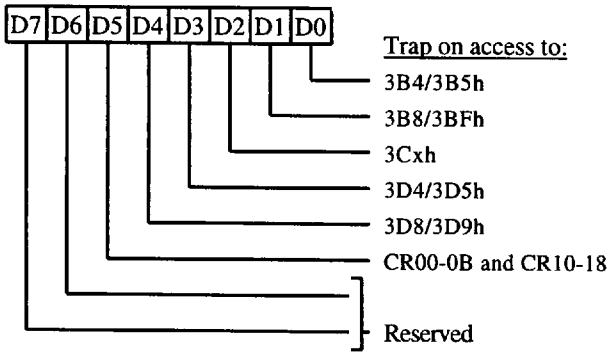
5 Write Protect Group 6. (I/O Addresses 3C6-3C9h). The PALRD/ and PALWR/ output signals are disabled and the 82C453 DAC state register is write protected.

6 Write Protect Group 0. Auxiliary Write Protect for CRT Controller registers CR00-CR07 except CR07 bit-4. This bit is logically ORed with CR11 bit-7.

7 Reserved (0)

TRAP ENABLE REGISTER (XR16)

Read/Write at I/O Address 3B7h/3D7h
Index 16h



Trap Enable bits:

0 Generate Trap on Access to I/O Addresses 3B4h or 3B5h.

1 Generate Trap on Access to I/O Addresses 3B8h or 3BFh.

2 Generate Trap on Access to I/O Addresses 3Cxh.

3 Generate Trap on Access to I/O Addresses 3D4h or 3D5h.

4 Generate Trap on Access to I/O Addresses 3D8h or 3D9h.

5 Generate Trap on Access to registers CR0B and CR10 through CR18.

7-6 Reserved (0)

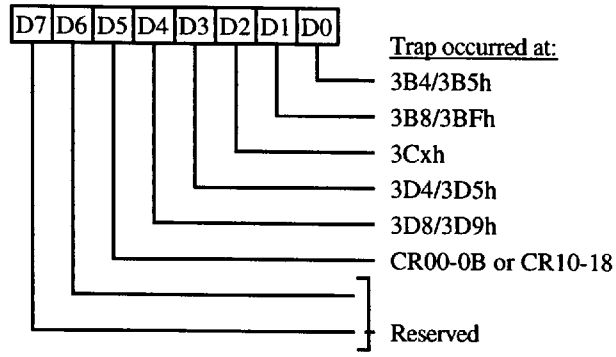
For all bits:

0 Disable trap
1 Enable trap

This register is cleared (0) on reset.

TRAP STATUS REGISTER (XR17)

Read/Clear at I/O Address 3B7h/3D7h
Index 17h



Trap Status bits:

0 Trap occurred on access to I/O Address 3B4h or 3B5h.

1 Trap occurred on access to I/O Address 3B8h or 3BFh.

2 Trap occurred on access to I/O Address 3Cxh.

3 Trap occurred on access to I/O Address 3D4h or 3D5h.

4 Trap occurred on access to I/O Address 3D8h or 3D9h.

5 Trap occurred on access to CRT Controller registers CR00 through CR0B and CR10 through CR18.

7-6 Reserved (0)

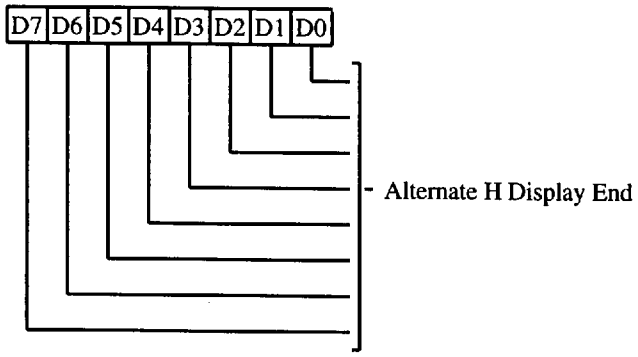
For all bits:

0 No access occurred
1 Access occurred

Note: Trap is no longer an output pin. However, Trap Status can be read in register XR17.

ALTERNATE HORIZONTAL DISPLAY END (XR18)

Read/Write at I/O Address 3B7h/3D7h
Index 18h

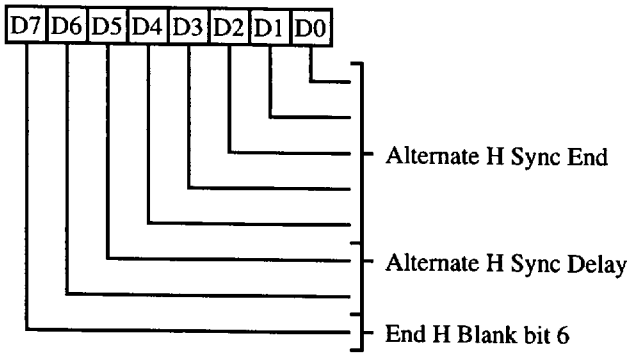


This register is used in low resolution CGA modes and Hercules graphics mode.

7-0 Alternate Horizontal Display End. See CR01 for description.

ALTERNATE HORIZONTAL SYNC END (XR1A)

Read/Write at I/O Address 3B7h/3D7h
Index 1Ah



This register is used in low resolution CGA modes and Hercules graphics mode.

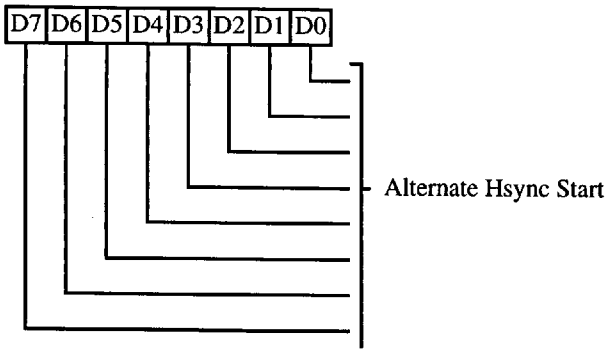
4-0 Alternate Horizontal Sync End. See CR05 for description.

6-5 Alternate Horizontal Sync Delay. See CR05 for description.

7 End Horizontal Blank bit 6. Sixth bit of the Alternate Horizontal Blanking Register.

ALTERNATE HORIZONTAL SYNC START (XR19)

Read/Write at I/O Address 3B7h/3D7h
Index 19h

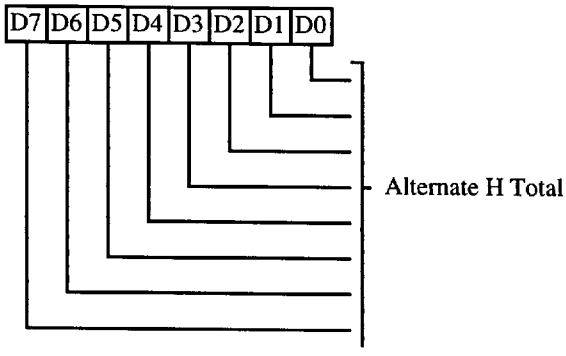


This register is used in low resolution CGA modes and Hercules graphics mode.

7-0 Alternate Horizontal Sync Start. See CR04 for description.

ALTERNATE HORIZONTAL TOTAL (XR1B)

Read/Write at I/O Address 3B7h/3D7h
Index 1Bh

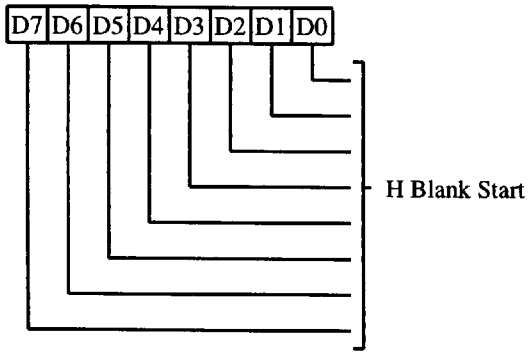


This register is used in low resolution CGA modes and Hercules graphics mode.

7-0 Alternate Horizontal Total. See CR00 for description.

ALTERNATE HORIZONTAL BLANK START (XR1C)

Read/Write at I/O Address 3B7h/3D7h
Index 1Ch

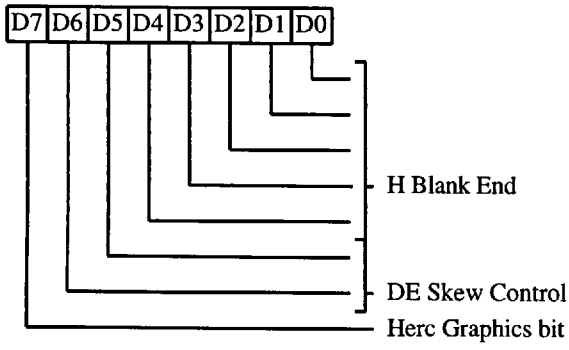


This register is used in low resolution CGA modes and Hercules graphics mode.

7-0 Alternate Horizontal Blank Start. See CR02 for description.

ALTERNATE HORIZONTAL BLANK END (XR1D)

Read/Write at I/O Address 3B7h/3D7h
Index 1Dh



This register is used in low resolution CGA modes and Hercules graphics mode.

4-0 Alternate Horizontal Blank End. See CR03 for description.

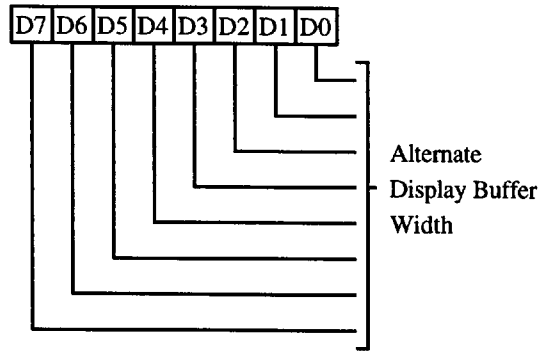
6-5 Display Enable Skew Control. See CR03 for description.

7 Hercules Graphics

0 For IBM VGA compatible operation
1 Enhances split screen functionality. Also this bit should be '1' for Hercules Graphics mode (720x348 line mode).

ALTERNATE OFFSET (XR1E)

Read/Write at I/O Address 3B7h/3D7h
Index 1Eh

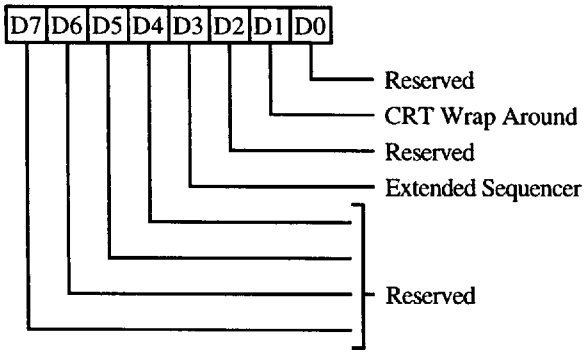


This register is used in low resolution CGA modes and Hercules graphics mode.

7-0 Alternate Offset. See CR13 for description.

INTERFACE REGISTER II (XR20)

Read/Write at I/O Address 3B7h/3D7h
Index 20h



0 Reserved (0)

1 CRT Wrap Around

- 0 82C453 will wrap around CRT addresses at 64K boundary for VGA compatibilty regardless of the memory on the board.
- 1 82C453 generates addresses for the entire memory on the board. This bit should be set for extended modes which use more than 256 Kbytes of display memory.

2 Reserved (0)

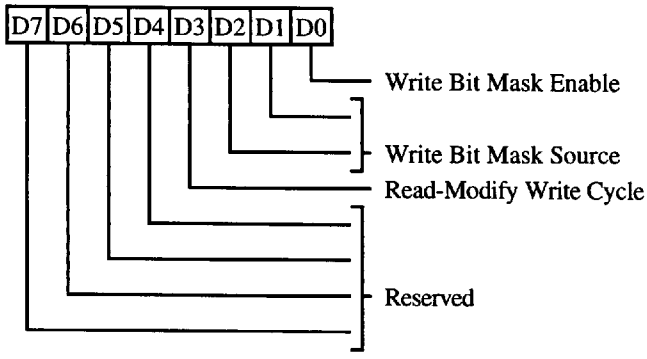
3 Extended Sequencer. This bit controls the Sequencer timing for extended modes.

- 0 This bit is set to '0' for normal VGA modes. Default on Reset.
- 1 This bit should be set for extended modes.

7-4 Reserved (0)

WRITE BIT MASK CONTROL REGISTER (XR23)

Read/Write at I/O Address 3B7h/3D7h
Index 23h



0 Write Bit Mask (WBM) Enable

- 0 Disable Write Bit Mask function (default on reset)
- 1 Enable Write Bit Mask function

2-1 Write Bit Mask Source; These two bits select the source of the Write Bit Mask pattern when the Write Bit Mask feature is enabled.

2	1	Source
0	0	Write Bit Mask Pattern Register (XR24)
0	1	Graphics Controller Bit Mask Register (GR08)
1	0	Rotated CPU Byte
1	1	Reserved

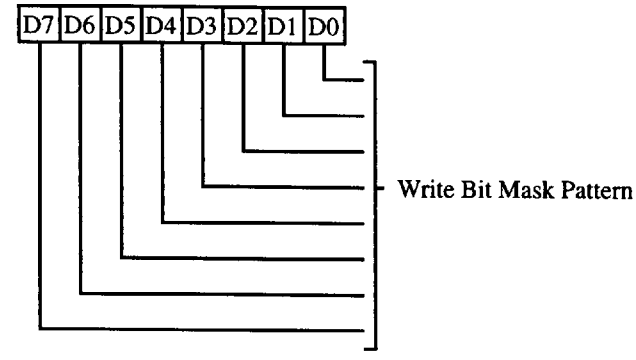
3 Read-Modify Write Cycle

- 0 No Read-Modify-Write Cycles (default on reset)
- 1 Enable CPU Read-Modify-Write cycles. When this bit is set, all CPU byte-write cycles to VGA memory are converted into Read-Modify-Write cycles. The CPU write operation address is used for executing a read cycle. Executing a CPU Read Cycle with this bit set is an illegal operation. The Write Bit Mask function is allowed (bit 0 of this register may be set) with read-modify write cycles.

7-4 Reserved (0)

WRITE BIT MASK PATTERN REGISTER (XR24)

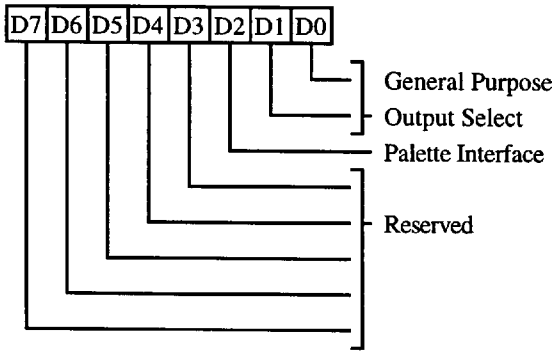
Read/Write at I/O Address 3B7h/3D7h
Index 24h



7-0 When this register is selected as a source for the Write Bit Mask pattern, the 8 bits of this register are used as a VRAM data write bit mask. These eight bits are duplicated four times and applied to all four memory maps as a write bit mask.

DEFINE PINS REGISTER (XR25)

Read/Write at I/O Address 3B7h/3D7h
Index 25h



0-1 These bits control the signal ouput on 'GPOUT' (pin 52) when in the ISA Bus. Pin 52 functions as 'CSFB/' in MC Bus configurations independent of the setting of these register bits.

1	0	Signal Output (RESET Inactive)
0	0	Inverted bit 0 of the Feature Control register (FCR)
0	1	Signal indicating that a VRAM data transfer cycle is in progress
1	x	Reserved (undefined)

1	0	Signal Output (RESET Active)
0	x	Diagnostic Function: Scan test signal
1	x	Diagnostic Function: Delayed IOCLK

Note: Bit 1 is not altered by RESET and is undefined on power up. Bit 0 is cleared by RESET.

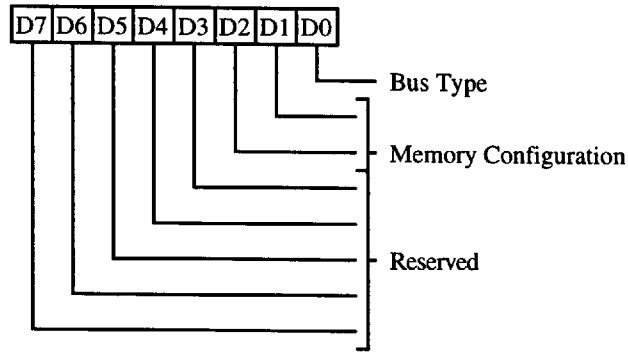
2 Palette Interface

0 Decode only address 3C6-3C9h (Selected on Reset)
1 Activate Palette at 3C6-3C9h and 83C6-83C9h

3-7 Reserved (0)

CONFIGURATION REGISTER (XR26)

Read/Write at I/O Address 3B7h/3D7h
Index 26h



At the end of the reset cycle, the 82C453 latches the state of pins A16-SW2, BHE/-SW1, and AEN-SW0 on bits 2-0 respectively. The 82C453 uses these bits to configure itself for various memory configurations and to select either ISA bus or MC bus interfaces. The bits are defined as follows:

0 Bus Type

0 MC bus interface
1 ISA bus interface

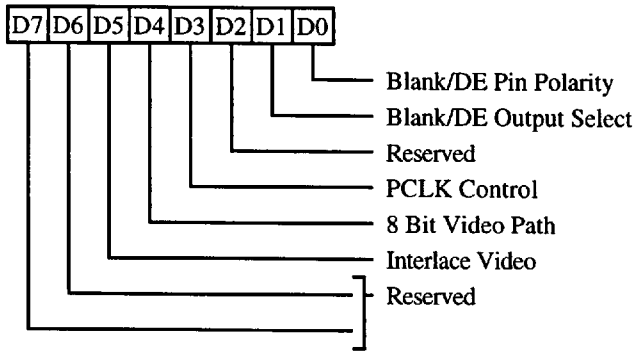
2-1 Memory Configuration

Bit 2	Bit 1	Configuration
0	0	Reserved
0	1	Four 256K x 4 VRAMs
1	0	Eight 256K x 4 VRAMs
1	1	Eight 64K x 4 VRAMs

3-7 Reserved (0)

VIDEO INTERFACE REGISTER (XR28)

Read/Write at I/O Address 3B7h/3D7h
Index 28h



0 BLANK / Display Enable Pin Polarity

- 0 Negative
- 1 Positive

1 BLANK / Display Enable Output Select

- 0 BLANK/ pin outputs BLANK/
- 1 BLANK/ pin outputs the DE signal (the polarity bit is still effective)

2 Reserved

3 PCLK Control

- 0 PCLK output is 451/452 compatible, default on reset.
- 1 PCLK is inverted before the output stage. This inversion of PCLK improves the setup/hold time of pixel data with respect to PCLK from the 82C453 as seen by the external color palette at high clock speeds (65MHz).

4 8 Bit Video Path

- 0 Select 4-bit VGA video path (default on reset)
- 1 Select 8-bit VGA video path

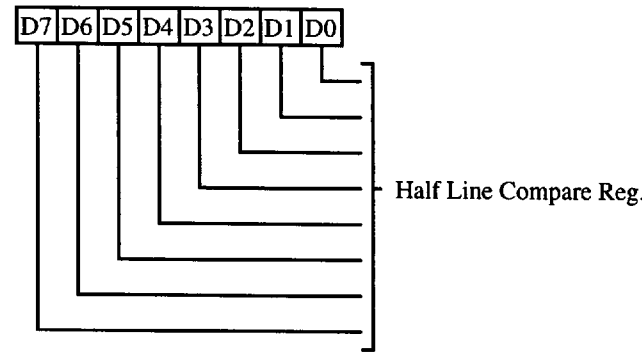
5 Interlace Video

- 0 Non-interlaced video (default on reset)
- 1 Interlaced video. This bit is set for 800x600 and 1024x768 interlaced modes.

7-6 Reserved (0)

HALF LINE COMPARE REGISTER (XR29)

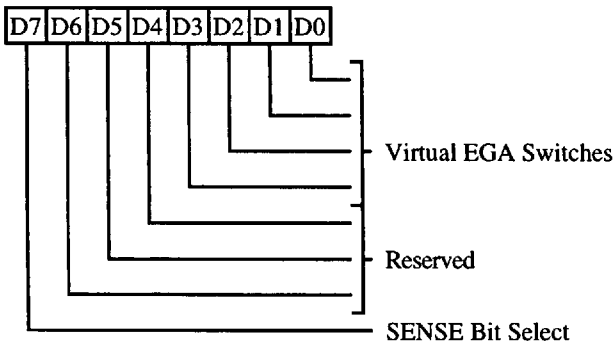
Read/Write at I/O Address 3B7h/3D7h
Index 29h



7-0 These 8 bits are use to generate the 'half line compare' signal that controls the positioning of the Vertical Sync for odd frames when the interlaced video output option is enabled, see the Video Interface Register.

EGA SWITCH REGISTER (XR41)

Read/Write at I/O Address 3B7h/3D7h
Index 41h



3-0 EGA Switches. These four bits are set/reset by software to reflect the status of the 'EGA switches'. When bit-7 of this register is set, one of these four 'virtual switch' bits are selected by bits 2-3 of the Miscellaneous Ouput Register port 3C3h (00 selects bit-3, 01 selects bit-2, etc). The selected bit may be read as SENSE bit 4 of Input Status Register 0 (ST00) at port 3C2h.

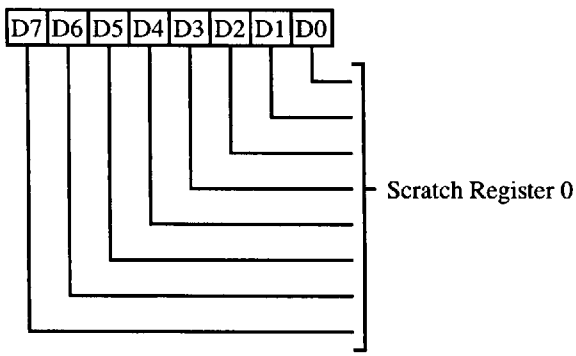
6-4 Reserved (0)

7 Sense Select. This bit selects between the 82C453 Sense input (from the VGA Analog comparator) or the Virtual EGA Switches (bits 0-3 of this register) for input to bit 4 of Input Status Register 0 (ST00) at port 3C2h.

0 Select the SENSE pin as bit 4 of ST00
1 Select one of bits 0-3 of this register as bit 4 of ST00

VIDEO FLAGS REGISTER (XR44)

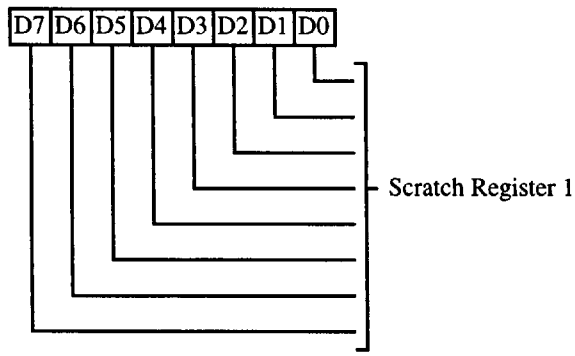
Read/Write at I/O Address 3B7h/3D7h
Index 44h



7-0 These eight bits are for software to store data that is not affected by RESET. This register is reserved for BIOS and driver use.

SCRATCH REGISTER 1 / FOREGROUND COLOR REGISTER (XR45)

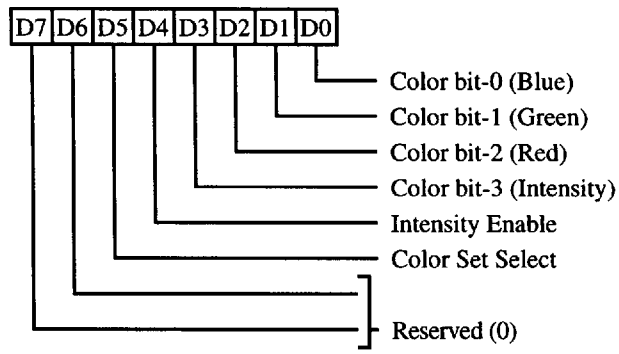
Read/Write at I/O Address 3B7h/3D7h
Index 45h



7-0 These eight bits are for software to store data that is not affected by reset. This register is also used to hold the fore ground color for text when using the 82C453's Packed Pixel Color Expansion feature.

CGA COLOR SELECT (XR7E)

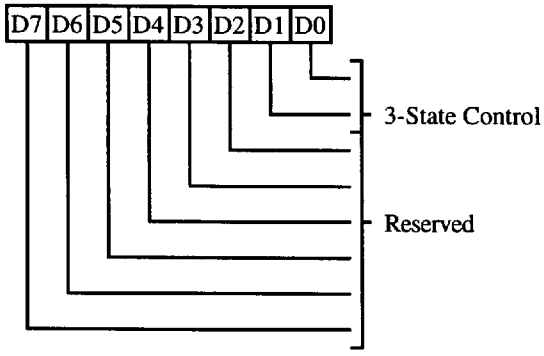
Read/Write at I/O Address 3B7h/3D7h
Index 7Eh



This register is a copy of the CGA color select register 3D9h. Writes to this register will change the copy at 3D9h. It is effective in CGA emulation mode. The copy at 3D9h is visible only in CGA emulation mode. The copy at XR7E is always visible.

DIAGNOSTIC REGISTER (XR7F)

Read/Write at I/O Address 3B7h/3D7h
Index 7Fh



0 3-State Control bit-0

0 Normal outputs (default)
1 3-State the following pins:

HSYNC, VSYNC, BLANK/, PCLK, P7:0, GPOUT, PALRD/, PALWR/

1 3-State control bit-1

0 Normal outputs (default)
1 3-State the following pins:

SCLK, SOEB0/, DISA16, AA8:0, BA8:0, RAS/, CAS/, WE3:0/, DTOE01/, DTOE23/

2-7 Reserved (0)

82C453 Functional Description

The 82C453 is the high performance VGA controller of the CHIPS 450 product family. This product is fully compatible with IBM's VGA standard at the gate, register and BIOS level. It also offers enhanced backward compatibility to EGA, CGA, Hercules and MDA standards without using NMI. The 82C453 has a dual bus interface to support both the PC (also called EISA/ISA or 'Industry Standard Architecture') Bus and the Micro Channel (MC) bus. All the control signals for both types of interfaces are integrated on the chip. The 82C453 automatically configures itself for either ISA or MC bus interfaces based on the status of configuration input bit, on pin AEN (SW0). This configuration bit is sampled at the end of the bus RESET signal and can be read in the extended Hardware Configuration Register.

The 82C453 architecture is optimized to use dual port Video RAMs (VRAM) only. The 82C453 uses the VRAM serial port for CRT refresh and the VRAM random read/write port for CPU read/write cycles. Due to this dual port architecture, the 82C453 can support resolutions up to 1024x768 256 colors with very high performance. In graphics modes the 82C453's highly optimized architecture uses less than 10% of VRAM bandwidth for CRT updates while allocating more than 90% of VGA memory bandwidth to the CPU. In fact, at 1024x768, 256 color resolution, the 82C453 can sustain a write data transfer bandwidth to VGA memory from system memory that is higher than that of an 8 MHz AT bus, allowing for very fast screen generation.

The 82C453 architecture offers non-interleaved access of plane-0 and plane-1 data in VGA text modes. The 82C453 has additional features like support for Read-Modify-Write cycles and it utilizes the VRAM's write bit mask capabilities to improve the performance of graphics applications. Features like Dual Paging make it easier to virtualize the VGA for improved multi-tasking under DOS, OS/2 and UNIX environments. The 82C453 also supports 16-bit memory and I/O accesses.

BUS INTERFACE

The 82C453 supports both PC (EISA/ISA) and Micro Channel (MC) bus interfaces. The 82C453 samples configuration bits on pins A16-SW2, BHE/-SW1, and AEN-SW0 at the end of a bus RESET cycle. The status of these pins are used by the 82C453 to configure itself for an appropriate bus and VRAM interface. These three configuration bits, with pull-ups internal to the 82C453, are readable in the 82C453 extensions Hardware Configuration Register. They are defined as follows:

A16 (SW2)	BHE/ (SW1)	Definition
0	0	(Reserved)
0	1	Four 256Kx4 VRAMs (512KB)
1	0	Eight 256Kx4 VRAMs (1024KB)
1	1	Eight 64Kx4 VRAMs (256KB)

AEN (SW0)	Definition
1	EISA/ISA Bus Interface
0	MC Bus Interface

16-Bit CPU BUS Interface

The 82C453 supports 16-bit accesses to both memory and I/O ports depending on the state of BHE/ and A0. For 16-bit interface, the 82C453 will always assert DS16/ (MEMCS16/ or IOCS16/ for the EISA/ISA Bus) after a valid memory or I/0 address is recognized. Depending on the state of A0 and BHE/, either an 8-bit or 16-bit cycle will actually be executed. This ensures that even for software-directed 8-bit accesses, faster non-converted cycles will be executed by the system logic. If both A0 and BHE/ are high then a byte transfer will be executed from the lower data bus to the odd byte (default 8 bit transfer mode). Depending on A0 and BHE/, the data transfer cycle will be executed as follows:

BHE/	A0	D8-D15	D7-D0
0	0	Byte-1	Byte-0
0	1	Byte-1	3-State
1	0	3-State	Byte-0
1	1	Invalid	Invalid

Caution:

It is important to note that the EISA/ISA bus supports 16-bit devices on 128 KByte boundaries only. This is because the 36-pin EISA/ISA connector outputs unlatched address bits A17 through A23 only. The absence of A16 forces the decode to take place on 128 KByte boundaries. 16-bit access of VGA memory requires that MDA, Hercules and CGA cards not be installed in the EISA/ISA bus.

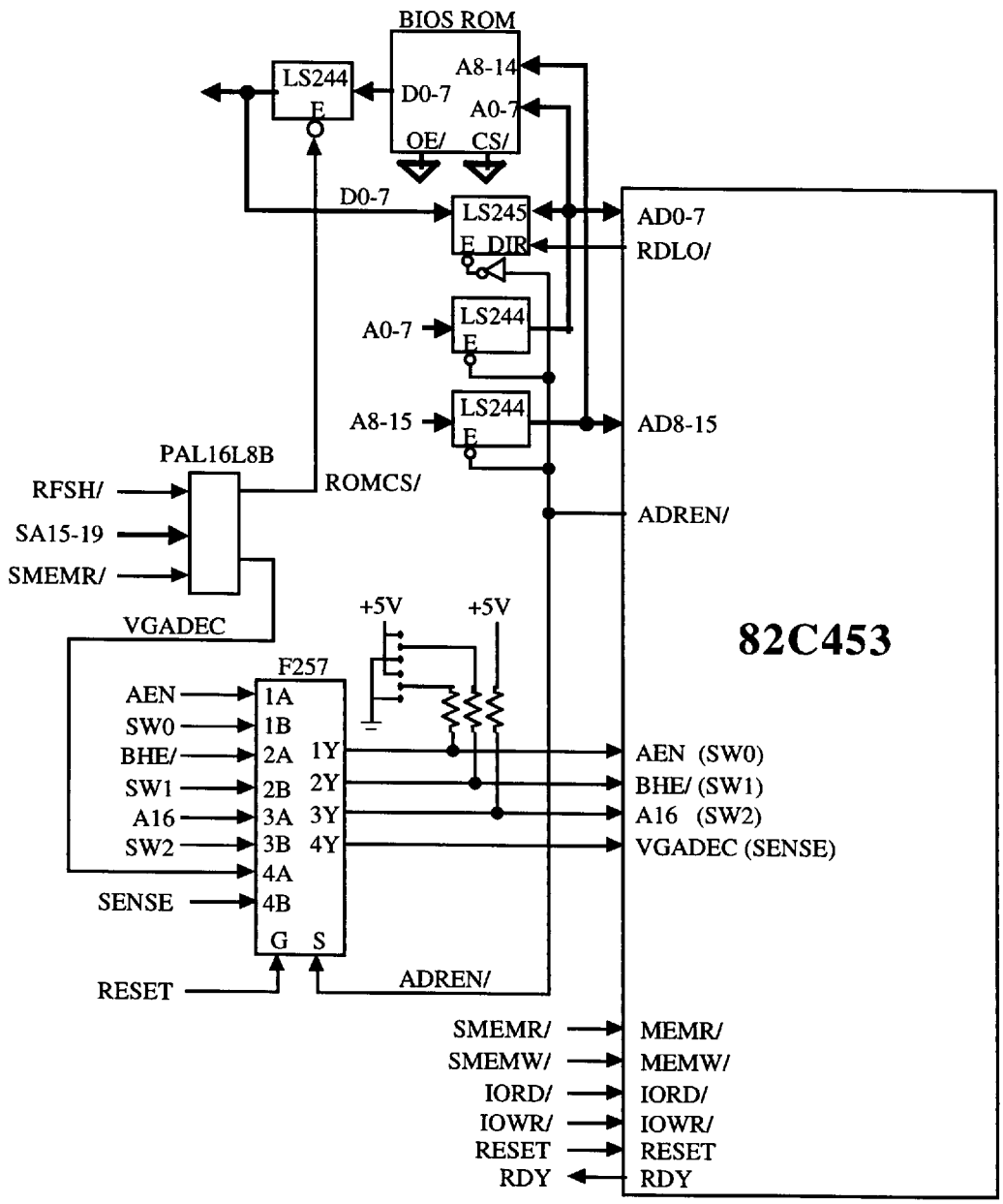
EISA/ISA Bus Interface

The configuration bit AEN (SW0) should be '1' for the EISA/ISA Bus interface. The 82C453 supports both 8-bit and 16-bit interfaces. The 82C453 uses multiplexed address and data buses to interface to the EISA/ISA bus.

Both 8-bit and 16-bit EISA/ISA Bus implementations of the 82C453 require a BIOS ROM. The 82C453 supports a 32 KByte ROM BIOS. An external PAL is required to generate a ROMCS/ signal for addresses C0000H-C7FFFH.

8-Bit EISA/ISA Bus Interface

To use an 8-bit EISA/ISA Bus interface, an external 8-bit multiplexer is required. This can be implemented using one buffer (LS244 or equivalent) for the lower 8 bits of the address bus (A0-A7) and one transceiver (LS245 or equivalent) for the data bus. Upper address bits A8 to A15 can be connected to the 82C453 via another buffer. The 82C453 provides direction and control signals for the external multiplexer. The ADREN/ signal from the 82C453 enables the address buffer onto the multiplexed 82C453 bus. The ADREN/ signal is inverted and



Note: See the Application Schematic Section for PAL EQUATIONS.

Block Diagram - 8-Bit EISA/ISA Bus Interface

used to enable the data transceiver during data transfer cycles. The 82C453 also provides the RDLO/ control signal to control the direction of the data transceiver during read and write operations.

The 82C453 has 17 address inputs (16 multiplexed with the data bus plus A16). The upper three address bits, A17 to A19, should be decoded externally and qualified with Refresh. The decoded address output should be connected to the VGADEC pin of the 82C453. The decode should occur when A19 A18 A17 = '101'.

When the BIOS ROM is being accessed, the 82C453 always keeps the external multiplexer in the address state. The ROM address pins can therefore be connected to the 82C453 multiplexed address/data bus. An additional buffer is needed to buffer the ROM data onto the EISA/ISA bus. The enable for this buffer (ROMCS/) is generated by the same external PAL that generates VGADEC.

16 Bit EISA/ISA Bus Interface

The 16-bit interface supports 16-bit accesses to display memory and index/data pairs of I/O registers. 16-bit accesses to display memory assume that the 82C453 controls the entire A0000 - BFFFFh address space. This requires that the 82C453 be the only active video card in the system (i.e., no co-resident Hercules or CGA cards may be present which also have display buffers in the A0000-BFFFF address range).

The external 16-bit multiplexer can be implemented using two address buffers (LS244 or equivalent) and two data transceivers (LS245 or equivalent). The control and direction signals are provided by the 82C453. ADREN/ provides the enable for the multiplexer. RDLO/ controls the direction of the data transceiver sitting on the low data bus (D0-D7), while RDHI/ controls the upper data transceiver.

The 82C453 has 17 address inputs (16 multiplexed with the data bus plus A16). For EISA/ISA bus interfacing, upper address bits LA20:23 and SA17:SA19 should be decoded externally and qualified with Refresh. The decoded address output should be connected to the 82C453 VGADEC pin. The address decoding is done for address range A0000-BFFFFh.

For 16-bit memory interface in the EISA/ISA bus, MEMCS16/ is generated externally by decoding unlatched addresses LA17:23. The DISA16 signal from the 82C453 should be used to qualify MEMCS16/. DISA16 is active high during 4VRAM text mode and when fonts are loaded in 8VRAM text mode. MEMCS16/ should be suppressed when DISA16 is high. The 82C453 generates IOCS16/ from latched addresses 'SA15:0'. IOCS16/ is generated only for index/data pairs of registers. This includes the Sequencer (3C4h), the Graphics Controller (3CEh), CRT Controller (3D4h/3B4h) Attribute Controller (3C0h) and Extension Register (3D6h/3D7h). All other VGA I/O ports (Color palette, Misc. Output Register and Status Registers) are always treated as 8-bit ports; IOCS16/ is not asserted during CPU access of these registers. The IOCS16/ pin can directly drive the EISA/ISA bus. When the BIOS ROM is being accessed, the 82C453 always keeps the external multiplexer in the address state. The ROM address pins can therefore be connected to the 82C453 multiplexed address/data bus. ROMCS/ is generated by external logic. A 16-bit BIOS interface is also supported. Note that extreme care should be taken to decode A15:23. In the EISA/ISA bus A15 and A16 are not available in unlatched form. Care should be taken to guarantee MEMCS16/ timing meets system specifications. Two additional buffers are needed to buffer the ROM data onto the EISA/ISA Bus.

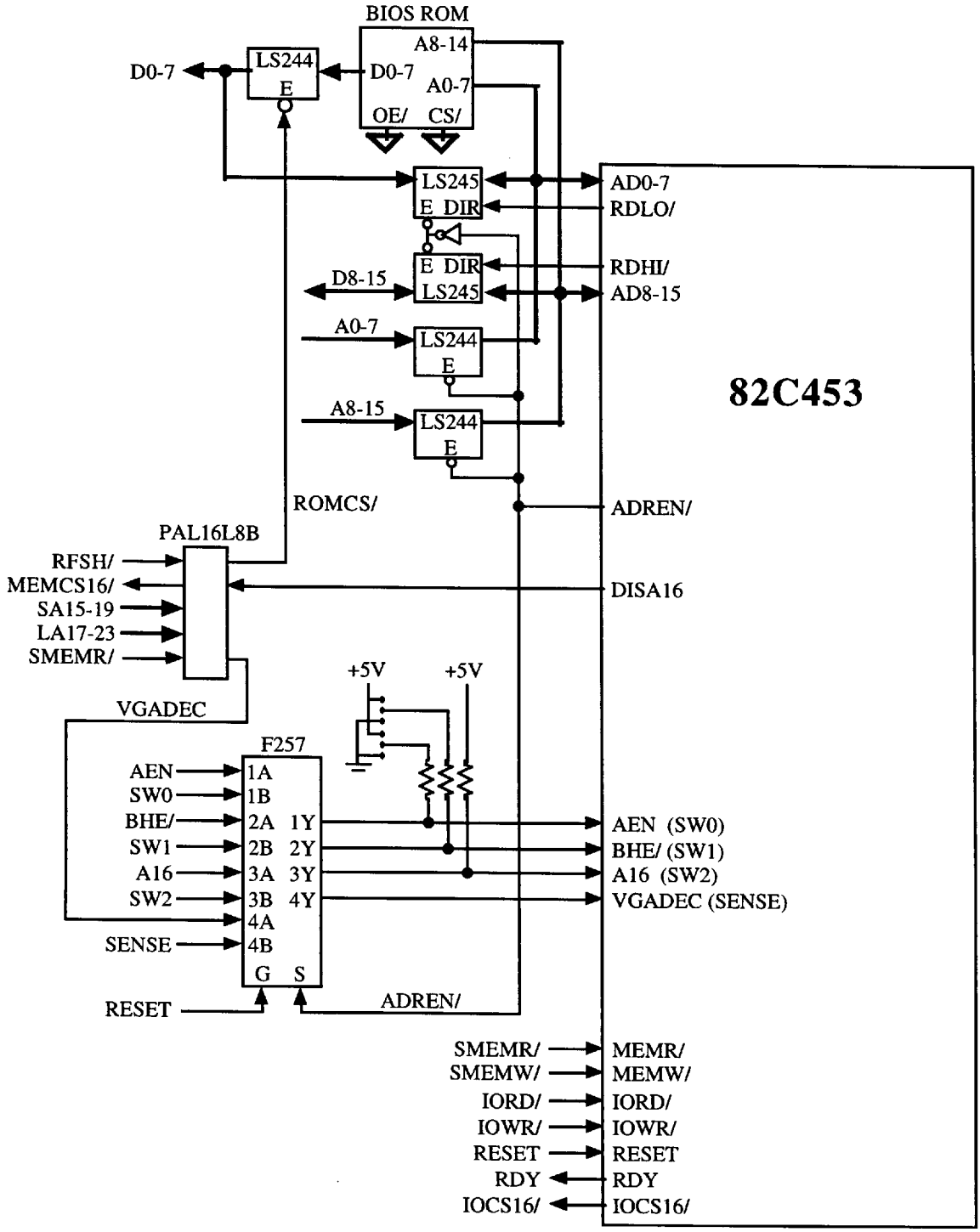
Micro Channel (MC) Bus Interface

The configuration bit SETUP/ (SW0) should be '0' for MC Bus interface. The 82C453 supports both 8-bit and 16-bit interfaces. The 82C453 uses multiplexed address and data buses to interface to the MC bus.

The external 16-bit multiplexer can be implemented using two address buffers (LS244s) and two data transceivers (LS245s). The control and direction signals are provided by the 82C453. ADREN/ provides the enable for the multiplexer. RDLO/ controls the direction of the data transceiver connected to the low data bus (D0:7), while RDHI/ controls the upper data transceiver (D8:15).

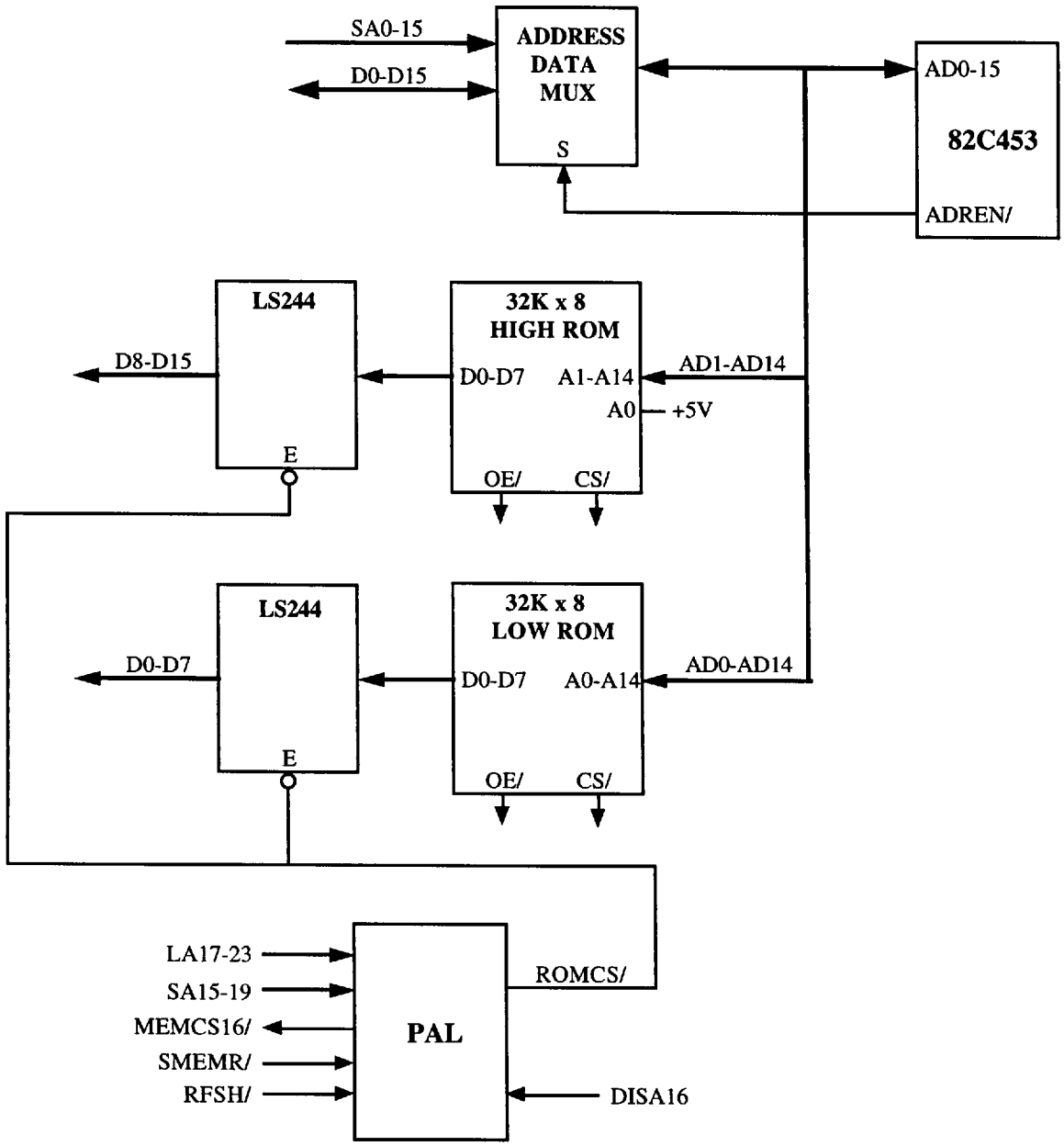
82C453 has 17 address inputs (16 multiplexed with the data bus plus A16). For the MC bus interface, the upper address bits A17:23 should be decoded externally and qualified with Refresh and MADE24. The decoded address output should be connected to the VGADEC pin on 82C453. The address decoding is done for address range A0000-BFFFFh.

For a mother-board implementation of the 82C453 with the CHIPset 250/280, the 82C453 generates DS16/, RDY, and CSFB/ (Card Select Feedback) by decoding VGADEC, A16:0 and M/IO as a valid memory or I/O address. These pins directly correspond to the DS16/, RDY, and CDSFDBK/ pins of the MC bus.



Note: See the Application Schematic Section for PAL EQUATIONS.

Block Diagram - 16-Bit EISA/ISA Bus Interface (8-Bit BIOS)

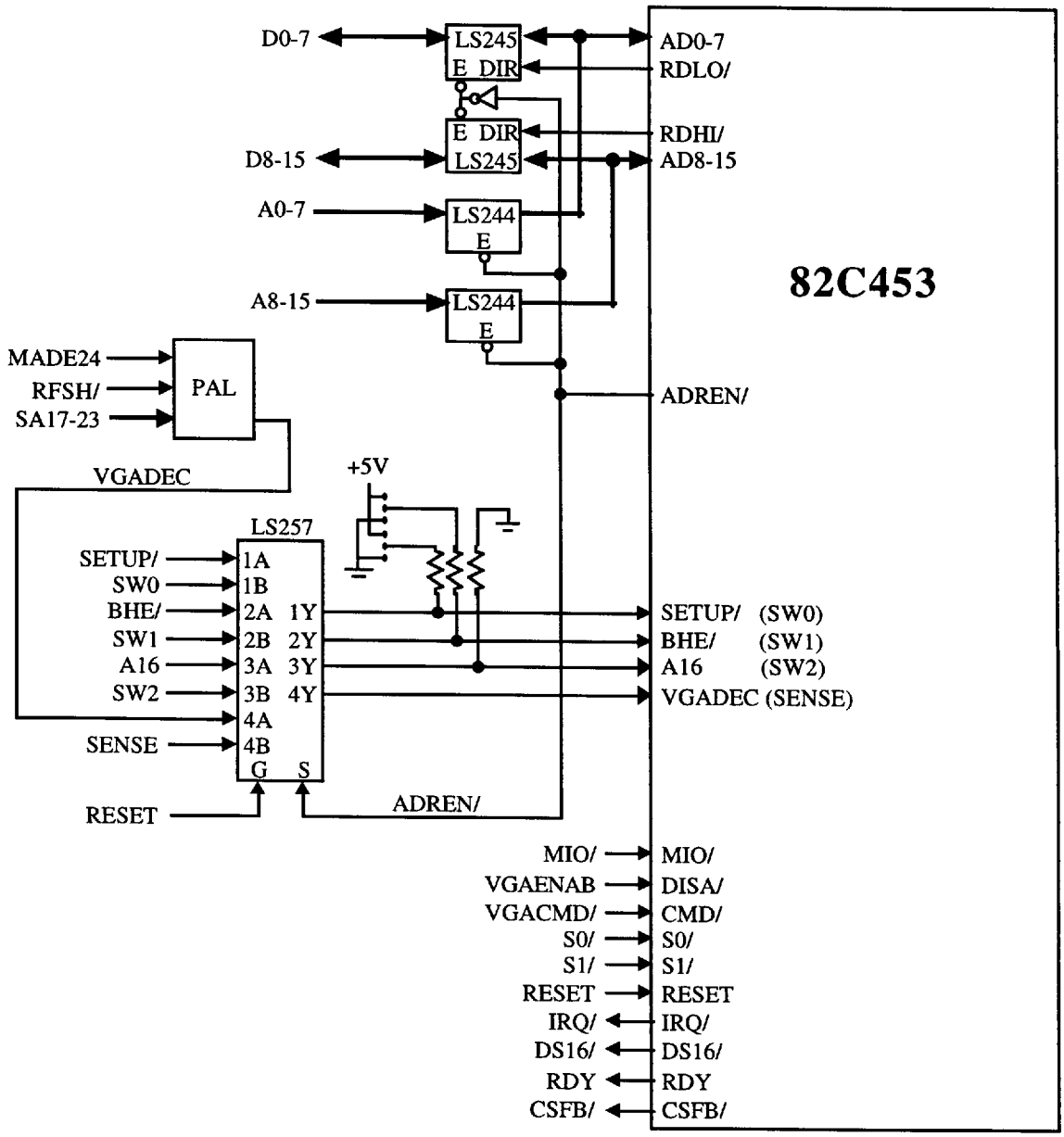


Note: See the Application Schematic Section for PAL EQUATIONS.

Block Diagram - 16-Bit EISA/ISA Bus Interface (16-Bit BIOS)

The RESET, S0/, S1/, M/IO signals on the MC can directly drive the corresponding pins on 82C453. The CMD/ signal on the MC bus must be qualified with Refresh/ and then connected to the CMD/ pin on 82C453. The CHIPS 250 and 280 chipsets provide a qualified command signal called VGACMD/.

The 82C453 implements register 3C3h bit-0 (VGA Enable) internal to the chip. Since this signal also comes from the CHIPS 250/280 chip sets, when the MC bus interface is selected, this register is made write-only. This will eliminate the data bus conflict on reads of the 3C3h register. The 82C453 will not



Note: See the Application Schematic Section for PAL EQUATIONS.

Block Diagram - 16-Bit MC Interface

generate MC bus signals CSFB/ and RDY when the CPU accesses this register. The 3C3h register can be read if bit-0 of the 82C453 extension Miscellaneous Interface Register is set to '1'; under this condition the 82C453 will generate MC bus signals CSFB/ and RDY for CPU Read and Write cycles to I/O address 3C3h.

The 82C453 can also be put in setup mode by pulling the SETUP/ pin low. This signal is either bit-5 of port 94h or a Micro Channel VGASETUP/ signal dedicated to a specific slot. Again, the CHIPS 250/280 chip sets implement register 94h internally and provide this bit on a pin called VGASETUP/. Refer to the MC interface diagram for the circuit implementation.

POS ID Registers

The standard IBM PS/2 system board implementation of the VGA does not have POS ID registers 100h and 101h. The 82C453 implements POS ID registers 102h, 103h, and 104h internally. If POS ID registers are needed at 100h, 101h, 105h, 106h, and 107H, an external PAL can be added for decoding those addresses. The 82C453 will continue to generate MC bus interface signals.

Setup and Enable/Disable Modes

IBM's VGA add-in card for the EISA/ISA Bus uses a register at I/O address 46E8H for ROM paging, VGA Setup, and VGA Enable functions. The 82C453 implements the VGA Setup and Enable bits of this register (46E8h) internally. 46E8h register bit-3 is used as display sub-system enable/disable and bit-4 is used to put the VGA in setup mode. The 82C453 does not support ROM paging.

In Micro Channel implementations the 82C453 is put into setup mode by asserting the SETUP/ pin low. Usually this pin is controlled by bit-5 of I/O port 94h and is implemented in the PS/2 system logic. If the 82C453 is on the Micro Channel bus (as opposed to the system board), the bus provides a SETUP/ input for each slot.

The 82C453 should be enabled for normal operation. In the MC interface, the 82C453 disappears from the memory and I/O space if bit-0 of I/O port 3C3h is reset to zero (low). For normal operation this bit should be set to one (high). It is important to note that the 82C453 implements this register internally. The Chips 250/280 family chip set also implements this register. To avoid the bus conflict, the 82C453 can be programmed to respond to 3C3h writes cycles only and during 3C3h read operations, Chips 250/280 logic drives the data bus. In the PC Bus interface, setting bit-3 of port 46E8h to zero (low) disables the 82C453 and setting it to one (high) enables the 82C453.

For normal operation the VGA should be programmed as follows:

MC Interface

a) Set bit-0 of port 3C3h to '1'. This enables the VGA after the CPU sets to one (high) bit-0 of I/O register 102h while driving the SETUP/ pin low.

b) Put the 82C453 into Setup Mode by writing '1' to bit-5 of I/O register 94h. This causes the SETUP/ pin to go low.

c) With the 82C453 in setup mode, write '1' to bit-0 (Video Enable bit) of I/O register 102h. I/O register 102h is accessible when the 82C453 is in setup mode.

d) Take the 82C453 out of Setup Mode by writing '0' to bit-5 of I/O register 94h. This causes the SETUP/ pin to go high.

EISA/ISA Bus Interface

a) Set bit-3 of port 46E8h to '1'. This enables the VGA after the CPU sets to one (high) bit-0 of I/O register 102h.

b) Put the 82C453 into Setup Mode by writing '1' to bit-4 of I/O register 46E8h.

c) With the 82C453 in setup mode, write '1' to bit-0 (Video Enable bit) of I/O register 102h. I/O register 102h is accessible when the 82C453 is in setup mode.

d) Take the 82C453 out of Setup Mode by writing '0' to bit-4 of I/O register 46E8h.

Multiple 82C453s

It is possible to support up to eight 82C453s in one system. Each 82C453 must have a unique number assigned to it through DIP switches. All 82C453s occupy the same I/O and memory address space. However, only one 82C453 responds to CPU accesses at a time. Refer to EISA/ISA and MC bus interface diagrams for DIP Switch support.

The currently active 82C453 is selected by writing an ID number for that 82C453 into the internal Extended Enable register for all 82C453s. Only the 82C453 that matches the ID number with that on its DIP switches connected to 82C453 pins A16, BHE/, and AEN will respond to further CPU accesses. This feature is available in the EISA/ISA bus only. For the MC bus, multiple VGAs may be implemented through the use of SETUP inputs that

are unique for each slot and using the global enable/disable bit-0 of register 102h.

This feature may also be used to allow motherboard VGA logic to co-exist with a plug-in VGA subsystem.

VRAM INTERFACE

The 82C453 supports 3 VRAM configurations:

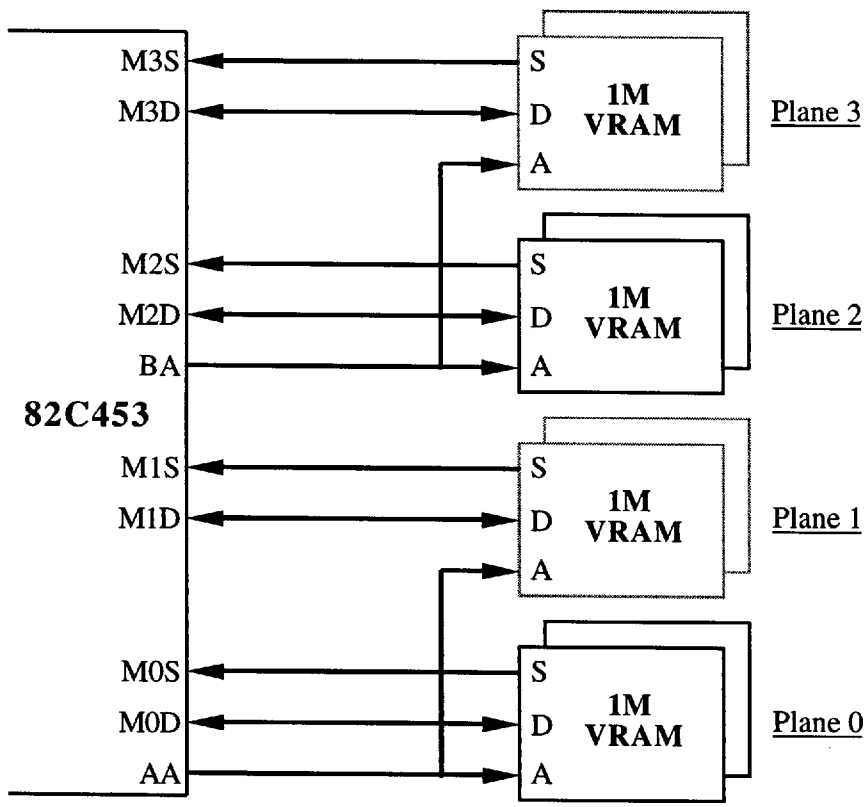
1) Eight 64Kx4, 256 Kbit VRAMs (256 KByte)
2) Eight 256Kx4, 1 Mbit VRAMs (1024 KByte)
3) Four 256Kx4, 1 Mbit VRAMs (512 KByte)

The 82C453 supports VRAMs only. The 82C453 uses a 32-bit data bus (MxD0:7, x=0-3) to read/write CPU data. A separate set of 32 pins are used to read video data from the VRAM serial port for CRT refresh. For VRAM configurations 1 and 2; the 82C453 VRAM serial data bus M3:0S7:0 connects to serial data outputs of memory planes 3:0. For configurations of four one megabit VRAMs, only serial data bus M0S0:7 and M2S0:7 are used (M1S0:7 and M3S0:7 are not used).

There are two 8(9) bit multiplexed address buses AA7:0 and BA7:0 that connect to planes 0:1 and 2:3 respectively. There are common RAS/ and CAS/ signals for all VRAMs in all configurations. The WE3:0/ signals are write enables for each of the four memory planes (WE1/ and WE3/ are not used in 4-VRAM configurations).

The DTOE01:23/ pins are asserted for reading RAM data for CPU cycles and to execute RAM to SAM transfer cycles of VRAMs. DTOE01/ connects to memory planes 0 and 1 while DTOE23/ connects to planes 2 and 3.

The SOE/ pins of 1Mbit VRAMs should be tied to ground. The SCLK pin is a common serial clock output to all VRAMs in all VRAM configurations. VRAM interface diagrams are shown in following pages. The AA8 and BA8 pins are left unconnected in memory configuration 1 (64Kx4 VRAMs).



Block Diagram - VRAM Address/Data Connections

Hardware Read-Modify-Write Cycles

The 82C453 supports CPU Read-Modify-Write cycles. When bit-3 of the 82C453 extended Write Bit Mask Control Register (XR23) is set to 1, all subsequent CPU byte write cycles to VGA memory are converted into Read-Modify-Write cycles. The CPU write cycle address is used for executing a read cycle. This feature of the 82C453 cuts in half the number of bus cycles needed to perform a read followed by a write cycle by software. The read-modify-write function is very effective for logical operations and inversions of rectangular sections of the screen.

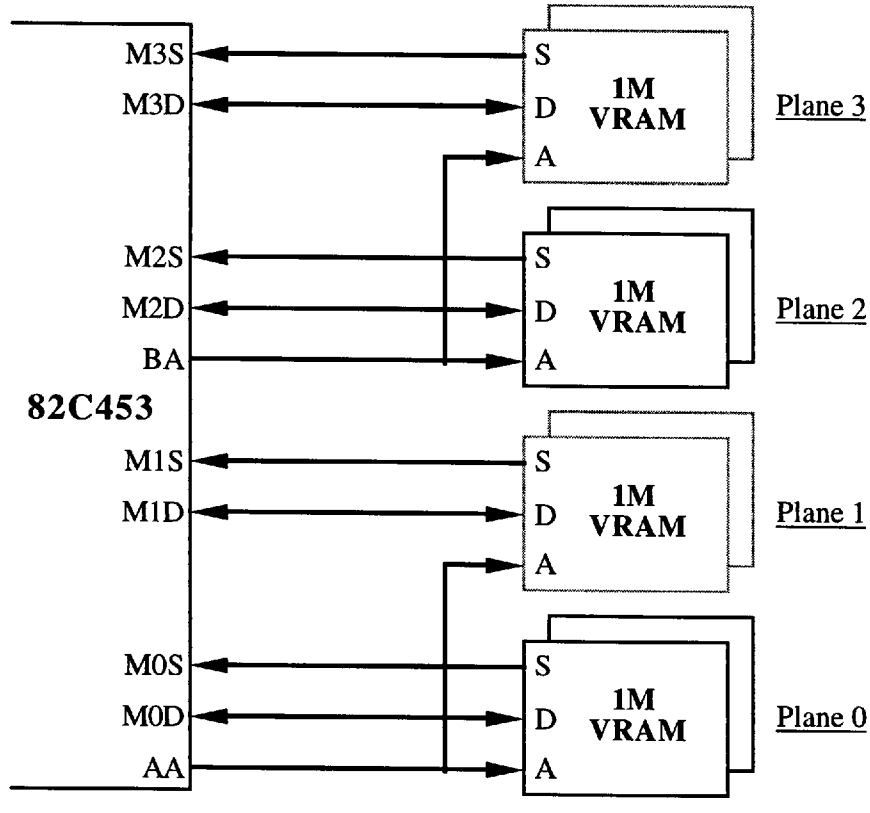
Hardware Bit Masking

In planar modes, a pixel of data is represented by one bit from each color plane. The data associated with 8 different pixels is stored in a single byte of display memory within a plane. Bit masking is required when writing to one or more pixels without affecting the other pixels in a given byte. The hardware bit mask feature of the 82C453 provides a very fast technique for bit masking.

Two registers in the 82C453 facilitate fast bit masking. The Write Bit Mask Control register, XR23, controls the bit masking operation. Bit 0 enables the write bit mask feature. Bits 1 and 2 control the source of the bit mask pattern as shown in the table below. The standard VGA uses the Graphics Controller Bit Mask register for bit masking and so this configuration is very useful when older code is converted since it provides a simple porting task.

XR23 Bits 2	1	Source
0	0	Write Bit Mask Pattern register (XR24)
0	1	Graphics Controller Bit Mask register
1	0	Rotated CPU byte
1	1	Reserved

If software is executing a Read-Modify-Write cycle for write protecting one or more bits of old data, then it is more efficient to use the VRAM write bit mask feature supported by the 82C453. However, if software intends to execute a logical operation in conjunction with a Read-Modify-Write cycle then the 82C453's Read-Modify-Write cycles are more efficient. It is possible to execute a Read-Modify-Write cycle with the VRAM write bit mask feature enabled.



Block Diagram - VRAM Control Connections

Hardware Packed Pixel Color Expansion

The raster font for each character is a monochrome bitmap stored in the premium system memory. In graphics modes, the monochrome bitmap must be expanded into color pixels in video memory. In the 256 color modes, this process is very time consuming and is limited by the CPU bandwidth and computation speed. The 82C453, however, provides a high speed path for processing alphanumerics in packed pixel graphics modes.

The Packed Pixel Color Expansion mode is enabled through bit-1 of the CPU Interface register, XR02. If bit-1 of XR02 is one, the Packed Pixel Color Expansion mode is enabled. If it is set to 0, the mode is disabled.

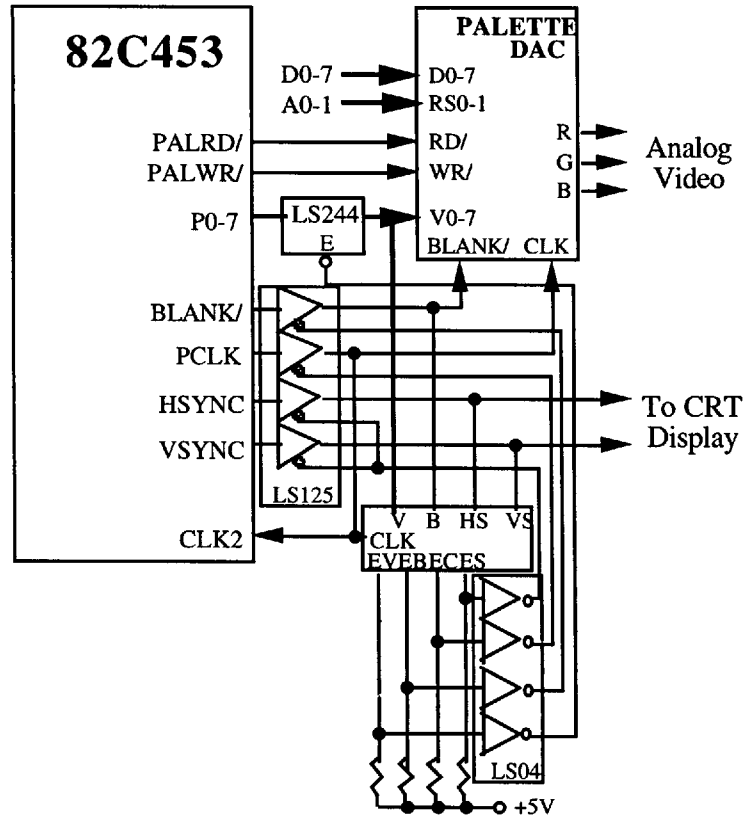
Normally in the packed pixel modes, each byte represents a pixel on the screen (8-bits are required to determine the color). If the Packed Pixel Color Expansion mode is enabled, each byte is expanded to represent 8 pixels. The foreground color is written to all pixels which correspond to a 1 and the background color is written to all pixels which correspond to a 0.

The foreground color is stored in the Scratch Register 1 /Foreground Color register (XR45). The 4 CPU latches hold the background color for the 4 bits of the lower or upper nibble of the CPU byte. The 82C453 requires two write operations per byte of character font. The result is that data is written into display memory 4 times faster than in the packed pixel modes. If the Packed Pixel Color Expansion mode is not enabled, XR45 can be used as scratch storage.

VIDEO INTERFACE

The 82C453 supports both digital and analog monitors. It generates all sync, blanking, video, and pixel clock signals to support both type of monitors.

The 82C453 supports programming of an external palette DAC by decoding the CPU addresses and generating the PALRD/ and PALWR/ signals to the external palette. The 82C453 decodes I/O addresses 3C6-3C9h as valid external palette addresses. The 82C453 also supports DAC diagnostic and VGA monitor type detection by making the SENSE input available to the programmer.



Block Diagram - External Palette/DAC Interface

Video Clock Support

The 82C453 has three direct display clock inputs: CLK0, CLK1 (CLKSEL0), and CLK2 (CLKSEL1). For a minimum system configuration these clock inputs can be connected directly to the clock sources. Alternately, 82C453 pins CLK1 (CLKSEL0), CLK2 (CLKSEL1) can be defined as outputs, through the 82C453 extension Sequencer Control register (XR05) to control an external one of four multiplexer or clock synthesizer chip. The CLK1 (CLKSEL0) and CLK2 (CLKSEL1) are driven by bits 2 and 3 of the VGA Miscellaneous Output register.

The 82C453 supports a General Purpose Output pin called 'GPOUT'. CLKSEL0, CLKSEL1, and GPOUT can be used to control an 8 to 1 Multiplexer. Up to eight display clocks can be supported in this fashion.

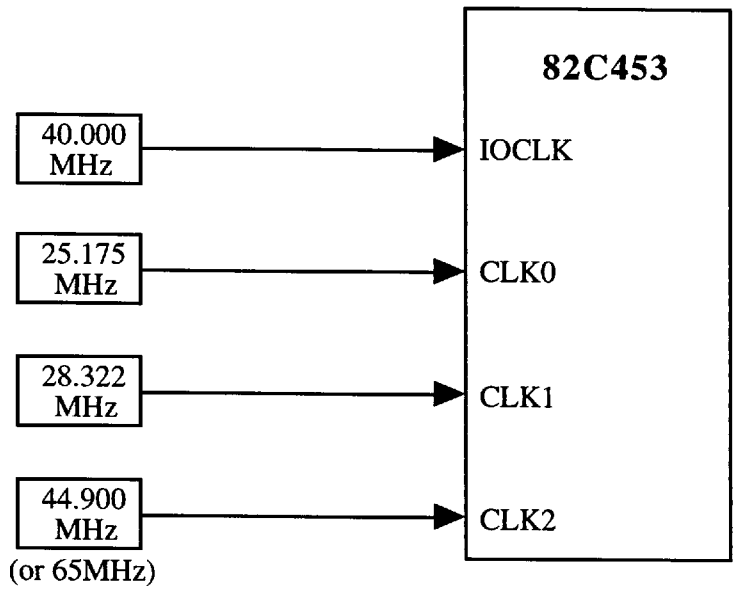
The 82C453 has another clock input called IOCLK. This input clock is used for internal sequencing of I/O registers. IOCLK should be between 35-40 MHz. IOCLK can also be used as a display clock (when MSR bits 3 & 2 = 11 and XR05 bit-0=0).
The 82C453 can also be interfaced to an external clock chip. CHIPS has designed a proprietary clock chip (82C403) to support the 82C453. Up to six different frequencies can be selected with the clock chip. CLK1, CLK2 and GPOUT are used as the select inputs into the clock chip (82C403). Three different clock schemes are shown in following pages.

Display Modes and Resolutions

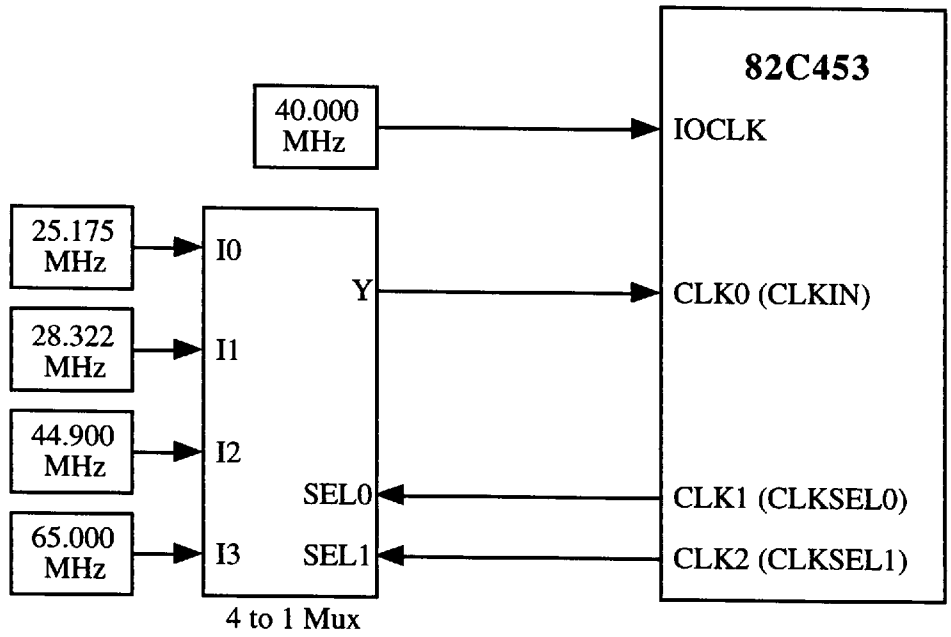
The 82C453 supports a superset of all VGA modes. It supports a screen resolution of up to 1024x768 in 16-color and 256-color graphics modes. 640x480 and 800x600 16-color and 256-color modes are also supported. The 82C453 also supports 132 Column Text Mode.

Screen Blanking

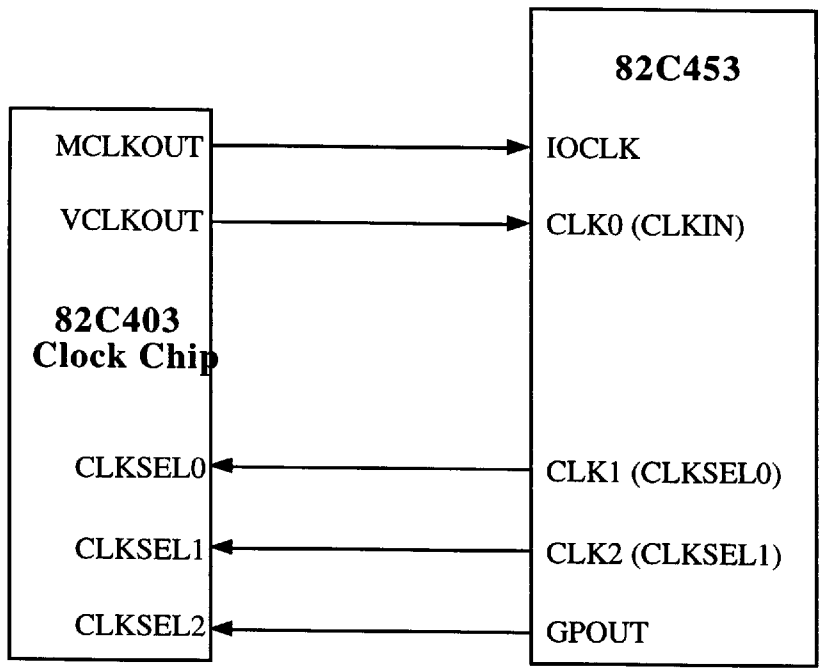
The 82C453 supports screen blanking by writing to a control register (as in IBM's VGA). During this time, all memory cycles are available to the CPU. During screen blanking, the video outputs are blanked to black level. This makes it easier to support TTL monitors. The IBM VGA's TTL video outputs (P7:0) are un-defined, making it difficult to



Block Diagram - Minimum Clock Configuration



Block Diagram - External Clock Multiplexer Interface



Block Diagram - 82C403 Clock Chip Interface

support TTL monitors. This is not a problem with analog monitors as the BLANK/ signal to the external RAMDAC is asserted which blanks the analog video.

Interlaced Video

The 82C453 can generate interlaced video for extended graphics modes like 1024x768 to use with inexpensive 8514-type display monitors. The 82C453 provides total freedom in positioning of Vertical Sync for odd frames within a horizontal scan line. This feature allows the 82C453 to drive a variety of 8514-type monitors. Interlaced video can be enabled by setting bit-5 of XR28.

DIP switch/Virtual EGA Switch Support

The 82C453 supports up to 3 external DIP switches. These switches are multiplexed on the A16 (SW2), BHE/ (SW1), and AEN (SW0) inputs. The state of the switches can be read at bits 2:0 in the 82C453 extended DIP Switch Register (XR01).

The 82C453 also supports virtual EGA switches. This feature allows software to write the status of EGA switches to the 82C453 extended EGA Switch Register (XR41) bits 3:0. Bit-7 of this register controls whether the status of the SENSE bit is from the SENSE pin or from the output of the EGA switch mux. The EGA switch select mux is controlled by bits 2 and 3 of the VGA/EGA Misc Output Register (3C2h). The output of the mux or the input from the 82C453 SENSE pin is read in bit-4 of the VGA/EGA Input Status Register 0.

DIP Switch support and the virtual EGA switch feature are available in both PC bus and Micro Channel bus configurations. However only two DIP switches are supported in MC bus. The AEN (SW0) pin becomes a SETUP/ pin only in MC interface.

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82C453 Compatibility

The 82C453 is compatible with the VGA, EGA, Hercules, CGA and MDA display standards. In general, application software written for one of these standards can be run on a 82C453-based system if a monitor with a resolution equal to or greater than that display standard is used.

The 82C453 provides several features which aid in the implementation of a display system compatible with these standards. These features are as follows:

- Write protection of internal registers using a Write Protect Register (one of the Backward Compatibility registers). This ensures that writes to internal registers initiated by applications software do not corrupt register values, enabling user to run software written for previous graphics standards.
- Two sets of display parameter registers are supplied. The 82C453 automatically selects the set to be used based on the current display mode and the type of display in use.

Certain assumptions are made regarding the VGA and backward compatibility:

- No NMI or any other interrupts have to be used. It is possible to generate NMI traps if required to support auto emulation.
- On power up the chip is always in VGA mode.
- There is no separate EGA mode. EGA mode is considered to be a special case of VGA mode. Special bits are provided to Write Protect some EGA specific registers. Software that uses the EGA in standard modes will work with the 82C453.
- In an implementation the display (CRT) is known and fixed.
- A software program can be executed to switch the chip into and out of CGA or Hercules modes. The software utility is consistent with the exact display being used. The BIOS for the 82C453 available from Chips & Technologies includes software to program the 82C453 in the VGA, EGA, CGA, MDA and Hercules modes.
- CGA/MDA/Hercules software can run on any monitor (EGA, Multisync™ or PS/2).
- When in CGA or Hercules mode, all VGA/EGA registers are unavailable.
- EGA, CGA, MDA and Hercules modes will definitely function in the standard defined modes.

VGA REGISTER WRITE PROTECTION

To use the write protect features:

A. Initialize the CRT controller or alternate registers to generate sync signals for the display in use.

B. Write protect the CRT controller or alternate registers using the Write Protect Register.

C. Permit the applications software to write CRT or alternate registers as if a particular display was in use. The 82C453 will operate as if a standard I/O write took place but will not permit protected registers to be altered.

ALTERNATE REGISTER SETS

The 82C453 supplies two sets of Display Parameter Registers. These are summarized in the table below. To make use of these two sets:

1. Program one set for text mode and the other set for graphics mode.
2. Write protect both sets of registers using the Write Protect Register to prevent the application software from corrupting them.

The contents of the internal mode registers are interpreted automatically and either the text or graphics set of CRTC or alternate registers is selected accordingly to generate the correct display. Since the display memory format in text and graphics is identical, switching between these modes does not require CPU or application software intervention.

Display Parameter Registers used in CGA and Hercules modes:

Emulation	Mode	H Reg Set	V Reg Set
CGA	320x200	Alternate	Regular
CGA	640x200	Regular	Regular
Hercules	Text	Regular	Regular
Hercules	Graphics	Alternate	Regular

The BIOS supplied by Chips & Technologies can be used to initialize both sets of registers.

COMPATIBILITY MODE PROGRAMMING

To enable backward compatibility, the chip is programmed as follows:

VGA Mode

A. Program the 82C453 exactly analogous to IBM's VGA. Disable the additional bits in the new registers.

B. Select VGA mode (default).

EGA Mode

A. Program the 82C451/452 exactly analogous to IBM's VGA. Disable the additional bits in the new registers.

B. Write protect Group 4 registers. Also protect the external palette, clock select register, internal palette (if desired) and all CRT sync registers.

C. Force all 10th bits of vertical counters (including line compare) to 0.

D. Select the EGA type frame interrupt. This is controlled with bit-7 of Emulation Mode Register.

CGA Mode

A. Program the regular CRT registers for the 640 pixels horizontal mode. The horizontal sync rate must be consistent with the monitor used. Program the Alternate Horizontal Register for 320 pixels horizontal mode.

B. The vertical resolution can be 200 or 400 lines. The vertical sync rate must be consistent with the monitor used.

C. Load the font in the memory .

D. Pre-program all registers in Sequencer, Attribute Controller and Graphics Controller as in Mode 2.

E. Set the sync polarity as required for 200 or 400 lines.

F. Enable Double Scanning (if required by the monitor).

G. Program the CGA Mode Control Register (3D8h) and Color Palette Register (3D9h) as required. These registers are implemented in hardware.

H. Write Protect Group 1, Group 3, and Group 4 registers.

I. Select CGA mode.

The 82C453 will automatically respond to 320/640 pixels/line and text/graphics mode as defined in the CGA Mode Control Register (3D8h). In 40 column CGA modes, the alternate CRTC registers are used.

MDA Mode

A. Program the regular CRT registers in the 720 pixels horizontal mode with 9 pixels/character. The horizontal sync rate must be consistent with the monitor used.

B. The vertical resolution must be 350 lines. The vertical sync rate must be consistent with the monitor used.

C. Load the font in memory .

D. Pre-program all registers in Sequencer, Attribute Controller and Graphics Controller as in Mode 7.

E. Set the sync polarity as required for 350 lines.

F. Write Protect Group 1, Group 3, and Group 4 registers.

G. Select MDA mode.

H. Hercules Control Registers do not work in this mode.

HERCULES Mode

A. Program the regular CRT registers for 720 pixels horizontal mode with 9 dots/character. Program the alternate registers for 720 pixels with 8 dots/character. The clock divide parameter must be set to divide by 8 (not 9).

B. The vertical resolution must be 350 lines. The vertical sync rate must be consistent with the monitor used. The vertical display end must be programmed to 350 Lines (Text Mode). In Graphics mode, 2 lines will automatically be subtracted. The Vertical Sync and Blank parameters must be programmed greater than 350 lines.

C. Load the font in the memory.

D. Pre-program all registers in the Sequencer, Attribute Controller, and Graphics Controller as in Mode 7. The 8/9 divide bit in the sequencer must be set to divide by 8.

E. Set the sync polarity as required for 350 lines.

F. Program the Display Mode Control Register (3B8h) and Hercules Configuration Register (3BFh) as required. These registers are implemented in hardware.

G. Write Protect Group 1, Group 2, and Group 3 registers.

H. Select Hercules mode.

The 82C453 will automatically respond to text, half graphics and full graphics modes as defined in the Mode Control Registers (3B8h and 3BFh). The regular CRT Offset Register is used in Hercules text mode. In Hercules graphics mode, the offset is defined in the Alternate Offset and Auxiliary Offset Registers. The Alternate Horizontal Registers are used in the Hercules Graphics mode.

When Emulation is enabled and the extended registers are disabled, bits 1 and 2 of the CRTC Register addresses are ignored (Similar to CGA and Hercules). The CRTC Registers occupy addresses 3B0h - 3B7h (3D0h - 3D7h).

LIGHT PEN REGISTERS

In the CGA and Hercules modes, the contents of the Display Address counter is saved at the end of the frame before being reset. The saved value can be read in the CRT Controller Register space 10h and 11h. This allows simulating the Light Pen Hit technique to detect text/graphics modes on the CGA/Hercules cards.

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82C453 Application Schematic Examples

This section includes schematic examples showing how to connect the 82C453 chip. The schematics are broken down into four main groups for discussion:

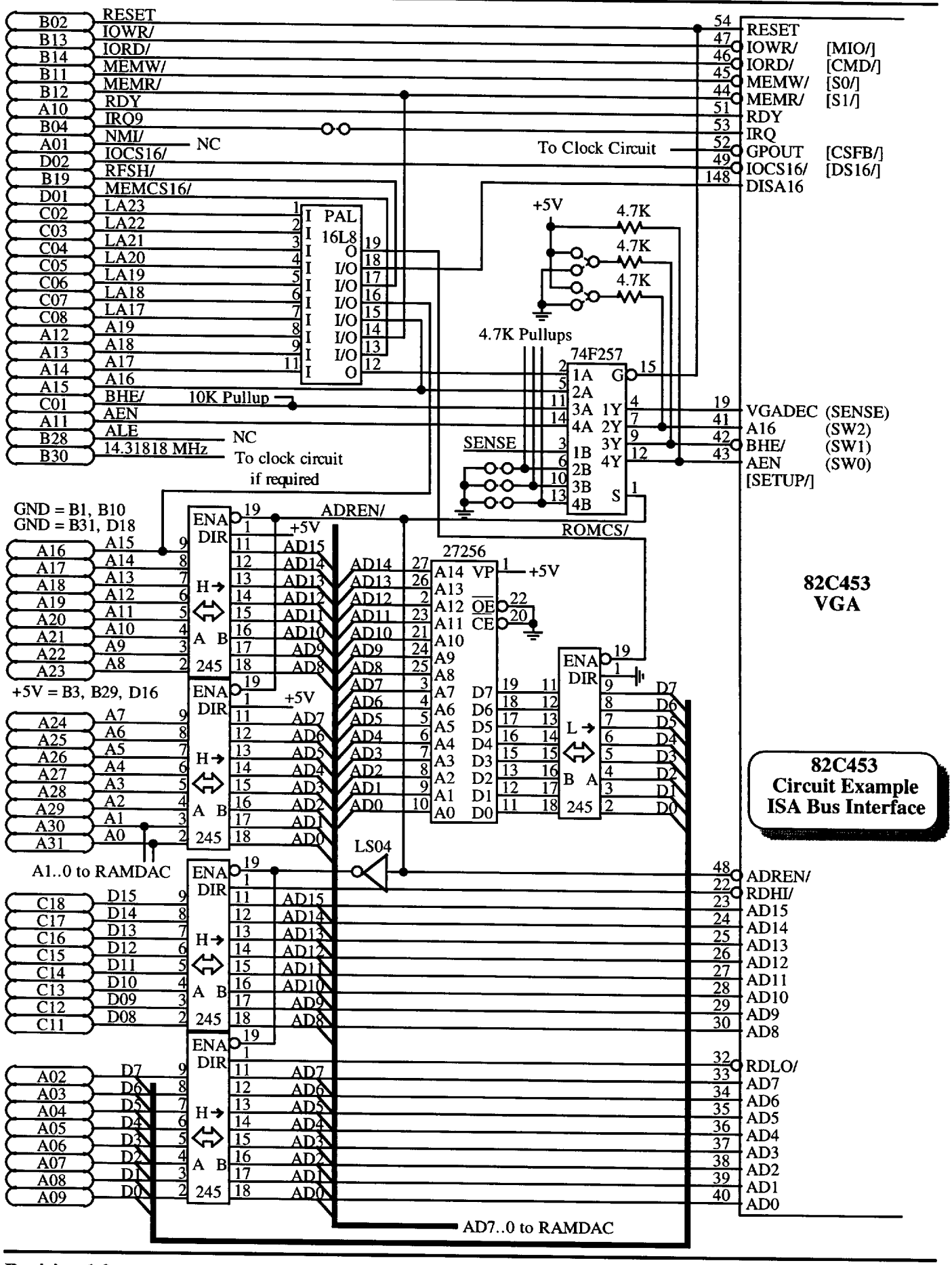
1) System Bus Interface
2) Display Memory Interface
3) Video Interface
4) Clock Interface

These equations are for a 16-bit EISA/ISA interface with 8-bit BIOS (schematic included in this section):

```
/** Inputs **/

Pin 1 = LA23   ;
Pin 2 = LA22   ;
Pin 3 = LA21   ;
Pin 4 = LA20   ;
Pin 5 = LA19   ;
Pin 6 = LA18   ;
Pin 7 = LA17   ;
Pin 8 = SA19   ;
Pin 9 =  SA18  ;
Pin 11 =SA17   ;
Pin 14 = !SMEMR
Pin 15 = SA16  ;
Pin 16 = SA15  ;
Pin 17 = !RFSH   ;
Pin 18 = DISA16  ;

/** Outputs **/

Pin 13 = !MMCS16  ;
Pin 12 = VGADEC   ;
Pin 19 = !ROMCS   ;

/** Declarations and Intermediate Variable Definitions **/

RAMADD = !LA23 & !LA22 & !LA21 & !LA20 & LA19 & !LA18 & LA17 ;

/** Logic Equations **/

MMCS16.OE = RAMADD & !RFSH ; (for 16-bit only)

MMCS16 = !DISA16 ; (for 16-bit only)

VGADEC = SA19 & !SA18 & SA17 & !RFSH;

ROMCS = SA19 & SA18 & !SA17 & !SA16 & !SA15 & !RFSH & SMEMR;
```

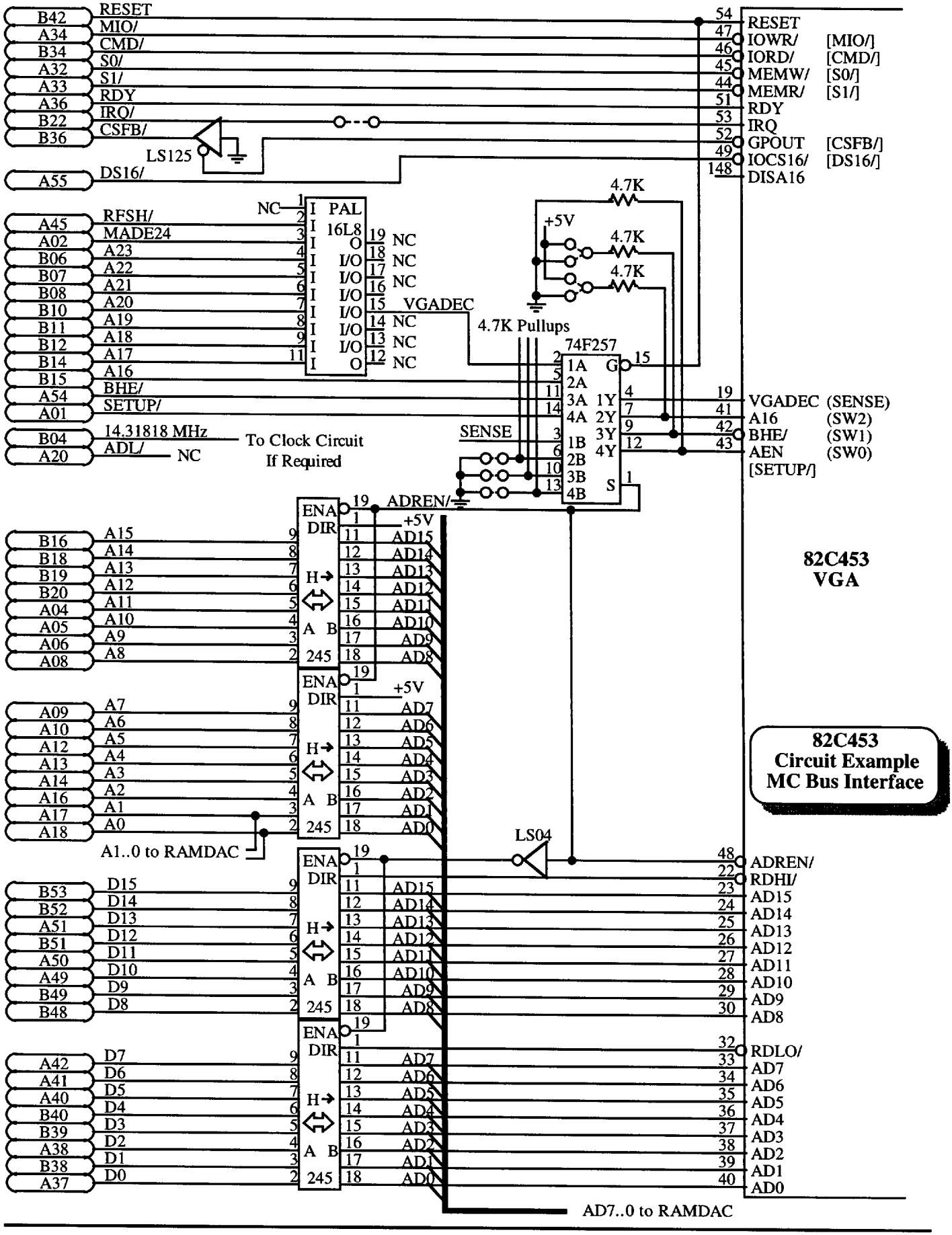
These equations are for a 16-bit EISA/ISA interface with 16-bit BIOS:

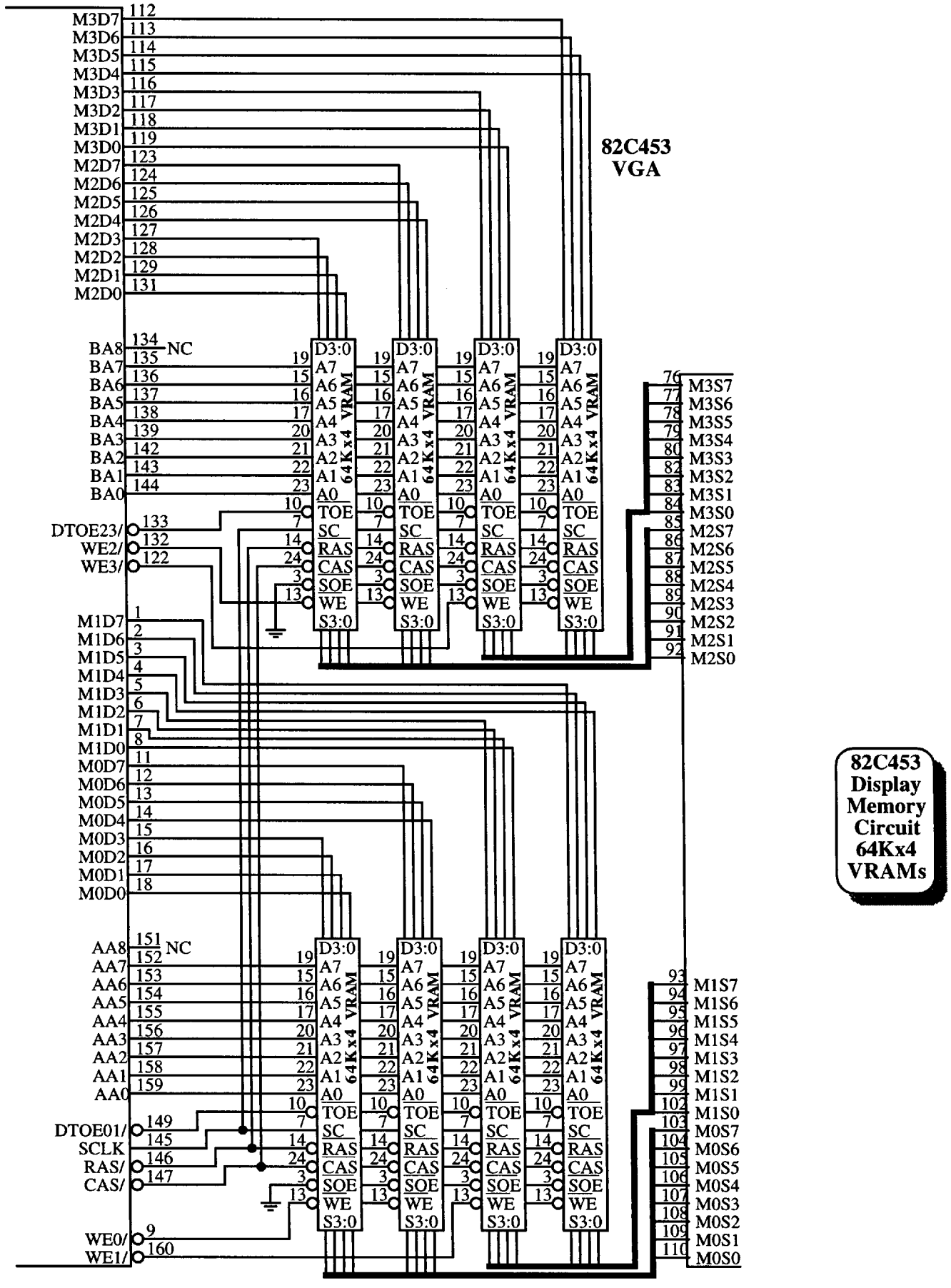
```
/** Inputs **/

Pin 1 = LA23    ;
Pin 2 = LA22    ;
Pin 3 = LA21    ;
Pin 4 = LA20    ;
Pin 5 = LA19    ;
Pin 6 = LA18    ;
Pin 7 = LA17    ;
Pin 8 = SA19    ;
Pin 9 =  SA18   ;
Pin 11 =SA17    ;
Pin 14 = !SMEMR
Pin 15 = SA16   ;
Pin 16 = SA15   ;
Pin 17 = !RFSH    ;
Pin 18 = DISA16   ;

/** Outputs **/

Pin 13 = !MMCS16  ;
Pin 12 = VGADEC   ;
Pin 19 = !ROMCS   ;

/** Declarations and Intermediate Variable Definitions **/

RAMADD = !LA23 & !LA22 & !LA21 & !LA20 & LA19 & !LA18 & LA17 ;

ROMADD = !LA23 & !LA22 & !LA21 & !LA20 & LA19 & LA18 & !LA17 & !SA16 & !SA15 ;

/** Logic Equations **/

MMCS16.OE = RAMADD & !RFSH + ROMADD & !RFSH ;

MMCS16 = !DISA16 ;

VGADEC = SA19 & !SA18 & SA17 & !RFSH;

ROMCS = SA19 & SA18 & !SA17 & !SA16 & !SA15 & !RFSH & SMEMR;
```



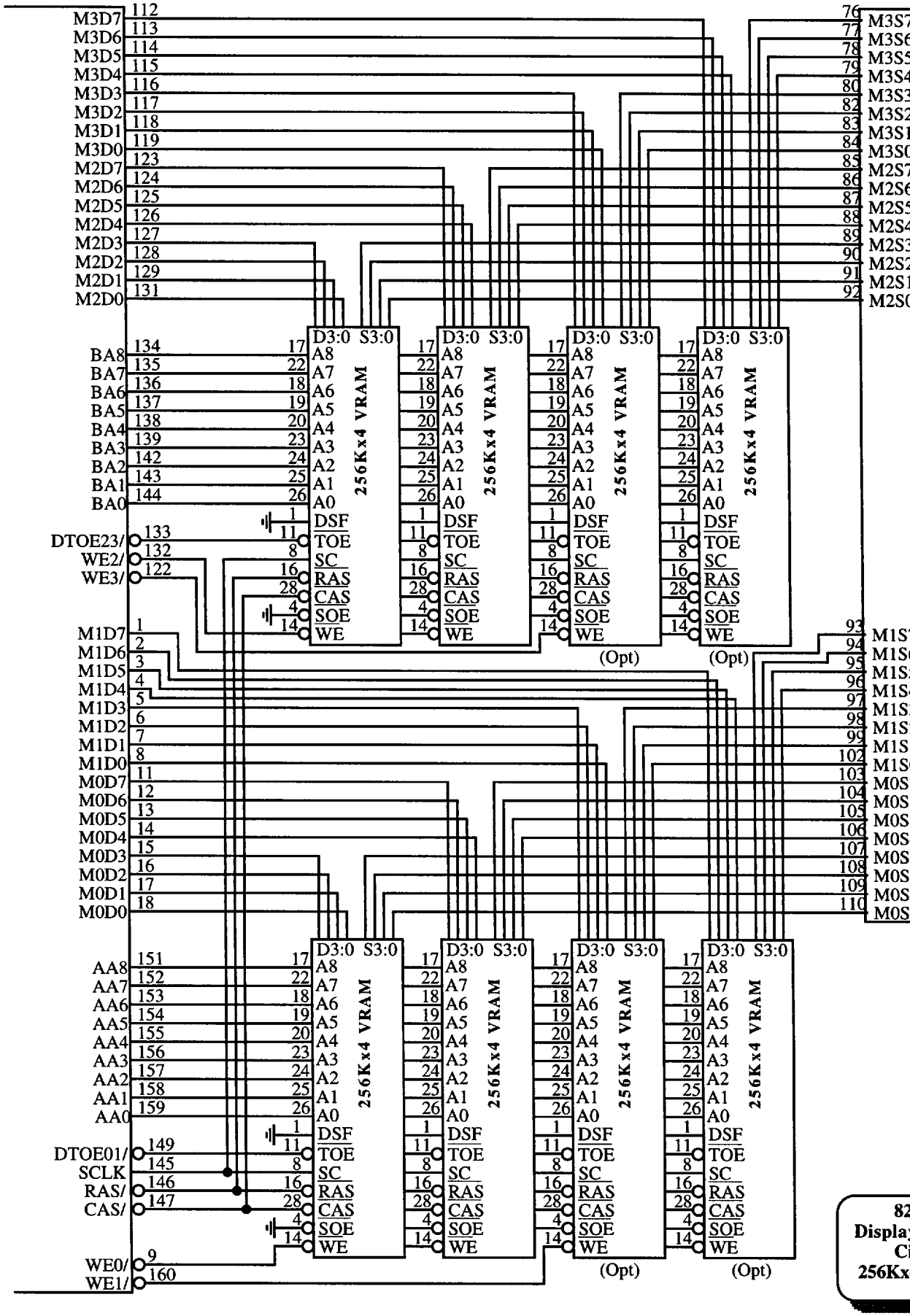
These equations are for a 16-bit Micro Channel Bus Interface (schematic included in this section):

```
/** Inputs **/

Pin 2 = RFSH/       ;
Pin 3 = MADE24      ;
Pin 4 = A23         ;
Pin 5 = A22         ;
Pin 6 = A21         ;
Pin 7 = A20         ;
Pin 8 = A19         ;
Pin 9 =  A18        ;
Pin 11 = A17        ;

/** Output **/

Pin 15 = VGADEC   ;

/** Logic Equations **/

VGADEC = MADE24 & !A23 & !A22 &!A21 &!A20 & A19 &!A18 & A17 & !RFSH;
```

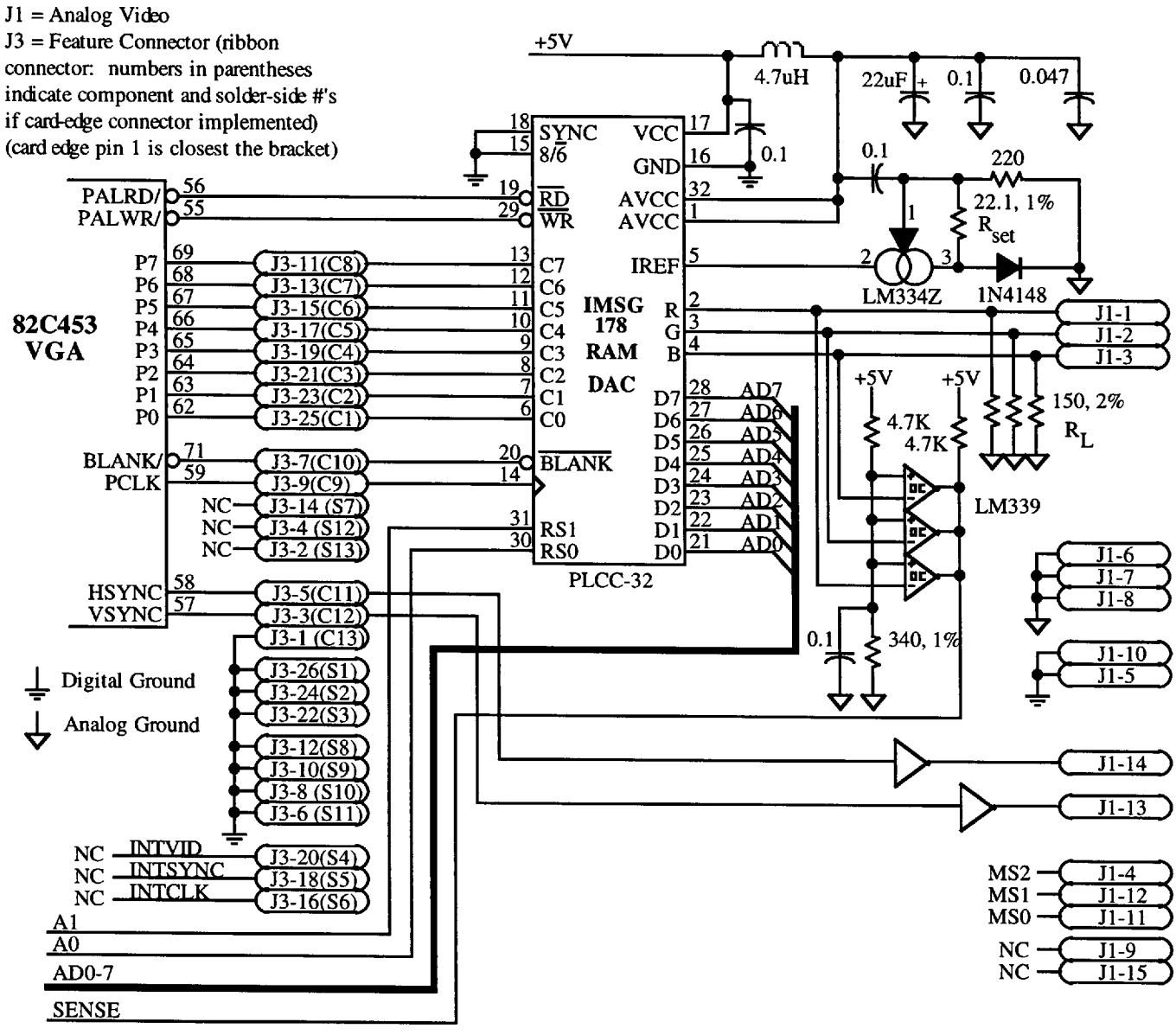




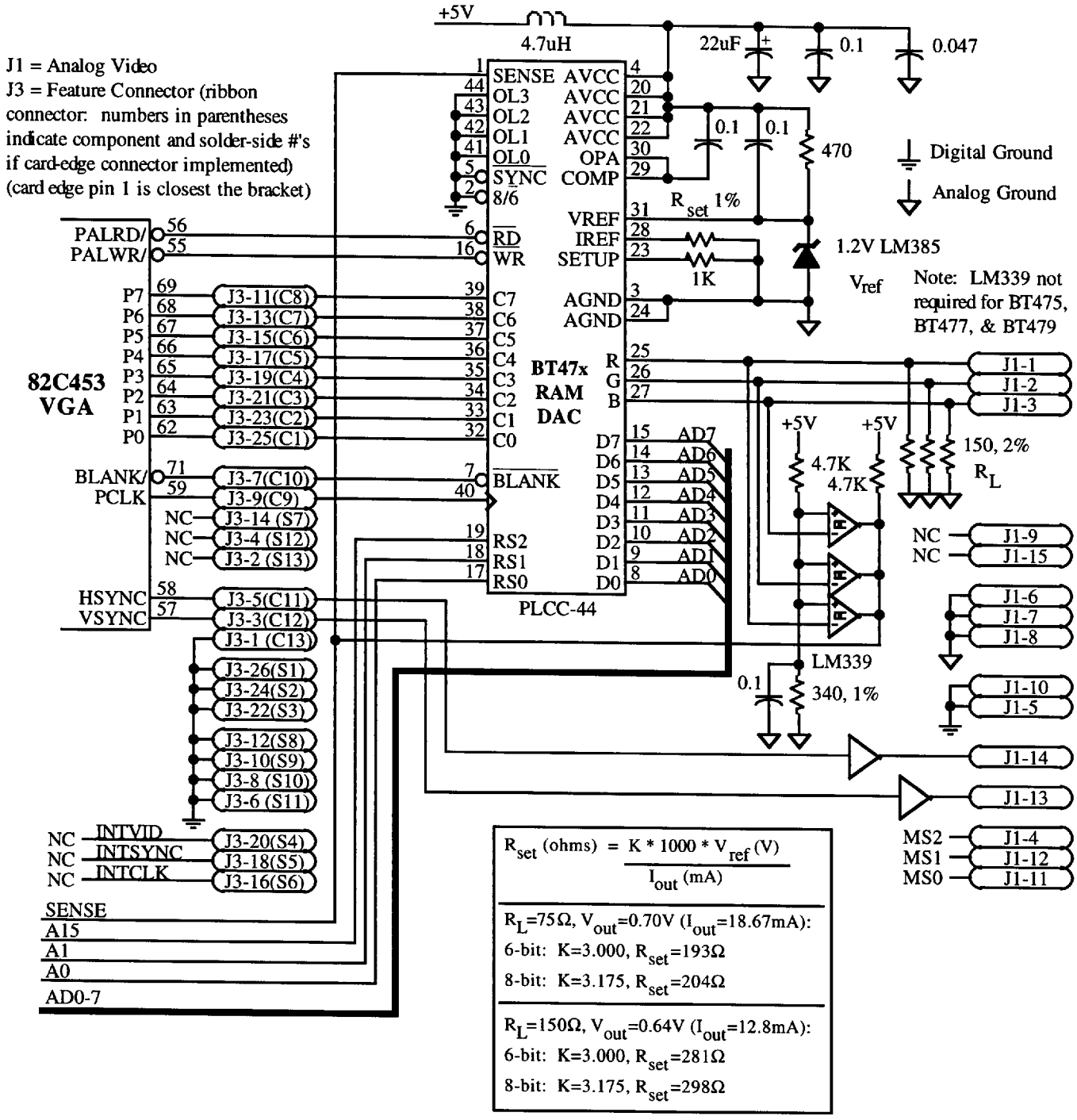
82C453 Display Memory Circuit 64Kx4 VRAMs



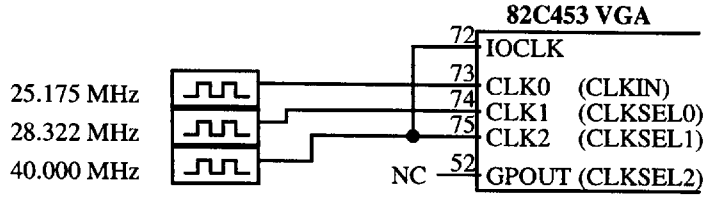
82C453 Display Memory Circuit 256Kx4 VRAMs



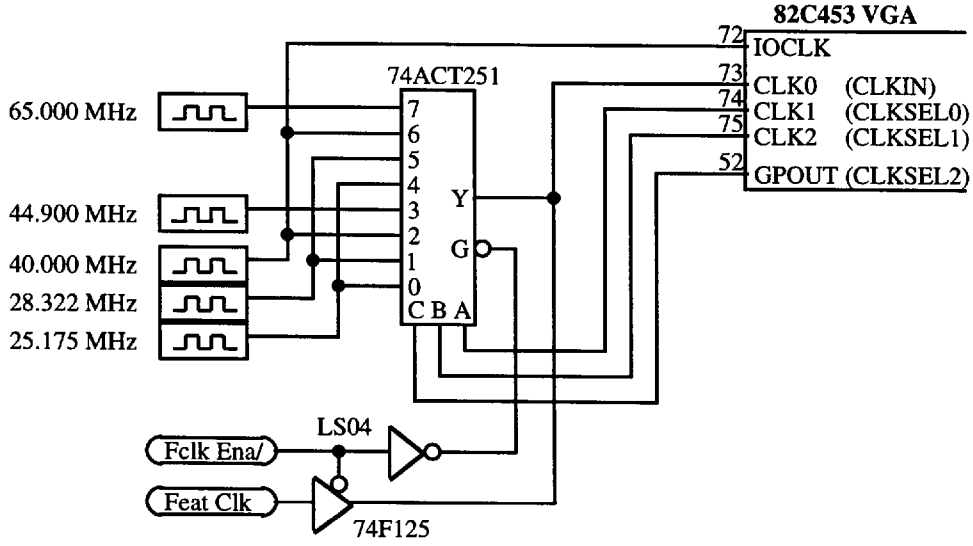
82C453 Video Circuit Example - External Color Palette (Inmos IMSG176 / 178)



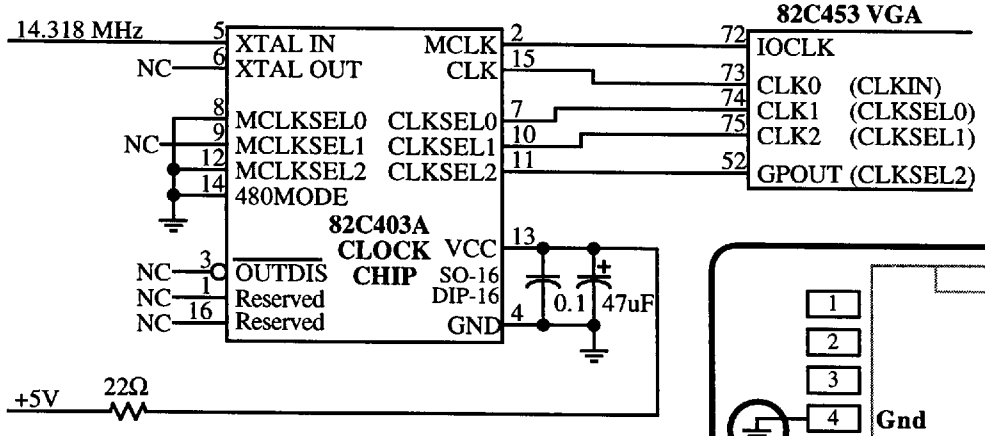
82C453 Video Circuit Example - External Color Palette (Brooktree BT471 / 475 / 477 / 478 / 479)

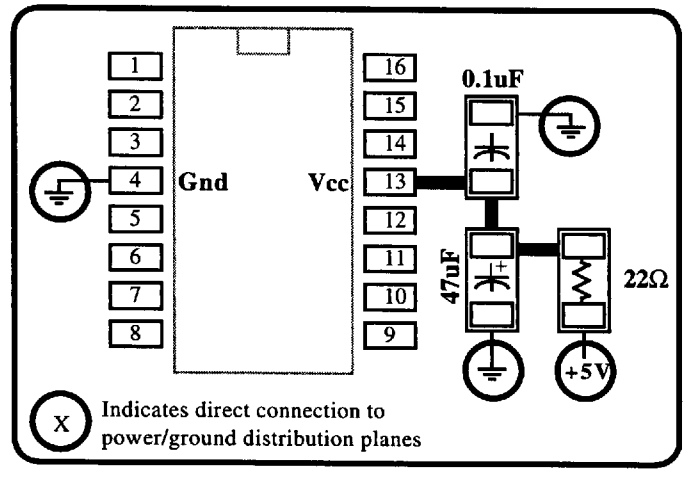


82C453 Clock Circuit Example - Minimum Oscillator Configu-



82C453 Clock Circuit Example - Full Oscillator Configuration





82C453 Clock Circuit Example
82C403A Clock Chip Configuration and Recommended PCB Layout

82C453 Electrical Specifications

82C453 ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	1	W
V_{CC}	Supply Voltage	–0.5	–	7	V
V_I	Input Voltage	–0.5	–	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	–	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	–	85	°C
T_{STG}	Storage Temperature	–40	–	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

82C453 NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	–	5.5	V
T_A	Ambient Temperature	0	–	70	°C

82C453 DC CHARACTERISTICS

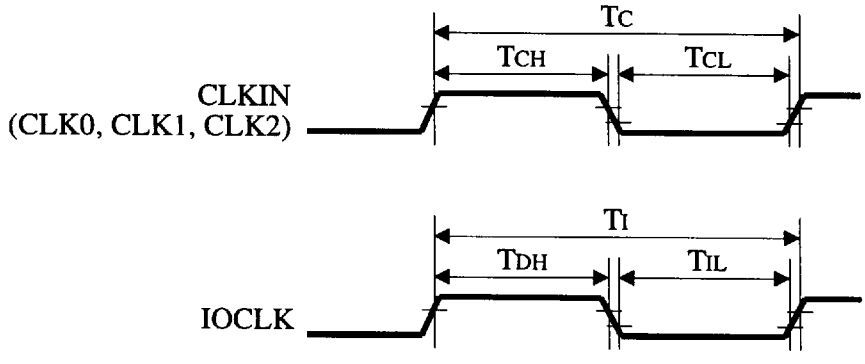
(Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Max	Units
I_{CC1}	Power Supply Current	@28.332 MHz CLK, 0°C, 5.5V	–	150	mA
I_{IL}	Input Leakage Current		–10	+10	uA
I_{OZ}	Output Leakage Current	High Impedance	–10	+10	uA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	IOL = 8 mA (IRQ, RDY, DS16/, RAS/, CAS/)	–	0.45	V
	(@4.5V)	IOL = 4 mA (all others)	–	0.45	V
V_{OH}	Output High Voltage	IOL = –8 mA (IRQ, RDY, DS16/, RAS/, CAS/)	2.4	–	V
	(@4.5V)	IOH = –4 mA (all others)	2.4	–	V

Electrical specifications contained herein are preliminary and subject to change without notice.

82C453 AC TIMING CHARACTERISTICS - CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_C	CLK Period	65 MHz	15.4	–	–	nS
T_{CH}	CLK High Time		$0.45T_C$	–	$0.55T_C$	nS
T_{CL}	CLK Low Time		$0.45T_C$	–	$0.55T_C$	nS
T_I	IOCLK Period	30-40 MHz	25	–	33	nS
T_{IH}	IOCLK High Time		$0.45T_I$	–	$0.55T_I$	nS
T_{IL}	IOCLK Low Time		$0.45T_I$	–	$0.55T_I$	nS
T_{RF}	Clock Rise / Fall		–	–	$0.05T_C$	nS



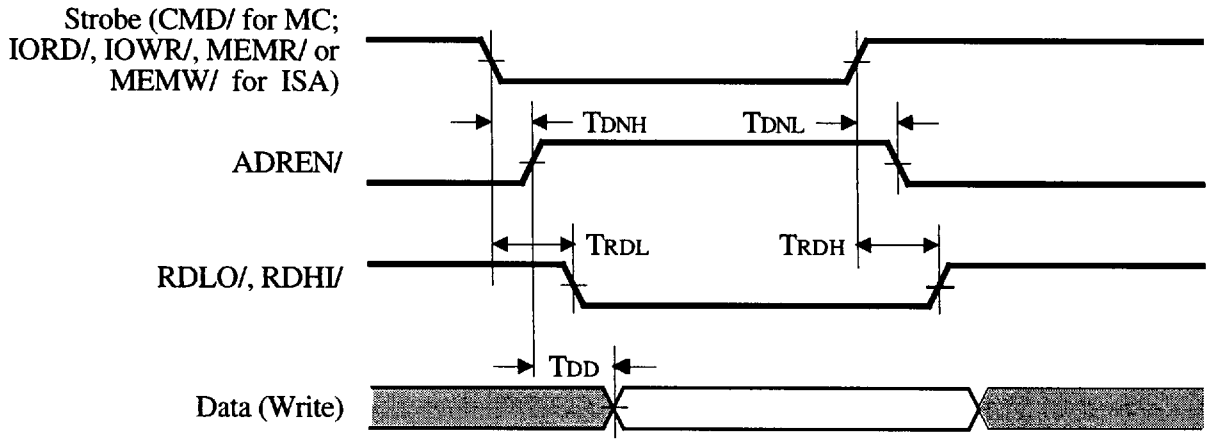
82C453 Clock Timing

82C453 AC TIMING CHARACTERISTICS - RESET TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
–	RESET Pulse Width		64 T_C	–	–	nS

82C453 AC TIMING CHARACTERISTICS - AD BUS MULTIPLEXER TIMING

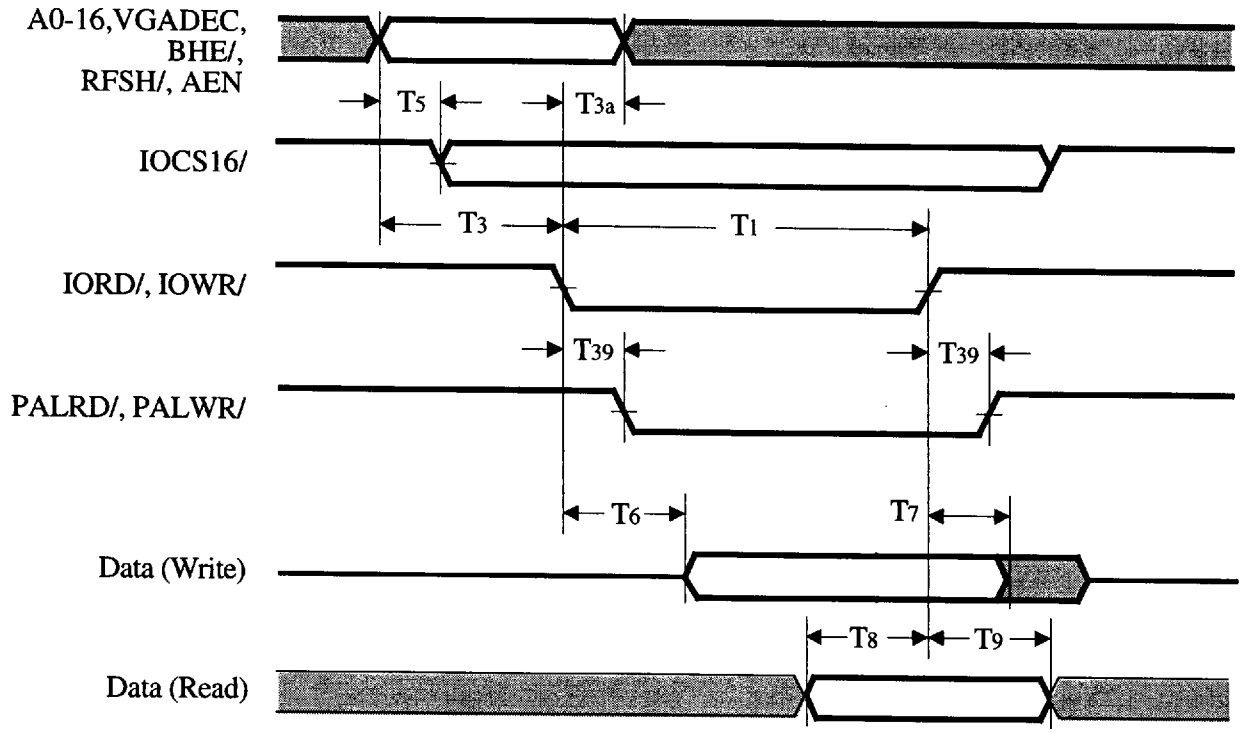
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{DNH}	Strobe falling to ADREN/ rising		–	–	15	nS
T_{DNL}	Strobe rising to ADREN/ falling		–	–	15	nS
T_{RDL}	Strobe falling to RDLO/ and/or RDHI/ falling		–	–	20	nS
T_{RDH}	Strobe rising to RDLO/ and/or RDHI/ rising		–	–	20	nS
T_{DD}	ADREN/ rising to write data driven		–	–	20	nS



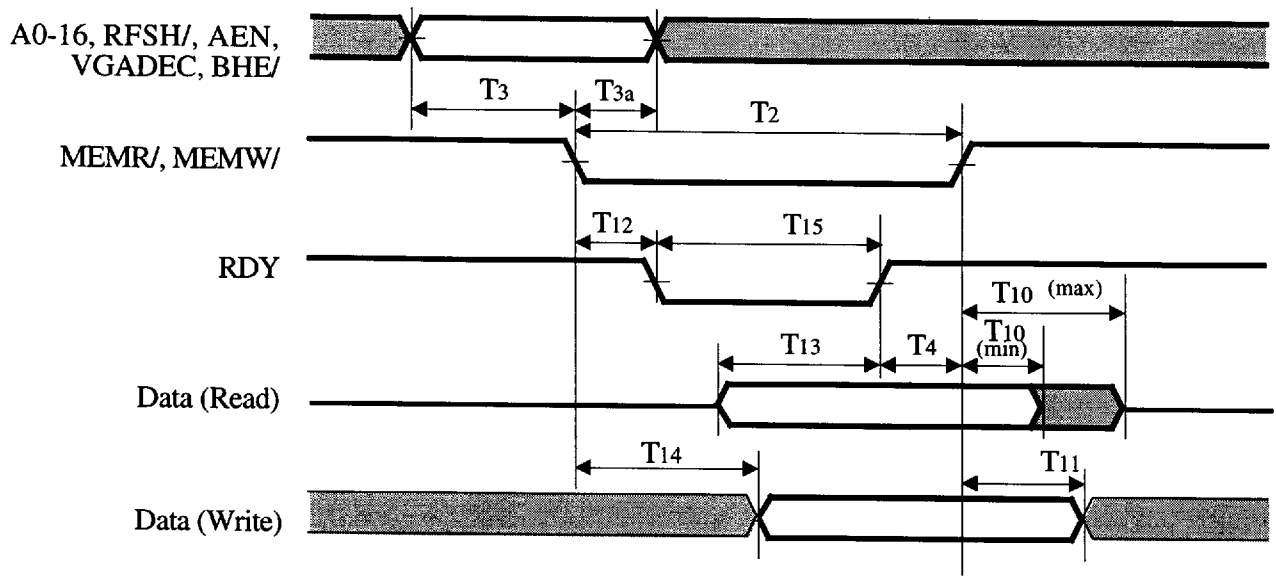
82C453 AD Bus Multiplexer Timing

82C453 AC TIMING CHARACTERISTICS - EISA/ISA BUS TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T1	IORD/, IOWR/ Pulse Width		175	–	–	nS
T2	MEMR/, MEMW/ Pulse Width		175	–	–	nS
T3	Address setup to Read/Write		80	–	–	nS
T3a	Address hold from Read/Write Signal		20	–	–	nS
T4	MEMR/, MEMW/ hold from RDY (Memory)		0	–	–	nS
T5	IOCS16/ Delay from valid address		–	–	40	nS
T6	I/O Read Data delay from IORD/		–	–	50	nS
T7	I/O Read Data hold from IORD/		5	–	40	nS
T8	I/O Write Data setup to IOWR/		40	–	–	nS
T9	I/O Write Data hold from IOWR/		10	–	–	nS
T10	Memory Read Data hold from MEMR/		10	–	40	nS
T11	Memory Write Data hold from MEMW/		0	–	–	nS
T12	MEMR/, MEMW/ to RDY Low delay		–	–	25	nS
T13	Memory Read Data setup to RDY		25	–	–	nS
T14	Memory Write Data delay from MEMW/		40	–	–	nS
T15	RDY width		$1T_C$	–	$128T_C$	nS
T39	PALRD/, PALWR/ delay from Read/Write		–	–	20	nS



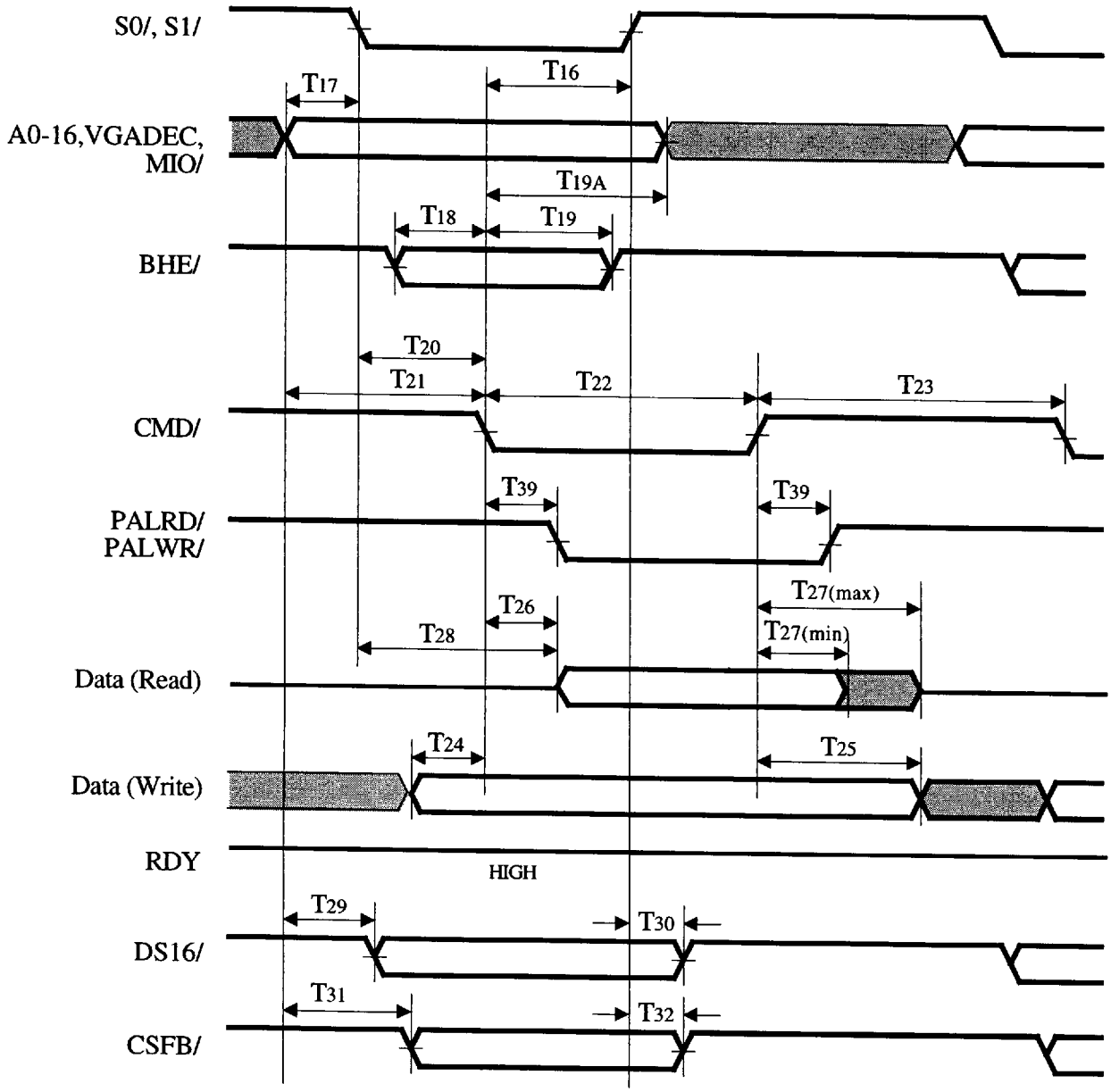
EISA/ISA Bus I/O Cycle Timing



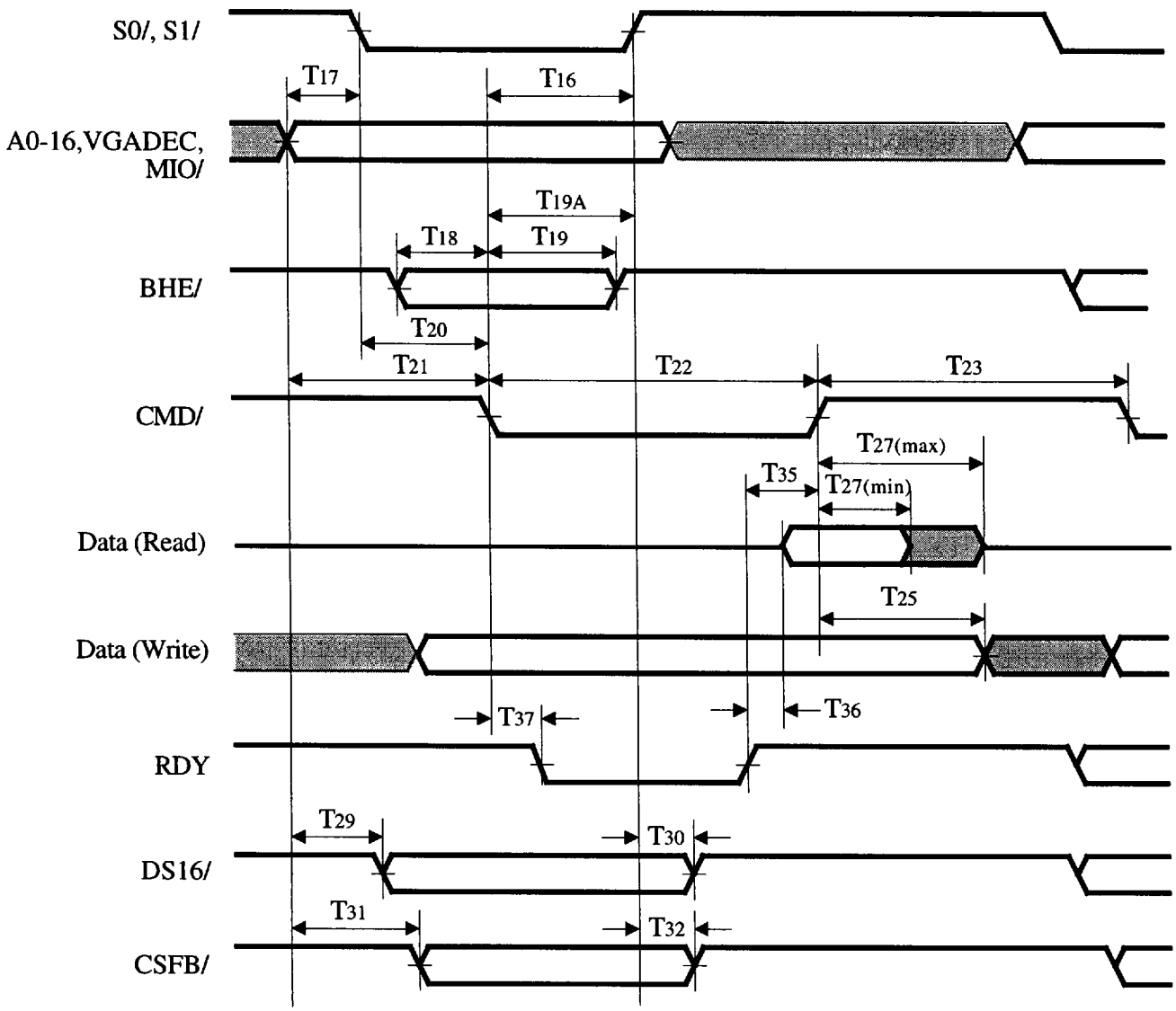
EISA/ISA Bus Memory Cycle Timing

82C453 AC TIMING CHARACTERISTICS - MC BUS TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T16	Status hold from CMD/		20	–	–	nS
T17	Status active from address valid		0	–	–	nS
T18	BHE/ Setup to CMD/		30	–	–	nS
T19	BHE/ hold from CMD/		20	–	–	nS
T19A	Address hold from CMD/		25	–	–	nS
T20	CMD/ active from Status		30	–	–	nS
T21	CMD/ from address valid		80	–	–	nS
T22	CMD/ Pulse Width		90	–	–	nS
T23	CMD/ inactive to next CMD/		80	–	–	nS
T24	Write data setup to CMD/		0	–	–	nS
T25	Write data hold from CMD/		10	–	–	nS
T26	Read data valid from CMD/		–	–	50	nS
T27	Read data hold from CMD/		5	–	40	nS
T28	Status to Read data valid		–	–	125	nS
T29	DS16/ active from address valid		–	–	25	nS
T30	DS16/ inactive from Status		5	–	25	nS
T31	CSFB/ active from address valid		–	–	25	nS
T32	CSFB/ inactive from Status		5	–	25	nS
T35	RDY rising edge to CMD/ rising edge		0	–	–	nS
T36	Read data from RDY high		–	–	50	nS
T37	RDY low delay from CMD/		–	–	25	nS
T39	PALRD/, PALWR/ delay from CMD/		–	–	20	nS



MC Bus I/O Cycle Timing



MC Bus Memory Cycle Timing

82C453 AC TIMING CHARACTERISTICS - DISPLAY MEMORY (VRAM)

VRAM TIMING - CLOCK USED FOR MEMORY TIMING

Symbol	Parameter	Min	Typ	Max	Units
T_{SC}	Sequencer Clock (Note 1)	–	T_C	–	nS

Note 1: Internal Sequencer Clock is used for memory timings. Sequencer Clock is equal to dot clock in all the modes except 1024x768 interlaced mode. In 1024x768 mode $T_{SC} = T_C/2$.

VRAM TIMING - MEMORY ACCESS TIME REQUIREMENTS

Symbol	Parameter	Min	Typ	Max	Units
T_{RAC}	Data Access Time from RAS/	–	–	4 T_{SC}	nS
T_{CAC}	Data Access Time from CAS/	–	–	T_{SC}	nS
T_{OEA}	Data Access Time from OE/	–	–	T_{SC}	nS
T_{AA}	Data Access Time from Column Address	–	–	3 T_{SC}	nS

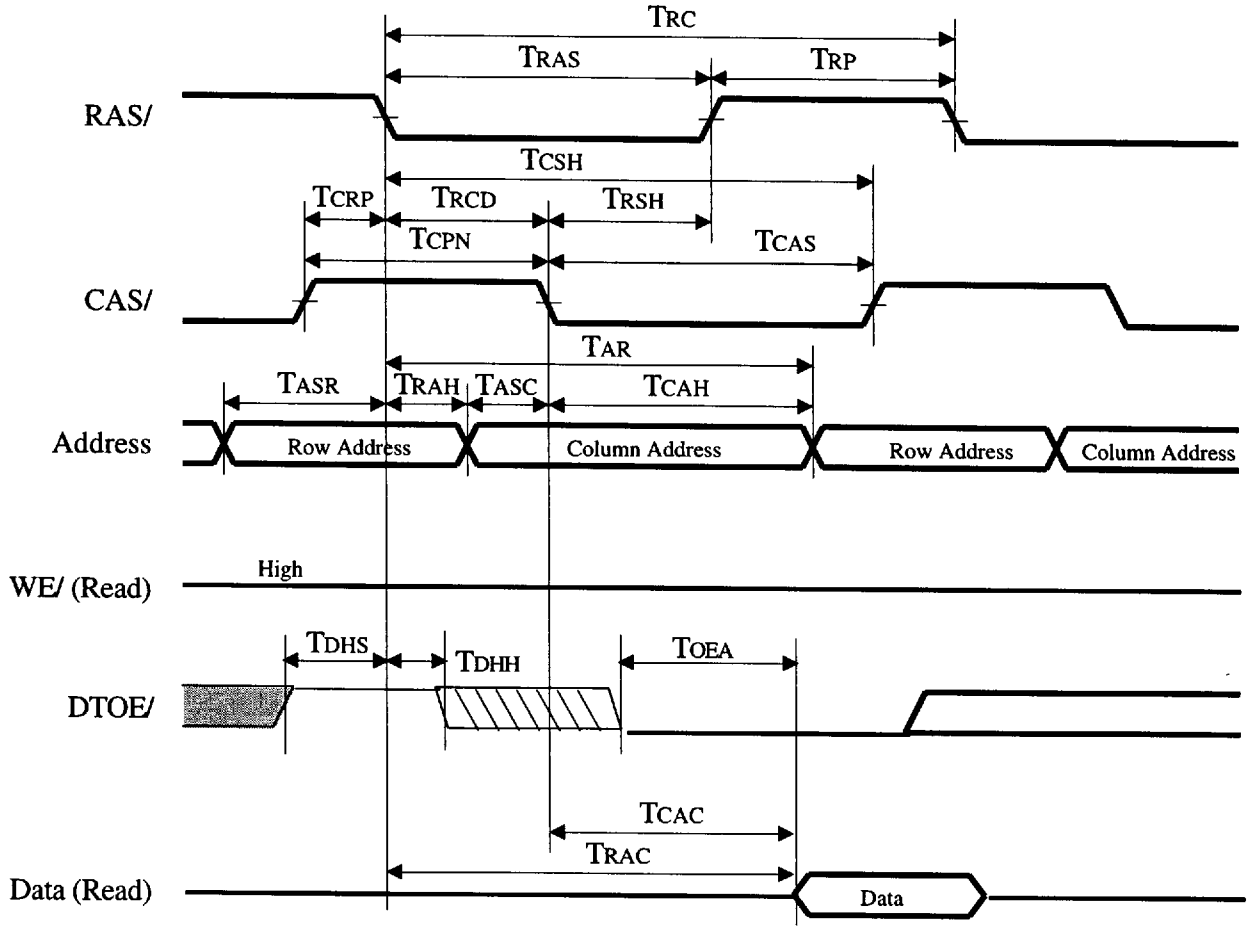
VRAM TIMING - TIMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Units
T_{RC}	Cycle Time (Randome Read or Write)	7 T_{SC}	–	–	nS
T_{RWC}	Cycle Time (Read-Modify-Write Cycle)	12 T_{SC}	–	–	nS
T_{PC}	Cycle Time (Fast Page Cycle)	3 T_{SC}	–	–	nS
T_{PRWC}	Cycle Time (Fast Page Read-Modify-Write Cycle)	12 T_{SC}	–	–	nS
T_{RP}	RAS/ Precharge	3 T_{SC}	–	–	nS
T_{RAS}	RAS/ Pulse Width	4 T_{SC}	–	–	nS
T_{RASP}	RAS/ Pulse Width (Fast Page Cycle)	8 T_{SC}	–	–	nS
T_{RSH}	RAS/ Hold from CAS/	2 T_{SC}	–	–	nS
T_{CPN}	CAS/ Precharge	3 T_{SC}	–	–	nS
T_{CP}	CAS/ Precharge (Fast Page Cycle)	T_{SC}	–	–	nS
T_{CAS}	CAS/ Pulse Width	4 T_{SC}	–	–	nS
T_{CAS1}	CAS/ Pulse Width (Fast Page Cycle)	3 T_{SC}	–	–	nS
T_{CAS2}	CAS/ Pulse Width (Fast Page Cycle)	2 T_{SC}	–	–	nS
T_{CAS1}	CAS/ Pulse Width (Read Modify Write)	6 T_{SC}	–	–	nS
T_{CAS2}	CAS/ Pulse Width (Read Modify Write)	7 T_{SC}	–	–	nS
T_{CSH}	CAS/ Hold from RAS/	5 T_{SC}	–	–	nS
T_{RCD}	CAS/ Delay from RAS/	2 T_{SC}	–	–	nS
T_{CRP}	CAS/ High to RAS/ Low	T_{SC}	–	–	nS
T_{ASR}	Row Address Setup	T_{SC}	–	–	nS
T_{RAH}	Row Address Hold	T_{SC}	–	–	nS

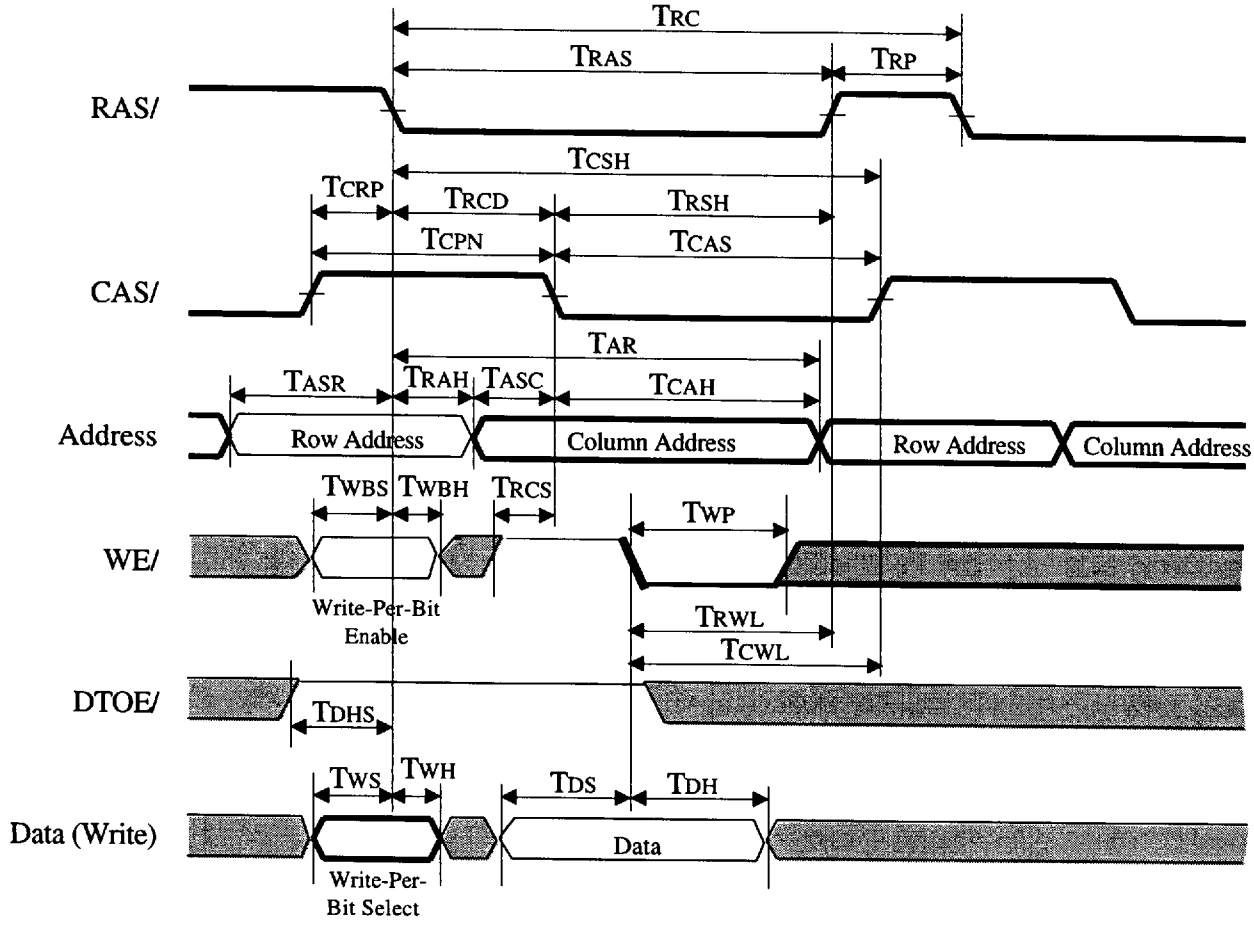
82C453 AC TIMING CHARACTERISTICS - DISPLAY MEMORY (VRAM)

VRAM TIMING - TIMING SPECIFICATIONS (continued)

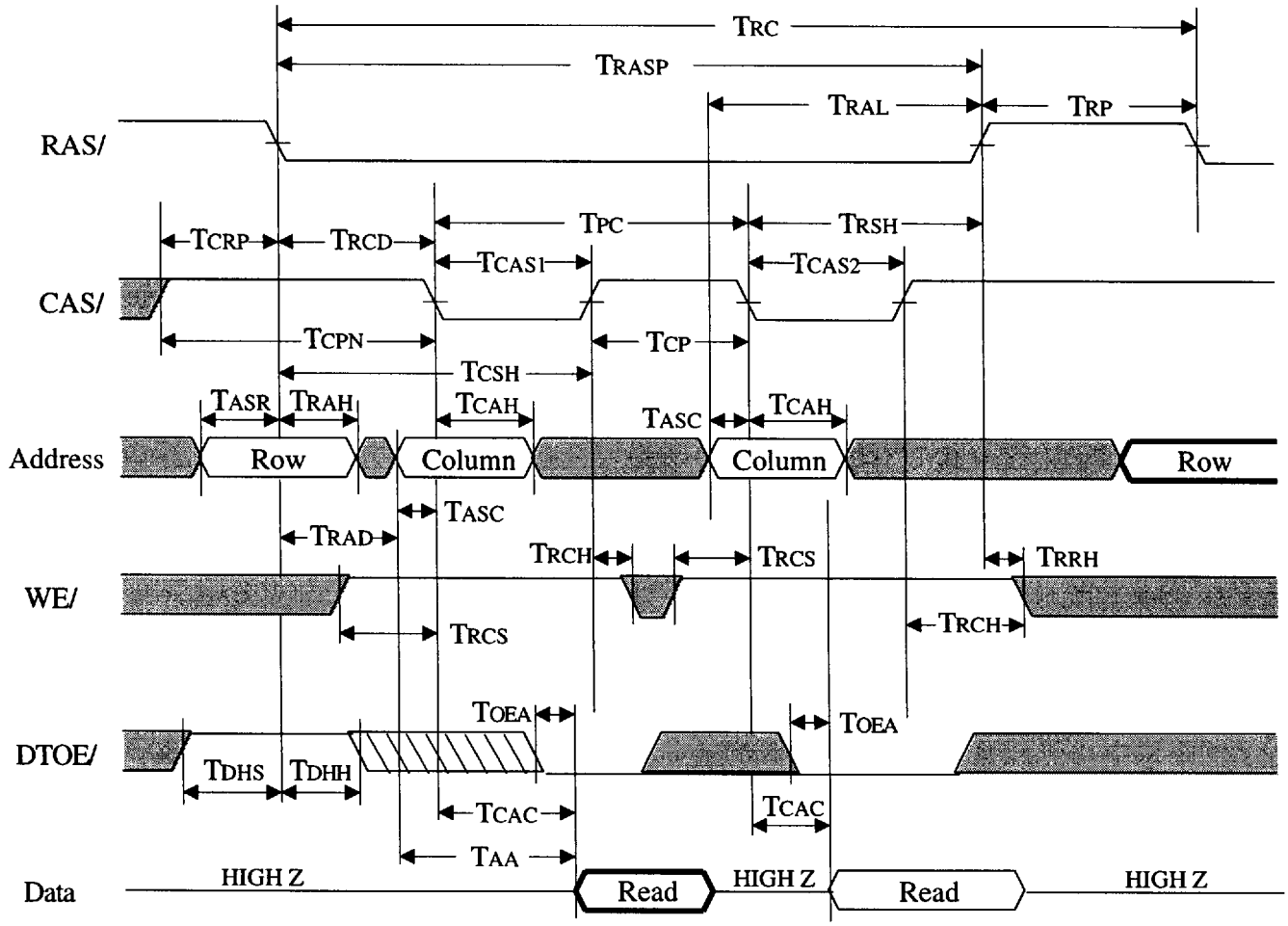
Symbol	Parameter	Min	Typ	Max	Units
T_{RAD}	Column Address Delay from RAS/	T_{SC}	–	45	nS
T_{RAL}	Column Address to RAS/ Lead Time	3 T_{SC}	–	–	nS
T_{ASC}	Column Address Setup to CAS/	T_{SC}	–	–	nS
T_{CAH}	Column Address Hold	T_{SC}	–	–	nS
T_{RCS}	Read Command Setup	3 T_{SC}	–	–	nS
T_{RRH}	Read Command Hold after RAS/ High	T_{SC}	–	–	nS
T_{RCH}	Read Command Hold after CAS/ High	T_{SC}	–	–	nS
T_{WP}	Write Command Pulse Width	3 T_{SC}	–	–	nS
T_{WP1}	Write Command Pulse Width (Fast Page Cycle)	3 T_{SC}	–	–	nS
T_{WP2}	Write Command Pulse Width (Fast Page Cycle)	2 T_{SC}	–	–	nS
T_{RWL}	Write Command to RAS/ Lead Time	2 T_{SC}	–	–	nS
T_{CWL}	Write Command to CAS/ Lead Time	2 T_{SC}	–	–	nS
T_{DS}	Data-in Setup	0.5 T_{SC}	–	–	nS
T_{DH}	Data-in Hold	T_{SC}	–	–	nS
T_{AWD}	WE/ Delay from Column Address	T_{SC}	–	–	nS
T_{CWD1}	WE/ Delay from CAS/ (Fast Page Cycle)	4 T_{SC}	–	–	nS
T_{CWD2}	WE/ Delay from CAS/ (Fast Page Cycle)	3 T_{SC}	–	–	nS
T_{RWD}	WE/ Delay from RAS/	6 T_{SC}	–	–	nS
T_{OED}	OE/ High to Data-in Setup Delay	0.5 T_{SC}	–	–	nS
T_{OEH}	OE/ High Hold after WE/ Low	T_{SC}	–	–	nS
T_{DLS}	DT/ Low Setup	0.5 T_{SC}	–	–	nS
T_{RDH}	DT/ Low Hold after RAS/ Low	3 T_{SC}	–	–	nS
T_{CDH}	DT/ Low Hold after CAS/ Low	1.5 T_{SC}	–	–	nS
T_{DHS}	DT/ High Setup	T_{SC}	–	–	nS
T_{DHH}	DT/ High Hold	T_{SC}	–	–	nS
T_{DTR}	DT/ High to RAS/ High Delay	0.5 T_{SC}	–	–	nS
T_{DTC}	DT/ High to CAS/ High Delay	2 T_{SC}	–	–	nS
T_{DTH}	DT/ High Hold after RAS/ High	2 T_{SC}	–	–	nS
T_{WBS}	Write-Per-Bit Setup	0.5 T_{SC}	–	–	nS
T_{WBH}	Write-Per-Bit Hold	T_{SC}	–	–	nS
T_{WS}	Write Bit Selection Setup	0.5 T_{SC}	–	–	nS
T_{WH}	Write Bit Selection Hold	T_{SC}	–	–	nS



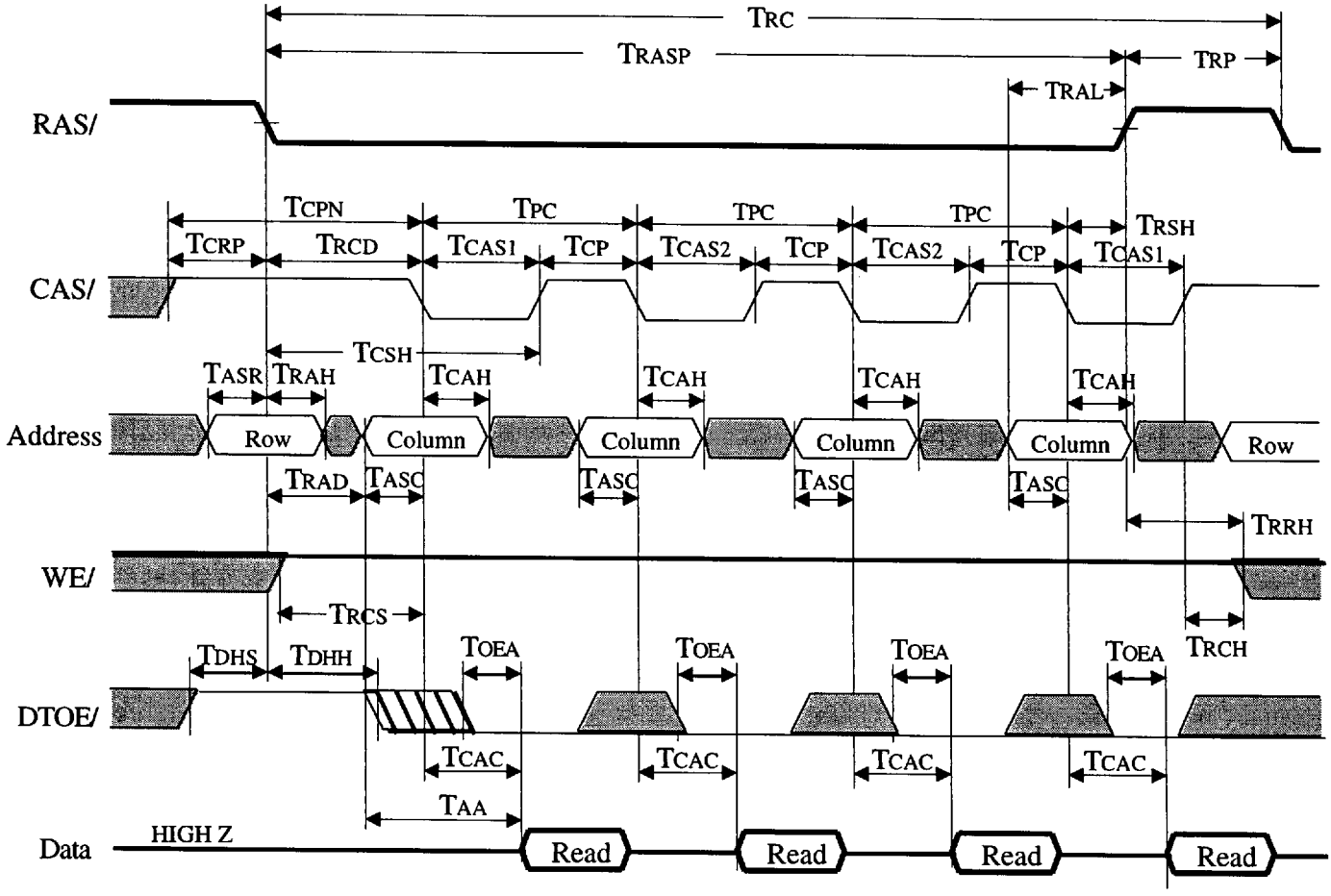
VRAM Random Read Cycle Timing



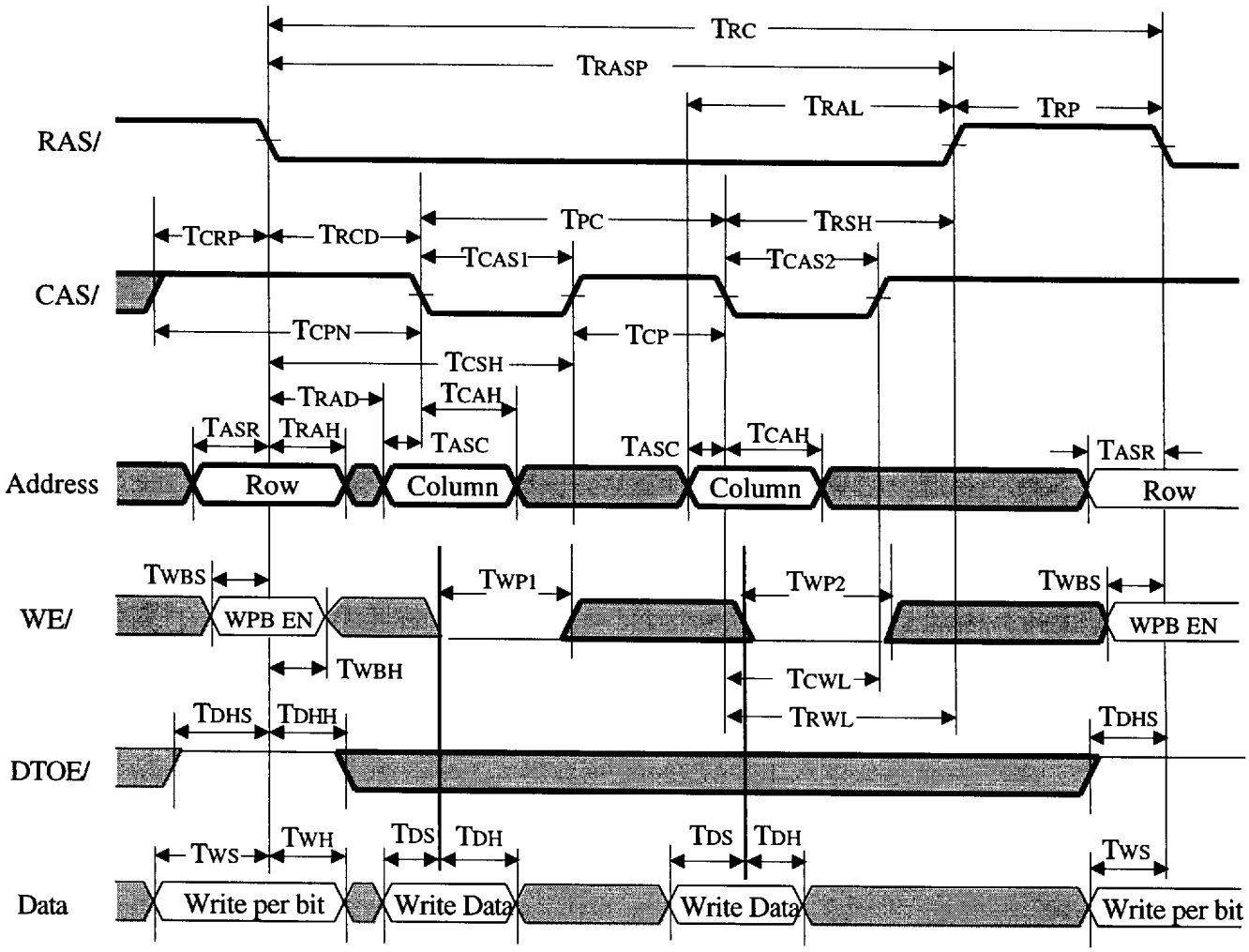
VRAM Random Write Cycle Timing



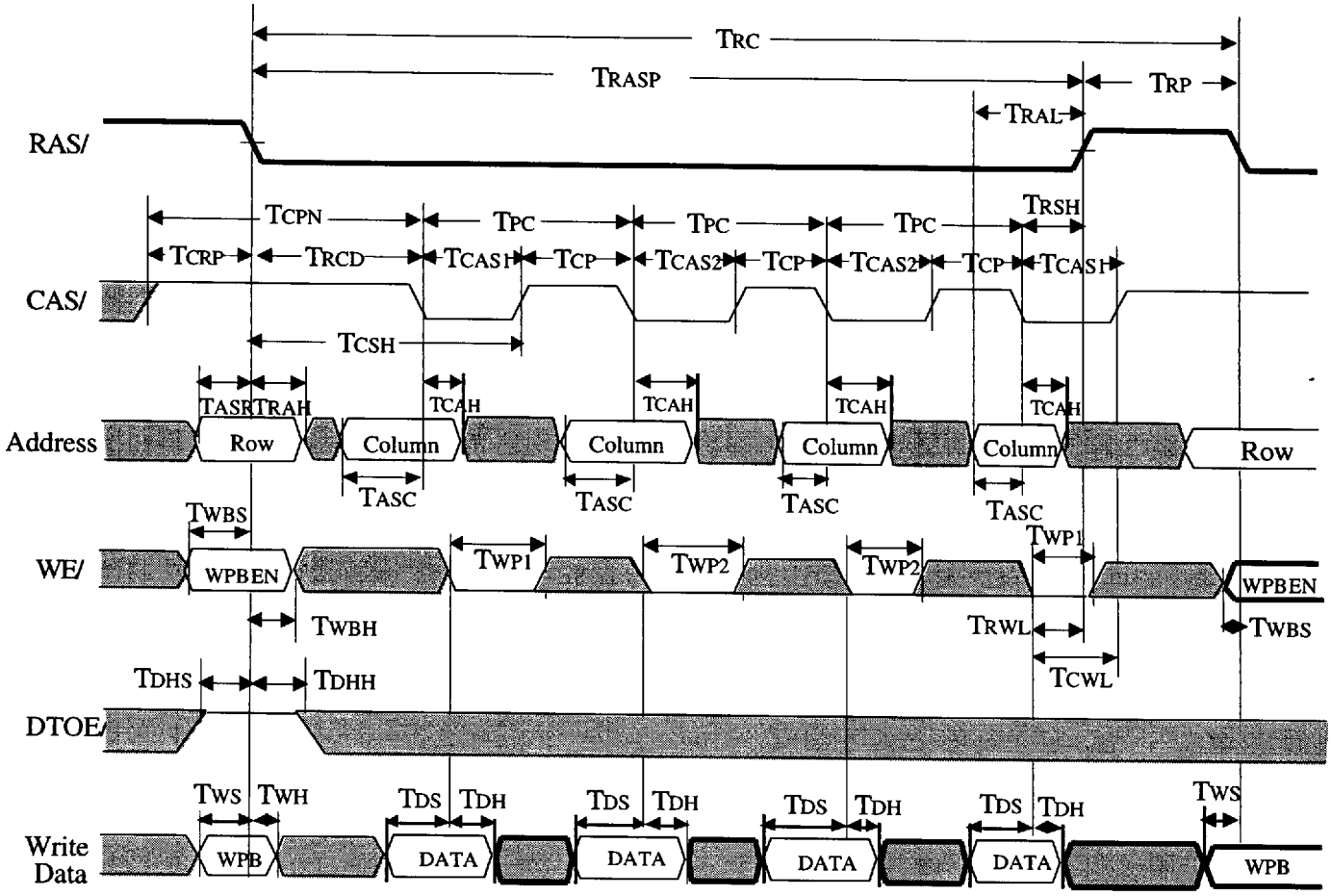
8-VRAM Fast-Page Read Cycle Timing



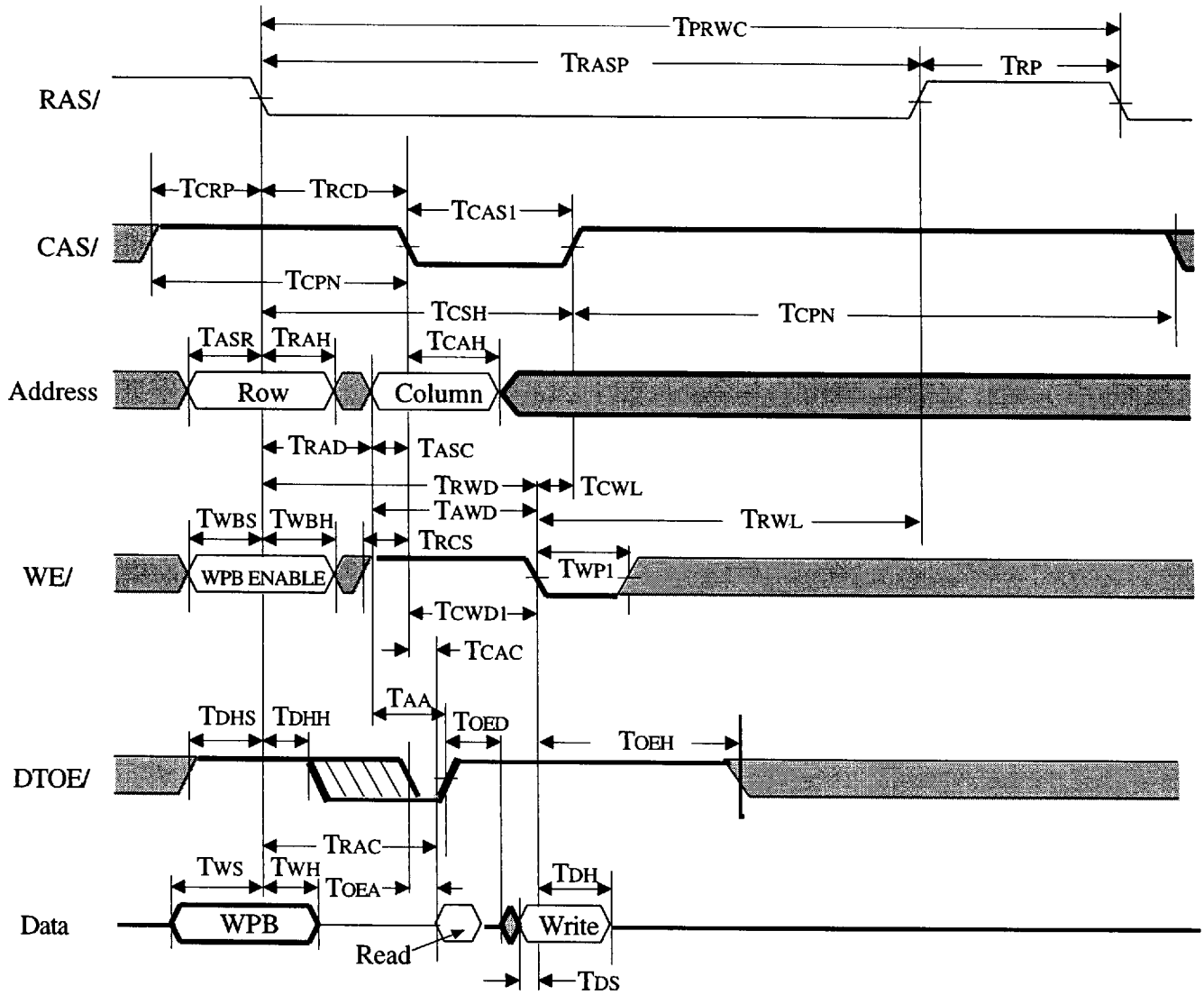
4-VRAM Fast-Page Read Cycle Timing



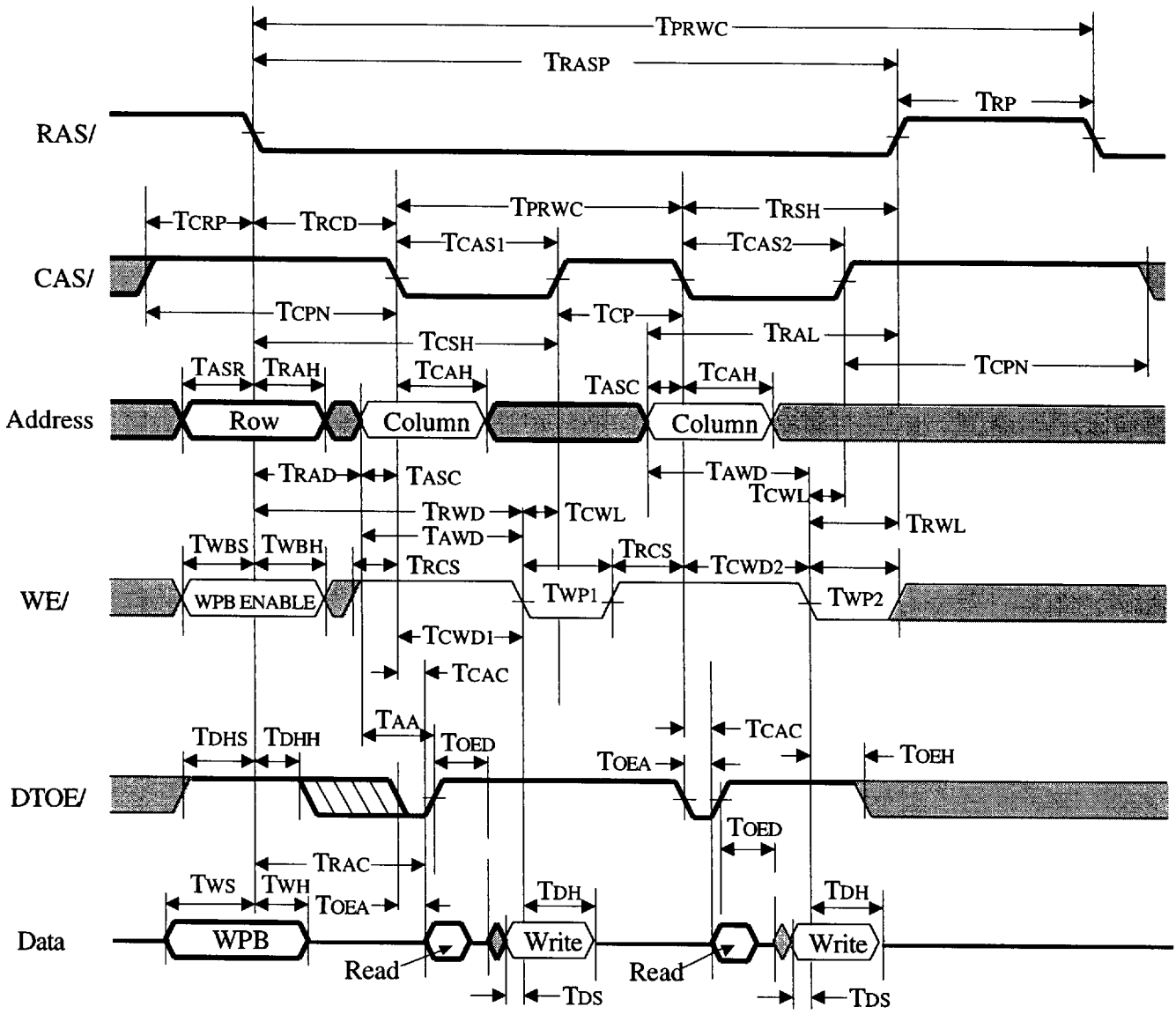
8-VRAM Fast-Page Write Cycle Timing



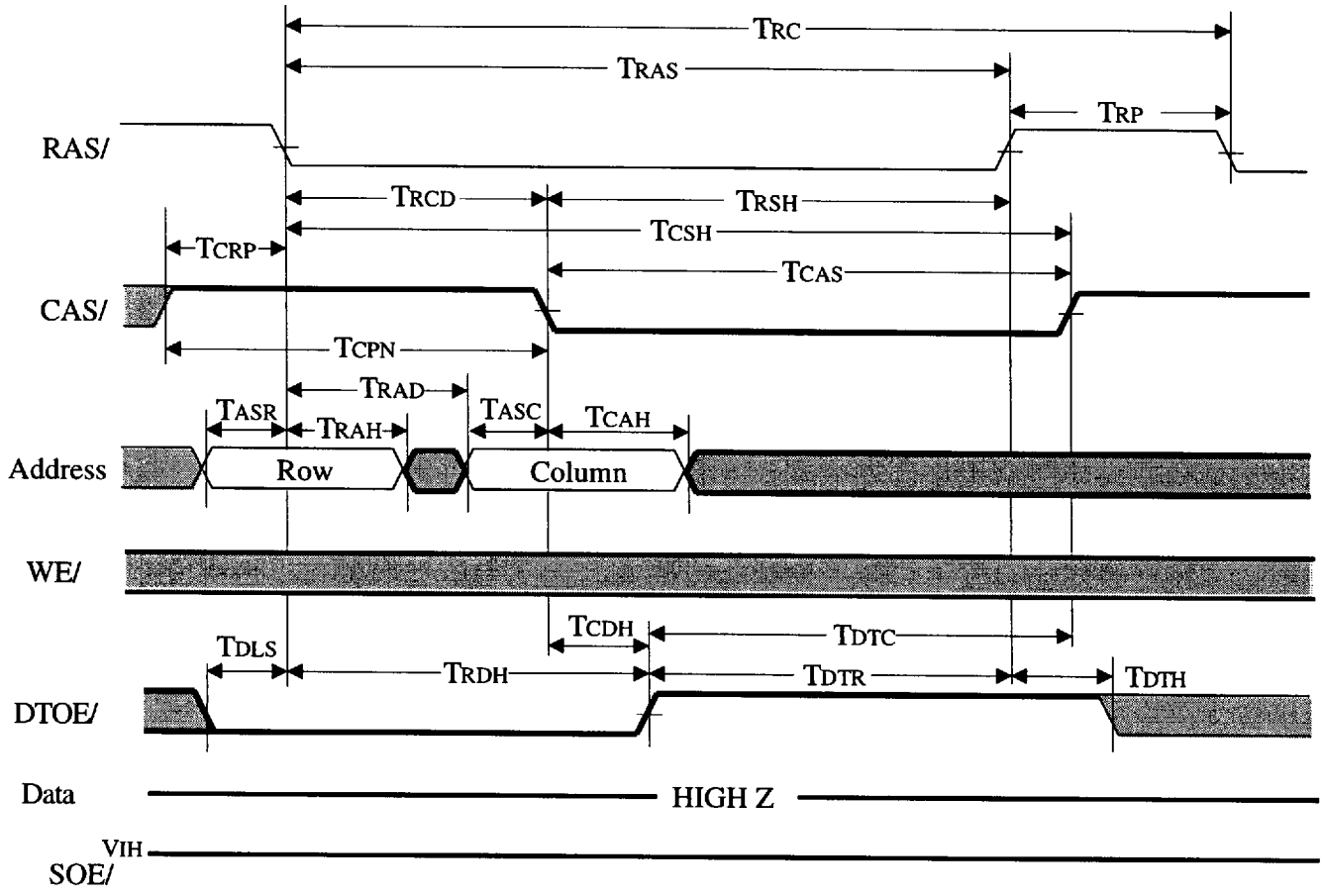
4-VRAM Fast-Page Write Cycle Timing



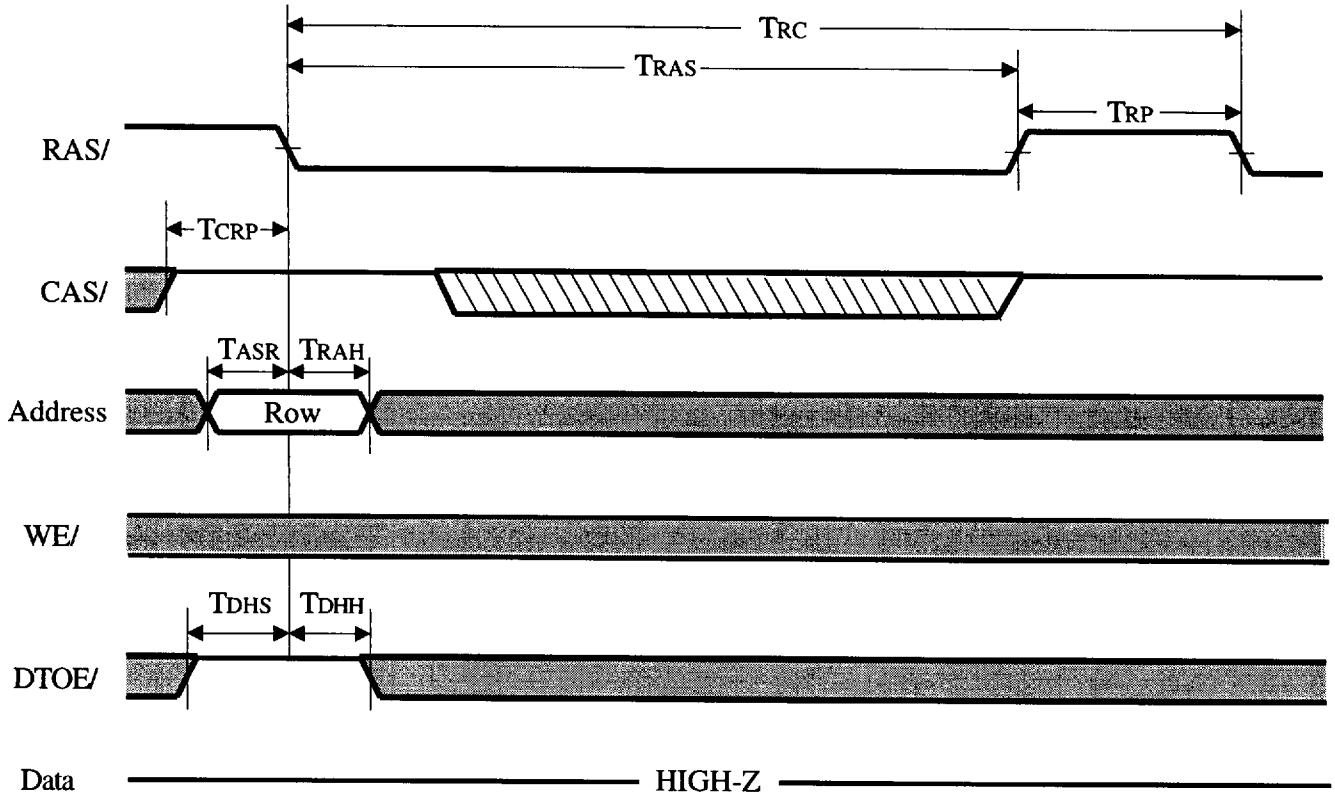
8-VRAM Fast-Page Read-Modify-Write Cycle Timing



4-VRAM Fast-Page Read-Modify-Write Cycle Timing



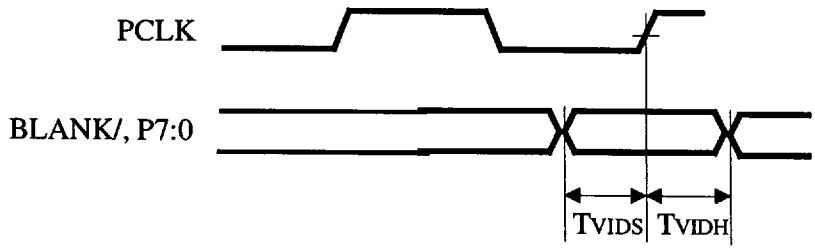
VRAM Data Transfer Cycle Timing



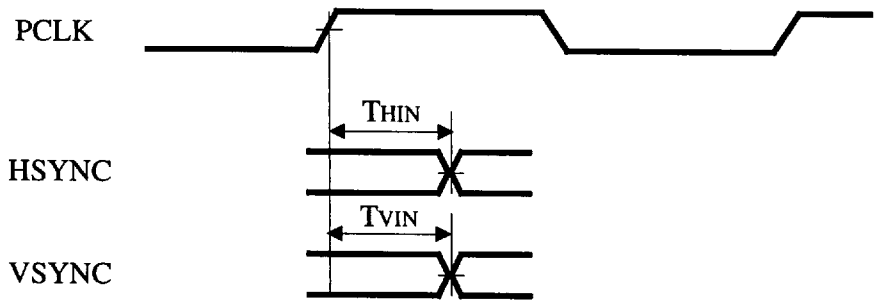
VRAM Refresh Cycle Timing

82C453 AC TIMING CHARACTERISTICS - VIDEO TIMING

Symbol	Parameter	Min	Typ	Max	Units
T_{VIDS}	Video Data and BLANK/ Setup	3	–	–	nS
T_{VIDH}	Video Data and BLANK/ Hold	3	–	–	nS
T_{HIN}	HSYNC Delay from PCLK Rising Edge	22	–	39	nS
T_{VIN}	VSYNC Delay from PCLK Rising Edge	25	–	48	nS



82C453 Video Data Timing



82C453 Video Sync Timing

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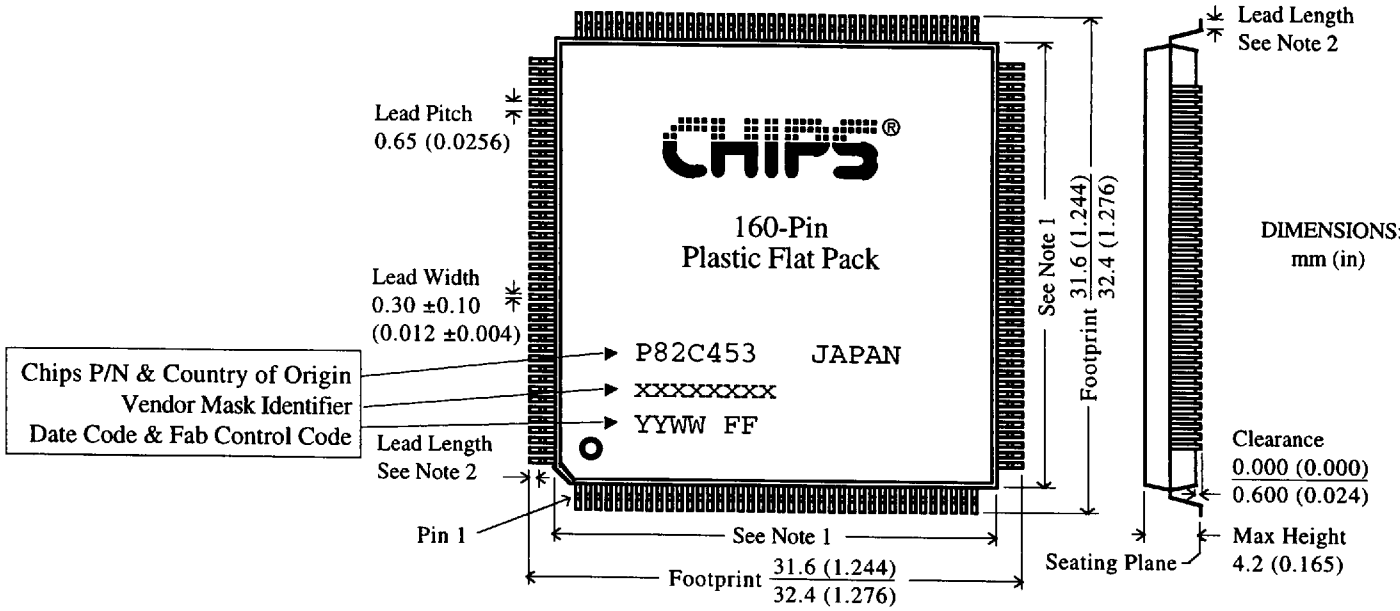
82C453 Mechanical Specifications



Note 1: Package Body Size = 28 ±0.2 (1.102 ±0.008)
Note 2: Lead Length = 0.8 ±0.2 (0.031 ±0.008)

82C453 Suggested PCB Pad Layout