# PC AT CLONE CHIPS OFFER SPEED, BETTER GRAPHICS

## CHIPS AND TECHNOLOGIES' ICs BOOST CLOCK SPEEDS 56% AND INCREASE EGA GRAPHICS RESOLUTION TO 1,128×560 PIXELS

Four chips from Chips and Technologies Inc.—the leading manufacturer of integrated circuits for clones of IBM Corp.'s Personal Computer AT—deliver triple the screen resolution, boost clock speeds from 8 MHz to either 10 or 12.5 MHz in systems compatible with Intel Corp.'s 80286 microprocessor, and boost clock speeds from 16 to 20 MHz for systems compatible with the 32-bit 80386.

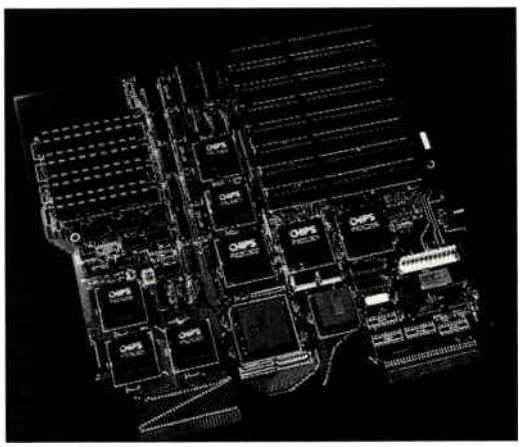
The 82C437 SharpScan delivers 1,128-by-560-pixel resolution while still retaining 100% compatibility with the 640-by-350-pixel Enhanced Graphics Adapter standard from IBM. It uses a proprietary pixel-multiplexing function that enables users to trade off the number of colors available—four instead of the normal 16—for higher resolution, says Gordon Campbell, president of Chips and Technologies.

**EGA COMPATIBLE.** Using the chip in an EGA chip set means that up to 300% more information can be presented on the screen than present EGA standards allow, he says. Additional software or setup changes to regular EGA monitors are not required.

Users can switch back and forth between high-resolution and normal EGA operation, depending on their application requirements. Because the new chip incorporates on-chip video drivers that were previously implemented externally with the Chips and Technologies EGA implementation, the total chip count for complete EGA implementation remains at 13—the lowest number in any configuration currently available, says Campbell.

To support clone computers that target speed-enhanced versions of the 80286, the Milpitas, Calif., company is introducing two speed-enhanced versions of its original 8-MHz CS8220 PC AT chip set: the 10-MHz CS8220-10 and the 12.5-MHz CS8220-12.

Both chips support very large memory configurations, from 1 to 4 Mbytes on the system board, making them appropriate for large memory systems and the next generation of operating systems.



**TOP CHIP.** The 20-MHz AT/386 chip set triples the performance of the IBM Corp.'s original PC AT.

The chip sets that complement these microprocessors have also been upgraded. A new memory-controller chip provides dynamic bus clock switching so that a system can run at full speed for on-board memory and then automatically switch to half speed for all off-board memory and input/output functions.

This capability, the company says, allows a 100% AT-compatible system to be upgraded to the higher speeds using the original add-on cards and application software with no alterations.

Chips and Technologies has targeted high-speed 386-type systems with its new CS8230-20, a 20-MHz microprocessor for the AT/386 chip set the company introduced in October 1986.

Coupled with the new chip, the enhanced AT/386 chip set delivers three times the performance of the original IBM PC AT system but uses one third the board space and one third the power. Designers achieved this by improving timing on all seven devices in the set.

The page/interleave memory controller has been enhanced to allow two-way interleave memory access for 16-MHz systems using page-mode dynamic random-access memories, as well as for 20-MHz systems that use static column DRAMs. Also, the bus controller now has an independent clock for AT bus operation, enabling the processor to run at 20 MHz while the expansion bus runs on another clock.

Available now in sample quantities, the 82C437 SharpScan EGA chips cost $6.70 each in 1,000-unit quantities. Samples of the CS8220-10/12 cost $69.10 in 100-lot quantities, and samples of the CS8230-20 cost $220 each in 100-lot quantities. A CMOS version of the CS8230 designed for low-power and portable systems will be available late in July for $184 per piece in 100-unit quantities. *–Bernard C. Cole*

Chips and Technologies Inc., 521 Cottonwood Dr., Milpitas, Calif. 95035.
Phone (408) 434-0600 [Circle 360]

# ICs SIMPLIFY PHONE-LINE EQUALIZATION

Two monolithic CMOS devices from Micro Linear Corp. virtually eliminate the need for manual adjustment of the frequency response and gain in telephone trunk lines—a costly and time-consuming problem that plagues conventional hybrid-circuit solutions.

The ML202 high-performance trunk-line equalizer offers a 105-dB dynamic range, more than enough for trunk-line applications. The ML203 logarithmic gain/attenuator operates over a range of −24 to +24 dB. Its ±1-dB response at 20 KHz exceeds telecommunications requirements and suits the chip to applications in instrumentation and audio systems that use remote control of signals.

Hybrid-based trunk-line conditioning solutions are highly susceptible to performance degradation resulting from temperature drift and aging, says Charles Gopen, vice president of marketing. System noise also accumulates as trunk lines are connected in series. The ML202/203 chip set eliminates these problems with an improved biasing scheme and highly matched device geometries that are virtually unattainable in hybrid circuits.

In equalizer operation, a 14-bit shift register in the ML202 loads data from an external microcontroller into a data latch. The latch's parallel output goes to three core filters that supply appropriate capacitor values to adjust the slope, height, and bandwidth of the input signal.

The ML203 adjusts gain with a coarse-gain stage, which handles 1.0-dB steps, and a fine-gain stage for 0.1-dB steps, all within a 0-to-1.5-dB range. A 9-bit shift register, latch, and output multiplexer allow the use of parallel or serial interfaces.

Both devices will be available in the third quarter of this year. In 1,000-unit quantities the ML202 will cost $8 each, and the ML203 will be $5 each. *–Bernard C. Cole*

Micro Linear Corp., 2092 Concourse Dr., San Jose, Calif. 95131.
Phone (408) 262-5200 [Circle 361]