64300 / 301

Wingine® DGX

Data Sheet

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P R E L I M I N A R Y

CHIPS®

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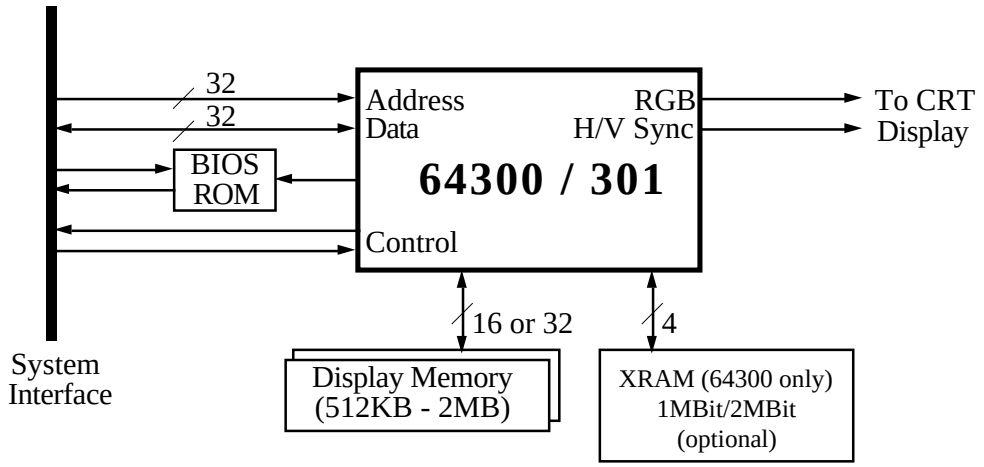
64300 / 301
Wingine® DGX
DRAM Graphics Accelerator

- High performance accelerator for computer graphic intensive applications, such as graphical user interface, word processor, spreadsheet and CAD/CAM programs.
- XRAM™ Technology (Patent Pending) (64300 only)
- The 64300 / 301 are identical except for one feature: the 64301 does not include XRAM technology
- Optimized interface to multiple bus architectures:
  - VESA Local Bus (32-Bit)
  - 386DX and 486SX/DX Local Bus (32-Bit)
  - ISA Peripheral Bus (16-Bit)
- Three Operand BITBLT
  - Supports all 256 logical combinations of Source, Destination and Pattern
- Hardware Assisted Line Draw
- 64x64x2 Hardware Cursor
- 32-Bit Color Expansion
- Zero Wait State Peripheral Bus Operation
- Direct linear mapping to system memory (up to 2MB selectable)
- A complete high performance local bus graphics system requires only the addition of DRAM and BIOS
- Full VGA compatibility
- Supports the VESA Display Power Management Signaling (DPMS) Protocol for desktop computer power management
- RAMDAC power-down and programmable clock provide additional power management capability
- Supports a wide variety of monitor resolutions and color depths (bits per pixel):
  - 640x480, 4bpp to 24bpp
  - 800x600, 4bpp to 16bpp
  - 1024x768, 4bpp to 16bpp
  - 1280x1024, 4bpp to 8bpp
- Integrated RAMDAC
  - Up to 16.7 Million Colors (24 bits per pixel)
  - 256x18 LUT
- Integrated Clock Synthesizer
  - Programmable MCLK up to 72MHz
  - Programmable PCLK up to 85MHz
- Flexible display memory configurations supporting 512KB to 2MB:
  - Four, eight or sixteen 256Kx4 DRAMs
  - One, two or four 256Kx16 DRAMs
- Support for Color Key and video overlay with external video data input
- 'Flash' ROM support for in-circuit BIOS upgrades
- 208-pin PFP pinouts optimized for PCB layout



System Diagram

Revision History

Revision	Date	By	Comment
0.1	9/92	DR	Internal Review - Rough Draft
0.2	12/92	DR	Internal Review
0.3	1/93	DR	Updated Pinouts & Added Functional Description
0.4	2/93	DR	Modified Register Summary &Added Electrical Specifications Section
0.5	5/93	DR / DH	Added Preliminary Timing & Application Schematics Removed 'autoincrement' bit from DR08 Changed memory interface pin names to match DRAM pin names: MAD0-7 & MBD0-7 changed to MAD0-15 MCD0-7 & MDD0-7 changed to MBD0-15 RASAB# & RASCD# changed to RASA# & RASB# CAS0A# & CAS0B# changed to CASAL0# & CASAH0# CAS0C# & CAS0D# changed to CASBL0# & CASBH0# CAS1A# & CAS1B# changed to CASAL1# & CASAH1# CAS1C# & CAS1D# changed to CASBL1# & CASBH1#
0.6	6/93	DR	Added 64301 Specifications Modified ISA Timing, Circuits and DAC specs Changed pinout - deleted GPI04 and added VREF
1.0	8/93	DR / DH	Changed pin location of VREF and RSET Fixed notation/naming of configuration pins Fixed pin numbers in Application Schematics Added proper clock synthesizer decoupling in Application Schematics Changed ICT mechanism Removed references to 16-bit 386SX support
1.1	9/93	DR	Modified DRAM Read/Write Timing Table
1.2	11/93	DR	Changed pinout from 104-156 Deleted GPIO0 and GPIO1 from XR71 and XR72 Changed definition of pin 104 from VREF to COMP Deleted support for a 2x clock input Added support for 1024x768x16BPP mode Added direct interface for VESA Standard IBM VGA Feature Connector Deleted MDA, Hercules, and CGA backwards compatibility support Removed support for external RAMDAC

Table of Contents

Table of Contents

List of Figures and Tables

Introduction

The 64300 / 301 Wingine® DGX combines three powerful elements aimed at addressing the requirements of mainstream desktop PC designs: 1) state of the art techniques for optimizing performance in computer graphic intensive applications, graphical user interfaces (GUI) and operating systems, such as Windows; 2) cost saving features such as integrated palette DAC and clock synthesizer, integrated support for multiple bus interfaces and flexible DRAM-based display memory configurations; and 3) differentiating factors such as optional XRAM Accelerator Cache (64300 only), desktop computer power management, Flash ROM support, linearly mapped display memory, and Multimedia support for color key and video overlays.

PERFORMANCE

XRAM Accelerator Cache (64300 only)

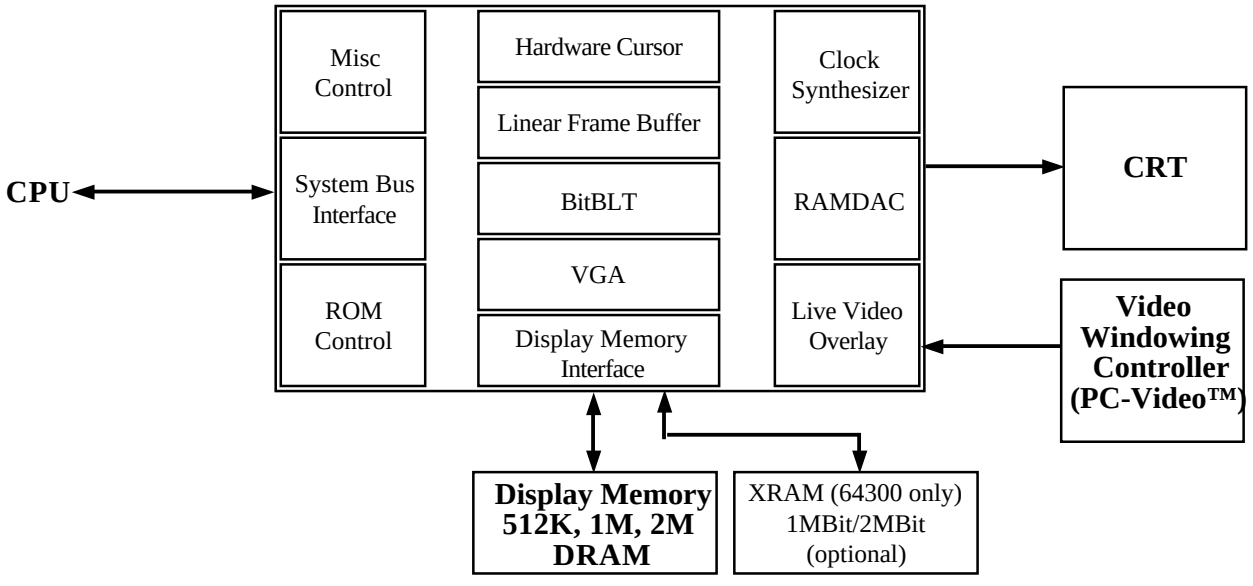
The XRAM Accelerator Cache (patent pending) is a breakthrough in performance technology. By using one standard 256Kx4 Fast Page DRAM, a proprietary algorithm implemented in the 64300 significantly increases graphics system performance. The result is performance never before achieved in standard DRAM-based graphics architectures. For added flexibility, the XRAM Accelerator Cache is optional.

Local Bus

To address the requirement of high performance (particularly in GUI environments) while maintaining a cost effective bill of materials for the graphics system, the 64300 / 301 offers the industry's most optimized price/performance/feature mix. A variety of industry standard 32-bit local bus interfaces are integrated on chip, including: VESA Local Bus (VL-Bus), 386DX and 486SX/DX CPU buses. The key is that local bus interfaces are 32-bit wide. This means full local bus performance potential is realized and no external TTL devices are required for multiplexing or demultiplexing bus signals. In addition to local bus support, ISA / EISA standard peripheral buses are also supported.

Scalability

A benefit provided by the 64300 XRAM technology is scalability. When a system's host CPU is upgraded (e.g. from a 486DX-25 to a 486DX-33 or from a 486DX-33 to a 486DX2-66) the 64300 Wingine DGX performance will scale with the processor and a significant improvement will be observed in the display. Other DRAM-based graphics accelerators gain some degree of performance which, while measurable, is not as significant nor as noticeable on the display.



64300 / 301 Internal Block Diagram

Acceleration Features

Several functions traditionally performed by software have been implemented in hardware to further improve performance. Three-Operand BITBLT logic supports all 256 logical combinations of Source, Destination and Pattern. Line drawing is accelerated with hardware assistance. A programmable-size 64x64x2 hardware cursor allows flexible cursor size and flicker free cursor display. The presence of the hardware cursor frees software from continuously generating the cursor image on the display. A 32-Bit Color Expansion engine allows the host CPU to transfer monochrome "maps" of color images over the system bus at high speeds to the 64300 / 301, which decodes the monochrome images into their color form.

For ISA implementations, the 64300 / 301 additionally supports Zero Wait State memory accesses.

COST OPTIMIZATION

High Integration

The 64300 / 301 integrates a Graphics Accelerator Engine together with a True-Color palette DAC and clock synthesizer. The integrated palette DAC supports 24-Bit direct color and features a 256x18 LUT. The integrated dual clock synthesizer allows full programmability of MCLK (memory clock) and PCLK (pixel clock). The integrated clock synthesizers support frequencies from 390KHz to 120MHz.

DRAM Display Memory

The 64300 / 301 supports from 512KB to 2MB of DRAM display memory. Both 256Kx4 and 256Kx16 Fast Page Mode DRAM organizations are supported. Display memory is linearly mapped up to 2MB, simplifying development of device drivers and optimizing driver performance.

DIFFERENTIATING FEATURES

The 64300 / 301 True-Color GUI Accelerator permits a high degree of differentiation at low cost. For example, in the 64300 the XRAM Accelerator significantly increases performance for the price of one standard 256Kx4 DRAM (for 1MByte video memory systems). However, the ability to differentiate does not end there. The VESA display power management signalling (DPMS) standard is supported, enabling stand-by, suspend, and "off" power saving modes. Color Key and video overlay are supported for optimal Multimedia applications. Flash ROMs (PEROMs) are supported for in-system BIOS upgrades. Pinouts are optimized for PCB board layout such that a 64300 / 301 GUI accelerator design can be implemented in less than 9 square inches (5800 sq mm). Additionally, the 64300 / 301 offers integrated palette DAC and dual clock synthesizer, but also allows use of these devices externally. The package may be checked for correct insertion via its in-circuit test features.

DESKTOP POWER MANAGEMENT

The 64300 / 301 supports the VESA DPMS (Display Power Management Signalling) protocol. This includes the ability to independently stop HSYNC or VSYNC and hold them at a static level. Additionally the RAMDAC may be powered-down and the clock frequencies lowered for further power savings.

MINIMUM CHIP COUNT / BOARD SPACE

The 64300 / 301 was designed to integrate as many functions as economically possible to minimize chip count and board space. The 64300 / 301 integrates a VGA core, True-Color palette DAC, and dual programmable clock synthesizer and employs separate address and data buses so that no external buffers are required (VL-Bus).

Using the 64300 / 301, a complete 32-bit, VGA-compatible, local bus GUI accelerator design for motherboard applications can be built with just 2 ICs, including display memory, as shown in the following bill of materials table:

Qty	Chip Type
1	64300 / 301 Wingine DGX
1	256Kx16 Fast Page Mode DRAM
2	Total

For add-in board applications, external bus drivers may be required for additional signal drive and a PEROM may be required for BIOS storage. Improved performance or other optional features may require implementation of more than one memory chip. In the 64300, the XRAM Accelerator Cache option, for example, would add a single 256Kx4 Fast Page Mode DRAM to the above bill of materials.

DISPLAY MEMORY INTERFACE

The 64300 Wingine DGX can employ multiple display memory configurations providing the OEM with flexibility to use it in several designs with differing cost and performance criteria.

The 64300 / 301 supports the following display memory configurations using Fast Page Mode DRAMs:

- One 256Kx16 DRAM (512 KBytes)
- Four 256Kx4 DRAMs (512 KBytes)
- Two 256Kx16 DRAMs (1 MByte)
- Eight 256Kx4 DRAMs (1 MByte)
- Four 256Kx16 DRAMs (2 MBytes)
- Sixteen 256Kx4 DRAMs (2 MByte)

In the 64300 performance is significantly improved when optional memory is added to support the XRAM. For 1MByte configurations one additional 256K x 4 DRAM is required. For 2MByte configurations, two 256K x 4 DRAMs are required. In all configurations the 64300 / 301 supports all standard VGA display modes.

The entire display memory (512 KBytes to 2 MBytes) is always available to the CPU in regular four-plane mode, chained two-plane mode, and super-chained one-plane mode.

Display memory control signals are derived from the memory clock (MCLK) input.

The 64300 / 301 serves as a DRAM controller for the system's display memory. It handles DRAM refresh, fetches data from display memory as required to refresh the screen, interfaces the CPU to display memory and supplies all necessary DRAM control signals. For VGA compatibility, the display memory is arranged as four planes of 64 KBytes each. Each plane is eight bits wide for a total of 32 bits. All planes share a common address bus. Each plane has a separate CAS signal and share a common write enable (except when using 256K x 16 DRAMs with 2 WE# / 1 CAS# which separates byte accesses based on WE#). Planes 0/1 and 2/3 have separate RAS signals which operate independently only when in text modes. In 2MByte configurations the second bank is a duplicate of the first with an additional set of CAS control signals.

CPU BUS INTERFACE

The 64300 / 301 provides on-chip support for interface to VESA Local Bus (VL-Bus), 486 SX Local Bus, 486 DX Local Bus, 386 DX Local Bus, and EISA/ISA Bus. Strap options allow the user to configure the chip for the type of interface desired. Control signals for all interface types are integrated on chip. Support is provided for 8-bit, 16-bit, and 32-bit cycles for both memory and I/O. All parameters necessary to ensure proper operation in these various environments are handled in a fashion transparent to the CPU. These include internal decoding of all memory and I/O addresses, bus width translations, and generation of the necessary control signals. In ISA/EISA bus implementations the 64300 / 301 must be placed in a 16-bit slot for proper operation. The 64300 / 301 also provides a 'linear addressing' feature which allows display memory to be accessed in any area of upper memory up to 2MB in size.

DISPLAY INTERFACE

The 64300 / 301 supports high resolution fixed frequency and variable frequency analog monitors in interlaced and non-interlaced modes of operation.

The 64300 / 301 supports resolutions up to 1280x1024 pixels with 256 colors or 1024x768 pixels with 65K colors in a 2 MB display memory configuration and supports Super-VGA resolutions such as 640 x 480 16.7M colors, 800x600 65K colors, and 1024x768 256 colors in 1MB display memory configurations.

FULL COMPATIBILITY

The 64300 / 301 is fully compatible with the IBM™ VGA standard at the hardware, register, and BIOS level. Mode initialization is supported at the BIOS and register levels, ensuring compatibility with all application software.

Write Protection

The 64300 / 301 has the ability to write protect the overscan or border color for European ergonomics display requirements.

Extension Registers

The 64300 / 301 employs an "Extension" Register set to control its enhanced features. These Extension Registers provide control of the CRT parameters for extended modes and control of the additional hardware features in the 64300 / 301. These registers are always accessible as an index/data register set at I/O port addresses 3D6-3D7h. None of the unused bits in the regular VGA registers are used for extensions. There are also 32-bit registers (DRXX) which control the BitBlt engine and hardware cursor.

Context Switching

For support of multi-tasking, windowing, and context switching, the state of the 64300 / 301 (internal registers) is readable and writable. This feature is fully compatible with IBM's VGA. Additional registers are provided to allow read back of internal latches not readable in the IBM VGA.

RESET, SETUP, AND TEST MODES

Reset Mode

When this mode is activated by pulling the RESET pin high, the 64300 / 301 is forced to VGA-compatible mode and is disabled. It must be enabled after deactivating the RESET pin by writing to the Global Enable Register (46E8h). The RESET pin must be active for at least 1.5µs for the 64300 / 301 to enter a stable state.

Setup Mode

In this mode, only the Global Enable register is accessible.

Setup mode is entered by writing a 1 to bit-4 of port 46E8h. This port is incorporated in the 64300 / 301. While in Setup mode, the video output is active if it was active prior to entering Setup mode and inactive if it was inactive prior to entering Setup mode.

After power up, video BIOS can optionally disable the video 46E8h register (via XR70) for compatibility in case other non-IBM-compatible peripheral devices use those ports.

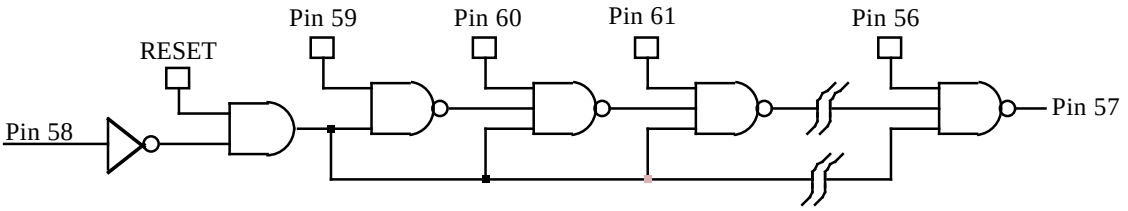
Tri-State Mode

In this mode, most output pins of the 64300 / 301 chip may be disabled for testing of circuitry external to the chip. The 64300 / 301 will enter Tri-State mode during RESET. The 64300 / 301 will exit Tri-State mode when RESET goes inactive.

ICT (In-Circuit Test) Mode

In this mode, pins on the 64300 / 301 chip may be tested individually to determine if they are properly connected. The 64300 / 301 will enter ICT mode when RESET is active (high) and MBD15 (pin 58) is low as shown below. In ICT mode, all digital signal pins except WE#, XA4:1 and MA4:1 become inputs which are part of a long path starting at pin 59 (MDD6) and proceeding around the chip to pin 56 (OE#). On the 64301, XWE pin 134 is a do not connect and thus is not part of the ICT test path. ICT mode tests all pins except XTALO, RED, GREEN, BLUE, COMP, RSET, XA4:1, MA4:1, LCLK, MCLK, VCC and GND. All other pins are part of a NAND ring as shown below. The result of the NAND ring is output on pin 57 (WE#). A typical test environment will place all test ring input pins at a logical high level after enabling the test ring with RESET high and MBD15 low. Pins in the test ring (starting at pin 59 and moving counter-clockwise around the chip) are sequentially brought low. Upon each high to low transition, the output of the test ring (pin 57) should toggle.

Warning: This method is subject to change on future revisions of the 64300 / 301. Always refer to the most current data sheet for this device.



64300 / 301 NAND Test Ring

CHIP ARCHITECTURE

The 64300 / 301 integrates eight major internal modules:

Sequencer

The Sequencer generates all CPU and display memory timing. It controls CPU access of display memory by inserting cycles dedicated to CPU access. It also contains mask registers which can prevent writes to individual display memory planes.

CRT Controller

The CRT Controller generates all the sync and timing signals for the display and also generates the addresses used for both display refresh and CPU access of display memory.

Graphics Controller

The Graphics Controller interfaces the 16 or 32-bit CPU data bus to the 32-bit internal data bus used by the four planes (Maps) of display memory. It also latches and supplies display memory data to the Attribute Controller for use in refreshing the screen image. For text modes this data is supplied in parallel form (character generator data and attribute code); for graphics modes it is converted to serial form (one bit from each of four bytes form a single pixel). The Graphics Controller can also perform any one of several types of logical operations on data while reading it from or writing it to display memory.

Attribute Controller

The Attribute Controller generates the 4-bit-wide VGA video data stream used to refresh the display. This is created in text modes from a font pattern and an attribute code which pass through a parallel to serial conversion. In graphics modes, the display memory contains the 4-bit pixel data. In text and 16 color graphics modes the 4-bit pixel data acts as an index into a set of 16 internal color look-up registers which generate a 6-bit color value. Two additional bits of color data are added to provide an 8-bit address to the VGA color palette. In 256-color modes, two 4-bit values may be passed through the color look-up registers and assembled into one 8-bit video data value. In high-resolution 256-color modes, an 8-bit video data value may be provided directly, bypassing the attribute controller color lookup registers. Text and cursor blink, underline and horizontal scrolling are also the responsibility of the Attribute Controller.

VGA Color Palette/DAC

The 64300 / 301 integrates an industry standard VGA-compatible palette DAC for support of analog-output CRT displays.

The on-board VGA color palette contains a pixel mask register, 256x18 color lookup table (LUT), and triple 8-bit DACs for driving analog CRTs directly. The 'LM339' comparator function is implemented internally to generate the SENSE signal. The voltage reference for the internal DACs is also implemented on-chip.

True Color Support

Each DAC analog output provides 8-bit resolution (256 shades of color on each of the analog R, G, and B outputs). The internal DAC supports generation of 15 bit/pixel TARGA format (5R + 5G + 5B + 1 unused), 16 bit/pixel (5R + 6G + 5B), and 24bpp (8R + 8G + 8B) graphics output to analog CRT displays. 15bpp (also called '555' mode) is compatible with Sierra RAMDACs and 16 bpp (also called '565' mode) is compatible with XGA high-color mode.

BitBlt Engine

The BitBlt engine performs a wide range of tasks in graphics modes. In its simplest form it transfers blocks of data from one area of the screen to another without CPU supervision. It is also capable of performing address generation for system to screen transfers. All 256 Microsoft Windows Raster Operations are supported. It may also be used for font and monochrome bitmap expansion to full color depth from bitmaps stored in either system memory or display memory. The BitBlt engine contains a Windows compatible monochrome or full color (8x8) pattern register and a 3-operand logical raster operation block. The BitBlt engine is controlled by a set of 32-bit wide registers.

Hardware Cursor

Hardware cursors are commonly used in windowing environments such as OS/2, X-Windows, and Microsoft Windows. The 64300 / 301 incorporates a 64x64x2 hardware cursor for support of these environments. The format is an AND plus an XOR plane which select between transparency, highlight (invert), and two user definable colors. The cursor RAM may also be divided up into quarters supporting storage for up to four cursors simultaneously. This has the advantage of allowing pseudo-dynamic cursor icons (rotating cartwheels, sand falling through an hourglass, etc.) and also eliminates the flashing which may occur when the active cursor's shape and position (hotspot) change simultaneously.

Clock Synthesizer

A dual programmable clock synthesizer complete with charge pumps and filters is integrated into the 64300 / 301. On reset the clock synthesizer defaults to VGA compatible values. It requires a 14.31818MHz crystal or oscillator input to generate a reference frequency. If a crystal is used it does not require other passive components externally (no additional resistors or capacitors). Both clocks are programmable to function across the full specified operating range of both PCLK and MCLK.

CONFIGURATION SWITCHES

The 64300 / 301 can read up to sixteen configuration bits. These signals are sampled on memory data bus bits MAD15:0 on the falling edge of RESET. The state of MAD1:0 on RESET determines the bus interface type. MAD2 is currently undefined. In ISA interfaces MAD3 chooses between MCLK and MCLK÷2 for the internal Host Clock (HCLK). MAD4 determines where the video and memory clocks are located (internal or external). If the internal clock synthesizer is selected, MAD5 determines if the reference is connected to a crystal or TTL oscillator input. MAD6 determines if the local bus controller expects a tri-state LDEV# signal or a straight unlatched decode. In VL-Bus mode MAD7 determines if the cache controller owns the RDY# signal during the first T2 of a local bus cycle. In ISA bus mode MAD7 chooses between an external HCLK or internal HCLK (see MAD3). All eight bits of the lower configuration byte (on MAD7:0) are latched into an extension register (XR01) on RESET so software may determine the hardware configuration.

A second configuration byte is latched on reset from MAD15:8 and may be read in XR74. These bits have no internal hardware function and may be used for any desired purpose by software.

Memory data lines MAD15:0 for the corresponding bits must be externally connected to 47KΩ pullups or pulldowns (or driven to the desired 0 or 1 level while RESET is high) so that they may be latched on the falling edge of RESET. The 64300 / 301 does not implement pullup or pulldown resistors on these pins internally.

GENERAL PURPOSE I/O

There are five general purpose I/O (GPIO) pins which are controlled via XR71 and XR72. Several of these pins are multiplexed with optional functions such as external clock synthesizer and feature connector support. If these features are not used then the corresponding pins may become user definable I/O pins. Additional features can be added to the 64300 / 301 by using these pins. These features include; reading the IBM monitor ID bits, controlling the programming voltage on a Flash ROM device, or as an interface to a serial Non-Volatile Memory (EEPROM).

CLOCK SELECTION

The 64300 / 301 will typically be configured to use its internal clock synthesizer. On RESET the internal MCLK is set to 60MHz. A 60MHz MCLK is within the operational specification for 80ns DRAMs and is high enough to operate all standard VGA modes. The fixed Video CLK registers (Video CLK selects 0 and 1) are set as close as possible to the standard VGA frequencies (25.175MHz and 28.322MHz). These are the required frequencies for VGA compatible designs. The CLKSEL1:0 bits in the MISC Status Register are also cleared on RESET thus selecting Video CLK0 (25.175MHz). The internal clock synthesizer accepts either a TTL 14.31818MHz oscillator input on XTAL IN or a 14.31818MHz crystal on its XTAL IN / XTAL OUT pins. The internal clocks may be programmed to within 0.5% of any frequency between 10MHz and 80MHz. Standard video frequencies in this range are achieved to within the VESA recommended accuracy.

If an external clock synthesizer is used (e.g. 82C404C) the pixel clock is input on XTAL IN; the memory clock on MCLK.

The MCLK frequency is dependent upon the access speed of the DRAMs connected to the 64300 / 301. DRAM's with access times of 60ns are matched with an MCLK frequency of approximately 72MHz. The maximum video data rate for a given

MCLK frequency is approximately 1.2x (Bytes/sec). Hence the maximum video data rate for 60ns DRAMs is about 90MBytes/sec.

BIOS ROM INTERFACE

The video BIOS is implemented as an 8-bit (32Kx8) ROM. Typically a system will shadow the BIOS in system memory and thus it will only be read at boot time.

In all ISA and VL-Bus add-on cards the video BIOS is physically on the card and the BIOS ROM requires a buffer to drive its data onto the bus. For ISA bus designs the 64300 / 301 generates control signals for the BIOS and turns on its external drivers. In VL-Bus add-in card designs the 64300 / 301 does not respond to BIOS accesses on the VL-Bus (no DEVSEL# is issued). Rather, the 64300 / 301 monitors accesses on the VL-Bus and performs the transfers across the ISA bus. This allows byte alignment translation to occur in the system logic interface rather than requiring four transceivers on the VL-Bus card. For implementation information refer to the circuit examples in the Application Schematics section.

In all motherboard direct processor interfaces it is presumed that the video BIOS is part of the system BIOS.

Chips and Technologies, Inc. supplies a video BIOS optimized for 64300 / 301 hardware. The BIOS supports the extended functions of the 64300 / 301, such as extended resolution modes. It is DPMS compatible and supports the VESA 'Super VGA' BIOS mode extensions. The BIOS Modification Program (BMP) enables OEMs to tailor their feature set by programming the extended functions. CHIPS offers the BIOS as a standard production version, a customized version, or as source code.

FLEXIBLE ARCHITECTURE

The 64300 / 301's flexible architecture enables OEMs to differentiate their products with enhanced features. OEMs can design one VGA sub-system and implement a wide range of features by selecting the display memory configuration, the XRAM accelerator option, and a live video overlay option. A single VGA sub-system design can provide:

- Lowest cost: use one 256Kx16 DRAM (512 KBytes) for a minimum VGA subsystem
- Standard Performance 1MByte subsystem: use two 256Kx16 DRAMs
- Highest Performance 1MByte DRAM system: use two 256Kx16 DRAMs plus a single 256Kx4 DRAM for XRAM acceleration
- Extended Resolution: use four 256Kx16 DRAMs plus two 256Kx4 DRAMs for acceleration
- Add live video via RGB 5-6-5 synchronized live video window (CHIPS 69001 PC-Video™)

The 64300 / 301 is an excellent option for main system motherboards which must support a wide range of processor performance. **The 64300, with its XRAM option, provides a scalability not available from any other DRAM based video controller.**

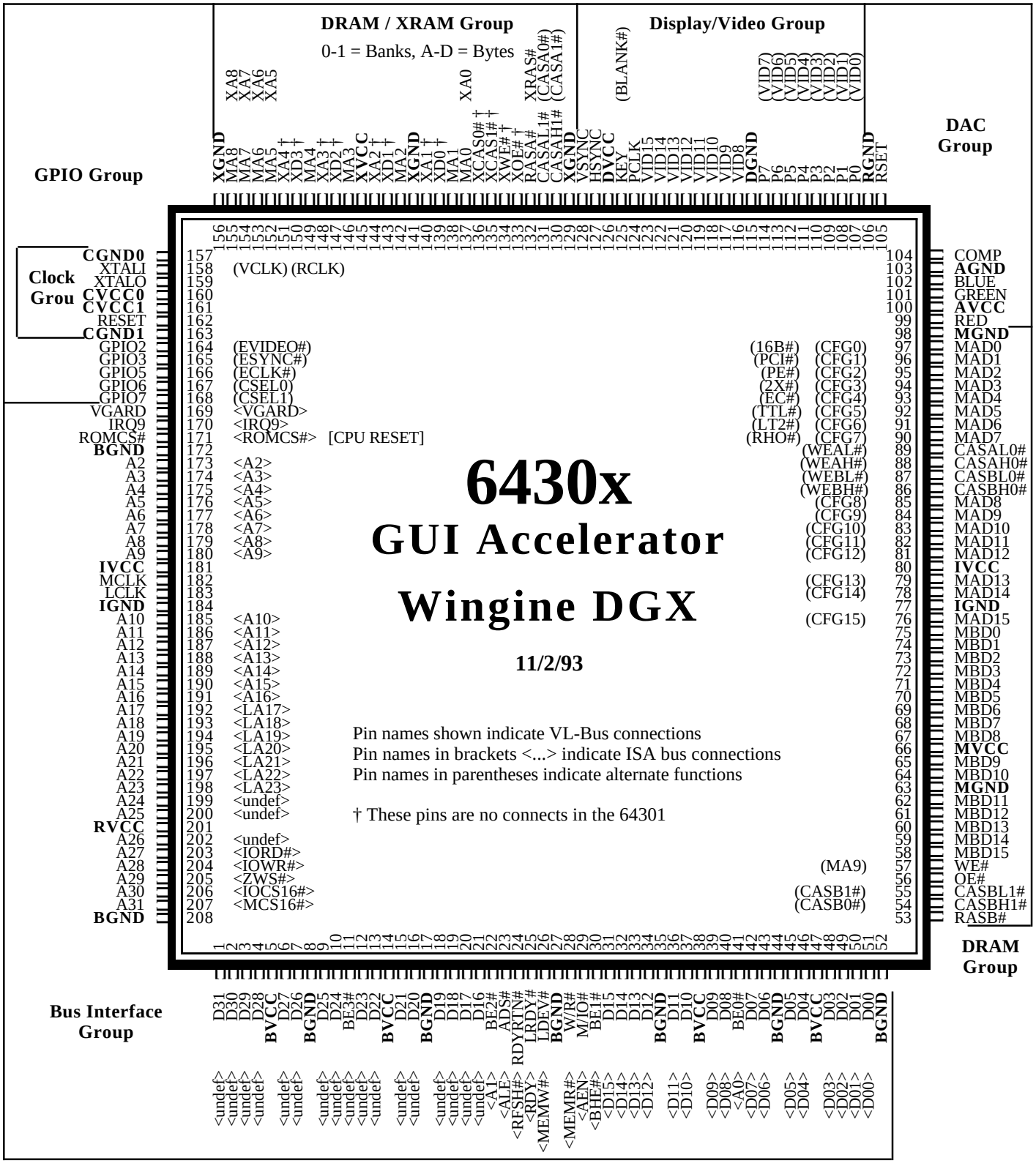
PACKAGE

The 64300 / 301 is available in a 208-pin plastic flat pack (PFP).

APPLICATION SCHEMATIC EXAMPLES

Included in this document are the following application schematic examples:

1. Bus Interface: 16-bit EISA/ISA Bus
   Bus Interface: 32-bit VL Bus
2. Memory Interface: 1, 2, 4 256Kx16 DRAMs 2-CAS#
   Memory Interface: 1, 2, 4 256Kx16 DRAMs 2-WE#
3. CRT/Video Interface: 8-bit Video Output
   CRT/Video Interface: 16-bit Video Output


DRAM / XRAM Group
0-1 = Banks, A-D = Bytes
Display/Video Group
DAC Group
GPIO Group
Clock Group
Bus Interface Group
DRAM Group
6430x
GUI Accelerator
Wingine DGX
11/2/93
Pin names shown indicate VL-Bus connections
Pin names in brackets <...> indicate ISA bus connections
Pin names in parentheses indicate alternate functions
† These pins are no connects in the 64301

Pin List - Bus Interface

Pin #	Type	PU	I_{OH}	I_{OL}	Load	VL Bus	386 DX	ISA Bus
183	In		—	—	—	LCLK	CLK2X	—
162	In		—	—	—	RESET	RESET	RESET
169	I/O		–4	4	50	VGARD	VGARD	VGARD
171	I/O		–4	4	50	ROMCS#	CRESET	ROMCS#
170	I/O		–12	12	50	IRQ9	IRQ9	IRQ9
26	I/O		–8	8	50	LDEV#	LDEV#	MEMW#
25	I/O		–12	12	50	LRDY#	LRDY#	RDY
24	In		—	—	—	RDYRTN#	RDYRTN#	RFSH#
28	In		—	—	—	W/R#	W/R#	MEMR#
29	In		–8	8	50	M/IO#	M/IO#	AEN
23	In		—	—	—	ADS#	ADS#	ALE
30	In		—	—	—	BE1#	BE1#	BHE#
11	In		—	—	—	BE3#	BE3#	—
41	In		—	—	—	BE0#	BE0#	A0
22	In		—	—	—	BE2#	BE2#	A1
173	In		—	—	—	A2	A2	A2
174	In		—	—	—	A3	A3	A3
175	In		—	—	—	A4	A4	A4
176	In		—	—	—	A5	A5	A5
177	In		—	—	—	A6	A6	A6
178	In		—	—	—	A7	A7	A7
179	In		—	—	—	A8	A8	A8
180	In		—	—	—	A9	A9	A9
185	In		—	—	—	A10	A10	A10
186	In		—	—	—	A11	A11	A11
187	In		—	—	—	A12	A12	A12
188	In		—	—	—	A13	A13	A13
189	In		—	—	—	A14	A14	A14
190	In		—	—	—	A15	A15	A15
191	In		—	—	—	A16	A16	A16
192	In		—	—	—	A17	A17	LA17
193	In		—	—	—	A18	A18	LA18
194	In		—	—	—	A19	A19	LA19
195	In		—	—	—	A20	A20	LA20
196	In		—	—	—	A21	A21	LA21
197	In		—	—	—	A22	A22	LA22
198	In		—	—	—	A23	A23	LA23
199	In		—	—	—	A24	A24	—
200	In		—	—	—	A25	A25	—
202	In		—	—	—	A26	A26	—
203	In		—	—	—	A27	A27	IORD#
204	In		—	—	—	A28	A28	IOWR#
205	I/O		–12	12	50	A29	A29	ZWS#
206	I/O		–12	12	50	A30	A30	IOCS16#
207	I/O		–12	12	50	A31	A31	MCS16#

Note: I_{OL}/I_{OH} are specified in mA; Load is specified in pF; • in 'PU' column indicates high value (50KΩ) internal pullup at RESET

Pin List - Bus Interface

Pin #	Type	PU	I_{OH}	I_{OL}	Load	VL Bus	386 DX	ISA Bus
51	I/O		–8	8	50	D0	D0	D0
50	I/O		–8	8	50	D1	D1	D1
49	I/O		–8	8	50	D2	D2	D2
48	I/O		–8	8	50	D3	D3	D3
46	I/O		–8	8	50	D4	D4	D4
45	I/O		–8	8	50	D5	D5	D5
43	I/O		–8	8	50	D6	D6	D6
42	I/O		–8	8	50	D7	D7	D7
40	I/O		–8	8	50	D8	D8	D8
39	I/O		–8	8	50	D9	D9	D9
37	I/O		–8	8	50	D10	D10	D10
36	I/O		–8	8	50	D11	D11	D11
34	I/O		–8	8	50	D12	D12	D12
33	I/O		–8	8	50	D13	D13	D13
32	I/O		–8	8	50	D14	D14	D14
31	I/O		–8	8	50	D15	D15	D15
21	I/O		–8	8	50	D16	D16	—
20	I/O		–8	8	50	D17	D17	—
19	I/O		–8	8	50	D18	D18	—
18	I/O		–8	8	50	D19	D19	—
16	I/O		–8	8	50	D20	D20	—
15	I/O		–8	8	50	D21	D21	—
13	I/O		–8	8	50	D22	D22	—
12	I/O		–8	8	50	D23	D23	—
10	I/O		–8	8	50	D24	D24	—
9	I/O		–8	8	50	D25	D25	—
7	I/O		–8	8	50	D26	D26	—
6	I/O		–8	8	50	D27	D27	—
4	I/O		–8	8	50	D28	D28	—
3	I/O		–8	8	50	D29	D29	—
2	I/O		–8	8	50	D30	D30	—
1	I/O		–8	8	50	D31	D31	—

Note: I_{OL}/I_{OH} are specified in mA; Load is specified in pF; • in 'PU' column indicates high value (50KΩ) internal pullup at RESET

Pin List - Display Memory Interface

Pin #	Type	PU	I_{OH}	I_{OL}	Load	Function	Alt
137	Out		–8	8	50	MA0	XA0
138	Out		–16	16	50	MA1	—
142	Out		–16	16	50	MA2	—
146	Out		–16	16	50	MA3	—
149	Out		–16	16	50	MA4	—
152	Out		–8	8	50	MA5	XA5
153	Out		–8	8	50	MA6	XA6
154	Out		–8	8	50	MA7	XA7
155	Out		–8	8	50	MA8	XA8
132	Out	✓	–8	8	50	RASA#	XRAS#
53	Out	✓	–8	8	50	RASB#	—
89	Out		–12	12	50	CASAL0#	WEAL#
88	Out		–12	12	50	CASAH0#	WEAH#
87	Out		–12	12	50	CASBL0#	WEBL#
86	Out		–12	12	50	CASBH0#	WEBH#
131	Out		–12	12	50	CASAL1#	CASA0#
130	Out		–12	12	50	CASAH1#	CASA1#
55	Out		–12	12	50	CASBL1#	CASB1#
54	Out		–12	12	50	CASBH1#	CASB0#
57	Out		–12	12	50	WE#	MA9
56	Out		–12	12	50	OE#	—
140	Out		–16	16	50	XA1	—
144	Out		–16	16	50	XA2	—
148	Out		–16	16	50	XA3	—
151	Out		–16	16	50	XA4	—
136	Out		–4	4	50	XCAS0#	—
135	Out	✓	–4	4	50	XCAS1#	—
134	Out	✓	–4	4	50	XWE#	—
133	Out		–4	4	50	XOE#	—
139	I/O		–4	4	50	XD0	—
143	I/O		–4	4	50	XD1	—
147	I/O		–4	4	50	XD2	—
150	I/O		–4	4	50	XD3	—

Pin #	Type	PU	I_{OH}	I_{OL}	Load	Function	Alt
97	I/O		–4	4	50	MAD0	CFG0
96	I/O		–4	4	50	MAD1	CFG1
95	I/O		–4	4	50	MAD2	CFG2
94	I/O		–4	4	50	MAD3	CFG3
93	I/O		–4	4	50	MAD4	CFG4
92	I/O		–4	4	50	MAD5	CFG5
91	I/O		–4	4	50	MAD6	CFG6
90	I/O		–4	4	50	MAD7	CFG7
85	I/O		–4	4	50	MAD8	CFG8
84	I/O		–4	4	50	MAD9	CFG9
83	I/O		–4	4	50	MAD10	CFG10
82	I/O		–4	4	50	MAD11	CFG11
81	I/O		–4	4	50	MAD12	CFG12
79	I/O		–4	4	50	MAD13	CFG13
78	I/O		–4	4	50	MAD14	CFG14
76	I/O		–4	4	50	MAD15	CFG15
75	I/O		–4	4	50	MBD0	—
74	I/O		–4	4	50	MBD1	—
73	I/O		–4	4	50	MBD2	—
72	I/O		–4	4	50	MBD3	—
71	I/O		–4	4	50	MBD4	—
70	I/O		–4	4	50	MBD5	—
69	I/O		–4	4	50	MBD6	—
68	I/O		–4	4	50	MBD7	—
67	I/O		–4	4	50	MBD8	—
65	I/O		–4	4	50	MBD9	—
64	I/O		–4	4	50	MBD10	—
62	I/O		–4	4	50	MBD11	—
61	I/O		–4	4	50	MBD12	—
60	I/O		–4	4	50	MBD13	—
59	I/O		–4	4	50	MBD14	—
58	I/O		–4	4	50	MBD15	—

Note: I_{OL}/I_{OH} are specified in mA; Load is specified in pF; • in 'PU' column indicates high value (50KΩ) internal pullup at RESET

Pin List - CRT Interface

Pin #	Type	PU	I_{OH}	I_{OL}	Load	Function	Alt
127	Out		–12	12	50	HSYNC	—
128	Out		–12	12	50	VSYNC	—
105	—		—	—	—	RSET	—
104	—		—	—	—	COMP	—
99	Out		—	—	—	RED	—
101	Out		—	—	—	GREEN	—
102	Out		—	—	—	BLUE	—
100	VCC		—	—	—	AVCC	—
103	GND		—	—	—	AGND	—

Pin List - Clock

Pin #	Type	PU	I_{OH}	I_{OL}	Load	Function	Alt
182	I/O		–2	2	50	MCLK	—
158	In		—	—	—	XTALI	VCLK
159	Out		–1	1	25	XTALO	—
160	VCC		—	—	—	CVCC0	—
161	VCC		—	—	—	CVCC1	—
157	GND		—	—	—	CGND0	—
163	GND		—	—	—	CGND1	—

Pin List - Video Port

Pin #	Type	PU	I_{OH}	I_{OL}	Load	Function	Alt
125	I/O		–4	4	50	KEY	BLANK#
124	Out		–8	8	50	PCLK	—
107	I/O		–4	4	50	VID0	P0
108	I/O		–4	4	50	VID1	P1
109	I/O		–4	4	50	VID2	P2
110	I/O		–4	4	50	VID3	P3
111	I/O		–4	4	50	VID4	P4
112	I/O		–4	4	50	VID5	P5
113	I/O		–4	4	50	VID6	P6
114	I/O		–4	4	50	VID7	P7
116	In		—	—	50	VID8	—
117	In		—	—	50	VID9	—
118	In		—	—	50	VID10	—
119	In		—	—	50	VID11	—
120	In		—	—	50	VID12	—
121	In		—	—	50	VID13	—
122	In		—	—	50	VID14	—
123	In		—	—	50	VID15	—

Pin List - Power and Ground

Pin #	Type	PU	I_{OH}	I_{OL}	Load	Function	Alt
5	VCC		—	—	—	BVCC	—
14	VCC		—	—	—	BVCC	—
38	VCC		—	—	—	BVCC	—
47	VCC		—	—	—	BVCC	—
66	VCC		—	—	—	MVCC	—
80	VCC		—	—	—	IVCC	—
126	VCC		—	—	—	DVCC	—
145	VCC		—	—	—	XVCC	—
181	VCC		—	—	—	IVCC	—
201	VCC		—	—	—	RVCC	—
8	GND		—	—	—	BGND	—
17	GND		—	—	—	BGND	—
27	GND		—	—	—	BGND	—
35	GND		—	—	—	BGND	—
44	GND		—	—	—	BGND	—
52	GND		—	—	—	BGND	—
63	GND		—	—	—	MGND	—
77	GND		—	—	—	IGND	—
98	GND		—	—	—	MGND	—
106	GND		—	—	—	RGND	—
115	GND		—	—	—	DGND	—
129	GND		—	—	—	XGND	—
141	GND		—	—	—	XGND	—
156	GND		—	—	—	XGND	—
172	GND		—	—	—	BGND	—
184	GND		—	—	—	IGND	—
208	GND		—	—	—	BGND	—

Pin List - General Purpose I/O

Pin #	Type	PU	I_{OH}	I_{OL}	Load	Function	Alt
164	I/O		–4	4	50	GPIO 2	EVIDEO#
165	I/O		–4	4	50	GPIO 3	ESYNC#
166	I/O		–4	4	50	GPIO 5	ECLK#
167	I/O		–4	4	50	GPIO 6	CSEL 0
168	I/O		–4	4	50	GPIO 7	CSEL 1

Note: I_{OL}/I_{OH} are specified in mA; Load is specified in pF; • in 'PU' column indicates high value (50KΩ) internal pullup at RESET

PIN DESCRIPTIONS

CPU Direct/VL-Bus Interface

Pin #	Pin Name	Type	Active	Description
51	D00	I/O	High	System Data Bus. In 32-bit CPU Local Bus designs these data lines connect directly to the processor data lines. On the VL-Bus they connect to the corresponding buffered or unbuffered data signal.
50	D01	I/O	High	
49	D02	I/O	High	
48	D03	I/O	High	
46	D04	I/O	High	
45	D05	I/O	High	
43	D06	I/O	High	
42	D07	I/O	High	
40	D08	I/O	High	
39	D09	I/O	High	
37	D10	I/O	High	
36	D11	I/O	High	
34	D12	I/O	High	
33	D13	I/O	High	
32	D14	I/O	High	
31	D15	I/O	High	
21	D16	I/O	High	
20	D17	I/O	High	
19	D18	I/O	High	
18	D19	I/O	High	
16	D20	I/O	High	
15	D21	I/O	High	
13	D22	I/O	High	
12	D23	I/O	High	
10	D24	I/O	High	
9	D25	I/O	High	
7	D26	I/O	High	
6	D27	I/O	High	
4	D28	I/O	High	
3	D29	I/O	High	
2	D30	I/O	High	
1	D31	I/O	High	

PIN DESCRIPTIONS **CPU Direct/VL-Bus Interface (continued)**

Pin #	Pin Name	Type	Active	Description
41	BE0#	In	Low	Byte Enable 0. Indicates data transfer on D7:D0 for the current cycle.
30	BE1#	In	Low	Byte Enable 1. Indicates data transfer on D15:D8 for the current cycle.
22	BE2#	In	Low	Byte Enable 2. Indicates data transfer on D23:D16 for the current cycle.
11	BE3#	In	Low	Byte Enable 3. BE3# indicates that data is to be transferred over the data bus on D31:24 during the current access.
173	A2	In	High	System Address Bus
174	A3	In	High	
175	A4	In	High	In both VL-Bus and 32-bit CPU address interfaces the pins are connected directly to the bus.
176	A5	In	High	
177	A6	In	High	
178	A7	In	High	
179	A8	In	High	
180	A9	In	High	
185	A10	In	High	
186	A11	In	High	
187	A12	In	High	
188	A13	In	High	
189	A14	In	High	
190	A15	In	High	
191	A16	In	High	
192	A17	In	High	
193	A18	In	High	
194	A19	In	High	
195	A20	In	High	
196	A21	In	High	
197	A22	In	High	
198	A23	In	High	
199	A24	In	High	
200	A25	In	High	
202	A26	In	High	
203	A27	In	High	
204	A28	In	High	
205	A29	In	High	
206	A30	In	High	
207	A31	In	High	

PIN DESCRIPTIONS **CPU Direct/VL-Bus Interface (continued)**

Pin #	Pin Name	Type	Active	Description
162	RESET	In	High	Reset. Connect directly to the system reset signal. In direct CPU local bus interfaces, RESET should be connected to the system reset which is generated by the motherboard system logic for all peripherals. It is not connected to the RESET# pin of the processor.
25	LRDY#	OC	Low	Local Ready. Driven low during VL-Bus and CPU local bus cycles to indicate the current cycle should be completed. This signal is driven high at the end of the cycle, then tristated. In VESA local bus cycles the end of the cycle is acknowledged with RDYRTN#.
24	RDYRTN#	In	Low	Handshaking signal in the VL-Bus interface indicating synchronization of RDY# by the local bus master/controller to the processor. Upon receipt of this HCLK synchronous signal the 64300 / 301 will stop driving the bus (if a read cycle was active) and terminate the current cycle. For processor interfaces other than VL-Bus the RDYRTN# pin should be connected to LRDY#.
26	LDEV#	Out/OC	Low	In VL-Bus and CPU local bus interfaces indicates that the 64300 / 301 owns the current cycle based on the memory or I/O address which has been broadcast. It may be an output buffer or an open collector driver sharing a common control signal with other local devices.
23	ADS#	In	Low	In VL-Bus and CPU local bus interfaces indicates valid address and control signal information is present. It is used for all decodes to indicate the start of a bus cycle.
29	M/IO#	In	Both	In VL-Bus and CPU local bus interfaces indicates memory or I/O cycle: 1 = memory, 0 = I/O. It is sampled on the rising edge of the (internal) 1x CPU clock when ADS# is active.
28	W/R#	In	Low	This control signal indicates a write (high) or read (low) operation. It is sampled on the rising edge of the (internal) 1x CPU clock when ADS# is active.
169	VGARD	Out	High	In interfaces requiring external bus drivers, controls the direction of bi-directional transceivers, 0 = VGA write or other bus transaction, 1 = VGA read (Drive transceivers on to bus).

PIN DESCRIPTIONS **CPU Direct/VL-Bus Interface (continued)**

Pin #	Pin Name	Type	Active	Description
183	LCLK	In	Both	Local Clock. In VL-Bus and CPU local bus interfaces it is connected to the CPU 1x clock. Most 386DX, and all 486 chipsets generate the required 1x clock. Note that the frequency of LCLK must be less than or equal to the internal memory clock: $f_{LCLK} \leq f_{MCLK}$
170	IRQ# (IRQ)	Out	Both	Frame Interrupt Output. Interrupt polarity is programmable. Set when interrupt on VSYNC is enabled. Cleared by reprogramming register 11h in the CRT Controller. See also XR14 bit–7.
171	ROMCS#	Out	Low	For VL-Bus add-on cards indicates valid ROM access in memory address range 00C0000-00C7FFFh. Note that the 64300 / 301 does not respond with LRDY#. It is expected that if a ROM is implemented it will transfer its data across the ISA bus. This permits the ISA controller to handle the byte steering to the CPU. For direct interface planar designs not requiring a VGA ROM simply do not connect this pin.

PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
51	D00	I/O	High	System Data Bus.
50	D01	I/O	High	
49	D02	I/O	High	The 64300 / 301 data bus should be buffered using
48	D03	I/O	High	74LS245 bus drivers to meet the required drive level of
46	D04	I/O	High	the ISA bus.
45	D05	I/O	High	
43	D06	I/O	High	
42	D07	I/O	High	
40	D08	I/O	High	
39	D09	I/O	High	
37	D10	I/O	High	
36	D11	I/O	High	
34	D12	I/O	High	
33	D13	I/O	High	
32	D14	I/O	High	
31	D15	I/O	High	
21	n/c			Do Not Connect
20	n/c			(Do not connect any signals to these pins. They are
19	n/c			used internally for other purposes.)
18	n/c			
16	n/c			
15	n/c			
13	n/c			
12	n/c			
10	n/c			
9	n/c			
7	n/c			
6	n/c			
4	n/c			
3	n/c			
2	n/c			
1	n/c			

PIN DESCRIPTIONS **ISA Bus Interface (continued)**

Pin #	Pin Name	Type	Active	Description
41	A0	In	High	System Address Bus
22	A1	In	High	
173	A2	In	High	For the ISA bus interface the system address pins are connected directly to the respective ISA bus signal.
174	A3	In	High	
175	A4	In	High	
176	A5	In	High	
177	A6	In	High	
178	A7	In	High	
179	A8	In	High	
180	A9	In	High	
185	A10	In	High	
186	A11	In	High	
187	A12	In	High	
188	A13	In	High	
189	A14	In	High	
190	A15	In	High	
191	A16	In	High	
192	LA17	In	High	
193	LA18	In	High	
194	LA19	In	High	
195	LA20	In	High	
196	LA21	In	High	
197	LA22	In	High	
198	LA23	In	High	
11	n/c			Do Not Connect
199	n/c			
200	n/c			
202	n/c			
183	n/c			
30	BHE#	In	Low	Byte High Enable. Indicates valid data to be transferred on D15:8 during current cycle.
205	ZWS#	OC	Low	Zero Wait State. Indicates that the current 16-bit ISA bus memory cycle may be terminated. This pin should be connected to the OWS# signal on the ISA bus.
206	IOCS16#	OC	High	I/O Select 16. Indicates that the 64300 / 301 is capable of handling a 16-bit I/O cycle at the current address. This pin should be connected to the I/O CS16# signal.
207	MCS16#	OC	High	Memory Select 16. Indicates that the 64300 / 301 is capable of handling a 16-bit memory cycle at the current address. This pin should be connected to the MEM CS16# signal.

PIN DESCRIPTIONS **ISA Bus Interface (continued)**

Pin #	Pin Name	Type	Active	Description
162	RESET	In	High	Reset. Connect directly to the ISA reset signal (RESET DRV).
25	RDY#	OC	High	Ready. Driven low during a 64300 / 301 cycle to indicate that the current cycle should be extended (not ready). This pin should be connected to the I/O CH RDY# signal on the ISA bus.
24	RFSH#	In	Low	Refresh. Indicates that the current memory read access is a refresh cycle.
23	ALE	In	High	Address Latch Enable. Indicates a valid address available on LA23:17 and SA16:0. Internally this is used to transparently latch the unlatched addresses LA23:17. The SA16:0 addresses are not latched.
28	MEMR#	In	Low	Indicates a Memory Read cycle. This pin should be connected to the MEMR# signal on the 16-bit ISA bus extension.
26	MEMW#	In	Low	Indicates a Memory Write cycle. This pin should be connected to the MEMW# signal on the 16-bit ISA bus extension.
203	IORD#	In	Low	Indicates an I/O Read Cycle. This pin should be connected to the IOR# signal on the ISA bus.
204	IOWR#	In	Low	Indicates an I/O Write Cycle. This pin should be connected to the IOW# signal on the ISA bus.
169	VGARD	Out	High	VGA Read. Indicates that a 64300 / 301 register, VGA display memory, or the VGA ROM BIOS is being read during the current cycle. This signal may be used to control the direction of data bus transceivers (eg. 74LS245) which are driving the ISA data bus.
29	AEN	In	High	Address Enable. Defines a valid (non-DMA) I/O address. 0 = Valid I/O address 1 = Invalid I/O address (DMA active)
170	IRQ#	Out	Both	Frame Interrupt Output. Interrupt polarity is programmable. Set when interrupt on VSYNC is enabled. Cleared by reprogramming register 11h in the CRT Controller.
171	ROMCS#	Out	Low	For ISA add-on cards indicate valid VGA ROM access in memory address range 00C0000-00C7FFFh. It is qualified with the address only. ROM data must share the low byte ISA data bus transceiver with the 64300 / 301. See schematic examples for implementation.

PIN DESCRIPTIONS

Display Memory Interface

Pin #	Pin Name		Type	Active	Description
137	MA0	(XA0)	Out	High	DRAM address bus. If an accelerator RAM is installed it uses address lines XA8:5,0 which are shared with MA8:5,0 in conjunction with XA4:1.
138	MA1		Out	High	
142	MA2		Out	High	
146	MA3		Out	High	
149	MA4		Out	High	
152	MA5	(XA5)	Out	High	
153	MA6	(XA6)	Out	High	
154	MA7	(XA7)	Out	High	
155	MA8	(XA8)	Out	High	
132	RASA#	(XRAS#)	Out	Low	Row address strobe for memory bus "A" (planes 0-1) and accelerator RAM if installed.
53	RASB#		Out	Low	Row address strobe for memory bus "B" (planes 2-3).
89	CASAL0#	(WEAL#)	Out	Low	Column address strobe for Bank 0/Plane 0 in configurations using 2 CAS#/1 WE#. In configurations using 2 WE#/1 CAS# this pin is the Write Enable for plane 0.
88	CASAH0#	(WEAH#)	Out	Low	Column address strobe for Bank 0/Plane 1 in configurations using 2 CAS#/1 WE#. In configurations using 2 WE#/1 CAS# this pin is the Write Enable for plane 1.
87	CASBL0#	(WEBL#)	Out	Low	Column address strobe for Bank 0/Plane 2 in configurations using 2 CAS#/1 WE#. In configurations using 2 WE#/1 CAS# this pin is the Write Enable for plane 2.
86	CASBH0#	(WEBH#)	Out	Low	Column address strobe for Bank 0/Plane 3 in configurations using 2 CAS#/1 WE#. In configurations using 2 WE#/1 CAS# this pin is the Write Enable for plane 3.
131	CASAL1#	(CASA0#)	Out	Low	Column address strobe for Bank 1/Plane 0 in configurations using 2 CAS#/1 WE#. In configurations using 2 WE#/1 CAS# this pin is the Column Address Strobe for Bank 0/Plane 0+1.
130	CASAH1#	(CASA1#)	Out	Low	Column address strobe for Bank 1/Plane 1 in configurations using 2 CAS#/1 WE#. In configurations using 2 WE#/1 CAS# this pin is the Column Address Strobe for Bank 1/Plane 0+1.
55	CASBL1#	(CASB1#)	Out	Low	Column address strobe for Bank 1/Plane 2 in configurations using 2 CAS#/1 WE#. In configurations using 2 WE#/1 CAS# this pin is the Column Address Strobe for Bank 1/Plane 2+3.
54	CASBH1#	(CASB0#)	Out	Low	Column address strobe for Bank 1/Plane 3 in configurations using 2 CAS#/1 WE#. In configurations using 2 WE#/1 CAS# this pin is the Column Address Strobe for Bank 0/Plane 2+3.

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS **Display Memory Interface (continued)**

Pin #	Pin Name		Type	Active	Description
57	WE#	(MA9)	Out	Low	Write Enable in configurations using a common Write Enable and one CAS per plane.
56	OE#		Out	Low	Output Enable
97	MAD0	(Bus Type)	I/O	High	Plane 0 Memory Data
96	MAD1	(Bus Type)	I/O	High	On the trailing edge of RESET the chip configuration is
95	MAD2	(Reserved)	I/O	High	latched from these pins. The state of the configuration
94	MAD3	(Reserved)	I/O	High	is saved in XR01.
93	MAD4	(Int Clock)	I/O	High	
92	MAD5	(Crystal)	I/O	High	
91	MAD6	(LDEV#)	I/O	High	
90	MAD7	(Cache Delay)	I/O	High	
85	MAD8	(CFG8)	I/O	High	Plane 1 Memory Data
84	MAD9	(CFG9)	I/O	High	The upper 8 configuration bits are latched from
83	MAD10	(CFG10)	I/O	High	MAD15:8 on the trailing edge of RESET. This data
82	MAD11	(CFG11)	I/O	High	may be read in XR74.
81	MAD12	(CFG12)	I/O	High	
79	MAD13	(CFG13)	I/O	High	
78	MAD14	(CFG14)	I/O	High	
76	MAD15	(CFG15)	I/O	High	
75	MBD0		I/O	High	Plane 2 Memory Data
74	MBD1		I/O	High	
73	MBD2		I/O	High	
72	MBD3		I/O	High	
71	MBD4		I/O	High	
70	MBD5		I/O	High	
69	MBD6		I/O	High	
68	MBD7		I/O	High	
67	MBD8		I/O	High	Plane 3 Memory Data
65	MBD9		I/O	High	
64	MBD10		I/O	High	
62	MBD11		I/O	High	
61	MBD12		I/O	High	
60	MBD13		I/O	High	
59	MBD14		I/O	High	
58	MBD15		I/O	High	

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS **Display Memory Interface (continued)**

Pin #	Pin Name	Type	Active	Description
140 144 148 151	XA1 XA2 XA3 XA4	Out Out Out Out	High High High High	Memory address for optional accelerator RAM. XA4:1 in combination with MA8:5, and MA0 define the nine bit address for the accelerator RAM.
136	XCAS0#	Out	Low	Column address strobe for bank 0 accelerator RAM
135	XCAS1#	Out	Low	Column address strobe for bank 1 accelerator RAM
134	XWE#	Out	Low	Write Enable for accelerator RAM
133	XOE#	Out	Low	Output Enable for accelerator RAM
139 143 147 150	XD0 XD1 XD2 XD3	I/O I/O I/O I/O	High High High High	Accelerator RAM Memory Data

Note: The above XRAM control signals are applicable to the 64300 only and should not be connected when using the 64301.

PIN DESCRIPTIONS — CRT Video Interface

Pin #	Pin Name		Type	Active	Description
127	HSYNC		Out	Both	CRT Horizontal Sync pulse (programmable polarity).
128	VSYNC		Out	Both	CRT Vertical Sync pulse (programmable polarity).
125	KEY		In	High	Live Video Key. If an external palette is not enabled (XR06[0]=0) then this pin is an input (KEY) which can be used to qualify live video overlays.
		(BLANK#)	Out	Both	Blanking signal for an external color palette chip (polarity is programmable: see XR28 bit-0). This pin may also be redefined as a Display Enable signal (see XR28 bit-1). External RAMDAC support may be enabled via XR06[0] and XR73[4]. BLANK# may also be used by an external secondary video source for synchronization.
164	GPIO 2	(EVIDEO#)	I/O	Both	This pin is a general purpose I/O pin. It is controlled through extended registers XR71 and XR72. When the feature connector is enabled, this pin becomes the EVIDEO# input. When low, it tri-states the P7:0 data.
165	GPIO 3	(ESYNC#)	I/O	Both	This pin is a general purpose I/O pin. It is controlled through extended registers XR71 and XR72. When the feature connector is enabled, this pin becomes the ESYNC# input. When low, it tri-states the VSYNC, HSYNC, and BLANK# outputs.
124	PCLK		Out	Both	Pixel Data clock. Pixel data is valid on P7:0 on the rising edge of PCLK while BLANK# is inactive. BLANK# is also sampled on the rising edge of PCLK.
105	RSET		In	n/a	Analog reference. The internal RAMDAC has an internal voltage reference to set its maximum output current. A resistor value of 383Ω is required between RSET and AGND to correctly set the maximum output voltage to 713mV assuming 150Ω output load resistors on the RGB outputs (a total load of 50Ω).
99	RED		Out	High	RGB analog outputs. These current sources have a maximum output current set by the internal voltage reference. They are PS/2 compatible (no sync on green; 50Ω load when connected to a 75Ω matched impedance cable).
101	GREEN		Out	High	
102	BLUE		Out	High	

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS **CRT Video Interface (continued)**

Pin #	Pin Name		Type	Active	Description
107	VID0	(P0)	I/O	High	8-bit CRT pixel data to external RAMDAC if XR06[0] = 1. If XR06[0] = 0, these pins are used to input the low byte of the 16-bit RGB live video overlay.
108	VID1	(P1)	I/O	High	
109	VID2	(P2)	I/O	High	
110	VID3	(P3)	I/O	High	
111	VID4	(P4)	I/O	High	
112	VID5	(P5)	I/O	High	
113	VID6	(P6)	I/O	High	
114	VID7	(P7)	I/O	High	
116	VID8		In	High	These pins input the high byte of the 16-bit RGB live video overlay.
117	VID9		In	High	
118	VID10		In	High	
119	VID11		In	High	
120	VID12		In	High	
121	VID13		In	High	
122	VID14		In	High	
123	VID15		In	High	
100	AVCC		VCC	--	Analog power for the internal RAMDAC. This power should be isolated from the digital VCC as described in the Functional Description of the internal RAMDAC.
103	AGND		GND	--	Analog ground for the internal RAMDAC. The analog ground should be common with the digital ground but must be tightly decoupled to the AVCC power pin. See the Functional Description of the internal RAMDAC for a complete description.
104	COMP		In	--	Decoupling node for internal DAC reference current. Connect a 0.1µf capacitor between this pin and AVCC as close to the 64300 / 301 as possible.

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS **Misc, Clock, Power, and Ground**

Pin #	Pin Name		Type	Active	Description
166	GPIO 5	(ECLK#)	I/O	Both	General Purpose I/O. When the feature connector is enabled, this pin becomes the ECLK# input. When low, it will tri-state the output of the pixel clock (PCLK).
167 168	GPIO 6 GPIO 7	(CSEL0) (CSEL1)	I/O I/O	Both Both	These pins are general purpose outputs when using the internal clock synthesizer. If an external clock synthesizer is used (XR01[4]=0) they reflect the state of MSR[3:2] clock select bits.
182	MCLK		I/O	n/a	When using the internal clock synthesizer this pin outputs the memory clock. If an external clock synthesizer is used (XR01[4]=0) then this is the input pin for the memory clock.
158	XTALI	(VCLK)	In	n/a	When using the internal clock synthesizer this pin should be connected directly to a series resonant 14.31818MHz crystal (XR01[5]=1) or a 14.31818MHz reference source (XR01[5]=0). If an external clock synthesizer is used (XR01[4]=0) then this is the video clock input.
159	XTALO		Out	n/a	For internal clock synthesizer use with an external crystal (XR01[5:4]=11) this pin should be connected directly to one of the pins of a series resonant 14.31818MHz crystal. If an external 14.3818MHz source or external clock synthesizer is used this pin must be left unconnected.
160 161 157 163	CVCC0 CVCC1 CGND0 CGND1		VCC VCC GND GND	-- -- -- --	Analog Power pins for the internal clock synthesizer. These power and ground pins must be carefully decoupled individually. Read the section on clock ground layout in the Functional Description.

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

Digital Power and Ground

Pin #	Pin Name	Type	Active	Description
5	BVCC	VCC	--	Power (Bus)
14	BVCC	VCC	--	Power (Bus)
38	BVCC	VCC	--	Power (Bus)
47	BVCC	VCC	--	Power (Bus)
66	MVCC	VCC	--	Power (Memory)
80	IVCC	VCC	--	Power (Internal Logic)
126	DVCC	VCC	--	Power (Display)
145	XVCC	VCC	--	Power (XRAM)
181	IVCC	VCC	--	Power (Internal Logic)
201	RVCC	VCC	--	Power (Reference)
8	BGND	GND	--	Ground (Bus)
17	BGND	GND	--	Ground (Bus)
27	BGND	GND	--	Ground (Bus)
35	BGND	GND	--	Ground (Bus)
44	BGND	GND	--	Ground (Bus)
52	BGND	GND	--	Ground (Bus)
63	MGND	GND	--	Ground (Memory)
77	IGND	GND	--	Ground (Internal Logic)
98	MGND	GND	--	Ground (Memory)
106	RGND	GND	--	Ground (Reference Current - DAC)
115	DGND	GND	--	Ground (Display)
129	XGND	GND	--	Ground (XRAM)
141	XGND	GND	--	Ground (XRAM)
156	XGND	GND	--	Ground (XRAM)
172	BGND	GND	--	Ground (Bus)
184	IGND	GND	--	Ground (Internal Logic)
208	BGND	GND	--	Ground (Bus)

Note: Pin names in parentheses (...) indicate alternate functions

I/O Map

Port Address	Read	Write	
0102	Global Enable	Global Enable	
03B0	Reserved for MDA/Hercules	Reserved for MDA/Hercules	
03B1	Reserved for MDA/Hercules	Reserved for MDA/Hercules	**Mono**
03B2	Reserved for MDA/Hercules	Reserved for MDA/Hercules	**Mode**
03B3	Reserved for MDA/Hercules	Reserved for MDA/Hercules	
03B4	CRTC Index	CRTC Index	
03B5	CRTC Data	CRTC Data	
03B6	Reserved for MDA/Hercules	Reserved for MDA/Hercules	
03B7	Reserved for MDA/Hercules	Reserved for MDA/Hercules	
03B8	Reserved for Hercules Mode Register	Reserved for Hercules Mode Register	
03B9	--	Set Light Pen FF (ignored)	
03BA	Status Register (STAT)	Feature Control Register (FCR)	
03BB	--	Clear Light Pen FF (ignored)	
03BC	Reserved for system parallel port		
03BD			
03BE			
03BF	Reserved for Hercules Configuration Reg	Reserved for Hercules Configuration Reg	
03C0	Attribute Controller Index / Data	Attribute Controller Index / Data	
03C1	Attribute Controller Index / Data	Attribute Controller Index / Data	
03C2	Feature Control Register (FCR)	Miscellaneous Output Register (MSR)	
03C3	Reserved	Reserved	
03C4	Sequencer Index	Sequencer Index	
03C5	Sequencer Data	Sequencer Data	
03C6, 83C6	Color Palette Mask	Color Palette Mask	
03C7, 83C7	Color Palette State	Color Palette Read Mode Index	
03C8, 83C8	Color Palette Write Mode Index	Color Palette Write Mode Index	
03C9, 83C9	Color Palette Data	Color Palette Data	
03CA	Feature Read Register (FEAT)	--	
03CB	--	--	
03CC	Miscellaneous Output Register (MSR)	--	
03CD	--	--	
03CE	Graphics Controller Index	Graphics Controller Index	
03CF	Graphics Controller Data	Graphics Controller Data	
N3D0†	CHIPS™ DR Register Extensions	CHIPS™ DR Register Extensions	
N3D1†	CHIPS™ DR Register Extensions	CHIPS™ DR Register Extensions	**Color**
N3D2†	CHIPS™ DR Register Extensions	CHIPS™ DR Register Extensions	**Mode**
N3D3†	CHIPS™ DR Register Extensions	CHIPS™ DR Register Extensions	
03D4	CRTC Index	CRTC Index	
03D5	CRTC Data	CRTC Data	
03D6	CHIPS™ Extensions Index	CHIPS™ Extensions Index	
03D7	CHIPS™ Extensions Data	CHIPS™ Extensions Data	
03D8	Reserved for CGA Mode Register	Reserved for CGA Mode Register	
03D9	Reserved for CGA Color Register	Reserved for CGA Color Register	
03DA	Status Register (STAT)	Feature Control Register (FCR)	
03DB	--	Clear Light Pen FF (ignored)	
03DC	--	Set Light Pen FF (ignored)	
46E8	--	Setup Control	

Note: † Addresses may be of the form 'bnnn nn1b bbbb bb00' where bbbbbbbb is specified by I/O Base register XR07 and nnnnn specifies 1 of 32 DR registers.

REGISTER SUMMARY - CGA, MDA, AND HERCULES MODEs

Register	Register Name	Bits	Access	I/O Port - MDA/Herc	I/O Port - CGA	Comment
ST00 (STAT)	Display Status	7	R	3BA	3DA	ref only
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
MODE	CGA/MDA/Hercules Mode Control	7	R/W	3B8	3D8	ref only
COLOR	CGA Color Select	6	R/W	n/a	3D9	ref only
HCFG	Hercules Configuration	2	W	3BF	n/a	ref only
RX, R0-11	'6845' Registers	0-8	R/W	3B4-3B5	3D4-3D5	ref only

REGISTER SUMMARY - EGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
MSR	Miscellaneous Output	7	W	3C2	3C2	ref only
FCR	Feature Control	3	W	3BA	3DA	ref only
ST00 (FEAT)	Feature Read (Input Status 0)	4	R	3C2	3C2	ref only
ST01 (STAT)	Display Status (Input Status 1)	7	R	3BA	3DA	ref only
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
SRX, SR0-7	Sequencer	0-8	R/W	3C4-3C5	3C4-3C5	ref only
CRX, CR0-24	CRT Controller	0-8	R/W	3B4-3B5	3D4-3D5	ref only
GRX, GR0-8	Graphics Controller	0-8	R/W	3CE-3CF	3CE-3CF	ref only
ARX, AR0-14	Attributes Controller	0-8	R/W	3C0-3C1	3C0-3C1	ref only

REGISTER SUMMARY - VGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
SETUP	Setup Control	2	W	46E8	46E8	Disabled by XR70 bit-7
ENABLE	Global Enable	1	R/W	102	102	Setup Only
MSR	Miscellaneous Output	7	W	3C2	3C2	
			R	3CC	3CC	
FCR	Feature Control	3	W	3BA	3DA	
			R	3CA	3CA	
ST00 (FEAT)	Feature Read (Input Status 0)	4	R	3C2	3C2	
ST01 (STAT)	Display Status (Input Status 1)	6	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
DACMASK	Color Palette Pixel Mask	8	R/W	3C6, 83C6	3C6, 83C6	
DACSTATE	Color Palette State	2	R	3C7, 83C7	3C7, 83C7	
DACRX	Color Palette Read-Mode Index	8	W	3C7, 83C7	3C7, 83C7	
DACWX	Color Palette Write-Mode Index	8	R/W	3C8, 83C8	3C8, 83C8	
DACDATA	Color Palette Data 0-FF	3x6 or 3x8	R/W	3C9, 83C9	3C9, 83C9	
SRX, SR0-7	Sequencer	0-8	R/W	3C4-3C5	3C4-3C5	
CRX, CR0-24	CRT Controller	0-8	R/W	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	R/W	3CE-3CF	3CE-3CF	
ARX, AR0-14	Attributes Controller	0-8	R/W	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	R/W	3D6-3D7	3D6-3D7	
DR00-DR0C	32-Bit Registers	32	R/W	X3D0-X3D3	X3D0-X3D3	

REGISTER SUMMARY - INDEXED REGISTERS (VGA)

Register	Register Name	Bits	Register Type	Access (VGA)	Access (EGA)	I/O Port
SRX	Sequencer Index	3	VGA/EGA	R/W	R/W	3C4
SR0	Reset	2	VGA/EGA	R/W	R/W	3C5
SR1	Clocking Mode	6	VGA/EGA	R/W	R/W	3C5
SR2	Plane Mask	4	VGA/EGA	R/W	R/W	3C5
SR3	Character Map Select	6	VGA/EGA	R/W	R/W	3C5
SR4	Memory Mode	3	VGA/EGA	R/W	R/W	3C5
SR7	Reset Horizontal Character Counter	0	VGA	W	n/a	3C5
CRX	CRTC Index	6	VGA/EGA	R/W	R/W	3B4 Mono, 3D4 Color
CR0	Horizontal Total	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR1	Horizontal Display End	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR2	Horizontal Blanking Start	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR3	Horizontal Blanking End	5+2+1	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR4	Horizontal Retrace Start	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR5	Horizontal Retrace End	5+2+1	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR6	Vertical Total	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR7	Overflow	5	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR8	Preset Row Scan	5+2	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR9	Character Cell Height	5+3	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRA	Cursor Start	5+1	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRB	Cursor End	5+2	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRC	Start Address High	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRD	Start Address Low	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRE	Cursor Location High	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRF	Cursor Location Low	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
LPENH	Light Pen High	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
LPENL	Light Pen Low	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
CR10	Vertical Retrace Start	8	VGA/EGA	R/W	W	3B5 Mono, 3D5 Color
CR11	Vertical Retrace End	4+4	VGA/EGA	R/W	W	3B5 Mono, 3D5 Color
CR12	Vertical Display End	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR13	Offset	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR14	Underline Row Scan	5+2	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR15	Vertical Blanking Start	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR16	Vertical Blanking End	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR17	CRT Mode Control	7	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR18	Line Compare	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR22	Graphics Controller Data Latches	8	VGA	R	n/a	3B5 Mono, 3D5 Color
CR24	Attribute Controller Index/Data Latch	1	VGA	R	n/a	3B5 Mono, 3D5 Color
GRX	Graphics Controller Index	4	VGA/EGA	R/W	R/W	3CE
GR0	Set/Reset	4	VGA/EGA	R/W	R/W	3CF
GR1	Enable Set/Reset	4	VGA/EGA	R/W	R/W	3CF
GR2	Color Compare	4	VGA/EGA	R/W	R/W	3CF
GR3	Data Rotate	5	VGA/EGA	R/W	R/W	3CF
GR4	Read Map Select	2	VGA/EGA	R/W	R/W	3CF
GR5	Mode	6	VGA/EGA	R/W	R/W	3CF
GR6	Miscellaneous	4	VGA/EGA	R/W	R/W	3CF
GR7	Color Don't Care	4	VGA/EGA	R/W	R/W	3CF
GR8	Bit Mask	8	VGA/EGA	R/W	R/W	3CF
ARX	Attribute Controller Index	6	VGA/EGA	R/W	R/W	3C0 (3C1)
AR0-F	Internal Palette Regs 0-15	6	VGA/EGA	R/W	R/W	3C0 (3C1)
AR10	Mode Control	7	VGA/EGA	R/W	R/W	3C0 (3C1)
AR11	Overscan Color	6	VGA/EGA	R/W	R/W	3C0 (3C1)
AR12	Color Plane Enable	6	VGA/EGA	R/W	R/W	3C0 (3C1)
AR13	Horizontal Pixel Panning	4	VGA/EGA	R/W	R/W	3C0 (3C1)
AR14	Color Select	4	VGA	R/W	n/a	3C0 (3C1)
AR14	Color Select	4	VGA	R/W	n/a	3C0 (3C1)

EXTENSION REGISTER SUMMARY: 00-2F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family							
						450	451	452	453	64200	65510	65530	65535
XRX	**Extension Index**	7	R/W	3B6/3D6	- x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓
XR00	**Chip Version**	8	R/O	3B7/3D7	1 0 1 1 r r r r	✓	✓	✓	✓	✓	✓	✓	✓
XR01	**Configuration 1** (Config Bits 0-7)	8	R/O	3B7/3D7	d d d d d d d d	✓	✓	✓	✓	✓	✓	✓	✓
XR02	**CPU Interface Control 1**	5	R/W	3B7/3D7	x 0 0 0 0 - - -	✓	✓	✓	✓	✓	✓	✓	✓
XR03	**CPU Interface Control 2** *(Master Ct*	2	R/W	3B7/3D7	- - - - - - - 0 x	.	.	.	.	✓	.	.	.
XR04	**Memory Control 1**	6	R/W	3B7/3D7	- 0 0 - 0 0 0 0	✓	✓	✓	.	✓	✓	✓	✓
XR05	**Memory Control 2**	1	R/W	3B7/3D7	- - - 0 - - - -	.	.	.	.	.	.	.	✓
XR06	**Palette Control** *(DRAM Intfc)*	5	R/W	3B7/3D7	- - - 0 0 0 0 0	.	.	✓	.	.	✓	✓	✓
XR07	**I/O Base**	8	R/W	3B7/3D7	1 1 1 1 0 1 0 0	.	.	.	.	.	.	.	.
XR08	**Linear Base Low**	5	R/W	3B7/3D7	x x x x x - - -	.	.	.	.	.	.	.	.
XR09	**Linear Base High**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	.	.	.	.
XR0A	**XRAM Mode**	6	R/W	3B7/3D7	- - x x x x x x	.	.	.	.	.	.	.	.
XR0B	**CPU Paging**	4	R/W	3B7/3D7	- - - 0 - 0 0 0	✓	.	✓	✓	✓	✓	✓	✓
XR0C	**Start Address Top**	6	R/W	3B7/3D7	- 0 - 0 0 0 0 0	✓	.	✓	✓	✓	✓	✓	✓
XR0D	**Auxiliary Offset**	4	R/W	3B7/3D7	- - - - 0 0 0 0	✓	✓	✓	✓	✓	✓	✓	✓
XR0E	**Text Mode Control**	3	R/W	3B7/3D7	- - - - 0 0 - 0	✓	.	✓	.	✓	✓	✓	✓
XR0F	**Software Flags 0**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	.	✓	✓	✓
XR10	**Single/Low Map**	8	R/W	3B7/3D7	x x x x x x x x	✓	.	✓	✓	✓	✓	✓	✓
XR11	**High Map**	8	R/W	3B7/3D7	x x x x x x x x	✓	.	✓	✓	✓	✓	✓	✓
XR12	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR13	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR14	**Emulation Mode**	2	R/W	3B7/3D7	0 x 0 x x x x x	✓	✓	✓	✓	✓	✓	✓	✓
XR15	**Write Protect**	8	R/W	3B7/3D7	0 0 0 0 0 0 0 0	✓	✓	✓	✓	✓	✓	✓	✓
XR16	**Vertical Overflow**	5	R/W	3B7/3D7	- 0 - 0 - 0 0 0	.	.	.	.	.	.	.	✓
XR17	**Horizontal Overflow**	8	R/W	3B7/3D7	0 0 x 0 x 0 0 0	.	.	.	.	.	.	.	✓
XR18	-reserved- (Alternate H Disp End)	--	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓
XR19	**Halfline Compare** (Alt H Sync Sta	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓
XR1A	-reserved- (Alternate H Sync End)	--	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓
XR1B	-reserved- (Alternate H Total)	--	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓
XR1C	Alternate H Blank Start *(H Panel Size)*	--	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓
XR1D	-reserved- (Alternate H Blank End)	--	R/W	3B7/3D7	0 x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓
XR1E	-reserved- (Alternate Offset)	--	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓
XR1F	-reserved- (Virtual EGA Switch)	--	R/W	3B7/3D7	0 - - - x x x x	✓	.	.	.	✓	✓	✓	✓
XR20	-reserved- *(453 Interface II)/(SUD)*	--	--	3B7/3D7		.	.	✓	✓	.	.	.	.
XR21	-reserved- *(Sliding Hold A)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.
XR22	-reserved- *(Sliding Hold B)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.
XR23	-reserved- *(SHC)/(WBM Ctrl)*	--	--	3B7/3D7		.	.	✓	✓	.	.	.	.
XR24	-reserved- *(Alt Max Scan/WBM Patt)*	--	--	3B7/3D7		.	.	✓	✓	.	✓	✓	✓
XR25	-reserved- *(FP AltTxtHVirtPanelSiz)*	--	--	3B7/3D7		.	.	.	✓	.	.	✓	✓
XR26	-reserved- *(Alt HsyncStartOffset)*	--	--	3B7/3D7		.	.	.	✓	.	.	.	✓
XR27	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR28	**Video Interface**	8	R/W	3B7/3D7	• 0 0 0 • 0 0 0	✓	✓	✓	✓	✓	✓	✓	✓
XR29	-reserved- *(Function Control)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.
XR2A	-reserved- *(Frame Intrpt Count)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.
XR2B	**Software Flags 1** *(Default Video)*	8	R/W	3B7/3D7	0 0 0 0 0 0 0 0	✓	✓	✓	.	✓	✓	✓	✓
XR2C	-reserved- *(FLM Delay)*	--	--	3B7/3D7		.	.	✓	.	.	✓	✓	✓
XR2D	-reserved- *(LP Delay)*	--	--	3B7/3D7		.	.	✓	.	.	✓	✓	✓
XR2E	-reserved- *(LP Delay)*	--	--	3B7/3D7		.	.	✓	.	.	.	✓	✓
XR2F	-reserved- *(LP Width)*	--	--	3B7/3D7		.	.	✓	.	.	✓	✓	✓

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• = Not implemented (read/write, reset to 0)
r = Chip revision # (starting from 0000)

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 450–453 & 64xxx VGAs drive CRTs only, 65xxx VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

EXTENSION REGISTER SUMMARY: 30-5F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family							
						450	451	452	453	64200	65510	65530	65535
XR30	**Clock Divide Control** *(452 Curs Ad H*	4	R/W	3B7/3D7	- - - - x x x x	.	.	✓	.	.	.	.	✓
XR31	**Clock M Divisor** *(452 Curs Addr L)*	7	R/W	3B7/3D7	- x x x x x x x	.	.	✓	.	.	.	.	✓
XR32	**Clock N Divisor** *(452 Curs End Addr*	7	R/W	3B7/3D7	- x x x x x x x	.	.	✓	.	.	.	.	✓
XR33	**Clock Control** *(452 Curs X Pos H)*	5	R/W	3B7/3D7	- - x 0 - 0 0 0	.	.	✓	.	.	.	.	✓
XR34	-reserved- *(452 Curs X Pos L)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.
XR35	-reserved- *(452 Curs Y Pos H)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.
XR36	-reserved- *(452 Curs Y Pos L)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.
XR37	-reserved- *(452 Cursor Mode)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.
XR38	-reserved- *(452 Cursor Mask)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.
XR39	-reserved- *(452 Cursor Color 0)*	--	--	3B7/3D7		.	.	✓	.	.	.	.	.
XR3A	**Color Key Data 0** *(452 Curs Color1)*	8	R/W	3B7/3D7	x x x x x x x x	.	.	✓	.	.	.	.	✓
XR3B	**Color Key Data 1**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	.	.	.	✓
XR3C	**Color Key Data 2** *(Serial/Row Cnt)*	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	.	.	✓
XR3D	**Color Key Mask 0** *(MuxMode)*	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	.	.	✓
XR3E	**Color Key Mask 1**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	.	.	.	✓
XR3F	**Color Key Mask 2**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	.	.	.	✓
XR40	**BitBlt Configuration**	2	R/W	3B7/3D7	- - - - - - x x	.	.	.	.	.	.	.	.
XR41	-reserved- *(Virtual EGA Switch Reg)*	--	--	3B7/3D7		.	.	.	✓	.	.	.	.
XR42	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR43	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR44	**Software Flags 2**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	✓	.	✓	✓	✓
XR45	-reserved- *(S/W Flag 2 / FG Color)*	--	--	3B7/3D7		.	.	.	✓	.	.	.	✓
XR46	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR47	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR48	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR49	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR4A	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR4B	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR4C	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR4D	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR4E	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR4F	-reserved- *(Panel Format 2)*	--	--	3B7/3D7		.	.	.	.	.	.	.	✓
XR50	-reserved- *(Panel Format)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR51	-reserved- *(Display Type)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR52	**Refresh Control** *(PwrDn Ctr*	4	R/W	3B7/3D7	0 - - - - 0 0 0	.	.	.	.	.	✓	✓	✓
XR53	-reserved- *(Line Gr Override)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR54	-reserved- *(FP Intfc)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR55	-reserved- *(H Comp)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR56	-reserved- *(H Centering)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR57	-reserved- *(V Comp)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR58	-reserved- *(V Centering)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR59	-reserved- *(V Line Insertion)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR5A	-reserved- *(V Line Replication)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR5B	-reserved- *(Power Sequencing)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR5C	-reserved- *(Activity Timer Ctrl)*	--	--	3B7/3D7		.	.	.	.	.	.	.	✓
XR5D	-reserved- *(FP Diagnostic)*	--	--	3B7/3D7		.	.	.	.	.	.	.	✓
XR5E	-reserved- *(ACDCLK Ctrl)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR5F	-reserved- *(PwrDn Mode Rfsh)*	--	--	3B7/3D7		.	.	.	.	.	.	✓	✓

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Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column

Note: 450–453 & 64xxx VGAs drive CRTs only, 65xxx VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

EXTENSION REGISTER SUMMARY: 60-7F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family							
						450	451	452	453	64200	65510	65530	65535
XR60	**Blink Rate Control**	8	R/W	3B7/3D7	1 0 0 0 0 0 1 1	.	.	.	.	.	✓	✓	✓
XR61	-reserved- *(SmartMap™ Ctrl)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR62	-reserved- *(SmartMap™ Shift Parm)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR63	-reserved- *(SmartMap™ ColorMap Ctrl*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR64	-reserved- *(FP Alt V Total)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR65	-reserved- *(FP Alt Ovfl)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR66	-reserved- *(FP Alt VSync Start)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR67	-reserved- *(FP Alt VSync End)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR68	-reserved- *(FP V panelsize/Alt VDEend)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR69	-reserved- *(FP V Display Start 350)*	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR6A	-reserved- *(FP V Display End 350)*	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR6B	-reserved- *(FP V Overflow 2)*	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR6C	-reserved- *(Prog Output Drive/Wclk C)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR6D	-reserved- *(FRC Control)*	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR6E	-reserved- *(Polynomial FRC Ctrl)*	--	--	3B7/3D7		.	.	.	.	.	✓	✓	✓
XR6F	-reserved- *(Frame Buffer Ctrl)*	--	--	3B7/3D7		.	.	.	.	.	.	✓	✓
XR70	**Setup / Disable Control**	1	R/W	3B7/3D7	0 - - - - - - -	✓	.	.	.	✓	✓	✓	✓
XR71	**GPIO Control**	8	R/W	3B7/3D7	0 0 0 0 0 0 0 0	.	.	.	.	.	.	.	.
XR72	**GPIO Data** *(External Devide I/O)*	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	.	.	.	✓
XR73	**Misc Control**	8	R/W	3B7/3D7	0 0 0 0 0 x 0 x	.	.	.	.	.	.	.	.
XR74	**Configuration 2** (Config Bits 8-15)	8	R/W	3B7/3D7	d d d d d d d d	.	.	.	.	.	.	.	.
XR75	**Software Flags 3**	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	.	.	.	.
XR76	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR77	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR78	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR79	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR7A	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR7B	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR7C	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.	.
XR7D	**Diagnostic** *(FP Comp Diag)*	8	--	3B7/3D7		.	.	.	.	.	✓	✓	.
XR7E	-reserved- (CGA/Hercules Color Select)	--	R/W	3B7/3D7	- - x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓
XR7F	**Diagnostic**	8	R/O	3B7/3D7	0 0 x x x x 0 0	✓	✓	✓	.	✓	✓	✓	✓

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Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column

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32-BIT EXTENSION REGISTER SUMMARY

Reg	Group	Register Name	Bits	Access	Port	Reset			
DR00	BitBlt	BitBlt Offset	16/32	R/W	83D0-3	----xxxx	xxxxxxxx	----xxxx	xxxxxxxx
DR01	BitBlt	BitBlt Pattern ROP	16/32	R/W	87D0-3	--------	---xxxxx	xxxxxxxx	xxxxxxxx
DR02	BitBlt	BitBlt BG Color	16/32	R/W	8BD0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx
DR03	BitBlt	BitBlt FG Color	16/32	R/W	8FD0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx
DR04	BitBlt	BitBlt Control	16/32	R/W	93D0-3	--------	---0xxxx	xxxxxxxx	xxxxxxxx
DR05	BitBlt	BitBlt Source	16/32	R/W	97D0-3	--------	---xxxxx	xxxxxxxx	xxxxxxxx
DR06	BitBlt	BitBlt Destination	16/32	R/W	9BD0-3	--------	---xxxxx	xxxxxxxx	xxxxxxxx
DR07	BitBlt	BitBlt Command	16/32	R/W	9FD0-3	----0000	00000000	----xxxx	xxxxxxxx
DR08	Cursor	Cursor R/W Index	16/32	R/W	A3D0-3	-------x	xxxxxxxx	--------	00000000
DR09	Cursor	Cursor Color 0	16/32	R/W	A7D0-3	--------	xxxxxxxx	xxxxxxxx	xxxxxxxx
DR0A	Cursor	Cursor Color 1	16/32	R/W	ABD0-3	--------	xxxxxxxx	xxxxxxxx	xxxxxxxx
DR0B	Cursor	Cursor Position	16/32	R/W	AFD0-3	x----xxx	xxxxxxxx	x----xxx	xxxxxxxx
DR0C	Cursor	Cursor Data	16/32	R/W	B3D0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
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– = Not implemented (always reads 0)
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Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 450–453 & 64xxx VGAs drive CRTs only, 65xxx VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

Registers

GLOBAL CONTROL (SETUP) REGISTERS

The Setup Control Register and Video Subsystem Enable registers are used to enable or disable the VGA. The Setup Control register is also used to place the VGA in normal or setup mode (the Global Enable Register is accessible only during Setup mode). The Setup Control register is used in both ISA and local bus interfaces. The various internal 'disable' bits 'OR' together to provide multiple ways of disabling the chip; all 'disable' bits must be off to enable access to the chip. When the chip is 'disabled' in this fashion, only bus access is disabled; other functions remain operational (memory refresh, display refresh, etc).

Note: In setup mode in the IBM VGA, the Global Setup Register (defined as port address 102h) actually occupies the *entire I/O space* . Only the lower 3 bits are used to decode and select this register. To avoid bus conflicts with other peripherals, reads should only be performed at the 10xh port addresses while in setup mode. To eliminate potential compatibility problems in widely varying PC systems, the 64300 / 301 decodes the Global Setup register at I/O port 102h only.

GENERAL CONTROL REGISTERS

Two Input Status Registers read the SENSE pin (or Virtual Switch Register or internal comparator output), pending CRT interrupt, display enable / horizontal sync output, and vertical retrace / video output. The Feature Control Register selects the vertical sync function while the Miscellaneous Output Register controls I/O address select, clock selection, access to video memory, memory page, and horizontal and vertical sync polarity.

SEQUENCER REGISTERS

The Sequencer Index Register contains a 3-bit index to the Sequencer Data Registers. The Reset Register forces an asynchronous or synchronous reset of the sequencer. The Sequencer Clocking Mode Register controls master clocking functions, video enable/disable and selects either an 8 or 9 dot character clock. A Plane/Map Mask Register enables the color plane and write protect. The Character Font Select Register handles video intensity and character generation and controls the display memory plane through the character generator select. The Sequencer Memory Mode Register handles all memory, giving access by the CPU to 4 / 16 / 32 KBytes, Odd / Even addresses (planes) and writing of data to display memory.

CRT CONTROLLER REGISTERS

The CRT Controller Index Register contains a 6-bit index to the CRT Controller Registers. Twenty eight registers perform all display functions for modes: horizontal and vertical blanking and sync, panning and scrolling, cursor size and location, light pen, and underline.

GRAPHICS CONTROLLER REGISTERS

The Graphics Controller Index Register contains a 4-bit index to the Graphics Controller Registers. The Set/Reset Register controls the format of the CPU data to display memory. It also works with the Enable Set/Reset Register. Reducing 32 bits of display data to 8 bits of CPU data is accomplished by the Color Compare Register. Data Rotate Registers specify the CPU data bits to be rotated and subjected to logical operations. The Read Map Select Register reduces memory data for the CPU in the four plane (16 color) graphics mode. The Graphics Mode Register controls the write, read, and shift register modes. The Miscellaneous Register handles graphics/text, chaining of odd/even planes, and display memory mapping. Additional registers include Color Don't Care and Bit Mask.

ATTRIBUTE CONTROLLER AND COLOR PALETTE REGISTERS

The Attribute Controller Index Register contains a 5-bit index to the Attribute Controller Registers. A 6th bit is used to enable the video. The Attribute Controller Registers handle internal color lookup table mapping, text/graphics mode, overscan color, and color plane enable. The horizontal Pixel Panning and Pixel Padding Registers control pixel attributes on screen.

Color palette registers handle CPU reads and writes to I/O address range x3C6h-x3C9h. Inmos IMSG176 (Brooktree BT471/476) compatible registers are documented in this manual.

EXTENSION REGISTERS

The 64300 / 301 defines a set of extension registers which are addressed with the 7-bit Extension Register Index. The I/O port address is fixed at 3D6-3D7h and read/write access is always enabled to improve software performance.

The extension registers handle a variety of interfacing, compatibility, and display functions as discussed below. They are grouped into the following logical groups for discussion purposes:

1. Miscellaneous Registers include the Version number, Dip Switch, CPU interface, paging control, memory mode control, and diagnostic functions.
2. General Purpose Registers handle video blanking and the video default color.
3. Memory Control Registers control the type, amount, and configuration of the memory subsystem.
4. VideoOverlay Registers control the color keying and overlay of live video information on the graphics background.
5. Clock Registers set the frequencies for both the pixel and memory clocks.

The 64300 / 301 also has a group of 32-bit doubleword extension registers (DRXX) which may be mapped anywhere in I/O space. Typically these registers are located at x3D0-x3D3h. These registers are used for control of the high-performance BitBlt and Hardware Cursor subsystems.

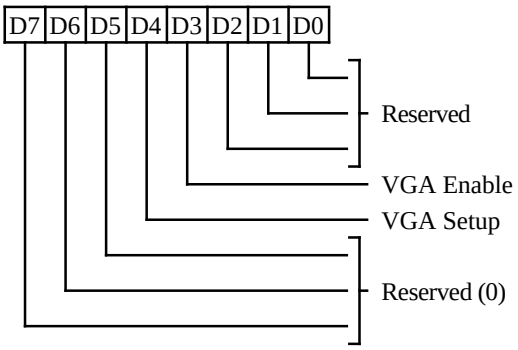
Note: The state of most of the Standard VGA Registers is undefined at reset. All registers specific to the 64300 / 301 (Extension Registers) are summarized in the Extension Register Table.

Global Control (Setup) Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SETUP	Setup Control	–	W	46E8h	–	45
ENAB	Global Enable	–	R/W	102h (Setup mode only)	–	45

SETUP CONTROL REGISTER (SETUP)

Write only at I/O Address 46E8h



This register is accessable in all bus configurations. It is also ignored if XR70 bit-7 is set to 1 (the default is 0).

This register is cleared by RESET.

2-0 Reserved

These bits are ignored and always read back 0. (BIOS may write non-zero values to these bits because they are implemented on 8514/a compatible display adapters to select which page of the ROM is mapped by the display adapter).

3 VGA Enable

0 VGA is disabled
1 VGA is enabled

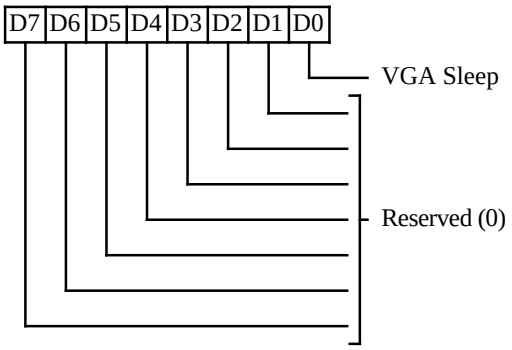
4 Setup Mode

0 VGA is in Normal Mode
1 VGA is in Setup Mode

7-5 Reserved (0)

GLOBAL ENABLE REGISTER (ENAB)

Read/Write at I/O Address 102h



This register is only accessible in Setup Mode (enabled by register 46E8h).

Bit-0 of this register is cleared by RESET.

0 VGA Sleep

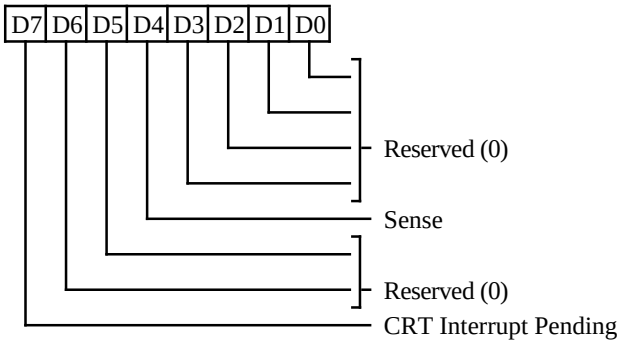
0 VGA is disabled
1 VGA is enabled

7-1 Reserved (0)

General Control & Status Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ST00	Input Status 0	–	R	3C2h	–	47
ST01	Input Status 1	–	R	3BAh/3DAh	–	47
FCR	Feature Control	–	W	3BAh/3DAh	5	48
			R	3CAh		
MSR	Miscellaneous Output	–	W	3C2h	5	48
			R	3CCh		

INPUT STATUS REGISTER 0 (ST00)
Read only at I/O Address at 3C2h



3-0 Reserved (0)

4 Sense

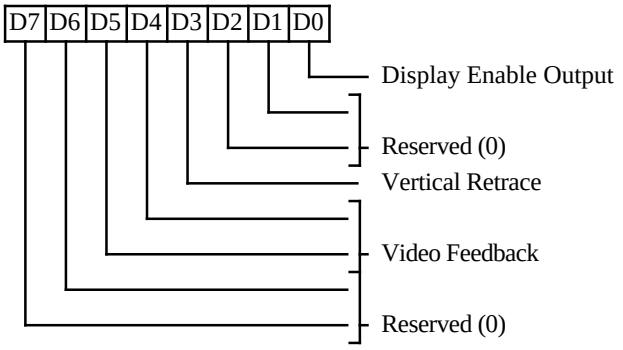
This bit returns the Status of the internal SENSE comparator or the output of an external comparator input on GPIO5 if enabled by XR06[0] and XR71[5].

6-5 Reserved (0)

7 CRT Interrupt Pending

0 Indicates no CRT interrupt is pending
1 Indicates a CRT interrupt is waiting to be serviced

INPUT STATUS REGISTER 1 (ST01)
Read only at I/O Address 3BAh/3DAh



0 Display Enable Output

This bit reflects the state of the vertical retrace AND horizontal retrace.

0 Indicates Display Enable inactive
1 Indicates Display Enable active

2-1 Reserved (0)

3 Vertical Retrace

The functionality of this bit is controlled by the Emulation Mode register (XR14[5]).

0 Indicates VSYNC inactive
1 Indicates VSYNC active

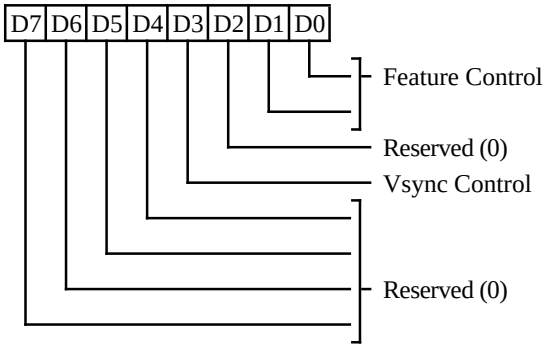
5-4 Video Feedback 1, 0

These are diagnostic video bits which are selected via the Color Plane Enable Register.

7-6 Reserved (0)

FEATURE CONTROL REGISTER (FCR)

Write at I/O Address 3BAh/3DAh
Read at I/O Address 3CAh
Group 5 Protection



1-0 Feature Control

These bits are read/write only and perform no function in the 64300 / 301. In the IBM VGA they control two external pins.

2 Reserved (0)

3 Vsync Control

This bit is cleared by RESET.

0 VSync output on the VSYNC pin
1 Logical 'OR' of VSync and Vertical Display Enable output on the VSYNC pin

This capability is not typically very useful, but is provided for IBM compatibility.

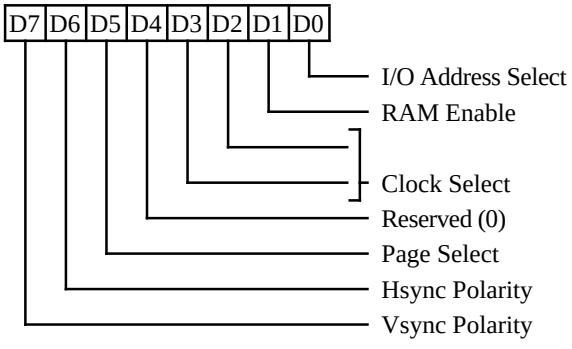
7-4 Reserved (0)

CRT Display Sync Polarities

V	H	Display	H Freq	V Freq
P	P	>480 Line	Variable	Variable
P	P	200 Line	15.7 KHz	60 Hz
N	P	350 Line	21.8 KHz	60 Hz
P	N	400 Line	31.5 KHz	70 Hz
N	N	480 Line	31.5 KHz	60 Hz

MISCELLANEOUS OUTPUT REGISTER (MSR)

Write at I/O Address 3C2h
Read at I/O Address 3CCh
Group 5 Protection



This register is cleared by RESET.

0 I/O Address Select. This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01).

0 Select 3Bxh I/O address
1 Select 3Dxh I/O address

1 RAM Enable

0 Prevent CPU access to display memory
1 Allow CPU access to display memory

3-2 Clock Select. These bits usually select the dot clock source for the CRT interface:

MSR3:2 = 00 = Select CLK0
MSR3:2 = 01 = Select CLK1
MSR3:2 = 10 = Select CLK2
MSR3:2 = 11 = Select CLK3

See extension register XR01[4] (Internal/External Clock) and Internal Clock Functional Description for variations of the above clock selection mapping.

4 Reserved (0)

5 Page Select. In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64 KByte page in display memory for CPU access: 0=select upper page; 1=select lower page.

6 CRT Hsync Polarity. 0=pos, 1=neg
7 CRT Vsync Polarity. 0=pos, 1=neg

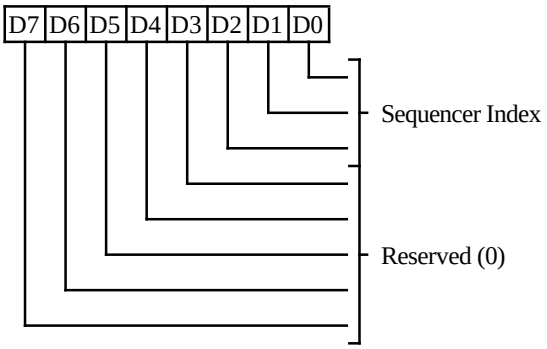
(Blank pin polarity can be controlled via the Video Interface Register, XR28).

Sequencer Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SRX	Sequencer Index	–	R/W	3C4h	1	49
SR00	Reset	00h	R/W	3C5h	1	49
SR01	Clocking Mode	01h	R/W	3C5h	1	50
SR02	Plane/Map Mask	02h	R/W	3C5h	1	50
SR03	Character Font	03h	R/W	3C5h	1	51
SR04	Memory Mode	04h	R/W	3C5h	1	52
SR07	Horizontal Character Counter Reset	07h	W	3C5h	–	52

SEQUENCER INDEX REGISTER (SRX)

Read/Write at I/O Address 3C4h



This register is cleared by reset.

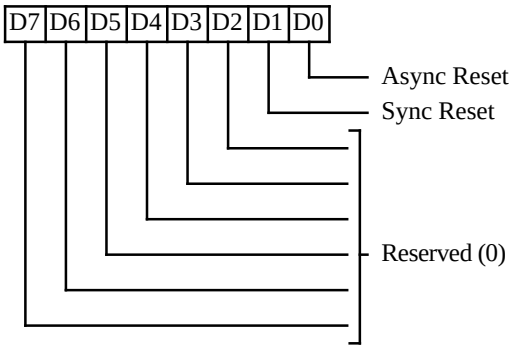
2-0 Sequencer Index

These bits contain a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7.

7-3 Reserved (0)

SEQUENCER RESET REGISTER (SR00)

Read/Write at I/O Address 3C5h
Index 00h
Group 1 Protection



0 Asynchronous Reset

0 Force asynchronous reset
1 Normal operation

Display memory data will be corrupted if this bit is set to zero.

1 Synchronous Reset

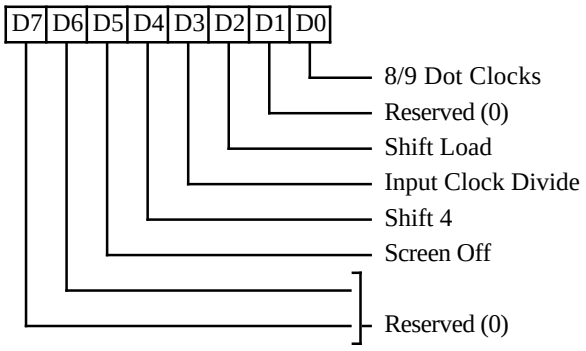
0 Force synchronous reset
1 Normal operation

Display memory data is not corrupted if this bit is set to zero for a short period of time (a few tens of microseconds).

7-2 Reserved (0)

SEQUENCER CLOCKING MODE REGISTER (SR01)

Read/Write at I/O Address 3C5h
Index 01h
Group 1 Protection



0 8/9 Dot Clocks

This bit determines whether a character clock is 8 or 9 dot clocks long.

0 Select 9 dots/character clock
1 Select 8 dots/character clock

1 Reserved (0)

2 Shift Load

0 Load video data shift registers every character clock
1 Load video data shift registers every other character clock

SR01[4] must be 0 for this bit to be effective.

3 Input Clock Divide

0 Sequencer master clock output on the PCLK pin (used for 640 (720) pixel modes)
1 Master clock divided by 2 output on the PCLK pin (used for 320 (360) pixel modes)

4 Shift 4

0 Load video shift registers every 1 or 2 character clocks (see SR01[2])
1 Load shift registers every 4th character clock.

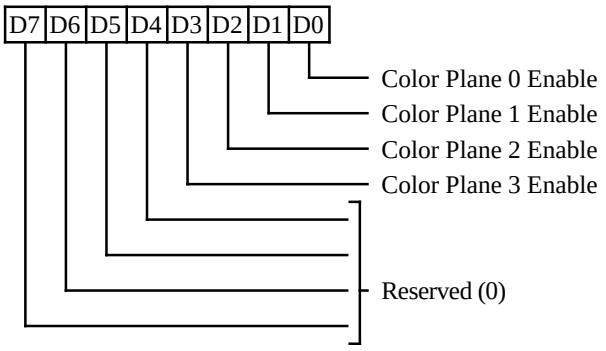
5 Screen Off

0 Normal Operation
1 Disable video output and assign all display memory bandwidth for CPU accesses

7-6 Reserved (0)

SEQUENCER PLANE/MAP MASK REGISTER (SR02)

Read/Write at I/O Address 3C5h
Index 02h
Group 1 Protection



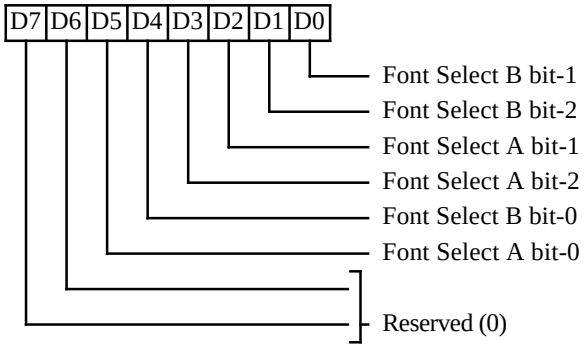
3-0 Color Plane Enable 3:0

0 Write protect corresponding color plane
1 Allow write to corresponding color plane

In Odd/Even and Quad modes, these bits still control access to the corresponding color plane [3:0].

7-4 Reserved (0)

CHARACTER FONT SELECT REGISTER (SR03)
Read/Write at I/O Address 3C5h
Index 03h
Group 1 Protection



In text modes, bit-3 of the video data's attribute byte normally controls the foreground intensity. This bit may be redefined to control switching between character sets. This latter function is enabled whenever there is a difference in the values of the Character Font Select A and the Character Font Select B bits. If the two values are the same, the character select function is disabled and attribute bit-3 controls the foreground intensity.

SR04[1] must be 1 for the character font select function to be active. Otherwise, only character fonts 0 and 4 are available.

1-0 High order bits of Character Generator Select B

3-2 High order bits of Character Generator Select A

4 Low order bit of Character Generator Select B

5 Low order bit of Character Generator Select A

7-6 Reserved (0)

The following table shows the display memory plane selected by the Character Generator Select A and B bits.

Code	Character Generator Table Location
0	First 8K of Plane 2
1	Second 8K of Plane 2
2	Third 8K of Plane 2
3	Fourth 8K of Plane 2
4	Fifth 8K of Plane 2
5	Sixth 8K of Plane 2
6	Seventh 8K of Plane 2
7	Eighth 8K of Plane 2

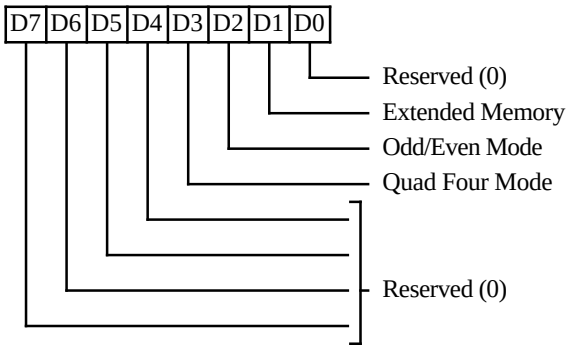
where 'code' is:

Character Generator Select A (bits 3, 2, 5) when bit-3 of the the attribute byte is one.

Character Generator Select B (bits 1, 0, 4) when bit-3 of the attribute byte is zero.

SEQUENCER MEMORY MODE REGISTER (SR04)

Read/Write at I/O Address 3C5h
Index 04h
Group 1 Protection



0 Reserved (0)

1 Extended Memory

0 Restrict CPU access to 4/16/32 KBytes
1 Allow complete access to memory

This bit should normally be 1.

2 Odd/Even Mode

0 CPU accesses to Odd/Even addresses are directed to corresponding odd/even planes
1 All planes are accessed simultaneously (IRGB color)

SR04[3] must be 0 for this bit to be effective. This bit affects only CPU write accesses to display memory.

3 Quad Four Mode

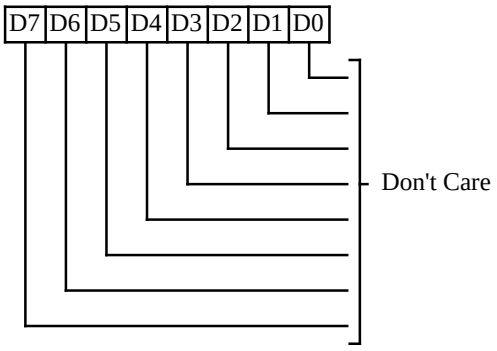
0 CPU addresses are mapped to display memory as defined by SR04[2]
1 CPU addresses are mapped to display memory modulo 4. The two low order CPU address bits select the display memory plane.

This bit affects both CPU reads and writes to display memory.

7-4 Reserved (0)

SEQUENCER HORIZONTAL CHARACTER COUNTER RESET (SR07)

Read/Write at I/O Address 3C5h
Index 07h



Writing to SR07 with any data will cause the horizontal character counter to be held reset (character counter output = 0) until a write to any other sequencer register with any data value. The write to any index in the range 0-6 clears the latch that is holding the reset condition on the character counter.

The vertical line counter is clocked by a signal derived from horizontal display enable (which does not occur if the horizontal counter is held reset). Therefore, if the write to SR07 occurs during vertical retrace, the horizontal counter will be set to zero and the vertical counter will not advance. A write to any other sequencer register may then be used to start both counters with reasonable synchronization to an external event via software control.

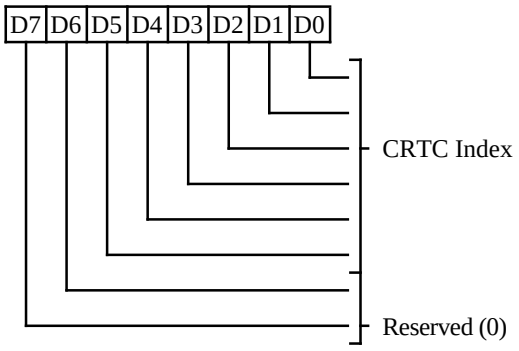
This is a standard VGA register which was not documented by IBM.

CRT Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
CRX	CRTC Index	–	R/W	3B4h/3D4h	–	54
CR00	Horizontal Total	00h	R/W	3B5h/3D5h	0	54
CR01	Horizontal Display Enable End	01h	R/W	3B5h/3D5h	0	54
CR02	Horizontal Blank Start	02h	R/W	3B5h/3D5h	0	55
CR03	Horizontal Blank End	03h	R/W	3B5h/3D5h	0	55
CR04	Horizontal Sync Start	04h	R/W	3B5h/3D5h	0	56
CR05	Horizontal Sync End	05h	R/W	3B5h/3D5h	0	56
CR06	Vertical Total	06h	R/W	3B5h/3D5h	0	57
CR07	Overflow	07h	R/W	3B5h/3D5h	0/3	57
CR08	Preset Row Scan	08h	R/W	3B5h/3D5h	3	58
CR09	Maximum Scan Line	09h	R/W	3B5h/3D5h	2/4	58
CR0A	Cursor Start Scan Line	0Ah	R/W	3B5h/3D5h	2	59
CR0B	Cursor End Scan Line	0Bh	R/W	3B5h/3D5h	2	59
CR0C	Start Address High	0Ch	R/W	3B5h/3D5h	–	60
CR0D	Start Address Low	0Dh	R/W	3B5h/3D5h	–	60
CR0E	Cursor Location High	0Eh	R/W	3B5h/3D5h	–	60
CR0F	Cursor Location Low	0Fh	R/W	3B5h/3D5h	–	60
CR10	Vertical Sync Start (See Note 1)	10h	W or R/W	3B5h/3D5h	4	61
CR11	Vertical Sync End (See Note 1)	11h	W or R/W	3B5h/3D5h	3/4	61
CR10	Lightpen High (See Note 1)	10h	R	3B5h/3D5h	–	61
CR11	Lightpen Low (See Note 1)	11h	R	3B5h/3D5h	–	61
CR12	Vertical Display Enable End	12h	R/W	3B5h/3D5h	4	62
CR13	Offset	13h	R/W	3B5h/3D5h	3	62
CR14	Underline Row	14h	R/W	3B5h/3D5h	3	63
CR15	Vertical Blank Start	15h	R/W	3B5h/3D5h	4	64
CR16	Vertical Blank End	16h	R/W	3B5h/3D5h	4	64
CR17	CRT Mode Control	17h	R/W	3B5h/3D5h	3/4	65
CR18	Line Compare	18h	R/W	3B5h/3D5h	3	66
CR22	Memory Data Latches	22h	R	3B5h/3D5h	–	67
CR24	Attribute Controller Toggle	24h	R	3B5h/3D5h	–	67

Note 1: In the VGA, the light pen registers (CR10 and CR11) are at index locations conflicting with the vertical sync registers. This would normally prevent reads and writes from occurring at the same index. Since the light pen registers are not normally useful, the VGA provides software control (CR03 bit-7) of whether the vertical sync or light pen registers are readable at indices 10-11.

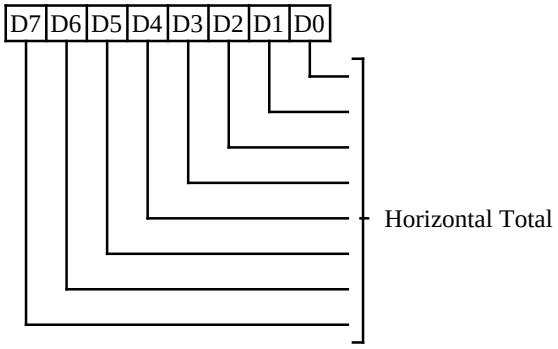
CRTC INDEX REGISTER (CRX)
Read/Write at I/O Address 3B4h/3D4h



5-0 CRTC data register index

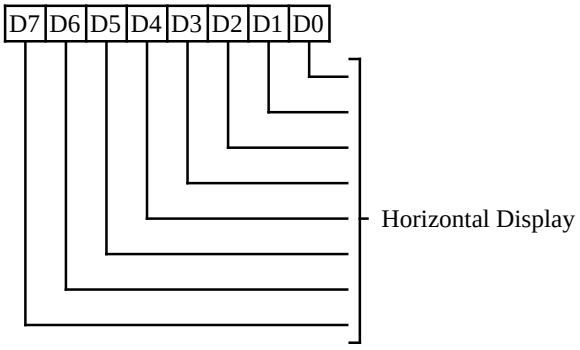
7-6 Reserved (0)

HORIZONTAL TOTAL REGISTER (CR00)
Read/Write at I/O Address 3B5h/3D5h
Index 00h
Group 0 Protection



7-0 Horizontal Total. Total number of character clocks per line = contents of this register + 5. This register determines the horizontal sweep rate.

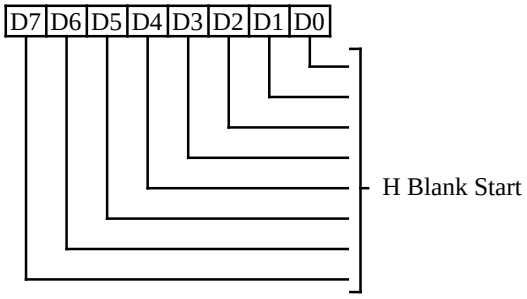
HORIZONTAL DISPLAY ENABLE END REGISTER (CR01)
Read/Write at I/O Address 3B5h/3D5h
Index 01h
Group 0 Protection



7-0 Number of Characters displayed per scan line – 1.

HORIZONTAL BLANK START REGISTER (CR02)

Read/Write at I/O Address 3B5h/3D5h
Index 02h
Group 0 Protection

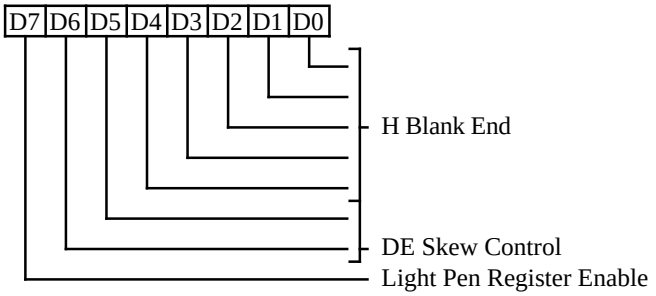


7-0 Horizontal Blank Start

These bits specify the beginning of horizontal blank in terms of character clocks from the beginning of the display scan. The period between Horizontal Display Enable End and Horizontal Blank Start is the right side border on screen.

HORIZONTAL BLANK END REGISTER (CR03)

Read/Write at I/O Address 3B5h/3D5h
Index 03h
Group 0 Protection



4-0 Horizontal Blank End

These are the lower 5 bits of the character clock count used to define the end of horizontal blank. The interval between the end of horizontal blank and the beginning of the display (a count of 0) is the left side border on the screen. If the horizontal blank width desired is W clocks, the 5-bit value programmed in this register = [contents of CR02 + W] AND 1Fh. The 6th bit is programmed in CR05[7]. This bit = [(CR02 + W) AND 20h]/20h. The most significant bit is programmed in XR17[5]. This bit = [(CR02 + W) AND 40h]/40h. The most significant bit is not VGA-compatible and is only enabled in extended high resolution modes. For standard modes only the standard 6 bits are programmed. The 7th bit is enabled by XR17[6].

6-5 Display Enable Skew Control

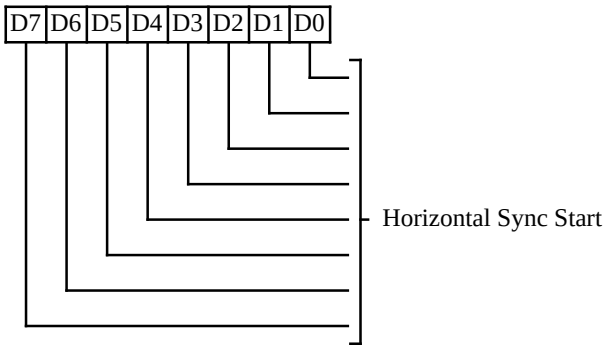
Defines the number of character clocks that the Display Enable signal is delayed to compensate for internal pipeline delays.

7 Light Pen Register Enable

This bit must be 1 for normal operation; when this bit is 0, CRTC registers CR10 and CR11 function as lightpen readback registers.

HORIZONTAL SYNC START REGISTER (CR04)

Read/Write at I/O Address 3B5h/3D5h
Index 04h
Group 0 Protection



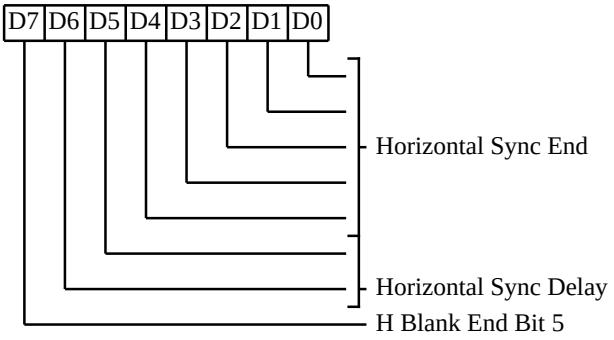
7-0 Horizontal Sync Start

These bits specify the beginning of Hsync in terms of Character clocks from the beginning of the display scan. These bits also determine display centering on the screen.

A 9th bit is available in XR17[2] for non-VGA high resolution modes. For VGA compatibility its default value is zero and is not expected to be programmed by VGA software.

HORIZONTAL SYNC END REGISTER (CR05)

Read/Write at I/O Address 3B5h/3D5h
Index 05h
Group 0 Protection



4-0 Horizontal Sync End

Lower 5 bits of the character clock count which specifies the end of Horizontal Sync. If the horizontal sync width desired is N clocks, then these bits = (N + contents of CR04) AND 1Fh.

A 6th bit, enabled by XR17[6], is available at XR17[3]. This is only used for non-VGA compatible high resolution modes. It is programmed = (N + contents of CR04/XR1A) AND 20h/20h.

6-5 Horizontal Sync Delay

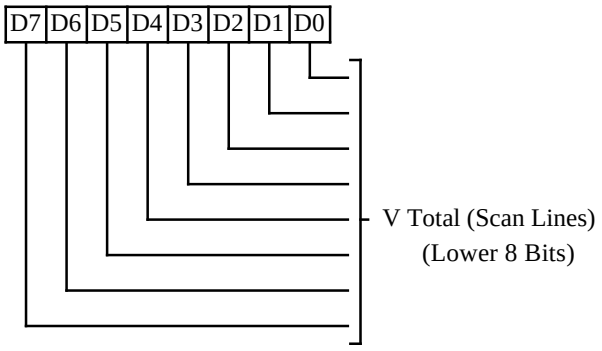
These bits specify the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.

7 Horizontal Blank End Bit 5

This bit is the sixth bit of the Horizontal Blank End Register (CR03).

VERTICAL TOTAL REGISTER (CR06)

Read/Write at I/O Address 3B5h/3D5h
Index 06h
Group 0 Protection



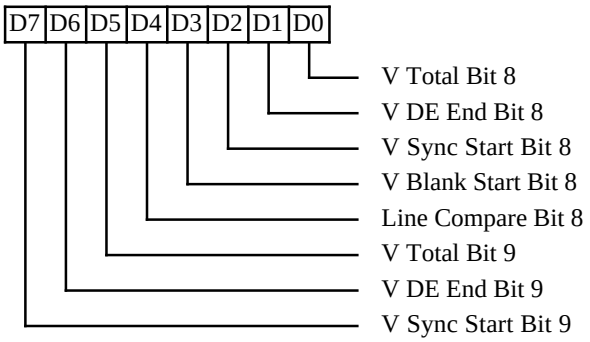
7-0 Vertical Total

These are the 8 low order bits of a 10/11-bit register. The VGA-compatible 9th and 10th bits are located in the CRT Controller Overflow Register. The 11th bit (XR16[0]) is only used in non-VGA compatible high resolution modes. In VGA modes XR16[0] is not programmed - it is assumed to be 0. The Vertical Total value specifies the total number of scan lines (horizontal retrace periods) per frame.

Programmed Count = Actual Count – 2

OVERFLOW REGISTER (CR07)

Read/Write at I/O Address 3B5h/3D5h
Index 07h
Group 0 Protection on bits 0-3 and bits 5-7
Group 3 Protection on bit 4



0 Vertical Total Bit 8

1 Vertical Display Enable End Bit 8

2 Vertical Sync Start Bit 8

3 Vertical Blank Start Bit 8

4 Line Compare Bit 8

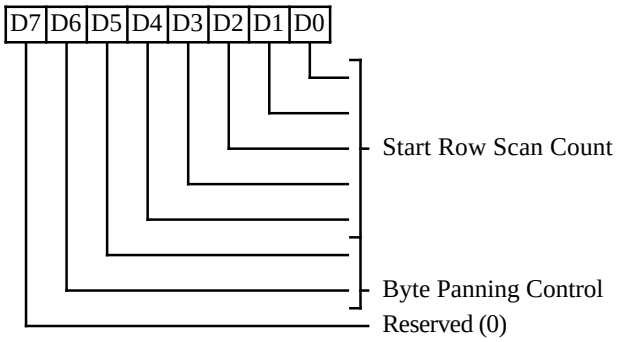
5 Vertical Total Bit 9

6 Vertical Display Enable End Bit 9

7 Vertical Sync Start Bit 9

PRESET ROW SCAN REGISTER (CR08)

Read/Write at I/O Address 3B5h/3D5h
Index 08h
Group 3 Protection



4-0 Start Row Scan Count

These bits specify the starting row scan count after each vertical retrace. Every horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count during active display. This register is used for soft scrolling in text modes.

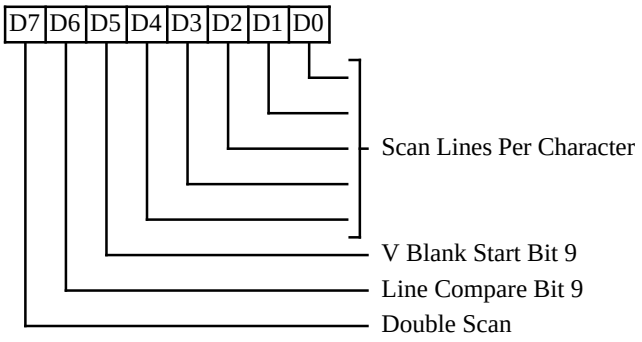
6-5 Byte Panning Control

These bits specify the lower order bits for the display start address. They are used for horizontal panning in Odd/Even and Quad modes.

7 Reserved (0)

MAXIMUM SCAN LINE REGISTER (CR09)

Read/Write at I/O Address 3B5h/3D5h
Index 09h
Group 2 Protection on bits 0-4
Group 4 Protection on bits 5-7



4-0 Scan Lines Per Character

These bits specify the number of scan lines in a row:

Programmed Value = Actual Value – 1

5 Vertical Blank Start Register Bit 9

Overflow bit from CR15

6 Line Compare Register Bit 9

Overflow bit from CR18

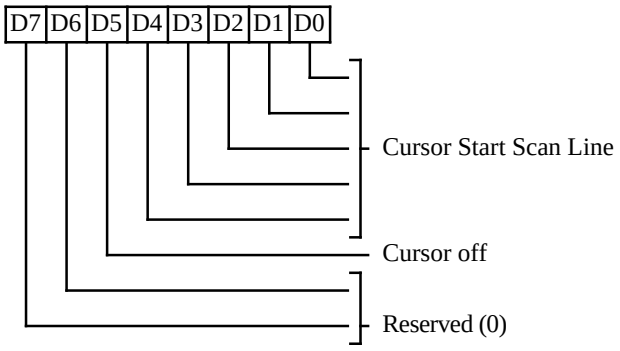
7 Double Scan

0 Normal Operation
1 Enable scan line doubling

The vertical parameters in the CRT Controller (even for a split screen) are not affected, only the CRTC row scan counter (bits 0-4 of this register) and display memory addressing screen refresh are affected.

CURSOR START SCAN LINE REGISTER (CR0A)

Read/Write at I/O Address 3B5h/3D5h
Index 0Ah
Group 2 Protection



4-0 Cursor Start Scan Line

These bits specify the scan line of the character cell where the cursor display begins (top scan line = 0).

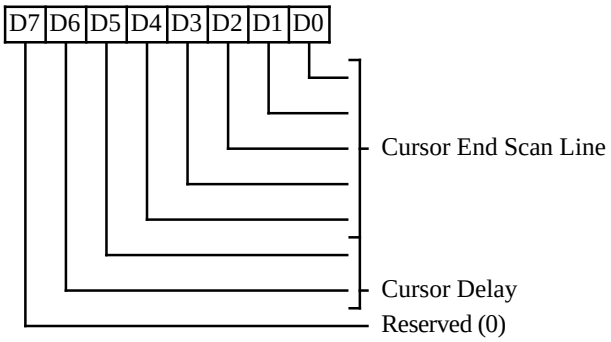
5 Cursor Off

0 Text Cursor On
1 Text Cursor Off

7-6 Reserved (0)

CURSOR END SCAN LINE REGISTER (CR0B)

Read/Write at I/O Address 3B5h/3D5h
Index 0Bh
Group 2 Protection



4-0 Cursor End Scan Line

These bits specify the scan line of a character row where the cursor display ends (i.e., last scan line for the block cursor).

6-5 Cursor Delay

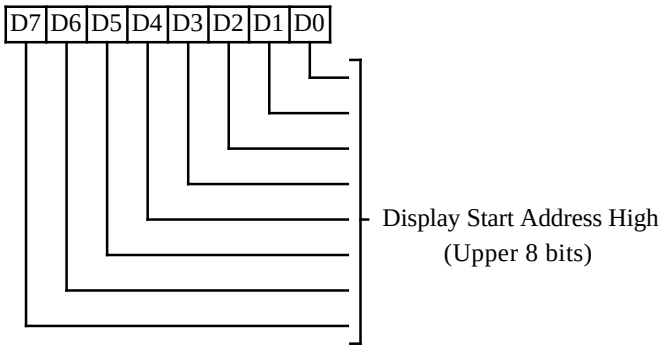
These bits define the number of character clocks that the cursor is delayed to compensate for internal pipeline delay.

7 Reserved (0)

Note: If the Cursor Start Line is greater than the Cursor End Line, then no cursor is generated. If the cursor end scan line is programmed to be greater than the number of scan lines per charater cell, then the last cursor line is the last line of the character cell.

START ADDRESS HIGH REGISTER (CR0C)

Read/Write at I/O Address 3B5h/3D5h
Index 0Ch

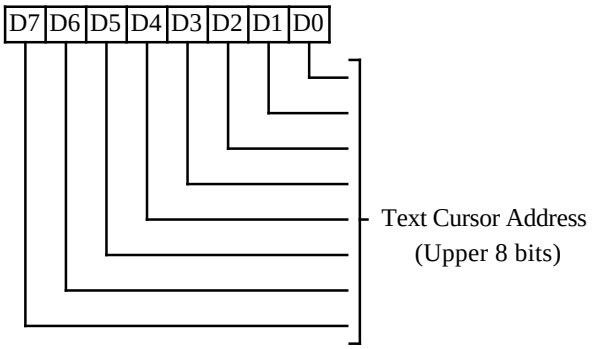


7-0 Display Start Address High (Bits 15:8)

This register contains the upper 8 bits of the display start address.

CURSOR LOCATION HIGH REGISTER (CR0E)

Read/Write at I/O Address 3B5h/3D5h
Index 0Eh

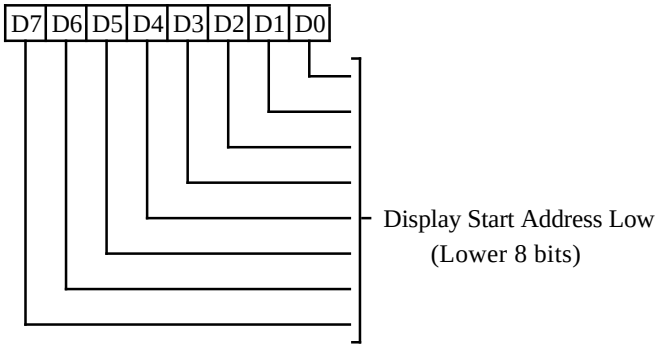


7-0 Cursor Location High (Bits 15:8)

This register contains the upper 8 bits of the memory address where the text cursor is active.

START ADDRESS LOW REGISTER (CR0D)

Read/Write at I/O Address 3B5h/3D5h
Index 0Dh

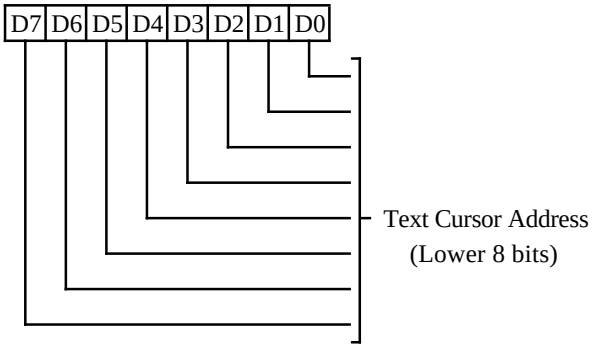


7-0 Display Start Address Low (Bits 7:0)

This register contains the lower 8 bits of the display start address. The display start address points to the memory address corresponding to the top left corner of the screen.

CURSOR LOCATION LOW REGISTER (CR0F)

Read/Write at I/O Address 3B5h/3D5h
Index 0Fh



7-0 Cursor Location Low (Bits 7:0)

This register contains the lower 8 bits of the memory address where the text cursor is active.

LIGHTPEN HIGH REGISTER (CR10)

Read only at I/O Address 3B5h/3D5h
Index 10h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only when CR03 bit-7 = 0.

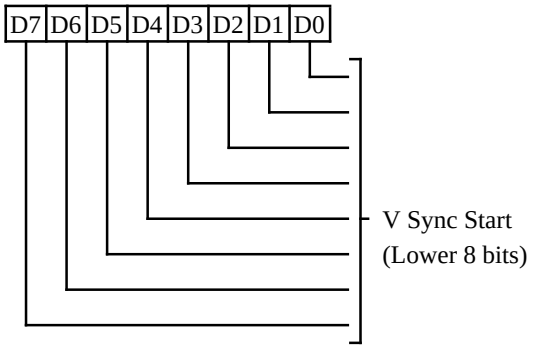
LIGHTPEN LOW REGISTER (CR11)

Read only at I/O Address 3B5h/3D5h
Index 11h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only when CR03 bit-7 = 0.

VERTICAL SYNC START REGISTER (CR10)

Read/Write at I/O Address 3B5h/3D5h
Index 10h
Group 4 Protection



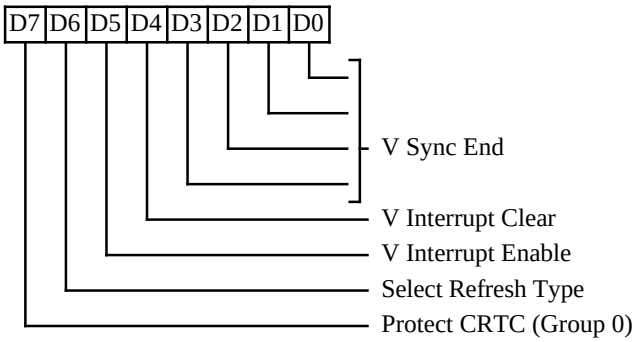
This register is not readable when CR03 bit-7=1.

7-0 Vertical Sync Start

The eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRTC Overflow Register. They define the scan line position at which Vertical Sync becomes active. There is an 11th bit located in XR16[2] used for non-VGA modes.

VERTICAL SYNC END REGISTER (CR11)

Read/Write at I/O Address 3B5h/3D5h
Index 11h
Group 3 Protection for bits 4 and 5
Group 4 Protection for bits 0-3, 6, and 7



This register is not readable when CR03 bit-7=1.

3-0 Vertical Sync End

The lower 4 bits of the scan line count that defines the end of vertical sync. If the vertical sync width desired is N lines, then bits 3-0 of this register = (CR10 + N) AND 0Fh.

4 Vertical Interrupt Clear

0=Clear vertical interrupt generated on the IRQ output; 1=Normal operation. This bit is cleared by RESET.

5 Vertical Interrupt Enable

0 Enable vertical interrupt (default)
1 Disable vertical interrupt

This bit is cleared by RESET.

6 Select Refresh Type

0 3 refresh cycles per scan line
1 5 refresh cycles per scan line

7 Group Protect 0

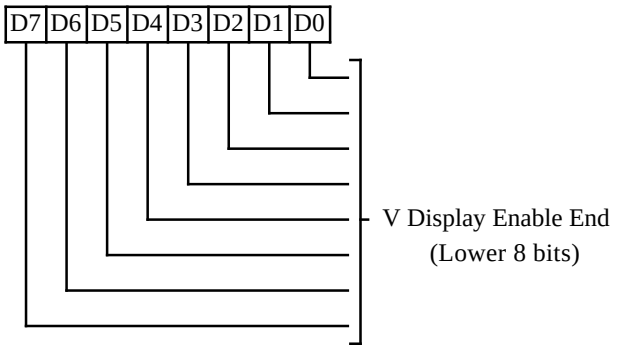
This bit is logically ORed with XR15 bit-6 to determine the protection for group 0 registers. This bit is cleared by RESET.

0 Enable writes to CR00-CR07
1 Disable writes to CR00-CR07

CR07 bit-4 (Line Compare bit-9) is not affected by this bit.

VERTICAL DISPLAY ENABLE END REGISTER (CR12)

Read/Write at I/O Address 3B5h/3D5h
Index 12h
Group 4 Protection

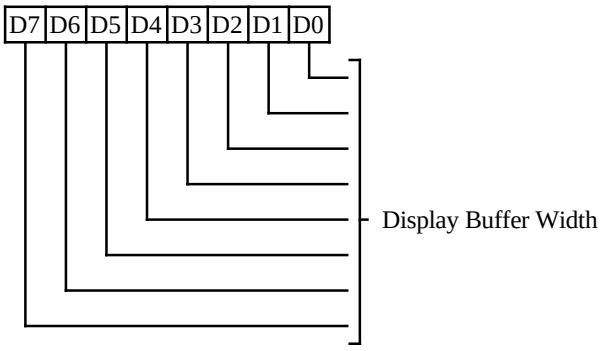


7-0 Vertical Display Enable End

These are the eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow register. The actual count = Contents of this register + 1. There is an 11th bit located in XR16[1] used for non-VGA modes.

OFFSET REGISTER (CR13)

Read/Write at I/O Address 3B5h/3D5h
Index 13h
Group 3 Protection

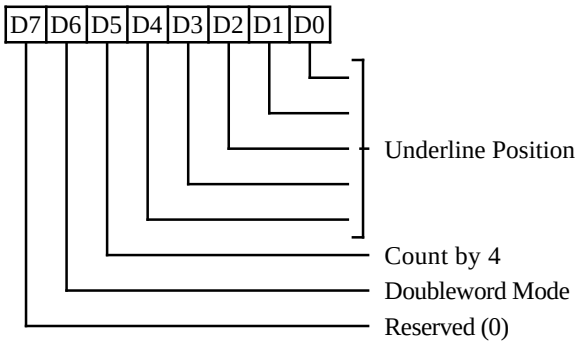


7-0 Display Buffer Width

The byte starting address of the next display row = Byte Start Address for current row + (K* CR13), where K = 2 in byte mode, K = 4 in word mode, and K = 8 in doubleword mode. Byte, word and doubleword modes are selected by CR17[6] and CR14[6]. Byte, word and doubleword modes affect the translation of the 'logical' display memory address to the 'physical' display memory address.

UNDERLINE LOCATION REGISTER (CR14)

Read/Write at I/O Address 3B5h/3D5h
Index 14h
Group 3 Protection



4-0 Underline Position

These bits specify the underline's scan line position within a character row.

Programmed Value = Actual scan line number – 1

5 Count by 4 for Doubleword Mode

0 Frame Buffer Address is incremented by 1 or 2
1 Frame Buffer Address is incremented by 4 or 2

See CR17 bit-3 for further details.

6 Doubleword Mode

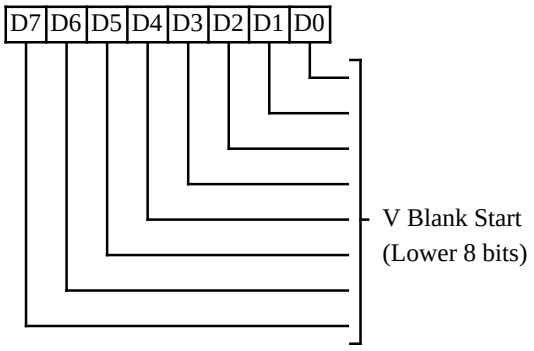
0 Frame Buffer Address is byte or word address
1 Frame Buffer Address is doubleword address

This bit is used in conjunction with CR17 bit-6 to select the display memory addressing mode.

7 Reserved (0)

VERTICAL BLANK START REGISTER (CR15)

Read/Write at I/O Address 3B5h/3D5h
Index 15h
Group 4 Protection

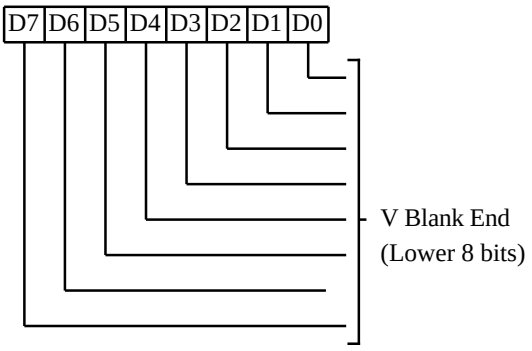


7-0 Vertical Blank Start

These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers respectively. Together these 10 bits define the scan line position where vertical blank begins. The interval between the end of the vertical display and the beginning of vertical blank is the bottom border on the screen.
There is an 11th bit located in XR16[4] used for non-VGA modes.

VERTICAL BLANK END REGISTER (CR16)

Read/Write at I/O Address 3B5h/3D5h
Index 16h
Group 4 Protection

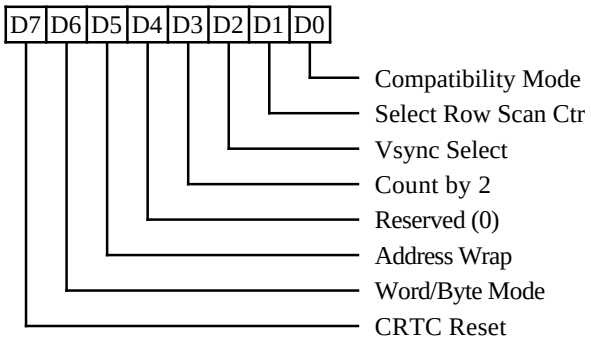


7-0 Vertical Blank End

These are the 8 low order bits of the scan line count which specifies the end of Vertical Blank. If the vertical blank width desired is Z lines these bits = (Vertical Blank Start + Z) and 0FFh.

CRT MODE CONTROL REGISTER (CR17)

Read/Write at I/O Address 3B5h/3D5h
Index 17h
Group 3 Protection for bits 0, 1, and 3-7
Group 4 Protection for bit 2



0 Compatibility Mode Support

This bit allows compatibility with the IBM CGA two-bank graphics mode.

0 Character row scan line counter bit 0 is substituted for memory address bit 13 during active display time
1 Normal operation, no substitution takes place

1 Select Row Scan Counter

This bit allows compatibility with Hercules graphics and with any other 4-bank graphics system.

0 Character row scan line counter bit 1 is substituted for memory address bit 14 during active display time
1 Normal operation, no substitution takes place

2 Vertical Sync Select

This bit controls the vertical resolution of the CRT Controller by permitting selection of the clock rate input to the vertical counters. When set to 1, the vertical counters are clocked by the horizontal retrace clock divided by 2.

3 Count By Two

0 Memory address counter is incremented every character clock (CCLK)
1 Memory address counter is incremented every two character clocks, used in conjunction with bit 5 of 0Fh.

Note: This bit is used in conjunction with CR14[5]. The net effect is as follows:

CR14[5]	CR17[3]	Increment Addressing Every
0	0	1 CCLK
0	1	2 CCLK
1	0	4 CCLK
1	1	2 CCLK

4 Reserved (0)

5 Address Wrap (effective only in word mode)

0 Wrap display memory address at 16 Kbytes. Used in IBM CGA mode.
1 Normal operation (extended mode).

6 Word Mode or Byte Mode

0 Select Word Mode. In this mode the display memory address counter bits are shifted down by one, causing the most-significant bit of the counter to appear on the least-significant bit of the display memory address output
1 Select byte mode

Note: This bit is used in conjunction with CR14[6] to select byte, word, or doubleword memory addressing as follows:

CR14[6]	CR17[6]	Addressing Mode
0	0	Word Mode
0	1	Byte Mode
1	0	Doubleword Mode
1	1	Doubleword Mode

Display memory addresses are affected as shown in the table on the following page.

7 Hardware Reset

0 Force HSYNC and VSYNC inactive. No other registers or outputs affected.(Default on RESET)
1 Normal Operation.

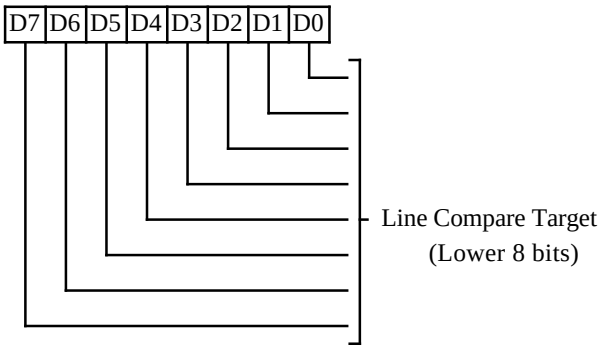
Display memory addresses are affected by CR17 bit 6 as shown in the table below:

Logical Memory Address	Physical Memory Address Byte Mode	Word Mode	Doubleword Mode
MA00	A00	Note 1	Note 2
MA01	A01	A00	Note 3
MA02	A02	A01	A00
MA03	A03	A02	A01
MA04	A04	A03	A02
MA05	A05	A04	A03
MA06	A06	A05	A04
MA07	A07	A06	A05
MA08	A08	A07	A06
MA09	A09	A08	A07
MA10	A10	A09	A08
MA11	A11	A10	A09
MA12	A12	A11	A10
MA13	A13	A12	A11
MA14	A14	A13	A12
MA15	A15	A14	A13

Note 1 = A13 * NOT CR17 bit 5
+ A15 * CR17 bit 5
Note 2 = A12 xor (A14 * XR04 bit 2)
Note 3 = A13 xor (A15 * XR04 bit 2)

LINE COMPARE REGISTER (CR18)

Read/Write at I/O Address 3B5h/3D5h
Index 18h
Group 3 Protection

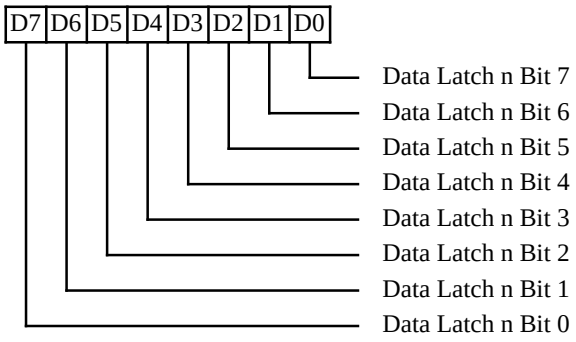


7-0 Line Compare Target

These are the low order 8 bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers, respectively. This register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address counter is cleared to 0. The display memory address counter then sequentially addresses the display memory starting at address 0. Each subsequent row address is generated by the addition of the Offset Register contents. This register is not affected by the double scanning bit (CR09[7]).

MEMORY DATA LATCH REGISTER (CR22)

Read only at I/O Address 3B5h/3D5h
Index 22h



7–0 Data Latch

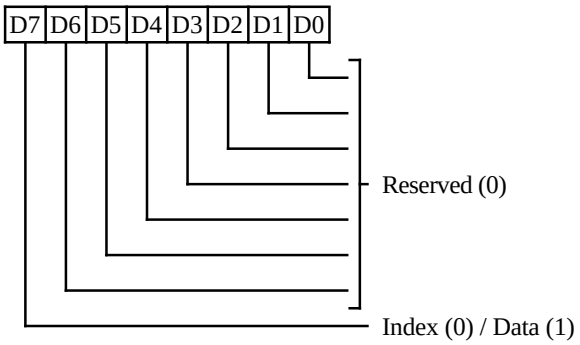
This register may be used to read the state of Graphics Controller Memory Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (GR04[1:0]) and is in the range 0–3.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

ATTRIBUTE CONTROLLER TOGGLE REGISTER (CR24)

Read only at I/O Address 3B5h/3D5h
Index 24h



6-0 Reserved (0)

7 Index/Data

This bit may be used to read back the state of the attribute controller index/data latch. This latch indicates whether the next write to the attribute controller at 3C0h will be to the register index pointer or to an indexed register.

0 Next write is to the index
1 Next write is to an indexed register

Writes to this register are not decoded and will be ignored.

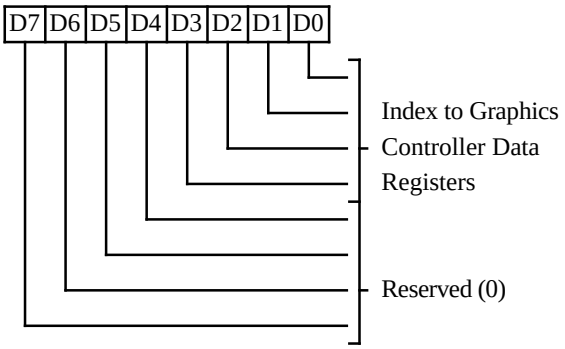
This is a standard VGA register which was not documented by IBM.

Graphics Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
GRX	Graphics Index	–	R/W	3CEh	1	69
GR00	Set/Reset	00h	R/W	3CFh	1	69
GR01	Enable Set/Reset	01h	R/W	3CFh	1	70
GR02	Color Compare	02h	R/W	3CFh	1	70
GR03	Data Rotate	03h	R/W	3CFh	1	71
GR04	Read Map Select	04h	R/W	3CFh	1	71
GR05	Graphics Mode	05h	R/W	3CFh	1	72
GR06	Miscellaneous	06h	R/W	3CFh	1	74
GR07	Color Don't Care	07h	R/W	3CFh	1	74
GR08	Bit Mask	08h	R/W	3CFh	1	75

GRAPHICS CONTROLLER INDEX REGISTER (GRX)

Write only at I/O Address 3CEh
Group 1 Protection

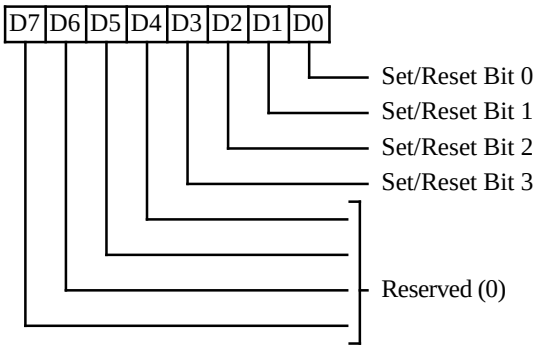


3-0 4-bit Index to Graphics Controller Registers

7-4 Reserved (0)

SET/RESET REGISTER (GR00)

Read/Write at I/O Address 3CFh
Index 00h
Group 1 Protection



The SET/RESET and ENABLE SET/RESET registers are used to 'expand' 8 bits of CPU data to 32 bits of display memory.

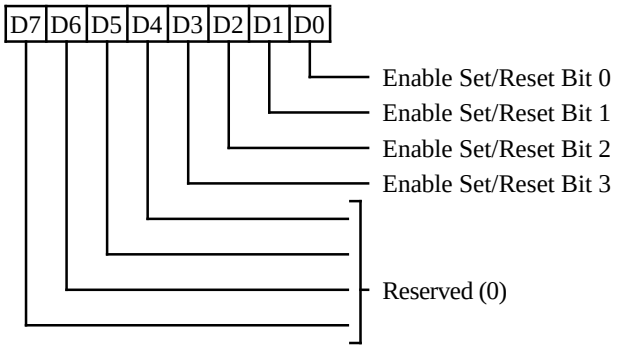
3-0 Set / Reset Planes 3-0

When the Graphics Mode register selects Write Mode 0, all 8 bits of each display memory plane are set as specified in the corresponding bit in this register. The Enable Set/Reset register (GR01) allows selection of some CPU data to be written to individual planes and other planes to be set or reset based on GR00. In Write Mode 3 (see GR05), these bits determine the color value.

7-4 Reserved (0)

ENABLE SET/RESET REGISTER (GR01)

Read/Write at I/O Address 3CFh
Index 01h
Group 1 Protection



3-0 Enable Set / Reset Planes 3-0

This register works in conjunction with the Set/Reset register (GR00). The Graphics Mode register must be programmed to Write Mode 0 in order for this register to have any effect.

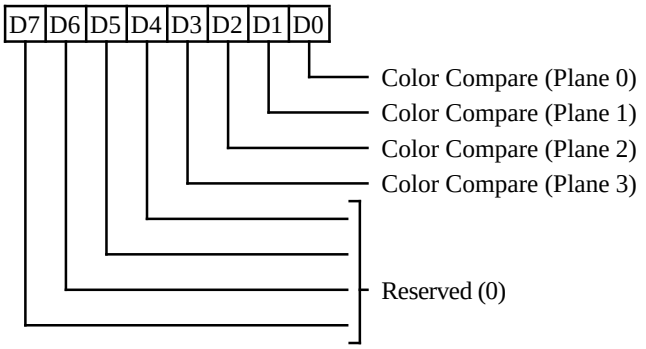
0 The corresponding plane is written with the data from the CPU data bus

1 The corresponding plane is set to 0 or 1 as specified in the Set/Reset Register

7-4 Reserved (0)

COLOR COMPARE REGISTER (GR02)

Read/Write at I/O Address 3CFh
Index 02h
Group 1 Protection



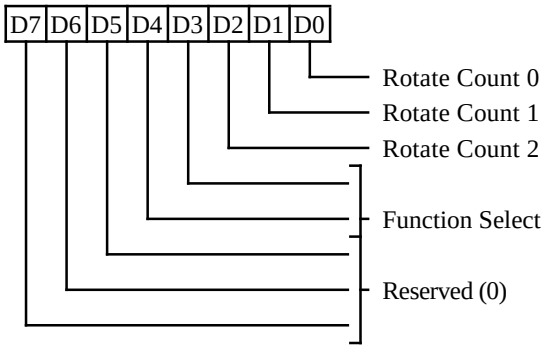
3-0 Color Compare Planes 3-0

This register is used to 'reduce' 32 bits of memory data to 8 bits for the CPU in 4-plane graphics mode. These bits provide a reference color value to be compared to data read from display memory planes 0-3. The Color Don't Care register (GR07) is used to affect the result. This register is active only if the Graphics Mode register (GR05) is set to Read Mode 1. A match between the memory data and the Color Compare register (GR02) (for the bits specified in the Color Don't Care register) causes a logical 1 to be placed on the CPU data bus for the corresponding data bit; a mis-match returns a logical 0.

7-4 Reserved (0)

DATA ROTATE REGISTER (GR03)

Read/Write at I/O Address 3CFh
Index 03h
Group 1 Protection



2-0 Data Rotate Count

These bits specify the number of bits to rotate to the right the data being written by the CPU. The CPU data bits are first rotated, then subjected to the logical operation as specified in the Function Select bit field. The rotate function is active only if the Graphics Mode register is programmed for Write Mode 0.

4-3 Function Select

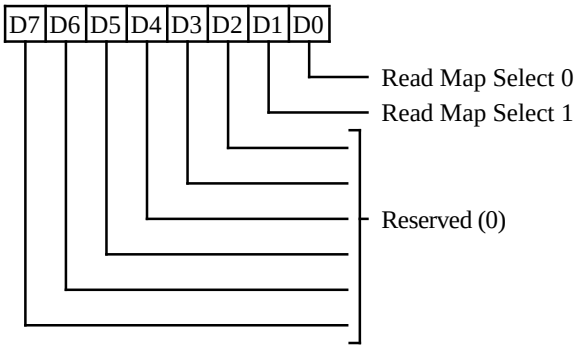
These Function Select bits specify the logical function performed on the contents of the processor latches (loaded on a previous CPU read cycle) before the data is written to display memory. These bits operate as follows:

Bit 4	Bit 3	Result
0	0	No change to the Data
0	1	Logical 'AND' between Data and latched data
1	0	Logical 'OR' between Data and latched data
1	1	Logical 'XOR' between Data and latched data

7-5 Reserved (0)

READ MAP SELECT REGISTER (GR04)

Read/Write at I/O Address 3CFh
Index 04h
Group 1 Protection



1-0 Read Map Select

This register is also used to 'reduce' 32 bits of memory data to 8 bits for the CPU in the 4-plane graphics mode. These bits select the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even mode, bit-0 is ignored. In Quad mode, bits 0 and 1 are both ignored.

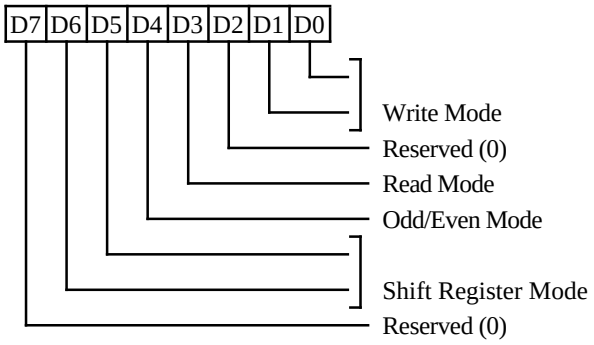
The four memory maps are selected as follows:

Bit 1	Bit 0	Map Selected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

7-2 Reserved (0)

GRAPHICS MODE REGISTER (GR05)

Read/Write at I/O Address 3CFh
Index 05h
Group 1 Protection



1-0 Write Mode

For 16/32-bit writes, the operation is repeated on all bytes of CPU data.

GR05[1:0]	Write Mode

00 **Write mode 0**. Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.

01 **Write mode 1**. Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.

10 **Write mode 2**. The CPU data bus data is treated as the color value for the addressed byte in planes 0-3. All eight pixels in the addressed byte are modified unless protected by the Bit Mask register setting. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset and Enable Set/Reset registers are ignored. The Function Select bits in the Data Rotate register are used.

11 **Write mode 3**. The CPU data is rotated then logically ANDed with the contents of the Bit Mask register (GR08) and then treated as the addressed data's bit mask, while the contents of the Set/Reset register is treated as the color value.

A '0' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the corresponding pixel in the processor latches.

A '1' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the color value specified in the Set/Reset register.

The Enable Set/Reset register is ignored. The Data Rotate is used. This write mode can be used to fill an area with a single color and pattern.

2 Reserved (0)

3 Read Mode

0 The CPU reads data from one of the planes as selected in the Read Map Select register.

1 The CPU reads the 8-bit result of the logical comparison between all eight pixels in the four display planes and the contents of the Color Compare and Color Don't Care registers. The CPU reads a logical 1 if a match occurs for each pixel and logical 0 if a mis-match occurs. In 16-bit read cycles, this operation is repeated on the lower and upper bytes.

(Continued on following page)

4 Odd/Even Mode

0 All CPU addresses sequentially access all planes

1 Even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for compatibility with the IBM CGA memory organization.

6-5 Shift Register Mode

These two bits select the data shift pattern used when passing data from the four memory planes through the four video shift registers. If data bits 0-7 in memory planes 0-3 are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7 respectively, then the data in the serial shift registers is shifted out as follows:

GR05[6:5]	Last Bit Shifted Out			Shift Direction →				1st Bit Shifted Out	Output to:
00:	M0D0	M0D1	M0D2	M0D3	M0D4	M0D5	M0D6	M0D7	Bit 0
	M1D0	M1D1	M1D2	M1D3	M1D4	M1D5	M1D6	M1D7	Bit 1
	M2D0	M2D1	M2D2	M2D3	M2D4	M2D5	M2D6	M2D7	Bit 2
	M3D0	M3D1	M3D2	M3D3	M3D4	M3D5	M3D6	M3D7	Bit 3
01:	M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	Bit 0
	M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	Bit 1
	M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	Bit 2
	M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	Bit 3
1x:	M3D0	M3D4	M2D0	M2D4	M1D0	M1D4	M0D0	M0D4	Bit 0
	M3D1	M3D5	M2D1	M2D5	M1D1	M1D5	M0D1	M0D5	Bit 1
	M3D2	M2D6	M3D2	M2D6	M1D2	M1D6	M0D2	M0D6	Bit 2
	M3D3	M3D7	M2D3	M2D7	M1D3	M1D7	M0D3	M0D7	Bit 3

Note: If the Shift Register is not loaded every character clock (see SR01[4,2]) then the four 8-bit shift registers are effectively 'chained' with the output of shift register 1 becoming the input to shift register 0 and so on. This allows one to have a large monochrome (or 4 color) bit map and display one portion thereof.

Note: If XR28[4] is set (8-bit video path), then GR05[6] must be set to 0:

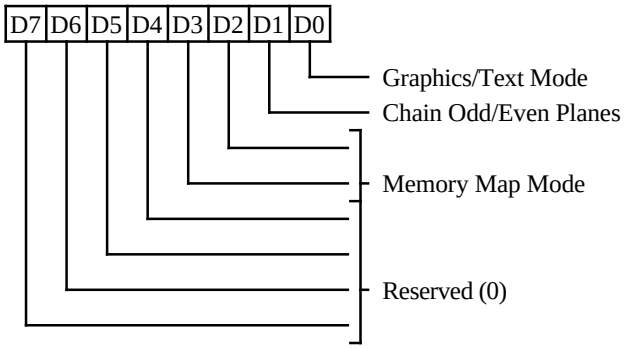
If XR28[4]=1:

GR05[6:5]	Last Bit Shifted Out	Shift Direction →			1st Bit Shifted Out	Output to:
0x		M3D0	M2D0	M1D0	M0D0	Bit 0
		M3D1	M2D1	M1D1	M0D1	Bit 1
		M3D2	M2D2	M1D2	M0D2	Bit 2
		M3D3	M2D3	M1D3	M0D3	Bit 3
		M3D4	M2D4	M1D4	M0D4	Bit 4
		M3D5	M2D5	M1D5	M0D5	Bit 5
		M3D6	M2D6	M1D6	M0D6	Bit 6
		M3D7	M2D7	M1D7	M0D7	Bit 7

7 Reserved (0)

MISCELLANEOUS REGISTER (GR06)

Read/Write at I/O Address 3CFh
Index 06h
Group 1 Protection



0 Graphics/Text Mode

0 Text Mode
1 Graphics mode

1 Chain Odd/Even Planes

This mode can be used to double the address space into display memory.

1 CPU address bit A0 is replaced by a higher order address bit. The state of A0 determines which memory plane is to be selected:

A0 = 0: select planes 0 and 2
A0 = 1: select planes 1 and 3

0 A0 not replaced

3-2 Memory Map Mode

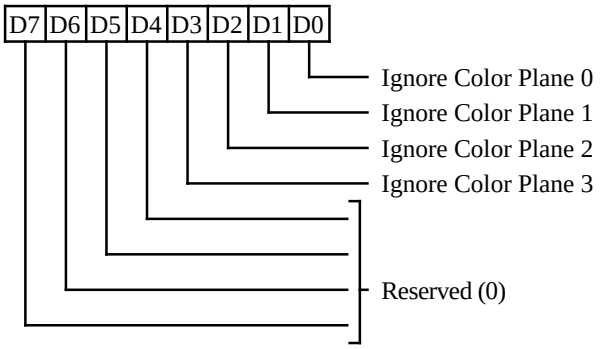
These bits control the mapping of the display memory into the CPU address space as follows (also used in extended modes):

Bit 3	Bit 2	CPU Address
0	0	A0000h-BFFFFh
0	1	A0000h-AFFFFh
1	0	B0000h-B7FFFh
1	1	B8000h-BFFFFh

7-4 Reserved (0)

COLOR DON'T CARE REGISTER (GR07)

Read/Write at I/O Address 3CFh
Index 07h
Group 1 Protection



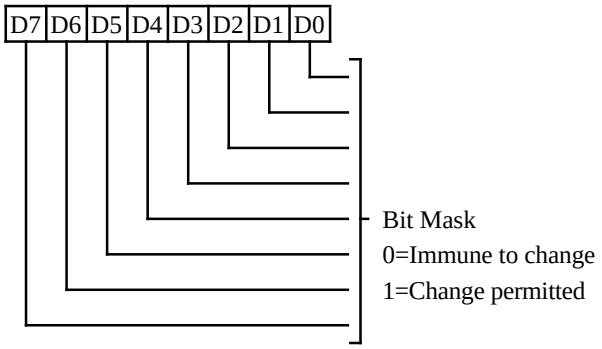
3-0 Ignore Color Plane (3-0)

0 This causes the corresponding bit of the Color Compare register to be a don't care during a comparison.

1 The corresponding bit of the Color Compare register is enabled for color comparison. This register is active in Read Mode 1 only.

7-4 Reserved (0)

BIT MASK REGISTER (GR08)
Read/Write at I/O Address 3CFh
Index 08h
Group 1 Protection



7-0 Bit Mask

This bit mask is applicable to any data written by the CPU, including that subject to a rotate, logical function (AND, OR, XOR), Set/Reset, and No Change. In order to execute a proper read-modify-write cycle into displayed memory, each byte must first be read (and latched by the VGA), the Bit Mask register set, and the new data then written. The bit mask applies to all four planes simultaneously.

0 The corresponding bit (7:0) in each of the four memory planes is written from the corresponding bit (7:0) in the latches.

1 Unrestricted manipulation of the corresponding data bit in each of the four memory planes is permitted.

Attribute Controller and VGA Color Palette Registers

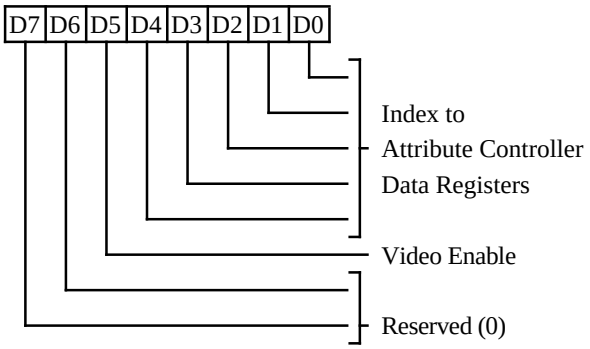
Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ARX	Attribute Index (for 3C0/3C1h)	–	R/W	3C0h	1	77
AR00-AR0F	Attribute Controller Color Data	00-0Fh	R/W	3C0h/3C1h	1	78
AR10	Mode Control	10h	R/W	3C0h/3C1h	1	78
AR11	Overscan Color	11h	R/W	3C0h/3C1h	1	79
AR12	Color Plane Enable	12h	R/W	3C0h/3C1h	1	79
AR13	Horizontal Pixel Panning	13h	R/W	3C0h/3C1h	1	80
AR14	Pixel Pad	14h	R/W	3C0h/3C1h	1	80
DACMASK	Color Palette Pixel Mask	–	R/W	3C6h	6	81
DACSTATE	Color Palette State	–	R	3C7h	–	81
DACRX	Color Palette Read-Mode Index	–	W	3C7h	6	82
DACX	Color Palette Index (for 3C9h)	–	R/W	3C8h	6	82
DACDATA	Color Palette Data	00-FFh	R/W	3C9h	6	82

In regular VGA mode, all Attribute Controller registers are located at the same byte address (3C0h) in the CPU I/O space. An internal flip-flop controls the selection of either the Attribute Index or Data Registers. To select the Index Register, an I/O Read is executed to address 3BAh/3DAh to clear this flip-flop. After the Index Register has been loaded by an I/O Write to address 3C0h, this flip-flop toggles, and the Data Register is ready to be accessed. Every I/O Write to address 3C0h toggles this flip-flop. The flip-flop does not have any effect on the reading of the Attribute Controller registers. The Attribute Controller index register is always read back at address 3C0h, the data register is always read back at address 3C1h.

In one of the extended modes (See "CPU Interface Register"), the Attribute Controller Index register is located at address 3C0h and the Attribute Controller Data register is located at address 3C1h (to allow word I/O accesses). In another extended mode, the Attribute Controller can be both read and written at either 3C0h or 3C1h (EGA compatible mode).

The VGA color palette logic is used to further modify the video color output following the attribute controller color registers. The color palette logic is contained on-chip. DAC logic is provided on-chip to convert the final video output of the color palette to analog RGB outputs for use in driving a CRT display.

ATTRIBUTE INDEX REGISTER (ARX)
Read/Write at I/O Address 3C0h
Group 1 Protection



4-0 Attribute Controller Index

These bits point to one of the internal registers of the Attribute Controller.

5 Enable Video

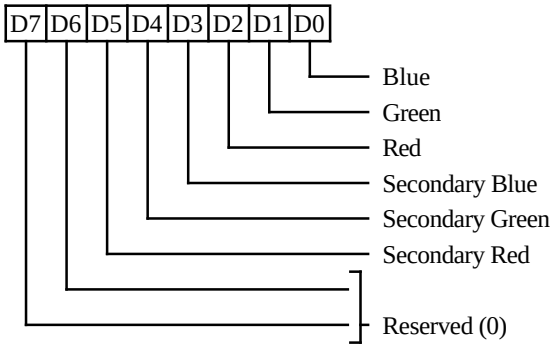
0 Disable video, allowing the Attribute Controller Color registers to be accessed by the CPU

1 Enable video, causing the Attribute Controller Color registers (AR00-AR0F) to be inaccessible to the CPU

7-6 Reserved (0)

ATTRIBUTE CONTROLLER COLOR REGISTERS (AR00-AR0F)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 00-0Fh
Group 1 Protection or XR63[6]



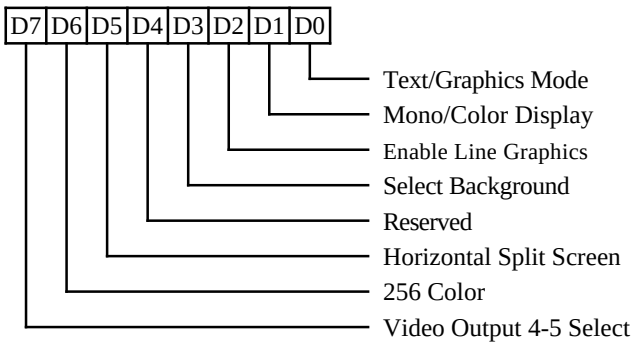
5-0 Color Value

These bits are the color value in the respective attribute controller color register as pointed to by the attribute index register.

7-6 Reserved (0)

ATTRIBUTE CONTROLLER MODE CONTROL REGISTER (AR10)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 10h
Group 1 Protection



0 Text/Graphics Mode

0 Select text mode
1 Select graphics mode

1 Monochrome/Color Display

0 Select color display attributes
1 Select mono display attributes

2 Enable Line Graphics Character Codes

0 Make the ninth pixel appear the same as the background

1 For special line graphics character codes (0C0h-0DFh), make the ninth pixel identical to the eighth pixel of the character. For other characters, the ninth pixel is the same as the background.

3 Enable Blink/Select Background Intensity

The blinking counter is clocked by the VSYNC signal. The Blink frequency is defined in the Blink Rate Control Register (XR60).

0 Disable Blinking and enable text mode background intensity

1 Enable the blink attribute in text and graphics modes.

4 Reserved (0)

5 Split Screen Horizontal Panning Mode

0 Scroll both screens horizontally as specified in the Pixel Panning register

1 Scroll horizontally only the top screen as specified in the Pixel panning register

6 256 Color Output Assembler

0 6-bits of video (translated from 4-bits by the internal color palette) are output every dot clock

1 Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot clock (256 color mode).

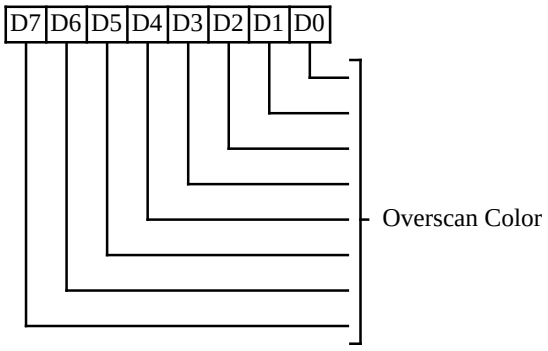
7 Video Output 5-4 Select

0 Video bits 4 and 5 are generated by the internal Attribute Controller color palette registers

1 Video bits 4 and 5 are the same as bits 0 and 1 in the Pixel Pad register (AR14[1:0])

OVERSCAN COLOR REGISTER (AR11)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 11H
Group 1 Protection



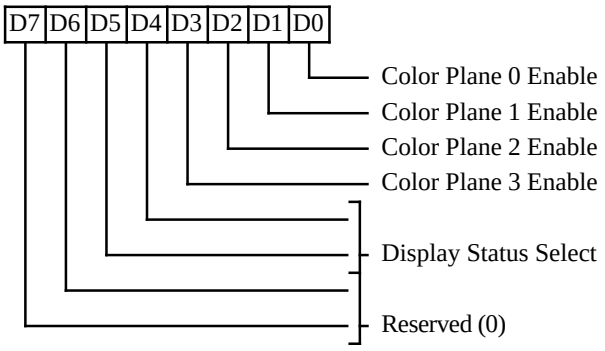
7-0 Overscan Color

These 8 bits define the overscan (border) color value. For monochrome displays, these bits should be zero.

The border color is displayed in the interval after Display Enable End and before Blank Start (end of display area; i.e. right side and bottom of screen) and between Blank End and Display Enable Start (beginning of display area; i.e. left side and top of screen).

COLOR PLANE ENABLE REGISTER (AR12)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 12h
Group 1 Protection



3-0 Color Plane (3-0) Enable

0 Force the corresponding color plane pixel bit to 0 before it addresses the color palette

1 Enable the plane data bit of the corresponding color plane to pass

5-4 Display Status Select

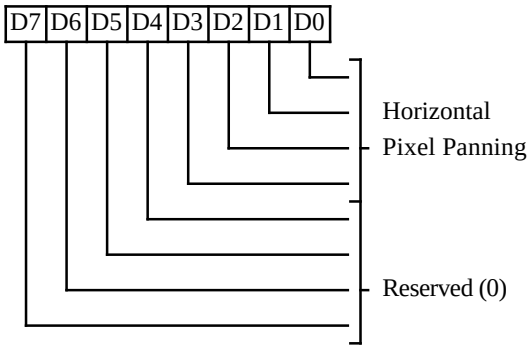
These bits select two of the eight color outputs to be read back in the Input Status Register 1 (port 3BAh or 3DAh). The output color combinations available on the status bits are as follows:

		Status Register 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

7-6 Reserved (0)

ATTRIBUTE CONTROLLER HORIZONTAL PIXEL PANNING REGISTER (AR13)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 13h
Group 1 Protection



3-0 Horizontal Pixel Panning

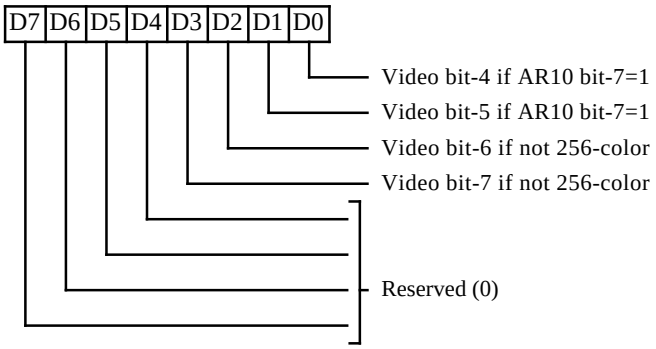
These bits select the number of pixels to shift the display horizontally to the left. Pixel panning is available in both text and graphics modes. In 9 pixel/character text mode, the output can be shifted a maximum of 9 pixels. In 8 pixel/character text mode and all graphics modes a maximum shift of 8 pixels is possible. In 256-color mode (output assembler AR10[6] = 1), bit 0 of this register must be 0 which results in only 4 panning positions per display byte. In Shift Load 2 and Shift Load 4 modes, register CR08 provides single pixel resolution for panning. Panning is controlled as follows:

	Number of Pixels Shifted		
AR13	**9-dot mode**	**8-dot mode**	**256-color mode**
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7-4 Reserved (0)

ATTRIBUTE CONTROLLER PIXEL PAD REGISTER (AR14)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 14h
Group 1 Protection



1-0 Video Bits 5-4

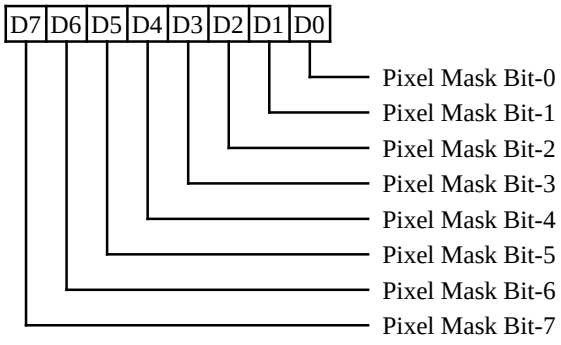
These bits are output as video bits 5 and 4 when AR10[7] = 1. They are disabled in the 256 color mode.

3-2 Video Bits 7-6

These bits are output as video bits 7 and 6 in all modes except 256-color mode.

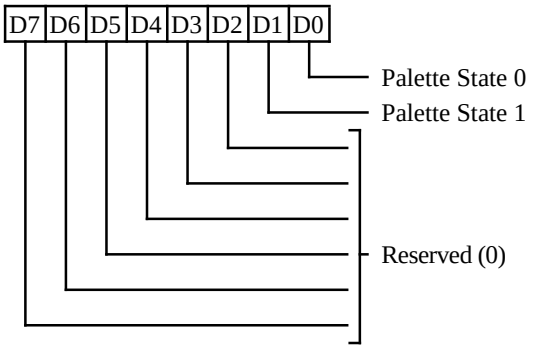
7-4 Reserved (0)

COLOR PALETTE
PIXEL MASK REGISTER (DACMASK)
Read/Write at I/O Address 3C6h
Group 6 Protection



The contents of this register are logically ANDed with the 8 bits of video data coming into the color palette. Zero bits in this register therefore cause the corresponding address input to the color palette to be zero. For example, if this register is programmed with 7, only color palette registers 0-7 would be accessible; video output bits 3-7 would be ignored and all color values would map into the lower 8 locations in the color palette.

COLOR PALETTE
STATE REGISTER (DACSTATE)
Read only at I/O Address 3C7h



1-0 Palette State 1-0

Status bits indicate the I/O address of the last CPU write to the Color Palette:

00 The last write was to 3C8h (write mode)

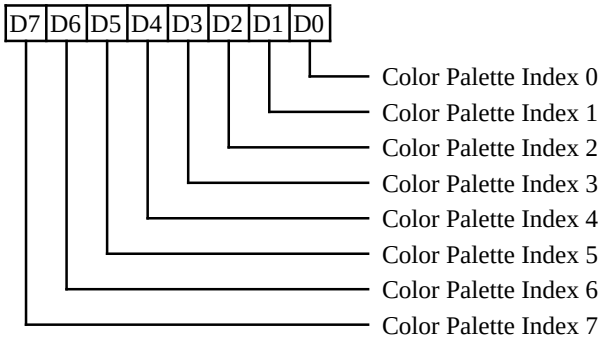
11 The last write was to 3C7h (read mode)

7-2 Reserved (0)

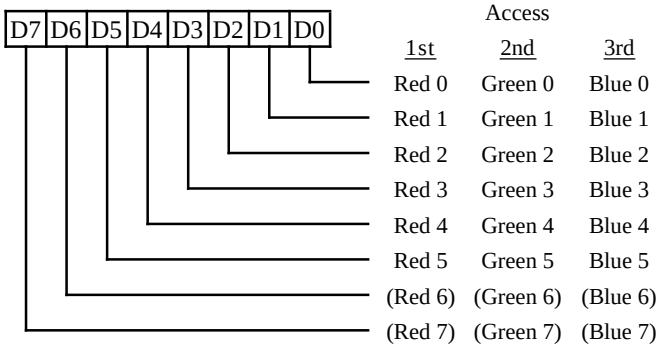
To allow saving and restoring the state of the video subsystem, this register is required since the color palette index register is automatically incremented differently depending on whether the index is written at 3C7h or 3C8h.

COLOR PALETTE
READ-MODE INDEX REGISTER (DACRX)
Write only at I/O Address 3C7h
Group 6 Protection

COLOR PALETTE
INDEX REGISTER (DACX)
Read/Write at I/O Address 3C8h
Group 6 Protection



COLOR PALETTE
DATA REGISTERS (DACDATA 00-FF)
Read/Write at I/O Address 3C9h
Index 00h-FFh
Group 6 Protection



The index register is used to point to one of 256 data registers. Each data register is either 18 or 24 bits in length depending on the type of palette chip used (6 or 8 bits each for red, green, and blue), so the data values must be read as a sequence of 3 bytes. After writing the index register (3C7h or 3C8h), data values may be read from or written to the color palette data register port (3C9h) in sequence: first red, then green, then blue, then repeat for the next location if desired (the index is incremented automatically by the palette logic).

The index may be written at 3C7h and may be read or written at 3C8h. When the index value is written to either port, it is written to both the index register and a 'save' register. The save register (not the index register) is used by the palette logic to point at the current data register. When the index value is written to 3C7h (**read mode**), it is written to both the index register and the save register, then the index register is automatically incremented. When the index value is written to 3C8h (**write mode**), the automatic incrementing of the index register does not occur.

After the third of the three sequential data reads from (or writes to) 3C9h is completed, the save and index registers are both automatically incremented by the palette logic. This allows the entire palette (or any subset) to be read (written) by writing the index of the first color in the set, then sequentially reading (writing) the values for each color, without having to reload the index every three bytes.

The state of the RGB sequence is not saved; the user must access each three bytes in an uninterruptable sequence (or be assured that interrupt service routines will not access the palette index or data registers). When the index register is written (at either port), the RGB sequence is restarted. Data value reads and writes may be intermixed; either reads or writes increment the palette logic's RGB sequence counter.

The palette's save register always contains a value one less than the readable index value if the last index write was to the 'read mode' port. The state is saved for which port (3C7h or 3C8h) was last written and that information is returned on reads from 3C7h.

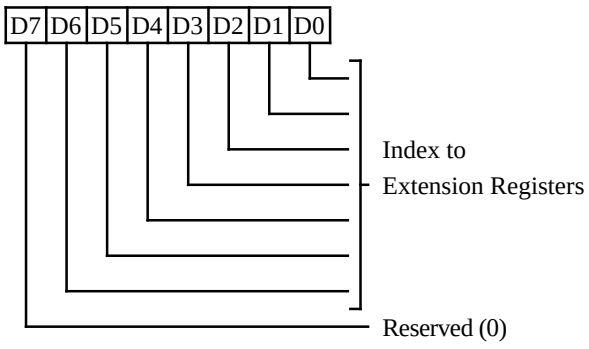
Extension Registers

Register Mnemonic	Register Group	Extension Register Name	Index	I/O Access	Address	State After Reset	Page
XRX	--	Extension Index	--	R/W	3D6h	- x x x x x x x	84
XR00	Config / Setup	Chip Version	00h	RO	3D7h	1 0 1 1 r r r r	84
XR01	Config / Setup	Configuration 1 (CFG0-7)	01h	RO	3D7h	d d d d d d d d	85
XR74	Config / Setup	Configuration 2 (CFG8-15)	74h	R/W	3D7h	d d d d d d d d	110
XR70	Config / Setup	Setup/Disable Control	70h	R/W	3D7h	0 - - - - - - -	107
XR02	Bus Interface	CPU Interface Control 1	02h	R/W	3D7h	x 0 0 0 0 - - -	86
XR03	Bus Interface	CPU Interface Control 2	03h	R/W	3D7h	- - - - - - 0 x	86
XR04	Memory Interface	Memory Control 1	04h	R/W	3D7h	- 0 0 - 0 0 0 0	87
XR05	Memory Interface	Memory Control 2	05h	R/W	3D7h	- - - 0 - - - -	88
XR0A	Memory Interface	XRAM Mode Control (64300 only)	0Ah	R/W	3D7h	x x 0 0 0 0 0 0	90
XR52	Memory Interface	Refresh Control	52h	R/W	3D7h	0 - - - - 0 0 0	106
XR06	Display Interface	Palette Control	06h	R/W	3D7h	- - - 0 0 0 0 0	88
XR28	Display Interface	Video Interface	28h	R/W	3D7h	• 0 0 0 • 0 0 0	98
XR73	Display Interface	Miscellaneous Control	73h	R/W	3D7h	- 0 0 0 0 x 0 x	109
XR0E	Text Control	Text Mode Control	0Eh	R/W	3D7h	- - - - 0 0 - 0	93
XR71	GPIO Interface	GPIO Control	71h	R/W	3D7h	0 0 0 0 0 0 0 0	108
XR72	GPIO Interface	GPIO Data	72h	R/W	3D7h	x x x x x x x x	108
XR40	BitBlt	BitBlt Configuration	40h	R/W	3D7h	- - - - - - x x	105
XR0F	Software Flags	Software Flags 0	0Fh	R/W	3D7h	x x x x x x x x	93
XR2B	Software Flags	Software Flags 1	2Bh	R/W	3D7h	x x x x x x x x	99
XR44	Software Flags	Software Flags 2	44h	R/W	3D7h	x x x x x x x x	106
XR75	Software Flags	Software Flags 3	75h	R/W	3D7h	x x x x x x x x	110
XR07	Mapping	I/O Base	07h	R/W	3D7h	1 1 1 1 0 1 0 0	89
XR08	Mapping	Linear Base Low	08h	R/W	3D7h	x x x x x - - -	89
XR09	Mapping	Linear Base High	09h	R/W	3D7h	x x x x x x x x	90
XR0B	Mapping	CPU Paging	0Bh	R/W	3D7h	- - - 0 - 0 0 0	91
XR0C	Mapping	Start Address Top	0Ch	R/W	3D7h	- 0 - 0 0 0 0 0	92
XR10	Mapping	Single/Low Map	10h	R/W	3D7h	x x x x x x x x	94
XR11	Mapping	High Map	11h	R/W	3D7h	x x x x x x x x	94
XR14	Compatibility	Emulation Mode	14h	R/W	3D7h	0 0 0 0 - - 0 0	95
XR15	Compatibility	Write Protect	15h	R/W	3D7h	0 0 0 0 0 0 0 0	95
XR0D	Alternate	Auxiliary Offset	0Dh	R/W	3D7h	- - - - 0 0 0 0	92
XR16	Alternate	Vertical Overflow	16h	R/W	3D7h	- 0 - 0 - 0 0 0	96
XR17	Alternate	Horizontal Overflow	17h	R/W	3D7h	0 0 x 0 x 0 0 0	96
XR19	Alternate	Alt H Sync Start / Half Line Compare	19h	R/W	3D7h	x x x x x x x x	97
XR30	Clock Control	Clock Divide Control	30h	R/W	3D7h	- - - - x x x x	100
XR31	Clock Control	Clock M-Divisor	31h	R/W	3D7h	- x x x x x x x	100
XR32	Clock Control	Clock N-Divisor	32h	R/W	3D7h	- x x x x x x x	101
XR33	Clock Control	Clock Control	33h	R/W	3D7h	- - x 0 - 0 0 0	101
XR3A	Multimedia	Color Key Compare Data 0	3Ah	R/W	3D7h	x x x x x x x x	102
XR3B	Multimedia	Color Key Compare Data 1	3Bh	R/W	3D7h	x x x x x x x x	102
XR3C	Multimedia	Color Key Compare Data 2	3Ch	R/W	3D7h	x x x x x x x x	103
XR3D	Multimedia	Color Key Compare Mask 0	3Dh	R/W	3D7h	x x x x x x x x	103
XR3E	Multimedia	Color Key Compare Mask 1	3Eh	R/W	3D7h	x x x x x x x x	104
XR3F	Multimedia	Color Key Compare Mask 2	3Fh	R/W	3D7h	x x x x x x x x	104
XR7D	Diagnostic	Diagnostic	7Dh	R/W	3D7h	0 0 0 0 0 0 0 0	111
XR7F	Diagnostic	Diagnostic	7Fh	R/W	3D7h	0 0 0 0 0 0 0 0	111

Reset Codes:
x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding pin on falling edge of RESET
0/1 = Reset to 0 or 1 by falling edge of RESET
– = Not implemented (always reads 0)
• = Not implemented (read/write, reset to 0)
r = Chip revision # (starting from 0000)

EXTENSION INDEX REGISTER (XRX)

Read/Write at I/O Address 3D6h

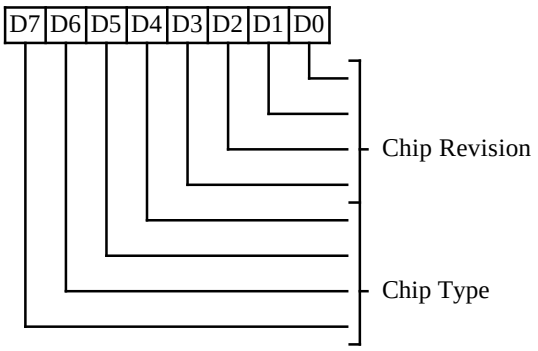


6-0 Index value used to access the extension registers

7 Reserved (0)

CHIPS VERSION REGISTER (XR00)

Read only at I/O Address 3D7h
Index 00h



3-0 Chip Revision

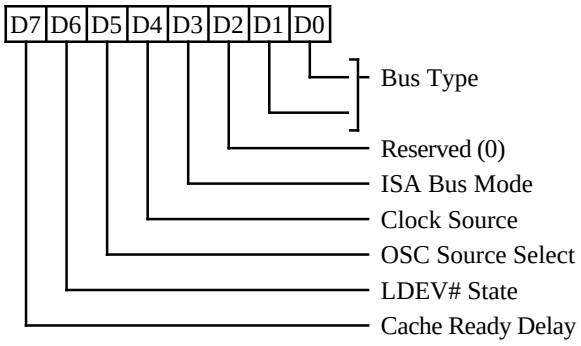
A revision number is stored in this nibble to identify the part. Numbering starts at 0h and is incremented for every silicon step.

7-4 Chip Type

Chips and Technologies drivers identify the 64300 / 301 via this nibble. For the 64300 / 301 this nibble will read back as 0Bh.

CONFIGURATION REGISTER 1 (XR01)

Read only at I/O Address 3D7h
Index 01h



These bits latch the state of MAD7:0 on the falling edge of RESET. The state of bits 7:0 after RESET effect chip internal logic as indicated below. MAD7:0 have no on-chip pullups or pull-downs; therefore, the state of these bits after RESET will be indeterminate if no external pullup or pulldown resistors are present.

This register is not related to the Virtual EGA Switch register (XR1F).

1-0 Processor Bus Type

00 16-bit ISA bus
01 Reserved
10 Reserved
11 32-bit local bus (386DX, 486DX, VL-Bus)

2 Reserved (0)

This bit is reserved and should be set to zero on reset for compatibility with future enhancements.

3 ISA Bus Mode

For ISA bus designs (XR01[10]=00) which use the internal clock as the host clock (XR0[7]=1) this bit chooses the divisor for host clock generation:

0 HCLK = MCLK
1 HCLK = MCLK÷2

For ISA bus interfaces:

25MHz ≤ HCLK ≤ 60MHz

Thus the HCLK frequency should be chosen based on the MCLK range at which the memory interface is to operate. Note that MCLK defaults to 60MHz on RESET.

For local bus designs (XR01[10]=1x) this bit is a "don't care" but should be set to zero for compatibility with future enhancements.

4 Clock Source

0 External Clock Source (82C404C)
1 Internal Clock Source

5 OSC Source Select

0 External Clock (TTL) drives XTAL IN. XTAL OUT is not connected.
1 Crystal connected to XTAL IN and XTAL OUT

6 LDEV# State

0 LDEV# is Open Collector driver driven only during first T2 of valid cycle. This is required to support some system logic chipsets which share the local device select line.
1 LDEV# is a straight decode driven active low for the duration of a valid decode; high otherwise. (VL-Bus compatible)

7 Cache Ready Delay

The VL-Bus specification allows the VL-controller to decide when the VL-Bus slave device can respond with RDY# on the VL-Bus during a slave access.

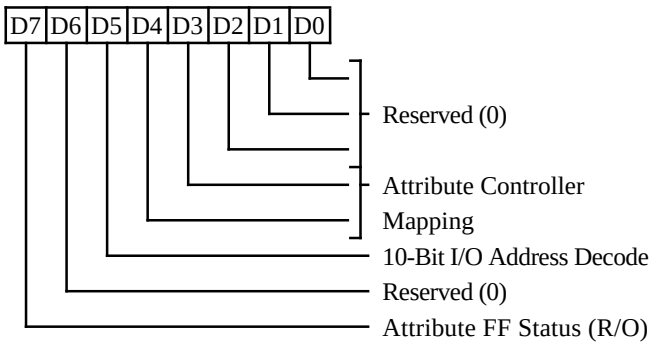
0 RDY# must hold off one HCLK cycle to allow CACHE to respond or relinguish the RDY# line.
1 RDY# may be exerted immediately to terminate a bus cycle.

In ISA bus mode, chooses between the internal MCLK as the host bus clock or an external clock input on LCLK.

0 Host clock is input on LCLK
1 Host clock is generated internally (see XR01[3])

CPU INTERFACE REGISTER 1 (XR02)

Read/Write at I/O Address 3D7h
Index 02h



2-0 Reserved (0)

4-3 Attribute Controller Mapping

00 Write Index and Data at 3C0h. (8-bit access only) (default - VGA mapping)
01 Write Index at 3C0h and Data at 3C1h (8-bit or 16-bit access). Attribute flip-flop (bit-7) is always reset in this mode (16-bit mapping)
10 Write Index and Data at 3C0h/3C1h (8-bit access only) (EGA mapping)
11 Reserved

5 I/O Address Decoding

0 Decode all 16 bits of I/O address (default)
1 Decode only lower 10 bits of I/O address. This affects the following addresses: 3B4h, 3B5h, 3B8h, 3BAh, 3BFh, 3C0h, 3C1h, 3C2h, 3C4h, 3C5h, 3CEh, 3CFh, 3D4h, 3D5h, 3D8h, 3D9h, and 3DAh.

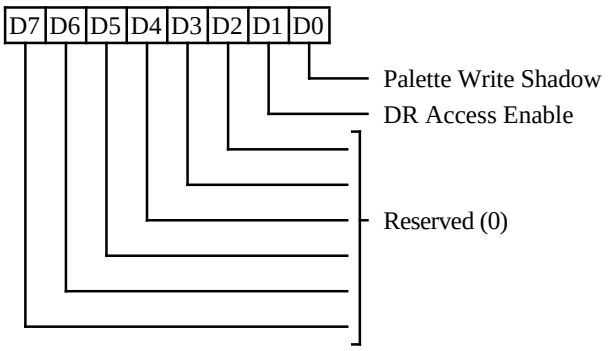
6 Reserved (0)

7 Attribute Flip-flop Status (read only)

0 = Index, 1 = Data

CPU INTERFACE REGISTER 2 (XR03)

Read/Write at I/O Address 3D7h
Index 02h



0 Palette Write Shadow

0 64300 / 301 responds to Palette Write accesses with LDEV#.
1 Palette Write commands are executed internally but the 64300 / 301 does not respond with LDEV#. This forces the ISA bus controller to broadcast the palette access onto the ISA bus where add-in cards may be shadowing the VGA LUT data. This is required for VL-Bus compatibility, so this bit should normally be set to 1.

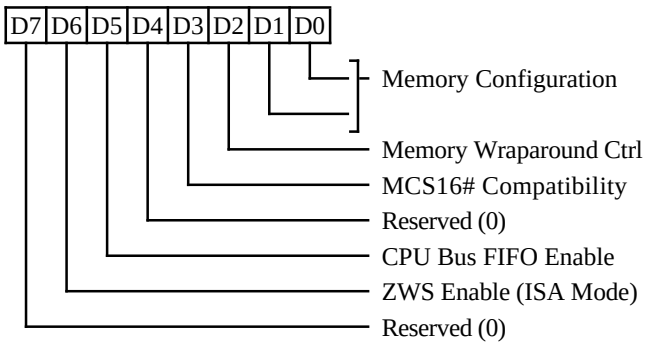
1 DR Register Access Enable

0 32-Bit DRxx register access Disabled (Default)
1 DRxx registers accessible at I/O port defined by XR07.

7-2 Reserved (0)

MEMORY CONTROL REGISTER (XR04)

Read/Write at I/O Address 3D7h
Index 04h



1-0 Memory Configuration

	Data Path	# of Chips	Memory Config	Total Memory
00	16-bit	4	256Kx4	1/2 MB
		1	256Kx16	1/2 MB
01	32-bit	8	256Kx4	1MB
		2	256Kx16	1MB
10	32-bit	16	256Kx4	2MB
		4	256Kx16	2MB
11	–	–	Reserved	–

2 Memory Wraparound Control

This bit enables bit-17 of the CRT Controller address counter (default = 0 on reset).

0 Disable CRTC address counter bit-17
1 Enable CRTC address counter bit-17

3 MCS16# Compatibility

The 64300 / 301 is a 16-bit memory slave on the ISA bus. If a secondary 8-bit MDA, Hercules, or CGA adapter is installed the 64300 / 301 must not exert MCS16# for that cards address range. Since MCS16# is expected to be an early unlatched decode this may cause problems in some machines:

0 Decode A0000 - BFFFFh using LA23:17 only. (Default).
1 Respond to the range enabled by GR06[3:2] (decode LA23:17 and SA16:15).

The 64300 / 301 always exerts MCS16# for accesses to its linear frame buffer.

4 Reserved (0)

5 CPU Bus FIFO Enable

0 Disable CPU bus FIFO (default)
1 Enable CPU bus FIFO

6 ZWS Enable

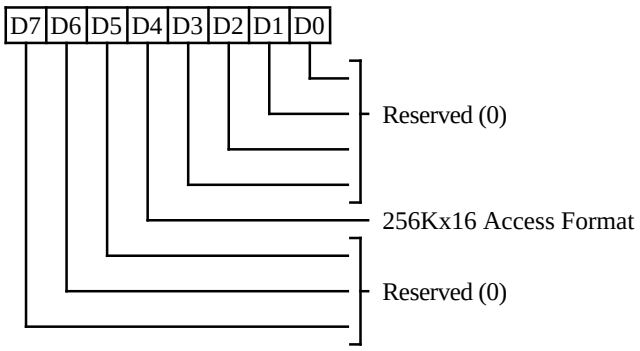
This bit affects only ISA bus operation.

0 Zero wait state disabled (default)
1 Zero wait state enabled

7 Reserved (0)

MEMORY CONTROL REGISTER 2 (XR05)

Read/Write at I/O Address 3D7h
Index 05h



3-0 Reserved (0)

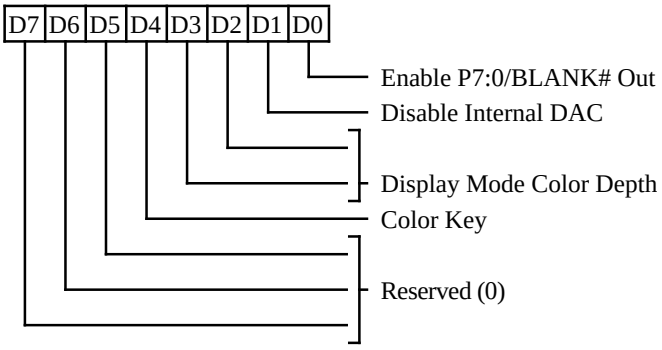
4 256Kx16 Access Format

0 2 CAS / 1 WE (default)
1 2 WE / 1 CAS

7–5 Reserved (0)

PALETTE CONTROL REGISTER (XR06)

Read/Write at I/O Address 3D7h
Index 06h



0 Enable External Pixel Data

This bit affects the direction of the Pixel Data Buffer (P7:0 / VID15:0) and BLANK# / KEY.

0 VID15:0 and KEY are inputs for live video overlay. (Default on reset)
1 P7:0 and BLANK# are outputs used for supporting an external feature connector or external color keying.

1 Disable/Powerdown Internal DAC

This bit affects the DAC analog outputs.

0 Enable internal DAC. DAC analog outputs (R, G, B) will be active. Default on reset.
1 Disable internal DAC. The DAC analog outputs (R, G, B) will be 3-stated. Setting this bit forces power down of the internal DAC.

3–2 Display Mode Color Depth

00 4BPP / 8BPP (default)
01 15BPP (5-5-5) Sierra Compatible
10 24BPP
11 16BPP (5-6-5) XGA Compatible

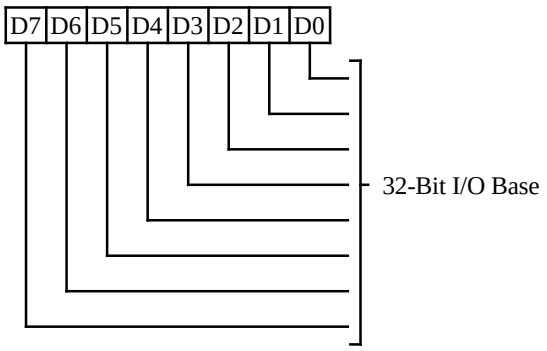
4 Video Color Key Enable

0 Video Overlay disabled (default)
1 Video Overlay on Color Key enabled

7–5 Reserved (0)

I/O BASE REGISTER (XR07)

Read/Write at I/O Address 3D7h
Index 07h



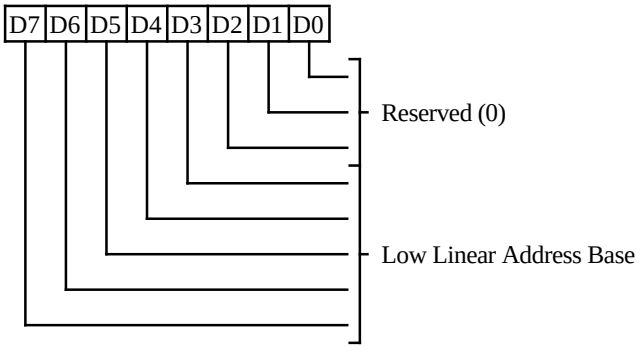
7–0 32-Bit I/O Base

These 8 bits determine the I/O range for the 32-bit Doubleword Hardware Cursor and BitBlt registers (DRxx). The value programmed in this register is matched against CPU addresses A15, A8:2. Address A9 must equal 1 and A14 through A10 select one of 32 registers.. For example, programming this register to 0F4h (111101 00b) will result in an address decode of 83D0-83D3h for register DR00. Upper address bits A14:10 are used to select one of 32 possible 32-Bit registers.

The DRxx registers are enabled for access by setting XR03[1]. They are disabled following reset. The programmer should write this register before enabling accesses to the DRxx registers.

LINEAR BASE LOW REGISTER (XR08)

Read/Write at I/O Address 3D7h
Index 08h



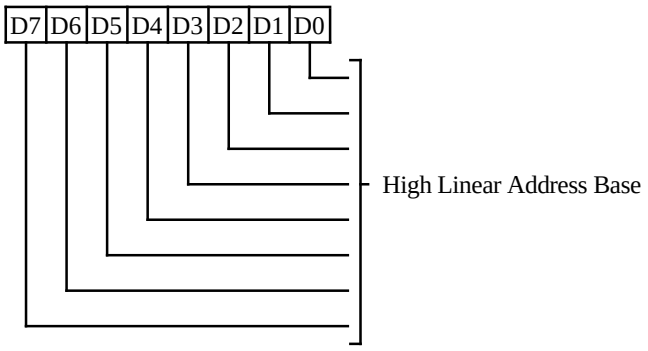
2–0 Reserved (0)

7–3 Low Linear Address Base

These 5 bits are compared to A23:19 in conbination with the High Linear Address Base for determining the base address of the linear frame buffer. This defines a 512 KByte boundary within the 4 GByte address space. If the frame buffer is 1MB (XR04[1:0]=01) then bit-3 must = 0 to align the frame buffer on a 1MB boundary. Similarly, if the frame buffer is 2MB (XR04[1:0]=10) then bits 4 and 3 must = 0 to align on a 2MB boundary.

LINEAR BASE HIGH REGISTER (XR09)

Read/Write at I/O Address 3D7h
Index 09h

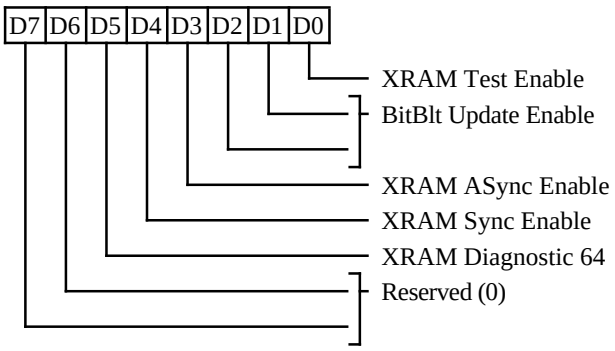


7–0 High Linear Address Base

These 8 bits are compared to A31:24 in conbination with the Low Linear Address Base for determining the base address of the linear frame buffer.

XRAM MODE REGISTER (XR0A)

Read/Write at I/O Address 3D7h
Index 0Ah **(64300 only)**



0 XRAM Test Enable

0 XRAM normal mode (default)
1 XRAM Read/Write

2-1 BitBlt Update Enable

00 No Update during BitBlt (default)
11 BitBlt Update Enabled

3 XRAM Asynchronous Enable

0 XRAM not enabled (default)
1 XRAM enabled asynchronously

4 XRAM Synchronous Enable

0 XRAM not enabled (default)
1 XRAM enabled synchronously

5 XRAM Diagnostic 64

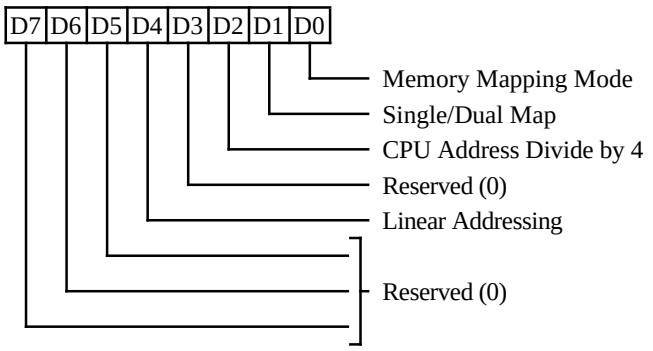
Must be set to zero.

7-6 Reserved (0)

Note: These bits should be programmed to 0 in the 64301. This register defaults to 0 on RESET.

CPU PAGING REGISTER (XR0B)

Read/Write at I/O Address 3D7h
Index 0Bh



0 Memory Mapping Mode

0 Normal Mode (VGA compatible) (default on Reset)

1 Extended Mode (mapping for ≥ 512 KByte memory configurations)

1 CPU Single/Dual Mapping

0 CPU uses only a single map to access the extended video memory space (default on Reset)

1 CPU uses two maps to access the extended video memory space. The base addresses for the two maps are defined in the Low Map Register (XR10) and High Map Register (XR11).

2 CPU Address Divide by 4

0 Disable divide by 4 for CPU addresses (default on Reset)

1 Enable divide by 4 for CPU addresses. This allows the video memory to be accessed sequentially in mode 13. In addition, all video memory is available in mode 13 by setting this bit.

3 Reserved (0)

4 Linear Addressing

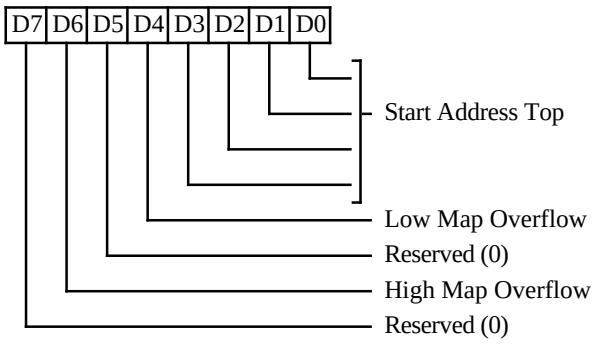
0 Standard VGA (0A0000h - 0BFFFFh) memory space decoded on-chip using A19-17 (default on Reset)

1 Linear Addressing (512K - 2MB depending on the Memory Config bits XR04[1:0]). The base address is defined by concatenating registers XR08, and XR09. The resulting 12-bit address is compared to address bits A31:20. When 1MB of memory is present, A20 must = 0 (any 1MB boundary). For 2MB both A21 and A20 must be zero (any 2MB boundary).

7–5 Reserved (0)

START ADDRESS TOP REGISTER (XR0C)

Read/Write at I/O Address 3D7h
Index 0Ch



3–0 Start Address Top

These bits define the high order bits for the Display Start Address (see XR04 bits 1–0). Note that this is a doubleword address.

4 Low Map Overflow

Contains the MSB for the Low Map Register (XR10). To map at any 4Kboundary inside of a 2MByte frame buffer 9 address bits are required. This bit along with the eight bits in XR10 define a 4K boundary.

5 Reserved (0)

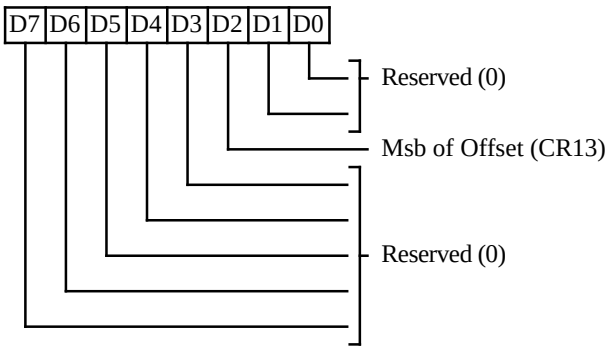
6 High Map Overflow

Contains the MSB for the High Map Register (XR11). To map at any 4Kboundary inside of a 2MByte frame buffer 9 address bits are required. This bit along with the eight bits in XR11 define a 4K boundary.

7 Reserved (0)

AUXILIARY OFFSET REGISTER (XR0D)

Read/Write at I/O Address 3D7h
Index 0Dh



1-0 Reserved (0)

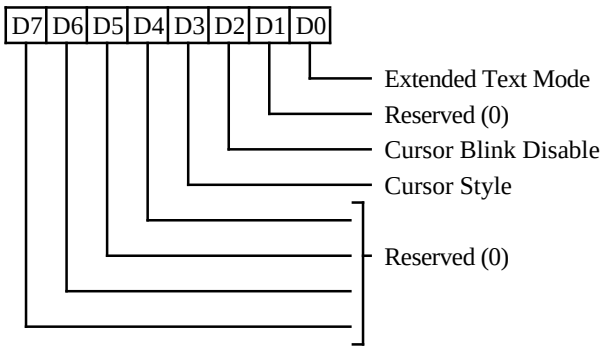
2 Offset Register MSB

This bit extends the addressing range to the next display line. This bit is used with the regular Offset register (CR13). It permits the byte offset to be as large as 4095 bytes between lines.

7-3 Reserved (0)

TEXT MODE CONTROL REGISTER (XR0E)

Read/Write at I/O Address 3D7h
Index 0Eh



0 Extended Text Mode

For high resolution text modes the font data may be scrambled in Plane 2 for improved page-mode accesses.

0 Normal font addressing (Default)
1 Font scrambling enabled

1 Reserved (0)

2 Cursor Mode

0 Blinking (default on Reset)
1 Non-blinking

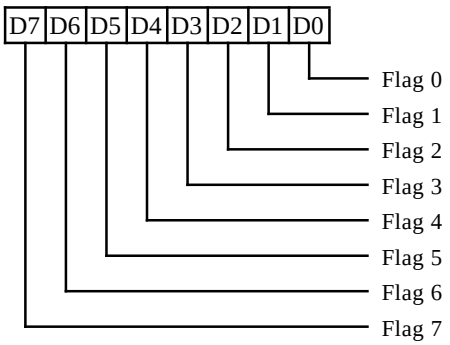
3 Cursor Style

0 Replace (default on Reset)
1 Exclusive-Or

7-4 Reserved (0)

SOFTWARE FLAG REGISTER 0 (XR0F)

Read/Write at I/O Address 3D7h
Index 0Fh

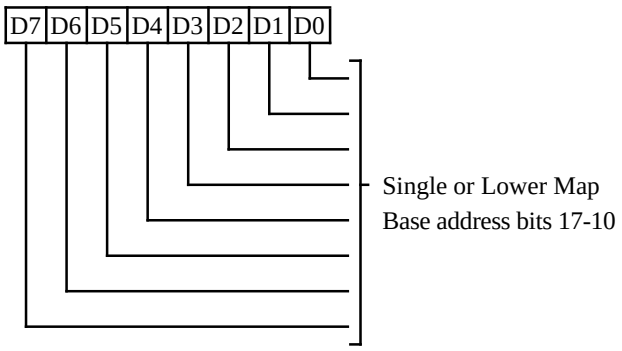


This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software.

7-0 Flags

SINGLE/LOW MAP REGISTER (XR10)

Read/Write at I/O Address 3D7h
Index 10h



This register effects CPU memory address mapping.

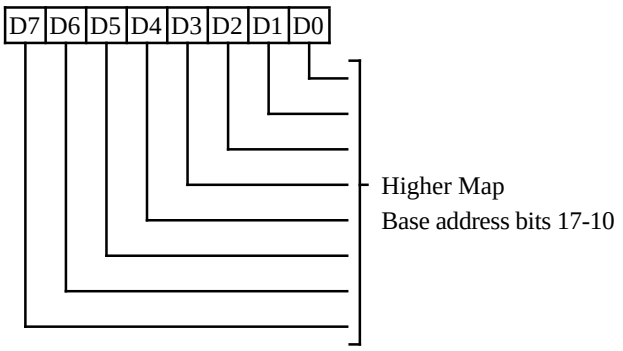
7-0 Single / Low Map Base Address Bits 17-10

These bits define the base address in single map mode (XR0B[1] = 0), or the lower map base address in dual map mode (XR0B[1] = 1). The memory map starts on a 4K boundary. In case of dual mapping, this register controls the CPU window into display memory based on the contents of GR06[3:2] as follows:

GR06[3:2]	Low Map	Comments
00	A0000-AFFFF	
01	A0000-A7FFF	
10	B0000-B7FFF	Single mapping only
11	B8000-BFFFF	Single mapping only

HIGH MAP REGISTER (XR11)

Read/Write at I/O Address 3D7h
Index 11h



This register effects CPU memory address mapping.

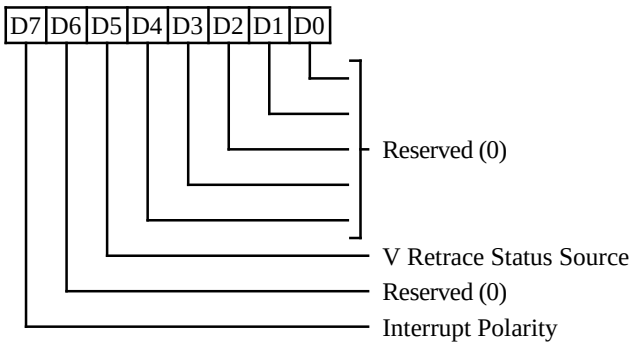
7-0 High Map Base Address Bits 17-10

These bits define the Higher Map base address in dual map modes (XR0B[1] =1). The memory map starts on a 1K boundary in planar modes and on a 4K boundary in packed pixel modes. This register controls the CPU window into display memory based on the contents of GR06[3:2] as follows:

GR06[3:2]	Low Map	Comments
00	B0000-BFFFF	
01	A8000-AFFFF	
10	Don't care	Not Valid
11	Don't care	Not Valid

EMULATION MODE REGISTER (XR14)

Read/Write at I/O Address 3D7h
Index 14h



4-0 Reserved (0)

5 Vertical Retrace Status Source

This bit affects the Vertical Retrace Status read back in the Input Status Register 1[3].

0 Select Vertical Retrace Status to be the same as at the pin.

1 Select Vertical Retrace Status to be the same as seen by the CRTC.

6 Reserved (0)

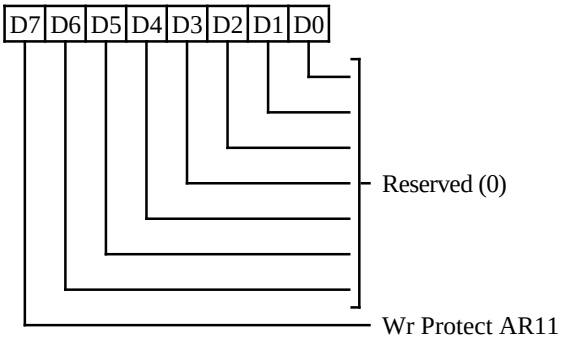
7 Interrupt Output Function

This bit controls the function of the interrupt output pin (IRQ). For all bus interfaces:

Interrupt State	bit-7=0	bit-7=1
Disabled	3-state	3-state
Enabled, Inactive	3-state	Low
Enabled, Active	3-state	High

WRITE PROTECT REGISTER (XR15)

Read/Write at I/O Address 3D7h
Index 15h



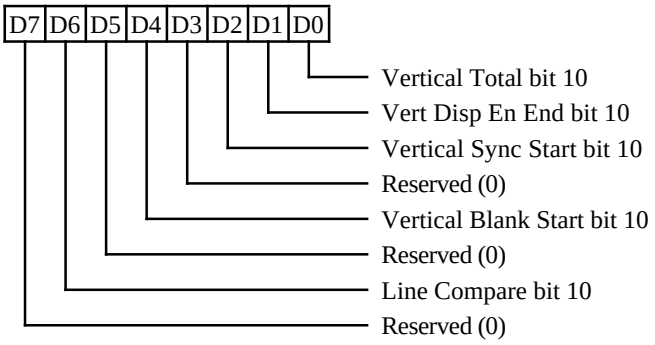
6-0 Reserved (0)

7 Write Protect AR11

Writing to AR11 is possible only if both XR15[7] is 0. This feature is used for write protection of the overscan color. This is important in order to keep application software from changing the border color while still permitting the attribute controller to be changed for the addressable portion of the display. Overscan is increasingly becoming an egronomic requirement and this bit will ensure software compatibility.

VERTICAL OVERFLOW REGISTER (XR16)

Read/Write at I/O Address 3D7h
Index 16h



This register is used in high resolution / high color graphics modes to handle vertical count values greater than is supported in the VGA register set.

0 Vertical Total (Bit 10)

Extension of Vertical Total count as defined by CR06[7:0], CR07[0], and CR07[5] (default = 0).

1 Vertical Display Enable End (Bit 10)

Extension of Vertical Display Enable count as defined by CR12[7:0], CR07[1], and CR07[6] (default = 0).

2 Vertical Sync Start (Bit 10)

Extension of Vertical Sync Start count as defined by CR10[7:0], CR07[2], and CR07[7] (default = 0).

3 Reserved (0)

4 Vertical Blank Start (Bit 10)

Extension of Vertical Blank Start count as defined by CR15[7:0], CR07[3], and CR09[5] (default = 0).

5 Reserved (0)

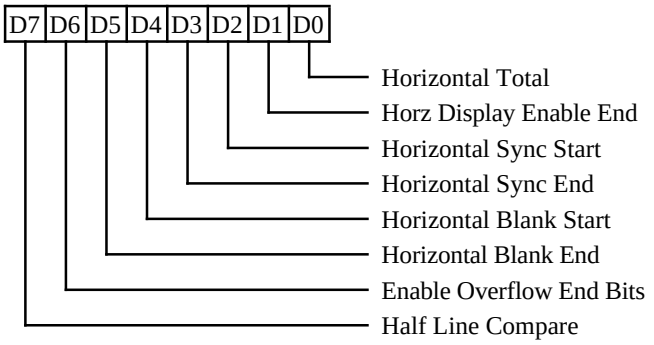
6 Line Compare (Bit 10)

Extension of Line Compare count as defined by CR18[7:0], CR07[4], and CR09[6] (default = 0).

7 Reserved (0)

HORIZONTAL OVERFLOW REGISTER (XR17)

Read/Write at I/O Address 3D7h
Index 17h



0 Horizontal Total (Bit 8)

Extension of Horizontal Total count as defined by CR00[7:0] (default = 0).

1 Horizontal Display Enable End (Bit 8)

Extension of Horizontal Display Enable count as defined by CR01[7:0] (default = 0).

2 Horizontal Sync Start (Bit 8)

Extension of Horizontal Sync Start count as defined by CR04[7:0] (default = 0).

3 Horizontal Sync End (Bit 5)

Extension of Horizontal Sync End count as defined by CR05[4:0].

4 Horizontal Blank Start (Bit 8)

Extension of Horizontal Blank Start count as defined by CR02[7:0] (default = 0).

5 Horizontal Blank End (Bit 6)

Extension of Horizontal Blank End count as defined by CR03[4:0] and CR05[7].

6 Enable Overflow End Bits

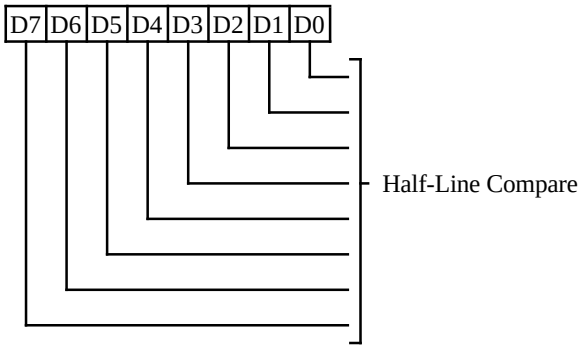
The values in XR17[5,3] are only enabled for use when this bit is set.

0 Not involved in comparison (default)
1 Enabled to participate in comparison

7 Half Line Compare (Bit 8)

Extension of Half Line count as defined by XR19[7:0] (default = 0).

HALF LINE REGISTER (XR19)
Read/Write at I/O Address 3D7h
Index 19h

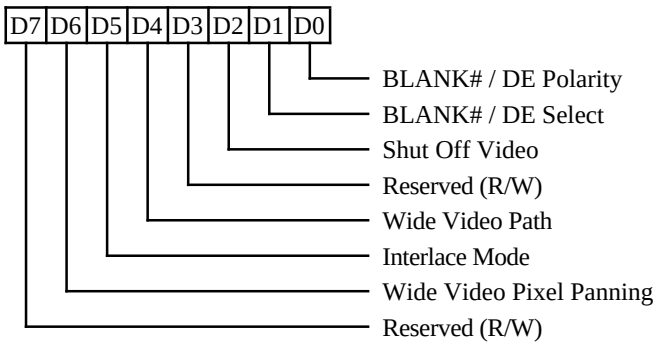


7-0 CRT Half-line Value

In CRT interlaced video mode this value is used to generate the 'half-line compare' signal that controls the positioning of the VSync for odd frames.

VIDEO INTERFACE REGISTER (XR28)

Read/Write at I/O Address 3D7h
Index 28h



0 BLANK# / Display Enable Polarity

This bit controls the polarity of the BLANK# pin.

0 Negative polarity (default on Reset)
1 Positive polarity

1 BLANK# / Display Enable Select

0 BLANK# pin outputs BLANK# (default on reset)
1 BLANK# pin outputs Display Enable

Note: The signal polarity selected by XR28[0] is applicable for either selection.

2 Shut Off Video

This bit is effective in CRT modes during horizontal / vertical blank time. This bit should be set properly when using CRT displays which look at video signals during blank time. It has no effect on displays that ignore video signals during blank time. This bit is also ignored when the screen is blanked.

0 When the screen is not blanked, video is forced to the border / overscan color (AR11) during blank time (default on Reset)
1 When the screen is not blanked, video is forced to 0.

3 Reserved (R/W)

This bit is implemented as a read/write bit but has no internal hardware function.

4 Wide Video Path

This bit doubles the values in all horizontal CRTC registers.

0 4-bit video data path (default on reset)
1 8-bit video data path (horizontal pixel panning is controlled by XR28[6])

Note: GR05[5] must be 0 if this bit is set

5 Interlace Video

This bit is effective only for CRT graphics mode. In interlace mode XR19 holds the half-line positioning of VSync for odd frames.

0 Non-interlaced video (default on reset)
1 Interlaced video

6 Wide Video Pixel Panning

This bit is effective when the wide video data path is selected (XR28[4] = 1 and AR10[6] = 1).

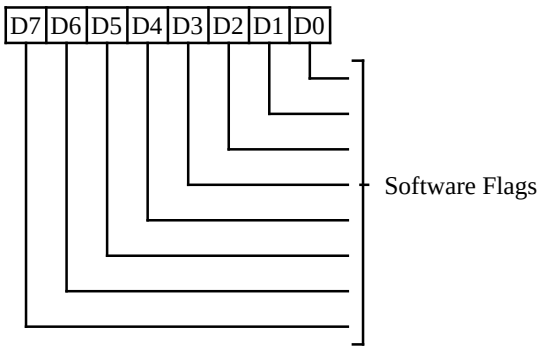
0 AR13[2:1] are used to control pixel panning (default on Reset)
1 AR13[2:0] are used to control pixel panning

7 Reserved (R/W)

This bit is implemented as a read/write bit but has no internal hardware function.

SOFTWARE FLAGS REGISTER 1 (XR2B)

Read/Write at I/O Address 3D7h
Index 2Bh

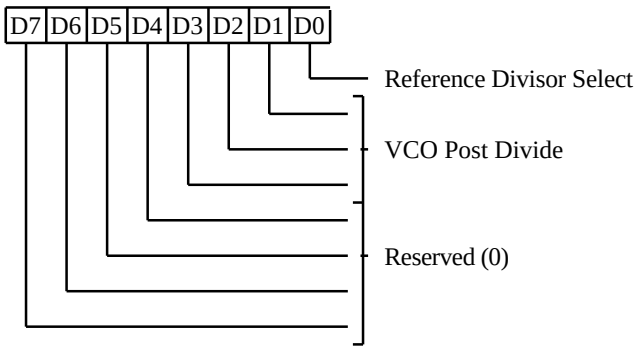


7-0 Software Flags

These bits are used by CHIPS software device drivers.

CLOCK DIVIDE CONTROL REGISTER (XR30)

Read/Write at I/O Address 3D7h
Index 30h



Three clock data ports (XR30-XR32) may be used to program loop parameters for loading into either the "memory" or "video" clock synthesizers. There are two sets of programmable registers, one for the Memory clock VCO and one for the Video clock VCO. The VCO currently selected for programming is determined by the Clock Register Program Pointer (XR33[5]).

The data written to these registers is calculated based on the reference frequency, the desired output frequency, and characteristic VCO constraints as described in the Functional Description.

Data must be written to these registers in sequence: first XR30, then XR31, and finally XR32. The completion of the write to XR32 causes data from all three registers to be transferred to the VCO register file simultaneously. This prevents wild fluctuations in the VCO output during intermediate stages of a clock programming sequence.

0 Reference Divisor Select

Selects the reference pre-scale factor:

0 Divide by 4
1 Divide by 1

3–1 Post Divisor Select

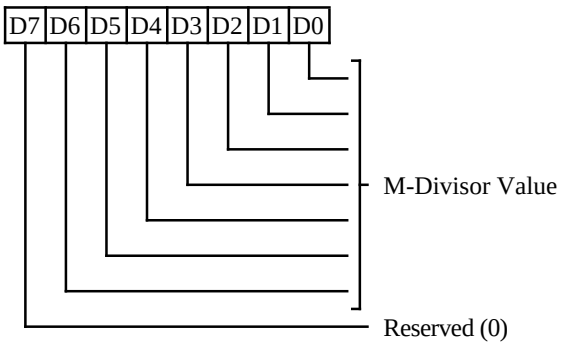
Selects the post-divide factor:

000 Divide by 1
001 Divide by 2
010 Divide by 4
011 Divide by 8
100 Divide by 16
101 Divide by 32
110 Divide by 64
111 Divide by 128

7–4 Reserved (0)

CLOCK M-DIVISOR REGISTER (XR31)

Read/Write at I/O Address 3D7h
Index 31h



Three clock data ports (XR30-XR32) may be used to program loop parameters for loading into either the "memory" or "video" clock synthesizers. There are two sets of programmable registers, one for the Memory clock VCO and one for the Video clock VCO. The VCO currently selected for programming is determined by the Clock Register Program Pointer (XR33[5]).

The data written to these registers is calculated based on the reference frequency, the desired output frequency, and characteristic VCO constraints as described in the Functional Description.

Data must be written to these registers in sequence: first XR30, then XR31, and finally XR32. The completion of the write to XR32 causes data from all three registers to be transferred to the VCO register file simultaneously. This prevents wild fluctuations in the VCO output during intermediate stages of a clock programming sequence.

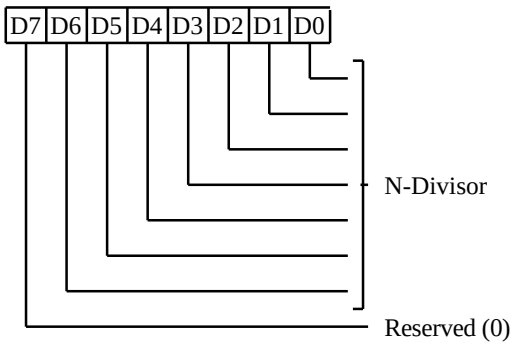
6–0 VCO M-Divisor

Programmed Value = Calculated Value – 2

7 Reserved (0)

CLOCK N-DIVISOR REGISTER (XR32)

Read/Write at I/O Address 3D7h
Index 32h



Three clock data ports (XR30-XR32) may be used to program loop parameters for loading into either the "memory" or "video" clock synthesizers. There are two sets of programmable registers, one for the Memory clock VCO and one for the Video clock VCO. The VCO currently selected for programming is determined by the Clock Register Program Pointer (XR33[5]).

The data written to these registers is calculated based on the reference frequency, the desired output frequency, and characteristic VCO constraints as described in the Functional Description.

Data must be written to these registers in sequence: first XR30, then XR31, and finally XR32. The completion of the write to XR32 causes data from all three registers to be transferred to the VCO register file simultaneously. This prevents wild fluctuations in the VCO output during intermediate stages of a clock programming sequence.

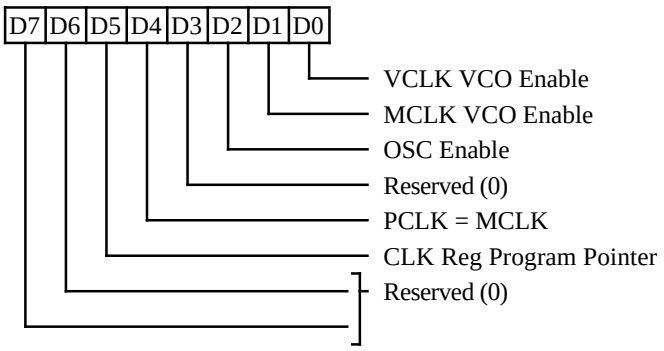
6–0 VCO N-Divisor

Programmed Value = Calculated Value – 2

7 Reserved (0)

CLOCK CONTROL REGISTER (XR33)

Read/Write at I/O Address 3D7h
Index 33h



0 VCLK VCO Enable

0 VCLK VCO Disabled
1 VCLK VCO Enabled (Default)

This bit is only effective if XR01[4] = 1.

1 MCLK VCO Enable

0 MCLK VCO Disabled
1 MCLK VCO Enabled (Default)

This bit is only effective if XR01[4] = 1.

2 OSC Enable

0 OSC Disabled
1 OSC Enabled (Default)

This bit is only effective if XR01[5] = 1.

3 Reserved (0)

4 PCLK Equals MCLK

For situations where VCLK and MCLK must be synchronous, the VCLK VCO may be shut down and MCLK may be routed to PCLK.

0 PCLK equals VCLK (default)
1 PCLK equals MCLK

5 Clock Register Program Pointer

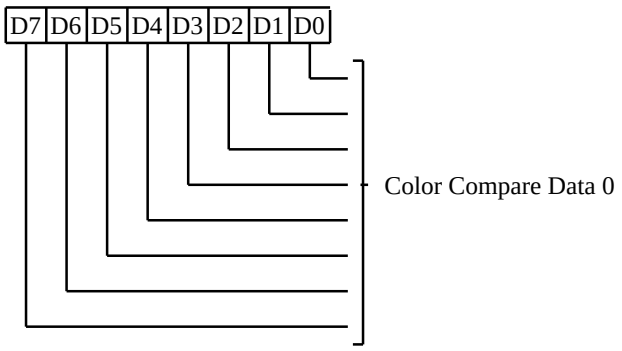
This bit determines which VCO is being programmed. Following a write to XR32 the data contained in XR30:32 is synchronously transferred to the appropriate VCO counter latch.

0 VCLK VCO selected
1 MCLK VCO selected

7–6 Reserved (0)

COLOR KEY COMPARE DATA 0 (XR3A)

Read/Write at I/O Address 3D7h
Index 3Ah



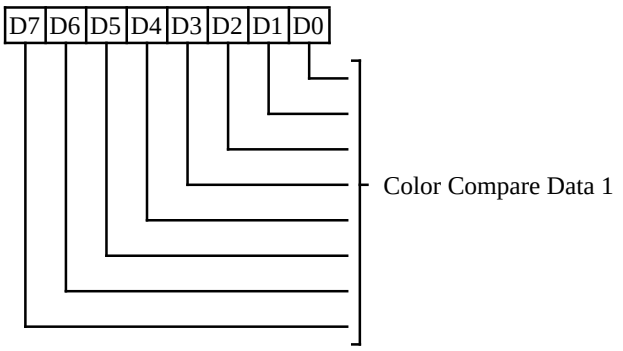
7-0 Color Compare Data 0

These bits are compared to the least significant 8 bits of the background video stream (64300 / 301 memory data). If a match occurs on all enabled bits (see Color Compare Mask Register XR3D) and the key is enabled (XR06[4]), external video is sent to the screen. External video is input on RGB15:0 pins. There may also be an external key qualifier input on GPIO enabled by XR72[3]. The logical masking and compare operations are described in the functional description.

The color comparison occurs before the RAMDAC. In 4BPP and 8BPP modes using palette LUT data, the LUT index is used in the comparison, not the 18BPP LUT data.

COLOR KEY COMPARE DATA 1 (XR3B)

Read/Write at I/O Address 3D7h
Index 3Bh

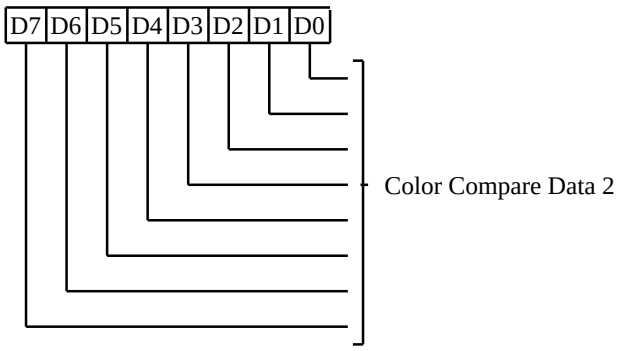


7-0 Color Compare Data 1

These bits are compared to bits 15:8 of the background video stream (64300 / 301 memory data). If a match occurs on all enabled bits (see Color Compare Mask Register XR3D) and the key is enabled (XR06[4]), external video is sent to the screen. External video is input on RGB15:0 pins. There may also be an external key qualifier input on GPIO enabled by XR72[3]. The logical masking and compare operations are described in the functional description. This register should be masked from participating in the comparison in 4BPP and 8BPP modes. This is accomplished by setting Color Mask Register 1 (XR3E) = 0FFh.

COLOR KEY COMPARE DATA 2 (XR3C)

Read/Write at I/O Address 3D7h
Index 3Ch

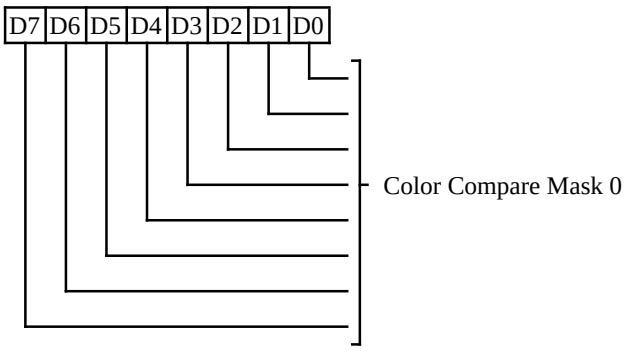


7-0 Color Compare Data 2

These bits are compared to bits 23:16 of the background video stream (64300 / 301 memory data). If a match occurs on all enabled bits (see Color Compare Mask Register XR3D) and the key is enabled (XR06[4]), external video is sent to the screen. External video is input on RGB15:0 pins. There may also be an external key qualifier input on GPIO enabled by XR72[3]. The logical masking and compare operations are described in the functional description. This register should be masked from participating in the comparison in 4BPP, 8BPP and 16BPP modes. It should only be used in 24BPP modes. This is accomplished by setting Color Mask Register 2 (XR3F) = 0FFh.

COLOR KEY COMPARE MASK 0 (XR3D)

Read/Write at I/O Address 3D7h
Index 3Dh



7-0 Color Compare Mask 0

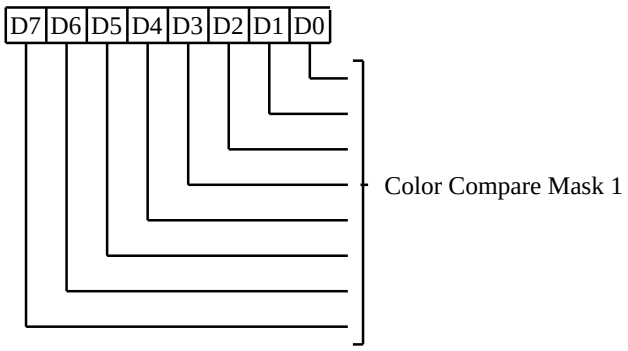
This register is used to select which bits of the background video data stream (64300 / 301 memory data) are used in the comparison with the Color Compare Data 23:0. This register controls bits 7:0.

0 Data does participate in compare operation

1 Data does not participate in compare operation (masked)

COLOR KEY COMPARE MASK 1 (XR3E)

Read/Write at I/O Address 3D7h
Index 3Eh



7-0 Color Compare Mask 1

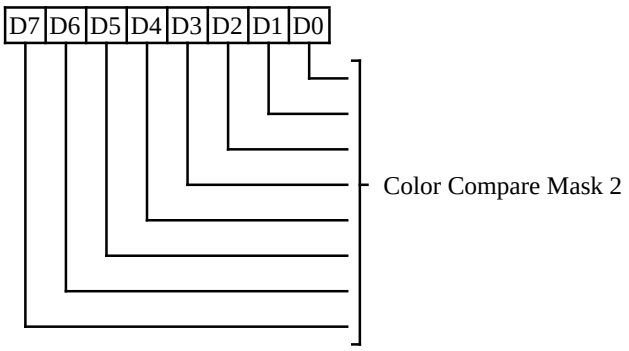
This register is used to select which bits of the background video data stream (64300 / 301 memory data) are used in the comparison with the Color Compare Data 23:0. This register controls bits 7:0.

0 Data does participate in compare operation

1 Data does not participate in compare operation (masked)

COLOR KEY COMPARE MASK 2 (XR3F)

Read/Write at I/O Address 3D7h
Index 3Fh



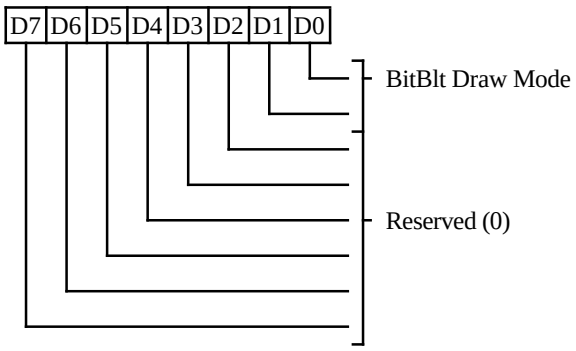
7-0 Color Compare Mask 2

This register is used to select which bits of the background video data stream (64300 / 301 memory data) are used in the comparison with the Color Compare Data 23:0. This register controls bits 7:0.

0 Data does participate in compare operation

1 Data does not participate in compare operation (masked)

BITBLT CONFIG REGISTER (XR40)
Read/Write at I/O Address 3D7h
Index 40h



1–0 BitBlt Draw Mode

The 64300 / 301 supports two color depths in its drawing engine:

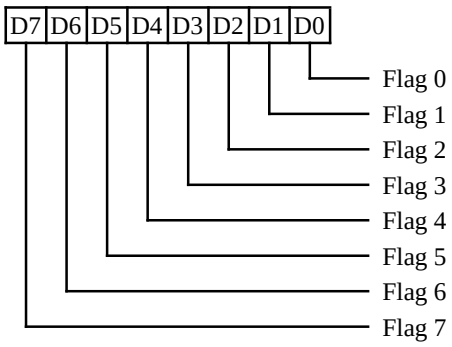
00 Reserved
01 8BPP
10 16BPP
11 Reserved

Note: 24BPP is handled in 8BPP mode. There is no nibble mode access for 4BPP modes.

7–2 Reserved (0)

SOFTWARE FLAG REGISTER 2 (XR44)

Read/Write at I/O Address 3D7h
Index 44h

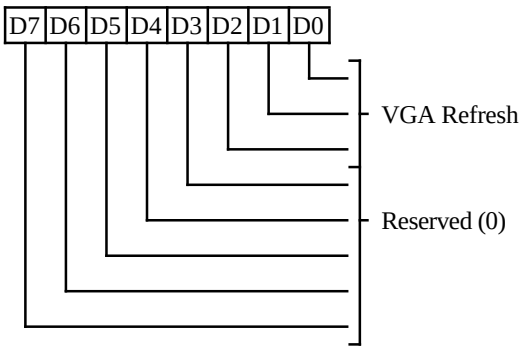


This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software.

7-0 Flags

REFRESH CONTROL REGISTER (XR52)

Read/Write at I/O Address 3D7h
Index 52h



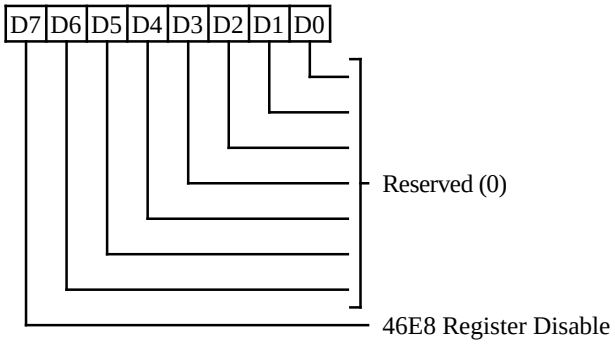
2-0 VGA Refresh

Standard VGA modes perform 3 or 5 memory refresh cycles at the end of each scan line. The 64300 / 301 supports a wider range of horizontal scan frequencies than the original VGA modes. For performance optimization the number of refresh cycles performed per line may be optimized:

000 Default
001 1 Refresh cycle per scan line
010 2 Refresh cycles per scan line
011 3 Refresh cycles per scan line
100 4 Refresh cycles per scan line
101 5 Refresh cycles per scan line
110 Illegal
111 Illegal

7-3 Reserved (0)

SETUP / DISABLE CONTROL REGISTER (XR70)
Read/Write at I/O Address 3D7h
Index 70h



6-0 Reserved (0)

7 46E8 Register Disable

0 Port 46E8h works as defined to provide control of VGA disable and setup mode.
1 Writes to I/O port 46E8h have no effect (the VGA remains enabled and will not go into setup mode).

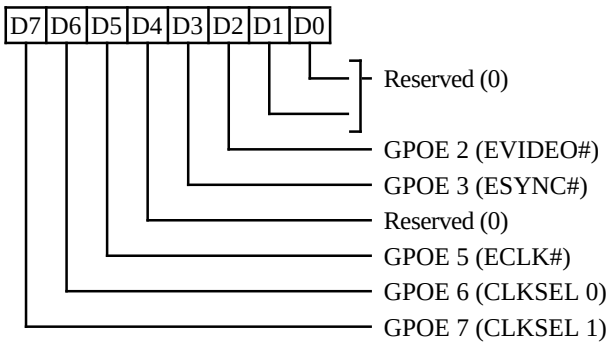
Note: Writes to register 46E8 are effective in all 64300 / 301 bus configurations

Reads from port 46E8h have no effect independent of the programming of this register (46E8h is a write-only register).

This register is cleared by RESET.

GPIO CONTROL REGISTER (XR71)

Read/Write at I/O Address 3D7h
Index 71h



1-0 Reserved (0)

3-2 GPOE

This register controls the direction (input / output) of the respective GPIO pins.

0 GPIO pin is an input (default)
1 GPIO pin is an output

If the IBM standard feature connector is enabled (XR73[4]=1) bits GPIO3:2 become alternate fixed function inputs (EVIDEO# and ESYNC#). XR71[3:2] must be set to the input state.

4 Reserved (0)

7-5 GPOE

This register controls the direction (input / output) of the respective GPIO pins.

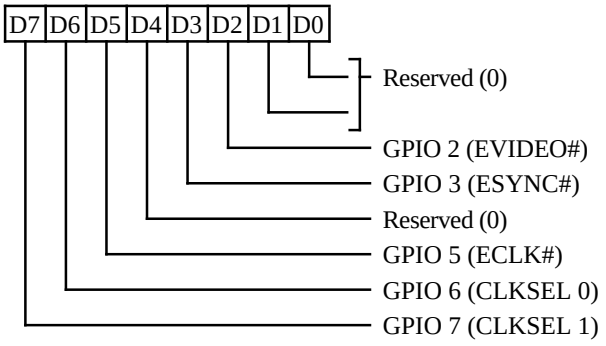
0 GPIO pin is an input (default)
1 GPIO pin is an output

If the IBM standard feature connector is enabled (XR73[4]=1) bits GPIO5 becomes an alternate fixed function input (ECLK#). XR71[5] must be set to the input state.

If XR01[4] is cleared on reset (external clock synthesizer selected) then GPOE 7:6 have no effect. General purpose bits GPIO 7:6 become CLKSEL1:0 and output the contents of MSR[3:2].

GPIO DATA REGISTER (XR72)

Read/Write at I/O Address 3D7h
Index 72h



1-0 Reserved (0)

3-2 GPIO

The data written to this register is latched and output on the respective GPIO pins. A read to this register always yields the data present on the respective GPIO pin regardless of its function. This is not necessarily the data which was last written to this register as some of the pins may be in input mode (see XR71) or may be defined as their alternate function (see XR73 and XR01).

When the IBM standard feature connector is enabled (XR73[4]=1) GPIO bits 3:2 become alternate fixed function inputs (EVIDEO# and ESYNC#).

4 Reserved (0)

7-5 GPIO

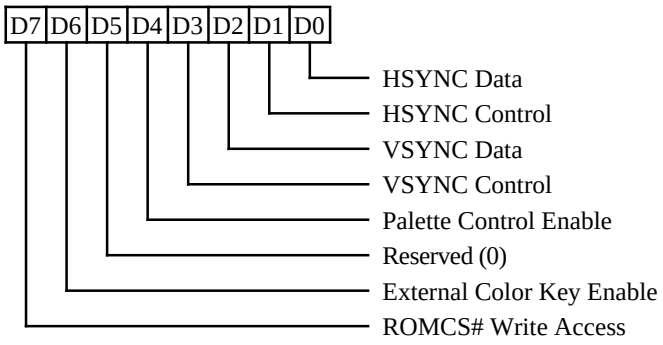
The data written to this register is latched and output on the respective GPIO pins. A read to this register always yields the data present on the respective GPIO pin regardless of its function. This is not necessarily the data which was last written to this register as some of the pins may be in input mode (see XR71) or may be defined as their alternate function (see XR73 and XR01).

When the IBM standard feature connector is enabled (XR73[4]=1) GPIO bit 5 becomes an alternate fixed function input (ECLK#).

Similarly when an external clock synthesizer is selected (XR01[4]=0) GPIO[7:6] become clock select outputs CLKSEL1:0 (MSR3:2).

MISC CONTROL REGISTER (XR73)

Read/Write at I/O Address 3D7h
Index 73h



0 HSYNC Data

If bit-1 of this register (XR73[1]) is programmed to 1, the state of this bit (XR73[0]) will be output on the HSYNC pin. This may be used in advanced monitor detection and monitor power-down schemes.

1 HSYNC Control

Determines whether XR73[0] or internal CRTC horizontal sync information is output on HSYNC pin 125.

0 CRTC HSYNC is output (Default)
1 XR73[0] is output

2 VSYNC Data

If bit-3 of this register (XR73[3]) is programmed to 1, the state of this bit (XR73[2]) will be output on the VSYNC pin. This may be used in advanced monitor detection and monitor power-down schemes.

3 VSYNC Control

Determines whether XR73[2] or internal CRTC vertical sync information is output on VSYNC pin 126.

0 CRTC VSYNC is output (Default)
1 XR73[2] is output

4 Reserved (0)

5 Standard Feature Connector Enable

0 Feature connector is not enabled. GPIO5, 3:2 are general purpose I/O pins. (default)

1 Feature Connector control pin functionality is enabled on GPIO pins 5, and 3:2. This bit must be set before the pixel data is enabled via XR06[0].

6 External Color Key Enable

0 Color Key input does not participate in color compare (default)

1 Color Key input must be valid (active high) to qualify live video. This may be used to define the rectangular window within which color matching will occur and permits other open windows to use the overlay color.

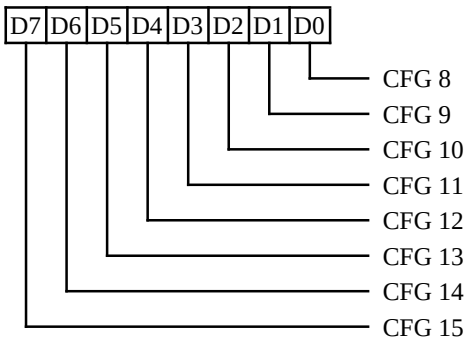
7 ROMCS# Write Access

0 ROMCS# is active only during read accesses to the memory range 00C0000 - 00C7FFFh. (Default)

1 ROMCS# is active for both reads and writes to the memory address range 00C0000 - 00C7FFFh. This may be used for programming Flash ROM devices.

CONFIGURATION REGISTER 2 (XR74)

Read/Write at I/O Address 3D7h
Index 74h

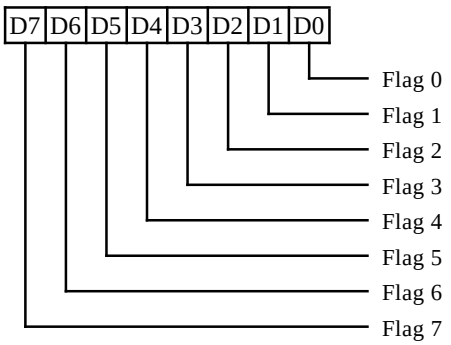


7-0 CFG15:8

Configuration Data latched from configuration pins 15:8 (MAD15:8) on the falling edge of RESET. Unlike configuration bits 7:0, these bits have no other defined direct hardware function. They may therefore be used by the system designer to input any desired information.

SOFTWARE FLAG REGISTER 3 (XR75)

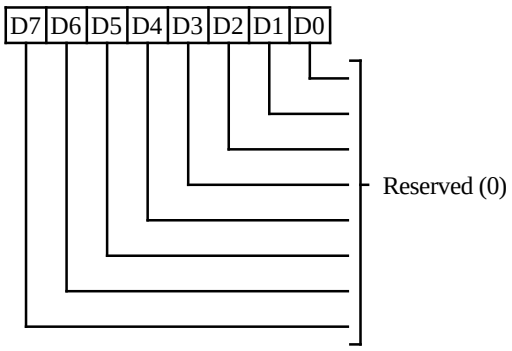
Read/Write at I/O Address 3D7h
Index 75h



This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software.

7-0 Software Flags

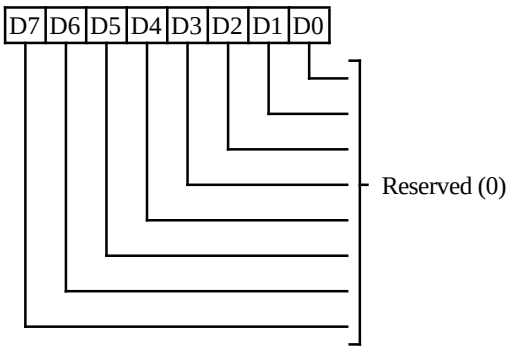
DIAGNOSTIC REGISTER (XR7D)
Read/Write at I/O Address 3D7h
Index 7Dh



7–0 Reserved (0)

WARNING: Software should never read or write this register.

DIAGNOSTIC REGISTER (XR7F)
Read/Write at I/O Address 3D7h
Index 7Fh



7–0 Reserved (0)

WARNING: Software should never read or write this register.

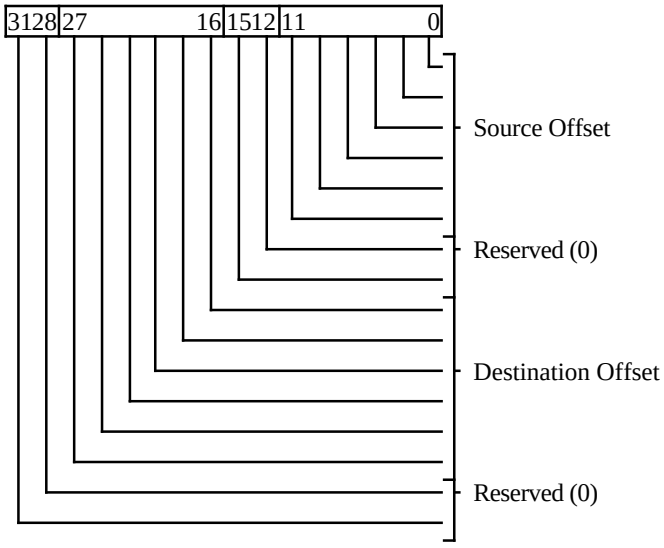
32-Bit Registers

Register Mnemoni	Register Group	Extension Register Name	Access	I/O Type	Address	State After Reset				Page
DR00	BitBlt	BitBlt Offset	16/32-bit	R/W	83D0-3	----xxxx	xxxxxxxx	----xxxx	xxxxxxxx	114
DR01	BitBlt	BitBlt Pattern ROP	16/32-bit	R/W	87D0-3	--------	---xxxxx	xxxxxxxx	xxxxxxxx	114
DR02	BitBlt	BitBlt BG Color	16/32-bit	R/W	8BD0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	115
DR03	BitBlt	BitBlt FG Color	16/32-bit	R/W	8FD0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	115
DR04	BitBlt	BitBlt Control	16/32-bit	R/W	93D0-3	--------	---0xxxx	xxxxxxxx	xxxxxxxx	116
DR05	BitBlt	BitBlt Source	16/32-bit	R/W	97D0-3	--------	---xxxxx	xxxxxxxx	xxxxxxxx	117
DR06	BitBlt	BitBlt Destination	16/32-bit	R/W	9BD0-3	--------	---xxxxx	xxxxxxxx	xxxxxxxx	118
DR07	BitBlt	BitBlt Command	16/32-bit	R/W	9FD0-3	----0000	00000000	----xxxx	xxxxxxxx	118
DR08	Cursor	Cursor R/W Index	16/32-bit	R/W	A3D0-3	-------x	xxxxxxxx	--------	00000000	119
DR09	Cursor	Cursor Color 0	16/32-bit	R/W	A7D0-3	--------	xxxxxxxx	xxxxxxxx	xxxxxxxx	120
DR0A	Cursor	Cursor Color 1	16/32-bit	R/W	ABD0-3	--------	xxxxxxxx	xxxxxxxx	xxxxxxxx	120
DR0B	Cursor	Cursor Position	16/32-bit	R/W	AFD0-3	x----xxx	xxxxxxxx	x----xxx	xxxxxxxx	121
DR0C	Cursor	Cursor Data	16/32-bit	R/W	B3D0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	122

Reset Codes:
x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding pin on falling edge of RESET
0/1 = Reset to 0 or 1 by falling edge of RESET
– = Not implemented (always reads 0)
• = Not implemented (read/write, reset to 0)
r = Chip revision # (starting from 0000)

BITBLT OFFSET REGISTER (DR00)

Write at I/O Address 83D0–83D3h
Read at I/O Address 83D0–83D3h
Word or DoubleWord Accessible



11–0 Source Offset

This value is added to the start address of the Source BitBlt to calculate the starting position for the next line.

15–12 Reserved (0)

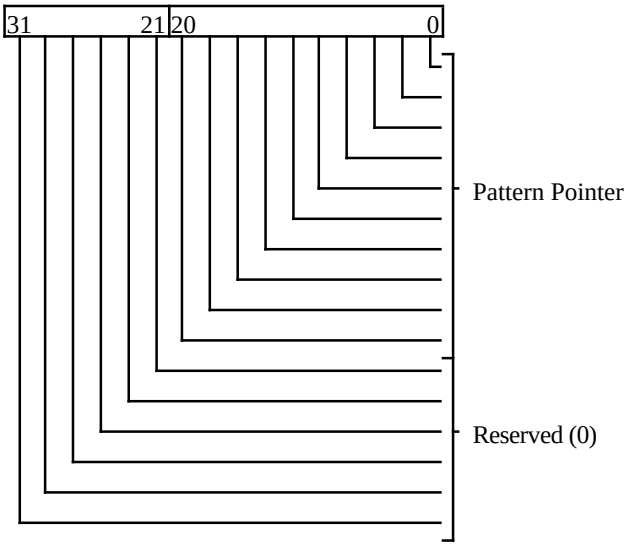
27–16 Destination Offset

This value is added to the start address of the Destination BitBlt to calculate the starting position for the next line.

31–28 Reserved (0)

BITBLT PATTERN ROP REGISTER (DR01)

Write at I/O Address 87D0–87D3h
Read at I/O Address 87D0–87D3h
Word or DoubleWord Accessible



20–0 Pattern Pointer

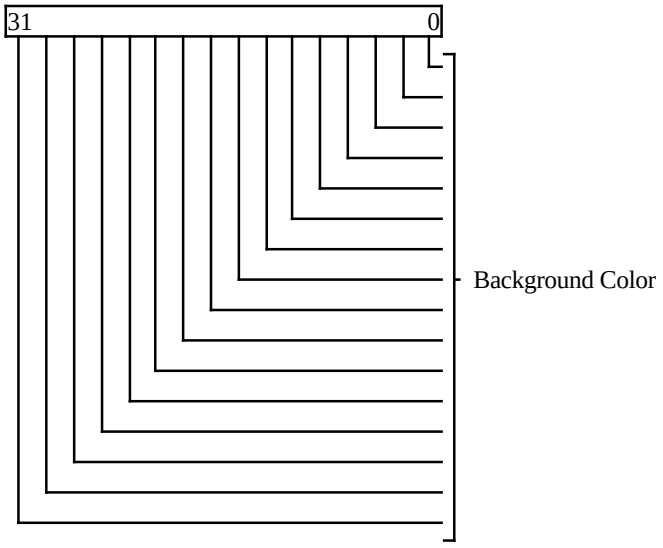
Address of Pattern Size - aligned 8 Pixel x 8 line pattern. For an 8BPP pattern (occupying 8 bits / pixel * 8 pixels / line * 8 lines / pattern) the pattern must be aligned on a 64 byte (16 DWord) boundary. For a 16BPP pattern (occupying 16bits / pixel * 8 pixels / line * 8 lines / pattern) the pattern must be aligned on a 128byte (32 DWord) boundary. For monochrome patterns (1 Bit / pixel * 8 pixels / line * 8 lines / pattern) the pattern must be aligned on an 8 byte (2 DWord) boundary. The lower bits of the Pattern Pointer are read/write, however the Drawing Engine forces them to zero for drawing operations.

31–21 Reserved (0)

Warning: Do not read this register while a BitBlt is active.

BITBLT BACKGROUND COLOR REGISTER (DR02)

Write at I/O Address 8BD0–8BD3h
Read at I/O Address 8BD0–8BD3h
Word or DoubleWord Accessible



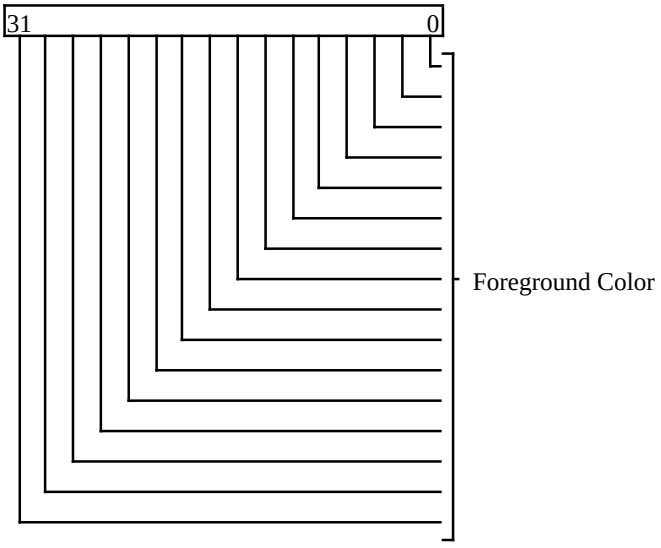
31–0 Background Color

This register contains the background color data used during opaque mono-color expansions.

All 32 bits must be written regardless of pixel depth. If the drawing engine is operating at 8BPP, then the same data should be duplicated in bits 31:24, 23:16, 15:8, and 7:0. For 16BPP the data is duplicated twice.

BITBLT FOREGROUND COLOR REGISTER (DR03)

Write at I/O Address 8FD0–8FD3h
Read at I/O Address 8FD0–8FD3h
Word or DoubleWord Accessible



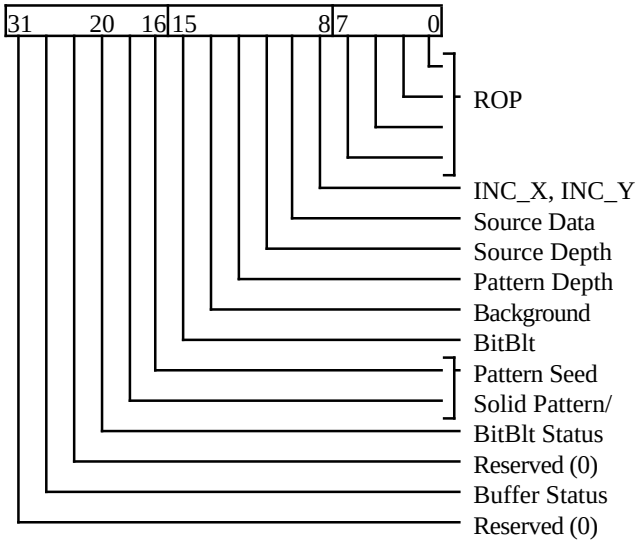
31–0 Foreground / Solid Color

This register contains the color data used during solid paint operations. It also is used as the foreground color during mono-color expansions.

All 32 bits must be written regardless of pixel depth. If the drawing engine is operating at 8BPP, then the same data should be duplicated in bits 31:24, 23:16, 15:8, and 7:0. For 16BPP the data is duplicated twice.

BITBLT CONTROL REGISTER (DR04)

Write at I/O Address 93D0–93D3h
Read at I/O Address 93D0–93D3h
Word or DoubleWord Accessible



7–0 ROP

Raster Operation as defined by Microsoft Windows. All logical operations of Source, Pattern, and Destination Data are supported.

8 INC_Y

Determines Y-direction for BitBLT

0 = Decrement (Bottom to Top)
1 = Increment (Top to Bottom)

9 INC_X

Determines X-direction for BitBLT

0 = Decrement (Right to Left)
1 = Increment (Left to Right)

10 Source Data

Selects variable data or color register data for the source:

1 = Source is Frgd Color Reg (DR03)
0 = Source data selected by DR04[14].

11 Source Depth

Selects between monochrome and color source data. This allows BitBlts to either transfer source data directly to the screen, or perform a font expansion (INC_X=1 only):

0 = Source is Color
1 = Source is Mono (Font expansion)

12 Pattern Depth

Selects between monochrome and color pattern data. This allows the pattern register to operate either as a full pixel depth 8x8 pattern for use by the ROP, or as an 8x8 monochrome pattern:

0 = Pattern is Color
1 = Pattern is Monochrome

13 Background

The 64300 / 301 supports both transparent and opaque backgrounds for monochrome patterns and font expansion:

0 = Background is Opaque (Background Color Register DR02)
1 = Background is Transparent (Unchanged)

15–14 BitBlt

The 64300 / 301 supports only its video frame buffer as the destination for BitBlt operations. The Source may be either the video frame buffer or system memory (CPU) as follows:

15	14	BitBlt Source —> Dest
0	0	Screen —> Screen (Dest)
0	1	System —> Screen (Dest)
1	0	Reserved
1	1	Reserved

18–16 Pattern Seed

Determines the starting row of the 8x8 pattern for the current BitBlt. A pattern is typically required to be destination aligned. The 64300 / 301 can determine the x-alignment from the destination address however the y-alignment must be generated by the programmer. These three bits determine which row of the pattern is output on the first line of the BitBlt. Incrementing and decrementing are controlled by bit DR04[8].

19 Solid Pattern

0 = Bitmap Pattern
1 = Solid Pattern (Brush)

20 BitBlt Status (Read Only)

0 = BitBlt Engine Idle
1 = BitBlt Active - Do not write BitBlt registers

23–21 Reserved (0)

27–24 Buffer Status

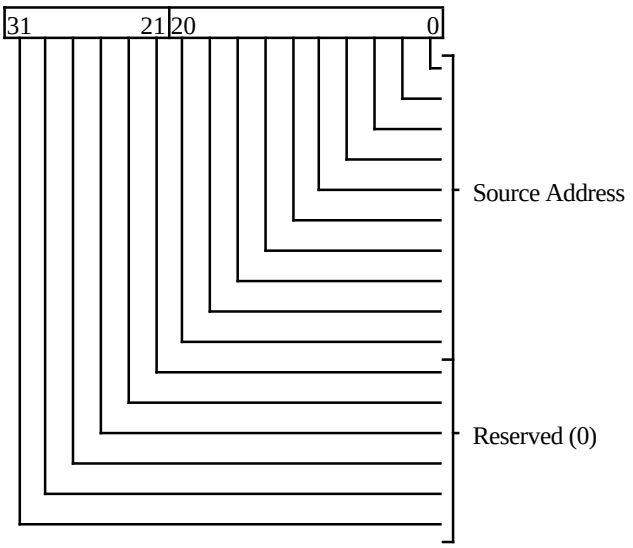
Number of DWords that can be written to the 64300 / 301.

0000	=	Buffer Full
0001	=	1 Space available in queue
0010	=	2 Spaces available in queue
.		.
.		.
.		.
.		.
1110	=	14 Spaces available in queue
1111	=	15 Spaces available in queue

31-25 Reserved (0)

BITBLT SOURCE REGISTER (DR05)

Write at I/O Address 97D0–97D3h
Read at I/O Address 97D0–97D3h
Word or DoubleWord Accessible



20–0 Source Address

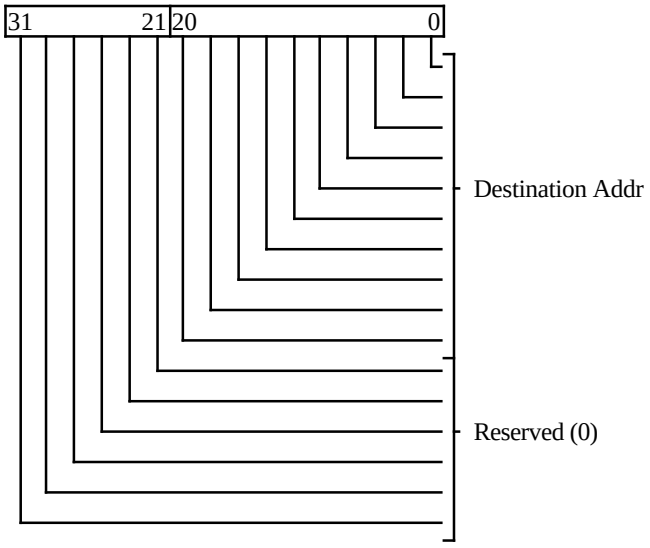
Address of Byte aligned source block.

31–21 Reserved (0)

Warning: Do not read this register while a BitBlt is active.

BITBLT DESTINATION REGISTER (DR06)

Write at I/O Address 9BD0–9BD3h
Read at I/O Address 9BD0–9BD3h
Word or DoubleWord Accessible



20–0 Destination Address

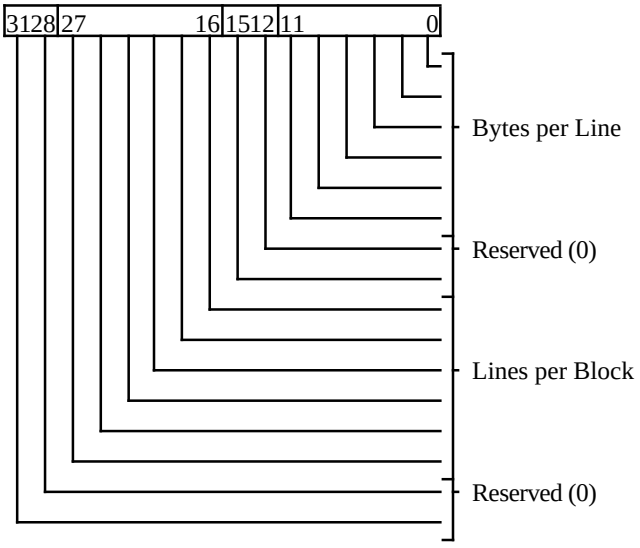
Address of Byte aligned destination block.

31–21 Reserved (0)

Warning: Do not read this register while a BitBlt is active.

BITBLT COMMAND REGISTER (DR07)

Write at I/O Address 9FD0–9FD3h
Read at I/O Address 9FD0–9FD3h
Word or DoubleWord Accessible



11–0 Bytes Per Line

Number of bytes to be transferred per line

15–12 Reserved (0)

27–16 Lines Per Block

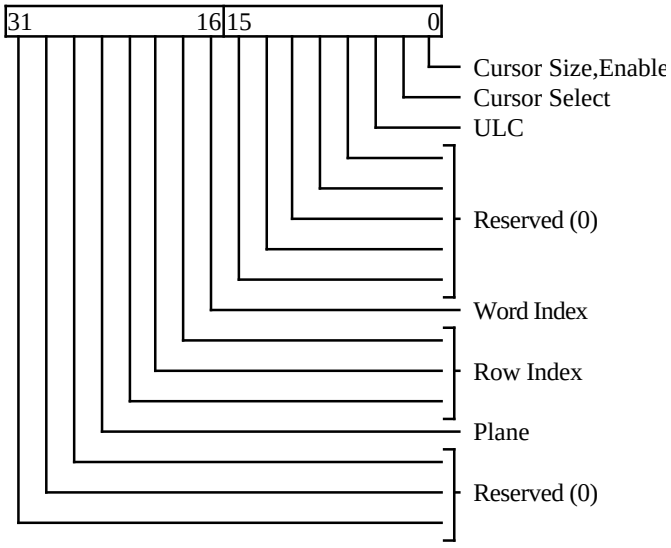
Height in lines of the block to be transferred

31–28 Reserved (0)

Warning: Do not attempt to perform a CPU read/write to display memory while a BitBlt is active.

CURSOR R/W INDEX REGISTER (DR08)

Write at I/O Address A3D0–A3D3h
Read at I/O Address A3D0–A3D3h
Word or DoubleWord Accessible



0 Cursor Enable

This bit enables the hardware cursor. The cursor will be enabled/disabled in the frame following the current active frame (synchronized to vertical sync).

0 = Cursor Disabled
1 = Cursor Enabled

1 Cursor Size 64

The 64300 / 301 supports either a single 64x64x2 cursor or four 32x32x2 cursors. This bit is synchronized to vertical sync.

0 = 32x32x2 cursor
1 = 64x64x2 cursor

3–2 Display Cursor Select

When DR08[1]=0, one of four 32x32x2 cursors may be selected. This permits caching of commonly used cursor icons. The new cursor will appear in the frame following the current active frame (cursor change is synchronized to vertical sync).

00 = display 32x32x2 cursor 0
01 = display 32x32x2 cursor 1
10 = display 32x32x2 cursor 2
11 = display 32x32x2 cursor 3

4 Reserved (0)

5 ULC

The cursor is set relative to either the Upper Left Corner (ULC) of the active display or the overscan region. When set relative to Display Enable, the cursor will not be visible in the overscan area. When relative to the active display (BLANK#) the cursor may appear in the overscan region. All x,y positioning is relative to the selected ULC.

0 = ULC is BLANK#
1 = ULC is Display Enable

6 Test (0)

15–7 Reserved (0)

17–16 Word Select

Selects a 16-bit word from the 64-bit row.

23–18 Row Select

Selects one of 64 rows. When DR8[1] = 0, DR8[23:22] selects one of four 32x32 cursors.

24 Plane

Selects between the 'AND' and 'XOR' planes.

0 AND Plane
1 XOR Plane

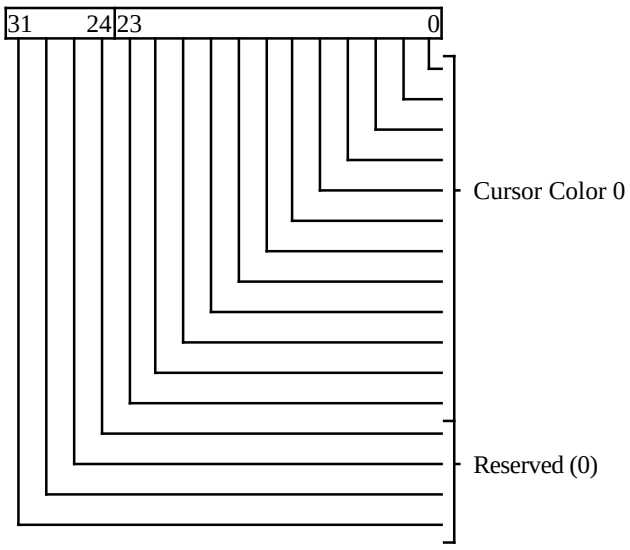
31–25 Reserved (0)

The Cursor Read/Write Index sets the internal pointer to a 16-bit word location within cursor memory. Cursor memory is mapped linearly as two consecutive 64x64x1 planes. The first plane is the 'AND' plane; the second the 'XOR' plane. The cursor RAM pointer will autoincrement when the Cursor Data Register (DR0C) is accessed. When in 32x32x2 cursor mode, DR08[23:22] chooses one of four cursors. DR08[24] always chooses between the AND and XOR planes.

When writing cursor RAM, the data is transferred first to an internal 64-bit buffer. After writing the 16-bit word at the address where DR08[17:16]=11, the entire 64-bit buffer is transferred to the cursor memory. Therefore when writing cursor memory the Word Select should begin at DR08[17:16]=00. When reading the cursor memory, any 16-bit word may be read selected by DR08[17:16].

CURSOR COLOR 0 REGISTER (DR09)

Write at I/O Address A7D0–A7D3h
Read at I/O Address A7D0–A7D3h
Word or DoubleWord Accessible



Cursor Color 0 is a 24-bit true color value consisting of 8 bits of Red, Green, and Blue. It is accessed either as two 16-bit registers or as a single 32-bit register. A write to this register immediately affects the cursor color displayed.

7–0 CC0 - Blue

Cursor Color 0 Blue value

15–8 CC0 - Green

Cursor Color 0 Green value

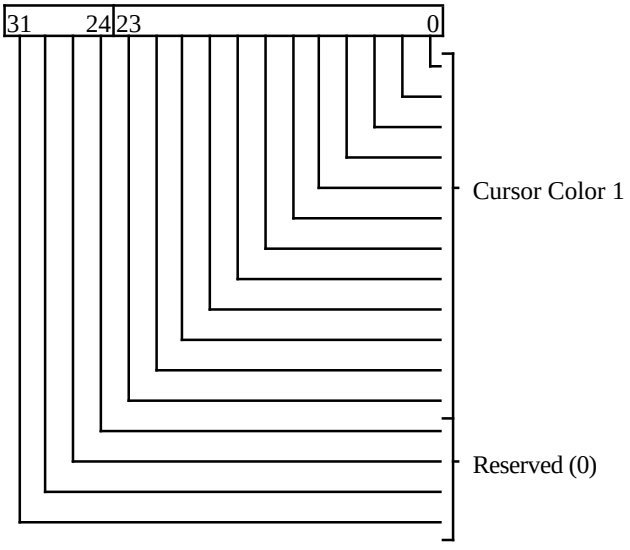
23–16 CC0 - Red

Cursor Color 0 Red value

31–24 Reserved (0)

CURSOR COLOR 1 REGISTER (DR0A)

Write at I/O Address ABD0–ABD3h
Read at I/O Address ABD0–ABD3h
Word or DoubleWord Accessible



Cursor Color 1 is a 24-bit true color value consisting of 8 bits of Red, Green, and Blue. It is accessed either as two 16-bit registers or as a single 32-bit register. A write to this register immediately affects the cursor color displayed.

7–0 CC1 - Blue

Cursor Color 1 Blue value

15–8 CC1 - Green

Cursor Color 1 Green value

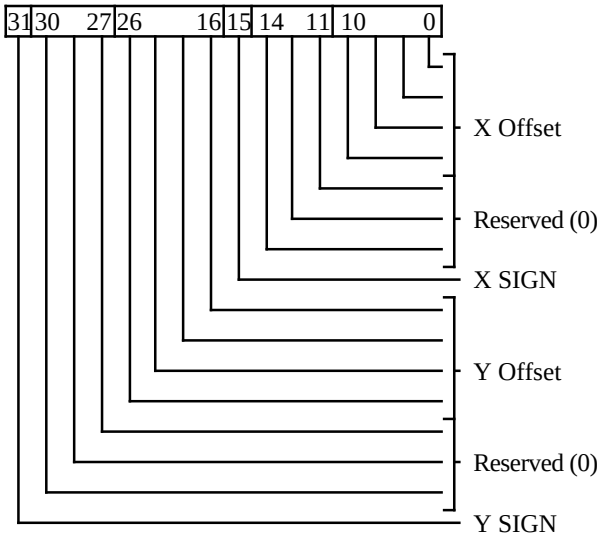
23–16 CC1 - Red

Cursor Color 1 Red value

31–24 Reserved (0)

CURSOR POSITION REGISTER (DR0B)

Write at I/O Address AFD0–AFD3h
Read at I/O Address AFD0–AFD3h
Word or DoubleWord Accessible



10–0 X Offset

Cursor X-position. The cursor position is calculated as the signed offset (in pixels) between the Upper Left Corner (ULC) of the screen (as defined by DR08[5]) and the Upper Left Corner of the cursor. X Offset is the magnitude portion of the signed offset of the cursor position in the horizontal axis. This magnitude in combination with the X SIGN bit (15) form the signed offset of the cursor in the X direction.

The X OFFSET and X SIGN may be written as a 16-bit quantity with bits 14-11 ignored.

The range for the ULC of the cursor is:

–2047 <= X-Position <= 2047

14–11 Reserved (0)

15 X Sign

Sign associated with the X OFFSET magnitude which together form the signed offset of the cursor in the X direction.

26–16 Y Offset

Cursor Y-position. The cursor position is calculated as the signed offset (in pixels) between the Upper Left Corner (ULC) of the screen (as defined by DR08[5]) and the Upper Left Corner of the cursor. Y Offset is the magnitude portion of the signed offset of the cursor position in the vertical axis. This magnitude in combination with the Y SIGN bit (31) form the signed offset of the cursor in the Y direction.

The Y OFFSET and Y SIGN may be written as a 16-bit quantity with bits 30-27 ignored.

The range for the ULC of the cursor is:

–2047 <= Y-Position <= 2047

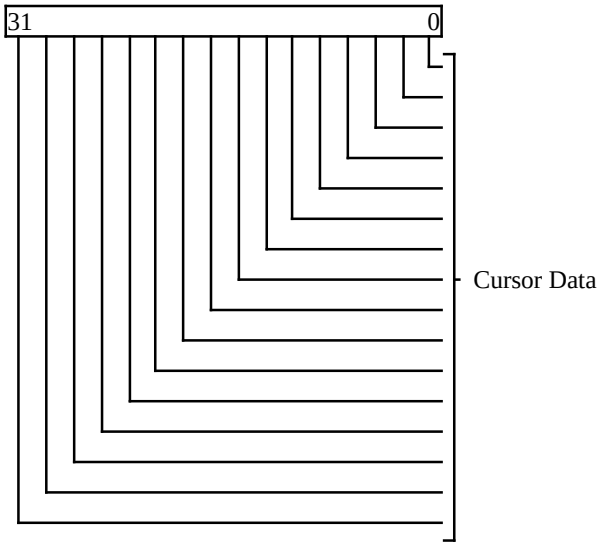
30–27 Reserved (0)

31 Y Sign

Sign associated with the Y OFFSET magnitude which together form the signed offset of the cursor in the Y direction.

CURSOR DATA REGISTER (DR0C)

Write at I/O Address B3D0–B3D3h
Read at I/O Address B3D0–B3D3h
Word or DoubleWord Accessible



31–0 Cursor Data

The cursor RAM data is accessed through this 32-bit register. The internal cursor RAM pointer is set through the Cursor R/W Index register (DR08). The Index may be set on a 16-bit boundary for word accesses. If accessing this register as a 32-bit register, always initialize the Cursor R/W Index to an even word address.

When writing the cursor RAM, all 64 bits of a row must be written with valid data. Data is transferred 64 bits at a time from a holding register to the internal cursor RAM following 16-bit writes to word index 3 or 32-bit writes to word index 2.

Any 16-bit word may be read randomly.

System Interface

Functional Blocks

The 64300 / 301 contains 5 major functional blocks including the standard VGA core (Sequencer, Attribute controller, Graphics Controller, and CRT Controller), a BitBlt engine, Hardware Cursor, Palette DAC, and Clock Synthesizer. There are also other subsystems such as the bus and memory interfaces which are transparent to both the user and software programmer. While in standard VGA modes only the VGA core, Palette DAC, and clock synthesizer are active. The 64300 / 301 is 100% register level compatible with the IBM VGA.

Bus Interface

Two major buses are directly supported by the 64300 / 301: Industry Standard Architecture (ISA), and VESA Local Bus (VL-BUS). Direct interfaces to popular 80486DX, 80486DX2, 80486SX, and 80386DX, processors are also supported. Connection to other 32-bit system buses such as EISA and Micro Channel (MC) are possible with external logic but are not inherently supported.

ISA Interface

The 64300 / 301 operates as a 16-bit slave device on the ISA bus. It maps its display memory into the standard VGA address range (0A0000-0BFFFFh). The VGA ROM is decoded in the 32K byte space 0C0000-0C7FFFh. Address lines LA23:17 are required for decoding MEMCS16# hence these addresses are latched internally by ALE. The remaining addresses (SA16:0) are accepted from the system without internal latching. The 64300 / 301 supports 16-bit memory and I/O cycles. Whenever possible the 64300 / 301 executes zero wait state memory cycles by asserting ZWS#. It does generates neither MEMCS16# nor ZWS# on ROM accesses. The memory may be mapped as a single linear frame buffer anywhere in the 16MByte ISA memory space on a 512K/1M/2MByte boundary (depending on amount of display memory installed - see XR0B[4]). The 16-bit bus extension signals MEMR# and MEMW# are used for memory control since mapping above the 1MByte boundary is permitted. For ISA compatibility the IRQ pin operates as an active high level-triggered interrupt.

VL-Bus Interface

The 64300 / 301 operates as a 32-bit target on the VL-Bus. It has an optimized direct pin-to-pin connection for all VL-Bus signals to eliminate external components. All 32 bits of address are decoded permitting location of the linear frame buffer anywhere in the available 4GByte address space. Zero wait state write cycles are supported if permitted by the High Speed Write bit (ID<2>). By definition zero wait state read accesses are not permitted, however, the 64300 / 301 will terminate a read cycle in the second T2 if the data is available. Burst cycles are not supported.

The VGA ROM is supported via the ISA bus connector. When a VL-Bus memory cycle occurs in the VGA ROM range the 64300 / 301 exerts ROMCS# to signal that the next ISA bus cycle will be an SMEMR# or SMEMW# to the ROM. The end of the cycle is monitored on the VL-Bus by the 64300 / 301 at which time it deactivates ROMCS#. This is necessary for VL-Bus add-in devices which have a ROM BIOS on the card. For motherboard VL-Bus designs it is common to integrate the VGA BIOS into the system BIOS. Leaving ROMCS# unconnected in this case causes no harm since the 64300 / 301 does not respond to the cycle with LDEV# or LRDY# in any event.

Direct Processor Interface

The 64300 / 301 can interface directly to a 32-bit processor. Its non-multiplexed 32-bit address bus makes it simple to connect to the CPU. On valid 64300 / 301 accesses it will generate LDEV# which the system logic controller should be monitoring. This interface is essentially the same as the VL-Bus interface with a few additional flavors. Both 1x and 2x CPU clocks are acceptable. When using a 2x clock the CPU Reset must be connected to the 64300 / 301 CPURESET input for phase coherency. In 16-bit interfaces the address lines and byte enables are interpreted differently as described in the pin definitions. The 64300 / 301 does not support pipelined mode in its 386 processor interface.

Display Memory Interface

Memory Architecture

The 64300 / 301 is designed to use 256K x 4 and 256K x 16 DRAMs only. Fast page mode and CAS Only Refresh features are required. The 64300 / 301 implements a 32-bit wide data bus. This bus is called the memory data bus and the pins are labelled MxDy where x = 16-bit DRAM interface (A-B) and y = bit (0-15). In 1MB/2MB interfaces, MAD7:0 corresponds to Plane 0, MAD15:8 to Plane 1, MBD7:0 to Plane 2, and MBD15:8 to Plane 3.

The 64300 / 301 can operate in planar, packed pixel, or odd/even chain modes.

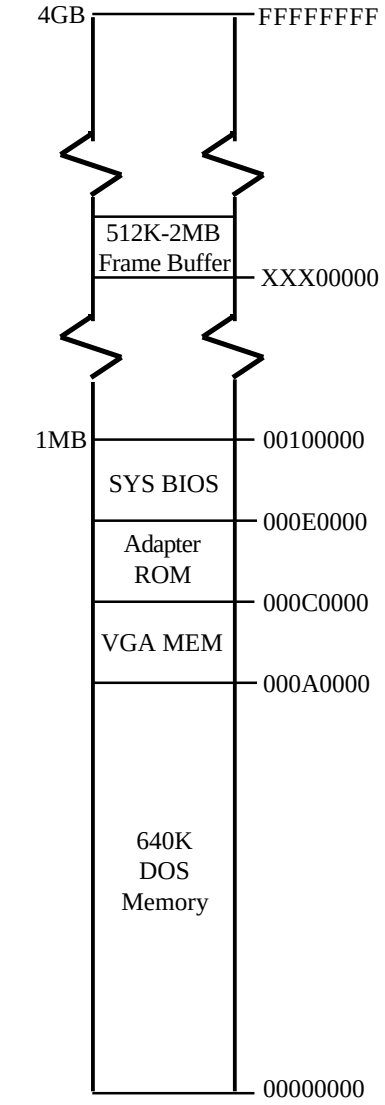
The 64300 / 301 supports 512K, 1MB, and 2MB configurations using 256Kx4 or 256Kx16 DRAMs. Both the dual-CAS# and dual-WE# types of 256Kx16 DRAMs are supported. It is possible for the BIOS to test the DRAMs to detect which flavor is being used.

The 64300 / 301 can generate Page Mode Read, Page Mode Write, Page Mode Read-Modify-Write, and CAS-Only Refresh cycles. It is optimized for 40ns page mode cycles but is flexible and can be tuned for any speed DRAM.

Configuration initialization data is latched from memory data pins MAD15:0 during reset. These bits are readable in XR01[7:0] and XR74[7:0]. Currently only XR01 contains information used to configure the 64300 / 301 hardware. XR74 is left to the user for software customization.

XRAM Accelerator (64300 only)

The 64300 supports an optional accelerator memory (one 256Kx4 DRAM for each bank of installed memory). A portion of the memory address bus is shared between the display memory and the accelerator memory. There are separate control signals for display memory and the accelerator memory.



VGA Memory Map

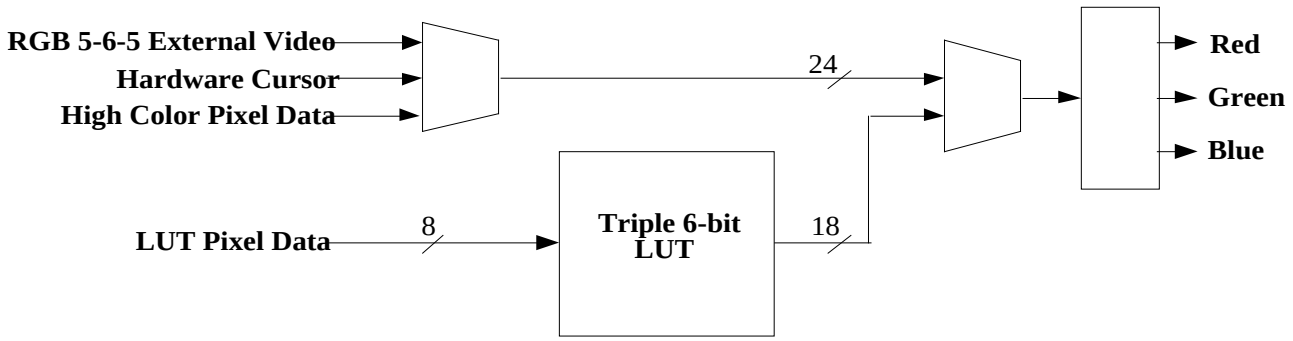
RAMDAC

The 64300 / 301 integrates a VGA compatible triple 6-bit LUT and high speed 6/8-bit DACs. Additionally the internal RAMDAC supports true color bypass modes displaying color depths of up to 24BPP (8-8-8). The palette DAC can switch between true color data and LUT data on a pixel by pixel basis. Thus, video overlays may be any arbitrary shape and can lie on any pixel boundary. The hardware cursor is also a true color bitmap which may overlay both video and graphics on any pixel boundary.

The internal palette DAC register I/O addresses and functionality are 100% compatible with the VGA standard. In all bus interfaces the palette DAC automatically controls accesses to its registers to avoid data overrun. This is accomplished by holding IOCHRDY in the ISA configuration and by delaying RDY# for VL-Bus and local bus interfaces.

For compatibility with the VL-Bus Specification (Palette Shadowing) the 64300 / 301 may be disabled from responding to palette writes (although it will perform them) so that an adapter card on a slow (ISA) bus which is shadowing the palette LUT may see the access. The 64300 / 301 must always respond to palette read accesses so it is still possible for the shadowing adapter to become out of phase with the internal modulo-3 RGB pointer. It is presumed that this will not be a problem with well-behaved software.

Extended RAMDAC display modes are selected in the Palette Control Register (XR06). Two 16BPP formats are supported: 5-5-5 Targa format and 5-6-5 XGA format. The internal RAMDAC may also be disabled/powered down via the Palette Control Register (XR06). When in power-down mode the DAC current outputs are shut off, but palette data is retained.



Internal RAMDAC Interface

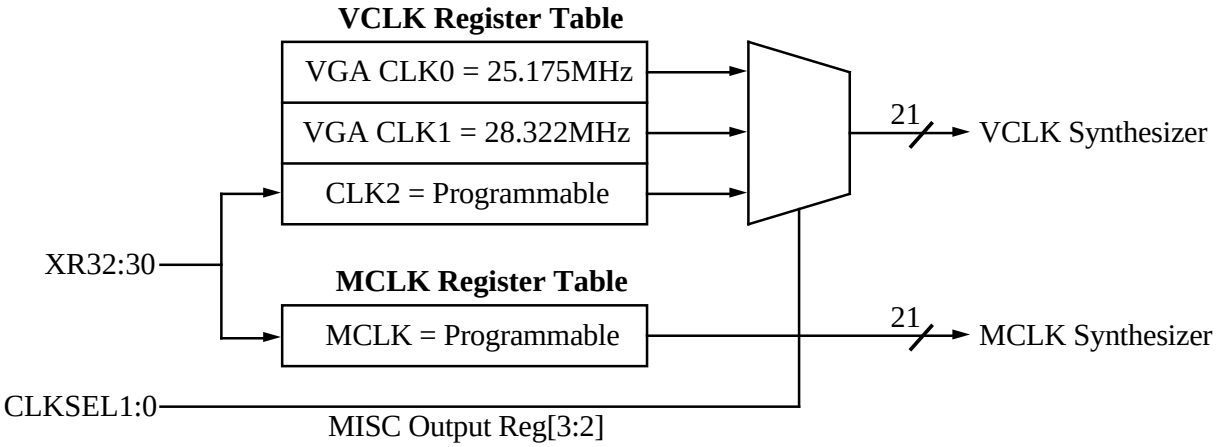
Clocks

Internal Clock Synthesizer

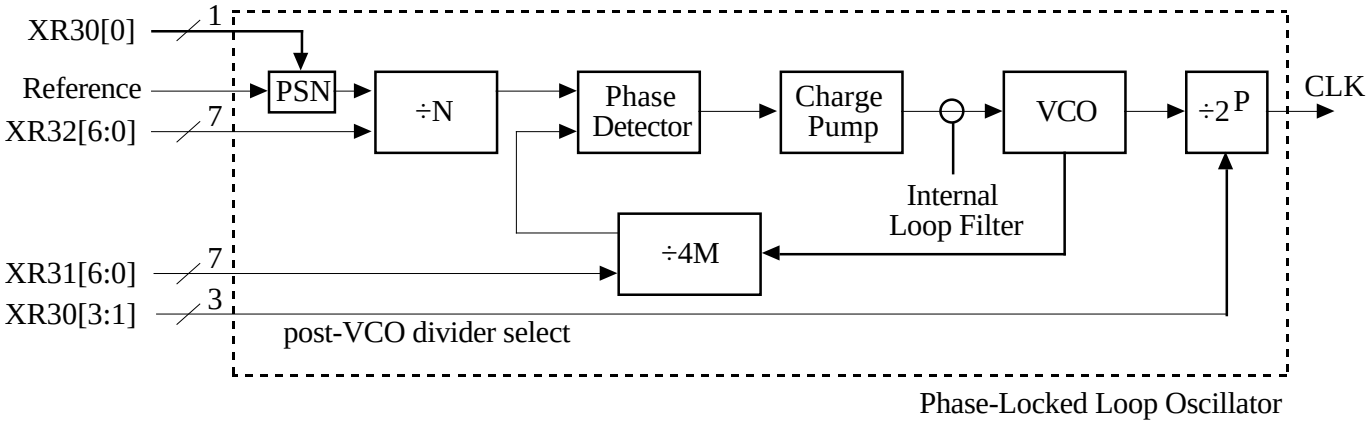
An integrated clock synthesizer supports all pixel clock (VCLK) and memory clock (MCLK) frequencies which may be required by the 64300 / 301. Each clock synthesizer may be programmed to output frequencies ranging between 1MHz and the maximum specified operating frequency for that clock in increments not exceeding 0.5%. The frequencies are generated by an 18-bit divisor word. This value contains divisor fields for the Phase Lock Loop (PLL), Voltage Controlled Oscillator (VCO) and Pre/Post Divide Control blocks. The divisor word for both synthesizers is programmable via Clock Control Registers XR30-32.

MCLK Operation

Normal operational frequencies for MCLK lie between 50MHz and 72MHz. This is defined by the display memory sequencer parameters described in the Memory Timing section. The frequency selected must also be also dependent upon the AC characteristics of the display memories connected to the 64300 / 301. A typical match is between industry standard 60ns access memories and a 72MHz MCLK. The MCLK output defaults to 60MHz on reset and is fully programmable. This initial value is conservative enough not to violate slow DRAM parameters but not so slow as to cause a system timeout on CPU accesses. The MCLK frequency must always equal or exceed the host clock (LCLK) frequency.



Clock Register Structure



Typical Clock Synthesizer Block Diagram

VCLK Operation

The VCLK output typically ranges between 19MHz and 80MHz. VCLK has a table of three frequencies from which to select a frequency. This is required for VGA compatibility. CLK0 and CLK1 are fixed at the VGA compatible frequencies of 25.175MHz and 28.322MHz respectively. These values can not be changed unlike CLK2 which is fully programmable. The active frequency is choosen by clock select bits MSR[3:2].

Programming the Clock Synthesizer

The desired output frequency is defined by an 18-bit value programmed in XR30-32. The 64300 / 301 has two programmable clock synthesizers; one for memory (MCLK) and one for video (VCLK). They are both programmed by writing the divisor values to XR30-32. The clock to be programmed is selected by the Clock Register Program Pointer XR33[5]. The output frequency of each of the clock synthesizers is based on the reference frequency (FREF) and the 4 programmed fields:

Field	# Bits	
Prescale N (PSN)	**XR30[0]**	**(÷1 or ÷4)**
M counter (M')	**XR31[6:0]**	**(M' = M - 2)**
N counter (N')	**XR32[6:0]**	**(N' = N - 2)**
Post-Divisor (P)	**XR30[3:1]**	**($\div 2^P$; $0 \le P \le 5$)**

$$F_{OUT} = \frac{F_{REF} * 4 * M}{PSN * N * 2^P}$$

The frequency of the Voltage Controlled Oscillator (FVCO) is determined by these fields as follows:

$$F_{VCO} = \frac{F_{REF} * 4 * M}{PSN * N}$$

where FREF = Reference frequency (between 4 MHz - 20 MHz; typically 14.31818 MHz)

Note: If a reference frequency other than 14.31818 MHz is used, then the frequencies loaded on RESET will not be correct.

P	Post Divisor
000	1
001	2
010	4
011	8
100	16
101	32

Programming Constraints

There are five primary programming constraints the programmer must be aware of:

$$4\ MHz \le F_{REF} \le 20\ MHz$$

$$150\ KHz \le F_{REF}/(PSN * N) \le 2\ MHz$$

$$48\ MHz < F_{VCO} \le 220\ MHz$$

$$3 \le M \le 127$$

$$3 \le N \le 127$$

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation.

The value of FVCO must remain between 48 MHz and 220 MHz inclusive. Therefore, for output frequencies below 48 MHz, FVCO must be brought into range by using the post-VCO Divisor.

To avoid crosstalk between the VCO's, the VCO frequencies should not be within 0.5% of each other nor should their harmonics be within 0.5% of the other's fundamental frequency.

The 64300 / 301 clock synthesizers will seek the new frequency as soon as it is loaded following a write to XR32. Any change in the post-divisor will take affect immediately. There is a possibility that the output may glitch during this transition of post divide values. Because of this, the programmer may wish to hold the post-divisor value constant across a range of frequencies (eg. changing MCLK from the reset value of 50MHz to 72MHz). There is also the consideration of changing from a low frequency VCO value with a post-divide ÷1 (eg. 50MHz) to a high frequency ÷4 (eg. 220MHz). Although the beginning and ending frequencies are close together, the intermediate frequencies may cause the 64300 / 301 to fail in some environments. In this example there will be a short-lived time frame during which the output frequency will be in the neighborhood of 12.5MHz. The bus interface may not function correctly if the MCLK frequency falls below a certain value. Register and memory accesses which are synchronized to MCLK may be so slow as to violate bus timing and cause a watchdog timer error. Programmers should time-out the system (CPU) for approximately 10ms after writing XR32 before accessing the VGA again. This will ensure that accesses do not occur to the VGA while the clocks are in an indeterminate state.

Note: On reset the MCLK is initialized to a 60MHz output with a post divisor = 2 (FVCO = 120MHz).

Programming Example

The following is an example of the calculations which are performed:

Derive the proper programming word for a 25.175 MHz output frequency using a 14.31818 MHz reference frequency:

Since 25.175 MHz < 48 MHz, double it to 50.350 MHz to get FVCO in its valid range. Set the post divide field (P) to 001.

Prescaling PSN = 4

The result:

FVCO = 50.350 = (14.31818 x 4 x M/4 x N)

M/N = 3.51655

Several choices for M and N are available:

M	N	FVCO	Error
109	31	50.344	-0.00300
102	29	50.360	+0.00500

Choose (M, N) = (109,31) for best accuracy.

Prescaling PSN = 1

The result:

FVCO = 50.350 = (14.31818 x 4 x M/1 x N)

M/N = 0.879127

M	N	FVCO	Error
80	91	50.349	-0.00050

FREF/(PSN x N) = 157.3KHz

Therefore M/N = 80/91 with PSN = 1 is even better than with PSN = 4.

XR30 = 0000010b (02h)
XR31 = 80 - 2 = 78 (4Eh)
XR32 = 91 - 2 = 89 (59h)

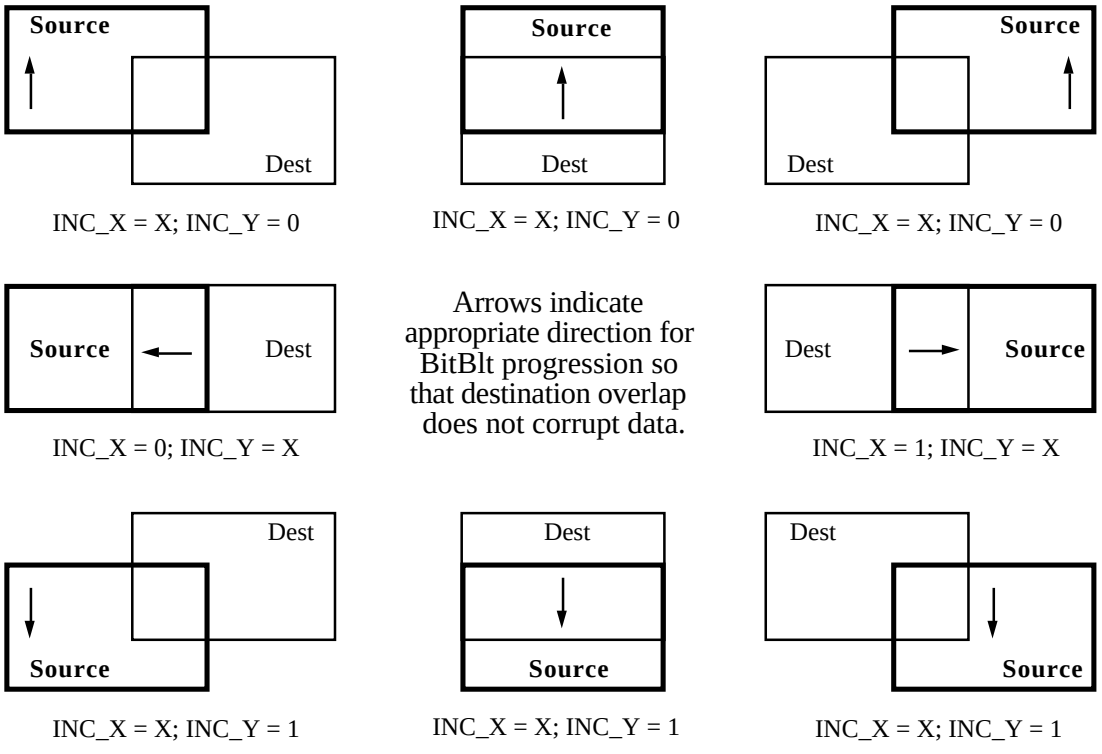
BitBlt Engine

Bit Block Transfer

The 64300 / 301 integrates a Bit Block Transfer (BitBlt) Engine which is optimized for operation in a Microsoft Windows environment. The BitBlt engine supports system-to-screen and screen-to-screen memory data transfers. It handles monochrome to color data expansion using either system or screen data sources. Color depths of 8 and 16BPP are supported in the expansion logic. Integrated with the screen and system BitBlt data streams is a 3-operand raster-op (ROP) block. This ROP block includes an independent 8x8 pixel (mono or color) pattern. Color depths of 8 and 16BPP are supported by the pattern array. All possible logical combinations of Source (system or screen data), Destination (screen data), and Pattern data are available.

The BitBlt and ROP subsystems have been architected for compatibility with the standard Microsoft Windows BitBlt parameter block. The source and destination screen widths are independently programmable. This permits expansion of a compressed off-screen bitmap transparent to the software driver. The BitBlt Control Register (DR04) uses the same raster-op format as the Microsoft Windows ROP so no translation is required. All 256 Windows defined ROPs are available.

All possible overlaps of source and destination data are handled by controlling the direction of the BitBlt in the x and y directions. As shown below there are eight possible directions for a screen-to-screen BitBlt (no change in position is a subset of all eight). Software must determine the overlap, if any, and set the INC_X and INC_Y bits accordingly. This is only critical if the source and destination actually overlap. For most BitBlts this will not be the case. In BitBlts where INC_X is a 'don't care' it should be set to 1 (proceed from left to right). This will increase the performance in some cases.



Possible BitBlt Orientations With Overlap

Sample Screen-to-Screen Transfer

Below is an example of how a screen-to-screen BitBlt operation is traditionally performed. The source and destination blocks both appear on the visible region of the screen and have the same dimensions. The BitBlt is to be a straight source copy with no raster operation. The memory address space is 2MBytes and display resolution is 1024 x 768. The size of the block to be transferred is 276 horizontal x 82 vertical pixels (114h x 52h). The coordinates of the upper left corner (ULC) of the source block is 25h,30h. The ULC coordinates of the destination block are 157h,153h. Because the source and destination blocks do not overlap, the INC_X and INC_Y BitBlt direction bits are not important. We will assume that INC_X = 1, INC_Y = 0, and the BitBlt will proceed one scan line at a time from the lower left corner of the source moving to the right and then from the bottom to the top.

The source and destination offsets are both the same as the screen width (400h):

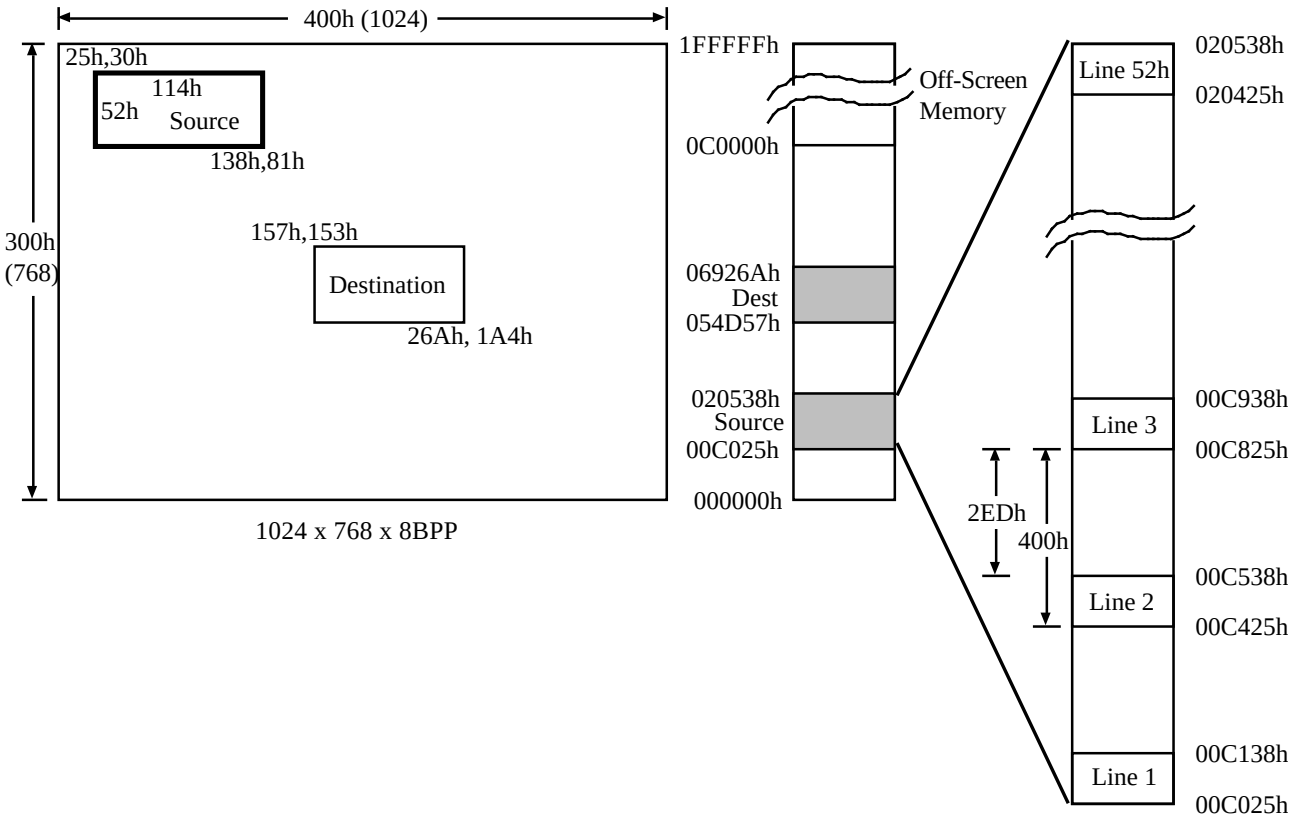
BitBlt Offset Register (DR00) = 04000400h

The Pattern ROP Register does not need to be programmed since there is no pattern involved. Neither the Foreground Color nor Background Color Register has to be programmed since this does not involve a color expansion or rectangle solid color paint. The BitBlt Control Register contains the most individual fields to be set:

ROP = Source Copy = 0CCh
INC_Y = 0 (Bottom to Top)
INC_X = 1 (Left to Right)
Source Data = Variable Data = 0
Source Depth = Source is Color = 0
Pattern Depth = Don't Care = 0
Background = Don't Care = 0
BitBlt = screen-to-screen = 00
Pattern Seed = Don't Care = 000

BitBlt Control Register (DR04) = 002CCh

Since the BitBlt will be starting in the lower left corner (LLC) of the source rectangle, the start address for the source data is calculated as:



Screen-to-Screen BitBlt

(81h * 400h) + 25h = 020425h
BitBlt Source Register (DR05) = 020425h

Similarly, the LLC of the destination register calculated as:

(1A4h * 400H) + 157h = 069157h

BitBlt Destination Register (DR06) = 069157h

To begin any BitBlt the Command Register must be written. This register contains key information about the size of the current BitBlt which must be written for all BitBlt operations:

Lines per Block = 52h
Bytes per line = 114h (Current example 8BPP)

Command Register (DR07) = 00520114h

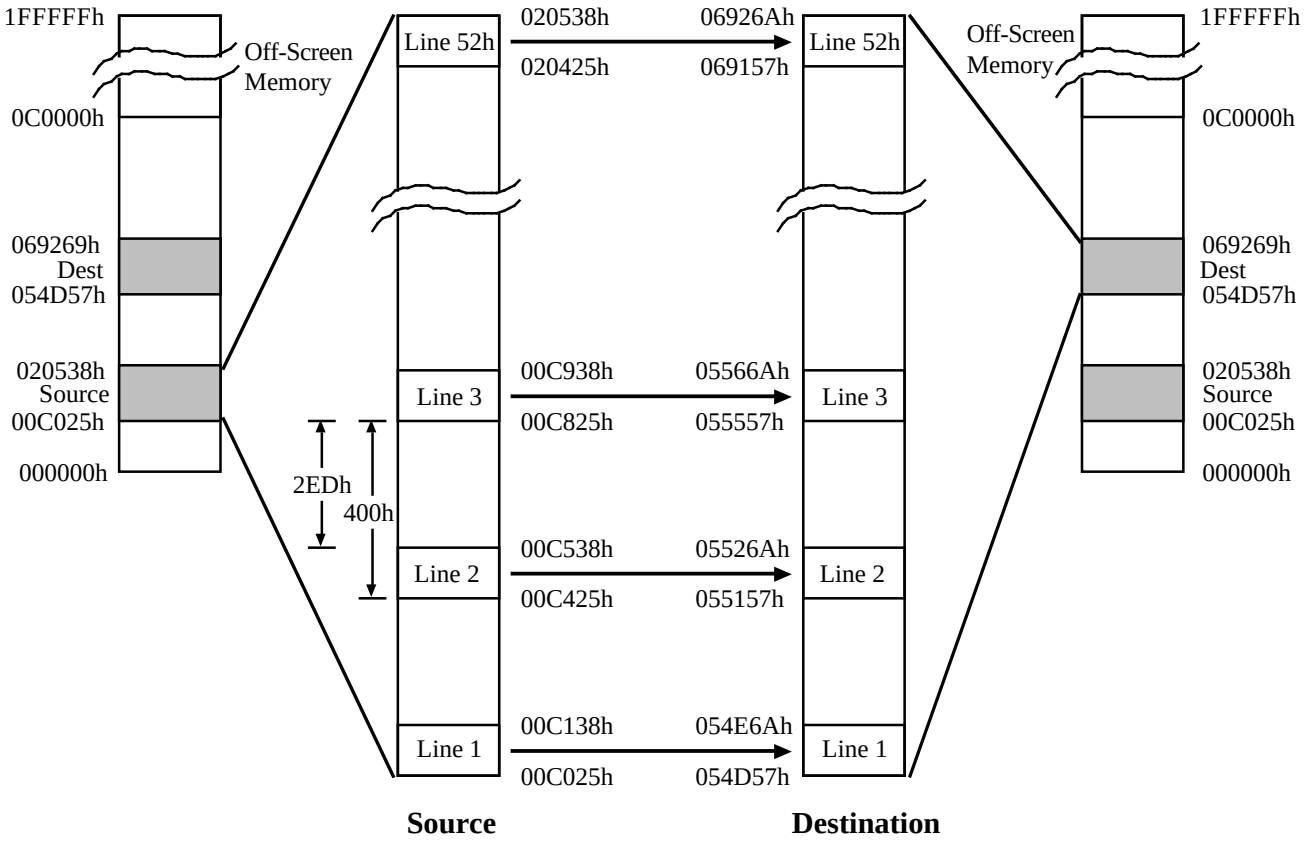
After the Command Register (XR07) is written the BitBlt engine performs the requested operation. The status of the BitBlt operation may be read in DR04[20] (read only bit). This is necessary to determine when the BitBlt is finished so that another BitBlt may be issued. No reads or writes of the display memory by the CPU are permitted while the BitBlt engine is active.

In the present example the BitBlt source and destination blocks have the same width as the display. As can be seen below each scan line is transferred from source to destination. Alignment is handled by the BitBlt engine without assistance from software.

Compressed Screen-to-Screen Transfer

Next we consider an example of how a screen-to-screen BitBlt operation is performed when the source and destination blocks have different widths (pitch). This type of BitBlt is commonly used to store bitmaps efficiently in offscreen memory or when recovering a saved bitmap from offscreen memory.

The 64300 / 301 display memory consists of a single linear frame buffer. The number of bytes per scan line and lines displayed changes with resolution and pixel depth. For simplification, the concepts of



BitBlt Data Transfer

pixels, lines, and columns are foreign to the BitBlt engine. Instead, the 64300 / 301 operates on groups of bytes (rows) which are separated by the width of the screen. The 64300 / 301 permits separation between the row lengths to be different for source and destination bitmaps. For efficient use of off-screen memory we may assume that the "width" of the screen is the same as the width of the data.

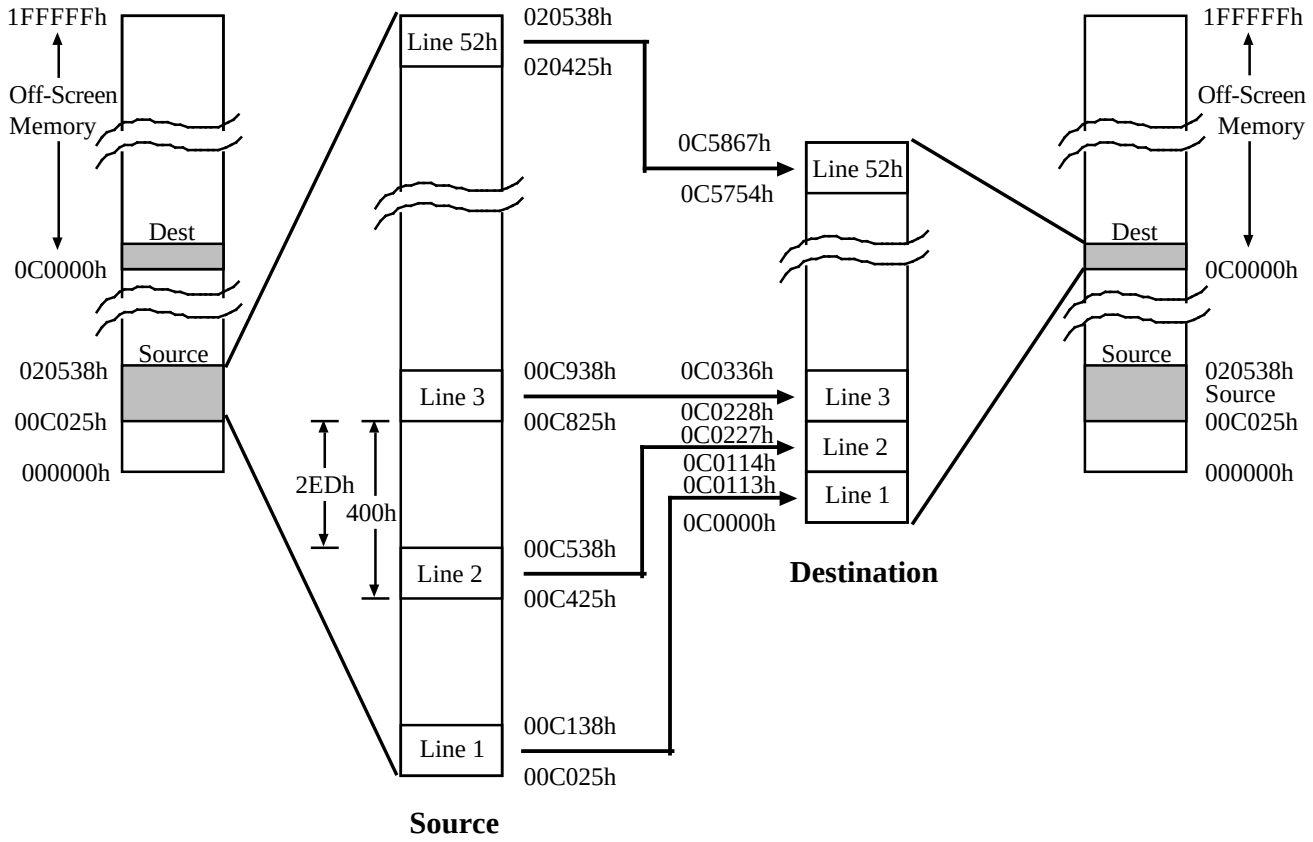
Below is an example of how a screen-to-screen BitBlt operation is performed with the destination data efficiently compressed into the offscreen area. The reverse operation is also valid to recreate the original block on the visible screen. Once again the BitBlt is to be a straight source copy with the source block in the same location as the previous example. The destination block is to be located beginning at the first byte of off-screen memory. Because the source and destination blocks do not overlap the INC_X and INC_Y BitBlt direction bits are not important. We will assume that INC_X = 1, INC_Y = 1 and the BitBlt will proceed one scan line at a time from the upper left corner of the source moving to the right and then from the top to the bottom.

The source offset is the same as the screen width (400h) and the destination offset is the same as the source block width (114h):

BitBlt Offset Register (DR00) = 01140400h

The Pattern ROP Register does not need to be programmed since there is no pattern involved. Neither the Foreground Color nor Background Color Register has to be programmed since there is no color expansion. The BitBlt Control Register contains the following bit fields:

ROP = Source Copy = 0CCh
INC_Y = 1 (Top to Bottom)
INC_X = 1 (Left to Right)
Source Data = Variable Data = 0
Source Depth = Source is Color = 0
Pattern Depth = Don't Care = 0
Background = Don't Care = 0
BitBlt = Screen --> Screen = 00
Pattern Seed = Don't Care = 000



Differential Pitch BitBlt Data Transfer

BitBlt Control Register (DR04) = 003CCh

Since the BitBlt will be beginning in the ULC of the source rectangle, the start address for the source data is calculated as:

(30h * 400h) + 25h = 0C025h
BitBlt Source Register (DR05) = 0C025h

Similarly, the ULC of the destination register calculated as (Number of scan lines * Bytes per scan line):

300h * 400h = 0C0000h

BitBlt Destination Register (DR06) = 0C0000h

As in the previous example the Command Register must be written to begin the BitBlt. This register contains the size of the current BitBlt which must be written for all BitBlt operations:

Lines per Block = 52h
Bytes per line = 114h (Current example 8BPP)

Command Register (DR07) = 00520114h

System-to-Screen BitBlts

When performing a System-to-Screen BitBlt the source rotation information is passed in the BitBlt Source Address and Source Offset registers. The 2 LSbits of the Source Address register indicate the alignment. For example if the system data resides at system address 0413456h then the processor pointer should be set to 0413454h (doubleword aligned) and the Source address register is written with xxxxx2h. When the end of the scan line is reached (the number of bytes programmed in the Command Register have been written) any remaining bytes in the last doubleword written to the 64300 / 301 are discarded. The 2 LSbits of the Source Offset Register are then added to the 2 LSbits of the Source Address Register to determine the starting byte alignment for the first doubleword of the next scanline. This process is continued until all scanlines are completed. The most common case will be a doubleword aligned bitmap in system memory in which case the 2 Lbits of the Source Address Register are zero. It is also common for bitmaps to be stored with each scanline doubleword aligned (Source Offset Register = xxxxx0h). Once the Command Register is written and the BitBlt operation has begun the 64300 / 301 will wait for data to be sent to its memory address space. Any write to a valid 64300 / 301 memory address, either in the VGA space or linear address space if enabled, will be recognized as BitBlt source data and will be routed to the correct address by the BitBlt engine. This enables the programmer to set up a destination pointer into the video address window (doubleword aligned) and simply perform a REP MOVSD. Any unused data in the last word/doubleword write will be discarded by the BitBlt Engine.

For system-to-screen monochrome (font) expansions the data is handled on a scanline by scanline basis. As with the system-to-screen Bitblt with ROP, this type of transfer uses the 2 LSbits of the source address register to determine the beginning byte index into the first doubleword. On subsequent scanlines the source offset register is added to the current scanline byte index to determine the indexing for the start of the next scan line. Monochrome data is taken from bit 7 thru bit 0, byte 0 thru 3 and expanded left to right in video memory (NOTE: monochrome source only supports left to right operation). At the end of the first scanline any remaining data in the active doubleword is flushed and the byte pointer for the starting byte in the next doubleword (for the next scanline) is calculated by adding 2 LSbits of the source offset to the starting byte position in the previous scanline. Monochrome expansion then continues bit 7 thru 0 incrementing byte (after byte 3 bit 0 a new doubleword begins at byte 0: bit 7) until the scanline is complete. Note that the number of bytes programmed into the Command register references the number of expanded bytes written; not the number of bytes to be expanded.

Hardware Cursor

Hardware Cursor

The 64300 / 301 supports either a single 64x64x2 hardware cursor or one of four 32x32x2 cursors. It supports the MS Windows AND/XOR cursor data plane structure. The hardware cursor can overlay both graphics data and live video data on a pixel by pixel basis. It may be positioned anywhere on screen resolutions up to 2048x2048 pixels. The hardware cursor is accessed through the 32-bit extension registers.

Programming

Once the 32-bit extension registers are enabled (XR03[1]=1), the cursor registers (DR08-DR0C) may be accessed. The first step is to program the cursor RAM with valid data. The cursor RAM is organized as two consecutive planes in the address space. The first plane is the "AND" plane and the second the "XOR" plane. To write a 64 x 64 cursor, the entire cursor RAM must be written. If the cursor is to be 32 x 32, then only one quarter of the cursor RAM needs to be written. The cursor RAM address must first be written to the Cursor Control Register. This is followed by a sequence of I/O writes to the Cursor Data Register (DR0C). The address is auto-incremented so that it does not need to be rewritten following each output of cursor data. After writing the entire AND plane to the cursor RAM the internal pointer automatically points to the beginning of the XOR plane (this is true for both 32x32 and 64x64 cursors). Next, the X-Y coordinates for positioning the cursor are written to the Cursor Position Register (DR0B). The cursor is then enabled through the Cursor Control Register (DR08).

To update the cursor position, perform a 32-bit write (or two 16-bit writes) to the Cursor Position Register (DR0B). This new position will take effect on the next frame (synchronized to VSYNC).

When the cursor changes shape, the 64x64 cursor should be disabled, reprogrammed as described above, and then re-enabled. When using a 32x32 cursor one of the unused cursors can be loaded with the new shape, the XY location updated for the hotspot, then the new 32x32 cursor selected as the active cursor. The 32x32 cursor select is also synchronized to VSYNC to avoid glitching of the cursor.

Application Schematic Examples

This section includes three groups of schematic examples showing various 64300 / 301 interface examples:

1) **System Bus Interface**
   - ISA Bus (Direct Bus Drive and Buffered)
   - VL Bus
2) **Display Memory Interface**
   - 2-CAS#
   - 2-WE#
3) **CRT / Video Interface**
   - 8-Bit Video Output for External Video Overlay (VGA-Style Feature Connector)
   - 16-Bit Video Input for Internal Video Overlay (PC-Video™ DK Board Interface)

All system bus interface schematics include optional BIOS circuits that support either a 32KB EPROM or 32KB Flash ROM. The 64300 / 301 may be programmed (see XR73 bit-7) to respond only to reads at C0000-C7FFFh (for EPROM support) or to both reads and writes (for flash ROM support). The ROM circuit is not required in motherboard implementations where the Graphics Controller BIOS is typically included in the system BIOS.

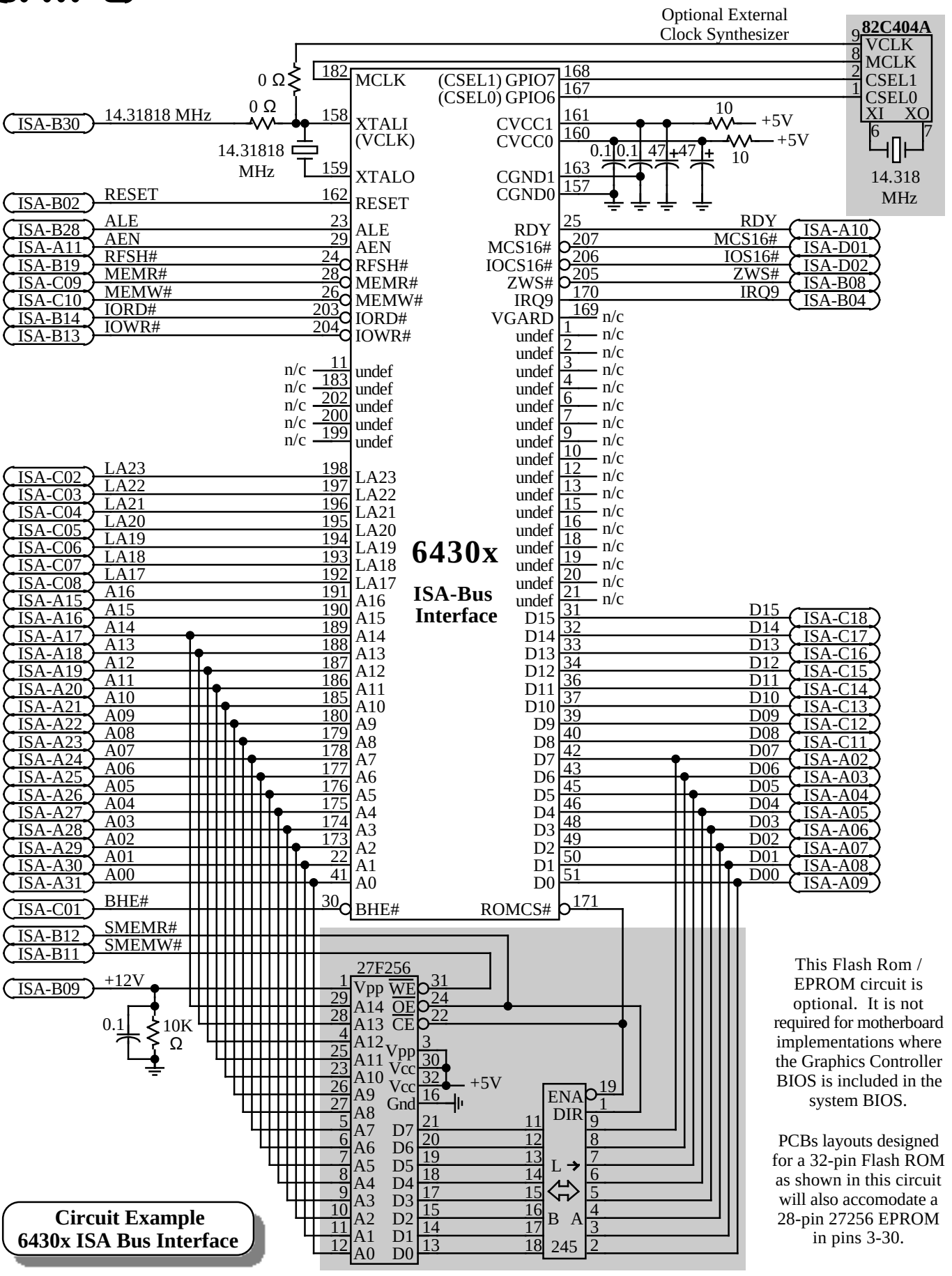
Each system bus interface schematic also includes options for a directly connected 14.31818 MHz reference crystal (configuration bit-5 pulled up with 48KΩ) or connection to the ISA bus 14.31818 MHz signal (CFG5 pulled down with 48KΩ). In either case, the internal clock may be programmed via XR33-30. Although an external clock synthesizer should not be required, the 64300 / 301 supports it. The circuits show how to design a system that allows for an external CHIPS' 82C404C synthesizer as an option should this be required. If an external clock synthesizer is used, configuration bit-4 should be pulled down; if the external clock synthesizer is not used, CFG4 should be pulled up and the 64300 / 301 MCLK pin left unconnected.

The 64300 / 301 has 12mA bus drive capability on the system data bus pins and can typically drive the ISA bus directly (a circuit is shown for this interface). However, if higher bus drive capability is required, an alternate circuit diagram is included that uses '245 transceivers on the ISA data bus. Transceivers are not required for VL bus interfacing, so only one VL bus interface circuit is shown. The 64300 / 301 bus interface may be set for VL bus by connecting CFG 0, 1, 3, 6, & 7 to +5V via 48K pullup resistors. For ISA bus, CFG0-1 must be pulled down and CFG3 & 7 pulled up (CFG6 is a don't care).

Two memory interface circuits are shown, one for use with 2-CAS / 1-WE DRAMs and another for 2-WE / 1-CAS DRAMs. The 64300 / 301 may be programmed for use with either DRAM type (see XR05) and for the number of DRAMs / banks installed (see XR04). Both circuit diagrams assume the use of DRAMs with symmetric addresses (A0-8). One circuit or another would be designed depending on the type of DRAM to be used. It is also possible to lay out a PCB to accommodate either type of DRAM through jumper options. The connections for this are not shown, but if there are any questions on how to do this, contact your local CHIPS Sales Office or Field Applications Engineer.

The 64300 is unique in having the capability to significantly increase its performance through the use of "Acceleration RAM" or "XRAM". The XRAM feature requires either one or two 256Kx4 DRAMs (one for each bank of display memory used). Both memory circuits shown indicate how to connect these optional DRAMs. The XRAM feature may be enabled / disabled via XR0A. The 64301 does not have XRAM capability.

Two CRT interface circuits are included. The CRT interface portions of both diagrams are identical. One circuit shows how to implement a "VGA Feature Connector" circuit to output 8-bit video data. This would be used to connect to existing 8-bit video overlay / capture boards. The second circuit shows an example of how to connect an external 16-bit RGB (5-6-5 format) digital video source to the 64300 / 301 for video overlay on-chip. The CHIPS' PC-Video™ Development Kit (DK) board connector pinouts are shown as an example, but this connector is not standard and is used for illustration purposes only. For possible future use (e.g., for a Display Communications Channel and/or connection to certain monitors implementing ID codes), both CRT interface circuits use GPIO pins to implement an interface to the monitor ID pins on the VGA CRT connector. If GPIO pins are needed for other functions, some or all of the ID pins may be left unconnected in most implementations.


Optional External
Clock Synthesizer
82C404A
VCLK
MCLK
CSEL1
CSEL0
XI XO
14.318 MHz
6430x
ISA-Bus Interface
MCLK
XTALI (VCLK)
XTALO
RESET
ALE
AEN
RFSH#
MEMR#
MEMW#
IORD#
IOWR#
(CSEL1) GPIO7
(CSEL0) GPIO6
CVCC1
CVCC0
CGND1
CGND0
RDY
MCS16#
IOCS16#
ZWS#
IRQ9
VGARD
ROMCS#
LA23
LA22
LA21
LA20
LA19
LA18
LA17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
BHE#
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
0 Ω
14.31818 MHz
10
+5V
0.1
47
ISA-B30
ISA-B02
ISA-B28
ISA-A11
ISA-B19
ISA-C09
ISA-C10
ISA-B14
ISA-B13
ISA-C02
ISA-C03
ISA-C04
ISA-C05
ISA-C06
ISA-C07
ISA-C08
ISA-A15
ISA-A16
ISA-A17
ISA-A18
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ISA-A21
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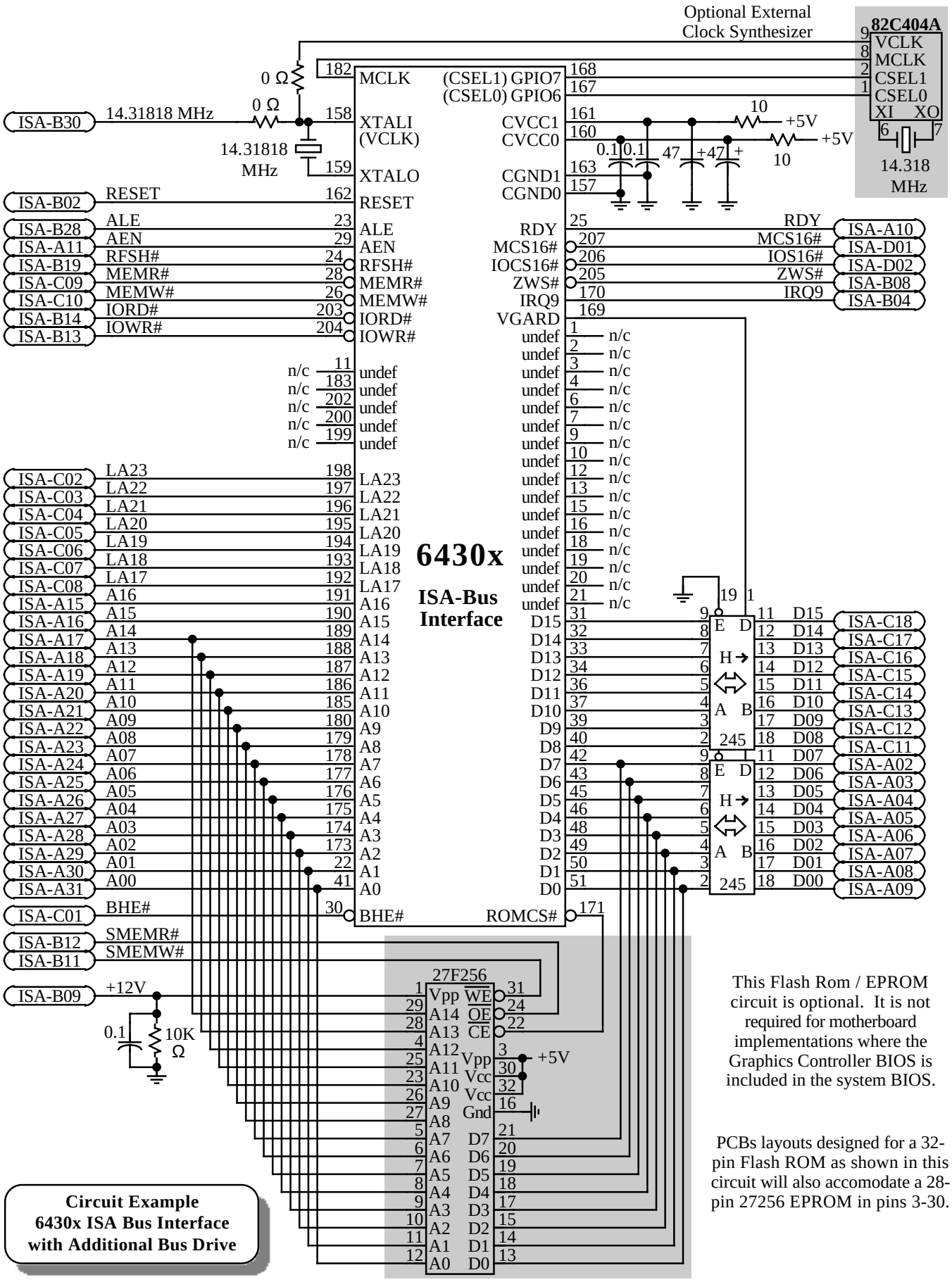
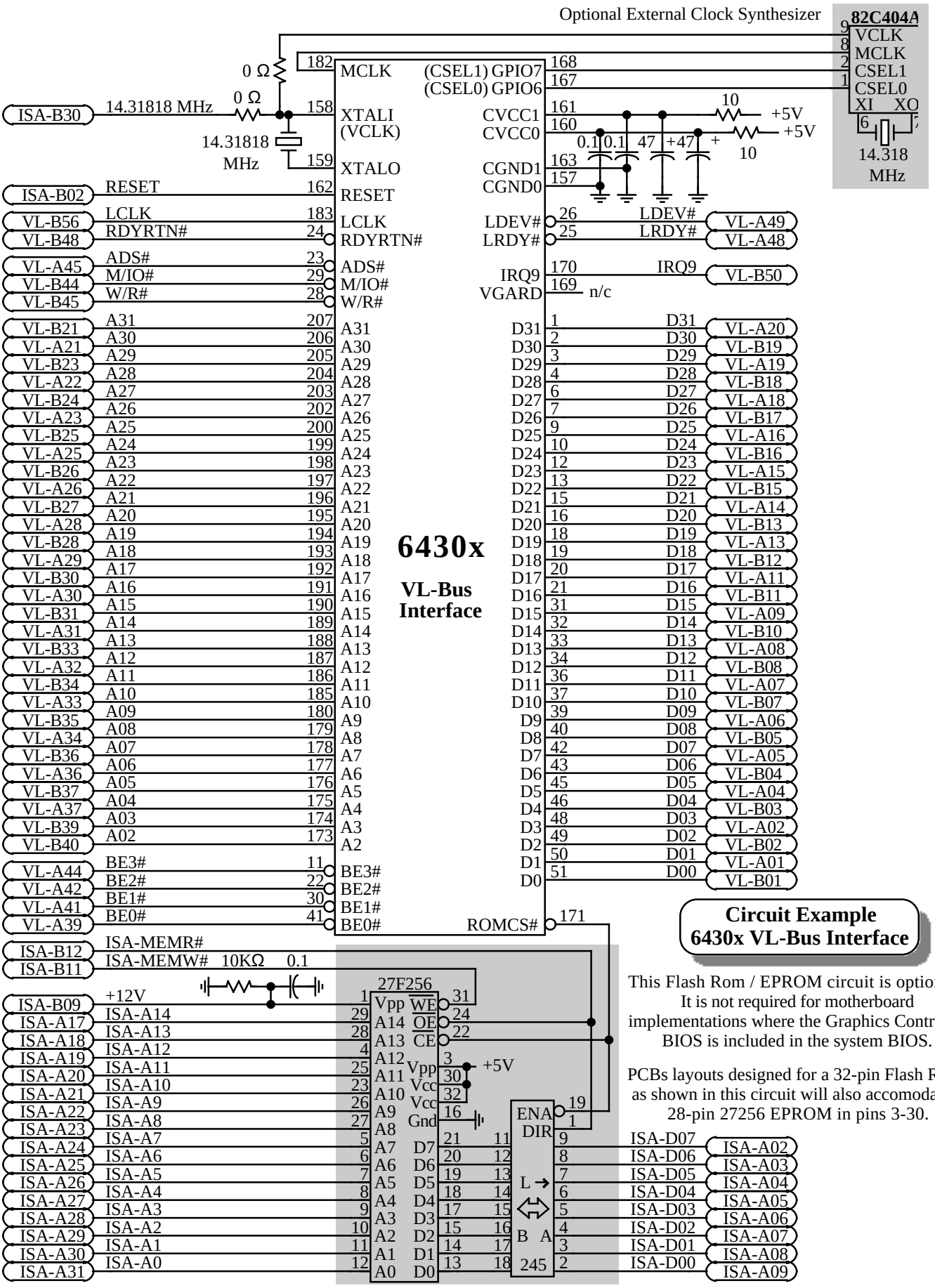
ISA-A25
ISA-A26
ISA-A27
ISA-A28
ISA-A29
ISA-A30
ISA-A31
ISA-C01
ISA-B12
ISA-B11
ISA-B09
ISA-A10
ISA-D01
ISA-D02
ISA-B08
ISA-B04
ISA-C18
ISA-C17
ISA-C16
ISA-C15
ISA-C14
ISA-C13
ISA-C12
ISA-C11
ISA-A02
ISA-A03
ISA-A04
ISA-A05
ISA-A06
ISA-A07
ISA-A08
ISA-A09
SMEMR#
SMEMW#
+12V
0.1
10K Ω
27F256
Vpp
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
WE
OE
CE
Vcc
Gnd
D7
D6
D5
D4
D3
D2
D1
D0
+5V
ENA
DIR
L
B A
245
Circuit Example
6430x ISA Bus Interface
This Flash Rom / EPROM circuit is optional. It is not required for motherboard implementations where the Graphics Controller BIOS is included in the system BIOS.
PCBs layouts designed for a 32-pin Flash ROM as shown in this circuit will also accomodate a 28-pin 27256 EPROM in pins 3-30.



Circuit Example
6430x ISA Bus Interface
with Additional Bus Drive

This Flash Rom / EPROM circuit is optional. It is not required for motherboard implementations where the Graphics Controller BIOS is included in the system BIOS.

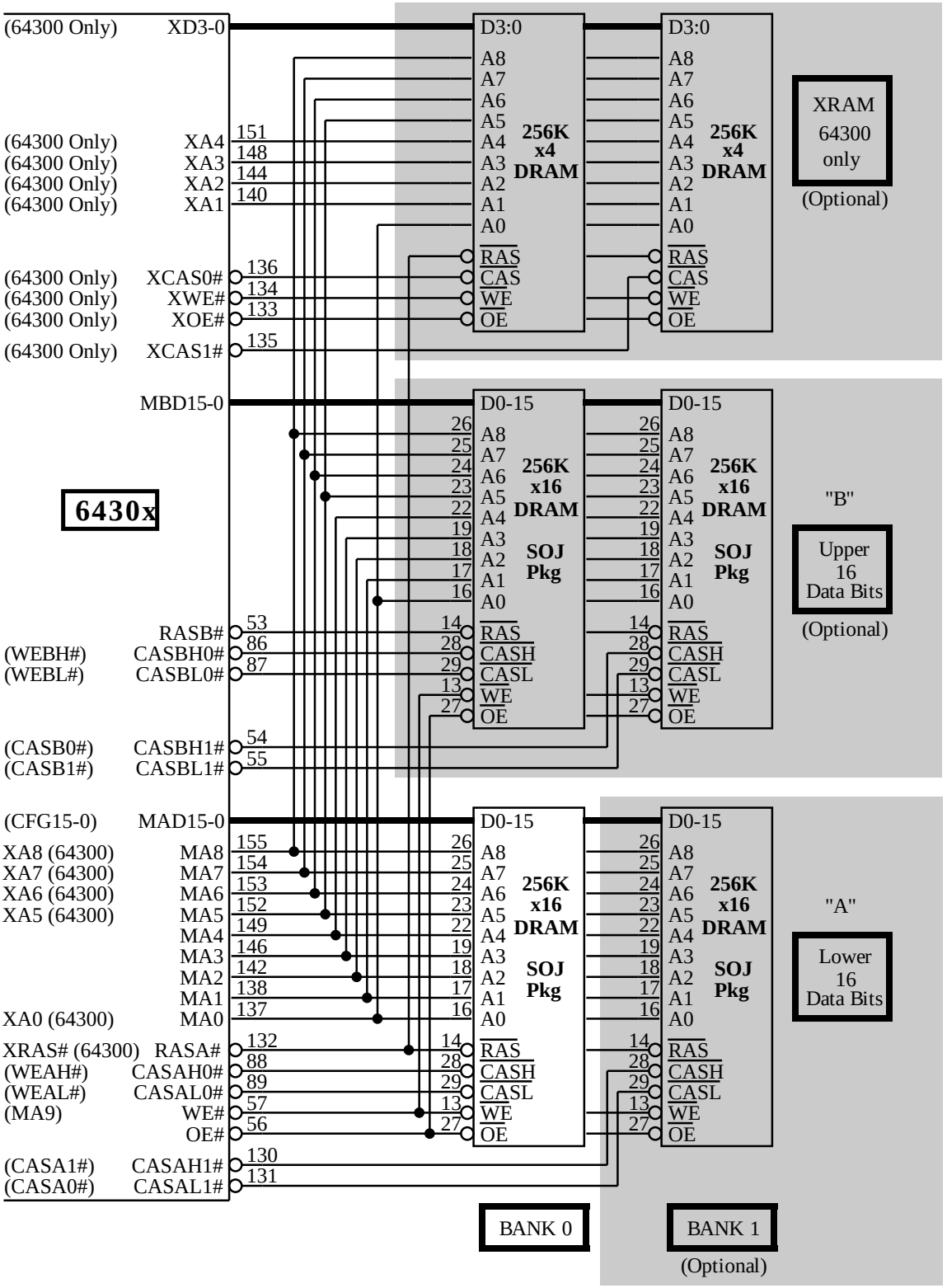
PCBs layouts designed for a 32-pin Flash ROM as shown in this circuit will also accomodate a 28-pin 27256 EPROM in pins 3-30.



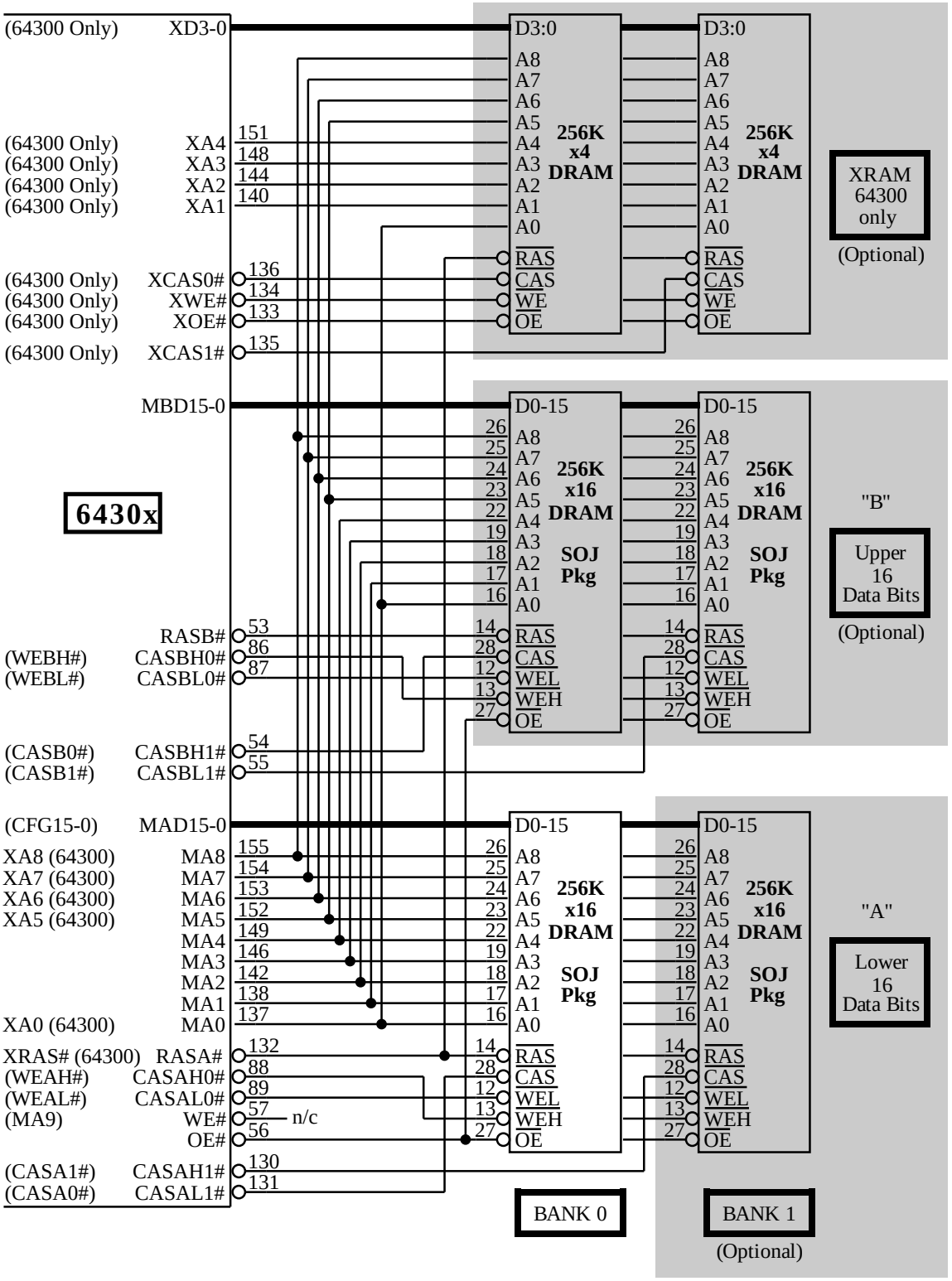
Circuit Example
6430x VL-Bus Interface

This Flash Rom / EPROM circuit is optional. It is not required for motherboard implementations where the Graphics Controller BIOS is included in the system BIOS.

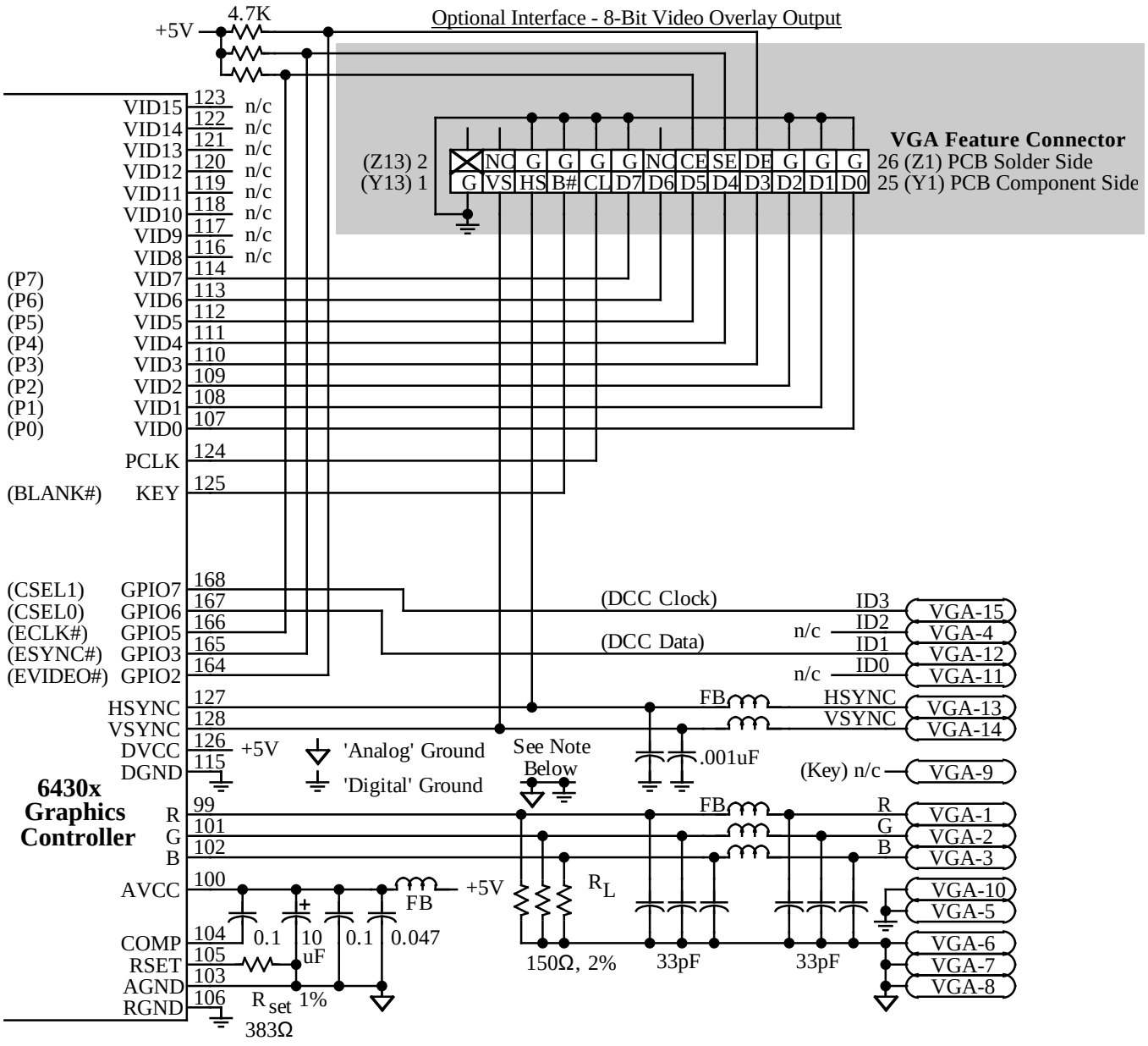
PCBs layouts designed for a 32-pin Flash ROM as shown in this circuit will also accomodate a 28-pin 27256 EPROM in pins 3-30.



Circuit Example - 6430x Display Memory 2CAS# Interface

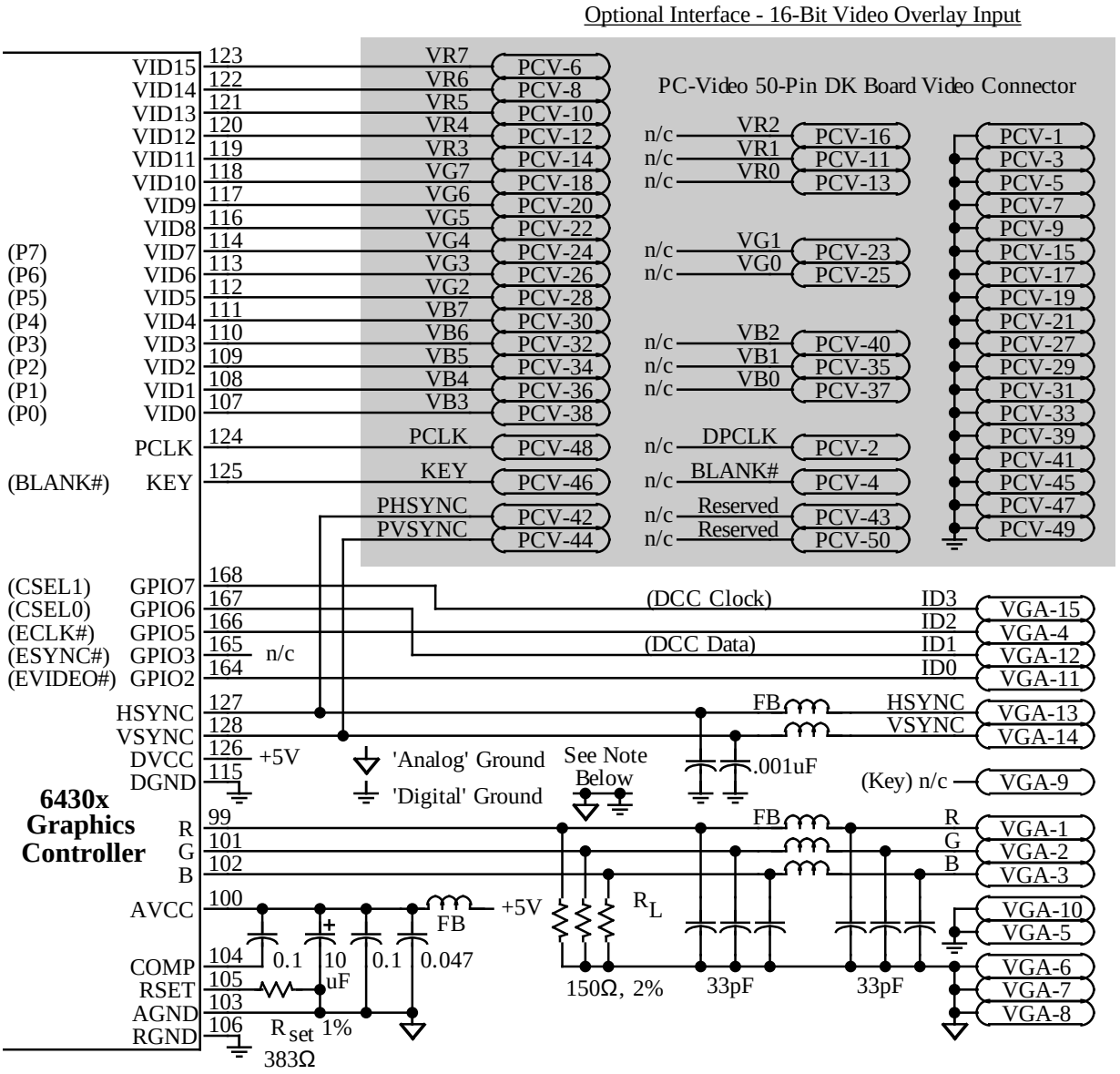


Circuit Example - 6430x Display Memory 2WE# Interface



Circuit Example - 6430x Video Interface (8-Bit Video Overlay Output)

Note: The RGB DAC uses 'analog' ground as a reference; all internal digital logic uses 'digital ground' as a reference. Connections are shown separately for information purposes only. Chips and Technologies, Inc. recommends a solid ground plane for connection of all grounds.



Circuit Example - 6430x Video Interface (16-Bit Video Overlay Input)

Note: The RGB DAC uses 'analog' ground as a reference; all internal digital logic uses 'digital ground' as a reference. Connections are shown separately for information purposes only. Chips and Technologies, Inc. recommends a solid ground plane for connection of all grounds.

Electrical Specifications

ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	1	W
V_{CC}	Supply Voltage	–0.5	–	7.0	V
V_I	Input Voltage	–0.5	–	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	–	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	–	85	°C
T_{STG}	Storage Temperature	–40	–	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage **(5V ±10%)**	4.5	5	5.5	V
T_A	Ambient Temperature	0	–	70	°C

DAC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
f_{MAX}	Clock Rate		–	–	85	MHz
	DAC-to-DAC Correlation	**See Note 1**	–	–	5	%
	DAC-to-DAC Crosstalk		–	TBD	–	dB
	Output Skew	**See Note 2**	–	–	2	ns
	Output Settling Time	**See Note 3**	–	13	–	ns
	Output Rise / Fall Time	10% to 90%	–	–	5	ns
	Comparator Sensitivity		–	50	–	mV
	Output Current	**See Note 4**				
	White referenced to Black		–	–	30	mA
	Black referenced to Blank		–	–	50	µA
	Blank Level		0	–	50	µA

Note: Monotonicity is guaranteed by design.
Unless otherwise specified, Analog Output Load = 50Ω, 30pF.
Note 1: Correlation is measured about the midpoint of the Red, Green, and Blue DAC outputs at full scale.
Note 2: Measured from the 50% point of the Red, Green, and Blue DAC outputs when switching from black level to full scale.
Note 3: Settling time is measured from 50% of the full scale transition to the output remaining within ±1 LSB of the final value.
Note 4: Measured with RSET = 383Ω, LOAD = 50Ω, ≤10pF.

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

DC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
I_{CCDE}	Power Supply Current	0°C, **5.5V**, 72 MHz MCLK	–	150	170	mA
I_{IL}	Input Leakage Current		–100	–	+100	µA
I_{OZ}	Output Leakage Current	High Impedance	–100	–	+100	µA
V_{IL}	Input Low Voltage	All input pins	–0.5	–	0.8	V
V_{IH}	Input High Voltage	All input pins except clocks	2.0	–	V_{CC}+0.5	V
		LCLK, (MCLK, VCLK if external)	2.8	–	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	Under max load per table below **(5V)**	–	–	0.5	V
V_{OH}	Output High Voltage	Under max load per table below **(5V)**	V_{CC}–0.5	–	–	V
ESR	Equivalent Series Resistance	XTAL In, XTAL Out Crystal Oscillator	–	–	100	Ω

DC DRIVE CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Output Pins	DC Test Conditions	Min	Units
I_{OL}	Output Low Drive	HSYNC, VSYNC, LRDY#, IRQ9, IOCS16#	$V_{OUT}=V_{OL}$, V_{CC}=5V	-12	mA
		MEMCS16#, ZWS#, WE#, OE#, CASxxx#	$V_{OUT}=V_{OL}$, V_{CC}=5V	-12	mA
		MA4:1, XA4:1	$V_{OUT}=V_{OL}$, V_{CC}=5V	-16	mA
		PCLK, RASx#, MA8:5, MA0, D31:0, AEN, LDEV#	$V_{OUT}=V_{OL}$, V_{CC}=5V	-8	mA
		MCLK	$V_{OUT}=V_{OL}$, V_{CC}=5V	-2	mA
		XTALO	$V_{OUT}=V_{OL}$, V_{CC}=5V	-1	mA
		All other outputs	$V_{OUT}=V_{OL}$, V_{CC}=5V	-4	mA
I_{OH}	Output High Drive	HSYNC, VSYNC, LRDY#, IRQ9, IOCS16#	$V_{OUT}=V_{OH}$, V_{CC}=5V	12	mA
		MEMCS16#, ZWS#, WE#, OE#, CASxxx#	$V_{OUT}=V_{OL}$, V_{CC}=5V	12	mA
		MA4:1, XA4:1	$V_{OUT}=V_{OL}$, V_{CC}=5V	16	mA
		PCLK, RASx#, MA8:5, MA0, D31:0, AEN, LDEV#	$V_{OUT}=V_{OL}$, V_{CC}=5V	8	mA
		MCLK	$V_{OUT}=V_{OL}$, V_{CC}=5V	2	mA
		XTALO	$V_{OUT}=V_{OL}$, V_{CC}=5V	1	mA
		All other outputs	$V_{OUT}=V_{OL}$, V_{CC}=5V	4	mA

AC TEST CONDITIONS

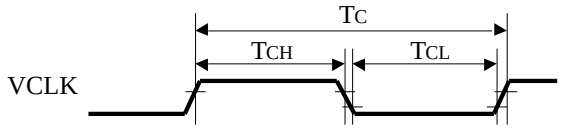
(Under Normal Operating Conditions Unless Noted Otherwise)

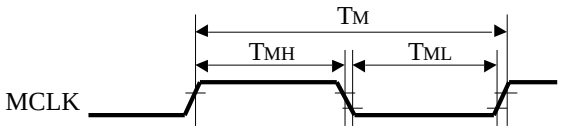
	Output	Output	Capacitive
Output Pins	**Low Voltage**	**High Voltage**	**Load**
All Outputs (except XTALO)	V_{OL}	2.4V	50pF

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

AC TIMING CHRACTERISTICS - EXTERNAL CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_C	CLK Period	65 MHz external VCLK	15.38	–	–	ns
T_{CH}	CLK High Time		$0.45T_C$	–	$0.55T_C$	ns
T_{CL}	CLK Low Time		$0.45T_C$	–	$0.55T_C$	ns
T_M	MCLK Period	65 MHz external MCLK	15.38	–	–	ns
T_{MH}	MCLK High Time		$0.45T_M$	–	$0.55T_M$	ns
T_{ML}	MCLK Low Time		$0.45T_M$	–	$0.55T_M$	ns
T_{RF}	Clock Rise / Fall		–	–	4	ns
T_{REF}	Reference Clock Period	Reference clock for internal synthesizer	50	69.8	100	ns

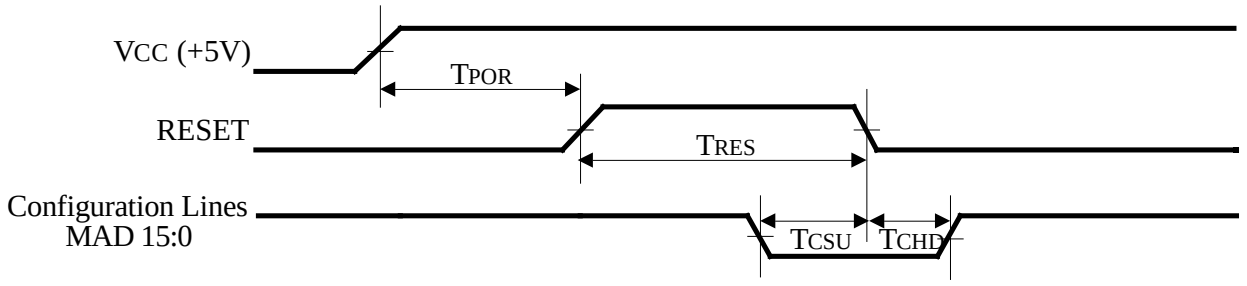




External Clock Timing

AC TIMING CHARACTERISTICS - RESET TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
TRES	RESET Pulse Width		64TM	–	–	ns
TCSU	Configuration setup time		20	–	–	ns
TCHD	Configuration hold time		5	–	–	ns
TPOR	Power on to RESET active delay		–	–	1	s



Reset Timing

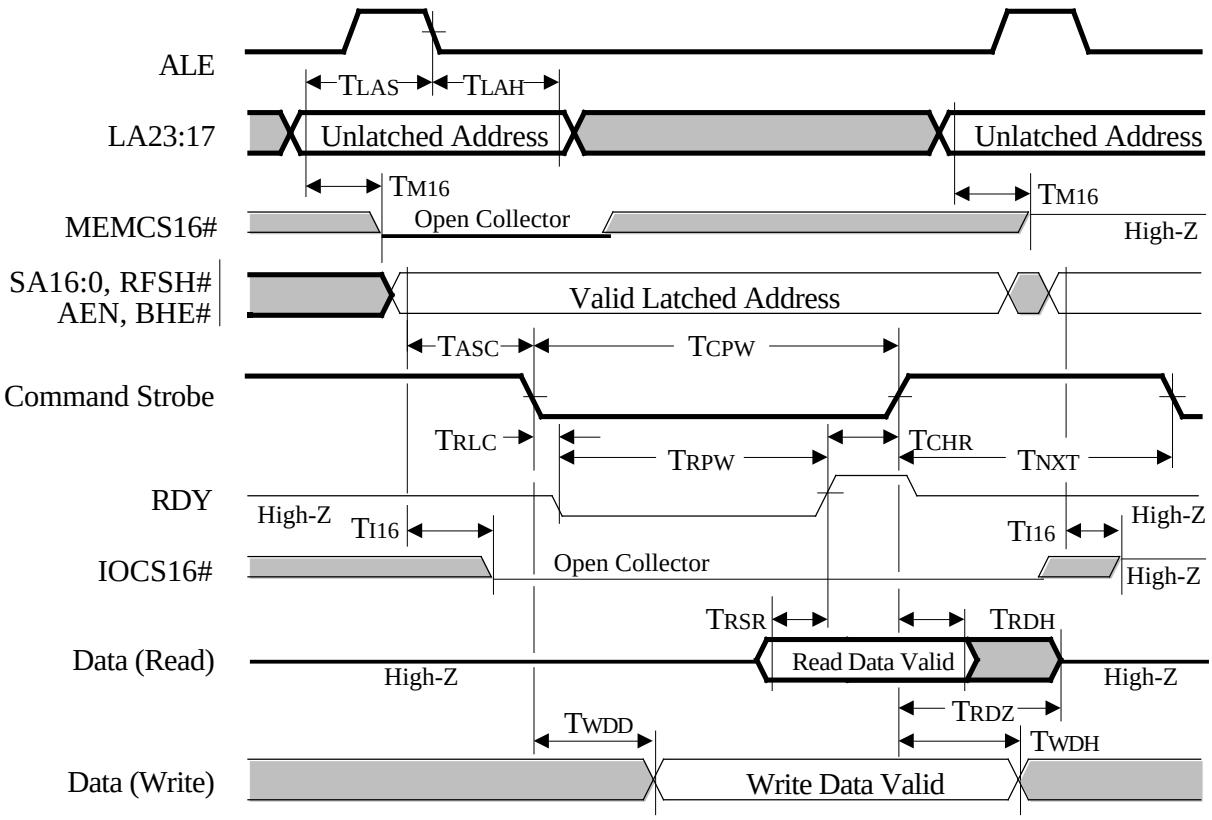
Note: Electrical specifications contained herein are preliminary and subject to change without notice.

AC TIMING CHARACTERISTICS - ISA BUS TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{ASC}	Address Setup to Command Strobe		30	–	–	ns
T_{LAS}	LA Address Setup to ALE Inactive		10	–	–	ns
T_{LAH}	LA Address Hold from ALE Inactive		10	–	–	ns
T_{CPW}	Command Strobe Pulse Width		60	–	–	ns
T_{CHR}	Command Strobe Hold from RDY high		30	–	–	ns
T_{NXT}	Command Strobe Inactive to Next Strobe	**See Note 1**	$3T_M$	–	–	ns
T_{M16}	MEMCS16# Delay from valid unlatched address		–	–	20	ns
T_{I16}	IOCS16# Delay from valid address		–	–	20	ns
T_{RLC}	RDY Active Low Delay from Command Strobe		–	–	30	ns
T_{RPW}	RDY Pulse Width		0	–	$100T_M$	ns
T_{RSR}	Read Data Setup to Ready		-25	–	–	ns
T_{RDH}	Read Data Hold from Command Strobe Inactive		10	–	–	ns
T_{RDZ}	Read Data Tristate from Command Strobe Inactive		–	–	40	ns
T_{WDD}	Write Data Delay from Command Strobe Active		–	–	T_{CPW}-15	ns
T_{WDH}	Write Data Hold from Command Strobe Inactive		10	–	–	ns

Note 1: This becomes $6T_M$ if host clock=MCLK/2. See XR01[3].

Note: Electrical specifications contained herein are preliminary and subject to change without notice.



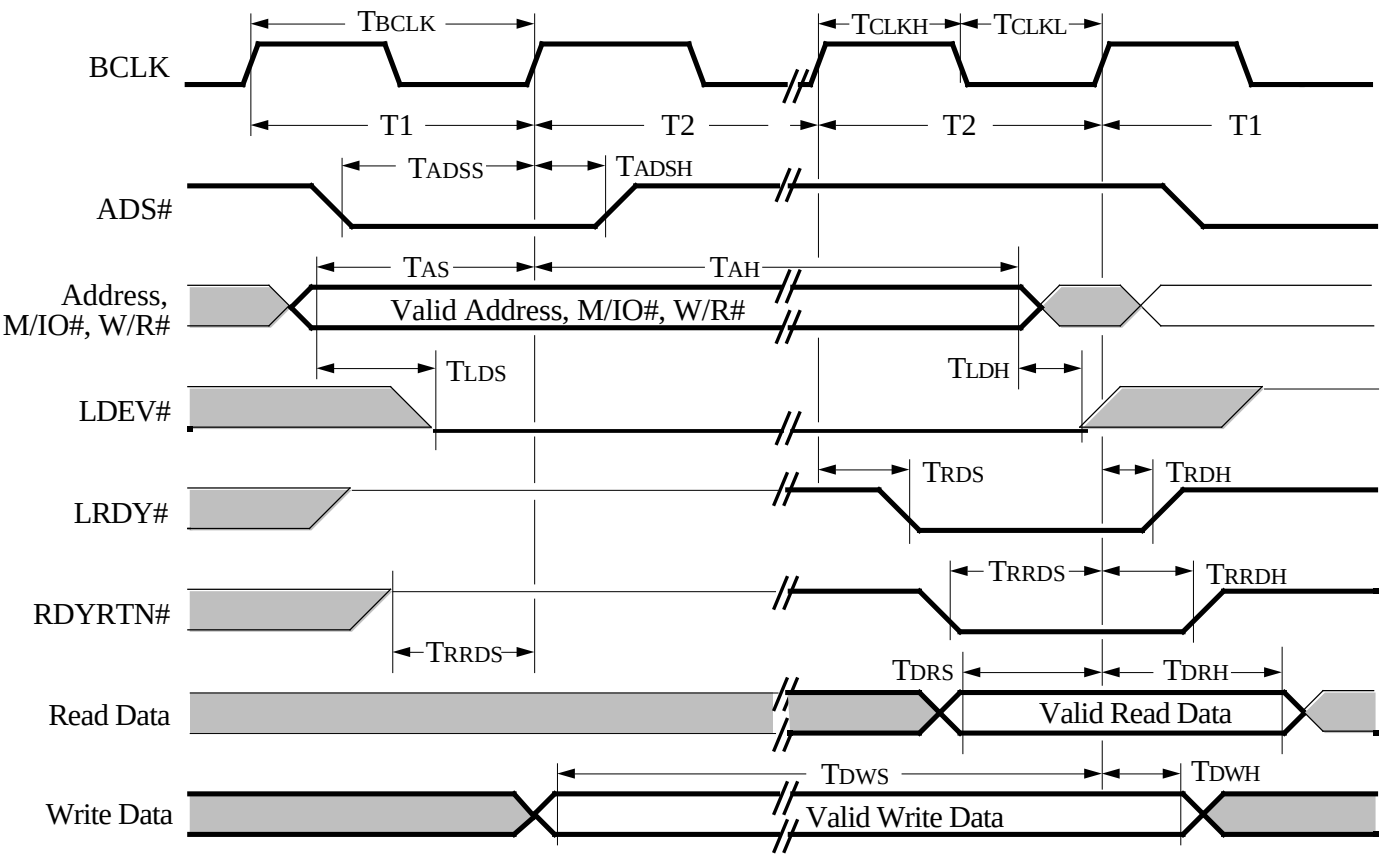
ISA Bus Cycle Timing

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

DC TIMING CHARACTERISTICS - 486 LOCAL BUS TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{BCLK}	Local Bus Clock Cycle Time	50MHz	20			ns
T_{CLKL}	Local Bus Clock Low Time	Duty Cycle 45/55	9	10	11	ns
T_{CLKH}	Local Bus Clock High Time	Duty Cycle 45/55	9	10	11	ns
T_{LDS}	Delay from Address Valid to LDEV#		0	–	20	ns
T_{LDH}	LDEV# Inactive from Address Not Valid		0	–	20	ns
T_{ADSS}	ADS# Setup to BCLK rising edge		4	–	–	ns
T_{ADSH}	ADS# Hold from BCLK rising edge		5	–	–	ns
T_{AS}	Address, M/IO#, R/W# Setup to End of T1		4	–	–	ns
T_{AH}	Address, M/IO#, R/W# Hold from End of T1		T_{CLKH}+8	–	–	ns
T_{RDS}	LRDY# Setup Time from Start of final T2		18	–	–	ns
T_{RDH}	LRDY# Hold Time from End of T2		0	–	15	ns
T_{RRDS}	RDYRTN# Setup Time to End of final T2		18	–	–	ns
T_{RRDH}	RDYRTN# Hold Time from End of final T2		0	–	15	ns
T_{DRS}	Read Data Setup Time to End of final T2		18	–	–	ns
T_{DRH}	Read Data hold Time from End of final T2		0	–	15	ns
T_{DWS}	Write Data Setup Time to End of first T2		18	–	–	ns
T_{DWH}	Write Data hold Time from End of final T2		0	–	15	ns

Note: Electrical specifications contained herein are preliminary and subject to change without notice.



64300 / 301 VL Bus (486 Local Bus) Timing

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

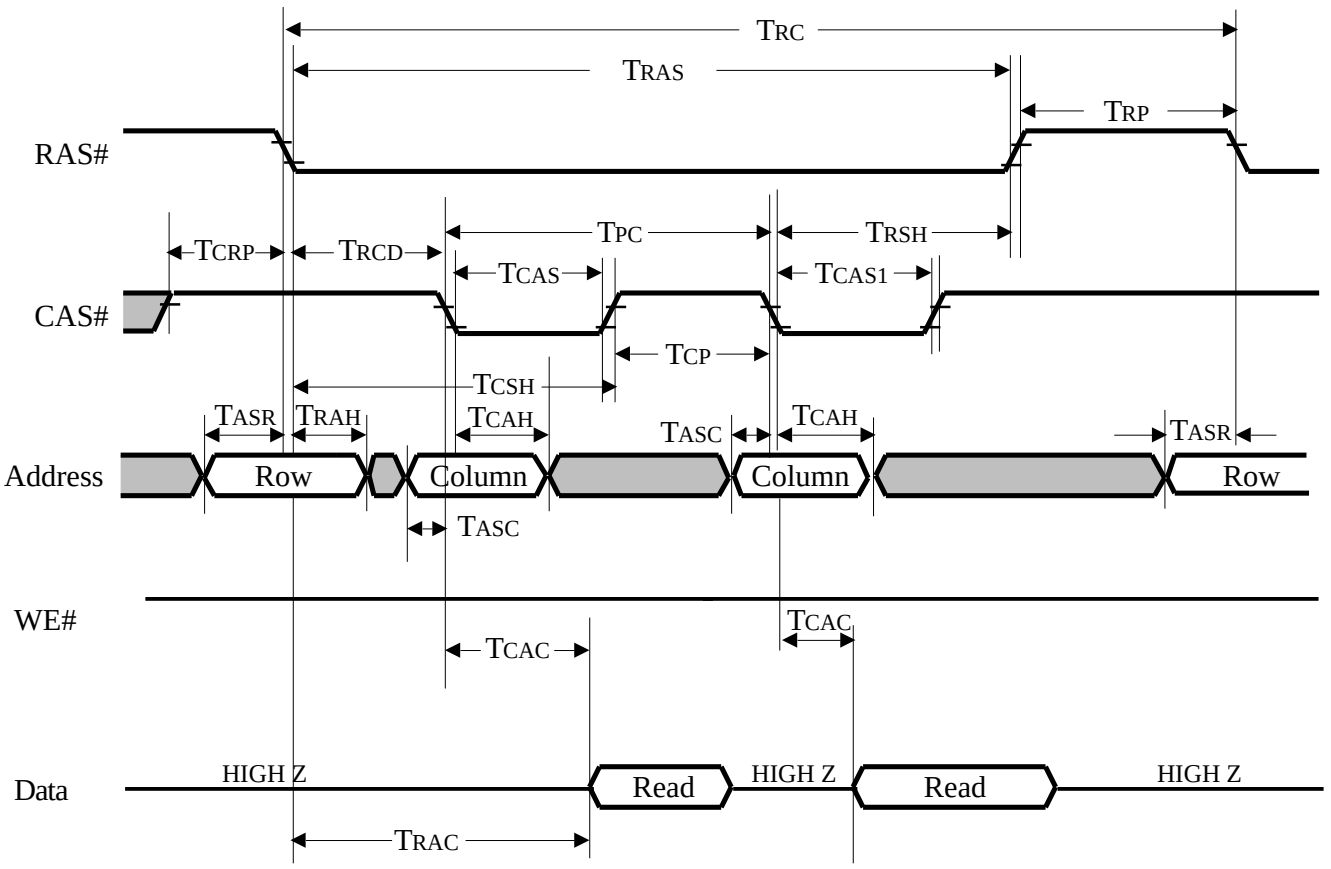
AC TIMING CHARACTERISTICS - DRAM READ/WRITE TIMING

				MCLK Frequency (MHz)			
				72.0	**64.3**	**52.9**	
				DRAM Access Time			
Symbol	**Parameter**	**Min**	**Max**	**-6**	**-7**	**-8**	**Units**
T_{RC}	Read/Write Cycle Time	$9T_M$-5	–	**120.0**	135.1	165.1	ns
T_{RAS}	RAS# Pulse Width (Min)	$5T_M$-5	**See Note 1**	64.4	72.8	89.5	ns
T_{RP}	RAS# Precharge	$4T_M$-5	–	50.6	57.3	70.6	ns
T_{CRP}	CAS# to RAS# precharge	$4T_M$-7	–	48.6	55.3	68.6	ns
TCSH	CAS# Hold from RAS#	$5T_M$-5	–	63.4	72.8	88.5	ns
T_{RCD}	RAS# to CAS# delay	$3T_M$-5		36.7	41.7	51.7	ns
			$3T_M$+5	46.7	51.7	61.7	ns
T_{RSH}	RAS# Hold from CAS#	$2T_M$-5	–	22.8	26.1	32.8	ns
T_{CP}	CAS# Precharge	T_M-3.9	–	**10.0**	11.7	15.0	ns
T_{CAS}	CAS# Pulse Width	$2T_M$-5	–	22.8	26.1	32.8	ns
T_{WP}	WE# Pulse Width	$2T_M$-5	–	22.8	26.1	32.8	ns
T_{CAS1}	CAS# Pulse Width (Fast Page Cycle)	$2T_M$-5	–	22.8	26.1	32.8	ns
T_{ASR}	Row Address Setup to RAS#	$(3T_M/2)$-15	–	5.8	8.3	13.4	ns
TASC	Column Address Setup to CAS#	$(3T_M/2)$-15	–	5.8	8.3	13.4	ns
T_{RAH}	Row Address Hold from RAS#	T_M-3.9	–	**10.0**	11.7	15.0	ns
T_{CAH}	Column Address Hold from CAS#	$(3T_M/2)$-5.8	–	**15.0**	17.5	22.6	ns
T_{CAC}	Data Access Time from CAS#	–	$2T_M$-7.8	**20.0**	23.3	30.0	ns
T_{AA}	Data Access Time from Column Address	–	$3T_M$-11.7	**30.0**	**35.0**	**45.0**	ns
T_{RAC}	Data Access time from RAS#	–	$5T_M$-5	64.4	72.8	89.5	ns
T_{DS}	Write Data Setup to CAS#	T_M-7	–	6.9	8.6	11.9	ns
T_{DH}	Write Data Hold from CAS#	$(3T_M/2)$-5.8	–	**15.0**	17.5	22.6	ns
T_{DS}	Write Data Setup to WE#	T_M-7	–	6.9	8.6	11.9	ns
T_{DH}	Write Data Hold from WE#	$(3T_M/2)$-5.8	–	**15.0**	17.5	22.6	ns
TPC	CAS# Cycle Time	$3T_M$-1.7	–	**40.0**	**45.0**	55.0	ns

Note: Parameters printed in **bold** are the limiting cases for industry standard DRAM specifications.

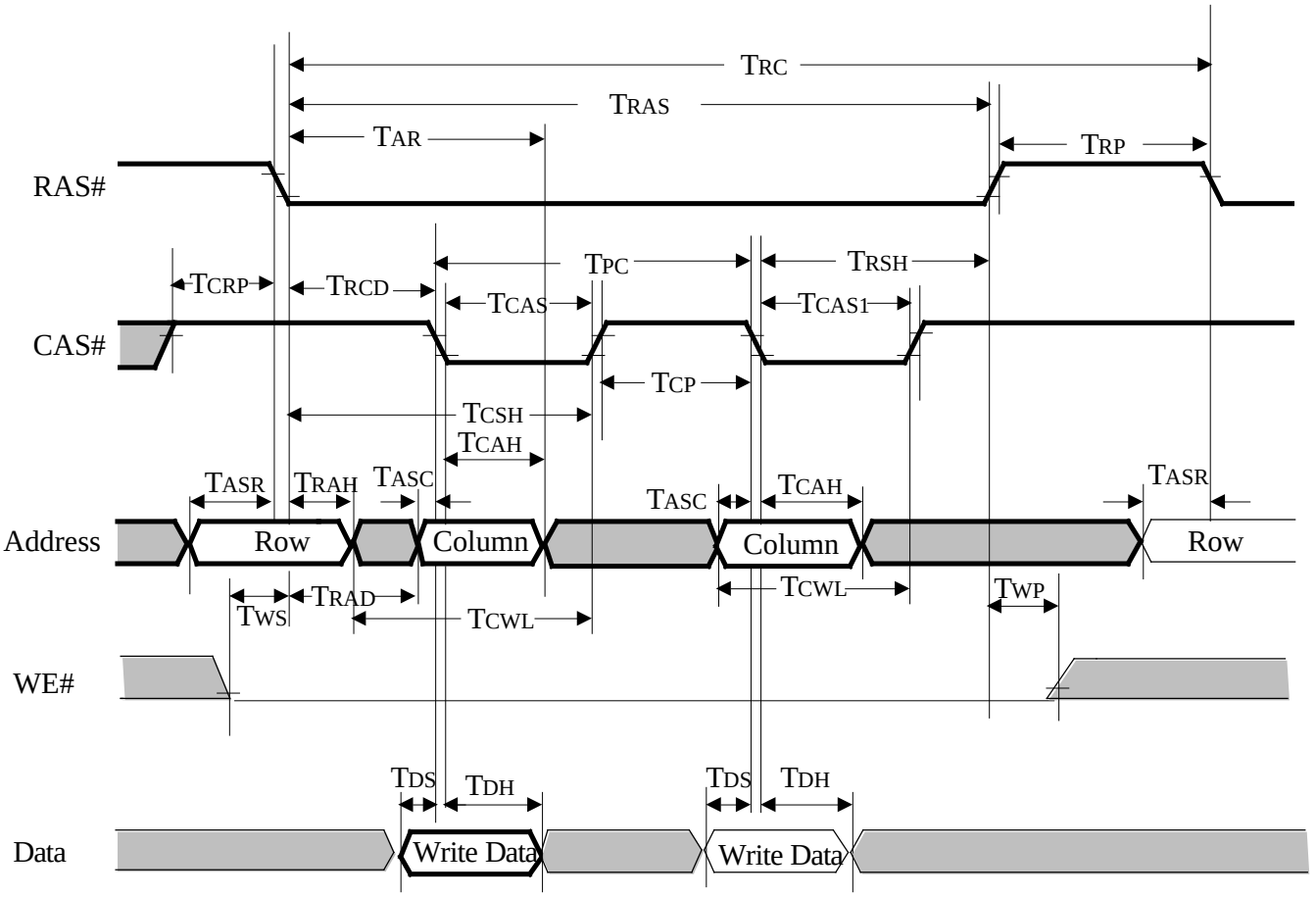
Note 1: Maximum RAS pulse width may be as high as 2+(256*3) memory clock cycles = $770T_M$ if the BitBlt Engine is given full memory bandwidth. This depends on other events which have higher priority including refresh cycles and display update.

Note: Electrical specifications contained herein are preliminary and subject to change without notice.



DRAM Page Mode Read Cycle Timing

Note: The above diagram represents a typical page mode read cycle. The number of actual CAS cycles may vary.

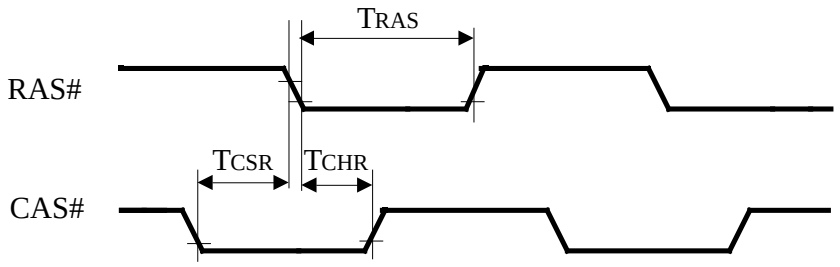


DRAM Page Mode Write Cycle Timing

Note: The above diagram represents a typical page mode write cycle.

AC TIMING CHARACTERISTICS - REFRESH TIMING

				MCLK Frequency (MHz)			
				72.0	64.3	52.9	
				DRAM Access Time			
Symbol	**Parameter**	**Min**	**Max**	**–6**	**–7**	**–8**	**Units**
T_{CHR}	RAS to CAS delay	$5T_M$–6	–	63.4	71.8	88.5	ns
T_{CSR}	CAS to RAS delay	$2T_M$–7.5	–	20.3	23.6	30.3	ns
TRAS	RAS pulse width	$5T_M$–5	–	64.4	72.8	89.5	ns



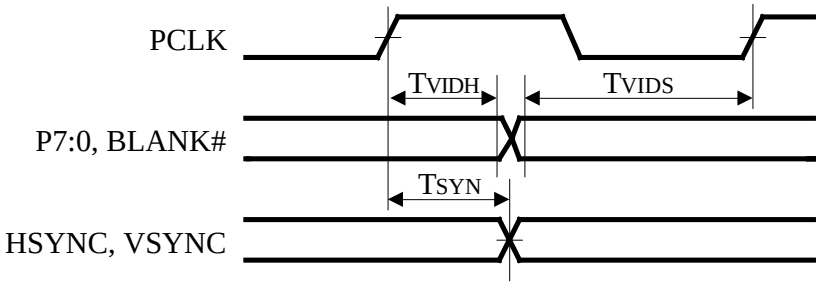
CAS-Before-RAS (CBR) DRAM Refresh Cycle Timing

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

AC TIMING CHARACTERISTICS - CRT VIDEO TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{VIDS}	PCLK Setup to P7:0, BLANK#	PCLK = 45MHz	3	–	19.2	ns
T_{VIDH}	PCLK Hold from P7:0, BLANK#	PCLK = 45MHz	3	–	19.2	ns
T_{SYN}	HSYNC, VSYNC delay from PCLK		–	–	40	ns

Note: Output load on PCLK, P7:0, and BLANK# = 30pF

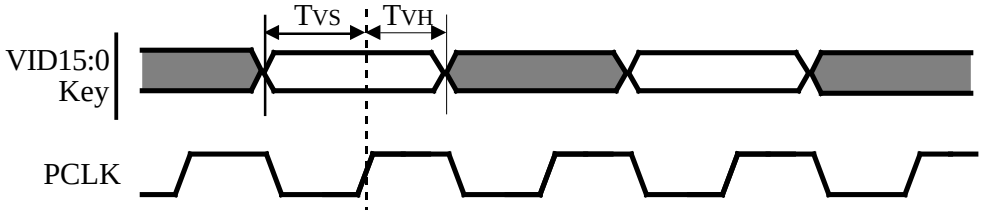


CRT Video Data and Control Signal Timing

AC TIMING CHARACTERISTICS - VIDEO OVERLAY INPUT TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{VS}	KEY, VID15:0 Setup to PCLK rising edge		15	–	–	ns
T_{VH}	KEY, VID15:0 Hold from PCLK rising edge		0	–	–	ns

Note: Output load on PCLK = 30pF



Video Overlay Timing

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

Mechanical Specifications