M56
Register Reference Guide

Technical Reference Manual
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Chapter 1
Introduction

1.1 About this Manual

This manual serves as a register reference guide to the M56 graphics controller.

- *Chapter 1* outlines the notations and conventions used throughout this manual.
- *Chapter 2* provides a detailed description of the registers.
- *Appendix A* provides several cross-referenced lists (sorted by Register Name and Address).

1.2 Nomenclature and Conventions

1.2.1 Numeric Representations

- Hexadecimal numbers are appended with “h” whenever there is a risk of ambiguity. Other numbers are assumed to be in decimal.
- Registers (or fields) of identical function are sometimes indicated by a single expression in which the part of the signal name that differs is enclosed in [ ] brackets. For example, the eight Host Data registers — HOST_DATA0 through to HOST_DATA7 — are represented by the single expression HOST_DATA[7:0].

1.2.2 Register Description

All registers in this document are described with the format of the sample table below. All offsets are in hexadecimal notation, while programmed bits are in either binomial or hexadecimal notation.

DST_HEIGHT_WIDTH_8 - W - 32 bits - [MMReg:0x158C]			
Field Name	**Bits**	**Default**	**Description**
DST_WIDTH *(mirror bits 0:7 of DST_WIDTH:DST_WIDTH)*	23:16	0x0	Destination Width Note: This is an initiator register. Y is incremented at end of blit. Write 15: 0 to E2_DST_X, Write 31: 16 to E2_DST_WIDTH, then signal blit_start. E2_DST_Y = E2_DEST_Y (+/-) E2_DST_HEIGHT as function of direction after blit is complete
DST_HEIGHT *(mirror bits 0:7 of DST_HEIGHT:DST_HEIGHT)*	31:24	0x0	Destination Height Write 15: 0 to E2_DST_Y, Write 31: 16 to E2_DST_HEIGHT

[W] (Reserved) 15: 0 DST_WIDTH 23: 16 Destination width: range 0 to 256 (ZERO extent)

Table 1-1 Register description table notation

Register Information	Example
Register name	DST_HEIGHT_WIDTH_8
Read / Write capability R = Readable W = Writable RW = Readable and Writable	W
Register size	32 bits
Register address(es)*	MMReg:0x158C
Field name	DST_WIDTH
Field position/size	23:16
Field default value	0x0
Field description	Destination....complete
Field mirror information	(mirror bits 0:7 of DST_WIDTH:DST_WIDTH)
Brief register description	[W] (Reserved) 15: 0 DST_WIDTH 23: 16 Destination width: range 0 to 256 (ZERO extent)
* Note: There may be more than one address; the convention used is as follows: **[aperName:offset]** - single mapping, to one aperture/decode and one offset **[aperName1, aperName2, …, aperNameN:offset]** - multiple mappings to different apertures/decodes but same offset **[aperName:startOffset-endOffset]** - mapped to an offset range in the same aperture/decode	

Chapter 2
Registers Description

To link to a topic of interest, use the following list of hypertext linked cross references:

2.1 Memory Controller Registers

NOTE: Channels A0, A1, B0 and B1 are also known as Channels A, B, C and D respectively.

MC_IND_INDEX - RW - 32 bits - MCDEC:0x70			
Field Name	**Bits**	**Default**	**Description**
MC_IND_ADDR	15:0	0x0	
MC_IND_SEQ_RBS_0	16	0x0	0=Do not access sequencer+gfx return bus block 0 (channels A0+A1) 1=Access sequencer+gfx return bus block 0 (channels A0+A1)
MC_IND_SEQ_RBS_1	17	0x0	0=Do not access sequencer+gfx return bus block 1 (channels B0+B1) 1=Access sequencer+gfx return bus block 1 (channels B0+B1)
MC_IND_SEQ_RBS_2	18	0x0	0=Reserved - do not program 1=Reserved - do not program
MC_IND_SEQ_RBS_3	19	0x0	0=Reserved - do not program 1=Reserved - do not program
MC_IND_AIC_RBS	20	0x0	0=Do not access aic+cpvf and glb return bus block 1=Access aic+cpvf and glb return bus block
MC_IND_CITF_ARB0	21	0x0	0=Do not access client MCT interface+arbitration block 1=Access client MCT interface+arbitration block
MC_IND_CITF_ARB1	22	0x0	0=Do not access client MCB interface+arbitration block 1=Access client MCB interface+arbitration block
MC_IND_WR_EN	23	0x0	0=Disable write capability (read only) 1=Enable write capability
MC_IND_RD_INV	24	0x0	0=Do not invert data on return bus 1=Invert data on return bus
Within MC_IND_INDEX, there are 16 bits of address, and 7 bits of mask. Each of the 7 bits of mask designates a physically distinct group of registers (in separate physical tile). One bit each for the four sequencer blocks (SQ), the AC block, MCT and MCB. A write may be done in a broadcast fashion, simultaneously programming all registers with the same indirect address in the 7 different blocks. The indirect address space is semantically non-overlapping, such that writes can typically be done with all mask bits being set to “on”. Reads tend to be from single registers, so only one mask bit is set. If more than one mask bit is set, the resulting return data will be the bitwise logical OR of all matching registers. If the MC_IND_RD_INV bit is set, with a single read mask, the return data will be bitwise inverted; if the bit is set with more than one mask bit set, the inverted data will then return the bitwise logical NAND of all matching registers. Thus this “collect” read could be useful for polling status bits with either a logical and or an or.			

MC_IND_DATA - RW - 32 bits - MCDEC:0x74			
Field Name	**Bits**	**Default**	**Description**
MC_IND_DATA	31:0	0x0	
This is the Indirect memory controller Data registers – aka the indirect data register			

MC_STATUS - RW - 8 bits - MCIND:0x0			
Field Name	**Bits**	**Default**	**Description**
MEM_PWRUP_COMPL (R)	0	0x0	0=SDRAM Init in Process 1=Ready
MC_IDLE (R)	1	0x0	Indicates that there are no pending or in-process requests in the MC 0=Not Idle 1=Idle
Status register for memory controller			

MC_TIMING_CNTL_2 - RW - 32 bits - MCIND:0x3			
Field Name	**Bits**	**Default**	**Description**
MEM_REFRESH_RATE	23:16	0x0	
Unused and invalid			

MC_FB_LOCATION - RW - 32 bits - MCIND:0x4			
Field Name	**Bits**	**Default**	**Description**
MC_FB_START	15:0	0x0	NOTE: Bits 0:7 of this field are hardwired to ZERO.
MC_FB_TOP	31:16	0xff	NOTE: Bits 0:7 of this field are hardwired to ONE.
This register defines the location of the frame buffer in the internal address space. The internal address space has 32 address bits. Minimum Frame buffer size for M56 is 16 MB, and the start location is required to be on a 16 MB boundary. Therefore START(23:0) must be 0x000000 and TOP(23:0) must be 0xFFFFFF. Only the 16 MSBs of each are loaded in the register.			

MC_AGP_LOCATION - RW - 32 bits - MCIND:0x5			
Field Name	**Bits**	**Default**	**Description**
MC_AGP_START	15:0	0x0	Defines the lowest address of the AGP Aperture
MC_AGP_TOP	31:16	0x0	Defines the highest address of the AGP Aperture
This register defines the location of the AGP space within the internal address space. The internal address space has 32 address bits (for a 4 Gbytes address range). The minimum AGP aperture granularity for M56 is 4 MB (same as Rage 6?). The start address is required to be on a 4 Mbytes boundary and the size is specified in 2 Mbytes chunks. Therefore START (21:0) must be 0x000000 and TOP (21:0) must be 0x3FFFFF. Only the 16 MSBs of each are loaded in the register. If the Start is specified to be higher than the Top, then the AGP Aperture will be non-existent and all addresses will be the PCI and/or Frame Buffer. Note that if the Frame Buffer Aperture is also non-existent, then all addresses will be PCI. There is also an AGP_BASE_ADDRESS, which is used to remap the AGP addresses before sending to the AIC. When a request occurs, the address sent to AIC = requested address - AGP_START + AGP_BASE_ADDRESS.			

AGP_BASE - RW - 32 bits - MCIND:0x6			
Field Name	**Bits**	**Default**	**Description**
AGP_BASE_ADDR	31:0	0x0	Defines the base address of the AGP aperture. Bits 21:0 must be '0'
This register is used to remap the AGP addresses before sending to the AIC. When a request occurs, the address sent to the AIC = Requested_Address - AGP_START + AGP_BASE_ADDRESS.			

AGP_BASE_2 - RW - 32 bits - MCIND:0x7			
Field Name	**Bits**	**Default**	**Description**
AGP_BASE_ADDR_2	3:0	0x0	
This is used for handling 32 Gbytes AGP Base Address. The 4 bits field represents the 4 MSBs. It extends the AGP_BASE to 36 bits instead of 32 bits.			

MC_CNTL0 - RW - 32 bits - MCIND:0x8			
Field Name	**Bits**	**Default**	**Description**
MEM_ADDR_MAP_ROWS	2:0	0x1	0=2**10 rows 1=2**11 rows 2=2**12 rows 3=2**13 rows 4=2**14 rows 5=reserved 6=reserved 7=reserved
MEM_MC_BLACKOUT	3	0x0	0=Enable MC requests - PM controlled 1=Disable MC requests - PM controlled
MEM_ADDR_MAP_COLS	5:4	0x0	0=2**8 columns 1=2**9 columns 2=2**10 columns 3=reserved
MC_CHANNEL_0_MAP	12:8	0x1	Ignored if NUM_CHANNELS = 0 0=Bit 7 1=Bit 8 2=Bit 9 3=Bit 10 4=Bit 11 5=Bit 12 6=Bit 13 7=Bit 14 8=Bit 15 9=Bit 16 10=Bit 17 11=Bit 18 12=Bit 19 13=Bit 20 14=Bit 21 15=Bit 22 16=Bit 23 17=Bit 24 18=Bit 25 19=Bit 26 20=Bit 27 21=Bit 28 22=Bit 29 23=Bit 30 24=Bit 31

MC_CHANNEL_1_MAP	17:13	0x2	Ignored if NUM_CHANNELS = 0 | 1 0=Bit 7 1=Bit 8 2=Bit 9 3=Bit 10 4=Bit 11 5=Bit 12 6=Bit 13 7=Bit 14 8=Bit 15 9=Bit 16 10=Bit 17 11=Bit 18 12=Bit 19 13=Bit 20 14=Bit 21 15=Bit 22 16=Bit 23 17=Bit 24 18=Bit 25 19=Bit 26 20=Bit 27 21=Bit 28 22=Bit 29 23=Bit 30 24=Bit 31
MC_CHANNEL_2_MAP	22:18	0x3	Unused & Invalid. 0=Bit 7 1=Bit 8 2=Bit 9 3=Bit 10 4=Bit 11 5=Bit 12 6=Bit 13 7=Bit 14 8=Bit 15 9=Bit 16 10=Bit 17 11=Bit 18 12=Bit 19 13=Bit 20 14=Bit 21 15=Bit 22 16=Bit 23 17=Bit 24 18=Bit 25 19=Bit 26 20=Bit 27 21=Bit 28 22=Bit 29 23=Bit 30 24=Bit 31
MC_CHANNEL_SIZE	23	0x0	64-bit per channel (not supported by M56 sequencer) 0=32-bit per channel 1=64-bit per channel
MEM_NUM_CHANNELS	25:24	0x0	0=One channel 1=Two channels 2=Four channels 3=Reserved
MEM_USE_XX_CH_ONLY	27:26	0x0	0=ChanA0 if NumofChan=1, A0B0 if 2, Reserved, Reserved 1=ChanB0 if NumofChan=1, A1B1 if 2, Reserved, Reserved 2=ChanA1 if NumofChan=1, A0A1 if 2, A0A1B0B1 if 4, Reserved 3=ChanB1 if NumofChan=1, B0B1 if 2, Reserved, Reserved
AIC_IDLE_DET	28	0x1	0=Ignore AIC idle signal when determining mc_idle signal 1=Use AIC idle signal when determining mc_idle signal

MC_INIT_COMPLETE	31	0x0	MC_INIT_COMPLETE is only to be set after all MC registers are properly programmed and at least 32 sclk cycles have elapsed since the last register was programmed. 0=Register Initialization Not Complete 1=Register Initialization Complete
Basic DRAM configuration (channel, rows and columns) and channel address mapping.			

MC_CNTL1 - RW - 32 bits - MCIND:0x9			
Field Name	**Bits**	**Default**	**Description**
MC_BANK_0_MAP	4:0	0x4	0=Bit 7 1=Bit 8 2=Bit 9 3=Bit 10 4=Bit 11 5=Bit 12 6=Bit 13 7=Bit 14 8=Bit 15 9=Bit 16 10=Bit 17 11=Bit 18 12=Bit 19 13=Bit 20 14=Bit 21 15=Bit 22 16=Bit 23 17=Bit 24 18=Bit 25 19=Bit 26 20=Bit 27 21=Bit 28 22=Bit 29 23=Bit 30 24=Bit 31
MC_BANK_1_MAP	9:5	0x5	0=Bit 7 1=Bit 8 2=Bit 9 3=Bit 10 4=Bit 11 5=Bit 12 6=Bit 13 7=Bit 14 8=Bit 15 9=Bit 16 10=Bit 17 11=Bit 18 12=Bit 19 13=Bit 20 14=Bit 21 15=Bit 22 16=Bit 23 17=Bit 24 18=Bit 25 19=Bit 26 20=Bit 27 21=Bit 28 22=Bit 29 23=Bit 30 24=Bit 31

MC_BANK_2_MAP	14:10	0x6	Ignored if MEM_ADDR_MAP_BANK = 0 0=Bit 7 1=Bit 8 2=Bit 9 3=Bit 10 4=Bit 11 5=Bit 12 6=Bit 13 7=Bit 14 8=Bit 15 9=Bit 16 10=Bit 17 11=Bit 18 12=Bit 19 13=Bit 20 14=Bit 21 15=Bit 22 16=Bit 23 17=Bit 24 18=Bit 25 19=Bit 26 20=Bit 27 21=Bit 28 22=Bit 29 23=Bit 30 24=Bit 31
MEM_ADDR_MAP_BANK	15	0x0	0=4 banks 1=8 banks
MC_RANK_MAP	20:16	0x7	Ignored if MEM_ADDR_MAP_RANK = 0 0=Bit 7 1=Bit 8 2=Bit 9 3=Bit 10 4=Bit 11 5=Bit 12 6=Bit 13 7=Bit 14 8=Bit 15 9=Bit 16 10=Bit 17 11=Bit 18 12=Bit 19 13=Bit 20 14=Bit 21 15=Bit 22 16=Bit 23 17=Bit 24 18=Bit 25 19=Bit 26 20=Bit 27 21=Bit 28 22=Bit 29 23=Bit 30 24=Bit 31
MEM_ADDR_MAP_RANK	21	0x0	0=1 rank 1=2 ranks
MC_BIST_ENABLE	24	0x0	Passes gfx generated bist signals to NPL 0=MC bist disabled 1=MC bist enabled
MC_RST_CTRL	25	0x0	0=MC soft-reset passthru 1=MC soft-reset force
ENABLE_PAGE_TABLES	26	0x0	0=disable page tables to dram interface 1=enable page tables to dram interface
Basic DRAM configuration and rank/bank address mapping.			

MC_RFSH_CNTL - RW - 32 bits - MCIND:0xA			
Field Name	**Bits**	**Default**	**Description**
MC_RFSH_RATE	7:0	0x1e	average (64*NUM) sclk cycles between dram refreshes when pm_slorate is deasserted (full system clock speed)
MC_RFSH_SLORATE	15:8	0xf	average (32*NUM) sclk cycles between dram refreshes when pm_slorate is asserted (dynamic clock mode)
MC_RFSH_URG	20:16	0x6	number of pending refreshes before urgency is asserted
MC_RFSH_DISABLE	21	0x1	0=DRAM Refreshes Enabled 1=DRAM Refreshes Disabled
Controls DRAM refresh timing. Example: 0x1E = 30 * 64 = 1920 cycles = 7.68nS @ 250MHz			

MC_ARB_MIN - RW - 32 bits - MCIND:0x10			
Field Name	**Bits**	**Default**	**Description**
MC_MIN_RD_CLKS	7:0	0x60	Try to stay reading for this many clocks
MC_MIN_RD_REQS	15:8	0x0	Number of pending reads required before switching away from writing
MC_MIN_WR_CLKS	23:16	0x60	Try to stay writing for this many clocks
MC_MIN_WR_REQS	31:24	0x0	Number of pending writes required before switching away from reading
These are global parameters that help determine when to switch between reading and writing. Should be tuned for optimal dram efficiency and client latency; but it is not necessary to modify defaults for functional bringup.			

MC_ARB_TIMERS - RW - 32 bits - MCIND:0x12			
Field Name	**Bits**	**Default**	**Description**
MC_IDLE_RD_CLKS	7:0	0x1	Number of elapsed clocks with no read requests before considering reads idle
MC_IDLE_WR_CLKS	15:8	0x1	Number of elapsed clocks with no write requests before considering writes idle
MC_WCMB_TIMEOUT	23:16	0xff	Number of clocks to wait in trying to combine 4Byte read requests into single 32B requests. For these clients only: CP, IDCT, VIP, MCIF
See MC_ARB_RDWR_SWITCH description for more information on IDLE fields. Should be tuned for optimal dram efficiency and client latency; but it is not necessary to modify defaults for functional bringup.			

MC_ARB_DRAM_PENALTIES - RW - 32 bits - MCIND:0x13			
Field Name	**Bits**	**Default**	**Description**
MC_RAS2RAS	6:0	0x2f	tRC
MC_SHORT_BURST_PENALTY	13:8	0x3	~1/2 MC_ACTIVATION_PENALTY
MC_ACTIVATION_PENALTY	21:16	0x8	(tRAR + tRAW) / 2
MC_NOT_MIN_PENALTY	29:24	0x20	~ 3/4 tRC
In HCLK units. Using DRAM timing parameters.			

MC_ARB_DRAM_PENALTIES2 - RW - 32 bits - MCIND:0x14			
Field Name	**Bits**	**Default**	**Description**
MC_SHORT_TO_COVER_PENALTY	5:0	0x4	~ 1/2 MC_ACTIVATION_PENALTY
MC_READ_ACTIVATION	13:8	0xe	tRAR
MC_WRITE_ACTIVATION	21:16	0xb	tRAW
MC_PRECHARGE	29:24	0xc	tRP

In HCLK units. Using DRAM timing parameters.

MC_ARB_DRAM_PENALTIES3 - RW - 32 bits - MCIND:0x15			
Field Name	**Bits**	**Default**	**Description**
MC_MIN_PENAL_ISSUE	5:0	0x23	~tRC
MC_RATIO_CLK_MODE	9:8	0x2	If 0 < (hclk / sclk) <= 1, = 0 If 1 < (hclk / sclk) <= 2, = 1 If 2 < (hclk / sclk) <= 3, = 2 If 3 < (hclk / sclk) <= 4, = 3
In HCLK units. Using DRAM timing parameters.			

MC_ARB_RATIO_CLK_SEQ - RW - 32 bits - MCIND:0x16			
Field Name	**Bits**	**Default**	**Description**
MC_RATIO_CLK_SEQ	31:0	0x0	Magic field, please use the excel programming guide. Sets the hclk/sclk ratio in the arbiter.

MC_ARB_RDWR_SWITCH - RW - 32 bits - MCIND:0x17			
Field Name	**Bits**	**Default**	**Description**
MC_RDWR_SWITCH_MODE	3:0	0x0	Read v. Write decision algorithm (see register description) 2'b00 => ~wrwt_gt_rdwt & (~|rwtimer_reg | idle_wrs); 2'b01 => ~wrwt_gt_rdwt & (~|rwtimer_reg | idle_wrs | (enough_rds & ~enough_wrs)); 2'b10 => ~wrwt_gt_rdwt & ~|rwtimer_reg & (enough_rds | idle_wrs); 2'b11 => ~|rwtimer_reg | idle_wrs;
MC_RD2WR_HYST	15:8	0x1	Read hysteresis
MC_WR2RD_HYST	23:16	0x1	Write hysteresis
Read v. Write decision algorithm. Should be tuned for optimal dram efficiency and client latency; but it is not necessary to modify defaults for functional bringup.			

MC_SW_CNTL - RW - 8 bits - MCIND:0x18			
Field Name	**Bits**	**Default**	**Description**
MC_BUBBLE_INSERT	2:0	0x1	Insert this many dead cycles between each burst of requests to the sequencer. Must not be set to 0.
Increasing this value may prevent inefficient requests from clogging the sequencer, and may provide for a smaller worst-case latency. Unverified for values other than 0x1.			

MC_WRITE_AGE1 - RW - 32 bits - MCIND:0x37			
Field Name	**Bits**	**Default**	**Description**
MC_CBW_AGEDIV	4:0	0x8	
MC_CBW_USEAGE	7	0x1	0=Do not age CB write requests 1=Age CB write requests
MC_ZBW_AGEDIV	12:8	0x8	
MC_ZBW_USEAGE	15	0x1	0=Do not age ZB write requests 1=Age ZB write requests
MC_MCIF_AGEDIV	20:16	0x8	
MC_MCIF_USEAGE	23	0x1	0=Do not age MCIF write requests 1=Age MCIF write requests

MC_VIP_AGEDIV	28:24	0x8	
MC_VIP_USEAGE	31	0x1	0=Do not age VIP write requests 1=Age VIP write requests
Arbitration parameters for these clients. Should be tuned for optimal dram efficiency and client latency; but it is not necessary to modify defaults for functional bringup.			

MC_WRITE_AGE2 - RW - 32 bits - MCIND:0x38			
Field Name	**Bits**	**Default**	**Description**
MC_DCT_AGEDIV	4:0	0x8	
MC_DCT_USEAGE	7	0x1	0=Do not age DCT write requests 1=Age DCT write requests
MC_HDP_AGEDIV	12:8	0x8	
MC_HDP_USEAGE	15	0x1	0=Do not age HDP write requests 1=Age HDP write requests
MC_CP_AGEDIV	20:16	0x8	
MC_CP_USEAGE	23	0x1	0=Do not age CP write requests 1=Age CP write requests
Arbitration parameters for these clients. Should be tuned for optimal dram efficiency and client latency; but it is not necessary to modify defaults for functional bringup.			

MC_SEQ_DRAM - RW - 32 bits - MCIND:0x60			
Field Name	**Bits**	**Default**	**Description**
ADR_2CK	0	0x0	Number of cycle(s) to send an address. One cycle for non-DDR4. Two cycles for DDR4. 0=One-cycle address 1=Two-cycle address
ADR_MUX	1	0x0	Address bus is shared between two channels or not. Not shared for DDR4. Shared for non-DDR4. 0=Address bus is not shared 1=Address bus is shared
ADR_DF1	2	0x0	Default value for address bus (during NOP). 0=Address default low 1=Address default high
AP8	3	0x0	Location of auto-precharge bit. 0=AP bit starts at MSB+1 1=AP bit is bit 8
DAT_DF1	4	0x0	Default value for data bus. 0=DAT default low 1=DAT default high
DQS_DF1	5	0x0	Default value for write strobes. 0=DQS default low 1=DQS default high
DQM_DF1	6	0x0	Default value for write mask. 0=DQM default low 1=DQM default high
DQM_ACT	7	0x0	Polarity of data mask. Active low for DDR4. Active high for non-DDR4. 0=DQM active low 1=DQM active high
STB_CNT	11:8	0xf	DRAM standby counter. Number of idle cycles before dynamic CKE is enabled. This prevents the CKE from turning off too easily.
CKE_DYN	12	0x0	Dynamic CKE. 0=Disable 1=Enable

CKE_ACT	13	0x1	Polarity of clock enable. Active low for DDR4. Active high for non-DDR4. 0=Active low 1=Active high
BO4	14	0x0	DRAM burst size. 0=DRAM is burst of 8 1=DRAM is burst of 4
DLL_CNT	19:16	0xf	DRAM DLL lock time in multiples of 16 mclk cycles.
DLL_CLR	20	0x0	Resets DLL lock timer. DRAM power up is completed once the DLL lock time is reached. If the DLL lock timer is reset, the DRAM power up flag is deasserted. 0=Not reset DLL timer 1=Reset DLL timer
DAT_INV	24	0x0	Enables/disables DDR write data inversion mode. 0=Disable write data inversion 1=Enable write data inversion
INV_ACM	25	0x1	Selects DDR write data inversion mode. 0=DC mode 1=AC mode
ODT_ENB	26	0x0	0=Disable ODT 1=Enable ODT
ODT_ACT	27	0x1	0=ODT active low 1=ODT active high
RST_CTL	28	0x0	Controls DRAM reset pin. Channel pair B only. 0=Drive reset low 1=Drive reset high
This register specifies the character of the DRAM interface.			

MC_SEQ_RAS_TIMING - RW - 32 bits - MCIND:0x61			
Field Name	**Bits**	**Default**	**Description**
TRCDW	4:0	0x0	Number of cycles from active to write - 1.
TRCDWA	9:5	0x0	Number of cycles from active to write with auto-precharge - 1. A special case for DDR1. Otherwise the same as TRCDW.
TRCDR	14:10	0x0	Number of cycles from active to read - 1.
TRCDRA	19:15	0x0	Number of cycles from active to read with auto-precharge - 1. A special case for DDR1. Otherwise the same as TRCDR.
TRRD	23:20	0x0	Number of cycles from active bank a to active bank b - 1.
TRC	30:24	0x0	Number of cycles from active to active/auto refresh - 1.
RAS related parameters in hclk cycles.			

MC_SEQ_CAS_TIMING - RW - 32 bits - MCIND:0x62			
Field Name	**Bits**	**Default**	**Description**
TNOPW	1:0	0x0	Extra cycle(s) between successive write bursts. For debugging purpose only.
TNOPR	3:2	0x0	Extra cycle(s) between successive read bursts. For debugging purpose only.
TR2W	8:4	0x0	Read to write turn around time - 1.
TR2R	15:12	0x0	Read to read time - 1 (different rank).
TW2R	20:16	0x0	Write to read turn around time - 1.
TCL	28:24	0x0	CAS to data return latency - 2 (0 to 20).
CAS related parameters in hclk cycles.			

MC_SEQ_MISC_TIMING - RW - 32 bits - MCIND:0x63			
Field Name	**Bits**	**Default**	**Description**
TRP_WRA	5:0	0x0	From write with auto-precharge to active - 1.
TRP_RDA	13:8	0x0	From read with auto-precharge to active - 1.
TRP	19:16	0x0	Precharge command period - 1.
TRFC	26:20	0x0	Auto-refresh command period - 1.
TCKE	31:28	0x0	CKE power down exit timer.
Misc. DRAM parameters in hclk cycles.			

MC_SEQ_RD_CTL_I0 - RW - 32 bits - MCIND:0x64			
Field Name	**Bits**	**Default**	**Description**
RCV_DLY	2:0	0x0	Delay to turn on receive enable. 0=Turn on receive enable at CL-2 1=Turn on receive enable at CL-1 2=Turn on receive enable at CL 3=Turn on receive enable at CL+1 4=Turn on receive enable at CL+2 5=Turn on receive enable at CL+3 6=Turn on receive enable at CL+4 7=Turn on receive enable at CL+5
RCV_EXT	7:4	0x0	Extends receive enable signal to cover clock drift. 0=DQS receive enable not extended 1=DQS receive enable extended by 1 cycle 2=DQS receive enable extended by 2 cycles 3=DQS receive enable extended by 3 cycles 4=DQS receive enable extended by 4 cycles 5=DQS receive enable extended by 5 cycles 6=DQS receive enable extended by 6 cycles 7=DQS receive enable extended by 7 cycles 8=DQS receive enable always on
RST_SEL	9:8	0x0	NPL FIFO pointer reset mode. 0=Reset pointers off 1=Reset pointers on 2=Reset pointers before read 3=Reset pointers during refresh
RST_HLD	15:12	0x0	Disables NPL FIFO pointer reset after a read command for a certain period of time. This prevents the pointers (read and write) from resetting before the FIFO is read. 0=Disable reset by 11 cycles 1=Disable reset by 12 cycles 2=Disable reset by 13 cycles 3=Disable reset by 14 cycles 4=Disable reset by 15 cycles 5=Disable reset by 16 cycles 6=Disable reset by 17 cycles 7=Disable reset by 18 cycles 8=Disable reset by 19 cycles 9=Disable reset by 20 cycles 10=Disable reset by 21 cycles 11=Disable reset by 22 cycles 12=Disable reset by 23 cycles 13=Disable reset by 24 cycles 14=Disable reset by 25 cycles
STR_PRE	16	0x0	Creates an extra strobe in the preamble of a burst. This is needed if DQS is default high and its falling edge is used as a trigger. 0=No read pre strobe 1=Extra read pre strobe

STR_PST	17	0x0	Creates an extra strobe in the postamble of a burst. This is needed if DQS is default high and its rising edge is used as a trigger. 0=No read post strobe 1=Extra read post strobe
RBS_DLY	24:20	0x0	Delay to read data out of a NPL FIFO. This is used to cover the NPL FIFO's write to read latency. 0=Assert RBS valid at CL+8 1=Assert RBS valid at CL+9 2=Assert RBS valid at CL+10 3=Assert RBS valid at CL+11 4=Assert RBS valid at CL+12 5=Assert RBS valid at CL+13 6=Assert RBS valid at CL+14 7=Assert RBS valid at CL+15 8=Assert RBS valid at CL+16 9=Assert RBS valid at CL+17 10=Assert RBS valid at CL+18 11=Assert RBS valid at CL+19 12=Assert RBS valid at CL+20 13=Assert RBS valid at CL+21 14=Assert RBS valid at CL+22 15=Assert RBS valid at CL+23 16=Assert RBS valid at CL+24 17=Assert RBS valid at CL+25
Channel 0's read command parameters in hclk.			

MC_SEQ_RD_CTL_I1 - RW - 32 bits - MCIND:0x65			
Field Name	**Bits**	**Default**	**Description**
RCV_DLY	2:0	0x0	0=Turn on receive enable at CL-2 1=Turn on receive enable at CL-1 2=Turn on receive enable at CL 3=Turn on receive enable at CL+1 4=Turn on receive enable at CL+2 5=Turn on receive enable at CL+3 6=Turn on receive enable at CL+4 7=Turn on receive enable at CL+5
RCV_EXT	7:4	0x0	0=DQS receive enable not extended 1=DQS receive enable extended by 1 cycle 2=DQS receive enable extended by 2 cycles 3=DQS receive enable extended by 3 cycles 4=DQS receive enable extended by 4 cycles 5=DQS receive enable extended by 5 cycles 6=DQS receive enable extended by 6 cycles 7=DQS receive enable extended by 7 cycles 8=DQS receive enable always on
RST_SEL	9:8	0x0	0=Reset pointers off 1=Reset pointers on 2=Reset pointers before read 3=Reset pointers during refresh

RST_HLD	15:12	0x0	0=Disable reset by 11 cycles 1=Disable reset by 12 cycles 2=Disable reset by 13 cycles 3=Disable reset by 14 cycles 4=Disable reset by 15 cycles 5=Disable reset by 16 cycles 6=Disable reset by 17 cycles 7=Disable reset by 18 cycles 8=Disable reset by 19 cycles 9=Disable reset by 20 cycles 10=Disable reset by 21 cycles 11=Disable reset by 22 cycles 12=Disable reset by 23 cycles 13=Disable reset by 24 cycles 14=Disable reset by 25 cycles
STR_PRE	16	0x0	0=No read pre strobe 1=Extra read pre strobe
STR_PST	17	0x0	0=No read post strobe 1=Extra read post strobe
RBS_DLY	24:20	0x0	0=Assert RBS valid at CL+8 1=Assert RBS valid at CL+9 2=Assert RBS valid at CL+10 3=Assert RBS valid at CL+11 4=Assert RBS valid at CL+12 5=Assert RBS valid at CL+13 6=Assert RBS valid at CL+14 7=Assert RBS valid at CL+15 8=Assert RBS valid at CL+16 9=Assert RBS valid at CL+17 10=Assert RBS valid at CL+18 11=Assert RBS valid at CL+19 12=Assert RBS valid at CL+20 13=Assert RBS valid at CL+21 14=Assert RBS valid at CL+22 15=Assert RBS valid at CL+23 16=Assert RBS valid at CL+24 17=Assert RBS valid at CL+25
Channel 1's read command parameters in hclk. See MC_SEQ_RD_CTL_I0.			

MC_SEQ_WR_CTL_I0 - RW - 32 bits - MCIND:0x66			
Field Name	**Bits**	**Default**	**Description**
DAT_DLY	3:0	0x0	Write command to data output latency.
DQS_DLY	7:4	0x0	Write command to DQS latency.
DQS_XTR	8	0x0	Controls write preamble. 0=No write preamble 1=Write preamble
OEN_DLY	15:12	0x0	Write command to output enable latency.
OEN_EXT	16	0x0	Extend output enable after data burst. 0=output enable not extended 1=output enable extended by one cycle
OEN_SEL	21:20	0x0	Output enable select mask (for debug only).
ODT_DLY	27:24	0x0	Write command to on-die-termination enable latency.
ODT_EXT	28	0x0	Extends on-die-termination enable after data burst. 0=ODT not extended 1=ODT extended by one cycle
Channel 0's write command parameters in hclk.			

MC_SEQ_WR_CTL_I1 - RW - 32 bits - MCIND:0x67

Field Name	Bits	Default	Description
DAT_DLY	3:0	0x0	Write command to data output latency.
DQS_DLY	7:4	0x0	Write command to DQS latency.
DQS_XTR	8	0x0	Controls write preamble. 0=No write preamble 1=Write preamble
OEN_DLY	15:12	0x0	Write command to output enable latency.
OEN_EXT	16	0x0	Extend output enable after data burst. 0=output enable not extended 1=output enable extended by one cycle
OEN_SEL	21:20	0x0	Output enable select mask (for debug only).
ODT_DLY	27:24	0x0	Write command to on-die-termination enable latency.
ODT_EXT	28	0x0	Extends on-die-termination enable after data burst. 0=ODT not extended 1=ODT extended by one cycle
Channel 1's write command parameters in hclk.			

MC_SEQ_IO_CTL_I0 - RW - 32 bits - MCIND:0x68			
Field Name	**Bits**	**Default**	**Description**
ADR_DLY	0	0x0	Delays address output by half a hclk.
CMD_DLY	1	0x0	Delays command output by half a hclk.
CKN_TRI	4	0x0	Turns off negative clock manually. 0=Normal 1=Tristate
CKP_TRI	5	0x0	Turns off positive clock manually. 0=Normal 1=Tristate
MIO_TRI	6	0x0	Turns off address and command manually. 0=Normal 1=Tristate
CKE_BIT	7	0x0	Bypass value for clock enable.
CKE_SEL	8	0x1	Selects clock enable bypass value. 0=Normal CKE 1=Set CKE bit
Channel 0's misc. control parameters.			

MC_SEQ_IO_CTL_I1 - RW - 32 bits - MCIND:0x69			
Field Name	**Bits**	**Default**	**Description**
ADR_DLY	0	0x0	Delays address output by half a hclk.
CMD_DLY	1	0x0	Delays command output by half a hclk.
CKN_TRI	4	0x0	Turns off negative clock manually. 0=Normal 1=Tristate
CKP_TRI	5	0x0	Turns off positive clock manually. 0=Normal 1=Tristate
MIO_TRI	6	0x0	Turns off address and command manually. 0=Normal 1=Tristate
CKE_BIT	7	0x0	Bypass value for clock enable.
CKE_SEL	8	0x1	Selects clock enable bypass value. 0=Normal CKE 1=Set CKE bit
Channel 1's misc. control parameters.			

MC_SEQ_NPL_CTL_I0 - RW - 32 bits - MCIND:0x6A			
Field Name	**Bits**	**Default**	**Description**
LD_INIT	1:0	0x0	NPL FIFO's pointer offset.
SYC_SEL	5:4	0x0	Selects mclk/yclk synchronization mode. 0=mclk/yclk sync off 1=mclk/yclk sync on 2=mclk/yclk sync during refresh
Channel 0's NPL control parameters.			

MC_SEQ_NPL_CTL_I1 - RW - 32 bits - MCIND:0x6B			
Field Name	**Bits**	**Default**	**Description**
LD_INIT	1:0	0x0	NPL FIFO's pointer offset.
SYC_SEL	5:4	0x0	Selects mclk/yclk synchronization mode. 0=mclk/yclk sync off 1=mclk/yclk sync on 2=mclk/yclk sync during refresh
Channel 1's NPL control parameters.			

MC_SEQ_CK_PAD_CNTL_I0 - RW - 32 bits - MCIND:0x6C			
Field Name	**Bits**	**Default**	**Description**
NMOS_PD	1:0	0x0	NMOS pulldown value.
PSTR_OFF	7:4	0x0	P drive strength/offset.
NSTR_OFF	11:8	0x0	N drive strength/offset.
USE_CAL_STR	12	0x0	If set, combines auto-calibration strength with programmed offset. Otherwise, use programmed drive strength directly. 0=Ignore cal ctl str 1=Use cal ctl str
LOAD_STR	13	0x0	Loads drive strength explicitly.
Channel 0's clock pad control parameters.			

MC_SEQ_CK_PAD_CNTL_I1 - RW - 32 bits - MCIND:0x6D			
Field Name	**Bits**	**Default**	**Description**
NMOS_PD	1:0	0x0	NMOS pulldown value.
PSTR_OFF	7:4	0x0	P drive strength/offset.
NSTR_OFF	11:8	0x0	N drive strength/offset.
USE_CAL_STR	12	0x0	If set, combines auto-calibration strength with programmed offset. Otherwise, use programmed drive strength directly. 0=Ignore cal ctl str 1=Use cal ctl str
LOAD_STR	13	0x0	Loads drive strength explicitly.
Channel 1's clock pad control parameters.			

MC_SEQ_CMD_PAD_CNTL_I0 - RW - 32 bits - MCIND:0x6E			
Field Name	**Bits**	**Default**	**Description**
NMOS_PD	1:0	0x0	NMOS pulldown value.
PSTR_OFF	7:4	0x0	P drive strength/offset.
NSTR_OFF	11:8	0x0	N drive strength/offset.

USE_CAL_STR	12	0x0	If set, combines auto-calibration strength with programmed offset. Otherwise, use programmed drive strength directly. 0=Ignore cal ctl str 1=Use cal ctl str
LOAD_STR	13	0x0	Loads drive strength explicitly.
Channel 0's command pad control parameters.			

MC_SEQ_CMD_PAD_CNTL_I1 - RW - 32 bits - MCIND:0x6F			
Field Name	**Bits**	**Default**	**Description**
NMOS_PD	1:0	0x0	NMOS pulldown value.
PSTR_OFF	7:4	0x0	P drive strength/offset.
NSTR_OFF	11:8	0x0	N drive strength/offset.
USE_CAL_STR	12	0x0	If set, combines auto-calibration strength with programmed offset. Otherwise, use programmed drive strength directly. 0=Ignore cal ctl str 1=Use cal ctl str
LOAD_STR	13	0x0	Loads drive strength explicitly.
Channel 1's command pad control parameters.			

MC_SEQ_DQ_PAD_CNTL_I0 - RW - 32 bits - MCIND:0x70			
Field Name	**Bits**	**Default**	**Description**
NMOS_PD	1:0	0x0	NMOS pulldown value.
PSTR_OFF	7:4	0x0	P drive strength/offset.
NSTR_OFF	11:8	0x0	N drive strength/offset.
USE_CAL_STR	12	0x0	If set, combines auto-calibration strength with programmed offset. Otherwise, use programmed drive strength directly. 0=Ignore cal ctl str 1=Use cal ctl str
LOAD_STR	13	0x0	Loads drive strength explicitly.
Channel 0's data pad control parameters.			

MC_SEQ_DQ_PAD_CNTL_I1 - RW - 32 bits - MCIND:0x71			
Field Name	**Bits**	**Default**	**Description**
NMOS_PD	1:0	0x0	NMOS pulldown value.
PSTR_OFF	7:4	0x0	P drive strength/offset.
NSTR_OFF	11:8	0x0	N drive strength/offset.
USE_CAL_STR	12	0x0	If set, combines auto-calibration strength with programmed offset. Otherwise, use programmed drive strength directly. 0=Ignore cal ctl str 1=Use cal ctl str
LOAD_STR	13	0x0	Loads drive strength explicitly.
Channel 1's data pad control parameters.			

MC_SEQ_QS_PAD_CNTL_I0 - RW - 32 bits - MCIND:0x72			
Field Name	**Bits**	**Default**	**Description**
NMOS_PD	1:0	0x0	NMOS pulldown value.
PSTR_OFF	7:4	0x0	P drive strength/offset.
NSTR_OFF	11:8	0x0	N drive strength/offset.

USE_CAL_STR	12	0x0	If set, combines auto-calibration strength with programmed offset. Otherwise, use programmed drive strength directly. 0=Ignore cal ctl str 1=Use cal ctl str
LOAD_STR	13	0x0	Loads drive strength explicitly.
Channel 0's strobe pad control parameters.			

MC_SEQ_QS_PAD_CNTL_I1 - RW - 32 bits - MCIND:0x73			
Field Name	**Bits**	**Default**	**Description**
NMOS_PD	1:0	0x0	NMOS pulldown value.
PSTR_OFF	7:4	0x0	P drive strength/offset.
NSTR_OFF	11:8	0x0	N drive strength/offset.
USE_CAL_STR	12	0x0	If set, combines auto-calibration strength with programmed offset. Otherwise, use programmed drive strength directly. 0=Ignore cal ctl str 1=Use cal ctl str
LOAD_STR	13	0x0	Loads drive strength explicitly.
Channel 1's strobe pad control parameters.			

MC_SEQ_A_PAD_CNTL_I0 - RW - 32 bits - MCIND:0x74			
Field Name	**Bits**	**Default**	**Description**
NMOS_PD	1:0	0x0	NMOS pulldown value.
PSTR_OFF	7:4	0x0	P drive strength/offset.
NSTR_OFF	11:8	0x0	N drive strength/offset.
USE_CAL_STR	12	0x0	If set, combines auto-calibration strength with programmed offset. Otherwise, use programmed drive strength directly. 0=Ignore cal ctl str 1=Use cal ctl str
LOAD_STR	13	0x0	Loads drive strength explicitly.
Lower address byte (b0 to b7) pad control parameters.			

MC_SEQ_A_PAD_CNTL_I1 - RW - 32 bits - MCIND:0x75			
Field Name	**Bits**	**Default**	**Description**
NMOS_PD	1:0	0x0	NMOS pulldown value.
PSTR_OFF	7:4	0x0	P drive strength/offset.
NSTR_OFF	11:8	0x0	N drive strength/offset.
USE_CAL_STR	12	0x0	If set, combines auto-calibration strength with programmed offset. Otherwise, use programmed drive strength directly. 0=Ignore cal ctl str 1=Use cal ctl str
LOAD_STR	13	0x0	Loads drive strength explicitly.
Upper address byte (b8 to b15) pad control parameters.			

MC_SEQ_CMD - RW - 32 bits - MCIND:0x76			
Field Name	**Bits**	**Default**	**Description**
ADR	15:0	0x0	This field is mapped directly to the address bus. Note: Previous write data is not stored.

MOP	18:16	0x0	DRAM command. 0=NOP 1=Load mode register 2=Precharge 3=Auto-refresh 4=Self-refresh
END	20	0x0	If set, the DLL lock timer starts counting. Once it reaches a pre-defined value, the DLL is stabilized and DRAM power up sequence is completed. See also DLL_CNT inside MC_SEQ_DRAM. 0=Not last operation 1=Last operation, wait for DLL to stabilize
CSB	22:21	0x0	Allows rank 0 and rank 1 to be selected independently. 0=Select both ranks 1=Select rank 1 2=Select rank 0 3=Select none
Command register for DRAM initialization.			

MC_SEQ_STATUS - RW - 32 bits - MCIND:0x77			
Field Name	**Bits**	**Default**	**Description**
PWRUP_COMPL	0	0x0	DRAM power up status. 0=SDRAM init in progress 1=SDRAM ready
CMD_RDY	1	0x0	Command register status. 0=Command register busy 1=Command register ready
Channel status register.			

MC_IO_PAD_CNTL_I0 - RW - 32 bits - MCIND:0x80			
Field Name	**Bits**	**Default**	**Description**
DELAY_DATA_SYNC	0	0x0	Delay memory data bits by 1 yclk 0=Don't delay data sync 1=delay data sync by 1 yclk
DELAY_STR_SYNC	1	0x0	Delay memory strobe bits by 1 yclk 0=Don't delay strobe sync 1=delay strobe sync by 1 yclk
DELAY_CLK_SYNC	2	0x0	Delay memory clk bits by 1 yclk 0=Don't delay clk sync 1=delay clk sync by 1 yclk
DELAY_CMD_SYNC	3	0x0	Delay memory command bits by 1 yclk 0=Don't delay cmd sync 1=delay cmd sync by 1 yclk
DELAY_ADR_SYNC	4	0x0	Delay memory address bits by 1 yclk 0=Don't delay adr sync 1=delay adr sync by 1 yclk
MEM_FALL_OUT_DATA	5	0x0	Advance 1/2 yclk in data bits 0=Data out on YCLK rise 1=Data out on YCLK fall, 1/4 clock delay
MEM_FALL_OUT_STR	6	0x0	Advance 1/2 yclk in strobe bits 0=Strobe out on YCLK rise 1=Strobe out on YCLK fall, 1/4 clock delay
MEM_FALL_OUT_CLK	7	0x0	Advance 1/2 yclk in clock bits 0=Clk out on YCLK rise 1=Clk out on YCLK fall, 1/4 clock delay
MEM_FALL_OUT_CMD	8	0x0	Advance 1/2 yclk in command bits 0=Command out on YCLK rise 1=Command out on YCLK fall, 1/4 clock delay

MEM_FALL_OUT_ADR	9	0x0	Advance 1/2 yclk in address bits 0=Address out on YCLK rise 1=Address out on YCLK fall, 1/4 clock delay
FORCE_EN_RD_STR	10	0x0	NOT USED 0=Read strb enabled by MC 1=Always enable read strb
EN_RD_STR_DLY	11	0x0	NOT USED 0=count rising edge 1=count falling edge
DISABLE_CMD	12	0x0	Enable/Disable memory command bits 0=Drive command 1=Disable command
DISABLE_ADR	13	0x0	Enable/Disable memory address bits 0=Drive address 1=Disable address
VREFI_EN	14	0x0	Enable/Disable VREFI 0=VREFI disable 1=VREFI enable
VREFI_SEL	19:15	0x0	Select VREFI levels (5'b10000 = VREFS, ~10mV per +/-step)
CK_AUTO_EN	20	0x0	Enable/Disable Auto memory differential clk skew calibration 0=No CK duty cycle correction 1=Correct CK duty cycle
CK_DELAY_SEL	21	0x0	Use Manual or Auto differential clock skew values 0=Use register value 1=Use auto cal value
CK_DELAY_N	23:22	0x0	Manual CLKN delay values (0-3)
CK_DELAY_P	25:24	0x0	Manual CLKP delay values (0-3)
Channel 0's Pad general control parameters			

MC_IO_PAD_CNTL_I1 - RW - 32 bits - MCIND:0x81			
Field Name	**Bits**	**Default**	**Description**
DELAY_DATA_SYNC	0	0x0	Delay memory data bits by 1 yclk 0=Don't delay data sync 1=delay data sync by 1 yclk
DELAY_STR_SYNC	1	0x0	Delay memory strobe bits by 1 yclk 0=Don't delay strobe sync 1=delay strobe sync by 1 yclk
DELAY_CLK_SYNC	2	0x0	Delay memory clk bits by 1 yclk 0=Don't delay clk sync 1=delay clk sync by 1 yclk
DELAY_CMD_SYNC	3	0x0	Delay memory command bits by 1 yclk 0=Don't delay cmd sync 1=delay cmd sync by 1 yclk
DELAY_ADR_SYNC	4	0x0	Delay memory address bits by 1 yclk 0=Don't delay adr sync 1=delay adr sync by 1 yclk
MEM_FALL_OUT_DATA	5	0x0	Advance 1/2 yclk in data bits 0=Data out on YCLK rise 1=Data out on YCLK fall, 1/4 clock delay
MEM_FALL_OUT_STR	6	0x0	Advance 1/2 yclk in strobe bits 0=Strobe out on YCLK rise 1=Strobe out on YCLK fall, 1/4 clock delay
MEM_FALL_OUT_CLK	7	0x0	Advance 1/2 yclk in clock bits 0=Clk out on YCLK rise 1=Clk out on YCLK fall, 1/4 clock delay
MEM_FALL_OUT_CMD	8	0x0	Advance 1/2 yclk in command bits 0=Command out on YCLK rise 1=Command out on YCLK fall, 1/4 clock delay

MEM_FALL_OUT_ADR	9	0x0	Advance 1/2 yclk in address bits 0=Address out on YCLK rise 1=Address out on YCLK fall, 1/4 clock delay
FORCE_EN_RD_STR	10	0x0	NOT USED 0=Read strb enabled by MC 1=Always enable read strb
EN_RD_STR_DLY	11	0x0	NOT USED 0=count rising edge 1=count falling edge
DISABLE_CMD	12	0x0	Enable/Disable memory command bits 0=Drive command 1=Disable command
DISABLE_ADR	13	0x0	Enable/Disable memory address bits 0=Drive address 1=Disable address
VREFI_EN	14	0x0	Enable/Disable VREFI 0=VREFI disable 1=VREFI enable
VREFI_SEL	19:15	0x0	VREFI levels select (5'b10000 = VREFS, ~10mV per +/-step)
CK_AUTO_EN	20	0x0	Enable/Disable Auto memory differential clk skew calibration 0=No CK duty cycle correction 1=Correct CK duty cycle
CK_DELAY_SEL	21	0x0	Use Manual or Auto differential clock skew values 0=Use register value 1=Use auto cal value
CK_DELAY_N	23:22	0x0	Manual CLKN delay values (0-3)
CK_DELAY_P	25:24	0x0	Manual CLKP delay values (0-3)
Channel 1's Pad general control parameters			

MC_IO_PAD_CNTL - RW - 32 bits - MCIND:0x82			
Field Name	**Bits**	**Default**	**Description**
DELAY_MASTER_SYNC	1:0	0x0	Delay Master Sync between Sequencer/NPL by (0-3) yclks Combined with MC_SEQ_NPL_CTL.LD_INIT[1:0] set the FIFO depth (in yclk) between mclk/yclk Format: (LD_INIT,DELAY_MASTER_SYNC) => FIFO_DEPTH (0,0)=>6,(0,1)=>7,(0,2)=>8,(0,3)=>9, (1,0)=>2,(1,1)=>3,(1,2)=>4,(1,3)=>5, (2,0)=>x,(2,1)=>x,(2,2)=>0,(2,3)=>1, (3,0)=>10,(3,1)=>11,(3,2)=>12,(3,3)=>x,
DIFF_STR	2	0x0	Differential Strobes select 0=Strobe single ended 1=Strobe differential
UNI_STR	3	0x0	Unidirectional Strobes select 0=Bidirectional strobes 1=Unidirectional strobes
IMP_VREF_INTR	5	0x0	VREFR select for Impedance control pad
IMP_VREF_INTN	7:6	0x0	VREFN select for Impedance control pad
IMP_VREF_INTP	9:8	0x0	VREFP select for Impedance control pad
Channel 0 and 1's Pad general control parameters			

MC_IO_RD_DQ_CNTL_I0 - RW - 32 bits - MCIND:0x84			
Field Name	**Bits**	**Default**	**Description**
MADJ0	7:0	0x0	Byte 0
MADJ1	15:8	0x0	Byte 1
MADJ2	23:16	0x0	Byte 2
MADJ3	31:24	0x0	Byte 3

Channel 0's DLL delay control parameters (MADJ). DLL delay (ns) = (ADJ[7:0]+24)/MADJ[7:0]*HCLK period

MC_IO_RD_DQ_CNTL_I1 - RW - 32 bits - MCIND:0x85			
Field Name	**Bits**	**Default**	**Description**
MADJ0	7:0	0x0	Byte 0
MADJ1	15:8	0x0	Byte 1
MADJ2	23:16	0x0	Byte 2
MADJ3	31:24	0x0	Byte 3
Channel 1's DLL delay control parameters (MADJ). DLL delay (ns) = (ADJ[7:0]+24)/MADJ[7:0]*HCLK period			

MC_IO_RD_QS_CNTL_I0 - RW - 32 bits - MCIND:0x86			
Field Name	**Bits**	**Default**	**Description**
DLY0	7:0	0x0	Byte 0
DLY1	15:8	0x0	Byte 1
DLY2	23:16	0x0	Byte 2
DLY3	31:24	0x0	Byte 3
Channel 0's DLL delay control parameters (ADJ). DLL delay (ns) = (ADJ[7:0]+24)/MADJ[7:0]*HCLK period			

MC_IO_RD_QS_CNTL_I1 - RW - 32 bits - MCIND:0x87			
Field Name	**Bits**	**Default**	**Description**
DLY0	7:0	0x0	Byte 0
DLY1	15:8	0x0	Byte 1
DLY2	23:16	0x0	Byte 2
DLY3	31:24	0x0	Byte 3
Channel 1's DLL delay control parameters (ADJ). DLL delay (ns) = (ADJ[7:0]+24)/MADJ[7:0]*HCLK period			

MC_IO_WR_CNTL_I0 - RW - 32 bits - MCIND:0x88			
Field Name	**Bits**	**Default**	**Description**
CK_DLY	4:0	0x0	Clock delay
CMD_DLY	9:5	0x0	Command delay
ADR_DLY	14:10	0x0	Address delay
Channel 0's delay line parameters clock/command/address bits			

MC_IO_WR_CNTL_I1 - RW - 32 bits - MCIND:0x89			
Field Name	**Bits**	**Default**	**Description**
CK_DLY	4:0	0x0	Clock delay
CMD_DLY	9:5	0x0	Command delay
ADR_DLY	14:10	0x0	Address delay
Channel 1's delay line parameters clock/command/address bits			

MC_IO_CK_PAD_CNTL_I0 - RW - 32 bits - MCIND:0x8A			
Field Name	**Bits**	**Default**	**Description**
PTERM	3:0	0x0	NPL Termination control P side
NTERM	7:4	0x0	NPL Termination control N side
PDRV	11:8	0x0	NPL Drive control P side
NDRV	15:12	0x0	NPL Drive control N side
RECV_DUTY	17:16	0x0	Pad Receive Duty control
DRV_DUTY	19:18	0x0	Pad Drive Duty control
PREAMP	21:20	0x0	NPL Pre-emphasis enable select, [1:0] for finger [7:6], 0=>disable, 1=>enable
SELFTIME	22	0x0	Pad Pre-emphasis delay select
SLEW	24:23	0x0	Pad slew rate control
VMODE	25	0x0	Receive Default pull-up/down
VREF_INT	27:26	0x0	Vref select
VREF_INTR	28	0x0	VrefR select
Channel 0's clock pad control parameters			

MC_IO_CK_PAD_CNTL_I1 - RW - 32 bits - MCIND:0x8B			
Field Name	**Bits**	**Default**	**Description**
PTERM	3:0	0x0	NPL Termination control P side
NTERM	7:4	0x0	NPL Termination control N side
PDRV	11:8	0x0	NPL Drive control P side
NDRV	15:12	0x0	NPL Drive control N side
RECV_DUTY	17:16	0x0	Pad Receive Duty control
DRV_DUTY	19:18	0x0	Pad Drive Duty control
PREAMP	21:20	0x0	NPL Pre-emphasis enable select, [1:0] for finger [7:6], 0=>disable, 1=>enable
SELFTIME	22	0x0	Pad Pre-emphasis delay select
SLEW	24:23	0x0	Pad slew rate control
VMODE	25	0x0	Receive Default pull-up/down
VREF_INT	27:26	0x0	Vref select
VREF_INTR	28	0x0	VrefR select
Channel 1's clock pad control parameters			

MC_IO_CMD_PAD_CNTL_I0 - RW - 32 bits - MCIND:0x8C			
Field Name	**Bits**	**Default**	**Description**
PTERM	3:0	0x0	NPL Termination control P side
NTERM	7:4	0x0	NPL Termination control N side
PDRV	11:8	0x0	NPL Drive control P side
NDRV	15:12	0x0	NPL Drive control N side
RECV_DUTY	17:16	0x0	Pad Receive Duty control

DRV_DUTY	19:18	0x0	Pad Drive Duty control
PREAMP	21:20	0x0	NPL Pre-emphasis enable select, [1:0] for finger [7:6], 0=>disable, 1=>enable
SELFTIME	22	0x0	Pad Pre-emphasis delay select
SLEW	24:23	0x0	Pad slew rate control
VMODE	25	0x0	Receive Default pull-up/down
VREF_INT	27:26	0x0	Vref select
Channel 0's command pad control parameters			

MC_IO_CMD_PAD_CNTL_I1 - RW - 32 bits - MCIND:0x8D			
Field Name	**Bits**	**Default**	**Description**
PTERM	3:0	0x0	NPL Termination control P side
NTERM	7:4	0x0	NPL Termination control N side
PDRV	11:8	0x0	NPL Drive control P side
NDRV	15:12	0x0	NPL Drive control N side
RECV_DUTY	17:16	0x0	Pad Receive Duty control
DRV_DUTY	19:18	0x0	Pad Drive Duty control
PREAMP	21:20	0x0	NPL Pre-emphasis enable select, [1:0] for finger [7:6], 0=>disable, 1=>enable
SELFTIME	22	0x0	Pad Pre-emphasis delay select
SLEW	24:23	0x0	Pad slew rate control
VMODE	25	0x0	Receive Default pull-up/down
VREF_INT	27:26	0x0	Vref select
Channel 1's command pad control parameters			

MC_IO_DQ_PAD_CNTL_I0 - RW - 32 bits - MCIND:0x8E			
Field Name	**Bits**	**Default**	**Description**
PTERM	3:0	0x0	NPL Termination control P side
NTERM	7:4	0x0	NPL Termination control N side
PDRV	11:8	0x0	NPL Drive control P side
NDRV	15:12	0x0	NPL Drive control N side
RECV_DUTY	17:16	0x0	Pad Receive Duty control
DRV_DUTY	19:18	0x0	Pad Drive Duty control
PREAMP	21:20	0x0	NPL Pre-emphasis enable select, [1:0] for finger [7:6], 0=>disable, 1=>enable
SELFTIME	22	0x0	Pad Pre-emphasis delay select
SLEW	24:23	0x0	Pad slew rate control
VMODE	25	0x0	Receive Default pull-up/down
VREF_INT	27:26	0x0	Vref select
Channel 0's data pad control parameters			

MC_IO_DQ_PAD_CNTL_I1 - RW - 32 bits - MCIND:0x8F			
Field Name	**Bits**	**Default**	**Description**
PTERM	3:0	0x0	NPL Termination control P side
NTERM	7:4	0x0	NPL Termination control N side
PDRV	11:8	0x0	NPL Drive control P side
NDRV	15:12	0x0	NPL Drive control N side
RECV_DUTY	17:16	0x0	Pad Receive Duty control
DRV_DUTY	19:18	0x0	Pad Drive Duty control

PREAMP	21:20	0x0	NPL Pre-emphasis enable select, [1:0] for finger [7:6], 0=>disable, 1=>enable
SELFTIME	22	0x0	Pad Pre-emphasis delay select
SLEW	24:23	0x0	Pad slew rate control
VMODE	25	0x0	Receive Default pull-up/down
VREF_INT	27:26	0x0	Vref select
Channel 1's data pad control parameters			

MC_IO_QS_PAD_CNTL_I0 - RW - 32 bits - MCIND:0x90			
Field Name	**Bits**	**Default**	**Description**
PTERM	3:0	0x0	NPL Termination control P side
NTERM	7:4	0x0	NPL Termination control N side
PDRV	11:8	0x0	NPL Drive control P side
NDRV	15:12	0x0	NPL Drive control N side
RECV_DUTY	17:16	0x0	Pad Receive Duty control
DRV_DUTY	19:18	0x0	Pad Drive Duty control
PREAMP	21:20	0x0	NPL Pre-emphasis enable select, [1:0] for finger [7:6], 0=>disable, 1=>enable
SELFTIME	22	0x0	Pad Pre-emphasis delay select
SLEW	24:23	0x0	Pad slew rate control
VMODE	25	0x0	Receive Default pull-up/down
VREF_INT	27:26	0x0	Vref select
Channel 0's strobe pad control parameters			

MC_IO_QS_PAD_CNTL_I1 - RW - 32 bits - MCIND:0x91			
Field Name	**Bits**	**Default**	**Description**
PTERM	3:0	0x0	NPL Termination control P side
NTERM	7:4	0x0	NPL Termination control N side
PDRV	11:8	0x0	NPL Drive control P side
NDRV	15:12	0x0	NPL Drive control N side
RECV_DUTY	17:16	0x0	Pad Receive Duty control
DRV_DUTY	19:18	0x0	Pad Drive Duty control
PREAMP	21:20	0x0	NPL Pre-emphasis enable select, [1:0] for finger [7:6], 0=>disable, 1=>enable
SELFTIME	22	0x0	Pad Pre-emphasis delay select
SLEW	24:23	0x0	Pad slew rate control
VMODE	25	0x0	Receive Default pull-up/down
VREF_INT	27:26	0x0	Vref select
Channel 1's strobe pad control parameters			

MC_IO_A_PAD_CNTL_I0 - RW - 32 bits - MCIND:0x92			
Field Name	**Bits**	**Default**	**Description**
PTERM	3:0	0x0	NPL Termination control P side
NTERM	7:4	0x0	NPL Termination control N side
PDRV	11:8	0x0	NPL Drive control P side
NDRV	15:12	0x0	NPL Drive control N side
RECV_DUTY	17:16	0x0	Pad Receive Duty control
DRV_DUTY	19:18	0x0	Pad Drive Duty control
PREAMP	21:20	0x0	NPL Pre-emphasis enable select, [1:0] for finger [7:6], 0=>disable, 1=>enable

SELFTIME	22	0x0	Pad Pre-emphasis delay select
SLEW	24:23	0x0	Pad slew rate control
VMODE	25	0x0	Receive Default pull-up/down
VREF_INT	27:26	0x0	Vref select
Channel 0's address pad control parameters			

MC_IO_A_PAD_CNTL_I1 - RW - 32 bits - MCIND:0x93			
Field Name	**Bits**	**Default**	**Description**
PTERM	3:0	0x0	NPL Termination control P side
NTERM	7:4	0x0	NPL Termination control N side
PDRV	11:8	0x0	NPL Drive control P side
NDRV	15:12	0x0	NPL Drive control N side
RECV_DUTY	17:16	0x0	Pad Receive Duty control
DRV_DUTY	19:18	0x0	Pad Drive Duty control
PREAMP	21:20	0x0	NPL Pre-emphasis enable select, [1:0] for finger [7:6], 0=>disable, 1=>enable
SELFTIME	22	0x0	Pad Pre-emphasis delay select
SLEW	24:23	0x0	Pad slew rate control
VMODE	25	0x0	Receive Default pull-up/down
VREF_INT	27:26	0x0	Vref select
Channel 1's address pad control parameters			

MC_IO_WR_DQ_CNTL_I0 - RW - 32 bits - MCIND:0x94			
Field Name	**Bits**	**Default**	**Description**
DLY0	4:0	0x0	Byte 3
DLY1	9:5	0x0	Byte 2
DLY2	14:10	0x0	Byte 1
DLY3	19:15	0x0	Byte 0
Channel 0's delay line parameters data bits. NOTE: Byte orders are swapped!!!			

MC_IO_WR_DQ_CNTL_I1 - RW - 32 bits - MCIND:0x95			
Field Name	**Bits**	**Default**	**Description**
DLY0	4:0	0x0	Byte 3
DLY1	9:5	0x0	Byte 2
DLY2	14:10	0x0	Byte 1
DLY3	19:15	0x0	Byte 0
Channel 1's delay line parameters data bits. NOTE: Byte orders are swapped!!!			

MC_IO_WR_QS_CNTL_I0 - RW - 32 bits - MCIND:0x96			
Field Name	**Bits**	**Default**	**Description**
DLY0	4:0	0x0	Byte 3
DLY1	9:5	0x0	Byte 2
DLY2	14:10	0x0	Byte 1
DLY3	19:15	0x0	Byte 0
Channel 0's delay line parameters strobe bits. NOTE: Byte orders are swapped!!!			

MC_IO_WR_QS_CNTL_I1 - RW - 32 bits - MCIND:0x97			
Field Name	**Bits**	**Default**	**Description**
DLY0	4:0	0x0	Byte 3
DLY1	9:5	0x0	Byte 2
DLY2	14:10	0x0	Byte 1
DLY3	19:15	0x0	Byte 0
Channel 1's delay line parameters strobe bits. NOTE: Byte orders are swapped!!!			

MC_VENDOR_ID_I0 - RW - 32 bits - MCIND:0x98			
Field Name	**Bits**	**Default**	**Description**
VALUE	31:0	0x0	Value returned by the DRAM data bus when the vendor ID is read.
Channel 0's vendor ID read back register.			

MC_VENDOR_ID_I1 - RW - 32 bits - MCIND:0x99			
Field Name	**Bits**	**Default**	**Description**
VALUE	31:0	0x0	Value returned by the DRAM data bus when the vendor ID is read.
Channel 1's vendor ID read back register. See MC_VENDOR_ID_I1.			

MC_NPL_STATUS_I0 - RW - 32 bits - MCIND:0x9A			
Field Name	**Bits**	**Default**	**Description**
PDELAY	1:0	0x0	Current Delay on CLKP
NDELAY	3:2	0x0	Current Delay on CLKN
PEARLY	4	0x0	Current CLKP is early than CLKN
NEARLY	5	0x0	Current CLKN is early than CLKP
Channel 0's NPL status.			

MC_NPL_STATUS_I1 - RW - 32 bits - MCIND:0x9B			
Field Name	**Bits**	**Default**	**Description**
PDELAY	1:0	0x0	Current Delay on CLKP
NDELAY	3:2	0x0	Current Delay on CLKN
PEARLY	4	0x0	Current CLKP is early than CLKN
NEARLY	5	0x0	Current CLKN is early than CLKP
Channel 1's NPL status.			

MC_IO_RD_QS2_CNTL_I0 - RW - 32 bits - MCIND:0x9C			
Field Name	**Bits**	**Default**	**Description**
DLY0	7:0	0x0	
DLY1	15:8	0x0	
DLY2	23:16	0x0	
DLY3	31:24	0x0	

MC_IO_RD_QS2_CNTL_I1 - RW - 32 bits - MCIND:0x9D			
Field Name	**Bits**	**Default**	**Description**
DLY0	7:0	0x0	
DLY1	15:8	0x0	
DLY2	23:16	0x0	
DLY3	31:24	0x0	

MC_IMP_CNTL - RW - 32 bits - MCIND:0xA0			
Field Name	**Bits**	**Default**	**Description**
MEM_IO_UPDATE_RATE	4:0	0x16	Calibration update rate. The programmed value is exponential.
MEM_IO_SAMPLE_DELAY	12:8	0x6	Calibration sample delay. The programmed value is exponential.
MEM_IO_INC_THRESHOLD	20:16	0x18	Calibration increment threshold.
MEM_IO_DEC_THRESHOLD	28:24	0x8	Calibration decrement threshold.
CAL_WHEN_IDLE	29	0x0	Calibration during idle. 0=Disable 1=Enable
CAL_WHEN_REFRESH	30	0x0	Calibration during refresh. 0=Disable 1=Enable
MEM_IMP_EN	31	0x0	Impedance controller enable. 0=Disable 1=Enable
Impedance control control register. Channel pair B only.			

MC_IMP_DEBUG - RW - 32 bits - MCIND:0xA1			
Field Name	**Bits**	**Default**	**Description**
MEM_IMP_DEBUG_N	3:0	0x0	Debug value for N drive.
MEM_IMP_DEBUG_P	7:4	0x0	Debug value for P drive.
MEM_IO_IMP_DEBUG_EN	8	0x0	Impedance debug enable. 0=Disable 1=Enable
Impedance control debug register. Channel pair B only.			

MC_IMP_STATUS - RW - 32 bits - MCIND:0xA2			
Field Name	**Bits**	**Default**	**Description**
IMP_N_MEM_DQ_SN_I0 (R)	3:0	0x0	N drive strength of sequencer 0 data byte 0.
IMP_P_MEM_DQ_SP_I0 (R)	7:4	0x0	
IMP_N_MEM_DQ_SN_I1 (R)	11:8	0x0	N drive strength of sequencer 1 data byte 0.
IMP_P_MEM_DQ_SP_I1 (R)	15:12	0x0	

IMP_N_VALUE_R_BACK (R)	19:16	0x0	Calibrated N drive read back value.
IMP_P_VALUE_R_BACK (R)	23:20	0x0	Calibrated P drive read back value.
IMP_CAL_COUNT (R)	27:24	0x0	Impedance calibrated count.
TEST_OUT_R_BACK (R)	28	0x0	Test output read back value.
DUMMY_OUT_R_BACK (R)	29	0x0	Dummy output read back value.
Impedance control status register. Channel pair B only.			

MC_RBS_MAP - RW - 32 bits - MCIND:0xB0			
Field Name	**Bits**	**Default**	**Description**
DIR0	1:0	0x0	Selects route to node 0. 0=ClocKWise 1=Counter-ClockWise 2=BYPass 3=TIE
DIR1	3:2	0x0	Selects route to node 1. 0=ClocKWise 1=Counter-ClockWise 2=BYPass 3=TIE
DIR2	5:4	0x0	Selects route to node 2. 0=ClocKWise 1=Counter-ClockWise 2=BYPass 3=TIE
DIR3	7:6	0x0	Selects route to node 3. 0=ClocKWise 1=Counter-ClockWise 2=BYPass 3=TIE
DIR4	9:8	0x0	Selects route to node 4. 0=ClocKWise 1=Counter-ClockWise 2=BYPass 3=TIE
CKW0	11:10	0x0	Selects flow control signals from node 0 in clockwise route. 0=Group 0 1=Group 1 2=Group 2 3=Block
CKW1	13:12	0x0	Selects flow control signals from node 1 in clockwise route. 0=Group 0 1=Group 1 2=Group 2 3=Block
CKW2	15:14	0x0	Selects flow control signals from node 2 in clockwise route. 0=Group 0 1=Group 1 2=Group 2 3=Block
CKW3	17:16	0x0	Selects flow control signals from node 3 in clockwise route. 0=Group 0 1=Group 1 2=Group 2 3=Block
CKW4	19:18	0x0	Selects flow control signals from node 4 in clockwise route. 0=Group 0 1=Group 1 2=Group 2 3=Block

CCW0	21:20	0x0	Selects flow control signals from node 0 in counter-clockwise route. 0=Group 0 1=Group 1 2=Group 2 3=Block
CCW1	23:22	0x0	Selects flow control signals from node 1 in counter-clockwise route. 0=Group 0 1=Group 1 2=Group 2 3=Block
CCW2	25:24	0x0	Selects flow control signals from node 2 in counter-clockwise route. 0=Group 0 1=Group 1 2=Group 2 3=Block
CCW3	27:26	0x0	Selects flow control signals from node 3 in counter-clockwise route. 0=Group 0 1=Group 1 2=Group 2 3=Block
CCW4	29:28	0x0	Selects flow control signals from node 4 in counter-clockwise route. 0=Group 0 1=Group 1 2=Group 2 3=Block
NID	31:30	0x0	Node identification. 0 to 3 for SQ nodes. 0 for the only AC node.
Controls data routing in RBS.			

MC_RBS_CZT_HWM - RW - 32 bits - MCIND:0xB1			
Field Name	**Bits**	**Default**	**Description**
RBP	5:0	0x16	High water mark for color and z read return FIFOs
RBT	13:8	0x16	High water mark for texture read return FIFO.
XBF	21:16	0x16	High water mark for mclk-to-sclk async FIFO.
High water marks for different FIFOs inside a SQ tile.			

MC_RBS_SUN_HWM - RW - 32 bits - MCIND:0xB2			
Field Name	**Bits**	**Default**	**Description**
RBC	5:0	0x16	High water mark for CP/VF read return FIFO.
RBD	13:8	0x16	High water mark for display read return FIFO.
RBG	21:16	0x16	High water mark for global read bus return FIFO.
High water marks for different FIFOs inside a AC tile.			

MC_RBS_MISC - RW - 32 bits - MCIND:0xB3			
Field Name	**Bits**	**Default**	**Description**
DAT_INV	0	0x0	Read data inversion control. 0=Disable read data inversion 1=Enable read data inversion
MSK_DF1	1	0x1	Data inversion mask polarity. 0=Inverse mask active low 1=Inverse mask active high
Misc. RBS control register.			

MC_PMG_CMD - RW - 32 bits - MCIND:0xE0			
Field Name	**Bits**	**Default**	**Description**
ADR	15:0	0x0	The value of the mode register for resetting DRAM DLL.
MOP	18:16	0x0	This field is not used. 0=NOP 1=Load mode register 2=Precharge 3=Auto-refresh 4=Self-refresh
END	20	0x0	This field is not used. 0=Not last operation 1=Last operation, wait for DLL to stabilize
CSB	22:21	0x0	This field is not used. 0=Select both ranks 1=Select rank 1 2=Select rank 0 3=Select none
Power manager command register. This register specifies the value used for resetting the DRAM DLL.			

MC_PMG_CFG - RW - 32 bits - MCIND:0xE1			
Field Name	**Bits**	**Default**	**Description**
SYC_CLK	0	0x0	Controls mclk/yclk synchronization after on-chip DLL is reset. 0=Don't synchronize YCLK/MCLK after DLL is reset 1=Synchronize YCLK/MCLK after DLL is reset
RST_DLL	1	0x0	Controls DRAM DLL reset after waking up from self-refresh. 0=Don't reset DRAM DLL after self-refresh 1=Reset DRAM DLL after self-refresh
TRI_MIO	2	0x0	Controls memory IO tristate during power down. 0=Don't reset DRAM DLL after self-refresh 1=Reset DRAM DLL after self-refresh
XSR_TMR	7:4	0x0	Multiple of 16 mclk cycles to wait before resetting DRAM DLL.
Power manager configuration register.			

MC_MISC_0 - RW - 32 bits - MCIND:0xF0			
Field Name	**Bits**	**Default**	**Description**
MISC0	31:0	0x0	32-bit storage.
Dummy register for temporary storage.			

MC_MISC_1 - RW - 32 bits - MCIND:0xF1			
Field Name	**Bits**	**Default**	**Description**
MISC1	31:0	0x0	32-bit storage.
Dummy register for temporary storage.			

MC_DEBUG - RW - 32 bits - MCIND:0xFE			
Field Name	**Bits**	**Default**	**Description**

MC_DLL_TSTOUT_SEL	5:0	0x0	Control bits in DLL [5:4] TSTCLK2 Mux select 0=ref_pd 1=fb_pd 2=DLL_in 3= DLL_out [3] Inv TSTCLK2 0=normal 1=invert [2:1] TSTCLK1 Mux select 0=ref_clk 1=fb_pd 2=DLL_in 3= DLL_out [0] Inv TSTCLK1 0=normal 1=invert
MC_DLL_TSTOUT_EN	6	0x0	TEST_YCLK/MCLK output mux select
MC_SEL_DLL_TSTOUT	7	0x0	DLL debug output mux select
DLL debug register NOTE: CORRECT definition MC_DLL_TSTOUT_SEL2 0 MC_DLL_TSTOUT_SEL3 1 MC_DLL_TSTOUT_SEL4 2 MC_DLL_TSTOUT_SEL5 3 MC_DLL_TSTOUT_EN 4 MC_SEL_DLL_TSTOUT 5 MC_DLL_TSTOUT_SEL1 6 MC_DLL_TSTOUT_SEL0 7			

MC_PT0_CNTL - RW - 32 bits - MCIND:0x100			
Field Name	**Bits**	**Default**	**Description**
ENABLE_PAGE_TABLES	0	0x0	0=off 1=on
SURFACE_PROBES	2:1	0x0	0=ignore 1=always pass 2=check probe 3=reserved
ISSUE_L3_CACHE_REQUESTS	3	0x0	0=no 1=yes
ACCEPT_L3_CACHE_REQUESTS	4	0x0	0=no 1=yes
SURFACE_PROBE_FAULTS	6:5	0x0	0=ignore 1=interrupt + continue 2=reserved 3=interrupt + halt
VALID_PROTECTION_FAULTS	8:7	0x0	0=ignore 1=interrupt + continue 2=reserved 3=interrupt + halt
READ_PROTECTION_FAULTS	10:9	0x0	0=ignore 1=interrupt + continue 2=reserved 3=interrupt + halt
WRITE_PROTECTION_FAULTS	12:11	0x0	0=ignore 1=interrupt + continue 2=reserved 3=interrupt + halt
PRIVILEGED_PROTECTION_FAULTS	14:13	0x0	0=ignore 1=interrupt + continue 2=reserved 3=interrupt + halt
EFFECTIVE_L2_CACHE_SIZE	18:15	0x7	(0...7) 2**(field) cache lines or 2**(5+field) bytes
CLEAR_SURFACE_PROBE_FAULT_STATUS	19	0x0	write 1 to clear fault status which occurs on rising edge 0=normal operation 1=clear
CLEAR_PROTECTION_FAULT_STATUS	20	0x0	write 1 to clear fault status which occurs on rising edge 0=normal operation 1=clear
EFFECTIVE_L2_QUEUE_SIZE	24:21	0x7	(3...7) 2**(field) latency compensation queue entries
ENABLE_SURFACE_PROBE_FLOW_CONTROL	25	0x0	0=off 1=on

ACKNOWLEDGE_SURFACE_PROBE_FAULT_INTERRUPT (W)	26	0x0	acknowledgement occurs on rising edge 0=normal operation 1=acknowledge
ACKNOWLEDGE_PROTECTION_FAULT_INTERRUPT (W)	27	0x0	acknowledgement occurs on rising edge 0=normal operation 1=acknowledge
INVALIDATE_ALL_L1_TLBS (W)	28	0x0	invalidation occurs on rising edge 0=normal operation 1=invalidate
INVALIDATE_L2_CACHE (W)	29	0x0	invalidation occurs on rising edge 0=normal operation 1=invalidate
This register provides control for Page Table Unit 0.			

MC_PT0_CONTEXT0_CNTL - RW - 32 bits - MCIND:0x102			
Field Name	**Bits**	**Default**	**Description**
ENABLE_PAGE_TABLE	0	0x0	l1 client will treat addresses as physical if context page table is off 0=off 1=on
PAGE_TABLE_TYPE	1	0x0	0=flat 1=multi-level
ENABLE_PRIVILEGED_MODE	2	0x0	0=off 1=on
This register provides control for Context 0 in Page Table Unit 0.			

MC_PT0_CONTEXT1_CNTL - RW - 32 bits - MCIND:0x103			
Field Name	**Bits**	**Default**	**Description**
ENABLE_PAGE_TABLE	0	0x0	l1 client will treat addresses as physical if context page table is off 0=off 1=on
PAGE_TABLE_TYPE	1	0x0	0=flat 1=multi-level
ENABLE_PRIVILEGED_MODE	2	0x0	0=off 1=on
This register provides control for Context 1 in Page Table Unit 0.			

MC_PT0_CONTEXT2_CNTL - RW - 32 bits - MCIND:0x104			
Field Name	**Bits**	**Default**	**Description**
ENABLE_PAGE_TABLE	0	0x0	l1 client will treat addresses as physical if context page table is off 0=off 1=on
PAGE_TABLE_TYPE	1	0x0	0=flat 1=multi-level
ENABLE_PRIVILEGED_MODE	2	0x0	0=off 1=on
This register provides control for Context 2 in Page Table Unit 0.			

MC_PT0_CONTEXT3_CNTL - RW - 32 bits - MCIND:0x105			
Field Name	**Bits**	**Default**	**Description**

ENABLE_PAGE_TABLE	0	0x0	I1 client will treat addresses as physical if context page table is off 0=off 1=on
PAGE_TABLE_TYPE	1	0x0	0=flat 1=multi-level
ENABLE_PRIVILEGED_MODE	2	0x0	0=off 1=on
This register provides control for Context 3 in Page Table Unit 0.			

MC_PT0_CONTEXT4_CNTL - RW - 32 bits - MCIND:0x106			
Field Name	**Bits**	**Default**	**Description**
ENABLE_PAGE_TABLE	0	0x0	I1 client will treat addresses as physical if context page table is off 0=off 1=on
PAGE_TABLE_TYPE	1	0x0	0=flat 1=multi-level
ENABLE_PRIVILEGED_MODE	2	0x0	0=off 1=on
This register provides control for Context 4 in Page Table Unit 0.			

MC_PT0_CONTEXT5_CNTL - RW - 32 bits - MCIND:0x107			
Field Name	**Bits**	**Default**	**Description**
ENABLE_PAGE_TABLE	0	0x0	I1 client will treat addresses as physical if context page table is off 0=off 1=on
PAGE_TABLE_TYPE	1	0x0	0=flat 1=multi-level
ENABLE_PRIVILEGED_MODE	2	0x0	0=off 1=on
This register provides control for Context 5 in Page Table Unit 0.			

MC_PT0_CONTEXT6_CNTL - RW - 32 bits - MCIND:0x108			
Field Name	**Bits**	**Default**	**Description**
ENABLE_PAGE_TABLE	0	0x0	I1 client will treat addresses as physical if context page table is off 0=off 1=on
PAGE_TABLE_TYPE	1	0x0	0=flat 1=multi-level
ENABLE_PRIVILEGED_MODE	2	0x0	0=off 1=on
This register provides control for Context 6 in Page Table Unit 0.			

MC_PT0_CONTEXT7_CNTL - RW - 32 bits - MCIND:0x109			
Field Name	**Bits**	**Default**	**Description**
ENABLE_PAGE_TABLE	0	0x0	l1 client will treat addresses as physical if context page table is off 0=off 1=on
PAGE_TABLE_TYPE	1	0x0	0=flat 1=multi-level
ENABLE_PRIVILEGED_MODE	2	0x0	0=off 1=on
This register provides control for Context 7 in Page Table Unit 0.			

MC_PT0_SYSTEM_APERTURE_LOW_ADDR - RW - 32 bits - MCIND:0x112			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_PAGE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the low end of the translatable address range when using the system context in Page Table Unit 0. This address must be aligned on a 4k-page boundary - the lower 12 bits will be treated as zero. The mapping range for the system aperture is inclusive between the low and high addresses.			

MC_PT0_SYSTEM_APERTURE_HIGH_ADDR - RW - 32 bits - MCIND:0x114			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_PAGE_ADDR	31:0	0xfff	NOTE: Bits 0:11 of this field are hardwired to ONE.
This register defines the high end of the translatable address range when using the system context in Page Table Unit 0. This address must be aligned on a 4k-page boundary -- the lower 12 bits will be treated as set. The mapping range for the system aperture is inclusive between the low and high addresses.			

MC_PT0_SURFACE_PROBE - W - 32 bits - MCIND:0x116			
Field Name	**Bits**	**Default**	**Description**
PROTECTIONS	3:0	0x0	bit 0: valid (0x1) bit 1: read (0x2) bit 2: write (0x4) bit 3: privileged (0x8) verify page address against these protection modes
CONTEXT	6:4	0x0	other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
LOGICAL_PAGE_ADDR	31:12	0x0	logical page address to be probed
This register initiates a surface probe sequence in Page Table Unit 0. The page address must be on a 4K-byte boundary. If handling of surface probes is not enabled, they are reported as always passing. Although both PT units contain this register, only PT0 can process surface probes.			

MC_PT0_SURFACE_PROBE_FAULT_STATUS - R - 32 bits - MCIND:0x118			
Field Name	**Bits**	**Default**	**Description**
PROTECTIONS	3:0	0x0	bit 0: valid (0x1) bit 1: read (0x2) bit 2: write (0x4) bit 3: privileged (0x8) indicates failing protection modes for page address
CONTEXT	6:4	0x0	other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
LOGICAL_PAGE_ADDR	31:12	0x0	logical page address of most recent fault
This register reports the most recent failing surface probe status in Page Table Unit 0. Although both PT units contain this register, only PT0 can process surface probes.			

MC_PT0_PROTECTION_FAULT_STATUS - R - 32 bits - MCIND:0x11A			
Field Name	**Bits**	**Default**	**Description**
PROTECTIONS	3:0	0x0	bit 0: valid (0x1) bit 1: read (0x2) bit 2: write (0x4) bit 3: privileged (0x8) indicates failing protection modes for page address
CONTEXT	6:4	0x0	other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
MEMORY_CLIENT_ID	11:7	0x0	(0...31)
LOGICAL_PAGE_ADDR	31:12	0x0	logical page address of most recent fault
This register reports the most recent failing protection fault status in Page Table Unit 0.			

MC_PT0_CONTEXT0_DEFAULT_READ_ADDR - RW - 32 bits - MCIND:0x11C			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_PAGE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical page address used for ignored protection faults while reading in Page Table Unit 0 Context 0. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT1_DEFAULT_READ_ADDR - RW - 32 bits - MCIND:0x11D			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_PAGE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical page address used for ignored protection faults while reading in Page Table Unit 0 Context 1. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT2_DEFAULT_READ_ADDR - RW - 32 bits - MCIND:0x11E			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_PAGE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical page address used for ignored protection faults while reading in Page Table Unit 0 Context 2. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT3_DEFAULT_READ_ADDR - RW - 32 bits - MCIND:0x11F			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_PAGE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical page address used for ignored protection faults while reading in Page Table Unit 0 Context 3. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT4_DEFAULT_READ_ADDR - RW - 32 bits - MCIND:0x120			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_PAGE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical page address used for ignored protection faults while reading in Page Table Unit 0 Context 4. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT5_DEFAULT_READ_ADDR - RW - 32 bits - MCIND:0x121			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_PAGE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical page address used for ignored protection faults while reading in Page Table Unit 0 Context 5. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT6_DEFAULT_READ_ADDR - RW - 32 bits - MCIND:0x122			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_PAGE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical page address used for ignored protection faults while reading in Page Table Unit 0 Context 6. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT7_DEFAULT_READ_ADDR - RW - 32 bits - MCIND:0x123			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_PAGE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical page address used for ignored protection faults while reading in Page Table Unit 0 Context 7. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT0_FLAT_BASE_ADDR - RW - 32 bits - MCIND:0x12C			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the flat page table for Context 0 in Page Table Unit 0. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT1_FLAT_BASE_ADDR - RW - 32 bits - MCIND:0x12D			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the flat page table for Context 1 in Page Table Unit 0. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT2_FLAT_BASE_ADDR - RW - 32 bits - MCIND:0x12E			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the flat page table for Context 2 in Page Table Unit 0. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT3_FLAT_BASE_ADDR - RW - 32 bits - MCIND:0x12F			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the flat page table for Context 3 in Page Table Unit 0. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT4_FLAT_BASE_ADDR - RW - 32 bits - MCIND:0x130			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the flat page table for Context 4 in Page Table Unit 0. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT5_FLAT_BASE_ADDR - RW - 32 bits - MCIND:0x131			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the flat page table for Context 5 in Page Table Unit 0. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT6_FLAT_BASE_ADDR - RW - 32 bits - MCIND:0x132			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the flat page table for Context 6 in Page Table Unit 0. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT7_FLAT_BASE_ADDR - RW - 32 bits - MCIND:0x133			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the flat page table for Context 7 in Page Table Unit 0. The page address must be on a 4K-byte boundary.			

MC_PT0_CONTEXT0_FLAT_START_ADDR - RW - 32 bits - MCIND:0x13C			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_START_ADDR	31:0	0x0	NOTE: Bits 0:20 of this field are hardwired to ZERO.
This register defines the starting logical address in the flat page table for Context 0 in Page Table Unit 0. This logical address must begin on a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT1_FLAT_START_ADDR - RW - 32 bits - MCIND:0x13D			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_START_ADDR	31:0	0x0	NOTE: Bits 0:20 of this field are hardwired to ZERO.
This register defines the starting logical address in the flat page table for Context 1 in Page Table Unit 0. This logical address must begin on a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT2_FLAT_START_ADDR - RW - 32 bits - MCIND:0x13E			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_START_ADDR	31:0	0x0	NOTE: Bits 0:20 of this field are hardwired to ZERO.
This register defines the starting logical address in the flat page table for Context 2 in Page Table Unit 0. This logical address must begin on a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT3_FLAT_START_ADDR - RW - 32 bits - MCIND:0x13F			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_START_ADDR	31:0	0x0	NOTE: Bits 0:20 of this field are hardwired to ZERO.
This register defines the starting logical address in the flat page table for Context 3 in Page Table Unit 0. This logical address must begin on a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT4_FLAT_START_ADDR - RW - 32 bits - MCIND:0x140			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_START_ADDR	31:0	0x0	NOTE: Bits 0:20 of this field are hardwired to ZERO.
This register defines the starting logical address in the flat page table for Context 4 in Page Table Unit 0. This logical address must begin on a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT5_FLAT_START_ADDR - RW - 32 bits - MCIND:0x141			
Field Name	**Bits**	**Default**	**Description**

LOGICAL_START_ADDR	31:0	0x0	NOTE: Bits 0:20 of this field are hardwired to ZERO.
This register defines the starting logical address in the flat page table for Context 5 in Page Table Unit 0. This logical address must begin on a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT6_FLAT_START_ADDR - RW - 32 bits - MCIND:0x142			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_START_ADDR	31:0	0x0	NOTE: Bits 0:20 of this field are hardwired to ZERO.
This register defines the starting logical address in the flat page table for Context 6 in Page Table Unit 0. This logical address must begin on a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT7_FLAT_START_ADDR - RW - 32 bits - MCIND:0x143			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_START_ADDR	31:0	0x0	NOTE: Bits 0:20 of this field are hardwired to ZERO.
This register defines the starting logical address in the flat page table for Context 7 in Page Table Unit 0. This logical address must begin on a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT0_FLAT_END_ADDR - RW - 32 bits - MCIND:0x14C			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_END_ADDR	31:0	0x1fffff	NOTE: Bits 0:20 of this field are hardwired to ONE.
This register defines the ending logical address in the flat page table for Context 0 in Page Table Unit 0. This logical address must fall immediately before a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT1_FLAT_END_ADDR - RW - 32 bits - MCIND:0x14D			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_END_ADDR	31:0	0x1fffff	NOTE: Bits 0:20 of this field are hardwired to ONE.
This register defines the ending logical address in the flat page table for Context 1 in Page Table Unit 0. This logical address must fall immediately before a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT2_FLAT_END_ADDR - RW - 32 bits - MCIND:0x14E			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_END_ADDR	31:0	0x1fffff	NOTE: Bits 0:20 of this field are hardwired to ONE.
This register defines the ending logical address in the flat page table for Context 2 in Page Table Unit 0. This logical address must fall immediately before a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT3_FLAT_END_ADDR - RW - 32 bits - MCIND:0x14F			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_END_ADDR	31:0	0x1fffff	NOTE: Bits 0:20 of this field are hardwired to ONE.

This register defines the ending logical address in the flat page table for Context 3 in Page Table Unit 0. This logical address must fall immediately before a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.

MC_PT0_CONTEXT4_FLAT_END_ADDR - RW - 32 bits - MCIND:0x150			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_END_ADDR	31:0	0x1fffff	NOTE: Bits 0:20 of this field are hardwired to ONE.
This register defines the ending logical address in the flat page table for Context 4 in Page Table Unit 0. This logical address must fall immediately before a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT5_FLAT_END_ADDR - RW - 32 bits - MCIND:0x151			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_END_ADDR	31:0	0x1fffff	NOTE: Bits 0:20 of this field are hardwired to ONE.
This register defines the ending logical address in the flat page table for Context 5 in Page Table Unit 0. This logical address must fall immediately before a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT6_FLAT_END_ADDR - RW - 32 bits - MCIND:0x152			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_END_ADDR	31:0	0x1fffff	NOTE: Bits 0:20 of this field are hardwired to ONE.
This register defines the ending logical address in the flat page table for Context 6 in Page Table Unit 0. This logical address must fall immediately before a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT7_FLAT_END_ADDR - RW - 32 bits - MCIND:0x153			
Field Name	**Bits**	**Default**	**Description**
LOGICAL_END_ADDR	31:0	0x1fffff	NOTE: Bits 0:20 of this field are hardwired to ONE.
This register defines the ending logical address in the flat page table for Context 7 in Page Table Unit 0. This logical address must fall immediately before a 2M-byte boundary. The mapping range is inclusive between starting and ending addresses. If the ending address is less than the starting address, all mappings will be invalid.			

MC_PT0_CONTEXT0_MULTI_LEVEL_BASE_ADDR - RW - 32 bits - MCIND:0x15C			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the multi-level page table for Context 0 in Page Table Unit 0. This physical address must begin on a 4K-byte boundary.			

MC_PT0_CONTEXT1_MULTI_LEVEL_BASE_ADDR - RW - 32 bits - MCIND:0x15D			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the multi-level page table for Context 1 in Page Table Unit 0. This physical address must begin on a 4K-byte boundary.			

MC_PT0_CONTEXT2_MULTI_LEVEL_BASE_ADDR - RW - 32 bits - MCIND:0x15E			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the multi-level page table for Context 2 in Page Table Unit 0. This physical address must begin on a 4K-byte boundary.			

MC_PT0_CONTEXT3_MULTI_LEVEL_BASE_ADDR - RW - 32 bits - MCIND:0x15F			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the multi-level page table for Context 3 in Page Table Unit 0. This physical address must begin on a 4K-byte boundary.			

MC_PT0_CONTEXT4_MULTI_LEVEL_BASE_ADDR - RW - 32 bits - MCIND:0x160			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the multi-level page table for Context 4 in Page Table Unit 0. This physical address must begin on a 4K-byte boundary.			

MC_PT0_CONTEXT5_MULTI_LEVEL_BASE_ADDR - RW - 32 bits - MCIND:0x161			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the multi-level page table for Context 5 in Page Table Unit 0. This physical address must begin on a 4K-byte boundary.			

MC_PT0_CONTEXT6_MULTI_LEVEL_BASE_ADDR - RW - 32 bits - MCIND:0x162			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the multi-level page table for Context 6 in Page Table Unit 0. This physical address must begin on a 4K-byte boundary.			

MC_PT0_CONTEXT7_MULTI_LEVEL_BASE_ADDR - RW - 32 bits - MCIND:0x163			
Field Name	**Bits**	**Default**	**Description**
PHYSICAL_BASE_ADDR	31:0	0x0	NOTE: Bits 0:11 of this field are hardwired to ZERO.
This register defines the physical base address of the multi-level page table for Context 7 in Page Table Unit 0. This physical address must begin on a 4K-byte boundary.			

MC_PT0_CLIENT0_CNTL - RW - 32 bits - MCIND:0x16C			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)

TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 0 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT1_CNTL - RW - 32 bits - MCIND:0x16D			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct

CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 1 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT2_CNTL - RW - 32 bits - MCIND:0x16E			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped

SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 2 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT3_CNTL - RW - 32 bits - MCIND:0x16F			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable

BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 3 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT4_CNTL - RW - 32 bits - MCIND:0x170			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 4 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT5_CNTL - RW - 32 bits - MCIND:0x171			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 5 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT6_CNTL - RW - 32 bits - MCIND:0x172			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on

CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 6 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT7_CNTL - RW - 32 bits - MCIND:0x173			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 7 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT8_CNTL - RW - 32 bits - MCIND:0x174			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on

CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 8 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT9_CNTL - RW - 32 bits - MCIND:0x175			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct

CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 9 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT10_CNTL - RW - 32 bits - MCIND:0x176			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped

SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 10 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT11_CNTL - RW - 32 bits - MCIND:0x177			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable

BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 11 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT12_CNTL - RW - 32 bits - MCIND:0x178			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 12 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT13_CNTL - RW - 32 bits - MCIND:0x179			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 13 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT14_CNTL - RW - 32 bits - MCIND:0x17A			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 14 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT15_CNTL - RW - 32 bits - MCIND:0x17B			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on

CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 15 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

MC_PT0_CLIENT16_CNTL - RW - 32 bits - MCIND:0x17C			
Field Name	**Bits**	**Default**	**Description**
ENABLE_TRANSLATION_MODE_OVERRIDE	0	0x0	can override translation mode requested by memory client at pt/l1 interface 0=no (obey client request) 1=yes (override client request)
TRANSLATION_MODE_OVERRIDE	1	0x0	l1 client will follow system access mode when translation is off 0=always translate off 1=always translate on
CONTEXT_SELECTION_0	4:2	0x0	context to use when interface context selection bit is 0. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct

CONTEXT_SELECTION_1	7:5	0x0	context to use when interface context selection bit is 1. other than system context, these assignments are suggestions only -- the driver will determine actual assignments. 0=system 1=gpu 2=host 3=idct
SYSTEM_ACCESS_MODE	9:8	0x0	values 1 and 2 are meaningful iff system context 0 itself is enabled 0=always physical access 1=always logical access via system context 0 page table 2=inside system aperture is mapped, outside is unmapped 3=inside system aperture is unmapped, outside is mapped
SYSTEM_APERTURE_UNMAPPED_ACCESS	10	0x0	mapped accesses (inside aperture) always go through system context 0 page table 0=pass through (physical access) 1=discard write, read from default address
EFFECTIVE_L1_CACHE_SIZE	13:11	0x3	(0...4) 2**(field) page table entries
ENABLE_FRAGMENT_PROCESSING	14	0x0	0=off 1=on
EFFECTIVE_L1_QUEUE_SIZE	17:15	0x3	(0...4) 2**(field) latency compensation queue entries
ENABLE_PROTECTION_FAULTS	18	0x1	enable/disable protection fault processing for this client 0=disable 1=enable
BYPASS_L2_CACHE	19	0x0	bypass L2 cache to test L1 client functionality with effective identity map 0=use L2 cache 1=bypass L2 cache test only
INVALIDATE_L1_TLB (W)	20	0x0	invalidate only the contents of the L1 TLB on rising edge 0=normal operation 1=invalidate L1 TLB
This register provides static control for Client 16 in Page Table Unit 0. There are currently 21 read clients and 12 write clients, so each Page Table Unit will service roughly 17 clients.			

2.2 Bus Interface Registers

GENENB - R - 8 bits - HIDEC:0x3C3			
Field Name	**Bits**	**Default**	**Description**
BLK_IO_BASE	7:0	0x0	I/O base address
Legacy register for VGA			

MM_INDEX - RW - 32 bits - HIDEC:0x0			
Field Name	**Bits**	**Default**	**Description**
MM_OFFSET	30:0	0x0	This field specifies the offset (in MM space) of the register or the offset in FB memory to be accessed. All accesses must be dword aligned, therefore, bits 1:0 are tied to zero. NOTE: Bits 0:1 of this field are hardwired to ZERO.
MM_APER	31	0x0	This bit specifies which aperture the access is for, Register aperture, or FB aperture (Linear Aperture). 0=Register Aperture 1=Linear Aperture 0
General Memory Access. The MM_INDEX and MM_DATA pair of registers are used to indirectly accessed all other BIF memory mapped registers and the Frame buffer.			

MM_DATA - RW - 32 bits - HIDEC:0x4			
Field Name	**Bits**	**Default**	**Description**
MM_DATA	31:0	0x0	This field contains the data to be written to or the data read from the address specified in MM_INDEX.
General Memory Access. The MM_INDEX and MM_DATA pair of registers are used to indirectly accessed all other BIF memory mapped registers and the Frame buffer.			

BUS_CNTL - RW - 32 bits - HIDEC:0x4C			
Field Name	**Bits**	**Default**	**Description**
BUS_DBL_RESYNC	0	0x1	0=Normal 1=Add extra resynchronizing clock
BIOS_ROM_WRT_EN	1	0x0	0=Disable 1=Enable
BIOS_ROM_DIS	2	0x0	0=Enable 1=Disable
PMI_IO_DIS	3	0x0	The PMI_STATUS.PMI_POWER_STATE is used program the power state. If the power state is D1-D3, then IO access is disabled. This bit, if set to 1, will disabled this behaviour. Meaning, it will enabled IO access. 0=Normal 1=Disable
PMI_MEM_DIS	4	0x0	The PMI_STATUS.PMI_POWER_STATE is used program the power state. If the power state is D1-D3, then MEM access is disabled. This bit, if set to 1, will disabled this behaviour. Meaning, it will enabled MEM access. 0=Normal 1=Disable

PMI_BM_DIS	5	0x0	The PMI_STATUS.PMI_POWER_STATE is used program the power state. If the power state is D1-D3, then busmastering is disabled. This bit, if set to 1, will disabled this behaviour. Meaning, it will enabled busmastering. 0=Normal 1=Disable
PMI_INT_DIS	6	0x0	The PMI_STATUS.PMI_POWER_STATE is used program the power state. If the power state is D1-D3, then interrupt is disabled. This bit, if set to 1, will disabled this behaviour. Meaning, it will enabled interrupt. 0=Normal 1=Disable
IMMEDIATE_PMI_DIS	7	0x0	0=Enable 1=Disable
VGA_REG_COHERENCY_DIS	8	0x0	0=Enable 1=Disable
VGA_MEM_COHERENCY_DIS	9	0x0	0=Enable 1=Disable
HDP_REG_COHERENCY_DIS	10	0x0	0=Enable 1=Disable
GUI_INITIATOR_COHERENCY_DIS	11	0x0	0=Enable 1=Disable
VAP_REG_COHERENCY_DIS	12	0x0	disable VAP registers coherency. 0=Enable 1=Disable

PCI Express Bus Control Register

CONFIG_CNTL - RW - 32 bits - HIDEC:0xE0			
Field Name	**Bits**	**Default**	**Description**
APER_REG_ENDIAN	5:4	0x0	0=No swapping 1=Swap both register apertures (32bpp swapping) 2=Swap register aperture 1 3=Swap register aperture 0
CFG_VGA_RAM_EN (R)	8	0x0	0=Disable 1=Enable
VGA_DIS	9	0x0	VGA Disable
Reserved	19:16	0x0	

Configuration Control Register

CONFIG_MEMSIZE - RW - 32 bits - HIDEC:0xF8			
Field Name	**Bits**	**Default**	**Description**
CONFIG_MEMSIZE	31:0	0x0	Configuration memory size NOTE: Bits 0:19 of this field are hardwired to ZERO.

Scratch register for BIOS to inform driver memory size

CONFIG_APER_0_BASE - R - 32 bits - HIDEC:0x100			
Field Name	**Bits**	**Default**	**Description**
APER_0_BASE	31:0	0x0	Aperture 0 Base NOTE: Bits 0:24 of this field are hardwired to ZERO.

Configuration Aperture 0 Base Register

CONFIG_APER_1_BASE - R - 32 bits - HIDEC:0x104			
Field Name	**Bits**	**Default**	**Description**
APER_1_BASE	31:0	0x0	Aperture 1 Base NOTE: Bits 0:23 of this field are hardwired to ZERO.

Configuration Aperture 1 Base Register

CONFIG_APER_SIZE - R - 32 bits - HIDEC:0x108			
Field Name	**Bits**	**Default**	**Description**
APER_SIZE	31:0	0x0	Aperture Size NOTE: Bits 0:23 of this field are hardwired to ZERO.

Configuration Aperture Size

CONFIG_REG_1_BASE - R - 32 bits - HIDEC:0x10C			
Field Name	**Bits**	**Default**	**Description**
REG_1_BASE	31:0	0x0	Configuration Register Space 1 Base NOTE: Bits 0:14 of this field are hardwired to ZERO.

Configuration Register Space 1 Base

CONFIG_REG_APER_SIZE - R - 32 bits - HIDEC:0x110			
Field Name	**Bits**	**Default**	**Description**
REG_APER_SIZE	18:0	0x0	Register Space Aperture Size

Configuration Register Aperture Size

MSI_REARM_EN - RW - 32 bits - HIDEC:0x160			
Field Name	**Bits**	**Default**	**Description**
MSI_REARM_EN (W)	0	0x0	MSI function enable/disable

MSI control register for GRAPHIC CHIP

VENDOR_ID - R - 16 bits - [CFGF0_DEC:0x0] [HIDEC:0x5000]			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID	15:0	0x1002	This field identifies the manufacturer of the device.

Vendor ID register.

DEVICE_ID - R - 16 bits - [CFGF0_DEC:0x2] [HIDEC:0x5002]			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x0	This field identifies the particular device. This identifier is allocated by the vendor.

Device ID register.

COMMAND - RW - 16 bits - [CFGF0_DEC:0x4] [HIDEC:0x5004]			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN	0	0x0	0=Disable 1=Enable
MEM_ACCESS_EN	1	0x0	0=Disable 1=Enable
BUS_MASTER_EN	2	0x0	0=Disable 1=Enable
SPECIAL_CYCLE_EN (R)	3	0x0	0=Disable 1=Enable
MEM_WRITE_INVALIDATE_EN (R)	4	0x0	0=Disable 1=Enable
PAL_SNOOP_EN (R)	5	0x0	0=Disable 1=Enable
PARITY_ERROR_EN	6	0x0	0=Disable 1=Enable
AD_STEPPING (R)	7	0x0	0=Disable 1=Enable
SERR_EN	8	0x0	0=Disable 1=Enable
FAST_B2B_EN (R)	9	0x0	0=Disable 1=Enable
INT_DIS	10	0x0	0=Enable 1=Disable

Command register.

STATUS - RW - 16 bits - [CFGF0_DEC:0x6] [HIDEC:0x5006]			
Field Name	**Bits**	**Default**	**Description**
INT_STATUS (R)	3	0x0	Indicates that an INTx interrupt Message is pending internally to the device.
CAP_LIST (R)	4	0x1	Indicates the presence of an extended capability list item. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit must be set to 1.
PCI_66_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0.
UDF_EN (R)	6	0x0	0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	Does not apply to PCI Express. Hardwired to 0.
MASTER_DATA_PARITY_ERROR	8	0x0	0=Inactive 1=Active
DEVSEL_TIMING (R)	10:9	0x0	Does not apply to PCI Express. Hardwired to 0.
SIGNAL_TARGET_ABORT (R)	11	0x0	This bit is set when a device completes a Request using Completer Abort Completion Status.
RECEIVED_TARGET_ABORT	12	0x0	0=Inactive 1=Active
RECEIVED_MASTER_ABORT	13	0x0	0=Inactive 1=Active
SIGNALED_SYSTEM_ERROR	14	0x0	This bit must be set whenever the device asserts SERR#.

PARITY_ERROR_DETECTED	15	0x0	This bit is set when a device sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1.

Status register.

REVISION_ID - R - 8 bits - [CFGF0_DEC:0x8] [HIDEC:0x5008]			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Major revision ID. Set by the vendor.
MAJOR_REV_ID	7:4	0x0	Minor revision ID. Set by the vendor.

Revision ID register.

REGPROG_INF - R - 8 bits - [CFGF0_DEC:0x9] [HIDEC:0x5009]			
Field Name	**Bits**	**Default**	**Description**
REG_LEVEL_PROG_INF	7:0	0x0	Unused, only in test environment

Register-Level Programming Interface Register

SUB_CLASS - R - 8 bits - [CFGF0_DEC:0xA] [HIDEC:0x500A]			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS_INF	7	0x0	The Sub Class Code register is read-only and is used to identify a more specific function of the device. 0=VGA device 1=Extended graphics

Sub Class Register

BASE_CODE - R - 8 bits - [CFGF0_DEC:0xB] [HIDEC:0x500B]			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS_CODE	7:0	0x3	The Class Code register is read-only and is used to identify the generic function of the device.

Base Class Code Register

CACHE_LINE - RW - 8 bits - [CFGF0_DEC:0xC] [HIDEC:0x500C]			
Field Name	**Bits**	**Default**	**Description**
CACHE_LINE_SIZE	7:0	0x0	This read/write register specifies the system cacheline size in units of DWORDs.

CacheLine Size register.

LATENCY - R - 8 bits - [CFGF0_DEC:0xD] [HIDEC:0x500D]			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER	7:0	0x0	Primary/Master latency timer does not apply to PCI Express. Register is hardwired to 0.

Latency Timer register.

HEADER - R - 8 bits - [CFGF0_DEC:0xE] [HIDEC:0x500E]			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE	6:0	0x0	Type 0 or Type 1 Configuration Space
DEVICE_TYPE	7	0x0	0=Single-Function Device 1=Multi-Function Device

Configuration Space Header

BIST - R - 8 bits - [CFGF0_DEC:0xF] [HIDEC:0x500F]			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP	3:0	0x0	A value of 0 means the device has passed its test. Non-zero values mean the device failed. Device-specific failure codes can be encoded in the non-zero value.
BIST_STRT	6	0x0	Write a 1 to invoke BIST. Device resets the bit when BIST is complete. Software should fail the device if BIST is not complete after 2 seconds.
BIST_CAP	7	0x0	This bit is read-only and returns 1 the bridge supports BIST, otherwise 0 is returned

BIST (Built-in Self Test) register.

MEM_BASE_LO - RW - 32 bits - [CFGF0_DEC:0x10] [HIDEC:0x5010]			
Field Name	**Bits**	**Default**	**Description**
BLOCK_MEM_BIT (R)	0	0x0	0=Memory space base address
BLOCK_MEM_TYPE (R)	2:1	0x2	2=Locate anywhere in 64-bit address space
PFTCH_MEM_EN (R)	3	0x1	1=Prefetchable
MEM_BASE_LO	31:25	0x0	Use only lower 32-bit base address

Base address low register for memory in 64-bit address mode or base address is 32bit mode

MEM_BASE_HI - RW - 32 bits - [CFGF0_DEC:0x14] [HIDEC:0x5014]			
Field Name	**Bits**	**Default**	**Description**
MEM_BASE_HI	31:0	0x0	Use upper 32-bit base address

Base address high register for memory in 64-bit address mode. Overlap with IO_BASE.

REG_BASE_LO - RW - 32 bits - [CFGF0_DEC:0x18] [HIDEC:0x5018]			
Field Name	**Bits**	**Default**	**Description**
BLOCK_REG_BIT (R)	0	0x0	0=Memory space base address
BLOCK_REG_TYPE (R)	2:1	0x2	2=Locate anywhere in 64-bit address space
PFTCH_REG_EN (R)	3	0x0	0=Not prefetchable
REG_BASE_LO	31:16	0x0	Use only lower 32-bit register base address

Base address low register for registers in 64-bit address mode or base address in 32bit mode

REG_BASE_HI - RW - 32 bits - [CFGF0_DEC:0x1C] [HIDEC:0x501C]			
Field Name	**Bits**	**Default**	**Description**
REG_BASE_HI	31:0	0x0	Use upper 32bit register base address
Base address high register for registers in 64-bit address mode. Valid only in 64-bit address mode.			

IO_BASE_WS - RW - 32 bits - [CFGF0_DEC:0x20] [HIDEC:0x5020]			
Field Name	**Bits**	**Default**	**Description**
BLOCK_IO_BIT (R)	0	0x1	1=IO space address
IO_BASE	31:8	0x0	This field is really a mirrored of IO_BASE.IO_BASE (mirrored in HW)
Base address register for IO in 64-bit address mode. Valid only in 64-bit address mode.			

IO_BASE - RW - 32 bits - [CFGF0_DEC:0x14] [HIDEC:0x5014]			
Field Name	**Bits**	**Default**	**Description**
BLOCK_IO_BIT (R)	0	0x1	If bit equals 1 the I/O space addressing is used 1=IO space address
IO_BASE	31:8	0x0	Use lower 32bit IO base address, where lower 8-bits are 0
Base address register for IO in 32-bit address mode. Overlap with MEM_BASE_HI.			

ADAPTER_ID - R - 32 bits - [CFGF0_DEC:0x2C] [HIDEC:0x502C]			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID (mirror of ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)	15:0	0x0	Subsystem Vendor ID. Specified by the vendor.
SUBSYSTEM_ID (mirror of ADAPTER_ID_W:SUBSYSTEM_ID)	31:16	0x0	Subsystem ID. Specified by the vendor.
Subsystem Vender ID and Subsystem ID register.			

BIOS_ROM - RW - 32 bits - [CFGF0_DEC:0x30] [HIDEC:0x5030]			
Field Name	**Bits**	**Default**	**Description**
BIOS_ROM_EN	0	0x0	0=Disable 1=Enable
BIOS_BASE_ADDR	31:17	0x0	Base Address of BIOS ROM
Expansion ROM Base Address register.			

CAPABILITIES_PTR - R - 32 bits - [CFGF0_DEC:0x34] [HIDEC:0x5034]			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR	7:0	0x50	50=Point to PMI Capability
Capabilities Pointer.			

INTERRUPT_LINE - RW - 8 bits - [CFGF0_DEC:0x3C] [HIDEC:0x503C]			
Field Name	**Bits**	**Default**	**Description**

INTERRUPT_LINE	7:0	0xff	Interrupt Line register communicates interrupt line routing information.

Interrupt Line Register

INTERRUPT_PIN - R - 8 bits - [CFGF0_DEC:0x3D] [HIDEC:0x503D]			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_PIN	0	0x0	The Interrupt Pin is a read-only register that identifies the legacy interrupt Message(s) the device (or device function) uses

Interrupt Pin register.

MIN_GRANT - R - 8 bits - [CFGF0_DEC:0x3E] [HIDEC:0x503E]			
Field Name	**Bits**	**Default**	**Description**
MIN_GNT	7:0	0x0	Registers do not apply to PCI Express. Hardwired to 0.

MIN_GNT register.

MAX_LATENCY - R - 8 bits - [CFGF0_DEC:0x3F] [HIDEC:0x503F]			
Field Name	**Bits**	**Default**	**Description**
MAX_LAT	7:0	0x0	Registers do not apply to PCI Express. Hardwired to 0.

MAX_LAT register.

ADAPTER_ID_W - RW - 32 bits - [CFGF0_DEC:0x4C] [HIDEC:0x504C]			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x0	Subsystem Vendor ID. Specified by the vendor.
SUBSYSTEM_ID	31:16	0x0	Subsystem Vendor ID. Specified by the vendor.

Adapter ID

PMI_CAP_ID - R - 8 bits - [CFGF0_DEC:0x50] [HIDEC:0x5050]			
Field Name	**Bits**	**Default**	**Description**
PMI_CAP_ID	7:0	0x1	1=PCI Bus Power Management Interface (PMI) register section

Power Management Interface (PMI) Capabilities ID Register

PMI_NXT_CAP_PTR - R - 8 bits - [CFGF0_DEC:0x51] [HIDEC:0x5051]			
Field Name	**Bits**	**Default**	**Description**
PMI_NXT_CAP_PTR	7:0	0x58	The next item is PCI Express Capability.

PMI_PMC_REG - R - 16 bits - [CFGF0_DEC:0x52] [HIDEC:0x5052]			
Field Name	**Bits**	**Default**	**Description**
PMI_VERSION	2:0	0x2	2=Compliant with PMI Specification version 1.1
PMI_PME_CLOCK	3	0x0	Does not apply to PCI Express. Hardwired to 0.

PMI_DEV_SPECIFIC_INIT	5	0x0	Device Specific Initialization
PMI_D1_SUPPORT	9	0x1	1=Support D1 Power Management State.
PMI_D2_SUPPORT	10	0x1	1=Support D2 Power Management State.
PMI_PME_SUPPORT	15:11	0x0	For a device, this indicates the power states in which the device may generate a PME.

Power Management Capabilities Register

PMI_STATUS - RW - 16 bits - [CFGF0_DEC:0x54] [HIDEC:0x5054]			
Field Name	**Bits**	**Default**	**Description**
PMI_POWER_STATE	1:0	0x0	Power State
PMI_PME_EN (R)	8	0x0	PME Enable
PMI_DATA_SELECT (R)	12:9	0x0	Data Select
PMI_DATA_SCALE (R)	14:13	0x0	Data Scale
PMI_PME_STATUS (R)	15	0x0	PME Status

Power Management Status/Control Register

PMI_BSE - R - 8 bits - [CFGF0_DEC:0x56] [HIDEC:0x5056]			
Field Name	**Bits**	**Default**	**Description**
B2_B3_SUPPORT	6	0x0	0=B2/B3 Support for D3Hot
BPCC_EN	7	0x0	0=Bus Power/Clock Control Enable

Power Management Bridge Support Extensions (BSE)

PMI_DATA - R - 8 bits - [CFGF0_DEC:0x57] [HIDEC:0x5057]			
Field Name	**Bits**	**Default**	**Description**
PMI_DATA	7:0	0x0	Power Management Data Register

Power Management Data Register

PCIE_CAP_LIST - R - 16 bits - [CFGF0_DEC:0x58] [HIDEC:0x5058]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x10	10=PCI Express capable
NEXT_PTR	15:8	0x80	Next Capability Pointer -- The offset to the next PCI capability structure or 00h if no other items exist in the linked list of capabilities.

The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 2.3 configuration space capability list.

PCIE_CAP - R - 16 bits - [CFGF0_DEC:0x5A] [HIDEC:0x505A]			
Field Name	**Bits**	**Default**	**Description**
VERSION	3:0	0x1	0=PCI Express Capabilities Version
DEVICE_TYPE	7:4	0x0	0=PCI Express Endpoint
INT_MESSAGE_NUM	13:9	0x0	Interrupt Message Number.

The PCI Express Capabilities register identifies PCI Express device type and associated capabilities.

DEVICE_CAP - R - 32 bits - [CFGF0_DEC:0x5C] [HIDEC:0x505C]			
Field Name	**Bits**	**Default**	**Description**

MAX_PAYLOAD_SUPPORT	2:0	0x0	0=128B size
PHANTOM_FUNC	4:3	0x0	0=No Phantom Functions
EXTENDED_TAG	5	0x1	0=8 Bit Tag Supported
L0S_ACCEPTABLE_LATENCY	8:6	0x0	This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state.
L1_ACCEPTABLE_LATENCY	11:9	0x0	This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state.
ATTN_BUTTON_PRESENT	12	0x0	0=Attention Button Present
ATTN_INDICATOR_PRESENT	13	0x0	0=Attention Indicator Present
POWER_INDICATOR_PRESENT	14	0x0	0=Power Indicator Present
CAPTURED_SLOT_POWER_LIMIT	25:18	0x0	(Upstream Ports only) In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot.
CAPTURED_SLOT_POWER_SCALE	27:26	0x0	Specifies the scale used for the Slot Power Limit Value.

The Device Capabilities register identifies PCI Express device specific capabilities.

DEVICE_CNTL - RW - 16 bits - [CFGF0_DEC:0x60] [HIDEC:0x5060]			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_EN	0	0x0	Correctable Error Reporting Enable. 0=Disable 1=Enable
NON_FATAL_ERR_EN	1	0x0	Non-Fatal Error Reporting Enable. 0=Disable 1=Enable
FATAL_ERR_EN	2	0x0	Fatal Error Reporting Enable. 0=Disable 1=Enable
USR_REPORT_EN	3	0x0	Unsupported Request (UR) Reporting Enable. 0=Disable 1=Enable
RELAXED_ORD_EN	4	0x1	Enable Relaxed Ordering. 0=Disable 1=Enable
MAX_PAYLOAD_SIZE	7:5	0x0	Max Payload Size. 0=128B size
EXTENDED_TAG_EN	8	0x0	Extended Tag Field Enable. 0=Disable 1=Enable
PHANTOM_FUNC_EN (R)	9	0x0	Phantom Functions Enable. 0=Disable 1=Enable
AUX_POWER_PM_EN (R)	10	0x0	Auxiliary (AUX) Power PM Enable. 0=Disable 1=Enable
NO_SNOOP_EN	11	0x1	Enable No Snoop. 0=Disable 1=Enable
MAX_REQUEST_SIZE (R)	14:12	0x0	Max Read Request Size. 0=128B size

The Device Control register controls various PCI Express features.

DEVICE_STATUS - RW - 16 bits - [CFGF0_DEC:0x62] [HIDEC:0x5062]			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR	0	0x0	This bit indicates status of correctable errors detected.
NON_FATAL_ERR	1	0x0	This bit indicates status of Nonfatal errors detected.
FATAL_ERR	2	0x0	This bit indicates status of Fatal errors detected.

USR_DETECTED	3	0x0	This bit indicates that the device received an Unsupported Request.
AUX_PWR (R)	4	0x0	Devices that require AUX power report this bit as set if AUX power is detected by the device.
TRANSACTIONS_PEND (R)	5	0x0	Endpoints: This bit when set indicates that the device has issued Non-Posted Requests which have not been completed. Root and Switch Ports: This bit when set indicates that a Port has issued Non-Posted Requests on its own behalf (using the Port's own Requester ID) which have not been completed.

The Device Status register provides information about PCI Express device specific parameters.

LINK_CAP - R - 32 bits - [CFGF0_DEC:0x64] [HIDEC:0x5064]			
Field Name	**Bits**	**Default**	**Description**
LINK_SPEED	3:0	0x1	0=2.5 Gb/s
LINK_WIDTH	9:4	0x10	0=16 Lanes
PM_SUPPORT	11:10	0x3	This field indicates the level of ASPM supported on the given PCI Express Link.
OUR_L0S_EXIT_LATENCY	14:12	0x1	This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
OUR_L1_EXIT_LATENCY	17:15	0x2	This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
OUR_PORT_NUM	31:24	0x0	This field indicates the PCI Express Port number for the given PCI Express Link.

The Link Capabilities register identifies PCI Express Link specific capabilities.

LINK_CNTL - RW - 16 bits - [CFGF0_DEC:0x68] [HIDEC:0x5068]			
Field Name	**Bits**	**Default**	**Description**
PM_CONTROL	1:0	0x0	This field controls the level of ASPM supported on the given PCI Express Link. Defined encodings are: 00b Disabled 01b L0s Entry Enabled 10b L1 Entry Enabled 11b L0s and L1 Entry Enabled
READ_CPL_BOUNDARY (R)	3	0x0	0=64 Byte 1=128 Byte
COMMON_CLOCK_CFG	6	0x0	This bit when set indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. Default value of this field is 0b.
EXTENDED_SYNC	7	0x0	This bit when set forces the transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP ordered set

The Link Control register controls PCI Express Link specific parameters.

LINK_STATUS - R - 16 bits - [CFGF0_DEC:0x6A] [HIDEC:0x506A]			
Field Name	**Bits**	**Default**	**Description**
NEGOTIATED_LINK_SPEED	3:0	0x1	0=2.5 Gb/s
NEGOTIATED_LINK_WIDTH	9:4	0x10	This field indicates the negotiated width of the given PCI Express Link. Defined encodings are: 000001b X1 000010b X2 000100b X4 001000b X8 001100b X12 010000b X16 100000b X32 All other encodings are reserved.

SLOT_CLOCK_CFG	12	0x1	0=Different Clock 1=Same Clock

The Link Status register provides information about PCI Express Link specific parameters.

MSI_CAP_ID - R - 8 bits - [CFGF0_DEC:0x80] [HIDEC:0x5080]			
Field Name	**Bits**	**Default**	**Description**
MSI_CAP_ID	7:0	0x5	MSI Capability ID

MSI Capability ID.

MSI_NXT_CAP_PTR - R - 8 bits - [CFGF0_DEC:0x81] [HIDEC:0x5081]			
Field Name	**Bits**	**Default**	**Description**
MSI_NXT_CAP_PTR	7:0	0x0	The last item in capabilities list.

MSI Next Capability Pointer.

MSI_MSG_CNTL - RW - 16 bits - [CFGF0_DEC:0x82] [HIDEC:0x5082]			
Field Name	**Bits**	**Default**	**Description**
MSI_EN	0	0x0	Enable MSI messaging 0=Disable 1=Enable
MSI_MULTMSG_CAP (R)	3:1	0x0	Multiple Message Capable register is read to determine the number of requested messages. 0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_MULTMSG_EN	6:4	0x0	Multiple Message Enable register is written to indicate the number of allocated messages. 0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_64BIT (R)	7	0x0	Signifies if a device function is capable of generating a 64-bit message address 0=Not capable of generating 1 64-bit message address 1=Capable of generating 1 64-bit message address

MSI Message Control register.

MSI_MSG_ADDR_LO - RW - 32 bits - [CFGF0_DEC:0x84] [HIDEC:0x5084]			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_LO	31:2	0x0	System-specified message lower address.

MSI Message Lower Address. MSI is assumed to be in 64 bit mode all the time.

MSI_MSG_ADDR_HI - RW - 32 bits - [CFGF0_DEC:0x88] [HIDEC:0x5088]			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_HI	31:0	0x0	System-specified message upper address.
MSI Message Upper Address. MSI is assumed to be in 64 bit mode all the time.			

MSI_MSG_DATA_64 - RW - 16 bits - [CFGF0_DEC:0x8C] [HIDEC:0x508C]			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA_64	15:0	0x0	Message Data. System specified.
64-bit MSI Message Data			

MSI_MSG_DATA - RW - 32 bits - [CFGF0_DEC:0x88] [HIDEC:0x5088]			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA	15:0	0x0	System-specified message.
MSI Message Data.			

PCIE_ENH_ADV_ERR_RPT_CAP_HDR - R - 32 bits - [CFGF0_DEC:0x100] [HIDEC:0x5100]			
Field Name	**Bits**	**Default**	**Description**
EXT_CAP_ID	15:0	0x1	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NXT_CAP_OFFSET	31:20	0x0	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
Advanced Error Reporting Enhanced Capability header			

PCIE_UNCORR_ERR_STATUS - RW - 32 bits - [CFGF0_DEC:0x104] [HIDEC:0x5104]			
Field Name	**Bits**	**Default**	**Description**
TRN_ERR_STATUS	0	0x0	Training Error Status
DLP_ERR_STATUS	4	0x0	Data Link Protocol Error Status
PSN_ERR_STATUS	12	0x0	Poisoned TLP Status
FC_ERR_STATUS	13	0x0	Flow Control Protocol Error Status
CPL_TIMEOUT_STATUS	14	0x0	Completion Timeout Status
CPL_ABORT_ERR_STATUS	15	0x0	Completer Abort Status
UNEXP_CPL_STATUS	16	0x0	Unexpected Completion Status
RCV_OVFL_STATUS	17	0x0	Receiver Overflow Status
MAL_TLP_STATUS	18	0x0	Malformed TLP Status
ECRC_ERR_STATUS	19	0x0	ECRC Error Status
UNSUPP_REQ_ERR_STATUS	20	0x0	Unsupported Request Error Status
The Uncorrectable Error Status register reports error status of individual error sources on a PCI Express device.			

PCIE_UNCORR_ERR_MASK - RW - 32 bits - [CFGF0_DEC:0x108] [HIDEC:0x5108]			
Field Name	**Bits**	**Default**	**Description**
TRN_ERR_MASK	0	0x0	Training Error Mask

DLP_ERR_MASK	4	0x0	Data Link Protocol Error Mask
PSN_ERR_MASK	12	0x0	Poisoned TLP Mask
FC_ERR_MASK	13	0x0	Flow Control Protocol Error Mask
CPL_TIMEOUT_MASK	14	0x0	Completion Timeout Mask
CPL_ABORT_ERR_MASK	15	0x0	Completer Abort Mask
UNEXP_CPL_MASK	16	0x0	Unexpected Completion Mask
RCV_OVFL_MASK	17	0x0	Receiver Overflow Mask
MAL_TLP_MASK	18	0x0	Malformed TLP Mask
ECRC_ERR_MASK	19	0x0	ECRC Error Mask
UNSUPP_REQ_ERR_MASK	20	0x0	Unsupported Request Error Mask

The Uncorrectable Error Mask register controls reporting of individual errors by the device to the PCI Express Root Complex via a PCI Express error Message.

PCIE_UNCORR_ERR_SEVERITY - RW - 32 bits - [CFGF0_DEC:0x10C] [HIDEC:0x510C]			
Field Name	**Bits**	**Default**	**Description**
TRN_ERR_SEVERITY	0	0x1	Training Error Severity
DLP_ERR_SEVERITY	4	0x1	Data Link Protocol Error Severity
PSN_ERR_SEVERITY	12	0x0	Poisoned TLP Severity
FC_ERR_SEVERITY	13	0x1	Flow Control Protocol Error Severity
CPL_TIMEOUT_SEVERITY	14	0x0	Completion Timeout Error Severity
CPL_ABORT_ERR_SEVERITY	15	0x0	Completer Abort Error Severity
UNEXP_CPL_SEVERITY	16	0x0	Unexpected Completion Error Severity
RCV_OVFL_SEVERITY	17	0x1	Receiver Overflow Error Severity
MAL_TLP_SEVERITY	18	0x1	Malformed TLP Severity
ECRC_ERR_SEVERITY	19	0x0	ECRC Error Severity
UNSUPP_REQ_ERR_SEVERITY	20	0x0	Unsupported Request Error Severity

The Uncorrectable Error Severity register controls whether an individual error is reported as a Nonfatal or Fatal error.

PCIE_CORR_ERR_STATUS - RW - 32 bits - [CFGF0_DEC:0x110] [HIDEC:0x5110]			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_STATUS	0	0x0	Receiver Error Status (
BAD_TLP_STATUS	6	0x0	Bad TLP Status
BAD_DLLP_STATUS	7	0x0	Bad DLLP Status
REPLAY_NUM_ROLLOVER_STATUS	8	0x0	REPLAY_NUM Rollover Status
REPLAY_TIMER_TIMEOUT_STATUS	12	0x0	Replay Timer Timeout Status

The Correctable Error Status register reports error status of individual correctable error sources on a PCI Express device.

PCIE_CORR_ERR_MASK - RW - 32 bits - [CFGF0_DEC:0x114] [HIDEC:0x5114]			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_MASK	0	0x0	Receiver Error Mask
BAD_TLP_MASK	6	0x0	Bad TLP Mask
BAD_DLLP_MASK	7	0x0	Bad DLLP Mask
REPLAY_NUM_ROLLOVER_MASK	8	0x0	REPLAY_NUM Rollover Mask
REPLAY_TIMER_TIMEOUT_MASK	12	0x0	Replay Timer Timeout Mask

The Correctable Error Mask register controls reporting of individual correctable errors by device to the PCI Express Root Complex via a PCI Express error Message.

PCIE_ADV_ERR_CAP_CNTL - RW - 32 bits - [CFGF0_DEC:0x118] [HIDEC:0x5118]			
Field Name	**Bits**	**Default**	**Description**
FIRST_ERR_PTR (R)	4:0	0x0	The First Error Pointer is a read-only register that identifies the bit position of the first error reported in the Uncorrectable Error Status register.
ECRC_GEN_CAP (R)	5	0x0	This bit indicates that the device is capable of generating ECRC
ECRC_GEN_EN	6	0x0	This bit when set enables ECRC generation. Default value of this field is 0.
ECRC_CHECK_CAP (R)	7	0x0	This bit indicates that the device is capable of checking ECRC
ECRC_CHECK_EN	8	0x0	This bit when set enables ECRC checking. Default value of this field is 0.

Advanced Error Capabilities and Control Register

PCIE_HDR_LOG0 - R - 32 bits - [CFGF0_DEC:0x11C] [HIDEC:0x511C]			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 1st DW

Header Log Register captures the Header for the TLP corresponding to a detected error;

PCIE_HDR_LOG1 - R - 32 bits - [CFGF0_DEC:0x120] [HIDEC:0x5120]			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 2nd DW

Header Log Register

PCIE_HDR_LOG2 - R - 32 bits - [CFGF0_DEC:0x124] [HIDEC:0x5124]			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 3rd DW

Header Log Register

PCIE_HDR_LOG3 - R - 32 bits - [CFGF0_DEC:0x128] [HIDEC:0x5128]			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 4th DW

Header Log Register

F1_VENDOR_ID - R - 16 bits - [CFGF1_DEC:0x0] [HIDEC:0x5400]			
Field Name	**Bits**	**Default**	**Description**
F1_VENDOR_ID	15:0	0x1002	This field identifies the manufacturer of the device.

Vendor ID register.

F1_DEVICE_ID - R - 16 bits - [CFGF1_DEC:0x2] [HIDEC:0x5402]			
Field Name	**Bits**	**Default**	**Description**
F1_DEVICE_ID	15:0	0x0	This field identifies the particular device. This identifier is allocated by the vendor.

Device ID register.

F1_COMMAND - RW - 16 bits - [CFGF1_DEC:0x4] [HIDEC:0x5404]			
Field Name	**Bits**	**Default**	**Description**
F1_IO_ACCESS_EN	0	0x0	0=Disable 1=Enable
F1_MEM_ACCESS_EN	1	0x0	0=Disable 1=Enable
F1_BUS_MASTER_EN	2	0x0	0=Disable 1=Enable

Command register.

F1_STATUS - R - 16 bits - [CFGF1_DEC:0x6] [HIDEC:0x5406]			
Field Name	**Bits**	**Default**	**Description**
F1_CAP_LIST	4	0x1	Indicates the presence of an extended capability list item. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit must be set to 1.
F1_MASTER_DATA_PARITY_ERROR	8	0x0	0=Inactive 1=Active
F1_SIGNAL_TARGET_ABORT	11	0x0	This bit is set when a device completes a Request using Completer Abort Completion Status.
F1_RECEIVED_TARGET_ABORT	12	0x0	0=Inactive 1=Active
F1_RECEIVED_MASTER_ABORT	13	0x0	0=Inactive 1=Active
F1_PARITY_ERROR_DETECTED	15	0x0	This bit is set when a device sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1.

Status register.

F1_REVISION_ID - R - 8 bits - [CFGF1_DEC:0x8] [HIDEC:0x5408]			
Field Name	**Bits**	**Default**	**Description**
F1_MINOR_REV_ID	3:0	0x0	Major revision ID. Set by the vendor.
F1_MAJOR_REV_ID	7:4	0x0	Minor revision ID. Set by the vendor.

Revision ID register.

F1_REGPROG_INF - R - 8 bits - [CFGF1_DEC:0x9] [HIDEC:0x5409]			
Field Name	**Bits**	**Default**	**Description**
F1_REG_LEVEL_PROG_INF	7:0	0x0	Unused, only in test environment

Register-Level Programming Interface Register

F1_SUB_CLASS - R - 8 bits - [CFGF1_DEC:0xA] [HIDEC:0x540A]			
Field Name	**Bits**	**Default**	**Description**
F1_SUB_CLASS_INF	7	0x1	The Sub Class Code register is read-only and is used to identify a more specific function of the device. 0=VGA device 1=Extended graphics

Sub Class Register

F1_BASE_CODE - R - 8 bits - [CFGF1_DEC:0xB] [HIDEC:0x540B]			
Field Name	**Bits**	**Default**	**Description**
F1_BASE_CLASS_CODE	7:0	0x3	The Class Code register is read-only and is used to identify the generic function of the device.

Base Class Code Register

F1_CACHE_LINE - RW - 8 bits - [CFGF1_DEC:0xC] [HIDEC:0x540C]			
Field Name	**Bits**	**Default**	**Description**
F1_CACHE_LINE_SIZE	7:0	0x0	This read/write register specifies the system cacheline size in units of DWORDs.

CacheLine Size register.

F1_LATENCY - R - 8 bits - [CFGF1_DEC:0xD] [HIDEC:0x540D]			
Field Name	**Bits**	**Default**	**Description**
F1_LATENCY_TIMER	7:0	0x0	Primary/Master latency timer does not apply to PCI Express. Register is hardwired to 0.

Latency Timer register.

F1_HEADER - R - 8 bits - [CFGF1_DEC:0xE] [HIDEC:0x540E]			
Field Name	**Bits**	**Default**	**Description**
F1_HEADER_TYPE	6:0	0x0	0 = non-bridge function 1 = PCI-to-PCI Bridge (or PCI-X to PCI-X Bridge) 2 = CardBus Bridge Hardwired to 0
F1_DEVICE_TYPE	7	0x0	0=Single-Function Device 1=Multi-Function Device

Configuration header format

F1_BIST - R - 8 bits - [CFGF1_DEC:0xF] [HIDEC:0x540F]			
Field Name	**Bits**	**Default**	**Description**
F1_BIST_COMP	3:0	0x0	A value of 0 means the device has passed its test. Non-zero values mean the device failed. Device-specific failure codes can be encoded in the non-zero value.
F1_BIST_STRT	6	0x0	Write a 1 to invoke BIST. Device resets the bit when BIST is complete. Software should fail the device if BIST is not complete after 2 seconds.
F1_BIST_CAP	7	0x0	This bit is read-only and returns 1 the bridge supports BIST, otherwise 0 is returned

BIST (Built-in Self Test) register.

F1_REG_BASE_LO - RW - 32 bits - [CFGF1_DEC:0x10] [HIDEC:0x5414]			
Field Name	**Bits**	**Default**	**Description**
F1_BLOCK_REG_BIT (R)	0	0x0	0=Memory space base address
F1_BLOCK_REG_TYPE (R)	2:1	0x2	2=Locate anywhere in 64-bit address space

F1_PFTCH_REG_EN (R)	3	0x0	0=Not prefetchable
F1_REG_BASE_LO	31:16	0x0	Use only lower 32-bit register base address

Base address low register for registers in 64-bit address mode or base address in 32bit mode.

F1_REG_BASE_HI - RW - 32 bits - [CFGF1_DEC:0x14] [HIDEC:0x541C]			
Field Name	**Bits**	**Default**	**Description**
F1_REG_BASE_HI	31:0	0x0	Use upper 32bit register base address

Base address high register for registers in 64-bit address mode. Valid only in 64-bit address mode.

F1_ADAPTER_ID - R - 32 bits - [CFGF1_DEC:0x2C] [HIDEC:0x542C]			
Field Name	**Bits**	**Default**	**Description**
F1_SUBSYSTEM_VENDOR_ID (mirror of ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)	15:0	0x0	Subsystem Vendor ID. Specified by the vendor.
F1_SUBSYSTEM_ID	31:16	0x0	Subsystem ID. Specified by the vendor.

Subsystem Vender ID and Subsystem ID register.

F1_CAPABILITIES_PTR - R - 32 bits - [CFGF1_DEC:0x34] [HIDEC:0x5434]			
Field Name	**Bits**	**Default**	**Description**
F1_CAP_PTR	7:0	0x50	50=Point to PMI Capability

Capabilities Pointer.

F1_INTERRUPT_LINE - RW - 8 bits - [CFGF1_DEC:0x3C] [HIDEC:0x543C]			
Field Name	**Bits**	**Default**	**Description**
F1_INTERRUPT_LINE	7:0	0xff	Interrupt Line register communicates interrupt line routing information.

Interrupt Line Register

F1_INTERRUPT_PIN - R - 8 bits - [CFGF1_DEC:0x3D] [HIDEC:0x543D]			
Field Name	**Bits**	**Default**	**Description**
F1_INTERRUPT_PIN	0	0x0	The Interrupt Pin is a read-only register that identifies the legacy interrupt Message(s) the device (or device function) uses

Interrupt Pin register.

F1_MIN_GRANT - R - 8 bits - [CFGF1_DEC:0x3E] [HIDEC:0x543E]			
Field Name	**Bits**	**Default**	**Description**
F1_MIN_GNT	7:0	0x0	Registers do not apply to PCI Express. Hardwired to 0.

MIN_GNT register.

F1_MAX_LATENCY - R - 8 bits - [CFGF1_DEC:0x3F] [HIDEC:0x543F]

Field Name	Bits	Default	Description
F1_MAX_LAT	7:0	0x0	Registers do not apply to PCI Express. Hardwired to 0.

MAX_LAT register.

F1_PMI_CAP_ID - R - 8 bits - [CFGF1_DEC:0x50] [HIDEC:0x5450]			
Field Name	**Bits**	**Default**	**Description**
F1_PMI_CAP_ID	7:0	0x1	1=PCI Bus Power Management Interface (PMI) register section

Power Management Interface (PMI) Capabilities ID Register

F1_PMI_NXT_CAP_PTR - R - 8 bits - [CFGF1_DEC:0x51] [HIDEC:0x5451]			
Field Name	**Bits**	**Default**	**Description**
F1_PMI_NXT_CAP_PTR	7:0	0x58	The last item.

F1_PMI_PMC_REG - R - 16 bits - [CFGF1_DEC:0x52] [HIDEC:0x5452]			
Field Name	**Bits**	**Default**	**Description**
F1_PMI_VERSION	2:0	0x2	2=Compliant with PMI Specification version 1.1
F1_PMI_PME_CLOCK	3	0x0	Does not apply to PCI Express. Hardwired to 0.
F1_PMI_DEV_SPECIFIC_INIT	5	0x0	Device Specific Initialization
F1_PMI_D1_SUPPORT	9	0x1	1=Support D1 Power Management State.
F1_PMI_D2_SUPPORT	10	0x1	1=Support D2 Power Management State.
F1_PMI_PME_SUPPORT	15:11	0x0	For a device, this indicates the power states in which the device may generate a PME.

Power Management Capabilities Register

F1_PMI_STATUS - RW - 16 bits - [CFGF1_DEC:0x54] [HIDEC:0x5454]			
Field Name	**Bits**	**Default**	**Description**
F1_PMI_POWER_STATE	1:0	0x0	Power State
F1_PMI_PME_EN (R)	8	0x0	PME Enable
F1_PMI_DATA_SELECT (R)	12:9	0x0	Data Select
F1_PMI_DATA_SCALE (R)	14:13	0x0	Data Scale
F1_PMI_PME_STATUS (R)	15	0x0	PME Status
Power Management Status/Control Register			

F1_PMI_BSE - R - 8 bits - [CFGF1_DEC:0x56] [HIDEC:0x5456]			
Field Name	**Bits**	**Default**	**Description**
F1_B2_B3_SUPPORT	6	0x0	0=B2/B3 Support for D3Hot
F1_BPCC_EN	7	0x0	0=Bus Power/Clock Control Enable
Power Management Bridge Support Extensions (BSE)			

F1_PMI_DATA - R - 8 bits - [CFGF1_DEC:0x57] [HIDEC:0x5457]			
Field Name	**Bits**	**Default**	**Description**
F1_PMI_DATA	7:0	0x0	Power Management Data Register
Power Management Data Register			

F1_PCIE_CAP_LIST - R - 16 bits - [CFGF1_DEC:0x58] [HIDEC:0x5458]			
Field Name	**Bits**	**Default**	**Description**
F1_CAP_ID	7:0	0x10	10=PCI Express capable
F1_NEXT_PTR	15:8	0x0	Next Capability Pointer -- The offset to the next PCI capability structure or 00h if no other items exist in the linked list of capabilities.
The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 2.3 configuration space capability list.			

F1_PCIE_CAP - R - 16 bits - [CFGF1_DEC:0x5A] [HIDEC:0x545A]			
Field Name	**Bits**	**Default**	**Description**
F1_VERSION	3:0	0x1	0=PCI Express Capabilities Version
F1_DEVICE_TYPE	7:4	0x0	0=PCI Express Endpoint
F1_INT_MESSAGE_NUM	13:9	0x0	Interrupt Message Number.
The PCI Express Capabilities register identifies PCI Express device type and associated capabilities.			

F1_DEVICE_CAP - R - 32 bits - [CFGF1_DEC:0x5C] [HIDEC:0x545C]			
Field Name	**Bits**	**Default**	**Description**
F1_MAX_PAYLOAD_SUPPORT	2:0	0x0	0=128B size
F1_PHANTOM_FUNC	4:3	0x0	0=No Phantom Functions
F1_EXTENDED_TAG	5	0x0	0=8 Bit Tag Supported
F1_L0S_ACCEPTABLE_LATENCY	8:6	0x0	This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state.
F1_L1_ACCEPTABLE_LATENCY	11:9	0x0	This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state.
F1_ATTN_BUTTON_PRESENT	12	0x0	0=Attention Button Present

F1_ATTN_INDICATOR_PRESENT	13	0x0	0=Attention Indicator Present
F1_POWER_INDICATOR_PRESENT	14	0x0	0=Power Indicator Present
F1_CAPTURED_SLOT_POWER_LIMIT	25:18	0x0	(Upstream Ports only) In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot.
F1_CAPTURED_SLOT_POWER_SCALE	27:26	0x0	Specifies the scale used for the Slot Power Limit Value.

The Device Capabilities register identifies PCI Express device specific capabilities.

F1_DEVICE_CNTL - RW - 16 bits - [CFGF1_DEC:0x60] [HIDEC:0x5460]			
Field Name	**Bits**	**Default**	**Description**
F1_CORR_ERR_EN	0	0x0	Correctable Error Reporting Enable. 0=Disable 1=Enable
F1_NON_FATAL_ERR_EN	1	0x0	Non-Fatal Error Reporting Enable. 0=Disable 1=Enable
F1_FATAL_ERR_EN	2	0x0	Fatal Error Reporting Enable. 0=Disable 1=Enable
F1_USR_REPORT_EN	3	0x0	Unsupported Request (UR) Reporting Enable. 0=Disable 1=Enable
F1_RELAXED_ORD_EN (R)	4	0x0	Enable Relaxed Ordering. 0=Disable 1=Enable
F1_MAX_PAYLOAD_SIZE	7:5	0x0	Max Payload Size. 0=128B size
F1_EXTENDED_TAG_EN (R)	8	0x0	Extended Tag Field Enable. 0=Disable 1=Enable
F1_PHANTOM_FUNC_EN (R)	9	0x0	Phantom Functions Enable. 0=Disable 1=Enable
F1_AUX_POWER_PM_EN (R)	10	0x0	Auxiliary (AUX) Power PM Enable. 0=Disable 1=Enable
F1_NO_SNOOP_EN (R)	11	0x0	Enable No Snoop. 0=Disable 1=Enable
F1_MAX_REQUEST_SIZE (R)	14:12	0x0	Max Read Request Size. 0=128B size

The Device Control register controls various PCI Express features.

F1_DEVICE_STATUS - R - 16 bits - [CFGF1_DEC:0x62] [HIDEC:0x5462]			
Field Name	**Bits**	**Default**	**Description**
F1_CORR_ERR	0	0x0	This bit indicates status of correctable errors detected.
F1_NON_FATAL_ERR	1	0x0	This bit indicates status of Nonfatal errors detected.
F1_FATAL_ERR	2	0x0	This bit indicates status of Fatal errors detected.
F1_USR_DETECTED	3	0x0	This bit indicates that the device received an Unsupported Request.
F1_AUX_PWR	4	0x0	Devices that require AUX power report this bit as set if AUX power is detected by the device.
F1_TRANSACTIONS_PEND	5	0x0	Endpoints: This bit when set indicates that the device has issued Non-Posted Requests which have not been completed. Root and Switch Ports: This bit when set indicates that a Port has issued Non-Posted Requests on its own behalf (using the Port's own Requester ID) which have not been completed.

The Device Status register provides information about PCI Express device specific parameters.

F1_LINK_CAP - R - 32 bits - [CFGF1_DEC:0x64] [HIDEC:0x5464]			
Field Name	**Bits**	**Default**	**Description**
F1_LINK_SPEED	3:0	0x1	0=2.5 Gb/s
F1_LINK_WIDTH	9:4	0x10	0=16 Lanes
F1_PM_SUPPORT	11:10	0x3	This field indicates the level of ASPM supported on the given PCI Express Link.
F1_OUR_L0S_EXIT_LATENCY	14:12	0x1	This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
F1_OUR_L1_EXIT_LATENCY	17:15	0x2	This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
F1_OUR_PORT_NUM	31:24	0x0	This field indicates the PCI Express Port number for the given PCI Express Link.

The Link Capabilities register identifies PCI Express Link specific capabilities.

F1_LINK_CNTL - RW - 16 bits - [CFGF1_DEC:0x68] [HIDEC:0x5468]			
Field Name	**Bits**	**Default**	**Description**
F1_PM_CONTROL	1:0	0x0	This field controls the level of ASPM supported on the given PCI Express Link. Defined encodings are: 00b Disabled 01b L0s Entry Enabled 10b L1 Entry Enabled 11b L0s and L1 Entry Enabled
F1_READ_CPL_BOUNDARY (R)	3	0x0	0=64 Byte 1=128 Byte
F1_COMMON_CLOCK_CFG	6	0x0	This bit when set indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. Default value of this field is 0b.
F1_EXTENDED_SYNC	7	0x0	This bit when set forces the transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP ordered set

The Link Control register controls PCI Express Link specific parameters.

F1_LINK_STATUS - R - 16 bits - [CFGF1_DEC:0x6A] [HIDEC:0x546A]			
Field Name	**Bits**	**Default**	**Description**
F1_NEGOTIATED_LINK_SPEED	3:0	0x1	0=2.5 Gb/s
F1_NEGOTIATED_LINK_WIDTH	9:4	0x10	This field indicates the negotiated width of the given PCI Express Link. Defined encodings are: 000001b X1 000010b X2 000100b X4 001000b X8 001100b X12 010000b X16 100000b X32 All other encodings are reserved.
F1_SLOT_CLOCK_CFG	12	0x1	0=Different Clock 1=Same Clock

The Link Status register provides information about PCI Express Link specific parameters.

PCIE_RESERVED - R - 32 bits - PCIEIND:0x0			
Field Name	**Bits**	**Default**	**Description**
PCIE_RESERVED	31:0	0xffffffff	Reserved for future use

PCIE Reserved Register

PCIE_TX_CNTL - RW - 32 bits - PCIEIND:0x1			
Field Name	**Bits**	**Default**	**Description**
TX_REPLAY_NUM_COUNT (R)	9:0	0x0	Replay number count
TX_SNR_OVERRIDE	15:14	0x0	Snoop Not Required Override 0=Generate bit as normal 1=Override equation, and always set bit 2=Override equation, and always clear bit 3=Invalid
TX_RO_OVERRIDE	17:16	0x0	Relaxed Ordering Override 0=Generate bit as normal 1=Override equation, and always set bit 2=Override equation, and always clear bit 3=Invalid
TX_SNR_RO_SEL	18	0x1	0=Use gart entry type to define SNR/RO 1=Use PCI/AGP bit to define SNR/RO
TX_PACK_PACKET_EN	19	0x0	0=Place STP/SDP in lane 0 only 1=Place packets as close as allowable
TX_HOLD_RQ_FIFO	21:20	0x0	Not used
TX_SEPARATE_PACKETS	23:22	0x0	Insert this field number of idle symbol times between packets (TLP or DLLP).
TX_FC_UPDATE_TIMEOUT_SEL	25:24	0x2	0=Disable flow control 1=4x clock cycle 2=1024x clock cycle 3=Invalid
TX_FC_UPDATE_TIMEOUT	31:26	0x7	Interval length to send flow control update

TX Control Register

PCIE_TX_SEQ - R - 32 bits - PCIEIND:0x2			
Field Name	**Bits**	**Default**	**Description**
TX_NEXT_TRANSMIT_SEQ	11:0	0x0	Next Transmit Sequence Number to send out
TX_ACKD_SEQ	27:16	0x0	Last Acknowledged Sequence Number

TX Sequence Register

PCIE_TX_REPLAY - RW - 32 bits - PCIEIND:0x3			
Field Name	**Bits**	**Default**	**Description**
TX_REPLAY_NUM	9:0	0x3	Register to control Replay Number before Link goes to Retrain
TX_REPLAY_TIMER_OVERWRITE	15	0x0	Trigger for Replay Timer
TX_REPLAY_TIMER	31:16	0x90	Replay Timer - when expired do Replay

TX Replay Register

PCIE_TX_CREDITS_CONSUMED - R - 32 bits - PCIEIND:0x4			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_CONSUMED_PH	7:0	0x0	For posted TLP header, total number of FC units consumed by TLP transmission made since FC initialization, modulo 256
TX_CREDITS_CONSUMED_NPH	15:8	0x0	For non-posed TLP header, total number of FC units consumed by TLP transmission made since FC initialization, modulo 256
TX_CREDITS_CONSUMED_CPLH	23:16	0x0	For completion TLP header, total number of FC units consumed by TLP transmission made since FC initialization, modulo 256

TX Header Credits Consumed Register

PCIE_TX_CREDITS_CONSUMED_D - R - 32 bits - PCIEIND:0x5			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_CONSUMED_PD	11:0	0x0	For posted TLP data, total number of FC units consumed by TLP transmission made since FC initialization, modulo 4096
TX_CREDITS_CONSUMED_NPD	23:12	0x0	For non-posted TLP data, total number of FC units consumed by TLP transmission made since FC initialization, modulo 4096

TX Data Credits Consumed Register

PCIE_TX_CREDITS_CONSUMED_CPLD - R - 32 bits - PCIEIND:0x6			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_CONSUMED_CPLD	11:0	0x0	For completion TLP data, total number of FC units consumed by TLP transmission made since FC initialization, modulo 4096

TX Completion Data Credits Consumed Register

PCIE_TX_CREDITS_LIMIT - R - 32 bits - PCIEIND:0x7			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_LIMIT_PH	7:0	0x0	For posted TLP header, total number of FC units advertised by the receiver since FC initialization, modulo 256
TX_CREDITS_LIMIT_NPH	15:8	0x0	For non-posed TLP header, total number of FC units advertised by the receiver since FC initialization, modulo 256
TX_CREDITS_LIMIT_CPLH	23:16	0x0	For completion TLP header, total number of FC units advertised by the receiver since FC initialization, modulo 256

TX Header Credits Limit Register

PCIE_TX_CREDITS_LIMIT_D - R - 32 bits - PCIEIND:0x8			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_LIMIT_PD	11:0	0x0	For posted TLP data, total number of FC units advertised by the receiver since FC initialization, modulo 4096
TX_CREDITS_LIMIT_NPD	23:12	0x0	For non-posed TLP data, total number of FC units advertised by the receiver since FC initialization, modulo 4096

TX Data Credits Limit Register

PCIE_TX_CREDITS_LIMIT_CPLD - R - 32 bits - PCIEIND:0x9			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_LIMIT_CPLD	11:0	0x0	For completion TLP data, total number of FC units advertised by the receiver since FC initialization, modulo 4096

TX Completion Data Credits Limit Register

PCIE_TX_GART_CNTL - RW - 32 bits - PCIEIND:0x10			
Field Name	**Bits**	**Default**	**Description**
GART_EN	0	0x0	Enable/disable the PCIE GART 0=Disable PCI Express GART 1=Enable PCI Express GART
GART_UNMAPPED_ACCESS	2:1	0x0	Controls how GART handles addresses that are not mapped into the GART table 0=PASS THRU 1=CLAMP LO ADDR 2=N/A 3=DISCARD
GART_MODE	4:3	0x0	The type of cache use for the GART TLB 0=32x128 cache 1=8x4x128 cache 2=Reserved 3=Reserved
GART_CHK_RW_VALID_EN	5	0x0	Enable/disable checking the RW Valid bit in the GART entry 0=Disable check 1=Enable Check
GART_RDREQPATH_SEL	6	0x0	Read request path 0=HDP 1=Direct Rd Req to MC
GART_INVALIDATE_TLB	8	0x0	Write 1 to invalidates all GART TLB entries

PCIE_TX_GART_DISCARD_RD_ADDR_LO - RW - 32 bits - PCIEIND:0x11			
Field Name	**Bits**	**Default**	**Description**
GART_DISCARD_RD_ADDR_LO	31:0	0x0	Lower address where GART should send reads that are suppose to be discarded NOTE: Bits 0:11 of this field are hardwired to ZERO.

PCIE_TX_GART_DISCARD_RD_ADDR_HI - RW - 32 bits - PCIEIND:0x12			
Field Name	**Bits**	**Default**	**Description**
GART_DISCARD_RD_ADDR_HI	7:0	0x0	Upper address where GART should send reads that are suppose to be discarded

PCIE_TX_GART_BASE - RW - 32 bits - PCIEIND:0x13			
Field Name	**Bits**	**Default**	**Description**
GART_BASE	31:0	0x0	Framebuffer offset where the start of GART table is located, if using the HDP path this should be programmed to offset from MC_FB_START. if using the MC-gart interface should be set to absolute address in the chip address space. NOTE: Bits 0:3 of this field are hardwired to ZERO.

PCIE_TX_GART_START_LO - RW - 32 bits - PCIEIND:0x14			
Field Name	**Bits**	**Default**	**Description**
GART_START_LO	31:0	0x0	Lower address of the start range of the GART translation NOTE: Bits 0:11 of this field are hardwired to ZERO.

PCIE_TX_GART_START_HI - RW - 32 bits - PCIEIND:0x15			
Field Name	**Bits**	**Default**	**Description**
GART_START_HI	7:0	0x0	Upper address of the start range of the GART translation

PCIE_TX_GART_END_LO - RW - 32 bits - PCIEIND:0x16			
Field Name	**Bits**	**Default**	**Description**
GART_END_LO	31:0	0x0	Lower address of the end range of the GART translation NOTE: Bits 0:11 of this field are hardwired to ZERO.

PCIE_TX_GART_END_HI - RW - 32 bits - PCIEIND:0x17			
Field Name	**Bits**	**Default**	**Description**
GART_END_HI	7:0	0x0	Upper address of the end range of the GART translation

PCIE_TX_GART_ERROR - R - 32 bits - PCIEIND:0x18			
Field Name	**Bits**	**Default**	**Description**
GART_UNMAPPED	1	0x0	Indicates a request was attempted with the address out of the GART range 0=No errors 1=A request was attempted with the address out of the GART range
GART_INVALID_READ	2	0x0	Indicates an invalid read was attempted 0=No errors 1=A read was attempted with the W bit not set in the gart entry

GART_INVALID_WRITE	3	0x0	Indicates an invalid write was attempted 0=No errors 1=A write was attempted with the R bit not set in the gart entry
GART_INVALID_ADDR	31:4	0x0	The lower address of the invalid request

GART ERROR status register

PCIE_TX_GART_LRU_MRU_PTR - R - 32 bits - PCIEIND:0x20			
Field Name	**Bits**	**Default**	**Description**
GART_LRU_PTR	4:0	0x0	LRU ptr
GART_MRU_PTR	12:8	0x0	MRU ptr

GART debug registers

PCIE_TX_GART_STATUS - R - 32 bits - PCIEIND:0x21			
Field Name	**Bits**	**Default**	**Description**
GART_STATUS	31:0	0x0	State of GART SM

GART debug registers

PCIE_TX_GART_TLB_VALID - R - 32 bits - PCIEIND:0x22			
Field Name	**Bits**	**Default**	**Description**
GART_TLB_VALID	31:0	0x0	Valid bit for the each TLB

GART debug registers

PCIE_TX_GART_TLB0_DATA - R - 32 bits - PCIEIND:0x23			
Field Name	**Bits**	**Default**	**Description**
GART_TLB0_DATA	25:0	0x0	Data for TLB
GART_TLB0_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB0

PCIE_TX_GART_TLB1_DATA - R - 32 bits - PCIEIND:0x24			
Field Name	**Bits**	**Default**	**Description**
GART_TLB1_DATA	25:0	0x0	Data for TLB
GART_TLB1_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB1

PCIE_TX_GART_TLB2_DATA - R - 32 bits - PCIEIND:0x25			
Field Name	**Bits**	**Default**	**Description**
GART_TLB2_DATA	25:0	0x0	Data for TLB
GART_TLB2_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB2

PCIE_TX_GART_TLB3_DATA - R - 32 bits - PCIEIND:0x26

Field Name	Bits	Default	Description
GART_TLB3_DATA	25:0	0x0	Data for TLB
GART_TLB3_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB3

PCIE_TX_GART_TLB4_DATA - R - 32 bits - PCIEIND:0x27			
Field Name	**Bits**	**Default**	**Description**
GART_TLB4_DATA	25:0	0x0	Data for TLB
GART_TLB4_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB4

PCIE_TX_GART_TLB5_DATA - R - 32 bits - PCIEIND:0x28			
Field Name	**Bits**	**Default**	**Description**
GART_TLB5_DATA	25:0	0x0	Data for TLB
GART_TLB5_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB5

PCIE_TX_GART_TLB6_DATA - R - 32 bits - PCIEIND:0x29			
Field Name	**Bits**	**Default**	**Description**
GART_TLB6_DATA	25:0	0x0	Data for TLB
GART_TLB6_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB6

PCIE_TX_GART_TLB7_DATA - R - 32 bits - PCIEIND:0x2A			
Field Name	**Bits**	**Default**	**Description**
GART_TLB7_DATA	25:0	0x0	Data for TLB
GART_TLB7_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB7

PCIE_TX_GART_TLB8_DATA - R - 32 bits - PCIEIND:0x2B			
Field Name	**Bits**	**Default**	**Description**
GART_TLB8_DATA	25:0	0x0	Data for TLB
GART_TLB8_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB8

PCIE_TX_GART_TLB9_DATA - R - 32 bits - PCIEIND:0x2C			
Field Name	**Bits**	**Default**	**Description**
GART_TLB9_DATA	25:0	0x0	Data for TLB
GART_TLB9_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB9

PCIE_TX_GART_TLB10_DATA - R - 32 bits - PCIEIND:0x2D			
Field Name	**Bits**	**Default**	**Description**
GART_TLB10_DATA	25:0	0x0	Data for TLB
GART_TLB10_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB10

PCIE_TX_GART_TLB11_DATA - R - 32 bits - PCIEIND:0x2E			
Field Name	**Bits**	**Default**	**Description**
GART_TLB11_DATA	25:0	0x0	Data for TLB
GART_TLB11_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB11

PCIE_TX_GART_TLB12_DATA - R - 32 bits - PCIEIND:0x2F			
Field Name	**Bits**	**Default**	**Description**
GART_TLB12_DATA	25:0	0x0	Data for TLB
GART_TLB12_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB12

PCIE_TX_GART_TLB13_DATA - R - 32 bits - PCIEIND:0x30			
Field Name	**Bits**	**Default**	**Description**
GART_TLB13_DATA	25:0	0x0	Data for TLB
GART_TLB13_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB13

PCIE_TX_GART_TLB14_DATA - R - 32 bits - PCIEIND:0x31			
Field Name	**Bits**	**Default**	**Description**
GART_TLB14_DATA	25:0	0x0	Data for TLB
GART_TLB14_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB14

PCIE_TX_GART_TLB15_DATA - R - 32 bits - PCIEIND:0x32			
Field Name	**Bits**	**Default**	**Description**
GART_TLB15_DATA	25:0	0x0	Data for TLB
GART_TLB15_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB15

PCIE_TX_GART_TLB16_DATA - R - 32 bits - PCIEIND:0x33			
Field Name	**Bits**	**Default**	**Description**
GART_TLB16_DATA	25:0	0x0	Data for TLB
GART_TLB16_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB16

PCIE_TX_GART_TLB17_DATA - R - 32 bits - PCIEIND:0x34			
Field Name	**Bits**	**Default**	**Description**
GART_TLB17_DATA	25:0	0x0	Data for TLB
GART_TLB17_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB17

PCIE_TX_GART_TLB18_DATA - R - 32 bits - PCIEIND:0x35			
Field Name	**Bits**	**Default**	**Description**
GART_TLB18_DATA	25:0	0x0	Data for TLB
GART_TLB18_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB18

PCIE_TX_GART_TLB19_DATA - R - 32 bits - PCIEIND:0x36			
Field Name	**Bits**	**Default**	**Description**
GART_TLB19_DATA	25:0	0x0	Data for TLB
GART_TLB19_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB19

PCIE_TX_GART_TLB20_DATA - R - 32 bits - PCIEIND:0x37			
Field Name	**Bits**	**Default**	**Description**
GART_TLB20_DATA	25:0	0x0	Data for TLB
GART_TLB20_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB20

PCIE_TX_GART_TLB21_DATA - R - 32 bits - PCIEIND:0x38			
Field Name	**Bits**	**Default**	**Description**
GART_TLB21_DATA	25:0	0x0	Data for TLB
GART_TLB21_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB21

PCIE_TX_GART_TLB22_DATA - R - 32 bits - PCIEIND:0x39			
Field Name	**Bits**	**Default**	**Description**
GART_TLB22_DATA	25:0	0x0	Data for TLB
GART_TLB22_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB22

PCIE_TX_GART_TLB23_DATA - R - 32 bits - PCIEIND:0x3A			
Field Name	**Bits**	**Default**	**Description**
GART_TLB23_DATA	25:0	0x0	Data for TLB
GART_TLB23_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB23

PCIE_TX_GART_TLB24_DATA - R - 32 bits - PCIEIND:0x3B			
Field Name	**Bits**	**Default**	**Description**
GART_TLB24_DATA	25:0	0x0	Data for TLB
GART_TLB24_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB24

PCIE_TX_GART_TLB25_DATA - R - 32 bits - PCIEIND:0x3C			
Field Name	**Bits**	**Default**	**Description**
GART_TLB25_DATA	25:0	0x0	Data for TLB
GART_TLB25_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB25

PCIE_TX_GART_TLB26_DATA - R - 32 bits - PCIEIND:0x3D			
Field Name	**Bits**	**Default**	**Description**
GART_TLB26_DATA	25:0	0x0	Data for TLB
GART_TLB26_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB26

PCIE_TX_GART_TLB27_DATA - R - 32 bits - PCIEIND:0x3E			
Field Name	**Bits**	**Default**	**Description**
GART_TLB27_DATA	25:0	0x0	Data for TLB
GART_TLB27_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB27

PCIE_TX_GART_TLB28_DATA - R - 32 bits - PCIEIND:0x3F			
Field Name	**Bits**	**Default**	**Description**
GART_TLB28_DATA	25:0	0x0	Data for TLB
GART_TLB28_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB28

PCIE_TX_GART_TLB29_DATA - R - 32 bits - PCIEIND:0x40			
Field Name	**Bits**	**Default**	**Description**
GART_TLB29_DATA	25:0	0x0	Data for TLB
GART_TLB29_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB29

PCIE_TX_GART_TLB30_DATA - R - 32 bits - PCIEIND:0x41			
Field Name	**Bits**	**Default**	**Description**
GART_TLB30_DATA	25:0	0x0	Data for TLB
GART_TLB30_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB330

PCIE_TX_GART_TLB31_DATA - R - 32 bits - PCIEIND:0x42			
Field Name	**Bits**	**Default**	**Description**
GART_TLB31_DATA	25:0	0x0	Data for TLB
GART_TLB31_VALID	31	0x0	Valid bit for TLB

GART debug registers - Data and valid bit on TLB31

PCIE_FLOW_CNTL - RW - 32 bits - PCIEIND:0x60			
Field Name	**Bits**	**Default**	**Description**
FC_P_CREDITS	1:0	0x0	0=30 credits 1=64 credits 2=16 credits 3=8 credits
FC_NP_CREDITS	3:2	0x0	0=2 credits 1=4 credits 2=1 credit 3=reserved
FC_CPL_CREDITS	5:4	0x0	0=128 credits 1=64 credits 2=32 credits 3=16 credits

Flow Control Register

PCIE_TXRX_DEBUG_SEQNUM - RW - 32 bits - PCIEIND:0x61			
Field Name	**Bits**	**Default**	**Description**
TXRX_DEBUG_SEQNUM	11:0	0x0	TX/RX Debug Sequence Number

TX/RX Debug Sequence Number Registers

PCIE_TXRX_TEST_MODE - RW - 32 bits - PCIEIND:0x62			
Field Name	**Bits**	**Default**	**Description**
TXRX_TEST_MODE	0	0x0	1=enable programmable Sequence Number

TX programmable Sequence Number for debug only

PCIE_RX_CNTL - RW - 32 bits - PCIEIND:0x70			
Field Name	**Bits**	**Default**	**Description**
RX_IGNORE_IOREQ_ERR	0	0x1	Ignore IO req errors
RX_IGNORE_LEN_MISMATCH_ERR	1	0x1	Ignore Malformed Length Mismatch Errors
RX_IGNORE_BE_ERR	2	0x1	Ignore Malformed Byte Enable TLP Errors
RX_IGNORE_MSG_ERR	3	0x0	Ignore Malformed Message Error
RX_IGNORE_CRC_ERR	4	0x0	Ignore CRC Errors
RX_IGNORE_CFG_ERR	5	0x0	Ignore Malformed Configuration Errors
RX_IGNORE_FC_ERR	6	0x0	Ignore Flow Control Error
RX_MRDLK_COMPAT	7	0x0	Mem RD LK transactions should be treated as UR for non-legacy devices
RX_NACK_IF_FIFO_FULL	8	0x0	Nak packets in case of overflow- not implemented
RX_NACK_IF_CFG_BUSY	9	0x0	Nak packets in case of CFG cycles busy- limited functionality
RX_MSG_LOCK_EN	10	0x0	Enable the lock msg
RX_SB_REORDER_EN	11	0x1	Enable the reorder 0=No re-ordering 1=Re-ordering
RX_EP_COMPAT_DIS	12	0x1	Disable detecting poisoned errors
RX_MAS_CPL_TIMEOUT	15:13	0x0	Master cpl time out 0=Disable 1=10ms 2=20ms 3=50ms 4=100ms 5=500ms 6=1s 7=10s
RX_CHECK_CFG_RD_ROUTE_ID_EN	16	0x0	Check the cfg route ID
RX_INVALID_SIZE_CPL_DIS	17	0x1	Disable detecting of invalid cpl sizes, limited functionality, should be set to one
RX_UNEXP_CPL_DIS	18	0x0	Disable reporting errors for unexpected cpl
RX_IGNORE_MAX_PAYLOAD_ERR	19	0x1	Ignore Malformed Maximum Payload Errors
RX_MRDLK_CPL_SEL	20	0x0	Select the cpl type of the mem rd lock
RX_GEN_ERR_INT	21	0x0	Gen errors in case of INT
RX_THROTTLE_MODE	23:22	0x0	Throttle transaction in case of unavailable credits, limited functionality, shouldn't be changed from the default, only for testing
RX_GENONENAK	30	0x1	Gen one Nak only until the next ACK
RX_UNLOCK_ON (R)	31	0x0	Unlock msg received

RX Control Register

PCIE_RX_NUM_NACK - R - 32 bits - PCIEIND:0x71

Field Name	Bits	Default	Description
RX_NUM_NACK	31:0	0x0	The number of Nak received from the time of Power up, hot reset, or link-dn

the number of Nak received

PCIE_RX_NUM_NACK_GENERATED - R - 32 bits - PCIEIND:0x72			
Field Name	**Bits**	**Default**	**Description**
RX_NUM_NACK_GENERATED	31:0	0x0	The number of Nak generated from the time of Power up, hot reset, or link-dn

The number of Nak generated

PCIE_RX_ACK_NACK_LATENCY - R - 32 bits - PCIEIND:0x73			
Field Name	**Bits**	**Default**	**Description**
RX_ACK_NACK_LATENCY	31:0	0x0	The number of cycles between the receiving the a tlp and to send back a Ack/Nak. this register is for debugging only

ACK/NACK Latency

PCIE_RX_ACK_NACK_LATENCY_THRESHOLD - R - 32 bits - PCIEIND:0x74			
Field Name	**Bits**	**Default**	**Description**
RX_ACK_NACK_LATENCY_TH	31:0	0x0	ACK/NACK Latency Threshold

PCIE_RX_TLP_HDR0 - R - 32 bits - PCIEIND:0x75			
Field Name	**Bits**	**Default**	**Description**
RX_TLP_HDR0	31:0	0x0	Contents of the last received TLP Header (bits 31:0)

RX TLP Header Register

PCIE_RX_TLP_HDR1 - R - 32 bits - PCIEIND:0x76			
Field Name	**Bits**	**Default**	**Description**
RX_TLP_HDR1	31:0	0x0	Contents of the last received Header (bits 63:32)

RX TLP Header Register

PCIE_RX_TLP_HDR2 - R - 32 bits - PCIEIND:0x77			
Field Name	**Bits**	**Default**	**Description**
RX_TLP_HDR2	31:0	0x0	Contents of the last received TLP Header (bits 95:64)

RX TLP Header Register

PCIE_RX_TLP_HDR3 - R - 32 bits - PCIEIND:0x78			
Field Name	**Bits**	**Default**	**Description**
RX_TLP_HDR3	31:0	0x0	Contents of the last received TLP Header (bits 127:96)

RX TLP Header Register

PCIE_RX_TLP_HDR4 - R - 32 bits - PCIEIND:0x79			
Field Name	**Bits**	**Default**	**Description**
RX_TLP_HDR4	31:0	0x0	Hard-coded to zero

RX TLP Header Register

PCIE_RX_TLP_CRC - R - 32 bits - PCIEIND:0x7A			
Field Name	**Bits**	**Default**	**Description**
RX_TLP_CRC	31:0	0x0	CRC value of the last received TLP

RX TLP CRC Register

PCIE_RX_DLP0 - R - 32 bits - PCIEIND:0x7B			
Field Name	**Bits**	**Default**	**Description**
RX_DLP0	31:0	0x0	Debug register: last received dlp bit [31:0]

last received dlp

PCIE_RX_DLP1 - R - 32 bits - PCIEIND:0x7C			
Field Name	**Bits**	**Default**	**Description**
RX_DLP1	31:0	0x0	Debug register: last received dlp bit [47:32]

last received dlp

PCIE_RX_DLP_CRC - R - 32 bits - PCIEIND:0x7D			
Field Name	**Bits**	**Default**	**Description**
RX_DLP_CRC	31:0	0x0	debug register: crc for the last received dlp

last dlp crc

PCIE_RX_CREDITS_ALLOCATED - R - 32 bits - PCIEIND:0x7E			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_PH	7:0	0x0	For posted TLP header, the number of FC units granted to transmitter since initialization, modulo 256
RX_CREDITS_ALLOCATED_NPH	15:8	0x0	For non-posted TLP header, the number of FC units granted to transmitter since initialization, modulo 256
RX_CREDITS_ALLOCATED_CPLH	23:16	0x0	For completion TLP header, the number of FC units granted to transmitter since initialization, modulo 256

PCIE_RX_CREDITS_ALLOCATED_D - R - 32 bits - PCIEIND:0x7F			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_PD	11:0	0x0	For posted TLP data, the number of FC units granted to transmitter since initialization, modulo 4096

RX_CREDITS_ALLOCATED_NPD	27:16	0x0	For non-posted TLP data, the number of FC units granted to transmitter since initialization, modulo 4096

PCIE_RX_CREDITS_ALLOCATED_CPLD - R - 32 bits - PCIEIND:0x80			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_CPLD	11:0	0x0	For completion TLP data, the number of FC units granted to transmitter since initialization, modulo 4096

PCIE_RX_CREDITS_RECEIVED - R - 32 bits - PCIEIND:0x81			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_PH	7:0	0x0	For posted TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256
RX_CREDITS_RECEIVED_NPH	15:8	0x0	For non-posted TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256
RX_CREDITS_RECEIVED_CPLH	23:16	0x0	For completion TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256

PCIE_RX_CREDITS_RECEIVED_D - R - 32 bits - PCIEIND:0x82			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_PD	11:0	0x0	For posted TLP data, the number of FC units consumed by valid TLP received since initialization, modulo 4096
RX_CREDITS_RECEIVED_NPD	27:16	0x0	For non-posted TLP data, the number of FC units consumed by valid TLP received since initialization, modulo 4096

PCIE_RX_CREDITS_RECEIVED_CPLD - R - 32 bits - PCIEIND:0x83			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_CPLD	11:0	0x0	For Completion TLP data, the number of FC units consumed by valid TLP received since initialization, module 4096

RX Credits Received Completion Data Register

PCIE_RX_MAL_TLP_COUNT - R - 32 bits - PCIEIND:0x84			
Field Name	**Bits**	**Default**	**Description**
RX_MAL_TLP_COUNT	11:0	0x0	Record the number of malfunction TLPs received

PCIE_RX_ERR_LOG - RW - 32 bits - PCIEIND:0x85			
Field Name	**Bits**	**Default**	**Description**

RX_ERR_LOG	31:0	0x0	errors detected by receiver, any write to this register will reset the value to zero. please note this is a debug register note to be used for driver or bios applications as the actual content of the register is not predictable

Receiver Error log

PCIE_RX_EXPECTED_SEQNUM - R - 32 bits - PCIEIND:0x86			
Field Name	**Bits**	**Default**	**Description**
RX_EXPECTED_SEQNUM	11:0	0x0	for debug only: should have the next expected seq number

next Expected Seq Number

PCIE_CI_CNTL - RW - 32 bits - PCIEIND:0x90			
Field Name	**Bits**	**Default**	**Description**
CI_BE_SPLIT_MODE	1:0	0x0	0=Normal byte splitting rules for PCI-Express 1.0A 1=Force a split on QW boundary with maximum packet length = 2 2=Bypass mode that forces full byte enables
CI_SLAVE_GEN_USR_DIS	2	0x0	0=Sends USR for invalid addresses 1=Disables slave from sending USR, and instead sends a successful CMPLT_D with dummy data.
CI_GART_PRIORITY	3	0x1	0=GART slave requests do not have priority 1=GART slave requests have priority
CI_WR_TO_RD_IDLE_INSERTION_EN	4	0x0	0=Disable inserting of idle cycle before the read request to HDP 1=Enable inserting of idle cycles before the read requests to HDP
CI_WR_TO_RD_IDLE_INSERTION_CNTR	12:5	0x20	Write to read idle insertion delay count

CI Control Register

PCIE_CI_FLUSH_CNTL - RW - 32 bits - PCIEIND:0x91			
Field Name	**Bits**	**Default**	**Description**
CI_FLUSH_EN	0	0x0	0=Disable 1=Enable
CI_FLUSH_COMPLETED	1	0x0	flush not done/DONE
CI_FLUSH_ADDR	31:3	0x0	flush specified address

FLUSH OPERATION CONTROL REGISTER

PCIE_CI_PANIC - RW - 32 bits - PCIEIND:0x92			
Field Name	**Bits**	**Default**	**Description**
CI_PANIC_TIMER	31:0	0x0	CI_PANIC_TIMER[0] 0 means disabled. CI_PANIC_TIMER[0] 1 to enable the PANIC timer. When non-zero => when HDP request is stalled for amount of BCLK cycles set in CI_PANIC_TIMER[31:0], BIF_MC_pri will be asserted

PCIE_CI_HANG - RW - 32 bits - PCIEIND:0x93			
Field Name	**Bits**	**Default**	**Description**
CI_HANG_TIMER	31:0	0x0	CI_HANG_TIMER[0] 0 means disabled. CI_HANG_TIMER[0] 1 to enable the Hang timer When non-zero => when RBBM or HDP is stalled for amount of clks request is dropped, and dummy data is taken for readback

PCIE_LC_CNTL - RW - 32 bits - PCIEIND:0xA0			
Field Name	**Bits**	**Default**	**Description**
LC_N_FTS (R)	7:0	0x0	Number of FTs from the other end of the link
LC_L0S_INACTIVITY	11:8	0x0	L0s inactivity timer setting
LC_L1_INACTIVITY	15:12	0x0	L1 inactivity timer setting
LC_PMI_TO_L1_DIS	16	0x0	Disable the transition to L1 caused by programming PMI_STATE to non-D0
LC_INC_N_FTS_EN	17	0x0	Enable incrementing N_FTS for each transition to recovery
LC_LOOK_FOR_IDLE_IN_L1L23	19:18	0x0	Controls the number of clocks to wait for Electrical Idle set in L1, L23
LC_FACTOR_IN_EXT_SYNC	20	0x0	Factor in the extended sync bit in the calculation for the replay timer adjustment
LC_WAIT_FOR_PM_ACK_DIS	21	0x0	Disables waiting for PM_ACK in L23 ready entry handshake
LC_HW_DEBUG	31:24	0x0	[0] Wait for Electrical idle in L1/L23 ready value (this bit is inverted before being used in the code). [1] Enable L1/L23 entry escape arcs, [2] Ignore PHY Electrical idle detector

Link Control Register

PCIE_LC_N_FTS_CNTL - RW - 32 bits - PCIEIND:0xA1			
Field Name	**Bits**	**Default**	**Description**
LC_XMIT_N_FTS	7:0	0xc	Programmable number of fast train sequences to override the strap value.
LC_XMIT_N_FTS_OVRIDE_EN	8	0x0	Enable the previous field to override the strap value for N_FTS.
LC_XMIT_N_FTS_LIMIT	23:16	0xff	Limit that the number of FTS can increment to, when incrementing is enabled.

Fast Train Sequence Control Register

PCIE_LC_STATE0 - R - 32 bits - PCIEIND:0xA5			
Field Name	**Bits**	**Default**	**Description**
LC_CURRENT_STATE	5:0	0x0	Current LC State
LC_PREV_STATE1	13:8	0x0	1st Previous LC State
LC_PREV_STATE2	21:16	0x0	2nd Previous LC State
LC_PREV_STATE3	29:24	0x0	3rd Previous LC State

Link Control State Register

PCIE_LC_STATE1 - R - 32 bits - PCIEIND:0xA6			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE4	5:0	0x0	4th Previous LC State
LC_PREV_STATE5	13:8	0x0	5th Previous LC State
LC_PREV_STATE6	21:16	0x0	6th Previous LC State
LC_PREV_STATE7	29:24	0x0	7th Previous LC State

Link Control State Register

PCIE_LC_STATE2 - R - 32 bits - PCIEIND:0xA7			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE8	5:0	0x0	8th Previous LC State
LC_PREV_STATE9	13:8	0x0	9th Previous LC State
LC_PREV_STATE10	21:16	0x0	10th Previous LC State
LC_PREV_STATE11	29:24	0x0	11th Previous LC State

Link Control State Register

PCIE_LC_STATE3 - R - 32 bits - PCIEIND:0xA8			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE12	5:0	0x0	12th Previous LC State
LC_PREV_STATE13	13:8	0x0	13th Previous LC State
LC_PREV_STATE14	21:16	0x0	14th Previous LC State
LC_PREV_STATE15	29:24	0x0	15th Previous LC State

Link Control State Register

PCIE_LC_STATE4 - R - 32 bits - PCIEIND:0xA9			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE16	5:0	0x0	16th Previous LC State
LC_PREV_STATE17	13:8	0x0	17th Previous LC State
LC_PREV_STATE18	21:16	0x0	18th Previous LC State
LC_PREV_STATE19	29:24	0x0	19th Previous LC State

Link Control State Register

PCIE_LC_STATE5 - R - 32 bits - PCIEIND:0xAA			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE20	5:0	0x0	20th Previous LC State
LC_PREV_STATE21	13:8	0x0	21st Previous LC State
LC_PREV_STATE22	21:16	0x0	22nd Previous LC State
LC_PREV_STATE23	29:24	0x0	23rd Previous LC State

Link Control State Register

PCIE_LC_LINK_WIDTH_CNTL - RW - 32 bits - PCIEIND:0xA2			
Field Name	**Bits**	**Default**	**Description**
LC_LINK_WIDTH	2:0	0x6	0=0 1=1 2=2 3=4 4=8 5=12 6=16
LC_LINK_WIDTH_RD (R)	6:4	0x0	Read back link width
LC_RECONFIG_NOW	8	0x0	RESERVED
LC_RECONFIG_LATER	9	0x0	RESERVED
LC_SHORT_RECONFIG_EN	11	0x0	RESERVED

Link Width Control

PCIE_LC_FORCE_SYNC_LOSS_CNTL - RW - 32 bits - PCIEIND:0xAB			
Field Name	**Bits**	**Default**	**Description**
LC_FORCE_SYNC_LOSS_DURATION	7:0	0x3	0=Duration of blocking the received data during enabling/disabling the transmitter
LC_FORCE_SYNC_LOSS_LATENCY	15:8	0x8	0=Latency for moving the event of blocking the received data
LC_FORCE_SYNC_LOSS_AT_ENTR_TXIDL_EN	16	0x0	0=Enable blocking the received data during disabling the transmitter
LC_FORCE_SYNC_LOSS_AT_EXT_TXIDL_EN	17	0x0	0=Enable blocking the received data during enabling the transmitter

PCIE_P_CNTL - RW - 32 bits - PCIEIND:0xB0			
Field Name	**Bits**	**Default**	**Description**
P_PWRDN_EN	0	0x0	0=All PLLs are always running 1=PLL is turned off on unused lanes
P_LOOPBACK_EN	1	0x0	0=This register does not apply to endpoint graphics card
P_PLL_TEST_MODE	2	0x0	Not used 0=Enable PLL Test mode. 1x TXCLK will be brought onto the transmitter
P_PLL_PWRDN_IN_L1	3	0x0	0=PLL is always running regardless of Link States 1=PLL will be turned off during L1
P_TXCLK_MUX_PROG_DLY	6:4	0x0	Programmable Delay for TXCLK before switching back to PLL clock when PLL is turned off during L1 or L2/L3 0=16us 1=24us 2=32us 3=40us 4=48us 5=56us 6=64us 7=72us
P_RX_DISABLE_IN_L0S	7	0x0	0=Keep B_PRX_EN high in L0s 1=Turn off B_PRX_EN in L0s
P_TXCLK_PM_MODE	8	0x1	0=Legacy TXCLK clock gating. Only TXCLK going to upper layers (tx, rx, ci) is OFF during L1 & L2/L3 1=Aggressive TXCLK clock gating. All TXCLK going to bif_core is OFF during L1 & L2/L3
P_PLL_BUF_PDNB	9	0x1	0=Turn off 10X CLKBUF inside PHY during L1 & L2/L3 1=Keep 10X CLKBUF running inside PHY

P_SYMALIGN_MODE	10	0x0	0=Relax Mode - Update symbol lock right away when detected bit shifts without waiting for confirmation 1=Agressive Mode - Always need confirmation for asserting Data Valid
P_VCOREF	13:12	0x0	0=OFF 1=VDD/4 2=VDD/2 3=3VDD/4
P_CALREF	15:14	0x0	PLL calibration reference voltage
P_BMODE_PLL_0 (R)	19:16	0x0	Status Signals generated by PLL_0 corresponding to Lanes 0-3
P_BMODE_PLL_1 (R)	23:20	0x0	Status Signals generated by PLL_1 corresponding to Lanes 4-7
P_BMODE_PLL_2 (R)	27:24	0x0	Status Signals generated by PLL_2 corresponding to Lanes 8-11
P_BMODE_PLL_3 (R)	31:28	0x0	Status Signals generated by PLL_3 corresponding to Lanes 12-15

PCIE_P_CNTL2 - RW - 32 bits - PCIEIND:0xB1			
Field Name	**Bits**	**Default**	**Description**
PI_PHY90_PLLCAL	7:0	0xb	Used to set PHY90 PLL calibration completion time

PCIE_P_BUF_STATUS - RW - 32 bits - PCIEIND:0xB2			
Field Name	**Bits**	**Default**	**Description**
P_ELASTIC_BUF_OVERFLOW_0	0	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 0
P_ELASTIC_BUF_OVERFLOW_1	1	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 1
P_ELASTIC_BUF_OVERFLOW_2	2	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 2
P_ELASTIC_BUF_OVERFLOW_3	3	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 3
P_ELASTIC_BUF_OVERFLOW_4	4	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 4
P_ELASTIC_BUF_OVERFLOW_5	5	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 5
P_ELASTIC_BUF_OVERFLOW_6	6	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 6
P_ELASTIC_BUF_OVERFLOW_7	7	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 7
P_ELASTIC_BUF_OVERFLOW_8	8	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 8
P_ELASTIC_BUF_OVERFLOW_9	9	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 9
P_ELASTIC_BUF_OVERFLOW_10	10	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 10
P_ELASTIC_BUF_OVERFLOW_11	11	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 11
P_ELASTIC_BUF_OVERFLOW_12	12	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 12
P_ELASTIC_BUF_OVERFLOW_13	13	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 13
P_ELASTIC_BUF_OVERFLOW_14	14	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 14
P_ELASTIC_BUF_OVERFLOW_15	15	0x0	Rx to Tx time domain hand-off buffer under/over flow: lane 15
P_DESKEW_BUF_OVERFLOW_0	16	0x0	Symbol skew buffer over/underflow: lane 0
P_DESKEW_BUF_OVERFLOW_1	17	0x0	Symbol skew buffer over/underflow: lane 1
P_DESKEW_BUF_OVERFLOW_2	18	0x0	Symbol skew buffer over/underflow: lane 2
P_DESKEW_BUF_OVERFLOW_3	19	0x0	Symbol skew buffer over/underflow: lane 3
P_DESKEW_BUF_OVERFLOW_4	20	0x0	Symbol skew buffer over/underflow: lane 4
P_DESKEW_BUF_OVERFLOW_5	21	0x0	Symbol skew buffer over/underflow: lane 5
P_DESKEW_BUF_OVERFLOW_6	22	0x0	Symbol skew buffer over/underflow: lane 6
P_DESKEW_BUF_OVERFLOW_7	23	0x0	Symbol skew buffer over/underflow: lane 7
P_DESKEW_BUF_OVERFLOW_8	24	0x0	Symbol skew buffer over/underflow: lane 8
P_DESKEW_BUF_OVERFLOW_9	25	0x0	Symbol skew buffer over/underflow: lane 9
P_DESKEW_BUF_OVERFLOW_10	26	0x0	Symbol skew buffer over/underflow: lane 10
P_DESKEW_BUF_OVERFLOW_11	27	0x0	Symbol skew buffer over/underflow: lane 11
P_DESKEW_BUF_OVERFLOW_12	28	0x0	Symbol skew buffer over/underflow: lane 12
P_DESKEW_BUF_OVERFLOW_13	29	0x0	Symbol skew buffer over/underflow: lane 13
P_DESKEW_BUF_OVERFLOW_14	30	0x0	Symbol skew buffer over/underflow: lane 14

P_DESKEW_BUF_OVERFLOW_15	31	0x0	Symbol skew buffer over/underflow: lane 15
PHY BUFFER STATUS REGISTER			

PCIE_P_DECODER_STATUS - RW - 32 bits - PCIEIND:0xB3			
Field Name	**Bits**	**Default**	**Description**
P_DECODE_ERR_0	0	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_1	1	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_2	2	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_3	3	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_4	4	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_5	5	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_6	6	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_7	7	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_8	8	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_9	9	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_10	10	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_11	11	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_12	12	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_13	13	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_14	14	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DECODE_ERR_15	15	0x0	Indicates which lane has the decoding error, i.e. Can't decode the incoming data. bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_0	16	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_1	17	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_2	18	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc

P_DISPARITY_ERR_3	19	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_4	20	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_5	21	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_6	22	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_7	23	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_8	24	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_9	25	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_10	26	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_11	27	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_12	28	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_13	29	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_14	30	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc
P_DISPARITY_ERR_15	31	0x0	Indicates which lane has the link error: bit15 => Lane 15 (0 = OK, 1 = error), etc

PCIE_P_MISC_DEBUG_STATUS - RW - 32 bits - PCIEIND:0xB4			
Field Name	**Bits**	**Default**	**Description**
P_POWER_STATE (R)	1:0	0x0	Indicates the current power state 0=L0 1=L0s 2=L1 3=L2
P_LANE_REVERSAL (R)	2	0x0	Indicates if there is lane reversal 0=Lane order is normal 1=Lane order is reversed
P_LANE_WIDTH (R)	6:4	0x0	Indicates the lane configuration of the link 0=x16 1=x1 2=x2 3=x4 4=x8 5=x12 6=reserved 7=reserved
P_INSERT_ERROR_0	16	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane0 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_1	17	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane1 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_2	18	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane2 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_3	19	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane3 by replacing one symbol with an invalid symbol

P_INSERT_ERROR_4	20	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane4 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_5	21	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane5 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_6	22	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane6 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_7	23	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane7 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_8	24	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane8 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_9	25	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane9 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_10	26	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane10 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_11	27	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane11 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_12	28	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane12 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_13	29	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane13 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_14	30	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane14 by replacing one symbol with an invalid symbol
P_INSERT_ERROR_15	31	0x0	0=Normal Operation 1=Inserting error on Transmitting Lane15 by replacing one symbol with an invalid symbol

PCIE_P_IMP_CNTL_STRENGTH - RW - 32 bits - PCIEIND:0xC0			
Field Name	**Bits**	**Default**	**Description**
P_TX_STR_CNTL_READ_BACK (R)	3:0	0x0	Store the readback value of current controller
P_TX_IMP_CNTL_READ_BACK (R)	7:4	0x0	Store the readback value of TX impedance controller
P_RX_IMP_CNTL_READ_BACK (R)	11:8	0x0	Store the readback value of RX impedance controller
P_TX_STR_CNTL	19:16	0x7	Set the initial default current strength to 4'b0111
P_TX_IMP_CNTL	23:20	0x7	Default TX impedance control value
P_RX_IMP_CNTL	27:24	0x7	Default RX impedance control value
P_PAD_MANUAL_OVERRIDE	31	0x0	0=Allow normal impedance compensation operation 1=Default to manual settings

PHY IMPEDANCE CONTROL STRENGTH REGISTER

PCIE_P_IMP_CNTL_UPDATE - RW - 32 bits - PCIEIND:0xC1			
Field Name	**Bits**	**Default**	**Description**
P_IMP_PAD_UPDATE_RATE	4:0	0xf	PAD's update interval
P_IMP_PAD_SAMPLE_DELAY	12:8	0x1	Sampling window
P_IMP_PAD_INC_THRESHOLD	20:16	0x18	Incremental resolution

P_IMP_PAD_DEC_THRESHOLD	28:24	0x8	Decremental resolution

Impedance PAD defaults

PCIE_P_STR_CNTL_UPDATE - RW - 32 bits - PCIEIND:0xC2			
Field Name	**Bits**	**Default**	**Description**
P_STR_PAD_UPDATE_RATE	4:0	0xf	Pad Strength update interval
P_STR_PAD_SAMPLE_DELAY	12:8	0x1	Sampling window
P_STR_PAD_INC_THRESHOLD	20:16	0x18	Incremental resolution
P_STR_PAD_DEC_THRESHOLD	28:24	0x8	Decremental resolution

Pad Strength Control Registers

PCIE_P_PAD_MISC_CNTL - RW - 32 bits - PCIEIND:0xC3			
Field Name	**Bits**	**Default**	**Description**
P_PAD_I_DUMMYOUT (R)	0	0x0	Input from analog - 0 if PMOS cur is stronger
P_PAD_IMP_DUMMYOUT (R)	1	0x0	Input from analog - 0 if PMOS imp is stronger
P_PAD_IMP_TESTOUT (R)	2	0x0	Input from analog - 1 if NMOS imp is stronger
P_LINK_RETRAIN_ON_ERR_ENABLE	3	0x0	Disable error counts in LaneDeskew if Symbol unlocking, Code Errors or Deskew Errors are detected
P_RCVR_SYMUNLOCK_ERR_VALUE	7:4	0xf	Threshold value for symbol unlock errors used by Receiver Error reporting
P_RCVR_DESKEW_ERR_VALUE	11:8	0xf	Threshold value for deskew errors used by Receiver Error reporting
P_RCVR_DECODE_ERR_VALUE	15:12	0xf	Threshold value for decode errors used by Receiver Error reporting
P_RCVR_TOTAL_ERR_VALUE	21:16	0x3f	Threshold value for combined symbol unlock, deskew and decode errors used by Receiver Error reporting

Pad Miscellaneous Control Registers

PCIE_P_SYMSYNC_CTL - RW - 32 bits - PCIEIND:0xC4			
Field Name	**Bits**	**Default**	**Description**
P_SYMSYNC_ELECT_IDLE_DET_EN	0	0x1	Use Electrical Idle Detect to filter out garbage data
P_SYMSYNC_SYNC_MODE	1	0x0	SYMSYNC synchronous mode - 1 look for iMGood consecutive good COMMAs, 0 look for iMGood consecutive good symbols
P_SYMSYNC_M_GOOD	9:2	0x10	M parameter of Good symbols or Commas (should be greater than two)
P_SYMSYNC_N_BAD	17:10	0x1	N parameter of Bad symbols (can be 1 or more)
P_SYMSYNC_PAD_MODE	19:18	0x3	Mode select of Good known symbols for replacement of the Bad symbols
Reserved	20	0x1	

SYMSYNC Control Registers

PCIE_P_DECODE_ERR_CNTL - RW - 32 bits - PCIEIND:0xC5			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_RESET	15:0	0x0	Decode Error Counter Reset
DISPARITY_ERR_CNT_RESET	31:16	0x0	Disparity Error Counter Reset

Receiver Decode Error Counter Control

PCIE_P_DECODE_ERR_CNT_0 - R - 32 bits - PCIEIND:0xF0			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_0	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_0	31:16	0x0	Disparity Error Counter

Receiver Decoder Error Counter for Lane 0

PCIE_P_DECODE_ERR_CNT_1 - R - 32 bits - PCIEIND:0xF1			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_1	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_1	31:16	0x0	Disparity Error Counter

Receiver Decoder Error Counter for Lane 1

PCIE_P_DECODE_ERR_CNT_2 - R - 32 bits - PCIEIND:0xF2			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_2	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_2	31:16	0x0	Disparity Error Counter

Receiver Decoder Error Counter for Lane 2

PCIE_P_DECODE_ERR_CNT_3 - R - 32 bits - PCIEIND:0xF3			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_3	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_3	31:16	0x0	Disparity Error Counter

Receiver Decoder Error Counter for Lane 3

PCIE_P_DECODE_ERR_CNT_4 - R - 32 bits - PCIEIND:0xF4			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_4	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_4	31:16	0x0	Disparity Error Counter

Receiver Decoder Error Counter for Lane 4

PCIE_P_DECODE_ERR_CNT_5 - R - 32 bits - PCIEIND:0xF5			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_5	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_5	31:16	0x0	Disparity Error Counter

Receiver Decoder Error Counter for Lane 5

PCIE_P_DECODE_ERR_CNT_6 - R - 32 bits - PCIEIND:0xF6			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_6	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_6	31:16	0x0	Disparity Error Counter

Receiver Decoder Error Counter for Lane 6

PCIE_P_DECODE_ERR_CNT_7 - R - 32 bits - PCIEIND:0xF7			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_7	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_7	31:16	0x0	Disparity Error Counter

Receiver Decoder Error Counter for Lane 7

PCIE_P_DECODE_ERR_CNT_8 - R - 32 bits - PCIEIND:0xF8			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_8	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_8	31:16	0x0	Disparity Error Counter

Receiver Decoder Error Counter for Lane 8

PCIE_P_DECODE_ERR_CNT_9 - R - 32 bits - PCIEIND:0xF9			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_9	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_9	31:16	0x0	Disparity Error Counter

Receiver Decoder Error Counter for Lane 9

PCIE_P_DECODE_ERR_CNT_10 - R - 32 bits - PCIEIND:0xFA			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_10	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_10	31:16	0x0	Disparity Error Counter

Receiver Decoder Error Counter for Lane 10

PCIE_P_DECODE_ERR_CNT_11 - R - 32 bits - PCIEIND:0xFB			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_11	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_11	31:16	0x0	Disparity Error Counter

Receiver Decoder Error Counter for Lane 11

PCIE_P_DECODE_ERR_CNT_12 - R - 32 bits - PCIEIND:0xFC			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_12	15:0	0x0	Decoder Error Counter

DISPARITY_ERR_CNT_12	31:16	0x0	Disparity Error Counter
Receiver Decoder Error Counter for Lane 12			

PCIE_P_DECODE_ERR_CNT_13 - R - 32 bits - PCIEIND:0xFD			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_13	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_13	31:16	0x0	Disparity Error Counter
Receiver Decoder Error Counter for Lane 13			

PCIE_P_DECODE_ERR_CNT_14 - R - 32 bits - PCIEIND:0xFE			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_14	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_14	31:16	0x0	Disparity Error Counter
Receiver Decoder Error Counter for Lane 14			

PCIE_P_DECODE_ERR_CNT_15 - R - 32 bits - PCIEIND:0xFF			
Field Name	**Bits**	**Default**	**Description**
CODE_ERR_CNT_15	15:0	0x0	Decoder Error Counter
DISPARITY_ERR_CNT_15	31:16	0x0	Disparity Error Counter
Receiver Decoder Error Counter for Lane 15			

PCIE_ERR_CNTL - RW - 32 bits - PCIEIND:0xE0			
Field Name	**Bits**	**Default**	**Description**
ERR_REPORTING_DIS	0	0x1	Disable PCI Express Advanced Error Reporting
SYM_UNLOCKED_EN	1	0x0	Enable Reporting of Symbol Unlocked Errors
Error Control Registers			

PCIE_CLK_RST_CNTL - RW - 32 bits - PCIEIND:0xE1			
Field Name	**Bits**	**Default**	**Description**
BIFBUSY_DLY_SEL	1:0	0x0	Select the delay to switch of the clock inside the PCIE blocks
GR_WHEN_LINK_DN_EN	8	0x0	Force Global reset when the link is down
GR_WHEN_HOT_RESET_EN	9	0x1	Force Global reset when hot reset is active
GR_DLY_SEL	11:10	0x0	Select the delay between link-down or hot-reset to the global reset assertion 0=0 msec 1=4 msec 2=8 msec 3=16 msec
PR_WHEN_LINK_DN_EN	12	0x0	Force Phy layer (PL) reset when the link is down
PR_WHEN_HOT_RESET_EN	13	0x1	DO NOT Force Phy reset (PL) when hot reset is active
PR_DLY_SEL	15:14	0x0	Select the delay between link-down or hot-reset to the phy reset assertion 0=0 msec 1=4 msec 2=8 msec 3=16 msec

Control the reset and clock inside the PCIE block

GENMO_WT - W - 8 bits - HIDEC:0x3C2			
Field Name	**Bits**	**Default**	**Description**
GENMO_MONO_ADDRESS_B	0	0x0	VGA addressing mode. 0=Monochrome emulation, regs at 0x3Bx 1=Color/Graphic emulation, regs at 0x3Dx
VGA_RAM_EN	1	0x0	Enables/Disables CPU access to video RAM at VGA aperture. 0=Disable 1=Enable

Miscellaneous Output Register (Write)

GENMO_RD - R - 8 bits - HIDEC:0x3CC			
Field Name	**Bits**	**Default**	**Description**
GENMO_MONO_ADDRESS_B (mirror of GENMO_WT:GENMO_MONO_ADDRESS_B)	0	0x0	VGA addressing mode. 0=Monochrome emulation, regs at 0x3Bx 1=Color/Graphic emulation, regs at 0x3Dx
VGA_RAM_EN (mirror of GENMO_WT:VGA_RAM_EN)	1	0x0	Enables/Disables CPU access to video RAM at VGA aperture. 0=Disable 1=Enable

Miscellaneous Output Register (Read)

PCIE_INDEX - RW - 32 bits - HIDEC:0x30			
Field Name	**Bits**	**Default**	**Description**
PCIE_INDEX	10:0	0x0	Indirect aperture index

PCIE Indirect Register Aperture Index Register

PCIE_DATA - RW - 32 bits - HIDEC:0x38			
Field Name	**Bits**	**Default**	**Description**
PCIE_DATA	31:0	0x0	Indirect aperture data

PCIE Indirect Register Aperture Data Register

2.3 PCIE Registers

PCIE_CLK_CNTL - RW - 32 bits - PCIEIND:0x400			
Field Name	**Bits**	**Default**	**Description**
FORCE_BIF_TXCLK	0	0x1	POSSIBLE VALUES: 0 - Dynamic, 1 - ForceOn
FORCE_BIF_TXCLK_IN_L0S	1	0x1	POSSIBLE VALUES: 0 - Dynamic, 1 - ForceOn
SEL_HDP_CLK	2	0x0	Select HDP CLK-Speed. POSSIBLE VALUES: 0 - PCIE_REFCLK, 1 - TXCLK
SEL_HDP_CLK_IN_VOLTAGE_DROP	3	0x1	Controls Dynamic Voltage drop for HDP CLK. POSSIBLE VALUES: 0 - EN, 1 - DIS
SEL_HDP_CLK_IN_STATIC_SCREEN	4	0x1	Selects HDP CLK in Static mode. POSSIBLE VALUES: 0 - TXCLK, 1 - PCIE_REFCLK -- works with SEL_HDP_CLK_IN_VOLTAGE_DROP
FORCE_RXCLK	5	0x1	Forces RXCLK in PM states. POSSIBLE VALUES: 0 - Dynamic, 1 - ForceOn
MAX_DELAY_RXCLK	9:6	0x4	Max delay b/w RX shut down request, and PHY realizing.

Registers for dynamic clock control

PCIE_PRBS10 - RW - 32 bits - PCIEIND:0x401			
Field Name	**Bits**	**Default**	**Description**
PRBS10_CLR	15:0	0x0	Clear PRBS10 checker for Lanes 15 down to 0
PRBS10_ERR (R)	31:16	0x0	PRBS10 error bit for Lanes 15 down to 0

PRBS10 registers for testing the PHY

PCIE_PRBS23_BITCNT0 - RW - 32 bits - PCIEIND:0x402			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane0

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT1 - RW - 32 bits - PCIEIND:0x403			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane1

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT2 - RW - 32 bits - PCIEIND:0x404			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane2

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT3 - RW - 32 bits - PCIEIND:0x405			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane3

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT4 - RW - 32 bits - PCIEIND:0x406			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane4

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT5 - RW - 32 bits - PCIEIND:0x407			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane5

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT6 - RW - 32 bits - PCIEIND:0x408			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane6

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT7 - RW - 32 bits - PCIEIND:0x409			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane7

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT8 - RW - 32 bits - PCIEIND:0x40A			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane8

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT9 - RW - 32 bits - PCIEIND:0x40B			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane9

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT10 - RW - 32 bits - PCIEIND:0x40C			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane10

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT11 - RW - 32 bits - PCIEIND:0x40D			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane11

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT12 - RW - 32 bits - PCIEIND:0x40E			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane12

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT13 - RW - 32 bits - PCIEIND:0x40F			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane13

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT14 - RW - 32 bits - PCIEIND:0x410			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane14

PRBS23 registers for testing the PHY

PCIE_PRBS23_BITCNT15 - RW - 32 bits - PCIEIND:0x411			
Field Name	**Bits**	**Default**	**Description**
PRBS23_BITCNT	31:0	0x0	A 32-bit counter to enable BER measurement by freezing error counter for Lane15

PRBS23 registers for testing the PHY

PCIE_PRBS23_ERRCNT0 - RW - 32 bits - PCIEIND:0x412			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane0

PRBS23 registers for testing the PHY

PCIE_PRBS23_ERRCNT1 - RW - 32 bits - PCIEIND:0x413			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane1

PRBS23 registers for testing the PHY

PCIE_PRBS23_ERRCNT2 - RW - 32 bits - PCIEIND:0x414			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane2

PRBS23 registers for testing the PHY

PCIE_PRBS23_ERRCNT3 - RW - 32 bits - PCIEIND:0x415			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane3

PRBS23 registers for testing the PHY

PCIE_PRBS23_ERRCNT4 - RW - 32 bits - PCIEIND:0x416			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane4

PRBS23 registers for testing the PHY

PCIE_PRBS23_ERRCNT5 - RW - 32 bits - PCIEIND:0x417			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane5

PRBS23 registers for testing the PHY

PCIE_PRBS23_ERRCNT6 - RW - 32 bits - PCIEIND:0x418			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane6

PRBS23 registers for testing the PHY

PCIE_PRBS23_ERRCNT7 - RW - 32 bits - PCIEIND:0x419			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane7
PRBS23 registers for testing the PHY			

PCIE_PRBS23_ERRCNT8 - RW - 32 bits - PCIEIND:0x41A			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane8
PRBS23 registers for testing the PHY			

PCIE_PRBS23_ERRCNT9 - RW - 32 bits - PCIEIND:0x41B			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane9
PRBS23 registers for testing the PHY			

PCIE_PRBS23_ERRCNT10 - RW - 32 bits - PCIEIND:0x41C			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane10
PRBS23 registers for testing the PHY			

PCIE_PRBS23_ERRCNT11 - RW - 32 bits - PCIEIND:0x41D			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane11
PRBS23 registers for testing the PHY			

PCIE_PRBS23_ERRCNT12 - RW - 32 bits - PCIEIND:0x41E			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane12
PRBS23 registers for testing the PHY			

PCIE_PRBS23_ERRCNT13 - RW - 32 bits - PCIEIND:0x41F			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane13
PRBS23 registers for testing the PHY			

PCIE_PRBS23_ERRCNT14 - RW - 32 bits - PCIEIND:0x420			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane14

PRBS23 registers for testing the PHY

PCIE_PRBS23_ERRCNT15 - RW - 32 bits - PCIEIND:0x421			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERRCNT (R)	31:0	0x0	Error counter for Lane15

PRBS23 registers for testing the PHY

PCIE_PRBS23_CTRL0 - RW - 32 bits - PCIEIND:0x422			
Field Name	**Bits**	**Default**	**Description**
PRBS23_ERR0 (R)	0	0x0	PRBS23 checker sticky error bit for Lane 0
PRBS23_ERR1 (R)	1	0x0	PRBS23 checker sticky error bit for Lane 1
PRBS23_ERR2 (R)	2	0x0	PRBS23 checker sticky error bit for Lane 2
PRBS23_ERR3 (R)	3	0x0	PRBS23 checker sticky error bit for Lane 3
PRBS23_ERR4 (R)	4	0x0	PRBS23 checker sticky error bit for Lane 4
PRBS23_ERR5 (R)	5	0x0	PRBS23 checker sticky error bit for Lane 5
PRBS23_ERR6 (R)	6	0x0	PRBS23 checker sticky error bit for Lane 6
PRBS23_ERR7 (R)	7	0x0	PRBS23 checker sticky error bit for Lane 7
PRBS23_ERR8 (R)	8	0x0	PRBS23 checker sticky error bit for Lane 8
PRBS23_ERR9 (R)	9	0x0	PRBS23 checker sticky error bit for Lane 9
PRBS23_ERR10 (R)	10	0x0	PRBS23 checker sticky error bit for Lane 10
PRBS23_ERR11 (R)	11	0x0	PRBS23 checker sticky error bit for Lane 11
PRBS23_ERR12 (R)	12	0x0	PRBS23 checker sticky error bit for Lane 12
PRBS23_ERR13 (R)	13	0x0	PRBS23 checker sticky error bit for Lane 13
PRBS23_ERR14 (R)	14	0x0	PRBS23 checker sticky error bit for Lane 14
PRBS23_ERR15 (R)	15	0x0	PRBS23 checker sticky error bit for Lane 15
PRBS23_CLR0	16	0x0	Clear PRBS23 checker error registers for Lane 0
PRBS23_CLR1	17	0x0	Clear PRBS23 checker error registers for Lane 1
PRBS23_CLR2	18	0x0	Clear PRBS23 checker error registers for Lane 2
PRBS23_CLR3	19	0x0	Clear PRBS23 checker error registers for Lane 3
PRBS23_CLR4	20	0x0	Clear PRBS23 checker error registers for Lane 4
PRBS23_CLR5	21	0x0	Clear PRBS23 checker error registers for Lane 5
PRBS23_CLR6	22	0x0	Clear PRBS23 checker error registers for Lane 6
PRBS23_CLR7	23	0x0	Clear PRBS23 checker error registers for Lane 7
PRBS23_CLR8	24	0x0	Clear PRBS23 checker error registers for Lane 8
PRBS23_CLR9	25	0x0	Clear PRBS23 checker error registers for Lane 9
PRBS23_CLR10	26	0x0	Clear PRBS23 checker error registers for Lane 10
PRBS23_CLR11	27	0x0	Clear PRBS23 checker error registers for Lane 11
PRBS23_CLR12	28	0x0	Clear PRBS23 checker error registers for Lane 12
PRBS23_CLR13	29	0x0	Clear PRBS23 checker error registers for Lane 13
PRBS23_CLR14	30	0x0	Clear PRBS23 checker error registers for Lane 14
PRBS23_CLR15	31	0x0	Clear PRBS23 checker error registers for Lane 15

PRBS23 registers for testing the PHY

PCIE_PRBS23_CTRL1 - RW - 32 bits - PCIEIND:0x423			
Field Name	**Bits**	**Default**	**Description**
PRBS23_FREERUN0	0	0x0	PRBS23 checker enable freerun for Lane 0
PRBS23_FREERUN1	1	0x0	PRBS23 checker enable freerun for Lane 1
PRBS23_FREERUN2	2	0x0	PRBS23 checker enable freerun for Lane 2
PRBS23_FREERUN3	3	0x0	PRBS23 checker enable freerun for Lane 3
PRBS23_FREERUN4	4	0x0	PRBS23 checker enable freerun for Lane 4
PRBS23_FREERUN5	5	0x0	PRBS23 checker enable freerun for Lane 5
PRBS23_FREERUN6	6	0x0	PRBS23 checker enable freerun for Lane 6
PRBS23_FREERUN7	7	0x0	PRBS23 checker enable freerun for Lane 7
PRBS23_FREERUN8	8	0x0	PRBS23 checker enable freerun for Lane 8
PRBS23_FREERUN9	9	0x0	PRBS23 checker enable freerun for Lane 9
PRBS23_FREERUN10	10	0x0	PRBS23 checker enable freerun for Lane 10
PRBS23_FREERUN11	11	0x0	PRBS23 checker enable freerun for Lane 11
PRBS23_FREERUN12	12	0x0	PRBS23 checker enable freerun for Lane 12
PRBS23_FREERUN13	13	0x0	PRBS23 checker enable freerun for Lane 13
PRBS23_FREERUN14	14	0x0	PRBS23 checker enable freerun for Lane 14
PRBS23_FREERUN15	15	0x0	PRBS23 checker enable freerun for Lane 15
PRBS23_LOCKED0 (R)	16	0x0	PRBS23 checker is locked for Lane 0
PRBS23_LOCKED1 (R)	17	0x0	PRBS23 checker is locked for Lane 1
PRBS23_LOCKED2 (R)	18	0x0	PRBS23 checker is locked for Lane 2
PRBS23_LOCKED3 (R)	19	0x0	PRBS23 checker is locked for Lane 3
PRBS23_LOCKED4 (R)	20	0x0	PRBS23 checker is locked for Lane 4
PRBS23_LOCKED5 (R)	21	0x0	PRBS23 checker is locked for Lane 5
PRBS23_LOCKED6 (R)	22	0x0	PRBS23 checker is locked for Lane 6
PRBS23_LOCKED7 (R)	23	0x0	PRBS23 checker is locked for Lane 7
PRBS23_LOCKED8 (R)	24	0x0	PRBS23 checker is locked for Lane 8
PRBS23_LOCKED9 (R)	25	0x0	PRBS23 checker is locked for Lane 9
PRBS23_LOCKED10 (R)	26	0x0	PRBS23 checker is locked for Lane 10
PRBS23_LOCKED11 (R)	27	0x0	PRBS23 checker is locked for Lane 11
PRBS23_LOCKED12 (R)	28	0x0	PRBS23 checker is locked for Lane 12
PRBS23_LOCKED13 (R)	29	0x0	PRBS23 checker is locked for Lane 13
PRBS23_LOCKED14 (R)	30	0x0	PRBS23 checker is locked for Lane 14
PRBS23_LOCKED15 (R)	31	0x0	PRBS23 checker is locked for Lane 15

PRBS23 registers for testing the PHY

PCIE_PRBS_EN - RW - 32 bits - PCIEIND:0x424			
Field Name	**Bits**	**Default**	**Description**
PRBS23_EN	0	0x0	PRBS23 generator is enabled for all 16 lanes
PRBS10_EN	16:1	0x0	PRBS10 generator is enabled for Lanes 15 down to 0
PRBS23_LOCKCNT	21:17	0xf	PRBS23 checker number of locked bits to sync

PRBS enable registers for testing the PHY

PCIE_XSTRAP1 - RW - 32 bits - PCIEIND:0x425			
Field Name	**Bits**	**Default**	**Description**
VGA_DIS (R)	0	0x0	Enable VGS controller capacity 0=VGA controller capacity enabled 1=the device will not be recognized as the system's VGA controller
Reserved	1:2	0x0	
SLV_ADR64_EN (R)	3	0x0	Slave DAC Decode. Decode dual address slave cycle and using 64-bit bar

ALL_VALID (R)	4	0x0	All the ROM straps are valid 0=false 1=true
Reserved	5:9	0x0	
MULTI_FUNC (R)	10	0x0	Multi-function device select 0=single function device 1=two function device
Reserved	11	0x0	
MSI_ENABLE (R)	12	0x0	Enable message signalled interrupt
Reserved	13:15	0x0	
DEBUG_ACCESS (R)	16	0x0	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible
Reserved	17:19, 21	0x0	
TX_PWRS_ENB (R)	22	0x0	Tx output current power save 0=50% less current 1=normal current
TX_DEEMPH_EN (R)	23	0x0	Tx de-emphasis enable 0=Tx de-emphasis disabled 1=Tx de-emphasis enabled
PLL_IBIAS_RD (R)	30:29	0x0	Bias current for the PCIE Express PHY PLL

Strap read back register 1

PCIE_XSTRAP2 - RW - 32 bits - PCIEIND:0x426			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	0x0	
Reserved	4	0x0	
MEM_AP_SIZE (R)	7:5	0x0	Size of the primary memory apertures claimed in PCI configuration space 0=128MB 1=256MB 2=64MB 3=32MB 4=512MB 5=1GB
Reserved	31:8	0x0	

Strap read back register 2

PCIE_XSTRAP5 - RW - 32 bits - PCIEIND:0x429			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID (R)	15:0	0x0	Sub-system vendor ID (SSVID) for PCIE configuration space
SUBSYSTEM_ID (R)	31:16	0x0	Sub-system ID (SSID) for PCI configuration space

Strap read back register 5

PCIE_INDEX - RW - 32 bits - HIDEC:0x30			
Field Name	**Bits**	**Default**	**Description**
PCIE_INDEX	10:0	0x0	Indirect aperture index

PCIE Indirect Register Aperture Index Register

PCIE_DATA - RW - 32 bits - HIDEC:0x38			
Field Name	**Bits**	**Default**	**Description**

PCIE_DATA	31:0	0x0	Indirect aperture data

PCIE Indirect Register Aperture Data Register

2.4 VIP/I2C Registers

2.4.1 I2C Registers

GEN_INT_CNTL - RW - 32 bits - VIPDEC:0x100			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH0_INT_EN	12	0x0	VIP host port channel 0 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH1_INT_EN	13	0x0	VIP host port channel 1 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH2_INT_EN	14	0x0	VIP host port channel 2 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH3_INT_EN	15	0x0	VIP host port channel 3 DMA interrupt mask. 0=Disable 1=Enable
I2C_INT_EN	17	0x0	I2C interrupt mask. 0=Disable 1=Enable
Reserved	20	0x0	
VIPH_INT_EN	24	0x0	VIP host port interrupt mask. 0=Disable 1=Enable

General Interrupt Control register.
The MASK/EN fields control whether the respective status bits are enabled to drive the system interrupt pin. Even if enabled here, the interrupt line is not driven unless enabled in the PCI configuration space.

GEN_INT_STATUS - RW - 32 bits - VIPDEC:0x104			
Field Name	**Bits**	**Default**	**Description**
CAP0_INT_ACTIVE (R)	8	0x0	Capture port 0 has active interrupt(s). 0=Capture port 0 not source of any active interrupt 1=Capture port 0 has active interrupt(s)
DMA_VIPH0_INT (R)	12	0x0	VIP host port channel 0 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH0_INT_AK (W)	12	0x0	VIP host port channel 0 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH1_INT (R)	13	0x0	VIP host port channel 1 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH1_INT_AK (W)	13	0x0	VIP host port channel 1 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH2_INT (R)	14	0x0	VIP host port channel 2 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH2_INT_AK (W)	14	0x0	VIP host port channel 2 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH3_INT (R)	15	0x0	VIP host port channel 3 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH3_INT_AK (W)	15	0x0	VIP host port channel 3 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status

I2C_INT (R)	17	0x0	I2C interrupt. 0=No event 1=Event has occurred, interrupting if enabled
I2C_INT_AK (W)	17	0x0	I2C interrupt acknowledge/reset. 0=No effect 1=Clear status
Reserved	20	0x0	
VIPH_INT (R)	24	0x0	VIP host port interrupt. 0=No event 1=Event has occurred, interrupting if enabled

General Interrupt Status register.
These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN_INT_CNTL register.

I2C_CNTL_0 - RW - 32 bits - VIPDEC:0x90			
Field Name	**Bits**	**Default**	**Description**
I2C_DONE	0	0x0	Read only. Indicate whether current I2C request is finished or not 0=I2c is busy 1=transfer is complete
I2C_NACK	1	0x0	Read only. Status bit indicate whether I2C slave did not acknowledge. 1=Slave did not issue acknowledge
I2C_HALT	2	0x0	Read only. Status bit indicate where I2C bus transfer is time out. 1=Time-out condition, transfer is halted
I2C_SOFT_RST	5	0x0	Software reset I2C interface block 0=Normal 1=Resets i2c controller
I2C_DRIVE_EN	6	0x0	Enable I2C pad driving pull-up action 0=Pullup by external resistor 1=I2C pads drive SDA
I2C_DRIVE_SEL	7	0x0	If DRIVE_EN is HIGH, select drive time 0=Drive for 10MCLKs 1=20MCLKS
I2C_START	8	0x0	Indicate whether use the start condition in I2C protocol. 0=No start 1=Start
I2C_STOP	9	0x0	Indicate whether use the stop condition in I2C protocol. 0=No stop 1=Stop
I2C_RECEIVE	10	0x0	Master receive/transmit mode selection 0=Send 1=Receive
I2C_ABORT	11	0x0	If 1, abort the current I2C operation by sending STOP bit. 0=No abort 1=Abort
I2C_GO	12	0x0	Write this bit initiate I2C operation. Read this bit indicate the I2C operation is finished or not.
I2C_PRESCALE	31:16	0x0	I2C clock divider to generate I2C SCL output. It also indirectly control the sampling rate.

I2C control registers

I2C_CNTL_1 - RW - 32 bits - VIPDEC:0x94			
Field Name	**Bits**	**Default**	**Description**
I2C_DATA_COUNT	3:0	0x0	Byte count for data to be transferred through I2C interface. The data should be in the 16 bytes I2C buffer
I2C_ADDR_COUNT	6:4	0x0	Byte count for I2C addresses. Maximum 3 bytes of address can be transferred.
I2C_INTRA_BYTE_DELAY	15:8	0x0	Number of SCLK cycles inserted between bytes.
I2C_SEL	16	0x0	Not used in Rage5 0=Pullup by external resistor 1=I2C pads drive SCL
I2C_EN	17	0x0	Enable I2C
I2C_TIME_LIMIT	31:24	0x0	Time out limit. Total wait time = TIME_LIMIT * 4 * PRESCLAE(15:8) cycles for SCL to be LOW

I2C control registers

I2C_DATA - RW - 32 bits - VIPDEC:0x98			
Field Name	**Bits**	**Default**	**Description**
I2C_DATA	7:0	0x0	I2C data interface. Programmers use this 8bits interface to write and read I2C bus data.

I2C data registers. Programmers use this 8bits interface to write and read I2C bus data.

2.4.2 Video Interface Port Host Port Registers

GEN_INT_CNTL - RW - 32 bits - VIPDEC:0x100			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH0_INT_EN	12	0x0	VIP host port channel 0 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH1_INT_EN	13	0x0	VIP host port channel 1 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH2_INT_EN	14	0x0	VIP host port channel 2 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH3_INT_EN	15	0x0	VIP host port channel 3 DMA interrupt mask. 0=Disable 1=Enable
I2C_INT_EN	17	0x0	I2C interrupt mask. 0=Disable 1=Enable
Reserved	20	0x0	
VIPH_INT_EN	24	0x0	VIP host port interrupt mask. 0=Disable 1=Enable

General Interrupt Control register.
The MASK/EN fields control whether the respective status bits are enabled to drive the system interrupt pin. Even if enabled here, the interrupt line is not driven unless enabled in the PCI configuration space.

GEN_INT_STATUS - RW - 32 bits - VIPDEC:0x104			
Field Name	**Bits**	**Default**	**Description**
CAP0_INT_ACTIVE (R)	8	0x0	Capture port 0 has active interrupt(s). 0=Capture port 0 not source of any active interrupt 1=Capture port 0 has active interrupt(s)
DMA_VIPH0_INT (R)	12	0x0	VIP host port channel 0 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH0_INT_AK (W)	12	0x0	VIP host port channel 0 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH1_INT (R)	13	0x0	VIP host port channel 1 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH1_INT_AK (W)	13	0x0	VIP host port channel 1 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH2_INT (R)	14	0x0	VIP host port channel 2 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH2_INT_AK (W)	14	0x0	VIP host port channel 2 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH3_INT (R)	15	0x0	VIP host port channel 3 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH3_INT_AK (W)	15	0x0	VIP host port channel 3 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status

I2C_INT (R)	17	0x0	I2C interrupt. 0=No event 1=Event has occurred, interrupting if enabled
I2C_INT_AK (W)	17	0x0	I2C interrupt acknowledge/reset. 0=No effect 1=Clear status
Reserved	20	0x0	
VIPH_INT (R)	24	0x0	VIP host port interrupt. 0=No event 1=Event has occurred, interrupting if enabled

General Interrupt Status register.
These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN_INT_CNTL register.

VIPH_CH0_DATA - RW - 32 bits - VIPDEC:0xC00			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH0_DT	31:0	0x0	VIPH0 data interface

VIPH0 data interface

VIPH_CH1_DATA - RW - 32 bits - VIPDEC:0xC04			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH1_DT	31:0	0x0	VIPH0 data interface

VIPH0 data interface

VIPH_CH2_DATA - RW - 32 bits - VIPDEC:0xC08			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH2_DT	31:0	0x0	VIPH0 data interface

VIPH0 data interface

VIPH_CH3_DATA - RW - 32 bits - VIPDEC:0xC0C			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH3_DT	31:0	0x0	VIPH0 data interface

VIPH0 data interface

VIPH_CH0_ADDR - RW - 32 bits - VIPDEC:0xC10			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH0_AD	7:0	0x0	Bit(3:0): FIFO address Bit(4): 0= register access, 1 = FIFO access. Bit(5): 0= register write, 1= register read. Bits(7:6): Slave device ID.

VIPH0 command + address.

VIPH_CH1_ADDR - RW - 32 bits - VIPDEC:0xC14			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH1_AD	7:0	0x0	Bit(3:0): FIFO address Bit(4): 0= register access, 1 = FIFO access. Bit(5): 0= register write, 1= register read. Bits(7:6): Slave device ID.

VIPH1 command + address.

VIPH_CH2_ADDR - RW - 32 bits - VIPDEC:0xC18			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH2_AD	7:0	0x0	Bit(3:0): FIFO address Bit(4): 0= register access, 1 = FIFO access. Bit(5): 0= register write, 1= register read. Bits(7:6): Slave device ID.

VIPH2 command + address.

VIPH_CH3_ADDR - RW - 32 bits - VIPDEC:0xC1C			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH3_AD	7:0	0x0	Bit(3:0): FIFO address Bit(4): 0= register access, 1 = FIFO access. Bit(5): 0= register write, 1= register read. Bits(7:6): Slave device ID.

VIPH3 command + address.

VIPH_CH0_SBCNT - RW - 32 bits - VIPDEC:0xC20			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH0_SCNT	19:0	0x0	Write non-zero byte count will trigger DMA. Maximum 2 jobs can be loaded into the queue any one time.

Byte count of transfer requested.

VIPH_CH1_SBCNT - RW - 32 bits - VIPDEC:0xC24			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH1_SCNT	19:0	0x0	Write non-zero byte count will trigger DMA. Maximum 2 jobs can be loaded into the queue any one time.

Byte count of transfer requested.

VIPH_CH2_SBCNT - RW - 32 bits - VIPDEC:0xC28			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH2_SCNT	19:0	0x0	Write non-zero byte count will trigger DMA. Maximum 2 jobs can be loaded into the queue any one time.

Byte count of transfer requested.

VIPH_CH3_SBCNT - RW - 32 bits - VIPDEC:0xC2C

Field Name	Bits	Default	Description
VIPH_CH3_SCNT	19:0	0x0	Write non-zero byte count will trigger DMA. Maximum 2 jobs can be loaded into the queue any one time.

Byte count of transfer requested.

VIPH_CH0_ABCNT - RW - 32 bits - VIPDEC:0xC30			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH0_ACNT (R)	19:0	0x0	Keep track of active byte-count remaining.

Read back of remaining byte count.

VIPH_CH1_ABCNT - RW - 32 bits - VIPDEC:0xC34			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH1_ACNT (R)	19:0	0x0	Keep track of active byte-count remaining.

Read back of remaining byte count.

VIPH_CH2_ABCNT - RW - 32 bits - VIPDEC:0xC38			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH2_ACNT (R)	19:0	0x0	Keep track of active byte-count remaining.

Read back of remaining byte count.

VIPH_CH3_ABCNT - RW - 32 bits - VIPDEC:0xC3C			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH3_ACNT (R)	19:0	0x0	Keep track of active byte-count remaining.

Read back of remaining byte count.

VIPH_CONTROL - RW - 32 bits - VIPDEC:0xC40			
Field Name	**Bits**	**Default**	**Description**
VIPH_CLK_SEL	7:0	0x0	VIPH clock select, only even divider is permitted. Which means VIPH_CLK_SEL(0) must be set to 1. 0=reserved 1=reserved 2=reserved 3=xclkby4 4=reserved 5=xclkby6 6=... (Only EVEN divider is permitted
VIPH_REG_RDY (R)	13	0x0	0= VIPH is ready for next register access. 1= VIPH is busy for current VIPH register access.
VIPH_MAX_WAIT	19:16	0x0	Number of VIP phases before issuing time out. Set to zero means no time out
VIPH_DMA_MODE	20	0x0	0= No DMA. 1= DMA
VIPH_EN	21	0x0	VIP Host port Enable
VIPH_DV0_WID	24	0x0	VIPH0 bus width 0=2-bit vipbus 1=4-bit vipbus

VIPH_DV1_WID	25	0x0	VIPH1 bus width 0=2-bit vipbus 1=4-bit vipbus
VIPH_DV2_WID	26	0x0	VIPH2 bus width 0=2-bit vipbus 1=4-bit vipbus
VIPH_DV3_WID	27	0x0	VIPH3 bus width 0=2-bit vipbus 1=4-bit vipbus
VIPH_PWR_DOWN (R)	28	0x0	'1' to wake up PCICLK. 0=Normal 1=STARTUP PCICLK
VIPH_PWR_DOWN_AK (W)	28	0x0	Clear PWR_DOWN by writing a 1. In order to support PCICLK power down mode, it is important to clear this bit every time there is an interrupt from any part of VIP 0=Normal 1=Allow the host bus to go back to power down state
VIPH_VIPCLK_DIS	29	0x0	'0' will supply VIP clock to slave. '1' will stops VIP clock to save power. 0= 1=turn off VIPCLK for power saving

VIP Host Port Control

VIPH_DV_LAT - RW - 32 bits - VIPDEC:0xC44			
Field Name	**Bits**	**Default**	**Description**
VIPH_TIME_UNIT	11:0	0x0	Basic time slice
VIPH_DV0_LAT	19:16	0x0	How many time slice port 0 gets
VIPH_DV1_LAT	23:20	0x0	How many time slice port 1 gets
VIPH_DV2_LAT	27:24	0x0	How many time slice port 2 gets
VIPH_DV3_LAT	31:28	0x0	How many time slice port 3 gets

Time slice partition

VIPH_DMA_CHUNK - RW - 32 bits - VIPDEC:0xC48			
Field Name	**Bits**	**Default**	**Description**
VIPH_CH0_CHUNK	3:0	0x0	Chunk size between VIP host port and DMA for port 0
VIPH_CH1_CHUNK	5:4	0x0	Chunk size between VIP host port and DMA for port 1
VIPH_CH2_CHUNK	7:6	0x0	Chunk size between VIP host port and DMA for port 2
VIPH_CH3_CHUNK	9:8	0x0	Chunk size between VIP host port and DMA for port 3
VIPH_CH0_ABORT	16	0x0	Abort DMA operation through port 0
VIPH_CH1_ABORT	17	0x0	Abort DMA operation through port 1
VIPH_CH2_ABORT	18	0x0	Abort DMA operation through port 2
VIPH_CH3_ABORT	19	0x0	Abort DMA operation through port 3

DMA transfer chunk size and abort control

VIPH_DV_INT - RW - 32 bits - VIPDEC:0xC4C			
Field Name	**Bits**	**Default**	**Description**
VIPH_DV0_INT_EN	0	0x0	Interrupt polling enable for VIP slave device 0
VIPH_DV1_INT_EN	1	0x0	Interrupt polling enable for VIP slave device 1
VIPH_DV2_INT_EN	2	0x0	Interrupt polling enable for VIP slave device 2
VIPH_DV3_INT_EN	3	0x0	Interrupt polling enable for VIP slave device 3
VIPH_DV0_INT (R)	4	0x0	Interrupt
VIPH_DV0_AK (W)	4	0x0	Clear interrupt with a '1'
VIPH_DV1_INT (R)	5	0x0	Interrupt
VIPH_DV1_AK (W)	5	0x0	Clear interrupt with a '1'
VIPH_DV2_INT (R)	6	0x0	Interrupt
VIPH_DV2_AK (W)	6	0x0	Clear interrupt with a '1'
VIPH_DV3_INT (R)	7	0x0	Interrupt
VIPH_DV3_AK (W)	7	0x0	Clear interrupt with a '1'

VIP Host port interrupt control

VIPH_TIMEOUT_STAT - RW - 32 bits - VIPDEC:0xC50			
Field Name	**Bits**	**Default**	**Description**
VIPH_FIFO0_STAT (R)	0	0x0	'1' if port 0 time out or hung.
VIPH_FIFO0_AK (W)	0	0x0	Clear FIFO0_STAT with a '1'
VIPH_FIFO1_STAT (R)	1	0x0	'1' if port 1 time out or hung.
VIPH_FIFO1_AK (W)	1	0x0	Clear FIFO1_STAT with a '1'
VIPH_FIFO2_STAT (R)	2	0x0	'1' if port 2 time out or hung.
VIPH_FIFO2_AK (W)	2	0x0	Clear FIFO2_STAT with a '1'
VIPH_FIFO3_STAT (R)	3	0x0	'1' if port 3 time out or hung.
VIPH_FIFO3_AK (W)	3	0x0	Clear FIFO3_STAT with a '1'
VIPH_REG_STAT (R)	4	0x0	'1' if register port time out or hung.
VIPH_REG_AK (W)	4	0x0	Clear REG_STAT with a '1'
VIPH_AUTO_INT_STAT (R)	5	0x0	'1' if auto interrupt polling time out or hung.
VIPH_AUTO_INT_AK (W)	5	0x0	Clear AUTO_INT_STAT with a '1'
VIPH_FIFO0_MASK	8	0x0	'0' disable interrupt.
VIPH_FIFO1_MASK	9	0x0	'0' disable interrupt.
VIPH_FIFO2_MASK	10	0x0	'0' disable interrupt.
VIPH_FIFO3_MASK	11	0x0	'0' disable interrupt.
VIPH_REG_MASK	12	0x0	'0' disable interrupt.
VIPH_AUTO_INT_MASK	13	0x0	'0' disable interrupt.
VIPH_DV0_INT_MASK	16	0x0	'0' disable interrupt.
VIPH_DV1_INT_MASK	17	0x0	'0' disable interrupt.
VIPH_DV2_INT_MASK	18	0x0	'0' disable interrupt.
VIPH_DV3_INT_MASK	19	0x0	'0' disable interrupt.
VIPH_INTPIN_EN	20	0x0	'0' means no physical pins used for VIP interrupt. 1= physical pins used.
VIPH_INTPIN_INT (R)	21	0x0	'1' if physical pins has interrupt.
VIPH_REGR_DIS	24	0x0	'0'= any host read from VIPH_REG_DATA will trigger VIP register cycle. 1= Read from VIPH_REG_DATA will not trigger VIP register cycle.

VIP Host Port Time Out Status

VIPH_REG_ADDR - RW - 32 bits - VIPDEC:0x80			
Field Name	**Bits**	**Default**	**Description**
VIPH_REG_AD	15:0	0x0	Bits (11:0): Slave registers address. Bits(12): 0 = register access, 1= FIFO access. Bits(13): 0= register write, 1 = register read. Bits(15:14): Slave device ID.

VIP Host register access command and address.

VIPH_REG_DATA - RW - 32 bits - VIPDEC:0x84			
Field Name	**Bits**	**Default**	**Description**
VIPH_REG_DT_R (R)	31:0	0x0	Read from VIP Host Port register data port
VIPH_REG_DT_W (W)	31:0	0x0	Write to VIP Host Port register data port

VIP Host Port register data port

2.4.3 Capture Registers

Registers to facilitate the capture of input video data

FCP_CNTL - RW - 32 bits - VIPDEC:0x910			
Field Name	**Bits**	**Default**	**Description**
FCP0_SRC_SEL	2:0	0x4	PCICLK,PCLK, PCLKb, HREF, GND, HREFb. 0=PCICLK 1=PCLK 2=PCLKb 3=HREF 4=GND 5=HREFb

Capture Port FCP clock mux control

GEN_INT_STATUS - RW - 32 bits - VIPDEC:0x104			
Field Name	**Bits**	**Default**	**Description**
CAP0_INT_ACTIVE (R)	8	0x0	Capture port 0 has active interrupt(s). 0=Capture port 0 not source of any active interrupt 1=Capture port 0 has active interrupt(s)
DMA_VIPH0_INT (R)	12	0x0	VIP host port channel 0 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH0_INT_AK (W)	12	0x0	VIP host port channel 0 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH1_INT (R)	13	0x0	VIP host port channel 1 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH1_INT_AK (W)	13	0x0	VIP host port channel 1 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH2_INT (R)	14	0x0	VIP host port channel 2 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH2_INT_AK (W)	14	0x0	VIP host port channel 2 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH3_INT (R)	15	0x0	VIP host port channel 3 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH3_INT_AK (W)	15	0x0	VIP host port channel 3 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
I2C_INT (R)	17	0x0	I2C interrupt. 0=No event 1=Event has occurred, interrupting if enabled
I2C_INT_AK (W)	17	0x0	I2C interrupt acknowledge/reset. 0=No effect 1=Clear status
Reserved	20	0x0	
VIPH_INT (R)	24	0x0	VIP host port interrupt. 0=No event 1=Event has occurred, interrupting if enabled

General Interrupt Status register.
These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN_INT_CNTL register.

CAP0_BUF0_OFFSET - RW - 32 bits - VIPDEC:0x920			
Field Name	**Bits**	**Default**	**Description**
CAP_BUF0_OFFSET	31:0	0x0	Capture Port 0 Buffer 0 starting address NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture Port 0 Buffer 0 starting address

CAP0_BUF1_OFFSET - RW - 32 bits - VIPDEC:0x924			
Field Name	**Bits**	**Default**	**Description**
CAP_BUF1_OFFSET	31:0	0x0	Capture Port 0 Buffer 1 starting address NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture Port 0 Buffer 1 starting address

CAP0_BUF0_EVEN_OFFSET - RW - 32 bits - VIPDEC:0x928			
Field Name	**Bits**	**Default**	**Description**
CAP_BUF0_EVEN_OFFSET	31:0	0x0	Capture Port 0 Buffer 0 even frame starting address NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture Port 0 Buffer 0 even frame starting address

CAP0_BUF1_EVEN_OFFSET - RW - 32 bits - VIPDEC:0x92C			
Field Name	**Bits**	**Default**	**Description**
CAP_BUF1_EVEN_OFFSET	31:0	0x0	Capture Port 0 Buffer 1 even frame starting address NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture Port 0 Buffer 1 even frame starting address

CAP0_BUF_PITCH - RW - 32 bits - VIPDEC:0x930			
Field Name	**Bits**	**Default**	**Description**
CAP_BUF_PITCH	11:0	0x0	Capture 0 buffer's pitch. NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 buffer's pitch.

CAP0_V_WINDOW - RW - 32 bits - VIPDEC:0x934			
Field Name	**Bits**	**Default**	**Description**
CAP_V_START	11:0	0x0	Vertical window starting line number.
CAP_V_END	27:16	0x0	Vertical window end line number.

Capture 0's Vertical window.

CAP0_H_WINDOW - RW - 32 bits - VIPDEC:0x938			
Field Name	**Bits**	**Default**	**Description**
CAP_H_START	11:0	0x0	Horizontal window's start.
CAP_H_WIDTH	27:16	0x0	Horizontal window's width. NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0's Horizontal window.

CAP0_VBI0_OFFSET - RW - 32 bits - VIPDEC:0x93C			
Field Name	**Bits**	**Default**	**Description**
CAP_VBI0_OFFSET	31:0	0x0	Capture 0 VBI 0 buffer's starting address. NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 VBI 0 buffer's starting address.

CAP0_VBI1_OFFSET - RW - 32 bits - VIPDEC:0x940			
Field Name	**Bits**	**Default**	**Description**
CAP_VBI1_OFFSET	31:0	0x0	Capture 0 VBI 1 buffer's starting address. NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 VBI 1 buffer's starting address.

CAP0_VBI_V_WINDOW - RW - 32 bits - VIPDEC:0x944			
Field Name	**Bits**	**Default**	**Description**
CAP_VBI_V_START	11:0	0x0	Capture 0 VBI's Vertical start.
CAP_VBI_V_END	27:16	0x0	Capture 0 VBI's Vertical End.

Capture 0 VBI's vertical window

CAP0_VBI_H_WINDOW - RW - 32 bits - VIPDEC:0x948			
Field Name	**Bits**	**Default**	**Description**
CAP_VBI_H_START	11:0	0x0	Capture 0 VBI's Horizontal start.
CAP_VBI_H_WIDTH	27:16	0x0	Capture 0 VBI's Horizontal Width. NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 VBI's horizontal window

CAP0_PORT_MODE_CNTL - RW - 32 bits - VIPDEC:0x94C

Field Name	Bits	Default	Description
CAP_PORT_WIDTH	1	0x0	Capture 0 port width. 0=8 bits 1=16 bits
CAP_PORT_BYTE_USED	2	0x0	In 8 bit width mode, which byte used. 0=lower byte used 1=upper byte used

Capture 0 mode control register.

CAP0_TRIG_CNTL - RW - 32 bits - VIPDEC:0x950			
Field Name	**Bits**	**Default**	**Description**
CAP_TRIGGER_R (R)	1:0	0x0	Read only. Capture status. 0=capture complete 1=capture pending 2=capture in progress
CAP_TRIGGER_W (W)	0	0x0	Write only. Start capture next frame. 0=no action 1=capture next field/frame
CAP_EN	4	0x0	Capture 0 enable. 0=disable 1=enable
CAP_VSYNC_CNT (R)	15:8	0x0	Read only. VSYNC counter.
CAP_VSYNC_CLR	16	0x0	Reset the VSYNC counter.

Capture 0 trigger control.

CAP0_DEBUG - RW - 32 bits - VIPDEC:0x954			
Field Name	**Bits**	**Default**	**Description**
CAP_H_STATUS (R)	11:0	0x0	Capture 0 Horizontal status.
CAP_V_STATUS (R)	27:16	0x0	Capture 0 vertical status.
CAP_V_SYNC (R)	28	0x0	Capture 0 VSYNC status.

Capture 0 debug status register.

CAP0_CONFIG - RW - 32 bits - VIPDEC:0x958			
Field Name	**Bits**	**Default**	**Description**
CAP_INPUT_MODE	0	0x0	Input mode. 0=OneShot trigger mode 1=Enable continuous capture
CAP_START_FIELD	1	0x0	Starting field. 0=Odd 1=Even
CAP_START_BUF_R (R)	2	0x0	Read only. Current starting buffer. 0=Buffer 0 1=Buffer 1
CAP_START_BUF_W (W)	3	0x0	Write only. Control starting buffer. 0=Buffer 0 1=Buffer 1
CAP_BUF_TYPE	5:4	0x0	Buffer type. 0=Field 1=Alternating 2=Frame
CAP_ONESHOT_MODE	6	0x0	ONESHOT mode. 0=FIELD 1=FRAME

CAP_BUF_MODE	8:7	0x0	Capture 0 buffer mode. 0=Single 1=Double 2=Triple
CAP_MIRROR_EN	9	0x0	Capture 0 mirroring function enable. 0=Normal 1=Mirror
CAP_ONESHOT_MIRROR_EN	10	0x0	ONESHOT buffer mirroring function enable. 0=Normal 1=Mirror
CAP_VIDEO_SIGNED_UV	11	0x0	Enable conversion to signed value. 1=Convert to signed
CAP_ANC_DECODE_EN	12	0x0	ANC enable. 0=disable 1=enable
CAP_VBI_EN	13	0x0	VBI enable. 0=disable 1=enable
CAP_SOFT_PULL_DOWN_EN	14	0x0	Software pull down enable. 0=disable 1=enable
CAP_VIP_EXTEND_FLAG_EN	15	0x0	Extended flag enable. 0=DISABLE 1=ENABLE
CAP_FAKE_FIELD_EN	16	0x1	Fake field enable. 0=DISABLE 1=ENABLE
CAP_FIELD_START_LINE_DIFF	18:17	0x0	Odd, Even frame line number differences. 0=EQUAL 1=ODD_ONE_MORE_LINE 2=EVEN_ONE_MORE_LINE
CAP_HORZ_DOWN	20:19	0x0	Horizontal decimation. 0=Normal 1=x2 2=x4
CAP_VERT_DOWN	22:21	0x0	Vertical decimation. 0=Normal 1=x2 2=x4
CAP_STREAM_FORMAT	25:23	0x0	Video stream format. 0=Brooktree 1=CCIR 656 2=ZV 3=16bit VIP 4=TRANSPORT STREAM
CAP_HDWNS_DEC	26	0x1	Horizontal downscaler or decimator. 0=downscaler 1=decimator
CAP_IMAGE_FLIP_EN	27	0x0	0=Normal 1=Flip
CAP_ONESHOT_IMAGE_FLIP_EN	28	0x0	0=Normal 1=Flip
CAP_VIDEO_IN_FORMAT	29	0x0	Input format. 0=YVYU422 1=VYUY422
VBI_HORZ_DOWN	31:30	0x0	0=Normal 1=x2 2=x4

Capture 0 configuration register.

CAP0_ANC0_OFFSET - RW - 32 bits - VIPDEC:0x95C

Field Name	Bits	Default	Description
CAP_ANC0_OFFSET	31:0	0x0	Starting address NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 ANC 0 starting address.

CAP0_ANC1_OFFSET - RW - 32 bits - VIPDEC:0x960			
Field Name	**Bits**	**Default**	**Description**
CAP_ANC1_OFFSET	31:0	0x0	Starting address NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 ANC 1 starting address.

CAP0_ANC_H_WINDOW - RW - 32 bits - VIPDEC:0x964			
Field Name	**Bits**	**Default**	**Description**
CAP_ANC_WIDTH	11:0	0x0	Window width. NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 ANC horizontal window.

CAP0_VIDEO_SYNC_TEST - RW - 32 bits - VIPDEC:0x968			
Field Name	**Bits**	**Default**	**Description**
CAP_TEST_VID_SOF	0	0x0	Start of field.
CAP_TEST_VID_EOF	1	0x0	End of field.
CAP_TEST_VID_EOL	2	0x0	End of line.
CAP_TEST_VID_FIELD	3	0x0	Odd/Even field. 0=Even Field 1=Odd Field
CAP_TEST_SYNC_EN	5	0x0	Test sync enable. 0=Normal 1=Test Mode

Capture port 0 sync test.

CAP0_ONESHOT_BUF_OFFSET - RW - 32 bits - VIPDEC:0x96C			
Field Name	**Bits**	**Default**	**Description**
CAP_ONESHOT_BUF_OFFSET	31:0	0x0	ONESHOT buffer starting address. NOTE: Bits 0:1 of this field are hardwired to ZERO.

ONESHOT buffer starting address.

CAP0_BUF_STATUS - RW - 32 bits - VIPDEC:0x970			
Field Name	**Bits**	**Default**	**Description**
CAP_PRE_VID_BUF (R)	1:0	0x0	Read only. Previous capture buffer.
CAP_CUR_VID_BUF (R)	3:2	0x0	Read only. Current Capture buffer.
CAP_PRE_FIELD (R)	4	0x0	Read only. Previous field.
CAP_CUR_FIELD (R)	5	0x0	Read only. Current field.

CAP_PRE_VBI_BUF (R)	7:6	0x0	Read only. Previous VBI buffer.
CAP_CUR_VBI_BUF (R)	9:8	0x0	Read only. Current VBI buffer.
CAP_VBI_BUF_STATUS (R)	10	0x0	Read only. VBI busy status. 0=done 1=busy
CAP_PRE_ANC_BUF (R)	12:11	0x0	Read only. Previous ANC buffer.
CAP_CUR_ANC_BUF (R)	14:13	0x0	Read only. Current ANC buffer.
CAP_ANC_BUF_STATUS (R)	15	0x0	Read only. Buffer busy status. 0=done 1=busy
CAP_ANC_PRE_BUF_CNT (R)	27:16	0x0	Read only. Buffer count.
CAP_VIP_INC (R)	28	0x0	Read only. Interlaced or not. 0=INTERLACED 1=NON_INTERLACED
CAP_VIP_PRE_REPEAT_FIELD (R)	29	0x0	Read only. Previous buffer is new/repeat field. 0=new_field 1=repeated_field
CAP_CAP_BUF_STATUS (R)	30	0x0	Read only. Capture buffer busy status. 0=done 1=busy

Capture 0 buffer status.

CAP0_VBI2_OFFSET - RW - 32 bits - VIPDEC:0x980			
Field Name	**Bits**	**Default**	**Description**
CAP_VBI2_OFFSET	31:0	0x0	Capture 0 VBI 2 buffer's starting address. NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 VBI 2 buffer's starting address.

CAP0_VBI3_OFFSET - RW - 32 bits - VIPDEC:0x984			
Field Name	**Bits**	**Default**	**Description**
CAP_VBI3_OFFSET	31:0	0x0	Capture 0 VBI 3 buffer's starting address. NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 VBI 3 buffer's starting address.

CAP0_ANC2_OFFSET - RW - 32 bits - VIPDEC:0x988			
Field Name	**Bits**	**Default**	**Description**
CAP_ANC2_OFFSET	31:0	0x0	Starting address NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 ANC 2 starting address.

CAP0_ANC3_OFFSET - RW - 32 bits - VIPDEC:0x98C			
Field Name	**Bits**	**Default**	**Description**
CAP_ANC3_OFFSET	31:0	0x0	Starting address NOTE: Bits 0:1 of this field are hardwired to ZERO.

Capture 0 ANC 3 starting address.

VID_BUFFER_CONTROL - RW - 32 bits - VIPDEC:0x900			
Field Name	**Bits**	**Default**	**Description**
CAP0_BUFFER_WATER_MARK	5:0	0x10	Capture 0 buffer water mark.
FULL_BUFFER_EN	16	0x0	1= The shared buffer is dedicated to one capture only. 0=DISABLE 1=ENABLE
CAP0_ANC_VBI_QUAD_BUF	17	0x0	0=Dual buffer 1=Quaduple buffer
VID_BUFFER_RESET	20	0x0	Reset the buffer pointers. 0=NOT RESET 1=RESET
CAP_SWAP	22:21	0x0	Capture Port Swap control.
CAP0_BUFFER_EMPTY (R)	24	0x0	Capture 0's buffer empty status. 0=EMPTY 1=NOT EMPTY

Video Capture port buffer control.

CAP_INT_CNTL - RW - 32 bits - VIPDEC:0x908			
Field Name	**Bits**	**Default**	**Description**
CAP0_BUF0_INT_EN	0	0x0	Capture 0 Buffer 0 Interrupt enable. 0=Disable 1=Enable
CAP0_BUF0_EVEN_INT_EN	1	0x0	Capture 0 Buffer 0 even frame Interrupt enable. 0=Disable 1=Enable
CAP0_BUF1_INT_EN	2	0x0	Capture 0 Buffer 1 Interrupt enable. 0=Disable 1=Enable
CAP0_BUF1_EVEN_INT_EN	3	0x0	Capture 0 Buffer 1 even frame Interrupt enable. 0=Disable 1=Enable
CAP0_VBI0_INT_EN	4	0x0	Capture 0 VBI Buffer 0 Interrupt enable. 0=Disable 1=Enable
CAP0_VBI1_INT_EN	5	0x0	Capture 0 VBI Buffer 1 Interrupt enable. 0=Disable 1=Enable
CAP0_ONESHOT_INT_EN	6	0x0	Capture 0 ONESHOT Buffer Interrupt enable. 0=Disable 1=Enable
CAP0_ANC0_INT_EN	7	0x0	Capture 0 ANC Buffer 0 Interrupt enable. 0=Disable 1=Enable
CAP0_ANC1_INT_EN	8	0x0	Capture 0 ANC Buffer 1 Interrupt enable. 0=Disable 1=Enable
CAP0_VBI2_INT_EN	9	0x0	Capture 0 VBI Buffer 2 Interrupt enable. 0=Disable 1=Enable
CAP0_VBI3_INT_EN	10	0x0	Capture 0 VBI Buffer 3 Interrupt enable. 0=Disable 1=Enable
CAP0_ANC2_INT_EN	11	0x0	Capture 0 ANC Buffer 2 Interrupt enable. 0=Disable 1=Enable
CAP0_ANC3_INT_EN	12	0x0	Capture 0 ANC Buffer 3 Interrupt enable. 0=Disable 1=Enable

Video Capture port interrupt control register

CAP_INT_STATUS - RW - 32 bits - VIPDEC:0x90C			
Field Name	**Bits**	**Default**	**Description**
CAP0_BUF0_INT (R)	0	0x0	Read only. Buffer 0 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_BUF0_INT_AK (W)	0	0x0	Buf0 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_BUF0_EVEN_INT (R)	1	0x0	Read only. Buffer 0 even frame interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_BUF0_EVEN_INT_AK (W)	1	0x0	Buf0 even frame buffer interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_BUF1_INT (R)	2	0x0	Read only. Buffer 1 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_BUF1_INT_AK (W)	2	0x0	Buf1 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_BUF1_EVEN_INT (R)	3	0x0	Read only. Buffer 1 even frame interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_BUF1_EVEN_INT_AK (W)	3	0x0	Buf1 even frame buffer interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_VBI0_INT (R)	4	0x0	Read only. VBI buffer 0 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_VBI0_INT_AK (W)	4	0x0	VBI buffer 0 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_VBI1_INT (R)	5	0x0	Read only. VBI buffer 1 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_VBI1_INT_AK (W)	5	0x0	VBI buffer 1 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_ONESHOT_INT (R)	6	0x0	Read only. ONESHOT buffer interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_ONESHOT_INT_AK (W)	6	0x0	ONESHOT buffer interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_ANC0_INT (R)	7	0x0	Read only. ANC buffer 0 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_ANC0_INT_AK (W)	7	0x0	ANC buffer 0 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_ANC1_INT (R)	8	0x0	Read only. ANC buffer 1 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_ANC1_INT_AK (W)	8	0x0	ANC buffer 1 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_VBI2_INT (R)	9	0x0	Read only. VBI buffer 2 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled

CAP0_VBI2_INT_AK (W)	9	0x0	VBI buffer 2 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_VBI3_INT (R)	10	0x0	Read only. VBI buffer 3 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_VBI3_INT_AK (W)	10	0x0	VBI buffer 3 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_ANC2_INT (R)	11	0x0	Read only. ANC buffer 2 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_ANC2_INT_AK (W)	11	0x0	ANC buffer 2 interrupt acknowledgment. 0=No effect 1=Clear status
CAP0_ANC3_INT (R)	12	0x0	Read only. ANC buffer 3 interrupt status. 0=No event 1=Event has occurred, interrupting if enabled
CAP0_ANC3_INT_AK (W)	12	0x0	ANC buffer 3 interrupt acknowledgment. 0=No effect 1=Clear status

Capture port interrupt control.

2.4.4 VIP Host Port DMA Registers

GEN_INT_CNTL - RW - 32 bits - VIPDEC:0x100			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH0_INT_EN	12	0x0	VIP host port channel 0 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH1_INT_EN	13	0x0	VIP host port channel 1 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH2_INT_EN	14	0x0	VIP host port channel 2 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH3_INT_EN	15	0x0	VIP host port channel 3 DMA interrupt mask. 0=Disable 1=Enable
I2C_INT_EN	17	0x0	I2C interrupt mask. 0=Disable 1=Enable
Reserved	20	0x0	
VIPH_INT_EN	24	0x0	VIP host port interrupt mask. 0=Disable 1=Enable

General Interrupt Control register.
The MASK/EN fields control whether the respective status bits are enabled to drive the system interrupt pin. Even if enabled here, the interrupt line is not driven unless enabled in the PCI configuration space.

GEN_INT_STATUS - RW - 32 bits - VIPDEC:0x104			
Field Name	**Bits**	**Default**	**Description**
CAP0_INT_ACTIVE (R)	8	0x0	Capture port 0 has active interrupt(s). 0=Capture port 0 not source of any active interrupt 1=Capture port 0 has active interrupt(s)
DMA_VIPH0_INT (R)	12	0x0	VIP host port channel 0 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH0_INT_AK (W)	12	0x0	VIP host port channel 0 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH1_INT (R)	13	0x0	VIP host port channel 1 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH1_INT_AK (W)	13	0x0	VIP host port channel 1 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH2_INT (R)	14	0x0	VIP host port channel 2 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH2_INT_AK (W)	14	0x0	VIP host port channel 2 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH3_INT (R)	15	0x0	VIP host port channel 3 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH3_INT_AK (W)	15	0x0	VIP host port channel 3 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status

I2C_INT (R)	17	0x0	I2C interrupt. 0=No event 1=Event has occurred, interrupting if enabled
I2C_INT_AK (W)	17	0x0	I2C interrupt acknowledge/reset. 0=No effect 1=Clear status
Reserved	20	0x0	
VIPH_INT (R)	24	0x0	VIP host port interrupt. 0=No event 1=Event has occurred, interrupting if enabled

General Interrupt Status register.
These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN_INT_CNTL register.

DMA_VIPH0_COMMAND - R - 32 bits - VIPDEC:0xA00			
Field Name	**Bits**	**Default**	**Description**
BYTE_COUNT	20:0	0x0	Byte Count of transfer size.
SWAP_CONTROL	25:24	0x0	Endian's swap control. 0=No Swapping 1=[15:0] = [31:16], [31:16] = [15:0] 2=[7:0] =[31:24], [15:8] = [23:16], [23:16] = [15:8], [31:24] = [7:0] 3=Undefined
TRANSFER_SOURCE	26	0x0	Address space of source data. 0=Transfer from memory 1=Transfer from VIPH
TRANSFER_DEST	27	0x0	Address space of destination data. 0=Transfer to memory 1=Transfer to VIPH
SOURCE_OFFSET_HOLD	28	0x0	Hold the source address without increase. 0=Increment 1=Hold
DEST_OFFSET_HOLD	29	0x0	Hold the destination address without increase. 0=Increment 1=Hold
INTERRUPT_DIS	30	0x0	End of DMA command table interrupt control. 0=Normal 1=Disable the end of list interrupt
END_OF_LIST_STATUS	31	0x0	Status bit show the last command of the DMA table. 0=Normal 1=End of Descriptor List

VIPH channel0 DMA command read back.

DMA_VIPH1_COMMAND - R - 32 bits - VIPDEC:0xA04			
Field Name	**Bits**	**Default**	**Description**
BYTE_COUNT	20:0	0x0	Byte Count of transfer size.
SWAP_CONTROL	25:24	0x0	Endian's swap control. 0=No Swapping 1=[15:0] = [31:16], [31:16] = [15:0] 2=[7:0] =[31:24], [15:8] = [23:16], [23:16] = [15:8], [31:24] = [7:0] 3=Undefined
TRANSFER_SOURCE	26	0x0	Address space of source data. 0=Transfer from memory 1=Transfer from VIPH
TRANSFER_DEST	27	0x0	Address space of destination data. 0=Transfer to memory 1=Transfer to VIPH

SOURCE_OFFSET_HOLD	28	0x0	Hold the source address without increase. 0=Increment 1=Hold
DEST_OFFSET_HOLD	29	0x0	Hold the destination address without increase. 0=Increment 1=Hold
INTERRUPT_DIS	30	0x0	End of DMA command table interrupt control. 0=Normal 1=Disable the end of list interrupt
END_OF_LIST_STATUS	31	0x0	Status bit show the last command of the DMA table. 0=Normal 1=End of Descriptor List

VIPH channel1 DMA command read back.

DMA_VIPH2_COMMAND - R - 32 bits - VIPDEC:0xA08			
Field Name	**Bits**	**Default**	**Description**
BYTE_COUNT	20:0	0x0	Byte Count of transfer size.
SWAP_CONTROL	25:24	0x0	Endian's swap control. 0=No Swapping 1=[15:0] = [31:16], [31:16] = [15:0] 2=[7:0] =[31:24], [15:8] = [23:16], [23:16] = [15:8], [31:24] = [7:0] 3=Undefined
TRANSFER_SOURCE	26	0x0	Address space of source data. 0=Transfer from memory 1=Transfer from VIPH
TRANSFER_DEST	27	0x0	Address space of destination data. 0=Transfer to memory 1=Transfer to VIPH
SOURCE_OFFSET_HOLD	28	0x0	Hold the source address without increase. 0=Increment 1=Hold
DEST_OFFSET_HOLD	29	0x0	Hold the destination address without increase. 0=Increment 1=Hold
INTERRUPT_DIS	30	0x0	End of DMA command table interrupt control. 0=Normal 1=Disable the end of list interrupt
END_OF_LIST_STATUS	31	0x0	Status bit show the last command of the DMA table. 0=Normal 1=End of Descriptor List

VIPH channel2 DMA command read back.

DMA_VIPH3_COMMAND - R - 32 bits - VIPDEC:0xA0C			
Field Name	**Bits**	**Default**	**Description**
BYTE_COUNT	20:0	0x0	Byte Count of transfer size.
SWAP_CONTROL	25:24	0x0	Endian's swap control. 0=No Swapping 1=[15:0] = [31:16], [31:16] = [15:0] 2=[7:0] =[31:24], [15:8] = [23:16], [23:16] = [15:8], [31:24] = [7:0] 3=Undefined
TRANSFER_SOURCE	26	0x0	Address space of source data. 0=Transfer from memory 1=Transfer from VIPH
TRANSFER_DEST	27	0x0	Address space of destination data. 0=Transfer to memory 1=Transfer to VIPH

SOURCE_OFFSET_HOLD	28	0x0	Hold the source address without increase. 0=Increment 1=Hold
DEST_OFFSET_HOLD	29	0x0	Hold the destination address without increase. 0=Increment 1=Hold
INTERRUPT_DIS	30	0x0	End of DMA command table interrupt control. 0=Normal 1=Disable the end of list interrupt
END_OF_LIST_STATUS	31	0x0	Status bit show the last command of the DMA table. 0=Normal 1=End of Descriptor List

VIPH channel3 DMA command read back.

DMA_VIPH_STATUS - R - 32 bits - VIPDEC:0xA10			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH0_AVAIL	3:0	0x3	VIPH DMA channel 0 available job queue number.
DMA_VIPH1_AVAIL	7:4	0x3	VIPH DMA channel 1 available job queue number.
DMA_VIPH2_AVAIL	11:8	0x3	VIPH DMA channel 2 available job queue number.
DMA_VIPH3_AVAIL	15:12	0x3	VIPH DMA channel 3 available job queue number.
DMA_VIPH0_CURRENT	17:16	0x0	VIPH DMA channel 0 current active job queue number
DMA_VIPH1_CURRENT	19:18	0x0	VIPH DMA channel 1 current active job queue number
DMA_VIPH2_CURRENT	21:20	0x0	VIPH DMA channel 2 current active job queue number
DMA_VIPH3_CURRENT	23:22	0x0	VIPH DMA channel 3 current active job queue number
DMA_VIPH0_ACTIVE	24	0x0	VIPH DMA channel 0 active status. 0=All VIP0 queue transfers are all done 1=A VIP0 queue transfer is active
DMA_VIPH1_ACTIVE	25	0x0	VIPH DMA channel 1 active status. 0=All VIP1 queue transfers are all done 1=A VIP1 queue transfer is active
DMA_VIPH2_ACTIVE	26	0x0	VIPH DMA channel 2 active status. 0=All VIP2 queue transfers are all done 1=A VIP2 queue transfer is active
DMA_VIPH3_ACTIVE	27	0x0	VIPH DMA channel 3 active status. 0=All VIP3 queue transfers are all done 1=A VIP3 queue transfer is active

VIPH DMA channels status register.

DMA_VIPH_CHUNK_0 - RW - 32 bits - VIPDEC:0xA18			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH3_TABLE_SWAP	1:0	0x0	VIPH DMA Channel 3 Endian swap control. 0=No swap 1=8bit swap 2=16bit swap 3=reserved
DMA_VIPH2_TABLE_SWAP	3:2	0x0	VIPH DMA Channel 2 Endian swap control. 0=No swap 1=8bit swap 2=16bit swap 3=reserved
DMA_VIPH1_TABLE_SWAP	5:4	0x0	VIPH DMA Channel 1 Endian swap control. 0=No swap 1=8bit swap 2=16bit swap 3=reserved

DMA_VIPH0_TABLE_SWAP	7:6	0x0	VIPH DMA Channel 0 Endian swap control. 0=No swap 1=8bit swap 2=16bit swap 3=reserved
DMA_VIPH3_NOCHUNK	28	0x0	VIPH DMA Channel 3 disregard chunk size 0=Use chunk value 1=Use infinity for the chunk value
DMA_VIPH2_NOCHUNK	29	0x0	VIPH DMA Channel 2 disregard chunk size 0=Use chunk value 1=Use infinity for the chunk value
DMA_VIPH1_NOCHUNK	30	0x0	VIPH DMA Channel 1 disregard chunk size 0=Use chunk value 1=Use infinity for the chunk value
DMA_VIPH0_NOCHUNK	31	0x0	VIPH DMA Channel 0 disregard chunk size 0=Use chunk value 1=Use infinity for the chunk value

VIP Host Port DMA Chunk control register.

DMA_VIPH_CHUNK_1_VAL - RW - 32 bits - VIPDEC:0xA1C			
Field Name	**Bits**	**Default**	**Description**
DMA_VIP0_CHUNK	7:0	0xf	VIP Host Port DMA channel 0 Chunk size
DMA_VIP1_CHUNK	15:8	0xf	VIP Host Port DMA channel 1 Chunk size
DMA_VIP2_CHUNK	23:16	0xf	VIP Host Port DMA channel 2 Chunk size
DMA_VIP3_CHUNK	31:24	0xf	VIP Host Port DMA channel 3 Chunk size

VIP Host Port DMA Chunk size

DMA_VIP0_TABLE_ADDR - W - 32 bits - VIPDEC:0xA20			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH_TABLE_ADDR	31:0	0x0	This points to first entry in the DMA table.

VIP Port 0 DMA table starting address

DMA_VIP1_TABLE_ADDR - W - 32 bits - VIPDEC:0xA30			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH_TABLE_ADDR	31:0	0x0	This points to first entry in the DMA table.

VIP Port 1 DMA table starting address

DMA_VIP2_TABLE_ADDR - W - 32 bits - VIPDEC:0xA40			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH_TABLE_ADDR	31:0	0x0	This points to first entry in the DMA table.

VIP Port 2 DMA table starting address

DMA_VIP3_TABLE_ADDR - W - 32 bits - VIPDEC:0xA50			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH_TABLE_ADDR	31:0	0x0	This points to first entry in the DMA table.
VIP Port 3 DMA table starting address			

DMA_VIPH0_ACTIVE - R - 32 bits - VIPDEC:0xA24			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH_TABLE_ADDR_ACT	31:0	0x0	This points to the current active entry in the DMA table.
VIP Port 0 DMA Current table address			

DMA_VIPH1_ACTIVE - R - 32 bits - VIPDEC:0xA34			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH_TABLE_ADDR_ACT	31:0	0x0	This points to the current active entry in the DMA table.
VIP Port 1 DMA Current table address			

DMA_VIPH2_ACTIVE - R - 32 bits - VIPDEC:0xA44			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH_TABLE_ADDR_ACT	31:0	0x0	This points to the current active entry in the DMA table.
VIP Port 2 DMA Current table address			

DMA_VIPH3_ACTIVE - R - 32 bits - VIPDEC:0xA54			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH_TABLE_ADDR_ACT	31:0	0x0	This points to the current active entry in the DMA table.
VIP Port 3 DMA Current table address			

DMA_VIPH_ABORT - RW - 32 bits - VIPDEC:0xA88			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH0_ABORT_EN	3	0x0	Enable abort action 0=Normal 1=Enable queue abort
DMA_VIPH1_ABORT_EN	7	0x0	Enable abort action 0=Normal 1=Enable queue abort
DMA_VIPH2_ABORT_EN	11	0x0	Enable abort action 0=Normal 1=Enable queue abort
DMA_VIPH3_ABORT_EN	15	0x0	Enable abort action 0=Normal 1=Enable queue abort
DMA_VIPH0_RESET	20	0x0	Soft reset. Reset the DMA and job queue.
DMA_VIPH1_RESET	21	0x0	Soft reset. Reset the DMA and job queue.
DMA_VIPH2_RESET	22	0x0	Soft reset. Reset the DMA and job queue.
DMA_VIPH3_RESET	23	0x0	Soft reset. Reset the DMA and job queue.

VIP Host Port DMA abort control registers

2.4.5 GPIO Registers

GEN_INT_CNTL - RW - 32 bits - VIPDEC:0x100			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH0_INT_EN	12	0x0	VIP host port channel 0 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH1_INT_EN	13	0x0	VIP host port channel 1 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH2_INT_EN	14	0x0	VIP host port channel 2 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH3_INT_EN	15	0x0	VIP host port channel 3 DMA interrupt mask. 0=Disable 1=Enable
I2C_INT_EN	17	0x0	I2C interrupt mask. 0=Disable 1=Enable
Reserved	20	0x0	
VIPH_INT_EN	24	0x0	VIP host port interrupt mask. 0=Disable 1=Enable

General Interrupt Control register.
The MASK/EN fields control whether the respective status bits are enabled to drive the system interrupt pin. Even if enabled here, the interrupt line is not driven unless enabled in the PCI configuration space.

GEN_INT_STATUS - RW - 32 bits - VIPDEC:0x104			
Field Name	**Bits**	**Default**	**Description**
CAP0_INT_ACTIVE (R)	8	0x0	Capture port 0 has active interrupt(s). 0=Capture port 0 not source of any active interrupt 1=Capture port 0 has active interrupt(s)
DMA_VIPH0_INT (R)	12	0x0	VIP host port channel 0 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH0_INT_AK (W)	12	0x0	VIP host port channel 0 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH1_INT (R)	13	0x0	VIP host port channel 1 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH1_INT_AK (W)	13	0x0	VIP host port channel 1 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH2_INT (R)	14	0x0	VIP host port channel 2 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH2_INT_AK (W)	14	0x0	VIP host port channel 2 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH3_INT (R)	15	0x0	VIP host port channel 3 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH3_INT_AK (W)	15	0x0	VIP host port channel 3 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status

I2C_INT (R)	17	0x0	I2C interrupt. 0=No event 1=Event has occurred, interrupting if enabled
I2C_INT_AK (W)	17	0x0	I2C interrupt acknowledge/reset. 0=No effect 1=Clear status
Reserved	20	0x0	
VIPH_INT (R)	24	0x0	VIP host port interrupt. 0=No event 1=Event has occurred, interrupting if enabled

General Interrupt Status register.
These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN_INT_CNTL register.

DMA_VIPH0_COMMAND - R - 32 bits - VIPDEC:0xA00			
Field Name	**Bits**	**Default**	**Description**
BYTE_COUNT	20:0	0x0	Byte Count of transfer size.
SWAP_CONTROL	25:24	0x0	Endian's swap control. 0=No Swapping 1=[15:0] = [31:16], [31:16] = [15:0] 2=[7:0] =[31:24], [15:8] = [23:16], [23:16] = [15:8], [31:24] = [7:0] 3=Undefined
TRANSFER_SOURCE	26	0x0	Address space of source data. 0=Transfer from memory 1=Transfer from VIPH
TRANSFER_DEST	27	0x0	Address space of destination data. 0=Transfer to memory 1=Transfer to VIPH
SOURCE_OFFSET_HOLD	28	0x0	Hold the source address without increase. 0=Increment 1=Hold
DEST_OFFSET_HOLD	29	0x0	Hold the destination address without increase. 0=Increment 1=Hold
INTERRUPT_DIS	30	0x0	End of DMA command table interrupt control. 0=Normal 1=Disable the end of list interrupt
END_OF_LIST_STATUS	31	0x0	Status bit show the last command of the DMA table. 0=Normal 1=End of Descriptor List

VIPH channel0 DMA command read back.

CONFIG_XSTRAP - RW - 32 bits - VIPDEC:0xE4			
Field Name	**Bits**	**Default**	**Description**
BLANK_ROM (R)	1	0x0	Blank Rom on board.
VIP_DEVICE (R)	2	0x0	Indicates if any slave VIP host devices drove this pin low during reset. 0=No slave VIP host port devices present 1=Slave VIP host port devices present
Reserved	3	0x0	

ROMIDCFG (R)	7:4	0x0	If no ROM attached, controls chip ID's. If ROM attached, identifies ROM type. 000x - No ROM, CHG_ID = 00 001x - No ROM, CHG_ID = 01 010x - No ROM, CHG_ID = 10 011x - No ROM, CHG_ID = 11 1001 - 1M Serial AT25F1024 ROM (Atmel) 1010 - 1M Serial AT45DB011 ROM (Atmel) 1011 - 1M Serial M25P10 ROM (ST) 1100 - 512K Serial M25P05 ROM (ST) 1101 - 1M Serial SST45LF010 ROM (SST) 1M Serial W45B512 ROM (WinBond) 512K Serial W45B012 ROM (WinBond) 1110 - 1M Serial SST25VF010 ROM (SST) 512K Serial SST25VF512 ROM (SST) 1111 - 1M NX25F011B ROM (NexFlash)
HDCP_DISABLE (R)	8	0x0	Disable HDCP.
MV_DISABLE (R)	9	0x0	Disable Macrovision.

Strap read back.

CONFIG_GPIO - RW - 32 bits - VIPDEC:0xE8			
Field Name	**Bits**	**Default**	**Description**
GPIO_0 (R)	0	0x0	Pin read back of GPIO_0.
GPIO_1 (R)	1	0x0	Pin read back of GPIO_1.
GPIO_2 (R)	2	0x0	Pin read back of GPIO_2.
GPIO_3 (R)	3	0x0	Pin read back of GPIO_3.
GPIO_4 (R)	4	0x0	Pin read back of GPIO_4.
GPIO_5 (R)	5	0x0	Pin read back of GPIO_5.
GPIO_6 (R)	6	0x0	Pin read back of GPIO_6.
GPIO_7 (R)	7	0x0	Pin read back of GPIO_7.
GPIO_8 (R)	8	0x0	Pin read back of GPIO_8.
GPIO_9 (R)	9	0x0	Pin read back of GPIO_9.
GPIO_10 (R)	10	0x0	Pin read back of GPIO_10.
GPIO_11 (R)	11	0x0	Pin read back of GPIO_11.
GPIO_12 (R)	12	0x0	Pin read back of GPIO_12.
GPIO_13 (R)	13	0x0	Pin read back of GPIO_13.
GPIO_14 (R)	14	0x0	Pin read back of GPIO_14.
GPIO_15 (R)	15	0x0	Pin read back of GPIO_15.
GPIO_16 (R)	16	0x0	Pin read back of GPIO_16.
GPIO_17 (R)	17	0x0	Pin read back of GPIO_17.

GPIO pin read back.

VIDEOMUX_CNTL - RW - 32 bits - VIPDEC:0x190			
Field Name	**Bits**	**Default**	**Description**
VIPH_INT_SEL	0	0x0	0=If VIP host port interrupt using input instead of polling, then AUX-WIN pin used as interrupt input. 1=If VIP host port interrupt using input instead of polling, then ZV_LCDCNTL(2) pin used as interrupt input.
Reserved	1	0x0	
Reserved	2	0x0	
ROM_CLK_DIVIDE	20:16	0x5	ROM clock divider
STR_ROMCLK	21	0x0	Extend ROM cycle
VIP_INTERNAL_DEBUG_SEL	24:22	0x0	Legacy. Not used.

GPIO pin mux control

SEPROM_CNTL1 - RW - 32 bits - VIPDEC:0x1C0			
Field Name	**Bits**	**Default**	**Description**
WRITE_ENABLE	0	0x0	Set WRITE_ENABLE to be the command field
WRITE_DISABLE	1	0x0	Set WRITE_DISABLE to be the command field
READ_CONFIG	2	0x0	Set READ_CONFIG to be the command field
WRITE_CONFIG	3	0x0	Set WRITE_CONFIG to be the command field
READ_STATUS	4	0x0	Set READ_STATUS to be the command field
SECT_TO_SRAM	5	0x0	Set SECT_TO_SRAM to be the command field
READY_BUSY (R)	7	0x0	Status bit that reflects the status of the HOLD/READY_BUSY bus
SEPROM_BUSY (R)	8	0x0	Status bit that indicates the status of the SPI state machine
BCNT_OVER_WTE_EN	9	0x0	This bit must be set to '1' for burst ROM write/read. This bit works coherently with the BYTE_CNT.
RB_MASKB	10	0x0	RBb mask.
SOFT_RESET	11	0x0	Soft reset
STATE_IDLEb (R)	12	0x0	Indicate whether the ROM controller state machine is idle
SECTOR_ERASE	13	0x0	This bit should be set to 1 when a performing a sector erase.
BYTE_CNT	23:16	0xff	The BYTE_CNT works coherently with the BCNT_OVER_WTE_EN. Programming the BYTE_CNT has no effect if BCNT_OVER_WTE_EN is '0'. The BYTE_CNT can be programmed to tell the SPI state machine how many byte will be sent/read. BYTE_CNT = 0 means 1 byte will be sent ' ' BYTE_CNT = 255 means 256 byte will be sent
SCK_PRESCALE	31:24	0x4	This changes the SCK period with this function: SCK period = (SCK_PRESCALE + 1) * 2 * (SYSTEM CLOCK period)

First SPI Serial ROM Control register

SEPROM_CNTL2 - RW - 32 bits - VIPDEC:0x1C4			
Field Name	**Bits**	**Default**	**Description**
WAIT_CYCLE	7:0	0x5	Number of wait cycles.
AUTO_ADDR_SAMPLE	8	0x1	Overriding the auto-increment for the ROM address.
SEC_COMMAND	23:16	0x0	Use this as the instruction.
SECTOR_TO_ERASE	28:24	0x0	When the SECTOR_ERASE bit is set to 1, this field specifies which sector to erase.
ROM_SCLK_SRC_SEL	30:29	0x3	0=SCLK/3 1=SCLK/2 2=SCLK/1 3=SCLK/1

Second SPI Serial ROM Control register

2.4.6 VIP Miscellaneous Registers

GPIO_STRENGTH - RW - 32 bits - VIPDEC:0x194			
Field Name	**Bits**	**Default**	**Description**
GPIO_STRENGTH_SN	3:0	0x9	for NMOS of GPIOs
GPIO_STRENGTH_SP	7:4	0xa	for PMOS of GPIOs

Pad strength for ZV_LCD and GPIOs

GPIOPAD_MASK - RW - 32 bits - VIPDEC:0x198			
Field Name	**Bits**	**Default**	**Description**
GPIO_MASK	17:0	0x0	GPIO pads mask.
GENERICD_MASK	18	0x0	GENERICD pad mask. 0=Pin not enabled for GPIO 1=Pin enabled for GPIO. Normal function overridden.

GPIO pads mask register

GPIOPAD_A - RW - 32 bits - VIPDEC:0x19C			
Field Name	**Bits**	**Default**	**Description**
GPIO_A	17:0	0x0	GPIO pads output.
GENERICD_A	18	0x0	GENERICD pad output. 0=GPIO output is low for this pin, if mask and output are enabled. 1=GPIO output is high for this pin, if mask and output are enabled.

GPIO pads output register

GPIOPAD_EN - RW - 32 bits - VIPDEC:0x1A0			
Field Name	**Bits**	**Default**	**Description**
GPIO_EN	17:0	0x0	GPIO pads output enable.
GENERICD_EN	18	0x0	GENERICD pad output enable. 0=GPIO output is disabled for this pin. 1=GPIO output is enabled for this pin.

GPIO pads output enable register

GPIOPAD_Y - RW - 32 bits - VIPDEC:0x1A4			
Field Name	**Bits**	**Default**	**Description**
GPIO_Y (R)	17:0	0x0	GPIO pads input.

GPIO pad input read back.

ZV_LCDPAD_Y - RW - 32 bits - VIPDEC:0x1B4			
Field Name	**Bits**	**Default**	**Description**
ZV_LCDDATA_Y (R)	23:0	0x0	DVO data pads read back.
ZV_LCDCNTL_Y (R)	27:24	0x0	DVO control pads read back.

DVO (Zoom Video/Video Capture/External TMDS) pads read back register

VIPPAD_STRENGTH - RW - 32 bits - VIPDEC:0x1B8			
Field Name	**Bits**	**Default**	**Description**
I2C_STRENGTH_SN	3:0	0x7	NMOS of GPIO[19:18].
I2C_STRENGTH_SP	7:4	0x4	PMOS of GPIO[19:18].
VIPHDAT_STRENGTH_SN	11:8	0x7	NMOS of GPIO[23:21].
VIPHDAT_STRENGTH_SP	15:12	0x4	PMOS of GPIO[23:21].
VIPHCLK_STRENGTH_SN	19:16	0x7	NMOS of GPIO[20].
VIPHCLK_STRENGTH_SP	23:20	0x4	PMOS of GPIO[20].
VIDCAP_STRENGTH_SN	27:24	0x7	NMOS of GPIO[34:24].
VIDCAP_STRENGTH_SP	31:28	0x4	PMOS of GPIO[34:24].

Additional GPIO Interface Output Driver Strength

EXTERN_TRIG_CNTL - RW - 32 bits - VIPDEC:0x1BC			
Field Name	**Bits**	**Default**	**Description**
EXTERN_TRIG_CLR (W)	0	0x0	0=Write 0 has no affect. 1=Write 1 sets EXTERN_TRIG to 0. This can then be used with WAIT_UNTIL(19) to stall until external signal pulses.
EXTERN_TRIG_READ (R)	1	0x0	0=Read 1 indicates WAIT condition not active. 1=Read 0 indicates WAIT condition active.

ROM_INDEX - RW - 32 bits - VIPDEC:0xA8			
Field Name	**Bits**	**Default**	**Description**
ROM_INDEX	16:0	0x0	ROM indirect aperture index register

ROM indirect aperture index register

ROM_DATA - R - 32 bits - VIPDEC:0xAC			
Field Name	**Bits**	**Default**	**Description**
ROM_DATA	7:0	0x0	ROM indirect aperture data register

ROM indirect aperture data register

VIP_HW_DEBUG - RW - 32 bits - VIPDEC:0x1CC			
Field Name	**Bits**	**Default**	**Description**
VIP_HW_0_DEBUG	0	0x0	Not used.
VIP_HW_1_DEBUG	1	0x0	Not used.
VIP_HW_2_DEBUG	2	0x0	Not used.
VIP_HW_3_DEBUG	3	0x0	Not used.
VIP_HW_4_DEBUG	4	0x0	Not used.
VIP_HW_5_DEBUG	5	0x0	Not used.

VIP_HW_6_DEBUG	6	0x0	Not used.
VIP_HW_7_DEBUG	7	0x0	Not used.
VIP_HW_8_DEBUG	8	0x0	Not used.
VIP_HW_9_DEBUG	9	0x0	Not used.
VIP_HW_A_DEBUG	10	0x0	Not used.
VIP_HW_B_DEBUG	11	0x0	Not used.
VIP_HW_C_DEBUG	12	0x0	Not used.
VIP_HW_D_DEBUG	13	0x0	Not used.
VIP_HW_E_DEBUG	14	0x0	Not used.
VIP_HW_F_DEBUG	15	0x0	Not used.

Legacy registers. Not used.

MEDIA_0_SCRATCH - RW - 32 bits - VIPDEC:0x1F0			
Field Name	**Bits**	**Default**	**Description**
MEDIA_0_SCRATCH	31:0	0x0	Scratch pad for MEDIA_0 information

Scratch pad for MEDIA_0 information

MEDIA_1_SCRATCH - RW - 32 bits - VIPDEC:0x1F4			
Field Name	**Bits**	**Default**	**Description**
MEDIA_1_SCRACH	31:0	0x0	Scratch pad for MEDIA_1 information

Scratch pad for MEDIA_1 information

CAP0_ANC_BUF01_BLOCK_CNT - RW - 32 bits - VIPDEC:0x974			
Field Name	**Bits**	**Default**	**Description**
CAP0_ANC_BUF0_BLOCK_CNT (R)	11:0	0x0	ANC buffer 0 block count.
CAP0_ANC_BUF1_BLOCK_CNT (R)	27:16	0x0	ANC buffer 1 block count.

ANC buffer block count

CAP0_ANC_BUF23_BLOCK_CNT - RW - 32 bits - VIPDEC:0x97C			
Field Name	**Bits**	**Default**	**Description**
CAP0_ANC_BUF2_BLOCK_CNT (R)	11:0	0x0	ANC buffer 2 block count.
CAP0_ANC_BUF3_BLOCK_CNT (R)	27:16	0x0	ANC buffer 3 block count.

ANC buffer block count

DMA_VIPH_MISC_CNTL - RW - 32 bits - VIPDEC:0xA14			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH_READ_TIMER	3:0	0xf	VIPH DMA read timer.
DMA_VIPH_READ_TIMEOUT_TO_PIORITY_EN	7	0x0	0=Disable 1=Enable
DMA_VIPH_READ_TIMEOUT_STATUS (R)	8	0x0	0=Normal 1=Timeout

VIPH DMA misc control register.

VIPPAD_MASK - RW - 32 bits - VIPDEC:0xC54			
Field Name	**Bits**	**Default**	**Description**
VIPPAD_MASK_SCL	0	0x0	GPIO override for GPIO[19]. 0=Pin not enabled for GPIO 1=Pin enabled for GPIO. Normal function overridden.
VIPPAD_MASK_SDA	1	0x0	GPIO override for GPIO[18]. 0=Pin not enabled for GPIO 1=Pin enabled for GPIO. Normal function overridden.
VIPPAD_MASK_VHAD	3:2	0x0	GPIO override for GPIO[23:22]. 0=Pin not enabled for GPIO 1=Pin enabled for GPIO. Normal function overridden.
VIPPAD_MASK_VPHCTL	4	0x0	GPIO override for GPIO[21]. 0=Pin not enabled for GPIO 1=Pin enabled for GPIO. Normal function overridden.
VIPPAD_MASK_VIPCLK	5	0x0	GPIO override for GPIO[20]. 0=Pin not enabled for GPIO 1=Pin enabled for GPIO. Normal function overridden.
VIPPAD_MASK_VID	15:8	0x0	GPIO override for GPIO[34:27]. 0=Pin not enabled for GPIO 1=Pin enabled for GPIO. Normal function overridden.
VIPPAD_MASK_VPCLK0	16	0x0	GPIO override for GPIO[24]. 0=Pin not enabled for GPIO 1=Pin enabled for GPIO. Normal function overridden.
VIPPAD_MASK_DVALID	17	0x0	GPIO override for GPIO[26]. 0=Pin not enabled for GPIO 1=Pin enabled for GPIO. Normal function overridden.
VIPPAD_MASK_PSYNC	18	0x0	GPIO override for GPIO[25]. 0=Pin not enabled for GPIO 1=Pin enabled for GPIO. Normal function overridden.

Additional GPIO Interface Mask Control

VIPPAD_A - RW - 32 bits - VIPDEC:0xC58			
Field Name	**Bits**	**Default**	**Description**
VIPPAD_A_SCL	0	0x0	Output for GPIO[19]. 0=GPIO output is low for this pin, if mask and output are enabled. 1=GPIO output is high for this pin, if mask and output are enabled.
VIPPAD_A_SDA	1	0x0	Output for GPIO[18]. 0=GPIO output is low for this pin, if mask and output are enabled. 1=GPIO output is high for this pin, if mask and output are enabled.
VIPPAD_A_VHAD	3:2	0x0	Output for GPIO[23:22]. 0=GPIO output is low for this pin, if mask and output are enabled. 1=GPIO output is high for this pin, if mask and output are enabled.
VIPPAD_A_VPHCTL	4	0x0	Output for GPIO[21]. 0=GPIO output is low for this pin, if mask and output are enabled. 1=GPIO output is high for this pin, if mask and output are enabled.
VIPPAD_A_VIPCLK	5	0x0	Output for GPIO[20]. 0=GPIO output is low for this pin, if mask and output are enabled. 1=GPIO output is high for this pin, if mask and output are enabled.
VIPPAD_A_VID	15:8	0x0	Output for GPIO[34:27]. 0=GPIO output is low for this pin, if mask and output are enabled. 1=GPIO output is high for this pin, if mask and output are enabled.
VIPPAD_A_VPCLK0	16	0x0	Output for GPIO[24]. 0=GPIO output is low for this pin, if mask and output are enabled. 1=GPIO output is high for this pin, if mask and output are enabled.
VIPPAD_A_DVALID	17	0x0	Output for GPIO[26]. 0=GPIO output is low for this pin, if mask and output are enabled. 1=GPIO output is high for this pin, if mask and output are enabled.

VIPPAD_A_PSYNC	18	0x0	Output for GPIO[25]. 0=GPIO output is low for this pin, if mask and output are enabled. 1=GPIO output is high for this pin, if mask and output are enabled.

Additional GPIO Interface Output Control

VIPPAD_EN - RW - 32 bits - VIPDEC:0xC5C			
Field Name	**Bits**	**Default**	**Description**
VIPPAD_EN_SCL	0	0x0	Output enable for GPIO[19]. 0=GPIO output is disabled for this pin. 1=GPIO output is enabled for this pin.
VIPPAD_EN_SDA	1	0x0	Output enable for GPIO[18]. 0=GPIO output is disabled for this pin. 1=GPIO output is enabled for this pin.
VIPPAD_EN_VHAD	3:2	0x0	Output enable for GPIO[23:22]. 0=GPIO output is disabled for this pin. 1=GPIO output is enabled for this pin.
VIPPAD_EN_VPHCTL	4	0x0	Output enable for GPIO[21]. 0=GPIO output is disabled for this pin. 1=GPIO output is enabled for this pin.
VIPPAD_EN_VIPCLK	5	0x0	Output enable for GPIO[20]. 0=GPIO output is disabled for this pin. 1=GPIO output is enabled for this pin.
VIPPAD_EN_VID	15:8	0x0	Output enable for GPIO[34:27]. 0=GPIO output is disabled for this pin. 1=GPIO output is enabled for this pin.
VIPPAD_EN_VPCLK0	16	0x0	Output enable for GPIO[24]. 0=GPIO output is disabled for this pin. 1=GPIO output is enabled for this pin.
VIPPAD_EN_DVALID	17	0x0	Output enable for GPIO[26]. 0=GPIO output is disabled for this pin. 1=GPIO output is enabled for this pin.
VIPPAD_EN_PSYNC	18	0x0	Output enable for GPIO[25]. 0=GPIO output is disabled for this pin. 1=GPIO output is enabled for this pin.

Additional GPIO Interface Output Enable Control

VIPPAD_Y - R - 32 bits - VIPDEC:0xC60			
Field Name	**Bits**	**Default**	**Description**
VIPPAD_Y_SCL	0	0x0	Input readback of GPIO[19]. 0=This pin was low at time of read. 1=This pin was high at time of read.
VIPPAD_Y_SDA	1	0x0	Input readback of GPIO[18]. 0=This pin was low at time of read. 1=This pin was high at time of read.
VIPPAD_Y_VHAD	3:2	0x0	Input readback of GPIO[23:22]. 0=This pin was low at time of read. 1=This pin was high at time of read.
VIPPAD_Y_VPHCTL	4	0x0	Input readback of GPIO[21]. 0=This pin was low at time of read. 1=This pin was high at time of read.
VIPPAD_Y_VIPCLK	5	0x0	Input readback of GPIO[20]. 0=This pin was low at time of read. 1=This pin was high at time of read.
VIPPAD_Y_VID	15:8	0x0	Input readback of GPIO[34:27]. 0=This pin was low at time of read. 1=This pin was high at time of read.

VIPPAD_Y_VPCLK0	16	0x0	Input readback of GPIO[24]. 0=This pin was low at time of read. 1=This pin was high at time of read.
VIPPAD_Y_DVALID	17	0x0	Input readback of GPIO[26]. 0=This pin was low at time of read. 1=This pin was high at time of read.
VIPPAD_Y_PSYNC	18	0x0	Input readback of GPIO[25]. 0=This pin was low at time of read. 1=This pin was high at time of read.

Additional GPIO Interface Input Readback

MAXX_PWM - RW - 32 bits - VIPDEC:0xC64			
Field Name	**Bits**	**Default**	**Description**
PWM_INC	7:0	0x0	PWM increment
PWM_CLK_DIV	11:8	0x0	PWM clock divider
PWM_OUT_EN	16	0x0	0=PWM output disabled. 1=PWM output enabled. PSYNC pin becomes output enabled and drives out PWM signal.

GEN_INT_CNTL - RW - 32 bits - VIPDEC:0x100			
Field Name	**Bits**	**Default**	**Description**
DMA_VIPH0_INT_EN	12	0x0	VIP host port channel 0 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH1_INT_EN	13	0x0	VIP host port channel 1 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH2_INT_EN	14	0x0	VIP host port channel 2 DMA interrupt mask. 0=Disable 1=Enable
DMA_VIPH3_INT_EN	15	0x0	VIP host port channel 3 DMA interrupt mask. 0=Disable 1=Enable
I2C_INT_EN	17	0x0	I2C interrupt mask. 0=Disable 1=Enable
Reserved	20	0x0	
VIPH_INT_EN	24	0x0	VIP host port interrupt mask. 0=Disable 1=Enable

General Interrupt Control register.
The MASK/EN fields control whether the respective status bits are enabled to drive the system interrupt pin. Even if enabled here, the interrupt line is not driven unless enabled in the PCI configuration space.

GEN_INT_STATUS - RW - 32 bits - VIPDEC:0x104			
Field Name	**Bits**	**Default**	**Description**
CAP0_INT_ACTIVE (R)	8	0x0	Capture port 0 has active interrupt(s). 0=Capture port 0 not source of any active interrupt 1=Capture port 0 has active interrupt(s)
DMA_VIPH0_INT (R)	12	0x0	VIP host port channel 0 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH0_INT_AK (W)	12	0x0	VIP host port channel 0 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH1_INT (R)	13	0x0	VIP host port channel 1 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH1_INT_AK (W)	13	0x0	VIP host port channel 1 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH2_INT (R)	14	0x0	VIP host port channel 2 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH2_INT_AK (W)	14	0x0	VIP host port channel 2 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
DMA_VIPH3_INT (R)	15	0x0	VIP host port channel 3 DMA interrupt. 0=No event 1=Event has occurred, interrupting if enabled
DMA_VIPH3_INT_AK (W)	15	0x0	VIP host port channel 3 DMA interrupt acknowledge/reset. 0=No effect 1=Clear status
I2C_INT (R)	17	0x0	I2C interrupt. 0=No event 1=Event has occurred, interrupting if enabled

I2C_INT_AK (W)	17	0x0	I2C interrupt acknowledge/reset. 0=No effect 1=Clear status
Reserved	20	0x0	
VIPH_INT (R)	24	0x0	VIP host port interrupt. 0=No event 1=Event has occurred, interrupting if enabled

General Interrupt Status register.
These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN_INT_CNTL register.

2.5 Clock Generator Registers

CLOCK_CNTL_INDEX - RW - 32 bits - CGDEC:0xE008			
Field Name	**Bits**	**Default**	**Description**
PLL_ADDR	5:0	0x0	Register address
PLL_WR_EN	7	0x0	0=Disable writes to CLOCK_CNTL_DATA 1=Enable writing to CLOCK_CNTL_DATA
PPLL_DIV_SEL	9:8	0x0	0=PPLL_DIV0 1=PPLL_DIV1 2=PPLL_DIV2 3=PPLL_DIV3

Clock generation block register index control

CLOCK_CNTL_DATA - RW - 32 bits - CGDEC:0xE00C			
Field Name	**Bits**	**Default**	**Description**
PLL_DATA	31:0	0x0	Register value

Clock generation block register data

SPLL_FUNC_CNTL - RW - 32 bits - CLKIND:0x0			
Field Name	**Bits**	**Default**	**Description**
SPLL_RESET	0	0x1	0=Run 1=Reset
SPLL_SLEEP	1	0x0	0=Power Up 1=Power Down
SPLL_REF_DIV	4:2	0x1	SPLL reference divider value
SPLL_FB_DIV	12:5	0x47	SPLL feedback divider value
SPLL_PULSEEN	13	0x0	0=Don't pulse clock 1=Send the number of pulses indicated by PULSENUM
SPLL_PULSENUM	15:14	0x0	Number of pulses required by SPLL
SPLL_SW_HILEN	19:16	0x0	Post divider value for SPLL (high pulse section)
SPLL_SW_LOLEN	23:20	0x0	Post divider value for SPLL (low pulse section)
SPLL_DIVEN	24	0x1	1=Enable PLL CLKOUT divider
SPLL_BYPASS_EN	25	0x1	1=Enable Bypass Clockout
SPLL_CHG_STATUS (R)	29	0x0	1=Previous write/change to SPLL_FUNC_CNTL register has been completed. SW should not issue another write to this register until this bit is asserted
SPLL_CTLREQ	30	0x0	1=For debug purpose: when SW_DIR_CONTROL is set, assert this bit will trigger an update of the PLL clock output mux control. Before write to this bit, HILEN/LOLEN/PULSEEN/PULSENUM should already contain the new set of value
SPLL_CTLACK (R)	31	0x0	1=For debug purpose: when SW_DIR_CONTROL is set, this value replicates the value of the CTLREQ once the command has been received and it is safe to send another request

SPLL control register

SPLL_BYPASSCLK_SEL - RW - 32 bits - CLKIND:0x1			
Field Name	**Bits**	**Default**	**Description**
SPLL_CLKOUT_SEL	5:0	0x6	1=BCLK 2=MCLK 4=DISP CLK 8=AUXSIN 32=INV BCLK

SPLL_CNTL_MODE - RW - 32 bits - CLKIND:0x2			
Field Name	**Bits**	**Default**	**Description**
SPLL_SW_DIR_CONTROL	0	0x1	1=SW controls the PLL directly. SW will make sure the way they program SPLL_FUNC_CNTL register follows the PLL's requested protocol

SPLL_CLK_SEL - RW - 32 bits - CLKIND:0x3			
Field Name	**Bits**	**Default**	**Description**
SPLL_REFCLK_SRC_SEL	0	0x0	0=Ref clock from GPIO 1=Ref clock from XTALIN
SPLL_TEST	1	0x0	1=Enable SPLL test mode
SPLL_FASTEN	2	0x1	1=Enable SPLL fast lock
SPLL_ENSAT	3	0x1	1=Enable saturation behavior

MPLL_FUNC_CNTL - RW - 32 bits - CLKIND:0x4			
Field Name	**Bits**	**Default**	**Description**
MPLL_RESET	0	0x1	0=Run 1=Reset
MPLL_SLEEP	1	0x0	0=Power Up 1=Power Down
MPLL_REF_DIV	4:2	0x1	MPLL reference divider value
MPLL_FB_DIV	12:5	0x6f	MPLL feedback divider value
MPLL_PULSEEN	13	0x0	0=Don't pulse clock 1=Send the number of pulses indicated by PULSENUM
MPLL_PULSENUM	15:14	0x0	Not used
MPLL_SW_HILEN	19:16	0x0	Not used
MPLL_SW_LOLEN	23:20	0x0	Not used
MPLL_DIVEN	24	0x0	1=Enable PLL CLKOUT divider
MPLL_BYPASS_EN	25	0x1	1=Enable Bypass mode
MPLL_MCLK_SEL	26	0x0	1=Use MPLL output as mclk
MPLL_CHG_STATUS (R)	29	0x0	1=Previous write/change to MPLL_FUNC_CNTL register has been completed. SW should not issue another write to this register until this bit is asserted
MPLL_CTLREQ	30	0x0	1=For debug purpose: when SW_DIR_CONTROL is set, assert this bit will trigger an update of the PLL clock output mux control. Before write to this bit, HILEN/LOLEN/PULSEEN/PULSENUM should already contain the new set of value
MPLL_CTLACK (R)	31	0x0	1=For debug purpose: when SW_DIR_CONTROL is set, this value replicates the value of the CTLREQ once the command has been received and it is safe to send another request

MPLL Control register

MPLL_BYPASSCLK_SEL - RW - 32 bits - CLKIND:0x5			
Field Name	**Bits**	**Default**	**Description**
MPLL_CLKOUT_SEL	5:0	0x6	1=BCLK 2=SCLK 4=DISP CLK 8=TEST YCLK 32=INV BCLK

MPLL_CNTL_MODE - RW - 32 bits - CLKIND:0x6			
Field Name	**Bits**	**Default**	**Description**
MPLL_SW_DIR_CONTROL	1	0x0	1=SW controls the PLL directly. SW will make sure the way they program MPLL_FUNC_CNTL register follows the PLL's requested protocol

MPLL_CLK_SEL - RW - 32 bits - CLKIND:0x7			
Field Name	**Bits**	**Default**	**Description**
MPLL_REFCLK_SRC_SEL	0	0x0	0=Ref clock from GPIO 1=Ref clock from XTALIN
MPLL_TEST	1	0x0	1=Enable MPLL test mode
MPLL_FASTEN	2	0x1	1=Enable MPLL fast lock
MPLL_ENSAT	3	0x1	1=Enable saturation behavior

GENERAL_PWRMGT - RW - 32 bits - CLKIND:0x8			
Field Name	**Bits**	**Default**	**Description**
GLOBAL_PWRMGT_EN	0	0x0	0=dynamic power management off 1=dynamic power management on
MOBILE_SU	2	0x0	0=Regular 1=Optimize power consumption in Suspend mode for mobile
SU_SUSTAIN_DISABLE	3	0x0	0=Sustain suspend until PLL lockup 1=Disable

SCLK_PWRMGT_CNTL - RW - 32 bits - CLKIND:0x9			
Field Name	**Bits**	**Default**	**Description**
SCLK_PWRMGT_OFF	0	0x0	0=SCLK power management on 1=SCLK power management off
SCLK_TURNOFF	1	0x0	1=Turn off SCLK, SW direct control, override HW pwrmgt control
SPLL_TURNOFF	2	0x0	1=Power down SPLL, SW direct control, override HW pwrmgt control
SPARE	3	0x0	Reserved

SU_SCLK_USE_BCLK	4	0x0	0=Use slower SCLK under suspend mode 1=Use BCLK as SCLK under suspend mode
ACCESS_REGS_IN_SUSPEND	5	0x0	0=disable 1=force all SCLK branches to allow accessing any registers in suspend mode

SCLK domain static power management

MCLK_PWRMGT_CNTL - RW - 32 bits - CLKIND:0xA			
Field Name	**Bits**	**Default**	**Description**
MPLL_PWRMGT_OFF	0	0x0	0=M domain clock power management off
YCLK_TURNOFF	1	0x0	0=Turn off YCLK
MPLL_TURNOFF	2	0x0	0=Enable M domain PLL to be turned off at power state D3
SU_MCLK_USE_BCLK	3	0x0	0=Shut down MCLK during suspend mode 1=Use BCLK as SCLK under suspend mode
DLL_READY	4	0x0	0=DLL is not ready 1=DLL is ready
MC_BUSY (R)	5	0x0	0=MC is idle 1=MC is not idle
MC_SWITCH	6	0x0	0=source of memory clock is not changed 1=source of memory clock is changed
MC_INT_CNTL	7	0x1	0=SW overwrite 1=HW control
MRDCKA_SLEEP	8	0x0	0=Enable Channel A DLL 1=PowerDown Channel A DLL
MRDCKB_SLEEP	9	0x0	0=Enable Channel B DLL 1=PowerDown Channel B DLL
MRDCKC_SLEEP	10	0x0	0=Enable Channel C DLL 1=PowerDown Channel C DLL
MRDCKD_SLEEP	11	0x0	0=Enable Channel D DLL 1=PowerDown Channel D DLL
MRDCKA_RESET	12	0x1	0=Enable Channel A DLL 1=Reset Channel A DLL
MRDCKB_RESET	13	0x1	0=Enable Channel B DLL 1=Reset Channel B DLL
MRDCKC_RESET	14	0x1	0=Enable Channel C DLL 1=Reset Channel C DLL
MRDCKD_RESET	15	0x1	0=Enable Channel D DLL 1=Reset Channel D DLL
DLL_READY_READ (R)	16	0x0	0=DLL is not ready 1=DLL is ready

DYN_PWRMGT_SCLK_CNTL - RW - 32 bits - CLKIND:0xB			
Field Name	**Bits**	**Default**	**Description**
ENGINE_DYNCLK_MODE	0	0x0	0=Treat engine as one single block 1=Provide clock for each engine block separately
SCLK_DYN_START_CNTL	1	0x1	0=SCLK starts 4 clocks after BUSY active 1=SCLK starts 1 clock after BUSY active
PROG_DELAY_OFFSET	9:2	0x0	This field is used to increase latency to turn on clocks/turn off clocks. The clock turnon/turnoff latency equals to (PROG_DELAY_OFFSET+1)*<client>_PROG_DELAY_VALUE
PROG_SHUTOFF_REVERT	10	0x0	1=Use revert value of PROG_DELAY_VALUE as shutoff counter value, only used when the corresponding client's PROG_SHUTOFF is set
DYN_STOP_LAT	14:11	0x5	delay between idle state get detected till sclk get turned off
ACTIVE_ENABLE_LAT	19:15	0x5	delay between clock_enable changes to cg_rbbm_active changes

STATIC_SCREEN_EN	20	0x0	1=Enable Static Screen Mode
CLIENT_SELECT_POWER_EN	21	0x0	1=Enable Client Based Power Request
LOWER_POWER_STATE (R)	22	0x0	1=CG is in Lower Power State based on client's request
STATIC_SCREEN_STATE (R)	23	0x0	1=CG is in static screen state
SW_NORMAL_POWER	24	0x0	1=Force to go back to normal power state
CLIENT_BUSY_GAP_LAT	29:25	0x8	0=Number of idle cycles allowed during 2 consecutive busy cycles

Dynamic clock gating control

DYN_PWRMGT_SCLK_LENGTH - RW - 32 bits - CLKIND:0xC			
Field Name	**Bits**	**Default**	**Description**
NORMAL_POWER_SCLK_HILEN	3:0	0x0	Post divider value for full power mode (high pulse)
NORMAL_POWER_SCLK_LOLEN	7:4	0x0	Post divider value for full power mode (low pulse)
REDUCED_POWER_SCLK_HILEN	11:8	0x1	Post divider value for reduced power mode (high pulse
REDUCED_POWER_SCLK_LOLEN	15:12	0x1	Post divider value for reduced power mode (low pulse)
POWER_D1_SCLK_HILEN	19:16	0x2	Post divider value for D1 mode (high pulse)
POWER_D1_SCLK_LOLEN	23:20	0x2	Post divider value for D1 mode (low pulse)
STATIC_SCREEN_HILEN	27:24	0x4	Post divider value for static screen mode (high pulse)
STATIC_SCREEN_LOLEN	31:28	0x4	Post divider value for static screen mode (low pulse)

Frequency control for different power stage

DYN_SCLK_PWMEN_PIPE - RW - 32 bits - CLKIND:0xD			
Field Name	**Bits**	**Default**	**Description**
PIPE_2D_MASK	3:0	0x1	Mask the pipe which is used by 2D
PIPE_3D_MASK	7:4	0x1	Mask the pipe which is used by 3D
PIPE_3D_NOT_AUTO	8	0x1	0=Auto disable unused pipes' clk 1=Enable pipes' clk based on PIPE_3D_MASK & PIPE_Z_MASK field
PIPE_Z_MASK	13:12	0x3	
PIPE_ALU_MASK	18:16	0x7	

Dynamic clock gating pipe control

DYN_SCLK_VOL_CNTL - RW - 32 bits - CLKIND:0xE			
Field Name	**Bits**	**Default**	**Description**
IO_CG_VOLTAGE_DROP	0	0x0	0=Disable dynamic core voltage drop 1=Enable dynamic core voltage drop
VOLTAGE_DROP_SYNC	2	0x0	0=Disable synchronization of reduced speed SCLK and core voltage drop 1=Enable synchronization
VOLTAGE_DELAY_SEL	22:3	0x0	delay (in sclk cycle) between voltage goes to normal till sclk speed goes back to normal

Static screen mode voltage control

VIP_DYN_CNTL - RW - 32 bits - CLKIND:0x14			
Field Name	**Bits**	**Default**	**Description**

VIP_FORCEON	0	0x1	0=Dynamic control VIP sclk branch 1=Disable dynamic control of VIP sclk branch
VIP_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
VIP_CLOCK_STATUS (R)	2	0x0	0=VIP branch is off 1=VIP branch is on
VIP_PROG_SHUTOFF	3	0x0	1=VIP branch shutoff with PROG_DELAY_VALUE delay
VIP_PROG_DELAY_VALUE	11:4	0x1	Delay VIP clock on/off by number of cycles
VIP_LOWER_POWER_IDLE	19:12	0xff	Count VIP idle for number of cycles before dropping the power level, only used when VIP_LOWER_POWER_IGNORE set to 0
VIP_LOWER_POWER_IGNORE	20	0x1	1=VIP not vote for going to lower power state
VIP_NORMAL_POWER_IGNORE	21	0x1	1=VIP not vote for going back to normal power state
SPARE	23:22	0x0	Reserved
VIP_NORMAL_POWER_BUSY	31:24	0xf	Count VIP busy for number of cycles before raising the power level, only used when VIP_NORMAL_POWER_IGNORE set to 0

VIP dynamic clock gating control

TCL_DYN_CNTL - RW - 32 bits - CLKIND:0x1A			
Field Name	**Bits**	**Default**	**Description**
TCL_FORCEON	0	0x1	0=Dynamic control CP sclk branch 1=Disable dynamic control of CP sclk branch
TCL_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
TCL_CLOCK_STATUS (R)	2	0x0	0=TCL branch is off 1=TCL branch is on
TCL_PROG_SHUTOFF	3	0x0	1=TCL branch shutoff with PROG_DELAY_VALUE delay
TCL_PROG_DELAY_VALUE	11:4	0x1	Delay TCL clock on/off by number of cycles

TCL dynamic clock gating control

MC_GUI_DYN_CNTL - RW - 32 bits - CLKIND:0x1D			
Field Name	**Bits**	**Default**	**Description**
MC_GUI_FORCEON	0	0x1	0=Dynamic control MC_GUI sclk branch 1=Disable dynamic control of MC_GUI sclk branch
MC_GUI_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
MC_GUI_CLOCK_STATUS (R)	2	0x0	0=MC_GUI branch is off 1=MC_GUI branch is on
MC_GUI_PROG_SHUTOFF	3	0x0	1=MC_GUI branch shutoff with PROG_DELAY_VALUE delay
MC_GUI_PROG_DELAY_VALUE	11:4	0x1	Delay MC_GUI clock on/off by number of cycles

MC_GUI dynamic clock gating control

MC_HOST_DYN_CNTL - RW - 32 bits - CLKIND:0x1E			
Field Name	**Bits**	**Default**	**Description**
MC_HOST_FORCEON	0	0x1	0=Dynamic control MC_HOST sclk branch 1=Disable dynamic control of MC_HOST sclk branch
MC_HOST_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
MC_HOST_CLOCK_STATUS (R)	2	0x0	0=MC_HOST branch is off 1=MC_HOST branch is on
MC_HOST_PROG_SHUTOFF	3	0x0	1=MC_HOST branch shutoff with PROG_DELAY_VALUE delay
MC_HOST_PROG_DELAY_VALUE	11:4	0x1	Delay MC_HOST clock on/off by number of cycles

MC_HOST dynamic clock gating control

MC_RBS_DYN_CNTL - RW - 32 bits - CLKIND:0x26			
Field Name	**Bits**	**Default**	**Description**
MC_RBS_FORCE	0	0x1	0=Dynamic control CP sclk branch 1=Disable dynamic control of CP sclk branch
MC_RBS_MAX_DYN_STOP_LAT	1	0x1	0=Programmable dynamic stopping latency 1=Max dynamic stopping latency
MC_RBS_CLOCK_STATUS (R)	2	0x0	0=MC_RBS branch is off 1=MC_RBS branch is on
MC_RBS_PROG_SHUTOFF	3	0x0	1=MC_RBS branch shutoff with PROG_DELAY_VALUE delay
MC_RBS_PROG_DELAY_VALUE	11:4	0x1	Delay MC_RBS clock on/off by number of cycles

MC_RBS dynamic clock gating control

CG_MISC_REG - RW - 32 bits - CLKIND:0x1F			
Field Name	**Bits**	**Default**	**Description**
STARTUP_COUNTER	11:0	0x28	Not used
SYNCHRONIZER_COUNTER	15:12	0x8	Debug purpose, number of cycles to be used by clock switch logic
DISPCLK_FUNC_SEL	16	0x0	1=Use non functional display clock
SPARE	23:17	0x0	Reserved

Miscellaneous control register

PLL_TEST_CNTL - RW - 32 bits - CLKIND:0x21			
Field Name	**Bits**	**Default**	**Description**
TST_SRC_SEL	3:0	0x0	Source clock to be measured
TST_REF_SEL	7:4	0x0	Clock used as a frequency reference
REF_TEST_COUNT	14:8	0x0	Run TST_REF_SEL by number of cycles
TST_RESET	15	0x0	Reset frequency counter
TEST_COUNT (R)	31:17	0x0	Frequency output value

PLL frequency measurement cntl

MCLK_MISC - RW - 32 bits - CLKIND:0x22			
Field Name	**Bits**	**Default**	**Description**
SPARE_0	1:0	0x0	Reserved
MRDCKA0_SOUTSEL	3:2	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKA1_SOUTSEL	5:4	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKB0_SOUTSEL	7:6	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKB1_SOUTSEL	9:8	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements

MRDCKC0_SOUTSEL	11:10	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKC1_SOUTSEL	13:12	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKD0_SOUTSEL	15:14	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MRDCKD1_SOUTSEL	17:16	0x0	0=DLL output clock 1=QS pin 2=QS delayed 2 elements 3=QS delayed 4 elements
MCLK_NONFUNC_SEL	18	0x0	0=Select functional mclk source 1=Select non-functional mode mclk source
SPARE	31:19	0x0	Reserved

Miscellaneous Control over MCLK

DLL_CNTL - RW - 32 bits - CLKIND:0x23			
Field Name	**Bits**	**Default**	**Description**
DLL_RESET_TIME	9:0	0x1f4	Number of cycles required to hold DLL reset high
DLL_LOCK_TIME	21:12	0xfa	Number of cycles required to wait for DLL get locked

DLL control register

SPLL_TIME - RW - 32 bits - CLKIND:0x24			
Field Name	**Bits**	**Default**	**Description**
SPLL_LOCK_TIME	15:0	0x2000	number of PCIE refclk cycles need to wait before PLL get locked
SPLL_RESET_TIME	31:16	0x1f4	PLL reset pulse width (in PCIE refclk cycles

SPLL related timing counter

MPLL_TIME - RW - 32 bits - CLKIND:0x25			
Field Name	**Bits**	**Default**	**Description**
MPLL_LOCK_TIME	15:0	0x2000	Number of PCIE refclk cycles need to wait before PLL get locked
MPLL_RESET_TIME	31:16	0x1f4	PLL reset pulse width (in PCIE refclk cycles)

MPLL related timing counter

DYN_BACKBIAS_CNTL - RW - 32 bits - CLKIND:0x29			
Field Name	**Bits**	**Default**	**Description**
IO_CG_BACKBIAS_EN	0	0x0	0=Disable dynamic back bias switching 1=Enable dynamic back bias switching
BACKBIAS_SYNC	1	0x0	0=Disable synchronization of reduced speed SCLK and back bias switching 1=Enable synchronization
BACKBIAS_DELAY_SEL	22:3	0x0	delay (in sclk cycle) between backbias disabled till sclk speed goes back to normal

Static screen mode backbias control

POLARITY_CNTL - RW - 32 bits - CLKIND:0x2A			
Field Name	**Bits**	**Default**	**Description**
IO_BACKBIAS_POLARITY	0	0x1	0=Negative 1=Positive
IO_VOLTAGE_REGULATOR_POLARITY	1	0x1	0=Negative 1=Positivie

ERROR_STATUS - RW - 32 bits - CLKIND:0x2C			
Field Name	**Bits**	**Default**	**Description**
Reserved	0:1	0x0	
SPLL_UNLOCK (R)	2	0x0	SCLK is not locked
YPLL_UNLOCK (R)	3	0x0	

CG related error status, any reads to this register will clean the status

CG_CLKPIN_CNTL - RW - 32 bits - CLKIND:0x3C			
Field Name	**Bits**	**Default**	**Description**
OSC_EN	0	0x1	0=Disable Oscillation 1=Enable Oscillation
XTL_LOW_GAIN	1	0x1	0=High Gain 1=Low Gain
CG_CLK_TO_OUTPIN	2	0x0	0=Disabled 1=Send out selected clock for jitter test
OSC_USE_CORE	3	0x0	0=Pad routing OSC 1=Core routing OSC

VOL_DROP_CNT - RW - 32 bits - CLKIND:0x36

Field Name	Bits	Default	Description
VOL_DROP_DELAY	31:0	0x100	delay (in sclk cycle) between static screen condition get detected till voltage get dropped

Static screen mode voltage control

CG_TC_JTAG_0 - RW - 32 bits - CLKIND:0x38			
Field Name	**Bits**	**Default**	**Description**
CG_TC_TMS	7:0	0x0	8 consecutive values for TMS. Bit 0 is sent first.
CG_TC_TDI	15:8	0x0	8 consecutive values for TDI. Bit 0 is sent first.
CG_TC_MODE	17:16	0x0	Indicates what clock should be used for TCK in the JTAG transactions. 0=No Clock 1=PCIE Reference Clock / 4 2=PCIE Reference Clock / 10 3=PCIE Reference Clock / 20
CG_TC_TDO_MASK	31:24	0x0	A mask indicating whether the TDO value should be read back for a given JTAG cycle. Bit 0 corresponds to the first TDO sample. This mask can be used to prevent the readback of unknown values across the bus interface during simulation. This field can be set to all 1's on real hardware.

CG Interface to the Test Controller (TC) using IEEE JTAG protocol. This register can be written with 8 consecutive values for the inputs to the TC's JTAG port. These 8 inputs are sent at consecutive TCK clock edges. The final value is held for indefinitely many TCK clock edges until the next write to this register. The register can be used to walk through several states of the JTAG state machine and typically the state machine would be left in a 'paused' state. The TDO values sampled at the 8 edges for which input was provided is available for readback from the TC_CG_TDO field of the CG_TC_JTAG_1 register.

CG_TC_JTAG_1 - R - 32 bits - CLKIND:0x39			
Field Name	**Bits**	**Default**	**Description**
TC_CG_TDO	7:0	0x0	8 consecutive sampled values of TDO. Bit 0 corresponds to the cycle that the first bit of CG_TC_JTAG_0.CG_TC_TMS and CG_TC_JTAG_0.CG_TC_TDI were sampled by the Test Controller.
TC_CG_DONE	31	0x0	Indicates whether the JTAG sequence has completed. 0=We have completed less than 8 JTAG cycles since the last write to CG_TC_JTAG_0 1=All 8 JTAG cycles have been completed since the last write to CG_TC_JTAG_0

TDO readback and status bits for the CG JTAG interface described in more detail in the CG_TC_JTAG_0 register description.

2.6 VGA Registers

2.6.1 VGA Control/Status Registers

General purpose status VGA

GENFC_RD - R - 8 bits - DISPDEC:0x3CA			
Field Name	**Bits**	**Default**	**Description**
VSYNC_SEL_R (mirror of GENFC_WT:VSYNC_SEL_W)	3	0x0	Vertical sync select (read). 0=Normal vertical sync 1=Sync is 'vertical sync' ORed with 'vertical display enable'
Feature Control Register (Read)			

GENFC_WT - W - 8 bits - [DISPDEC:0x3BA] [DISPDEC:0x3DA]			
Field Name	**Bits**	**Default**	**Description**
VSYNC_SEL_W	3	0x0	Vertical sync select (write). 0=Normal vertical sync 1=Sync is 'vertical sync' ORed with 'vertical display enable'
Feature Control Register (Read)			

GENMO_WT - W - 8 bits - DISPDEC:0x3C2			
Field Name	**Bits**	**Default**	**Description**
GENMO_MONO_ADDRESS_B	0	0x0	VGA addressing mode. 0=Monochrome emulation, regs at 0x3Bx 1=Color/Graphic emulation, regs at 0x3Dx
VGA_RAM_EN	1	0x0	Enables/Disables CPU access to video RAM at VGA aperture. 0=Disable 1=Enable
VGA_CKSEL	3:2	0x0	Selects pixel clock frequency to use in VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN=0. See CLOCK_CNTL_INDEX.PPLL_DIV_SEL for non-VGA mode pixel clock selection. 0=25.1744MHz (640 Pels) 1=28.3212MHz (720 Pels) 2=Reserved 3=Reserved
ODD_EVEN_MD_PGSEL	5	0x0	This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled. Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory. 0=Selects odd (high) memory locations 1=Selects even (low) memory locations
VGA_HSYNC_POL	6	0x0	Determines polarity of horizontal sync (HSYNC) for VGA modes. 0 = HSYNC pulse active high 1 = HSYNC pulse active low The convention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.

VGA_VSYNC_POL	7	0x0	Determines polarity of vertical sync (VSYNC) for VGA modes. 0 = VSYNC pulse active high 1 = VSYNC pulse active low The convention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.

Miscellaneous Output Register (Write)

GENMO_RD - R - 8 bits - DISPDEC:0x3CC			
Field Name	**Bits**	**Default**	**Description**
GENMO_MONO_ADDRESS_B (mirror of GENMO_WT:GENMO_MONO_ADDRESS_B)	0	0x0	VGA addressing mode. 0=Monochrome emulation, regs at 0x3Bx 1=Color/Graphic emulation, regs at 0x3Dx
VGA_RAM_EN (mirror of GENMO_WT:VGA_RAM_EN)	1	0x0	Enables/Disables CPU access to video RAM at VGA aperture. 0=Disable 1=Enable
VGA_CKSEL (mirror of GENMO_WT:VGA_CKSEL)	3:2	0x0	Selects pixel clock frequency to use. 0=25.1744MHz (640 Pels) 1=28.3212MHz (720 Pels) 2=Reserved 3=Reserved
ODD_EVEN_MD_PGSEL (mirror of GENMO_WT:ODD_EVEN_MD_PGSEL)	5	0x0	This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled. Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory. 0=Selects odd (high) memory locations 1=Selects even (low) memory locations
VGA_HSYNC_POL (mirror of GENMO_WT:VGA_HSYNC_POL)	6	0x0	Determines polarity of horizontal sync (HSYNC) for VGA modes. 0 = HSYNC pulse active high 1 = HSYNC pulse active low The convention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.
VGA_VSYNC_POL (mirror of GENMO_WT:VGA_VSYNC_POL)	7	0x0	Determines polarity of vertical sync (VSYNC) for VGA modes. 0 = VSYNC pulse active high 1 = VSYNC pulse active low The convention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.

Miscellaneous Output Register (Read)

GENS0 - R - 8 bits - DISPDEC:0x3C2			
Field Name	**Bits**	**Default**	**Description**
SENSE_SWITCH	4	0x0	DAC comparator read back. Used for monitor detection. Mirror of DAC_CMP_OUTPUT@DAC_CNTL. See description there.
CRT_INTR	7	0x0	CRT Interrupt: 0=Vertical retrace interrupt is cleared 1=Vertical retrace interrupt is pending

Input Status 0 Register

GENS1 - R - 8 bits - [DISPDEC:0x3BA] [DISPDEC:0x3DA]			
Field Name	**Bits**	**Default**	**Description**
NO_DISPLAY	0	0x0	Display enable. 0=Enable 1=Disable
VGA_VSTATUS	3	0x0	Vertical Retrace Status. 0=Vertical retrace not active 1=Vertical retrace active
PIXEL_READ_BACK	5:4	0x0	Diagnostic bits 0, 1 respectively. These two bits are connected to two of the eight colour outputs (P7:P0) of the attribute controller. Connections are controlled by ATTR12(5,4) as follows: 0=P2,P0 1=P5,P4 2=P3,P1 3=P7,P6

Input Status 1 Register

2.6.2 VGA DAC Control Registers

VGA DAC Registers

DAC_DATA - RW - 8 bits - DISPDEC:0x3C9			
Field Name	**Bits**	**Default**	**Description**
DAC_DATA	5:0	0x0	VGA Palette (DAC) Data. Use DAC_R_INDEX and DAC_W_INDEX to set read or write mode, and entry to access. Access order is Red, Green, Blue, and then auto-increment occurs to next entry. DAC_8BIT_EN controls whether 6 or 8 bit access.

VGA Palette (DAC) Data

DAC_MASK - RW - 8 bits - DISPDEC:0x3C6			
Field Name	**Bits**	**Default**	**Description**
DAC_MASK	7:0	0x0	Masks off usage of individual palette index bits before pixel index is looked-up in the palette. 0 = do not use this bit of the index 1 = use this bit of the index Only has an effect in VGA emulation modes (CRTC_EXT_DISP_EN=0), not for VESA modes or extended display modes.

Palette index mask for VGA emulation modes.

DAC_R_INDEX - RW - 8 bits - DISPDEC:0x3C7			
Field Name	**Bits**	**Default**	**Description**
DAC_R_INDEX	7:0	0x0	Write: Sets the index for a palette (DAC) read operation. Index auto-increments after every third read of DAC_DATA. Read: Indicates if palette in read or write mode. 0 = Palette in write mode (DAC_W_INDEX last written). 3 = Palette in read mode (DAC_R_INDEX last written). Also see DAC_W_INDEX.

Palette (DAC) Read Index

DAC_W_INDEX - RW - 8 bits - DISPDEC:0x3C8			
Field Name	**Bits**	**Default**	**Description**
DAC_W_INDEX	7:0	0x0	Sets the index for a palette (DAC) write operation. Index auto-increments after every third write of DAC_DATA. Also see DAC_R_INDEX.

Palette (DAC) Write Index

2.6.3 VGA Sequencer Registers

SEQ00 - RW - 8 bits - VGASEQIND:0x0			
Field Name	**Bits**	**Default**	**Description**
SEQ_RST0B	0	0x1	Synchronous reset bit 0: 0=Follows SEQ_RST1B 1=Sequencer runs unless SEQ_RST1B=0
SEQ_RST1B	1	0x1	Synchronous reset bit 1: 0=Disable character clock, display requests, and H/V syncs 1=Sequencer runs unless SEQ_RST0B=0

Reset Register

SEQ01 - RW - 8 bits - VGASEQIND:0x1			
Field Name	**Bits**	**Default**	**Description**
SEQ_DOT8	0	0x1	8/9 Dot Clocks (Modes 1, 2, 3, and 7 use 9-dot characters. To change bit 0, GENVS(0) must be logical 0). 0=9 dot char clock. Modes 0, 1, 2, 3 & 7 1=8 dot char clock.
SEQ_SHIFT2	2	0x0	Shift load bits. 0=Load video serializer every clock, if SEQ_SHIFT4=0 1=Load video serializer every other clock, if SEQ_SHIFT4=0
SEQ_PCLKBY2	3	0x0	Dot Clock (typically, 320 and 360 horizontal modes use divide-by-2 to provide 40 column displays. To change this bit SEQ00[0:0] must be first set to zero.)). 0=Dot clock is normal 1=Dot clock is divided by 2
SEQ_SHIFT4	4	0x0	Shift load bits. 0=SEQ_SHIFT2 determines serializer loading 1=Load video serializer every fourth clock. Ignore SEQ_SHIFT2
SEQ_MAXBW	5	0x1	Screen off: 0=Normal. Screen on 1=Sreen off and blanked. CPU has uninterrupted access to frame buffer

Clock Mode Register

SEQ02 - RW - 8 bits - VGASEQIND:0x2			
Field Name	**Bits**	**Default**	**Description**
SEQ_MAP0_EN	0	0x0	Enable map 0 0=Disable write to memory map 0 1=Enable write to memory map 0
SEQ_MAP1_EN	1	0x0	Enable map 1 0=Disable write to memory map 1 1=Enable write to memory map 1
SEQ_MAP2_EN	2	0x0	Enable map 2 0=Disable write to memory map 2 1=Enable write to memory map 2
SEQ_MAP3_EN	3	0x0	Enable map 3 0=Disable write to memory map 3 1=Enable write to memory map 3

Map Mask Register

SEQ03 - RW - 8 bits - VGASEQIND:0x3			
Field Name	**Bits**	**Default**	**Description**
SEQ_FONT_B1	0	0x0	Character Map Select B Bit 1
SEQ_FONT_B2	1	0x0	Character Map Select B Bit 2
SEQ_FONT_A1	2	0x0	Character Map Select A Bit 1
SEQ_FONT_A2	3	0x0	Character Map Select A Bit 2
SEQ_FONT_B0	4	0x0	Character Map Select B Bit 0
SEQ_FONT_A0	5	0x0	Character Map Select A Bit 0

Character Map Select Register

SEQ04 - RW - 8 bits - VGASEQIND:0x4			
Field Name	**Bits**	**Default**	**Description**
SEQ_256K	1	0x0	Extended memory - 1 indicates 256 KB of video memory is present. It also enables the character map selection in SEQ03. 0=64KB memory present. Has no effect since 256KB always available 1=256KB memory present
SEQ_ODDEVEN	2	0x0	Odd/Even 0=Even CPU address (A0=0) accesses maps 0 and 2. Odd address accesses maps 1 and 3 1=Enables sequential access to maps for odd/even modes. SEQ02 (Map Mask) selects which maps are used
SEQ_CHAIN	3	0x0	Chain (when logical 1, it takes priority over off/even mode bits SEQ04[2] and GRA05[4]. Unlike odd/even mode, SEQ04[2] is the only bit used to enable chain mode (double odd/even). Chain does not affect CRTC access to video memory. Odd/even bit SEQ04[2] should be the opposite of GRA05[4]. 0=Enables sequential access to maps. SEQ02 (Map Mask) selects which maps are used 1=For 256 color modes. Map select by CPU address bits A1:A0

Memory Mode Register

SEQ8_IDX - RW - 8 bits - DISPDEC:0x3C4			
Field Name	**Bits**	**Default**	**Description**
SEQ_IDX	2:0	0x0	This index points to one of the sequencer registers (SEQ_) at I/O port address 0x3C5, for the next SEQ read/write operation.

SEQ Index Register

SEQ8_DATA - RW - 8 bits - DISPDEC:0x3C5			
Field Name	**Bits**	**Default**	**Description**
SEQ_DATA	7:0	0x0	SEQ data indirect access

SEQ Data Register

2.6.4 VGA CRT Registers

CRTC8_IDX - RW - 8 bits - [DISPDEC:0x3B4] [DISPDEC:0x3D4]			
Field Name	**Bits**	**Default**	**Description**
VCRTC_IDX (mirror bits 0:5 of CRTC_EXT_CNTL:VCRTC_IDX_MASTER)	5:0	0x0	This index points to one of the internal registers of the CRT controller (CRTC) at address 0x3?5, for the next CRTC read/write operation.

CRT Index Register

CRTC8_DATA - RW - 8 bits - [DISPDEC:0x3B5] [DISPDEC:0x3D5]			
Field Name	**Bits**	**Default**	**Description**
VCRTC_DATA	7:0	0x0	CRTC data indirect access

CTRC Data Register

CRT00 - RW - 8 bits - VGACRTIND:0x0			
Field Name	**Bits**	**Default**	**Description**
H_TOTAL	7:0	0x0	These bits define the active horizontal display in a scan line, including the retrace period. The value is five less than the total number of displayed characters in a scan line.

Horizontal Total Register

CRT01 - RW - 8 bits - VGACRTIND:0x1			
Field Name	**Bits**	**Default**	**Description**
H_DISP_END	7:0	0x0	These bits define the active horizontal display in a scan line. The value is one less than the total number of displayed characters in a scan line.

Horizontal Display Enable End Register

CRT02 - RW - 8 bits - VGACRTIND:0x2			
Field Name	**Bits**	**Default**	**Description**
H_BLANK_START	7:0	0x0	These bits define the horizontal character count that represents the character count in the active display area plus the right border. In other words, the count is from the start of active display to the start of triggering of the H blanking pulse.

Start Horizontal Blanking Register

CRT03 - RW - 8 bits - VGACRTIND:0x3			
Field Name	**Bits**	**Default**	**Description**
H_BLANK_END	4:0	0x0	H blanking bits 4-0 respectively. These are the five low-order bits (of six bits in total) of horizontal character count for triggering the end of the horizontal blanking pulse.

H_DE_SKEW	6:5	0x0	Display-enable skew: 0=0Skew 1=1Skew 2=2Skew 3=3Skew
CR10CR11_R_DIS_B	7	0x0	Compatibility Read: 0=WrtOnlyToCRT10-11 1=WrtRdToCRT10-11

End Horizontal Blanking Register

CRT04 - RW - 8 bits - VGACRTIND:0x4			
Field Name	**Bits**	**Default**	**Description**
H_SYNC_START	7:0	0x0	These bits define the horizontal character count at which the horizontal retrace pulse becomes active.

Start Horizontal Retrace Register

CRT05 - RW - 8 bits - VGACRTIND:0x5			
Field Name	**Bits**	**Default**	**Description**
H_SYNC_END	4:0	0x0	H Retrace Bits (these are the 5-bit result from the sum of CRT0 plus the width of the horizontal retrace pulse, in character clock units).
H_SYNC_SKEW	6:5	0x0	H Retrace Delay bits (these two bits skew the horizontal retrace pulse).
H_BLANK_END_B5	7	0x0	H blocking end bit 5 (this is the bit of the 6-bit character count for the H blanking end pulse). The other five low-order bits are CRT03[4:0].

End Horizontal Retrace Register

CRT06 - RW - 8 bits - VGACRTIND:0x6			
Field Name	**Bits**	**Default**	**Description**
V_TOTAL	7:0	0x0	These are the eight low-order bits of the 10-bit vertical total register. The 2 high-order bits are CRT07[5:0] in the CRTC overflow register. The value of this register represents the total number of H raster scans plus vertical retrace (active display, blanking), minus two scan lines.

Vertical Total Register

CRT07 - RW - 8 bits - VGACRTIND:0x7			
Field Name	**Bits**	**Default**	**Description**
V_TOTAL_B8	0	0x0	V Total Bit 8 (CRT06). Bit 8 of 10 bit vertical count for V Total. For functional description see CRT06 register.
V_DISP_END_B8	1	0x0	End V Display Bit 8 (CRT12). Bit 8 of 10-bit vertical count for V Display enable. For functional description see CRT12 register.
V_SYNC_START_B8	2	0x0	Start V Retrace Bit 8 (CRT10). Bit 8 of 10-bit varietal count for V Retrace start. For functional description see CRT10 register.
V_BLANK_START_B8	3	0x0	Start V Blanking Bit 8 (CRT15). Bit 8 of the 10-bit vertical count for V Blanking start. For functional description see CRT15 register.
LINE_CMP_B8	4	0x0	Line compare bit 8 (CRT18). Bit 8 of the 10-bit vertical count for line compare. For functional description see CRT18 register.
V_TOTAL_B9	5	0x0	V Total Bit 9 (CRT06). Bit 9 of 10-bit vertical count for V Total. For functional description see CRT06 register.
V_DISP_END_B9	6	0x0	End V Display Bit 9 (CRT12). Bit 9 of 10-bit vertical count for V Display enable end (for functional description see CRT12 register).

V_SYNC_START_B9	7	0x0	Start V Retrace Bit (CRT10). Bit 9 of 10-bit vertical count for V Retrace start. For functional description see CRT10 register.

CRTC Overflow Register

CRT08 - RW - 8 bits - VGACRTIND:0x8			
Field Name	**Bits**	**Default**	**Description**
ROW_SCAN_START	4:0	0x0	Preset row scan bit 4:0. This register is used for software-controlled vertical scrolling in text or graphics modes. The value specifies the first line to be scanned after a V retrace (in the next frame). Each H Retrace pulse increments the counter by 1, up to the maximum scan line value programmed by CRT09, then the counter is cleared.
BYTE_PAN	6:5	0x0	Byte panning control bits 1 and 0 (respectively). Bits 6 and 5 extend the capability of byte panning (shifting) by up to three characters (for description H_PEL Panning register ATTR13).

Preset Row Scan Register

CRT09 - RW - 8 bits - VGACRTIND:0x9			
Field Name	**Bits**	**Default**	**Description**
MAX_ROW_SCAN	4:0	0x0	Maximum scan line bits. These bits define a value that is the actual number of scan line per character minus 1.
V_BLANK_START_B9	5	0x0	Start V Blanking bit 9 (CRT15). Bit 9 of 10-bit vertical count for line compare. For functional description see CRT18 register.
LINE_CMP_B9	6	0x0	Line Compare Bit 9 (CRT18). Bit 9 of 10-bit vertical count for line compare. For functional description see CRT18 register.
DOUBLE_CHAR_HEIGHT	7	0x0	200/400 line scan. NOTE H/V display and blanking timings etc. (in CRT00-CRT06 registers) are not affected. 0=200LineScan 1=400LineScan

Maximum Scan Line Register

CRT0A - RW - 8 bits - VGACRTIND:0xA			
Field Name	**Bits**	**Default**	**Description**
CURSOR_START	4:0	0x0	Cursor start bits 4:0 (respectively). These bits define a value that is the starting scan line (on a character row) for the line cursor. The 5-bit value is equal to the actual number minus one. This value is used together with the Cursor End Bits CRT0B[4:0] to determine the height of the cursor. The cursor height in VGA does not wrap around (as in EGA) and is actually absent when the 'end' value is less than the 'start' value. In EGA when the 'end' value is less, the cursor is a full block cursor the same height as the character cell.
CURSOR_DISABLE	5	0x0	Cursor on/off. 0=on 1=off

Cursor Start Register

CRT0B - RW - 8 bits - VGACRTIND:0xB			
Field Name	**Bits**	**Default**	**Description**
CURSOR_END	4:0	0x0	Cursor End Bits 4-0, respectively.- These bits define the ending scan row (on a character line) for the line cursor. In EGA, this 5-bit value is equal to the actual number of lines plus one.- The cursor height in VGA does not wrap around (as in EGA) and is actually absent when the 'end' value is less than the 'start' value. In EGA when the 'end' value is less, the cursor is a full block cursor the same height as the character cell.
CURSOR_SKEW	6:5	0x0	Cursor Skew Bits 1 and 0, respectively.- These bits define the number of characters the cursor is to be shifted to the right (skewed) from the character pointed at by the cursor location (registers CRT0E and CRT0F), in VGA mode. Skew values when in EGA mode are enclosed in brackets.

Cursor End Register

CRT0C - RW - 8 bits - VGACRTIND:0xC			
Field Name	**Bits**	**Default**	**Description**
DISP_START	7:0	0x0	SA bits 15:8-These are the eight high-order bits of the 16-bit display buffer start location. The low order bits are contained in CRT0D.-In split screen mode, CRT0C = CRT0D point to the starting location of screen A (top half.) The starting address for screen B is always zero.

Start Address (High Byte) Register

CRT0D - RW - 8 bits - VGACRTIND:0xD			
Field Name	**Bits**	**Default**	**Description**
DISP_START	7:0	0x0	SA bits 7:0- These are the eight low-order bits of the 16-bit display buffer start location. The high-order bits are contained in CRT0C. - In split screen mode, CRT0C + CRT0D points to the starting location of screen A (top half.) The starting address for screen B is always zero.

Start Address (Low Byte) Register

CRT0E - RW - 8 bits - VGACRTIND:0xE			
Field Name	**Bits**	**Default**	**Description**
CURSOR_LOC_HI	7:0	0x0	CA bits 15:8- These are the eight high-order bits of the 16 bit cursor start address. The low-order CA bits are contained in CRT0F. This address is relative to the start of physical display memory address pointed to by CRT0C + CRT0D. In other words, if CRT0C + CRT0D is changed, the cursor still pints to the same character as before.

Cursor Location (High Byte) Register

CRT0F - RW - 8 bits - VGACRTIND:0xF			
Field Name	**Bits**	**Default**	**Description**
CURSOR_LOC_LO	7:0	0x0	CA bits 7:0- These are the eight low-order bits of the 16 bit cursor start address. The high-order CA bits are contained in CRT0E. This address is relative to the start of physical display memory address pointed to by CRT0C + CRT0D. In other words, if CRT0C + T0D is changed, the cursor still points to the same character as before

Cursor Location (Low Byte) Register

CRT10 - RW - 8 bits - VGACRTIND:0x10			
Field Name	**Bits**	**Default**	**Description**
V_SYNC_START	7:0	0x0	Bits CRT10[7:0] are the eight low-order bits of the 10-bit vertical retrace start count. The two high-order bits are CRTt07[2:7], located in the CRTC overflow register.- These bits define the horizontal scan count that triggers the V retrace pulse.

Start Vertical Retrace Register

CRT11 - RW - 8 bits - VGACRTIND:0x11			
Field Name	**Bits**	**Default**	**Description**
V_SYNC_END	3:0	0x0	V Retrace End Bits 3-0- Bits CRT11[0:3] define the horizontal scan count that triggers the end of the V Retrace pulse.
V_INTR_CLR	4	0x0	V Retrace Interrupt Set: 0=VRetraceIntCleared 1=Not Cleared
V_INTR_EN	5	0x0	V Retrace Interrupt Disabled: 0=VRetraceIntEna 1=Disable
SEL5_REFRESH_CYC	6	0x0	0=3 DRAM Refresh/Horz Line 1=5 DRAM Refresh/Horz Line
C0T7_WR_ONLY	7	0x0	Write Protect (CRT00-CRT06). All register bits except CRTO7[4] are write protected. 0=EnaWrtToCRT00-07 1=C0T7B4WrtOnly

End Vertical Retrace Register

CRT12 - RW - 8 bits - VGACRTIND:0x12			
Field Name	**Bits**	**Default**	**Description**
V_DISP_END	7:0	0x0	These are the eight low-order bits of the 10-bit register containing the horizontal scan count indicating where the active display on the screen should end. The high-order bits are CRT07 [1:6] in the CRT overflow register.

Vertical Display Enable End Register

CRT13 - RW - 8 bits - VGACRTIND:0x13			
Field Name	**Bits**	**Default**	**Description**
DISP_PITCH	7:0	0x0	- These bits define an offset value, equal to the logical line width of the screen (from the first character of the current line to the first character of the next line).- Memory organization is dependent on the video mode. Bit CRT17[6] selects byte or word mode. Bit CRT14[6], which overrides the byte/word mode setting, selects Double-Word mode when it is logical one.- The first character of the next line is specified by the start address (CRT0C + CRT0D) plus the offset. The offset for byte mode is 2x CRT13; for word mode, 4x; for double word mode 8x.

Offset Register

CRT14 - RW - 8 bits - VGACRTIND:0x14			
Field Name	**Bits**	**Default**	**Description**
UNDRLN_LOC	4:0	0x0	H Row Scan Bits 4-0.- These bits define the horizontal scan row, from the top of the character line, that should be used for underlining. The 5-bit value is equal to the actual number minus one.
ADDR_CNT_BY4	5	0x0	Count-by-4: 0=Char. Clock 1=CountBy4
DOUBLE_WORD	6	0x0	Double-Word Mode: 0=Disable 1=DoubleWordMdEna

Underline Location Register

CRT15 - RW - 8 bits - VGACRTIND:0x15			
Field Name	**Bits**	**Default**	**Description**
V_BLANK_START	7:0	0x0	These are the eight low-order bits of the 10-bit vertical blanking start register. Bit 9 is CRT09[5]; bit 8 is CRT07[3]- The 10 bits specify the starting location of the vertical blanking pulse, in units of horizontal scan lines. The value is equal to the actual number of displayed lines minus one.

Start Vertical Blanking Register

CRT16 - RW - 8 bits - VGACRTIND:0x16			
Field Name	**Bits**	**Default**	**Description**
V_BLANK_END	7:0	0x0	These bits define the point at which to trigger the end of the vertical blanking pulse. The location is specified in units of horizontal scan lines.- The value to be stored in this register is the seven low-order bits of the sum of 'pulse width count' plus the content of Start Vertical Blanking register (CRT15) minus one.

End Vertical Blanking Register

CRT17 - RW - 8 bits - VGACRTIND:0x17			
Field Name	**Bits**	**Default**	**Description**
RA0_AS_A13B	0	0x0	Compatibility Mode:
RA1_AS_A14B	1	0x0	Select Row Scan Counter:

VCOUNT_BY2	2	0x0	Vertical_by_2 NOTE: When bit 2 is logical one, other vertical register values should be adjusted as well (CRT06, CRT10, CRT12, CRT15, and CRT18).
ADDR_CNT_BY2	3	0x0	Count_by_2: ENGINEERING NOTE: Bit can be written and read, but has no effect.
WRAP_A15TOA0	5	0x0	Address Wrap: ENGINEERING NOTE: Bit can be written and read, but has no effect.
BYTE_MODE	6	0x0	Byte/Word Mode: 0=WordMode 1=ByteMode
CRTC_SYNC_EN	7	0x0	H/V Retrace Enable: 0=Disable HVSync 1=EnaHVSync

CRT Mode Register

CRT18 - RW - 8 bits - VGACRTIND:0x18			
Field Name	**Bits**	**Default**	**Description**
LINE_CMP	7:0	0x0	- These bits are the eight low-order of the 10-bit line compare register. Bit 8 is CRT07[4], bit 9 is CRT09[6]. The value of this register is used to disable scrolling on a portion of the display screen, as when split screen is active. When the vertical counter reaches this value, the memory address and row scan counters are cleared.- The screen area above the line specified by the register is commonly called screen A. The screen below is screen B. Screen B cannot be scrolled, but it can panned only together with screen A, controlled by the PEL panning compatibility bit ATTR10[5]. (For a description of this control bit see ATTR10[5].)

Line Compare Register

CRT1E - R - 8 bits - VGACRTIND:0x1E			
Field Name	**Bits**	**Default**	**Description**
GRPH_DEC_RD1	1	0x0	This register is used to read back the graphics controller index decode.

Graphics Controller Index Decode Register

CRT1F - R - 8 bits - VGACRTIND:0x1F			
Field Name	**Bits**	**Default**	**Description**
GRPH_DEC_RD0	7:0	0x0	This register is used to read back the graphics controller index decode.

Graphics Controller Index Decode Register

CRT22 - R - 8 bits - VGACRTIND:0x22			
Field Name	**Bits**	**Default**	**Description**
GRPH_LATCH_DATA	7:0	0x0	This register is used to read the data in the Graphics Controller CPU data latches. The Graphics Controller Read Map Select register bits 0 and 1 determines which byte is read back.

RAM Data Latch Readback Register

2.6.5 VGA Graphics Registers

VGA Graphics Registers

GRPH8_IDX - RW - 8 bits - DISPDEC:0x3CE			
Field Name	**Bits**	**Default**	**Description**
GRPH_IDX	3:0	0x0	VGA graphics index as per VGA specified by IBM

GRPH Index Register

GRPH8_DATA - RW - 8 bits - DISPDEC:0x3CF			
Field Name	**Bits**	**Default**	**Description**
GRPH_DATA	7:0	0x0	GRPH data indirect access

GRPH Data Register

GRA00 - RW - 8 bits - VGAGRPHIND:0x0			
Field Name	**Bits**	**Default**	**Description**
GRPH_SET_RESET0	0	0x0	Set/Reset Map 0
GRPH_SET_RESET1	1	0x0	Set/Reset Map 1
GRPH_SET_RESET2	2	0x0	Set/Reset Map 2
GRPH_SET_RESET3	3	0x0	Set/Reset Map 3

Set/Reset Register

GRA01 - RW - 8 bits - VGAGRPHIND:0x1			
Field Name	**Bits**	**Default**	**Description**
GRPH_SET_RESET_ENA0	0	0x0	Enable Set/Reset Map 0
GRPH_SET_RESET_ENA1	1	0x0	Enable Set/Reset Map 1
GRPH_SET_RESET_ENA2	2	0x0	Enable Set/Reset Map 2
GRPH_SET_RESET_ENA3	3	0x0	Enable Set/Reset Map 3

Enable Set/Reset Register

GRA02 - RW - 8 bits - VGAGRPHIND:0x2			
Field Name	**Bits**	**Default**	**Description**
GRPH_CCOMP	3:0	0x0	Colour Compare Map bits 3:0. In Read mode (GRA05[3] being logical 1), the 4 bits from this register are compared with the 4-bit PEL value (made up of one bit from each map), from bit positions 0 through 7. As long as the colour don't care bits (GRA07[0:3]) for the respective maps are logical 1's, the compare takes place only on those bits of the PEL value, and the CPU reads a one for a match in that bit position. If Colour Don't Care bit for one map is a logical zero, the latched data from the map is excluded from the compare, and only the remaining three bits are compared to generate bus data.

Colour Compare Register

GRA03 - RW - 8 bits - VGAGRPHIND:0x3			
Field Name	**Bits**	**Default**	**Description**
GRPH_ROTATE	2:0	0x0	Rotate Count Bits 2-0. Specifies the number of bit positions that the CPU data is to be rotated to the right, before doing the function selected by bits 3 and 4 above and subsequent bit mask select and write operations. Rotation is carried out only in write modes 0 and 3. In these two modes, the CPU data is rotated first, the operated only the function bits GRA03[4:3], the updated by the bit mask register GRA05.
GRPH_FN_SEL	4:3	0x0	Function Select Bits 1 and 2. These functions are performed on the CPU data before the selected bits are updated by the bit mask register, and then written to the display buffers. 0=Replace 1=AND 2=OR 3=XOR

Data Rotate Register

GRA04 - RW - 8 bits - VGAGRPHIND:0x4			
Field Name	**Bits**	**Default**	**Description**
GRPH_RMAP	1:0	0x0	Read Mode 0 Only: GRA controller returns the contents of one of the four latched buffer bytes to CPU each time a CPU read loads these latches. The 2 bits (0 and 1) define a value that represents the bit map where CPU is to read data - useful in transferring bit map data between the maps and system RAM.

Read Map Select Register

GRA05 - RW - 8 bits - VGAGRPHIND:0x5			
Field Name	**Bits**	**Default**	**Description**
GRPH_WRITE_MODE	1:0	0x0	Write Mode: 0=Write mode 0 1=Write mode 1 2=Write mode 2 3=Write mode 3
GRPH_READ1	3	0x0	Read Mode: 0=Read mode 0, byte oriented 1=Read mode 1, pixel oriented
CGA_ODDEVEN	4	0x0	Odd/Even Addressing Enable. Used to enable CGA emulation, this bit enables off/even addressing mode when it is logical one. Normally, this bit and memory mode bit SEQ04[2] are set to agree with each other in enabling odd/even mode emulation. 0=Disable Odd/Even Addressing 1=Enable Odd/Even Addressing
GRPH_OES	5	0x0	Shift Register Mode: This bit controls how data from memory is loaded into the shift registers M0D0:M0D7, M1D0:M1D7; M2D0:M2D7, and M3D0:M3D7 are representations of this data. 0=Linear shift mode 1=Tiled shift mode
GRPH_PACK	6	0x0	256 Colour Mode. This bit also controls how data from memory is loaded into the shift registers. 0=Use shift register mode as per GRPH_OES 1=256 color mode, read as packed pixels, ignore GRPH_OES

Graphics Mode Register

GRA06 - RW - 8 bits - VGAGRPHIND:0x6			
Field Name	**Bits**	**Default**	**Description**
GRPH_GRAPHICS	0	0x0	Graphics/Alphanumeric Mode 0=Alpha Numeric Mode 1=Graphics Mode
GRPH_ODDEVEN	1	0x0	Chains Odd Maps to Even 0=Normal 1=Chain Odd maps to Even
GRPH_ADRSEL	3:2	0x0	Memory Map Read Bits 1 and 0, respectively. 0=A0000-128K 1=A0000-64K 2=B0000-32K 3=B8000-32K

Graphics Miscellaneous Register

GRA07 - RW - 8 bits - VGAGRPHIND:0x7			
Field Name	**Bits**	**Default**	**Description**
GRPH_XCARE0	0	0x0	Ignore Map 0 0=Ignore map 0 1=Use map 0 for read mode 1
GRPH_XCARE1	1	0x0	Ignore Map 1 0=Ignore map 1 1=Use map 1 for read mode 1
GRPH_XCARE2	2	0x0	Ignore Map 2 0=Ignore map 2 1=Use map 2 for read mode 1
GRPH_XCARE3	3	0x0	Ignore Map 3 0=Ignore map 3 1=Use map 3 for read mode 1

Colour Don't Care Register

GRA08 - RW - 8 bits - VGAGRPHIND:0x8			
Field Name	**Bits**	**Default**	**Description**
GRPH_BMSK	7:0	0x0	Bit Mask

Bit Mask Register

2.6.6 VGA Attribute Registers

ATTRX - RW - 8 bits - DISPDEC:0x3C0			
Field Name	**Bits**	**Default**	**Description**
ATTR_IDX	4:0	0x0	ATTR Index. This index points to one of the internal registers of the attribute controller (ATTR) at addresses 0x3C1/0x3C0, for the next ATTR read/write operation. Since both the index and data registers are at the same I/O, a pointer to the registers is necessary. This pointer can be initialized to point to the index register by a read of GENS1.
ATTR_PAL_RW_ENB	5	0x0	Palette Address Source. After loading the colour palette, this bit should be set to logical 1. 0=Processor to load 1=Memory data to access

Attribute Index Register

ATTRDW - W - 8 bits - DISPDEC:0x3C0			
Field Name	**Bits**	**Default**	**Description**
ATTR_DATA	7:0	0x0	Attribute Data Write

Attribute Data Write Register

ATTRDR - R - 8 bits - DISPDEC:0x3C1			
Field Name	**Bits**	**Default**	**Description**
ATTR_DATA	7:0	0x0	Attribute Data Read

Attribute Data Read Register

ATTR00 - RW - 8 bits - VGAATTRIND:0x0			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 0

ATTR01 - RW - 8 bits - VGAATTRIND:0x1			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 1

ATTR02 - RW - 8 bits - VGAATTRIND:0x2			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 2

ATTR03 - RW - 8 bits - VGAATTRIND:0x3			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 3

ATTR04 - RW - 8 bits - VGAATTRIND:0x4			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 4

ATTR05 - RW - 8 bits - VGAATTRIND:0x5			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 5

ATTR06 - RW - 8 bits - VGAATTRIND:0x6			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 6

ATTR07 - RW - 8 bits - VGAATTRIND:0x7			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 7

ATTR08 - RW - 8 bits - VGAATTRIND:0x8

Field Name	Bits	Default	Description
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 8

ATTR09 - RW - 8 bits - VGAATTRIND:0x9			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register 9

ATTR0A - RW - 8 bits - VGAATTRIND:0xA			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register Ah (10)

ATTR0B - RW - 8 bits - VGAATTRIND:0xB			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register Bh (11)

ATTR0C - RW - 8 bits - VGAATTRIND:0xC			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register Ch (12)

ATTR0D - RW - 8 bits - VGAATTRIND:0xD			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register Dh (13)

ATTR0E - RW - 8 bits - VGAATTRIND:0xE			
Field Name	**Bits**	**Default**	**Description**

ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register Eh (14)

ATTR0F - RW - 8 bits - VGAATTRIND:0xF			
Field Name	**Bits**	**Default**	**Description**
ATTR_PAL	5:0	0x0	Colour Bits 5:0 map the text attribute or graphics colour input value to a display colour on the screen. Colour is disabled for those bits that are set to logical 0; enabled for those bits set to logical 1.

Palette Register Fh (15)

ATTR10 - RW - 8 bits - VGAATTRIND:0x10			
Field Name	**Bits**	**Default**	**Description**
ATTR_GRPH_MODE	0	0x0	Graphics/Alphanumeric Mode. 0=Alphanumeric Mode 1=Graphic Mode
ATTR_MONO_EN	1	0x0	Monochrome/Colour Attributes Select: 0=Color Disp 1=Monochrome Disp
ATTR_LGRPH_EN	2	0x0	Line Graphics Enable. Must be 0 for character fonts that do not use line graphics character codes for graphics. Zero will force the 9th dot to the background colour. One will allow the 8th bit of the line graphics characters to be stretched to the 9th dot. 0=Disable line graphics 8th dot stretch 1=Enable line graphics 8th dot stretch
ATTR_BLINK_EN	3	0x0	Blink Enable/Background Intensity: Selects whether bit 7 of the attribute controls intensity or blinking. 0=Intensity control 1=Blink control
ATTR_PANTOPONLY	5	0x0	PEL Panning Compatibility: 0=Pan both halves of the screen 1=Pan only the top half screen
ATTR_PCLKBY2	6	0x0	PEL Clock Select: 0=Shift register clocked every dot clock 1=For mode 13 (256 colour), 8 bits packed to form a pixel
ATTR_CSEL_EN	7	0x0	Alternate Colour Source: 0=Select ATTR00-0F bit 5:4 as P5 and P4 1=Select ATTR14 bit 1:0 as P5 and P4

Mode Control Register

ATTR11 - RW - 8 bits - VGAATTRIND:0x11			
Field Name	**Bits**	**Default**	**Description**
ATTR_OVSC	7:0	0x0	Overscan Colour

Overscan Colour Register

ATTR12 - RW - 8 bits - VGAATTRIND:0x12			
Field Name	**Bits**	**Default**	**Description**

ATTR_MAP_EN	3:0	0x0	Enable Colour Map bits. 0 = Disables data from respective map from being used for video output. 1 = Enables data from respective map for use in video output.
ATTR_VSMUX	5:4	0x0	Video Status Mux bits 1:0. These are control bits for the multiplexer on colour bits P0-P7. The bit selection is also indicated at GENS1[5:4]: 00 = P2, P0 01 = P5, P4 10 = P3, P1 11 = P7, P6

Colour Map Enable Register

ATTR13 - RW - 8 bits - VGAATTRIND:0x13			
Field Name	**Bits**	**Default**	**Description**
ATTR_PPAN	3:0	0x0	Shift Count Bits 3:0. The shift count value (0-8) indicates how many pixel positions to shift left. Shift in respective modes Count 0+,1+,2+, 13 All other Value 3+,7,7+ 0 1 0 0 1 2 - 1 2 3 1 2 3 4 - 3 4 5 2 4 5 6 - 5 6 7 3 6 7 8 - 7 8 0 - -

Horizontal PEL Panning Register

ATTR14 - RW - 8 bits - VGAATTRIND:0x14			
Field Name	**Bits**	**Default**	**Description**
ATTR_CSEL1	1:0	0x0	Colour bits P5 and P4, respectively. These are the colour output bits (instead of bits 5 and 4 of the internal palette registers ATTR00-0F) when alternate colour source, bit ATTR10[7] is logical 1.
ATTR_CSEL2	3:2	0x0	Colour bits P7 and P6, respectively. These two bits are the two high-order bits of the 8-bit colour, used for rapid colour set switching (addressing different parts of the DAC colour lookup table). The lower order bits are in registers ATTR00-0F.

Colour Select Register

2.6.7 VGA Miscellaneous Registers

VGA_RENDER_CONTROL - RW - 32 bits - DISPDEC:0x300			
Field Name	**Bits**	**Default**	**Description**
VGA_BLINK_RATE	4:0	0xf	One less than the number of frames that the cursor remains OFF = one less than the number of frames that the cursor remains ON = one less than half the cursor blink period = one less than a quarter of the character blink period. If register set to 0 test mode will happen, blink counter is reset and VGA_BLINK_MODE is followed, if set to 1, as an exception, cursor blink will be ON one frame, OFF one frame, if set to 2, cursor blink will be ON three frames, OFF three frames, etc
VGA_BLINK_MODE	6:5	0x0	Determines whether the blinking sequence starts with blinking characters and cursor visible or invisible. If VGA_BLINK_RATE = 0 the frame remains static at the start of the sequence. 0=Blinking sequence starts with blinking characters visible and cursor visible 1=Blinking sequence starts with blinking characters visible and cursor invisible 2=Blinking sequence starts with blinking characters invisible and cursor visible 3=Blinking sequence starts with blinking characters invisible and cursor invisible
VGA_CURSOR_BLINK_INVERT	7	0x0	Determines if the blinking characters toggle when the cursor toggles from invisible to visible (default) or when the cursor toggles from visible to invisible 0=Sequence is (regardless of where it starts) : blinking chars visible and cursor visible, blinking chars visible and cursor invisible, blinking chars invisible and cursor visible, blinking chars invisible and cursor invisible, blinking chars visible and cursor visible,... etc. The starting point in the sequence is determined by VGA_BLINK_MODE 1=Sequence is (regardless of where it starts): blinking chars visible and cursor visible, blinking chars invisible and cursor invisible, blinking chars invisible and cursor visible, blinking chars visible and cursor invisible, blinking chars visible and cursor visible,... etc. The starting point in the sequence is determined by VGA_BLINK_MODE
VGA_EXTD_ADDR_COUNT_ENABLE	8	0x0	Determines if the render will allow reading beyond 256K 0=Disable 1=Enable Extended Address Counter beyond 256K
VGA_VSTATUS_CNTL	17:16	0x0	controls the main state machine of the VGA render 0=VGA render disable (no VGA engine trigger enabled) 1=Use CRTC1 vblank to trigger VGA engine 2=Use CRTC2 vblank to trigger VGA engine 3=Use both CRTC1 and CRTC2 vblank to trigger VGA engine
VGA_LOCK_8DOT	24	0x0	Determines if 9 dot text characters will be allowed or not 0=respect SEQ_DOT8 value 1=Force SEQ_DOT8 =1, VGA_CKSEL = 0 for functionality
VGAREG_LINECMP_COMPATIBILITY_SEL	25	0x0	Selects point at which line compare is activated 0=line==line_cmp(default). As per VGA specification 1=line>line_cmp. As per legacy ATI VGA controllers

VGA Render control Register

VGA_SEQUENCER_RESET_CONTROL - RW - 32 bits - DISPDEC:0x304			
Field Name	**Bits**	**Default**	**Description**
D1_BLANK_DISPLAY_WHEN_SEQUENCER_RESET	0	0x1	controls whether to blank the display 1 in a sequencer reset 0=Reseting Sequencer (SEQ00:SEQ_RST) has no effect on Display Controller 1 1=Reseting Sequencer (SEQ00:SEQ_RST) blanks the output of Display Controller 1
D2_BLANK_DISPLAY_WHEN_SEQUENCER_RESET	4	0x1	controls whether to blank the display 1 in a sequencer reset 0=Reseting Sequencer (SEQ00:SEQ_RST) has no effect on Display Controller 2 1=Reseting Sequencer (SEQ00:SEQ_RST) blanks the output of Display Controller 2
D1_DISABLE_SYNCS_AND_DE_WHEN_SEQUENCER_RESET	8	0x1	controls whether to disable syncs for display 1 in a sequencer reset 0=Reseting Sequencer (SEQ00:SEQ_RST) has no effect on Display Controller 1 1=Reseting Sequencer (SEQ00:SEQ_RST) disables HSync, VSync, and DE on Display Controller 2
D2_DISABLE_SYNCS_AND_DE_WHEN_SEQUENCER_RESET	12	0x1	controls whether to disable syncs for display 2 in a sequencer reset 0=Reseting Sequencer (SEQ00:SEQ_RST) has no effect on Display Controller 2 1=Reseting Sequencer (SEQ00:SEQ_RST) disables HSync, VSync, and DE on Display Controller 2
VGA_MODE_AUTO_TRIGGER_ENABLE	16	0x0	enables the auto-trigger of the VGA mode in a VGA register write 0=disable the auto-trigger mode 1=enable the auto-trigger mode
VGA_MODE_AUTO_TRIGGER_REGISTER_SELECT	17	0x0	selects which register write to use for VGA mode auto-trigger 0=GENFC_WT is used for auto-trigger 1=CRTC_DATA is used for auto-trigger, see VGA_MODE_ENABLE_AUTO_TRIGGER_INDEX_SELECT
VGA_MODE_AUTO_TRIGGER_INDEX_SELECT	23:18	0x0	Selects which CRTC register write will trigger VGA mode

VGA sequencer reset control Register

VGA_MODE_CONTROL - RW - 32 bits - DISPDEC:0x308			
Field Name	**Bits**	**Default**	**Description**
VGA_ATI_LINEAR	0	0x0	Sets linear mode for VESA modes 0=Disable 1=Enable
VGA_128K_APERTURE_PAGING	8	0x0	Controls wether the B0000 to BFFFF aperture will wrap on top of the A0000 to AFFFF aperture 0=Normal 1=Enable
VGA_TEXT_132_COLUMNS_EN	16	0x0	Controls 132 column text 0=inActive 1=Active

VGA mode control register

VGA_SURFACE_PITCH_SELECT - RW - 32 bits - DISPDEC:0x30C			
Field Name	**Bits**	**Default**	**Description**
VGA_SURFACE_PITCH_SELECT	1:0	0x2	Selects the pitch of the display buffer 0=768 pixels 1=1024 pixels 2=1280 pixels 3=1408 pixels

VGA_SURFACE_HEIGHT_SELECT	9:8	0x0	Selects the height of the display buffer 0=768 lines 1=1024 lines 2=1280 lines 3=1408 lines

display buffer pitch Register

VGA_MEMORY_BASE_ADDRESS - RW - 32 bits - DISPDEC:0x310			
Field Name	**Bits**	**Default**	**Description**
VGA_MEMORY_BASE_ADDRESS	31:0	0x0	Base address of the 32 Meg area that the VGAHDP and VGARENDER access NOTE: Bits 0:24 of this field are hardwired to ZERO.

VGA Base address Register

VGA_DISPBUF1_SURFACE_ADDR - RW - 32 bits - DISPDEC:0x318			
Field Name	**Bits**	**Default**	**Description**
VGA_DISPBUF1_SURFACE_ADDR	24:0	0x0	Base address of display 1 buffer within the 32 Meg defined by VGA_MEMORY_BASE_ADDRESS NOTE: Bits 0:19 of this field are hardwired to ZERO.

display 1 buffer base address

VGA_DISPBUF2_SURFACE_ADDR - RW - 32 bits - DISPDEC:0x320			
Field Name	**Bits**	**Default**	**Description**
VGA_DISPBUF2_SURFACE_ADDR	24:0	0x0	Base address of display 2 buffer within the 32 Meg defined by VGA_MEMORY_BASE_ADDRESS NOTE: Bits 0:19 of this field are hardwired to ZERO.

display 2 buffer base address

VGA_HDP_CONTROL - RW - 32 bits - DISPDEC:0x328			
Field Name	**Bits**	**Default**	**Description**
VGA_MEM_PAGE_SELECT_EN	0	0x0	Enables write and read paging 0=Don't use VGA_MEM_WRITE_PAGE_ADDR and VGA_MEM_READ_PAGE_ADDR registers 1=Use VGA_MEM_WRITE_PAGE_ADDR and VGA_MEM_READPAGE_ADDR registers
VGA_RBBM_LOCK_DISABLE	8	0x0	Disables the lock that holds register writes while the memory pipe is full 0=The RBBM write requests will be held until the data pipe is idle. 1=The RBBM write requests will not be held.
VGA_SOFT_RESET	16	0x0	Does soft reset for VGA, does not reset the registers 0=VGA running in normal operating mode 1=Soft Reset to VGA
VGA_TEST_RESET_CONTROL	24	0x0	Not used

VGAHDP control register

VGA_CACHE_CONTROL - RW - 32 bits - DISPDEC:0x32C

Field Name	Bits	Default	Description
VGA_WRITE_THROUGH_CACHE_DIS	0	0x0	Disables the snooping of memory writes into the read buffer 0=Writes that hit the read cache will update it 1=Writes will invalidate the read cache
VGA_READ_CACHE_DISABLE	8	0x0	Disables the read buffer 0=reads taken from cache, if possible. 1=reads always sent to memory.
VGA_READ_BUFFER_INVALIDATE	16	0x0	Every time this bit is written with a '1' the VGA read buffer invalidates for coherency purposes
VGA_DCCIF_W256ONLY	20	0x0	Controls whether the write requests from VGADCC to MH will be always 256 bits or optimized for 128 or 256 bit 0=Optimized for 128 or 256 bits 1=Always 256 bits
VGA_DCCIF_WC_TIMEOUT	29:24	0x0	DCCIF write combiner timeout. If there is write inactivity, this field defines the number of SCLKs to wait before flushing write combiner. Minimum value is 9.

VGAHDP caching and VGADCCIF write combining control register

D1VGA_CONTROL - RW - 32 bits - DISPDEC:0x330			
Field Name	**Bits**	**Default**	**Description**
D1VGA_MODE_ENABLE	0	0x0	Controls whether display 1 serves the VGA or not 0=VGA display 1 disabled 1=VGA display 1 enabled
D1VGA_TIMING_SELECT	8	0x0	Controls whether display 1 uses the VGA or extended timing parameters 0=display 1 uses extended timing 1=display 1 uses VGA timing
D1VGA_SYNC_POLARITY_SELECT	9	0x0	Controls whether display 1 uses the VGA or extended sync polarities 0=display 1 uses extended sync polarity 1=display 1 uses VGA sync polarity
D1VGA_OVERSCAN_TIMING_SELECT	10	0x1	Controls whether display 1 uses the VGA or extended overscan timing. Only followed if D1VGA_TIMING_SELECT=1 0=display 1 uses extended overscan timing 1=display 1 uses VGA overscan timing
D1VGA_OVERSCAN_COLOR_EN	16	0x0	Controls whether display 1 uses the VGA or extended overscan color 0=display 1 uses CRTC register for overscan color 1=display 1 uses VGA register for overscan color
D1VGA_ROTATE	25:24	0x0	Controls rotation, only looked at if D1VGA_TIMING_SELECT =0 0=no rotation, displays do not interchange VGA_DISP_h_disp_width and VGA_DISP_v_disp_height parameters 1=rotation 90 degrees, displays do interchange VGA_DISP_h_disp_width and VGA_DISP_v_disp_height parameters 2=rotation 180 degrees, displays do not interchange VGA_DISP_h_disp_width and VGA_DISP_v_disp_height parameters 3=rotation 270 degrees, displays do interchange VGA_DISP_h_disp_width and VGA_DISP_v_disp_height parameters

VGA-Display1 interface control register

D2VGA_CONTROL - RW - 32 bits - DISPDEC:0x338			
Field Name	**Bits**	**Default**	**Description**
D2VGA_MODE_ENABLE	0	0x0	Controls whether display 2 serves the VGA or not 0=VGA display 2 disabled 1=VGA display 2 enabled
D2VGA_TIMING_SELECT	8	0x0	Controls whether display 2 uses the VGA or extended timing parameters 0=display 2 uses extended timing 1=display 2 uses VGA timing
D2VGA_SYNC_POLARITY_SELECT	9	0x0	Controls whether display 2 uses the VGA or extended sync polarities 0=display 2 uses extended sync polarity 1=display 2 uses VGA sync polarity
D2VGA_OVERSCAN_TIMING_SELECT	10	0x1	Controls whether display 2 uses the VGA or extended overscan timing. Only followed if D2VGA_TIMING_SELECT=1 0=display 2 uses extended overscan timing 1=display 2 uses VGA overscan timing
D2VGA_OVERSCAN_COLOR_EN	16	0x0	Controls whether display 2 uses the VGA or extended overscan color 0=display 2 uses CRTC register for overscan color 1=display 2 uses VGA register for overscan color
D2VGA_ROTATE (mirror of D1VGA_CONTROL:D1VGA_ROTATE)	25:24	0x0	Controls rotation, only looked at if D2VGA_TIMING_SELECT=0 0=no rotation, displays do not interchange VGA_DISP_h_disp_width and VGA_DISP_v_disp_height parameters 1=rotation 90 degrees, displays do interchange VGA_DISP_h_disp_width and VGA_DISP_v_disp_height parameters 2=rotation 180 degrees, displays do not interchange VGA_DISP_h_disp_width and VGA_DISP_v_disp_height parameters 3=rotation 270 degrees, displays do interchange VGA_DISP_h_disp_width and VGA_DISP_v_disp_height parameters

VGA-Display2 interface control register

VGA_STATUS - RW - 32 bits - DISPDEC:0x340			
Field Name	**Bits**	**Default**	**Description**
VGA_MEM_ACCESS_STATUS (R)	0	0x0	Memory access status 0=No event 1=Event has occurred, interrupting if enabled
VGA_REG_ACCESS_STATUS (R)	1	0x0	Register access status 0=No event 1=Event has occurred, interrupting if enabled
VGA_DISPLAY_SWITCH_STATUS (R)	2	0x0	Display switch status 0=No event 1=Event has occurred, interrupting if enabled
VGA_MODE_AUTO_TRIGGER_STATUS (R)	3	0x0	VGA mode auto trigger status 0=No event 1=Event has occurred, interrupting if enabled

VGA status register

VGA_INTERRUPT_CONTROL - RW - 32 bits - DISPDEC:0x344			
Field Name	**Bits**	**Default**	**Description**
VGA_MEM_ACCESS_INT_MASK	0	0x0	Enables the interrupt for the Memory access status 0=Disable the interrupt which is set when VGA memory is written or read 1=Enable the interrupt which is set when VGA memory is written or read
VGA_REG_ACCESS_INT_MASK	8	0x0	Enables the interrupt for the register access status 0=Disable the interrupt which is set when the standard VGA registers are written or read 1=Enable the interrupt which is set when the standard VGA registers are written or read
VGA_DISPLAY_SWITCH_INT_MASK	16	0x0	Enables the interrupt for the Display switch status 0=Disable the interrupt which is set when the VGA render switches display buffers 1=Enable the interrupt which is set when the VGA render switches display buffers
VGA_MODE_AUTO_TRIGGER_INT_MASK	24	0x0	Enables the interrupt for VGA mode auto trigger 0=Disable the interrupt which is set when VGA mode is auto-triggered 1=Enable the interrupt which is set when VGA mode is auto-triggered

VGA interrupt mask register

VGA_STATUS_CLEAR - RW - 32 bits - DISPDEC:0x348			
Field Name	**Bits**	**Default**	**Description**
VGA_MEM_ACCESS_INT_CLEAR (W)	0	0x0	Clears the Memory access interrupt 0=No effect 1=Clear status
VGA_REG_ACCESS_INT_CLEAR (W)	8	0x0	Clears the register access interrupt 0=No effect 1=Clear status
VGA_DISPLAY_SWITCH_INT_CLEAR (W)	16	0x0	Clears the display switch interrupt 0=No effect 1=Clear status
VGA_MODE_AUTO_TRIGGER_INT_CLEAR (W)	24	0x0	Clears the VGA mode auto trigger interrupt 0=No effect 1=Clear status

VGA interrupt clear register

VGA_INTERRUPT_STATUS - RW - 32 bits - DISPDEC:0x34C			
Field Name	**Bits**	**Default**	**Description**
VGA_MEM_ACCESS_INT_STATUS (R)	0	0x0	Memory access interrupt status 0=No event 1=Event has occurred
VGA_REG_ACCESS_INT_STATUS (R)	1	0x0	Register access interrupt status 0=No event 1=Event has occurred
VGA_DISPLAY_SWITCH_INT_STATUS (R)	2	0x0	Display switch interrupt status 0=No event 1=Event has occurred
VGA_MODE_AUTO_TRIGGER_INT_STATUS (R)	3	0x0	VGA mode auto trigger interrupt status 0=No event 1=Event has occurred

VGA Interrupt status register

VGA_MAIN_CONTROL - RW - 32 bits - DISPDEC:0x350			
Field Name	**Bits**	**Default**	**Description**
VGA_CRTC_TIMEOUT	1:0	0x0	Controls whether and in what conditions the vga crtc calculations will be forced to start if the VBLANK from display takes too long to come 0=VGACRTC times out and is restarted after 1/50 sec without VBLANK 1=VGACRTC times out and is restarted after 1/10 sec without VBLANK 2=reserved 3=VGACRTC does not timeout
VGA_RENDER_TIMEOUT_COUNT	4:3	0x3	Controls whether and in how many display frames the vga render will be forced to finish or timeout 0=No timeout 1=2 frame 2=3 frames 3=4 frames
VGA_VIRTUAL_VERTICAL_RETRACE_DURATION	7:5	0x0	specifies the duration of the vga main state machine of the vga render virtual vertical retrace 0=256 us 1=512 us 2=768 us 3=1024 us 4=1280 us 5=1536 us 6=1792 us 7=2048 us
VGA_READBACK_VGA_VSTATUS_SOURCE_SELECT	9:8	0x0	selects the source for the VGA_VSTATUS readback register bit 0=Uses vga main render state machine virtual vertical retrace - a timer is used to make the duration equivalent as specified by VGA_VIRTUAL_VERTICAL_RETRACE_DURATION 1=reserved 2=Uses CRTC1 vblank signal 3=Uses CRTC2 vblank signal
VGA_READBACK_NO_DISPLAY_SOURCE_SELECT	17:16	0x0	selects the source for the NO_DISPLAY readback register bit 0=Uses vga main render state machine virtual vertical retrace - a timer is used to make the duration specified by VGA_VIRTUAL_VERTICAL_RETRACE_DURATION. Outside of the virtual vertical retrace we have a 31.25 KHz, 5/32 duty cycle pulse train generated independently by a timer asynchronous to the virtual vertical retrace, roughly equivalent to standard horizontal retrace times in standard VGA timings 1=Uses the time the vga render is not rendering. Outside of this time we have a 31.25 kHz pulse train of 5/32 duty cycle, asynchronous to the time the render is rendering and generated independently 2=Uses CRTC1 nodisplay signal 3=Uses CRTC2 nodisplay signal
VGA_READBACK_CRT_INTR_SOURCE_SELECT	25:24	0x0	selects the source for the CRT_INTR readback register bit and associated interrupt 0=Uses vga main render state machine virtual vertical retrace 1=reserved 2=Uses CRTC1 vblank signal 3=Uses CRTC2 vblank signal
VGA_READBACK_SENSE_SWITCH_SELECT	26	0x0	selects the source for the SENSE_SWITCH readback register bit 0=Uses CRTC1 sense_switch signal 1=Uses CRTC2 sense_switch signal

VGA_MAIN_TEST_VSTATUS_NO_DISPLAY_CRTC_TIMEOUT	31	0x0	For testing purposes, makes the virtual vertical retrace, the crtc time-out and the virtual no display horizontal pulses faster by using the engine clock frequency instead of 1MHz reference 0=VGACRTC timeout is as indicated by VGA_CRTC_TIMEOUT, virtual vertical retrace duration is as indicated by VGA_VIRTUAL_VERTICAL_RETRACE_DURATION, virtual no display horizontal pulses are 31.25 KHz if VGA_READBACK_NO_DISPLAY_SOURCE_SELECT is zero 1=VGACRTC timeout is one 400th of what is indicated by VGA_CRTC_TIMEOUT, virtual vertical retrace duration one 400th of what is indicated by VGA_VIRTUAL_VERTICAL_RETRACE_DURATION, virtual no display horizontal pulses are 400*31.25 KHz if VGA_READBACK_NO_DISPLAY_SOURCE_SELECT is zero

VGA Main control

VGA_TEST_CONTROL - RW - 32 bits - DISPDEC:0x354			
Field Name	**Bits**	**Default**	**Description**
VGA_TEST_ENABLE	0	0x0	Controls wether the vga render looks at vertical blank signals from the displays to start rendering or will start through a register write 0=Render responds to status signals from DISP1, DISP2 1=Render responds to VGA_TEST_RENDER_START
VGA_TEST_RENDER_START	8	0x0	Starts the vga render 0=No event 1=Every time this is written with a high, if VGA_TEST_ENABLE is set, VGA Rendering starts
VGA_TEST_RENDER_DONE (R)	16	0x0	Signals when the vga render is done rendering 0=No event 1=If VGA_TEST_ENABLE is set, VGA Rendering is done
VGA_TEST_RENDER_DISPBUF_SELECT	24	0x0	Selects to which display buffer the render will render in test mode (VGA_TEST_ENABLE=1) 0=VGA Render will write into DISPBUF1 starting at VGA_DISPBUF1_SURFACE_ADDR 1=VGA Render will write into DISPBUF2 starting at VGA_DISPBUF2_SURFACE_ADDR

VGA test control register

VGA_DEBUG_READBACK_INDEX - RW - 32 bits - DISPDEC:0x358			
Field Name	**Bits**	**Default**	**Description**
VGA_DEBUG_READBACK_INDEX	7:0	0x0	Index for the VGA debug readback

VGA debug readback index register

VGA_DEBUG_READBACK_DATA - RW - 32 bits - DISPDEC:0x35C			
Field Name	**Bits**	**Default**	**Description**
VGA_DEBUG_READBACK_DATA (R)	31:0	0x0	According to the value of VGA_DEBUG_READBACK_INDEX, VGA_DEBUG_READBACK_DATA will have this values: 0: VGAREG_DISP_h_total[10:0] 1: VGAREG_DISP_h_sync_end[10:0] 2: VGAREG_DISP_h_disp_start[10:0] 3: VGAREG_DISP_h_disp_width[10:0] 4: VGAREG_DISP_h_blank_start[10:0] 5: VGAREG_DISP_h_blank_end[10:0] 6: VGAREG_DISP_v_total[10:0] 7: VGAREG_DISP_v_sync_end[10:0] 8: VGAREG_DISP_v_disp_start[10:0] 9: VGAREG_DISP_v_disp_height[10:0] 10: VGAREG_DISP_v_blank_start[10:0] 11: VGAREG_DISP_v_blank_end[10:0] 12: VGAREG_DISP_overscan_colorR[5:0] 13: VGAREG_DISP_overscan_colorG[5:0] 14: VGAREG_DISP_overscan_colorB[5:0] 15: reserved 16 VGA_DISP_viewport_x_start 17 VGA_DISP_viewport_y_start

VGA debug readback data register

GENMO_WT - W - 8 bits - DISPDEC:0x3C2			
Field Name	**Bits**	**Default**	**Description**
GENMO_MONO_ADDRESS_B	0	0x0	VGA addressing mode. 0=Monochrome emulation, regs at 0x3Bx 1=Color/Graphic emulation, regs at 0x3Dx
VGA_RAM_EN	1	0x0	Enables/Disables CPU access to video RAM at VGA aperture. 0=Disable 1=Enable
VGA_CKSEL	3:2	0x0	Selects pixel clock frequency to use in VGA modes. Used when CRTC_GEN_CNTL.CRTC_EXT_DISP_EN=0. See CLOCK_CNTL_INDEX.PPLL_DIV_SEL for non-VGA mode pixel clock selection. 0=25.1744MHz (640 Pels) 1=28.3212MHz (720 Pels) 2=Reserved 3=Reserved
ODD_EVEN_MD_PGSEL	5	0x0	This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled. Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory. 0=Selects odd (high) memory locations 1=Selects even (low) memory locations
VGA_HSYNC_POL	6	0x0	Determines polarity of horizontal sync (HSYNC) for VGA modes. 0 = HSYNC pulse active high 1 = HSYNC pulse active low The convention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.
VGA_VSYNC_POL	7	0x0	Determines polarity of vertical sync (VSYNC) for VGA modes. 0 = VSYNC pulse active high 1 = VSYNC pulse active low The convention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.

Miscellaneous Output Register (Write)

GENMO_RD - R - 8 bits - DISPDEC:0x3CC			
Field Name	**Bits**	**Default**	**Description**
GENMO_MONO_ADDRESS_B (mirror of GENMO_WT:GENMO_MONO_ADDRESS_B)	0	0x0	VGA addressing mode. 0=Monochrome emulation, regs at 0x3Bx 1=Color/Graphic emulation, regs at 0x3Dx
VGA_RAM_EN (mirror of GENMO_WT:VGA_RAM_EN)	1	0x0	Enables/Disables CPU access to video RAM at VGA aperture. 0=Disable 1=Enable
VGA_CKSEL (mirror of GENMO_WT:VGA_CKSEL)	3:2	0x0	Selects pixel clock frequency to use. 0=25.1744MHz (640 Pels) 1=28.3212MHz (720 Pels) 2=Reserved 3=Reserved
ODD_EVEN_MD_PGSEL (mirror of GENMO_WT:ODD_EVEN_MD_PGSEL)	5	0x0	This bit is used in odd/even display modes (A/N modes: 0, 1, 2, 3, and 7). This bit is ignored when either bit GRA06[1] or SEQ4[3] are enabled. Used to determine if the VGA aperture maps into the lower (even) or upper (odd) page of memory. 0=Selects odd (high) memory locations 1=Selects even (low) memory locations
VGA_HSYNC_POL (mirror of GENMO_WT:VGA_HSYNC_POL)	6	0x0	Determines polarity of horizontal sync (HSYNC) for VGA modes. 0 = HSYNC pulse active high 1 = HSYNC pulse active low The convention of VGA is to use active low VSYNC for 400 (and 200) and 480 line modes. Active high is normally used for 350 line modes.
VGA_VSYNC_POL (mirror of GENMO_WT:VGA_VSYNC_POL)	7	0x0	Determines polarity of vertical sync (VSYNC) for VGA modes. 0 = VSYNC pulse active high 1 = VSYNC pulse active low The convention of VGA is to use active high VSYNC for 400 (and 200) line modes. Active low is normally used for 350 and 480 line modes.

Miscellaneous Output Register (Read)

SEQ8_IDX - RW - 8 bits - DISPDEC:0x3C4			
Field Name	**Bits**	**Default**	**Description**
SEQ_IDX	2:0	0x0	This index points to one of the sequencer registers (SEQ_) at I/O port address 0x3C5, for the next SEQ read/write operation.

SEQ Index Register

SEQ8_DATA - RW - 8 bits - DISPDEC:0x3C5			
Field Name	**Bits**	**Default**	**Description**
SEQ_DATA	7:0	0x0	SEQ data indirect access

SEQ Data Register

CRTC8_IDX - RW - 8 bits - [DISPDEC:0x3B4] [DISPDEC:0x3D4]			
Field Name	**Bits**	**Default**	**Description**
VCRTC_IDX (mirror bits 0:5 of CRTC_EXT_CNTL:VCRTC_IDX_MASTER)	5:0	0x0	This index points to one of the internal registers of the CRT controller (CRTC) at address 0x3?5, for the next CRTC read/write operation.

CRT Index Register

CRTC8_DATA - RW - 8 bits - [DISPDEC:0x3B5] [DISPDEC:0x3D5]			
Field Name	**Bits**	**Default**	**Description**
VCRTC_DATA	7:0	0x0	CRTC data indirect access

CTRC Data Register

CRTC_EXT_CNTL - RW - 32 bits - DISPDEC:0xE054			
Field Name	**Bits**	**Default**	**Description**
VGA_ATI_LINEAR	3	0x0	0=Disable 1=Enable
VGA_128KAP_PAGING	4	0x0	0=Normal 1=Enable
VGA_TEXT_132	5	0x0	0=inActive 1=Active
VGA_PACK_DIS	18	0x0	0=Fast VGA write in packed modes 1=Normal VGA write in packed modes
VGA_MEM_PS_EN	19	0x0	0=Don't use MEM_VGA_WP_SEL and MEM_VGA_RP_SEL registers 1=Use MEM_VGA_WP_SEL and MEM_VGA_RP_SEL registers
VCRTC_IDX_MASTER	30:24	0x0	Mirror of the vga crtc index as per VGA specified by IBM. The top bit is unused

VGA Extended control Register

GRPH8_IDX - RW - 8 bits - DISPDEC:0x3CE			
Field Name	**Bits**	**Default**	**Description**
GRPH_IDX	3:0	0x0	VGA graphics index as per VGA specified by IBM

GRPH Index Register

GRPH8_DATA - RW - 8 bits - DISPDEC:0x3CF			
Field Name	**Bits**	**Default**	**Description**
GRPH_DATA	7:0	0x0	GRPH data indirect access

GRPH Data Register

VGA_MEM_WRITE_PAGE_ADDR - RW - 32 bits - DISPDEC:0x38			
Field Name	**Bits**	**Default**	**Description**
VGA_MEM_WRITE_PAGE0_ADDR	9:0	0x0	Write page 0 address
VGA_MEM_WRITE_PAGE1_ADDR	25:16	0x0	Write page 1 address

VGA write page register

VGA_MEM_READ_PAGE_ADDR - RW - 32 bits - DISPDEC:0x3C			
Field Name	**Bits**	**Default**	**Description**
VGA_MEM_READ_PAGE0_ADDR	9:0	0x0	Read page 0 address
VGA_MEM_READ_PAGE1_ADDR	25:16	0x0	Read page 1 address

VGA read page register

2.7 Display Controller Registers

2.7.1 Primary Display Graphics Controller Registers

D1GRPH_ENABLE - RW - 32 bits - DISPDEC:0x6100			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_ENABLE	0	0x1	Primary graphic enabled. 0=disable 1=enable

Primary graphic enabled.

D1GRPH_CONTROL - RW - 32 bits - DISPDEC:0x6104			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_DEPTH	1:0	0x0	Primary graphic pixel depth. 0=8bpp 1=16bpp 2=32bpp 3=64bpp
D1GRPH_FORMAT	10:8	0x0	Primary graphic pixel format. It is used together with D1GRPH_DEPTH to define the graphic pixel format. If (D1GRPH_DEPTH = 0x0)(8 bpp) 0x0 - indexed others - reserved else if (D1GRPH_DEPTH = 0x1)(16 bpp) 0x0 - ARGB 1555 0x1 - RGB 565 0x2 - ARGB 4444 0x3 - Alpha index 88 0x4 - monochrome 16 others - reserved else if (D1GRPH_DEPTH = 0x2)(32 bpp) 0x0 - ARGB 8888 0x1 - ARGB 2101010 0x2 - 32bpp digital output 0x3 - 8-bit ARGB 2101010 others - reserved else if (D1GRPH_DEPTH = 0x3)(64 bpp) 0x0 - ARGB 16161616 0x1 - 64bpp digital output ARGB[13:2] 0x2 - 64bpp digital output RGB[15:0] 0x3 - 64bpp digital output ARGB[11:0] others - reserved
D1GRPH_SWAP_RB	16	0x0	Primary graphic pixel format R and B swap 0=no swap 1=swap R and B
D1GRPH_TILED	20	0x1	0=Linear surface 1=Tiled surface
D1GRPH_MACRO_ADDRESS_MODE	21	0x0	Sets macro addressing mode when D1GRPH_TILED = 0 (micro linear mode). This field is don't care when D1GRPH_TILED = 1 (micro tiled mode). Display does not support macro-linear and micro-tiled surfaces. When D1GRPH_TILED = 1, addressing mode is macro-tiled and micro-tiled. 0=macro-linear (and micro-linear) 1=macro-tiled (and micro-linear)

D1GRPH_16BIT_ALPHA_MODE	25:24	0x0	This field is only used if 64 bpp graphics bit depth and graphics/overlay blend using per-pixel alpha from graphics channel. It is used for processing 16 bit alpha. The fixed point graphics alpha value in the frame buffer is always clamped to 0.0 - 1.0 data range. 0x0 - Floating point alpha (1 sign bit, 5 bit exponent, 10 bit mantissa) 0x1 - Fixed point alpha with normalization from 256/256 to 255/255 to represent 1.0 0x2 - Fixed point alpha with no normalization 0x3 - Fixed point alpha using lower 8 bits of frame buffer value, no normalization
D1GRPH_16BIT_FIXED_ALPHA_RANGE	30:28	0x0	This register field is only used if 64 bpp graphics bit depth and D1GRPH_16BIT_ALPHA_MODE = 01 or 10. Also only used if graphics/overlay blend using per-pixel alpha from graphics channel. Final alpha blend value is rounded to 8 bits after optional normalization step (see D1GRPH_16BIT_ALPHA_MODE). 0x0 - Use bits 15:0 of input alpha value for blend alpha 0x1 - Use bits 14:0 of input alpha value for blend alpha 0x2 - Use bits 13:0 of input alpha value for blend alpha 0x3 - Use bits 12:0 of input alpha value for blend alpha 0x4 - Use bits 11:0 of input alpha value for blend alpha 0x5 - Use bits 10:0 of input alpha value for blend alpha 0x6 - Use bits 9:0 of input alpha value for blend alpha 0x7 - Use bits 8:0 of input alpha value for blend alpha

Primary graphic pixel depth and format.

D1GRPH_LUT_SEL - RW - 32 bits - DISPDEC:0x6108			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_LUT_SEL	0	0x0	Primary graphic LUT selection. 0=select LUTA 1=select LUTB
D1GRPH_LUT_10BIT_BYPASS_EN	8	0x0	Enable bypass primary graphic LUT for 2101010 format 0=Use LUT 1=Bypass LUT when in 2101010 format. Ignored for other formats
D1GRPH_LUT_10BIT_BYPASS_DBL_BUF_EN	16	0x0	Enable double buffer D1GRPH_LUT_10BIT_BYPASS_EN 0=D1GRPH_LUT_10BIT_BYPASS_EN take effect right away 1=D1GRPH_LUT_10BIT_BYPASS_EN are double buffered

Primary graphic LUT selection.

D1GRPH_PRIMARY_SURFACE_ADDRESS - RW - 32 bits - DISPDEC:0x6110			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_PRIMARY_SURFACE_ADDRESS	31:0	0x0	Primary surface address for primary graphics in byte. It is 4K byte aligned. NOTE: Bits 0:10 of this field are hardwired to ZERO.

Primary surface address for primary graphics in byte.

D1GRPH_SECONDARY_SURFACE_ADDRESS - RW - 32 bits - DISPDEC:0x6118			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_SECONDARY_SURFACE_ADDRESS	31:0	0x0	Secondary surface address for primary graphics in byte. It is 4K byte aligned. NOTE: Bits 0:10 of this field are hardwired to ZERO.

Secondary surface address for primary graphics in byte.

D1GRPH_PITCH - RW - 32 bits - DISPDEC:0x6120			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_PITCH	13:0	0x0	Primary graphic surface pitch in pixels. For Micro-tiled/Macro-tiled surface, it must be multiple of 64 pixels in 8bpp mode. For Micro-linear/Macro-tiled surface, it must be multiple of 256 pixels in 8bpp mode, multiple of 128 pixels in 16bpp mode and multiple of 64 pixels in 32bpp mode. For Micro-linear/Macro-linear surface, it must be multiple of 64 pixels in 8bpp mode. For other modes, it must be multiple of 32. NOTE: Bits 0:4 of this field are hardwired to ZERO.

Primary graphic surface pitch in pixels.

D1GRPH_SURFACE_OFFSET_X - RW - 32 bits - DISPDEC:0x6124			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_SURFACE_OFFSET_X	12:0	0x0	Primary graphic X surface offset. It is 256 pixels aligned. NOTE: Bits 0:7 of this field are hardwired to ZERO.

Primary graphic X surface offset.

D1GRPH_SURFACE_OFFSET_Y - RW - 32 bits - DISPDEC:0x6128			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_SURFACE_OFFSET_Y	12:0	0x0	Primary graphic Y surface offset. It must be even value NOTE: Bit 0 of this field is hardwired to ZERO.

Primary graphic Y surface offset.

D1GRPH_X_START - RW - 32 bits - DISPDEC:0x612C			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_X_START	12:0	0x0	Primary graphic X start coordinate relative to the desktop coordinates.

Primary graphic X start coordinate relative to the desktop coordinates.

D1GRPH_Y_START - RW - 32 bits - DISPDEC:0x6130			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_Y_START	12:0	0x0	Primary graphic Y start coordinate relative to the desktop coordinates.
Primary graphic Y start coordinate relative to the desktop coordinates.			

D1GRPH_X_END - RW - 32 bits - DISPDEC:0x6134			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_X_END	13:0	0x0	Primary graphic X end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K
Primary graphic X end coordinate relative to the desktop coordinates.			

D1GRPH_Y_END - RW - 32 bits - DISPDEC:0x6138			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_Y_END	13:0	0x0	Primary graphic Y end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K
Primary graphic Y end coordinate relative to the desktop coordinates.			

D1GRPH_UPDATE - RW - 32 bits - DISPDEC:0x6144			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_MODE_UPDATE_PENDING (R)	0	0x0	Primary graphic mode register update pending control. It is set to 1 after a host write to graphics mode register. It is cleared after double buffering is done. This signal is only visible through register. The graphics surface register includes: D1GRPH_DEPTH D1GRPH_FORMAT D1GRPH_SWAP_RB D1GRPH_LUT_SEL D1GRPH_LUT_10BIT_BYPASS_EN D1GRPH_ENABLE D1GRPH_X_START D1GRPH_Y_START D1GRPH_X_END D1GRPH_Y_END The mode register double buffering can only occur at vertical retrace. The double buffering occurs when D1GRPH_MODE_UPDATE_PENDING = 1 and D1GRPH_UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC1 is disabled, the registers will be updated instantly. 0=No update pending 1=Update pending
D1GRPH_MODE_UPDATE_TAKEN (R)	1	0x0	Primary graphics update taken status for mode registers. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0.

D1GRPH_SURFACE_UPDATE_PENDING (R)	2	0x0	Primary graphic surface register update pending control. If it is set to 1 after a host write to graphics surface register. It is cleared after double buffering is done. It is cleared after double buffering is done. This signal also goes to both the RBBM wait_until and to the CP_RTS_discrete inputs. The graphics surface register includes: D1GRPH_PRIMARY_SURFACE_ADDRESS D1GRPH_SECONDARY_SURFACE_ADDRESS D1GRPH_PITCH D1GRPH_SURFACE_OFFSET_X D1GRPH_SURFACE_OFFSET_Y. If D1GRPH_SURFACE_UPDATE_H_RETRACE_EN = 0, the double buffering occurs in vertical retrace when D1GRPH_SURFACE_UPDATE_PENDING = 1 and D1GRPH_UPDATE_LOCK = 0 and V_UPDATE = 1. Otherwise the double buffering happens at horizontal retrace when D1GRPH_SURFACE_UPDATE_PENDING = 1 and D1GRPH_UPDATE_LOCK = 0 and Data request for last chunk of the line is sent from DCP to DMIF. If CRTC1 is disabled, the registers will be updated instantly
D1GRPH_SURFACE_UPDATE_TAKEN (R)	3	0x0	Primary graphics update taken status for surface registers. If D1GRPH_SURFACE_UPDATE_H_RETRACE_EN = 0, it is set to 1 when double buffering occurs and cleared when V_UPDATE = 0. Otherwise, it is active for one clock cycle when double buffering occurs at the horizontal retrace.
D1GRPH_UPDATE_LOCK	16	0x0	Primary graphic register update lock control. This lock bit control both surface and mode register double buffer 0=Unlocked 1=Locked

Primary graphic update control

D1GRPH_FLIP_CONTROL - RW - 32 bits - DISPDEC:0x6148			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_SURFACE_UPDATE_H_RETRACE_EN	0	0x0	Enable primary graphic surface register double buffer in horizontal retrace. 0=Vertical retrace flipping 1=Horizontal retrace flipping

Enable primary graphic surface register double buffer in horizontal retrace

D1GRPH_SURFACE_ADDRESS_INUSE - RW - 32 bits - DISPDEC:0x614C			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_SURFACE_ADDRESS_INUSE (R)	31:11	0x0	This register reads back snapshot of primary graphics surface address used for data request. The address is the signal sent to DMIF and is updated on SOF or horizontal surface update. The snapshot is triggered by writing 1 into field D1CRTC_SNAPSHOT_MANUAL_TRIGGER of CRTC register D1CRTC_SNAPSHOT_STATUS.

Snapshot of primary graphics surface address in use

2.7.2 Primary Display Video Overlay Control Registers

D1OVL_ENABLE - RW - 32 bits - DISPDEC:0x6180			
Field Name	**Bits**	**Default**	**Description**
D1OVL_ENABLE	0	0x0	Primary overlay enabled. 0=disable 1=enable

Primary overlay enabled.

D1OVL_CONTROL1 - RW - 32 bits - DISPDEC:0x6184			
Field Name	**Bits**	**Default**	**Description**
D1OVL_DEPTH	1:0	0x0	Primary overlay pixel depth 0=reserved 1=16bpp 2=32bpp 3=reserved
D1OVL_FORMAT	10:8	0x0	Primary overlay pixel format. It is used together with D1OVL_DEPTH to define the overlay format. If (D1OVL_DEPTH = 0x1)(16 bpp) 0x0- ARGB 1555 0x1 - RGB 565 others - reserved else if (D1OVL_DEPTH = 0x2)(32 bpp) 0x0 - ACrYCb 8888 or ARGB 8888 0x1 - ACrYCb 2101010 or ARGB 2101010 others - reserved
D1OVL_SWAP_RB	16	0x0	Primary overlay pixel format R and B swap 0=no swap 1=swap R and B
D1OVL_TILED	20	0x1	0=Reserved 1=Tiled surface
D1OVL_MACRO_ADDRESS_MODE	21	0x0	Sets macro addressing mode when D1OVL_TILED = 0 (micro linear mode). This field is don't care when D1OVL_TILED = 1 (micro tiled mode). Display does not support macro-linear and micro-tiled surfaces. When D1OVL_TILED = 1, addressing mode is macro-tiled and micro-tiled. 0=macro-linear (and micro-linear) 1=macro-tiled (and micro-linear)
D1OVL_COLOR_EXPANSION_MODE	24	0x0	Primary overlay pixel format expansion mode. 0=dynamic expansion for RGB 1=zero expansion for YCbCr

Primary overlay pixel depth and format.

D1OVL_CONTROL2 - RW - 32 bits - DISPDEC:0x6188			
Field Name	**Bits**	**Default**	**Description**
D1OVL_HALF_RESOLUTION_ENABLE	0	0x0	Primary overlay half resolution control 0=disable 1=enable

Primary overlay half resolution control

D1OVL_SURFACE_ADDRESS - RW - 32 bits - DISPDEC:0x6190			
Field Name	**Bits**	**Default**	**Description**
D1OVL_SURFACE_ADDRESS	31:0	0x0	Primary overlay surface base address in byte. It is 4K bytes aligned. NOTE: Bits 0:10 of this field are hardwired to ZERO.

Primary overlay surface base address in byte.

D1OVL_PITCH - RW - 32 bits - DISPDEC:0x6198			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PITCH	13:0	0x0	Primary overlay surface pitch in pixels. For Micro-tiled/Macro-tiled surface, it must be multiple of 64 pixels in 8bpp mode. For Micro-linear/Macro-tiled surface, it must be multiple of 256 pixeld in 8bpp mode, multiple of 128 pixels in 16bpp mode and multiple of 64 pixels in 32bpp mode. For Micro-linear/Macro-linear surface, it must be multiple of 64 pixels in 8bpp mode. For other modes, it must be multiple of 32. NOTE: Bits 0:4 of this field are hardwired to ZERO.

Primary overlay surface pitch in pixels.

D1OVL_SURFACE_OFFSET_X - RW - 32 bits - DISPDEC:0x619C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_SURFACE_OFFSET_X	12:0	0x0	Primary overlay X surface offset. It is 256 pixels aligned. NOTE: Bits 0:7 of this field are hardwired to ZERO.

Primary overlay X surface offset.

D1OVL_SURFACE_OFFSET_Y - RW - 32 bits - DISPDEC:0x61A0			
Field Name	**Bits**	**Default**	**Description**
D1OVL_SURFACE_OFFSET_Y	12:0	0x0	Primary overlay Y surface offset. It is even value. NOTE: Bit 0 of this field is hardwired to ZERO.

Primary overlay Y surface offset.

D1OVL_START - RW - 32 bits - DISPDEC:0x61A4			
Field Name	**Bits**	**Default**	**Description**
D1OVL_Y_START	12:0	0x0	Primary overlay Y start coordinate relative to the desktop coordinates.
D1OVL_X_START	28:16	0x0	Primary overlay X start coordinate relative to the desktop coordinates.

Primary overlay X, Y start coordinate relative to the desktop coordinates.

D1OVL_END - RW - 32 bits - DISPDEC:0x61A8			
Field Name	**Bits**	**Default**	**Description**
D1OVL_Y_END	13:0	0x0	Primary overlay Y end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K.
D1OVL_X_END	29:16	0x0	Primary overlay X end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K.

Primary overlay X, Y end coordinate relative to the desktop coordinates.

D1OVL_UPDATE - RW - 32 bits - DISPDEC:0x61AC			
Field Name	**Bits**	**Default**	**Description**
D1OVL_UPDATE_PENDING (R)	0	0x0	Primary overlay register update pending control. It is set to 1 after a host write to overlay double buffer register. It is cleared after double buffering is done. The double buffering occurs when UPDATE_PENDING = 1 and UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC1 is disabled, the registers will be updated instantly. D1OVL double buffer registers include: D1OVL_ENABLE D1OVL_DEPTH D1OVL_FORMAT D1OVL_SWAP_RB D1OVL_COLOR_EXPANSION_MODE D1OVL_HALF_RESOLUTION_ENABLE D1OVL_SURFACE_ADDRESS D1OVL_PITCH D1OVL_SURFACE_OFFSET_X D1OVL_SURFACE_OFFSET_Y D1OVL_START D1OVL_END 0=No update pending 1=Update pending
D1OVL_UPDATE_TAKEN (R)	1	0x0	Primary overlay update taken status. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0.
D1OVL_UPDATE_LOCK	16	0x0	Primary overlay register update lock control. 0=Unlocked 1=Locked

Primary overlay register update

D1OVL_SURFACE_ADDRESS_INUSE - RW - 32 bits - DISPDEC:0x61B0			
Field Name	**Bits**	**Default**	**Description**
D1OVL_SURFACE_ADDRESS_INUSE (R)	31:11	0x0	This register reads back snapshot of primary overlay surface address used for data request. The address is the signal sent to DMIF and is updated on SOF or horizontal surface update. The snapshot is triggered by writing 1 into field D1CRTC_SNAPSHOT_MANUAL_TRIGGER of CRTC register D1CRTC_SNAPSHOT_STATUS.

Snapshot of primary overlay surface address in use

2.7.3 Primary Display Video Overlay Transform Registers

D1OVL_MATRIX_TRANSFORM_EN - RW - 32 bits - DISPDEC:0x6200			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_TRANSFORM_EN	0	0x0	Primary overlay matrix conversion enable 0=disable 1=enable

Primary overlay matrix conversion enable.

D1OVL_MATRIX_COEF_1_1 - RW - 32 bits - DISPDEC:0x6204			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_1_1	18:0	0x198a0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1OVL_MATRIX_SIGN_1_1	31	0x0	Sign bit of combined matrix constant

Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.

D1OVL_MATRIX_COEF_1_2 - RW - 32 bits - DISPDEC:0x6208			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_1_2	18:0	0x12a20	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1OVL_MATRIX_SIGN_1_2	31	0x0	Sign bit of combined matrix constant

Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.

D1OVL_MATRIX_COEF_1_3 - RW - 32 bits - DISPDEC:0x620C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_1_3	18:0	0x0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1OVL_MATRIX_SIGN_1_3	31	0x0	Sign bit of combined matrix constant

Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.

D1OVL_MATRIX_COEF_1_4 - RW - 32 bits - DISPDEC:0x6210			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_1_4	26:8	0x48700	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S11.1. NOTE: Bits 0:6 of this field are hardwired to ZERO.
D1OVL_MATRIX_SIGN_1_4	31	0x1	Sign bit of combined matrix constant

Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.

D1OVL_MATRIX_COEF_2_1 - RW - 32 bits - DISPDEC:0x6214			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_2_1	18:0	0x72fe0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1OVL_MATRIX_SIGN_2_1	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_2_2 - RW - 32 bits - DISPDEC:0x6218			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_2_2	18:0	0x12a20	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1OVL_MATRIX_SIGN_2_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_2_3 - RW - 32 bits - DISPDEC:0x621C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_2_3	18:0	0x79bc0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1OVL_MATRIX_SIGN_2_3	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_2_4 - RW - 32 bits - DISPDEC:0x6220			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_2_4	26:8	0x22100	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S11.1. NOTE: Bits 0:6 of this field are hardwired to ZERO.
D1OVL_MATRIX_SIGN_2_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_3_1 - RW - 32 bits - DISPDEC:0x6224			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_3_1	18:0	0x0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1OVL_MATRIX_SIGN_3_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_3_2 - RW - 32 bits - DISPDEC:0x6228			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_3_2	18:0	0x12a20	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1OVL_MATRIX_SIGN_3_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_3_3 - RW - 32 bits - DISPDEC:0x622C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_3_3	18:0	0x20460	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1OVL_MATRIX_SIGN_3_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

D1OVL_MATRIX_COEF_3_4 - RW - 32 bits - DISPDEC:0x6230			
Field Name	**Bits**	**Default**	**Description**
D1OVL_MATRIX_COEF_3_4	26:8	0x3af80	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay. Format fix-point S11.1. NOTE: Bits 0:6 of this field are hardwired to ZERO.
D1OVL_MATRIX_SIGN_3_4	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for primary overlay.			

2.7.4 Primary Display Video Overlay Gamma Correction Registers

D1OVL_PWL_TRANSFORM_EN - RW - 32 bits - DISPDEC:0x6280			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_TRANSFORM_EN	0	0x0	Primary overlay gamma correction enable. 0=disable 1=enable

Primary overlay gamma correction enable.

D1OVL_PWL_0TOF - RW - 32 bits - DISPDEC:0x6284			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_0TOF_OFFSET	8:0	0x0	Primary overlay gamma correction non-linear offset for input 0x0-0xF. Format fix-point 8.1 (0.0 to +255.5).
D1OVL_PWL_0TOF_SLOPE	26:16	0x100	Primary overlay gamma correction non-linear slope for input 0x0-0xF. Format fix-point 3.8 (0.00 to +7.99).

Primary overlay gamma correction non-linear offset and slope for input 0x0-0xF

D1OVL_PWL_10TO1F - RW - 32 bits - DISPDEC:0x6288			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_10TO1F_OFFSET	8:0	0x20	Primary overlay gamma correction non-linear offset for input 0x10-0x1F. Format fix-point 8.1 (0.0 to +255.5).
D1OVL_PWL_10TO1F_SLOPE	26:16	0x100	Primary overlay gamma correction non-linear slope for input 0x10-0x1F. Format fix-point 3.8 (0.00 to +7.99).

Primary overlay gamma correction non-linear offset and slope for input 0x10-0x1F

D1OVL_PWL_20TO3F - RW - 32 bits - DISPDEC:0x628C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_20TO3F_OFFSET	9:0	0x40	Primary overlay gamma correction non-linear offset for input 0x20-0x3F. Format fix-point 9.1 (0.0 to +511.5).
D1OVL_PWL_20TO3F_SLOPE	25:16	0x100	Primary overlay gamma correction non-linear slope for input 0x20-0x3F. Format fix-point 2.8 (0.00 to +3.99).

Primary overlay gamma correction non-linear offset and slope for input 0x20-0x3F

D1OVL_PWL_40TO7F - RW - 32 bits - DISPDEC:0x6290			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_40TO7F_OFFSET	9:0	0x80	Primary overlay gamma correction non-linear offset for input 40-7F. Format fix-point 9.1 (0.0 to +511.5).
D1OVL_PWL_40TO7F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 40-7F. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 40-7F.

D1OVL_PWL_80TOBF - RW - 32 bits - DISPDEC:0x6294			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_80TOBF_OFFSET	10:0	0x100	Primary overlay gamma correction non-linear offset for input 80-BF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_80TOBF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 80-BF. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 80-BF.

D1OVL_PWL_C0TOFF - RW - 32 bits - DISPDEC:0x6298			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_C0TOFF_OFFSET	10:0	0x180	Primary overlay gamma correction non-linear offset for input C0-FF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_C0TOFF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input C0-FF. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input C0-FF.

D1OVL_PWL_100TO13F - RW - 32 bits - DISPDEC:0x629C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_100TO13F_OFFSET	10:0	0x200	Primary overlay gamma correction non-linear offset for input 100-13F. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_100TO13F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 100-13F. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 100-13F.

D1OVL_PWL_140TO17F - RW - 32 bits - DISPDEC:0x62A0			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_140TO17F_OFFSET	10:0	0x280	Primary overlay gamma correction non-linear offset for input 140-17F. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_140TO17F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 140-17F. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 140-17F.

D1OVL_PWL_180TO1BF - RW - 32 bits - DISPDEC:0x62A4			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_180TO1BF_OFFSET	10:0	0x300	Primary overlay gamma correction non-linear offset for input 180-1BF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_180TO1BF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 180-1BF. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 180-1BF.

D1OVL_PWL_1C0TO1FF - RW - 32 bits - DISPDEC:0x62A8			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_1C0TO1FF_OFFSET	10:0	0x380	Primary overlay gamma correction non-linear offset for input 1C0-1FF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_1C0TO1FF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 1C0-1FF. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 1C0-1FF.

D1OVL_PWL_200TO23F - RW - 32 bits - DISPDEC:0x62AC			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_200TO23F_OFFSET	10:0	0x400	Primary overlay gamma correction non-linear offset for input 200-23F. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_200TO23F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 200-23F. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 200-23F.

D1OVL_PWL_240TO27F - RW - 32 bits - DISPDEC:0x62B0			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_240TO27F_OFFSET	10:0	0x480	Primary overlay gamma correction non-linear offset for input 240-27F. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_240TO27F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 240-27F. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 240-27F.

D1OVL_PWL_280TO2BF - RW - 32 bits - DISPDEC:0x62B4			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_280TO2BF_OFFSET	10:0	0x500	Primary overlay gamma correction non-linear offset for input 280-2BF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_280TO2BF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 280-2BF. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 280-2BF.

D1OVL_PWL_2C0TO2FF - RW - 32 bits - DISPDEC:0x62B8			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_2C0TO2FF_OFFSET	10:0	0x580	Primary overlay gamma correction non-linear offset for input 2C0-2FF. Format fix-point 10.1(0.0 to +1023.5).
D1OVL_PWL_2C0TO2FF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 2C0-2FF. Format fix-point 1.8(0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 2C0-2FF.

D1OVL_PWL_300TO33F - RW - 32 bits - DISPDEC:0x62BC			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_300TO33F_OFFSET	10:0	0x600	Primary overlay gamma correction non-linear offset for input 300-33F. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_300TO33F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 300-33F. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 300-33F.

D1OVL_PWL_340TO37F - RW - 32 bits - DISPDEC:0x62C0

Field Name	Bits	Default	Description
D1OVL_PWL_340TO37F_OFFSET	10:0	0x680	Primary overlay gamma correction non-linear offset for input 340-37F. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_340TO37F_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 340-37F. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 340-37F.

D1OVL_PWL_380TO3BF - RW - 32 bits - DISPDEC:0x62C4			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_380TO3BF_OFFSET	10:0	0x700	Primary overlay gamma correction non-linear offset for input 380-3BF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_380TO3BF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 380-3BF. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 380-3BF.

D1OVL_PWL_3C0TO3FF - RW - 32 bits - DISPDEC:0x62C8			
Field Name	**Bits**	**Default**	**Description**
D1OVL_PWL_3C0TO3FF_OFFSET	10:0	0x780	Primary overlay gamma correction non-linear offset for input 3C0-3FF. Format fix-point 10.1 (0.0 to +1023.5).
D1OVL_PWL_3C0TO3FF_SLOPE	24:16	0x100	Primary overlay gamma correction non-linear slope for input 3C0-3FF. Format fix-point 1.8 (0.00 to +1.99).

Primary overlay gamma correction non-linear offset and slope for input 3C0-3FF.

2.7.5 Primary Display Graphics and Overlay Blending Registers

D1OVL_KEY_CONTROL - RW - 32 bits - DISPDEC:0x6300			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_KEY_FUNCTION	1:0	0x0	Selects graphic keyer result equation for primary display. 0=GRPH1_KEY = FALSE = 0 1=GRPH1_KEY = TRUE = 1 2=GPPH1_KEY = (GRPH1_RED in range) AND (GRPH1_GREEN in range) AND (GRPH1_BLUE in range) AND(GRPH1_ALPHA in range) 3=GRPH1_KEY = not [(GRPH1_RED in range) AND (GRPH1_GREEN in range) AND (GRPH1_BLUE in range) AND(GRPH1_ALPHA in range)]
D1OVL_KEY_FUNCTION	9:8	0x0	Selects overlay keyer result equation for primary display. 0=OVL1_KEY = FALSE = 0 1=OVL1_KEY = TRUE = 1 2=OVL1_KEY = (OVL1_Cr_RED in range) AND (OVL1_Y_GREEN in range) AND (OVL1_Cb_BLUE in range) AND (OVL1_ALPHA in range) 3=OVL1_KEY = not [(OVL1_Cr_RED in range) AND (OVL1_Y_GREEN in range) AND (OVL1_Cb_BLUE in range) AND (OVL1_ALPHA in range)]
D1OVL_KEY_COMPARE_MIX	16	0x0	Selects final mix of graphics and overlay keys for primary display. 0=GRPH_OVL_KEY = GRPH_KEY or OVL_KEY 1=GRPH_OVL_KEY = GRPH_KEY and OVL_KEY

Primary display key control

D1GRPH_ALPHA - RW - 32 bits - DISPDEC:0x6304			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_ALPHA	7:0	0xff	Global graphic alpha for use in key mode and global alpha modes. See D1OVL_ALPHA_MODE register filed for more details

Global graphic alpha for use in key mode and global alpha modes.

D1OVL_ALPHA - RW - 32 bits - DISPDEC:0x6308			
Field Name	**Bits**	**Default**	**Description**
D1OVL_ALPHA	7:0	0xff	Global overlay alpha for use in key mode and global alpha modes. See D1OVL_ALPHA_MODE register filed for more details

Global overlay alpha for use in key mode and global alpha modes.

D1OVL_ALPHA_CONTROL - RW - 32 bits - DISPDEC:0x630C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_ALPHA_MODE	1:0	0x0	Graphics/overlay alpha blending mode for primary controller. In any case, if there is only graphics, the input OVL_DATA is forced to blank. If there is only overlay, the input GRPH_DATA is forced to blank. 0=Keyer mode, select graphic or overlay keyer to mix graphics and overlay 1=Per pixel graphic alpha mode.Alpha blend graphic and overlay layer. The alpha from graphic pixel may be inverted according to register field 2=Global alpha mode 3=Per pixel overlay alpha mode
D1OVL_ALPHA_PREMULT	8	0x0	For use with per pixel alpha blend mode. Selects whether pre-multiplied alpha or non-multiplied alpha. 0=0x0 - When DxOVL_ALPHA_MODE = 0x1, then Pixel = PIX_ALPHA * graphics pixel + (1-PIX_ALPHA) * overlay pixel.When DxOVL_ALPHA_MODE = 0x3, then Pixel = PIX_ALPHA * overlay pixel + (1-PIX_ALPHA) * graphic pixel 1=0x1 - When DxOVL_ALPHA_MODE = 0x1, then Pixel = graphic pixel + (1-PIX_ALPHA) * overlay pixel.When DxOVL_ALPHA_MODE = 0x3, then Pixel = overlay pixel + (1-PIX_ALPHA) * graphic pixel
D1OVL_ALPHA_INV	16	0x0	For use with pixel blend mode. Apply optional inversion to the alpha value extracted form the graphics or overlay surface data. 0=PIX_ALPHA = alpha from graphics or overlay 1=PIX_ALPHA = 1 - alpha from graphics or overlay

Primary display graphics/overlay alpha blending control

D1GRPH_KEY_RANGE_RED - RW - 32 bits - DISPDEC:0x6310			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_KEY_RED_LOW	15:0	0x0	Primary graphics keyer red component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D1GRPH_KEY_RED_HIGH	31:16	0x0	Primary graphics keyer red component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.

Primary graphics keyer red component range

D1GRPH_KEY_RANGE_GREEN - RW - 32 bits - DISPDEC:0x6314			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_KEY_GREEN_LOW	15:0	0x0	Primary graphics keyer green component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D1GRPH_KEY_GREEN_HIGH	31:16	0x0	Primary graphics keyer green component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.

Primary graphics keyer green component range

D1GRPH_KEY_RANGE_BLUE - RW - 32 bits - DISPDEC:0x6318			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_KEY_BLUE_LOW	15:0	0x0	Primary graphics keyer blue component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D1GRPH_KEY_BLUE_HIGH	31:16	0x0	Primary graphics keyer blue component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.

Primary graphics keyer blue component range

D1GRPH_KEY_RANGE_ALPHA - RW - 32 bits - DISPDEC:0x631C			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_KEY_ALPHA_LOW	15:0	0x0	Primary graphics keyer alpha component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D1GRPH_KEY_ALPHA_HIGH	31:16	0x0	Primary graphics keyer alpha component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.

Primary graphics keyer alpha component range

D1OVL_KEY_RANGE_RED_CR - RW - 32 bits - DISPDEC:0x6320			
Field Name	**Bits**	**Default**	**Description**
D1OVL_KEY_RED_CR_LOW	9:0	0x0	Primary overlay keyer red component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D1OVL_KEY_RED_CR_HIGH	25:16	0x0	Primary overlay keyer red component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.

Primary overlay keyer red component range

D1OVL_KEY_RANGE_GREEN_Y - RW - 32 bits - DISPDEC:0x6324			
Field Name	**Bits**	**Default**	**Description**
D1OVL_KEY_GREEN_Y_LOW	9:0	0x0	Primary overlay keyer green component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D1OVL_KEY_GREEN_Y_HIGH	25:16	0x0	Primary overlay keyer green component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.

Primary overlay keyer green component range

D1OVL_KEY_RANGE_BLUE_CB - RW - 32 bits - DISPDEC:0x6328			
Field Name	**Bits**	**Default**	**Description**
D1OVL_KEY_BLUE_CB_LOW	9:0	0x0	Primary overlay keyer blue component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D1OVL_KEY_BLUE_CB_HIGH	25:16	0x0	Primary overlay keyer blue component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.

Primary overlay keyer blue component range

D1OVL_KEY_ALPHA - RW - 32 bits - DISPDEC:0x632C			
Field Name	**Bits**	**Default**	**Description**
D1OVL_KEY_ALPHA_LOW	7:0	0x0	Primary overlay keyer alpha component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D1OVL_KEY_ALPHA_HIGH	23:16	0x0	Primary overlay keyer alpha component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.

Primary overlay keyer alpha component range

2.7.6 Primary Display Color Matrix Transform Registers

D1GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL - RW - 32 bits - DISPDEC:0x6380			
Field Name	**Bits**	**Default**	**Description**
D1GRPH_COLOR_MATRIX_TRANSFORMATION_EN	0	0x0	Matrix transformation control for primary display graphics and cursor pixel. It is used when PIX_TYPE is 1. 0=disable 1=enable
Matrix transformation control for primary display graphics and cursor pixel.			

D1OVL_COLOR_MATRIX_TRANSFORMATION_CNTL - RW - 32 bits - DISPDEC:0x6140			
Field Name	**Bits**	**Default**	**Description**
D1OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	2:0	0x0	Matrix transformation control for primary display overlay pixels. It is used when PIX_TYPE is 0. 0=No color space adjustment on display output of overlay pixels 1=Apply display x color space control on the overlay pixels based on DxCOLOR_MATRIX_COEF register settings 2=Convert overlay pixel to standard definition YCbCr(601) color space 3=Convert overlay pixels to high definition YCbCR(709) color space 4=Convert overlay pixels to high definition TVRGB color space
Matrix transformation control for primary display overlay pixels.			

D1COLOR_MATRIX_COEF_1_1 - RW - 32 bits - DISPDEC:0x6384			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_1_1	16:0	0x0	Combined matrix constant C11 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S1.11(-2.00 to +1.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1COLOR_MATRIX_SIGN_1_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C11 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_1_2 - RW - 32 bits - DISPDEC:0x6388			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_1_2	15:0	0x0	Combined matrix constant C12 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S0.11(-1.00 to + 0.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1COLOR_MATRIX_SIGN_1_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C12 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_1_3 - RW - 32 bits - DISPDEC:0x638C			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_1_3	15:0	0x0	Combined matrix constant C13 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S0.11(-1.0 to +0.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1COLOR_MATRIX_SIGN_1_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C13 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_1_4 - RW - 32 bits - DISPDEC:0x6390			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_1_4	26:8	0x0	Combined matrix constant C14 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S11.1(-2048.5 to +2047.5). It includes subtraction of 512 offset NOTE: Bits 0:6 of this field are hardwired to ZERO.
D1COLOR_MATRIX_SIGN_1_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C14 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_2_1 - RW - 32 bits - DISPDEC:0x6394			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_2_1	15:0	0x0	Combined matrix constant C21 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S0.11(-1.00 to +0.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1COLOR_MATRIX_SIGN_2_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C21 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_2_2 - RW - 32 bits - DISPDEC:0x6398			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_2_2	16:0	0x0	Combined matrix constant C22 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S1.11(-2.00 to +1.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1COLOR_MATRIX_SIGN_2_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C22 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_2_3 - RW - 32 bits - DISPDEC:0x639C			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_2_3	15:0	0x0	Combined matrix constant C23 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S0.11(-1.00 to +0.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1COLOR_MATRIX_SIGN_2_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C23 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

D1COLOR_MATRIX_COEF_2_4 - RW - 32 bits - DISPDEC:0x63A0			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_2_4	26:8	0x0	Combined matrix constant C24 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S11.1(-2048.5 to +2047.5). It includes subtraction of 512 offset NOTE: Bits 0:6 of this field are hardwired to ZERO.
D1COLOR_MATRIX_SIGN_2_4	31	0x0	Sign bit of combined matrix constant

Combined matrix constant C24 of RGB->YCbCr, contrast and brightness adjustment for primary display.

D1COLOR_MATRIX_COEF_3_1 - RW - 32 bits - DISPDEC:0x63A4			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_3_1	15:0	0x0	Combined matrix constant C31 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S0.11(-1.00 to +0.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1COLOR_MATRIX_SIGN_3_1	31	0x0	Sign bit of combined matrix constant

Combined matrix constant C31 of RGB->YCbCr, contrast and brightness adjustment for primary display.

D1COLOR_MATRIX_COEF_3_2 - RW - 32 bits - DISPDEC:0x63A8			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_3_2	15:0	0x0	Combined matrix constant C32 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S0.11(-1.00 to +0.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1COLOR_MATRIX_SIGN_3_2	31	0x0	Sign bit of combined matrix constant

Combined matrix constant C32 of RGB->YCbCr, contrast and brightness adjustment for primary display.

D1COLOR_MATRIX_COEF_3_3 - RW - 32 bits - DISPDEC:0x63AC			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_3_3	16:0	0x0	Combined matrix constant C33 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S1.11(-2.00 to +1.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D1COLOR_MATRIX_SIGN_3_3	31	0x0	Sign bit of combined matrix constant

Combined matrix constant C33 of RGB->YCbCr, contrast and brightness adjustment for primary display.

D1COLOR_MATRIX_COEF_3_4 - RW - 32 bits - DISPDEC:0x63B0			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_MATRIX_COEF_3_4	26:8	0x0	Combined matrix constant C34 of RGB->YCbCr, contrast and brightness adjustment for primary display. Format fix-point S11.1(-2048.5 to +2047.5). It includes subtraction of 512 offset NOTE: Bits 0:6 of this field are hardwired to ZERO.
D1COLOR_MATRIX_SIGN_3_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C34 of RGB->YCbCr, contrast and brightness adjustment for primary display.			

2.7.7 Primary Display Subsampling Registers

D1COLOR_SPACE_CONVERT - RW - 32 bits - DISPDEC:0x613C			
Field Name	**Bits**	**Default**	**Description**
D1COLOR_SUBSAMPLE_CRCB_MODE	1:0	0x0	Sub-sampling control for primary display 0=do not subsample CrCb(RB) 1=subsample CrCb (RB) by using 2 tap average method 2=subsample CrCb (RB) by using 1 tap on even pixel 3=subsample CrCb (RB) by using 1 tap on odd pixel

Sub-sampling control for primary display.

2.7.8 Primary Display Hardware Cursor Registers

D1CUR_CONTROL - RW - 32 bits - DISPDEC:0x6400			
Field Name	**Bits**	**Default**	**Description**
D1CURSOR_EN	0	0x0	Primary display hardware cursor enabled. 0=disable 1=enable
D1CURSOR_MODE	9:8	0x0	Primary display hardware cursor mode. For 2bpp mode, each line of cursor data is stored in memory as 16 bits of AND data followed by 16 bits XOR data. For color AND/XOR mode, each pixel is stored sequentially in memory as 32bits each in aRGB8888 format with bit 31 of each DWord being the AND bit. For the color alpha modes the format is also 32bpp aRGB8888 with all 8 bits of the alpha being used.All HW cursor lines must be 64 pixels wide and all lines must be stored sequentially in memory. 0=Mono (2bpp) 1=Color 24bpp + 1 bit AND (32bpp) 2=Color 24bpp + 8 bit alpha (32bpp) premultiplied alpha 3=Color 24bpp + 8 bit alpha (32bpp)unmultiplied alpha
D1CURSOR_2X_MAGNIFY	16	0x0	Primary display hardware cursor 2x2 magnification. 0=no 2x2 magnification 1=2x2 magnification in horizontal and vertical direction

Primary display hardware control

D1CUR_SURFACE_ADDRESS - RW - 32 bits - DISPDEC:0x6408			
Field Name	**Bits**	**Default**	**Description**
D1CURSOR_SURFACE_ADDRESS	31:0	0x0	Primary display hardware cursor surface base address in byte. It is 4K byte aligned. NOTE: Bits 0:11 of this field are hardwired to ZERO.

Primary display hardware cursor surface base address.

D1CUR_SIZE - RW - 32 bits - DISPDEC:0x6410			
Field Name	**Bits**	**Default**	**Description**
D1CURSOR_HEIGHT	5:0	0x0	Primary display hardware cursor height minus 1.
D1CURSOR_WIDTH	21:16	0x0	Primary display hardware cursor width minus 1.

Primary display hardware size

D1CUR_POSITION - RW - 32 bits - DISPDEC:0x6414			
Field Name	**Bits**	**Default**	**Description**
D1CURSOR_Y_POSITION	12:0	0x0	Primary display hardware cursor X coordinate at the hot spot relative to the desktop coordinates.
D1CURSOR_X_POSITION	28:16	0x0	Primary display hardware cursor X coordinate at the hot spot relative to the desktop coordinates.

Primary display hardware cursor position

D1CUR_HOT_SPOT - RW - 32 bits - DISPDEC:0x6418

Field Name	Bits	Default	Description
D1CURSOR_HOT_SPOT_Y	5:0	0x0	Primary display hardware cursor hot spot X length relative to the top left corner.
D1CURSOR_HOT_SPOT_X	21:16	0x0	Primary display hardware cursor hot spot Y length relative to the top left corner.

Primary display hardware cursor hot spot position

D1CUR_COLOR1 - RW - 32 bits - DISPDEC:0x641C			
Field Name	**Bits**	**Default**	**Description**
D1CUR_COLOR1_BLUE	7:0	0x0	Primary display hardware cursor blue component of color 1.
D1CUR_COLOR1_GREEN	15:8	0x0	Primary display hardware cursor green component of color 1.
D1CUR_COLOR1_RED	23:16	0x0	Primary display hardware cursor red component of color 1.

Primary display hardware cursor color 1.

D1CUR_COLOR2 - RW - 32 bits - DISPDEC:0x6420			
Field Name	**Bits**	**Default**	**Description**
D1CUR_COLOR2_BLUE	7:0	0x0	Primary display hardware cursor blue component of color 2.
D1CUR_COLOR2_GREEN	15:8	0x0	Primary display hardware cursor green component of color 2.
D1CUR_COLOR2_RED	23:16	0x0	Primary display hardware cursor red component of color 2.

Primary display hardware cursor color 2.

D1CUR_UPDATE - RW - 32 bits - DISPDEC:0x6424			
Field Name	**Bits**	**Default**	**Description**
D1CURSOR_UPDATE_PENDING (R)	0	0x0	Primary display hardware cursor update pending status. It is set to 1 after a host write to cursor double buffer register. It is cleared after double buffering is done. The double buffering occurs when D1CURSOR_UPDATE_PENDING = 1 and D1CURSOR_UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC1 is disabled, the registers will be updated instantly. The D1CUR double buffer registers are: D1CURSOR_EN D1CURSOR_MODE D1CURSOR_2X_MAGNIFY D1CURSOR_SURFACE_ADDRESS D1CURSOR_HEIGHT D1CURSOR_WIDTH D1CURSOR_X_POSITION D1CURSOR_Y_POSITION D1CURSOR_HOT_SPOT_X D1CURSOR_HOT_SPOT_Y 0=No update pending 1=Update pending
D1CURSOR_UPDATE_TAKEN (R)	1	0x0	Primary display hardware cursor update taken status. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0
D1CURSOR_UPDATE_LOCK	16	0x0	Primary display hardware cursor update lock control. 0=Unlocked 1=Locked

2.7.9 Primary Display Hardware Icon Registers

D1ICON_CONTROL - RW - 32 bits - DISPDEC:0x6440			
Field Name	**Bits**	**Default**	**Description**
D1ICON_ENABLE	0	0x0	Primary display hardware icon enable. 0=disable 1=enable
D1ICON_2X_MAGNIFY	16	0x0	Primary display hardware icon 2x2 magnification. 0=no 2x2 magnification 1=2x2 magnification in horizontal and vertical direction

Primary display hardware icon control.

D1ICON_SURFACE_ADDRESS - RW - 32 bits - DISPDEC:0x6448			
Field Name	**Bits**	**Default**	**Description**
D1ICON_SURFACE_ADDRESS	31:0	0x0	Primary display hardware icon surface base address in byte. It is 4K byte aligned. NOTE: Bits 0:11 of this field are hardwired to ZERO.

Primary display hardware icon surface base address.

D1ICON_SIZE - RW - 32 bits - DISPDEC:0x6450			
Field Name	**Bits**	**Default**	**Description**
D1ICON_HEIGHT	6:0	0x0	Primary display hardware icon height minus 1.
D1ICON_WIDTH	22:16	0x0	Primary display hardware icon width minus 1.

Primary display hardware icon size.

D1ICON_START_POSITION - RW - 32 bits - DISPDEC:0x6454			
Field Name	**Bits**	**Default**	**Description**
D1ICON_Y_POSITION	12:0	0x0	Primary display hardware icon Y start coordinate related to the desktop coordinates. Note: Icon can not be off the top and off the left edge of the display surface. But can be off the bottom and off the right edge of the display.
D1ICON_X_POSITION	28:16	0x0	Primary display hardware icon X start coordinate relative to the desktop coordinates. Note: Icon can not be off the top and off the left edge of the display surface. But can be off the bottom and off the right edge of the display.

Primary display hardware icon position

D1ICON_COLOR1 - RW - 32 bits - DISPDEC:0x6458			
Field Name	**Bits**	**Default**	**Description**
D1ICON_COLOR1_BLUE	7:0	0x0	Primary display hardware icon blue component of color 1.
D1ICON_COLOR1_GREEN	15:8	0x0	Primary display hardware icon green component of color 1.
D1ICON_COLOR1_RED	23:16	0x0	Primary display hardware icon red component of color 1.

Primary display hardware icon color 1.

D1ICON_COLOR2 - RW - 32 bits - DISPDEC:0x645C			
Field Name	**Bits**	**Default**	**Description**
D1ICON_COLOR2_BLUE	7:0	0x0	Primary display hardware icon blue component of color 2.
D1ICON_COLOR2_GREEN	15:8	0x0	Primary display hardware icon green component of color 2.
D1ICON_COLOR2_RED	23:16	0x0	Primary display hardware icon red component of color 2.

Primary display hardware icon color 2.

D1ICON_UPDATE - RW - 32 bits - DISPDEC:0x6460			
Field Name	**Bits**	**Default**	**Description**
D1ICON_UPDATE_PENDING (R)	0	0x0	Primary display hardware icon update Pending status. It is set to 1 after a host write to icon double buffer register. It is cleared after double buffering is done. The double buffering occurs when D1ICON_UPDATE_PENDING = 1 and D1ICON_UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC1 is disabled, the registers will be updated instantly. D1IOCN double buffer registers include: D1ICON_ENABLE D1ICON_2X_MAGNIFY D1ICON_SURFACE_ADDRESS D1ICON_HEIGHT D1ICON_WIDTH D1ICON_Y_POSITION D1ICON_X_POSITION 0=No update pending 1=Update pending
D1ICON_UPDATE_TAKEN (R)	1	0x0	Primary display hardware icon update Taken status. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0
D1ICON_UPDATE_LOCK	16	0x0	Primary display hardware icon update lock control. 0=Unlocked 1=Locked

Primary display hardware icon update control

2.7.10 Display Look Up Table Control Registers

DC_LUT_RW_SELECT - RW - 32 bits - DISPDEC:0x6480			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_RW_SELECT	0	0x0	LUT host Read/write selection. 0=Host reads/writes to the LUT access the lower half of the LUT 1=Host reads/writes to the LUT access the upper half of the LUT

LUT host Read/write selection.

DC_LUT_RW_MODE - RW - 32 bits - DISPDEC:0x6484			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_RW_MODE	0	0x0	LUT host read/write mode. 0=Host reads/writes to the LUT in 256-entry table mode 1=Host reads/writes to the LUT in piece wise linear (PWL) mode

LUT host read/write mode.

DC_LUT_RW_INDEX - RW - 32 bits - DISPDEC:0x6488			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_RW_INDEX	7:0	0x0	LUT index for host read/write. In 256-entry table mode: LUT_ADDR[6:0] = INDEX[7:1]. INDEX[0] is used to select LUT lower or upper 10 bits. In piece wise linear (PWL) mode: LUT_ADDR[6:0] = INDEX[6:0]. INDEX[7] is not used

LUT index for host read/write.

DC_LUT_SEQ_COLOR - RW - 32 bits - DISPDEC:0x648C			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_SEQ_COLOR	15:0	0x0	Sequential 10-bit R,G,B host read/write for LUT 256-entry table mode. After reset or writing DC_LUT_RW_INDEX register, first DC_LUT_SEQ_COLOR access is for red component, the second one is for green component and the third one is for blue component. Always access this register three times for one LUT entry in LUT 256-entry table mode. The LUT index is increased by 1 when LUT blue data is accessed. This allow you to access the next LUT entry without programming DC_LUT_RW_INDEX again. NOTE: Bits 0:5 of this field are hardwired to ZERO.

Sequential 10-bit R,G,B host read/write for LUT 256-entry table mode.

DC_LUT_PWL_DATA - RW - 32 bits - DISPDEC:0x6490			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_BASE	15:0	0x0	Linear interpolation of base value for host read/write. NOTE: Bits 0:5 of this field are hardwired to ZERO.
DC_LUT_DELTA	31:16	0x0	Linear interpolation of delta value for host read/write. The LUT index is increased by 1 when register DC_LUT_PWL_DATA is accessed. NOTE: Bits 0:5 of this field are hardwired to ZERO.

Linear interpolation of base and delta host read/write for LUT PWL mode

DC_LUT_30_COLOR - RW - 32 bits - DISPDEC:0x6494			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_COLOR_10_BLUE	9:0	0x0	10-bit blue value for host read/write. The LUT index is increased by 1 when register DC_LUT_30_COLOR is accessed.
DC_LUT_COLOR_10_GREEN	19:10	0x0	10-bit green value for host read/write.
DC_LUT_COLOR_10_RED	29:20	0x0	10-bit red value for host read/write.

Host read/write LUT R,G,B value for LUT 256-entry table mode

DC_LUT_READ_PIPE_SELECT - RW - 32 bits - DISPDEC:0x6498			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_READ_PIPE_SELECT	0	0x0	LUT pipe selection for host read. 0=Host read select pipe 0 1=Host read select pipe 1

LUT pipe selection for host read.

DC_LUT_WRITE_EN_MASK - RW - 32 bits - DISPDEC:0x649C			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_WRITE_EN_MASK	5:0	0x3f	Look-up table macro write enable mask for host write. For each bit 0 - host write disable 1 - host write enable Bit[0] - For pipe 1, B macro Bit[1] - For pipe 1, G macro Bit[2] - For pipe 1, R macro Bit[3] - For pipe 0, B macro Bit[4] - For pipe 0, G macro Bit[5] - For pipe 0, R macro

Look-up table macro write enable mask for host write.

DC_LUT_AUTOFILL - RW - 32 bits - DISPDEC:0x64A0			
Field Name	**Bits**	**Default**	**Description**
DC_LUT_AUTOFILL (W)	0	0x0	Enable LUT autofill when 1 is written into this field 0=No effect 1=Start LUT autofill
DC_LUT_AUTOFILL_DONE (R)	1	0x0	LUT autofill is done 0=LUT autofill is not completed 1=LUT autofill is done

LUT autofill control

2.7.11 Display Controller Look Up Table A Registers

DC_LUTA_CONTROL - RW - 32 bits - DISPDEC:0x64C0			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_INC_B	3:0	0x0	Exponent of Power-of-two of blue data increment of LUTA palette. If INC = 0, LUT 256-entry table mode is enabled. LUT_INDEX = PIX_DATA[7:0]. Output = LUT_DATA[LUT_INDEX]. If INC > 0, LUT PWL mode is enabled with 128 entries of base and delta values. LUT_INDEX = PIX_DATA[INC+6:INC]. Mult = PIX_DATA[INC-1:0]. Base = LUT_BASE[LUT_INDEX]. Delta = LUT_DELTA[LUT_INDEX]. Output = Base + (Mult * Delta) / increment 0=Blue data increment = N/A 1=Blue data increment = 2 2=Blue data increment = 4 3=Blue data increment = 8 4=Blue data increment = 16 5=Blue data increment = 32 6=Blue data increment = 64 7=Blue data increment = 128 8=Blue data increment = 256 9=Blue data increment = 512
DC_LUTA_DATA_B_SIGNED_EN	4	0x0	Frame buffer blue data signed enable for look-up table A. 0=Blue data is unsigned 1=Blue data is signed
DC_LUTA_DATA_B_FLOAT_POINT_EN	5	0x0	Frame buffer blue data float point enable for look-up table A. 0=Blue data is fix point 1=Blue data is float point
DC_LUTA_INC_G	11:8	0x0	Exponent of Power-of-two of green data increment of LUTA palette. If INC = 0, LUT 256-entry table mode is enabled. LUT_INDEX = PIX_DATA[7:0]. Output = LUT_DATA[LUT_INDEX]. If INC > 0, LUT PWL mode is enabled with 128 entries of base and delta values. LUT_INDEX = PIX_DATA[INC+6:INC]. Mult = PIX_DATA[INC-1:0]. Base = LUT_BASE[LUT_INDEX]. Delta = LUT_DELTA[LUT_INDEX]. Output = Base + (Mult * Delta) / increment 0=Green data increment = N/A 1=Green data increment = 2 2=Green data increment = 4 3=Green data increment = 8 4=Green data increment = 16 5=Green data increment = 32 6=Green data increment = 64 7=Green data increment = 128 8=Green data increment = 256 9=Green data increment = 512
DC_LUTA_DATA_G_SIGNED_EN	12	0x0	Frame buffer green data signed enable for look-up table A. 0=Green data is unsigned 1=Green data is signed
DC_LUTA_DATA_G_FLOAT_POINT_EN	13	0x0	Frame buffer green data float point enable for look-up table A. 0=Green data is fix point 1=Green data is float point

DC_LUTA_INC_R	19:16	0x0	Exponent of Power-of-two of red data increment of LUTA palette. If INC = 0, LUT 256-entry table mode is enabled. LUT_INDEX = PIX_DATA[7:0]. Output = LUT_DATA[LUT_INDEX]. If INC > 0, LUT PWL mode is enabled with 128 entries of base and delta values. LUT_INDEX = PIX_DATA[INC+6:INC]. Mult = PIX_DATA[INC-1:0]. Base = LUT_BASE[LUT_INDEX]. Delta = LUT_DELTA[LUT_INDEX]. Output = Base + (Mult * Delta) / increment 0=Red data increment = N/A 1=Red data increment = 2 2=Red data increment = 4 3=Red data increment = 8 4=Red data increment = 16 5=Red data increment = 32 6=Red data increment = 64 7=Red data increment = 128 8=Red data increment = 256 9=Red data increment = 512
DC_LUTA_DATA_R_SIGNED_EN	20	0x0	Frame buffer red data signed enable for look-up table A. 0=Red data is unsigned 1=Red data is signed
DC_LUTA_DATA_R_FLOAT_POINT_EN	21	0x0	Frame buffer red data float point enable for look-up table A. 0=Red data is fix point 1=Red data is float point

LUTA mode control

DC_LUTA_BLACK_OFFSET_BLUE - RW - 32 bits - DISPDEC:0x64C4			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_BLACK_OFFSET_BLUE	15:0	0x0	Black value offset of blue component for LUTA.

Black value offset of blue component for LUTA.

DC_LUTA_BLACK_OFFSET_GREEN - RW - 32 bits - DISPDEC:0x64C8			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_BLACK_OFFSET_GREEN	15:0	0x0	Black value offset of green component for LUTA.

Black value offset of green component for LUTA.

DC_LUTA_BLACK_OFFSET_RED - RW - 32 bits - DISPDEC:0x64CC			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_BLACK_OFFSET_RED	15:0	0x0	Black value offset of red component for LUTA.

Black value offset of red component for LUTA.

DC_LUTA_WHITE_OFFSET_BLUE - RW - 32 bits - DISPDEC:0x64D0			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_WHITE_OFFSET_BLUE	15:0	0xffff	White value offset of blue component for LUTA

White value offset of blue component for LUTA.

DC_LUTA_WHITE_OFFSET_GREEN - RW - 32 bits - DISPDEC:0x64D4			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_WHITE_OFFSET_GREEN	15:0	0xffff	White value offset of green component for LUTA

White value offset of green component for LUTA

DC_LUTA_WHITE_OFFSET_RED - RW - 32 bits - DISPDEC:0x64D8			
Field Name	**Bits**	**Default**	**Description**
DC_LUTA_WHITE_OFFSET_RED	15:0	0xffff	White value offset of red component for LUTA

White value offset of red component for LUTA

2.7.12 Secondary Display Graphics Control Registers

D2GRPH_ENABLE - RW - 32 bits - DISPDEC:0x6900			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_ENABLE	0	0x1	Secondary graphic enabled. 0=disable 1=enable

Secondary graphic enabled.

D2GRPH_CONTROL - RW - 32 bits - DISPDEC:0x6904			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_DEPTH	1:0	0x0	Secondary graphic pixel depth. 0=8bpp 1=16bpp 2=32bpp 3=64bpp
D2GRPH_FORMAT	10:8	0x0	Secondary graphic pixel format. It is used together with D2GRPH_DEPTH to define the graphic pixel format. If (D2GRPH_DEPTH = 0x0)(8 bpp) 0x0 - indexed others - reserved else if (D2GRPH_DEPTH = 0x1)(16 bpp) 0x0 - ARGB 1555 0x1 - RGB 565 0x2 - ARGB 4444 0x3 - Alpha index 88 0x4 - monochrome 16 others - reserved else if (D2GRPH_DEPTH = 0x2)(32 bpp) 0x0 - ARGB 8888 0x1 - ARGB 2101010 0x2 - 32bpp digital output 0x3 - 8-bit ARGB 2101010 others - reserved else if (D2GRPH_DEPTH = 0x3)(64 bpp) 0x0 - ARGB 16161616 0x1 - 64bpp digital output ARGB[13:2] 0x2 - 64bpp digital output RGB[15:0] 0x3 - 64bpp digital output ARGB[11:0] others - reserved
D2GRPH_SWAP_RB	16	0x0	Secondary graphic pixel format R and B swap 0=no swap 1=swap R and B
D2GRPH_TILED	20	0x1	0=Linear surface 1=Tiled surface
D2GRPH_MACRO_ADDRESS_MODE	21	0x0	Sets macro addressing mode when D2GRPH_TILED = 0 (micro linear mode). This field is don't care when D2GRPH_TILED = 1 (micro tiled mode). Display does not support macro-linear and micro-tiled surfaces. When D2GRPH_TILED = 1, addressing mode is macro-tiled and micro-tiled. 0=macro-linear (and micro-linear) 1=macro-tiled (and micro-linear)

D2GRPH_16BIT_ALPHA_MODE	25:24	0x0	This field is only used if 64 bpp graphics bit depth and graphics/overlay blend using per-pixel alpha from graphics channel. It is used for processing 16 bit alpha. The fixed point graphics alpha value in the frame buffer is always clamped to 0.0 - 1.0 data range. 0x0 - Floating point alpha (1 sign bit, 5 bit exponent, 10 bit mantissa) 0x1 - Fixed point alpha with normalization from 256/256 to 255/255 to represent 1.0 0x2 - Fixed point alpha with no normalization 0x3 - Fixed point alpha using lower 8 bits of frame buffer value, no normalization
D2GRPH_16BIT_FIXED_ALPHA_RANGE	30:28	0x0	This register field is only used if 64 bpp graphics bit depth and D2GRPH_16BIT_ALPHA_MODE = 01 or 10. Also only used if graphics/overlay blend using per-pixel alpha from graphics channel. Final alpha blend value is rounded to 8 bits after optional normalization step (see D2GRPH_16BIT_ALPHA_MODE). 0x0 - Use bits 15:0 of input alpha value for blend alpha 0x1 - Use bits 14:0 of input alpha value for blend alpha 0x2 - Use bits 13:0 of input alpha value for blend alpha 0x3 - Use bits 12:0 of input alpha value for blend alpha 0x4 - Use bits 11:0 of input alpha value for blend alpha 0x5 - Use bits 10:0 of input alpha value for blend alpha 0x6 - Use bits 9:0 of input alpha value for blend alpha 0x7 - Use bits 8:0 of input alpha value for blend alpha

Secondary graphic pixel depth and format.

D2GRPH_LUT_SEL - RW - 32 bits - DISPDEC:0x6908			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_LUT_SEL	0	0x0	Secondary graphic LUT selection. 0=select LUTA 1=select LUTB
D2GRPH_LUT_10BIT_BYPASS_EN	8	0x0	Enable bypass secondary graphic LUT for 2101010 format 0=Use LUT 1=Bypass LUT when in 2101010 format. Ignored for other formats
D2GRPH_LUT_10BIT_BYPASS_DBL_BUF_EN	16	0x0	Enable double buffer D2GRPH_LUT_10BIT_BYPASS_EN 0=D1GRPH_LUT_10BIT_BYPASS_EN take effect right away 1=D1GRPH_LUT_10BIT_BYPASS_EN are double buffered

Secondary graphic LUT selection.

D2GRPH_PRIMARY_SURFACE_ADDRESS - RW - 32 bits - DISPDEC:0x6910			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_PRIMARY_SURFACE_ADDRESS	31:0	0x0	Secondary surface address for secondary graphics in byte. It is 4K byte aligned. NOTE: Bits 0:10 of this field are hardwired to ZERO.

Secondary surface address for secondary graphics in byte.

D2GRPH_SECONDARY_SURFACE_ADDRESS - RW - 32 bits - DISPDEC:0x6918			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_SECONDARY_SURFACE_ADDRESS	31:0	0x0	Secondary surface address for secondary graphics in byte. It is 4K byte aligned. NOTE: Bits 0:10 of this field are hardwired to ZERO.
Secondary surface address for secondary graphics in byte.			

D2GRPH_PITCH - RW - 32 bits - DISPDEC:0x6920			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_PITCH	13:0	0x0	Secondary graphic surface pitch in pixels. For Micro-tiled/Macro-tiled surface, it must be multiple of 64 pixeld in 8bpp mode. For Micro-linear/Macro-tiled surface, it must be multiple of 256 pixeld in 8bpp mode, multiple of 128 pixels in 16bpp mode and multiple of 64 pixels in 32bpp mode. For Micro-linear/Macro-linear surface, it must be multiple of 64 pixels in 8bpp mode. For other modes, it must be multiple of 32. NOTE: Bits 0:4 of this field are hardwired to ZERO.
Secondary graphic surface pitch in pixels.			

D2GRPH_SURFACE_OFFSET_X - RW - 32 bits - DISPDEC:0x6924			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_SURFACE_OFFSET_X	12:0	0x0	Secondary graphic X surface offset. It is 256 pixels aligned. NOTE: Bits 0:7 of this field are hardwired to ZERO.
Secondary graphic X surface offset.			

D2GRPH_SURFACE_OFFSET_Y - RW - 32 bits - DISPDEC:0x6928			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_SURFACE_OFFSET_Y	12:0	0x0	Secondary graphic Y surface offset. It must be even value NOTE: Bit 0 of this field is hardwired to ZERO.
Secondary graphic Y surface offset.			

D2GRPH_X_START - RW - 32 bits - DISPDEC:0x692C			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_X_START	12:0	0x0	Secondary graphic X start coordinate relative to the desktop coordinates.
Secondary graphic X start coordinate relative to the desktop coordinates.			

D2GRPH_Y_START - RW - 32 bits - DISPDEC:0x6930			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_Y_START	12:0	0x0	Secondary graphic Y start coordinate relative to the desktop coordinates.

Secondary graphic Y start coordinate relative to the desktop coordinates.

D2GRPH_X_END - RW - 32 bits - DISPDEC:0x6934			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_X_END	13:0	0x0	Secondary graphic X end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K

Secondary graphic X end coordinate relative to the desktop coordinates.

D2GRPH_Y_END - RW - 32 bits - DISPDEC:0x6938			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_Y_END	13:0	0x0	Secondary graphic Y end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K

Secondary graphic Y end coordinate relative to the desktop coordinates.

D2GRPH_UPDATE - RW - 32 bits - DISPDEC:0x6944			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_MODE_UPDATE_PENDING (R)	0	0x0	Secondary graphic mode register update pending control. It is set to 1 after a host write to graphics mode register. It is cleared after double buffering is done. This signal is only visible through register. The graphics surface register includes: D2GRPH_DEPTH D2GRPH_FORMAT D2GRPH_SWAP_RB D2GRPH_LUT_SEL D2GRPH_LUT_10BIT_BYPASS_EN D2GRPH_ENABLE D2GRPH_X_START D2GRPH_Y_START D2GRPH_X_END D2GRPH_Y_END The mode register double buffering can only occur at vertical retrace. The double buffering occurs when D2GRPH_MODE_UPDATE_PENDING = 1 and D2GRPH_UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC2 is disabled, the registers will be updated instantly. 0=No update pending 1=Update pending
D2GRPH_MODE_UPDATE_TAKEN (R)	1	0x0	Secondary graphics update taken status for mode registers. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0.

D2GRPH_SURFACE_UPDATE_PENDING (R)	2	0x0	Secondary graphic surface register update pending control. If it is set to 1 after a host write to graphics surface register. It is cleared after double buffering is done. It is cleared after double buffering is done. This signal also goes to both the RBBM wait_until and to the CP_RTS_discrete inputs. The graphics surface register includes: D2GRPH_PRIMARY_SURFACE_ADDRESS D2GRPH_SECONDARY_SURFACE_ADDRESS D2GRPH_PITCH D2GRPH_SURFACE_OFFSET_X D2GRPH_SURFACE_OFFSET_Y. If D2GRPH_SURFACE_UPDATE_H_RETRACE_EN = 0, the double buffering occurs in vertical retrace when D2GRPH_SURFACE_UPDATE_PENDING = 1 and D2GRPH_UPDATE_LOCK = 0 and V_UPDATE = 1. Otherwise the double buffering happens at horizontal retrace when D2GRPH_SURFACE_UPDATE_PENDING = 1 and D2GRPH_UPDATE_LOCK = 0 and Data request for last chunk of the line is sent from DCP to DMIF. If CRTC2 is disabled, the registers will be updated instantly.
D2GRPH_SURFACE_UPDATE_TAKEN (R)	3	0x0	Secondary graphics update taken status for surface registers. If D2GRPH_SURFACE_UPDATE_H_RETRACE_EN = 0, it is set to 1 when double buffering occurs and cleared when V_UPDATE = 0. Otherwise, it is active for one clock cycle when double buffering occurs at the horizontal retrace.
D2GRPH_UPDATE_LOCK	16	0x0	Secondary graphic register update lock control. This lock bit control both surface and mode register double buffer 0=Unlocked 1=Locked

Secondary graphic update control

D2GRPH_FLIP_CONTROL - RW - 32 bits - DISPDEC:0x6948			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_SURFACE_UPDATE_H_RETRACE_EN	0	0x0	Enable secondary graphic surface register double buffer in horizontal retrace. 0=Vertical retrace flipping 1=Horizontal retrace flipping

Enable secondary graphic surface register double buffer in horizontal retrace

D2GRPH_SURFACE_ADDRESS_INUSE - RW - 32 bits - DISPDEC:0x694C			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_SURFACE_ADDRESS_INUSE (R)	31:11	0x0	This register reads back snapshot of secondary graphics surface address used for data request. The address is the signal sent to DMIF and is updated on SOF or horizontal surface update. The snapshot is triggered by writing 1 into field D1CRTC_SNAPSHOT_MANUAL_TRIGGER of CRTC register D1CRTC_SNAPSHOT_STATUS.

Snapshot of secondary graphics surface address in use

2.7.13 Secondary Display Video Overlay Control Registers

D2OVL_ENABLE - RW - 32 bits - DISPDEC:0x6980			
Field Name	**Bits**	**Default**	**Description**
D2OVL_ENABLE	0	0x0	Secondary overlay enabled. 0=disable 1=enable

Secondary overlay enabled.

D2OVL_CONTROL1 - RW - 32 bits - DISPDEC:0x6984			
Field Name	**Bits**	**Default**	**Description**
D2OVL_DEPTH	1:0	0x0	Secondary overlay pixel depth 0=reserved 1=16bpp 2=32bpp 3=reserved
D2OVL_FORMAT	10:8	0x0	Secondary overlay pixel format. It is used together with D2OVL_DEPTH to define the overlay format. If (D2OVL_DEPTH = 0x1)(16 bpp) 0x0- ARGB 1555 0x1 - RGB 565 others - reserved else if (D2OVL_DEPTH = 0x2)(32 bpp) 0x0 - ACrYCb 8888 or ARGB 8888 0x1 - ACrYCb 2101010 or ARGB 2101010 others - reserved
D2OVL_SWAP_RB	16	0x0	Secondary overlay pixel format R and B swap 0=no swap 1=swap R and B
D2OVL_TILED	20	0x1	0=Reserved 1=Tiled surface
D2OVL_MACRO_ADDRESS_MODE	21	0x0	Sets macro addressing mode when D2OVL_TILED = 0 (micro linear mode). This field is don't care when D2OVL_TILED = 1 (micro tiled mode). Display does not support macro-linear and micro-tiled surfaces. When D2OVL_TILED = 1, addressing mode is macro-tiled and micro-tiled. 0=macro-linear (and micro-linear) 1=macro-tiled (and micro-linear)
D2OVL_COLOR_EXPANSION_MODE	24	0x0	Secondary overlay pixel format expansion mode. 0=dynamic expansion for RGB 1=zero expansion for YCbCr

Secondary overlay pixel depth and format.

D2OVL_CONTROL2 - RW - 32 bits - DISPDEC:0x6988			
Field Name	**Bits**	**Default**	**Description**
D2OVL_HALF_RESOLUTION_ENABLE	0	0x0	Secondary overlay half resolution control 0=disable 1=enable

Secondary overlay half resolution control

D2OVL_SURFACE_ADDRESS - RW - 32 bits - DISPDEC:0x6990

Field Name	Bits	Default	Description
D2OVL_SURFACE_ADDRESS	31:0	0x0	Secondary overlay surface base address in byte. It is 4K bytes aligned. NOTE: Bits 0:10 of this field are hardwired to ZERO.

Secondary overlay surface base address in byte.

D2OVL_PITCH - RW - 32 bits - DISPDEC:0x6998			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PITCH	13:0	0x0	Secondary overlay surface pitch in pixels. For Micro-tiled/Macro-tiled surface, it must be multiple of 64 pixeld in 8bpp mode. For Micro-linear/Macro-tiled surface, it must be multiple of 256 pixeld in 8bpp mode, multiple of 128 pixels in 16bpp mode and multiple of 64 pixels in 32bpp mode. For Micro-linear/Macro-linear surface, it must be multiple of 64 pixels in 8bpp mode. For other modes, it must be multiple of 32. NOTE: Bits 0:4 of this field are hardwired to ZERO.

Secondary overlay surface pitch in pixels.

D2OVL_SURFACE_OFFSET_X - RW - 32 bits - DISPDEC:0x699C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_SURFACE_OFFSET_X	12:0	0x0	Secondary overlay X surface offset. It is 256 pixels aligned. NOTE: Bits 0:7 of this field are hardwired to ZERO.

Secondary overlay X surface offset.

D2OVL_SURFACE_OFFSET_Y - RW - 32 bits - DISPDEC:0x69A0			
Field Name	**Bits**	**Default**	**Description**
D2OVL_SURFACE_OFFSET_Y	12:0	0x0	Secondary overlay Y surface offset. It is even value. NOTE: Bit 0 of this field is hardwired to ZERO.

Secondary overlay Y surface offset.

D2OVL_START - RW - 32 bits - DISPDEC:0x69A4			
Field Name	**Bits**	**Default**	**Description**
D2OVL_Y_START	12:0	0x0	Secondary overlay Y start coordinate relative to the desktop coordinates.
D2OVL_X_START	28:16	0x0	Secondary overlay X start coordinate relative to the desktop coordinates.

Secondary overlay X, Y start coordinate relative to the desktop coordinates.

D2OVL_END - RW - 32 bits - DISPDEC:0x69A8			
Field Name	**Bits**	**Default**	**Description**
D2OVL_Y_END	13:0	0x0	Secondary overlay Y end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K
D2OVL_X_END	29:16	0x0	Secondary overlay X end coordinate relative to the desktop coordinates. It is exclusive and the maximum value is 8K

Secondary overlay X, Y end coordinate relative to the desktop coordinates.

D2OVL_UPDATE - RW - 32 bits - DISPDEC:0x69AC			
Field Name	**Bits**	**Default**	**Description**
D2OVL_UPDATE_PENDING (R)	0	0x0	Secondary overlay register update pending control. It is set to 1 after a host write to overlay double buffer register. It is cleared after double buffering is done. The double buffering occurs when UPDATE_PENDING = 1 and UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC2 is disabled, the registers will be updated instantly. D2OVL double buffer registers include: D2OVL_ENABLE D2OVL_DEPTH D2OVL_FORMAT D2OVL_SWAP_RB D2OVL_COLOR_EXPANSION_MODE D2OVL_HALF_RESOLUTION_ENABLE D2OVL_SURFACE_ADDRESS D2OVL_PITCH D2OVL_SURFACE_OFFSET_X D2OVL_SURFACE_OFFSET_Y D2OVL_START D2OVL_END 0=No update pending 1=Update pending
D2OVL_UPDATE_TAKEN (R)	1	0x0	Secondary overlay update taken status. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0.
D2OVL_UPDATE_LOCK	16	0x0	Secondary overlay register update lock control. 0=Unlocked 1=Locked

Secondary overlay register update

D2OVL_SURFACE_ADDRESS_INUSE - RW - 32 bits - DISPDEC:0x69B0			
Field Name	**Bits**	**Default**	**Description**
D2OVL_SURFACE_ADDRESS_INUSE (R)	31:11	0x0	This register reads back snapshot of secondary overlay surface address used for data request. The address is the signal sent to DMIF and is updated on SOF or horizontal surface update. The snapshot is triggered by writing 1 into field D1CRTC_SNAPSHOT_MANUAL_TRIGGER of CRTC register D1CRTC_SNAPSHOT_STATUS.

Snapshot of secondary overlay surface address in use

2.7.14 Secondary Display Video Overlay Transform Registers

D2OVL_MATRIX_TRANSFORM_EN - RW - 32 bits - DISPDEC:0x6A00			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_TRANSFORM_EN	0	0x0	Secondary overlay matrix conversion enable 0=disable 1=enable

Secondary overlay matrix conversion enable.

D2OVL_MATRIX_COEF_1_1 - RW - 32 bits - DISPDEC:0x6A04			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_1_1	18:0	0x198a0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2OVL_MATRIX_SIGN_1_1	31	0x0	Sign bit of combined matrix constant

Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.

D2OVL_MATRIX_COEF_1_2 - RW - 32 bits - DISPDEC:0x6A08			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_1_2	18:0	0x12a20	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2OVL_MATRIX_SIGN_1_2	31	0x0	Sign bit of combined matrix constant

Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.

D2OVL_MATRIX_COEF_1_3 - RW - 32 bits - DISPDEC:0x6A0C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_1_3	18:0	0x0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2OVL_MATRIX_SIGN_1_3	31	0x0	Sign bit of combined matrix constant

Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.

D2OVL_MATRIX_COEF_1_4 - RW - 32 bits - DISPDEC:0x6A10			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_1_4	26:8	0x48700	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S11.1. NOTE: Bits 0:6 of this field are hardwired to ZERO.
D2OVL_MATRIX_SIGN_1_4	31	0x1	Sign bit of combined matrix constant

Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.

D2OVL_MATRIX_COEF_2_1 - RW - 32 bits - DISPDEC:0x6A14			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_2_1	18:0	0x72fe0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2OVL_MATRIX_SIGN_2_1	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_2_2 - RW - 32 bits - DISPDEC:0x6A18			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_2_2	18:0	0x12a20	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2OVL_MATRIX_SIGN_2_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_2_3 - RW - 32 bits - DISPDEC:0x6A1C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_2_3	18:0	0x79bc0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2OVL_MATRIX_SIGN_2_3	31	0x1	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_2_4 - RW - 32 bits - DISPDEC:0x6A20			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_2_4	26:8	0x22100	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S11.1. NOTE: Bits 0:6 of this field are hardwired to ZERO.
D2OVL_MATRIX_SIGN_2_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_3_1 - RW - 32 bits - DISPDEC:0x6A24			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_3_1	18:0	0x0	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2OVL_MATRIX_SIGN_3_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.			

D2OVL_MATRIX_COEF_3_2 - RW - 32 bits - DISPDEC:0x6A28

Field Name	Bits	Default	Description
D2OVL_MATRIX_COEF_3_2	18:0	0x12a20	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2OVL_MATRIX_SIGN_3_2	31	0x0	Sign bit of combined matrix constant

Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.

D2OVL_MATRIX_COEF_3_3 - RW - 32 bits - DISPDEC:0x6A2C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_3_3	18:0	0x20460	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S3.11. NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2OVL_MATRIX_SIGN_3_3	31	0x0	Sign bit of combined matrix constant

Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.

D2OVL_MATRIX_COEF_3_4 - RW - 32 bits - DISPDEC:0x6A30			
Field Name	**Bits**	**Default**	**Description**
D2OVL_MATRIX_COEF_3_4	26:8	0x3af80	Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay. Format fix-point S11.1. NOTE: Bits 0:6 of this field are hardwired to ZERO.
D2OVL_MATRIX_SIGN_3_4	31	0x1	Sign bit of combined matrix constant

Combined matrix constant of YCbCr->RGB, contrast and brightness adjustment for secondary overlay.

2.7.15 Secondary Display Video Overlay Gamma Correction Registers

D2OVL_PWL_TRANSFORM_EN - RW - 32 bits - DISPDEC:0x6A80			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_TRANSFORM_EN	0	0x0	Secondary overlay gamma correction enable. 0=disable 1=enable

Secondary overlay gamma correction enable.

D2OVL_PWL_0TOF - RW - 32 bits - DISPDEC:0x6A84			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_0TOF_OFFSET	8:0	0x0	Secondary overlay gamma correction non-linear offset for input 0x0-0xF. Format fix-point 8.1 (0.0 to +255.5).
D2OVL_PWL_0TOF_SLOPE	26:16	0x100	Secondary overlay gamma correction non-linear slope for input 0x0-0xF. Format fix-point 3.8 (0.00 to +7.99).

Secondary overlay gamma correction non-linear offset and slope for input 0x0-0xF

D2OVL_PWL_10TO1F - RW - 32 bits - DISPDEC:0x6A88			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_10TO1F_OFFSET	8:0	0x20	Secondary overlay gamma correction non-linear offset for input 0x10-0x1F. Format fix-point 8.1 (0.0 to +255.5).
D2OVL_PWL_10TO1F_SLOPE	26:16	0x100	Secondary overlay gamma correction non-linear slope for input 0x10-0x1F. Format fix-point 3.8 (0.00 to +7.99).

Secondary overlay gamma correction non-linear offset and slope for input 0x10-0x1F

D2OVL_PWL_20TO3F - RW - 32 bits - DISPDEC:0x6A8C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_20TO3F_OFFSET	9:0	0x40	Secondary overlay gamma correction non-linear offset for input 0x20-0x3F. Format fix-point 9.1 (0.0 to +511.5).
D2OVL_PWL_20TO3F_SLOPE	25:16	0x100	Secondary overlay gamma correction non-linear slope for input 0x20-0x3F. Format fix-point 2.8 (0.00 to +3.99).

Secondary overlay gamma correction non-linear offset and slope for input 0x20-0x3F

D2OVL_PWL_40TO7F - RW - 32 bits - DISPDEC:0x6A90			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_40TO7F_OFFSET	9:0	0x80	Secondary overlay gamma correction non-linear offset for input 40-7F. Format fix-point 9.1 (0.0 to +511.5).
D2OVL_PWL_40TO7F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 40-7F. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 40-7F.

D2OVL_PWL_80TOBF - RW - 32 bits - DISPDEC:0x6A94			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_80TOBF_OFFSET	10:0	0x100	Secondary overlay gamma correction non-linear offset for input 80-BF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_80TOBF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 80-BF. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 80-BF.

D2OVL_PWL_C0TOFF - RW - 32 bits - DISPDEC:0x6A98			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_C0TOFF_OFFSET	10:0	0x180	Secondary overlay gamma correction non-linear offset for input C0-FF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_C0TOFF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input C0-FF. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input C0-FF.

D2OVL_PWL_100TO13F - RW - 32 bits - DISPDEC:0x6A9C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_100TO13F_OFFSET	10:0	0x200	Secondary overlay gamma correction non-linear offset for input 100-13F. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_100TO13F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 100-13F. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 100-13F.

D2OVL_PWL_140TO17F - RW - 32 bits - DISPDEC:0x6AA0			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_140TO17F_OFFSET	10:0	0x280	Secondary overlay gamma correction non-linear offset for input 140-17F. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_140TO17F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 140-17F. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 140-17F.

D2OVL_PWL_180TO1BF - RW - 32 bits - DISPDEC:0x6AA4			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_180TO1BF_OFFSET	10:0	0x300	Secondary overlay gamma correction non-linear offset for input 180-1BF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_180TO1BF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 180-1BF. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 180-1BF.

D2OVL_PWL_1C0TO1FF - RW - 32 bits - DISPDEC:0x6AA8			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_1C0TO1FF_OFFSET	10:0	0x380	Secondary overlay gamma correction non-linear offset for input 1C0-1FF. Format fix-point 10.1 (0.0 to +1023.5).

D2OVL_PWL_1C0TO1FF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 1C0-1FF. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 1C0-1FF.

D2OVL_PWL_200TO23F - RW - 32 bits - DISPDEC:0x6AAC			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_200TO23F_OFFSET	10:0	0x400	Secondary overlay gamma correction non-linear offset for input 200-23F. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_200TO23F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 200-23F. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 200-23F.

D2OVL_PWL_240TO27F - RW - 32 bits - DISPDEC:0x6AB0			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_240TO27F_OFFSET	10:0	0x480	Secondary overlay gamma correction non-linear offset for input 240-27F. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_240TO27F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 240-27F. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 240-27F.

D2OVL_PWL_280TO2BF - RW - 32 bits - DISPDEC:0x6AB4			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_280TO2BF_OFFSET	10:0	0x500	Secondary overlay gamma correction non-linear offset for input 280-2BF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_280TO2BF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 280-2BF. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 280-2BF.

D2OVL_PWL_2C0TO2FF - RW - 32 bits - DISPDEC:0x6AB8			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_2C0TO2FF_OFFSET	10:0	0x580	Secondary overlay gamma correction non-linear offset for input 2C0-2FF. Format fix-point 10.1(0.0 to +1023.5).
D2OVL_PWL_2C0TO2FF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 2C0-2FF. Format fix-point 1.8(0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 2C0-2FF.

D2OVL_PWL_300TO33F - RW - 32 bits - DISPDEC:0x6ABC			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_300TO33F_OFFSET	10:0	0x600	Secondary overlay gamma correction non-linear offset for input 300-33F. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_300TO33F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 300-33F. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 300-33F.

D2OVL_PWL_340TO37F - RW - 32 bits - DISPDEC:0x6AC0			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_340TO37F_OFFSET	10:0	0x680	Secondary overlay gamma correction non-linear offset for input 340-37F. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_340TO37F_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 340-37F. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 340-37F.

D2OVL_PWL_380TO3BF - RW - 32 bits - DISPDEC:0x6AC4			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_380TO3BF_OFFSET	10:0	0x700	Secondary overlay gamma correction non-linear offset for input 380-3BF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_380TO3BF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 380-3BF. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 380-3BF.

D2OVL_PWL_3C0TO3FF - RW - 32 bits - DISPDEC:0x6AC8			
Field Name	**Bits**	**Default**	**Description**
D2OVL_PWL_3C0TO3FF_OFFSET	10:0	0x780	Secondary overlay gamma correction non-linear offset for input 3C0-3FF. Format fix-point 10.1 (0.0 to +1023.5).
D2OVL_PWL_3C0TO3FF_SLOPE	24:16	0x100	Secondary overlay gamma correction non-linear slope for input 3C0-3FF. Format fix-point 1.8 (0.00 to +1.99).

Secondary overlay gamma correction non-linear offset and slope for input 3C0-3FF.

2.7.16 Secondary Display Graphics and Overlay Blending Registers

D2OVL_KEY_CONTROL - RW - 32 bits - DISPDEC:0x6B00			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_KEY_FUNCTION	1:0	0x0	Selects graphic keyer result equation for secondary display. 0=GRPH2_KEY = FALSE = 0 1=GRPH2_KEY = TRUE = 1 2=GPPH2_KEY = (GRPH2_RED in range) AND (GRPH2_GREEN in range) AND (GRPH2_BLUE in range) AND (GRPH2_ALPHA in range) 3=GRPH2_KEY = not [(GRPH2_RED in range) AND (GRPH2_GREEN in range) AND (GRPH2_BLUE in range) AND (GRPH2_ALPHA in range)]
D2OVL_KEY_FUNCTION	9:8	0x0	Selects overlay keyer result equation for secondary display. 0=OVL2_KEY = FALSE = 0 1=OVL2_KEY = TRUE = 1 2=OVL2_KEY = (OVL2_Cr_RED in range) AND (OVL2_Y_GREEN in range) AND (OVL2_Cb_BLUE in range) AND (OVL2_ALPHA in range) 3=OVL2_KEY = not [(OVL2_Cr_RED in range) AND (OVL2_Y_GREEN in range) AND (OVL2_Cb_BLUE in range) AND (OVL2_ALPHA in range)]
D2OVL_KEY_COMPARE_MIX	16	0x0	Selects final mix of graphics and overlay keys for secondary display. 0=GRPH_OVL_KEY = GRPH_KEY or OVL_KEY 1=GRPH_OVL_KEY = GRPH_KEY and OVL_KEY

Secondary display key control

D2GRPH_ALPHA - RW - 32 bits - DISPDEC:0x6B04			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_ALPHA	7:0	0xff	Global graphic alpha for use in key mode and global alpha modes. See D2OVL_ALPHA_MODE register filed for more details

Global graphic alpha for use in key mode and global alpha modes.

D2OVL_ALPHA - RW - 32 bits - DISPDEC:0x6B08			
Field Name	**Bits**	**Default**	**Description**
D2OVL_ALPHA	7:0	0xff	Global overlay alpha for use in key mode and global alpha modes. See D2OVL_ALPHA_MODE register filed for more details

Global overlay alpha for use in key mode and global alpha modes.

D2OVL_ALPHA_CONTROL - RW - 32 bits - DISPDEC:0x6B0C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_ALPHA_MODE	1:0	0x0	Graphics/overlay alpha blending mode for secondary controller. In any case, if there is only graphics, the input OVL_DATA is forced to blank. If there is only overlay, the input GRPH_DATA is forced to blank. 0=Keyer mode, select graphic or overlay keyer to mix graphics and overlay 1=Per pixel graphic alpha mode.Alpha blend graphic and overlay layer. The alpha from graphic pixel may be inverted according to register field 2=Global alpha mode 3=Per pixel overlay alpha mode
D2OVL_ALPHA_PREMULT	8	0x0	For use with per pixel alpha blend mode. Selects whether pre-multiplied alpha or non-multiplied alpha. 0=0x0 - When DxOVL_ALPHA_MODE = 0x1, then Pixel = PIX_ALPHA * graphics pixel + (1-PIX_ALPHA) * overlay pixel.When DxOVL_ALPHA_MODE = 0x3, then Pixel = PIX_ALPHA * overlay pixel + (1-PIX_ALPHA) * graphic pixel 1=0x1 - When DxOVL_ALPHA_MODE = 0x1, then Pixel = graphic pixel + (1-PIX_ALPHA) * overlay pixel.When DxOVL_ALPHA_MODE = 0x3, then Pixel = overlay pixel + (1-PIX_ALPHA) * graphic pixel
D2OVL_ALPHA_INV	16	0x0	For use with pixel blend mode. Apply optional inversion to the alpha value extracted form the graphics or overlay surface data. 0=PIX_ALPHA = alpha from graphics or overlay 1=PIX_ALPHA = 1 - alpha from graphics or overlay

Secondary display graphics/overlay alpha blending control

D2GRPH_KEY_RANGE_RED - RW - 32 bits - DISPDEC:0x6B10			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_KEY_RED_LOW	15:0	0x0	Secondary graphics keyer red component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D2GRPH_KEY_RED_HIGH	31:16	0x0	Secondary graphics keyer red component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.

Secondary graphics keyer red component range

D2GRPH_KEY_RANGE_GREEN - RW - 32 bits - DISPDEC:0x6B14			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_KEY_GREEN_LOW	15:0	0x0	Secondary graphics keyer green component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D2GRPH_KEY_GREEN_HIGH	31:16	0x0	Secondary graphics keyer green component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.

Secondary graphics keyer green component range

D2GRPH_KEY_RANGE_BLUE - RW - 32 bits - DISPDEC:0x6B18			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_KEY_BLUE_LOW	15:0	0x0	Secondary graphics keyer blue component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D2GRPH_KEY_BLUE_HIGH	31:16	0x0	Secondary graphics keyer blue component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.

Secondary graphics keyer blue component range

D2GRPH_KEY_RANGE_ALPHA - RW - 32 bits - DISPDEC:0x6B1C			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_KEY_ALPHA_LOW	15:0	0x0	Secondary graphics keyer alpha component lower limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.
D2GRPH_KEY_ALPHA_HIGH	31:16	0x0	Secondary graphics keyer alpha component upper limit. Note: If the graphic component is less than 16 bit, msbs are all zeros.

Secondary graphics keyer alpha component range

D2OVL_KEY_RANGE_RED_CR - RW - 32 bits - DISPDEC:0x6B20			
Field Name	**Bits**	**Default**	**Description**
D2OVL_KEY_RED_CR_LOW	9:0	0x0	Secondary overlay keyer red component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D2OVL_KEY_RED_CR_HIGH	25:16	0x0	Secondary overlay keyer red component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.

Secondary overlay keyer red component range

D2OVL_KEY_RANGE_GREEN_Y - RW - 32 bits - DISPDEC:0x6B24			
Field Name	**Bits**	**Default**	**Description**
D2OVL_KEY_GREEN_Y_LOW	9:0	0x0	Secondary overlay keyer green component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D2OVL_KEY_GREEN_Y_HIGH	25:16	0x0	Secondary overlay keyer green component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.

Secondary overlay keyer green component range

D2OVL_KEY_RANGE_BLUE_CB - RW - 32 bits - DISPDEC:0x6B28			
Field Name	**Bits**	**Default**	**Description**
D2OVL_KEY_BLUE_CB_LOW	9:0	0x0	Secondary overlay keyer blue component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D2OVL_KEY_BLUE_CB_HIGH	25:16	0x0	Secondary overlay keyer blue component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.

Secondary overlay keyer blue component range

D2OVL_KEY_ALPHA - RW - 32 bits - DISPDEC:0x6B2C			
Field Name	**Bits**	**Default**	**Description**
D2OVL_KEY_ALPHA_LOW	7:0	0x0	Secondary overlay keyer alpha component lower limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.
D2OVL_KEY_ALPHA_HIGH	23:16	0x0	Secondary overlay keyer alpha component upper limit. Note: If the overlay component is less than 16 bit, msbs are all zeros.

Secondary overlay keyer alpha component range

2.7.17 Secondary Display Color Matrix Transform Registers

D2GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL - RW - 32 bits - DISPDEC:0x6B80			
Field Name	**Bits**	**Default**	**Description**
D2GRPH_COLOR_MATRIX_TRANSFORMATION_EN	0	0x0	Matrix transformation control for secondary display graphics and cursor pixel. It is used when PIX_TYPE is 1. 0=disable 1=enable

Matrix transformation control for secondary display graphics and cursor pixel.

D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL - RW - 32 bits - DISPDEC:0x6940			
Field Name	**Bits**	**Default**	**Description**
D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	2:0	0x0	Matrix transformation control for secondary display overlay pixels. It is used when PIX_TYPE is 0.

Matrix transformation control for secondary display overlay pixels.

D2COLOR_MATRIX_COEF_1_1 - RW - 32 bits - DISPDEC:0x6B84			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_1_1	16:0	0x0	Combined matrix constant C11 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S1.11(-2.00 to +1.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2COLOR_MATRIX_SIGN_1_1	31	0x0	Sign bit of combined matrix constant

Combined matrix constant C11 of RGB->YCbCr, contrast and brightness adjustment for secondary display.

D2COLOR_MATRIX_COEF_1_2 - RW - 32 bits - DISPDEC:0x6B88			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_1_2	15:0	0x0	Combined matrix constant C12 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S0.11(-1.00 to + 0.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2COLOR_MATRIX_SIGN_1_2	31	0x0	Sign bit of combined matrix constant

Combined matrix constant C12 of RGB->YCbCr, contrast and brightness adjustment for secondary display.

D2COLOR_MATRIX_COEF_1_3 - RW - 32 bits - DISPDEC:0x6B8C			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_1_3	15:0	0x0	Combined matrix constant C13 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S0.11(-1.0 to +0.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2COLOR_MATRIX_SIGN_1_3	31	0x0	Sign bit of combined matrix constant

Combined matrix constant C13 of RGB->YCbCr, contrast and brightness adjustment for secondary display.

D2COLOR_MATRIX_COEF_1_4 - RW - 32 bits - DISPDEC:0x6B90			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_1_4	26:8	0x0	Combined matrix constant C14 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S11.1(-2048.5 to +2047.5). It includes subtraction of 512 offset NOTE: Bits 0:6 of this field are hardwired to ZERO.
D2COLOR_MATRIX_SIGN_1_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C14 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_2_1 - RW - 32 bits - DISPDEC:0x6B94			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_2_1	15:0	0x0	Combined matrix constant C21 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S0.11(-1.00 to +0.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2COLOR_MATRIX_SIGN_2_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C21 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_2_2 - RW - 32 bits - DISPDEC:0x6B98			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_2_2	16:0	0x0	Combined matrix constant C22 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S1.11(-2.00 to +1.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2COLOR_MATRIX_SIGN_2_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C22 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_2_3 - RW - 32 bits - DISPDEC:0x6B9C			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_2_3	15:0	0x0	Combined matrix constant C23 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S0.11(-1.00 to +0.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2COLOR_MATRIX_SIGN_2_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C23 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_2_4 - RW - 32 bits - DISPDEC:0x6BA0			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_2_4	26:8	0x0	Combined matrix constant C24 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S11.1(-2048.5 to +2047.5). It includes subtraction of 512 offset NOTE: Bits 0:6 of this field are hardwired to ZERO.
D2COLOR_MATRIX_SIGN_2_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C24 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_3_1 - RW - 32 bits - DISPDEC:0x6BA4			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_3_1	15:0	0x0	Combined matrix constant C31 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S0.11(-1.00 to +0.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2COLOR_MATRIX_SIGN_3_1	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C31 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_3_2 - RW - 32 bits - DISPDEC:0x6BA8			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_3_2	15:0	0x0	Combined matrix constant C32 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S0.11(-1.00 to +0.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2COLOR_MATRIX_SIGN_3_2	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C32 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_3_3 - RW - 32 bits - DISPDEC:0x6BAC			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_3_3	16:0	0x0	Combined matrix constant C33 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S1.11(-2.00 to +1.99). NOTE: Bits 0:4 of this field are hardwired to ZERO.
D2COLOR_MATRIX_SIGN_3_3	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C33 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

D2COLOR_MATRIX_COEF_3_4 - RW - 32 bits - DISPDEC:0x6BB0			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_MATRIX_COEF_3_4	26:8	0x0	Combined matrix constant C34 of RGB->YCbCr, contrast and brightness adjustment for secondary display. Format fix-point S11.1(-2048.5 to +2047.5). It includes subtraction of 512 offset NOTE: Bits 0:6 of this field are hardwired to ZERO.
D2COLOR_MATRIX_SIGN_3_4	31	0x0	Sign bit of combined matrix constant
Combined matrix constant C34 of RGB->YCbCr, contrast and brightness adjustment for secondary display.			

2.7.18 Secondary Display Subsampling Registers

D2COLOR_SPACE_CONVERT - RW - 32 bits - DISPDEC:0x693C			
Field Name	**Bits**	**Default**	**Description**
D2COLOR_SUBSAMPLE_CRCB_MODE	1:0	0x0	Sub-sampling control for secondary display 0=do not subsample CrCb(RB) 1=subsample CrCb (RB) by using 2 tap average method 2=subsample CrCb (RB) by using 1 tap on even pixel 3=subsample CrCb (RB) by using 1 tap on odd pixel

Sub-sampling control for secondary display.

2.7.19 Secondary Display Hardware Cursor Registers

D2CUR_CONTROL - RW - 32 bits - DISPDEC:0x6C00			
Field Name	**Bits**	**Default**	**Description**
D2CURSOR_EN	0	0x0	Secondary display hardware cursor enabled. 0=disable 1=enable
D2CURSOR_MODE	9:8	0x0	Secondary display hardware cursor mode. For 2bpp mode, each line of cursor data is stored in memory as 16 bits of AND data followed by 16 bits XOR data. For color AND/XOR mode, each pixel is stored sequentially in memory as 32bits each in aRGB8888 format with bit 31 of each DWord being the AND bit. For the color alpha modes the format is also 32bpp aRGB8888 with all 8 bits of the alpha being used.All HW cursor lines must be 64 pixels wide and all lines must be stored sequentially in memory. 0=Mono (2bpp) 1=Color 24bpp + 1 bit AND (32bpp) 2=Color 24bpp + 8 bit alpha (32bpp) premultiplied alpha 3=Color 24bpp + 8 bit alpha (32bpp)unmultiplied alpha
D2CURSOR_2X_MAGNIFY	16	0x0	Secondary display hardware cursor 2x2 magnification. 0=no 2x2 magnification 1=2x2 magnification in horizontal and vertical direction

Secondary display hardware control

D2CUR_SURFACE_ADDRESS - RW - 32 bits - DISPDEC:0x6C08			
Field Name	**Bits**	**Default**	**Description**
D2CURSOR_SURFACE_ADDRESS	31:0	0x0	Secondary display hardware cursor surface base address in byte. It is 4K byte aligned. NOTE: Bits 0:11 of this field are hardwired to ZERO.

Secondary display hardware cursor surface base address.

D2CUR_SIZE - RW - 32 bits - DISPDEC:0x6C10			
Field Name	**Bits**	**Default**	**Description**
D2CURSOR_HEIGHT	5:0	0x0	Secondary display hardware cursor height minus 1.
D2CURSOR_WIDTH	21:16	0x0	Secondary display hardware cursor width minus 1.

Secondary display hardware size

D2CUR_POSITION - RW - 32 bits - DISPDEC:0x6C14			
Field Name	**Bits**	**Default**	**Description**
D2CURSOR_Y_POSITION	12:0	0x0	Secondary display hardware cursor X coordinate at the hot spot relative to the desktop coordinates.
D2CURSOR_X_POSITION	28:16	0x0	Secondary display hardware cursor X coordinate at the hot spot relative to the desktop coordinates.

Secondary display hardware cursor position

D2CUR_HOT_SPOT - RW - 32 bits - DISPDEC:0x6C18			
Field Name	**Bits**	**Default**	**Description**
D2CURSOR_HOT_SPOT_Y	5:0	0x0	Secondary display hardware cursor hot spot X length relative to the top left corner.
D2CURSOR_HOT_SPOT_X	21:16	0x0	Secondary display hardware cursor hot spot Y length relative to the top left corner.

Secondary display hardware cursor hot spot position

D2CUR_COLOR1 - RW - 32 bits - DISPDEC:0x6C1C			
Field Name	**Bits**	**Default**	**Description**
D2CUR_COLOR1_BLUE	7:0	0x0	Secondary display hardware cursor blue component of color 1.
D2CUR_COLOR1_GREEN	15:8	0x0	Secondary display hardware cursor green component of color 1.
D2CUR_COLOR1_RED	23:16	0x0	Secondary display hardware cursor red component of color 1.

Secondary display hardware cursor color 1.

D2CUR_COLOR2 - RW - 32 bits - DISPDEC:0x6C20			
Field Name	**Bits**	**Default**	**Description**
D2CUR_COLOR2_BLUE	7:0	0x0	Secondary display hardware cursor blue component of color 2.
D2CUR_COLOR2_GREEN	15:8	0x0	Secondary display hardware cursor green component of color 2.
D2CUR_COLOR2_RED	23:16	0x0	Secondary display hardware cursor red component of color 2.

Secondary display hardware cursor color 2.

D2CUR_UPDATE - RW - 32 bits - DISPDEC:0x6C24			
Field Name	**Bits**	**Default**	**Description**
D2CURSOR_UPDATE_PENDING (R)	0	0x0	Secondary display hardware cursor update pending status. It is set to 1 after a host write to cursor double buffer register. It is cleared after double buffering is done. The double buffering occurs when D2CURSOR_UPDATE_PENDING = 1 and D2CURSOR_UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC2 is disabled, the registers will be updated instantly. The D2CUR double buffer registers are: D2CURSOR_EN D2CURSOR_MODE D2CURSOR_2X_MAGNIFY D2CURSOR_SURFACE_ADDRESS D2CURSOR_HEIGHT D2CURSOR_WIDTH D2CURSOR_X_POSITION D2CURSOR_Y_POSITION D2CURSOR_HOT_SPOT_X D2CURSOR_HOT_SPOT_Y 0=No update pending 1=Update pending
D2CURSOR_UPDATE_TAKEN (R)	1	0x0	Secondary display hardware cursor update taken status. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0
D2CURSOR_UPDATE_LOCK	16	0x0	Secondary display hardware cursor update lock control. 0=Unlocked 1=Locked

2.7.20 Secondary Display Hardware Icon Registers

D2ICON_CONTROL - RW - 32 bits - DISPDEC:0x6C40			
Field Name	**Bits**	**Default**	**Description**
D2ICON_ENABLE	0	0x0	Secondary display hardware icon enable. 0=disable 1=enable
D2ICON_2X_MAGNIFY	16	0x0	Secondary display hardware icon 2x2 magnification. 0=no 2x2 magnification 1=2x2 magnification in horizontal and vertical direction

Secondary display hardware icon control.

D2ICON_SURFACE_ADDRESS - RW - 32 bits - DISPDEC:0x6C48			
Field Name	**Bits**	**Default**	**Description**
D2ICON_SURFACE_ADDRESS	31:0	0x0	Secondary display hardware icon surface base address in byte. It is 4K byte aligned. NOTE: Bits 0:11 of this field are hardwired to ZERO.

Secondary display hardware icon surface base address.

D2ICON_SIZE - RW - 32 bits - DISPDEC:0x6C50			
Field Name	**Bits**	**Default**	**Description**
D2ICON_HEIGHT	6:0	0x0	Secondary display hardware icon height minus 1.
D2ICON_WIDTH	22:16	0x0	Secondary display hardware icon width minus 1.

Secondary display hardware icon size.

D2ICON_START_POSITION - RW - 32 bits - DISPDEC:0x6C54			
Field Name	**Bits**	**Default**	**Description**
D2ICON_Y_POSITION	12:0	0x0	Secondary display hardware icon Y start coordinate related to the desktop coordinates. Note: Icon can not be off the top and off the left edge of the display surface. But can be off the bottom and off the right edge of the display.
D2ICON_X_POSITION	28:16	0x0	Secondary display hardware icon X start coordinate relative to the desktop coordinates. Note: Icon can not be off the top and off the left edge of the display surface. But can be off the bottom and off the right edge of the display.

Secondary display hardware icon position

D2ICON_COLOR1 - RW - 32 bits - DISPDEC:0x6C58			
Field Name	**Bits**	**Default**	**Description**
D2ICON_COLOR1_BLUE	7:0	0x0	Secondary display hardware icon blue component of color 1.
D2ICON_COLOR1_GREEN	15:8	0x0	Secondary display hardware icon green component of color 1.

D2ICON_COLOR1_RED	23:16	0x0	Secondary display hardware icon red component of color 1.

Secondary display hardware icon color 1.

D2ICON_COLOR2 - RW - 32 bits - DISPDEC:0x6C5C			
Field Name	**Bits**	**Default**	**Description**
D2ICON_COLOR2_BLUE	7:0	0x0	Secondary display hardware icon blue component of color 2.
D2ICON_COLOR2_GREEN	15:8	0x0	Secondary display hardware icon green component of color 2.
D2ICON_COLOR2_RED	23:16	0x0	Secondary display hardware icon red component of color 2.

Secondary display hardware icon color 2.

D2ICON_UPDATE - RW - 32 bits - DISPDEC:0x6C60			
Field Name	**Bits**	**Default**	**Description**
D2ICON_UPDATE_PENDING (R)	0	0x0	Secondary display hardware icon update Pending status. It is set to 1 after a host write to icon double buffer register. It is cleared after double buffering is done. The double buffering occurs when D2ICON_UPDATE_PENDING = 1 and D2ICON_UPDATE_LOCK = 0 and V_UPDATE = 1. If CRTC2 is disabled, the registers will be updated instantly. D2IOCN double buffer registers include: D2ICON_ENABLE D2ICON_2X_MAGNIFY D2ICON_SURFACE_ADDRESS D2ICON_HEIGHT D2ICON_WIDTH D2ICON_Y_POSITION D2ICON_X_POSITION 0=No update pending 1=Update pending
D2ICON_UPDATE_TAKEN (R)	1	0x0	Secondary display hardware icon update Taken status. It is set to 1 when double buffering occurs and cleared when V_UPDATE = 0
D2ICON_UPDATE_LOCK	16	0x0	Secondary display hardware icon update lock control. 0=Unlocked 1=Locked

Secondary display hardware icon update control

2.7.21 Display Controller Look Up Table B Registers

DC_LUTB_CONTROL - RW - 32 bits - DISPDEC:0x6CC0			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_INC_B	3:0	0x0	Exponent of Power-of-two of blue data increment of LUTB palette. If INC = 0, LUT 256-entry table mode is enabled. LUT_INDEX = PIX_DATA[7:0]. Output = LUT_DATA[LUT_INDEX]. If INC > 0, LUT PWL mode is enabled with 128 entries of base and delta values. LUT_INDEX = PIX_DATA[INC+6:INC]. Mult = PIX_DATA[INC-1:0]. Base = LUT_BASE[LUT_INDEX]. Delta = LUT_DELTA[LUT_INDEX]. Output = Base + (Mult * Delta) / increment 0=Blue data increment = N/A 1=Blue data increment = 2 2=Blue data increment = 4 3=Blue data increment = 8 4=Blue data increment = 16 5=Blue data increment = 32 6=Blue data increment = 64 7=Blue data increment = 128 8=Blue data increment = 256 9=Blue data increment = 512
DC_LUTB_DATA_B_SIGNED_EN	4	0x0	Frame buffer blue data signed enable for look-up table A. 0=Blue data is unsigned 1=Blue data is signed
DC_LUTB_DATA_B_FLOAT_POINT_EN	5	0x0	Frame buffer blue data float point enable for look-up table A. 0=Blue data is fix point 1=Blue data is float point
DC_LUTB_INC_G	11:8	0x0	Exponent of Power-of-two of green data increment of LUTB palette. If INC = 0, LUT 256-entry table mode is enabled. LUT_INDEX = PIX_DATA[7:0]. Output = LUT_DATA[LUT_INDEX]. If INC > 0, LUT PWL mode is enabled with 128 entries of base and delta values. LUT_INDEX = PIX_DATA[INC+6:INC]. Mult = PIX_DATA[INC-1:0]. Base = LUT_BASE[LUT_INDEX]. Delta = LUT_DELTA[LUT_INDEX]. Output = Base + (Mult * Delta) / increment 0=Green data increment = N/A 1=Green data increment = 2 2=Green data increment = 4 3=Green data increment = 8 4=Green data increment = 16 5=Green data increment = 32 6=Green data increment = 64 7=Green data increment = 128 8=Green data increment = 256 9=Green data increment = 512
DC_LUTB_DATA_G_SIGNED_EN	12	0x0	Frame buffer green data signed enable for look-up table A. 0=Green data is unsigned 1=Green data is signed
DC_LUTB_DATA_G_FLOAT_POINT_EN	13	0x0	Frame buffer green data float point enable for look-up table A. 0=Green data is fix point 1=Green data is float point

DC_LUTB_INC_R	19:16	0x0	Exponent of Power-of-two of red data increment of LUTB palette. If INC = 0, LUT 256-entry table mode is enabled. LUT_INDEX = PIX_DATA[7:0]. Output = LUT_DATA[LUT_INDEX]. If INC > 0, LUT PWL mode is enabled with 128 entries of base and delta values. LUT_INDEX = PIX_DATA[INC+6:INC]. Mult = PIX_DATA[INC-1:0]. Base = LUT_BASE[LUT_INDEX]. Delta = LUT_DELTA[LUT_INDEX]. Output = Base + (Mult * Delta) / increment 0=Red data increment = N/A 1=Red data increment = 2 2=Red data increment = 4 3=Red data increment = 8 4=Red data increment = 16 5=Red data increment = 32 6=Red data increment = 64 7=Red data increment = 128 8=Red data increment = 256 9=Red data increment = 512
DC_LUTB_DATA_R_SIGNED_EN	20	0x0	Frame buffer red data signed enable for look-up table A. 0=Red data is unsigned 1=Red data is signed
DC_LUTB_DATA_R_FLOAT_POINT_EN	21	0x0	Frame buffer red data float point enable for look-up table A. 0=Red data is fix point 1=Red data is float point

LUTB mode control

DC_LUTB_BLACK_OFFSET_BLUE - RW - 32 bits - DISPDEC:0x6CC4			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_BLACK_OFFSET_BLUE	15:0	0x0	Black value offset of blue component for LUTB.

Black value offset of blue component for LUTB.

DC_LUTB_BLACK_OFFSET_GREEN - RW - 32 bits - DISPDEC:0x6CC8			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_BLACK_OFFSET_GREEN	15:0	0x0	Black value offset of green component for LUTB.

Black value offset of green component for LUTB.

DC_LUTB_BLACK_OFFSET_RED - RW - 32 bits - DISPDEC:0x6CCC			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_BLACK_OFFSET_RED	15:0	0x0	Black value offset of red component for LUTB.

Black value offset of red component for LUTB.

DC_LUTB_WHITE_OFFSET_BLUE - RW - 32 bits - DISPDEC:0x6CD0			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_WHITE_OFFSET_BLUE	15:0	0xffff	White value offset of blue component for LUTB

White value offset of blue component for LUTB.

DC_LUTB_WHITE_OFFSET_GREEN - RW - 32 bits - DISPDEC:0x6CD4			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_WHITE_OFFSET_GREEN	15:0	0xffff	White value offset of green component for LUTB

White value offset of green component for LUTB

DC_LUTB_WHITE_OFFSET_RED - RW - 32 bits - DISPDEC:0x6CD8			
Field Name	**Bits**	**Default**	**Description**
DC_LUTB_WHITE_OFFSET_RED	15:0	0xffff	White value offset of red component for LUTB

White value offset of red component for LUTB

2.7.22 Display Controller CRC Registers

DCP_CRC_CONTROL - RW - 32 bits - DISPDEC:0x6C80			
Field Name	**Bits**	**Default**	**Description**
DCP_CRC_ENABLE	0	0x0	Enable DCP CRC.
DCP_CRC_DISPLAY_SEL	1	0x0	Select display number for DCP CRC. 0= from display 1 1= from display 2
DCP_CRC_SOURCE_SEL	4:2	0x0	Select data source for DCP CRC. 0=DCP to LB pixel data 1=Lower 32 bits of graphics input data to DCP from DMIF 2=Upper 32 bits of graphics input data to DCP from DMIF 3=Overlay input data to DCP from DMIF 4=DCP to LB control signals TAG[2:0] and end of chunk

DCP CRC control

DCP_CRC_MASK - RW - 32 bits - DISPDEC:0x6C84			
Field Name	**Bits**	**Default**	**Description**
DCP_CRC_MASK	31:0	0x0	Mask bits to apply to DCP CRC function. Allows CRC of only specific color and/or specific bits if wanted. Ignore those bits with mask bits to be 0

Mask bits to apply to DCP CRC function.

DCP_CRC_P0_CURRENT - RW - 32 bits - DISPDEC:0x6C88			
Field Name	**Bits**	**Default**	**Description**
DCP_CRC_P0_CURRENT (R)	31:0	0x0	Current value of CRC for current frame pipe 0.

Current value of CRC for current frame pipe 0.

DCP_CRC_P1_CURRENT - RW - 32 bits - DISPDEC:0x6C8C			
Field Name	**Bits**	**Default**	**Description**
DCP_CRC_P1_CURRENT (R)	31:0	0x0	Current value of CRC for current frame pipe 1.

Current value of CRC for current frame pipe 1.

DCP_CRC_P0_LAST - RW - 32 bits - DISPDEC:0x6C90			
Field Name	**Bits**	**Default**	**Description**
DCP_CRC_P0_LAST (R)	31:0	0x0	Final value of CRC for previous frame pipe 0.

Final value of CRC for previous frame pipe 0.

DCP_CRC_P1_LAST - RW - 32 bits - DISPDEC:0x6C94			
Field Name	**Bits**	**Default**	**Description**
DCP_CRC_P1_LAST (R)	31:0	0x0	Final value of CRC for previous frame pipe 1.

Final value of CRC for previous frame pipe 1.

2.7.23 Display/Memory Interface Control and Status registers

DMIF_CONTROL - RW - 32 bits - DISPDEC:0x6CB0			
Field Name	**Bits**	**Default**	**Description**
DMIF_BUFF_SIZE	1:0	0x0	DMIF memory size. 0x0 - full memory size, 256x128bits. 0x1 - 3/4 memory size. 0x2 - 1/2 memory size. 0x3 - 1/4 memory size.
DMIF_D1_REQ_BURST_SIZE	10:8	0x2	DMIF request burst size for display 1. 0x0 - 1 request. 0x1 - 2 requests. 0x2 - 4 requests. 0x3 - 8 requests. 0x4 - 16 requests.
DMIF_D2_REQ_BURST_SIZE	18:16	0x2	DMIF request burst size for display 2. 0x0 - 1 request. 0x1 - 2 requests. 0x2 - 4 requests. 0x3 - 8 requests. 0x4 - 16 requests.

DMIF control register

DMIF_STATUS - RW - 32 bits - DISPDEC:0x6CB4			
Field Name	**Bits**	**Default**	**Description**
DMIF_MC_SEND_ON_IDLE (R)	0	0x0	This register bit is set to 1 if MH returns data to DMIF when there is no pending request. It is sticky bit. Once this bit is set to high, it will stay high until it is cleared by writing 1 to register DMIF_CLEAR_MH_DATA_ON_IDLE 0=MC does not send data to DMIF when there is no data request pending 1=MH sends data to DMIF when there is no data pending request.
DMIF_CLEAR_MC_SEND_ON_IDLE (W)	1	0x0	This register bit is used to clear register DMIF_MH_SEND_ON_IDLE 0=No effect 1=Clear register bit DMIF_MH_SEND_ON_IDLE

This is a debug register. DMIF status.

2.7.24 MCIF Control Registers

MCIF_CONTROL - RW - 32 bits - DISPDEC:0x6CB8			
Field Name	**Bits**	**Default**	**Description**
MCIF_BUFF_SIZE	1:0	0x0	MCIF memory size. 0x0 - full memory size, 16x143bits. 0x1 - 3/4 memory size. 0x2 - 1/2 memory size. 0x3 - 1/4 memory size.
MCIF control register			

2.7.25 Display Controller to Line Buffer Control Registers

DCP to LB chunk gap control

DCP_LB_DATA_GAP_BETWEEN_CHUNK - RW - 32 bits - DISPDEC:0x6CBC			
Field Name	**Bits**	**Default**	**Description**
DCP_LB_GAP_BETWEEN_CHUNK_20BPP	3:0	0x5	This register is used to control gap between data chunks sent from DCP to LB when the next LB data chunk is in 20bpp mode. The gap between current chunk and next chunk will be register value plus 1. The default value is 5. If any display has 32bpp digital output enabled, this values should be set to 6.
DCP_LB_GAP_BETWEEN_CHUNK_30BPP	7:4	0x1	This register is used to control gap between data chunks sent from DCP to LB when the next LB data chunk is in 30bpp mode. The gap between current chunk and next chunk will be register value plus 1. The default value is 1. If any display has 32bpp digital output enabled, this values should be set to 4

DCP LB chunk gap control

2.8 CRTC Registers

D1CRTC_H_TOTAL - RW - 32 bits - DISPDEC:0x6000			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_H_TOTAL	12:0	0x0	Horizontal total minus one. Sum of display width, overscan left and right, front and back porch and H sync width. E.g. for 800 pixels set to 799 = 0x31F Double-buffered with D1MODE_MASTER_UPDATE_LOCK

Defines horizontal dimension of the display timing for CRTC1

D1CRTC_H_BLANK_START_END - RW - 32 bits - DISPDEC:0x6004			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_H_BLANK_START	12:0	0x0	Start of the horizontal blank. The location of the first pixel of horizontal blank, relative to pixel zero. If right overscan border, then blank starts after border ends. Double-buffered with D1MODE_MASTER_UPDATE_LOCK
D1CRTC_H_BLANK_END	28:16	0x0	End of the horizontal blank. The location of the next pixel after the last pixel of horizontal blank, relative to pixel zero. Double-buffered with D1MODE_MASTER_UPDATE_LOCK

Defines horizontal blank region of the display timing for CRTC1

D1CRTC_H_SYNC_A - RW - 32 bits - DISPDEC:0x6008			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_H_SYNC_A_START	12:0	0x0	First pixel of horizontal sync A. In normal cases, it is set to 0. It is only set to non-zero value when we want to test the higher bits of the H counter. This register should be ignored and set to 0x0 in VGA timing mode. Hardware does not support odd number value for this register.
D1CRTC_H_SYNC_A_END	28:16	0x0	Horizontal sync A end. Determines position of the next pixel after last pixel of horizontal sync A. The last pixel of horizontal sync A is D1CRTC_H_SYNC_A_END - 1. The first pixel of horizontal sync A is pixel 0. It should be programmed to a value one greater than the actual last pixel of horizontal sync A. Double-buffered with D1MODE_MASTER_UPDATE_LOCK

Defines horizontal sync A position for CRTC1

D1CRTC_H_SYNC_A_CNTL - RW - 32 bits - DISPDEC:0x600C			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_H_SYNC_A_POL	0	0x0	Polarity of H SYNC A 0 = active high 1 = active low Double-buffered with D1MODE_MASTER_UPDATE_LOCK
D1CRTC_COMP_SYNC_A_EN	16	0x0	Enables composite H sync A 0 = disabled 1 = enabled
D1CRTC_H_SYNC_A_CUTOFF	17	0x0	Cutoff H sync A at end of H BLANK when end of H sync A is beyond H BLANK 0 = cutoff is enabled 1 = cutoff is disabled

Controls the H SYNC A for CRTC1

D1CRTC_H_SYNC_B - RW - 32 bits - DISPDEC:0x6010			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_H_SYNC_B_START	12:0	0x0	First pixel of horizontal sync B
D1CRTC_H_SYNC_B_END	28:16	0x0	Horizontal sync B end. Determines position of the next pixel after last pixel of horizontal sync B. The last pixel of horizontal sync B is D1CRTC_H_SYNC_B_END - 1. This register value is exclusive. It should be programmed to a value one greater than the actual last pixel of horizontal sync B

Defines the position of horizontal sync B for CRTC1

D1CRTC_H_SYNC_B_CNTL - RW - 32 bits - DISPDEC:0x6014			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_H_SYNC_B_POL	0	0x0	Polarity of H SYNC B 0 = active high 1 = active low
D1CRTC_COMP_SYNC_B_EN	16	0x0	Enables composite H SYNC B 0 = disabled 1 = enabled
D1CRTC_H_SYNC_B_CUTOFF	17	0x0	Cutoff horizontal sync B at end of horizontal blank region when end of H SYNC B is beyond horizontal blank 0 = cutoff is enabled 1 = cutoff is disabled

Controls horizontal sync B for CRTC1

D1CRTC_V_TOTAL - RW - 32 bits - DISPDEC:0x6020			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_V_TOTAL	12:0	0x0	Vertical total minus one. Sum of vertical active display, top and bottom overscan, front and back porch and vertical sync width. E.g. for 525 lines set to 524 = 0x20C Double-buffered with D1MODE_MASTER_UPDATE_LOCK

Defines the vertical dimension of display timing for CRTC1

D1CRTC_V_BLANK_START_END - RW - 32 bits - DISPDEC:0x6024			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_V_BLANK_START	12:0	0x0	Vertical blank start. Determines the position of the first blank line in a frame. Line 0 is the first line of vertical sync A. Double-buffered with D1MODE_MASTER_UPDATE_LOCK
D1CRTC_V_BLANK_END	28:16	0x0	Vertical blank end. Determines the position of the next line after the last line of vertical blank. The last line of vertical blank is D1CRTC_V_BLANK_END - 1. Double-buffered with D1MODE_MASTER_UPDATE_LOCK

Defines the vertical blank region of the display timing for CRTC1

D1CRTC_V_SYNC_A - RW - 32 bits - DISPDEC:0x6028			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_V_SYNC_A_START	12:0	0x0	The first line of vertical sync A. In normal cases, it is set to 0. It is set to non-zero value only when trying to test the higher bits of the vertical counter
D1CRTC_V_SYNC_A_END	28:16	0x0	Vertical sync A end. Determines the position of the next line after the last line of vertical sync A. The last line of vertical sync A is D1CRTC_V_SYNC_A_END - 1. The first line of vertical sync A is line 0. This register value is exclusive. It should be programmed to a value one greater than the actual last line of vertical sync A Double-buffered with D1MODE_MASTER_UPDATE_LOCK

Defines the position of vertical sync A for CRTC1

D1CRTC_V_SYNC_A_CNTL - RW - 32 bits - DISPDEC:0x602C			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_V_SYNC_A_POL	0	0x0	Polarity of V SYNC A 0 = active high 1 = active low Double-buffered with D1MODE_MASTER_UPDATE_LOCK

Controls V SYNC A for CRTC1

D1CRTC_V_SYNC_B - RW - 32 bits - DISPDEC:0x6030			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_V_SYNC_B_START	12:0	0x0	Vertical sync B start. Determines the position of the first line of vertical sync B.
D1CRTC_V_SYNC_B_END	28:16	0x0	Vertical sync B end. Determines the position of the next line after the last line of vertical sync B. Last line of vertical sync B is D1CRTC_V_SYNC_B_END - 1. This register value is exclusive. It should be programmed to a value one greater than the actual last line of vertical sync B

Defines the position of vertical sync B for CRTC1

D1CRTC_V_SYNC_B_CNTL - RW - 32 bits - DISPDEC:0x6034			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_V_SYNC_B_POL	0	0x0	Controls polarity of vertical sync B 0 = active high 1 = active low

Controls vertical sync B for CRTC1

D1CRTC_TRIGA_CNTL - RW - 32 bits - DISPDEC:0x6060			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_TRIGA_SOURCE_SELECT	3:0	0x0	Select source of input signals for external trigger A 0 = logic 0 1 = VSYNCA from another CRTC of the chip 2 = HSYNCA from another CRTC of the chip 3 = VSYNCB from another CRTC of the chip 4 = HSYNCB from another CRTC of the chip 5 = GENERICA pin 6 = GENERICB pin 7 = VSYNCA pin 8 = HSYNCA pin 9 = VSYNCB pin 10 = HSYNCB pin 11 = HPD1 pin 12 = HPD2 pin 13 = DVALID pin 14 = PSYNC pin 15 = Video capture complete signal from VIP
D1CRTC_TRIGA_POLARITY_SELECT	6:4	0x0	Selects source of input signal from polarity of external trigger A 0 = logic 0 1 = interlace polarity from another CRTC of the chip 2 = GENERICA pin 3 = GENERICB pin 4 = HSYNCA pin 5 = HSYNCB pin 6 = video capture polarity input from VIP 7 = DVALID pin
D1CRTC_TRIGA_RESYNC_BYPASS_EN	8	0x0	Bypass the resync logic for the external trigger A signal and its polarity input signal 0 = do not bypass 1 = bypass the resync logic
D1CRTC_TRIGA_INPUT_STATUS (R)	9	0x0	Read back the value of the external trigger A input signal after the mux
D1CRTC_TRIGA_POLARITY_STATUS (R)	10	0x0	Reports the value of the external trigger A polarity signal after the mux
D1CRTC_TRIGA_OCCURRED (R)	11	0x0	Reports whether external trigger A has occurred. A sticky bit. 0 = has not occurred 1 = has occurred
D1CRTC_TRIGA_RISING_EDGE_DETECT_CNTL	13:12	0x0	Controls the detection of rising edge of the external trigger A signal 00 = do not detect rising edge 01 = always detect rising edge 10 = detect rising edge only when field polarity is low 11 = detect rising edge only when field polarity is high
D1CRTC_TRIGA_FALLING_EDGE_DETECT_CNTL	17:16	0x0	Controls the detection of falling edge of external trigger A signal 00 = do not detect falling edge 01 = always detect falling edge 10 = detect falling edge only when field polarity is low 11 = detect falling edge only when field polarity is high
D1CRTC_TRIGA_FREQUENCY_SELECT	21:20	0x0	Determines the frequency of the external trigger A signal 00 = send every signal 01 = send every 2 signals 10 = reserved 11 = send every 4 signals
D1CRTC_TRIGA_DELAY	28:24	0x0	A programmable PCLK_CRTC1 delay to send external trigger A signal.
D1CRTC_TRIGA_CLEAR (W)	31	0x0	Clears the sticky bit D1CRTC_TRIGA_OCCURRED when written with '1'

Controls for external trigger A signal in CRTC1

D1CRTC_TRIGA_MANUAL_TRIG - RW - 32 bits - DISPDEC:0x6064

Field Name	Bits	Default	Description
D1CRTC_TRIGA_MANUAL_TRIG (W)	0	0x0	One shot trigger for external trigger A signal when written with '1' Manual trigger for external trigger A signal of CRTC1

D1CRTC_TRIGB_CNTL - RW - 32 bits - DISPDEC:0x6068			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_TRIGB_SOURCE_SELECT	3:0	0x0	Select source of input signals for external trigger B 0 = logic 0 1 = VSYNCA from another CRTC of the chip 2 = HSYNCA from another CRTC of the chip 3 = VSYNCB from another CRTC of the chip 4 = HSYNCB from another CR TC of the chip 5 = GENERICA pin 6 = GENERICB pin 7 = VSYNCA pin 8 = HSYNCA pin 9 = VSYNCB pin 10 = HSYNCB pin 11 = HPD1 pin 12 = HPD2 pin 13 = DVALID pin 14 = PSYNC pin 15 = Video capture complete signal from VIP
D1CRTC_TRIGB_POLARITY_SELECT	6:4	0x0	Selects source of input signal from polarity of external trigger A 0 = logic 0 1 = interlace polarity from another CRTC of the chip 2 = GENERICA pin 3 = GENERICB pin 4 = HSYNCA pin 5 = HSYNCB pin 6 = video capture polarity input from VIP 7 = DVALID pin
D1CRTC_TRIGB_RESYNC_BYPASS_EN	8	0x0	Bypass the resync logic for the external trigger A signal and its polarity input signal 0 = do not bypass 1 = bypass the resync logic
D1CRTC_TRIGB_INPUT_STATUS (R)	9	0x0	Read back the value of the external trigger B input signal after the mux
D1CRTC_TRIGB_POLARITY_STATUS (R)	10	0x0	Reports the value of the external trigger B polarity signal after the mux
D1CRTC_TRIGB_OCCURRED (R)	11	0x0	Reports whether external trigger B has occurred. A sticky bit. 0 = has not occurred 1 = has occurred
D1CRTC_TRIGB_RISING_EDGE_DETECT_CNTL	13:12	0x0	Controls the detection of rising edge of the external trigger B signal 00 = do not detect rising edge 01 = always detect rising edge 10 = detect rising edge only when field polarity is low 11 = detect rising edge only when field polarity is high
D1CRTC_TRIGB_FALLING_EDGE_DETECT_CNTL	17:16	0x0	Controls the detection of falling edge of external trigger B signal 00 = do not detect falling edge 01 = always detect falling edge 10 = detect falling edge only when field polarity is low 11 = detect falling edge only when field polarity is high
D1CRTC_TRIGB_FREQUENCY_SELECT	21:20	0x0	Determines the frequency of the external trigger B signal 00 = send every signal 01 = send every 2 signals 10 = reserved 11 = send every 4 signals
D1CRTC_TRIGB_DELAY	28:24	0x0	A programmable delay to send external trigger B signal
D1CRTC_TRIGB_CLEAR (W)	31	0x0	Clears the sticky bit D1CRTC_TRIGB_OCCURRED when written with '1'

Control for external trigger B signal of CRTC1

D1CRTC_TRIGB_MANUAL_TRIG - RW - 32 bits - DISPDEC:0x606C			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_TRIGB_MANUAL_TRIG (W)	0	0x0	One shot trigger for external trigger B signal when written with '1'

Manual trigger for external trigger B signal for CRTC1

D1CRTC_FORCE_COUNT_NOW_CNTL - RW - 32 bits - DISPDEC:0x6070			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_FORCE_COUNT_NOW_MODE	1:0	0x0	Controls which timing counter is forced 0 = force counter now mode is disabled 1 = force H count now to H_TOTAL only 2 = force H count to H_TOTAL and V count to V_TOTAL in progressive mode and V_TOTAL-1 in interlaced mode 3 = reserved
D1CRTC_FORCE_COUNT_NOW_TRIG_SEL	8	0x0	Selects the trigger signal as force count now trigger 0 = selects CRTC_TRIG_A and CRTC_TRIG_A_POL 1 = selects CRTC_TRIG_B and CRTC_TRIG_B_POL
D1CRTC_FORCE_COUNT_NOW_OCCURRED (R)	16	0x0	Reports the status of force count now, a sticky bit. 0 = CRTC force count now has not occurred 1 = CRTC force count now has occurred
D1CRTC_FORCE_COUNT_NOW_CLEAR (W)	24	0x0	Resets D1CRTC_FORCE_COUNT_NOW_OCCURRED when written with '1'

Controls CRTC1 force count now logic

D1CRTC_FLOW_CONTROL - RW - 32 bits - DISPDEC:0x6074			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_FLOW_CONTROL_SOURCE_SELECT	3:0	0x0	Selects the signal used for flow control in CRTC1 0 = logic 0 1 = GENERICA pin 2 = GENERICB pin 3 = HPD1 pin 4 = HPD2 pin 5 = DDC1DATA pin 6 = DDC1CLK pin 7 = DDC2DATA pin 8 = DDC2CLK pin 9 = DVOCLK pin 10 = VHAD(0] pin 11 = VHAD[1] pin 12 = VPHCTL pin 13 = VIPCLK pin 14 = DVALID pin 15 = PSYNC pin
D1CRTC_FLOW_CONTROL_POLARITY	8	0x0	Controls the polarity of the flow control input signal 0 = keep the signal the same polarity 1 = invert the polarity of the input signal
D1CRTC_FLOW_CONTROL_GRANULARITY	16	0x0	Controls at which pixel position flow control can start to happen 0 = flow control only start to happen on odd-even pixel boundary 1 = flow control can start at any pixel position
D1CRTC_FLOW_CONTROL_INPUT_STATUS (R)	24	0x0	Reports the value of the flow control input signal 0 = output of source mux of flow control signal is low 1 = output of source mux of flow control signal is high

Controls flow control of CRTC1

D1CRTC_PIXEL_DATA_READBACK - RW - 32 bits - DISPDEC:0x6078			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_PIXEL_DATA_BLUE_CB (R)	9:0	0x0	B/Cb component sent to DISPOUT
D1CRTC_PIXEL_DATA_GREEN_Y (R)	19:10	0x0	G/Y component sent to DISPOUT
D1CRTC_PIXEL_DATA_RED_CR (R)	29:20	0x0	R/Cr component sent to DISPOUT

Read back of the CRTC1 pixel data sent to DISPOUT. This is a debug register. Intended for use in one shot clocking mode.

D1CRTC_STEREO_FORCE_NEXT_EYE - RW - 32 bits - DISPDEC:0x607C			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_STEREO_FORCE_NEXT_EYE (W)	1:0	0x0	Force next frame eye view - One shot. 00: No force - next eye opposite of current eye 01: Right eye force - force right eye next field/frame 10: Left eye force - force right eye next field/frame 11: Reserved After a force has occurred, readback of this register will be 00

Force Next Eye register

D1CRTC_CONTROL - RW - 32 bits - DISPDEC:0x6080			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_MASTER_EN	0	0x0	Enables/Disables CRTC1. H counter is at H_TOTAL and V counter is at first line of blank when CRTC is disabled. 0 = Disabled 1 = Enabled
D1CRTC_SYNC_RESET_SEL	4	0x0	Allows power management to lower CRTC1 enable.
D1CRTC_DISABLE_POINT_CNTL	9:8	0x1	When D1CRTC_MASTER_EN is set to 0, delay the disabling of CRTC1 until certain point within the frame 00 = disable CRTC immediately 01 = delay disable CRTC until the end of the current line 10 = reserved 11 = delay disable CRTC until end of the first line in the vertical blank region
D1CRTC_CURRENT_MASTER_EN_STATE (R)	16	0x0	Read-only field indicates the current status of the timing generator. Can be used to poll for when a delayed disable takes effect. 0 = CRTC is disabled 1 = CRTC is enabled
D1CRTC_DISP_READ_REQUEST_DISABLE	24	0x0	Disables data read request from the display controller. Can be used to stop display reads from system memory but keep display timing generation running. Has no effect if CRTC is disabled. 0 = do not disable data read request 1 = disable data read request

Controls CRTC1 timing generator and data read request to display1

D1CRTC_BLANK_CONTROL - RW - 32 bits - DISPDEC:0x6084			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_CURRENT_BLANK_STATE (R)	0	0x0	Read only status indicating current state of display blanking. 0 = screen not blanked 1 = screen is blanked

D1CRTC_BLANK_DATA_EN	8	0x0	Enable for blanking active display area. The active area of display that is forced will use the D1CRTC_BLACK_COLOR value. This field is optionally double buffered with D1CRTC_BLANK_DATA_DOUBLE_BUFFER_EN. 0 = disable blanking 1 = enable blanking
D1CRTC_BLANK_DE_MODE	16	0x0	Determines whether BLANK and DATA_ACTIVE signal keeps toggling when screen is blank 0 = toggles BLANK and DATA_ACTIVE 1 = keep BLANK active and DATA_ACTIVE inactive

Controls forced blanking of active area of display timing. Useful for display mode switches when corrupted image may be generated for a frame or two.

D1CRTC_INTERLACE_CONTROL - RW - 32 bits - DISPDEC:0x6088			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_INTERLACE_ENABLE	0	0x0	Enables interlaced timing 0 = Progressive timing 1 = Interlaced timing
D1CRTC_INTERLACE_FORCE_NEXT_FIELD (W)	17:16	0x0	One shot force next field polarity when written 00 = does not force next field 01 = force only next field to odd 10 = force only next field to even 11 = does not force next field

Interlaced timing control for CRTC1

D1CRTC_INTERLACE_STATUS - RW - 32 bits - DISPDEC:0x608C			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_INTERLACE_CURRENT_FIELD (R)	0	0x0	Reports the polarity of current field 0 = even 1 = odd
D1CRTC_INTERLACE_NEXT_FIELD (R)	1	0x0	Reports the polarity of the next field. Normally the opposite of the current field. When D1CRTC_INTERLACE_FORCE_NEXT_FIELD is used to force polarity of next field, then next field can match current field. 0 = even 1 = odd

Read-only register reports the polarity of the current and next field for interlaced timing

D1CRTC_BLANK_DATA_COLOR - RW - 32 bits - DISPDEC:0x6090			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_BLANK_DATA_COLOR_BLUE_CB	9:0	0x0	B / Cb component
D1CRTC_BLANK_DATA_COLOR_GREEN_Y	19:10	0x0	G / Y component
D1CRTC_BLANK_DATA_COLOR_RED_CR	29:20	0x0	R / Cr component

Set the color for pixels in blank region

D1CRTC_OVERSCAN_COLOR - RW - 32 bits - DISPDEC:0x6094			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_OVERSCAN_COLOR_BLUE	9:0	0x0	B or Cb component
D1CRTC_OVERSCAN_COLOR_GREEN	19:10	0x0	G or Y component
D1CRTC_OVERSCAN_COLOR_RED	29:20	0x0	R or Cr component

Defines color of the overscan region for CRTC1

D1CRTC_BLACK_COLOR - RW - 32 bits - DISPDEC:0x6098			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_BLACK_COLOR_B_CB	9:0	0x0	B / Cb component of the black color
D1CRTC_BLACK_COLOR_G_Y	19:10	0x0	G / Y component of the black color
D1CRTC_BLACK_COLOR_R_CR	29:20	0x0	R / Cr component of the black color

Black color applied to the active display region when blanking the screen

D1CRTC_STATUS - RW - 32 bits - DISPDEC:0x609C			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_V_BLANK (R)	0	0x0	Current vertical position 0 = outside vertical blank region 1 = within vertical blank region
D1CRTC_V_ACTIVE_DISP (R)	1	0x0	Current vertical position 0 = outside vertical active display region 1 = within vertical active display region
D1CRTC_V_SYNC_A (R)	2	0x0	Current vertical position 0 = outside VSYNC 1 = within VSYNC
D1CRTC_V_UPDATE (R)	3	0x0	Current vertical position 0 = outside the V_UPDATE region 1 = within the V_UPDATE region (between end of vertical active display and start_line)
D1CRTC_V_START_LINE (R)	4	0x0	Current vertical position 0 = outside start_line region 1 = within start_line region
D1CRTC_H_BLANK (R)	16	0x0	Current horizontal position 0 = outside horizontal blank region 1 = within horizontal blank region
D1CRTC_H_ACTIVE_DISP (R)	17	0x0	Current horizontal region 0 = outside horizontal active display region 1 = within horizontal active display region
D1CRTC_H_SYNC_A (R)	18	0x0	Current horizontal position 0 = outside horizontal sync 1 = within horizontal sync

Reports the position of CRTC1

D1CRTC_STATUS_POSITION - RW - 32 bits - DISPDEC:0x60A0			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_VERT_COUNT (R)	12:0	0x0	Reports current vertical count
D1CRTC_HORZ_COUNT (R)	28:16	0x0	Reports current horizontal count

Current horizontal and vertical count of CRTC1

D1CRTC_STATUS_FRAME_COUNT - RW - 32 bits - DISPDEC:0x60A4			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_FRAME_COUNT (R)	23:0	0x0	Reports current frame count

Current frame count for CRTC1

D1CRTC_STATUS_VF_COUNT - RW - 32 bits - DISPDEC:0x60A8

Field Name	Bits	Default	Description
D1CRTC_VF_COUNT (R)	28:0	0x0	Reports current vertical and frame count

Current composite vertical and frame count for CRTC1

D1CRTC_STATUS_HV_COUNT - RW - 32 bits - DISPDEC:0x60AC			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_HV_COUNT (R)	28:0	0x0	Reports current horizontal and vertical count

Current composite H/V count of CRTC1

D1CRTC_COUNT_RESET - RW - 32 bits - DISPDEC:0x60B0			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_RESET_FRAME_COUNT (W)	0	0x0	One-shot reset of frame counter of CRTC1 when written with '1'

Resets CRTC1 counters

D1CRTC_COUNT_CONTROL - RW - 32 bits - DISPDEC:0x60B4			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_HORZ_COUNT_BY2_EN	0	0x0	Enable the horizontal replication of 2. CRTC increments the H counter every 2 pixel clocks 0 = disabled 1 = enabled

Controls the counters in CRTC1

D1CRTC_MANUAL_FORCE_VSYNC_NEXT_LINE - RW - 32 bits - DISPDEC:0x60B8			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_MANUAL_FORCE_VSYNC_NEXT_LINE (W)	0	0x0	One shot force VSYNCA to happen next line when written with '1'

Manual force of VSYNC to happen next line

D1CRTC_VERT_SYNC_CONTROL - RW - 32 bits - DISPDEC:0x60BC			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_FORCE_VSYNC_NEXT_LINE_OCCURRED (R)	0	0x0	Reports whether force vsync next line event has occurred. Sticky bit. 0 = event has not occurred 1 = event has occurred
D1CRTC_FORCE_VSYNC_NEXT_LINE_CLEAR (W)	8	0x0	One shot clear to the sticky bit D1CRTC_FORCE_VSYNC_NEXT_LINE_OCCURRED when written with '1'
D1CRTC_AUTO_FORCE_VSYNC_MODE	17:16	0x0	Selection of auto mode for forcing vsync next line 00 = disables auto mode 01 = force VSYNC next line on CRTC trigger A signal 10 = force VSYNC next line on CRTC trigger B signal 11 = reserved

Controls the feature to force VSYNC next line for CRTC1

D1CRTC_STEREO_STATUS - RW - 32 bits - DISPDEC:0x60C0			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_STEREO_CURRENT_EYE (R)	0	0x0	Reports the polarity of the current frame/field 0 = right eye image 1 = left eye image
D1CRTC_STEREO_SYNC_OUTPUT (R)	8	0x0	Reports current value of STEREOSYNC signal (STEREOSYNC sent to the DISPOUT block)
D1CRTC_STEREO_SYNC_SELECT (R)	16	0x0	Reports current value of SYNC_SELECT signal (SYNC_SELECT sent to the SCL block)
D1CRTC_STEREO_FORCE_NEXT_EYE_PENDING (R)	25:24	0x0	Reports the status of D1CRTC_STEREO_FORCE_NEXT_EYE write. 00: No force pending 01: Right force pending 10: Left force pending 11: Reserved

Reports CRTC1 status in stereoscopic display

D1CRTC_STEREO_CONTROL - RW - 32 bits - DISPDEC:0x60C4			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_STEREO_SYNC_OUTPUT_POLARITY	8	0x0	Controls polarity of the stereosync signal 0 = 0 means right eye image and 1 means left eye image 1 = 0 means left eye image and 1 means right eye image
D1CRTC_STEREO_SYNC_SELECT_POLARITY	16	0x0	Controls polarity of STEREO_SELECT signal sent to scaler 0 = 0 means right eye image and 1 means left eye image 1 = 0 means left eye image and 1 means right eye image
D1CRTC_STEREO_EN	24	0x0	Enables toggling of STEREOSYNC and STEREO_SELECT signals 0 = disable toggling. 1 = enable toggling at every frame (progressive) or every field (interlace) at leading edge of VSYNCA

Stereosync control for CRTC1

D1CRTC_SNAPSHOT_STATUS - RW - 32 bits - DISPDEC:0x60C8			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_SNAPSHOT_OCCURRED (R)	0	0x0	Reports status of snapshot. A sticky bit to be cleared by writing 1 to D1CRTC_SNAPSHOT_CLEAR 0 = snapshot has not occurred 1 = snapshot has occurred
D1CRTC_SNAPSHOT_CLEAR (W)	1	0x0	Clears the D1CRTC_SNAPSHOT_OCCURRED sticky bit when written with '1'
D1CRTC_SNAPSHOT_MANUAL_TRIGGER (W)	2	0x0	One shot trigger to perform snapshot when written with '1'

Controls CRTC1 snapshot

D1CRTC_SNAPSHOT_CONTROL - RW - 32 bits - DISPDEC:0x60CC			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_AUTO_SNAPSHOT_TRIG_SEL	1:0	0x0	Determines signal source for auto-snapshot 00 = auto-snapshot is disabled 01 = uses CRTC trigger A as trigger event in auto-snapshot mode 10 = uses CRTC trigger B as trigger event in auto-snapshot mode 11 = reserved

Controls snapshot mode for CRTC1

D1CRTC_SNAPSHOT_POSITION - RW - 32 bits - DISPDEC:0x60D0			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_SNAPSHOT_VERT_COUNT (R)	12:0	0x0	Reads back the snapshoted vertical count
D1CRTC_SNAPSHOT_HORZ_COUNT (R)	28:16	0x0	Reads back the snapshoted horizontal count

Snapshot H and V count for CRTC1

D1CRTC_SNAPSHOT_FRAME - RW - 32 bits - DISPDEC:0x60D4			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_SNAPSHOT_FRAME_COUNT (R)	23:0	0x0	Reports the snapshoted frame count

Snapshot frame count of CRTC1

D1CRTC_START_LINE_CONTROL - RW - 32 bits - DISPDEC:0x60D8			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_PROGRESSIVE_START_LINE_EARLY	0	0x0	move start_line signal by 1 line earlier in progressive mode
D1CRTC_INTERLACE_START_LINE_EARLY	8	0x1	move start_line signal by 1 line earlier in interlaced timing mode

move start_line signal earlier by 1 line in CRTC1

D1CRTC_INTERRUPT_CONTROL - RW - 32 bits - DISPDEC:0x60DC			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_SNAPSHOT_INT_MSK	0	0x0	Interrupt mask for CRTC snapshot event 0 = disables interrupt 1 = enables interrupt
D1CRTC_FORCE_COUNT_NOW_INT_MSK	8	0x0	Interrupt mask for force count now event 0 = disables interrupt 1 = enables interrupt

D1CRTC_FORCE_VSYNC_NEXT_LINE_INT_MSK	16	0x0	Interrupt mask for force VSYNC next line event 0 = disables interrupt 1 = enables interrupt
D1CRTC_TRIGA_INT_MSK	24	0x0	Interrupt mask for CRTC external trigger A 0 = disables interrupt 1 = enables interrupt
D1CRTC_TRIGB_INT_MSK	25	0x0	Interrupt mask for CRTC external trigger B 0 = disables interrupt 1 = enables interrupt

Interrupt mask for CRTC1 events

D1MODE_MASTER_UPDATE_LOCK - RW - 32 bits - DISPDEC:0x60E0			
Field Name	**Bits**	**Default**	**Description**
D1MODE_MASTER_UPDATE_LOCK	0	0x0	Set the master update lock for V_UPDATE signal 0 = no master lock, V_UPDATE signal will occur 1 = set master lock to prevent V_UPDATE signal occurring, thus prevent double buffering of display registers

Master update lock for CRTC1 V_UPDATE signal

D1MODE_MASTER_UPDATE_MODE - RW - 32 bits - DISPDEC:0x60E4			
Field Name	**Bits**	**Default**	**Description**
D1MODE_MASTER_UPDATE_MODE	1:0	0x0	Controls the position of the V_UPDATE signal 00 = V_UPDATE occurs between end of active display region and start line signal 01 = V_UPDATE occurs at first leading edge of HSYNCA after leading edge of VSYNCA 10 = V_UPDATE occurs at the leading edge of VSYNC_A 11 = V_UPDATE occurs at the beginning of the first line of vertical front porch
D1MODE_MASTER_UPDATE_INTERLACED_MODE	17:16	0x0	Controls generation of V_UPDATE signal in interlaced mode 00 = generates V_UPDATE at both even and odd field 01 = generates V_UPDATE only at even field. when D1MODE_MASTER_UPDATE_MODE = 00, V_UPDATE starts at odd field and ends at even field 10 = generates V_UPDATE only at odd field. when D1MODE_MASTER_UPDATE_MODE = 00, V_UPDATE starts at even field and ends at odd field 11 = reserved

Controls the generation of the V_UPDATE signal in CRTC1

D1CRTC_UPDATE_LOCK - RW - 32 bits - DISPDEC:0x60E8			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_UPDATE_LOCK	0	0x0	Set the lock for CRTC timing registers 0 = no lock, double buffering can occur 1 = set lock to prevent double buffering

Update lock for CRTC1 timing registers

D1CRTC_DOUBLE_BUFFER_CONTROL - RW - 32 bits - DISPDEC:0x60EC			
Field Name	**Bits**	**Default**	**Description**

D1CRTC_UPDATE_PENDING (R)	0	0x0	Reports the status of double-buffered timing registers in CRTC1 0 = update has completed 1 = update is still pending
D1CRTC_UPDATE_INSTANTLY	8	0x0	Disables double buffering of CRTC1 timing registers 0 = enables double buffering 1 = disables double buffering
D1CRTC_BLANK_DATA_DOUBLE_BUFFER_EN	16	0x0	Enables the double buffering of D1CRTC_BLANK_DATA_EN 0 = disables double buffering. D1CRTC_BLANK_DATA_EN is updated immediately 1 = enables double buffering of D1CRTC_BLANK_DATA_EN when V_UPDATE is active

Controls double buffering of CRTC1 registers

D1CRTC_VGA_PARAMETER_CAPTURE_MODE - RW - 32 bits - DISPDEC:0x60F0			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_VGA_PARAMETER_CAPTURE_MODE	0	0x0	Controls how VGA timing parameters are captured. 0: CRTC1 will continuously latch in timing parameters from VGA 1: CRTC1 will continuously latch in timing parameters from VGA except during VGA parameter recalculated window

Controls how VGA timing parameters are captured

DC_CRTC_MASTER_EN - RW - 32 bits - DISPDEC:0x60F8			
Field Name	**Bits**	**Default**	**Description**
D1CRTC_MASTER_EN (mirror of D1CRTC_CONTROL:D1CRTC_MASTER_EN)	0	0x0	Mirror of D1CRTC_MASTER_EN field in D1CRTC_CONTROL register
D2CRTC_MASTER_EN (mirror of D2CRTC_CONTROL:D2CRTC_MASTER_EN)	1	0x0	Mirror of D2CRTC_MASTER_EN field in D1CRTC_CONTROL register

Contains mirror of DxCRTC_MASTER_EN register field in DxCRTC_CONTROL registers

DC_CRTC_TV_CONTROL - RW - 32 bits - DISPDEC:0x60FC			
Field Name	**Bits**	**Default**	**Description**
CRTC_TV_DATA_SOURCE	0	0x0	Determines source of pixel data and control signals to TV encoder 0 = CRTC1 1 = CRTC2

Controls source of pixel data and control signals to TV encoder

D2CRTC_H_TOTAL - RW - 32 bits - DISPDEC:0x6800			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_H_TOTAL	12:0	0x0	Horizontal total minus one. Sum of display width, overscan left and right, front and back porch and H sync width. E.g. for 800 pixels set to 799 = 0x31F Double-buffered with D2MODE_MASTER_UPDATE_LOCK

Defines horizontal dimension of the display timing for CRTC2

D2CRTC_H_BLANK_START_END - RW - 32 bits - DISPDEC:0x6804			
Field Name	**Bits**	**Default**	**Description**

D2CRTC_H_BLANK_START	12:0	0x0	Start of the horizontal blank. The location of the first pixel of horizontal blank, relative to pixel zero. If right overscan border, then blank starts after border ends. Double-buffered with D2MODE_MASTER_UPDATE_LOCK
D2CRTC_H_BLANK_END	28:16	0x0	End of the horizontal blank. The location of the next pixel after the last pixel of horizontal blank, relative to pixel zero. Double-buffered with D2MODE_MASTER_UPDATE_LOCK

Defines horizontal blank region of the display timing for CRTC2

D2CRTC_H_SYNC_A - RW - 32 bits - DISPDEC:0x6808			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_H_SYNC_A_START	12:0	0x0	First pixel of horizontal sync A. In normal cases, it is set to 0. It is only set to non-zero value when we want to test the higher bits of the H counter. This register should be ignored and set to 0x0 in VGA timing mode. Hardware does not support odd number value for this register.
D2CRTC_H_SYNC_A_END	28:16	0x0	Horizontal sync A end. Determines position of the next pixel after last pixel of horizontal sync A. The last pixel of horizontal sync A is D2CRTC_H_SYNC_A_END - 1. The first pixel of horizontal sync A is pixel 0. It should be programmed to a value one greater than the actual last pixel of horizontal sync A. Double-buffered with D2MODE_MASTER_UPDATE_LOCK

Defines horizontal sync A position for CRTC2

D2CRTC_H_SYNC_A_CNTL - RW - 32 bits - DISPDEC:0x680C			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_H_SYNC_A_POL	0	0x0	Polarity of H SYNC A 0 = active high 1 = active low Double-buffered with D2MODE_MASTER_UPDATE_LOCK
D2CRTC_COMP_SYNC_A_EN	16	0x0	Enables composite H sync A 0 = disabled 1 = enabled
D2CRTC_H_SYNC_A_CUTOFF	17	0x0	Cutoff H sync A at end of H BLANK when end of H sync A is beyond H BLANK 0 = cutoff is enabled 1 = cutoff is disabled

Controls the H SYNC A for CRTC1

D2CRTC_H_SYNC_B - RW - 32 bits - DISPDEC:0x6810			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_H_SYNC_B_START	12:0	0x0	First pixel of horizontal sync B
D2CRTC_H_SYNC_B_END	28:16	0x0	Horizontal sync B end. Determines position of the next pixel after last pixel of horizontal sync B. The last pixel of horizontal sync B is D2CRTC_H_SYNC_B_END - 1. This register value is exclusive. It should be programmed to a value one greater than the actual last pixel of horizontal sync B

Defines the position of horizontal sync B for CRTC2

D2CRTC_H_SYNC_B_CNTL - RW - 32 bits - DISPDEC:0x6814			
Field Name	**Bits**	**Default**	**Description**

D2CRTC_H_SYNC_B_POL	0	0x0	Polarity of H SYNC B 0 = active high 1 = active low
D2CRTC_COMP_SYNC_B_EN	16	0x0	Enables composite H SYNC B 0 = disabled 1 = enabled
D2CRTC_H_SYNC_B_CUTOFF	17	0x0	Cutoff horizontal sync B at end of horizontal blank region when end of H SYNC B is beyond horizontal blank 0 = cutoff is enabled 1 = cutoff is disabled

Controls horizontal sync B for CRTC2

D2CRTC_V_TOTAL - RW - 32 bits - DISPDEC:0x6820			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_V_TOTAL	12:0	0x0	Vertical total minus one. Sum of vertical active display, top and bottom overscan, front and back porch and vertical sync width. E.g. for 525 lines set to 524 = 0x20C Double-buffered with D2MODE_MASTER_UPDATE_LOCK

Defines the vertical dimension of display timing for CRTC2

D2CRTC_V_BLANK_START_END - RW - 32 bits - DISPDEC:0x6824			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_V_BLANK_START	12:0	0x0	Vertical blank start. Determines the position of the first blank line in a frame. Line 0 is the first line of vertical sync A. Double-buffered with D2MODE_MASTER_UPDATE_LOCK
D2CRTC_V_BLANK_END	28:16	0x0	Vertical blank end. Determines the position of the next line after the last line of vertical blank. The last line of vertical blank is D2CRTC_V_BLANK_END - 1. Double-buffered with D2MODE_MASTER_UPDATE_LOCK

Defines the position of the vertical blank region for CRTC2

D2CRTC_V_SYNC_A - RW - 32 bits - DISPDEC:0x6828			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_V_SYNC_A_START	12:0	0x0	The first line of vertical sync A. In normal cases, it is set to 0. It is set to non-zero value only when trying to test the higher bits of the vertical counter
D2CRTC_V_SYNC_A_END	28:16	0x0	Vertical sync A end. Determines the position of the next line after the last line of vertical sync A. The last line of vertical sync A is D2CRTC_V_SYNC_A_END - 1. The first line of vertical sync A is line 0. This register value is exclusive. It should be programmed to a value one greater than the actual last line of vertical sync A Double-buffered with D2MODE_MASTER_UPDATE_LOCK

Defines the position of vertical sync A for CRTC2

D2CRTC_V_SYNC_A_CNTL - RW - 32 bits - DISPDEC:0x682C			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_V_SYNC_A_POL	0	0x0	Polarity of V SYNC A 0 = active high 1 = active low Double-buffered with D2MODE_MASTER_UPDATE_LOCK

Controls V SYNC A for CRTC2

D2CRTC_V_SYNC_B - RW - 32 bits - DISPDEC:0x6830			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_V_SYNC_B_START	12:0	0x0	Vertical sync B start. Determines the position of the first line of vertical sync B.
D2CRTC_V_SYNC_B_END	28:16	0x0	Vertical sync B end. Determines the position of the next line after the last line of vertical sync B. Last line of vertical sync B is D2CRTC_V_SYNC_B_END - 1. This register value is exclusive. It should be programmed to a value one greater than the actual last line of vertical sync B

Defines the position of vertical sync B for CRTC2

D2CRTC_V_SYNC_B_CNTL - RW - 32 bits - DISPDEC:0x6834			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_V_SYNC_B_POL	0	0x0	Controls polarity of vertical sync B 0 = active high 1 = active low

Controls vertical sync B for CRTC2

D2CRTC_TRIGA_CNTL - RW - 32 bits - DISPDEC:0x6860			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_TRIGA_SOURCE_SELECT	3:0	0x0	Select source of input signals for external trigger A 0 = logic 0 1 = VSYNCA from another CRTC of the chip 2 = HSYNCA from another CRTC of the chip 3 = VSYNCB from another CRTC of the chip 4 = HSYNCB from another CRTC of the chip 5 = GENERICA pin 6 = GENERICB pin 7 = VSYNCA pin 8 = HSYNCA pin 9 = VSYNCB pin 10 = HSYNCB pin 11 = HPD1 pin 12 = HPD2 pin 13 = DVALID pin 14 = PSYNC pin 15 = Video capture complete signal from VIP
D2CRTC_TRIGA_POLARITY_SELECT	6:4	0x0	Selects source of input signal from polarity of external trigger A 0 = logic 0 1 = interlace polarity from another CRTC of the chip 2 = GENERICA pin 3 = GENERICB pin 4 = HSYNCA pin 5 = HSYNCB pin 6 = video capture polarity input from VIP 7 = DVALID pin
D2CRTC_TRIGA_RESYNC_BYPASS_EN	8	0x0	Bypass the resync logic for the external trigger A signal and its polarity input signal 0 = do not bypass 1 = bypass the resync logic
D2CRTC_TRIGA_INPUT_STATUS (R)	9	0x0	Read back the value of the external trigger A input signal after the mux
D2CRTC_TRIGA_POLARITY_STATUS (R)	10	0x0	Reports the value of the external trigger A polarity signal after the mux

D2CRTC_TRIGA_OCCURRED (R)	11	0x0	Reports whether external trigger A has occurred. A sticky bit. 0 = has not occurred 1 = has occurred
D2CRTC_TRIGA_RISING_EDGE_DETECT_CNTL	13:12	0x0	Controls the detection of rising edge of the external trigger A signal 00 = do not detect rising edge 01 = always detect rising edge 10 = detect rising edge only when field polarity is low 11 = detect rising edge only when field polarity is high
D2CRTC_TRIGA_FALLING_EDGE_DETECT_CNTL	17:16	0x0	Controls the detection of falling edge of external trigger A signal 00 = do not detect falling edge 01 = always detect falling edge 10 = detect falling edge only when field polarity is low 11 = detect falling edge only when field polarity is high
D2CRTC_TRIGA_FREQUENCY_SELECT	21:20	0x0	Determines the frequency of the external trigger A signal 00 = send every signal 01 = send every 2 signals 10 = reserved 11 = send every 4 signals
D2CRTC_TRIGA_DELAY	28:24	0x0	A programmable delay to send external trigger A signal
D2CRTC_TRIGA_CLEAR (W)	31	0x0	Clears the sticky bit D2CRTC_TRIGA_OCCURRED when written with '1'

Controls for external trigger A signal in CRTC2

D2CRTC_TRIGA_MANUAL_TRIG - RW - 32 bits - DISPDEC:0x6864			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_TRIGA_MANUAL_TRIG (W)	0	0x0	One shot trigger for external trigger A signal when written with '1'

Manual trigger for external trigger A signal of CRTC2

D2CRTC_TRIGB_CNTL - RW - 32 bits - DISPDEC:0x6868			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_TRIGB_SOURCE_SELECT	3:0	0x0	Select source of input signals for external trigger B 0 = logic 0 1 = VSYNCA from another CRTC of the chip 2 = HSYNCA from another CRTC of the chip 3 = VSYNCB from another CRTC of the chip 4 = HSYNCB from another CRTC of the chip 5 = GENERICA pin 6 = GENERICB pin 7 = VSYNCA pin 8 = HSYNCA pin 9 = VSYNCB pin 10 = HSYNCB pin 11 = HPD1 pin 12 = HPD2 pin 13 = DVALID pin 14 = PSYNC pin 15 = Video capture complete signal from VIP
D2CRTC_TRIGB_POLARITY_SELECT	6:4	0x0	Selects source of input signal from polarity of external trigger B 0 = logic 0 1 = interlace polarity from another CRTC of the chip 2 = GENERICA pin 3 = GENERICB pin 4 = HSYNCA pin 5 = HSYNCB pin 6 = video capture polarity input from VIP 7 = DVALID pin
D2CRTC_TRIGB_RESYNC_BYPASS_EN	8	0x0	Bypass the resync logic for the external trigger B signal and its polarity input signal 0 = do not bypass 1 = bypass the resync logic
D2CRTC_TRIGB_INPUT_STATUS (R)	9	0x0	Read back the value of the external trigger B input signal after the mux
D2CRTC_TRIGB_POLARITY_STATUS (R)	10	0x0	Reports the value of the external trigger B polarity signal after the mux
D2CRTC_TRIGB_OCCURRED (R)	11	0x0	Reports whether external trigger B has occurred. A sticky bit. 0 = has not occurred 1 = has occurred
D2CRTC_TRIGB_RISING_EDGE_DETECT_CNTL	13:12	0x0	Controls the detection of rising edge of the external trigger B signal 00 = do not detect rising edge 01 = always detect rising edge 10 = detect rising edge only when field polarity is low 11 = detect rising edge only when field polarity is high
D2CRTC_TRIGB_FALLING_EDGE_DETECT_CNTL	17:16	0x0	Controls the detection of falling edge of external trigger B signal 00 = do not detect falling edge 01 = always detect falling edge 10 = detect falling edge only when field polarity is low 11 = detect falling edge only when field polarity is high
D2CRTC_TRIGB_FREQUENCY_SELECT	21:20	0x0	Determines the frequency of the external trigger B signal 00 = send every signal 01 = send every 2 signals 10 = reserved 11 = send every 4 signals
D2CRTC_TRIGB_DELAY	28:24	0x0	A programmable delay to send external trigger B signal
D2CRTC_TRIGB_CLEAR (W)	31	0x0	Clears the sticky bit D2CRTC_TRIGB_OCCURRED when written with '1'

Control for external trigger B signal of CRTC2

D2CRTC_TRIGB_MANUAL_TRIG - RW - 32 bits - DISPDEC:0x686C

Field Name	Bits	Default	Description
D2CRTC_TRIGB_MANUAL_TRIG (W)	0	0x0	One shot trigger for external trigger B signal when written with '1'

Manual trigger for external trigger B signal of CRTC2

D2CRTC_FORCE_COUNT_NOW_CNTL - RW - 32 bits - DISPDEC:0x6870			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_FORCE_COUNT_NOW_MODE	1:0	0x0	Controls which timing counter is forced 0 = force counter now mode is disabled 1 = force H count now to H_TOTAL only 2 = force H count to H_TOTAL and V count to V_TOTAL in progressive mode and V_TOTAL-1 in interlaced mode 3 = reserved
D2CRTC_FORCE_COUNT_NOW_TRIG_SEL	8	0x0	Selects the trigger signal as force count now trigger 0 = selects CRTC_TRIG_A and CRTC_TRIG_A_POL 1 = selects CRTC_TRIG_B and CRTC_TRIG_B_POL
D2CRTC_FORCE_COUNT_NOW_OCCURRED (R)	16	0x0	Reports the status of force count now, a sticky bit. 0 = CRTC force count now has not occurred 1 = CRTC force count now has occurred
D2CRTC_FORCE_COUNT_NOW_CLEAR (W)	24	0x0	Resets D2CRTC_FORCE_COUNT_NOW_OCCURRED when written with '1'

Controls CRTC2 force count now logic

D2CRTC_FLOW_CONTROL - RW - 32 bits - DISPDEC:0x6874			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_FLOW_CONTROL_SOURCE_SELECT	3:0	0x0	Selects the signal used for flow control in CRTC2 0 = logic 0 1 = GENERICA pin 2 = GENERICB pin 3 = HPD1 pin 4 = HPD2 pin 5 = DDC1DATA pin 6 = DDC1CLK pin 7 = DDC2DATA pin 8 = DDC2CLK pin 9 = DVOCLK(1) pin 10 = VHAD(0] pin 11 = VHAD[1] pin 12 = VPHCTL pin 13 = VIPCLK pin 14 = DVALID pin 15 = PSYNC pin
D2CRTC_FLOW_CONTROL_POLARITY	8	0x0	Reports the status of force count now, a sticky bit. 0 = CRTC force count now has not occurred 1 = CRTC force count now has occurred
D2CRTC_FLOW_CONTROL_GRANULARITY	16	0x0	Controls at which pixel position flow control can start to happen 0 = flow control only start to happen on odd-even pixel boundary 1 = flow control can start at any pixel position
D2CRTC_FLOW_CONTROL_INPUT_STATUS (R)	24	0x0	Reports the value of the flow control input signal 0 = output of source mux of flow control signal is low 1 = output of source mux of flow control signal is high

Controls flow control of CRTC2

D2CRTC_PIXEL_DATA_READBACK - RW - 32 bits - DISPDEC:0x6878			
Field Name	**Bits**	**Default**	**Description**

D2CRTC_PIXEL_DATA_BLUE_CB (R)	9:0	0x0	B/Cb component sent to DISPOUT
D2CRTC_PIXEL_DATA_GREEN_Y (R)	19:10	0x0	G/Y component sent to DISPOUT
D2CRTC_PIXEL_DATA_RED_CR (R)	29:20	0x0	R/Cr component sent to DISPOUT

Read back of the CRTC2 pixel data sent to DISPOUT. This is a debug register. Intended for use in one shot clocking mode.

D2CRTC_STEREO_FORCE_NEXT_EYE - RW - 32 bits - DISPDEC:0x687C			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_STEREO_FORCE_NEXT_EYE (W)	1:0	0x0	Force next frame eye view - One shot. 00: No force - next eye opposite of current eye 01: Right eye force - force right eye next field/frame 10: Left eye force - force right eye next field/frame 11: Reserved After a force has occurred, readback of this register will be 00

Force Next Eye register

D2CRTC_CONTROL - RW - 32 bits - DISPDEC:0x6880			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_MASTER_EN	0	0x0	Enables/Disables CRTC2. H counter is at H_TOTAL and V counter is at first line of blank when CRTC is disabled. 0 = disabled 1 = enabled
D2CRTC_SYNC_RESET_SEL	4	0x0	Allows power management to lower CRTC2 enable.
D2CRTC_DISABLE_POINT_CNTL	9:8	0x1	When D2CRTC_MASTER_EN is set to 0, delay the disabling of CRTC2 until certain point within the frame 00 = disable CRTC immediately 01 = delay disable CRTC until the end of the current line 10 = reserved 11 = delay disable CRTC until end of the first line in the vertical blank region
D2CRTC_CURRENT_MASTER_EN_STATE (R)	16	0x0	Read-only field indicates the current status of the timing generator. Can be used to poll for when a delayed disable takes effect. 0 = CRTC is disabled 1 = CRTC is enabled
D2CRTC_DISP_READ_REQUEST_DISABLE	24	0x0	Disables data read request from the display controller. Can be used to stop display reads from system memory but keep display timing generation running. Has no effect if CRTC is disabled. 0 = do not disable data read request 1 = disable data read request

Controls CRTC2 timing generator and data read request to display2

D2CRTC_BLANK_CONTROL - RW - 32 bits - DISPDEC:0x6884			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_CURRENT_BLANK_STATE (R)	0	0x0	Read only status indicating current state of display blanking. 0 = screen not blanked 1 = screen is blanked

D2CRTC_BLANK_DATA_EN	8	0x0	Enable for blanking active display area. The active area of display that is forced will use the D2CRTC_BLACK_COLOR value. This field is optionally double buffered with D2CRTC_BLANK_DATA_DOUBLE_BUFFER_EN. 0 = disable blanking 1 = enable blanking
D2CRTC_BLANK_DE_MODE	16	0x0	Determines whether BLANK and DATA_ACTIVE signal keeps toggling when screen is blank 0 = toggles BLANK and DATA_ACTIVE 1 = keep BLANK active and DATA_ACTIVE inactive

Controls forced blanking of active area of display timing. Useful for display mode switches when corrupted image may be generated for a frame or two.

D2CRTC_INTERLACE_CONTROL - RW - 32 bits - DISPDEC:0x6888			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_INTERLACE_ENABLE	0	0x0	Enables interlaced timing 0 = Progressive timing 1 = Interlaced timing
D2CRTC_INTERLACE_FORCE_NEXT_FIELD (W)	17:16	0x0	One shot force next field polarity when written 00 = does not force next field 01 = force only next field to odd 10 = force only next field to even 11 = does not force next field

Interlaced timing control for CRTC2

D2CRTC_INTERLACE_STATUS - RW - 32 bits - DISPDEC:0x688C			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_INTERLACE_CURRENT_FIELD (R)	0	0x0	Reports the polarity of current field 0 = even 1 = odd
D2CRTC_INTERLACE_NEXT_FIELD (R)	1	0x0	Reports the polarity of the next field. Normally the opposite of the current field. When D2CRTC_INTERLACE_FORCE_NEXT_FIELD is used to force polarity of next field, then next field can match current field. 0 = even 1 = odd

Read-only register reports the polarity of the current and next field for interlaced timing

D2CRTC_BLANK_DATA_COLOR - RW - 32 bits - DISPDEC:0x6890			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_BLANK_DATA_COLOR_BLUE_CB	9:0	0x0	B / Cb component
D2CRTC_BLANK_DATA_COLOR_GREEN_Y	19:10	0x0	G / Y component
D2CRTC_BLANK_DATA_COLOR_RED_CR	29:20	0x0	R / Cr component

Set the color for pixels in blank region

D2CRTC_OVERSCAN_COLOR - RW - 32 bits - DISPDEC:0x6894			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_OVERSCAN_COLOR_BLUE	9:0	0x0	B or Cb component
D2CRTC_OVERSCAN_COLOR_GREEN	19:10	0x0	G or Y component
D2CRTC_OVERSCAN_COLOR_RED	29:20	0x0	R or Cr component

Defines color of the overscan region for CRTC2

D2CRTC_BLACK_COLOR - RW - 32 bits - DISPDEC:0x6898			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_BLACK_COLOR_B_CB	9:0	0x0	B / Cb component of the black color
D2CRTC_BLACK_COLOR_G_Y	19:10	0x0	G / Y component of the black color
D2CRTC_BLACK_COLOR_R_CR	29:20	0x0	R / Cr component of the black color

Black color applied to the active display region when blanking the screen

D2CRTC_STATUS - RW - 32 bits - DISPDEC:0x689C			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_V_BLANK (R)	0	0x0	Current vertical position 0 = outside vertical blank region 1 = within vertical blank region
D2CRTC_V_ACTIVE_DISP (R)	1	0x0	Current vertical position 0 = outside vertical active display region 1 = within vertical active display region
D2CRTC_V_SYNC_A (R)	2	0x0	Current vertical position 0 = outside VSYNC 1 = within VSYNC
D2CRTC_V_UPDATE (R)	3	0x0	Current vertical position 0 = outside the V_UPDATE region 1 = within the V_UPDATE region (between end of vertical active display and start_line]
D2CRTC_V_START_LINE (R)	4	0x0	Current vertical position 0 = outside start_line region 1 = within start_line region
D2CRTC_H_BLANK (R)	16	0x0	Current horizontal position 0 = outside horizontal blank region 1 = within horizontal blank region
D2CRTC_H_ACTIVE_DISP (R)	17	0x0	Current horizontal region 0 = outside horizontal active display region 1 = within horizontal active display region
D2CRTC_H_SYNC_A (R)	18	0x0	Current horizontal position 0 = outside horizontal sync 1 = within horizontal sync

Reports the position of CRTC2

D2CRTC_STATUS_POSITION - RW - 32 bits - DISPDEC:0x68A0			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_VERT_COUNT (R)	12:0	0x0	Reports current vertical count
D2CRTC_HORZ_COUNT (R)	28:16	0x0	Reports current horizontal count

Current horizontal and vertical count of CRTC2

D2CRTC_STATUS_FRAME_COUNT - RW - 32 bits - DISPDEC:0x68A4			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_FRAME_COUNT (R)	23:0	0x0	Reports current frame count

Current frame count for CRTC2

D2CRTC_STATUS_VF_COUNT - RW - 32 bits - DISPDEC:0x68A8			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_VF_COUNT (R)	28:0	0x0	Reports current vertical and frame count

Current composite vertical and frame count for CRTC2

D2CRTC_STATUS_HV_COUNT - RW - 32 bits - DISPDEC:0x68AC			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_HV_COUNT (R)	28:0	0x0	Reports current horizontal and vertical count

Current composite H/V count of CRTC2

D2CRTC_COUNT_RESET - RW - 32 bits - DISPDEC:0x68B0			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_RESET_FRAME_COUNT (W)	0	0x0	One-shot reset of frame counter of CRTC2 when written with '1'

Resets CRTC2 counters

D2CRTC_COUNT_CONTROL - RW - 32 bits - DISPDEC:0x68B4			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_HORZ_COUNT_BY2_EN	0	0x0	Enable the horizontal replication of 2. CRTC increments the H counter every 2 pixel clocks 0 = disabled 1 = enabled

Controls the counters in CRTC2

D2CRTC_MANUAL_FORCE_VSYNC_NEXT_LINE - RW - 32 bits - DISPDEC:0x68B8			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_MANUAL_FORCE_VSYNC_NEXT_LINE (W)	0	0x0	One shot force VSYNCA to happen next line when written with '1'

Manual force of VSYNC to happen next line

D2CRTC_VERT_SYNC_CONTROL - RW - 32 bits - DISPDEC:0x68BC			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_FORCE_VSYNC_NEXT_LINE_OCCURRED (R)	0	0x0	Reports whether force vsync next line event has occurred. Sticky bit. 0 = event has not occurred 1 = event has occurred

D2CRTC_FORCE_VSYNC_NEXT_LINE_CLEAR (W)	8	0x0	One shot clear to the sticky bit D1CRTC_FORCE_VSYNC_NEXT_LINE_OCCURRED when written with '1'
D2CRTC_AUTO_FORCE_VSYNC_MODE	17:16	0x0	Selection of auto mode for forcing vsync next line 00 = disables auto mode 01 = force VSYNC next line on CRTC trigger A signal 10 = force VSYNC next line on CRTC trigger B signal 11 = reserved

Controls the feature to force VSYNC next line for CRTC2

D2CRTC_STEREO_STATUS - RW - 32 bits - DISPDEC:0x68C0			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_STEREO_CURRENT_EYE (R)	0	0x0	Reports the polarity of the current frame/field 0 = right eye image 1 = left eye image
D2CRTC_STEREO_SYNC_OUTPUT (R)	8	0x0	Reports current value of STEREOSYNC signal
D2CRTC_STEREO_SYNC_SELECT (R)	16	0x0	Reports current value of SYNC_SELECT signal
D2CRTC_STEREO_FORCE_NEXT_EYE_PENDING (R)	25:24	0x0	Reports the status of D2CRTC_STEREO_FORCE_NEXT_EYE write. 00: No force pending 01: Right force pending 10: Left force pending 11: Reserved

Reports CRTC2 status in stereoscopic display

D2CRTC_STEREO_CONTROL - RW - 32 bits - DISPDEC:0x68C4			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_STEREO_SYNC_OUTPUT_POLARITY	8	0x0	Controls polarity of the stereosync signal 0 = 0 means right eye image and 1 means left eye image 1 = 0 means left eye image and 1 means right eye image
D2CRTC_STEREO_SYNC_SELECT_POLARITY	16	0x0	Controls polarity of STEREO_SELECT signal sent to scaler 0 = 0 means right eye image and 1 means left eye image 1 = 0 means left eye image and 1 means right eye image
D2CRTC_STEREO_EN	24	0x0	Enables toggling of STEREOSYNC and STEREO_SELECT signals 0 = disable toggling. 1 = enable toggling at every frame (progressive) or every field (interlace) at leading edge of VSYNCA

Stereosync control for CRTC2

D2CRTC_SNAPSHOT_STATUS - RW - 32 bits - DISPDEC:0x68C8			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_SNAPSHOT_OCCURRED (R)	0	0x0	Reports status of snapshot. A sticky bit to be cleared by writing 1 to D2CRTC_SNAPSHOT_CLEAR 0 = snapshot has not occurred 1 = snapshot has occurred
D2CRTC_SNAPSHOT_CLEAR (W)	1	0x0	Clears the D2CRTC_SNAPSHOT_OCCURRED sticky bit when written with '1'
D2CRTC_SNAPSHOT_MANUAL_TRIGGER (W)	2	0x0	One shot trigger to perform snapshot when written with '1'

Controls CRTC2 snapshot

D2CRTC_SNAPSHOT_CONTROL - RW - 32 bits - DISPDEC:0x68CC			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_AUTO_SNAPSHOT_TRIG_SEL	1:0	0x0	Determines signal source for auto-snapshot 00 = auto-snapshot is disabled 01 = uses CRTC trigger A as trigger event in auto-snapshot mode 10 = uses CRTC trigger B as trigger event in auto-snapshot mode 11 = reserved

Controls snapshot mode for CRTC2

D2CRTC_SNAPSHOT_POSITION - RW - 32 bits - DISPDEC:0x68D0			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_SNAPSHOT_VERT_COUNT (R)	12:0	0x0	Reads back the snapshoted vertical count
D2CRTC_SNAPSHOT_HORZ_COUNT (R)	28:16	0x0	Reads back the snapshoted horizontal count

Snapshot H and V count for CRTC2

D2CRTC_SNAPSHOT_FRAME - RW - 32 bits - DISPDEC:0x68D4			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_SNAPSHOT_FRAME_COUNT (R)	23:0	0x0	Reports the snapshoted frame count

Snapshot frame count of CRTC2

D2CRTC_START_LINE_CONTROL - RW - 32 bits - DISPDEC:0x68D8			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_PROGRESSIVE_START_LINE_EARLY	0	0x0	move start_line signal by 1 line earlier in progressive mode
D2CRTC_INTERLACE_START_LINE_EARLY	8	0x1	move start_line signal by 1 line earlier in interlaced timing mode

move start_line signal earlier by 1 line in CRTC2

D2CRTC_INTERRUPT_CONTROL - RW - 32 bits - DISPDEC:0x68DC			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_SNAPSHOT_INT_MSK	0	0x0	Interrupt mask for CRTC snapshot event 0 = disables interrupt 1 = enables interrupt
D2CRTC_FORCE_COUNT_NOW_INT_MSK	8	0x0	Interrupt mask for force count now event 0 = disables interrupt 1 = enables interrupt
D2CRTC_FORCE_VSYNC_NEXT_LINE_INT_MSK	16	0x0	Interrupt mask for force VSYNC next line event 0 = disables interrupt 1 = enables interrupt
D2CRTC_TRIGA_INT_MSK	24	0x0	Interrupt mask for CRTC external trigger A 0 = disables interrupt 1 = enables interrupt
D2CRTC_TRIGB_INT_MSK	25	0x0	Interrupt mask for CRTC external trigger B 0 = disables interrupt 1 = enables interrupt

Interrupt mask for CRTC2 events

D2MODE_MASTER_UPDATE_LOCK - RW - 32 bits - DISPDEC:0x68E0			
Field Name	**Bits**	**Default**	**Description**
D2MODE_MASTER_UPDATE_LOCK	0	0x0	Set the master update lock for V_UPDATE signal 0 = no master lock, V_UPDATE signal will occur 1 = set master lock to prevent V_UPDATE signal occurring, thus prevent double buffering of display registers

Master update lock for CRTC2 V_UPDATE signal

D2MODE_MASTER_UPDATE_MODE - RW - 32 bits - DISPDEC:0x68E4			
Field Name	**Bits**	**Default**	**Description**
D2MODE_MASTER_UPDATE_MODE	1:0	0x0	Controls the position of the V_UPDATE signal 00 = V_UPDATE occurs between end of active display region and start line signal 01 = V_UPDATE occurs when leading edge of HSYNCA meets leading edge of VSYNCA 10 = V_UPDATE occurs at the leading edge of VSYNC_A 11 = V_UPDATE occurs at the beginning of the first line of vertical front porch
D2MODE_MASTER_UPDATE_INTERLACED_MODE	17:16	0x0	Controls generation of V_UPDATE signal in interlaced mode 00 = generates V_UPDATE at both even and odd field 01 = generates V_UPDATE only at even field. when D1MODE_MASTER_UPDATE_MODE = 00, V_UPDATE starts at odd field and ends at even field 10 = generates V_UPDATE only at odd field. when D1MODE_MASTER_UPDATE_MODE = 00, V_UPDATE starts at even field and ends at odd field 11 = reserved

Controls the generation of the V_UPDATE signal in CRTC2

D2CRTC_UPDATE_LOCK - RW - 32 bits - DISPDEC:0x68E8			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_UPDATE_LOCK	0	0x0	Set the lock for CRTC timing registers 0 = no lock, double buffering can occur 1 = set lock to prevent double buffering

Update lock for CRTC2 timing registers

D2CRTC_DOUBLE_BUFFER_CONTROL - RW - 32 bits - DISPDEC:0x68EC			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_UPDATE_PENDING (R)	0	0x0	Reports the status of double-buffered timing registers in CRTC2 0 = update has completed 1 = update is still pending
D2CRTC_UPDATE_INSTANTLY	8	0x0	Disables double buffering of CRTC2 timing registers 0 = enables double buffering 1 = disables double buffering
D2CRTC_BLANK_DATA_DOUBLE_BUFFER_EN	16	0x0	Enables the double buffering of D2CRTC_BLANK_DATA_EN 0 = disables double buffering. D2CRTC_BLANK_DATA_EN is updated immediately 1 = enables double buffering of D2CRTC_BLANK_DATA_EN when V_UPDATE is active

Controls double buffering of CRTC2 registers

D2CRTC_VGA_PARAMETER_CAPTURE_MODE - RW - 32 bits - DISPDEC:0x68F0			
Field Name	**Bits**	**Default**	**Description**
D2CRTC_VGA_PARAMETER_CAPTURE_MODE	0	0x0	Controls how VGA timing parameters are captured. 0: CRTC2 will continuously latch in timing parameters from VGA 1: CRTC2 will continuously latch in timing parameters from VGA except during VGA parameter recalculated window

Controls how VGA timing parameters are captured

2.9 Display Output Registers

DACA_ENABLE - RW - 32 bits - DISPDEC:0x7800			
Field Name	**Bits**	**Default**	**Description**
DACA_ENABLE	0	0x0	0=Disable 1=Enable
Turn on/off DACA			

DACA_SOURCE_SELECT - RW - 32 bits - DISPDEC:0x7804			
Field Name	**Bits**	**Default**	**Description**
DACA_SOURCE_SELECT	1:0	0x0	0=Source is CRTC1 1=Source is CRTC2 2=Source is TV Encoder 3=Reserved
Select between 1st display, 2nd display & TV encoder streams			

DACA_CRC_EN - RW - 32 bits - DISPDEC:0x7808			
Field Name	**Bits**	**Default**	**Description**
DACA_CRC_EN	0	0x0	Enable signal for DACA CRC 0=Disable 1=Enable
DACA_CRC_CONT_EN	16	0x0	Determines whether CRC is calculated continuously or for one frame (one shot) 0=CRC is calculated over 1 frame 1=CRC is continuously calculated for every frame
DACA CRC enable signals			

DACA_CRC_CONTROL - RW - 32 bits - DISPDEC:0x780C			
Field Name	**Bits**	**Default**	**Description**
DACA_CRC_FIELD	0	0x0	Controls which field polarity starts the DACA CRC block after DACA_CRC_EN is set high. Used only for interlaced mode CRCs 0=Even field begins CRC calculation 1=Odd field begins CRC calculation
DACA_CRC_ONLY_BLANKb	8	0x0	Determines whether CRC is calculated for the whole frame or only during non-blank period for DACA 0=CRC calculated over entire field 1=CRC calculated only during BLANKb
DACA CRC controls signals			

DACA_CRC_SIG_RGB_MASK - RW - 32 bits - DISPDEC:0x7810			
Field Name	**Bits**	**Default**	**Description**
DACA_CRC_SIG_BLUE_MASK	9:0	0x3ff	Mask bits for DACA B channel CRC
DACA_CRC_SIG_GREEN_MASK	19:10	0x3ff	Mask bits for DACA G channel CRC
DACA_CRC_SIG_RED_MASK	29:20	0x3ff	Mask bits for DACA R channel CRC
Mask bits for R, G & B CRC calculations			

DACA_CRC_SIG_CONTROL_MASK - RW - 32 bits - DISPDEC:0x7814			
Field Name	**Bits**	**Default**	**Description**
DACA_CRC_SIG_CONTROL_MASK	5:0	0x3f	Mask bits for DACA control signal CRC

Mask bits for DACA control signal CRC

DACA_CRC_SIG_RGB - RW - 32 bits - DISPDEC:0x7818			
Field Name	**Bits**	**Default**	**Description**
DACA_CRC_SIG_BLUE (R)	9:0	0x3ff	CRC signature value for DACA blue component
DACA_CRC_SIG_GREEN (R)	19:10	0x3ff	CRC signature value for DACA green component
DACA_CRC_SIG_RED (R)	29:20	0x3ff	CRC signature value for DACA red component

DACA CRC R, G & B results

DACA_CRC_SIG_CONTROL - RW - 32 bits - DISPDEC:0x781C			
Field Name	**Bits**	**Default**	**Description**
DACA_CRC_SIG_CONTROL (R)	5:0	0x3f	CRC signature value for DACA control signals

CRC signature value for DACA control signals

DACA_SYNC_TRISTATE_CONTROL - RW - 32 bits - DISPDEC:0x7820			
Field Name	**Bits**	**Default**	**Description**
DACA_HSYNCA_TRISTATE	0	0x0	DACA hsync tristate. Used to determine hsynca enable
DACA_VSYNCA_TRISTATE	8	0x0	DACA vsync tristate. Used to determine vsynca enable
DACA_SYNCA_TRISTATE	16	0x0	DACA sync tristate. Used to determine sync enables

DACA SYNC Tristate control

DACA_SYNC_SELECT - RW - 32 bits - DISPDEC:0x7824			
Field Name	**Bits**	**Default**	**Description**
DACA_SYNC_SELECT	0	0x0	0: selects sync_a 1: selects sync_b. Used in conjunction with DACA_SOURCE_SEL(0). 0=DACA uses HSYNC_A & VSYNC_A 1=DACA used HSYNC_B & VSYNC_B
DACA_STEREOSYNC_SELECT	8	0x0	0: selects crtc1 stereosync 1: selects crtc2 stereosync 0=DACA uses CRTC1 STEREOSYNC 1=DACA uses CRTC2 STEREOSYNC

DACA ...SYNC selection

DACA_AUTODETECT_CONTROL - RW - 32 bits - DISPDEC:0x7828			
Field Name	**Bits**	**Default**	**Description**
DACA_AUTODETECT_MODE	1:0	0x0	Operation control of DACA Autodetect logic: 0: No checking 1: Connection checking 2: Disconnection checking
DACA_AUTODETECT_FRAME_TIME_COUNTER	15:8	0x0	If an enabled display pipe is connected to DACA, autodetect logic will count number of frames before DACA comparator enabled.Otherwise, the autodetect logic will count number of 0.1-second units.
DACA_AUTODETECT_CHECK_MASK	18:16	0x7	Mask to select which of the 3 RGB channels will be checked for connection or disconnection. Bit 18: Check R/C channel if bit set to 1. Bit 17: Check G/Y channel if bit set to 1. Bit 16: Check B/Comp channel if bit set to 1.

DACA_AUTODETECT_CONTROL2 - RW - 32 bits - DISPDEC:0x782C			
Field Name	**Bits**	**Default**	**Description**
DACA_AUTODETECT_POWERUP_COUNTER	7:0	0xb	DACA macro Bandgap voltage reference power up time. Default = 11 microseconds.
DACA_AUTODETECT_TESTMODE	8	0x0	0: Normal operation 1: Test mode - count in 1us units

DACA_AUTODETECT_STATUS - RW - 32 bits - DISPDEC:0x7834			
Field Name	**Bits**	**Default**	**Description**
DACA_AUTODETECT_STATUS (R)	0	0x0	Result from autodetect logic sequence: 0: DACA was looking for a connection and has yet found a connection or DACA was looking for a disconnection has not yet found a disconnection 1: DACA was looking for a connection and found a connection or DACA was looking for a disconnection and found a disconnection
DACA_AUTODETECT_CONNECT (R)	4	0x0	1: At least one channel has a properly terminated device connected. 0: No devices are connected
DACA_AUTODETECT_RED_SENSE (R)	9:8	0x0	Two bit result from last Red/C compare: 0: Channel is disconnected 1: Channel is connected 2: Channel is not checked 3: Reserved
DACA_AUTODETECT_GREEN_SENSE (R)	17:16	0x0	Two bit result from last Green/Y compare: 0: Channel is disconnected 1: Channel is connected 2: Channel is not checked 3: Reserved
DACA_AUTODETECT_BLUE_SENSE (R)	25:24	0x0	Two bit result from last Blue/Comp compare: 0: Channel is disconnected 1: Channel is connected 2: Channel is not checked 3: Reserved

DACA_AUTODETECT_INT_CONTROL - RW - 32 bits - DISPDEC:0x7838			
Field Name	**Bits**	**Default**	**Description**
DACA_AUTODETECT_ACK (W)	0	0x0	Auto detect interrupt acknowledge and clear DACA_AUTODETECT_STATUS bit.
DACA_AUTODETECT_INT_ENABLE	16	0x0	Enable for auto detect interrupt 0=Disable 1=Enable

DACA_FORCE_OUTPUT_CNTL - RW - 32 bits - DISPDEC:0x783C			
Field Name	**Bits**	**Default**	**Description**
DACA_FORCE_DATA_EN	0	0x0	Enable synchronous force option on DACA. 0=Disable 1=Enable
DACA_FORCE_DATA_SEL	10:8	0x0	Select which DACA channels have data forced 0=Don't Force, 1=ForceBit 0: Blue channel Bit 1: Green channel Bit 2: Red channel
DACA_FORCE_DATA_ON_BLANKb_ONLY	24	0x0	Data is force only during active region. 0=Disable 1=Enable

Data Force Control

DACA_FORCE_DATA - RW - 32 bits - DISPDEC:0x7840			
Field Name	**Bits**	**Default**	**Description**
DACA_FORCE_DATA	9:0	0x0	Data to be forced on R, G & B channels. When auto detect logic is enabled, this must be programmed to 0x000 (Default).

DACA_POWERDOWN - RW - 32 bits - DISPDEC:0x7850			
Field Name	**Bits**	**Default**	**Description**
DACA_POWERDOWN	0	0x0	Bandgap Voltage Reference Power down enable (BGSLEEP)
DACA_POWERDOWN_BLUE	8	0x0	Blue channel power down enable (BDACPD)
DACA_POWERDOWN_GREEN	16	0x0	Green channel power down enable (GDACPD)
DACA_POWERDOWN_RED	24	0x0	Red channel power down enable (RDACPD)

Controls for DACA Start-Up & Power-Down sequences

DACA_CONTROL1 - RW - 32 bits - DISPDEC:0x7854			
Field Name	**Bits**	**Default**	**Description**
DACA_WHITE_LEVEL	1:0	0x0	Video Standard Select bits - STD(1:0) 0x0: PAL 0x1: NTSC PS2 (VGA) 0x3 HDTV (Component Video)
DACA_WHITE_FINE_CONTROL	12:8	0x10	Full-scale Output Adjustment - DACADJ(4:0)
DACA_BANDGAP_ADJUSTMENT	19:16	0x8	Bandgap Reference Voltage Adjustment - BGADJ(3:0)
DACA_ANALOG_MONITOR	27:24	0x0	Analog test mux select - MON(3:0)

DACA_CONTROL2 - RW - 32 bits - DISPDEC:0x7858			
Field Name	**Bits**	**Default**	**Description**
DACA_DFORCE_EN	0	0x0	DACA asynchronous data force enable. Can be used for sync force as well but DACA_FORCE_OUTPUT_CNTL achieves the same goal with a more complete feature set. Asynchronous force requires DACA_x_ASYNC_ENABLE in DACA_COMPARATOR_ENABLE to be set as well. Drives DFORCE_EN pin on macro. Forces all DACA channels to DACA_FORCE_DATA value. Overrides DACA_FORCE_OUTPUT_CNTL/DACA_FORCE_DATA_EN control.
DACA_ZSCALE_SHIFT	16	0x0	DACA zero scale shift enable. Causes DACA to add a small offset to the levels of all outputs. Drives DACA ZSCALE_SHIFT pin.

DACA_COMPARATOR_ENABLE - RW - 32 bits - DISPDEC:0x785C			
Field Name	**Bits**	**Default**	**Description**
DACA_COMP_DDET_REF_EN	0	0x0	Enables DACA comparators for analog termination checking with DDETECT_REF as the reference. The DDETECT reference level is lower than SDETECT_REF to allow termination checking on an active channel while the data being driven is the ZSCALE_SHIFT offset.Must be used in conjunction with ZSCALE_SHIFT=1 and with some forced data on the DAC inputs. Only one of COMP_DDET_REF_EN and COMP_SDET_REF_EN should be active at a time.Used in conjunction with core logic to drive the DAC DDETECT pin. 0=Disable 1=Enable
DACA_COMP_SDET_REF_EN	8	0x0	Enables DACA comparators for analog termination checking with SDETECT_REF as the reference. The data must be forced to a sufficiently high value using one of the DAC force features. Only one of COMP_DDET_REF_EN and COMP_SDET_REF_EN should be active at a time.Goes directly to the DAC SDETECT pin. 0=Disable 1=Enable
DACA_R_ASYNC_ENABLE	16	0x0	DACA red channel asynchronous mode enable.Allows DAC outputs to be updated without a clock.Used in conjunction with core logic to drive the DAC R_ASYNC_EN pin. 0=Disable 1=Enable
DACA_G_ASYNC_ENABLE	17	0x0	DACA green channel asynchronous mode enable.Used in conjunction with core logic to drive the DAC G_ASYNC_EN pin. 0=Disable 1=Enable
DACA_B_ASYNC_ENABLE	18	0x0	DACA blue channel asynchronous mode enable.Used in conjunction with core logic to drive the DAC B_ASYNC_EN pin. 0=Disable 1=Enable

DACA_COMPARATOR_OUTPUT - RW - 32 bits - DISPDEC:0x7860			
Field Name	**Bits**	**Default**	**Description**
DACA_COMPARATOR_OUTPUT (R)	0	0x0	Monitor Detect Output. This signal is an AND of 3 DAC macro signals: R_CDET, G_YDET & B_COMPDET.
DACA_COMPARATOR_OUTPUT_BLUE (R)	1	0x0	DACA blue channel comparator output value comes from DAC R_CDET pin
DACA_COMPARATOR_OUTPUT_GREEN (R)	2	0x0	DACA green channel comparator output value comes from DAC G_YDET pin
DACA_COMPARATOR_OUTPUT_RED (R)	3	0x0	DACA red channel comparator output value comes from DAC B_COMPDET pin

DACA_TEST_ENABLE - RW - 32 bits - DISPDEC:0x7864			
Field Name	**Bits**	**Default**	**Description**
DACA_TEST_ENABLE	0	0x0	DACATEST Enable 0=Disable 1=Enable

DACA_PWR_CNTL - RW - 32 bits - DISPDEC:0x7868			
Field Name	**Bits**	**Default**	**Description**
DACA_BG_MODE	1:0	0x0	DACA bandgap macro configuration. Allows bandgap macro to be configured to optimize performance.Goes directly to DAC BG_MODE[1:0] input.

DACB_ENABLE - RW - 32 bits - DISPDEC:0x7A00			
Field Name	**Bits**	**Default**	**Description**
DACB_ENABLE	0	0x0	0=Disable 1=Enable

Turn on/off DACB

DACB_SOURCE_SELECT - RW - 32 bits - DISPDEC:0x7A04			
Field Name	**Bits**	**Default**	**Description**
DACB_SOURCE_SELECT	1:0	0x0	0=Source is CRTC1 1=Source is CRTC2 2=Source is TV Encoder 3=Reserved

Select between 1st display, 2nd display & TV encoder streams

DACB_CRC_EN - RW - 32 bits - DISPDEC:0x7A08			
Field Name	**Bits**	**Default**	**Description**
DACB_CRC_EN	0	0x0	Enable signal for DACB CRC 0=Disable 1=Enable
DACB_CRC_CONT_EN	16	0x0	Determines whether CRC is calculated for the whole frame or only during non-blank period for DACB 0=Disable 1=Enable

DACB CRC enable signals

DACB_CRC_CONTROL - RW - 32 bits - DISPDEC:0x7A0C			
Field Name	**Bits**	**Default**	**Description**
DACB_CRC_FIELD	0	0x0	Controls which field polarity starts the DACB CRC block after DACA_CRC_EN is set high. Used only for interlaced mode CRCs. 0=Even field begins CRC calculation 1=Odd field begins CRC calculation
DACB_CRC_ONLY_BLANKb	8	0x0	CRC only during the Non-blank region 0=CRC calculated over entire field 1=CRC calculated only during BLANKb

DACB CRC controls signals

DACB_CRC_SIG_RGB_MASK - RW - 32 bits - DISPDEC:0x7A10			
Field Name	**Bits**	**Default**	**Description**
DACB_CRC_SIG_BLUE_MASK	9:0	0x3ff	Mask bits for DACB B channel CRC
DACB_CRC_SIG_GREEN_MASK	19:10	0x3ff	Mask bits for DACB G channel CRC
DACB_CRC_SIG_RED_MASK	29:20	0x3ff	Mask bits for DACB R channel CRC

Mask bits for R, G & B CRC calculations

DACB_CRC_SIG_CONTROL_MASK - RW - 32 bits - DISPDEC:0x7A14			
Field Name	**Bits**	**Default**	**Description**
DACB_CRC_SIG_CONTROL_MASK	5:0	0x3f	Mask bits for DACB control signal CRC

Mask bits for DACB control signal CRC

DACB_CRC_SIG_RGB - RW - 32 bits - DISPDEC:0x7A18			
Field Name	**Bits**	**Default**	**Description**
DACB_CRC_SIG_BLUE (R)	9:0	0x3ff	CRC signature value for DACB blue component
DACB_CRC_SIG_GREEN (R)	19:10	0x3ff	CRC signature value for DACB green component
DACB_CRC_SIG_RED (R)	29:20	0x3ff	CRC signature value for DACB red component

DACB CRC R, G & B results

DACB_CRC_SIG_CONTROL - RW - 32 bits - DISPDEC:0x7A1C			
Field Name	**Bits**	**Default**	**Description**
DACB_CRC_SIG_CONTROL (R)	5:0	0x3f	CRC signature value for DACB control signals

CRC signature value for DACB control signals

DACB_SYNC_TRISTATE_CONTROL - RW - 32 bits - DISPDEC:0x7A20			
Field Name	**Bits**	**Default**	**Description**
DACB_HSYNCB_TRISTATE	0	0x0	DACB hsync tristate. Used to determine hsyncb enable
DACB_VSYNCB_TRISTATE	8	0x0	DACB vsync tristate. Used to determine vsyncb enable
DACB_SYNCB_TRISTATE	16	0x0	DACB sync tristate. Used to determine sync enables

DACB SYNC Tristate control

DACB_SYNC_SELECT - RW - 32 bits - DISPDEC:0x7A24			
Field Name	**Bits**	**Default**	**Description**
DACB_SYNC_SELECT	0	0x0	0=DACB uses HSYNC_A & VSYNC_A 1=DACB used HSYNC_B & VSYNC_B
DACB_STEREOSYNC_SELECT	8	0x0	0=DACB uses CRTC1 STEREOSYNC 1=DACB uses CRTC2 STEREOSYNC

DACB_AUTODETECT_CONTROL - RW - 32 bits - DISPDEC:0x7A28			
Field Name	**Bits**	**Default**	**Description**
DACB_AUTODETECT_MODE	1:0	0x0	Operation control of DACB Autodetect logic: 0: No checking 1: Connection checking 2: Disconnection checking
DACB_AUTODETECT_FRAME_TIME_COUNTER	15:8	0x0	If an enabled display pipe is connected to DACB, autodetect logic will count number of frames before DACB comparator enabled.Otherwise, the autodetect logic will count number of 0.1-second units.
DACB_AUTODETECT_CHECK_MASK	18:16	0x7	Mask to select which of the 3 RGB channels will be checked for connection or disconnection. Bit 18: Check R/C channel if bit set to 1. Bit 17: Check G/Y channel if bit set to 1. Bit 16: Check B/Comp channel if bit set to 1.

DACB_AUTODETECT_CONTROL2 - RW - 32 bits - DISPDEC:0x7A2C			
Field Name	**Bits**	**Default**	**Description**
DACB_AUTODETECT_POWERUP_COUNTER	7:0	0xb	DACB macro Bandgap voltage reference power up time. Default = 11 microseconds.
DACB_AUTODETECT_TESTMODE	8	0x0	0: Normal operation 1: Test mode - count in 1us units

DACB_AUTODETECT_STATUS - RW - 32 bits - DISPDEC:0x7A34			
Field Name	**Bits**	**Default**	**Description**

DACB_AUTODETECT_STATUS (R)	0	0x0	Result from autodetect logic sequence: 0: DACB was looking for a connection and has yet found a connection or DACB was looking for a disconnection has not yet found a disconnection 1: DACB was looking for a connection and found a connection or DACB was looking for a disconnection and did not find a disconnection
DACB_AUTODETECT_CONNECT (R)	4	0x0	0=No devices are connected 1=At least one channel has a properly terminated device connected
DACB_AUTODETECT_RED_SENSE (R)	9:8	0x0	Two bit result from last Red/C compare: 0: Channel is disconnected 1: Channel is connected 2: Channel is not checked 3: Reserved
DACB_AUTODETECT_GREEN_SENSE (R)	17:16	0x0	Two bit result from last Green/Y compare: 0: Channel is disconnected 1: Channel is connected 2: Channel is not checked 3: Reserved
DACB_AUTODETECT_BLUE_SENSE (R)	25:24	0x0	Two bit result from last Blue/Comp compare: 0: Channel is disconnected 1: Channel is connected 2: Channel is not checked 3: Reserved

DACB_AUTODETECT_INT_CONTROL - RW - 32 bits - DISPDEC:0x7A38			
Field Name	**Bits**	**Default**	**Description**
DACB_AUTODETECT_ACK (W)	0	0x0	Auto detect interrupt acknowledge and clear DACB_AUTODETECT_STATUS bit.
DACB_AUTODETECT_INT_ENABLE	16	0x0	Enable for auto detect interrupt 0=Disable 1=Enable

DACB_FORCE_OUTPUT_CNTL - RW - 32 bits - DISPDEC:0x7A3C			
Field Name	**Bits**	**Default**	**Description**
DACB_FORCE_DATA_EN	0	0x0	Enable synchronous force option on DACB 0=Disable 1=Enable
DACB_FORCE_DATA_SEL	10:8	0x0	Select which DACB channels have data forced 0=Don't Force, 1=Force Bit 0: Blue channel Bit 1: Green channel Bit 2: Red channel
DACB_FORCE_DATA_ON_BLANKb_ONLY	24	0x0	Data is force only during active region. 0=Disable 1=Enable

Data Force Control

DACB_FORCE_DATA - RW - 32 bits - DISPDEC:0x7A40			
Field Name	**Bits**	**Default**	**Description**
DACB_FORCE_DATA	9:0	0x0	Data to be forced on R, G & B channels

DACB_POWERDOWN - RW - 32 bits - DISPDEC:0x7A50			
Field Name	**Bits**	**Default**	**Description**
DACB_POWERDOWN	0	0x0	Bandgap Voltage Reference Power down enable (BGSLEEP)ANDed with controls from power management and LVDS power sequencer.
DACB_POWERDOWN_BLUE	8	0x0	Blue channel power-down enable - BDACPD
DACB_POWERDOWN_GREEN	16	0x0	Green channel power-down enable - GDACPD
DACB_POWERDOWN_RED	24	0x0	Red channel power-down enable - RDACPD

Controls for DACB Start-Up & Power-Down sequences

DACB_CONTROL1 - RW - 32 bits - DISPDEC:0x7A54			
Field Name	**Bits**	**Default**	**Description**
DACB_WHITE_LEVEL	1:0	0x0	Video Standard Select bits - STD(1:0) 0x0: PAL 0x1: NTSC PS2 (VGA) 0x3 HDTV (Component Video)
DACB_WHITE_FINE_CONTROL	12:8	0x10	Full-scale Output Adjustment - DACADJ(4:0)
DACB_BANDGAP_ADJUSTMENT	19:16	0x8	Bandgap Reference Voltage Adjustment - BGADJ(3:0)
DACB_ANALOG_MONITOR	27:24	0x0	Analog test mux select - MON(3:0)
DACB_COREMON	28	0x0	Core voltage monitor input port

DACB_CONTROL2 - RW - 32 bits - DISPDEC:0x7A58			
Field Name	**Bits**	**Default**	**Description**
DACB_DFORCE_EN	0	0x0	DACB asynchronous data force enable. Can be used for sync force as well but DACB_FORCE_OUTPUT_CNTL achieves the same goal with a more complete feature set. Async force requires async bits in DACB_COMPARATOR_ENABLE to be set as well. Drives DFORCE_EN pin on macro. Forces all DACB channels to DACB_FORCE_DATA value. Overrides DACB_FORCE_OUTPUT_CNTL/DACB_FORCE_DATA_EN control.
DACB_TV_ENABLE	8	0x0	DACB tv enable. Controls DACB output demux. R/G/B is selected when TV_ENABLE=0, Y/C/Comp when TV_ENABLE=1. Drives DAC TVENABLE input.
DACB_ZSCALE_SHIFT	16	0x0	DACB zero scale shift enable. Causes DAC to add a small offset to the levels of all outputs. Drives DAC ZSCALE_SHIFT pin.

DACB_COMPARATOR_ENABLE - RW - 32 bits - DISPDEC:0x7A5C			
Field Name	**Bits**	**Default**	**Description**
DACB_COMP_DDET_REF_EN	0	0x0	Enables DACB comparators for analog termination checking with DDETECT_REF as the reference. The DDETECT reference level is lower than SDETECT_REF to allow termination checking on an active channel while the data being driven is the ZSCALE_SHIFT offset.Must be used in conjunction with ZSCALE_SHIFT=1 or with some forced data on the DAC inputs. Only one of COMP_DDET_REF_EN and COMP_SDET_REF_EN should be active at a time.Used in conjunction with core logic to drive the DAC DDETECT pin. 0=Disable 1=Enable
DACB_COMP_SDET_REF_EN	8	0x0	Enables DACB comparators for analog termination checking with SDETECT_REF as the reference. The data must be forced to a sufficiently high value using one of the DAC force features. Only one of COMP_DDET_REF_EN and COMP_SDET_REF_EN should be active at a time.Goes directly to the DAC SDETECT pin. 0=Disable 1=Enable
DACB_R_ASYNC_ENABLE	16	0x0	DACB red channel asynchronous mode enable.Allows DAC outputs to be updated without a clock.Used in conjunction with core logic to drive the DAC R_ASYNC_EN pin. 0=Disable 1=Enable
DACB_G_ASYNC_ENABLE	17	0x0	DACB green channel asynchronous mode enable.Used in conjunction with core logic to drive the DAC G_ASYNC_EN pin. 0=Disable 1=Enable
DACB_B_ASYNC_ENABLE	18	0x0	DACB blue channel asynchronous mode enable.Used in conjunction with core logic to drive the DAC B_ASYNC_EN pin. 0=Disable 1=Enable

DACB_COMPARATOR_OUTPUT - RW - 32 bits - DISPDEC:0x7A60			
Field Name	**Bits**	**Default**	**Description**
DACB_COMPARATOR_OUTPUT (R)	0	0x0	Monitor Detect Output. This signal is an AND of 4 dac macro signals: DETECT, RDACDET, GDACDET & BDACDET.
DACB_COMPARATOR_OUTPUT_BLUE (R)	1	0x0	DACB blue channel comparator output value comes from DAC BDACDET pin
DACB_COMPARATOR_OUTPUT_GREEN (R)	2	0x0	DACB green channel comparator output value comes from DAC GDACDET pin
DACB_COMPARATOR_OUTPUT_RED (R)	3	0x0	DACB red channel comparator output value comes from DAC RDACDET pin

DACB_TEST_ENABLE - RW - 32 bits - DISPDEC:0x7A64			
Field Name	**Bits**	**Default**	**Description**
DACB_TEST_ENABLE	0	0x0	0=Disable 1=Enable

DACBTEST Enable. Use for DAC test only. Drives DAC

DACB_PWR_CNTL - RW - 32 bits - DISPDEC:0x7A68			
Field Name	**Bits**	**Default**	**Description**
DACB_BG_MODE	1:0	0x0	DACB bandgap macro configuration. Allows bandgap macro to be configured to optimize performance.Goes directly to DAC BG_MODE[1:0] input.
DACB_PWRCNTL	17:16	0x0	DACB bias current level control. Allows analog bias current levels to be adjusted for performance vs. power consumption tradeoff.Goes directly to DAC PWRCNTL[1:0] input.

TMDSA_CNTL - RW - 32 bits - DISPDEC:0x7880			
Field Name	**Bits**	**Default**	**Description**
TMDSA_ENABLE	0	0x0	Enable for the reduction/encoding logic 0=Disable 1=Enable
TMDSA_ENABLE_HPD_MASK	4	0x0	0:Disallow 1:Allow override of TMDSA_ENABLE by HPD on disconnect 0=Result from HPD circuit can not override TMDSA_ENABLE 1=Result from HPD circuit can override TMDSA_ENABLE on disconnect
TMDSA_HPD_SELECT	8	0x0	Select which hot plug detect unit to use for TMDSA. This selection is only relevant if one of the HPD mask bits in this and other registers is enabled. 0=Use HPD1 1=Use HPD2
TMDSA_SYNC_PHASE	12	0x1	Determine whether to reset phase signal on frame pulse 0: don't reset 1: reset
TMDSA_PIXEL_ENCODING	16	0x0	0=RGB 4:4:4 or YCBCR 4:4:4 1=YCbCr 4:2:2
TMDSA_DUAL_LINK_ENABLE	24	0x0	Enable dual-link 0=Disable 1=Enable
TMDSA_SWAP	28	0x0	Swap upper and lower data channels 0=Disable 1=Enable

TMDSA_SOURCE_SELECT - RW - 32 bits - DISPDEC:0x7884			
Field Name	**Bits**	**Default**	**Description**
TMDSA_SOURCE_SELECT	0	0x0	Select between display stream 1 & display stream 2 0=CRTC1 data is used 1=CRTC2 data is used
TMDSA_SYNC_SELECT	8	0x0	Select between SYNCA and SYNCB signals 0=HSYNC_A & VSYNC_A from the selected CRTC are used 1=HSYNC_B & VSYNC_B from the selected CRTC are used
TMDSA_STEREOSYNC_SELECT	16	0x0	Select between CRTC1 and CRTC2 stereosync signals 0=CRTC1 STEREOSYNC used 1=CRTC2 STEREOSYNC used

Source Select control for Data, H/VSYNC & Stereosync

TMDSA_COLOR_FORMAT - RW - 32 bits - DISPDEC:0x7888			
Field Name	**Bits**	**Default**	**Description**

TMDSA_COLOR_FORMAT	1:0	0x0	Controls TMDSA output colour format 0=Normal (24bpp) or Twin Single (8 MSBs of each component) 1=Twin-Single (2 LSB of each component) 2=Dual-Link 30bpp 3=Reserved

TMDSA_FORCE_OUTPUT_CNTL - RW - 32 bits - DISPDEC:0x788C			
Field Name	**Bits**	**Default**	**Description**
TMDSA_FORCE_DATA_EN	0	0x0	Enable force option on TMDSA 0=Disable 1=Enable
TMDSA_FORCE_DATA_SEL	10:8	0x0	Select TMDSA channels that have data forced0=Don't Force, 1=Force Bit 0: Blue channel Bit 1: Green channel Bit 2: Red channel
TMDSA_FORCE_DATA_ON_BLANKb_ONLY	16	0x0	Data is forced only during active region. 0=Disable 1=Enable

Data Force Control

TMDSA_FORCE_DATA - RW - 32 bits - DISPDEC:0x7890			
Field Name	**Bits**	**Default**	**Description**
TMDSA_FORCE_DATA	7:0	0x0	8 bit Data put on TMDS output data channels according to TMDSA_FORCE_DATA_SEL when Force feature enabled (TMDSA_FORCE_DATA_EN = 1)

TMDSA_BIT_DEPTH_CONTROL - RW - 32 bits - DISPDEC:0x7894			
Field Name	**Bits**	**Default**	**Description**
TMDSA_TRUNCATE_EN	0	0x0	Enable bit reduction by truncation 0=Disable 1=Enable
TMDSA_TRUNCATE_DEPTH	4	0x0	Controls bits per pixel 0=18bpp 1=24bpp
TMDSA_SPATIAL_DITHER_EN	8	0x0	Enable bit reduction by spatial (random) dither 0=Disable 1=Enable
TMDSA_SPATIAL_DITHER_DEPTH	12	0x0	Controls bits per pixel 0=18bpp 1=24bpp
TMDSA_TEMPORAL_DITHER_EN	16	0x0	Enable bit reduction by temporal dither (frame mod.) 0=Disable 1=Enable
TMDSA_TEMPORAL_DITHER_DEPTH	20	0x0	Controls bits per pixel 0=18bpp 1=24bpp
TMDSA_TEMPORAL_LEVEL	24	0x0	Gray level select (2 or 4 levels) 0=Gray level 2(1 bit - LSB) 1=Gray level 4(2 bits - 2 LSBs)

TMDSA_TEMPORAL_DITHER_RESET	26	0x0	Reset temporal dither (frame modulation) 0=Temporal Dither Ready 1=Reset Temporal Dither Circuit

Control the method in which the data input into the TMDS block is reduced and the length it is reduced to.

TMDSA_CONTROL_CHAR - RW - 32 bits - DISPDEC:0x7898			
Field Name	**Bits**	**Default**	**Description**
TMDSA_CONTROL_CHAR0_OUT_EN	0	0x0	Programmable sync character 0 enable
TMDSA_CONTROL_CHAR1_OUT_EN	1	0x0	Programmable sync character 1 enable
TMDSA_CONTROL_CHAR2_OUT_EN	2	0x0	Programmable sync character 2 enable
TMDSA_CONTROL_CHAR3_OUT_EN	3	0x0	Programmable sync character 3 enable

SYNC Character Enable. Each bit represents the use of register defined sync character.

TMDSA_CONTROL0_FEEDBACK - RW - 32 bits - DISPDEC:0x789C			
Field Name	**Bits**	**Default**	**Description**
TMDSA_CONTROL0_FEEDBACK_SELECT	1:0	0x0	Select input of CTL0 for TMDSA
TMDSA_CONTROL0_FEEDBACK_DELAY	9:8	0x0	Select delay of CTL0 for TMDSA

TMDSA_STEREOSYNC_CTL_SEL - RW - 32 bits - DISPDEC:0x78A0			
Field Name	**Bits**	**Default**	**Description**
TMDSA_STEREOSYNC_CTL_SEL	1:0	0x0	Controls which CTL signal STEREOSYNC goes on to 0=TMDS CTL registers have normal functionality 1=Stereosync will use TMDS CTL1 register 2=Stereosync will use TMDS CTL2 register 3=Stereosync will use TMDS CTL3 register

TMDSA_SYNC_CHAR_PATTERN_SEL - RW - 32 bits - DISPDEC:0x78A4			
Field Name	**Bits**	**Default**	**Description**
TMDSA_SYNC_CHAR_PATTERN_SEL	3:0	0x0	Reserved

Not Currently Connected

TMDSA_SYNC_CHAR_PATTERN_0_1 - RW - 32 bits - DISPDEC:0x78A8			
Field Name	**Bits**	**Default**	**Description**
TMDSA_SYNC_CHAR_PATTERN0	9:0	0x0	TMDSA SYNC character set 0
TMDSA_SYNC_CHAR_PATTERN1	25:16	0x0	TMDSA SYNC character set 1

TMDSA_SYNC_CHAR_PATTERN_2_3 - RW - 32 bits - DISPDEC:0x78AC			
Field Name	**Bits**	**Default**	**Description**
TMDSA_SYNC_CHAR_PATTERN2	9:0	0x0	TMDSA SYNC character set 2
TMDSA_SYNC_CHAR_PATTERN3	25:16	0x0	TMDSA SYNC character set 3

TMDSA_CRC_CNTL - RW - 32 bits - DISPDEC:0x78B0			
Field Name	**Bits**	**Default**	**Description**
TMDSA_CRC_EN	0	0x0	Enable TMDSA primary CRC calculation 0=Disable 1=Enable
TMDSA_CRC_CONT_EN	4	0x0	Select continuous or one-shot mode for primary CRC 0=CRC is calculated over 1 frame 1=CRC is continuously calculated for every frame
TMDSA_CRC_ONLY_BLANKb	8	0x0	Determines whether primary CRC is calculated for the whole frame or only during non-blank period. 0=CRC calculated over entire field 1=CRC calculated only during BLANKb
TMDSA_CRC_FIELD	12	0x0	Controls which field polarity starts the TMDSA CRC block after TMDSA_CRC_EN is set to 1. Used only for interlaced mode CRCs 0=Even field begins CRC calculation 1=Odd field begins CRC calculation
TMDSA_2ND_CRC_EN	16	0x0	Enable TMDSA 2nd CRC calculation 0=Disable 1=Enable
TMDSA_2ND_CRC_SEL	20	0x0	Select which TMDS link to perform CRC on. 0=Perform CRC on link0 1=Perform CRC on link1
TMDSA_2ND_CRC_DE_ONLY	24	0x1	Select whether to perform CRC on all data or active (data enable) region only. 0=2ND CRC calculated over entire field 1=2ND CRC calculated only during BLANKb

Enable TMDSA CRC Calculation

TMDSA_CRC_SIG_MASK - RW - 32 bits - DISPDEC:0x78B4			
Field Name	**Bits**	**Default**	**Description**
TMDSA_CRC_SIG_BLUE_MASK	7:0	0xff	CRC mask bits for TMDSA blue component
TMDSA_CRC_SIG_GREEN_MASK	15:8	0xff	CRC mask bits for TMDSA green component
TMDSA_CRC_SIG_RED_MASK	23:16	0xff	CRC mask bits for TMDSA red component
TMDSA_CRC_SIG_CONTROL_MASK	26:24	0x7	CRC mask bits for TMDSA control signals 3-bit input value: bit 2 = Vsync bit 1 = Hsync bit 0 =Data Enable

RGB and Control CRC Mask

TMDSA_CRC_SIG_RGB - RW - 32 bits - DISPDEC:0x78B8			
Field Name	**Bits**	**Default**	**Description**
TMDSA_CRC_SIG_BLUE (R)	7:0	0x0	CRC signature value for TMDSA blue component
TMDSA_CRC_SIG_GREEN (R)	15:8	0x0	CRC signature value for TMDSA green component
TMDSA_CRC_SIG_RED (R)	23:16	0x0	CRC signature value for TMDSA red component
TMDSA_CRC_SIG_CONTROL (R)	26:24	0x0	CRC signature value for TMDSA control signals3-bit input value: bit 2 = Vsync bit 1 = Hsync bit 0 =Data Enable

RGB and Control CRC Result

TMDSA_2ND_CRC_RESULT - RW - 32 bits - DISPDEC:0x78BC			
Field Name	**Bits**	**Default**	**Description**
TMDSA_2ND_CRC_RESULT (R)	29:0	0x0	Secondary TMDS CRC Result

TMDSA_TEST_PATTERN - RW - 32 bits - DISPDEC:0x78C0			
Field Name	**Bits**	**Default**	**Description**
TMDSA_TEST_PATTERN_OUT_EN	0	0x0	Controls the TMDSA output test pattern 0=Normal functionality determined by value of TMDSA_RANDOM_PATTERN_OUT_EN register 1=Test pattern output mode. The value of TMDSA_HALF_CLOCK_PATTERN_SEL determines whether a static 10-bit test data pattern or an alternating half-clock pattern will be output.
TMDSA_HALF_CLOCK_PATTERN_SEL	1	0x0	Controls between static pattern output and alternating static pattern output 0=10 bit test pattern from TMDSA_STATIC_TEST_PATTERN is sent for TMDS output during every pixel clock 1=Alternating pattern of TMDSA_STATIC_TEST_PATTERN and !(TMDSA_STATIC_TEST_PATTERN) on each subsequent pixel clock cycle is sent during every pixel clock
TMDSA_RANDOM_PATTERN_OUT_EN	4	0x0	Enable for random pattern output 0=Normal 1=TMDS Random Pixel Data Generator circuit generates 24-bit pixel data to be encoded and transmitted
TMDSA_RANDOM_PATTERN_RESET	5	0x1	Reset random pattern to pattern seed 0=Enable Random Pixel Data Generator 1=Random Pixel Data Generator is Reset to the value in TMDSA_RANDOM_PATTERN_SEED
TMDSA_TEST_PATTERN_EXTERNAL_RESET_EN	6	0x1	0: Normal 1: Hold non-static test pattern (random, half clock) in reset when external signal is asserted 0=Normal 1=External signal resets random and half clock patterns
TMDSA_STATIC_TEST_PATTERN	25:16	0x0	TMDSA test pixel. Replace the pixel value when TMDSA_TEST_PATTERN_OUT_EN=1

TMDSA_RANDOM_PATTERN_SEED - RW - 32 bits - DISPDEC:0x78C4			
Field Name	**Bits**	**Default**	**Description**
TMDSA_RANDOM_PATTERN_SEED	23:0	0x222222	Initial pattern for eye pattern measurement
TMDSA_RAN_PAT_DURING_DE_ONLY	24	0x0	Controls between random pattern out during entire field and DE 0=TMDS Random Data Pattern is output for all pixels 1=TMDS Random Data Pattern is only output when DE is high

TMDSA_DEBUG - RW - 32 bits - DISPDEC:0x78C8			
Field Name	**Bits**	**Default**	**Description**
TMDSA_DEBUG_EN	0	0x0	Set to 1 to enable debug mode
TMDSA_DEBUG_HSYNC	8	0x0	Debug mode HSYNC
TMDSA_DEBUG_HSYNC_EN	9	0x0	Set to 1 to enable debug mode HSYNC
TMDSA_DEBUG_VSYNC	16	0x0	Debug mode VSYNC
TMDSA_DEBUG_VSYNC_EN	17	0x0	Set to 1 to enable debug mode VSYNC

TMDSA_DEBUG_DE	24	0x0	Debug mode display enable
TMDSA_DEBUG_DE_EN	25	0x0	Set to 1 to enable debug mode display enable

TMDSA_CTL_BITS - RW - 32 bits - DISPDEC:0x78CC			
Field Name	**Bits**	**Default**	**Description**
TMDSA_CTL0	0	0x0	Control signal for TMDSA (encoded in Green channel).
TMDSA_CTL1	8	0x0	Control signal for TMDSA (encoded in Green channel).
TMDSA_CTL2	16	0x0	Control signal for TMDSA (encoded in Red channel).
TMDSA_CTL3	24	0x0	Control signal for TMDSA (encoded in Red channel).

TMDSA_DCBALANCER_CONTROL - RW - 32 bits - DISPDEC:0x78D0			
Field Name	**Bits**	**Default**	**Description**
TMDSA_DCBALANCER_EN	0	0x1	DC Balancer Enable 0=Disable 1=Enable
TMDSA_DCBALANCER_TEST_EN	8	0x0	DC Balancer Test Enable
TMDSA_DCBALANCER_TEST_IN	19:16	0x0	DC Balancer Test Input
TMDSA_DCBALANCER_FORCE	24	0x0	DC Balancer select value to use when DCBALANCER_EN=0

TMDSA_RED_BLUE_SWITCH - RW - 32 bits - DISPDEC:0x78D4			
Field Name	**Bits**	**Default**	**Description**
TMDSA_RB_SWITCH_EN	0	0x0	Switch Red and Blue encoding position. 0=Disable 1=Enable

TMDSA_DATA_SYNCHRONIZATION - RW - 32 bits - DISPDEC:0x78D8			
Field Name	**Bits**	**Default**	**Description**
TMDSA_DSYNSEL	0	0x0	Data synchronization circuit select enable 0=Disable 1=Enable
TMDSA_PFREQCHG (W)	8	0x0	Write to 1 to restarts read and write address generation logic. Write of 0 has no effect. Read value is always 0. PFREQCHG must be written to 1 when the data synchronizer is started by setting DSYNSEL to 1, TMDSA_DUAL_LINK_ENABLE is reprogrammed, or either PCLK_TMDSA or PCLK_TMDSA_DIRECT (IDCLK) is reprogrammed or stopped and restarted.

TMDSA Data Sychronization Control

TMDSA_CTL0_1_GEN_CNTL - RW - 32 bits - DISPDEC:0x78DC			
Field Name	**Bits**	**Default**	**Description**

TMDSA_CTL0_DATA_SEL	3:0	0x0	Select data to be used to generate CTL0 pattern (selected fields are ORed together) [0]: Display Enable [1]: VSYNC [2]: HSYNC [3] Random data
TMDSA_CTL0_DATA_DELAY	6:4	0x0	Number of pixel clocks to delay CTL0 data 0=CTL0 data is delayed 0 pixel clocks 1=CTL0 data is delayed 1 pixel clocks 2=CTL0 data is delayed 2 pixel clocks 3=CTL0 data is delayed 3 pixel clocks 4=CTL0 data is delayed 4 pixel clocks 5=CTL0 data is delayed 5 pixel clocks 6=CTL0 data is delayed 6 pixel clocks 7=CTL0 data is delayed 7 pixel clocks
TMDSA_CTL0_DATA_INVERT	7	0x0	Set to 1 to invert CTL0 data 0=CTL0 data is normal 1=CTL0 data is inverted
TMDSA_CTL0_DATA_MODULATION	9:8	0x0	CTL0 data modulation control 0=CTL0 data is not modulated 1=CTL0 data is modulated by bit 0 of 2 bit counter 2=CTL0 data is modulated by bit 1 of 2 bit counter 3=CTL0 data is modulated every time 2 bit counter overflows
TMDSA_CTL0_USE_FEEDBACK_PATH	10	0x0	Set to 1 to enable CTL0 internal feedback path
TMDSA_CTL0_FB_SYNC_CONT	11	0x0	Set to 1 to force continunous toggle on CTL0 internal feedback path
TMDSA_CTL0_PATTERN_OUT_EN	12	0x0	Select CTL0 output data 0=Register value 1=Pattern generator output
TMDSA_CTL1_DATA_SEL	19:16	0x0	Select data to be used to generate CTL1 pattern (selected fields are ORed together) [0]: Display Enable [1]: VSYNC [2]: HSYNC [3] Always (blank time)
TMDSA_CTL1_DATA_DELAY	22:20	0x0	Number of pixel clocks to delay CTL1 data 0=CTL1 data is delayed 0 pixel clocks 1=CTL1 data is delayed 1 pixel clocks 2=CTL1 data is delayed 2 pixel clocks 3=CTL1 data is delayed 3 pixel clocks 4=CTL1 data is delayed 4 pixel clocks 5=CTL1 data is delayed 5 pixel clocks 6=CTL1 data is delayed 6 pixel clocks 7=CTL1 data is delayed 7 pixel clocks
TMDSA_CTL1_DATA_INVERT	23	0x0	Set to 1 to invert CTL1 data 0=CTL1 data is normal 1=CTL1 data is inverted
TMDSA_CTL1_DATA_MODULATION	25:24	0x0	CTL1 data modulation control 0=CTL1 data is not modulated 1=CTL1 data is modulated by bit 0 of 2 bit counter 2=CTL1 data is modulated by bit 1 of 2 bit counter 3=CTL1 data is modulated every time 2 bit counter overflows
TMDSA_CTL1_USE_FEEDBACK_PATH	26	0x0	Set to 1 to enable CTL1 internal feedback path
TMDSA_CTL1_FB_SYNC_CONT	27	0x0	Set to 1 to force continunous toggle on CTL1 internal feedback path
TMDSA_CTL1_PATTERN_OUT_EN	28	0x0	Select CTL1 output data 0=Register value 1=Pattern generator output
TMDSA_2BIT_COUNTER_EN	31	0x0	Set to 1 to enable 2-bit data modulation counter 0=Disable 1=Enable

TMDSA_CTL2_3_GEN_CNTL - RW - 32 bits - DISPDEC:0x78E0

Field Name	Bits	Default	Description
TMDSA_CTL2_DATA_SEL	3:0	0x0	Select data to be used to generate CTL2 pattern (selected fields are ORed together) [0]: Display Enable [1]: VSYNC [2]: HSYNC [3] Always (blank time)
TMDSA_CTL2_DATA_DELAY	6:4	0x0	Number of pixel clocks to delay CTL2 data 0=CTL2 data is delayed 0 pixel clocks 1=CTL2 data is delayed 1 pixel clocks 2=CTL2 data is delayed 2 pixel clocks 3=CTL2 data is delayed 3 pixel clocks 4=CTL2 data is delayed 4 pixel clocks 5=CTL2 data is delayed 5 pixel clocks 6=CTL2 data is delayed 6 pixel clocks 7=CTL2 data is delayed 7 pixel clocks
TMDSA_CTL2_DATA_INVERT	7	0x0	Set to 1 to invert CTL2 data 0=CTL2 data is normal 1=CTL2 data is inverted
TMDSA_CTL2_DATA_MODULATION	9:8	0x0	CTL2 data modulation control 0=CTL2 data is not modulated 1=CTL2 data is modulated by bit 0 of 2 bit counter 2=CTL2 data is modulated by bit 1 of 2 bit counter 3=CTL2 data is modulated every time 2 bit counter overflows
TMDSA_CTL2_USE_FEEDBACK_PATH	10	0x0	Set to 1 to enable CTL2 internal feedback path
TMDSA_CTL2_FB_SYNC_CONT	11	0x0	Set to 1 to force continunous toggle on CTL2 internal feedback path
TMDSA_CTL2_PATTERN_OUT_EN	12	0x0	Select CTL2 output data 0=Register value 1=Pattern generator output
TMDSA_CTL3_DATA_SEL	19:16	0x0	Select data to be used to generate CTL3 pattern (selected fields are ORed together) [0]: Display Enable [1]: VSYNC [2]: HSYNC [3] Always (blank time)
TMDSA_CTL3_DATA_DELAY	22:20	0x0	Number of pixel clocks to delay CTL3 data 0=CTL3 data is delayed 0 pixel clocks 1=CTL3 data is delayed 1 pixel clocks 2=CTL3 data is delayed 2 pixel clocks 3=CTL3 data is delayed 3 pixel clocks 4=CTL3 data is delayed 4 pixel clocks 5=CTL3 data is delayed 5 pixel clocks 6=CTL3 data is delayed 6 pixel clocks 7=CTL3 data is delayed 7 pixel clocks
TMDSA_CTL3_DATA_INVERT	23	0x0	Set to 1 to invert CTL3 data 0=CTL3 data is normal 1=CTL3 data is inverted
TMDSA_CTL3_DATA_MODULATION	25:24	0x0	CTL3 data modulation control 0=CTL3 data is not modulated 1=CTL3 data is modulated by bit 0 of 2 bit counter 2=CTL3 data is modulated by bit 1 of 2 bit counter 3=CTL3 data is modulated every time 2 bit counter overflows
TMDSA_CTL3_USE_FEEDBACK_PATH	26	0x0	Set to 1 to enable CTL3 internal feedback path
TMDSA_CTL3_FB_SYNC_CONT	27	0x0	Set to 1 to force continunous toggle on CTL3 internal feedback path
TMDSA_CTL3_PATTERN_OUT_EN	28	0x0	Select CTL3 output data 0=Register value 1=Pattern generator output

TMDSA_TRANSMITTER_ENABLE - RW - 32 bits - DISPDEC:0x7904			
Field Name	**Bits**	**Default**	**Description**

TMDSA_TX0_ENABLE	0	0x0	TMDSA link0 enable (ILNK0EN)(set to 1 whenever TMDS is enabled) 0=Disable 1=Enable
TMDSA_LNKC0EN	1	0x0	TMDSA clock channel enable (ICHCEN)(set to 1 whenever TMDS is enabled)
TMDSA_LNKD00EN	2	0x0	TMDSA link0 data channel 0 enable (ICHD0EN)(set to 1 whenever TMDS is enabled)
TMDSA_LNKD01EN	3	0x0	TMDSA link0 data channel 1 enable (ICHD1EN)(set to 1 whenever TMDS is enabled)
TMDSA_LNKD02EN	4	0x0	TMDSA link0 data channel 2 enable (ICHD2EN)(set to 1 whenever TMDS is enabled)
TMDSA_TX1_ENABLE	8	0x0	TMDSA link1 enable (ILNKD1EN)(set to 1 whenever TMDS is enabled in dual-link mode)
TMDSA_LNKD10EN	10	0x0	TMDSA link1 data channel 0 enable (ICHD3EN)(set to 1 whenever TMDS is enabled in dual-link mode)
TMDSA_LNKD11EN	11	0x0	TMDSA link1 data channel 1 enable (ICHD4EN)(set to 1 whenever TMDS is enabled in dual-link mode)
TMDSA_LNKD12EN	12	0x0	TMDSA link1 data channel 2 enable (ICHD5EN)(set to 1 whenever TMDS is enabled in dual-link mode)
TMDSA_TX_ENABLE_HPD_MASK	16	0x0	0:Disallow 1:Allow override of TMDSA_TXX_ENABLE by HPD on disconnect 0=Result from HPD circuit can not override TMDSA_TXX_ENABLE 1=Result from HPD circuit can override TMDSA_TXX_ENABLE on disconnect
TMDSA_LNKCEN_HPD_MASK	17	0x0	0:Disallow 1:Allow override of TMDSA_LNKCXEN by HPD on disconnect 0=Result from HPD circuit can not override TMDSA_LNKC0EN 1=Result from HPD circuit overrides TMDSA_LNKC0EN on disconnect
TMDSA_LNKDEN_HPD_MASK	18	0x0	0:Disallow 1:Allow override of TMDSA_LNKDXEN by HPD on disconnect 0=Result from HPD circuit can not override TMDSA_LNKDXEN 1=Result from HPD circuit overrides TMDSA_LNKDXEN on disconnect

TMDSA_LOAD_DETECT - RW - 32 bits - DISPDEC:0x7908			
Field Name	**Bits**	**Default**	**Description**
TMDSA_LOAD_DETECT_ENABLE	0	0x0	0: Disable 1: Enable TMDSA macro load detect functionDrives IMSEN macro input
TMDSA_LOAD_DETECT (R)	4	0x0	From TMDSA macro OMSEN output 0: No load detected 1: Load detected

TMDSA_MACRO_CONTROL - RW - 32 bits - DISPDEC:0x790C			
Field Name	**Bits**	**Default**	**Description**
TMDSA_PLL_CP_GAIN	5:0	0xb	TMDSA PLL charge-pump gain control. Go to IPPLCP(5:0) pins of TMDSA macro.
TMDSA_PLL_VCO_GAIN	13:8	0x7	TMDSA PLL VCO gain control. Go to IPPLVG(5:0) pins of TMDSA macro.
TMDSA_PLL_DUTY_CYCLE	17:16	0x0	TMDSA PLL duty cycle control. Go to IPPLDC(2:0) pins of TMDSA macro.
TMDSA_TX_VOLTAGE_SWING	23:20	0xa	TMDSA driver voltage swing control. Go to IPTXVS(3:0) pins of TMDSA macro.

TMDSA_TRANSMITTER_CONTROL - RW - 32 bits - DISPDEC:0x7910			
Field Name	**Bits**	**Default**	**Description**
TMDSA_PLL_ENABLE	0	0x0	TMDSA transmitter's PLL enable. This can power down the PLL. 0=Disable 1=Enable
TMDSA_PLL_RESET	1	0x1	TMDSA transmitter's PLL reset. PLL will start the locking acquisition process once this becomes low.
TMDSA_PLL_ENABLE_HPD_MASK	3:2	0x0	Determines whether result from HPD circuit can override TMDSA_PLL_ENABLE and TMDSA_PLL_RESET Bit 0: Set to 1 to enable override on disconnect Bit 1: Set to 1 to enable override on connect. 0=Result from HPD circuit can not override TMDSA_PLL_ENABLE 1=Result from HPD circuit overrides TMDSA_PLL_ENABLE on disconnect 2=Result from HPD circuit overrides TMDSA_PLL_ENABLE on connect 3=Result from HPD circuit overrides TMDSA_PLL_ENABLE
TMDSA_IDSCKSEL	4	0x1	0=TMDS Transmitter uses pclk_tmdsa (IPIXCLK) 1=TMDS Transmitter uses pclk_tmdsa_direct (IDCLK)
TMDSA_PLL_PWRUP_SEQ_EN	6	0x0	Enable hardware delay of PLL enable / reset on power up / down to match macro timing requirements. When TMDSA_PLL_PWRUP_SEQ_EN=1, PLL will be reset 1 us before PLL enable is deasserted, and PLL reset will be asserted for 10 us after PLL enable is asserted. This timing is provided to match the TMDS macro timing specification. 0=Disabled 1=Delay Enable/ Reset for clean PLL power up/down
TMDSA_TMCLK	12:8	0x0	For macro debug only
TMDSA_TMCLK_FROM_PADS	13	0x0	Controls input to ITMCLK pin on macro for macro debug only 0=Input to ITMCLK pins on macro come from TMDSA_TMCLK field 1=Input to ITMCLK pins on macro come from pads
TMDSA_TDCLK	14	0x0	For macro debug only
TMDSA_TDCLK_FROM_PADS	15	0x0	Controls input to ITDCLK pin on macro for macro debug only 0=Input to ITDCLK pin on macro comes from TMDSA_TDCLK field 1=Input to ITDCLK pin on macro comes from pads
TMDSA_BYPASS_PLL	28	0x1	Controls ICHCSEL pin on TMDSA macro 0: Coherent mode: transmitted clock is PLL output 1: Incoherent mode: transmitted clock is PLL input
TMDSA_INPUT_TEST_CLK_SEL	31	0x0	Controls ITCLKSEL pin on TMDSA macro

TMDSA_REG_TEST_OUTPUT - RW - 32 bits - DISPDEC:0x7914			
Field Name	**Bits**	**Default**	**Description**
TMDSA_REG_TEST_OUTPUT (R)	9:0	0x0	Outputs of the 10 shift registers (OTDATX[9:0]) from one of the channels during test mode.
TMDSA_TEST_CNTL	18:16	0x0	Selects which of six register test output channels from TMDSA macro is visible in TMDSA_REG_TEST_OUTPUT. 0=OTDAT0 1=OTDAT1 2=OTDAT2 3=OTDAT3 4=OTDAT4 5=OTDAT5 6=OTDAT0 7=OTDAT0

TMDSA_TRANSMITTER_DEBUG - RW - 32 bits - DISPDEC:0x7918			
Field Name	**Bits**	**Default**	**Description**
TMDSA_PLL_DEBUG	7:0	0x0	Drives ITPL pins on TMDSA macro
TMDSA_TX_DEBUG	11:8	0x0	Drives ITX pins on TMDSA macro

Reserved for debugging purposes

DVOA_ENABLE - RW - 32 bits - DISPDEC:0x7980			
Field Name	**Bits**	**Default**	**Description**
DVOA_ENABLE	0	0x0	Enable for DVO 0=Disable 1=Enable
DVOA_PIXEL_ENCODING	8	0x0	Selects pixel encoding format 0=RGB 4:4:4 or YCBCR 4:4:4 1=YCbCr 4:2:2

DVOA_SOURCE_SELECT - RW - 32 bits - DISPDEC:0x7984			
Field Name	**Bits**	**Default**	**Description**
DVOA_SOURCE_SELECT	0	0x0	Select between 1st and 2nd display streams 0=CRTC1 data is used 1=CRTC2 data is used
DVOA_SYNC_SELECT	8	0x0	Select between SYNCA and SYNCB signals from CRTC 0=HSYNC_A & VSYNC_A from the selected CRTC are used 1=HSYNC_B & VSYNC_B from the selected CRTC are used
DVOA_STEREOSYNC_SELECT	16	0x0	Select between CRTC1 and CRTC2 stereosync signals 0=DVOA Stereosync from CRTC1 used 1=DVOA Stereosync from CRTC2 used

Source Select control for Data, H/VSYNC & Stereosync

DVOA_BIT_DEPTH_CONTROL - RW - 32 bits - DISPDEC:0x7988			
Field Name	**Bits**	**Default**	**Description**
DVOA_TRUNCATE_EN	0	0x0	Enable bit reduction by truncation 0=Disable 1=Enable
DVOA_TRUNCATE_DEPTH	4	0x0	Select truncation depth 0=18bpp 1=24bpp
DVOA_SPATIAL_DITHER_EN	8	0x0	Enable bit reduction by spatial (random) dither 0=Disable 1=Enable
DVOA_SPATIAL_DITHER_DEPTH	12	0x0	Select spatial dither depth 0=18bpp 1=24bpp
DVOA_TEMPORAL_DITHER_EN	16	0x0	Enable bit reduction by temporal dither (frame mod.) 0=Disable 1=Enable
DVOA_TEMPORAL_DITHER_DEPTH	20	0x0	Select temporal dither depth 0=18bpp 1=24bpp

DVOA_TEMPORAL_LEVEL	24	0x0	Gray level select (2 or 4 levels) 0=Gray level 2 1=Gray level 4
DVOA_TEMPORAL_DITHER_RESET	26	0x0	Reset temporal dither (frame modulation)

Control the method in which the data input into the DVO block is reduced and the length it is reduced to.

DVOA_OUTPUT - RW - 32 bits - DISPDEC:0x798C			
Field Name	**Bits**	**Default**	**Description**
DVOA_OUTPUT_ENABLE_MODE	1:0	0x0	Output mode for DVO 0=disabled 1=lower 12 output en 2=upper 12 output en 3=all 24 output enable
DVOA_CLOCK_MODE	8	0x0	Reserved 0=differential clocking enabled 1=single ended clocking enabled

Output enable control for DVO pads.

DVOA_CONTROL - RW - 32 bits - DISPDEC:0x7990			
Field Name	**Bits**	**Default**	**Description**
DVOA_RATE_SELECT	0	0x0	Select between DDR and SDR modes 0=DDR Speed 1=SDR Speed
DVOA_DUAL_CHANNEL_EN	8	0x0	Enable Dual Channel DVO Mode 0=Disable 1=Enable
DVOA_RESET_BETWEEN_FRAMES	16	0x1	Reset control of DVO fifo between frames 0=DVO fifos not reset in between frames 1=DVO fifos reset at beginning of every new frame
DVOA_SYNC_PHASE	17	0x1	Determine whether to reset phase signal on frame pulse 0=Disable 1=Enable
DVOA_COLOR_FORMAT	25:24	0x0	0=8-bit DVO display 1=Twin Single Link 10-bit mode 2=Dual-Link 10-bit mode 3=Reserved
DVOA_REORDER_BITS	28	0x0	Reorder DVO bits output = input 1:0, input 7:2 0=Disable 1=Enable

DVOA_CRC_EN - RW - 32 bits - DISPDEC:0x7994			
Field Name	**Bits**	**Default**	**Description**
DVOA_CRC_EN	0	0x0	Enable DVO CRC 0=Disable 1=Enable
DVOA_CRC_CONT_EN	8	0x0	Select between one shot and continuous mode 0=CRC is calculated over 1 frame 1=CRC is continuously calculated for every frame
DVOA_CRC2_EN	16	0x0	Enable DVO output CRC2 0=Disable 1=Enable

DVOA_CRC_CONTROL - RW - 32 bits - DISPDEC:0x7998			
Field Name	**Bits**	**Default**	**Description**
DVOA_CRC_FIELD	0	0x0	Controls which field polarity starts the DVO CRC block after DAC_CRC_EN is set high 0=Even field begins CRC calculation 1=Odd field begins CRC calculation
DVOA_CRC_ONLY_BLANKb	8	0x0	Determines whether CRC is calculated for the whole frame or only during non-blank period for DVO 0=CRC calculated over entire field 1=CRC calculated only during BLANKb

DVOA_CRC_SIG_MASK1 - RW - 32 bits - DISPDEC:0x799C			
Field Name	**Bits**	**Default**	**Description**
DVOA_CRC_SIG_BLUE_MASK	7:0	0xff	Mask bits for DVO B channel CRC.
DVOA_CRC_SIG_GREEN_MASK	23:16	0xff	Mask bits for DVO G channel CRC.

Select which data the CRC calculation is performed on.

DVOA_CRC_SIG_MASK2 - RW - 32 bits - DISPDEC:0x79A0			
Field Name	**Bits**	**Default**	**Description**
DVOA_CRC_SIG_RED_MASK	7:0	0xff	Mask bits for DVO R channel CRC.
DVOA_CRC_SIG_CONTROL_MASK	18:16	0x7	Mask bits for DVO control signal CRC Bit 18: Vsync signal Bit 17: Hsync Signal Bit 16: Data Enable

Select which control signals the CRC calculation is performed on.

DVOA_CRC_SIG_RESULT1 - RW - 32 bits - DISPDEC:0x79A4			
Field Name	**Bits**	**Default**	**Description**
DVOA_CRC_SIG_BLUE (R)	7:0	0x0	CRC signature value for DVO B channel CRC.
DVOA_CRC_SIG_GREEN (R)	23:16	0x0	CRC signature value for DVO G channel CRC.

DVOA Data CRC Results

DVOA_CRC_SIG_RESULT2 - RW - 32 bits - DISPDEC:0x79A8			
Field Name	**Bits**	**Default**	**Description**
DVOA_CRC_SIG_RED (R)	7:0	0x0	CRC signature value for DVO R channel CRC.
DVOA_CRC_SIG_CONTROL (R)	18:16	0x0	CRC signature value for DVO control CRC.

DVOA DATA and Control CRC Results

DVOA_CRC2_SIG_MASK - RW - 32 bits - DISPDEC:0x79AC			
Field Name	**Bits**	**Default**	**Description**
DVOA_CRC2_SIG_MASK	26:0	0x7ffffff	Mask bits for DVO output CRC2 Bit 26: Vsync signal Bit 25: Hsync Signal Bit 24: Data Enable Bit 23-0:DVO Data

Control for secondary DVO CRC

DVOA_CRC2_SIG_RESULT - RW - 32 bits - DISPDEC:0x79B0			
Field Name	**Bits**	**Default**	**Description**
DVOA_CRC2_SIG_RESULT (R)	26:0	0x0	CRC2 signature value for DVO output

CRC2 signature value for DVO output

DVOA_STRENGTH_CONTROL - RW - 32 bits - DISPDEC:0x79B4

Field Name	Bits	Default	Description
DVOA_SP	3:0	0x0	Strength of pull-up section of output buffer for DVO signals.
DVOA_SN	7:4	0x6	Strength of pull-down section of output buffer for DVO signals.
DVOACLK_SP	11:8	0x0	Strength of pull-up section of output buffer for DVO clock output.
DVOACLK_SN	15:12	0x6	Strength of pull-down section of output buffer for DVO clock output.
DVOA_SRP	16	0x1	Increases slew rate to pull-up section of output buffer for DVO signals.
DVOA_SRN	17	0x1	Increases slew rate to pull-down section of output buffer for DVO signals.
DVOACLK_SRP	24	0x1	Increases slew rate to pull-up section of output buffer for DVO clock.
DVOACLK_SRN	25	0x1	Increases slew rate to pull-down section of output buffer for DVO clock.
DVOA_LSB_VMODE	28	0x1	Select pad output voltage for DVODATA[11:0], DVOCNTL and DVOCLK 0: 1.8V 1: 3.3V
DVOA_MSB_VMODE	29	0x1	Select pad output voltage for DVODATA[23:12] 0: 1.8V 1: 3.3V

DVOA_FORCE_OUTPUT_CNTL - RW - 32 bits - DISPDEC:0x79B8			
Field Name	**Bits**	**Default**	**Description**
DVOA_FORCE_DATA_EN	0	0x0	Enable force option on DVOA 0=Disable 1=Enable
DVOA_FORCE_DATA_SEL	10:8	0x0	Select which DVOA channels have data forced0=Don't Force, 1=Force Bit 0: Blue channel Bit 1: Green channel Bit 2: Red channel
DVOA_FORCE_DATA_ON_BLANKb_ONLY	16	0x0	Data is forced only during active region. 0=Disable 1=Enable

DVOA Force Data control register

DVOA_FORCE_DATA - RW - 32 bits - DISPDEC:0x79BC			
Field Name	**Bits**	**Default**	**Description**
DVOA_FORCE_DATA	7:0	0x0	Data to be forced on R, G & B channels

Data to be forced on R, G & B channels

DC_HOT_PLUG_DETECT1_CONTROL - RW - 32 bits - DISPDEC:0x7D00			
Field Name	**Bits**	**Default**	**Description**
DC_HOT_PLUG_DETECT1_EN	0	0x0	Enable 1st HPD circuit When disabled, HPD interrupts will not happen and DC_HOT_PLUG_DETECT1_SENSE will not change 0=Disable 1=Enable

DC_HOT_PLUG_DETECT1_INT_STATUS - RW - 32 bits - DISPDEC:0x7D04

Field Name	Bits	Default	Description
DC_HOT_PLUG_DETECT1_INT_STATUS (R)	0	0x0	Interrupt generated by 1st HPD circuit - connect or disconnect has taken place
DC_HOT_PLUG_DETECT1_SENSE (R)	1	0x0	Connection status of panel being monitored by the 1st HPD circuit 0=nothing connected to HPD1 1=panel connected to HPD1

DC_HOT_PLUG_DETECT1_INT_CONTROL - RW - 32 bits - DISPDEC:0x7D08			
Field Name	**Bits**	**Default**	**Description**
DC_HOT_PLUG_DETECT1_INT_ACK (W)	0	0x0	Interrupt acknowledge for the 1st HPD circuit
DC_HOT_PLUG_DETECT1_INT_POLARITY	8	0x0	Polarity of 1st HPD circuit 0=generate interrupt on disconnect 1=generate interrupt on connect
DC_HOT_PLUG_DETECT1_INT_EN	16	0x0	Enable Interrupts on the 1st HPD circuit 0=Disable 1=Enable

DC_HOT_PLUG_DETECT2_CONTROL - RW - 32 bits - DISPDEC:0x7D10			
Field Name	**Bits**	**Default**	**Description**
DC_HOT_PLUG_DETECT2_EN	0	0x0	Enable 2nd HPD circuit When disabled, HPD interrupts will not happen and DC_HOT_PLUG_DETECT2_SENSE will not change 0=Disable 1=Enable

DC_HOT_PLUG_DETECT2_INT_STATUS - RW - 32 bits - DISPDEC:0x7D14			
Field Name	**Bits**	**Default**	**Description**
DC_HOT_PLUG_DETECT2_INT_STATUS (R)	0	0x0	Interrupt generated by 2nd HPD circuit - connect or disconnect has taken place
DC_HOT_PLUG_DETECT2_SENSE (R)	1	0x0	Connection status of panel being monitored by the 2nd HPD circuit 0=nothing connected to HPD2 1=panel connected to HPD2

DC_HOT_PLUG_DETECT2_INT_CONTROL - RW - 32 bits - DISPDEC:0x7D18			
Field Name	**Bits**	**Default**	**Description**
DC_HOT_PLUG_DETECT2_INT_ACK (W)	0	0x0	Interrupt acknowledge for the 2nd HPD circuit
DC_HOT_PLUG_DETECT2_INT_POLARITY	8	0x0	Polarity of 2nd HPD circuit. 0=generate interrupt on disconnect 1=generate interrupt on connect
DC_HOT_PLUG_DETECT2_INT_EN	16	0x0	Enable Interrupts on the 2nd HPD circuit 0=Disable 1=Enable

DC_HOT_PLUG_DETECT_CLOCK_CONTROL - RW - 32 bits - DISPDEC:0x7D20			
Field Name	**Bits**	**Default**	**Description**
DC_HOT_PLUG_DETECT_CLOCK_ENABLE	0	0x1	Enable HPD clock 0=Disable 1=Enable
DC_HOT_PLUG_DETECT_CLOCK_SEL	17:16	0x0	Select HPD reference frequency 0=1/8192 of crystal clock 1=1/512 of crystal clock 2=1/32 of crystal clock 3=1/2 of crystal clock

DC_I2C_STATUS1 - RW - 32 bits - DISPDEC:0x7D30			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_DONE	0	0x0	DVI_I2C busy/transfer complete 0=I2c is busy 1=transfer is complete
DC_I2C_NACK	1	0x0	I2C slave did not issue acknowledge 1=Slave did not issue acknowledge
DC_I2C_HALT	2	0x0	Timeout condition. Transfer is halted 1=Time-out condition, transfer is halted
DC_I2C_GO	3	0x0	Write 1 to start I2C transfer

DC_I2C_RESET - RW - 32 bits - DISPDEC:0x7D34			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_SOFT_RESET	0	0x0	Reset I2C controller 0=Normal 1=Resets i2c controller
DC_I2C_ABORT	8	0x0	Write 1 to abort I2C transfer 0=No abort 1=Abort

DC_I2C_CONTROL1 - RW - 32 bits - DISPDEC:0x7D38			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_START	0	0x0	Control whether a START is sent at the start of the transfer 0=No start 1=Start
DC_I2C_STOP	1	0x0	Control whether a STOP is sent at the end of the transfer 0=No stop 1=Stop
DC_I2C_RECEIVE	2	0x0	Select whether master will send or receive data 0=Send 1=Receive
DC_I2C_EN	8	0x0	I2C pads drive SDA when 1
DC_I2C_PIN_SELECT	17:16	0x0	Select DDC pins to be used by DOUT I2C master 0=DOUT I2C Master uses DDC1_DATA and DDC1_CLK pins 1=DOUT I2C Master uses DDC2_DATA and DDC2_CLK pins 2=DOUT I2C Master uses DDC3_DATA and DDC3_CLK pins 3=Reserved

DC_I2C_CONTROL2 - RW - 32 bits - DISPDEC:0x7D3C			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_ADDR_COUNT	2:0	0x0	Number of address bytes
DC_I2C_DATA_COUNT	11:8	0x0	Number of data bytes
DC_I2C_PRESCALE_LOWER	23:16	0x0	Divider to create TOCLK from SCLK
DC_I2C_PRESCALE_UPPER	31:24	0x0	Divider to create QSCL (4x SCL) from TOCLK

DC_I2C_CONTROL3 - RW - 32 bits - DISPDEC:0x7D40			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_DATA_DRIVE_EN	0	0x0	0:Pullup by external resistor 1:I2C pads drive SDA high 0=Pullup by external resistor 1=I2C pads drive SDA
DC_I2C_DATA_DRIVE_SEL	1	0x0	0:Drive for 10 MCLKs 1:Drive for 20 MCLKs 0=Drive for 10MCLKs 1=20MCLKS
DC_I2C_CLK_DRIVE_EN	7	0x0	0:Pullup by external resistor 1:I2C pads drive SCL high 0=Pullup by external resistor 1=I2C pads drive SCL
DC_I2C_RD_INTRA_BYTE_DELAY	15:8	0x0	Delay (in QSCL pulses) between bytes during reads
DC_I2C_WR_INTRA_BYTE_DELAY	23:16	0x0	Delay (in QSCL pulses) between bytes during writes
DC_I2C_TIME_LIMIT	31:24	0x0	Use to set upper limit before state machine will time out and terminate transfer. Time limit is 256 * this field, in units of 'TOCLK'.

DC_I2C_DATA - RW - 32 bits - DISPDEC:0x7D44			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_DATA	7:0	0x0	I2C buffer read/write data

DC_I2C_INTERRUPT_CONTROL - RW - 32 bits - DISPDEC:0x7D48			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_INTERRUPT_STATUS (R)	0	0x0	DC I2C interrupt status
DC_I2C_INTERRUPT_AK (W)	8	0x0	Acknowledge DC_I2C_COUNT_REACHED
DC_I2C_INTERRUPT_ENABLE	16	0x0	Enable interrupt

DC_I2C_ARBITRATION - RW - 32 bits - DISPDEC:0x7D50			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_SW_WANTS_TO_USE_I2C (W)	0	0x0	Asserted when HOST wants to use DOUT I2C 0=No effect 1=SW requests to use DOUT I2C interface

DC_I2C_SW_CAN_USE_I2C (R)	1	0x0	Asserted when HOST can use I2C (i.e. HDCP is not using DOUT I2C) 0=DOUT I2C interface is not available to be used if HDCP is enabled 1=SW has control of the DOUT I2C interface
DC_I2C_SW_DONE_USING_I2C (W)	8	0x0	Indicates that HOST is done using DUT I2C 0=Has no effect. If SW has control of DOUT I2C, free to use it 1=Indicates that SW is done using DOUT I2C i/f and that control of DOUT I2C is freed up
DC_I2C_HW_NEEDS_I2C (R)	9	0x0	HDCP requests use of DOUT I2C interface 0=no request by H/W for use of DOUT I2C 1=H/W HDCP requests use of the DOUT I2C i/f. SW should try to complete the current I2C operation as soon as possible and return control of the DOUT I2C to H/W by writing DC_I2C_SW_DONE_USING_I2C to 1 when it is safe to do so.
DC_I2C_ABORT_HDCP_I2C (W)	16	0x0	Abort current HDCP use of I2C interface 0=normal operation of H/W using DOUT I2C 1=abort current H/W HDCP use of DOUT I2C interface. Force hardware to give up control of the DOUT I2C i/f.
DC_I2C_HW_USING_I2C (R)	17	0x0	HDCP currently using DOUT I2C interface 0=DOUT I2C i/f not in use by HDCP hardware 1=HDCP hardware currently using DOUT I2C interface.

DC_GENERICA - RW - 32 bits - DISPDEC:0x7DC0			
Field Name	**Bits**	**Default**	**Description**
GENERICA_EN	0	0x0	Enable signal for GENERICA pad
GENERICA_SEL	11:8	0x0	Select signals for GENERICA pad 0=DACA Stereosync 1=DACB Stereosync 2=DACA Pixclk 3=DACB Pixclk 4=DVOA CTL3 5=P1 PLLCLK 6=P2 PLLCLK 7=DVOA Stereosync 8=DACA Field Number 9=DACB Field Number 10=GENERICA test debug clock from DCCG 11=SYNCEN 12=GENERICA test debug clock from SCG 13=Reserved 14=Reserved 15=Reserved

DC_GENERICB - RW - 32 bits - DISPDEC:0x7DC4			
Field Name	**Bits**	**Default**	**Description**
GENERICB_EN	0	0x0	Enable signals for GENERICB pad

GENERICB_SEL	11:8	0x0	Select signal for GENERICB pad 0=DACA Stereosync 1=DACB Stereosync 2=DACA PIXCLK 3=DACB PIXCLK 4=DVOA CTL3 5=P1 PLLCLK 6=P2 PLLCLK 7=DVOA Stereosync 8=DACA Field Number 9=DACB Field Number 10=GENERICB test debug clock from DCCG 11=SYNCEN 12=GENERICA test debug clock from SCG 13=Reserved 14=Reserved 15=Reserved

DC_PAD_EXTERN_SIG - RW - 32 bits - DISPDEC:0x7DCC			
Field Name	**Bits**	**Default**	**Description**
DC_PAD_EXTERN_SIG_SEL	3:0	0x0	Select pin PAD_EXTERN_SIGNAL is connected to 0=PAD_EXTERN_SIGNAL is connected to HSYNCA pin 1=PAD_EXTERN_SIGNAL is connected to VSYNCA pin 2=PAD_EXTERN_SIGNAL is connected to HSYNCB pin 3=PAD_EXTERN_SIGNAL is connected to VSYNCB pin 4=PAD_EXTERN_SIGNAL is connected to GENERICA pin 5=PAD_EXTERN_SIGNAL is connected to GENERICB pin 6=PAD_EXTERN_SIGNAL is connected to GENERICC pin 7=PAD_EXTERN_SIGNAL is connected to HPD1 pin 8=PAD_EXTERN_SIGNAL is connected to HPD2 pin 9=PAD_EXTERN_SIGNAL is connected to DDC1CLK pin 10=PAD_EXTERN_SIGNAL is connected to DDC1DATA pin 11=PAD_EXTERN_SIGNAL is connected to DDC2CLK pin 12=PAD_EXTERN_SIGNAL is connected to DDC2DATA pin 13=PAD_EXTERN_SIGNAL is connected to VHAD(0) pin 14=PAD_EXTERN_SIGNAL is connected to VHAD(1) pin 15=PAD_EXTERN_SIGNAL is connected to VPHCTL pin

Select for PAD_EXTERN_SIGNAL

DC_REF_CLK_CNTL - RW - 32 bits - DISPDEC:0x7DD4			
Field Name	**Bits**	**Default**	**Description**
HSYNCA_OUTPUT_SEL	1:0	0x0	0=Reference Clock Output disabled 1=PPLL1 Reference Clock Output 2=PPLL2 Reference Clock Output 3=Reserved
HSYNCB_OUTPUT_SEL	9:8	0x0	0=Reference Clock Output disabled 1=PPLL1 Reference Clock Output 2=PPLL2 Reference Clock Output 3=Reserved

Control output of external reference clocks

DC_GPIO_GENERIC_MASK - RW - 32 bits - DISPDEC:0x7DE0			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_GENERICA_MASK	0	0x0	0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.
DC_GPIO_GENERICB_MASK	8	0x0	0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.
DC_GPIO_GENERICC_MASK	16	0x0	0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.

Control GPIO functionality of GENERIC pads - active high.

DC_GPIO_GENERIC_A - RW - 32 bits - DISPDEC:0x7DE4			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_GENERICA_A	0	0x0	Asynchronous input for GENERICA pad when DC_GPIO_GENERICA_MASK = 1.
DC_GPIO_GENERICB_A	8	0x0	Asynchronous input for GENERICB pad when DC_GPIO_GENERICB_MASK = 1.
DC_GPIO_GENERICC_A	16	0x0	Asynchronous input for GENERICC pad when DC_GPIO_GENERICC_MASK = 1.

Asynchronous inputs for GENERIC pads when GPIO functionality enabled by DC_GPIO_GENERIC_MASK register.

DC_GPIO_GENERIC_EN - RW - 32 bits - DISPDEC:0x7DE8			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_GENERICA_EN	0	0x0	Output enable used for GENERICA when DC_GPIO_GENERICA_MASK = 1.
DC_GPIO_GENERICB_EN	8	0x0	Output enable used for GENERICB when DC_GPIO_GENERICB_MASK = 1.
DC_GPIO_GENERICC_EN	16	0x0	Output enable used for GENERICC when DC_GPIO_GENERICC_MASK = 1.

Output enable for GENERIC pads when GPIO functionality enabled by DC_GPIO_GENERIC_MASK register.

DC_GPIO_GENERIC_Y - RW - 32 bits - DISPDEC:0x7DEC			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_GENERICA_Y (R)	0	0x0	Value on GENERICA pad.
DC_GPIO_GENERICB_Y (R)	8	0x0	Value on GENERICB pad.
DC_GPIO_GENERICC_Y (R)	16	0x0	Value on GENERICC pad.

Output values of GENERIC pads.

DC_GPIO_VIP_DEBUG - RW - 32 bits - DISPDEC:0x7E2C			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_VIP_DEBUG	0	0x0	Control whether display or VIP controls DVODATA[23:16] and DVOCNTL[2] 0: VIP / test/debug bus control pads 1: display controls pads

DC_GPIO_MACRO_DEBUG	9:8	0x0	Mux TMDS or LVDS debug output data onto DVODATA[15:6] 0=Normal 1=Reserved 2=TMDSA debug output on dvo[15:6] 3=LVDS debug output on dvo[15:6]

Mux control to allow VIP and DCO Debug to share DVO Pads.

DC_GPIO_DVODATA_MASK - RW - 32 bits - DISPDEC:0x7E30			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DVODATA_MASK	23:0	0x0	Enable/Disable GPIO functionality on DVODATA pads. Bits can be set individually.
DC_GPIO_DVOCNTL_MASK	26:24	0x0	Enable/Disable GPIO functionality on DVOCNTL pads. Bits can be set individually.
DC_GPIO_DVOCLK_MASK	28	0x0	Enable/Disable GPIO functionality on DVOCLK pads. Bits can be set individually.

Control GPIO functionality of the DVO pads - all fields are active high.

DC_GPIO_DVODATA_A - RW - 32 bits - DISPDEC:0x7E34			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DVODATA_A	23:0	0x0	Asynchronous inputs for DVODATA pads when associated DC_GPIO_DVODATA_MASK = 1.
DC_GPIO_DVOCNTL_A	26:24	0x0	Asynchronous inputs for DVOCNTL pads when associated DC_GPIO_DVOCNTL_MASK = 1.
DC_GPIO_DVOCLK_A	28	0x0	Asynchronous inputs for DVOCLK pads when associated DC_GPIO_DVOCLK_MASK = 1.

Asynchronous inputs for the DVO pads when the GPIO functionality is enabled by the DC_GPIO_DVODATA_MASK register.

DC_GPIO_DVODATA_EN - RW - 32 bits - DISPDEC:0x7E38			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DVODATA_EN	23:0	0x0	Output enables for DVODATA pads when associated DC_GPIO_DVODATA_MASK = 1.
DC_GPIO_DVOCNTL_EN	26:24	0x0	Output enables for DVOCNTL pads when associated DC_GPIO_DVOCNTL_MASK = 1.
DC_GPIO_DVOCLK_EN	28	0x0	Output enables for DVOCLK pads when associated DC_GPIO_DVOCLK_MASK = 1.

Output enable values for the DVO pads when the GPIO functionality is enabled by the DC_GPIO_DVODATA_MASK register.

DC_GPIO_DVODATA_Y - RW - 32 bits - DISPDEC:0x7E3C			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DVODATA_Y (R)	23:0	0x0	Values on DVODATA pads.
DC_GPIO_DVOCNTL_Y (R)	26:24	0x0	Values on DVOCNTL pads.
DC_GPIO_DVOCLK_Y (R)	28	0x0	Values on DVOCLK pads.

Output values of the DVO pads.

DC_GPIO_DDC1_MASK - RW - 32 bits - DISPDEC:0x7E40			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DDC1CLK_MASK	0	0x0	Enable/Disable GPIO functionality on DDC1CLK pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.
DC_GPIO_DDC1DATA_MASK	8	0x0	Enable/Disable GPIO functionality on DDC1DATA pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.

Control GPIO functionality of the DDC1 pads - all fields are active high.

DC_GPIO_DDC1_A - RW - 32 bits - DISPDEC:0x7E44			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DDC1CLK_A	0	0x0	Asynchronous input for DDC1CLK when DC_GPIO_DDC1CLK_MASK = 1.
DC_GPIO_DDC1DATA_A	8	0x0	Asynchronous input for DDC1DATA when DC_GPIO_DDC1DATA_MASK = 1.

Asynchronous inputs for the DDC1 pads when the GPIO functionality is enabled by the DC_GPIO_DDC1_MASK register.

DC_GPIO_DDC1_EN - RW - 32 bits - DISPDEC:0x7E48			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DDC1CLK_EN	0	0x0	Output enable for DDC1CLK when DC_GPIO_DDC1CLK_MASK = 1.
DC_GPIO_DDC1DATA_EN	8	0x0	Output enable for DDC1DATA when DC_GPIO_DDC1DATA_MASK = 1.

Output enable values for the DDC1 pads when the GPIO functionality is enabled by the DC_GPIO_DDC1_MASK register.

DC_GPIO_DDC1_Y - RW - 32 bits - DISPDEC:0x7E4C			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DDC1CLK_Y (R)	0	0x0	Value on DDC1CLK pad.
DC_GPIO_DDC1DATA_Y (R)	8	0x0	Value on DDC1DATA pad.

Output values of the DDC1 pads.

DC_GPIO_DDC2_MASK - RW - 32 bits - DISPDEC:0x7E50			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DDC2CLK_MASK	0	0x0	Enable/Disable GPIO functionality on DDC2CLK pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.
DC_GPIO_DDC2DATA_MASK	8	0x0	Enable/Disable GPIO functionality on DDC2DATA pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.

Control GPIO functionality of the DDC2 pads - all fields are active high.

DC_GPIO_DDC2_A - RW - 32 bits - DISPDEC:0x7E54

Field Name	Bits	Default	Description
DC_GPIO_DDC2CLK_A	0	0x0	Asynchronous input for DDC2CLK when DC_GPIO_DDC2CLK_MASK = 1.
DC_GPIO_DDC2DATA_A	8	0x0	Asynchronous input for DDC2DATA when DC_GPIO_DDC2DATA_MASK = 1.

Asynchronous inputs for the DDC2 pads when the GPIO functionality is enabled by the DC_GPIO_DDC2_MASK register.

DC_GPIO_DDC2_EN - RW - 32 bits - DISPDEC:0x7E58			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DDC2CLK_EN	0	0x0	Output enable for DDC2CLK when DC_GPIO_DDC2CLK_MASK = 1.
DC_GPIO_DDC2DATA_EN	8	0x0	Output enable for DDC2DATA when DC_GPIO_DDC2DATA_MASK = 1.

Output enable values for the DDC2 pads when the GPIO functionality is enabled by the DC_GPIO_DDC2_MASK register.

DC_GPIO_DDC2_Y - RW - 32 bits - DISPDEC:0x7E5C			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DDC2CLK_Y (R)	0	0x0	Value on DDC2CLK pad.
DC_GPIO_DDC2DATA_Y (R)	8	0x0	Value on DDC2DATA pad.

Output values of the DDC2 pads.

DC_GPIO_DDC3_MASK - RW - 32 bits - DISPDEC:0x7E60			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DDC3CLK_MASK	0	0x0	Enable/Disable GPIO functionality on DDC3CLK pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.
DC_GPIO_DDC3DATA_MASK	8	0x0	Enable/Disable GPIO functionality on DDC3DATA pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.

Control GPIO functionality of the DDC3 pads - all fields are active high.

DC_GPIO_DDC3_A - RW - 32 bits - DISPDEC:0x7E64			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DDC3CLK_A	0	0x0	Asynchronous input for DDC3CLK when DC_GPIO_DDC3CLK_MASK = 1.
DC_GPIO_DDC3DATA_A	8	0x0	Asynchronous input for DDC3DATA when DC_GPIO_DDC3DATA_MASK = 1.

Asynchronous inputs for the DDC3 pads when the GPIO functionality is enabled by the DC_GPIO_DDC3_MASK register.

DC_GPIO_DDC3_EN - RW - 32 bits - DISPDEC:0x7E68			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DDC3CLK_EN	0	0x0	Output enable for DDC3CLK when DC_GPIO_DDC3CLK_MASK = 1.
DC_GPIO_DDC3DATA_EN	8	0x0	Output enable for DDC3DATA when DC_GPIO_DDC3DATA_MASK = 1.

Output enable values for the DDC3 pads when the GPIO functionality is enabled by the DC_GPIO_DDC3_MASK register.

DC_GPIO_DDC3_Y - RW - 32 bits - DISPDEC:0x7E6C			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_DDC3CLK_Y (R)	0	0x0	Value on DDC3CLK pad.
DC_GPIO_DDC3DATA_Y (R)	8	0x0	Value on DDC3DATA pad.

Output values for the DDC3 pads.

DC_GPIO_SYNCA_MASK - RW - 32 bits - DISPDEC:0x7E70			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_HSYNCA_MASK	0	0x0	Enable/Disable GPIO functionality on HSYNCA pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.
DC_GPIO_VSYNCA_MASK	8	0x0	Enable/Disable GPIO functionality on VSYNCA pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.

Control GPIO functionality of the HSYNCA & VSYNCA pads - all fields are active high.

DC_GPIO_SYNCA_A - RW - 32 bits - DISPDEC:0x7E74			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_HSYNCA_A	0	0x0	Asynchronous input for HSYNCA when DC_GPIO_HSYNCA_MASK = 1.
DC_GPIO_VSYNCA_A	8	0x0	Asynchronous input for VSYNCA when DC_GPIO_VSYNCA_MASK = 1.

Asynchronous inputs for the HSYNCA & VSYNCA pads when the GPIO functionality is enabled by the DC_GPIO_SYNCA_MASK register.

DC_GPIO_SYNCA_EN - RW - 32 bits - DISPDEC:0x7E78			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_HSYNCA_EN	0	0x0	Output enable for HSYNCA when DC_GPIO_HSYNCA_MASK = 1.
DC_GPIO_VSYNCA_EN	8	0x0	Output enable for VSYNCA when DC_GPIO_VSYNCA_MASK = 1.

Output enable values for the HSYNCA & VSYNCA pads when the GPIO functionality is enabled by the DC_GPIO_SYNCA_MASK register.

DC_GPIO_SYNCA_Y - RW - 32 bits - DISPDEC:0x7E7C			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_HSYNCA_Y (R)	0	0x0	Value on HSYNCA pad.
DC_GPIO_VSYNCA_Y (R)	8	0x0	Value on VSYNCA pad.
Output values of the HSYNCA & VSYNCA pads.			

DC_GPIO_SYNCB_MASK - RW - 32 bits - DISPDEC:0x7E80			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_HSYNCB_MASK	0	0x0	Enable/Disable GPIO functionality on HSYNCB pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.
DC_GPIO_VSYNCB_MASK	8	0x0	Enable/Disable GPIO functionality on VSYNCB pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.
Control GPIO functionality of the HSYNCB & VSYNCB pads - all fields are active high.			

DC_GPIO_SYNCB_A - RW - 32 bits - DISPDEC:0x7E84			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_HSYNCB_A	0	0x0	Asynchronous input for HSYNCB when DC_GPIO_HSYNCB_MASK = 1.
DC_GPIO_VSYNCB_A	8	0x0	Asynchronous input for VSYNCB when DC_GPIO_VSYNCB_MASK = 1.
Asynchronous inputs for the HSYNCB & VSYNCB pads when the GPIO functionality is enabled by the DC_GPIO_SYNCB_MASK register.			

DC_GPIO_SYNCB_EN - RW - 32 bits - DISPDEC:0x7E88			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_HSYNCB_EN	0	0x0	Output enable for HSYNCB when DC_GPIO_HSYNCB_MASK = 1.
DC_GPIO_VSYNCB_EN	8	0x0	Output enable for VSYNCB when DC_GPIO_VSYNCB_MASK = 1.
Output enable values for the HSYNCB & VSYNCB pads when the GPIO functionality is enabled by the DC_GPIO_SYNCB_MASK register.			

DC_GPIO_SYNCB_Y - RW - 32 bits - DISPDEC:0x7E8C			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_HSYNCB_Y (R)	0	0x0	Value on HSYNCB pad.
DC_GPIO_VSYNCB_Y (R)	8	0x0	Value on VSYNCB pad.
Output values of the HSYNCB & VSYNCB pads.			

DC_GPIO_HPD_MASK - RW - 32 bits - DISPDEC:0x7E90			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_HPD1_MASK	0	0x0	Enable/Disable GPIO functionality on HPD1 pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.

DC_GPIO_HPD2_MASK	8	0x0	Enable/Disable GPIO functionality on HPD2 pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.

Control GPIO functionality of the Hot Plug Detect pads - all fields are active high.

DC_GPIO_HPD_A - RW - 32 bits - DISPDEC:0x7E94			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_HPD1_A	0	0x0	Asynchronous input for HPD1 when DC_GPIO_HPD1_MASK = 1.
DC_GPIO_HPD2_A	8	0x0	Asynchronous input for HPD2 when DC_GPIO_HPD2_MASK = 1.

Asynchronous inputs for the HPD pads when the GPIO functionality is enabled by the DC_GPIO_HPD_MASK register.

DC_GPIO_HPD_EN - RW - 32 bits - DISPDEC:0x7E98			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_HPD1_EN	0	0x0	Output enable for HPD1 when DC_GPIO_HPD1_MASK = 1.
DC_GPIO_HPD2_EN	8	0x0	Output enable for HPD2 when DC_GPIO_HPD2_MASK = 1.

Output enable values for the HPD pads when the GPIO functionality is enabled by the DC_GPIO_HPD_MASK register.

DC_GPIO_HPD_Y - RW - 32 bits - DISPDEC:0x7E9C			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_HPD1_Y (R)	0	0x0	Value on HPD1 pad.
DC_GPIO_HPD2_Y (R)	8	0x0	Value on HPD2 pad.

Output values of the HPD pads.

DC_GPIO_PWRSEQ_MASK - RW - 32 bits - DISPDEC:0x7EA0			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_BLON_MASK	0	0x0	Enable/Disable GPIO functionality on BLON pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.
DC_GPIO_DIGON_MASK	8	0x0	Enable/Disable GPIO functionality on DIGON pad 0=Pad Driven by Hardware - Normal Operation 1=Pad Controlled by Software through associated GPIO registers. Pad values generated by hardware are overridden.

Control GPIO functionality of the BLON & DIGON pads - all fields are active high.

DC_GPIO_PWRSEQ_A - RW - 32 bits - DISPDEC:0x7EA4			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_BLON_A	0	0x0	Asynchronous input for BLON when DC_GPIO_BLON_MASK = 1.
DC_GPIO_DIGON_A	8	0x0	Asynchronous input for BIGON when DC_GPIO_DIGON_MASK = 1.

Asynchronous inputs for the BLON & DIGON pads when the GPIO functionality is enabled by the DC_GPIO_PWRSEQ_MASK register.

DC_GPIO_PWRSEQ_EN - RW - 32 bits - DISPDEC:0x7EA8			
Field Name	**Bits**	**Default**	**Description**

DC_GPIO_BLON_EN	0	0x0	Output enable for BLON when DC_GPIO_BLON_MASK = 1.
DC_GPIO_DIGON_EN	8	0x0	Output enable for DIGON when DC_GPIO_DIGON_MASK = 1.

Output enable values for the BLON & DIGON pads when the GPIO functionality is enabled by the DC_GPIO_PWRSEQ_MASK register.

DC_GPIO_PWRSEQ_Y - RW - 32 bits - DISPDEC:0x7EAC			
Field Name	**Bits**	**Default**	**Description**
DC_GPIO_BLON_Y (R)	0	0x0	Value on BLON pad.
DC_GPIO_DIGON_Y (R)	8	0x0	Value on DIGON pad.

Output values of the BLON & DIGON pads.

CAPTURE_START_STATUS - RW - 32 bits - DISPDEC:0x7ED0			
Field Name	**Bits**	**Default**	**Description**
DACA_CAPTURE_START (R)	0	0x0	Extended DACA Capture Start that is used for test & debug purposes. This Capture Start is de-asserted by DACA_CAPTURE_START_AK. 0=No event 1=Capture_start has occurred
DACB_CAPTURE_START (R)	1	0x0	Extended DACB Capture Start that is used for test & debug purposes. This Capture Start is de-asserted by DACB_CAPTURE_START_AK. 0=No event 1=Capture_start has occurred
TMDSA_CAPTURE_START (R)	2	0x0	Extended TMDSA Capture Start that is used for test & debug purposes. This Capture Start is de-asserted by TMDSA_CAPTURE_START_AK. 0=No event 1=Capture_start has occurred
LVTMA_CAPTURE_START (R)	3	0x0	00 - No event 01 - Capture_start has occurred
DVOA_CAPTURE_START (R)	4	0x0	Extended DVOA Capture Start that is used for test & debug purposes. This Capture Start is de-asserted by DVOA_CAPTURE_START_AK. 0=No event 1=Capture_start has occurred
DACA_CAPTURE_START_AK (W)	5	0x0	Acknowledge bit for DACA Capture Start. This bit will clear DACA_CAPTURE_START and DISP_INTERRUPT_STATUS.DACA_CAPTURE_START_INTERRUPT. 0=No effect 1=Clear Capture_start
DACB_CAPTURE_START_AK (W)	6	0x0	Acknowledge bit for DACB Capture Start. This bit will clear DACB_CAPTURE_START and DISP_INTERRUPT_STATUS.DACB_CAPTURE_START_INTERRUPT. 0=No effect 1=Clear Capture_start
TMDSA_CAPTURE_START_AK (W)	7	0x0	Acknowledge bit for TMDSA Capture Start. This bit will clear TMDSA_CAPTURE_START and DISP_INTERRUPT_STATUS.TMDSA_CAPTURE_START_INTERRUPT. 0=No effect 1=Clear Capture_start
LVTMA_CAPTURE_START_AK (W)	8	0x0	00 - No effect 01 - Clear Capture_start
DVOA_CAPTURE_START_AK (W)	9	0x0	Acknowledge bit for DVOA Capture Start. This bit will clear DVOA_CAPTURE_START and DISP_INTERRUPT_STATUS.DVOA_CAPTURE_START_INTERRUPT. 0=No effect 1=Clear Capture_start

DACA_CAPTURE_START_INT_EN	10	0x0	Enable interrupts on DACA Capture Start. Interrupt can be monitored by polling DISP_INTERRUPT_STATUS.DACA_CAPTURE_START_INTERRUPT. 0=Disable 1=Enable
DACB_CAPTURE_START_INT_EN	11	0x0	Enable interrupts on DACB Capture Start. Interrupt can be monitored by polling DISP_INTERRUPT_STATUS.DACB_CAPTURE_START_INTERRUPT. 0=Disable 1=Enable
TMDSA_CAPTURE_START_INT_EN	12	0x0	Enable interrupts on TMDSA Capture Start. Interrupt can be monitored by polling DISP_INTERRUPT_STATUS.TMDSA_CAPTURE_START_INTERRUPT. 0=Disable 1=Enable
LVTMA_CAPTURE_START_INT_EN	13	0x0	00 - Disable 01 - Enable
DVOA_CAPTURE_START_INT_EN	14	0x0	Enable interrupts on DVOA Capture Start. Interrupt can be monitored by polling DISP_INTERRUPT_STATUS.DVOA_CAPTURE_START_INTERRUPT. 0=Disable 1=Enable
DACA_CAPTURE_START_STATUS (R)	15	0x0	Capture Start used by DACA.
DACB_CAPTURE_START_STATUS (R)	16	0x0	Capture Start used by DACB.
TMDSA_CAPTURE_START_STATUS (R)	17	0x0	Capture Start used by TMDSA.
LVTMA_CAPTURE_START_STATUS (R)	18	0x0	Capture Start used by LVTMA.
DVOA_CAPTURE_START_STATUS (R)	19	0x0	Capture Start used by DVOA.

Capture Start Control

DC_GPIO_PAD_STRENGTH_1 - RW - 32 bits - DISPDEC:0x7ED4			
Field Name	**Bits**	**Default**	**Description**
SYNC_STRENGTH_SN	27:24	0x7	Control SN strengths for HSYNCA, HSYNCB, VSYNCA & VSYNCB
SYNC_STRENGTH_SP	31:28	0x4	Control SP strengths for HSYNCA, HSYNCB, VSYNCA & VSYNCB

DC_GPIO_PAD_STRENGTH_2 - RW - 32 bits - DISPDEC:0x7ED8			
Field Name	**Bits**	**Default**	**Description**
STRENGTH_SN	3:0	0x7	Control SN strengths for DDC1, DDC2, DDC3, GENERICA, GENERICB, GENERICC, HPD1 & HPD2 pads
STRENGTH_SP	7:4	0x4	Control SP strengths for DDC1, DDC2, DDC3, GENERICA, GENERICB, GENERICC, HPD1 & HPD2 pads
PWRSEQ_STRENGTH_SN	19:16	0x7	Control SN strengths for BLON & DIGON pads
PWRSEQ_STRENGTH_SP	23:20	0x4	Control SP strengths for BLON & DIGON pads

DISP_INTERRUPT_STATUS - RW - 32 bits - DISPDEC:0x7EDC			
Field Name	**Bits**	**Default**	**Description**

SCL_DISP1_MODE_CHANGE_INTERRUPT (R)	0	0x0	Interrupt that can be generated by the primary display controller's scaler when it detects any change in the scale ratio or number of taps the scaling filter is using. In automatic mode, the scale ratio can change whenever the source size (i.e. viewport) changes or the destination size (i.e. active display of the CRTC output timing).
SCL_DISP2_MODE_CHANGE_INTERRUPT (R)	1	0x0	Interrupt that can be generated by the secondary display controller's scaler when it detects any change in the scale ratio or number of taps the scaling filter is using. In automatic mode, the scale ratio can change whenever the source size (i.e. viewport) changes or the destination size (i.e. active display of the CRTC output timing).
LB_D1_VLINE_INTERRUPT (R)	2	0x0	Interrupt that can be generated by the primary display controller's line buffer logic when the source image line counter falls within a programmed range of line numbers.
LB_D2_VLINE_INTERRUPT (R)	3	0x0	Interrupt that can be generated by the secondary display controller's line buffer logic when the source image line counter falls within a programmed range of line numbers.
LB_D1_VBLANK_INTERRUPT (R)	4	0x0	Interrupt that can be programmed to be generated by the primary display controller's line buffer logic either when the source image line counter is not requesting any active display data (i.e. in the vertical blank) or the output CRTC timing generator is within the vertical blanking region.
LB_D2_VBLANK_INTERRUPT (R)	5	0x0	Interrupt that can be programmed to be generated by the secondary display controller's line buffer logic either when the source image line counter is not requesting any active display data (i.e. in the vertical blank) or the output CRTC timing generator is within the vertical blanking region.
CRTC1_SNAPSHOT_INTERRUPT (R)	6	0x0	Interrupt that can be programmed to be generated by the primary display controller's snapshot logic when either manually forced to trigger by writing a register, or by either a primary CRTC TRIG_A or TRIG_B event occurring.
CRTC1_FORCE_VSYNC_NEXT_LINE_INTERRUPT (R)	7	0x0	Interrupt that can be programmed to be generated by the primary display controller's force VSYNC next line logic when a force VSYNC next line event occurs, caused by either manually writing a register, or by either a primary CRTC TRIG_A or TRIG_B event occurring.
CRTC1_FORCE_COUNT_NOW_INTERRUPT (R)	8	0x0	Interrupt that can be programmed to be generated by the primary display controller's force count now logic when either a primary CRTC TRIG_A or TRIG_B event occur and the horizontal and/or vertical primary CRTC output timing counters reach the H_TOTAL and/or V_TOTAL position selected by the D1CRTC_FORCE_COUNT_NOW_MODE.
CRTC1_TRIGA_INTERRUPT (R)	9	0x0	Interrupt that can be generated by the primary display controller when it detects a primary TRIGA event has occurred.
CRTC1_TRIGB_INTERRUPT (R)	10	0x0	Interrupt that can be generated by the primary display controller when it detects a primary TRIGB event has occurred.
CRTC2_SNAPSHOT_INTERRUPT (R)	11	0x0	Interrupt that can be programmed to be generated by the secondary display controller's snapshot logic when either manually forced to trigger by writing a register, or by either a CRTC TRIG_A or TRIG_B event from the secondary display controller occurring.
CRTC2_FORCE_VSYNC_NEXT_LINE_INTERRUPT (R)	12	0x0	Interrupt that can be programmed to be generated by the secondary display controller's force VSYNC next line logic when a force VSYNC next line event occurs, caused by either manually writing a register, or by either a secondary CRTC TRIG_A or TRIG_B event occurring.
CRTC2_FORCE_COUNT_NOW_INTERRUPT (R)	13	0x0	Interrupt that can be programmed to be generated by the secondary display controller's force count now logic when either a primary CRTC TRIG_A or TRIG_B event occur and the horizontal and/or vertical secondary CRTC output timing counters reach the H_TOTAL and/or V_TOTAL position selected by the D2CRTC_FORCE_COUNT_NOW_MODE.
CRTC2_TRIGA_INTERRUPT (R)	14	0x0	Interrupt that can be generated by the secondary display controller when it detects a secondary TRIGA event has occurred.
CRTC2_TRIGB_INTERRUPT (R)	15	0x0	Interrupt that can be generated by the secondary display controller when it detects a secondary TRIGB event has occurred.

DACA_AUTODETECT_INTERRUPT (R)	16	0x0	Interrupt that can be programmed to be generated when the Autodetect device connected to DACA output detects either a display being first connected or, once connected, first detects the display being disconnected.
DACB_AUTODETECT_INTERRUPT (R)	17	0x0	Interrupt that can be programmed to be generated when the Autodetect device connected to DACA output detects either a display being first connected or, once connected, first detects the display being disconnected.
DC_HOT_PLUG_DETECT1_INTERRUPT (R)	18	0x0	Interrupt that can be programmed to be generated when a Flat Panel (supporting the hot plug feature) is detected to be first connected to the HPD1 pin or, once connected, is detected to have disconnected from the HPD1 pin.
DC_HOT_PLUG_DETECT2_INTERRUPT (R)	19	0x0	Interrupt that can be programmed to be generated when a Flat Panel (supporting the hot plug feature) is detected to be first connected to the HPD2 pin or, once connected, is detected to have disconnected from the HPD2 pin.
HDCP_AUTHORIZED_INTERRUPT (R)	20	0x0	Interrupt that can be programmed to be generated when the HDCP hardware either becomes authorized, or, once authorized, loses authentication
DOUT_I2C_INTERRUPT (R)	21	0x0	Interrupt that can be generated when the current I2C read or write operation done by the DISPOUT hardware assisted I2C finishes execution.
DISP_TIMER_INTERRUPT (R)	22	0x0	Interrupt that can be generated when the display Timer Control logic has generated a hardware interrupt.
DACA_CAPTURE_START_INTERRUPT (R)	23	0x0	Interrupt that can be generated each time a start of frame pulse arrives at the DACA output.
DACB_CAPTURE_START_INTERRUPT (R)	24	0x0	Interrupt that can be generated each time a start of frame pulse arrives at the DACB output.
TMDSA_CAPTURE_START_INTERRUPT (R)	25	0x0	Interrupt that can be generated each time a start of frame pulse arrives at the integrated TMDS transmitter output.
LVTMA_CAPTURE_START_INTERRUPT (R)	26	0x0	Interrupt that can be generated each time a start of frame pulse arrives at the integrated LVTM transmitter output.
DVOA_CAPTURE_START_INTERRUPT (R)	27	0x0	Interrupt that can be generated each time a start of frame pulse arrives at the DVOA port.

Status of all display block interrupts

DOUT_POWER_MANAGEMENT_CNTL - RW - 32 bits - DISPDEC:0x7EE0			
Field Name	**Bits**	**Default**	**Description**
PWRDN_WAIT_BUSY_OFF	0	0x0	Control whether power management waits for signal indicating all block busy signals =0 from DCCG during powerdown 0=When in WAIT_BUSY_OFF, don't wait for all busy=0 1=When in WAIT_BUSY_OFF, wait for all busy=0
PWRDN_WAIT_PWRSEQ_OFF	4	0x1	Control whether power management waits for signal indicating power sequencer is off during powerdown 0=When in WAIT_BUSY_OFF, don't wait for pwrseq off 1=When in WAIT_BUSY_OFF, wait pwrseq off
PWRDN_WAIT_PPLL_OFF	8	0x0	Control whether power management waits for DCCG to report pixel PLLs are off during powerdown 0=When in WAIT_PPLL_OFF, proceed to next state 1=When in WAIT_PPLL_OFF, wait for pixel PLL off indicator
PWRUP_WAIT_PPLL_ON	12	0x0	Control whether power management waits for 1 ms to allow pixel PLLs to lock during powerup 0=When in WAIT_PPLL_ON, proceed to next state 1=When in WAIT_PPLL_ON, wait for 1 ms proceeding to next state
PWRUP_WAIT_MEM_INIT_DONE	16	0x1	Control whether power management mem_init_done indicator 0=When in WAIT_MEM_INIT_DONE, proceed to next state 1=When in WAIT_MEM_INIT_DONE, wait for mem_init_done indicator

PM_ASSERT_RESET	20	0x0	Control whether power management asserts DOUT_CRTC_pwr_down_reset on powerdown 0=Don't assert pm_reset when in 'OFF' state 1=Assert pm_reset when in 'OFF' state
PM_PWRDN_PPLL	24	0x0	Control whether power management asserts pixel PLL reset on powerdown 0=Don't reset pixel PLLs when in 'OFF' state 1=Reset pixel PLLs when in 'OFF' state
PM_CURRENT_STATE (R)	30:28	0x0	Current power management state 0=PM_OFF 1=PM_WAIT_PPLL_ON 2=PM_WAIT_MEM_INIT_DONE 3=PM_ON 4=PM_WAIT_BUSY_OFF 5=PM_WAIT_PPLL_OFF 6=Reserved 7=Reserved

DISP_TIMER_CONTROL - RW - 32 bits - DISPDEC:0x7EF0			
Field Name	**Bits**	**Default**	**Description**
DISP_TIMER_INT_COUNT	24:0	0x0	Desired value for Display Timer Counter to count to before generating event that can cause a hardware interrupt to occur. The counter value is decremented each clock pulse of the CG_xtal_ref_sclk signal. CG_xtal_ref_sclk = a one clock wide pulse on core clock (SCLK) that occurs (Crystal Oscillator Frequency (i.e. 27 MHz)) / (CG_RT_CNTL2_DIV) times per second.
DISP_TIMER_INT_ENABLE (W)	25	0x0	0=No effect 1=Start timer interrupt if TIMER_INT_CNT > 0.
DISP_TIMER_INT_RUNNING (R)	26	0x0	0=Timer interrupt counter not running 1=Timer interrupt counter running
DISP_TIMER_INT_MSK	27	0x0	0=Display Countdown Timer cannot generate hardware interrupt. 1=Display Countdown Timer can generate hardware interrupt when count reached.
DISP_TIMER_INT_STAT (R)	28	0x0	Status of the Display Timer Counter logic. When this bit is high, it does not indicate that a hardware interrupt has occurred.
DISP_TIMER_INT_STAT_AK (W)	29	0x0	Write 1 to acknowledge and clear interrupt 0=No effect 1=Interrupt Acknowledged and will be cleared.
DISP_TIMER_INT (R)	30	0x0	When this bit is high, it indicates that the Display Timer Control logic has generated a hardware interrupt. This bit equals the display timer status (DISP_TIMER_INT_STAT) logically 'AND'ed with the display timer interrupt mask (DISP_TIMER_INT_MSK).

Display Countdown Timer capable of generating a hardware interrupt

2.9.1 Display Output Miscellaneous Registers

DO_PERFCOUNTER0_SELECT - RW - 32 bits - DISPDEC:0x7F00			
Field Name	**Bits**	**Default**	**Description**
DO_PERFCOUNTER0_SELECT	7:0	0x0	Mux control to select what first counter will count
DO_PERFCOUNTER0_MODE	17:16	0x0	Select increment mode of first counter: 0: use 5-bit increment 2: use resync'd LSB of increment 3: resync, rising edge detect on LSB of increment

DO_PERFCOUNTER0_HI - RW - 32 bits - DISPDEC:0x7F04			
Field Name	**Bits**	**Default**	**Description**
DO_PERFCOUNTER0_HI (R)	15:0	0x0	Readback of the high order bits of the first performance counter

DO_PERFCOUNTER0_LOW - RW - 32 bits - DISPDEC:0x7F08			
Field Name	**Bits**	**Default**	**Description**
DO_PERFCOUNTER0_LOW (R)	31:0	0x0	Readback of the low order bits of the first performance counter

DO_PERFCOUNTER1_SELECT - RW - 32 bits - DISPDEC:0x7F0C			
Field Name	**Bits**	**Default**	**Description**
DO_PERFCOUNTER1_SELECT	7:0	0x0	Mux control to select what second counter will count
DO_PERFCOUNTER1_MODE	17:16	0x0	Select increment mode of second counter: 0: use 5-bit increment 2: use resync'd LSB of increment 3: resync, rising edge detect on LSB of increment

DO_PERFCOUNTER1_HI - RW - 32 bits - DISPDEC:0x7F10			
Field Name	**Bits**	**Default**	**Description**
DO_PERFCOUNTER1_HI (R)	15:0	0x0	Readback of the high order bits of the second performance counter

DO_PERFCOUNTER1_LOW - RW - 32 bits - DISPDEC:0x7F14			
Field Name	**Bits**	**Default**	**Description**
DO_PERFCOUNTER1_LOW (R)	31:0	0x0	Readback of the low order bits of the second performance counter

DCO_PERFMON_CNTL_R - RW - 32 bits - DISPDEC:0x7F18			
Field Name	**Bits**	**Default**	**Description**

PERFMON_STATE (R)	1:0	0x0	When written, put the counters into some state: 0: disable and reset 1: start counting 2: freeze- stop counting

GEN_INT_STATUS - RW - 32 bits - DISPDEC:0x104			
Field Name	**Bits**	**Default**	**Description**
DISPLAY_INT_STAT (R)	0	0x0	0=No interrupt 1=Display controller interrupt has occurred
VGA_INT_STAT (R)	1	0x0	0=No interrupt 1=VGA interrupt has occurred

General Interrupt Status register.
These fields can be polled and acknowledged even if interrupts are disabled, or the respective fields are masked in the GEN_INT_CNTL register.

2.10 LVDS Registers

LVTMA_CNTL - RW - 32 bits - DISPDEC:0x7A80			
Field Name	**Bits**	**Default**	**Description**
LVTMA_ENABLE	0	0x0	Enable for the reduction/encoding logic 0=Disable 1=Enable
LVTMA_ENABLE_HPD_MASK	4	0x0	0:Disallow 1:Allow override of LVTMA_ENABLE by HPD on disconnect 0=Result from HPD circuit can not override LVTMA_ENABLE_HPD_MASK 1=Result from HPD circuit can override LVTMA_ENABLE_HPD_MASK on disconnect
LVTMA_HPD_SELECT	8	0x0	Select which hot plug detect unit to use for LVTMA. This selection is only relevant if one of the HPD mask bits in this and other registers is enabled. 0=Use HPD1 1=Use HPD2
LVTMA_SYNC_PHASE	12	0x1	Determine whether to reset phase signal on frame pulse 0: don't reset 1: reset
LVTMA_PIXEL_ENCODING	16	0x0	Pixel encoding format 0=RGB 4:4:4 or YCBCR 4:4:4 1=YCbCr 4:2:2
LVTMA_DUAL_LINK_ENABLE	24	0x0	Enable dual-link 0=Disable 1=Enable
LVTMA_SWAP	28	0x0	Swap upper and lower data channels 0=Disable 1=Enable

LVTMA_SOURCE_SELECT - RW - 32 bits - DISPDEC:0x7A84			
Field Name	**Bits**	**Default**	**Description**
LVTMA_SOURCE_SELECT	0	0x0	Select between display stream 1 & display stream 2 0=CRTC1 data is used 1=CRTC2 data is used
LVTMA_SYNC_SELECT	8	0x0	Select between SYNCA and SYNCB signals 0=HSYNC_A & VSYNC_A from the selected CRTC are used 1=HSYNC_B & VSYNC_B from the selected CRTC are used
LVTMA_STEREOSYNC_SELECT	16	0x0	Select between CRTC1 and CRTC2 stereosync signals 0=CRTC1 STEREOSYNC used 1=CRTC2 STEREOSYNC used
Source Select control for Data, H/VSYNC & Stereosync			

LVTMA_COLOR_FORMAT - RW - 32 bits - DISPDEC:0x7A88			
Field Name	**Bits**	**Default**	**Description**
LVTMA_COLOR_FORMAT	1:0	0x0	0: Normal (24bpp) or Twin Single 30bpp (8 MSBs of each component) 1: Twin-Single 30bpp (2 LSBs of each component) 2: Dual-Link 30bpp (8 MSBs on one link, 2 LSBs on the other) 3: Reserved

LVTMA_FORCE_OUTPUT_CNTL - RW - 32 bits - DISPDEC:0x7A8C			
Field Name	**Bits**	**Default**	**Description**
LVTMA_FORCE_DATA_EN	0	0x0	Enable force option on LVTMA 0=Disable 1=Enable
LVTMA_FORCE_DATA_SEL	10:8	0x0	Select LVTMA channels that have data forced0=Don't Force, 1=Force Bit 0: Blue channel Bit 1: Green channel Bit 2: Red channel
LVTMA_FORCE_DATA_ON_BLANKb_ONLY	16	0x0	Force Data during active region 0=Disable 1=Enable
Data Force Control			

LVTMA_FORCE_DATA - RW - 32 bits - DISPDEC:0x7A90			
Field Name	**Bits**	**Default**	**Description**
LVTMA_FORCE_DATA	7:0	0x0	Data to be forced on R, G & B channels

LVTMA_BIT_DEPTH_CONTROL - RW - 32 bits - DISPDEC:0x7A94			
Field Name	**Bits**	**Default**	**Description**
LVTMA_TRUNCATE_EN	0	0x0	Enable bit reduction by truncation 0=Disable 1=Enable
LVTMA_TRUNCATE_DEPTH	4	0x0	Controls truncation depth 0=18bpp 1=24bpp
LVTMA_SPATIAL_DITHER_EN	8	0x0	Enable bit reduction by spatial (random) dither 0=Disable 1=Enable
LVTMA_SPATIAL_DITHER_DEPTH	12	0x0	Controls reduction depth 0=18bpp 1=24bpp
LVTMA_TEMPORAL_DITHER_EN	16	0x0	Enable bit reduction by temporal dither (frame mod.) 0=Disable 1=Enable
LVTMA_TEMPORAL_DITHER_DEPTH	20	0x0	Controls dither Depth 0=18bpp 1=24bpp

LVTMA_TEMPORAL_LEVEL	24	0x0	Gray level select (2 or 4 levels) 0=Gray level 2(1 bit - LSB) 1=Gray level 4(2 bits - 2 LSBs)
LVTMA_TEMPORAL_DITHER_RESET	26	0x0	Reset temporal dither (frame modulation) 0=Temporal Dither Ready 1=Reset Temporal Dither Circuit
Control the method in which the data input into the TMDS block is reduced and the length it is reduced to.			

LVTMA_CONTROL_CHAR - RW - 32 bits - DISPDEC:0x7A98			
Field Name	**Bits**	**Default**	**Description**
LVTMA_CONTROL_CHAR0_OUT_EN	0	0x0	Programmable sync character 0 enable
LVTMA_CONTROL_CHAR1_OUT_EN	1	0x0	Programmable sync character 1 enable
LVTMA_CONTROL_CHAR2_OUT_EN	2	0x0	Programmable sync character 2 enable
LVTMA_CONTROL_CHAR3_OUT_EN	3	0x0	Programmable sync character 3 enable
SYNC Character Enable. Each bit represents the use of register defined sync character.			

LVTMA_CONTROL0_FEEDBACK - RW - 32 bits - DISPDEC:0x7A9C			
Field Name	**Bits**	**Default**	**Description**
LVTMA_CONTROL0_FEEDBACK_SELECT	1:0	0x0	Select input of CTL0 for TMDS
LVTMA_CONTROL0_FEEDBACK_DELAY	9:8	0x0	Select delay of CTL0 for TMDS

LVTMA_STEREOSYNC_CTL_SEL - RW - 32 bits - DISPDEC:0x7AA0			
Field Name	**Bits**	**Default**	**Description**
LVTMA_STEREOSYNC_CTL_SEL	1:0	0x0	Controls with CTL signal STEREOSYNC goes on to 0=TMDS CTL registers have normal functionality 1=Stereosync will use TMDS CTL1 register 2=Stereosync will use TMDS CTL2 register 3=Stereosync will use TMDS CTL3 register

LVTMA_SYNC_CHAR_PATTERN_SEL - RW - 32 bits - DISPDEC:0x7AA4			
Field Name	**Bits**	**Default**	**Description**
LVTMA_SYNC_CHAR_PATTERN_SEL	3:0	0x0	Reserved
Not Currently Connected			

LVTMA_SYNC_CHAR_PATTERN_0_1 - RW - 32 bits - DISPDEC:0x7AA8			
Field Name	**Bits**	**Default**	**Description**
LVTMA_SYNC_CHAR_PATTERN0	9:0	0x0	LVTMA SYNC character set 0
LVTMA_SYNC_CHAR_PATTERN1	25:16	0x0	LVTMA SYNC character set 1

LVTMA_SYNC_CHAR_PATTERN_2_3 - RW - 32 bits - DISPDEC:0x7AAC

Field Name	Bits	Default	Description
LVTMA_SYNC_CHAR_PATTERN2	9:0	0x0	LVTMA SYNC character set 2
LVTMA_SYNC_CHAR_PATTERN3	25:16	0x0	LVTMA SYNC character set 3

LVTMA_CRC_CNTL - RW - 32 bits - DISPDEC:0x7AB0			
Field Name	**Bits**	**Default**	**Description**
LVTMA_CRC_EN	0	0x0	Enable LVTMA CRC calculation 0=Disable 1=Enable
LVTMA_CRC_CONT_EN	4	0x0	Select continuous or one-shot mode for primary CRC 0=CRC is calculated over 1 frame 1=CRC is continuously calculated for every frame
LVTMA_CRC_ONLY_BLANKb	8	0x0	Determines whether primary CRC is calculated for the whole frame or only during non-blank period. 0=CRC calculated over entire field 1=CRC calculated only during BLANKb
LVTMA_CRC_FIELD	12	0x0	Controls which field polarity starts the LVTMA CRC block after LVTMA_CRC_EN is set to 1. Used only for interlaced mode CRCs 0=Even field begins CRC calculation 1=Odd field begins CRC calculation
LVTMA_2ND_CRC_EN	16	0x0	Enable LVTMA 2nd CRC calculation 0=Disable 1=Enable
LVTMA_2ND_CRC_SEL	20	0x0	Select which LVTM link to perform CRC on 0=Perform CRC on link0 1=Perform CRC on link1
LVTMA_2ND_CRC_DE_ONLY	24	0x1	Select whether to perform CRC on all data or active (data enable) region only 0=2ND CRC calculated over entire field 1=2ND CRC calculated only during BLANKb
Enable LVTMA CRC Calculation			

LVTMA_CRC_SIG_MASK - RW - 32 bits - DISPDEC:0x7AB4			
Field Name	**Bits**	**Default**	**Description**
LVTMA_CRC_SIG_BLUE_MASK	7:0	0xff	CRC mask bits for LVTMA blue component
LVTMA_CRC_SIG_GREEN_MASK	15:8	0xff	CRC mask bits for LVTMA green component
LVTMA_CRC_SIG_RED_MASK	23:16	0xff	CRC mask bits for LVTMA red component
LVTMA_CRC_SIG_CONTROL_MASK	26:24	0x7	CRC mask bits for LVTMA control signals 3-bit input value: bit 2 = Vsync bit 1 = Hsync bit 0 =Data Enable
RGB and Control CRC Mask			

LVTMA_CRC_SIG_RGB - RW - 32 bits - DISPDEC:0x7AB8			
Field Name	**Bits**	**Default**	**Description**
LVTMA_CRC_SIG_BLUE (R)	7:0	0x0	CRC signature value for LVTMA blue component
LVTMA_CRC_SIG_GREEN (R)	15:8	0x0	CRC signature value for LVTMA green component
LVTMA_CRC_SIG_RED (R)	23:16	0x0	CRC signature value for LVTMA red component
LVTMA_CRC_SIG_CONTROL (R)	26:24	0x0	CRC signature value for LVTMA control signals3-bit input value: bit 2 = Vsync bit 1 = Hsync bit 0 =Data Enable
RGB and Control CRC Result			

LVTMA_2ND_CRC_RESULT - RW - 32 bits - DISPDEC:0x7ABC			
Field Name	**Bits**	**Default**	**Description**
LVTMA_2ND_CRC_RESULT (R)	29:0	0x0	LVTMA 2ND CRC readback

LVTMA_TEST_PATTERN - RW - 32 bits - DISPDEC:0x7AC0			
Field Name	**Bits**	**Default**	**Description**
LVTMA_TEST_PATTERN_OUT_EN	0	0x0	LVTMA Test output pattern 0=Normal functionality determined by value of LVTMA_RANDOM_PATTERN_OUT_EN register 1=Test pattern output mode. The value of LVTMA_HALF_CLOCK_PATTERN_SEL determines whether a static 10-bit test data pattern or an alternating half-clock pattern will be output.
LVTMA_HALF_CLOCK_PATTERN_SEL	1	0x0	Controls between Static test pattern output and alternating static output pattern 0=10 bit test pattern from LVTMA_STATIC_TEST_PATTERN is sent during every pixel clock 1=Alternating pattern of LVTMA_STATIC_TEST_PATTERN and !(LVTMA_STATIC_TEST_PATTERN) on each subsequent pixel clock cycle is sent during every pixel clock
LVTMA_LVDS_TEST_CLOCK_DATA	2	0x0	Controls between normal output and clock output test pattern 0=Normal 1=Replace clock pattern with test data
LVTMA_RANDOM_PATTERN_OUT_EN	4	0x0	0: Output normal data or eye pattern (LVDS only) 1: Output random data 0=Normal 1=Random Pixel Data Generator circuit generates 24-bit pixel data to be encoded and transmitted
LVTMA_RANDOM_PATTERN_RESET	5	0x1	Reset random pattern to pattern seed 0=Enable Random Pixel Data Generator 1=Random Pixel Data Generator is Reset to the value in LVTMA_RANDOM_PATTERN_SEED
LVTMA_TEST_PATTERN_EXTERNAL_RESET_EN	6	0x1	0=Normal 1=External signal resets random and half clock patterns
LVTMA_LVDS_EYE_PATTERN	8	0x0	Controls between normal output and LVDS eye pattern 0=Normal 1=Replace data with eye pattern
LVTMA_STATIC_TEST_PATTERN	25:16	0x0	LVTMA test pixel. Replace the pixel value when LVTMA_TEST_PATTERN_OUT_EN=1

LVTMA_RANDOM_PATTERN_SEED - RW - 32 bits - DISPDEC:0x7AC4			
Field Name	**Bits**	**Default**	**Description**
LVTMA_RANDOM_PATTERN_SEED	23:0	0x222222	Initial pattern for eye pattern measurement
LVTMA_RAN_PAT_DURING_DE_ONLY	24	0x0	Controls when to output random data 0=TMDS Random Data Pattern is output for all pixels 1=TMDS Random Data Pattern is only output when DE is high

LVTMA_DEBUG - RW - 32 bits - DISPDEC:0x7AC8			
Field Name	**Bits**	**Default**	**Description**
LVTMA_DEBUG_EN	0	0x0	Set to 1 to enable debug mode
LVTMA_DEBUG_HSYNC	8	0x0	Debug mode HSYNC
LVTMA_DEBUG_HSYNC_EN	9	0x0	Set to 1 to enable debug mode HSYNC
LVTMA_DEBUG_VSYNC	16	0x0	Debug mode VSYNC
LVTMA_DEBUG_VSYNC_EN	17	0x0	Set to 1 to enable debug mode VSYNC
LVTMA_DEBUG_DE	24	0x0	Debug mode display enable
LVTMA_DEBUG_DE_EN	25	0x0	Set to 1 to enable debug mode display enable

LVTMA_CTL_BITS - RW - 32 bits - DISPDEC:0x7ACC			
Field Name	**Bits**	**Default**	**Description**
LVTMA_CTL0	0	0x0	Control signal for LVTMA (encoded in Green channel).
LVTMA_CTL1	8	0x0	Control signal for LVTMA (encoded in Green channel).
LVTMA_CTL2	16	0x0	Control signal for LVTMA (encoded in Red channel).
LVTMA_CTL3	24	0x0	Control signal for LVTMA (encoded in Red channel).

LVTMA_DCBALANCER_CONTROL - RW - 32 bits - DISPDEC:0x7AD0			
Field Name	**Bits**	**Default**	**Description**
LVTMA_DCBALANCER_EN	0	0x1	DC Balancer Enable 0=Disable 1=Enable
LVTMA_DCBALANCER_TEST_EN	8	0x0	DC Balancer Test Enable
LVTMA_DCBALANCER_TEST_IN	19:16	0x0	DC Balancer Test Input
LVTMA_DCBALANCER_FORCE	24	0x0	DC Balancer select value to use when DCBALANCER_EN=0

LVTMA_RED_BLUE_SWITCH - RW - 32 bits - DISPDEC:0x7AD4			
Field Name	**Bits**	**Default**	**Description**
LVTMA_RB_SWITCH_EN	0	0x0	Switch Red and Blue encoding position. 0=Disable 1=Enable

LVTMA_DATA_SYNCHRONIZATION - RW - 32 bits - DISPDEC:0x7AD8			
Field Name	**Bits**	**Default**	**Description**
LVTMA_DSYNSEL	0	0x0	Data synchronization circuit select enable 0=Disable 1=Enable
LVTMA_PFREQCHG (W)	8	0x0	Write to 1 to restarts read and write address generation logic. Write of 0 has no effect. Read value is always 0. PFREQCHG must be written to 1 when the data synchronizer is started by setting DSYNSEL to 1, whenever LVTMA_DUAL_LINK_ENABLE is reprogrammed, or either PCLK_LVTMA or PCLK_LVTMA_DIRECT (IDCLK) is reprogrammed or stopped and restarted.
LVTMA Data Sychronization Control			

LVTMA_CTL0_1_GEN_CNTL - RW - 32 bits - DISPDEC:0x7ADC			
Field Name	**Bits**	**Default**	**Description**
LVTMA_CTL0_DATA_SEL	3:0	0x0	Select data to be used to generate CTL0 pattern (selected fields are ORed together) [0]: Display Enable [1]: VSYNC [2]: HSYNC [3] Random data
LVTMA_CTL0_DATA_DELAY	6:4	0x0	Number of pixel clocks to delay CTL0 data 0=CTL0 data is delayed 0 pixel clocks 1=CTL0 data is delayed 1 pixel clocks 2=CTL0 data is delayed 2 pixel clocks 3=CTL0 data is delayed 3 pixel clocks 4=CTL0 data is delayed 4 pixel clocks 5=CTL0 data is delayed 5 pixel clocks 6=CTL0 data is delayed 6 pixel clocks 7=CTL0 data is delayed 7 pixel clocks
LVTMA_CTL0_DATA_INVERT	7	0x0	Set to 1 to invert CTL0 data 0=CTL0 data is normal 1=CTL0 data is inverted
LVTMA_CTL0_DATA_MODULATION	9:8	0x0	CTL0 data modulation control 0=CTL0 data is not modulated 1=CTL0 data is modulated by bit 0 of 2 bit counter 2=CTL0 data is modulated by bit 1 of 2 bit counter 3=CTL0 data is modulated every time 2 bit counter overflows
LVTMA_CTL0_USE_FEEDBACK_PATH	10	0x0	Set to 1 to enable CTL0 internal feedback path
LVTMA_CTL0_FB_SYNC_CONT	11	0x0	Set to 1 to force continuous toggle on CTL0 internal feedback path
LVTMA_CTL0_PATTERN_OUT_EN	12	0x0	Select CTL0 output data 0=Register value 1=Pattern generator output
LVTMA_CTL1_DATA_SEL	19:16	0x0	Select data to be used to generate CTL1 pattern (selected fields are ORed together) [0]: Display Enable [1]: VSYNC [2]: HSYNC [3] Always (blank time)
LVTMA_CTL1_DATA_DELAY	22:20	0x0	Number of pixel clocks to delay CTL1 data 0=CTL1 data is delayed 0 pixel clocks 1=CTL1 data is delayed 1 pixel clocks 2=CTL1 data is delayed 2 pixel clocks 3=CTL1 data is delayed 3 pixel clocks 4=CTL1 data is delayed 4 pixel clocks 5=CTL1 data is delayed 5 pixel clocks 6=CTL1 data is delayed 6 pixel clocks 7=CTL1 data is delayed 7 pixel clocks

LVTMA_CTL1_DATA_INVERT	23	0x0	Set to 1 to invert CTL1 data 0=CTL1 data is normal 1=CTL1 data is inverted
LVTMA_CTL1_DATA_MODULATION	25:24	0x0	CTL1 data modulation control 0=CTL1 data is not modulated 1=CTL1 data is modulated by bit 0 of 2 bit counter 2=CTL1 data is modulated by bit 1 of 2 bit counter 3=CTL1 data is modulated every time 2 bit counter overflows
LVTMA_CTL1_USE_FEEDBACK_PATH	26	0x0	Set to 1 to enable CTL1 internal feedback path
LVTMA_CTL1_FB_SYNC_CONT	27	0x0	Set to 1 to force continuous toggle on CTL1 internal feedback path
LVTMA_CTL1_PATTERN_OUT_EN	28	0x0	Select CTL1 output data 0=Register value 1=Pattern generator output
LVTMA_2BIT_COUNTER_EN	31	0x0	Set to 1 to enable 2-bit data modulation counter 0=Disable 1=Enable

LVTMA_CTL2_3_GEN_CNTL - RW - 32 bits - DISPDEC:0x7AE0			
Field Name	**Bits**	**Default**	**Description**
LVTMA_CTL2_DATA_SEL	3:0	0x0	Select data to be used to generate CTL2 pattern (selected fields are ORed together) [0]: Display Enable [1]: VSYNC [2]: HSYNC [3] Always (blank time)
LVTMA_CTL2_DATA_DELAY	6:4	0x0	Number of pixel clocks to delay CTL2 data 0=CTL2 data is delayed 0 pixel clocks 1=CTL2 data is delayed 1 pixel clocks 2=CTL2 data is delayed 2 pixel clocks 3=CTL2 data is delayed 3 pixel clocks 4=CTL2 data is delayed 4 pixel clocks 5=CTL2 data is delayed 5 pixel clocks 6=CTL2 data is delayed 6 pixel clocks 7=CTL2 data is delayed 7 pixel clocks
LVTMA_CTL2_DATA_INVERT	7	0x0	Set to 1 to invert CTL2 data 0=CTL2 data is normal 1=CTL2 data is inverted
LVTMA_CTL2_DATA_MODULATION	9:8	0x0	CTL2 data modulation control 0=CTL2 data is not modulated 1=CTL2 data is modulated by bit 0 of 2 bit counter 2=CTL2 data is modulated by bit 1 of 2 bit counter 3=CTL2 data is modulated every time 2 bit counter overflows
LVTMA_CTL2_USE_FEEDBACK_PATH	10	0x0	Set to 1 to enable CTL2 internal feedback path
LVTMA_CTL2_FB_SYNC_CONT	11	0x0	Set to 1 to force continuous toggle on CTL2 internal feedback path
LVTMA_CTL2_PATTERN_OUT_EN	12	0x0	Select CTL2 output data 0=Register value 1=Pattern generator output
LVTMA_CTL3_DATA_SEL	19:16	0x0	Select data to be used to generate CTL3 pattern (selected fields are ORed together) [0]: Display Enable [1]: VSYNC [2]: HSYNC [3] Always (blank time)

LVTMA_CTL3_DATA_DELAY	22:20	0x0	Number of pixel clocks to delay CTL3 data 0=CTL3 data is delayed 0 pixel clocks 1=CTL3 data is delayed 1 pixel clocks 2=CTL3 data is delayed 2 pixel clocks 3=CTL3 data is delayed 3 pixel clocks 4=CTL3 data is delayed 4 pixel clocks 5=CTL3 data is delayed 5 pixel clocks 6=CTL3 data is delayed 6 pixel clocks 7=CTL3 data is delayed 7 pixel clocks
LVTMA_CTL3_DATA_INVERT	23	0x0	Set to 1 to invert CTL3 data 0=CTL3 data is normal 1=CTL3 data is inverted
LVTMA_CTL3_DATA_MODULATION	25:24	0x0	CTL3 data modulation control 0=CTL3 data is not modulated 1=CTL3 data is modulated by bit 0 of 2 bit counter 2=CTL3 data is modulated by bit 1 of 2 bit counter 3=CTL3 data is modulated every time 2 bit counter overflows
LVTMA_CTL3_USE_FEEDBACK_PATH	26	0x0	Set to 1 to enable CTL3 internal feedback path
LVTMA_CTL3_FB_SYNC_CONT	27	0x0	Set to 1 to force continuous toggle on CTL3 internal feedback path
LVTMA_CTL3_PATTERN_OUT_EN	28	0x0	Select CTL3 output data 0=Register value 1=Pattern generator output

LVTMA_PWRSEQ_REF_DIV - RW - 32 bits - DISPDEC:0x7AE4			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PWRSEQ_REF_DIV	11:0	0x0	Determines frequency of reference for power sequencing Frequency = REF/(PWREQ_REF_DIV+1), REF=1MHz (normally)
LVTMA_BL_MOD_REF_DIV	27:16	0x0	Determines frequency of modulated BLON Frequency = REF/(256*(BL_MOD_REF_DIV+1)), REF=1MHz (normally)

LVTMA_PWRSEQ_DELAY1 - RW - 32 bits - DISPDEC:0x7AE8			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PWRUP_DELAY1	7:0	0x0	Number of LVTMA_PWRSEQ_REF pulses to delay from DIGON enable to SYNCEN (LVTMA transmitter macro) enable during powerup. Must be long enough for bandgap reference and PLL startup (= reset assertion time + PLL lock time).
LVTMA_PWRUP_DELAY2	15:8	0x0	Number of LVTMA_PWRSEQ_REF pulses to delay from SYNCEN enable to BLON enable during powerup
LVTMA_PWRDN_DELAY1	23:16	0x0	Number of LVTMA_PWRSEQ_REF pulses to delay from BLON disable to SYNCEN disable during power down
LVTMA_PWRDN_DELAY2	31:24	0x0	Number of LVTMA_PWRSEQ_REF pulses to delay from SYNCEN disable to DIGON disable during power down

LVTMA_PWRSEQ_DELAY2 - RW - 32 bits - DISPDEC:0x7AEC			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PWRDN_MIN_LENGTH	7:0	0x0	Number of LVTMA_PWRSEQ_REF pulses to delay from completion of powerdown to powerup

LVTMA_PWRSEQ_CNTL - RW - 32 bits - DISPDEC:0x7AF0			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PWRSEQ_EN	0	0x0	Set to 1 to enable the power sequencer. When disabled, SYNCEN will be set to 1 and all other outputs set to 0. This allows software or HPD logic to control the LVTM macro transmitter enable bits.Software should set the target state and macro enable bits in LVTMA_TRANSMITTER_ENABLE to 0 (off) before enabling this bit. When enabled, the power sequencer will be in the POWERDOWN_DONE state. Once the power sequencer is enabled, the macro enable bits in LVTMA_TRANSMITTER_ENABLE should be set to 1 if the LVTMA macro is to be used. This allows the power sequencer to control the macro enable bits.The macro will not be turned on until LVTMA_PWRSEQ_TARGET_STATE is set to 1.
LVTMA_PLL_ENABLE_PWRSEQ_MASK	2	0x0	Determines whether power sequencer can force LVTMA_PLL_ENABLE to 0. When LVTMA_PLL_ENABLE_PWRSEQ_MASK=1, enable will be deasserted 1 us after hardware asserts PLL reset to match LVTMA macro timing requirements 0=Power Sequencer cannot override PLL enable 1=Power Sequencer can override PLL enable
LVTMA_PLL_RESET_PWRSEQ_MASK	3	0x0	Determines whether power sequencer can force LVTMA_PLL_RESET to 1. When LVTMA_PLL_RESET_PWRSEQ_MASK=1, reset will be asserted for 10 us after hardware enables PLL to match LVTMA macro timing requirements 0=Power Sequencer cannot override PLL reset 1=Power Sequencer can override PLL reset
LVTMA_PWRSEQ_TARGET_STATE	4	0x0	0:LCD off 1:LCD on PM_PWRSEQ_TARGET_STATE (from power management) must also be 1 to enable the panel.
LVTMA_SYNCEN	8	0x0	LVDS transmitter enable
LVTMA_SYNCEN_OVRD	9	0x0	Enable override of power sequencer SYNCEN by register value 0=Disable 1=Enable
LVTMA_SYNCEN_POL	10	0x0	Polarity of output SYNCEN signal 0=Non-invert 1=Invert
LVTMA_DIGON	16	0x0	LVDS digital voltage 0:off 1:on
LVTMA_DIGON_OVRD	17	0x0	Enable override of power sequencer DIGON by register value 0=Disable 1=Enable
LVTMA_DIGON_POL	18	0x0	Polarity of output DIGON signal 0=Non-invert 1=Invert
LVTMA_BLON	24	0x0	LVDS backlight voltage 0:off 1:on
LVTMA_BLON_OVRD	25	0x0	Enable override of power sequencer BLON (before modulation) by register value 0=Disable 1=Enable
LVTMA_BLON_POL	26	0x0	Polarity of output BLON signal 0=Non-invert 1=Invert

LVTMA_PWRSEQ_STATE - RW - 32 bits - DISPDEC:0x7AF4			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PWRSEQ_TARGET_STATE_R (R)	0	0x0	Power sequencer target state (0=powerdown, 1=powerup)This is an AND of LVTMA_PWRSEQ_TARGET_STATE and the enable from power management logic. 0=power down 1=power up
LVTMA_PWRSEQ_DIGON (R)	1	0x0	Power sequencer DIGON state 0=off 1=on
LVTMA_PWRSEQ_SYNCEN (R)	2	0x0	Power sequencer SYNCEN state 0=off 1=on
LVTMA_PWRSEQ_BLON (R)	3	0x0	Power sequencer BLON state 0=off 1=on
LVTMA_PWRSEQ_DONE (R)	4	0x0	Indicates that power sequencer has reached target state (either DISABLED, POWERDOWN_DONE, or POWERUP_DONE depending on LVTMA_PWRSEQ_EN and LVTMA_PWRSEQ_TARGET_STATE_R) 0=active 1=done
LVTMA_PWRSEQ_STATE (R)	11:8	0x0	Indicates power sequencer's state 0=DISABLED: D=0, B=0, S=LVTMA_PWRSEQ_TARGET_STATE_R 1=POWERUP0: D=0 S=0 B=0 2=POWERUP1: D=1 S=0 B=0 3=POWERUP2: D=1 S=1 B=0 4=POWERUP_DONE: D=1 S=1 B=1 5=POWERDOWN0: D=1 S=1 B=1 6=POWERDOWN1: D=1 S=1 B=0 7=POWERDOWN2: D=1 S=0 B=0 8=POWERDOWN_DELAY: D=0 S=0 B=0 Ignore powerup request 9=POWERDOWN_DONE: D=0 S=0 B=0

LVTMA_BL_MOD_CNTL - RW - 32 bits - DISPDEC:0x7AF8			
Field Name	**Bits**	**Default**	**Description**
LVTMA_BL_MOD_EN	0	0x0	Enable backlight modulation 0=Disable LCD backlight modulation 1=Enable LCD backlight modulation
LVTMA_BL_MOD_LEVEL	15:8	0x0	Determines duty cycle of BLON signal duty cycle = BL_MOD_LEVEL/256

LVTMA_LVDS_DATA_CNTL - RW - 32 bits - DISPDEC:0x7AFC			
Field Name	**Bits**	**Default**	**Description**
LVTMA_LVDS_24BIT_ENABLE	0	0x0	Enable 4th data channel for 24-bit output 0=Disable 1=Enable

LVTMA_LVDS_24BIT_FORMAT	4	0x0	0: Use LDI format for 888 RGB: (LSB first) CH0: G2, R7-2 CH1: B3-2, G7-3 CH2: DE, VSYN, HSYN, B7-4 CH3: N/A, B1-0, G1-0, R1-0 1: Use FPDI format for 888 RGB: (LSB first) CH0: G0, R5-0 CH1: B1-0, G5-1 CH2: DE, VSYN, HSYN, B5-2 CH3: N/A, B7-6, G7-6, R7-6
LVTMA_LVDS_2ND_CHAN_DE	8	0x0	0=Control bit[0] in third channel of 2nd link 1=DE in third data port of 2nd channel
LVTMA_LVDS_2ND_CHAN_VS	9	0x0	0=Control bit[1] in third channel of 2nd link 1=VS in third data port of 2nd channel
LVTMA_LVDS_2ND_CHAN_HS	10	0x0	0=Control bit[2] in third channel of 2nd link 1=HS in third data port of 2nd channel
LVTMA_LVDS_2ND_LINK_CNTL_BITS	14:12	0x0	Bits to put in place of DE (bit 2), VS (bit 1), HS (bit 0) based on programming of bits 8, 9 & 11 above
LVTMA_LVDS_FP_POL	16	0x0	Polarity of frame pulse encoded in lvds data stream 0=active high Frame Pulse / Vsync 1=active low Frame Pulse / Vsync
LVTMA_LVDS_LP_POL	17	0x0	Polarity of line pulse encoded in lvds data stream 0=active high Line Pulse / Hsync 1=active low Line Pulse / Hsync
LVTMA_LVDS_DTMG_POL	18	0x0	Polarity of display enable encoded in lvds data stream 0=active high Display Enable / MOD 1=active low Display Enable / MOD

LVTMA_MODE - RW - 32 bits - DISPDEC:0x7B00			
Field Name	**Bits**	**Default**	**Description**
LVTMA_TMDS_LVDSb	0	0x0	Selects whether LVTMA path is in LVDS or TMDS mode.Also drives LVTMA macro ITXSEL pin. HW for mode that is not selected is disabled. 0=LVDS 1=TMDS

LVTMA_TRANSMITTER_ENABLE - RW - 32 bits - DISPDEC:0x7B04			
Field Name	**Bits**	**Default**	**Description**
LVTMA_LNKC0EN	1	0x0	LVTMA link0 clock channel enable (ICH3EN)(set to 1 whenever LVTM is enabled)
LVTMA_LNKD00EN	2	0x0	LVTMA link0 data channel 0 enable (ICH0EN)(set to 1 whenever LVTM is enabled)
LVTMA_LNKD01EN	3	0x0	LVTMA link0 data channel 1 enable (ICH1EN)(set to 1 whenever LVTM is enabled)
LVTMA_LNKD02EN	4	0x0	LVTMA link0 data channel 2 enable (ICH2EN)(set to 1 whenever LVTM is enabled)
LVTMA_LNKD03EN	5	0x0	LVTMA link0 data channel 3 enable (ICH4EN)(set to 1 when LVTM is enabled and in 24bpp LVDS mode)
LVTMA_LNKC1EN	9	0x0	LVTMA link1 clock channel enable (ICH8EN)(set to 1 when LVTM is enabled and in LVDS dual-link mode)
LVTMA_LNKD10EN	10	0x0	LVTMA link1 data channel 0 enable (ICH5EN)(set to 1 when LVTM is enabled and in dual-link mode)
LVTMA_LNKD11EN	11	0x0	LVTMA link1 data channel 1 enable (ICH6EN)(set to 1 when LVTM is enabled and in dual-link mode)

LVTMA_LNKD12EN	12	0x0	LVTMA link1 data channel 2 enable (ICH7EN)(set to 1 when LVTM is enabled and in dual-link mode)
LVTMA_LNKD13EN	13	0x0	LVTMA link1 data channel 3 enable (ICH9EN)(set to 1 when LVTM is enabled and in 24bpp LVDS dual-link mode)
LVTMA_LNKCEN_HPD_MASK	17	0x0	0:Disallow 1:Allow override of LVTMA_LNKCXEN by HPD on disconnect 0=Result from HPD circuit can not override LVTMA_LNKC0EN 1=Result from HPD circuit overrides LVTMA_LNKC0EN on disconnect
LVTMA_LNKDEN_HPD_MASK	18	0x0	0:Disallow 1:Allow override of LVTMA_LNKDXEN by HPD on disconnect 0=Result from HPD circuit can not override LVTMA_LNKDXEN 1=Result from HPD circuit overrides LVTMA_LNKDXEN on disconnect

LVTMA_LOAD_DETECT - RW - 32 bits - DISPDEC:0x7B08			
Field Name	**Bits**	**Default**	**Description**
LVTMA_LOAD_DETECT_ENABLE	0	0x0	0: Disable 1: Enable LVTMA macro load detect function. Drives IMSEN macro input Note: macro doesn't currently have this function, but leave register or placeholder here for future implementations
LVTMA_LOAD_DETECT (R)	4	0x0	From LVTMA macro load detect output 0: No load detected 1: Load detected Note: macro doesn't currently have this function, but leave register or placeholder here for future implementations
RTL support for this feature is included although LVTM macro doesn't support it yet			

LVTMA_MACRO_CONTROL - RW - 32 bits - DISPDEC:0x7B0C			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PLL_CP_GAIN	5:0	0x3	LVTMA PLL charge-pump gain control. Go to IPPLCP(5:0) pins of LVTMA macro.
LVTMA_PLL_VCO_GAIN	13:8	0x4	LVTMA PLL VCO gain control. Go to IPPLVG(5:0) pins of LVTMA macro.
LVTMA_PLL_DUTY_CYCLE	17:16	0x2	LVTMA PLL duty cycle control. Go to IPPLDC(1:0) pins of LVTMA macro.
LVTMA_TX_VOLTAGE_SWING	23:20	0x4	LVTMA driver voltage swing control. Go to IPTXVS(3:0) pins of LVTMA macro.
LVTMA_TX_OPAMP	27:24	0x4	LVTMA Tx opamp adjustment. Go to IPTXOP(3:0) pins of LVTMA macro.

LVTMA_TRANSMITTER_CONTROL - RW - 32 bits - DISPDEC:0x7B10			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PLL_ENABLE	0	0x0	LVTMA transmitter PLL enable. 0=LVTMA Transmitter PLL is disabled 1=LVTMA Transmitter PLL is enabled
LVTMA_PLL_RESET	1	0x1	LVTMA transmitter PLL reset. PLL will start the locking acquisition process once this becomes low.

LVTMA_PLL_ENABLE_HPD_MASK	3:2	0x0	Determines whether result from HPD circuit can override LVTMA_PLL_ENABLE and LVTMA_ PLL_RESET. 0=Result from HPD circuit can not override LVTMA_PLL_ENABLE 1=Result from HPD circuit overrides LVTMA_PLL_ENABLE on disconnect 2=Result from HPD circuit overrides LVTMA_PLL_ENABLE on connect 3=Result from HPD circuit overrides LVTMA_PLL_ENABLE
LVTMA_IDSCKSEL	4	0x1	0=LVTM Transmitter uses pclk_lvtma (IPIXCLK) 1=LVTM Transmitter uses pclk_lvtma_direct (IDCLK)
LVTMA_BGSLEEP	5	0x0	LVTMA Bandgap macro disable. Set to 0 for normal operation (hardware will enable the macro whenever LVTMA is active), 1 to turn the bandgap macro off regardless of LVTMA status.Note that LVTMA shares the bandgap macro with DACB. For the shared macro either DACB or LVTMA can turn the macro on. Set to 0 in LVDS mode, 1 in TMDS mode. 0=Normal operation 1=Disable bandgap
LVTMA_TMCLK	12:8	0x0	(only bit0 is used in LVTM macro). For macro debug only
LVTMA_TMCLK_FROM_PADS	13	0x0	0=Input to ITMCLK pins on macro come from LVTMA_TMCLK field 1=Input to ITMCLK pins on macro come from pads
LVTMA_TDCLK	14	0x0	For macro debug only
LVTMA_TDCLK_FROM_PADS	15	0x0	0=Input to ITDCLK pin on macro comes from LVTMA_TDCLK field 1=Input to ITDCLK pin on macro comes from pads
LVTMA_CLK_PATTERN	25:16	0x63	Data to be serialized to generate a clock when LVTMA_USE_CLK_DATA=0 If LVTMA_USE_CLK_DATA=1, LVTMA_CLK_PATTERN is 'don't care' and can be set to 0 In LVDS mode the 7 LSBs are used, in TMDS mode all 10 bits are used. For National Compatible mode, set LVTMA_CLK_PATTERN to XXX1100011 For VESA FPDI-2 Compatible mode, set LVTMA_CLK_PATTERN to XXX0001111 For TMDS, set LVTMA_CLK_PATTERN to 0000011111
LVTMA_BYPASS_PLL	28	0x1	Controls ICHCSEL1 pin on LVTM macro 0: Coherent mode: transmitted clock is PLL output 1: Incoherent mode: transmitted clock is PLL input 0=0: Coherent mode: transmitted clock is PLL output 1=1: Incoherent mode: transmitted clock is PLL input
LVTMA_USE_CLK_DATA	29	0x0	Controls ICHCSEL2 pin on LVTM macro Use to determine whether clock comes from PLL output or serialized LVTMA_CLK_PATTERN See macro spec for recommended settings in TMDS and LVDS modes 0=0: Use serialized data (LVTMA_CLK_PATTERN) as clock 1=1: Use clock selected by LVTMA_BYPASS_PLL (ICHCSEL1)
LVTMA_INPUT_TEST_CLK_SEL	31	0x0	Controls ITCLKSEL pin on LVTM macro

LVTMA_REG_TEST_OUTPUT - RW - 32 bits - DISPDEC:0x7B14			
Field Name	**Bits**	**Default**	**Description**
LVTMA_REG_TEST_OUTPUT (R)	9:0	0x0	From LVTMA macro OTDAT(9:0) outputs
LVTMA_TEST_CNTL	21:16	0x0	Drives LVTMA macro ITEST(5:0) control bits (for debug only)

LVTMA_TRANSMITTER_DEBUG - RW - 32 bits - DISPDEC:0x7B18			
Field Name	**Bits**	**Default**	**Description**
LVTMA_PLL_DEBUG	7:0	0x0	Drives ITPL pins on LVTMA macro (this functionality doesn't exist - pins are unconnected)
LVTMA_TX_DEBUG	11:8	0x0	Drives ITX pins on LVTMA macro (this functionality doesn't exist ? pins are unconnected)
Reserved for debugging purposes			

Appendix A
Cross Referenced Index

A.1 Quick Cross-Reference Index

A.2 Configuration Registers Sorted by Name

Table A-1 Configuration Registers Sorted by Name

Register Name	Address	Secondary Address	Page
ADAPTER_ID	*CFGF0_DEC:0x2C*	*HIDEC:0x502C*	*2-64*
ADAPTER_ID_W	*CFGF0_DEC:0x4C*	*HIDEC:0x504C*	*2-65*
BASE_CODE	*CFGF0_DEC:0xB*	*HIDEC:0x500B*	*2-62*
BIOS_ROM	*CFGF0_DEC:0x30*	*HIDEC:0x5030*	*2-64*
BIST	*CFGF0_DEC:0xF*	*HIDEC:0x500F*	*2-63*
CACHE_LINE	*CFGF0_DEC:0xC*	*HIDEC:0x500C*	*2-62*
CAPABILITIES_PTR	*CFGF0_DEC:0x34*	*HIDEC:0x5034*	*2-64*
COMMAND	*CFGF0_DEC:0x4*	*HIDEC:0x5004*	*2-61*
DEVICE_CAP	*CFGF0_DEC:0x5C*	*HIDEC:0x505C*	*2-67*
DEVICE_CNTL	*CFGF0_DEC:0x60*	*HIDEC:0x5060*	*2-67*
DEVICE_ID	*CFGF0_DEC:0x2*	*HIDEC:0x5002*	*2-61*
DEVICE_STATUS	*CFGF0_DEC:0x62*	*HIDEC:0x5062*	*2-68*
F1_ADAPTER_ID	*CFGF1_DEC:0x2C*	*HIDEC:0x542C*	*2-75*
F1_BASE_CODE	*CFGF1_DEC:0xB*	*HIDEC:0x540B*	*2-74*
F1_BIST	*CFGF1_DEC:0xF*	*HIDEC:0x540F*	*2-75*
F1_CACHE_LINE	*CFGF1_DEC:0xC*	*HIDEC:0x540C*	*2-74*
F1_CAPABILITIES_PTR	*CFGF1_DEC:0x34*	*HIDEC:0x5434*	*2-75*
F1_COMMAND	*CFGF1_DEC:0x4*	*HIDEC:0x5404*	*2-73*
F1_DEVICE_CAP	*CFGF1_DEC:0x5C*	*HIDEC:0x545C*	*2-77*
F1_DEVICE_CNTL	*CFGF1_DEC:0x60*	*HIDEC:0x5460*	*2-78*
F1_DEVICE_ID	*CFGF1_DEC:0x2*	*HIDEC:0x5402*	*2-73*
F1_DEVICE_STATUS	*CFGF1_DEC:0x62*	*HIDEC:0x5462*	*2-78*
F1_HEADER	*CFGF1_DEC:0xE*	*HIDEC:0x540E*	*2-74*
F1_INTERRUPT_LINE	*CFGF1_DEC:0x3C*	*HIDEC:0x543C*	*2-75*
F1_INTERRUPT_PIN	*CFGF1_DEC:0x3D*	*HIDEC:0x543D*	*2-76*
F1_LATENCY	*CFGF1_DEC:0xD*	*HIDEC:0x540D*	*2-74*
F1_LINK_CAP	*CFGF1_DEC:0x64*	*HIDEC:0x5464*	*2-79*
F1_LINK_CNTL	*CFGF1_DEC:0x68*	*HIDEC:0x5468*	*2-79*
F1_LINK_STATUS	*CFGF1_DEC:0x6A*	*HIDEC:0x546A*	*2-79*
F1_MAX_LATENCY	*CFGF1_DEC:0x3F*	*HIDEC:0x543F*	*2-76*
F1_MIN_GRANT	*CFGF1_DEC:0x3E*	*HIDEC:0x543E*	*2-76*
F1_PCIE_CAP	*CFGF1_DEC:0x5A*	*HIDEC:0x545A*	*2-77*
F1_PCIE_CAP_LIST	*CFGF1_DEC:0x58*	*HIDEC:0x5458*	*2-77*
F1_PMI_BSE	*CFGF1_DEC:0x56*	*HIDEC:0x5456*	*2-77*
F1_PMI_CAP_ID	*CFGF1_DEC:0x50*	*HIDEC:0x5450*	*2-76*
F1_PMI_DATA	*CFGF1_DEC:0x57*	*HIDEC:0x5457*	*2-77*
F1_PMI_NXT_CAP_PTR	*CFGF1_DEC:0x51*	*HIDEC:0x5451*	*2-76*
F1_PMI_PMC_REG	*CFGF1_DEC:0x52*	*HIDEC:0x5452*	*2-76*
F1_PMI_STATUS	*CFGF1_DEC:0x54*	*HIDEC:0x5454*	*2-77*
F1_REG_BASE_HI	*CFGF1_DEC:0x14*	*HIDEC:0x541C*	*2-75*
F1_REG_BASE_LO	*CFGF1_DEC:0x10*	*HIDEC:0x5414*	*2-75*
F1_REGPROG_INF	*CFGF1_DEC:0x9*	*HIDEC:0x5409*	*2-74*
F1_REVISION_ID	*CFGF1_DEC:0x8*	*HIDEC:0x5408*	*2-73*
F1_STATUS	*CFGF1_DEC:0x6*	*HIDEC:0x5406*	*2-73*

Table A-1 Configuration Registers Sorted by Name (Continued)

Register Name	Address	Secondary Address	Page
F1_SUB_CLASS	CFGF1_DEC:0xA	HIDEC:0x540A	2-74
F1_VENDOR_ID	CFGF1_DEC:0x0	HIDEC:0x5400	2-73
HEADER	CFGF0_DEC:0xE	HIDEC:0x500E	2-63
INTERRUPT_LINE	CFGF0_DEC:0x3C	HIDEC:0x503C	2-65
INTERRUPT_PIN	CFGF0_DEC:0x3D	HIDEC:0x503D	2-65
IO_BASE	CFGF0_DEC:0x14	HIDEC:0x5014	2-64
IO_BASE_WS	CFGF0_DEC:0x20	HIDEC:0x5020	2-64
LATENCY	CFGF0_DEC:0xD	HIDEC:0x500D	2-62
LINK_CAP	CFGF0_DEC:0x64	HIDEC:0x5064	2-68
LINK_CNTL	CFGF0_DEC:0x68	HIDEC:0x5068	2-68
LINK_STATUS	CFGF0_DEC:0x6A	HIDEC:0x506A	2-69
MAX_LATENCY	CFGF0_DEC:0x3F	HIDEC:0x503F	2-65
MEM_BASE_HI	CFGF0_DEC:0x14	HIDEC:0x5014	2-63
MEM_BASE_LO	CFGF0_DEC:0x10	HIDEC:0x5010	2-63
MIN_GRANT	CFGF0_DEC:0x3E	HIDEC:0x503E	2-65
MSI_CAP_ID	CFGF0_DEC:0x80	HIDEC:0x5080	2-69
MSI_MSG_ADDR_HI	CFGF0_DEC:0x88	HIDEC:0x5088	2-70
MSI_MSG_ADDR_LO	CFGF0_DEC:0x84	HIDEC:0x5084	2-70
MSI_MSG_CNTL	CFGF0_DEC:0x82	HIDEC:0x5082	2-69
MSI_MSG_DATA	CFGF0_DEC:0x88	HIDEC:0x5088	2-70
MSI_MSG_DATA_64	CFGF0_DEC:0x8C	HIDEC:0x508C	2-70
MSI_NXT_CAP_PTR	CFGF0_DEC:0x81	HIDEC:0x5081	2-69
PCIE_ADV_ERR_CAP_CNTL	CFGF0_DEC:0x118	HIDEC:0x5118	2-72
PCIE_CAP	CFGF0_DEC:0x5A	HIDEC:0x505A	2-66
PCIE_CAP_LIST	CFGF0_DEC:0x58	HIDEC:0x5058	2-66
PCIE_CORR_ERR_MASK	CFGF0_DEC:0x114	HIDEC:0x5114	2-72
PCIE_CORR_ERR_STATUS	CFGF0_DEC:0x110	HIDEC:0x5110	2-71
PCIE_ENH_ADV_ERR_RPT_CAP_HDR	CFGF0_DEC:0x100	HIDEC:0x5100	2-70
PCIE_HDR_LOG0	CFGF0_DEC:0x11C	HIDEC:0x511C	2-72
PCIE_HDR_LOG1	CFGF0_DEC:0x120	HIDEC:0x5120	2-72
PCIE_HDR_LOG2	CFGF0_DEC:0x124	HIDEC:0x5124	2-72
PCIE_HDR_LOG3	CFGF0_DEC:0x128	HIDEC:0x5128	2-72
PCIE_UNCORR_ERR_MASK	CFGF0_DEC:0x108	HIDEC:0x5108	2-71
PCIE_UNCORR_ERR_SEVERITY	CFGF0_DEC:0x10C	HIDEC:0x510C	2-71
PCIE_UNCORR_ERR_STATUS	CFGF0_DEC:0x104	HIDEC:0x5104	2-70
PMI_BSE	CFGF0_DEC:0x56	HIDEC:0x5056	2-66
PMI_CAP_ID	CFGF0_DEC:0x50	HIDEC:0x5050	2-65
PMI_DATA	CFGF0_DEC:0x57	HIDEC:0x5057	2-66
PMI_NXT_CAP_PTR	CFGF0_DEC:0x51	HIDEC:0x5051	2-65
PMI_PMC_REG	CFGF0_DEC:0x52	HIDEC:0x5052	2-66
PMI_STATUS	CFGF0_DEC:0x54	HIDEC:0x5054	2-66
REG_BASE_HI	CFGF0_DEC:0x1C	HIDEC:0x501C	2-64
REG_BASE_LO	CFGF0_DEC:0x18	HIDEC:0x5018	2-63
REGPROG_INF	CFGF0_DEC:0x9	HIDEC:0x5009	2-62
REVISION_ID	CFGF0_DEC:0x8	HIDEC:0x5008	2-62
STATUS	CFGF0_DEC:0x6	HIDEC:0x5006	2-61

Table A-1 Configuration Registers Sorted by Name (Continued)

Register Name	Address	Secondary Address	Page
SUB_CLASS	*CFGF0_DEC:0xA*	*HIDEC:0x500A*	*2-62*
VENDOR_ID	*CFGF0_DEC:0x0*	*HIDEC:0x5000*	*2-60*

A.3 Configuration Registers Sorted by Address

Table A-2 Configuration Registers Sorted by Address

Register Name	Address	Secondary Address	Page
VENDOR_ID	CFGF0_DEC:0x0	HIDEC:0x5000	2-60
MEM_BASE_LO	CFGF0_DEC:0x10	HIDEC:0x5010	2-63
PCIE_ENH_ADV_ERR_RPT_CAP_HDR	CFGF0_DEC:0x100	HIDEC:0x5100	2-70
PCIE_UNCORR_ERR_STATUS	CFGF0_DEC:0x104	HIDEC:0x5104	2-70
PCIE_UNCORR_ERR_MASK	CFGF0_DEC:0x108	HIDEC:0x5108	2-71
PCIE_UNCORR_ERR_SEVERITY	CFGF0_DEC:0x10C	HIDEC:0x510C	2-71
PCIE_CORR_ERR_STATUS	CFGF0_DEC:0x110	HIDEC:0x5110	2-71
PCIE_CORR_ERR_MASK	CFGF0_DEC:0x114	HIDEC:0x5114	2-72
PCIE_ADV_ERR_CAP_CNTL	CFGF0_DEC:0x118	HIDEC:0x5118	2-72
PCIE_HDR_LOG0	CFGF0_DEC:0x11C	HIDEC:0x511C	2-72
PCIE_HDR_LOG1	CFGF0_DEC:0x120	HIDEC:0x5120	2-72
PCIE_HDR_LOG2	CFGF0_DEC:0x124	HIDEC:0x5124	2-72
PCIE_HDR_LOG3	CFGF0_DEC:0x128	HIDEC:0x5128	2-72
MEM_BASE_HI	CFGF0_DEC:0x14	HIDEC:0x5014	2-63
IO_BASE	CFGF0_DEC:0x14	HIDEC:0x5014	2-64
REG_BASE_LO	CFGF0_DEC:0x18	HIDEC:0x5018	2-63
REG_BASE_HI	CFGF0_DEC:0x1C	HIDEC:0x501C	2-64
DEVICE_ID	CFGF0_DEC:0x2	HIDEC:0x5002	2-61
IO_BASE_WS	CFGF0_DEC:0x20	HIDEC:0x5020	2-64
ADAPTER_ID	CFGF0_DEC:0x2C	HIDEC:0x502C	2-64
BIOS_ROM	CFGF0_DEC:0x30	HIDEC:0x5030	2-64
CAPABILITIES_PTR	CFGF0_DEC:0x34	HIDEC:0x5034	2-64
INTERRUPT_LINE	CFGF0_DEC:0x3C	HIDEC:0x503C	2-65
INTERRUPT_PIN	CFGF0_DEC:0x3D	HIDEC:0x503D	2-65
MIN_GRANT	CFGF0_DEC:0x3E	HIDEC:0x503E	2-65
MAX_LATENCY	CFGF0_DEC:0x3F	HIDEC:0x503F	2-65
COMMAND	CFGF0_DEC:0x4	HIDEC:0x5004	2-61
ADAPTER_ID_W	CFGF0_DEC:0x4C	HIDEC:0x504C	2-65
PMI_CAP_ID	CFGF0_DEC:0x50	HIDEC:0x5050	2-65
PMI_NXT_CAP_PTR	CFGF0_DEC:0x51	HIDEC:0x5051	2-65
PMI_PMC_REG	CFGF0_DEC:0x52	HIDEC:0x5052	2-66
PMI_STATUS	CFGF0_DEC:0x54	HIDEC:0x5054	2-66
PMI_BSE	CFGF0_DEC:0x56	HIDEC:0x5056	2-66
PMI_DATA	CFGF0_DEC:0x57	HIDEC:0x5057	2-66
PCIE_CAP_LIST	CFGF0_DEC:0x58	HIDEC:0x5058	2-66
PCIE_CAP	CFGF0_DEC:0x5A	HIDEC:0x505A	2-66
DEVICE_CAP	CFGF0_DEC:0x5C	HIDEC:0x505C	2-67
STATUS	CFGF0_DEC:0x6	HIDEC:0x5006	2-61
DEVICE_CNTL	CFGF0_DEC:0x60	HIDEC:0x5060	2-67
DEVICE_STATUS	CFGF0_DEC:0x62	HIDEC:0x5062	2-68
LINK_CAP	CFGF0_DEC:0x64	HIDEC:0x5064	2-68
LINK_CNTL	CFGF0_DEC:0x68	HIDEC:0x5068	2-68
LINK_STATUS	CFGF0_DEC:0x6A	HIDEC:0x506A	2-69
REVISION_ID	CFGF0_DEC:0x8	HIDEC:0x5008	2-62

Table A-2 Configuration Registers Sorted by Address (Continued)

Register Name	Address	Secondary Address	Page
MSI_CAP_ID	*CFGF0_DEC:0x80*	*HIDEC:0x5080*	*2-69*
MSI_NXT_CAP_PTR	*CFGF0_DEC:0x81*	*HIDEC:0x5081*	*2-69*
MSI_MSG_CNTL	*CFGF0_DEC:0x82*	*HIDEC:0x5082*	*2-69*
MSI_MSG_ADDR_LO	*CFGF0_DEC:0x84*	*HIDEC:0x5084*	*2-70*
MSI_MSG_ADDR_HI	*CFGF0_DEC:0x88*	*HIDEC:0x5088*	*2-70*
MSI_MSG_DATA	*CFGF0_DEC:0x88*	*HIDEC:0x5088*	*2-70*
MSI_MSG_DATA_64	*CFGF0_DEC:0x8C*	*HIDEC:0x508C*	*2-70*
REGPROG_INF	*CFGF0_DEC:0x9*	*HIDEC:0x5009*	*2-62*
SUB_CLASS	*CFGF0_DEC:0xA*	*HIDEC:0x500A*	*2-62*
BASE_CODE	*CFGF0_DEC:0xB*	*HIDEC:0x500B*	*2-62*
CACHE_LINE	*CFGF0_DEC:0xC*	*HIDEC:0x500C*	*2-62*
LATENCY	*CFGF0_DEC:0xD*	*HIDEC:0x500D*	*2-62*
HEADER	*CFGF0_DEC:0xE*	*HIDEC:0x500E*	*2-63*
BIST	*CFGF0_DEC:0xF*	*HIDEC:0x500F*	*2-63*
F1_VENDOR_ID	*CFGF1_DEC:0x0*	*HIDEC:0x5400*	*2-73*
F1_REG_BASE_LO	*CFGF1_DEC:0x10*	*HIDEC:0x5414*	*2-75*
F1_REG_BASE_HI	*CFGF1_DEC:0x14*	*HIDEC:0x541C*	*2-75*
F1_DEVICE_ID	*CFGF1_DEC:0x2*	*HIDEC:0x5402*	*2-73*
F1_ADAPTER_ID	*CFGF1_DEC:0x2C*	*HIDEC:0x542C*	*2-75*
F1_CAPABILITIES_PTR	*CFGF1_DEC:0x34*	*HIDEC:0x5434*	*2-75*
F1_INTERRUPT_LINE	*CFGF1_DEC:0x3C*	*HIDEC:0x543C*	*2-75*
F1_INTERRUPT_PIN	*CFGF1_DEC:0x3D*	*HIDEC:0x543D*	*2-76*
F1_MIN_GRANT	*CFGF1_DEC:0x3E*	*HIDEC:0x543E*	*2-76*
F1_MAX_LATENCY	*CFGF1_DEC:0x3F*	*HIDEC:0x543F*	*2-76*
F1_COMMAND	*CFGF1_DEC:0x4*	*HIDEC:0x5404*	*2-73*
F1_PMI_CAP_ID	*CFGF1_DEC:0x50*	*HIDEC:0x5450*	*2-76*
F1_PMI_NXT_CAP_PTR	*CFGF1_DEC:0x51*	*HIDEC:0x5451*	*2-76*
F1_PMI_PMC_REG	*CFGF1_DEC:0x52*	*HIDEC:0x5452*	*2-76*
F1_PMI_STATUS	*CFGF1_DEC:0x54*	*HIDEC:0x5454*	*2-77*
F1_PMI_BSE	*CFGF1_DEC:0x56*	*HIDEC:0x5456*	*2-77*
F1_PMI_DATA	*CFGF1_DEC:0x57*	*HIDEC:0x5457*	*2-77*
F1_PCIE_CAP_LIST	*CFGF1_DEC:0x58*	*HIDEC:0x5458*	*2-77*
F1_PCIE_CAP	*CFGF1_DEC:0x5A*	*HIDEC:0x545A*	*2-77*
F1_DEVICE_CAP	*CFGF1_DEC:0x5C*	*HIDEC:0x545C*	*2-77*
F1_STATUS	*CFGF1_DEC:0x6*	*HIDEC:0x5406*	*2-73*
F1_DEVICE_CNTL	*CFGF1_DEC:0x60*	*HIDEC:0x5460*	*2-78*
F1_DEVICE_STATUS	*CFGF1_DEC:0x62*	*HIDEC:0x5462*	*2-78*
F1_LINK_CAP	*CFGF1_DEC:0x64*	*HIDEC:0x5464*	*2-79*
F1_LINK_CNTL	*CFGF1_DEC:0x68*	*HIDEC:0x5468*	*2-79*
F1_LINK_STATUS	*CFGF1_DEC:0x6A*	*HIDEC:0x546A*	*2-79*
F1_REVISION_ID	*CFGF1_DEC:0x8*	*HIDEC:0x5408*	*2-73*
F1_REGPROG_INF	*CFGF1_DEC:0x9*	*HIDEC:0x5409*	*2-74*
F1_SUB_CLASS	*CFGF1_DEC:0xA*	*HIDEC:0x540A*	*2-74*
F1_BASE_CODE	*CFGF1_DEC:0xB*	*HIDEC:0x540B*	*2-74*
F1_CACHE_LINE	*CFGF1_DEC:0xC*	*HIDEC:0x540C*	*2-74*
F1_LATENCY	*CFGF1_DEC:0xD*	*HIDEC:0x540D*	*2-74*

Table A-2 Configuration Registers Sorted by Address (Continued)

Register Name	Address	Secondary Address	Page
F1_HEADER	*CFGF1_DEC:0xE*	*HIDEC:0x540E*	*2-74*
F1_BIST	*CFGF1_DEC:0xF*	*HIDEC:0x540F*	*2-75*

A.4 Clock Registers Sorted by Name

Table A-3 Clock Registers Sorted by Name

Register Name	Address	Page
CG_CLKPIN_CNTL	CLKIND:0x3C	2-163
CG_MISC_REG	CLKIND:0x1F	2-161
CG_TC_JTAG_0	CLKIND:0x38	2-164
CG_TC_JTAG_1	CLKIND:0x39	2-164
CLOCK_CNTL_DATA	CGDEC:0xE00C	2-155
CLOCK_CNTL_INDEX	CGDEC:0xE008	2-155
DLL_CNTL	CLKIND:0x23	2-162
DYN_BACKBIAS_CNTL	CLKIND:0x29	2-163
DYN_PWRMGT_SCLK_CNTL	CLKIND:0xB	2-158
DYN_PWRMGT_SCLK_LENGTH	CLKIND:0xC	2-159
DYN_SCLK_PWMEN_PIPE	CLKIND:0xD	2-159
DYN_SCLK_VOL_CNTL	CLKIND:0xE	2-159
ERROR_STATUS	CLKIND:0x2C	2-163
GENERAL_PWRMGT	CLKIND:0x8	2-157
MC_GUI_DYN_CNTL	CLKIND:0x1D	2-160
MC_HOST_DYN_CNTL	CLKIND:0x1E	2-160
MC_RBS_DYN_CNTL	CLKIND:0x26	2-161
MCLK_MISC	CLKIND:0x22	2-161
MCLK_PWRMGT_CNTL	CLKIND:0xA	2-158
MPLL_BYPASSCLK_SEL	CLKIND:0x5	2-157
MPLL_CLK_SEL	CLKIND:0x7	2-157
MPLL_CNTL_MODE	CLKIND:0x6	2-157
MPLL_FUNC_CNTL	CLKIND:0x4	2-156
MPLL_TIME	CLKIND:0x25	2-163
PLL_TEST_CNTL	CLKIND:0x21	2-161
POLARITY_CNTL	CLKIND:0x2A	2-163
SCLK_PWRMGT_CNTL	CLKIND:0x9	2-157
SPLL_BYPASSCLK_SEL	CLKIND:0x1	2-156
SPLL_CLK_SEL	CLKIND:0x3	2-156
SPLL_CNTL_MODE	CLKIND:0x2	2-156
SPLL_FUNC_CNTL	CLKIND:0x0	2-155
SPLL_TIME	CLKIND:0x24	2-162
TCL_DYN_CNTL	CLKIND:0x1A	2-160
VIP_DYN_CNTL	CLKIND:0x14	2-160
VOL_DROP_CNT	CLKIND:0x36	2-164

A.5 Clock Registers Sorted by Address

Table A-4 Clock Registers Sorted by Address

Register Name	Address	Page
CLOCK_CNTL_INDEX	CGDEC:0xE008	2-155
CLOCK_CNTL_DATA	CGDEC:0xE00C	2-155
SPLL_FUNC_CNTL	CLKIND:0x0	2-155
SPLL_BYPASSCLK_SEL	CLKIND:0x1	2-156
VIP_DYN_CNTL	CLKIND:0x14	2-160
TCL_DYN_CNTL	CLKIND:0x1A	2-160
MC_GUI_DYN_CNTL	CLKIND:0x1D	2-160
MC_HOST_DYN_CNTL	CLKIND:0x1E	2-160
CG_MISC_REG	CLKIND:0x1F	2-161
SPLL_CNTL_MODE	CLKIND:0x2	2-156
PLL_TEST_CNTL	CLKIND:0x21	2-161
MCLK_MISC	CLKIND:0x22	2-161
DLL_CNTL	CLKIND:0x23	2-162
SPLL_TIME	CLKIND:0x24	2-162
MPLL_TIME	CLKIND:0x25	2-163
MC_RBS_DYN_CNTL	CLKIND:0x26	2-161
DYN_BACKBIAS_CNTL	CLKIND:0x29	2-163
POLARITY_CNTL	CLKIND:0x2A	2-163
ERROR_STATUS	CLKIND:0x2C	2-163
SPLL_CLK_SEL	CLKIND:0x3	2-156
VOL_DROP_CNT	CLKIND:0x36	2-164
CG_TC_JTAG_0	CLKIND:0x38	2-164
CG_TC_JTAG_1	CLKIND:0x39	2-164
CG_CLKPIN_CNTL	CLKIND:0x3C	2-163
MPLL_FUNC_CNTL	CLKIND:0x4	2-156
MPLL_BYPASSCLK_SEL	CLKIND:0x5	2-157
MPLL_CNTL_MODE	CLKIND:0x6	2-157
MPLL_CLK_SEL	CLKIND:0x7	2-157
GENERAL_PWRMGT	CLKIND:0x8	2-157
SCLK_PWRMGT_CNTL	CLKIND:0x9	2-157
MCLK_PWRMGT_CNTL	CLKIND:0xA	2-158
DYN_PWRMGT_SCLK_CNTL	CLKIND:0xB	2-158
DYN_PWRMGT_SCLK_LENGTH	CLKIND:0xC	2-159
DYN_SCLK_PWMEN_PIPE	CLKIND:0xD	2-159
DYN_SCLK_VOL_CNTL	CLKIND:0xE	2-159

A.6 Display Registers Stored by Name

Table A-5 Display Registers Sorted by Name

Register Name	Address	Page
ATTRDR	DISPDEC:0x3C1	2-181
ATTRDW	DISPDEC:0x3C0	2-181
ATTRX	DISPDEC:0x3C0	2-181
CAPTURE_START_STATUS	DISPDEC:0x7ED0	2-333
CRTC_EXT_CNTL	DISPDEC:0xE054	2-196
CRTC8_DATA	DISPDEC:0x3B5 DISPDEC:0x3D5	2-171
CRTC8_DATA	DISPDEC:0x3B5 DISPDEC:0x3D5	2-196
CRTC8_IDX	DISPDEC:0x3B4 DISPDEC:0x3D4	2-171
CRTC8_IDX	DISPDEC:0x3B4 DISPDEC:0x3D4	2-196
D1COLOR_MATRIX_COEF_1_1	DISPDEC:0x6384	2-217
D1COLOR_MATRIX_COEF_1_2	DISPDEC:0x6388	2-217
D1COLOR_MATRIX_COEF_1_3	DISPDEC:0x638C	2-218
D1COLOR_MATRIX_COEF_1_4	DISPDEC:0x6390	2-218
D1COLOR_MATRIX_COEF_2_1	DISPDEC:0x6394	2-218
D1COLOR_MATRIX_COEF_2_2	DISPDEC:0x6398	2-218
D1COLOR_MATRIX_COEF_2_3	DISPDEC:0x639C	2-218
D1COLOR_MATRIX_COEF_2_4	DISPDEC:0x63A0	2-219
D1COLOR_MATRIX_COEF_3_1	DISPDEC:0x63A4	2-219
D1COLOR_MATRIX_COEF_3_2	DISPDEC:0x63A8	2-219
D1COLOR_MATRIX_COEF_3_3	DISPDEC:0x63AC	2-219
D1COLOR_MATRIX_COEF_3_4	DISPDEC:0x63B0	2-220
D1COLOR_SPACE_CONVERT	DISPDEC:0x613C	2-221
D1CRTC_BLACK_COLOR	DISPDEC:0x6098	2-275
D1CRTC_BLANK_CONTROL	DISPDEC:0x6084	2-274
D1CRTC_BLANK_DATA_COLOR	DISPDEC:0x6090	2-275
D1CRTC_CONTROL	DISPDEC:0x6080	2-273
D1CRTC_COUNT_CONTROL	DISPDEC:0x60B4	2-276
D1CRTC_COUNT_RESET	DISPDEC:0x60B0	2-276
D1CRTC_DOUBLE_BUFFER_CONTROL	DISPDEC:0x60EC	2-280
D1CRTC_FLOW_CONTROL	DISPDEC:0x6074	2-272
D1CRTC_FORCE_COUNT_NOW_CNTL	DISPDEC:0x6070	2-272
D1CRTC_H_BLANK_START_END	DISPDEC:0x6004	2-267
D1CRTC_H_SYNC_A	DISPDEC:0x6008	2-267
D1CRTC_H_SYNC_A_CNTL	DISPDEC:0x600C	2-267
D1CRTC_H_SYNC_B	DISPDEC:0x6010	2-268
D1CRTC_H_SYNC_B_CNTL	DISPDEC:0x6014	2-268

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
D1CRTC_H_TOTAL	DISPDEC:0x6000	2-267
D1CRTC_INTERLACE_CONTROL	DISPDEC:0x6088	2-274
D1CRTC_INTERLACE_STATUS	DISPDEC:0x608C	2-274
D1CRTC_INTERRUPT_CONTROL	DISPDEC:0x60DC	2-278
D1CRTC_MANUAL_FORCE_VSYNC_NEXT_LINE	DISPDEC:0x60B8	2-276
D1CRTC_OVERSCAN_COLOR	DISPDEC:0x6094	2-275
D1CRTC_PIXEL_DATA_READBACK	DISPDEC:0x6078	2-273
D1CRTC_SNAPSHOT_CONTROL	DISPDEC:0x60CC	2-278
D1CRTC_SNAPSHOT_FRAME	DISPDEC:0x60D4	2-278
D1CRTC_SNAPSHOT_POSITION	DISPDEC:0x60D0	2-278
D1CRTC_SNAPSHOT_STATUS	DISPDEC:0x60C8	2-278
D1CRTC_START_LINE_CONTROL	DISPDEC:0x60D8	2-278
D1CRTC_STATUS	DISPDEC:0x609C	2-275
D1CRTC_STATUS_FRAME_COUNT	DISPDEC:0x60A4	2-276
D1CRTC_STATUS_HV_COUNT	DISPDEC:0x60AC	2-276
D1CRTC_STATUS_POSITION	DISPDEC:0x60A0	2-276
D1CRTC_STATUS_VF_COUNT	DISPDEC:0x60A8	2-276
D1CRTC_STEREO_CONTROL	DISPDEC:0x60C4	2-277
D1CRTC_STEREO_FORCE_NEXT_EYE	DISPDEC:0x607C	2-273
D1CRTC_STEREO_STATUS	DISPDEC:0x60C0	2-277
D1CRTC_TRIGA_CNTL	DISPDEC:0x6060	2-270
D1CRTC_TRIGA_MANUAL_TRIG	DISPDEC:0x6064	2-271
D1CRTC_TRIGB_CNTL	DISPDEC:0x6068	2-271
D1CRTC_TRIGB_MANUAL_TRIG	DISPDEC:0x606C	2-272
D1CRTC_UPDATE_LOCK	DISPDEC:0x60E8	2-279
D1CRTC_V_BLANK_START_END	DISPDEC:0x6024	2-268
D1CRTC_V_SYNC_A	DISPDEC:0x6028	2-269
D1CRTC_V_SYNC_A_CNTL	DISPDEC:0x602C	2-269
D1CRTC_V_SYNC_B	DISPDEC:0x6030	2-269
D1CRTC_V_SYNC_B_CNTL	DISPDEC:0x6034	2-269
D1CRTC_V_TOTAL	DISPDEC:0x6020	2-268
D1CRTC_VERT_SYNC_CONTROL	DISPDEC:0x60BC	2-277
D1CRTC_VGA_PARAMETER_CAPTURE_MODE	DISPDEC:0x60F0	2-280
D1CUR_COLOR1	DISPDEC:0x641C	2-223
D1CUR_COLOR2	DISPDEC:0x6420	2-223
D1CUR_CONTROL	DISPDEC:0x6400	2-222
D1CUR_HOT_SPOT	DISPDEC:0x6418	2-223
D1CUR_POSITION	DISPDEC:0x6414	2-222
D1CUR_SIZE	DISPDEC:0x6410	2-222
D1CUR_SURFACE_ADDRESS	DISPDEC:0x6408	2-222

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
D1CUR_UPDATE	DISPDEC:0x6424	2-223
D1GRPH_ALPHA	DISPDEC:0x6304	2-213
D1GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL	DISPDEC:0x6380	2-217
D1GRPH_CONTROL	DISPDEC:0x6104	2-198
D1GRPH_ENABLE	DISPDEC:0x6100	2-198
D1GRPH_FLIP_CONTROL	DISPDEC:0x6148	2-202
D1GRPH_KEY_RANGE_ALPHA	DISPDEC:0x631C	2-215
D1GRPH_KEY_RANGE_BLUE	DISPDEC:0x6318	2-215
D1GRPH_KEY_RANGE_GREEN	DISPDEC:0x6314	2-214
D1GRPH_KEY_RANGE_RED	DISPDEC:0x6310	2-214
D1GRPH_LUT_SEL	DISPDEC:0x6108	2-199
D1GRPH_PITCH	DISPDEC:0x6120	2-200
D1GRPH_PRIMARY_SURFACE_ADDRESS	DISPDEC:0x6110	2-199
D1GRPH_SECONDARY_SURFACE_ADDRESS	DISPDEC:0x6118	2-200
D1GRPH_SURFACE_ADDRESS_INUSE	DISPDEC:0x614C	2-202
D1GRPH_SURFACE_OFFSET_X	DISPDEC:0x6124	2-200
D1GRPH_SURFACE_OFFSET_Y	DISPDEC:0x6128	2-200
D1GRPH_UPDATE	DISPDEC:0x6144	2-201
D1GRPH_X_END	DISPDEC:0x6134	2-201
D1GRPH_X_START	DISPDEC:0x612C	2-200
D1GRPH_Y_END	DISPDEC:0x6138	2-201
D1GRPH_Y_START	DISPDEC:0x6130	2-201
D1ICON_COLOR1	DISPDEC:0x6458	2-224
D1ICON_COLOR2	DISPDEC:0x645C	2-225
D1ICON_CONTROL	DISPDEC:0x6440	2-224
D1ICON_SIZE	DISPDEC:0x6450	2-224
D1ICON_START_POSITION	DISPDEC:0x6454	2-224
D1ICON_SURFACE_ADDRESS	DISPDEC:0x6448	2-224
D1ICON_UPDATE	DISPDEC:0x6460	2-225
D1MODE_MASTER_UPDATE_LOCK	DISPDEC:0x60E0	2-279
D1MODE_MASTER_UPDATE_MODE	DISPDEC:0x60E4	2-279
D1OVL_ALPHA	DISPDEC:0x6308	2-213
D1OVL_ALPHA_CONTROL	DISPDEC:0x630C	2-214
D1OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	DISPDEC:0x6140	2-217
D1OVL_CONTROL1	DISPDEC:0x6184	2-203
D1OVL_CONTROL2	DISPDEC:0x6188	2-203
D1OVL_ENABLE	DISPDEC:0x6180	2-203
D1OVL_END	DISPDEC:0x61A8	2-205
D1OVL_KEY_ALPHA	DISPDEC:0x632C	2-216
D1OVL_KEY_CONTROL	DISPDEC:0x6300	2-213

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
D1OVL_KEY_RANGE_BLUE_CB	*DISPDEC:0x6328*	*2-216*
D1OVL_KEY_RANGE_GREEN_Y	*DISPDEC:0x6324*	*2-215*
D1OVL_KEY_RANGE_RED_CR	*DISPDEC:0x6320*	*2-215*
D1OVL_MATRIX_COEF_1_1	*DISPDEC:0x6204*	*2-206*
D1OVL_MATRIX_COEF_1_2	*DISPDEC:0x6208*	*2-206*
D1OVL_MATRIX_COEF_1_3	*DISPDEC:0x620C*	*2-206*
D1OVL_MATRIX_COEF_1_4	*DISPDEC:0x6210*	*2-206*
D1OVL_MATRIX_COEF_2_1	*DISPDEC:0x6214*	*2-207*
D1OVL_MATRIX_COEF_2_2	*DISPDEC:0x6218*	*2-207*
D1OVL_MATRIX_COEF_2_3	*DISPDEC:0x621C*	*2-207*
D1OVL_MATRIX_COEF_2_4	*DISPDEC:0x6220*	*2-207*
D1OVL_MATRIX_COEF_3_1	*DISPDEC:0x6224*	*2-207*
D1OVL_MATRIX_COEF_3_2	*DISPDEC:0x6228*	*2-208*
D1OVL_MATRIX_COEF_3_3	*DISPDEC:0x622C*	*2-208*
D1OVL_MATRIX_COEF_3_4	*DISPDEC:0x6230*	*2-208*
D1OVL_MATRIX_TRANSFORM_EN	*DISPDEC:0x6200*	*2-206*
D1OVL_PITCH	*DISPDEC:0x6198*	*2-204*
D1OVL_PWL_0TOF	*DISPDEC:0x6284*	*2-209*
D1OVL_PWL_100TO13F	*DISPDEC:0x629C*	*2-210*
D1OVL_PWL_10TO1F	*DISPDEC:0x6288*	*2-209*
D1OVL_PWL_140TO17F	*DISPDEC:0x62A0*	*2-210*
D1OVL_PWL_180TO1BF	*DISPDEC:0x62A4*	*2-210*
D1OVL_PWL_1C0TO1FF	*DISPDEC:0x62A8*	*2-210*
D1OVL_PWL_200TO23F	*DISPDEC:0x62AC*	*2-211*
D1OVL_PWL_20TO3F	*DISPDEC:0x628C*	*2-209*
D1OVL_PWL_240TO27F	*DISPDEC:0x62B0*	*2-211*
D1OVL_PWL_280TO2BF	*DISPDEC:0x62B4*	*2-211*
D1OVL_PWL_2C0TO2FF	*DISPDEC:0x62B8*	*2-211*
D1OVL_PWL_300TO33F	*DISPDEC:0x62BC*	*2-211*
D1OVL_PWL_340TO37F	*DISPDEC:0x62C0*	*2-212*
D1OVL_PWL_380TO3BF	*DISPDEC:0x62C4*	*2-212*
D1OVL_PWL_3C0TO3FF	*DISPDEC:0x62C8*	*2-212*
D1OVL_PWL_40TO7F	*DISPDEC:0x6290*	*2-209*
D1OVL_PWL_80TOBF	*DISPDEC:0x6294*	*2-210*
D1OVL_PWL_C0TOFF	*DISPDEC:0x6298*	*2-210*
D1OVL_PWL_TRANSFORM_EN	*DISPDEC:0x6280*	*2-209*
D1OVL_START	*DISPDEC:0x61A4*	*2-204*
D1OVL_SURFACE_ADDRESS	*DISPDEC:0x6190*	*2-204*
D1OVL_SURFACE_ADDRESS_INUSE	*DISPDEC:0x61B0*	*2-205*
D1OVL_SURFACE_OFFSET_X	*DISPDEC:0x619C*	*2-204*

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
D1OVL_SURFACE_OFFSET_Y	DISPDEC:0x61A0	2-204
D1OVL_UPDATE	DISPDEC:0x61AC	2-205
D1VGA_CONTROL	DISPDEC:0x330	2-189
D2COLOR_MATRIX_COEF_1_1	DISPDEC:0x6B84	2-250
D2COLOR_MATRIX_COEF_1_2	DISPDEC:0x6B88	2-250
D2COLOR_MATRIX_COEF_1_3	DISPDEC:0x6B8C	2-250
D2COLOR_MATRIX_COEF_1_4	DISPDEC:0x6B90	2-251
D2COLOR_MATRIX_COEF_2_1	DISPDEC:0x6B94	2-251
D2COLOR_MATRIX_COEF_2_2	DISPDEC:0x6B98	2-251
D2COLOR_MATRIX_COEF_2_3	DISPDEC:0x6B9C	2-251
D2COLOR_MATRIX_COEF_2_4	DISPDEC:0x6BA0	2-252
D2COLOR_MATRIX_COEF_3_1	DISPDEC:0x6BA4	2-252
D2COLOR_MATRIX_COEF_3_2	DISPDEC:0x6BA8	2-252
D2COLOR_MATRIX_COEF_3_3	DISPDEC:0x6BAC	2-252
D2COLOR_MATRIX_COEF_3_4	DISPDEC:0x6BB0	2-253
D2COLOR_SPACE_CONVERT	DISPDEC:0x693C	2-254
D2CRTC_BLACK_COLOR	DISPDEC:0x6898	2-289
D2CRTC_BLANK_CONTROL	DISPDEC:0x6884	2-287
D2CRTC_BLANK_DATA_COLOR	DISPDEC:0x6890	2-288
D2CRTC_CONTROL	DISPDEC:0x6880	2-287
D2CRTC_COUNT_CONTROL	DISPDEC:0x68B4	2-290
D2CRTC_COUNT_RESET	DISPDEC:0x68B0	2-290
D2CRTC_DOUBLE_BUFFER_CONTROL	DISPDEC:0x68EC	2-293
D2CRTC_FLOW_CONTROL	DISPDEC:0x6874	2-286
D2CRTC_FORCE_COUNT_NOW_CNTL	DISPDEC:0x6870	2-286
D2CRTC_H_BLANK_START_END	DISPDEC:0x6804	2-281
D2CRTC_H_SYNC_A	DISPDEC:0x6808	2-281
D2CRTC_H_SYNC_A_CNTL	DISPDEC:0x680C	2-281
D2CRTC_H_SYNC_B	DISPDEC:0x6810	2-281
D2CRTC_H_SYNC_B_CNTL	DISPDEC:0x6814	2-282
D2CRTC_H_TOTAL	DISPDEC:0x6800	2-280
D2CRTC_INTERLACE_CONTROL	DISPDEC:0x6888	2-288
D2CRTC_INTERLACE_STATUS	DISPDEC:0x688C	2-288
D2CRTC_INTERRUPT_CONTROL	DISPDEC:0x68DC	2-292
D2CRTC_MANUAL_FORCE_VSYNC_NEXT_LINE	DISPDEC:0x68B8	2-290
D2CRTC_OVERSCAN_COLOR	DISPDEC:0x6894	2-288
D2CRTC_PIXEL_DATA_READBACK	DISPDEC:0x6878	2-287
D2CRTC_SNAPSHOT_CONTROL	DISPDEC:0x68CC	2-292
D2CRTC_SNAPSHOT_FRAME	DISPDEC:0x68D4	2-292
D2CRTC_SNAPSHOT_POSITION	DISPDEC:0x68D0	2-292

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
D2CRTC_SNAPSHOT_STATUS	DISPDEC:0x68C8	2-291
D2CRTC_START_LINE_CONTROL	DISPDEC:0x68D8	2-292
D2CRTC_STATUS	DISPDEC:0x689C	2-289
D2CRTC_STATUS_FRAME_COUNT	DISPDEC:0x68A4	2-290
D2CRTC_STATUS_HV_COUNT	DISPDEC:0x68AC	2-290
D2CRTC_STATUS_POSITION	DISPDEC:0x68A0	2-289
D2CRTC_STATUS_VF_COUNT	DISPDEC:0x68A8	2-290
D2CRTC_STEREO_CONTROL	DISPDEC:0x68C4	2-291
D2CRTC_STEREO_FORCE_NEXT_EYE	DISPDEC:0x687C	2-287
D2CRTC_STEREO_STATUS	DISPDEC:0x68C0	2-291
D2CRTC_TRIGA_CNTL	DISPDEC:0x6860	2-283
D2CRTC_TRIGA_MANUAL_TRIG	DISPDEC:0x6864	2-284
D2CRTC_TRIGB_CNTL	DISPDEC:0x6868	2-285
D2CRTC_TRIGB_MANUAL_TRIG	DISPDEC:0x686C	2-286
D2CRTC_UPDATE_LOCK	DISPDEC:0x68E8	2-293
D2CRTC_V_BLANK_START_END	DISPDEC:0x6824	2-282
D2CRTC_V_SYNC_A	DISPDEC:0x6828	2-282
D2CRTC_V_SYNC_A_CNTL	DISPDEC:0x682C	2-283
D2CRTC_V_SYNC_B	DISPDEC:0x6830	2-283
D2CRTC_V_SYNC_B_CNTL	DISPDEC:0x6834	2-283
D2CRTC_V_TOTAL	DISPDEC:0x6820	2-282
D2CRTC_VERT_SYNC_CONTROL	DISPDEC:0x68BC	2-290
D2CRTC_VGA_PARAMETER_CAPTURE_MODE	DISPDEC:0x68F0	2-294
D2CUR_COLOR1	DISPDEC:0x6C1C	2-256
D2CUR_COLOR2	DISPDEC:0x6C20	2-256
D2CUR_CONTROL	DISPDEC:0x6C00	2-255
D2CUR_HOT_SPOT	DISPDEC:0x6C18	2-256
D2CUR_POSITION	DISPDEC:0x6C14	2-255
D2CUR_SIZE	DISPDEC:0x6C10	2-255
D2CUR_SURFACE_ADDRESS	DISPDEC:0x6C08	2-255
D2CUR_UPDATE	DISPDEC:0x6C24	2-256
D2GRPH_ALPHA	DISPDEC:0x6B04	2-246
D2GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL	DISPDEC:0x6B80	2-250
D2GRPH_CONTROL	DISPDEC:0x6904	2-231
D2GRPH_ENABLE	DISPDEC:0x6900	2-231
D2GRPH_FLIP_CONTROL	DISPDEC:0x6948	2-235
D2GRPH_KEY_RANGE_ALPHA	DISPDEC:0x6B1C	2-248
D2GRPH_KEY_RANGE_BLUE	DISPDEC:0x6B18	2-248
D2GRPH_KEY_RANGE_GREEN	DISPDEC:0x6B14	2-247
D2GRPH_KEY_RANGE_RED	DISPDEC:0x6B10	2-247

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
D2GRPH_LUT_SEL	DISPDEC:0x6908	2-232
D2GRPH_PITCH	DISPDEC:0x6920	2-233
D2GRPH_PRIMARY_SURFACE_ADDRESS	DISPDEC:0x6910	2-232
D2GRPH_SECONDARY_SURFACE_ADDRESS	DISPDEC:0x6918	2-233
D2GRPH_SURFACE_ADDRESS_INUSE	DISPDEC:0x694C	2-235
D2GRPH_SURFACE_OFFSET_X	DISPDEC:0x6924	2-233
D2GRPH_SURFACE_OFFSET_Y	DISPDEC:0x6928	2-233
D2GRPH_UPDATE	DISPDEC:0x6944	2-234
D2GRPH_X_END	DISPDEC:0x6934	2-234
D2GRPH_X_START	DISPDEC:0x692C	2-233
D2GRPH_Y_END	DISPDEC:0x6938	2-234
D2GRPH_Y_START	DISPDEC:0x6930	2-234
D2ICON_COLOR1	DISPDEC:0x6C58	2-257
D2ICON_COLOR2	DISPDEC:0x6C5C	2-258
D2ICON_CONTROL	DISPDEC:0x6C40	2-257
D2ICON_SIZE	DISPDEC:0x6C50	2-257
D2ICON_START_POSITION	DISPDEC:0x6C54	2-257
D2ICON_SURFACE_ADDRESS	DISPDEC:0x6C48	2-257
D2ICON_UPDATE	DISPDEC:0x6C60	2-258
D2MODE_MASTER_UPDATE_LOCK	DISPDEC:0x68E0	2-293
D2MODE_MASTER_UPDATE_MODE	DISPDEC:0x68E4	2-293
D2OVL_ALPHA	DISPDEC:0x6B08	2-246
D2OVL_ALPHA_CONTROL	DISPDEC:0x6B0C	2-247
D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	DISPDEC:0x6940	2-250
D2OVL_CONTROL1	DISPDEC:0x6984	2-236
D2OVL_CONTROL2	DISPDEC:0x6988	2-236
D2OVL_ENABLE	DISPDEC:0x6980	2-236
D2OVL_END	DISPDEC:0x69A8	2-238
D2OVL_KEY_ALPHA	DISPDEC:0x6B2C	2-249
D2OVL_KEY_CONTROL	DISPDEC:0x6B00	2-246
D2OVL_KEY_RANGE_BLUE_CB	DISPDEC:0x6B28	2-248
D2OVL_KEY_RANGE_GREEN_Y	DISPDEC:0x6B24	2-248
D2OVL_KEY_RANGE_RED_CR	DISPDEC:0x6B20	2-248
D2OVL_MATRIX_COEF_1_1	DISPDEC:0x6A04	2-239
D2OVL_MATRIX_COEF_1_2	DISPDEC:0x6A08	2-239
D2OVL_MATRIX_COEF_1_3	DISPDEC:0x6A0C	2-239
D2OVL_MATRIX_COEF_1_4	DISPDEC:0x6A10	2-239
D2OVL_MATRIX_COEF_2_1	DISPDEC:0x6A14	2-240
D2OVL_MATRIX_COEF_2_2	DISPDEC:0x6A18	2-240
D2OVL_MATRIX_COEF_2_3	DISPDEC:0x6A1C	2-240

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
D2OVL_MATRIX_COEF_2_4	DISPDEC:0x6A20	2-240
D2OVL_MATRIX_COEF_3_1	DISPDEC:0x6A24	2-240
D2OVL_MATRIX_COEF_3_2	DISPDEC:0x6A28	2-241
D2OVL_MATRIX_COEF_3_3	DISPDEC:0x6A2C	2-241
D2OVL_MATRIX_COEF_3_4	DISPDEC:0x6A30	2-241
D2OVL_MATRIX_TRANSFORM_EN	DISPDEC:0x6A00	2-239
D2OVL_PITCH	DISPDEC:0x6998	2-237
D2OVL_PWL_0TOF	DISPDEC:0x6A84	2-242
D2OVL_PWL_100TO13F	DISPDEC:0x6A9C	2-243
D2OVL_PWL_10TO1F	DISPDEC:0x6A88	2-242
D2OVL_PWL_140TO17F	DISPDEC:0x6AA0	2-243
D2OVL_PWL_180TO1BF	DISPDEC:0x6AA4	2-243
D2OVL_PWL_1C0TO1FF	DISPDEC:0x6AA8	2-243
D2OVL_PWL_200TO23F	DISPDEC:0x6AAC	2-244
D2OVL_PWL_20TO3F	DISPDEC:0x6A8C	2-242
D2OVL_PWL_240TO27F	DISPDEC:0x6AB0	2-244
D2OVL_PWL_280TO2BF	DISPDEC:0x6AB4	2-244
D2OVL_PWL_2C0TO2FF	DISPDEC:0x6AB8	2-244
D2OVL_PWL_300TO33F	DISPDEC:0x6ABC	2-244
D2OVL_PWL_340TO37F	DISPDEC:0x6AC0	2-245
D2OVL_PWL_380TO3BF	DISPDEC:0x6AC4	2-245
D2OVL_PWL_3C0TO3FF	DISPDEC:0x6AC8	2-245
D2OVL_PWL_40TO7F	DISPDEC:0x6A90	2-242
D2OVL_PWL_80TOBF	DISPDEC:0x6A94	2-243
D2OVL_PWL_C0TOFF	DISPDEC:0x6A98	2-243
D2OVL_PWL_TRANSFORM_EN	DISPDEC:0x6A80	2-242
D2OVL_START	DISPDEC:0x69A4	2-237
D2OVL_SURFACE_ADDRESS	DISPDEC:0x6990	2-237
D2OVL_SURFACE_ADDRESS_INUSE	DISPDEC:0x69B0	2-238
D2OVL_SURFACE_OFFSET_X	DISPDEC:0x699C	2-237
D2OVL_SURFACE_OFFSET_Y	DISPDEC:0x69A0	2-237
D2OVL_UPDATE	DISPDEC:0x69AC	2-238
D2VGA_CONTROL	DISPDEC:0x338	2-190
DAC_DATA	DISPDEC:0x3C9	2-168
DAC_MASK	DISPDEC:0x3C6	2-168
DAC_R_INDEX	DISPDEC:0x3C7	2-168
DAC_W_INDEX	DISPDEC:0x3C8	2-168
DACA_AUTODETECT_CONTROL	DISPDEC:0x7828	2-297
DACA_AUTODETECT_CONTROL2	DISPDEC:0x782C	2-297
DACA_AUTODETECT_INT_CONTROL	DISPDEC:0x7838	2-298

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
DACA_AUTODETECT_STATUS	*DISPDEC:0x7834*	*2-297*
DACA_COMPARATOR_ENABLE	*DISPDEC:0x785C*	*2-299*
DACA_COMPARATOR_OUTPUT	*DISPDEC:0x7860*	*2-300*
DACA_CONTROL1	*DISPDEC:0x7854*	*2-298*
DACA_CONTROL2	*DISPDEC:0x7858*	*2-299*
DACA_CRC_CONTROL	*DISPDEC:0x780C*	*2-295*
DACA_CRC_EN	*DISPDEC:0x7808*	*2-295*
DACA_CRC_SIG_CONTROL	*DISPDEC:0x781C*	*2-296*
DACA_CRC_SIG_CONTROL_MASK	*DISPDEC:0x7814*	*2-296*
DACA_CRC_SIG_RGB	*DISPDEC:0x7818*	*2-296*
DACA_CRC_SIG_RGB_MASK	*DISPDEC:0x7810*	*2-295*
DACA_ENABLE	*DISPDEC:0x7800*	*2-295*
DACA_FORCE_DATA	*DISPDEC:0x7840*	*2-298*
DACA_FORCE_OUTPUT_CNTL	*DISPDEC:0x783C*	*2-298*
DACA_POWERDOWN	*DISPDEC:0x7850*	*2-298*
DACA_PWR_CNTL	*DISPDEC:0x7868*	*2-300*
DACA_SOURCE_SELECT	*DISPDEC:0x7804*	*2-295*
DACA_SYNC_SELECT	*DISPDEC:0x7824*	*2-296*
DACA_SYNC_TRISTATE_CONTROL	*DISPDEC:0x7820*	*2-296*
DACA_TEST_ENABLE	*DISPDEC:0x7864*	*2-300*
DACB_AUTODETECT_CONTROL	*DISPDEC:0x7A28*	*2-302*
DACB_AUTODETECT_CONTROL2	*DISPDEC:0x7A2C*	*2-302*
DACB_AUTODETECT_INT_CONTROL	*DISPDEC:0x7A38*	*2-303*
DACB_AUTODETECT_STATUS	*DISPDEC:0x7A34*	*2-303*
DACB_COMPARATOR_ENABLE	*DISPDEC:0x7A5C*	*2-305*
DACB_COMPARATOR_OUTPUT	*DISPDEC:0x7A60*	*2-305*
DACB_CONTROL1	*DISPDEC:0x7A54*	*2-304*
DACB_CONTROL2	*DISPDEC:0x7A58*	*2-304*
DACB_CRC_CONTROL	*DISPDEC:0x7A0C*	*2-301*
DACB_CRC_EN	*DISPDEC:0x7A08*	*2-301*
DACB_CRC_SIG_CONTROL	*DISPDEC:0x7A1C*	*2-302*
DACB_CRC_SIG_CONTROL_MASK	*DISPDEC:0x7A14*	*2-301*
DACB_CRC_SIG_RGB	*DISPDEC:0x7A18*	*2-301*
DACB_CRC_SIG_RGB_MASK	*DISPDEC:0x7A10*	*2-301*
DACB_ENABLE	*DISPDEC:0x7A00*	*2-300*
DACB_FORCE_DATA	*DISPDEC:0x7A40*	*2-304*
DACB_FORCE_OUTPUT_CNTL	*DISPDEC:0x7A3C*	*2-303*
DACB_POWERDOWN	*DISPDEC:0x7A50*	*2-304*
DACB_PWR_CNTL	*DISPDEC:0x7A68*	*2-306*
DACB_SOURCE_SELECT	*DISPDEC:0x7A04*	*2-300*

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
DACB_SYNC_SELECT	DISPDEC:0x7A24	2-302
DACB_SYNC_TRISTATE_CONTROL	DISPDEC:0x7A20	2-302
DACB_TEST_ENABLE	DISPDEC:0x7A64	2-305
DC_CRTC_MASTER_EN	DISPDEC:0x60F8	2-280
DC_CRTC_TV_CONTROL	DISPDEC:0x60FC	2-280
DC_GENERICA	DISPDEC:0x7DC0	2-324
DC_GENERICB	DISPDEC:0x7DC4	2-325
DC_GPIO_DDC1_A	DISPDEC:0x7E44	2-328
DC_GPIO_DDC1_EN	DISPDEC:0x7E48	2-328
DC_GPIO_DDC1_MASK	DISPDEC:0x7E40	2-328
DC_GPIO_DDC1_Y	DISPDEC:0x7E4C	2-328
DC_GPIO_DDC2_A	DISPDEC:0x7E54	2-329
DC_GPIO_DDC2_EN	DISPDEC:0x7E58	2-329
DC_GPIO_DDC2_MASK	DISPDEC:0x7E50	2-328
DC_GPIO_DDC2_Y	DISPDEC:0x7E5C	2-329
DC_GPIO_DDC3_A	DISPDEC:0x7E64	2-329
DC_GPIO_DDC3_EN	DISPDEC:0x7E68	2-330
DC_GPIO_DDC3_MASK	DISPDEC:0x7E60	2-329
DC_GPIO_DDC3_Y	DISPDEC:0x7E6C	2-330
DC_GPIO_DVODATA_A	DISPDEC:0x7E34	2-327
DC_GPIO_DVODATA_EN	DISPDEC:0x7E38	2-327
DC_GPIO_DVODATA_MASK	DISPDEC:0x7E30	2-327
DC_GPIO_DVODATA_Y	DISPDEC:0x7E3C	2-327
DC_GPIO_GENERIC_A	DISPDEC:0x7DE4	2-326
DC_GPIO_GENERIC_EN	DISPDEC:0x7DE8	2-326
DC_GPIO_GENERIC_MASK	DISPDEC:0x7DE0	2-326
DC_GPIO_GENERIC_Y	DISPDEC:0x7DEC	2-326
DC_GPIO_HPD_A	DISPDEC:0x7E94	2-332
DC_GPIO_HPD_EN	DISPDEC:0x7E98	2-332
DC_GPIO_HPD_MASK	DISPDEC:0x7E90	2-331
DC_GPIO_HPD_Y	DISPDEC:0x7E9C	2-332
DC_GPIO_PAD_STRENGTH_1	DISPDEC:0x7ED4	2-334
DC_GPIO_PAD_STRENGTH_2	DISPDEC:0x7ED8	2-334
DC_GPIO_PWRSEQ_A	DISPDEC:0x7EA4	2-332
DC_GPIO_PWRSEQ_EN	DISPDEC:0x7EA8	2-333
DC_GPIO_PWRSEQ_MASK	DISPDEC:0x7EA0	2-332
DC_GPIO_PWRSEQ_Y	DISPDEC:0x7EAC	2-333
DC_GPIO_SYNCA_A	DISPDEC:0x7E74	2-330
DC_GPIO_SYNCA_EN	DISPDEC:0x7E78	2-330
DC_GPIO_SYNCA_MASK	DISPDEC:0x7E70	2-330

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
DC_GPIO_SYNCA_Y	*DISPDEC:0x7E7C*	*2-331*
DC_GPIO_SYNCB_A	*DISPDEC:0x7E84*	*2-331*
DC_GPIO_SYNCB_EN	*DISPDEC:0x7E88*	*2-331*
DC_GPIO_SYNCB_MASK	*DISPDEC:0x7E80*	*2-331*
DC_GPIO_SYNCB_Y	*DISPDEC:0x7E8C*	*2-331*
DC_GPIO_VIP_DEBUG	*DISPDEC:0x7E2C*	*2-326*
DC_HOT_PLUG_DETECT_CLOCK_CONTROL	*DISPDEC:0x7D20*	*2-322*
DC_HOT_PLUG_DETECT1_CONTROL	*DISPDEC:0x7D00*	*2-320*
DC_HOT_PLUG_DETECT1_INT_CONTROL	*DISPDEC:0x7D08*	*2-321*
DC_HOT_PLUG_DETECT1_INT_STATUS	*DISPDEC:0x7D04*	*2-321*
DC_HOT_PLUG_DETECT2_CONTROL	*DISPDEC:0x7D10*	*2-321*
DC_HOT_PLUG_DETECT2_INT_CONTROL	*DISPDEC:0x7D18*	*2-321*
DC_HOT_PLUG_DETECT2_INT_STATUS	*DISPDEC:0x7D14*	*2-321*
DC_I2C_ARBITRATION	*DISPDEC:0x7D50*	*2-324*
DC_I2C_CONTROL1	*DISPDEC:0x7D38*	*2-322*
DC_I2C_CONTROL2	*DISPDEC:0x7D3C*	*2-323*
DC_I2C_CONTROL3	*DISPDEC:0x7D40*	*2-323*
DC_I2C_DATA	*DISPDEC:0x7D44*	*2-323*
DC_I2C_INTERRUPT_CONTROL	*DISPDEC:0x7D48*	*2-323*
DC_I2C_RESET	*DISPDEC:0x7D34*	*2-322*
DC_I2C_STATUS1	*DISPDEC:0x7D30*	*2-322*
DC_LUT_30_COLOR	*DISPDEC:0x6494*	*2-227*
DC_LUT_AUTOFILL	*DISPDEC:0x64A0*	*2-227*
DC_LUT_PWL_DATA	*DISPDEC:0x6490*	*2-226*
DC_LUT_READ_PIPE_SELECT	*DISPDEC:0x6498*	*2-227*
DC_LUT_RW_INDEX	*DISPDEC:0x6488*	*2-226*
DC_LUT_RW_MODE	*DISPDEC:0x6484*	*2-226*
DC_LUT_RW_SELECT	*DISPDEC:0x6480*	*2-226*
DC_LUT_SEQ_COLOR	*DISPDEC:0x648C*	*2-226*
DC_LUT_WRITE_EN_MASK	*DISPDEC:0x649C*	*2-227*
DC_LUTA_BLACK_OFFSET_BLUE	*DISPDEC:0x64C4*	*2-229*
DC_LUTA_BLACK_OFFSET_GREEN	*DISPDEC:0x64C8*	*2-229*
DC_LUTA_BLACK_OFFSET_RED	*DISPDEC:0x64CC*	*2-229*
DC_LUTA_CONTROL	*DISPDEC:0x64C0*	*2-228*
DC_LUTA_WHITE_OFFSET_BLUE	*DISPDEC:0x64D0*	*2-230*
DC_LUTA_WHITE_OFFSET_GREEN	*DISPDEC:0x64D4*	*2-230*
DC_LUTA_WHITE_OFFSET_RED	*DISPDEC:0x64D8*	*2-230*
DC_LUTB_BLACK_OFFSET_BLUE	*DISPDEC:0x6CC4*	*2-260*
DC_LUTB_BLACK_OFFSET_GREEN	*DISPDEC:0x6CC8*	*2-260*
DC_LUTB_BLACK_OFFSET_RED	*DISPDEC:0x6CCC*	*2-260*

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
DC_LUTB_CONTROL	DISPDEC:0x6CC0	2-259
DC_LUTB_WHITE_OFFSET_BLUE	DISPDEC:0x6CD0	2-261
DC_LUTB_WHITE_OFFSET_GREEN	DISPDEC:0x6CD4	2-261
DC_LUTB_WHITE_OFFSET_RED	DISPDEC:0x6CD8	2-261
DC_PAD_EXTERN_SIG	DISPDEC:0x7DCC	2-325
DC_REF_CLK_CNTL	DISPDEC:0x7DD4	2-325
DCO_PERFMON_CNTL_R	DISPDEC:0x7F18	2-339
DCP_CRC_CONTROL	DISPDEC:0x6C80	2-262
DCP_CRC_MASK	DISPDEC:0x6C84	2-262
DCP_CRC_P0_CURRENT	DISPDEC:0x6C88	2-262
DCP_CRC_P0_LAST	DISPDEC:0x6C90	2-262
DCP_CRC_P1_CURRENT	DISPDEC:0x6C8C	2-262
DCP_CRC_P1_LAST	DISPDEC:0x6C94	2-263
DCP_LB_DATA_GAP_BETWEEN_CHUNK	DISPDEC:0x6CBC	2-266
DISP_INTERRUPT_STATUS	DISPDEC:0x7EDC	2-335
DISP_TIMER_CONTROL	DISPDEC:0x7EF0	2-337
DMIF_CONTROL	DISPDEC:0x6CB0	2-264
DMIF_STATUS	DISPDEC:0x6CB4	2-264
DO_PERFCOUNTER0_HI	DISPDEC:0x7F04	2-338
DO_PERFCOUNTER0_LOW	DISPDEC:0x7F08	2-338
DO_PERFCOUNTER0_SELECT	DISPDEC:0x7F00	2-338
DO_PERFCOUNTER1_HI	DISPDEC:0x7F10	2-338
DO_PERFCOUNTER1_LOW	DISPDEC:0x7F14	2-338
DO_PERFCOUNTER1_SELECT	DISPDEC:0x7F0C	2-338
DOUT_POWER_MANAGEMENT_CNTL	DISPDEC:0x7EE0	2-336
DVOA_BIT_DEPTH_CONTROL	DISPDEC:0x7988	2-317
DVOA_CONTROL	DISPDEC:0x7990	2-318
DVOA_CRC_CONTROL	DISPDEC:0x7998	2-318
DVOA_CRC_EN	DISPDEC:0x7994	2-318
DVOA_CRC_SIG_MASK1	DISPDEC:0x799C	2-319
DVOA_CRC_SIG_MASK2	DISPDEC:0x79A0	2-319
DVOA_CRC_SIG_RESULT1	DISPDEC:0x79A4	2-319
DVOA_CRC_SIG_RESULT2	DISPDEC:0x79A8	2-319
DVOA_CRC2_SIG_MASK	DISPDEC:0x79AC	2-319
DVOA_CRC2_SIG_RESULT	DISPDEC:0x79B0	2-319
DVOA_ENABLE	DISPDEC:0x7980	2-316
DVOA_FORCE_DATA	DISPDEC:0x79BC	2-320
DVOA_FORCE_OUTPUT_CNTL	DISPDEC:0x79B8	2-320
DVOA_OUTPUT	DISPDEC:0x798C	2-317
DVOA_SOURCE_SELECT	DISPDEC:0x7984	2-317

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
DVOA_STRENGTH_CONTROL	*DISPDEC:0x79B4*	*2-320*
GEN_INT_STATUS	*DISPDEC:0x104*	*2-339*
GENFC_RD	*DISPDEC:0x3CA*	*2-165*
GENFC_WT	*DISPDEC:0x3BA* *DISPDEC:0x3DA*	*2-165*
GENMO_RD	*DISPDEC:0x3CC*	*2-166*
GENMO_RD	*DISPDEC:0x3CC*	*2-195*
GENMO_WT	*DISPDEC:0x3C2*	*2-165*
GENMO_WT	*DISPDEC:0x3C2*	*2-194*
GENS0	*DISPDEC:0x3C2*	*2-166*
GENS1	*DISPDEC:0x3BA* *DISPDEC:0x3DA*	*2-167*
GRPH8_DATA	*DISPDEC:0x3CF*	*2-178*
GRPH8_DATA	*DISPDEC:0x3CF*	*2-196*
GRPH8_IDX	*DISPDEC:0x3CE*	*2-178*
GRPH8_IDX	*DISPDEC:0x3CE*	*2-196*
LVTMA_2ND_CRC_RESULT	*DISPDEC:0x7ABC*	*2-344*
LVTMA_BIT_DEPTH_CONTROL	*DISPDEC:0x7A94*	*2-341*
LVTMA_BL_MOD_CNTL	*DISPDEC:0x7AF8*	*2-350*
LVTMA_CNTL	*DISPDEC:0x7A80*	*2-340*
LVTMA_COLOR_FORMAT	*DISPDEC:0x7A88*	*2-341*
LVTMA_CONTROL_CHAR	*DISPDEC:0x7A98*	*2-342*
LVTMA_CONTROL0_FEEDBACK	*DISPDEC:0x7A9C*	*2-342*
LVTMA_CRC_CNTL	*DISPDEC:0x7AB0*	*2-343*
LVTMA_CRC_SIG_MASK	*DISPDEC:0x7AB4*	*2-343*
LVTMA_CRC_SIG_RGB	*DISPDEC:0x7AB8*	*2-344*
LVTMA_CTL_BITS	*DISPDEC:0x7ACC*	*2-345*
LVTMA_CTL0_1_GEN_CNTL	*DISPDEC:0x7ADC*	*2-346*
LVTMA_CTL2_3_GEN_CNTL	*DISPDEC:0x7AE0*	*2-347*
LVTMA_DATA_SYNCHRONIZATION	*DISPDEC:0x7AD8*	*2-346*
LVTMA_DCBALANCER_CONTROL	*DISPDEC:0x7AD0*	*2-345*
LVTMA_DEBUG	*DISPDEC:0x7AC8*	*2-345*
LVTMA_FORCE_DATA	*DISPDEC:0x7A90*	*2-341*
LVTMA_FORCE_OUTPUT_CNTL	*DISPDEC:0x7A8C*	*2-341*
LVTMA_LOAD_DETECT	*DISPDEC:0x7B08*	*2-352*
LVTMA_LVDS_DATA_CNTL	*DISPDEC:0x7AFC*	*2-351*
LVTMA_MACRO_CONTROL	*DISPDEC:0x7B0C*	*2-352*
LVTMA_MODE	*DISPDEC:0x7B00*	*2-351*
LVTMA_PWRSEQ_CNTL	*DISPDEC:0x7AF0*	*2-349*
LVTMA_PWRSEQ_DELAY1	*DISPDEC:0x7AE8*	*2-348*
LVTMA_PWRSEQ_DELAY2	*DISPDEC:0x7AEC*	*2-349*

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
LVTMA_PWRSEQ_REF_DIV	*DISPDEC:0x7AE4*	*2-348*
LVTMA_PWRSEQ_STATE	*DISPDEC:0x7AF4*	*2-350*
LVTMA_RANDOM_PATTERN_SEED	*DISPDEC:0x7AC4*	*2-345*
LVTMA_RED_BLUE_SWITCH	*DISPDEC:0x7AD4*	*2-345*
LVTMA_REG_TEST_OUTPUT	*DISPDEC:0x7B14*	*2-354*
LVTMA_SOURCE_SELECT	*DISPDEC:0x7A84*	*2-340*
LVTMA_STEREOSYNC_CTL_SEL	*DISPDEC:0x7AA0*	*2-342*
LVTMA_SYNC_CHAR_PATTERN_0_1	*DISPDEC:0x7AA8*	*2-342*
LVTMA_SYNC_CHAR_PATTERN_2_3	*DISPDEC:0x7AAC*	*2-343*
LVTMA_SYNC_CHAR_PATTERN_SEL	*DISPDEC:0x7AA4*	*2-342*
LVTMA_TEST_PATTERN	*DISPDEC:0x7AC0*	*2-344*
LVTMA_TRANSMITTER_CONTROL	*DISPDEC:0x7B10*	*2-353*
LVTMA_TRANSMITTER_DEBUG	*DISPDEC:0x7B18*	*2-354*
LVTMA_TRANSMITTER_ENABLE	*DISPDEC:0x7B04*	*2-351*
MCIF_CONTROL	*DISPDEC:0x6CB8*	*2-265*
SEQ8_DATA	*DISPDEC:0x3C5*	*2-170*
SEQ8_DATA	*DISPDEC:0x3C5*	*2-195*
SEQ8_IDX	*DISPDEC:0x3C4*	*2-170*
SEQ8_IDX	*DISPDEC:0x3C4*	*2-195*
TMDSA_2ND_CRC_RESULT	*DISPDEC:0x78BC*	*2-310*
TMDSA_BIT_DEPTH_CONTROL	*DISPDEC:0x7894*	*2-307*
TMDSA_CNTL	*DISPDEC:0x7880*	*2-306*
TMDSA_COLOR_FORMAT	*DISPDEC:0x7888*	*2-307*
TMDSA_CONTROL_CHAR	*DISPDEC:0x7898*	*2-308*
TMDSA_CONTROL0_FEEDBACK	*DISPDEC:0x789C*	*2-308*
TMDSA_CRC_CNTL	*DISPDEC:0x78B0*	*2-309*
TMDSA_CRC_SIG_MASK	*DISPDEC:0x78B4*	*2-309*
TMDSA_CRC_SIG_RGB	*DISPDEC:0x78B8*	*2-309*
TMDSA_CTL_BITS	*DISPDEC:0x78CC*	*2-311*
TMDSA_CTL0_1_GEN_CNTL	*DISPDEC:0x78DC*	*2-312*
TMDSA_CTL2_3_GEN_CNTL	*DISPDEC:0x78E0*	*2-313*
TMDSA_DATA_SYNCHRONIZATION	*DISPDEC:0x78D8*	*2-311*
TMDSA_DCBALANCER_CONTROL	*DISPDEC:0x78D0*	*2-311*
TMDSA_DEBUG	*DISPDEC:0x78C8*	*2-311*
TMDSA_FORCE_DATA	*DISPDEC:0x7890*	*2-307*
TMDSA_FORCE_OUTPUT_CNTL	*DISPDEC:0x788C*	*2-307*
TMDSA_LOAD_DETECT	*DISPDEC:0x7908*	*2-315*
TMDSA_MACRO_CONTROL	*DISPDEC:0x790C*	*2-315*
TMDSA_RANDOM_PATTERN_SEED	*DISPDEC:0x78C4*	*2-310*
TMDSA_RED_BLUE_SWITCH	*DISPDEC:0x78D4*	*2-311*

Table A-5 Display Registers Sorted by Name (Continued)

Register Name	Address	Page
TMDSA_REG_TEST_OUTPUT	DISPDEC:0x7914	2-316
TMDSA_SOURCE_SELECT	DISPDEC:0x7884	2-306
TMDSA_STEREOSYNC_CTL_SEL	DISPDEC:0x78A0	2-308
TMDSA_SYNC_CHAR_PATTERN_0_1	DISPDEC:0x78A8	2-308
TMDSA_SYNC_CHAR_PATTERN_2_3	DISPDEC:0x78AC	2-309
TMDSA_SYNC_CHAR_PATTERN_SEL	DISPDEC:0x78A4	2-308
TMDSA_TEST_PATTERN	DISPDEC:0x78C0	2-310
TMDSA_TRANSMITTER_CONTROL	DISPDEC:0x7910	2-315
TMDSA_TRANSMITTER_DEBUG	DISPDEC:0x7918	2-316
TMDSA_TRANSMITTER_ENABLE	DISPDEC:0x7904	2-314
VGA_CACHE_CONTROL	DISPDEC:0x32C	2-189
VGA_DEBUG_READBACK_DATA	DISPDEC:0x35C	2-194
VGA_DEBUG_READBACK_INDEX	DISPDEC:0x358	2-193
VGA_DISPBUF1_SURFACE_ADDR	DISPDEC:0x318	2-188
VGA_DISPBUF2_SURFACE_ADDR	DISPDEC:0x320	2-188
VGA_HDP_CONTROL	DISPDEC:0x328	2-188
VGA_INTERRUPT_CONTROL	DISPDEC:0x344	2-191
VGA_INTERRUPT_STATUS	DISPDEC:0x34C	2-191
VGA_MAIN_CONTROL	DISPDEC:0x350	2-192
VGA_MEM_READ_PAGE_ADDR	DISPDEC:0x3C	2-197
VGA_MEM_WRITE_PAGE_ADDR	DISPDEC:0x38	2-197
VGA_MEMORY_BASE_ADDRESS	DISPDEC:0x310	2-188
VGA_MODE_CONTROL	DISPDEC:0x308	2-187
VGA_RENDER_CONTROL	DISPDEC:0x300	2-186
VGA_SEQUENCER_RESET_CONTROL	DISPDEC:0x304	2-187
VGA_STATUS	DISPDEC:0x340	2-190
VGA_STATUS_CLEAR	DISPDEC:0x348	2-191
VGA_SURFACE_PITCH_SELECT	DISPDEC:0x30C	2-187
VGA_TEST_CONTROL	DISPDEC:0x354	2-193

A.7 Display Registers Stored by Address

Table A-6 Display Registers Sorted by Address

Register Name	Address	Page
GEN_INT_STATUS	DISPDEC:0x104	2-339
VGA_RENDER_CONTROL	DISPDEC:0x300	2-186
VGA_SEQUENCER_RESET_CONTROL	DISPDEC:0x304	2-187
VGA_MODE_CONTROL	DISPDEC:0x308	2-187
VGA_SURFACE_PITCH_SELECT	DISPDEC:0x30C	2-187
VGA_MEMORY_BASE_ADDRESS	DISPDEC:0x310	2-188
VGA_DISPBUF1_SURFACE_ADDR	DISPDEC:0x318	2-188
VGA_DISPBUF2_SURFACE_ADDR	DISPDEC:0x320	2-188
VGA_HDP_CONTROL	DISPDEC:0x328	2-188
VGA_CACHE_CONTROL	DISPDEC:0x32C	2-189
D1VGA_CONTROL	DISPDEC:0x330	2-189
D2VGA_CONTROL	DISPDEC:0x338	2-190
VGA_STATUS	DISPDEC:0x340	2-190
VGA_INTERRUPT_CONTROL	DISPDEC:0x344	2-191
VGA_STATUS_CLEAR	DISPDEC:0x348	2-191
VGA_INTERRUPT_STATUS	DISPDEC:0x34C	2-191
VGA_MAIN_CONTROL	DISPDEC:0x350	2-192
VGA_TEST_CONTROL	DISPDEC:0x354	2-193
VGA_DEBUG_READBACK_INDEX	DISPDEC:0x358	2-193
VGA_DEBUG_READBACK_DATA	DISPDEC:0x35C	2-194
VGA_MEM_WRITE_PAGE_ADDR	DISPDEC:0x38	2-197
CRTC8_IDX	DISPDEC:0x3B4 DISPDEC:0x3D4	2-171
CRTC8_IDX	DISPDEC:0x3B4 DISPDEC:0x3D4	2-196
CRTC8_DATA	DISPDEC:0x3B5 DISPDEC:0x3D5	2-171
CRTC8_DATA	DISPDEC:0x3B5 DISPDEC:0x3D5	2-196
GENFC_WT	DISPDEC:0x3BA DISPDEC:0x3DA	2-165
GENS1	DISPDEC:0x3BA DISPDEC:0x3DA	2-167
VGA_MEM_READ_PAGE_ADDR	DISPDEC:0x3C	2-197
ATTRDW	DISPDEC:0x3C0	2-181
ATTRX	DISPDEC:0x3C0	2-181
ATTRDR	DISPDEC:0x3C1	2-181
GENMO_WT	DISPDEC:0x3C2	2-165
GENMO_WT	DISPDEC:0x3C2	2-194
GENS0	DISPDEC:0x3C2	2-166

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
SEQ8_IDX	DISPDEC:0x3C4	2-170
SEQ8_IDX	DISPDEC:0x3C4	2-195
SEQ8_DATA	DISPDEC:0x3C5	2-170
SEQ8_DATA	DISPDEC:0x3C5	2-195
DAC_MASK	DISPDEC:0x3C6	2-168
DAC_R_INDEX	DISPDEC:0x3C7	2-168
DAC_W_INDEX	DISPDEC:0x3C8	2-168
DAC_DATA	DISPDEC:0x3C9	2-168
GENFC_RD	DISPDEC:0x3CA	2-165
GENMO_RD	DISPDEC:0x3CC	2-166
GENMO_RD	DISPDEC:0x3CC	2-195
GRPH8_IDX	DISPDEC:0x3CE	2-178
GRPH8_IDX	DISPDEC:0x3CE	2-196
GRPH8_DATA	DISPDEC:0x3CF	2-178
GRPH8_DATA	DISPDEC:0x3CF	2-196
D1CRTC_H_TOTAL	DISPDEC:0x6000	2-267
D1CRTC_H_BLANK_START_END	DISPDEC:0x6004	2-267
D1CRTC_H_SYNC_A	DISPDEC:0x6008	2-267
D1CRTC_H_SYNC_A_CNTL	DISPDEC:0x600C	2-267
D1CRTC_H_SYNC_B	DISPDEC:0x6010	2-268
D1CRTC_H_SYNC_B_CNTL	DISPDEC:0x6014	2-268
D1CRTC_V_TOTAL	DISPDEC:0x6020	2-268
D1CRTC_V_BLANK_START_END	DISPDEC:0x6024	2-268
D1CRTC_V_SYNC_A	DISPDEC:0x6028	2-269
D1CRTC_V_SYNC_A_CNTL	DISPDEC:0x602C	2-269
D1CRTC_V_SYNC_B	DISPDEC:0x6030	2-269
D1CRTC_V_SYNC_B_CNTL	DISPDEC:0x6034	2-269
D1CRTC_TRIGA_CNTL	DISPDEC:0x6060	2-270
D1CRTC_TRIGA_MANUAL_TRIG	DISPDEC:0x6064	2-271
D1CRTC_TRIGB_CNTL	DISPDEC:0x6068	2-271
D1CRTC_TRIGB_MANUAL_TRIG	DISPDEC:0x606C	2-272
D1CRTC_FORCE_COUNT_NOW_CNTL	DISPDEC:0x6070	2-272
D1CRTC_FLOW_CONTROL	DISPDEC:0x6074	2-272
D1CRTC_PIXEL_DATA_READBACK	DISPDEC:0x6078	2-273
D1CRTC_STEREO_FORCE_NEXT_EYE	DISPDEC:0x607C	2-273
D1CRTC_CONTROL	DISPDEC:0x6080	2-273
D1CRTC_BLANK_CONTROL	DISPDEC:0x6084	2-274
D1CRTC_INTERLACE_CONTROL	DISPDEC:0x6088	2-274
D1CRTC_INTERLACE_STATUS	DISPDEC:0x608C	2-274
D1CRTC_BLANK_DATA_COLOR	DISPDEC:0x6090	2-275

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
D1CRTC_OVERSCAN_COLOR	DISPDEC:0x6094	2-275
D1CRTC_BLACK_COLOR	DISPDEC:0x6098	2-275
D1CRTC_STATUS	DISPDEC:0x609C	2-275
D1CRTC_STATUS_POSITION	DISPDEC:0x60A0	2-276
D1CRTC_STATUS_FRAME_COUNT	DISPDEC:0x60A4	2-276
D1CRTC_STATUS_VF_COUNT	DISPDEC:0x60A8	2-276
D1CRTC_STATUS_HV_COUNT	DISPDEC:0x60AC	2-276
D1CRTC_COUNT_RESET	DISPDEC:0x60B0	2-276
D1CRTC_COUNT_CONTROL	DISPDEC:0x60B4	2-276
D1CRTC_MANUAL_FORCE_VSYNC_NEXT_LINE	DISPDEC:0x60B8	2-276
D1CRTC_VERT_SYNC_CONTROL	DISPDEC:0x60BC	2-277
D1CRTC_STEREO_STATUS	DISPDEC:0x60C0	2-277
D1CRTC_STEREO_CONTROL	DISPDEC:0x60C4	2-277
D1CRTC_SNAPSHOT_STATUS	DISPDEC:0x60C8	2-278
D1CRTC_SNAPSHOT_CONTROL	DISPDEC:0x60CC	2-278
D1CRTC_SNAPSHOT_POSITION	DISPDEC:0x60D0	2-278
D1CRTC_SNAPSHOT_FRAME	DISPDEC:0x60D4	2-278
D1CRTC_START_LINE_CONTROL	DISPDEC:0x60D8	2-278
D1CRTC_INTERRUPT_CONTROL	DISPDEC:0x60DC	2-278
D1MODE_MASTER_UPDATE_LOCK	DISPDEC:0x60E0	2-279
D1MODE_MASTER_UPDATE_MODE	DISPDEC:0x60E4	2-279
D1CRTC_UPDATE_LOCK	DISPDEC:0x60E8	2-279
D1CRTC_DOUBLE_BUFFER_CONTROL	DISPDEC:0x60EC	2-280
D1CRTC_VGA_PARAMETER_CAPTURE_MODE	DISPDEC:0x60F0	2-280
DC_CRTC_MASTER_EN	DISPDEC:0x60F8	2-280
DC_CRTC_TV_CONTROL	DISPDEC:0x60FC	2-280
D1GRPH_ENABLE	DISPDEC:0x6100	2-198
D1GRPH_CONTROL	DISPDEC:0x6104	2-198
D1GRPH_LUT_SEL	DISPDEC:0x6108	2-199
D1GRPH_PRIMARY_SURFACE_ADDRESS	DISPDEC:0x6110	2-199
D1GRPH_SECONDARY_SURFACE_ADDRESS	DISPDEC:0x6118	2-200
D1GRPH_PITCH	DISPDEC:0x6120	2-200
D1GRPH_SURFACE_OFFSET_X	DISPDEC:0x6124	2-200
D1GRPH_SURFACE_OFFSET_Y	DISPDEC:0x6128	2-200
D1GRPH_X_START	DISPDEC:0x612C	2-200
D1GRPH_Y_START	DISPDEC:0x6130	2-201
D1GRPH_X_END	DISPDEC:0x6134	2-201
D1GRPH_Y_END	DISPDEC:0x6138	2-201
D1COLOR_SPACE_CONVERT	DISPDEC:0x613C	2-221
D1OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	DISPDEC:0x6140	2-217

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
D1GRPH_UPDATE	DISPDEC:0x6144	2-201
D1GRPH_FLIP_CONTROL	DISPDEC:0x6148	2-202
D1GRPH_SURFACE_ADDRESS_INUSE	DISPDEC:0x614C	2-202
D1OVL_ENABLE	DISPDEC:0x6180	2-203
D1OVL_CONTROL1	DISPDEC:0x6184	2-203
D1OVL_CONTROL2	DISPDEC:0x6188	2-203
D1OVL_SURFACE_ADDRESS	DISPDEC:0x6190	2-204
D1OVL_PITCH	DISPDEC:0x6198	2-204
D1OVL_SURFACE_OFFSET_X	DISPDEC:0x619C	2-204
D1OVL_SURFACE_OFFSET_Y	DISPDEC:0x61A0	2-204
D1OVL_START	DISPDEC:0x61A4	2-204
D1OVL_END	DISPDEC:0x61A8	2-205
D1OVL_UPDATE	DISPDEC:0x61AC	2-205
D1OVL_SURFACE_ADDRESS_INUSE	DISPDEC:0x61B0	2-205
D1OVL_MATRIX_TRANSFORM_EN	DISPDEC:0x6200	2-206
D1OVL_MATRIX_COEF_1_1	DISPDEC:0x6204	2-206
D1OVL_MATRIX_COEF_1_2	DISPDEC:0x6208	2-206
D1OVL_MATRIX_COEF_1_3	DISPDEC:0x620C	2-206
D1OVL_MATRIX_COEF_1_4	DISPDEC:0x6210	2-206
D1OVL_MATRIX_COEF_2_1	DISPDEC:0x6214	2-207
D1OVL_MATRIX_COEF_2_2	DISPDEC:0x6218	2-207
D1OVL_MATRIX_COEF_2_3	DISPDEC:0x621C	2-207
D1OVL_MATRIX_COEF_2_4	DISPDEC:0x6220	2-207
D1OVL_MATRIX_COEF_3_1	DISPDEC:0x6224	2-207
D1OVL_MATRIX_COEF_3_2	DISPDEC:0x6228	2-208
D1OVL_MATRIX_COEF_3_3	DISPDEC:0x622C	2-208
D1OVL_MATRIX_COEF_3_4	DISPDEC:0x6230	2-208
D1OVL_PWL_TRANSFORM_EN	DISPDEC:0x6280	2-209
D1OVL_PWL_0TOF	DISPDEC:0x6284	2-209
D1OVL_PWL_10TO1F	DISPDEC:0x6288	2-209
D1OVL_PWL_20TO3F	DISPDEC:0x628C	2-209
D1OVL_PWL_40TO7F	DISPDEC:0x6290	2-209
D1OVL_PWL_80TOBF	DISPDEC:0x6294	2-210
D1OVL_PWL_C0TOFF	DISPDEC:0x6298	2-210
D1OVL_PWL_100TO13F	DISPDEC:0x629C	2-210
D1OVL_PWL_140TO17F	DISPDEC:0x62A0	2-210
D1OVL_PWL_180TO1BF	DISPDEC:0x62A4	2-210
D1OVL_PWL_1C0TO1FF	DISPDEC:0x62A8	2-210
D1OVL_PWL_200TO23F	DISPDEC:0x62AC	2-211
D1OVL_PWL_240TO27F	DISPDEC:0x62B0	2-211

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
D1OVL_PWL_280TO2BF	DISPDEC:0x62B4	2-211
D1OVL_PWL_2C0TO2FF	DISPDEC:0x62B8	2-211
D1OVL_PWL_300TO33F	DISPDEC:0x62BC	2-211
D1OVL_PWL_340TO37F	DISPDEC:0x62C0	2-212
D1OVL_PWL_380TO3BF	DISPDEC:0x62C4	2-212
D1OVL_PWL_3C0TO3FF	DISPDEC:0x62C8	2-212
D1OVL_KEY_CONTROL	DISPDEC:0x6300	2-213
D1GRPH_ALPHA	DISPDEC:0x6304	2-213
D1OVL_ALPHA	DISPDEC:0x6308	2-213
D1OVL_ALPHA_CONTROL	DISPDEC:0x630C	2-214
D1GRPH_KEY_RANGE_RED	DISPDEC:0x6310	2-214
D1GRPH_KEY_RANGE_GREEN	DISPDEC:0x6314	2-214
D1GRPH_KEY_RANGE_BLUE	DISPDEC:0x6318	2-215
D1GRPH_KEY_RANGE_ALPHA	DISPDEC:0x631C	2-215
D1OVL_KEY_RANGE_RED_CR	DISPDEC:0x6320	2-215
D1OVL_KEY_RANGE_GREEN_Y	DISPDEC:0x6324	2-215
D1OVL_KEY_RANGE_BLUE_CB	DISPDEC:0x6328	2-216
D1OVL_KEY_ALPHA	DISPDEC:0x632C	2-216
D1GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL	DISPDEC:0x6380	2-217
D1COLOR_MATRIX_COEF_1_1	DISPDEC:0x6384	2-217
D1COLOR_MATRIX_COEF_1_2	DISPDEC:0x6388	2-217
D1COLOR_MATRIX_COEF_1_3	DISPDEC:0x638C	2-218
D1COLOR_MATRIX_COEF_1_4	DISPDEC:0x6390	2-218
D1COLOR_MATRIX_COEF_2_1	DISPDEC:0x6394	2-218
D1COLOR_MATRIX_COEF_2_2	DISPDEC:0x6398	2-218
D1COLOR_MATRIX_COEF_2_3	DISPDEC:0x639C	2-218
D1COLOR_MATRIX_COEF_2_4	DISPDEC:0x63A0	2-219
D1COLOR_MATRIX_COEF_3_1	DISPDEC:0x63A4	2-219
D1COLOR_MATRIX_COEF_3_2	DISPDEC:0x63A8	2-219
D1COLOR_MATRIX_COEF_3_3	DISPDEC:0x63AC	2-219
D1COLOR_MATRIX_COEF_3_4	DISPDEC:0x63B0	2-220
D1CUR_CONTROL	DISPDEC:0x6400	2-222
D1CUR_SURFACE_ADDRESS	DISPDEC:0x6408	2-222
D1CUR_SIZE	DISPDEC:0x6410	2-222
D1CUR_POSITION	DISPDEC:0x6414	2-222
D1CUR_HOT_SPOT	DISPDEC:0x6418	2-223
D1CUR_COLOR1	DISPDEC:0x641C	2-223
D1CUR_COLOR2	DISPDEC:0x6420	2-223
D1CUR_UPDATE	DISPDEC:0x6424	2-223
D1ICON_CONTROL	DISPDEC:0x6440	2-224

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
D1ICON_SURFACE_ADDRESS	DISPDEC:0x6448	2-224
D1ICON_SIZE	DISPDEC:0x6450	2-224
D1ICON_START_POSITION	DISPDEC:0x6454	2-224
D1ICON_COLOR1	DISPDEC:0x6458	2-224
D1ICON_COLOR2	DISPDEC:0x645C	2-225
D1ICON_UPDATE	DISPDEC:0x6460	2-225
DC_LUT_RW_SELECT	DISPDEC:0x6480	2-226
DC_LUT_RW_MODE	DISPDEC:0x6484	2-226
DC_LUT_RW_INDEX	DISPDEC:0x6488	2-226
DC_LUT_SEQ_COLOR	DISPDEC:0x648C	2-226
DC_LUT_PWL_DATA	DISPDEC:0x6490	2-226
DC_LUT_30_COLOR	DISPDEC:0x6494	2-227
DC_LUT_READ_PIPE_SELECT	DISPDEC:0x6498	2-227
DC_LUT_WRITE_EN_MASK	DISPDEC:0x649C	2-227
DC_LUT_AUTOFILL	DISPDEC:0x64A0	2-227
DC_LUTA_CONTROL	DISPDEC:0x64C0	2-228
DC_LUTA_BLACK_OFFSET_BLUE	DISPDEC:0x64C4	2-229
DC_LUTA_BLACK_OFFSET_GREEN	DISPDEC:0x64C8	2-229
DC_LUTA_BLACK_OFFSET_RED	DISPDEC:0x64CC	2-229
DC_LUTA_WHITE_OFFSET_BLUE	DISPDEC:0x64D0	2-230
DC_LUTA_WHITE_OFFSET_GREEN	DISPDEC:0x64D4	2-230
DC_LUTA_WHITE_OFFSET_RED	DISPDEC:0x64D8	2-230
D2CRTC_H_TOTAL	DISPDEC:0x6800	2-280
D2CRTC_H_BLANK_START_END	DISPDEC:0x6804	2-281
D2CRTC_H_SYNC_A	DISPDEC:0x6808	2-281
D2CRTC_H_SYNC_A_CNTL	DISPDEC:0x680C	2-281
D2CRTC_H_SYNC_B	DISPDEC:0x6810	2-281
D2CRTC_H_SYNC_B_CNTL	DISPDEC:0x6814	2-282
D2CRTC_V_TOTAL	DISPDEC:0x6820	2-282
D2CRTC_V_BLANK_START_END	DISPDEC:0x6824	2-282
D2CRTC_V_SYNC_A	DISPDEC:0x6828	2-282
D2CRTC_V_SYNC_A_CNTL	DISPDEC:0x682C	2-283
D2CRTC_V_SYNC_B	DISPDEC:0x6830	2-283
D2CRTC_V_SYNC_B_CNTL	DISPDEC:0x6834	2-283
D2CRTC_TRIGA_CNTL	DISPDEC:0x6860	2-283
D2CRTC_TRIGA_MANUAL_TRIG	DISPDEC:0x6864	2-284
D2CRTC_TRIGB_CNTL	DISPDEC:0x6868	2-285
D2CRTC_TRIGB_MANUAL_TRIG	DISPDEC:0x686C	2-286
D2CRTC_FORCE_COUNT_NOW_CNTL	DISPDEC:0x6870	2-286
D2CRTC_FLOW_CONTROL	DISPDEC:0x6874	2-286

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
D2CRTC_PIXEL_DATA_READBACK	*DISPDEC:0x6878*	*2-287*
D2CRTC_STEREO_FORCE_NEXT_EYE	*DISPDEC:0x687C*	*2-287*
D2CRTC_CONTROL	*DISPDEC:0x6880*	*2-287*
D2CRTC_BLANK_CONTROL	*DISPDEC:0x6884*	*2-287*
D2CRTC_INTERLACE_CONTROL	*DISPDEC:0x6888*	*2-288*
D2CRTC_INTERLACE_STATUS	*DISPDEC:0x688C*	*2-288*
D2CRTC_BLANK_DATA_COLOR	*DISPDEC:0x6890*	*2-288*
D2CRTC_OVERSCAN_COLOR	*DISPDEC:0x6894*	*2-288*
D2CRTC_BLACK_COLOR	*DISPDEC:0x6898*	*2-289*
D2CRTC_STATUS	*DISPDEC:0x689C*	*2-289*
D2CRTC_STATUS_POSITION	*DISPDEC:0x68A0*	*2-289*
D2CRTC_STATUS_FRAME_COUNT	*DISPDEC:0x68A4*	*2-290*
D2CRTC_STATUS_VF_COUNT	*DISPDEC:0x68A8*	*2-290*
D2CRTC_STATUS_HV_COUNT	*DISPDEC:0x68AC*	*2-290*
D2CRTC_COUNT_RESET	*DISPDEC:0x68B0*	*2-290*
D2CRTC_COUNT_CONTROL	*DISPDEC:0x68B4*	*2-290*
D2CRTC_MANUAL_FORCE_VSYNC_NEXT_LINE	*DISPDEC:0x68B8*	*2-290*
D2CRTC_VERT_SYNC_CONTROL	*DISPDEC:0x68BC*	*2-290*
D2CRTC_STEREO_STATUS	*DISPDEC:0x68C0*	*2-291*
D2CRTC_STEREO_CONTROL	*DISPDEC:0x68C4*	*2-291*
D2CRTC_SNAPSHOT_STATUS	*DISPDEC:0x68C8*	*2-291*
D2CRTC_SNAPSHOT_CONTROL	*DISPDEC:0x68CC*	*2-292*
D2CRTC_SNAPSHOT_POSITION	*DISPDEC:0x68D0*	*2-292*
D2CRTC_SNAPSHOT_FRAME	*DISPDEC:0x68D4*	*2-292*
D2CRTC_START_LINE_CONTROL	*DISPDEC:0x68D8*	*2-292*
D2CRTC_INTERRUPT_CONTROL	*DISPDEC:0x68DC*	*2-292*
D2MODE_MASTER_UPDATE_LOCK	*DISPDEC:0x68E0*	*2-293*
D2MODE_MASTER_UPDATE_MODE	*DISPDEC:0x68E4*	*2-293*
D2CRTC_UPDATE_LOCK	*DISPDEC:0x68E8*	*2-293*
D2CRTC_DOUBLE_BUFFER_CONTROL	*DISPDEC:0x68EC*	*2-293*
D2CRTC_VGA_PARAMETER_CAPTURE_MODE	*DISPDEC:0x68F0*	*2-294*
D2GRPH_ENABLE	*DISPDEC:0x6900*	*2-231*
D2GRPH_CONTROL	*DISPDEC:0x6904*	*2-231*
D2GRPH_LUT_SEL	*DISPDEC:0x6908*	*2-232*
D2GRPH_PRIMARY_SURFACE_ADDRESS	*DISPDEC:0x6910*	*2-232*
D2GRPH_SECONDARY_SURFACE_ADDRESS	*DISPDEC:0x6918*	*2-233*
D2GRPH_PITCH	*DISPDEC:0x6920*	*2-233*
D2GRPH_SURFACE_OFFSET_X	*DISPDEC:0x6924*	*2-233*
D2GRPH_SURFACE_OFFSET_Y	*DISPDEC:0x6928*	*2-233*
D2GRPH_X_START	*DISPDEC:0x692C*	*2-233*

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
D2GRPH_Y_START	DISPDEC:0x6930	2-234
D2GRPH_X_END	DISPDEC:0x6934	2-234
D2GRPH_Y_END	DISPDEC:0x6938	2-234
D2COLOR_SPACE_CONVERT	DISPDEC:0x693C	2-254
D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	DISPDEC:0x6940	2-250
D2GRPH_UPDATE	DISPDEC:0x6944	2-234
D2GRPH_FLIP_CONTROL	DISPDEC:0x6948	2-235
D2GRPH_SURFACE_ADDRESS_INUSE	DISPDEC:0x694C	2-235
D2OVL_ENABLE	DISPDEC:0x6980	2-236
D2OVL_CONTROL1	DISPDEC:0x6984	2-236
D2OVL_CONTROL2	DISPDEC:0x6988	2-236
D2OVL_SURFACE_ADDRESS	DISPDEC:0x6990	2-237
D2OVL_PITCH	DISPDEC:0x6998	2-237
D2OVL_SURFACE_OFFSET_X	DISPDEC:0x699C	2-237
D2OVL_SURFACE_OFFSET_Y	DISPDEC:0x69A0	2-237
D2OVL_START	DISPDEC:0x69A4	2-237
D2OVL_END	DISPDEC:0x69A8	2-238
D2OVL_UPDATE	DISPDEC:0x69AC	2-238
D2OVL_SURFACE_ADDRESS_INUSE	DISPDEC:0x69B0	2-238
D2OVL_MATRIX_TRANSFORM_EN	DISPDEC:0x6A00	2-239
D2OVL_MATRIX_COEF_1_1	DISPDEC:0x6A04	2-239
D2OVL_MATRIX_COEF_1_2	DISPDEC:0x6A08	2-239
D2OVL_MATRIX_COEF_1_3	DISPDEC:0x6A0C	2-239
D2OVL_MATRIX_COEF_1_4	DISPDEC:0x6A10	2-239
D2OVL_MATRIX_COEF_2_1	DISPDEC:0x6A14	2-240
D2OVL_MATRIX_COEF_2_2	DISPDEC:0x6A18	2-240
D2OVL_MATRIX_COEF_2_3	DISPDEC:0x6A1C	2-240
D2OVL_MATRIX_COEF_2_4	DISPDEC:0x6A20	2-240
D2OVL_MATRIX_COEF_3_1	DISPDEC:0x6A24	2-240
D2OVL_MATRIX_COEF_3_2	DISPDEC:0x6A28	2-241
D2OVL_MATRIX_COEF_3_3	DISPDEC:0x6A2C	2-241
D2OVL_MATRIX_COEF_3_4	DISPDEC:0x6A30	2-241
D2OVL_PWL_TRANSFORM_EN	DISPDEC:0x6A80	2-242
D2OVL_PWL_0TOF	DISPDEC:0x6A84	2-242
D2OVL_PWL_10TO1F	DISPDEC:0x6A88	2-242
D2OVL_PWL_20TO3F	DISPDEC:0x6A8C	2-242
D2OVL_PWL_40TO7F	DISPDEC:0x6A90	2-242
D2OVL_PWL_80TOBF	DISPDEC:0x6A94	2-243
D2OVL_PWL_C0TOFF	DISPDEC:0x6A98	2-243
D2OVL_PWL_100TO13F	DISPDEC:0x6A9C	2-243

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
D2OVL_PWL_140TO17F	DISPDEC:0x6AA0	2-243
D2OVL_PWL_180TO1BF	DISPDEC:0x6AA4	2-243
D2OVL_PWL_1C0TO1FF	DISPDEC:0x6AA8	2-243
D2OVL_PWL_200TO23F	DISPDEC:0x6AAC	2-244
D2OVL_PWL_240TO27F	DISPDEC:0x6AB0	2-244
D2OVL_PWL_280TO2BF	DISPDEC:0x6AB4	2-244
D2OVL_PWL_2C0TO2FF	DISPDEC:0x6AB8	2-244
D2OVL_PWL_300TO33F	DISPDEC:0x6ABC	2-244
D2OVL_PWL_340TO37F	DISPDEC:0x6AC0	2-245
D2OVL_PWL_380TO3BF	DISPDEC:0x6AC4	2-245
D2OVL_PWL_3C0TO3FF	DISPDEC:0x6AC8	2-245
D2OVL_KEY_CONTROL	DISPDEC:0x6B00	2-246
D2GRPH_ALPHA	DISPDEC:0x6B04	2-246
D2OVL_ALPHA	DISPDEC:0x6B08	2-246
D2OVL_ALPHA_CONTROL	DISPDEC:0x6B0C	2-247
D2GRPH_KEY_RANGE_RED	DISPDEC:0x6B10	2-247
D2GRPH_KEY_RANGE_GREEN	DISPDEC:0x6B14	2-247
D2GRPH_KEY_RANGE_BLUE	DISPDEC:0x6B18	2-248
D2GRPH_KEY_RANGE_ALPHA	DISPDEC:0x6B1C	2-248
D2OVL_KEY_RANGE_RED_CR	DISPDEC:0x6B20	2-248
D2OVL_KEY_RANGE_GREEN_Y	DISPDEC:0x6B24	2-248
D2OVL_KEY_RANGE_BLUE_CB	DISPDEC:0x6B28	2-248
D2OVL_KEY_ALPHA	DISPDEC:0x6B2C	2-249
D2GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL	DISPDEC:0x6B80	2-250
D2COLOR_MATRIX_COEF_1_1	DISPDEC:0x6B84	2-250
D2COLOR_MATRIX_COEF_1_2	DISPDEC:0x6B88	2-250
D2COLOR_MATRIX_COEF_1_3	DISPDEC:0x6B8C	2-250
D2COLOR_MATRIX_COEF_1_4	DISPDEC:0x6B90	2-251
D2COLOR_MATRIX_COEF_2_1	DISPDEC:0x6B94	2-251
D2COLOR_MATRIX_COEF_2_2	DISPDEC:0x6B98	2-251
D2COLOR_MATRIX_COEF_2_3	DISPDEC:0x6B9C	2-251
D2COLOR_MATRIX_COEF_2_4	DISPDEC:0x6BA0	2-252
D2COLOR_MATRIX_COEF_3_1	DISPDEC:0x6BA4	2-252
D2COLOR_MATRIX_COEF_3_2	DISPDEC:0x6BA8	2-252
D2COLOR_MATRIX_COEF_3_3	DISPDEC:0x6BAC	2-252
D2COLOR_MATRIX_COEF_3_4	DISPDEC:0x6BB0	2-253
D2CUR_CONTROL	DISPDEC:0x6C00	2-255
D2CUR_SURFACE_ADDRESS	DISPDEC:0x6C08	2-255
D2CUR_SIZE	DISPDEC:0x6C10	2-255
D2CUR_POSITION	DISPDEC:0x6C14	2-255

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
D2CUR_HOT_SPOT	DISPDEC:0x6C18	2-256
D2CUR_COLOR1	DISPDEC:0x6C1C	2-256
D2CUR_COLOR2	DISPDEC:0x6C20	2-256
D2CUR_UPDATE	DISPDEC:0x6C24	2-256
D2ICON_CONTROL	DISPDEC:0x6C40	2-257
D2ICON_SURFACE_ADDRESS	DISPDEC:0x6C48	2-257
D2ICON_SIZE	DISPDEC:0x6C50	2-257
D2ICON_START_POSITION	DISPDEC:0x6C54	2-257
D2ICON_COLOR1	DISPDEC:0x6C58	2-257
D2ICON_COLOR2	DISPDEC:0x6C5C	2-258
D2ICON_UPDATE	DISPDEC:0x6C60	2-258
DCP_CRC_CONTROL	DISPDEC:0x6C80	2-262
DCP_CRC_MASK	DISPDEC:0x6C84	2-262
DCP_CRC_P0_CURRENT	DISPDEC:0x6C88	2-262
DCP_CRC_P1_CURRENT	DISPDEC:0x6C8C	2-262
DCP_CRC_P0_LAST	DISPDEC:0x6C90	2-262
DCP_CRC_P1_LAST	DISPDEC:0x6C94	2-263
DMIF_CONTROL	DISPDEC:0x6CB0	2-264
DMIF_STATUS	DISPDEC:0x6CB4	2-264
MCIF_CONTROL	DISPDEC:0x6CB8	2-265
DCP_LB_DATA_GAP_BETWEEN_CHUNK	DISPDEC:0x6CBC	2-266
DC_LUTB_CONTROL	DISPDEC:0x6CC0	2-259
DC_LUTB_BLACK_OFFSET_BLUE	DISPDEC:0x6CC4	2-260
DC_LUTB_BLACK_OFFSET_GREEN	DISPDEC:0x6CC8	2-260
DC_LUTB_BLACK_OFFSET_RED	DISPDEC:0x6CCC	2-260
DC_LUTB_WHITE_OFFSET_BLUE	DISPDEC:0x6CD0	2-261
DC_LUTB_WHITE_OFFSET_GREEN	DISPDEC:0x6CD4	2-261
DC_LUTB_WHITE_OFFSET_RED	DISPDEC:0x6CD8	2-261
DACA_ENABLE	DISPDEC:0x7800	2-295
DACA_SOURCE_SELECT	DISPDEC:0x7804	2-295
DACA_CRC_EN	DISPDEC:0x7808	2-295
DACA_CRC_CONTROL	DISPDEC:0x780C	2-295
DACA_CRC_SIG_RGB_MASK	DISPDEC:0x7810	2-295
DACA_CRC_SIG_CONTROL_MASK	DISPDEC:0x7814	2-296
DACA_CRC_SIG_RGB	DISPDEC:0x7818	2-296
DACA_CRC_SIG_CONTROL	DISPDEC:0x781C	2-296
DACA_SYNC_TRISTATE_CONTROL	DISPDEC:0x7820	2-296
DACA_SYNC_SELECT	DISPDEC:0x7824	2-296
DACA_AUTODETECT_CONTROL	DISPDEC:0x7828	2-297
DACA_AUTODETECT_CONTROL2	DISPDEC:0x782C	2-297

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
DACA_AUTODETECT_STATUS	DISPDEC:0x7834	2-297
DACA_AUTODETECT_INT_CONTROL	DISPDEC:0x7838	2-298
DACA_FORCE_OUTPUT_CNTL	DISPDEC:0x783C	2-298
DACA_FORCE_DATA	DISPDEC:0x7840	2-298
DACA_POWERDOWN	DISPDEC:0x7850	2-298
DACA_CONTROL1	DISPDEC:0x7854	2-298
DACA_CONTROL2	DISPDEC:0x7858	2-299
DACA_COMPARATOR_ENABLE	DISPDEC:0x785C	2-299
DACA_COMPARATOR_OUTPUT	DISPDEC:0x7860	2-300
DACA_TEST_ENABLE	DISPDEC:0x7864	2-300
DACA_PWR_CNTL	DISPDEC:0x7868	2-300
TMDSA_CNTL	DISPDEC:0x7880	2-306
TMDSA_SOURCE_SELECT	DISPDEC:0x7884	2-306
TMDSA_COLOR_FORMAT	DISPDEC:0x7888	2-307
TMDSA_FORCE_OUTPUT_CNTL	DISPDEC:0x788C	2-307
TMDSA_FORCE_DATA	DISPDEC:0x7890	2-307
TMDSA_BIT_DEPTH_CONTROL	DISPDEC:0x7894	2-307
TMDSA_CONTROL_CHAR	DISPDEC:0x7898	2-308
TMDSA_CONTROL0_FEEDBACK	DISPDEC:0x789C	2-308
TMDSA_STEREOSYNC_CTL_SEL	DISPDEC:0x78A0	2-308
TMDSA_SYNC_CHAR_PATTERN_SEL	DISPDEC:0x78A4	2-308
TMDSA_SYNC_CHAR_PATTERN_0_1	DISPDEC:0x78A8	2-308
TMDSA_SYNC_CHAR_PATTERN_2_3	DISPDEC:0x78AC	2-309
TMDSA_CRC_CNTL	DISPDEC:0x78B0	2-309
TMDSA_CRC_SIG_MASK	DISPDEC:0x78B4	2-309
TMDSA_CRC_SIG_RGB	DISPDEC:0x78B8	2-309
TMDSA_2ND_CRC_RESULT	DISPDEC:0x78BC	2-310
TMDSA_TEST_PATTERN	DISPDEC:0x78C0	2-310
TMDSA_RANDOM_PATTERN_SEED	DISPDEC:0x78C4	2-310
TMDSA_DEBUG	DISPDEC:0x78C8	2-311
TMDSA_CTL_BITS	DISPDEC:0x78CC	2-311
TMDSA_DCBALANCER_CONTROL	DISPDEC:0x78D0	2-311
TMDSA_RED_BLUE_SWITCH	DISPDEC:0x78D4	2-311
TMDSA_DATA_SYNCHRONIZATION	DISPDEC:0x78D8	2-311
TMDSA_CTL0_1_GEN_CNTL	DISPDEC:0x78DC	2-312
TMDSA_CTL2_3_GEN_CNTL	DISPDEC:0x78E0	2-313
TMDSA_TRANSMITTER_ENABLE	DISPDEC:0x7904	2-314
TMDSA_LOAD_DETECT	DISPDEC:0x7908	2-315
TMDSA_MACRO_CONTROL	DISPDEC:0x790C	2-315
TMDSA_TRANSMITTER_CONTROL	DISPDEC:0x7910	2-315

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
TMDSA_REG_TEST_OUTPUT	DISPDEC:0x7914	2-316
TMDSA_TRANSMITTER_DEBUG	DISPDEC:0x7918	2-316
DVOA_ENABLE	DISPDEC:0x7980	2-316
DVOA_SOURCE_SELECT	DISPDEC:0x7984	2-317
DVOA_BIT_DEPTH_CONTROL	DISPDEC:0x7988	2-317
DVOA_OUTPUT	DISPDEC:0x798C	2-317
DVOA_CONTROL	DISPDEC:0x7990	2-318
DVOA_CRC_EN	DISPDEC:0x7994	2-318
DVOA_CRC_CONTROL	DISPDEC:0x7998	2-318
DVOA_CRC_SIG_MASK1	DISPDEC:0x799C	2-319
DVOA_CRC_SIG_MASK2	DISPDEC:0x79A0	2-319
DVOA_CRC_SIG_RESULT1	DISPDEC:0x79A4	2-319
DVOA_CRC_SIG_RESULT2	DISPDEC:0x79A8	2-319
DVOA_CRC2_SIG_MASK	DISPDEC:0x79AC	2-319
DVOA_CRC2_SIG_RESULT	DISPDEC:0x79B0	2-319
DVOA_STRENGTH_CONTROL	DISPDEC:0x79B4	2-320
DVOA_FORCE_OUTPUT_CNTL	DISPDEC:0x79B8	2-320
DVOA_FORCE_DATA	DISPDEC:0x79BC	2-320
DACB_ENABLE	DISPDEC:0x7A00	2-300
DACB_SOURCE_SELECT	DISPDEC:0x7A04	2-300
DACB_CRC_EN	DISPDEC:0x7A08	2-301
DACB_CRC_CONTROL	DISPDEC:0x7A0C	2-301
DACB_CRC_SIG_RGB_MASK	DISPDEC:0x7A10	2-301
DACB_CRC_SIG_CONTROL_MASK	DISPDEC:0x7A14	2-301
DACB_CRC_SIG_RGB	DISPDEC:0x7A18	2-301
DACB_CRC_SIG_CONTROL	DISPDEC:0x7A1C	2-302
DACB_SYNC_TRISTATE_CONTROL	DISPDEC:0x7A20	2-302
DACB_SYNC_SELECT	DISPDEC:0x7A24	2-302
DACB_AUTODETECT_CONTROL	DISPDEC:0x7A28	2-302
DACB_AUTODETECT_CONTROL2	DISPDEC:0x7A2C	2-302
DACB_AUTODETECT_STATUS	DISPDEC:0x7A34	2-303
DACB_AUTODETECT_INT_CONTROL	DISPDEC:0x7A38	2-303
DACB_FORCE_OUTPUT_CNTL	DISPDEC:0x7A3C	2-303
DACB_FORCE_DATA	DISPDEC:0x7A40	2-304
DACB_POWERDOWN	DISPDEC:0x7A50	2-304
DACB_CONTROL1	DISPDEC:0x7A54	2-304
DACB_CONTROL2	DISPDEC:0x7A58	2-304
DACB_COMPARATOR_ENABLE	DISPDEC:0x7A5C	2-305
DACB_COMPARATOR_OUTPUT	DISPDEC:0x7A60	2-305
DACB_TEST_ENABLE	DISPDEC:0x7A64	2-305

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
DACB_PWR_CNTL	DISPDEC:0x7A68	2-306
LVTMA_CNTL	DISPDEC:0x7A80	2-340
LVTMA_SOURCE_SELECT	DISPDEC:0x7A84	2-340
LVTMA_COLOR_FORMAT	DISPDEC:0x7A88	2-341
LVTMA_FORCE_OUTPUT_CNTL	DISPDEC:0x7A8C	2-341
LVTMA_FORCE_DATA	DISPDEC:0x7A90	2-341
LVTMA_BIT_DEPTH_CONTROL	DISPDEC:0x7A94	2-341
LVTMA_CONTROL_CHAR	DISPDEC:0x7A98	2-342
LVTMA_CONTROL0_FEEDBACK	DISPDEC:0x7A9C	2-342
LVTMA_STEREOSYNC_CTL_SEL	DISPDEC:0x7AA0	2-342
LVTMA_SYNC_CHAR_PATTERN_SEL	DISPDEC:0x7AA4	2-342
LVTMA_SYNC_CHAR_PATTERN_0_1	DISPDEC:0x7AA8	2-342
LVTMA_SYNC_CHAR_PATTERN_2_3	DISPDEC:0x7AAC	2-343
LVTMA_CRC_CNTL	DISPDEC:0x7AB0	2-343
LVTMA_CRC_SIG_MASK	DISPDEC:0x7AB4	2-343
LVTMA_CRC_SIG_RGB	DISPDEC:0x7AB8	2-344
LVTMA_2ND_CRC_RESULT	DISPDEC:0x7ABC	2-344
LVTMA_TEST_PATTERN	DISPDEC:0x7AC0	2-344
LVTMA_RANDOM_PATTERN_SEED	DISPDEC:0x7AC4	2-345
LVTMA_DEBUG	DISPDEC:0x7AC8	2-345
LVTMA_CTL_BITS	DISPDEC:0x7ACC	2-345
LVTMA_DCBALANCER_CONTROL	DISPDEC:0x7AD0	2-345
LVTMA_RED_BLUE_SWITCH	DISPDEC:0x7AD4	2-345
LVTMA_DATA_SYNCHRONIZATION	DISPDEC:0x7AD8	2-346
LVTMA_CTL0_1_GEN_CNTL	DISPDEC:0x7ADC	2-346
LVTMA_CTL2_3_GEN_CNTL	DISPDEC:0x7AE0	2-347
LVTMA_PWRSEQ_REF_DIV	DISPDEC:0x7AE4	2-348
LVTMA_PWRSEQ_DELAY1	DISPDEC:0x7AE8	2-348
LVTMA_PWRSEQ_DELAY2	DISPDEC:0x7AEC	2-349
LVTMA_PWRSEQ_CNTL	DISPDEC:0x7AF0	2-349
LVTMA_PWRSEQ_STATE	DISPDEC:0x7AF4	2-350
LVTMA_BL_MOD_CNTL	DISPDEC:0x7AF8	2-350
LVTMA_LVDS_DATA_CNTL	DISPDEC:0x7AFC	2-351
LVTMA_MODE	DISPDEC:0x7B00	2-351
LVTMA_TRANSMITTER_ENABLE	DISPDEC:0x7B04	2-351
LVTMA_LOAD_DETECT	DISPDEC:0x7B08	2-352
LVTMA_MACRO_CONTROL	DISPDEC:0x7B0C	2-352
LVTMA_TRANSMITTER_CONTROL	DISPDEC:0x7B10	2-353
LVTMA_REG_TEST_OUTPUT	DISPDEC:0x7B14	2-354
LVTMA_TRANSMITTER_DEBUG	DISPDEC:0x7B18	2-354

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
DC_HOT_PLUG_DETECT1_CONTROL	DISPDEC:0x7D00	2-320
DC_HOT_PLUG_DETECT1_INT_STATUS	DISPDEC:0x7D04	2-321
DC_HOT_PLUG_DETECT1_INT_CONTROL	DISPDEC:0x7D08	2-321
DC_HOT_PLUG_DETECT2_CONTROL	DISPDEC:0x7D10	2-321
DC_HOT_PLUG_DETECT2_INT_STATUS	DISPDEC:0x7D14	2-321
DC_HOT_PLUG_DETECT2_INT_CONTROL	DISPDEC:0x7D18	2-321
DC_HOT_PLUG_DETECT_CLOCK_CONTROL	DISPDEC:0x7D20	2-322
DC_I2C_STATUS1	DISPDEC:0x7D30	2-322
DC_I2C_RESET	DISPDEC:0x7D34	2-322
DC_I2C_CONTROL1	DISPDEC:0x7D38	2-322
DC_I2C_CONTROL2	DISPDEC:0x7D3C	2-323
DC_I2C_CONTROL3	DISPDEC:0x7D40	2-323
DC_I2C_DATA	DISPDEC:0x7D44	2-323
DC_I2C_INTERRUPT_CONTROL	DISPDEC:0x7D48	2-323
DC_I2C_ARBITRATION	DISPDEC:0x7D50	2-324
DC_GENERICA	DISPDEC:0x7DC0	2-324
DC_GENERICB	DISPDEC:0x7DC4	2-325
DC_PAD_EXTERN_SIG	DISPDEC:0x7DCC	2-325
DC_REF_CLK_CNTL	DISPDEC:0x7DD4	2-325
DC_GPIO_GENERIC_MASK	DISPDEC:0x7DE0	2-326
DC_GPIO_GENERIC_A	DISPDEC:0x7DE4	2-326
DC_GPIO_GENERIC_EN	DISPDEC:0x7DE8	2-326
DC_GPIO_GENERIC_Y	DISPDEC:0x7DEC	2-326
DC_GPIO_VIP_DEBUG	DISPDEC:0x7E2C	2-326
DC_GPIO_DVODATA_MASK	DISPDEC:0x7E30	2-327
DC_GPIO_DVODATA_A	DISPDEC:0x7E34	2-327
DC_GPIO_DVODATA_EN	DISPDEC:0x7E38	2-327
DC_GPIO_DVODATA_Y	DISPDEC:0x7E3C	2-327
DC_GPIO_DDC1_MASK	DISPDEC:0x7E40	2-328
DC_GPIO_DDC1_A	DISPDEC:0x7E44	2-328
DC_GPIO_DDC1_EN	DISPDEC:0x7E48	2-328
DC_GPIO_DDC1_Y	DISPDEC:0x7E4C	2-328
DC_GPIO_DDC2_MASK	DISPDEC:0x7E50	2-328
DC_GPIO_DDC2_A	DISPDEC:0x7E54	2-329
DC_GPIO_DDC2_EN	DISPDEC:0x7E58	2-329
DC_GPIO_DDC2_Y	DISPDEC:0x7E5C	2-329
DC_GPIO_DDC3_MASK	DISPDEC:0x7E60	2-329
DC_GPIO_DDC3_A	DISPDEC:0x7E64	2-329
DC_GPIO_DDC3_EN	DISPDEC:0x7E68	2-330
DC_GPIO_DDC3_Y	DISPDEC:0x7E6C	2-330

Table A-6 Display Registers Sorted by Address (Continued)

Register Name	Address	Page
DC_GPIO_SYNCA_MASK	DISPDEC:0x7E70	2-330
DC_GPIO_SYNCA_A	DISPDEC:0x7E74	2-330
DC_GPIO_SYNCA_EN	DISPDEC:0x7E78	2-330
DC_GPIO_SYNCA_Y	DISPDEC:0x7E7C	2-331
DC_GPIO_SYNCB_MASK	DISPDEC:0x7E80	2-331
DC_GPIO_SYNCB_A	DISPDEC:0x7E84	2-331
DC_GPIO_SYNCB_EN	DISPDEC:0x7E88	2-331
DC_GPIO_SYNCB_Y	DISPDEC:0x7E8C	2-331
DC_GPIO_HPD_MASK	DISPDEC:0x7E90	2-331
DC_GPIO_HPD_A	DISPDEC:0x7E94	2-332
DC_GPIO_HPD_EN	DISPDEC:0x7E98	2-332
DC_GPIO_HPD_Y	DISPDEC:0x7E9C	2-332
DC_GPIO_PWRSEQ_MASK	DISPDEC:0x7EA0	2-332
DC_GPIO_PWRSEQ_A	DISPDEC:0x7EA4	2-332
DC_GPIO_PWRSEQ_EN	DISPDEC:0x7EA8	2-333
DC_GPIO_PWRSEQ_Y	DISPDEC:0x7EAC	2-333
CAPTURE_START_STATUS	DISPDEC:0x7ED0	2-333
DC_GPIO_PAD_STRENGTH_1	DISPDEC:0x7ED4	2-334
DC_GPIO_PAD_STRENGTH_2	DISPDEC:0x7ED8	2-334
DISP_INTERRUPT_STATUS	DISPDEC:0x7EDC	2-335
DOUT_POWER_MANAGEMENT_CNTL	DISPDEC:0x7EE0	2-336
DISP_TIMER_CONTROL	DISPDEC:0x7EF0	2-337
DO_PERFCOUNTER0_SELECT	DISPDEC:0x7F00	2-338
DO_PERFCOUNTER0_HI	DISPDEC:0x7F04	2-338
DO_PERFCOUNTER0_LOW	DISPDEC:0x7F08	2-338
DO_PERFCOUNTER1_SELECT	DISPDEC:0x7F0C	2-338
DO_PERFCOUNTER1_HI	DISPDEC:0x7F10	2-338
DO_PERFCOUNTER1_LOW	DISPDEC:0x7F14	2-338
DCO_PERFMON_CNTL_R	DISPDEC:0x7F18	2-339
CRTC_EXT_CNTL	DISPDEC:0xE054	2-196

A.8 Host Interface Decode Space Registers Sorted by Name

Table A-7 Host Interface Decode Space Registers Sorted by Name

Register Name	Address	Page
BUS_CNTL	*HIDEC:0x4C*	*2-58*
CONFIG_APER_0_BASE	*HIDEC:0x100*	*2-59*
CONFIG_APER_1_BASE	*HIDEC:0x104*	*2-60*
CONFIG_APER_SIZE	*HIDEC:0x108*	*2-60*
CONFIG_CNTL	*HIDEC:0xE0*	*2-59*
CONFIG_MEMSIZE	*HIDEC:0xF8*	*2-59*
CONFIG_REG_1_BASE	*HIDEC:0x10C*	*2-60*
CONFIG_REG_APER_SIZE	*HIDEC:0x110*	*2-60*
GENENB	*HIDEC:0x3C3*	*2-58*
GENMO_RD	*HIDEC:0x3CC*	*2-106*
GENMO_WT	*HIDEC:0x3C2*	*2-106*
MM_DATA	*HIDEC:0x4*	*2-58*
MM_INDEX	*HIDEC:0x0*	*2-58*
MSI_REARM_EN	*HIDEC:0x160*	*2-60*
PCIE_DATA	*HIDEC:0x38*	*2-106*
PCIE_DATA	*HIDEC:0x38*	*2-115*
PCIE_INDEX	*HIDEC:0x30*	*2-106*
PCIE_INDEX	*HIDEC:0x30*	*2-114*

A.9 Memory Controller Registers Sorted By Name

Table A-8 Memory Controller Registers Sorted by Name

Register Name	Address	Page
AGP_BASE	MCIND:0x6	2-3
AGP_BASE_2	MCIND:0x7	2-3
MC_AGP_LOCATION	MCIND:0x5	2-3
MC_ARB_DRAM_PENALTIES	MCIND:0x13	2-8
MC_ARB_DRAM_PENALTIES2	MCIND:0x14	2-8
MC_ARB_DRAM_PENALTIES3	MCIND:0x15	2-9
MC_ARB_MIN	MCIND:0x10	2-8
MC_ARB_RATIO_CLK_SEQ	MCIND:0x16	2-9
MC_ARB_RDWR_SWITCH	MCIND:0x17	2-9
MC_ARB_TIMERS	MCIND:0x12	2-8
MC_CNTL0	MCIND:0x8	2-4
MC_CNTL1	MCIND:0x9	2-6
MC_DEBUG	MCIND:0xFE	2-32
MC_FB_LOCATION	MCIND:0x4	2-3
MC_IMP_CNTL	MCIND:0xA0	2-28
MC_IMP_DEBUG	MCIND:0xA1	2-28
MC_IMP_STATUS	MCIND:0xA2	2-28
MC_IND_DATA	MCDEC:0x74	2-2
MC_IND_INDEX	MCDEC:0x70	2-2
MC_IO_A_PAD_CNTL_I0	MCIND:0x92	2-25
MC_IO_A_PAD_CNTL_I1	MCIND:0x93	2-26
MC_IO_CK_PAD_CNTL_I0	MCIND:0x8A	2-23
MC_IO_CK_PAD_CNTL_I1	MCIND:0x8B	2-23
MC_IO_CMD_PAD_CNTL_I0	MCIND:0x8C	2-23
MC_IO_CMD_PAD_CNTL_I1	MCIND:0x8D	2-24
MC_IO_DQ_PAD_CNTL_I0	MCIND:0x8E	2-24
MC_IO_DQ_PAD_CNTL_I1	MCIND:0x8F	2-24
MC_IO_PAD_CNTL	MCIND:0x82	2-21
MC_IO_PAD_CNTL_I0	MCIND:0x80	2-19
MC_IO_PAD_CNTL_I1	MCIND:0x81	2-20
MC_IO_QS_PAD_CNTL_I0	MCIND:0x90	2-25
MC_IO_QS_PAD_CNTL_I1	MCIND:0x91	2-25
MC_IO_RD_DQ_CNTL_I0	MCIND:0x84	2-22
MC_IO_RD_DQ_CNTL_I1	MCIND:0x85	2-22
MC_IO_RD_QS_CNTL_I0	MCIND:0x86	2-22
MC_IO_RD_QS_CNTL_I1	MCIND:0x87	2-22
MC_IO_RD_QS2_CNTL_I0	MCIND:0x9C	2-28
MC_IO_RD_QS2_CNTL_I1	MCIND:0x9D	2-28
MC_IO_WR_CNTL_I0	MCIND:0x88	2-22
MC_IO_WR_CNTL_I1	MCIND:0x89	2-23
MC_IO_WR_DQ_CNTL_I0	MCIND:0x94	2-26
MC_IO_WR_DQ_CNTL_I1	MCIND:0x95	2-26
MC_IO_WR_QS_CNTL_I0	MCIND:0x96	2-26
MC_IO_WR_QS_CNTL_I1	MCIND:0x97	2-27

Table A-8 Memory Controller Registers Sorted by Name (Continued)

Register Name	Address	Page
MC_MISC_0	MCIND:0xF0	2-31
MC_MISC_1	MCIND:0xF1	2-31
MC_NPL_STATUS_I0	MCIND:0x9A	2-27
MC_NPL_STATUS_I1	MCIND:0x9B	2-27
MC_PMG_CFG	MCIND:0xE1	2-31
MC_PMG_CMD	MCIND:0xE0	2-31
MC_PT0_CLIENT0_CNTL	MCIND:0x16C	2-43
MC_PT0_CLIENT1_CNTL	MCIND:0x16D	2-43
MC_PT0_CLIENT10_CNTL	MCIND:0x176	2-51
MC_PT0_CLIENT11_CNTL	MCIND:0x177	2-52
MC_PT0_CLIENT12_CNTL	MCIND:0x178	2-53
MC_PT0_CLIENT13_CNTL	MCIND:0x179	2-54
MC_PT0_CLIENT14_CNTL	MCIND:0x17A	2-55
MC_PT0_CLIENT15_CNTL	MCIND:0x17B	2-55
MC_PT0_CLIENT16_CNTL	MCIND:0x17C	2-56
MC_PT0_CLIENT2_CNTL	MCIND:0x16E	2-44
MC_PT0_CLIENT3_CNTL	MCIND:0x16F	2-45
MC_PT0_CLIENT4_CNTL	MCIND:0x170	2-46
MC_PT0_CLIENT5_CNTL	MCIND:0x171	2-47
MC_PT0_CLIENT6_CNTL	MCIND:0x172	2-48
MC_PT0_CLIENT7_CNTL	MCIND:0x173	2-49
MC_PT0_CLIENT8_CNTL	MCIND:0x174	2-49
MC_PT0_CLIENT9_CNTL	MCIND:0x175	2-50
MC_PT0_CNTL	MCIND:0x100	2-32
MC_PT0_CONTEXT0_CNTL	MCIND:0x102	2-33
MC_PT0_CONTEXT0_DEFAULT_READ_ADDR	MCIND:0x11C	2-36
MC_PT0_CONTEXT0_FLAT_BASE_ADDR	MCIND:0x12C	2-37
MC_PT0_CONTEXT0_FLAT_END_ADDR	MCIND:0x14C	2-40
MC_PT0_CONTEXT0_FLAT_START_ADDR	MCIND:0x13C	2-39
MC_PT0_CONTEXT0_MULTI_LEVEL_BASE_ADDR	MCIND:0x15C	2-41
MC_PT0_CONTEXT1_CNTL	MCIND:0x103	2-33
MC_PT0_CONTEXT1_DEFAULT_READ_ADDR	MCIND:0x11D	2-36
MC_PT0_CONTEXT1_FLAT_BASE_ADDR	MCIND:0x12D	2-38
MC_PT0_CONTEXT1_FLAT_END_ADDR	MCIND:0x14D	2-40
MC_PT0_CONTEXT1_FLAT_START_ADDR	MCIND:0x13D	2-39
MC_PT0_CONTEXT1_MULTI_LEVEL_BASE_ADDR	MCIND:0x15D	2-42
MC_PT0_CONTEXT2_CNTL	MCIND:0x104	2-33
MC_PT0_CONTEXT2_DEFAULT_READ_ADDR	MCIND:0x11E	2-37
MC_PT0_CONTEXT2_FLAT_BASE_ADDR	MCIND:0x12E	2-38
MC_PT0_CONTEXT2_FLAT_END_ADDR	MCIND:0x14E	2-40
MC_PT0_CONTEXT2_FLAT_START_ADDR	MCIND:0x13E	2-39
MC_PT0_CONTEXT2_MULTI_LEVEL_BASE_ADDR	MCIND:0x15E	2-42
MC_PT0_CONTEXT3_CNTL	MCIND:0x105	2-34
MC_PT0_CONTEXT3_DEFAULT_READ_ADDR	MCIND:0x11F	2-37
MC_PT0_CONTEXT3_FLAT_BASE_ADDR	MCIND:0x12F	2-38
MC_PT0_CONTEXT3_FLAT_END_ADDR	MCIND:0x14F	2-41

Table A-8 Memory Controller Registers Sorted by Name (Continued)

Register Name	Address	Page
MC_PT0_CONTEXT3_FLAT_START_ADDR	MCIND:0x13F	2-39
MC_PT0_CONTEXT3_MULTI_LEVEL_BASE_ADDR	MCIND:0x15F	2-42
MC_PT0_CONTEXT4_CNTL	MCIND:0x106	2-34
MC_PT0_CONTEXT4_DEFAULT_READ_ADDR	MCIND:0x120	2-37
MC_PT0_CONTEXT4_FLAT_BASE_ADDR	MCIND:0x130	2-38
MC_PT0_CONTEXT4_FLAT_END_ADDR	MCIND:0x150	2-41
MC_PT0_CONTEXT4_FLAT_START_ADDR	MCIND:0x140	2-39
MC_PT0_CONTEXT4_MULTI_LEVEL_BASE_ADDR	MCIND:0x160	2-42
MC_PT0_CONTEXT5_CNTL	MCIND:0x107	2-34
MC_PT0_CONTEXT5_DEFAULT_READ_ADDR	MCIND:0x121	2-37
MC_PT0_CONTEXT5_FLAT_BASE_ADDR	MCIND:0x131	2-38
MC_PT0_CONTEXT5_FLAT_END_ADDR	MCIND:0x151	2-41
MC_PT0_CONTEXT5_FLAT_START_ADDR	MCIND:0x141	2-40
MC_PT0_CONTEXT5_MULTI_LEVEL_BASE_ADDR	MCIND:0x161	2-42
MC_PT0_CONTEXT6_CNTL	MCIND:0x108	2-34
MC_PT0_CONTEXT6_DEFAULT_READ_ADDR	MCIND:0x122	2-37
MC_PT0_CONTEXT6_FLAT_BASE_ADDR	MCIND:0x132	2-38
MC_PT0_CONTEXT6_FLAT_END_ADDR	MCIND:0x152	2-41
MC_PT0_CONTEXT6_FLAT_START_ADDR	MCIND:0x142	2-40
MC_PT0_CONTEXT6_MULTI_LEVEL_BASE_ADDR	MCIND:0x162	2-42
MC_PT0_CONTEXT7_CNTL	MCIND:0x109	2-35
MC_PT0_CONTEXT7_DEFAULT_READ_ADDR	MCIND:0x123	2-37
MC_PT0_CONTEXT7_FLAT_BASE_ADDR	MCIND:0x133	2-39
MC_PT0_CONTEXT7_FLAT_END_ADDR	MCIND:0x153	2-41
MC_PT0_CONTEXT7_FLAT_START_ADDR	MCIND:0x143	2-40
MC_PT0_CONTEXT7_MULTI_LEVEL_BASE_ADDR	MCIND:0x163	2-42
MC_PT0_PROTECTION_FAULT_STATUS	MCIND:0x11A	2-36
MC_PT0_SURFACE_PROBE	MCIND:0x116	2-35
MC_PT0_SURFACE_PROBE_FAULT_STATUS	MCIND:0x118	2-36
MC_PT0_SYSTEM_APERTURE_HIGH_ADDR	MCIND:0x114	2-35
MC_PT0_SYSTEM_APERTURE_LOW_ADDR	MCIND:0x112	2-35
MC_RBS_CZT_HWM	MCIND:0xB1	2-30
MC_RBS_MAP	MCIND:0xB0	2-29
MC_RBS_MISC	MCIND:0xB3	2-30
MC_RBS_SUN_HWM	MCIND:0xB2	2-30
MC_RFSH_CNTL	MCIND:0xA	2-8
MC_SEQ_A_PAD_CNTL_I0	MCIND:0x74	2-18
MC_SEQ_A_PAD_CNTL_I1	MCIND:0x75	2-18
MC_SEQ_CAS_TIMING	MCIND:0x62	2-11
MC_SEQ_CK_PAD_CNTL_I0	MCIND:0x6C	2-16
MC_SEQ_CK_PAD_CNTL_I1	MCIND:0x6D	2-16
MC_SEQ_CMD	MCIND:0x76	2-19
MC_SEQ_CMD_PAD_CNTL_I0	MCIND:0x6E	2-17
MC_SEQ_CMD_PAD_CNTL_I1	MCIND:0x6F	2-17
MC_SEQ_DQ_PAD_CNTL_I0	MCIND:0x70	2-17
MC_SEQ_DQ_PAD_CNTL_I1	MCIND:0x71	2-17

Table A-8 Memory Controller Registers Sorted by Name (Continued)

Register Name	Address	Page
MC_SEQ_DRAM	*MCIND:0x60*	*2-10*
MC_SEQ_IO_CTL_I0	*MCIND:0x68*	*2-15*
MC_SEQ_IO_CTL_I1	*MCIND:0x69*	*2-15*
MC_SEQ_MISC_TIMING	*MCIND:0x63*	*2-12*
MC_SEQ_NPL_CTL_I0	*MCIND:0x6A*	*2-16*
MC_SEQ_NPL_CTL_I1	*MCIND:0x6B*	*2-16*
MC_SEQ_QS_PAD_CNTL_I0	*MCIND:0x72*	*2-18*
MC_SEQ_QS_PAD_CNTL_I1	*MCIND:0x73*	*2-18*
MC_SEQ_RAS_TIMING	*MCIND:0x61*	*2-11*
MC_SEQ_RD_CTL_I0	*MCIND:0x64*	*2-12*
MC_SEQ_RD_CTL_I1	*MCIND:0x65*	*2-13*
MC_SEQ_STATUS	*MCIND:0x77*	*2-19*
MC_SEQ_WR_CTL_I0	*MCIND:0x66*	*2-14*
MC_SEQ_WR_CTL_I1	*MCIND:0x67*	*2-15*
MC_STATUS	*MCIND:0x0*	*2-2*
MC_SW_CNTL	*MCIND:0x18*	*2-9*
MC_TIMING_CNTL_2	*MCIND:0x3*	*2-3*
MC_VENDOR_ID_I0	*MCIND:0x98*	*2-27*
MC_VENDOR_ID_I1	*MCIND:0x99*	*2-27*
MC_WRITE_AGE1	*MCIND:0x37*	*2-9*
MC_WRITE_AGE2	*MCIND:0x38*	*2-10*

A.10 Memory Controller Registers Sorted By Address

Table A-9 Memory Controller Registers Sorted by Address

Register Name	Address	Page
MC_IND_INDEX	MCDEC:0x70	2-2
MC_IND_DATA	MCDEC:0x74	2-2
MC_STATUS	MCIND:0x0	2-2
MC_ARB_MIN	MCIND:0x10	2-8
MC_PT0_CNTL	MCIND:0x100	2-32
MC_PT0_CONTEXT0_CNTL	MCIND:0x102	2-33
MC_PT0_CONTEXT1_CNTL	MCIND:0x103	2-33
MC_PT0_CONTEXT2_CNTL	MCIND:0x104	2-33
MC_PT0_CONTEXT3_CNTL	MCIND:0x105	2-34
MC_PT0_CONTEXT4_CNTL	MCIND:0x106	2-34
MC_PT0_CONTEXT5_CNTL	MCIND:0x107	2-34
MC_PT0_CONTEXT6_CNTL	MCIND:0x108	2-34
MC_PT0_CONTEXT7_CNTL	MCIND:0x109	2-35
MC_PT0_SYSTEM_APERTURE_LOW_ADDR	MCIND:0x112	2-35
MC_PT0_SYSTEM_APERTURE_HIGH_ADDR	MCIND:0x114	2-35
MC_PT0_SURFACE_PROBE	MCIND:0x116	2-35
MC_PT0_SURFACE_PROBE_FAULT_STATUS	MCIND:0x118	2-36
MC_PT0_PROTECTION_FAULT_STATUS	MCIND:0x11A	2-36
MC_PT0_CONTEXT0_DEFAULT_READ_ADDR	MCIND:0x11C	2-36
MC_PT0_CONTEXT1_DEFAULT_READ_ADDR	MCIND:0x11D	2-36
MC_PT0_CONTEXT2_DEFAULT_READ_ADDR	MCIND:0x11E	2-37
MC_PT0_CONTEXT3_DEFAULT_READ_ADDR	MCIND:0x11F	2-37
MC_ARB_TIMERS	MCIND:0x12	2-8
MC_PT0_CONTEXT4_DEFAULT_READ_ADDR	MCIND:0x120	2-37
MC_PT0_CONTEXT5_DEFAULT_READ_ADDR	MCIND:0x121	2-37
MC_PT0_CONTEXT6_DEFAULT_READ_ADDR	MCIND:0x122	2-37
MC_PT0_CONTEXT7_DEFAULT_READ_ADDR	MCIND:0x123	2-37
MC_PT0_CONTEXT0_FLAT_BASE_ADDR	MCIND:0x12C	2-37
MC_PT0_CONTEXT1_FLAT_BASE_ADDR	MCIND:0x12D	2-38
MC_PT0_CONTEXT2_FLAT_BASE_ADDR	MCIND:0x12E	2-38
MC_PT0_CONTEXT3_FLAT_BASE_ADDR	MCIND:0x12F	2-38
MC_ARB_DRAM_PENALTIES	MCIND:0x13	2-8
MC_PT0_CONTEXT4_FLAT_BASE_ADDR	MCIND:0x130	2-38
MC_PT0_CONTEXT5_FLAT_BASE_ADDR	MCIND:0x131	2-38
MC_PT0_CONTEXT6_FLAT_BASE_ADDR	MCIND:0x132	2-38
MC_PT0_CONTEXT7_FLAT_BASE_ADDR	MCIND:0x133	2-39
MC_PT0_CONTEXT0_FLAT_START_ADDR	MCIND:0x13C	2-39
MC_PT0_CONTEXT1_FLAT_START_ADDR	MCIND:0x13D	2-39
MC_PT0_CONTEXT2_FLAT_START_ADDR	MCIND:0x13E	2-39
MC_PT0_CONTEXT3_FLAT_START_ADDR	MCIND:0x13F	2-39
MC_ARB_DRAM_PENALTIES2	MCIND:0x14	2-8
MC_PT0_CONTEXT4_FLAT_START_ADDR	MCIND:0x140	2-39
MC_PT0_CONTEXT5_FLAT_START_ADDR	MCIND:0x141	2-40

Table A-9 Memory Controller Registers Sorted by Address (Continued)

Register Name	Address	Page
MC_PT0_CONTEXT6_FLAT_START_ADDR	MCIND:0x142	2-40
MC_PT0_CONTEXT7_FLAT_START_ADDR	MCIND:0x143	2-40
MC_PT0_CONTEXT0_FLAT_END_ADDR	MCIND:0x14C	2-40
MC_PT0_CONTEXT1_FLAT_END_ADDR	MCIND:0x14D	2-40
MC_PT0_CONTEXT2_FLAT_END_ADDR	MCIND:0x14E	2-40
MC_PT0_CONTEXT3_FLAT_END_ADDR	MCIND:0x14F	2-41
MC_ARB_DRAM_PENALTIES3	MCIND:0x15	2-9
MC_PT0_CONTEXT4_FLAT_END_ADDR	MCIND:0x150	2-41
MC_PT0_CONTEXT5_FLAT_END_ADDR	MCIND:0x151	2-41
MC_PT0_CONTEXT6_FLAT_END_ADDR	MCIND:0x152	2-41
MC_PT0_CONTEXT7_FLAT_END_ADDR	MCIND:0x153	2-41
MC_PT0_CONTEXT0_MULTI_LEVEL_BASE_ADDR	MCIND:0x15C	2-41
MC_PT0_CONTEXT1_MULTI_LEVEL_BASE_ADDR	MCIND:0x15D	2-42
MC_PT0_CONTEXT2_MULTI_LEVEL_BASE_ADDR	MCIND:0x15E	2-42
MC_PT0_CONTEXT3_MULTI_LEVEL_BASE_ADDR	MCIND:0x15F	2-42
MC_ARB_RATIO_CLK_SEQ	MCIND:0x16	2-9
MC_PT0_CONTEXT4_MULTI_LEVEL_BASE_ADDR	MCIND:0x160	2-42
MC_PT0_CONTEXT5_MULTI_LEVEL_BASE_ADDR	MCIND:0x161	2-42
MC_PT0_CONTEXT6_MULTI_LEVEL_BASE_ADDR	MCIND:0x162	2-42
MC_PT0_CONTEXT7_MULTI_LEVEL_BASE_ADDR	MCIND:0x163	2-42
MC_PT0_CLIENT0_CNTL	MCIND:0x16C	2-43
MC_PT0_CLIENT1_CNTL	MCIND:0x16D	2-43
MC_PT0_CLIENT2_CNTL	MCIND:0x16E	2-44
MC_PT0_CLIENT3_CNTL	MCIND:0x16F	2-45
MC_ARB_RDWR_SWITCH	MCIND:0x17	2-9
MC_PT0_CLIENT4_CNTL	MCIND:0x170	2-46
MC_PT0_CLIENT5_CNTL	MCIND:0x171	2-47
MC_PT0_CLIENT6_CNTL	MCIND:0x172	2-48
MC_PT0_CLIENT7_CNTL	MCIND:0x173	2-49
MC_PT0_CLIENT8_CNTL	MCIND:0x174	2-49
MC_PT0_CLIENT9_CNTL	MCIND:0x175	2-50
MC_PT0_CLIENT10_CNTL	MCIND:0x176	2-51
MC_PT0_CLIENT11_CNTL	MCIND:0x177	2-52
MC_PT0_CLIENT12_CNTL	MCIND:0x178	2-53
MC_PT0_CLIENT13_CNTL	MCIND:0x179	2-54
MC_PT0_CLIENT14_CNTL	MCIND:0x17A	2-55
MC_PT0_CLIENT15_CNTL	MCIND:0x17B	2-55
MC_PT0_CLIENT16_CNTL	MCIND:0x17C	2-56
MC_SW_CNTL	MCIND:0x18	2-9
MC_TIMING_CNTL_2	MCIND:0x3	2-3
MC_WRITE_AGE1	MCIND:0x37	2-9
MC_WRITE_AGE2	MCIND:0x38	2-10
MC_FB_LOCATION	MCIND:0x4	2-3
MC_AGP_LOCATION	MCIND:0x5	2-3
AGP_BASE	MCIND:0x6	2-3
MC_SEQ_DRAM	MCIND:0x60	2-10

Table A-9 Memory Controller Registers Sorted by Address (Continued)

Register Name	Address	Page
MC_SEQ_RAS_TIMING	MCIND:0x61	2-11
MC_SEQ_CAS_TIMING	MCIND:0x62	2-11
MC_SEQ_MISC_TIMING	MCIND:0x63	2-12
MC_SEQ_RD_CTL_I0	MCIND:0x64	2-12
MC_SEQ_RD_CTL_I1	MCIND:0x65	2-13
MC_SEQ_WR_CTL_I0	MCIND:0x66	2-14
MC_SEQ_WR_CTL_I1	MCIND:0x67	2-15
MC_SEQ_IO_CTL_I0	MCIND:0x68	2-15
MC_SEQ_IO_CTL_I1	MCIND:0x69	2-15
MC_SEQ_NPL_CTL_I0	MCIND:0x6A	2-16
MC_SEQ_NPL_CTL_I1	MCIND:0x6B	2-16
MC_SEQ_CK_PAD_CNTL_I0	MCIND:0x6C	2-16
MC_SEQ_CK_PAD_CNTL_I1	MCIND:0x6D	2-16
MC_SEQ_CMD_PAD_CNTL_I0	MCIND:0x6E	2-17
MC_SEQ_CMD_PAD_CNTL_I1	MCIND:0x6F	2-17
AGP_BASE_2	MCIND:0x7	2-3
MC_SEQ_DQ_PAD_CNTL_I0	MCIND:0x70	2-17
MC_SEQ_DQ_PAD_CNTL_I1	MCIND:0x71	2-17
MC_SEQ_QS_PAD_CNTL_I0	MCIND:0x72	2-18
MC_SEQ_QS_PAD_CNTL_I1	MCIND:0x73	2-18
MC_SEQ_A_PAD_CNTL_I0	MCIND:0x74	2-18
MC_SEQ_A_PAD_CNTL_I1	MCIND:0x75	2-18
MC_SEQ_CMD	MCIND:0x76	2-19
MC_SEQ_STATUS	MCIND:0x77	2-19
MC_CNTL0	MCIND:0x8	2-4
MC_IO_PAD_CNTL_I0	MCIND:0x80	2-19
MC_IO_PAD_CNTL_I1	MCIND:0x81	2-20
MC_IO_PAD_CNTL	MCIND:0x82	2-21
MC_IO_RD_DQ_CNTL_I0	MCIND:0x84	2-22
MC_IO_RD_DQ_CNTL_I1	MCIND:0x85	2-22
MC_IO_RD_QS_CNTL_I0	MCIND:0x86	2-22
MC_IO_RD_QS_CNTL_I1	MCIND:0x87	2-22
MC_IO_WR_CNTL_I0	MCIND:0x88	2-22
MC_IO_WR_CNTL_I1	MCIND:0x89	2-23
MC_IO_CK_PAD_CNTL_I0	MCIND:0x8A	2-23
MC_IO_CK_PAD_CNTL_I1	MCIND:0x8B	2-23
MC_IO_CMD_PAD_CNTL_I0	MCIND:0x8C	2-23
MC_IO_CMD_PAD_CNTL_I1	MCIND:0x8D	2-24
MC_IO_DQ_PAD_CNTL_I0	MCIND:0x8E	2-24
MC_IO_DQ_PAD_CNTL_I1	MCIND:0x8F	2-24
MC_CNTL1	MCIND:0x9	2-6
MC_IO_QS_PAD_CNTL_I0	MCIND:0x90	2-25
MC_IO_QS_PAD_CNTL_I1	MCIND:0x91	2-25
MC_IO_A_PAD_CNTL_I0	MCIND:0x92	2-25
MC_IO_A_PAD_CNTL_I1	MCIND:0x93	2-26
MC_IO_WR_DQ_CNTL_I0	MCIND:0x94	2-26

Table A-9 Memory Controller Registers Sorted by Address (Continued)

Register Name	Address	Page
MC_IO_WR_DQ_CNTL_I1	*MCIND:0x95*	*2-26*
MC_IO_WR_QS_CNTL_I0	*MCIND:0x96*	*2-26*
MC_IO_WR_QS_CNTL_I1	*MCIND:0x97*	*2-27*
MC_VENDOR_ID_I0	*MCIND:0x98*	*2-27*
MC_VENDOR_ID_I1	*MCIND:0x99*	*2-27*
MC_NPL_STATUS_I0	*MCIND:0x9A*	*2-27*
MC_NPL_STATUS_I1	*MCIND:0x9B*	*2-27*
MC_IO_RD_QS2_CNTL_I0	*MCIND:0x9C*	*2-28*
MC_IO_RD_QS2_CNTL_I1	*MCIND:0x9D*	*2-28*
MC_RFSH_CNTL	*MCIND:0xA*	*2-8*
MC_IMP_CNTL	*MCIND:0xA0*	*2-28*
MC_IMP_DEBUG	*MCIND:0xA1*	*2-28*
MC_IMP_STATUS	*MCIND:0xA2*	*2-28*
MC_RBS_MAP	*MCIND:0xB0*	*2-29*
MC_RBS_CZT_HWM	*MCIND:0xB1*	*2-30*
MC_RBS_SUN_HWM	*MCIND:0xB2*	*2-30*
MC_RBS_MISC	*MCIND:0xB3*	*2-30*
MC_PMG_CMD	*MCIND:0xE0*	*2-31*
MC_PMG_CFG	*MCIND:0xE1*	*2-31*
MC_MISC_0	*MCIND:0xF0*	*2-31*
MC_MISC_1	*MCIND:0xF1*	*2-31*
MC_DEBUG	*MCIND:0xFE*	*2-32*

A.11 PCIE Registers Sorted By Name

Table A-10 PCIE Registers Sorted by Name

Register Name	Address	Page
PCIE_CI_CNTL	PCIEIND:0x90	2-94
PCIE_CI_FLUSH_CNTL	PCIEIND:0x91	2-94
PCIE_CI_HANG	PCIEIND:0x93	2-95
PCIE_CI_PANIC	PCIEIND:0x92	2-94
PCIE_CLK_CNTL	PCIEIND:0x400	2-107
PCIE_CLK_RST_CNTL	PCIEIND:0xE1	2-105
PCIE_ERR_CNTL	PCIEIND:0xE0	2-105
PCIE_FLOW_CNTL	PCIEIND:0x60	2-89
PCIE_LC_CNTL	PCIEIND:0xA0	2-95
PCIE_LC_FORCE_SYNC_LOSS_CNTL	PCIEIND:0xAB	2-97
PCIE_LC_LINK_WIDTH_CNTL	PCIEIND:0xA2	2-97
PCIE_LC_N_FTS_CNTL	PCIEIND:0xA1	2-95
PCIE_LC_STATE0	PCIEIND:0xA5	2-95
PCIE_LC_STATE1	PCIEIND:0xA6	2-96
PCIE_LC_STATE2	PCIEIND:0xA7	2-96
PCIE_LC_STATE3	PCIEIND:0xA8	2-96
PCIE_LC_STATE4	PCIEIND:0xA9	2-96
PCIE_LC_STATE5	PCIEIND:0xAA	2-96
PCIE_P_BUF_STATUS	PCIEIND:0xB2	2-98
PCIE_P_CNTL	PCIEIND:0xB0	2-97
PCIE_P_CNTL2	PCIEIND:0xB1	2-98
PCIE_P_DECODE_ERR_CNT_0	PCIEIND:0xF0	2-103
PCIE_P_DECODE_ERR_CNT_1	PCIEIND:0xF1	2-103
PCIE_P_DECODE_ERR_CNT_10	PCIEIND:0xFA	2-104
PCIE_P_DECODE_ERR_CNT_11	PCIEIND:0xFB	2-104
PCIE_P_DECODE_ERR_CNT_12	PCIEIND:0xFC	2-105
PCIE_P_DECODE_ERR_CNT_13	PCIEIND:0xFD	2-105
PCIE_P_DECODE_ERR_CNT_14	PCIEIND:0xFE	2-105
PCIE_P_DECODE_ERR_CNT_15	PCIEIND:0xFF	2-105
PCIE_P_DECODE_ERR_CNT_2	PCIEIND:0xF2	2-103
PCIE_P_DECODE_ERR_CNT_3	PCIEIND:0xF3	2-103
PCIE_P_DECODE_ERR_CNT_4	PCIEIND:0xF4	2-103
PCIE_P_DECODE_ERR_CNT_5	PCIEIND:0xF5	2-103
PCIE_P_DECODE_ERR_CNT_6	PCIEIND:0xF6	2-104
PCIE_P_DECODE_ERR_CNT_7	PCIEIND:0xF7	2-104
PCIE_P_DECODE_ERR_CNT_8	PCIEIND:0xF8	2-104
PCIE_P_DECODE_ERR_CNT_9	PCIEIND:0xF9	2-104
PCIE_P_DECODE_ERR_CNTL	PCIEIND:0xC5	2-103
PCIE_P_DECODER_STATUS	PCIEIND:0xB3	2-99
PCIE_P_IMP_CNTL_STRENGTH	PCIEIND:0xC0	2-101
PCIE_P_IMP_CNTL_UPDATE	PCIEIND:0xC1	2-102
PCIE_P_MISC_DEBUG_STATUS	PCIEIND:0xB4	2-100
PCIE_P_PAD_MISC_CNTL	PCIEIND:0xC3	2-102
PCIE_P_STR_CNTL_UPDATE	PCIEIND:0xC2	2-102

Table A-10 PCIE Registers Sorted by Name (Continued)

Register Name	Address	Page
PCIE_P_SYMSYNC_CTL	PCIEIND:0xC4	2-102
PCIE_PRBS_EN	PCIEIND:0x424	2-113
PCIE_PRBS10	PCIEIND:0x401	2-107
PCIE_PRBS23_BITCNT0	PCIEIND:0x402	2-107
PCIE_PRBS23_BITCNT1	PCIEIND:0x403	2-107
PCIE_PRBS23_BITCNT10	PCIEIND:0x40C	2-109
PCIE_PRBS23_BITCNT11	PCIEIND:0x40D	2-109
PCIE_PRBS23_BITCNT12	PCIEIND:0x40E	2-109
PCIE_PRBS23_BITCNT13	PCIEIND:0x40F	2-109
PCIE_PRBS23_BITCNT14	PCIEIND:0x410	2-109
PCIE_PRBS23_BITCNT15	PCIEIND:0x411	2-109
PCIE_PRBS23_BITCNT2	PCIEIND:0x404	2-107
PCIE_PRBS23_BITCNT3	PCIEIND:0x405	2-108
PCIE_PRBS23_BITCNT4	PCIEIND:0x406	2-108
PCIE_PRBS23_BITCNT5	PCIEIND:0x407	2-108
PCIE_PRBS23_BITCNT6	PCIEIND:0x408	2-108
PCIE_PRBS23_BITCNT7	PCIEIND:0x409	2-108
PCIE_PRBS23_BITCNT8	PCIEIND:0x40A	2-108
PCIE_PRBS23_BITCNT9	PCIEIND:0x40B	2-108
PCIE_PRBS23_CTRL0	PCIEIND:0x422	2-112
PCIE_PRBS23_CTRL1	PCIEIND:0x423	2-113
PCIE_PRBS23_ERRCNT0	PCIEIND:0x412	2-110
PCIE_PRBS23_ERRCNT1	PCIEIND:0x413	2-110
PCIE_PRBS23_ERRCNT10	PCIEIND:0x41C	2-111
PCIE_PRBS23_ERRCNT11	PCIEIND:0x41D	2-111
PCIE_PRBS23_ERRCNT12	PCIEIND:0x41E	2-111
PCIE_PRBS23_ERRCNT13	PCIEIND:0x41F	2-111
PCIE_PRBS23_ERRCNT14	PCIEIND:0x420	2-112
PCIE_PRBS23_ERRCNT15	PCIEIND:0x421	2-112
PCIE_PRBS23_ERRCNT2	PCIEIND:0x414	2-110
PCIE_PRBS23_ERRCNT3	PCIEIND:0x415	2-110
PCIE_PRBS23_ERRCNT4	PCIEIND:0x416	2-110
PCIE_PRBS23_ERRCNT5	PCIEIND:0x417	2-110
PCIE_PRBS23_ERRCNT6	PCIEIND:0x418	2-110
PCIE_PRBS23_ERRCNT7	PCIEIND:0x419	2-111
PCIE_PRBS23_ERRCNT8	PCIEIND:0x41A	2-111
PCIE_PRBS23_ERRCNT9	PCIEIND:0x41B	2-111
PCIE_RESERVED	PCIEIND:0x0	2-80
PCIE_RX_ACK_NACK_LATENCY	PCIEIND:0x73	2-91
PCIE_RX_ACK_NACK_LATENCY_THRESHOLD	PCIEIND:0x74	2-91
PCIE_RX_CNTL	PCIEIND:0x70	2-90
PCIE_RX_CREDITS_ALLOCATED	PCIEIND:0x7E	2-92
PCIE_RX_CREDITS_ALLOCATED_CPLD	PCIEIND:0x80	2-93
PCIE_RX_CREDITS_ALLOCATED_D	PCIEIND:0x7F	2-93
PCIE_RX_CREDITS_RECEIVED	PCIEIND:0x81	2-93
PCIE_RX_CREDITS_RECEIVED_CPLD	PCIEIND:0x83	2-93

Table A-10 PCIE Registers Sorted by Name (Continued)

Register Name	Address	Page
PCIE_RX_CREDITS_RECEIVED_D	PCIEIND:0x82	2-93
PCIE_RX_DLP_CRC	PCIEIND:0x7D	2-92
PCIE_RX_DLP0	PCIEIND:0x7B	2-92
PCIE_RX_DLP1	PCIEIND:0x7C	2-92
PCIE_RX_ERR_LOG	PCIEIND:0x85	2-94
PCIE_RX_EXPECTED_SEQNUM	PCIEIND:0x86	2-94
PCIE_RX_MAL_TLP_COUNT	PCIEIND:0x84	2-93
PCIE_RX_NUM_NACK	PCIEIND:0x71	2-91
PCIE_RX_NUM_NACK_GENERATED	PCIEIND:0x72	2-91
PCIE_RX_TLP_CRC	PCIEIND:0x7A	2-92
PCIE_RX_TLP_HDR0	PCIEIND:0x75	2-91
PCIE_RX_TLP_HDR1	PCIEIND:0x76	2-91
PCIE_RX_TLP_HDR2	PCIEIND:0x77	2-91
PCIE_RX_TLP_HDR3	PCIEIND:0x78	2-92
PCIE_RX_TLP_HDR4	PCIEIND:0x79	2-92
PCIE_TX_CNTL	PCIEIND:0x1	2-80
PCIE_TX_CREDITS_CONSUMED	PCIEIND:0x4	2-81
PCIE_TX_CREDITS_CONSUMED_CPLD	PCIEIND:0x6	2-81
PCIE_TX_CREDITS_CONSUMED_D	PCIEIND:0x5	2-81
PCIE_TX_CREDITS_LIMIT	PCIEIND:0x7	2-81
PCIE_TX_CREDITS_LIMIT_CPLD	PCIEIND:0x9	2-82
PCIE_TX_CREDITS_LIMIT_D	PCIEIND:0x8	2-81
PCIE_TX_GART_BASE	PCIEIND:0x13	2-83
PCIE_TX_GART_CNTL	PCIEIND:0x10	2-82
PCIE_TX_GART_DISCARD_RD_ADDR_HI	PCIEIND:0x12	2-82
PCIE_TX_GART_DISCARD_RD_ADDR_LO	PCIEIND:0x11	2-82
PCIE_TX_GART_END_HI	PCIEIND:0x17	2-83
PCIE_TX_GART_END_LO	PCIEIND:0x16	2-83
PCIE_TX_GART_ERROR	PCIEIND:0x18	2-83
PCIE_TX_GART_LRU_MRU_PTR	PCIEIND:0x20	2-84
PCIE_TX_GART_START_HI	PCIEIND:0x15	2-83
PCIE_TX_GART_START_LO	PCIEIND:0x14	2-83
PCIE_TX_GART_STATUS	PCIEIND:0x21	2-84
PCIE_TX_GART_TLB_VALID	PCIEIND:0x22	2-84
PCIE_TX_GART_TLB0_DATA	PCIEIND:0x23	2-84
PCIE_TX_GART_TLB1_DATA	PCIEIND:0x24	2-84
PCIE_TX_GART_TLB10_DATA	PCIEIND:0x2D	2-86
PCIE_TX_GART_TLB11_DATA	PCIEIND:0x2E	2-86
PCIE_TX_GART_TLB12_DATA	PCIEIND:0x2F	2-86
PCIE_TX_GART_TLB13_DATA	PCIEIND:0x30	2-86
PCIE_TX_GART_TLB14_DATA	PCIEIND:0x31	2-86
PCIE_TX_GART_TLB15_DATA	PCIEIND:0x32	2-86
PCIE_TX_GART_TLB16_DATA	PCIEIND:0x33	2-87
PCIE_TX_GART_TLB17_DATA	PCIEIND:0x34	2-87
PCIE_TX_GART_TLB18_DATA	PCIEIND:0x35	2-87
PCIE_TX_GART_TLB19_DATA	PCIEIND:0x36	2-87

Table A-10 PCIE Registers Sorted by Name (Continued)

Register Name	Address	Page
PCIE_TX_GART_TLB2_DATA	PCIEIND:0x25	2-84
PCIE_TX_GART_TLB20_DATA	PCIEIND:0x37	2-87
PCIE_TX_GART_TLB21_DATA	PCIEIND:0x38	2-87
PCIE_TX_GART_TLB22_DATA	PCIEIND:0x39	2-88
PCIE_TX_GART_TLB23_DATA	PCIEIND:0x3A	2-88
PCIE_TX_GART_TLB24_DATA	PCIEIND:0x3B	2-88
PCIE_TX_GART_TLB25_DATA	PCIEIND:0x3C	2-88
PCIE_TX_GART_TLB26_DATA	PCIEIND:0x3D	2-88
PCIE_TX_GART_TLB27_DATA	PCIEIND:0x3E	2-88
PCIE_TX_GART_TLB28_DATA	PCIEIND:0x3F	2-89
PCIE_TX_GART_TLB29_DATA	PCIEIND:0x40	2-89
PCIE_TX_GART_TLB3_DATA	PCIEIND:0x26	2-85
PCIE_TX_GART_TLB30_DATA	PCIEIND:0x41	2-89
PCIE_TX_GART_TLB31_DATA	PCIEIND:0x42	2-89
PCIE_TX_GART_TLB4_DATA	PCIEIND:0x27	2-85
PCIE_TX_GART_TLB5_DATA	PCIEIND:0x28	2-85
PCIE_TX_GART_TLB6_DATA	PCIEIND:0x29	2-85
PCIE_TX_GART_TLB7_DATA	PCIEIND:0x2A	2-85
PCIE_TX_GART_TLB8_DATA	PCIEIND:0x2B	2-85
PCIE_TX_GART_TLB9_DATA	PCIEIND:0x2C	2-85
PCIE_TX_REPLAY	PCIEIND:0x3	2-80
PCIE_TX_SEQ	PCIEIND:0x2	2-80
PCIE_TXRX_DEBUG_SEQNUM	PCIEIND:0x61	2-90
PCIE_TXRX_TEST_MODE	PCIEIND:0x62	2-90
PCIE_XSTRAP1	PCIEIND:0x425	2-113
PCIE_XSTRAP2	PCIEIND:0x426	2-114
PCIE_XSTRAP5	PCIEIND:0x429	2-114

A.12 PCIE Registers Sorted By Address

Table A-11 PCIE Registers Sorted by Address

Register Name	Address	Page
PCIE_RESERVED	PCIEIND:0x0	2-80
PCIE_TX_CNTL	PCIEIND:0x1	2-80
PCIE_TX_GART_CNTL	PCIEIND:0x10	2-82
PCIE_TX_GART_DISCARD_RD_ADDR_LO	PCIEIND:0x11	2-82
PCIE_TX_GART_DISCARD_RD_ADDR_HI	PCIEIND:0x12	2-82
PCIE_TX_GART_BASE	PCIEIND:0x13	2-83
PCIE_TX_GART_START_LO	PCIEIND:0x14	2-83
PCIE_TX_GART_START_HI	PCIEIND:0x15	2-83
PCIE_TX_GART_END_LO	PCIEIND:0x16	2-83
PCIE_TX_GART_END_HI	PCIEIND:0x17	2-83
PCIE_TX_GART_ERROR	PCIEIND:0x18	2-83
PCIE_TX_SEQ	PCIEIND:0x2	2-80
PCIE_TX_GART_LRU_MRU_PTR	PCIEIND:0x20	2-84
PCIE_TX_GART_STATUS	PCIEIND:0x21	2-84
PCIE_TX_GART_TLB_VALID	PCIEIND:0x22	2-84
PCIE_TX_GART_TLB0_DATA	PCIEIND:0x23	2-84
PCIE_TX_GART_TLB1_DATA	PCIEIND:0x24	2-84
PCIE_TX_GART_TLB2_DATA	PCIEIND:0x25	2-84
PCIE_TX_GART_TLB3_DATA	PCIEIND:0x26	2-85
PCIE_TX_GART_TLB4_DATA	PCIEIND:0x27	2-85
PCIE_TX_GART_TLB5_DATA	PCIEIND:0x28	2-85
PCIE_TX_GART_TLB6_DATA	PCIEIND:0x29	2-85
PCIE_TX_GART_TLB7_DATA	PCIEIND:0x2A	2-85
PCIE_TX_GART_TLB8_DATA	PCIEIND:0x2B	2-85
PCIE_TX_GART_TLB9_DATA	PCIEIND:0x2C	2-85
PCIE_TX_GART_TLB10_DATA	PCIEIND:0x2D	2-86
PCIE_TX_GART_TLB11_DATA	PCIEIND:0x2E	2-86
PCIE_TX_GART_TLB12_DATA	PCIEIND:0x2F	2-86
PCIE_TX_REPLAY	PCIEIND:0x3	2-80
PCIE_TX_GART_TLB13_DATA	PCIEIND:0x30	2-86
PCIE_TX_GART_TLB14_DATA	PCIEIND:0x31	2-86
PCIE_TX_GART_TLB15_DATA	PCIEIND:0x32	2-86
PCIE_TX_GART_TLB16_DATA	PCIEIND:0x33	2-87
PCIE_TX_GART_TLB17_DATA	PCIEIND:0x34	2-87
PCIE_TX_GART_TLB18_DATA	PCIEIND:0x35	2-87
PCIE_TX_GART_TLB19_DATA	PCIEIND:0x36	2-87
PCIE_TX_GART_TLB20_DATA	PCIEIND:0x37	2-87
PCIE_TX_GART_TLB21_DATA	PCIEIND:0x38	2-87
PCIE_TX_GART_TLB22_DATA	PCIEIND:0x39	2-88
PCIE_TX_GART_TLB23_DATA	PCIEIND:0x3A	2-88
PCIE_TX_GART_TLB24_DATA	PCIEIND:0x3B	2-88
PCIE_TX_GART_TLB25_DATA	PCIEIND:0x3C	2-88
PCIE_TX_GART_TLB26_DATA	PCIEIND:0x3D	2-88

Table A-11 PCIE Registers Sorted by Address (Continued)

Register Name	Address	Page
PCIE_TX_GART_TLB27_DATA	PCIEIND:0x3E	2-88
PCIE_TX_GART_TLB28_DATA	PCIEIND:0x3F	2-89
PCIE_TX_CREDITS_CONSUMED	PCIEIND:0x4	2-81
PCIE_TX_GART_TLB29_DATA	PCIEIND:0x40	2-89
PCIE_CLK_CNTL	PCIEIND:0x400	2-107
PCIE_PRBS10	PCIEIND:0x401	2-107
PCIE_PRBS23_BITCNT0	PCIEIND:0x402	2-107
PCIE_PRBS23_BITCNT1	PCIEIND:0x403	2-107
PCIE_PRBS23_BITCNT2	PCIEIND:0x404	2-107
PCIE_PRBS23_BITCNT3	PCIEIND:0x405	2-108
PCIE_PRBS23_BITCNT4	PCIEIND:0x406	2-108
PCIE_PRBS23_BITCNT5	PCIEIND:0x407	2-108
PCIE_PRBS23_BITCNT6	PCIEIND:0x408	2-108
PCIE_PRBS23_BITCNT7	PCIEIND:0x409	2-108
PCIE_PRBS23_BITCNT8	PCIEIND:0x40A	2-108
PCIE_PRBS23_BITCNT9	PCIEIND:0x40B	2-108
PCIE_PRBS23_BITCNT10	PCIEIND:0x40C	2-109
PCIE_PRBS23_BITCNT11	PCIEIND:0x40D	2-109
PCIE_PRBS23_BITCNT12	PCIEIND:0x40E	2-109
PCIE_PRBS23_BITCNT13	PCIEIND:0x40F	2-109
PCIE_TX_GART_TLB30_DATA	PCIEIND:0x41	2-89
PCIE_PRBS23_BITCNT14	PCIEIND:0x410	2-109
PCIE_PRBS23_BITCNT15	PCIEIND:0x411	2-109
PCIE_PRBS23_ERRCNT0	PCIEIND:0x412	2-110
PCIE_PRBS23_ERRCNT1	PCIEIND:0x413	2-110
PCIE_PRBS23_ERRCNT2	PCIEIND:0x414	2-110
PCIE_PRBS23_ERRCNT3	PCIEIND:0x415	2-110
PCIE_PRBS23_ERRCNT4	PCIEIND:0x416	2-110
PCIE_PRBS23_ERRCNT5	PCIEIND:0x417	2-110
PCIE_PRBS23_ERRCNT6	PCIEIND:0x418	2-110
PCIE_PRBS23_ERRCNT7	PCIEIND:0x419	2-111
PCIE_PRBS23_ERRCNT8	PCIEIND:0x41A	2-111
PCIE_PRBS23_ERRCNT9	PCIEIND:0x41B	2-111
PCIE_PRBS23_ERRCNT10	PCIEIND:0x41C	2-111
PCIE_PRBS23_ERRCNT11	PCIEIND:0x41D	2-111
PCIE_PRBS23_ERRCNT12	PCIEIND:0x41E	2-111
PCIE_PRBS23_ERRCNT13	PCIEIND:0x41F	2-111
PCIE_TX_GART_TLB31_DATA	PCIEIND:0x42	2-89
PCIE_PRBS23_ERRCNT14	PCIEIND:0x420	2-112
PCIE_PRBS23_ERRCNT15	PCIEIND:0x421	2-112
PCIE_PRBS23_CTRL0	PCIEIND:0x422	2-112
PCIE_PRBS23_CTRL1	PCIEIND:0x423	2-113
PCIE_PRBS_EN	PCIEIND:0x424	2-113
PCIE_XSTRAP1	PCIEIND:0x425	2-113
PCIE_XSTRAP2	PCIEIND:0x426	2-114
PCIE_XSTRAP5	PCIEIND:0x429	2-114

Table A-11 PCIE Registers Sorted by Address (Continued)

Register Name	Address	Page
PCIE_TX_CREDITS_CONSUMED_D	PCIEIND:0x5	2-81
PCIE_TX_CREDITS_CONSUMED_CPLD	PCIEIND:0x6	2-81
PCIE_FLOW_CNTL	PCIEIND:0x60	2-89
PCIE_TXRX_DEBUG_SEQNUM	PCIEIND:0x61	2-90
PCIE_TXRX_TEST_MODE	PCIEIND:0x62	2-90
PCIE_TX_CREDITS_LIMIT	PCIEIND:0x7	2-81
PCIE_RX_CNTL	PCIEIND:0x70	2-90
PCIE_RX_NUM_NACK	PCIEIND:0x71	2-91
PCIE_RX_NUM_NACK_GENERATED	PCIEIND:0x72	2-91
PCIE_RX_ACK_NACK_LATENCY	PCIEIND:0x73	2-91
PCIE_RX_ACK_NACK_LATENCY_THRESHOLD	PCIEIND:0x74	2-91
PCIE_RX_TLP_HDR0	PCIEIND:0x75	2-91
PCIE_RX_TLP_HDR1	PCIEIND:0x76	2-91
PCIE_RX_TLP_HDR2	PCIEIND:0x77	2-91
PCIE_RX_TLP_HDR3	PCIEIND:0x78	2-92
PCIE_RX_TLP_HDR4	PCIEIND:0x79	2-92
PCIE_RX_TLP_CRC	PCIEIND:0x7A	2-92
PCIE_RX_DLP0	PCIEIND:0x7B	2-92
PCIE_RX_DLP1	PCIEIND:0x7C	2-92
PCIE_RX_DLP_CRC	PCIEIND:0x7D	2-92
PCIE_RX_CREDITS_ALLOCATED	PCIEIND:0x7E	2-92
PCIE_RX_CREDITS_ALLOCATED_D	PCIEIND:0x7F	2-93
PCIE_TX_CREDITS_LIMIT_D	PCIEIND:0x8	2-81
PCIE_RX_CREDITS_ALLOCATED_CPLD	PCIEIND:0x80	2-93
PCIE_RX_CREDITS_RECEIVED	PCIEIND:0x81	2-93
PCIE_RX_CREDITS_RECEIVED_D	PCIEIND:0x82	2-93
PCIE_RX_CREDITS_RECEIVED_CPLD	PCIEIND:0x83	2-93
PCIE_RX_MAL_TLP_COUNT	PCIEIND:0x84	2-93
PCIE_RX_ERR_LOG	PCIEIND:0x85	2-94
PCIE_RX_EXPECTED_SEQNUM	PCIEIND:0x86	2-94
PCIE_TX_CREDITS_LIMIT_CPLD	PCIEIND:0x9	2-82
PCIE_CI_CNTL	PCIEIND:0x90	2-94
PCIE_CI_FLUSH_CNTL	PCIEIND:0x91	2-94
PCIE_CI_PANIC	PCIEIND:0x92	2-94
PCIE_CI_HANG	PCIEIND:0x93	2-95
PCIE_LC_CNTL	PCIEIND:0xA0	2-95
PCIE_LC_N_FTS_CNTL	PCIEIND:0xA1	2-95
PCIE_LC_LINK_WIDTH_CNTL	PCIEIND:0xA2	2-97
PCIE_LC_STATE0	PCIEIND:0xA5	2-95
PCIE_LC_STATE1	PCIEIND:0xA6	2-96
PCIE_LC_STATE2	PCIEIND:0xA7	2-96
PCIE_LC_STATE3	PCIEIND:0xA8	2-96
PCIE_LC_STATE4	PCIEIND:0xA9	2-96
PCIE_LC_STATE5	PCIEIND:0xAA	2-96
PCIE_LC_FORCE_SYNC_LOSS_CNTL	PCIEIND:0xAB	2-97
PCIE_P_CNTL	PCIEIND:0xB0	2-97

Table A-11 PCIE Registers Sorted by Address (Continued)

Register Name	Address	Page
PCIE_P_CNTL2	PCIEIND:0xB1	2-98
PCIE_P_BUF_STATUS	PCIEIND:0xB2	2-98
PCIE_P_DECODER_STATUS	PCIEIND:0xB3	2-99
PCIE_P_MISC_DEBUG_STATUS	PCIEIND:0xB4	2-100
PCIE_P_IMP_CNTL_STRENGTH	PCIEIND:0xC0	2-101
PCIE_P_IMP_CNTL_UPDATE	PCIEIND:0xC1	2-102
PCIE_P_STR_CNTL_UPDATE	PCIEIND:0xC2	2-102
PCIE_P_PAD_MISC_CNTL	PCIEIND:0xC3	2-102
PCIE_P_SYMSYNC_CTL	PCIEIND:0xC4	2-102
PCIE_P_DECODE_ERR_CNTL	PCIEIND:0xC5	2-103
PCIE_ERR_CNTL	PCIEIND:0xE0	2-105
PCIE_CLK_RST_CNTL	PCIEIND:0xE1	2-105
PCIE_P_DECODE_ERR_CNT_0	PCIEIND:0xF0	2-103
PCIE_P_DECODE_ERR_CNT_1	PCIEIND:0xF1	2-103
PCIE_P_DECODE_ERR_CNT_2	PCIEIND:0xF2	2-103
PCIE_P_DECODE_ERR_CNT_3	PCIEIND:0xF3	2-103
PCIE_P_DECODE_ERR_CNT_4	PCIEIND:0xF4	2-103
PCIE_P_DECODE_ERR_CNT_5	PCIEIND:0xF5	2-103
PCIE_P_DECODE_ERR_CNT_6	PCIEIND:0xF6	2-104
PCIE_P_DECODE_ERR_CNT_7	PCIEIND:0xF7	2-104
PCIE_P_DECODE_ERR_CNT_8	PCIEIND:0xF8	2-104
PCIE_P_DECODE_ERR_CNT_9	PCIEIND:0xF9	2-104
PCIE_P_DECODE_ERR_CNT_10	PCIEIND:0xFA	2-104
PCIE_P_DECODE_ERR_CNT_11	PCIEIND:0xFB	2-104
PCIE_P_DECODE_ERR_CNT_12	PCIEIND:0xFC	2-105
PCIE_P_DECODE_ERR_CNT_13	PCIEIND:0xFD	2-105
PCIE_P_DECODE_ERR_CNT_14	PCIEIND:0xFE	2-105
PCIE_P_DECODE_ERR_CNT_15	PCIEIND:0xFF	2-105

A.13 VIP Registers Sorted By Name

Table A-12 VIP Registers Sorted by Name

Register Name	Address	Page
CAP_INT_CNTL	VIPDEC:0x908	2-133
CAP_INT_STATUS	VIPDEC:0x90C	2-134
CAP0_ANC_BUF01_BLOCK_CNT	VIPDEC:0x974	2-149
CAP0_ANC_BUF23_BLOCK_CNT	VIPDEC:0x97C	2-149
CAP0_ANC_H_WINDOW	VIPDEC:0x964	2-131
CAP0_ANC0_OFFSET	VIPDEC:0x95C	2-131
CAP0_ANC1_OFFSET	VIPDEC:0x960	2-131
CAP0_ANC2_OFFSET	VIPDEC:0x988	2-132
CAP0_ANC3_OFFSET	VIPDEC:0x98C	2-133
CAP0_BUF_PITCH	VIPDEC:0x930	2-127
CAP0_BUF_STATUS	VIPDEC:0x970	2-132
CAP0_BUF0_EVEN_OFFSET	VIPDEC:0x928	2-127
CAP0_BUF0_OFFSET	VIPDEC:0x920	2-127
CAP0_BUF1_EVEN_OFFSET	VIPDEC:0x92C	2-127
CAP0_BUF1_OFFSET	VIPDEC:0x924	2-127
CAP0_CONFIG	VIPDEC:0x958	2-129
CAP0_DEBUG	VIPDEC:0x954	2-129
CAP0_H_WINDOW	VIPDEC:0x938	2-128
CAP0_ONESHOT_BUF_OFFSET	VIPDEC:0x96C	2-131
CAP0_PORT_MODE_CNTL	VIPDEC:0x94C	2-129
CAP0_TRIG_CNTL	VIPDEC:0x950	2-129
CAP0_V_WINDOW	VIPDEC:0x934	2-128
CAP0_VBI_H_WINDOW	VIPDEC:0x948	2-128
CAP0_VBI_V_WINDOW	VIPDEC:0x944	2-128
CAP0_VBI0_OFFSET	VIPDEC:0x93C	2-128
CAP0_VBI1_OFFSET	VIPDEC:0x940	2-128
CAP0_VBI2_OFFSET	VIPDEC:0x980	2-132
CAP0_VBI3_OFFSET	VIPDEC:0x984	2-132
CAP0_VIDEO_SYNC_TEST	VIPDEC:0x968	2-131
CONFIG_GPIO	VIPDEC:0xE8	2-145
CONFIG_XSTRAP	VIPDEC:0xE4	2-144
DMA_VIP0_TABLE_ADDR	VIPDEC:0xA20	2-140
DMA_VIP1_TABLE_ADDR	VIPDEC:0xA30	2-140
DMA_VIP2_TABLE_ADDR	VIPDEC:0xA40	2-140
DMA_VIP3_TABLE_ADDR	VIPDEC:0xA50	2-141
DMA_VIPH_ABORT	VIPDEC:0xA88	2-142
DMA_VIPH_CHUNK_0	VIPDEC:0xA18	2-139
DMA_VIPH_CHUNK_1_VAL	VIPDEC:0xA1C	2-140
DMA_VIPH_MISC_CNTL	VIPDEC:0xA14	2-149
DMA_VIPH_STATUS	VIPDEC:0xA10	2-139
DMA_VIPH0_ACTIVE	VIPDEC:0xA24	2-141
DMA_VIPH0_COMMAND	VIPDEC:0xA00	2-137
DMA_VIPH0_COMMAND	VIPDEC:0xA00	2-144
DMA_VIPH1_ACTIVE	VIPDEC:0xA34	2-141

Table A-12 VIP Registers Sorted by Name (Continued)

Register Name	Address	Page
DMA_VIPH1_COMMAND	VIPDEC:0xA04	2-137
DMA_VIPH2_ACTIVE	VIPDEC:0xA44	2-141
DMA_VIPH2_COMMAND	VIPDEC:0xA08	2-138
DMA_VIPH3_ACTIVE	VIPDEC:0xA54	2-141
DMA_VIPH3_COMMAND	VIPDEC:0xA0C	2-138
EXTERN_TRIG_CNTL	VIPDEC:0x1BC	2-148
FCP_CNTL	VIPDEC:0x910	2-126
GEN_INT_CNTL	VIPDEC:0x100	2-116
GEN_INT_CNTL	VIPDEC:0x100	2-119
GEN_INT_CNTL	VIPDEC:0x100	2-136
GEN_INT_CNTL	VIPDEC:0x100	2-143
GEN_INT_CNTL	VIPDEC:0x100	2-153
GEN_INT_STATUS	VIPDEC:0x104	2-116
GEN_INT_STATUS	VIPDEC:0x104	2-119
GEN_INT_STATUS	VIPDEC:0x104	2-126
GEN_INT_STATUS	VIPDEC:0x104	2-136
GEN_INT_STATUS	VIPDEC:0x104	2-143
GEN_INT_STATUS	VIPDEC:0x104	2-153
GPIO_STRENGTH	VIPDEC:0x194	2-147
GPIOPAD_A	VIPDEC:0x19C	2-147
GPIOPAD_EN	VIPDEC:0x1A0	2-147
GPIOPAD_MASK	VIPDEC:0x198	2-147
GPIOPAD_Y	VIPDEC:0x1A4	2-147
I2C_CNTL_0	VIPDEC:0x90	2-117
I2C_CNTL_1	VIPDEC:0x94	2-118
I2C_DATA	VIPDEC:0x98	2-118
MAXX_PWM	VIPDEC:0xC64	2-152
MEDIA_0_SCRATCH	VIPDEC:0x1F0	2-149
MEDIA_1_SCRATCH	VIPDEC:0x1F4	2-149
ROM_DATA	VIPDEC:0xAC	2-148
ROM_INDEX	VIPDEC:0xA8	2-148
SEPROM_CNTL1	VIPDEC:0x1C0	2-146
SEPROM_CNTL2	VIPDEC:0x1C4	2-146
VID_BUFFER_CONTROL	VIPDEC:0x900	2-133
VIDEOMUX_CNTL	VIPDEC:0x190	2-145
VIP_HW_DEBUG	VIPDEC:0x1CC	2-148
VIPH_CH0_ABCNT	VIPDEC:0xC30	2-122
VIPH_CH0_ADDR	VIPDEC:0xC10	2-120
VIPH_CH0_DATA	VIPDEC:0xC00	2-120
VIPH_CH0_SBCNT	VIPDEC:0xC20	2-121
VIPH_CH1_ABCNT	VIPDEC:0xC34	2-122
VIPH_CH1_ADDR	VIPDEC:0xC14	2-121
VIPH_CH1_DATA	VIPDEC:0xC04	2-120
VIPH_CH1_SBCNT	VIPDEC:0xC24	2-121
VIPH_CH2_ABCNT	VIPDEC:0xC38	2-122
VIPH_CH2_ADDR	VIPDEC:0xC18	2-121

Table A-12 VIP Registers Sorted by Name (Continued)

Register Name	Address	Page
VIPH_CH2_DATA	*VIPDEC:0xC08*	*2-120*
VIPH_CH2_SBCNT	*VIPDEC:0xC28*	*2-121*
VIPH_CH3_ABCNT	*VIPDEC:0xC3C*	*2-122*
VIPH_CH3_ADDR	*VIPDEC:0xC1C*	*2-121*
VIPH_CH3_DATA	*VIPDEC:0xC0C*	*2-120*
VIPH_CH3_SBCNT	*VIPDEC:0xC2C*	*2-122*
VIPH_CONTROL	*VIPDEC:0xC40*	*2-122*
VIPH_DMA_CHUNK	*VIPDEC:0xC48*	*2-123*
VIPH_DV_INT	*VIPDEC:0xC4C*	*2-124*
VIPH_DV_LAT	*VIPDEC:0xC44*	*2-123*
VIPH_REG_ADDR	*VIPDEC:0x80*	*2-125*
VIPH_REG_DATA	*VIPDEC:0x84*	*2-125*
VIPH_TIMEOUT_STAT	*VIPDEC:0xC50*	*2-124*
VIPPAD_A	*VIPDEC:0xC58*	*2-150*
VIPPAD_EN	*VIPDEC:0xC5C*	*2-151*
VIPPAD_MASK	*VIPDEC:0xC54*	*2-150*
VIPPAD_STRENGTH	*VIPDEC:0x1B8*	*2-148*
VIPPAD_Y	*VIPDEC:0xC60*	*2-151*
ZV_LCDPAD_Y	*VIPDEC:0x1B4*	*2-148*

A.14 VIP Registers Sorted By Address

Table A-13 VIP Registers Sorted by Address

Register Name	Address	Page
GEN_INT_CNTL	VIPDEC:0x100	2-116
GEN_INT_CNTL	VIPDEC:0x100	2-119
GEN_INT_CNTL	VIPDEC:0x100	2-136
GEN_INT_CNTL	VIPDEC:0x100	2-143
GEN_INT_CNTL	VIPDEC:0x100	2-153
GEN_INT_STATUS	VIPDEC:0x104	2-116
GEN_INT_STATUS	VIPDEC:0x104	2-119
GEN_INT_STATUS	VIPDEC:0x104	2-126
GEN_INT_STATUS	VIPDEC:0x104	2-136
GEN_INT_STATUS	VIPDEC:0x104	2-143
GEN_INT_STATUS	VIPDEC:0x104	2-153
VIDEOMUX_CNTL	VIPDEC:0x190	2-145
GPIO_STRENGTH	VIPDEC:0x194	2-147
GPIOPAD_MASK	VIPDEC:0x198	2-147
GPIOPAD_A	VIPDEC:0x19C	2-147
GPIOPAD_EN	VIPDEC:0x1A0	2-147
GPIOPAD_Y	VIPDEC:0x1A4	2-147
ZV_LCDPAD_Y	VIPDEC:0x1B4	2-148
VIPPAD_STRENGTH	VIPDEC:0x1B8	2-148
EXTERN_TRIG_CNTL	VIPDEC:0x1BC	2-148
SEPROM_CNTL1	VIPDEC:0x1C0	2-146
SEPROM_CNTL2	VIPDEC:0x1C4	2-146
VIP_HW_DEBUG	VIPDEC:0x1CC	2-148
MEDIA_0_SCRATCH	VIPDEC:0x1F0	2-149
MEDIA_1_SCRATCH	VIPDEC:0x1F4	2-149
VIPH_REG_ADDR	VIPDEC:0x80	2-125
VIPH_REG_DATA	VIPDEC:0x84	2-125
I2C_CNTL_0	VIPDEC:0x90	2-117
VID_BUFFER_CONTROL	VIPDEC:0x900	2-133
CAP_INT_CNTL	VIPDEC:0x908	2-133
CAP_INT_STATUS	VIPDEC:0x90C	2-134
FCP_CNTL	VIPDEC:0x910	2-126
CAP0_BUF0_OFFSET	VIPDEC:0x920	2-127
CAP0_BUF1_OFFSET	VIPDEC:0x924	2-127
CAP0_BUF0_EVEN_OFFSET	VIPDEC:0x928	2-127
CAP0_BUF1_EVEN_OFFSET	VIPDEC:0x92C	2-127
CAP0_BUF_PITCH	VIPDEC:0x930	2-127
CAP0_V_WINDOW	VIPDEC:0x934	2-128
CAP0_H_WINDOW	VIPDEC:0x938	2-128
CAP0_VBI0_OFFSET	VIPDEC:0x93C	2-128
I2C_CNTL_1	VIPDEC:0x94	2-118
CAP0_VBI1_OFFSET	VIPDEC:0x940	2-128
CAP0_VBI_V_WINDOW	VIPDEC:0x944	2-128
CAP0_VBI_H_WINDOW	VIPDEC:0x948	2-128

Table A-13 VIP Registers Sorted by Address (Continued)

Register Name	Address	Page
CAP0_PORT_MODE_CNTL	VIPDEC:0x94C	2-129
CAP0_TRIG_CNTL	VIPDEC:0x950	2-129
CAP0_DEBUG	VIPDEC:0x954	2-129
CAP0_CONFIG	VIPDEC:0x958	2-129
CAP0_ANC0_OFFSET	VIPDEC:0x95C	2-131
CAP0_ANC1_OFFSET	VIPDEC:0x960	2-131
CAP0_ANC_H_WINDOW	VIPDEC:0x964	2-131
CAP0_VIDEO_SYNC_TEST	VIPDEC:0x968	2-131
CAP0_ONESHOT_BUF_OFFSET	VIPDEC:0x96C	2-131
CAP0_BUF_STATUS	VIPDEC:0x970	2-132
CAP0_ANC_BUF01_BLOCK_CNT	VIPDEC:0x974	2-149
CAP0_ANC_BUF23_BLOCK_CNT	VIPDEC:0x97C	2-149
I2C_DATA	VIPDEC:0x98	2-118
CAP0_VBI2_OFFSET	VIPDEC:0x980	2-132
CAP0_VBI3_OFFSET	VIPDEC:0x984	2-132
CAP0_ANC2_OFFSET	VIPDEC:0x988	2-132
CAP0_ANC3_OFFSET	VIPDEC:0x98C	2-133
DMA_VIPH0_COMMAND	VIPDEC:0xA00	2-137
DMA_VIPH0_COMMAND	VIPDEC:0xA00	2-144
DMA_VIPH1_COMMAND	VIPDEC:0xA04	2-137
DMA_VIPH2_COMMAND	VIPDEC:0xA08	2-138
DMA_VIPH3_COMMAND	VIPDEC:0xA0C	2-138
DMA_VIPH_STATUS	VIPDEC:0xA10	2-139
DMA_VIPH_MISC_CNTL	VIPDEC:0xA14	2-149
DMA_VIPH_CHUNK_0	VIPDEC:0xA18	2-139
DMA_VIPH_CHUNK_1_VAL	VIPDEC:0xA1C	2-140
DMA_VIP0_TABLE_ADDR	VIPDEC:0xA20	2-140
DMA_VIPH0_ACTIVE	VIPDEC:0xA24	2-141
DMA_VIP1_TABLE_ADDR	VIPDEC:0xA30	2-140
DMA_VIPH1_ACTIVE	VIPDEC:0xA34	2-141
DMA_VIP2_TABLE_ADDR	VIPDEC:0xA40	2-140
DMA_VIPH2_ACTIVE	VIPDEC:0xA44	2-141
DMA_VIP3_TABLE_ADDR	VIPDEC:0xA50	2-141
DMA_VIPH3_ACTIVE	VIPDEC:0xA54	2-141
ROM_INDEX	VIPDEC:0xA8	2-148
DMA_VIPH_ABORT	VIPDEC:0xA88	2-142
ROM_DATA	VIPDEC:0xAC	2-148
VIPH_CH0_DATA	VIPDEC:0xC00	2-120
VIPH_CH1_DATA	VIPDEC:0xC04	2-120
VIPH_CH2_DATA	VIPDEC:0xC08	2-120
VIPH_CH3_DATA	VIPDEC:0xC0C	2-120
VIPH_CH0_ADDR	VIPDEC:0xC10	2-120
VIPH_CH1_ADDR	VIPDEC:0xC14	2-121
VIPH_CH2_ADDR	VIPDEC:0xC18	2-121
VIPH_CH3_ADDR	VIPDEC:0xC1C	2-121
VIPH_CH0_SBCNT	VIPDEC:0xC20	2-121

Table A-13 VIP Registers Sorted by Address (Continued)

Register Name	Address	Page
VIPH_CH1_SBCNT	*VIPDEC:0xC24*	*2-121*
VIPH_CH2_SBCNT	*VIPDEC:0xC28*	*2-121*
VIPH_CH3_SBCNT	*VIPDEC:0xC2C*	*2-122*
VIPH_CH0_ABCNT	*VIPDEC:0xC30*	*2-122*
VIPH_CH1_ABCNT	*VIPDEC:0xC34*	*2-122*
VIPH_CH2_ABCNT	*VIPDEC:0xC38*	*2-122*
VIPH_CH3_ABCNT	*VIPDEC:0xC3C*	*2-122*
VIPH_CONTROL	*VIPDEC:0xC40*	*2-122*
VIPH_DV_LAT	*VIPDEC:0xC44*	*2-123*
VIPH_DMA_CHUNK	*VIPDEC:0xC48*	*2-123*
VIPH_DV_INT	*VIPDEC:0xC4C*	*2-124*
VIPH_TIMEOUT_STAT	*VIPDEC:0xC50*	*2-124*
VIPPAD_MASK	*VIPDEC:0xC54*	*2-150*
VIPPAD_A	*VIPDEC:0xC58*	*2-150*
VIPPAD_EN	*VIPDEC:0xC5C*	*2-151*
VIPPAD_Y	*VIPDEC:0xC60*	*2-151*
MAXX_PWM	*VIPDEC:0xC64*	*2-152*
CONFIG_XSTRAP	*VIPDEC:0xE4*	*2-144*
CONFIG_GPIO	*VIPDEC:0xE8*	*2-145*

A.15 VGA ATTR Registers Sorted By Name

Table A-14 VGA ATTR Registers Sorted by Name

Register Name	Address	Page
ATTR00	*VGAATTRIND:0x0*	*2-181*
ATTR01	*VGAATTRIND:0x1*	*2-181*
ATTR02	*VGAATTRIND:0x2*	*2-182*
ATTR03	*VGAATTRIND:0x3*	*2-182*
ATTR04	*VGAATTRIND:0x4*	*2-182*
ATTR05	*VGAATTRIND:0x5*	*2-182*
ATTR06	*VGAATTRIND:0x6*	*2-182*
ATTR07	*VGAATTRIND:0x7*	*2-182*
ATTR08	*VGAATTRIND:0x8*	*2-183*
ATTR09	*VGAATTRIND:0x9*	*2-183*
ATTR0A	*VGAATTRIND:0xA*	*2-183*
ATTR0B	*VGAATTRIND:0xB*	*2-183*
ATTR0C	*VGAATTRIND:0xC*	*2-183*
ATTR0D	*VGAATTRIND:0xD*	*2-183*
ATTR0E	*VGAATTRIND:0xE*	*2-184*
ATTR0F	*VGAATTRIND:0xF*	*2-184*
ATTR10	*VGAATTRIND:0x10*	*2-184*
ATTR11	*VGAATTRIND:0x11*	*2-184*
ATTR12	*VGAATTRIND:0x12*	*2-185*
ATTR13	*VGAATTRIND:0x13*	*2-185*
ATTR14	*VGAATTRIND:0x14*	*2-185*

A.16 VGA CRT Registers Sorted By Name

Table A-15 VGA CRT Registers Sorted by Name

Register Name	Address	Page
CRT00	*VGACRTIND:0x0*	*2-171*
CRT01	*VGACRTIND:0x1*	*2-171*
CRT02	*VGACRTIND:0x2*	*2-171*
CRT03	*VGACRTIND:0x3*	*2-171*
CRT04	*VGACRTIND:0x4*	*2-172*
CRT05	*VGACRTIND:0x5*	*2-172*
CRT06	*VGACRTIND:0x6*	*2-172*
CRT07	*VGACRTIND:0x7*	*2-172*
CRT08	*VGACRTIND:0x8*	*2-173*
CRT09	*VGACRTIND:0x9*	*2-173*
CRT0A	*VGACRTIND:0xA*	*2-173*
CRT0B	*VGACRTIND:0xB*	*2-174*
CRT0C	*VGACRTIND:0xC*	*2-174*
CRT0D	*VGACRTIND:0xD*	*2-174*
CRT0E	*VGACRTIND:0xE*	*2-174*
CRT0F	*VGACRTIND:0xF*	*2-175*
CRT10	*VGACRTIND:0x10*	*2-175*
CRT11	*VGACRTIND:0x11*	*2-175*
CRT12	*VGACRTIND:0x12*	*2-175*
CRT13	*VGACRTIND:0x13*	*2-176*
CRT14	*VGACRTIND:0x14*	*2-176*
CRT15	*VGACRTIND:0x15*	*2-176*
CRT16	*VGACRTIND:0x16*	*2-176*
CRT17	*VGACRTIND:0x17*	*2-176*
CRT18	*VGACRTIND:0x18*	*2-177*
CRT1E	*VGACRTIND:0x1E*	*2-177*
CRT1F	*VGACRTIND:0x1F*	*2-177*
CRT22	*VGACRTIND:0x22*	*2-177*

A.17 VGA GRPH Registers Sorted By Name

Table A-16 VGA GRPH Registers Sorted by Name

Register Name	Address	Page
GRA00	*VGAGRPHIND:0x0*	*2-178*
GRA01	*VGAGRPHIND:0x1*	*2-178*
GRA02	*VGAGRPHIND:0x2*	*2-178*
GRA03	*VGAGRPHIND:0x3*	*2-179*
GRA04	*VGAGRPHIND:0x4*	*2-179*
GRA05	*VGAGRPHIND:0x5*	*2-179*
GRA06	*VGAGRPHIND:0x6*	*2-180*
GRA07	*VGAGRPHIND:0x7*	*2-180*
GRA08	*VGAGRPHIND:0x8*	*2-180*

A.18 VGA SEQ Registers Sorted By Name

Table A-17 VGA SEQ Registers Sorted by Name

Register Name	Address	Page
SEQ00	*VGASEQIND:0x0*	*2-169*
SEQ01	*VGASEQIND:0x1*	*2-169*
SEQ02	*VGASEQIND:0x2*	*2-169*
SEQ03	*VGASEQIND:0x3*	*2-170*
SEQ04	*VGASEQIND:0x4*	*2-170*

A.19 All Registers Sorted by Name

Table A-18 All Registers Sorted by Name

Table A-18 All Registers Sorted by Name (Continued)

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CAP0_ANC0_OFFSET	2-131
CAP0_ANC1_OFFSET	2-131
CAP0_ANC2_OFFSET	2-132
CAP0_ANC3_OFFSET	2-133
CAP0_BUF_PITCH	2-127
CAP0_BUF_STATUS	2-132
CAP0_BUF0_EVEN_OFFSET	2-127
CAP0_BUF0_OFFSET	2-127
CAP0_BUF1_EVEN_OFFSET	2-127
CAP0_BUF1_OFFSET	2-127
CAP0_CONFIG	2-129
CAP0_DEBUG	2-129
CAP0_H_WINDOW	2-128
CAP0_ONESHOT_BUF_OFFSET	2-131
CAP0_PORT_MODE_CNTL	2-129
CAP0_TRIG_CNTL	2-129
CAP0_V_WINDOW	2-128
CAP0_VBI_H_WINDOW	2-128
CAP0_VBI_V_WINDOW	2-128
CAP0_VBI0_OFFSET	2-128
CAP0_VBI1_OFFSET	2-128
CAP0_VBI2_OFFSET	2-132
CAP0_VBI3_OFFSET	2-132
CAP0_VIDEO_SYNC_TEST	2-131
CAPABILITIES_PTR	2-64
CAPTURE_START_STATUS	2-333
CG_CLKPIN_CNTL	2-163
CG_MISC_REG	2-161
CG_TC_JTAG_0	2-164
CG_TC_JTAG_1	2-164
CLOCK_CNTL_DATA	2-155
CLOCK_CNTL_INDEX	2-155
COMMAND	2-61
CONFIG_APER_0_BASE	2-59
CONFIG_APER_1_BASE	2-60
CONFIG_APER_SIZE	2-60
CONFIG_CNTL	2-59
CONFIG_GPIO	2-145
CONFIG_MEMSIZE	2-59
CONFIG_REG_1_BASE	2-60

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CONFIG_REG_APER_SIZE	2-60
CONFIG_XSTRAP	2-144
CRT00	2-171
CRT01	2-171
CRT02	2-171
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CRT04	2-172
CRT05	2-172
CRT06	2-172
CRT07	2-172
CRT08	2-173
CRT09	2-173
CRT0A	2-173
CRT0B	2-174
CRT0C	2-174
CRT0D	2-174
CRT0E	2-174
CRT0F	2-175
CRT10	2-175
CRT11	2-175
CRT12	2-175
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CRT14	2-176
CRT15	2-176
CRT16	2-176
CRT17	2-176
CRT18	2-177
CRT1E	2-177
CRT1F	2-177
CRT22	2-177
CRTC_EXT_CNTL	2-196
CRTC8_DATA	2-171
CRTC8_DATA	2-196
CRTC8_IDX	2-171
CRTC8_IDX	2-196
D1COLOR_MATRIX_COEF_1_1	2-217
D1COLOR_MATRIX_COEF_1_2	2-217
D1COLOR_MATRIX_COEF_1_3	2-218
D1COLOR_MATRIX_COEF_1_4	2-218
D1COLOR_MATRIX_COEF_2_1	2-218

Table A-18 All Registers Sorted by Name (Continued)

Table A-18 All Registers Sorted by Name (Continued)

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D1CRTC_STEREO_FORCE_NEXT_EYE	2-273
D1CRTC_STEREO_STATUS	2-277
D1CRTC_TRIGA_CNTL	2-270
D1CRTC_TRIGA_MANUAL_TRIG	2-271
D1CRTC_TRIGB_CNTL	2-271
D1CRTC_TRIGB_MANUAL_TRIG	2-272
D1CRTC_UPDATE_LOCK	2-279
D1CRTC_V_BLANK_START_END	2-268
D1CRTC_V_SYNC_A	2-269
D1CRTC_V_SYNC_A_CNTL	2-269
D1CRTC_V_SYNC_B	2-269
D1CRTC_V_SYNC_B_CNTL	2-269
D1CRTC_V_TOTAL	2-268
D1CRTC_VERT_SYNC_CONTROL	2-277
D1CRTC_VGA_PARAMETER_CAPTURE_MODE	2-280
D1CUR_COLOR1	2-223
D1CUR_COLOR2	2-223
D1CUR_CONTROL	2-222
D1CUR_HOT_SPOT	2-223
D1CUR_POSITION	2-222
D1CUR_SIZE	2-222
D1CUR_SURFACE_ADDRESS	2-222
D1CUR_UPDATE	2-223
D1GRPH_ALPHA	2-213
D1GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL	2-217
D1GRPH_CONTROL	2-198
D1GRPH_ENABLE	2-198
D1GRPH_FLIP_CONTROL	2-202
D1GRPH_KEY_RANGE_ALPHA	2-215
D1GRPH_KEY_RANGE_BLUE	2-215
D1GRPH_KEY_RANGE_GREEN	2-214
D1GRPH_KEY_RANGE_RED	2-214
D1GRPH_LUT_SEL	2-199
D1GRPH_PITCH	2-200
D1GRPH_PRIMARY_SURFACE_ADDRESS	2-199
D1GRPH_SECONDARY_SURFACE_ADDRESS	2-200
D1GRPH_SURFACE_ADDRESS_INUSE	2-202
D1GRPH_SURFACE_OFFSET_X	2-200
D1GRPH_SURFACE_OFFSET_Y	2-200
D1GRPH_UPDATE	2-201

Table A-18 All Registers Sorted by Name (Continued)

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D1GRPH_X_START	2-200
D1GRPH_Y_END	2-201
D1GRPH_Y_START	2-201
D1ICON_COLOR1	2-224
D1ICON_COLOR2	2-225
D1ICON_CONTROL	2-224
D1ICON_SIZE	2-224
D1ICON_START_POSITION	2-224
D1ICON_SURFACE_ADDRESS	2-224
D1ICON_UPDATE	2-225
D1MODE_MASTER_UPDATE_LOCK	2-279
D1MODE_MASTER_UPDATE_MODE	2-279
D1OVL_ALPHA	2-213
D1OVL_ALPHA_CONTROL	2-214
D1OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	2-217
D1OVL_CONTROL1	2-203
D1OVL_CONTROL2	2-203
D1OVL_ENABLE	2-203
D1OVL_END	2-205
D1OVL_KEY_ALPHA	2-216
D1OVL_KEY_CONTROL	2-213
D1OVL_KEY_RANGE_BLUE_CB	2-216
D1OVL_KEY_RANGE_GREEN_Y	2-215
D1OVL_KEY_RANGE_RED_CR	2-215
D1OVL_MATRIX_COEF_1_1	2-206
D1OVL_MATRIX_COEF_1_2	2-206
D1OVL_MATRIX_COEF_1_3	2-206
D1OVL_MATRIX_COEF_1_4	2-206
D1OVL_MATRIX_COEF_2_1	2-207
D1OVL_MATRIX_COEF_2_2	2-207
D1OVL_MATRIX_COEF_2_3	2-207
D1OVL_MATRIX_COEF_2_4	2-207
D1OVL_MATRIX_COEF_3_1	2-207
D1OVL_MATRIX_COEF_3_2	2-208
D1OVL_MATRIX_COEF_3_3	2-208
D1OVL_MATRIX_COEF_3_4	2-208
D1OVL_MATRIX_TRANSFORM_EN	2-206
D1OVL_PITCH	2-204
D1OVL_PWL_0TOF	2-209

Table A-18 All Registers Sorted by Name (Continued)

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D1OVL_PWL_10TO1F	2-209
D1OVL_PWL_140TO17F	2-210
D1OVL_PWL_180TO1BF	2-210
D1OVL_PWL_1C0TO1FF	2-210
D1OVL_PWL_200TO23F	2-211
D1OVL_PWL_20TO3F	2-209
D1OVL_PWL_240TO27F	2-211
D1OVL_PWL_280TO2BF	2-211
D1OVL_PWL_2C0TO2FF	2-211
D1OVL_PWL_300TO33F	2-211
D1OVL_PWL_340TO37F	2-212
D1OVL_PWL_380TO3BF	2-212
D1OVL_PWL_3C0TO3FF	2-212
D1OVL_PWL_40TO7F	2-209
D1OVL_PWL_80TOBF	2-210
D1OVL_PWL_C0TOFF	2-210
D1OVL_PWL_TRANSFORM_EN	2-209
D1OVL_START	2-204
D1OVL_SURFACE_ADDRESS	2-204
D1OVL_SURFACE_ADDRESS_INUSE	2-205
D1OVL_SURFACE_OFFSET_X	2-204
D1OVL_SURFACE_OFFSET_Y	2-204
D1OVL_UPDATE	2-205
D1VGA_CONTROL	2-189
D2COLOR_MATRIX_COEF_1_1	2-250
D2COLOR_MATRIX_COEF_1_2	2-250
D2COLOR_MATRIX_COEF_1_3	2-250
D2COLOR_MATRIX_COEF_1_4	2-251
D2COLOR_MATRIX_COEF_2_1	2-251
D2COLOR_MATRIX_COEF_2_2	2-251
D2COLOR_MATRIX_COEF_2_3	2-251
D2COLOR_MATRIX_COEF_2_4	2-252
D2COLOR_MATRIX_COEF_3_1	2-252
D2COLOR_MATRIX_COEF_3_2	2-252
D2COLOR_MATRIX_COEF_3_3	2-252
D2COLOR_MATRIX_COEF_3_4	2-253
D2COLOR_SPACE_CONVERT	2-254
D2CRTC_BLACK_COLOR	2-289
D2CRTC_BLANK_CONTROL	2-287

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D2CRTC_CONTROL	2-287
D2CRTC_COUNT_CONTROL	2-290
D2CRTC_COUNT_RESET	2-290
D2CRTC_DOUBLE_BUFFER_CONTROL	2-293
D2CRTC_FLOW_CONTROL	2-286
D2CRTC_FORCE_COUNT_NOW_CNTL	2-286
D2CRTC_H_BLANK_START_END	2-281
D2CRTC_H_SYNC_A	2-281
D2CRTC_H_SYNC_A_CNTL	2-281
D2CRTC_H_SYNC_B	2-281
D2CRTC_H_SYNC_B_CNTL	2-282
D2CRTC_H_TOTAL	2-280
D2CRTC_INTERLACE_CONTROL	2-288
D2CRTC_INTERLACE_STATUS	2-288
D2CRTC_INTERRUPT_CONTROL	2-292
D2CRTC_MANUAL_FORCE_VSYNC_NEXT_LINE	2-290
D2CRTC_OVERSCAN_COLOR	2-288
D2CRTC_PIXEL_DATA_READBACK	2-287
D2CRTC_SNAPSHOT_CONTROL	2-292
D2CRTC_SNAPSHOT_FRAME	2-292
D2CRTC_SNAPSHOT_POSITION	2-292
D2CRTC_SNAPSHOT_STATUS	2-291
D2CRTC_START_LINE_CONTROL	2-292
D2CRTC_STATUS	2-289
D2CRTC_STATUS_FRAME_COUNT	2-290
D2CRTC_STATUS_HV_COUNT	2-290
D2CRTC_STATUS_POSITION	2-289
D2CRTC_STATUS_VF_COUNT	2-290
D2CRTC_STEREO_CONTROL	2-291
D2CRTC_STEREO_FORCE_NEXT_EYE	2-287
D2CRTC_STEREO_STATUS	2-291
D2CRTC_TRIGA_CNTL	2-283
D2CRTC_TRIGA_MANUAL_TRIG	2-284
D2CRTC_TRIGB_CNTL	2-285
D2CRTC_TRIGB_MANUAL_TRIG	2-286
D2CRTC_UPDATE_LOCK	2-293
D2CRTC_V_BLANK_START_END	2-282
D2CRTC_V_SYNC_A	2-282
D2CRTC_V_SYNC_A_CNTL	2-283

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D2CRTC_V_SYNC_B_CNTL	2-283
D2CRTC_V_TOTAL	2-282
D2CRTC_VERT_SYNC_CONTROL	2-290
D2CRTC_VGA_PARAMETER_CAPTURE_MODE	2-294
D2CUR_COLOR1	2-256
D2CUR_COLOR2	2-256
D2CUR_CONTROL	2-255
D2CUR_HOT_SPOT	2-256
D2CUR_POSITION	2-255
D2CUR_SIZE	2-255
D2CUR_SURFACE_ADDRESS	2-255
D2CUR_UPDATE	2-256
D2GRPH_ALPHA	2-246
D2GRPH_COLOR_MATRIX_TRANSFORMATION_CNTL	2-250
D2GRPH_CONTROL	2-231
D2GRPH_ENABLE	2-231
D2GRPH_FLIP_CONTROL	2-235
D2GRPH_KEY_RANGE_ALPHA	2-248
D2GRPH_KEY_RANGE_BLUE	2-248
D2GRPH_KEY_RANGE_GREEN	2-247
D2GRPH_KEY_RANGE_RED	2-247
D2GRPH_LUT_SEL	2-232
D2GRPH_PITCH	2-233
D2GRPH_PRIMARY_SURFACE_ADDRESS	2-232
D2GRPH_SECONDARY_SURFACE_ADDRESS	2-233
D2GRPH_SURFACE_ADDRESS_INUSE	2-235
D2GRPH_SURFACE_OFFSET_X	2-233
D2GRPH_SURFACE_OFFSET_Y	2-233
D2GRPH_UPDATE	2-234
D2GRPH_X_END	2-234
D2GRPH_X_START	2-233
D2GRPH_Y_END	2-234
D2GRPH_Y_START	2-234
D2ICON_COLOR1	2-257
D2ICON_COLOR2	2-258
D2ICON_CONTROL	2-257
D2ICON_SIZE	2-257
D2ICON_START_POSITION	2-257
D2ICON_SURFACE_ADDRESS	2-257

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D2MODE_MASTER_UPDATE_MODE	2-293
D2OVL_ALPHA	2-246
D2OVL_ALPHA_CONTROL	2-247
D2OVL_COLOR_MATRIX_TRANSFORMATION_CNTL	2-250
D2OVL_CONTROL1	2-236
D2OVL_CONTROL2	2-236
D2OVL_ENABLE	2-236
D2OVL_END	2-238
D2OVL_KEY_ALPHA	2-249
D2OVL_KEY_CONTROL	2-246
D2OVL_KEY_RANGE_BLUE_CB	2-248
D2OVL_KEY_RANGE_GREEN_Y	2-248
D2OVL_KEY_RANGE_RED_CR	2-248
D2OVL_MATRIX_COEF_1_1	2-239
D2OVL_MATRIX_COEF_1_2	2-239
D2OVL_MATRIX_COEF_1_3	2-239
D2OVL_MATRIX_COEF_1_4	2-239
D2OVL_MATRIX_COEF_2_1	2-240
D2OVL_MATRIX_COEF_2_2	2-240
D2OVL_MATRIX_COEF_2_3	2-240
D2OVL_MATRIX_COEF_2_4	2-240
D2OVL_MATRIX_COEF_3_1	2-240
D2OVL_MATRIX_COEF_3_2	2-241
D2OVL_MATRIX_COEF_3_3	2-241
D2OVL_MATRIX_COEF_3_4	2-241
D2OVL_MATRIX_TRANSFORM_EN	2-239
D2OVL_PITCH	2-237
D2OVL_PWL_0TOF	2-242
D2OVL_PWL_100TO13F	2-243
D2OVL_PWL_10TO1F	2-242
D2OVL_PWL_140TO17F	2-243
D2OVL_PWL_180TO1BF	2-243
D2OVL_PWL_1C0TO1FF	2-243
D2OVL_PWL_200TO23F	2-244
D2OVL_PWL_20TO3F	2-242
D2OVL_PWL_240TO27F	2-244
D2OVL_PWL_280TO2BF	2-244
D2OVL_PWL_2C0TO2FF	2-244

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D2OVL_PWL_340TO37F	2-245
D2OVL_PWL_380TO3BF	2-245
D2OVL_PWL_3C0TO3FF	2-245
D2OVL_PWL_40TO7F	2-242
D2OVL_PWL_80TOBF	2-243
D2OVL_PWL_C0TOFF	2-243
D2OVL_PWL_TRANSFORM_EN	2-242
D2OVL_START	2-237
D2OVL_SURFACE_ADDRESS	2-237
D2OVL_SURFACE_ADDRESS_INUSE	2-238
D2OVL_SURFACE_OFFSET_X	2-237
D2OVL_SURFACE_OFFSET_Y	2-237
D2OVL_UPDATE	2-238
D2VGA_CONTROL	2-190
DAC_DATA	2-168
DAC_MASK	2-168
DAC_R_INDEX	2-168
DAC_W_INDEX	2-168
DACA_AUTODETECT_CONTROL	2-297
DACA_AUTODETECT_CONTROL2	2-297
DACA_AUTODETECT_INT_CONTROL	2-298
DACA_AUTODETECT_STATUS	2-297
DACA_COMPARATOR_ENABLE	2-299
DACA_COMPARATOR_OUTPUT	2-300
DACA_CONTROL1	2-298
DACA_CONTROL2	2-299
DACA_CRC_CONTROL	2-295
DACA_CRC_EN	2-295
DACA_CRC_SIG_CONTROL	2-296
DACA_CRC_SIG_CONTROL_MASK	2-296
DACA_CRC_SIG_RGB	2-296
DACA_CRC_SIG_RGB_MASK	2-295
DACA_ENABLE	2-295
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DACA_FORCE_OUTPUT_CNTL	2-298
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DACB_AUTODETECT_INT_CONTROL	2-303
DACB_AUTODETECT_STATUS	2-303
DACB_COMPARATOR_ENABLE	2-305
DACB_COMPARATOR_OUTPUT	2-305
DACB_CONTROL1	2-304
DACB_CONTROL2	2-304
DACB_CRC_CONTROL	2-301
DACB_CRC_EN	2-301
DACB_CRC_SIG_CONTROL	2-302
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DACB_CRC_SIG_RGB	2-301
DACB_CRC_SIG_RGB_MASK	2-301
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DACB_FORCE_DATA	2-304
DACB_FORCE_OUTPUT_CNTL	2-303
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DC_GPIO_DDC1_EN	2-328
DC_GPIO_DDC1_MASK	2-328
DC_GPIO_DDC1_Y	2-328
DC_GPIO_DDC2_A	2-329
DC_GPIO_DDC2_EN	2-329
DC_GPIO_DDC2_MASK	2-328
DC_GPIO_DDC2_Y	2-329
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DC_GPIO_DDC3_EN	2-330
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DC_GPIO_DVODATA_EN	2-327
DC_GPIO_DVODATA_MASK	2-327
DC_GPIO_DVODATA_Y	2-327
DC_GPIO_GENERIC_A	2-326
DC_GPIO_GENERIC_EN	2-326
DC_GPIO_GENERIC_MASK	2-326
DC_GPIO_GENERIC_Y	2-326
DC_GPIO_HPD_A	2-332
DC_GPIO_HPD_EN	2-332
DC_GPIO_HPD_MASK	2-331
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DC_GPIO_PAD_STRENGTH_1	2-334
DC_GPIO_PAD_STRENGTH_2	2-334
DC_GPIO_PWRSEQ_A	2-332
DC_GPIO_PWRSEQ_EN	2-333
DC_GPIO_PWRSEQ_MASK	2-332
DC_GPIO_PWRSEQ_Y	2-333
DC_GPIO_SYNCA_A	2-330
DC_GPIO_SYNCA_EN	2-330
DC_GPIO_SYNCA_MASK	2-330
DC_GPIO_SYNCA_Y	2-331
DC_GPIO_SYNCB_A	2-331
DC_GPIO_SYNCB_EN	2-331
DC_GPIO_SYNCB_MASK	2-331
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DC_HOT_PLUG_DETECT1_INT_CONTROL	2-321
DC_HOT_PLUG_DETECT1_INT_STATUS	2-321
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DC_HOT_PLUG_DETECT2_INT_CONTROL	2-321
DC_HOT_PLUG_DETECT2_INT_STATUS	2-321
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Appendix B
Revision History

Rev 0.1 (June 05)

- This document is based on the engineering document created on June 16.

Rev 0.2 (Aug 05)

- This document is based on the engineering document created on Aug 9.

Rev 0.3 (Sept 05)

- Added section “LVDS Registers” on page 2-340.

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