3GA GRAPHICS ACCELERATOR

Preliminary Data Sheet

Features

The ARTIST Graphics 3GA™ graphics accelerator is a 64 bit, state-of-the-art 3D graphics processor designed to accelerate graphical user interfaces, 2D and 3D vector drawing, and 3D rendering.

- **High performance 3D graphics processor**
  - 16 bit Z-buffer for automatic 3D hidden surface removal
  - Secondary 16 bit Z-buffer for arbitrary frontal Z clipping
  - Gouraud shading for realistic 3D rendering
  - Dithering for superior shading at 8 and 16 bits per pixel
  - Texture mapping to map 2D textures onto 3D surfaces
  - Six arithmetic raster operations (Add, Add with Saturation, Sub, Sub with Saturation, Min, Max)
- **Powerful 2D GUI accelerator**
  - Accelerated drawing at 8, 16, 24 and 32 bits per pixel
  - 256 Microsoft® Windows™ raster operations in hardware
  - Color expanding BitBLTs provide extremely fast text
  - On-chip 8 x 8 color expanding pattern
  - Variable sized color pattern up to 64 x 64 pixels
  - Rectangular and arbitrary region clipping
  - Eight stencil modes
  - Multicolored “styled” lines and polylines
- **Display controller**
  - VRAM based display controller for maximum performance
  - Supports displays up to 2048 x 2048 pixels
  - Refresh rates up to 90Hz at 1600 x 1200 resolution
  - VESA® DPMS™ support for green PC applications
- **Video interface**
  - Shared frame buffer interface for multimedia
  - Supports S3® Vision/VA™ full screen video with a shared frame buffer
- **Flexible local memory**
  - 64 bit wide memory bus
  - VRAM block write support
  - Supports 1 to 4 megabytes VRAM display memory
  - Supports 0 to 8 megabytes of off screen DRAM for Z-buffers, fonts, etc.
- **Single chip accelerator**
  - On-chip 32 bit VGA for fast DOS performance
  - Support for Microsoft Plug & Play ISA specification
  - Interfaces directly to VESA VL-Bus™ and PCI™ with no glue logic
  - Interfaces to ISA bus with two 74F245 buffers
  - 128 byte host FIFO for passing data and commands
  - 240 pin plastic quad flat pack
  - 50 MHz clock frequency
- **Software drivers**
  - Microsoft Windows 3.1, Windows NT™ and Windows ‘95™ (when released)
  - OS/2® 2.1 and OS/2 Warp
  - AutoCAD®
  - Hoops
  - OpenGL
  - 3D APIs: Argonaut BRender, Criterion Software RenderWare, Rendermorphic Reality Lab, Intel 3DR

System Overview

A graphics system designed around the 3GA graphics accelerator requires only VRAM, a video DAC, clock generator, and a small number of external buffers. The 3GA graphics accelerator supports a 64 bit wide data path to its local memory array and contains interfaces to an external clock generator, DAC, and ROM BIOS.

Performance

Estimated performance, based on 8 bits per pixel, 10 pixel lines, 50 pixel triangles, 90MHz Pentium CPU, PCI bus.

- 2D lines ..... 1,600,000 lines/second
- 3D lines (shaded, Z-buffered) ..... 280,000 lines/second
- 2D texture mapped triangles ..... 75,000 triangles/second
- 3D texture mapped triangles (Z-buffered) ..... 65,000 triangles/second
- 3D Gouraud shaded triangles (Z-buffered) ..... 110,000 triangles/second
- Screen-to-screen BitBLTs ..... 80,000,000 pixels/second
- Memory-to-screen BitBLTs (color expanding) ..... 245,000,000 pixels/second
- Fill rate ..... 1,100,000,000 pixels/second

Pin Information

The 3GA graphics accelerator is available in a 240-pin quad flat pack for PCI, ISA, and VESA VL-Bus configurations.

Pin Diagram — PCI Bus

Pin Diagram — VESA VL-Bus

Pin Diagram — ISA Bus

3GA Pin Descriptions

The following table gives a brief description of each of the 3GA graphic accelerator's pins and their function for the PCI, ISA, and VESA VL-Bus interface:

I Defines an input signal
O Defines an output signal
I/O Defines a bi-directional signal

PCI Bus Interface

Name	Type	Pin Number(s)	Description
AD[31-0]	I/O	222, 223, 227, 228, 229, 230, 231, 232, 235, 236, 237, 238, 239, 2, 3, 4, 14, 15, 18, 19, 20, 21, 22, 23, 26, 27, 28, 29, 30, 32, 33, 34	PCI Multiplexed Address/Data Bus. A bus transaction consists of an address phase followed by one or more data phases.
$\overline{C/BE[3-0]}$	I	233, 5, 13, 24	PCI Multiplexed Bus Commands/Byte Enables. During the address phase they define the bus command. During the data phase they are used as byte enables. When used as byte enables these signals are active low.
$\overline{RST}$	I	220	PCI System Reset. Resets PCI-specific registers, 3GA registers, and sets 3GA state machines to a known state. Active low.
CLK	I	221	PCI System Clock. Provides timing for all transactions on the PCI interface. All timing is referenced to the rising edge.
IDSEL	I	219	PCI Initialization Device Select. Used as a chip select during configuration read and write transactions. Active high.
$\overline{FRAME}$	I	6	PCI Cycle Frame. Indicates beginning and duration of an access. Active low.

PCI Bus Interface (continued)

Name	Type	Pin Number(s)	Description
$\overline{\text{IRDY}}$	I	7	PCI Initiator Ready. Indicates the initiating agent's ability to complete the current data phase of the transaction. Active low.
$\overline{\text{INTA}}$	O	218	PCI Interrupt A. Used to request an interrupt. Active low.
$\overline{\text{TRDY}}$	O	8	PCI Target Ready. Indicates the target agent's ability to complete the current data phase of the transaction. Active low.
$\overline{\text{DEVSEL}}$	O	9	PCI Device Select. Indicates the driving device has decoded its address as the target of the current access. Active low.
$\overline{\text{STOP}}$	O	11	PCI Stop. Indicates the current target is requesting the master to stop the current transaction. Active low.
PAR	O	12	PCI Parity. Parity is even across AD[31-0] and C/BE[3-0]. Active high.
Unused PCI	I	184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 211, 212, 213, 214, 215, 216, 217	These pins are not used when the 3GA is configured for the PCI interface, but they must be connected to ground.

VESA VL-Bus Interface

Name	Type	Pin Number(s)	Description
A[31-2]	I	219, 218, 217, 216, 215, 214, 213, 196, 212, 211, 207, 206, 205, 204, 203, 202, 201, 200, 199, 198, 197, 193, 192, 191, 190, 189, 188, 187, 186, 185	VL-Bus Address Bus. Provides memory or I/O port addresses to the VL-Bus target.
D[31-0]	I/O	222, 223, 227, 228, 229, 230, 231, 232, 235, 236, 237, 238, 239, 2, 3, 4, 14, 15, 18, 19, 20, 21, 22, 23, 26, 27, 28, 29, 30, 32, 33, 34	VL-Bus Data Bus. Provides a bi-directional data path between VL-Bus devices and the CPU.
$\overline{BE[3-0]}$	I	6, 7, 8, 9	VL-Bus Byte Enables. Indicates which byte lanes of the 32-bit data bus are involved with the current VL-Bus transfer. Active low.
LCLK	I	221	VL-Bus Local CPU Clock. A 1x clock that follows the same phase as a 486-type CPU. The rising edge of the clock signifies the change of CPU states.
$W / \overline{R}$	I	184	VL-Bus Write or Read Status. Indicates the type of access currently executing on the VL-Bus. Write access is indicated by a high, while a read access is indicated by a low.
$M / \overline{IO}$	I	5	VL-Bus Memory or I/O Status. Indicates the type of access currently executing on the VL-Bus. Memory access is indicated by a high, while an I/O access is indicated by a low.
$\overline{ADS}$	I	24	VL-Bus Address Data Strobe. Indicates the start of the VL-Bus cycle. Active low.
$\overline{RDYRTN}$	I	13	VL-Bus Ready Return. Establishes a handshake so the VL-Bus target knows when the cycle has ended. Active low.

VESA VL-Bus Interface (continued)

Name	Type	Pin Number(s)	Description
$\overline{\text{RESET}}$	I	220	VL-Bus System Reset. A master reset that is asserted after system power up and before any valid CPU cycles take place. Active low.
IRQ	O	233	Interrupt Request Line. Used to request an interrupt. Compatible with the ISA interrupt request lines. Triggered on the Rising edge.
$\overline{\text{LRDY}}$	O	12	VL-Bus Local Ready. Begins the handshake that terminates the current active bus cycle when the target is not bursting. Active low.
$\overline{\text{LDEV}}$	O	11	VL-Bus Local Device. Indicates that the current address on the VL-Bus is addressing the VL-Bus target. Active low.

ISA Bus Interface

Name	Type	Pin Number(s)	Description
SD[15-0]	I/O	14, 15, 18, 19, 20, 21, 22, 23, 26, 27, 28, 29, 30, 32, 33, 34	ISA System Data Bus. Used for data transfer.
SA[16-0]	I	202, 201, 200, 199, 198, 197, 193, 192, 191, 190, 189, 188, 187, 186, 185, 11, 6	ISA System Address Bus. They are used to address I/O and Memory cycles and are valid throughout the bus command cycle.
LA[23-17]	I	212, 211, 207, 206, 205, 204, 203	ISA Latchable Address Bus. Used to address memory cycles and are not valid throughout the bus command cycle.
$\overline{\text{MEMW}}$	I	213	ISA Memory Write. Is asserted to indicate that the addressed memory slave may latch data from the memory bus. Active low.

ISA Bus Interface (continued)

Name	Type	Pin Number(s)	Description
$\overline{\text{MEMR}}$	I	214	ISA Memory Read. Is asserted to indicate that the addressed memory slave should drive data onto the memory bus. Active low.
$\overline{\text{IOW}}$	I	8	ISA I/O Write. Is asserted to indicate that the addressed I/O slave may latch data from the data bus. Active low.
$\overline{\text{IOR}}$	I	7	ISA I/O Read. Is asserted to indicate that the addressed I/O slave should drive data onto the data bus. Active low.
$\overline{\text{SBHE}}$	I	216	ISA System Bus High Enable. Indicates that expansion boards that support 16-bit data transfers should drive data on the high half of the system data bus. Active low.
BALE	I	217	ISA Buffered Address Latch Enable. Indicates that a valid address is present in the latchable address bus. Active High.
$\overline{\text{REFRESH}}$	I	5	ISA Refresh. Indicates a refresh cycle in progress. Active low.
AEN	I	13	ISA Address Enable. Indicates that the I/O slave may respond to addresses and I/O commands on the bus. Active high.
BCLK	I	215	ISA Bus Clock. Provided to synchronize events with the main system clock.
SYSCLK	I	221	3GA System Clock. Used to synchronize the host interface to the local interface.
$\overline{\text{RESDRV}}$	I	220	ISA Reset Driver. When asserted causes a hardware reset of ISA expansion boards. Active low.

ISA Bus Interface (continued)

Name	Type	Pin Number(s)	Description
Unused ISA	I	4, 3, 2, 239, 238, 237, 236, 235, 232, 231, 230, 229, 228, 227, 223, 222	These pins are not used when the 3GA is configured for the ISA interface, but they must be connected to VCC through a pull-up resistor.
IRQ10	O	233	ISA Interrupt Request Level 10. Used to interrupt the CPU to request some service. Positive edge triggered.
IRQ12	O	219	ISA Interrupt Request Level 12. Used to interrupt the CPU to request some service. Positive edge triggered.
$\overline{\text{MCS16}}$	O	184	ISA Memory Chip Select 16. Signals the system that the ISA memory is capable of transferring 16 bits of data at once. Active low.
CHRDY	O	196	ISA Channel Ready. An I/O or memory slave can negate the signal to lengthen the bus cycle from the default time. Active high.
$\overline{\text{NOWS}}$	O	218	ISA No Wait State. An ISA memory slave asserts this signal after the address and command have been decoded to indicate that the remaining clock cycles are not required. Active low.
HDIR	O	9	Host Data Buffer Direction. Controls the direction of the data buffers for read and write operations. A high it indicates a write to the 3GA. A low indicates a read from the 3GA.
$\overline{\text{HDEN0}}$	O	24	Host Data Buffer Enable 0. Enables the data buffer that is connected to the 8 low order bits of the host data bus. Active low.
$\overline{\text{HDEN1}}$	O	12	Host Data Buffer Enable 1. Enables the data buffer that is connected to the 8 high order bits of the host data bus. Active low.

Clock Inputs

Name	Type	Pin Number(s)	Description
PIXCLK	I	75	VGA Pixel Clock. The internal VGA's pixel clock on the 3GA. Used exclusively as the pixel clock to the internal VGA. Up to 80MHz.
SCLKIN	I	89	3GA Shift Clock Input. Free Running reference clock. Not gated off with the blanking signal. Used to generate shift clock outputs to the frame buffer, load clock to the DAC, and as a reference for all video signals in non VGA modes. Up to 50MHz/
SYSCLK	I	150	3GA System Clock. 50MHz clock provides timing for all local data bus transactions.

Memory Interface

Name	Type	Pin Number(s)	Description
RCA[9-0]	O	81, 80, 79, 78, 77, 72, 71, 70, 69, 68	Local Memory Address Bus. Specify the row and column address for the local memory.
LD[63-0]	I/O	178, 177, 176, 175, 174, 173, 172, 171, 170, 169, 168, 167, 166, 165, 162, 161, 160, 159, 158, 157, 156, 155, 154, 153, 152, 147, 146, 145, 144, 143, 142, 141, 139, 138, 137, 134, 133, 132, 131, 130, 129, 128, 127, 126, 125, 124, 123, 118, 117, 116, 115, 114, 113, 112, 111, 110, 109, 108, 107, 106, 103, 102, 101, 100	Local Memory Data Bus. LD[31-0] are also used as system configuration strapping bits, that are sensed at reset. LD[63-32] are used to provide an interface for local devices such as a RAMDAC, and a BIOS.
SCLK[1-0]	O	86, 87	Video Memory Shift Clock. SCLK[1-0] are used to shift pixel data out of the VRAM to the RAMDAC. Serial data is accessed on the rising edge of SCLK[1-0].

Memory Interface (continued)

Name	Type	Pin Number(s)	Description
$\overline{\text{SOE}}[1-0]$	O	58, 56	Video Memory Serial Output Enable. Enable/disable the serial data outputs on the VRAM. Active low.
DSF	O	65	Video Memory Special Function Select. Determines which of the special functions are invoked on VRAM cycles. Active high.
$\overline{\text{DTOE}}$	O	63	Video Memory Data Transfer Output Enable. Selects either DRAM or transfer operation on the VRAM. Active low.
$\overline{\text{VGADTOE}}$	O	53	Video Memory Data Transfer Output Enable for the VRAM that is used by internal VGA. Selects either DRAM or transfer operation on the VRAM. Active low.
$\overline{\text{VWE}}$	O	64	Video Memory Write enable. Enables data to be written to the VRAM. Active low.
$\overline{\text{VGAWE}}$	O	54	Video Memory Write enable for the VRAM that is used by the internal VGA. Enables data to be written to the VRAM. Active low.
$\overline{\text{DWE}}$	O	67	DRAM Write Enable. DWE- enables data to be written to the expansion DRAM. Active low.
$\overline{\text{VRAS}}[1-0]$	O	57, 55	Video Memory Row Address Strobe. Initiates all DRAM cycles and transfer cycles on the falling edge. Active low.
$\overline{\text{VGARAS}}[1-0]$	O	52, 51	Video Memory Row Address Strobe for the VRAM that is used by the internal VGA. All DRAM cycles and transfer cycles are initiated by the falling edge. Active low.

Memory Interface (continued)

Name	Type	Pin Number(s)	Description
$\overline{\text{DRAS}}$	O	66	DRAM Row Address Strobe. All DRAM cycles are initiated by the falling edge. Active low.
$\overline{\text{CAS}[7-0]}$	O	99, 98, 97, 96, 94, 92, 84, 82	Local Memory Column Address Strobe. Latch the states of DSF and column address. Active low.
$\overline{\text{VGACAS}[3-0]}$	O	95, 93, 85, 83	Video Memory Column Address Strobe for the VRAM that is used by the internal VGA. Latch the states of DSF and column address. Active low.

RAMDAC Interface

Name	Type	Pin Number(s)	Description
VP[7-0]	O	36, 37, 38, 39, 40, 41, 42, 43	VGA Pixel outputs. VGA pixel bus from the internal VGA.
PCLK	O	76	VGA Pixel Clock Output. VGA pixel clock output that is synchronized to the VGA pixel outputs. VGA pixels are latched in on the rising edge. Up to 80MHz.
HSYNC	O	50	Horizontal Sync Pulse. Horizontal sync output used for both internal VGA modes and 3GA modes. Polarity is programmable.
VSYNC	O	49	Vertical Sync Pulse. Vertical sync output used for both internal VGA modes and 3GA modes. Polarity is programmable.
$\overline{\text{BLANK}}$	O	48	Blanking Pulse. Blanking output used for both internal VGA modes and 3GA modes. Active low.
LCLKOUT	O	148	Load Clock output. LCLK is synchronized with BLANK- to load pixels into the RAMDAC. Pixels are latched on the rising edge. Up to 50MHz.

Miscellaneous

Name	Type	Pin Number(s)	Description
CLKSEL[1-0]	O	46, 47	Clock Select Bits. Used in VGA and 3GA modes to select the appropriate pixel clock from the clocking source.
$\overline{\text{DEVSTRB}}$	O	140	Local Device Strobe. Used to decode access to devices connected to the LD[63-32] bus, such as the RAMDAC and BIOS. Active low.
TN	O	183	Test Mode Input. Must be connected to VCC for all applications.

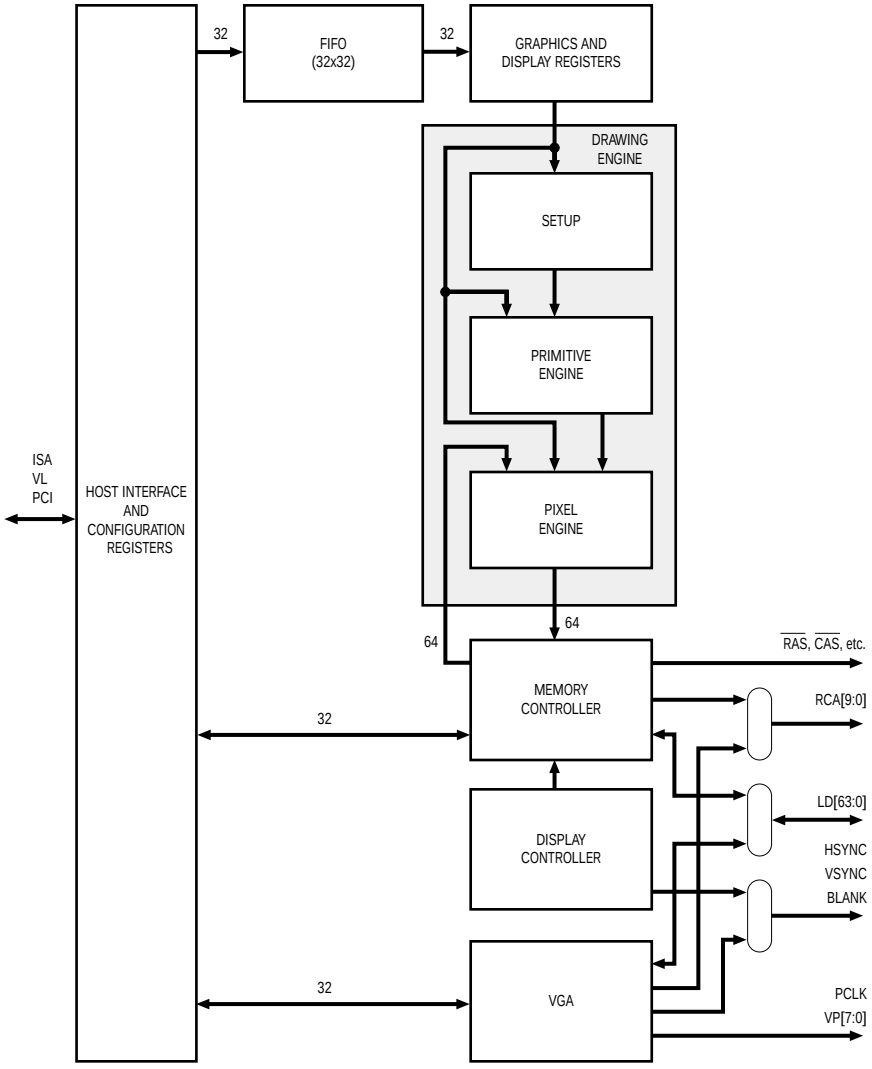
Power and Ground

Name	Type	Pin Number(s)	Description
VIO		10, 25, 35, 226, 234	Power supply input for PCI I/O. The voltage level on these supply inputs can be either +5v or +3.3v. This is selected by a system configuration strapping bit. In ISA and VESA VL-Bus modes these power pins are connected to the same +5v supply as the VCC pins.
VCC		31, 45, 60, 61, 88, 91, 120, 121, 149, 151, 180, 181, 208, 209	Power Supply. The voltage level on these supply inputs must be +5v.
GND		1, 16, 17, 44, 59, 62, 73, 74, 90, 104, 105, 119, 122, 135, 136, 163, 164, 179, 182, 194, 195, 210, 224, 225, 240	Ground.

Functional Description

The 3GA offers a 3D graphics accelerator with VGA compatibility.

3GA Chip Block Diagram



Functional Blocks

The following functional blocks are integrated into the 3GA graphics accelerator.

- **Host Interface and Configuration Registers**

  The host interface provides a 32-bit interface on the PCI bus and VESA VL-Bus. It also provides a 16-bit interface to the ISA bus. The ISA interface is Plug and Play compatible.

- **FIFO**

  The FIFO is a write buffer for drawing engine commands that decouples the CPU-host interface from the 3GA drawing engine. It contains 32 longword (32 bits) entries. On the input side, the FIFO captures host writes to the drawing engine registers and allows the host to proceed immediately without waiting. In conjunction with the drawing engine, the FIFO passes the data on to the appropriate registers. The FIFO manages all pipeline issues with the drawing engine and will not overwrite a register that is in use. When using the FIFO, programmers need only to determine if their is enough free locations in the FIFO prior to writing data.

- **Graphics and Display Registers**

  These registers control most of the 3GA Enhanced Mode operations. They consist of display control, frame buffer base addresses and pitches, coordinates, primitive and interpolation registers.

- **Drawing Engine**

  Setup: Computes the initial decision variables and dimensions for each primitive. It runs concurrent with the primitive engine. Example: If the primitive engine is working on primitive N, setup can be calculating primitive N+1.

  Primitive Engine: The primitive engine tracks X, Y, Z, R, G, B values for each graphics primitive.

  Pixel Engine: The pixel engine services requests from the primitive engine, fetching and writing the data necessary for each set of pixels provided by the primitive engine.

- **Display Controller**

  The display controller provides the memory requests for REFRESH, READ-TRANSFER and SPLIT-READ-TRANSFER operations in 3GA Enhanced Mode. It also generates the syncs and blanks needed by the external VIDEO RAMDAC. Note that the display controller is distinct from the VGA CRT controller.

- **Memory Controller**

  The memory controller services requests from the display controller, host interface and pixel engine. It generates all of the VRAM/DRAM control signals as well as the local device cycles needed to access the BIOS ROM, DAC and clock generator.

- **VGA**

  The VGA is 100% VGA compatible. It supports the following extended SuperVGA modes: 800 x 600 x 16 and 256 colors, and 1024 x 768 x 16 and 256 colors. The VGA is VESA compatible and VESA drivers are available. The PCI bus and VESA VL-Bus provide a 32 bit host interface to the VGA.

Reference Design

The following reference designs are example graphics systems designed around the 3GA graphic accelerator. Three examples are given: one interfacing to the PCI bus, one to the VL-Bus, and one to the ISA bus. These designs use two megabytes of VRAM and support the following resolutions and pixel depths at high refresh:

Resolution	Bits per pixel
640 x 480	8, 16, 24, or 32
800 x 600	8, 16, 24, or 32
1024 x 768	8 or 16
1152 x 870	8 or 16
1280 x 1024	8
1600 x 1200	8

The reference designs use the IBM RGB525 DAC with a 64 bit wide pixel data path. The DAC has an on-chip clock generator for the pixel clock.

Interfacing to the PCI and VL busses require no glue logic, and the 3GA connects directly to the bus. The ISA design requires two additional 74F245 data buffers to connect to the ISA bus. The display memory is 64 bits wide and is made up of four 256Kx16 VRAM's with the $\overline{SOE}$ inputs tied to ground. Series dampening resistors are recommended on all memory control signals. The local device interface uses a 74F138 for decoding and a 74F245 for a data buffer. The local device interface is used to read and write the DAC and to read the BIOS ROM. The SYSCLK signal is provided by a 50MHz TTL oscillator. The pixel clock is generated by the DAC's on-chip clock generator. Video timing for the VGA is provided by the SCLK output from the DAC. The 3GA outputs the VGA pixel clock on its PCLKOUT pin. For 3GA enhanced modes, the 3GA outputs the DAC load clock on its LCLKOUT pin. The rising edge of this clock latches sixty-four bits of pixel data in the DAC. The 3GA automatically generates the VRAM shift clocks, and the BLANK and SYNC signals.

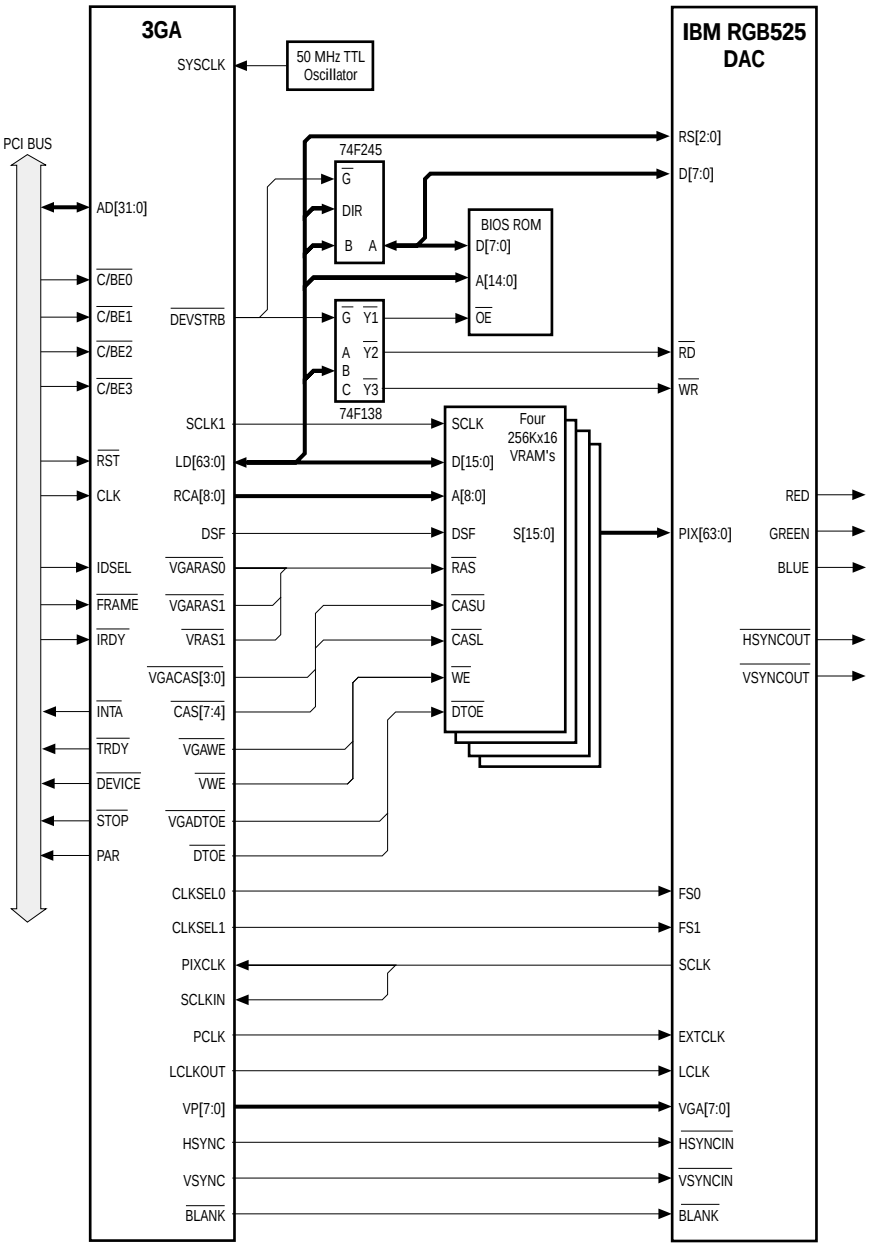
Bill of Materials

The following is a bill of materials for a reference graphics adapter using the 3GA graphic accelerator.

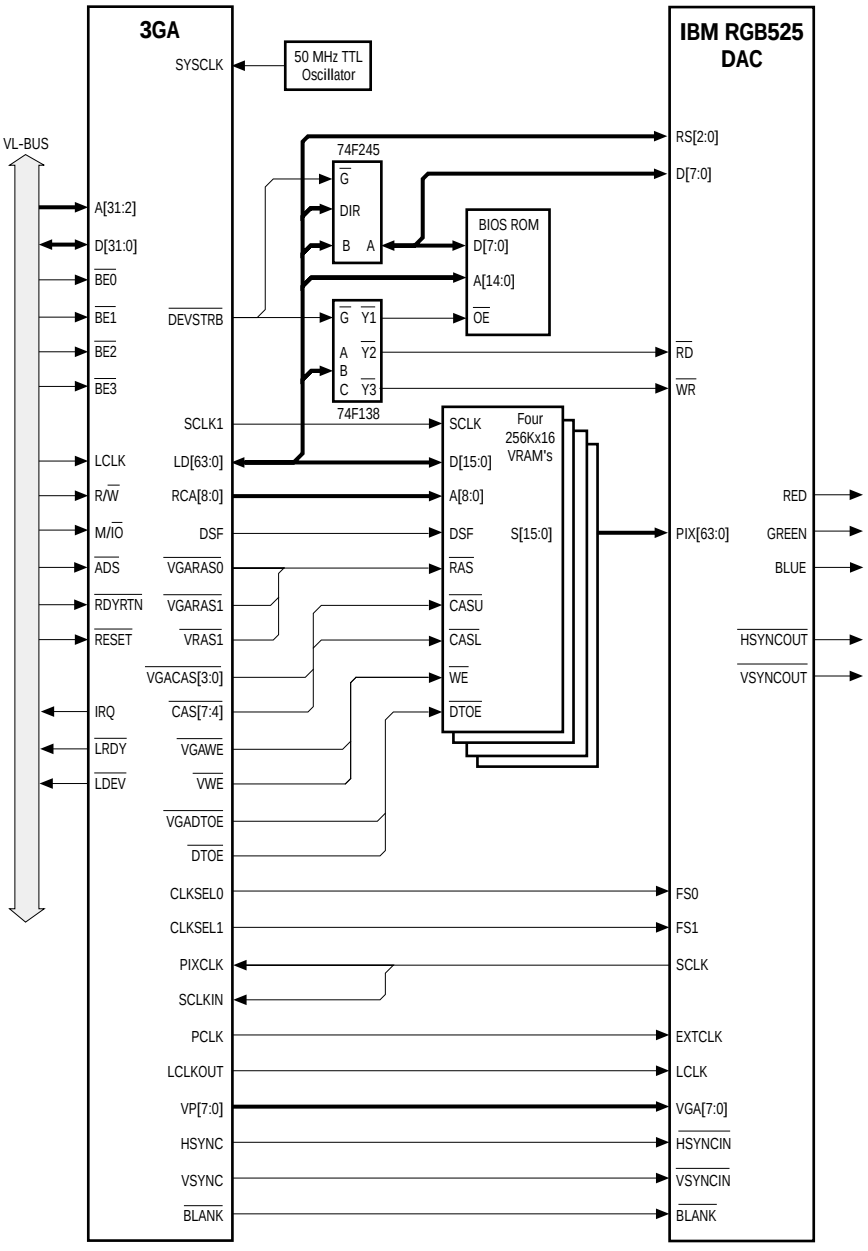
Item	Quantity	Description
1	1	3GA 3D graphics accelerator
2	1	IBM RGB525 DAC
3	4	256Kx16 70ns VRAM's
4	1	BIOS ROM—32K x 8 bits 150ns EPROM
5	1 [1]	74F245
6	1	74F138
7	1	50MHz TTL oscillator
8	1	four layer printed circuit board
9	32	power-up configuration resistors
10	28	series dampening resistors
11	60	decoupling capacitors
12	—	miscellaneous DAC components: ferrite beads, diodes, etc.
13	1	15 pin D-Sub connector

[1]ISA interface requires three 74F245 buffers.

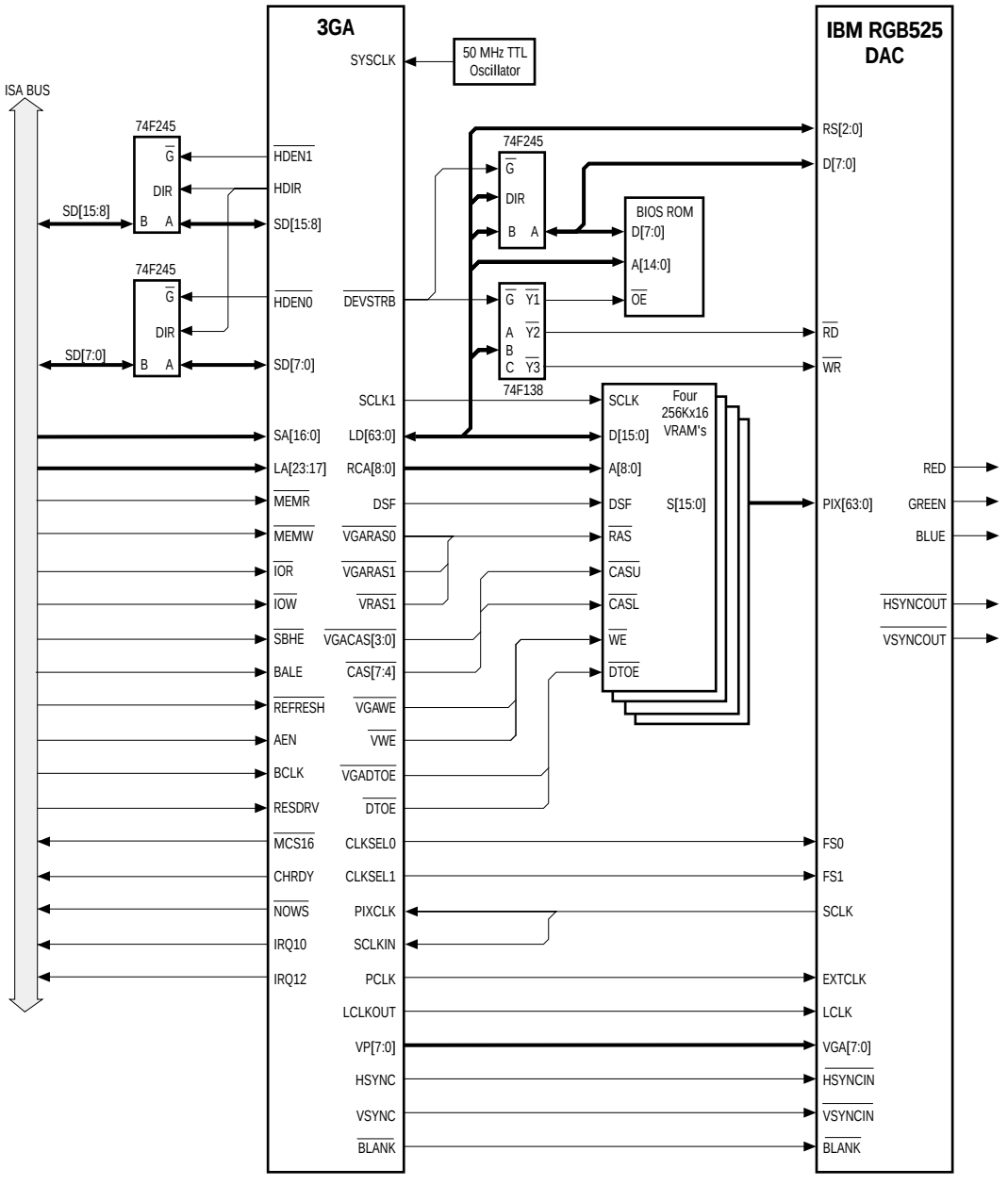
PCI System Block Diagram



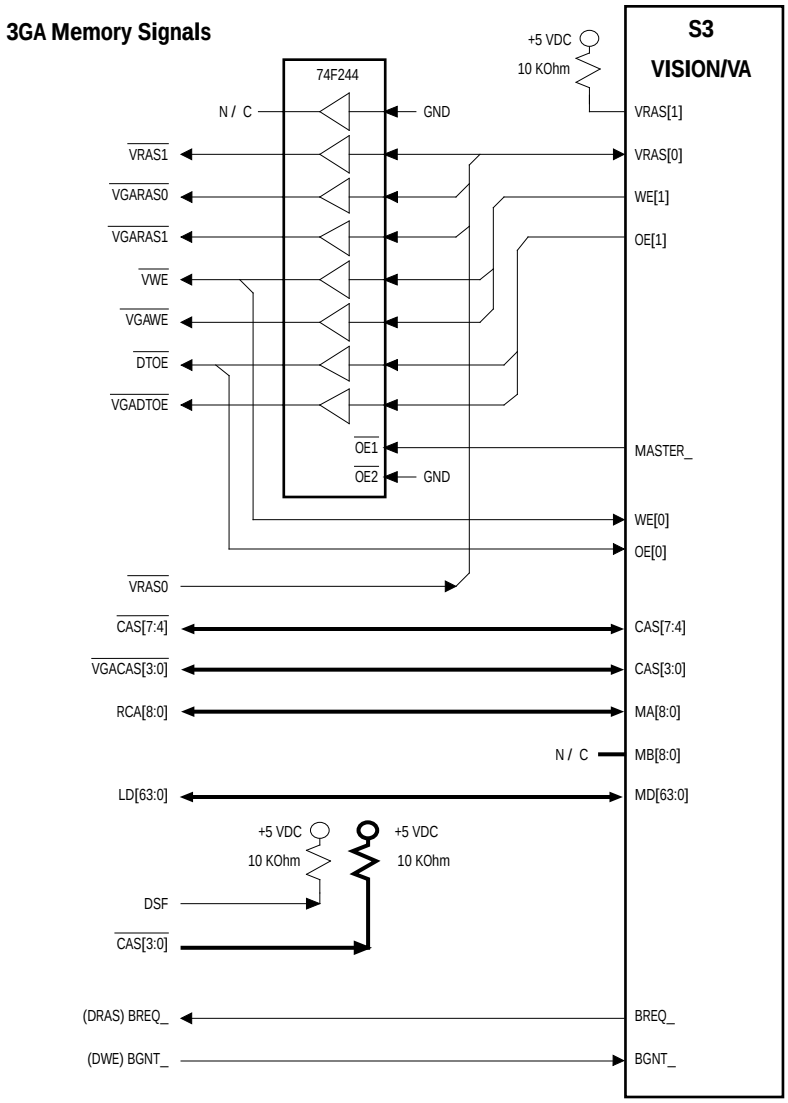
VL-Bus System Block Diagram



ISA Interface System Block Diagram



Shared Frame Buffer Block Diagram:



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