High-Bandwidth Memory (HBM)

REINVENTING MEMORY TECHNOLOGY

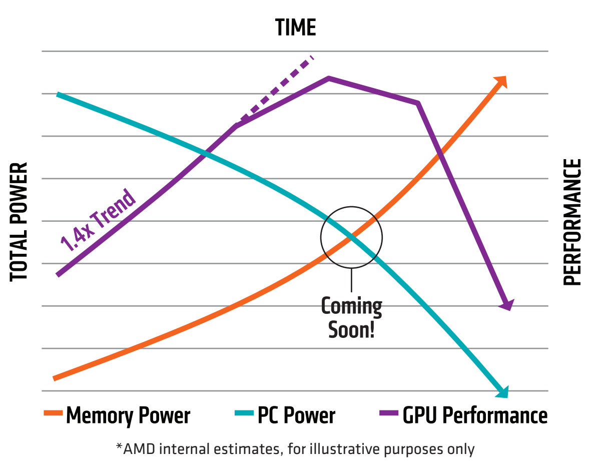
AMD

HBM blasts through existing performance limitations

INDUSTRY PROBLEM #1

GDDR5 can't keep up with GPU performance growth

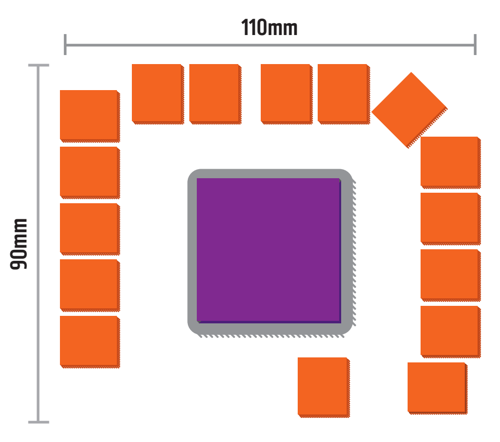
GDDR5's rising power consumption may soon be great enough to actively stall the growth of graphics performance.



INDUSTRY PROBLEM #2

GDDR5 limits form factors

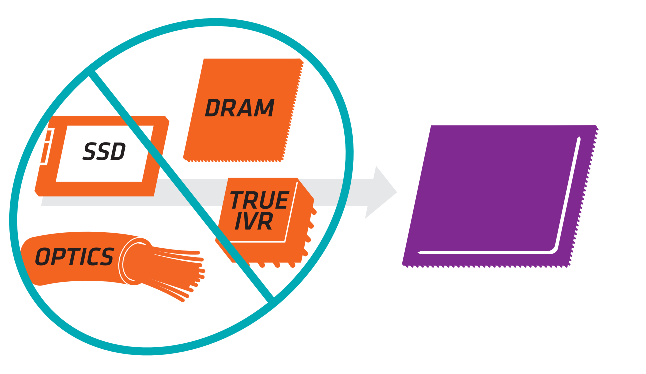
A large number of GDDR5 chips are required to reach high bandwidth. Larger voltage circuitry is also required. This determines the size of a high-performance product.



INDUSTRY PROBLEM #3

On-chip integration not ideal for everything

Technologies like NAND, DRAM and Optics would benefit from on-chip integration, but aren't technologically compatible.



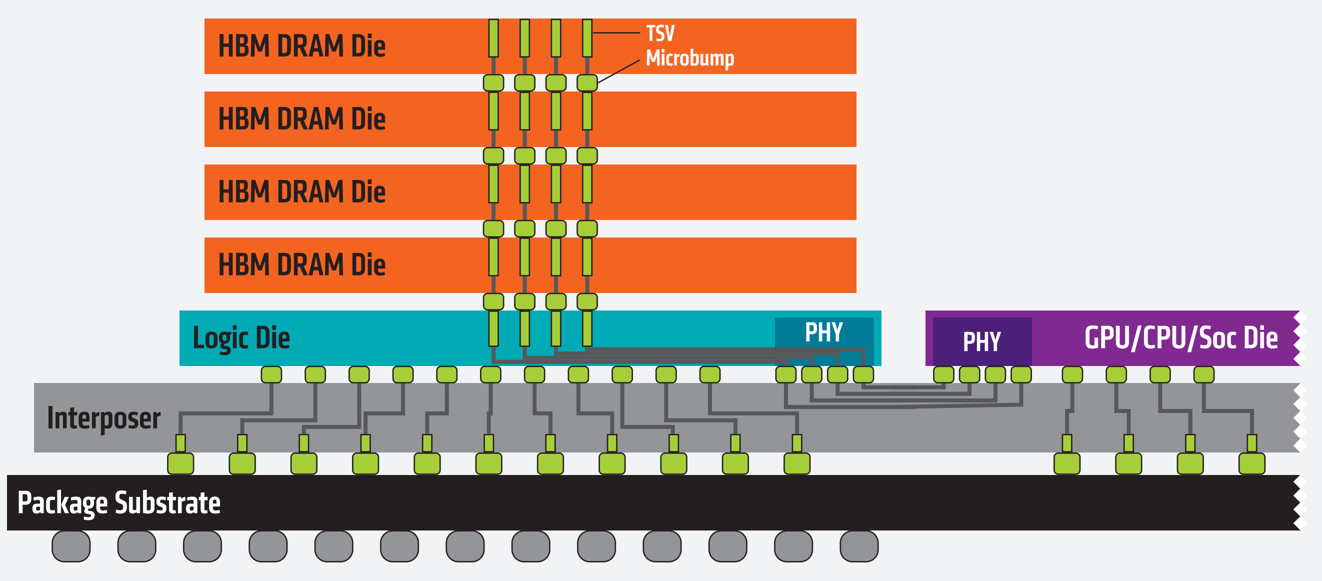
MOORE'S INSIGHT

> *"Over the history of computing hardware, the number of transistors in a dense integrated circuit has doubled approximately every two years.*
>
> *(Thus) it may prove to be more economical to build large systems out of larger functions, which are separately packaged and interconnected… to design and construct a considerable variety of equipment both rapidly and economically."*

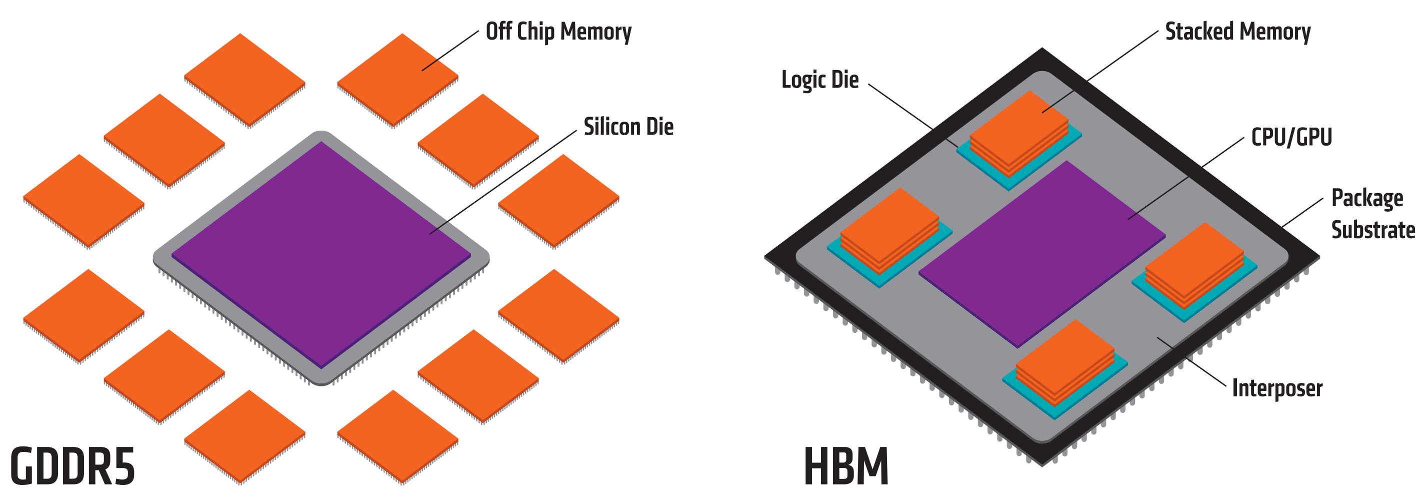
Source: "Cramming more components onto integrated circuits," Gordon E. Moore, Fairchild Semiconductor, 1965

Revolutionary HBM breaks the processing bottleneck

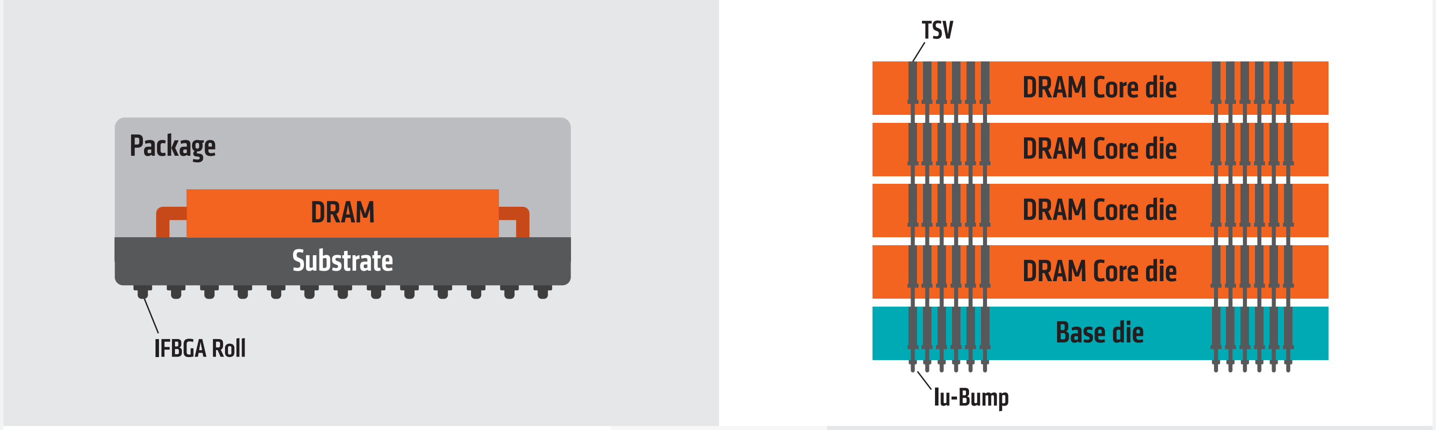
HBM is a new type of memory chip with low power consumption and ultra-wide communication lanes. It uses vertically stacked memory chips interconnected by microscopic wires called "through-silicon vias," or TSVs.



HBM vs GDDR5: *HBM shortens your information commute*

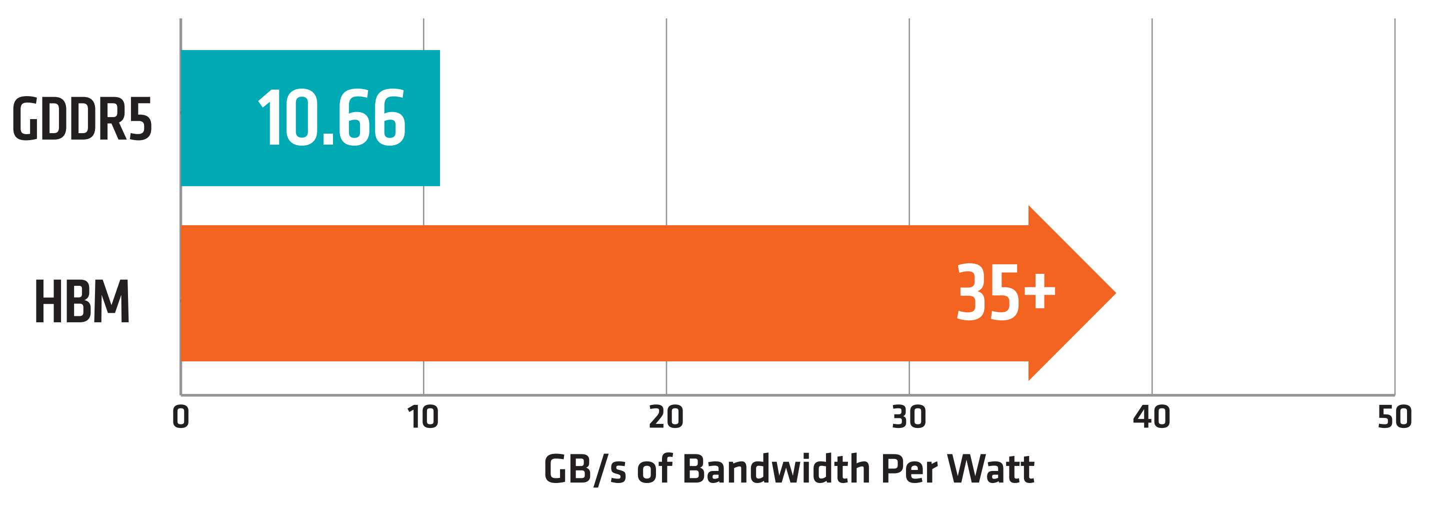


HBM vs GDDR5: *Compare side by side*

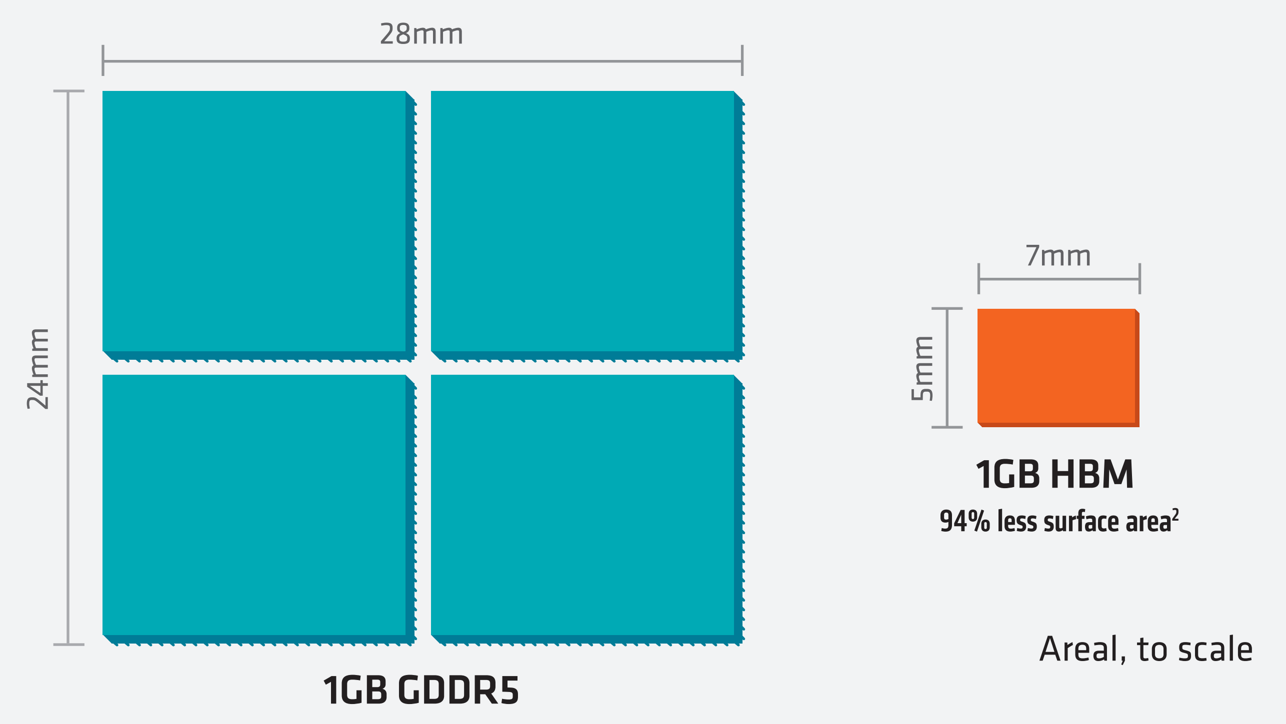


GDDR5	Per Package	HBM
32-bit	Bus Width	1024-bit
Up to 1750MHz (7GBps)	Clock Speed	Up to 500MHz (1GBps)
Up to 28GB/s per chip	Bandwidth	>100GB/s per stack
1.5V	Voltage	1.3V

HBM vs GDDR5: *Better bandwidth per watt*[1]



HBM vs GDDR5: *Massive space savings*



HBM: AMD and JEDEC establish a new industry standard

Design and implementation	Industry standards	ICs/PHY
AMD	**JEDEC**	**SK hynix**

AMD's history of pioneering innovations and open technologies sets industry standards and enables the entire industry to push the boundaries of what is possible.

- Mantle
- GDDR
- Wake-on-LAN/Magic Packet
- DisplayPort™ Adaptive-Sync
- x86-64
- Integrated Memory Controllers
- On-die GPUs
- Consumer Multicore CPUs

1. Testing conducted by AMD engineering on the AMD Radeon™ R9 290X GPU vs. an HBM-based device. Data obtained through isolated direct measurement of GDDR5 and HBM power delivery rails at full memory utilization. Power efficiency calculated as GB/s of bandwidth delivered per watt of power consumed. AMD Radeon™ R9 290X (10.66 GB/s bandwidth per watt) and HBM-based device (35+ GB/s bandwidth per watt), AMD FX-8350, Gigabyte GA-990FX-UD5, 8GB DDR3-1866, Windows 8.1 x64 Professional, AMD Catalyst™ 15.20 Beta. HBM-1

2. Measurements conducted by AMD Engineering on 1GB GDDR5 (4x256MB ICs) @ 672mm^2 vs. 1zGB HBM (1x4-Hi) @ 35mm^2. HBM-2