# CASCADED GRAPHICS CHIPS DRAW 3.3 MILLION PIXELS/S

## AMD'S CONTROLLER INTEGRATES TEXT, GRAPHICS; 64-CHIP CASCADE HANDLES 256 BIT-MAPPED MEMORY PLANES

Aimed at high-performance graphics applications, a new controller chip from Advanced Micro Devices Inc. handles up to 256 bit-mapped memory planes when cascaded with other units, and it draws vectors at the rate of 3.3 million pixels/ns.

Using 4-K-by-4-K memory planes, the Am95C60 also features the integration of text and graphics in the same bit map with a bit-block-transfer algorithm.

AMD expects the chip to be used in engineering work stations, computer-aided design and manufacturing equipment, graphic arts, and desktop publishing. It is one more example of the move by semiconductor companies to incorporate more graphics control at the chip level to accommodate ever more sophisticated graphics applications.

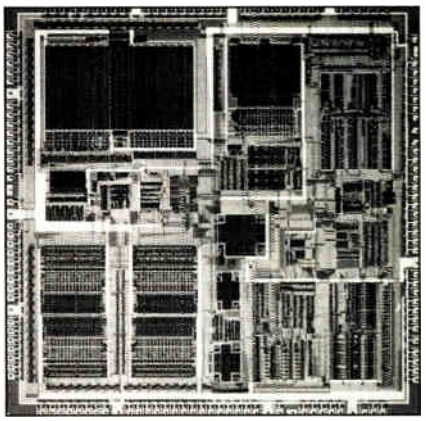
**256 PLANES.** AMD calls the device a quad pixel dataflow manager, because each chip manages and updates four bit-mapped memory planes from a single control channel. As many as 64 chips can be cascaded to create 256 memory planes without performance degradation, says the company.

The 95C60 supports screen displays up to 2-K by 2-K pixels and can update a 1-K-by-1-K-pixel screen—the most common high-resolution screen on the market—in 0.2 s at its 20-MHz clock speed.

AMD speeded bit-mapping in the 95C60 by using both graphic and raster primitives to update each bit map. Graphics are drawn with line and arc vectors at a speed of 3.3 million pixels/s. Polygon-fill operations are accomplished at a rate of 50 ns/pixel.

The 95C60 efficiently mixes text and graphics. A bit-block-transfer primitive replaces the usual alphanumeric control for characters, which means that text is treated as a special form of graphics. The command, called BITBLT, can transfer blocks of data at up to 20 Mb/s. A single 13-bit character-address instruction can access up to 8,192 characters—enough to support any character set, including oriental Kanji characters. Fonts are stored in the bit map.

The chip's performance results in part from extensive parallelism in its architecture. Fetch, execute, and display cycles overlap. All chip cycles are decoupled from system bus cycles. The chip can fetch its own instructions via the display memory bus, off-loading this task from the central processor. Arbitration between refresh cycles, update cycles, and external-memory-refresh cycles is performed on-chip.



**CONCURRENCY.** AMD's graphics controller chip overlaps cycles for higher performance.

The instruction set supports windowing in both hardware and, via BITBLT, software. Scroll, pan, and zoom may be performed on the screen itself and on any window on the screen. Anti-aliasing is used to eliminate jagged "steps" in diagonal lines.

A 16-MHz version of the chip costs $250 in lots of 100. It has been offered in sample lots since January and will be available in quantity next month. The 20-MHz version of the chip will also be available next month for $287.57 each in lots of 100.

[Circle 360]

## CHIP CUTS COST AND SPACE NEEDS

Adaptec's AIC-610 peripheral controller chip replaces 10 logic components formerly implemented in discrete form on most controllers, including a programmable storage buffer, a dual-port buffer controller, and buffer addressing logic.

By integrating more components on-chip, Adaptec achieved a 60% to 70% space reduction over controllers now on the market, says the company. Consequently, logic-hardware costs will be reduced by 40% and power requirements by 30%.

Offering a maximum 15-MHz data-transfer speed and a maximum bus transfer rate of 1.5 megabytes/s, the chip is compatible with any standard interface used by Winchester-disk, floppy-disk, and tape drives.