Permedia4®

Reference Guide - Volume III

DRAFT ONLY

PROPRIETARY AND CONFIDENTIAL INFORMATION

3D*labs*®

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Issue 5

Proprietary Notice

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Change History

Document	Issue	Date	Change
160.2.3	1	19 April 1999	Creation
160.2.3	2	16 June 1999	FBSourceData, FBData added; minor corrections
160.2.3	3	15 September 1999	New Package information, corrections, footer typography
160.2.3	4	20 September 1999	Clarification to Reset and some pin descriptions
160.2.3	5	30 Jan 2000	PEREN0017 Horizontal Resolution, 32bpp constant color span

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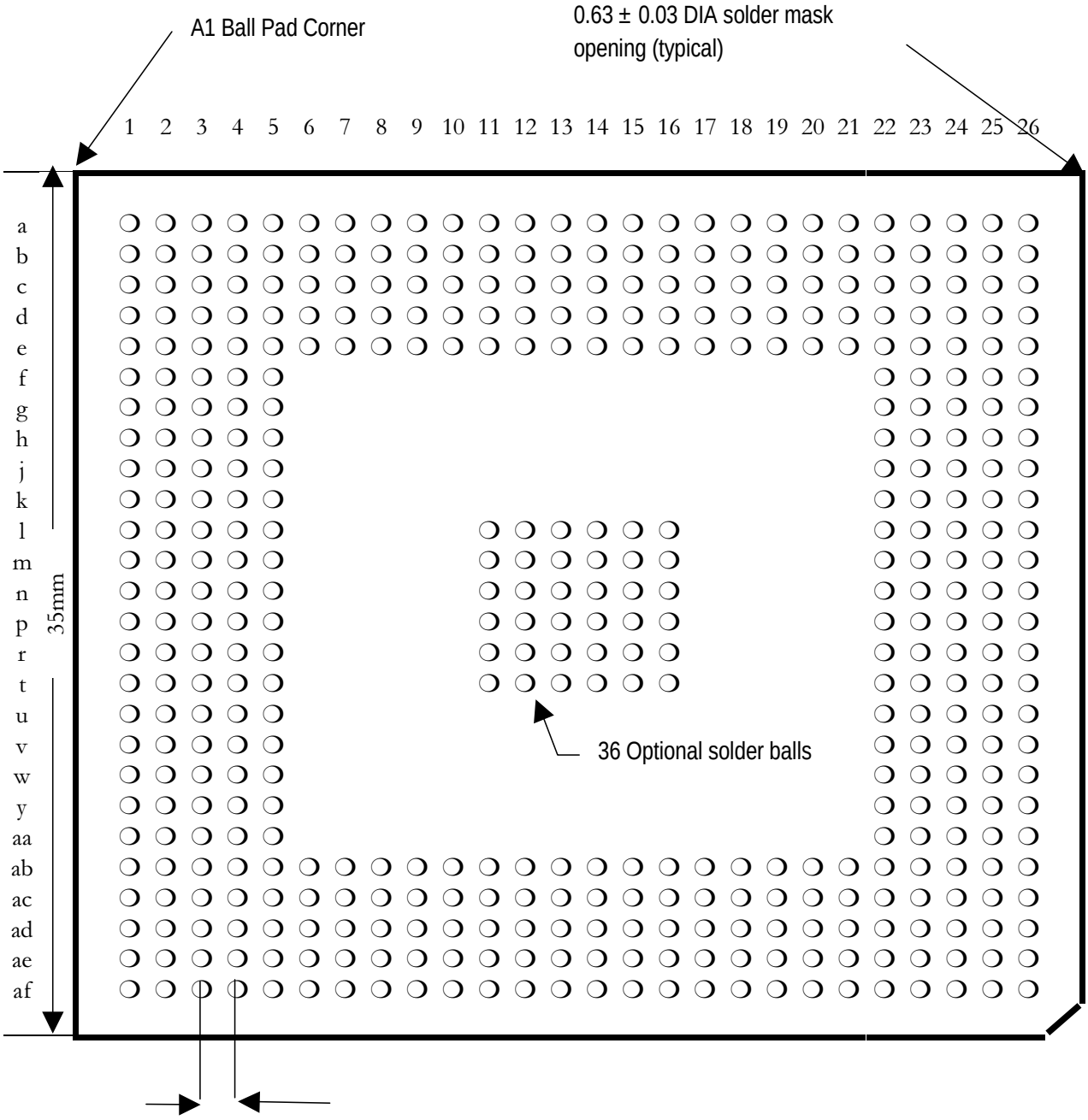
Package Diagrams



SOLDER MASK LAYER 4 - BOTTOM

Unit shown from Die Side

Figure 7-1 Package Diagram (Bottom View)

The Permedia4 package is a standard PBGA 456-ball open tool package. Package height is 2.33mm, body size is 35x35mm. Other specifications are as listed in table 7-1.

Table 7-1 Mechanical Diagrams

Dimension		mm
a	Ball Pitch	1.27
b	Lead Width	0.63 ±0.03
c	Foot Length	
d	Height	2.33
E	Width (toe to toe)	
F	Body Width	35

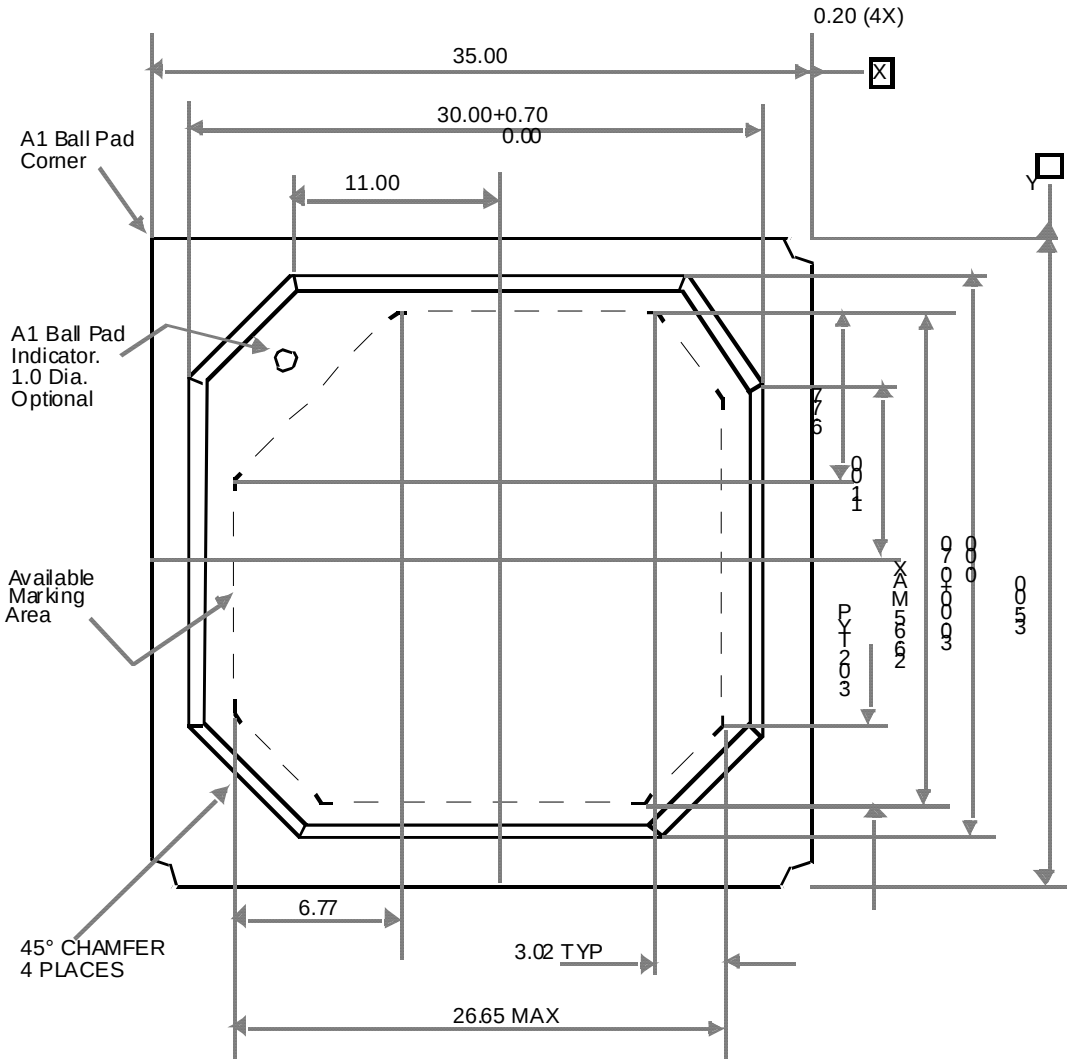


Figure 7-2 PQFP Package Dimensions (Top)

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Pin Assignment

8.1 Pinlist by Number

The table below provides a brief description of each pin. It is organized alphabetically by pin number.

The pin type definitions used are:

I/O: Input Signal

GND: Ground

VSS_3.3: Power at 3.3V

VSS_2.5: Power at 2.5 Volts

VDDQ: AGP I/O Interface voltage from motherboard[1]

8.1.1 Unused AGP pins

Where AGP pins are unused, the following terminations are recommended:

AGPSBA(7:0)	No connection - output only
AGPPipeN	No connection - output only
AGPADSTB(1:0)	Tie high (input only)
AGPADSTBN(1:0)	Tie low (input only)
AGPADSTB	No connection - output only
AGPADSTBN	No connection - output only
AGPADSt(2:0)	Tie high - input only
AGPVoltSel	Tie low (input only, used in test only)
ZSET	As per AGP termination
AGPVREF	As per AGP termination
AGPRbfN	No connection (output only)

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
GND_C		gnd	
VCC_3.3		vcc_3.3	

[1] Depending on TypeDet, this will be either 1.5 or 3.3 VDC. If TypeDet is set for 3.3V signalling, then the configuration resistor AGP4Xcapable must not be set.

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VCC_2.5		vdd	
VDDQ		vddq	
GND_IO		vsso	
VCC_2.5	A01		
VCC_2.5	A02		
I/O	A03	MDat_124	Memory data line 124
I/O	A04	MDat_98	Memory data line 98
I/O	A05	MDat_113	Memory data line 113
I/O	A06	MDat_112	Memory data line 112
I/O	A07	MDat_119	Memory data line 119
I/O	A08	MDat_111	Memory data line 111
I/O	A09	MDat_104	Memory data line 104
I/O	A10	MemClkRet_3	Memory Clock Return 3
I/O	A11	MDat_90	Memory data line 90
I/O	A12	MDat_91	Memory data line 91
I/O	A13	MDat_70	Memory data line 70
I/O	A14	MDat_82	Memory data line 82
I/O	A15	MDat_83	Memory data line 83
I/O	A16	MDat_77	Memory data line 77
I/O	A17	MDat_76	Memory data line 76
I/O	A18	MDat_75	Memory data line 75
I/O	A19	MemClkRet_2	Memory Clock Return 2
I/O	A20	MDat_60	Memory data line 60
I/O	A21	MDat_59	Memory data line 59
I/O	A22	MDat_35	Memory data line 35
I/O	A23	MDat_36	Memory data line 36
I/O	A24	MDat_38	Memory data line 38
VCC_2.5	A25		
VCC_2.5	A26		
I/O	AA01	SClkIn	
I/O	AA02	VSAdata_2	VideoStream A data line 2
I/O	AA03	VSAData_1	VideoStream A data line 1
I/O	AA04	VSAData_0	VideoStream A data line 0
GND	AA05		

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
GND	AA22		
I/O	AA23	MAddr_5	Memory address line 5
I/O	AA24	MAddr_6	Memory address line 6
I/O	AA25	MAddr_7	Memory address line 7
I/O	AA26	MAddr_8	Memory address line 8
I/O	AB01	PCIFIFOInDis	Disable PCI Input FIFO
I/O	AB02	PCIFIFOOutDis	Disable PCI Output FIFO
I/O	AB03	PCIRSTN	PCI reset
I/O	AB04	MclkIn	Memory Clock In
GND	AB05		
GND	AB06		
VDDQ	AB07		
VDDQ	AB08		
GND	AB09		
GND	AB10		
VDDQ	AB11		
VDDQ	AB12		
GND	AB13		
GND	AB14		
VDDQ	AB15		
VDDQ	AB16		
GND	AB17		
GND	AB18		
VDDQ	AB19		
VDDQ	AB20		
GND	AB21		
GND	AB22		
I/O	AB23	MemClkOut_0	Memory Clock Out 0
I/O	AB24	MAddr_2	Memory address line 2
I/O	AB25	MAddr_3	Memory address line 3
I/O	AB26	MAddr_4	Memory address line 4
I/O	AC01	PCIClkSel	33/66 MHz PCI Select
I/O	AC02	PCICLK	PCI clock
I/O	AC03	KClkIn	Core Clock In

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VCC_2.5	AC04		
I/O	AC05	AGPSt_2	AGP status 2
I/O	AC06	AGPSBA_0	AGP Sideband Address 0
I/O	AC07	AGPSBA_3	AGP Sideband Address 3
I/O	AC08	AGPSBA_4	AGP Sideband Address 4
I/O	AC09	AGPVCC_3.3_2	
I/O	AC10	PCIAD_29	PCI address/data line 29
I/O	AC11	PCIAD_26	PCI address/data line 26
I/O	AC12	PCIAD_23	PCI address/data line 23
I/O	AC13	PCIAD_21	PCI address/data line 21
I/O	AC14	PCIAD_20	PCI address/data line 20
I/O	AC15	PCICBEN_2	PCI Byte Enable 2
I/O	AC16	PCIFrameN	PCI Frame Signal
I/O	AC17	**SPARE**	
I/O	AC18	PCIAD_15	PCI address/data line 15
I/O	AC19	PCIAD_12	PCI address/data line 12
I/O	AC20	PCIAD_8	PCI address/data line 8
I/O	AC21	**SPARE**	
I/O	AC22	PCIAD_4	PCI address/data line 4
VCC_2.5	AC23		
I/O	AC24	MemClkOut_1	Memory clock out 1
I/O	AC25	MAddr_0	Memory address line 0
I/O	AC26	MAddr_1	Memory address line 1
I/O	AD01	PCIIntAN	PCI interrupt
I/O	AD02	AGPVoltSel	
VCC_2.5	AD03		
I/O	AD04	AGPSt_0	AGP status 0
I/O	AD05	AGPRbfN	AGP Read Data Buffer full
I/O	AD06	**SPARE**	
I/O	AD07	AGPSBSTB	AGP Sideband Address 2X strobe
I/O	AD08	AGPSBA_5	AGP Sideband Address 5
I/O	AD09	PCIAD_31	PCI address/data line 31
I/O	AD10	**SPARE**	

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AD11	PCIAD_25	PCI address/data line 25
I/O	AD12	PCIAD_24	PCI address/data line 24
I/O	AD13	PCIAD_22	PCI address/data line 22
I/O	AD14	AGPVCC_3.3_3	
I/O	AD15	PCIAD_16	PCI address/data line 16
I/O	AD16	PCIDevSelN	PCI device select
I/O	AD17	PCIStopN	PCI stop
I/O	AD18	AGPVCC_3.3_4	
I/O	AD19	PCIAD_11	PCI address/data line 11
I/O	AD20	PCICBEN_0	PCI byte enable 0
I/O	AD21	PCIAD_7	PCI address/data line 7
I/O	AD22	AGPVCC_3.3_5	
I/O	AD23	AGPvREF	not connected
VCC_2.5	AD24		
I/O	AD25	MemClkOut_2	Memory Clock Out 2
I/O	AD26	MemClkOut_3	Memory Clock Out 3
VCC_2.5	AE01		
VCC_2.5	AE02		
I/O	AE03	PCIReqN	PCI request
I/O	AE04	AGPSt_1	AGP status 1
I/O	AE05	AGPPipeN	AGP Pipelined Address
I/O	AE06	AGPSBA_1	AGP Sideband Address 1
I/O	AE07	AGPSBSTBN	
I/O	AE08	AGPSBA_6	AGP Sideband Address 6
I/O	AE09	PCIAD_30	PCI address/data line 30
I/O	AE10	PCIAD_28	PCI address/data line 28
I/O	AE11	AGPADSTBN_1	
I/O	AE12	PCICBEN_3	PCI byte enable 3
I/O	AE13	PCIAD_19	PCI address/data line 19
I/O	AE14	PCIAD_17	PCI address/data line 17
I/O	AE15	PCIIRdyN	PCI ready
I/O	AE16	PCITRdyN	PCI T ready
I/O	AE17	PCIPar	PCI parity
I/O	AE18	PCIAD_14	PCI address/data line 14

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AE19	PCIAD_10	PCI address/data line 10
I/O	AE20	AGPADSTB_0	AGP AD 2X strobe
I/O	AE21	PCIAD_6	PCI address/data line 6
I/O	AE22	PCIAD_3	PCI address/data line 3
I/O	AE23	PCIAD_1	PCI address/data line 1
I/O	AE24	ZSET	
VCC_2.5	AE25		
VCC_2.5	AE26		
VCC_2.5	AF01		
VCC_2.5	AF02		
I/O	AF03	PCIGntN	PCI grant signal
I/O	AF04	AGPVCC_3.3_1	
I/O	AF05	**SPARE**	
I/O	AF06	AGPSBA_2	AGP Sideband Address 2
I/O	AF07	**SPARE**	
I/O	AF08	**SPARE**	
I/O	AF09	AGPSBA_7	AGP Sideband Address 7
I/O	AF10	PCIAD_27	PCI address/data line 27
I/O	AF11	AGPADSTB_1	
I/O	AF12	**SPARE**	
I/O	AF13	PCIIdSel	PCI ID select
I/O	AF14	PCIAD_18	PCI address/data line 18
I/O	AF15	**SPARE**	
I/O	AF16	**SPARE**	
I/O	AF17	PCICBEN_1	PCI byte enable 1
I/O	AF18	PCIAD_13	PCI address/data line 13
I/O	AF19	PCIAD_9	PCI address/data line 9
I/O	AF20	AGPADSTBN_0	
I/O	AF21	PCIAD_5	PCI address/data line 5
I/O	AF22	PCIAD_2	PCI address/data line 2
I/O	AF23	PCIAD_0	PCI address/data line 0
I/O	AF24	**SPARE**	
VCC_2.5	AF25		
VCC_2.5	AF26		

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VCC_2.5	B01		
VCC_2.5	B02		
I/O	B03	MDat_99	Memory data line 99
I/O	B04	MDat_97	Memory data line 97
I/O	B05	MDat_115	Memory data line 115
I/O	B06	MDat_116	Memory data line 116
I/O	B07	MDat_108	Memory data line 108
I/O	B08	MDat_107	Memory data line 107
I/O	B09	MByte_15	Memory byte select 15
I/O	B10	MDat_93	Memory data line 93
I/O	B11	MDat_89	Memory data line 89
I/O	B12	MDat_66	Memory data line 66
I/O	B13	MDat_69	Memory data line 69
I/O	B14	MDat_81	Memory data line 81
I/O	B15	MDat_85	Memory data line 85
I/O	B16	MDat_78	Memory data line 78
I/O	B17	MDat_74	Memory data line 74
I/O	B18	MByte_11	Memory byte select 11
I/O	B19	MByte_9	Memory byte select 9
I/O	B20	MDat_61	Memory data line 61
I/O	B21	MDat_58	Memory data line 58
I/O	B22	MDat_34	Memory data line 34
I/O	B23	MDat_37	Memory data line 37
I/O	B24	MDat_39	Memory data line 39
VCC_2.5	B25		
VCC_2.5	B26		
I/O	C01	MDat_123	Memory data line 123
I/O	C02	MDat_125	Memory data line 125
VCC_2.5	C03		
I/O	C04	MDat_96	Memory data line 96
I/O	C05	MDat_114	Memory data line 114
I/O	C06	MDat_117	Memory data line 117
I/O	C07	MDat_109	Memory data line 109
I/O	C08	MDat_106	Memory data line 106

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	C09	MByte_13	Memory byte select 13
I/O	C10	MDat_94	Memory data line 94
I/O	C11	MDat_88	Memory data line 88
I/O	C12	MDat_65	Memory data line 65
I/O	C13	MDat_67	Memory data line 67
I/O	C14	MDat_80	Memory data line 80
I/O	C15	MDat_86	Memory data line 86
I/O	C16	MDat_79	Memory data line 79
I/O	C17	MDat_73	Memory data line 73
I/O	C18	MByte_8	Memory byte select 8
I/O	C19	MByte_10	Memory byte select 10
I/O	C20	MDat_62	Memory data line 62
I/O	C21	MDat_57	Memory data line 57
I/O	C22	MDat_33	Memory data line 33
I/O	C23	MDat_48	Memory data line 48
VCC_2.5	C24		
I/O	C25	MDat_49	Memory data line 49
I/O	C26	MDat_50	Memory data line 50
I/O	D01	MDat_122	Memory data line 122
I/O	D03	MDat_126	Memory data line 126
VCC_2.5	D04		
I/O	D05	MDat_118	Memory data line 118
I/O	D06	MDat_110	Memory data line 110
I/O	D07	MDat_105	Memory data line 105
I/O	D08	MByte_12	Memory byte select 12
I/O	D09	MByte_14	Memory byte select 14
I/O	D10	MDat_95	Memory data line 95
I/O	D11	MDat_92	Memory data line 92
I/O	D12	MDat_64	Memory data line 64
I/O	D13	MDat_71	Memory data line 71
I/O	D14	MDat_68	Memory data line 68
I/O	D15	MDat_87	Memory data line 87
I/O	D16	MDat_84	Memory data line 84
I/O	D17	MDat_72	Memory data line 72

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	D18	RenderSyncN	Multi-rasterizer i/o sync
I/O	D19	MDat_63	Memory data line 63
I/O	D2	MDat_100	Memory data line 100
I/O	D20	MDat_56	Memory data line 56
I/O	D21	MDat_32	Memory data line 32
I/O	D22	VideoExtCtrl	Video External control
VCC_2.5	D23		
I/O	D24	MDat_51	Memory data line 51
I/O	D25	MDat_52	Memory data line 52
I/O	D26	MDat_53	Memory data line 53
I/O	E01	MDat_121	Memory data line 121
I/O	E02	MDat_101	Memory data line 101
I/O	E03	MDat_102	Memory data line 102
I/O	E04	MDat_127	Memory data line 127
GND	E05		
GND	E06		
VCC_3.3	E07		
VCC_3.3	E08		
GND	E09		
GND	E10		
VCC_3.3	E11		
VCC_3.3	E12		
GND	E13		
GND	E14		
VCC_3.3	E15		
VCC_3.3	E16		
GND	E17		
GND	E18		
VCC_3.3	E19		
VCC_3.3	E20		
GND	E21		
GND	E22		
I/O	E23	MDat_47	Memory data line 47
I/O	E24	MDat_46	Memory data line 46

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	E25	MDat_55	Memory data line 55
I/O	E26	MDat_54	Memory data line 54
I/O	F01	MDat_120	Memory data line 120
I/O	F02	VSBResetN	Video Stream B Reset Out
I/O	F03	MDat_103	Memory data line 103
I/O	F04	VSBData_0	VideoStream B data line 0
GND	F05		
GND	F22		
I/O	F23	MDat_45	Memory data line 45
I/O	F24	MDat_44	Memory data line 44
I/O	F25	MDat_43	Memory data line 43
I/O	F26	MDat_42	Memory data line 42
I/O	G01	VSBData_1	VideoStream B data line 1
I/O	G02	VSBData_2	VideoStream B data line 2
I/O	G03	VSBData_3	VideoStream B data line 3
I/O	G04	VSBData_4	VideoStream B data line 4
VCC_3.3	G05		
VCC_3.3	G22		
I/O	G23	MByte_4	Memory byte select 4
I/O	G24	MByte_7	Memory byte select 7
I/O	G25	MDat_40	Memory data line 40
I/O	G26	MDat_41	Memory data line 41
I/O	H01	VSBData_5	VideoStream B data line 5
I/O	H02	VSBData_6	VideoStream B data line 6
I/O	H03	VSBData_7	VideoStream B data line 7
I/O	H04	VSBClk	VideoStream B clock
VCC_3.3	H05		
VCC_3.3	H22		
I/O	H23	MDat_31	Memory data line 31
I/O	H24	MByte_6	Memory byte select 6
I/O	H25	MByte_5	Memory byte select 5
I/O	H26	MemClkRet_1	Memory Clock Return 1
I/O	J01	VSGPDataStrobeN	VS GP bus data strobe
I/O	J02	VSGPReadWriteN	VS GP bus read/write signal

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	J03	VSBClkOut	Video Streams B Clock Out
I/O	J04	VSCtl_0	VideoStreams Control line 0
GND	J05		
GND	J22		
I/O	J23	MDat_30	Memory data line 30
I/O	J24	MDat_29	Memory data line 29
I/O	J25	MDat_28	Memory data line 28
I/O	J26	MBank_3	Memory bank select 3
I/O	K01	VSCtl_1	VideoStreams Control line 1
I/O	K02	VSGPChipSelectN	VS GP bus chip select
I/O	K03	VSGPDataAckN	VS GP bus data ack
I/O	K04	VSCtl_2	VideoStreams Control line 2
GND	K05		
GND	K22		
I/O	K23	MDat_24	Memory data line 24
I/O	K24	MDat_25	Memory data line 25
I/O	K25	MDat_26	Memory data line 26
I/O	K26	MDat_27	Memory data line 27
I/O	L01	VSCtl_4	VideoStreams Control line 4
I/O	L02	VSCtl_5	VideoStreams Control line 5
I/O	L03	TestSel_0	Test Mode Select 0
I/O	L04	VSCtl_3	VideoStreams Control line 3
VCC_3.3	L05		
GND	L11		
GND	L12		
GND	L13		
GND	L14		
GND	L15		
GND	L16		
VCC_3.3	L22		
I/O	L23	MDat_3	Memory data line 3
I/O	L24	MDat_0	Memory data line 0
I/O	L25	MDat_1	Memory data line 1
I/O	L26	MDat_2	Memory data line 2

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	M01	VSCtl_6	VideoStreams Control line 6
I/O	M02	VSCtl_7	VideoStreams Control line 7
I/O	M03	VidRightEye	
I/O	M04	DacAGnd	
I/O	M05	TestSel_2	Test Mode Select 2
GND	M11		
GND	M12		
GND	M13		
GND	M14		
GND	M15		
GND	M16		
VCC_3.3	M22		
I/O	M23	MDat_7	Memory data line 7
I/O	M24	MDat_6	Memory data line 6
I/O	M25	MDat_5	Memory data line 5
I/O	M26	MDat_4	Memory data line 4
I/O	N01	DacAGnd	
I/O	N02	VidGreen	Analog green signal
I/O	N03	DacVRef	
I/O	N04	VidRed	Analog red signal
I/O	N05	DacAVDD	Analog/video DAC
GND	N11		
GND	N12		
GND	N13		
GND	N14		
GND	N15		
GND	N16		
GND	N22		
I/O	N23	MDat_16	Memory data line 16
I/O	N24	MDat_19	Memory data line 19
I/O	N25	MDat_18	Memory data line 18
I/O	N26	MDat_17	Memory data line 17
I/O	P01	DacAVDD	
I/O	P02	DacComp	Compensation pin

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	P03	DacAVDD	
I/O	P04	VidBlue	Analog blue signal
GND	P05		
GND	P11		
GND	P12		
GND	P13		
GND	P14		
GND	P15		
GND	P16		
GND	P22		
I/O	P23	MDat_20	Memory data line 20
I/O	P24	MDat_23	Memory data line 23
I/O	P25	MDat_22	Memory data line 22
I/O	P26	MDat_21	Memory data line 21
I/O	R01	VidHSync	Horizontal sync
I/O	R02	DacAGnd	
I/O	R03	DacFSAdj	
I/O	R04	DacAGnd	DAC Power/Gnd pin
I/O	R05	TestSel_1	Test Mode Select 1
GND	R11		
GND	R12		
GND	R13		
GND	R14		
GND	R15		
GND	R16		
VCC_3.3	R22		
I/O	R23	MDat_15	Memory data line 15
I/O	R24	MDat_14	Memory data line 14
I/O	R25	MDat_13	Memory data line 13
I/O	R26	MDat_12	Memory data line 12
I/O	T01	VidVsync	Vertical sync
I/O	T02	PLLDISABLE	PLL Disable
I/O	T03	TestMode	TestMode control
I/O	T04	Xtal1	Crystal i/p 1

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VCC_3.3	T05		
GND	T11		
GND	T12		
GND	T13		
GND	T14		
GND	T15		
GND	T16		
VCC_3.3	T22		
I/O	T23	MDat_11	Memory data line 11
I/O	T24	MDat_8	Memory data line 8
I/O	T25	MDat_9	Memory data line 9
I/O	T26	MDat_10	Memory data line 10
I/O	U01	ROMSelectN	ROM Select signal
I/O	U02	VidDDCData	Data line for DDC
I/O	U03	VidDDCClk	Clock line for DDC
I/O	U04	Xtal2	Crystal i/p 2
GND	U05		
GND	U22		
I/O	U23	MBank_2	Memory bank select 2
I/O	U24	MByte_0	Memory byte select 0
I/O	U25	MByte_3	Memory byte select 3
I/O	U26	MByte_1	Memory byte select 1
I/O	V01	SBClk	Serial bus clock
I/O	V02	VSAClk	VideoStream A clock
I/O	V03	VSAResetN	
I/O	V04	ROMWeN	ROM Write Enable
GND	V05		
GND	V22		
I/O	V23	MBank_0	Video bank select 0
I/O	V24	MBank_1	Memory bank select 1
I/O	V25	MByte_2	Memory byte select 2
I/O	V26	MemClkRet_0	Memory Clock Return 0
I/O	W01	PLLPower	PLL Power/Gnd pin
I/O	W02	VSAData_5	VideoStream A data line 5

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	W03	VSAData_7	VideoStream A data line 7
I/O	W04	SBData	serial bus data
VCC_3.3	W05		
VCC_3.3	W22		
I/O	W23	MDSF	Memory DSF line
I/O	W24	MRAS	Memory RAS line
I/O	W25	MCAS	Memory CAS line
I/O	W26	MClkE	Memory clock enable
I/O	Y01	VSAData_3	VideoStream A data line 3
I/O	Y02	VSAData_6	VideoStream A data line 6
I/O	Y03	VSAData_4	VideoStream A data line 4
I/O	Y04	PLLGND	PLL Power/Gnd pin
VCC_3.3	Y05		
VCC_3.3	Y22		
I/O	Y23	MAddr_9	Memory address line 9
I/O	Y24	MAddr_10	Memory address line 10
I/O	Y25	MAddr_11	Memory address line 11
I/O	Y26	MWE	Memory write enable

Table 8-1 Pinlist by Number

8.2 Pinlist by Name

The table below provides a brief description of each pin. It is organized alphabetically by pin name.

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VCC_2.5	A01		
VCC_2.5	A02		
VCC_2.5	A25		
VCC_2.5	A26		
GND	AA05		
GND	AA22		
GND	AB05		
GND	AB06		

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VDDQ	AB07		
VDDQ	AB08		
GND	AB09		
GND	AB10		
VDDQ	AB11		
VDDQ	AB12		
GND	AB13		
GND	AB14		
VDDQ	AB15		
VDDQ	AB16		
GND	AB17		
GND	AB18		
VDDQ	AB19		
VDDQ	AB20		
GND	AB21		
GND	AB22		
VCC_2.5	AC04		
VCC_2.5	AC23		
VCC_2.5	AD03		
VCC_2.5	AD24		
VCC_2.5	AE01		
VCC_2.5	AE02		
VCC_2.5	AE25		
VCC_2.5	AE26		
VCC_2.5	AF01		
VCC_2.5	AF02		
VCC_2.5	AF25		
VCC_2.5	AF26		
VCC_2.5	B01		
VCC_2.5	B02		
VCC_2.5	B25		
VCC_2.5	B26		
VCC_2.5	C03		
VCC_2.5	C24		

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VCC_2.5	D04		
VCC_2.5	D23		
GND	E05		
GND	E06		
VCC_3.3	E07		
VCC_3.3	E08		
GND	E09		
GND	E10		
VCC_3.3	E11		
VCC_3.3	E12		
GND	E13		
GND	E14		
VCC_3.3	E15		
VCC_3.3	E16		
GND	E17		
GND	E18		
VCC_3.3	E19		
VCC_3.3	E20		
GND	E21		
GND	E22		
GND	F05		
GND	F22		
VCC_3.3	G05		
VCC_3.3	G22		
VCC_3.3	H05		
VCC_3.3	H22		
GND	J05		
GND	J22		
GND	K05		
GND	K22		
VCC_3.3	L05		
GND	L11		
GND	L12		
GND	L13		

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
GND	L14		
GND	L15		
GND	L16		
VCC_3.3	L22		
GND	M11		
GND	M12		
GND	M13		
GND	M14		
GND	M15		
GND	M16		
VCC_3.3	M22		
GND	N11		
GND	N12		
GND	N13		
GND	N14		
GND	N15		
GND	N16		
GND	N22		
GND	P05		
GND	P11		
GND	P12		
GND	P13		
GND	P14		
GND	P15		
GND	P16		
GND	P22		
GND	R11		
GND	R12		
GND	R13		
GND	R14		
GND	R15		
GND	R16		
VCC_3.3	R22		
VCC_3.3	T05		

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
GND	T11		
GND	T12		
GND	T13		
GND	T14		
GND	T15		
GND	T16		
VCC_3.3	T22		
GND	U05		
GND	U22		
GND	V05		
GND	V22		
VCC_3.3	W05		
VCC_3.3	W22		
VCC_3.3	Y05		
VCC_3.3	Y22		
I/O	AE20	AGPADSTB_0	AGP AD 2X strobe
I/O	AF11	AGPADSTB_1	
I/O	AF20	AGPADSTBN_0	
I/O	AE11	AGPADSTBN_1	
I/O	AE05	AGPPipeN	AGP Pipelined Address
I/O	AD05	AGPRbfN	AGP Read Data Buffer full
I/O	AC06	AGPSBA_0	AGP Sideband Address 0
I/O	AE06	AGPSBA_1	AGP Sideband Address 1
I/O	AF06	AGPSBA_2	AGP Sideband Address 2
I/O	AC07	AGPSBA_3	AGP Sideband Address 3
I/O	AC08	AGPSBA_4	AGP Sideband Address 4
I/O	AD08	AGPSBA_5	AGP Sideband Address 5
I/O	AE08	AGPSBA_6	AGP Sideband Address 6
I/O	AF09	AGPSBA_7	AGP Sideband Address 7
I/O	AD07	AGPSBSTB	AGP Sideband Address 2X strobe
I/O	AE07	AGPSBSTBN	
I/O	AD04	AGPSt_0	AGP status 0
I/O	AE04	AGPSt_1	AGP status 1

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AC05	AGPSt_2	AGP status 2
I/O	AF04	AGPVCC_3.3_1	
I/O	AC09	AGPVCC_3.3_2	
I/O	AD14	AGPVCC_3.3_3	
I/O	AD18	AGPVCC_3.3_4	
I/O	AD22	AGPVCC_3.3_5	
I/O	AD02	AGPVoltSel	
I/O	AD23	AGPvREF	not connected
I/O	M04	DacAGnd	
I/O	N01	DacAGnd	
I/O	R02	DacAGnd	
I/O	R04	DacAGnd	DAC Power/Gnd pin
I/O	P01	DacAVDD	
I/O	P03	DacAVDD	
I/O	N05	DacAVDD	Analog/video DAC
I/O	P02	DacComp	Compensation pin
I/O	R03	DacFSAdj	
I/O	N03	DacVRef	
GND_C		gnd	
I/O	AC03	KClkIn	
I/O	AC25	MAddr_0	Memory address line 0
I/O	AC26	MAddr_1	Memory address line 1
I/O	Y24	MAddr_10	Memory address line 10
I/O	Y25	MAddr_11	Memory address line 11
I/O	AB24	MAddr_2	Memory address line 2
I/O	AB25	MAddr_3	Memory address line 3
I/O	AB26	MAddr_4	Memory address line 4
I/O	AA23	MAddr_5	Memory address line 5
I/O	AA24	MAddr_6	Memory address line 6
I/O	AA25	MAddr_7	Memory address line 7
I/O	AA26	MAddr_8	Memory address line 8
I/O	Y23	MAddr_9	Memory address line 9
I/O	V23	MBank_0	Video Stream reset

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	V24	MBank_1	Memory bank select 1
I/O	U23	MBank_2	Memory bank select 2
I/O	J26	MBank_3	Memory bank select 3
I/O	U24	MByte_0	Memory byte select 0
I/O	U26	MByte_1	Memory byte select 1
I/O	C19	MByte_10	Memory byte select 10
I/O	B18	MByte_11	Memory byte select 11
I/O	D08	MByte_12	Memory byte select 12
I/O	C09	MByte_13	Memory byte select 13
I/O	D09	MByte_14	Memory byte select 14
I/O	B09	MByte_15	Memory byte select 15
I/O	V25	MByte_2	Memory byte select 2
I/O	U25	MByte_3	Memory byte select 3
I/O	G23	MByte_4	Memory byte select 4
I/O	H25	MByte_5	Memory byte select 5
I/O	H24	MByte_6	Memory byte select 6
I/O	G24	MByte_7	Memory byte select 7
I/O	C18	MByte_8	Memory byte select 8
I/O	B19	MByte_9	Memory byte select 9
I/O	W25	MCAS	Memory CAS line
I/O	W26	MClkE	Memory clock enable
I/O	AB04	MclkIn	
I/O	L24	MDat_0	Memory data line 0
I/O	L25	MDat_1	Memory data line 1
I/O	T26	MDat_10	Memory data line 10
I/O	D2	MDat_100	Memory data line 100
I/O	E02	MDat_101	Memory data line 101
I/O	E03	MDat_102	Memory data line 102
I/O	F03	MDat_103	Memory data line 103
I/O	A09	MDat_104	Memory data line 104
I/O	D07	MDat_105	Memory data line 105
I/O	C08	MDat_106	Memory data line 106
I/O	B08	MDat_107	Memory data line 107
I/O	B07	MDat_108	Memory data line 108

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	C07	MDat_109	Memory data line 109
I/O	T23	MDat_11	Memory data line 11
I/O	D06	MDat_110	Memory data line 110
I/O	A08	MDat_111	Memory data line 111
I/O	A06	MDat_112	Memory data line 112
I/O	A05	MDat_113	Memory data line 113
I/O	C05	MDat_114	Memory data line 114
I/O	B05	MDat_115	Memory data line 115
I/O	B06	MDat_116	Memory data line 116
I/O	C06	MDat_117	Memory data line 117
I/O	D05	MDat_118	Memory data line 118
I/O	A07	MDat_119	Memory data line 119
I/O	R26	MDat_12	Memory data line 12
I/O	F01	MDat_120	Memory data line 120
I/O	E01	MDat_121	Memory data line 121
I/O	D01	MDat_122	Memory data line 122
I/O	C01	MDat_123	Memory data line 123
I/O	A03	MDat_124	Memory data line 124
I/O	C02	MDat_125	Memory data line 125
I/O	D03	MDat_126	Memory data line 126
I/O	E04	MDat_127	Memory data line 127
I/O	R25	MDat_13	Memory data line 13
I/O	R24	MDat_14	Memory data line 14
I/O	R23	MDat_15	Memory data line 15
I/O	N23	MDat_16	Memory data line 16
I/O	N26	MDat_17	Memory data line 17
I/O	N25	MDat_18	Memory data line 18
I/O	N24	MDat_19	Memory data line 19
I/O	L26	MDat_2	Memory data line 2
I/O	P23	MDat_20	Memory data line 20
I/O	P26	MDat_21	Memory data line 21
I/O	P25	MDat_22	Memory data line 22
I/O	P24	MDat_23	Memory data line 23
I/O	K23	MDat_24	Memory data line 24

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	K24	MDat_25	Memory data line 25
I/O	K25	MDat_26	Memory data line 26
I/O	K26	MDat_27	Memory data line 27
I/O	J25	MDat_28	Memory data line 28
I/O	J24	MDat_29	Memory data line 29
I/O	L23	MDat_3	Memory data line 3
I/O	J23	MDat_30	Memory data line 30
I/O	H23	MDat_31	Memory data line 31
I/O	D21	MDat_32	Memory data line 32
I/O	C22	MDat_33	Memory data line 33
I/O	B22	MDat_34	Memory data line 34
I/O	A22	MDat_35	Memory data line 35
I/O	A23	MDat_36	Memory data line 36
I/O	B23	MDat_37	Memory data line 37
I/O	A24	MDat_38	Memory data line 38
I/O	B24	MDat_39	Memory data line 39
I/O	M26	MDat_4	Memory data line 4
I/O	G25	MDat_40	Memory data line 40
I/O	G26	MDat_41	Memory data line 41
I/O	F26	MDat_42	Memory data line 42
I/O	F25	MDat_43	Memory data line 43
I/O	F24	MDat_44	Memory data line 44
I/O	F23	MDat_45	Memory data line 45
I/O	E24	MDat_46	Memory data line 46
I/O	E23	MDat_47	Memory data line 47
I/O	C23	MDat_48	Memory data line 48
I/O	C25	MDat_49	Memory data line 49
I/O	M25	MDat_5	Memory data line 5
I/O	C26	MDat_50	Memory data line 50
I/O	D24	MDat_51	Memory data line 51
I/O	D25	MDat_52	Memory data line 52
I/O	D26	MDat_53	Memory data line 53
I/O	E26	MDat_54	Memory data line 54
I/O	E25	MDat_55	Memory data line 55

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	D20	MDat_56	Memory data line 56
I/O	C21	MDat_57	Memory data line 57
I/O	B21	MDat_58	Memory data line 58
I/O	A21	MDat_59	Memory data line 59
I/O	M24	MDat_6	Memory data line 6
I/O	A20	MDat_60	Memory data line 60
I/O	B20	MDat_61	Memory data line 61
I/O	C20	MDat_62	Memory data line 62
I/O	D19	MDat_63	Memory data line 63
I/O	D12	MDat_64	Memory data line 64
I/O	C12	MDat_65	Memory data line 65
I/O	B12	MDat_66	Memory data line 66
I/O	C13	MDat_67	Memory data line 67
I/O	D14	MDat_68	Memory data line 68
I/O	B13	MDat_69	Memory data line 69
I/O	M23	MDat_7	Memory data line 7
I/O	A13	MDat_70	Memory data line 70
I/O	D13	MDat_71	Memory data line 71
I/O	D17	MDat_72	Memory data line 72
I/O	C17	MDat_73	Memory data line 73
I/O	B17	MDat_74	Memory data line 74
I/O	A18	MDat_75	Memory data line 75
I/O	A17	MDat_76	Memory data line 76
I/O	A16	MDat_77	Memory data line 77
I/O	B16	MDat_78	Memory data line 78
I/O	C16	MDat_79	Memory data line 79
I/O	T24	MDat_8	Memory data line 8
I/O	C14	MDat_80	Memory data line 80
I/O	B14	MDat_81	Memory data line 81
I/O	A14	MDat_82	Memory data line 82
I/O	A15	MDat_83	Memory data line 83
I/O	D16	MDat_84	Memory data line 84
I/O	B15	MDat_85	Memory data line 85
I/O	C15	MDat_86	Memory data line 86

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	D15	MDat_87	Memory data line 87
I/O	C11	MDat_88	Memory data line 88
I/O	B11	MDat_89	Memory data line 89
I/O	T25	MDat_9	Memory data line 9
I/O	A11	MDat_90	Memory data line 90
I/O	A12	MDat_91	Memory data line 91
I/O	D11	MDat_92	Memory data line 92
I/O	B10	MDat_93	Memory data line 93
I/O	C10	MDat_94	Memory data line 94
I/O	D10	MDat_95	Memory data line 95
I/O	C04	MDat_96	Memory data line 96
I/O	B04	MDat_97	Memory data line 97
I/O	A04	MDat_98	Memory data line 98
I/O	B03	MDat_99	Memory data line 99
I/O	W23	MDSF	Memory DSF line
I/O	AB23	MemClkOut_0	Memory Clock Out 0
I/O	AC24	MemClkOut_1	Memory clock out 1
I/O	AD25	MemClkOut_2	Memory Clock Out 2
I/O	AD26	MemClkOut_3	Memory Clock Out 3
I/O	V26	MemClkRet_0	Memory Clock Return 0
I/O	H26	MemClkRet_1	Memory Clock Return 1
I/O	A19	MemClkRet_2	Memory Clock Return 2
I/O	A10	MemClkRet_3	Memory Clock Return 3
I/O	W24	MRAS	Memory RAS line
I/O	Y26	MWE	Memory write enable
I/O	AF23	PCIAD_0	PCI address/data line 0
I/O	AE23	PCIAD_1	PCI address/data line 1
I/O	AE19	PCIAD_10	PCI address/data line 10
I/O	AD19	PCIAD_11	PCI address/data line 11
I/O	AC19	PCIAD_12	PCI address/data line 12
I/O	AF18	PCIAD_13	PCI address/data line 13
I/O	AE18	PCIAD_14	PCI address/data line 14
I/O	AC18	PCIAD_15	PCI address/data line 15
I/O	AD15	PCIAD_16	PCI address/data line 16

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AE14	PCIAD_17	PCI address/data line 17
I/O	AF14	PCIAD_18	PCI address/data line 18
I/O	AE13	PCIAD_19	PCI address/data line 19
I/O	AF22	PCIAD_2	PCI address/data line 2
I/O	AC14	PCIAD_20	PCI Address/Data line 20
I/O	AC13	PCIAD_21	PCI address/data line 21
I/O	AD13	PCIAD_22	PCI address/data line 22
I/O	AC12	PCIAD_23	PCI address/data line 23
I/O	AD12	PCIAD_24	PCI address/data line 24
I/O	AD11	PCIAD_25	PCI address/data line 25
I/O	AC11	PCIAD_26	PCI address/data line 26
I/O	AF10	PCIAD_27	PCI address/data line 27
I/O	AE10	PCIAD_28	PCI address/data line 28
I/O	AC10	PCIAD_29	PCI address/data line 29
I/O	AE22	PCIAD_3	PCI address/data line 3
I/O	AE09	PCIAD_30	PCI address/data line 30
I/O	AD09	PCIAD_31	PCI address/data line 31
I/O	AC22	PCIAD_4	PCI address/data line 4
I/O	AF21	PCIAD_5	PCI address/data line 5
I/O	AE21	PCIAD_6	PCI address/data line 6
I/O	AD21	PCIAD_7	PCI address/data line 7
I/O	AC20	PCIAD_8	PCI address/data line 8
I/O	AF19	PCIAD_9	PCI address/data line 9
I/O	AD20	PCICBEN_0	PCI byte enable 0
I/O	AF17	PCICBEN_1	PCI byte enable 1
I/O	AC15	PCICBEN_2	PCI Byte Enable 2
I/O	AE12	PCICBEN_3	PCI byte enable 3
I/O	AC02	PCICLK	PCI clock
I/O	AC01	PCIClkSel	33/66 MHz PCI Select
I/O	AD16	PCIDevSelN	PCI device select
I/O	AB01	PCIFIFOInDis	Disable PCI Input FIFO
I/O	AB02	PCIFIFOOutDis	Disable PCI Output FIFO
I/O	AC16	PCIFrameN	PCI Frame Signal
I/O	AF03	PCIGntN	PCI grant signal

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	AF13	PCIIdSel	PCI ID select
I/O	AD01	PCIIntAN	PCI interrupt
I/O	AE15	PCIIRdyN	PCI ready
I/O	AE17	PCIPar	PCI parity
I/O	AE03	PCIReqN	PCI request
I/O	AB03	PCIRSTN	PCI reset
I/O	AD17	PCIStopN	PCI stop
I/O	AE16	PCITRdyN	PCI T ready
I/O	T02	PLLDISABLE	PLL Disable
I/O	Y04	PLLGND	PLL Power/Gnd pin
I/O	W01	PLLPower	PLL Power/Gnd pin
I/O	D18	RenderSyncN	Multi-rasterizer i/o sync
I/O	U01	ROMSelectN	ROM Select signal
I/O	V04	ROMWeN	ROM Write Enable
I/O	V01	SBClk	Serial bus clock
I/O	W04	SBData	serial bus data
I/O	AA01	SClkIn	
I/O	AC17	**SPARE**	
I/O	AC21	**SPARE**	
I/O	AD06	**SPARE**	
I/O	AD10	**SPARE**	
I/O	AF05	**SPARE**	
I/O	AF07	**SPARE**	
I/O	AF08	**SPARE**	
I/O	AF12	**SPARE**	
I/O	AF15	**SPARE**	
I/O	AF16	**SPARE**	
I/O	AF24	**SPARE**	
I/O	T03	TestMode	TestMode control
I/O	L03	TestSel_0	Test Mode Select 0
I/O	R05	TestSel_1	Test Mode Select 1
I/O	M05	TestSel_2	Test Mode Select 2
VCC_3.3		vcc_3.3	

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
VCC_2.5		vdd	
VDDQ		vddq	
I/O	P04	VidBlue	Analog blue signal
I/O	U03	VidDDCClk	Clock line for DDC
I/O	U02	VidDDCData	Data line for DDC
I/O	D22	VideoExtCtrl	Video External control
I/O	N02	VidGreen	Analog green signal
I/O	R01	VidHSync	Horizontal sync
I/O	N04	VidRed	Analog red signal
I/O	M03	VidRightEye	
I/O	T01	VidVsync	Vertical sync
I/O	V02	VSAClk	VideoStream A clock
I/O	AA04	VSAData_0	VideoStream A data line 0 (BaseClassZero config)
I/O	AA03	VSAData_1	VideoStream A data line 1 (VGAEnable config)
I/O	AA02	VSAdata_2	VideoStream A data line 2 (VGAFixed config)
I/O	Y01	VSAData_3	VideoStream A data line 3 (RetryDisable config)
I/O	Y03	VSAData_4	VideoStream A data line 4 (ShortReset config)
I/O	W02	VSAData_5	VideoStream A data line 5 (AGP1Xcapable config)
I/O	Y02	VSAData_6	VideoStream A data line 6 AGP2Xcapable config)
I/O	W03	VSAData_7	VideoStream A data line 7 AGP4Xcapable config)
I/O	V03	VSAResetN	
I/O	H04	VSBClk	VideoStream B clock
I/O	J03	VSBClkOut	Video Streams B Clock Out
I/O	F04	VSBData_0	VideoStream B data line 0 (SBACapable config)
I/O	G01	VSBData_1	VideoStream B data line 1 (SubsystemFromROM config)
I/O	G02	VSBData_2	VideoStream B data line 2 (IndirectIOEnable config)
I/O	G03	VSBData_3	VideoStream B data line 3 (WCEnable config)

NET TYPE	BGA PAD	SIGNAL NAME	DESCRIPTION
I/O	G04	VSBData_4	VideoStream B data line 4 (PrefetchEnable config)
I/O	H01	VSBData_5	VideoStream B data line 5
I/O	H02	VSBData_6	VideoStream B data line 6
I/O	H03	VSBData_7	VideoStream B data line 7
I/O	F02	VSBResetN	Video Stream B Reset Out
I/O	J04	VSCtl_0	VideoStreams Control line 0
I/O	K01	VSCtl_1	VideoStreams Control line 1
I/O	K04	VSCtl_2	VideoStreams Control line 2
I/O	L04	VSCtl_3	VideoStreams Control line 3
I/O	L01	VSCtl_4	VideoStreams Control line 4
I/O	L02	VSCtl_5	VideoStreams Control line 5
I/O	M01	VSCtl_6	VideoStreams Control line 6
I/O	M02	VSCtl_7	VideoStreams Control line 7
I/O	K02	VSGPChipSelectN	VS GP bus chip select
I/O	K03	VSGPDataAckN	VS GP bus data ack
I/O	J01	VSGPDataStrobeN	VS GP bus data strobe
I/O	J02	VSGPReadWriteN	VS GP bus read/write signal
GND_IO		vsso	
I/O	T04	Xtal1	Crystal i/p 1
I/O	U04	Xtal2	Crystal i/p 2
I/O	AE24	ZSET	

9

Memory System

The Permedia4 memory system is intended for use with Synchronous Dynamic Memories. The memories can be SGRAM or SDRAM devices. The width of the memory interface is 128 bits, but can be configured to 64 bits. Control lines are provided for 4 blocks of memories, these are Select (3 – 0). Four ClockOut and ClockReturn signals are also provided, these are to assist in de-skewing the return data and reducing the load on each clock line. The Clock lines should be wired as illustrated in Figure 9.1.

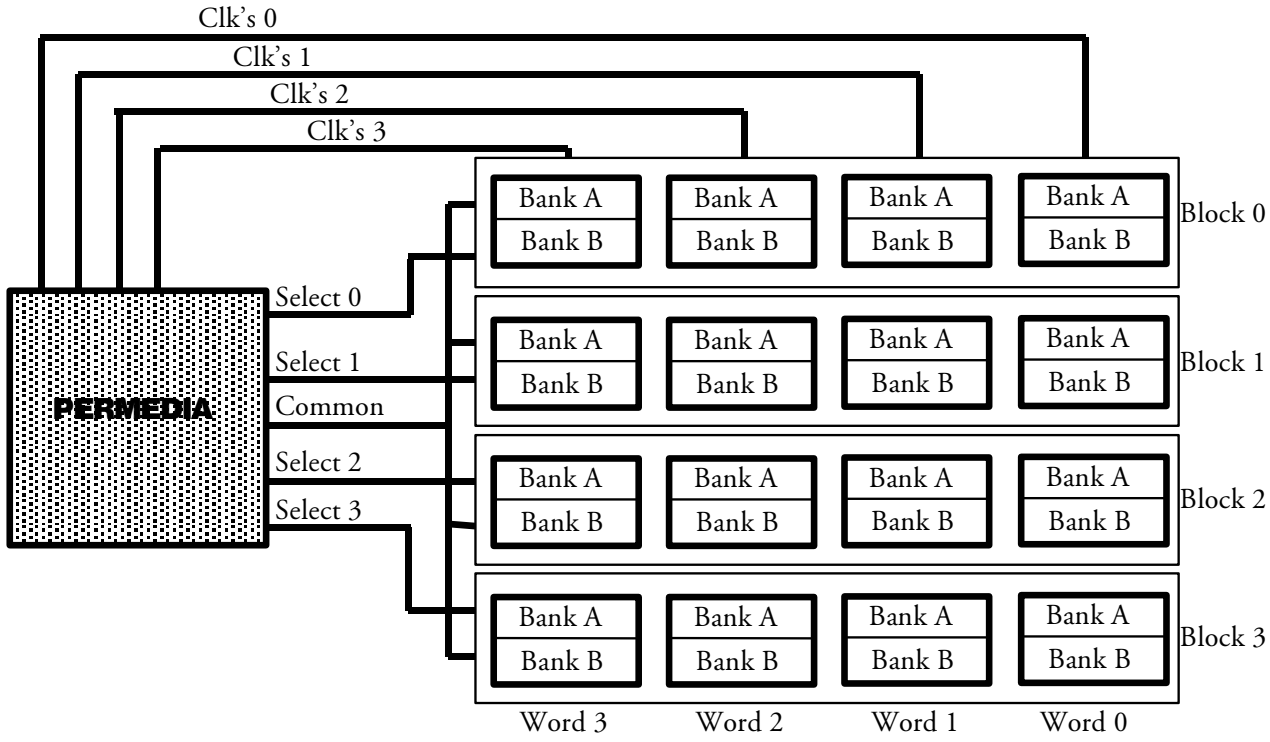


Figure 9.1 Organization of memory devices

The diagram shows a 32-megabyte memory array, constructed from 16, 16-Megabit memories, arranged into 4 blocks. The devices used are 32 bit wide with 2 banks. This layout would typically be used with SGRAMs for, e.g., CAD workstations.

To address all targeted market segments PERMEDIA4 supports 64 and 128 bit wide memory arrays for optimum price/performance positioning. The maximum configuration is 32Mbytes SDRAM or SGRAM, however configurations down to 2MB are supported. For representative layouts see chapter 5, section 5.4 of the *Permedia4 Architecture Overview.*

- Using two 64Mbit x 32 SDRAM memory devices to give 16 Mbytes on a 64 bit bus is the cost effective, minimum part count memory organization.
- A mid-range memory organization uses four 64 Mbit x 32 SDRAM memory devices to give 32 Mbytes on a 128 bit bus.

- Four banks of devices give 32 Mbyte configurations suitable for smaller SGRAM devices and higher performance needs, as shown above.

The memory array requires no external logic and has been designed to deliver optimum performance on low cost boards by minimizing susceptibility to signal skew.

9.1 System Parameters

The Memory System employs a rich set of registers, which allow for a diverse range of memory configurations. The various timing parameters used to control synchronous memories can be adjusted to allow for optimum performance depending on memory type, speed grade and the PERMEDIA system clock frequency (MClk). Memory functionally can be enabled depending on the type fitted. Full addressing control is available so that virtually any memory configuration can be fitted.

The following parameters are used to control accesses to the memory. These values fall into three categories

- Addressing
- Functionality and Optimizations
- Timing and Mode

9.1.1 Addressing

9.1.1.1 ColumnAddress

This parameter defines the number of address bits required to generate the column addresses for the memory devices fitted. This parameter is normally quoted in the memory device data sheet.

For example CA7~CA0 therefore the Column Address parameter would be 8

9.1.1.2 RowAddress

This parameter defines the number of address bits required to generate the row addresses for the memory device fitted. This parameter is normally quoted in the memory device data sheet.

For example RA8~RA0 therefore the Row Address parameter would be 9

9.1.1.3 BankAddress

This parameter defines the number of address bits required to generate the bank addresses for the memory device fitted. This parameter is normally quoted in the memory device data sheet.

Note: When using InterLeave with AddressExtension the BankAddress value is incremented by 1.

For example A9(BA) therefore the Bank Address parameter would be 1

9.1.1.4 ChipSelect

This parameter defines the number of address bits needed to select all the blocks of memory devices fitted to the PERMEDIA device.

For 1 Block of memories	Chip Select = 1
For 2 Blocks of memories	Chip Select = 1
For 3 Blocks of memories	Chip Select = 2
For 4 Blocks of memories	Chip Select = 2

9.1.1.5 PageSize

This parameter defines the address range for a memory page of the memory array fitted. The value can be calculated as (column address bits of device – 5). The PageSize parameter modified if either Interleave (0) or Halfwidth (9.1.1.9) are set. PageSize can be calculated as ((column address bits) – 5) + Interleave – Halfwidth.

9.1.1.6 RegionSize

This parameter defines the addressing range for each of the four page-detectors implemented in the memory controller. The minimum region a page-detector can be assigned to is one internal bank, the maximum is all of the memory fitted. There are some memory configurations where not all the page-detectors can be deployed. An example of this is when three blocks of memory devices are used. The value can be calculated as

Where

TotalMemory = The total size of memory fitted in

$$\mathrm{Log2}\left(\frac{\mathrm{TotalMemory}}{\mathrm{BytesperMemWidth} \times \mathrm{RegionsUsed}}\right) - 5$$

megabytes

Bytes per Memory Width = 16 (128 / 8)

Regions Used =

(if total number of Banks (Blocks fitted x Internal Banks) > 4

then Blocks Fitted

else Total Banks)

As an example the memory configuration in Figure 9-1 is constructed from sixteen 8-megabit devices each with two internal banks

TotalMemory = 16777216 (16-megabytes)

Bytes per Memory Width = 16

Regions Used = (Blocks fitted = 4) x (Internal Banks = 2) = 8

= 8 > 4

= 4

$$\text{Log2}\left(\frac{16777216}{16\times 4}\right)-5$$

RegionSize = 13

9.1.1.7 CombineBanks

This flag should be set, when the total number of banks fitted is greater than 4. The total number of banks can be determined by multiplying the number of internal banks of the device by the number of device blocks fitted. In the example shown in Figure 9-1, there are 4 device blocks fitted (Blocks 0 to 3), each device has 2 internal banks (Banks A and B), so the total number of banks is 8, therefore CombineBanks should be set.

9.1.1.8 InterLeave

This flag when set doubles the page size of the memory array. This is accomplished by combining two blocks of memory and operating them as one. Both blocks are PRECHARGED and ACTIVATED together, and any command sequences issued that cross from one block to the other, do so without incurring a page break. From the example configuration detailed in Figure 9-1, Block 1 would interleave with Block 0, and Block 3 with Block 2. When this flag is set the value loaded into the PageSize parameter (9.1.1.5) should be increased by one. As the Blocks are now operating in pairs the total number of banks fitted is halved. This may have a bearing on the CombineBanks flag (9.1.1.7).

Note: When using InterLeave with AddressExtension the BankAddress value is incremented by 1.

9.1.1.9 HalfWidth

This flag should be set only when the memory buffer fitted is 64 bits wide. When set, this flag has an impact on the PageSize register, (section 9.1.1.5).

9.1.2 Functionality and Optimizations

9.1.2.1 NoPrechargeOpt

This flag when set will disable the back to back READ - PRECHARGE optimization, inserting clocks to the value of the CAS Latency between the commands. If the memory devices fitted are capable of executing a READ command directly followed by a PRECHARGE command, this flag should be left clear for optimal performance.

9.1.2.2 SpecialModeOpt

This flag when set enables the memory controller to issue a Special Mode Register Set (SMRS) command, without regard to the current state of the internal banks of the SGRAM. Some memory devices require all internal banks to be in the same state before an SMRS command is issued. For these devices, ensure that the flag is cleared. The memory controller will issue a PRECHARGE command to the devices to ensure all internal banks are in the IDLE mode before issuing the SMRS command. If the memory devices fitted are capable of this function, optimally this flag should be set.

9.1.2.3 TwoColorBlockFill

This flag when set allows the memory controller to utilize the 2 internal Color Registers that some SGRAM devices are equipped with. If the memory devices fitted only have 1 Color Register, this flag should be cleared. When this flag is cleared the memory controller will fully emulate the two color fill operations.

9.1.2.4 NoWriteMask

This flag when set disables the memory controller from using the internal MASK Register of an SGRAM. This flag must be set if SDRAMS are fitted. When this flag is set, the memory controller will emulate the write mask operations. This is only a partial emulation using the byte enables so bit precision is not achieved.

9.1.2.5 NoBlockFill

This flag when set disables the memory controller from issuing a Block Fill command to the memories. This flag must be set if SDRAMS are fitted. When this flag is set the memory controller will fully emulate the block fill operations.

9.1.2.6 NoLookAhead

This flag when set disables the memory controller from issuing command to one bank of memory, whilst another bank is in the process of PRECHARGHING. Nominally for performance, this flag should be left cleared.

9.1.3 Timing and Mode

9.1.3.1 TurnOn (Block to Block Read Delay)

This parameter defines the number of MClk cycles that need to be inserted between issuing a READ command to one block of memory devices to a READ of another Block. (Block to Block Read Delay). Two parameters from the memory device data sheet must be used to determine what value TurnOn must be set to. The timing parameter tHZ defines the tri-state time and the parameter tLZ defines the drive time of the device. If tLZ is greater than tHZ, then this parameter can safely be set to zero.

9.1.3.2 TurnOff (Read to Write Turn around)

This parameter defines the number of MClk cycles that need to be inserted between issuing a READ and a WRITE command (Read – Write turn around). This parameter is defined in the memory device data sheet, usually as tHZ.

9.1.3.3 RegisterLoad (RL)

This parameter defines the number of MClk cycles that need to be inserted between issuing a SMRS and another command. This parameter is usually detailed in the memory device data sheet as tRSC. If tRSC is quoted including the SMRS cycle, then RegisterLoad should be calculated as tRSC (in MClk cycles) – 1.

9.1.3.4 BlockWrite (BW)

This parameter defines the number of MClk cycles that need to be inserted between issuing a BLOCK WRITE and another command. This parameter is usually detailed in the memory device data sheet as tBWC. If tBWC is quoted including the SMRS cycle, then BlockWrite should be calculated as tBWC (in MClk cycles) – 1.

9.1.3.5 ActivateToCommand (ATC)

This parameter defines the number of MClk cycles that need to be inserted between issuing an ACTIVATE and a command. This parameter is usually detailed in the memory device data sheet as tRCD. If tRCD is quoted including the ACTIVATE cycle, then ActivateToCommand should be calculated as tRCD (in MClk cycles) – 1.

9.1.3.6 PrechargeToActivate (PTA)

This parameter defines the number of MClk cycles that need to be inserted between issuing a PRECHARGE and an ACTIVATE command. This parameter is usually detailed in the memory device data sheet as tRP. If tRP is quoted including the PRECHARGE cycle, then PreChargeToActivate should be calculated as tRP (in MClk cycles) – 1.

9.1.3.7 BlockWriteToPrecharge (BTP)

This parameter defines the number of MClk cycles that need to be inserted between issuing a BLOCKWRITE and a PRECHARGE command. This parameter is usually detailed in the memory device data sheet as tBPL (tBWR). If tBPL is quoted including the BLOCKWRITE cycle, then BlockWriteToPrecharge should be calculated as tBPL (in MClk cycles) – 1.

9.1.3.8 WriteToPrecharge (WTP)

This parameter defines the number of MClk cycles that need to be inserted between issuing a WRITE and a PRECHARGE command. This parameter is usually detailed in the memory device data sheet as tRDL (tWR). If tRDL is quoted including the WRITE cycle, then WriteToPrecharge should be calculated as tRDL (in MClk cycles) – 1.

9.1.3.9 ActivateToPrecharge (ATP)

This parameter defines the number of MClk cycles that need to be inserted between issuing an ACTIVATE and a PRECHARGE command. This parameter is usually detailed in the memory device data sheet as tRAS. If tRAS is quoted including the ACTIVATE cycle, then ActivateToPrecharge should be calculated as tRAS (in MClk cycles) – 1.

9.1.3.10 RefreshCycle (RC)

This parameter defines the number of MClk cycles that need to be inserted between issuing a REFRESH and an ACTIVATE command. This parameter is usually detailed in the memory device data sheet as tRC. If tRC is quoted including the REFRESH command cycle, then RefreshCycle should be calculated as tRC (in MClk cycles) – 1.

9.1.3.11 CasLatency (CL)

This parameter determines the CAS latency expected by the memory controller. The CasLatency parameter can be loaded directly with the appropriate value from the memory device data sheet. For example, if a CAS latency of 2 is required then the CasLatency parameter should be set to 2.

9.1.3.12 Mode

This parameter defines the value of the Mode Register loaded into the SGRAM at the end of the boot sequence (see data sheet). Items to note: Burst type should be sequential, burst length should be set to one and CAS latency should be consistent with the CASLatency parameter. For devices that have a Color Register field, this should be

consistent with the TwoColorBlockFill flag. All other bits in the Mode field should be set low.

9.1.3.13 RefreshEnable

This flag should be set for Refresh commands to be issued by the memory controller.

9.1.3.14 RefreshCount

This parameter defines the period between AUTO-REFRESH commands being issued to the synchronous memories. The count is in ((MClks/32) + 16) i.e. if RefreshCount = 1, the synchronous memories will be refreshed every 48 MClk cycles. For the required refresh rate, see the synchronous memory data sheet.

9.2 Example Parameter Values

The following device types and values are given as examples and should not be taken as recommendations.

9.2.1 100MHz/Samsung KM4132G271A-10 SGRAM /total SGRAM 12MB

For a PERMEDIA device running with an MClk of 100MHz, fitted with 12, 8Mbit, 2x512x256x32 SGRAMS arranged into 3 Blocks.

Table 9.1 100MHz/Samsung KM4132G271A-10 SGRAM /total SGRAM 12MB

Addressing Parameters	Value (binary)	Comment
ColumnAddress	1000	8
RowAddress	1001	9
BankAddress	0001	1 (2 Banks A/B)
ChipSelect	0010	2 (3 Blocks)
PageSize	0011	3 (256)
RegionSize	1101	13 (4 MB)
CombineBanks	1	6 = 3 Blocks x 2Banks
Interleave	0	Optional
HalfWidth	0	Unavailable 128 bit

Functionality Parameters	Value (binary)	Comment
NoPrechargeOpt	0	Preferred
SpecialModeOpt	1	Preferred
TwoColorBlockFill	0	Only 1 Color Register
NoWriteMask	0	Preferred
NoBlockFill	0	Preferred
NoLookAhead	0	Preferred

Timing and Mode Parameters	Value (binary)	Comment
TurnOn (Block to Block Read)	01	Tshz 7ns
TurnOff (Read to Write)	01	Tshz 7ns
RegisterLoad (RL)	00	New command next Clk

Timing and Mode Parameters	Value (binary)	Comment
BlockWrite (BW)	01	Tbwc 20ns, 2Clk -1
ActivateToCommand (ATC)	001	Trcd 20ns, 2Clk –1
PrechargeToActivate (PTA)	010	Trp 26ns, 3Clk -1
BlockWriteToPrecharge (BTP)	001	Tbpl 20ns, 2Clk -1
WriteToPrecharge (WTP)	000	Trdl 1Clk -1
ActivateToPrecharge (ATP)	0100	Tras 50ns, 5Clk –1
RefreshCycle (RC)	0111	Trc 80ns 8Clk -1
CasLatency (CL)	011	CasLatency 3
Mode	0000110000	CL3
RefreshEnable	1	
RefreshCount	0110000	64432 Refresh c/s

9.2.2 125MHz[2]/SIEMENS HYB39S16320-7 SGRAM /total SGRAM 16MB

For a PERMEDIA device running with an MClk of 125MHz, fitted with 8, 16Mbit, 2x1024x256x32 SGRAMS arranged into 2 Blocks.

Table 9.2 125MHz/SIEMENS HYB39S16320-7 SGRAM /total SGRAM 16MB

Addressing Parameters	Value (binary)	Comment
ColumnAddress	1000	8
RowAddress	1010	10
BankAddress	0001	1 (2 Banks A/B)
ChipSelect	0001	1 (2 Blocks)
PageSize	0011	3 (256)
RegionSize	1101	13 (4 MB)
CombineBanks	0	4 = 2 Blocks x 2Banks
Interleave	0	Optional
HalfWidth	0	Unavailable 128 bit

Functionality Parameters	Value (binary)	Comment
NoPrechargeOpt	0	Preferred
SpecialModeOpt	1	Preferred
TwoColorBlockFill	1	Preferred
NoWriteMask	0	Preferred
NoBlockFill	0	Preferred
NoLookAhead	0	Preferred

Timing and Mode Parameters	Value (binary)	Comment
TurnOn (Block to Block Read)	01	Thz 8ns
TurnOff (Read to Write)	01	Thz 8ns
RegisterLoad (RL)	01	Trsc 2Clk -1
BlockWrite (BW)	01	Tbwc 14ns, 2Clk -1
ActivateToCommand (ATC)	010	Trcd 21ns, 3Clk –1
PrechargeToActivate (PTA)	010	Trp 21ns, 3Clk -1
BlockWriteToPrecharge (BTP)	001	Tbwr 14ns, 2Clk -1
WriteToPrecharge (WTP)	000	Trdl 1Clk -1
ActivateToPrecharge (ATP)	0110	Tras 49ns, 7Clk –1
RefreshCycle (RC)	1001	Trc 70ns 9Clk -1
CasLatency (CL)	010	CasLatency 2
Mode	0001100000	2 Color Reg + CL2
RefreshEnable	1	
RefreshCount	0111100	64566 Refresh c/s

[2] Please note: 125MHz MClk is provisional.

4.1.1 125MHz[3]/ MICRON MT48LC1M16A1-8A SDRAM /total SDRAM 16MB

For a PERMEDIA device running with an MClk of 125MHz, fitted with 8, 16Mbit, 2x2048x256x16 SDRAMS arranged into 1 Block.

Table 9.3 125MHz/MICRON MT48LC1M16A1-8A SDRAM /total SDRAM 16MB

Addressing Parameters	Value (binary)	Comment
ColumnAddress	1000	8
RowAddress	1011	11
BankAddress	0001	1 A/B
ChipSelect	0001	1 (1 Blocks)
PageSize	0011	3 (256)
RegionSize	1101	14 (8 MB)
CombineBanks	0	2 = 1 Block x 2Banks
Interleave	0	Unavailable only 1 block
HalfWidth	0	Unavailable 128 bit

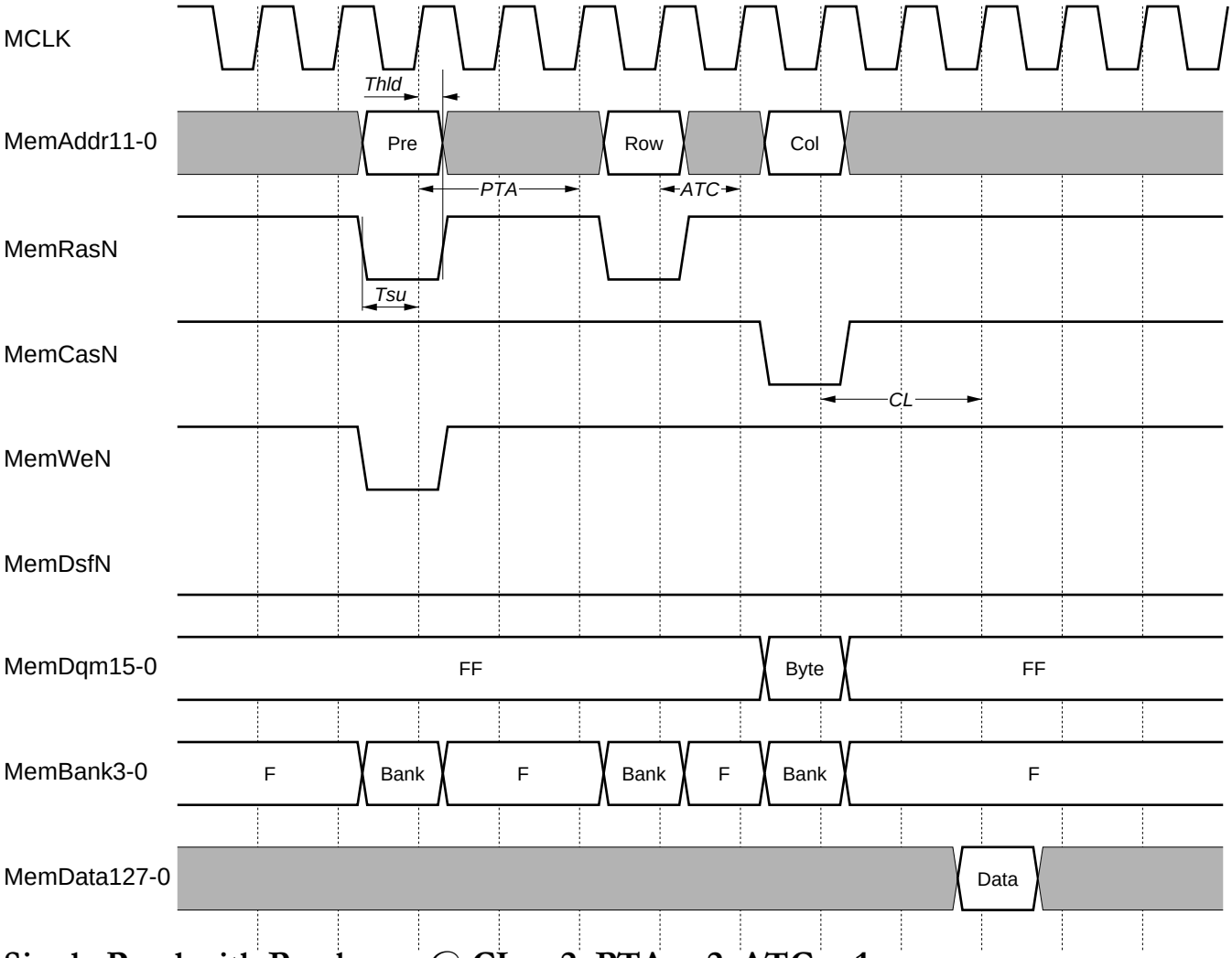
Functionality Parameters	Value (binary)	Comment
NoPrechargeOpt	0	Preferred
SpecialModeOpt	1	Preferred
TwoColorBlockFill	0	Unavailable
NoWriteMask	1	Unavailable
NoBlockFill	1	Unavailable
NoLookAhead	0	Preferred

Timing and Mode Parameters	Value (binary)	Comment
TurnOn (Block to Block Read)	01	Thz 7ns
TurnOff (Read to Write)	01	Thz 7ns
RegisterLoad (RL)	01	Tmrd 2Clk -1
BlockWrite (BW)	00	NA
ActivateToCommand (ATC)	011	Trcd 30ns, 4Clk –1
PrechargeToActivate (PTA)	011	Trp 30ns, 4Clk -1
BlockWriteToPrecharge (BTP)	000	NA
WriteToPrecharge (WTP)	000	Twr 1Clk -1
ActivateToPrecharge (ATP)	0110	Tras 50ns, 7Clk –1
RefreshCycle (RC)	1001	Trc 80ns 10Clk -1
CasLatency (CL)	010	CasLatency 2
Mode	0000100000	CL2
RefreshEnable	1	
RefreshCount	0111100	64566 Refresh c/s

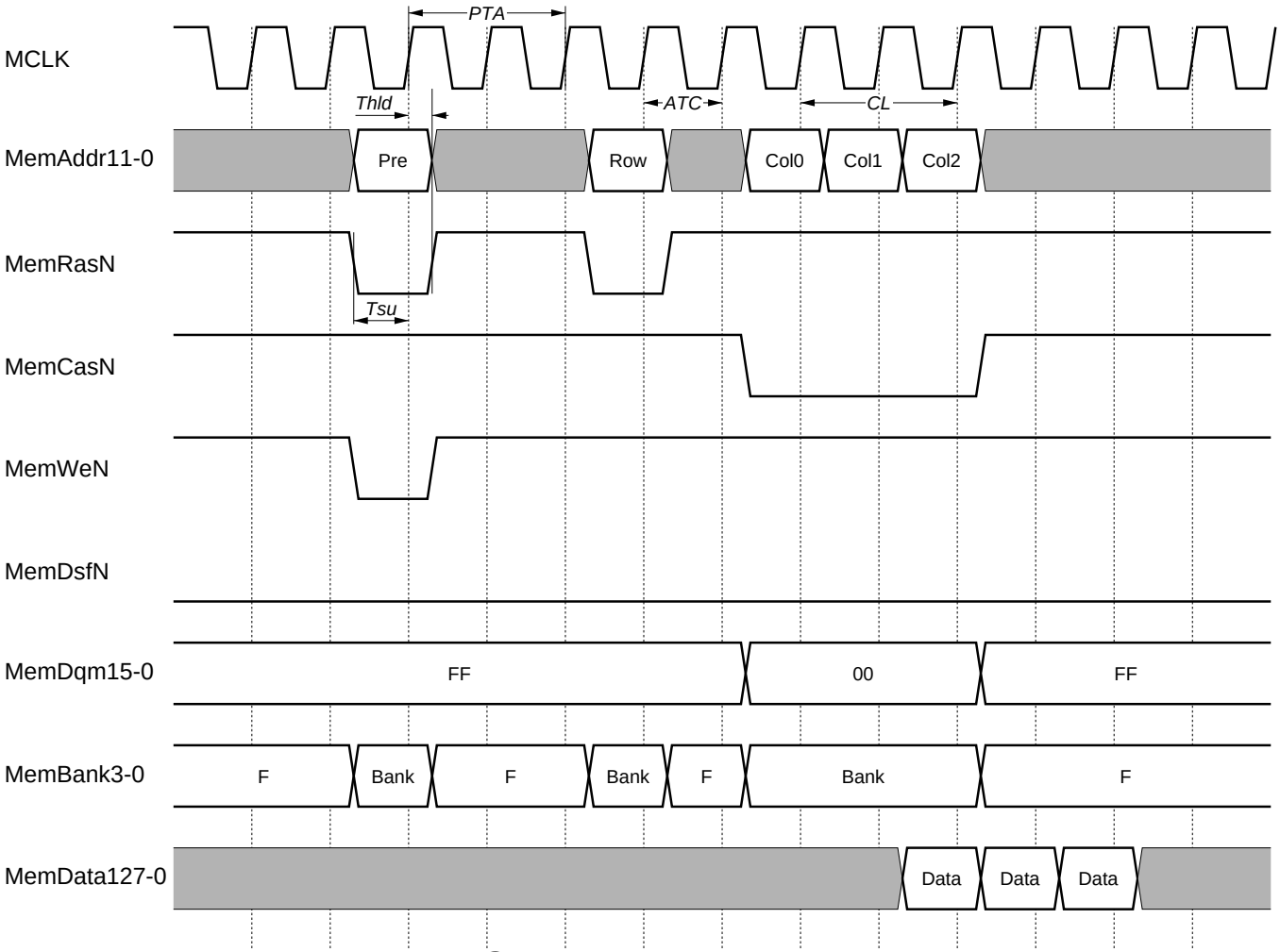
[3] Please note: 125MHz MClk is provisional.

9.3 Timing Diagrams

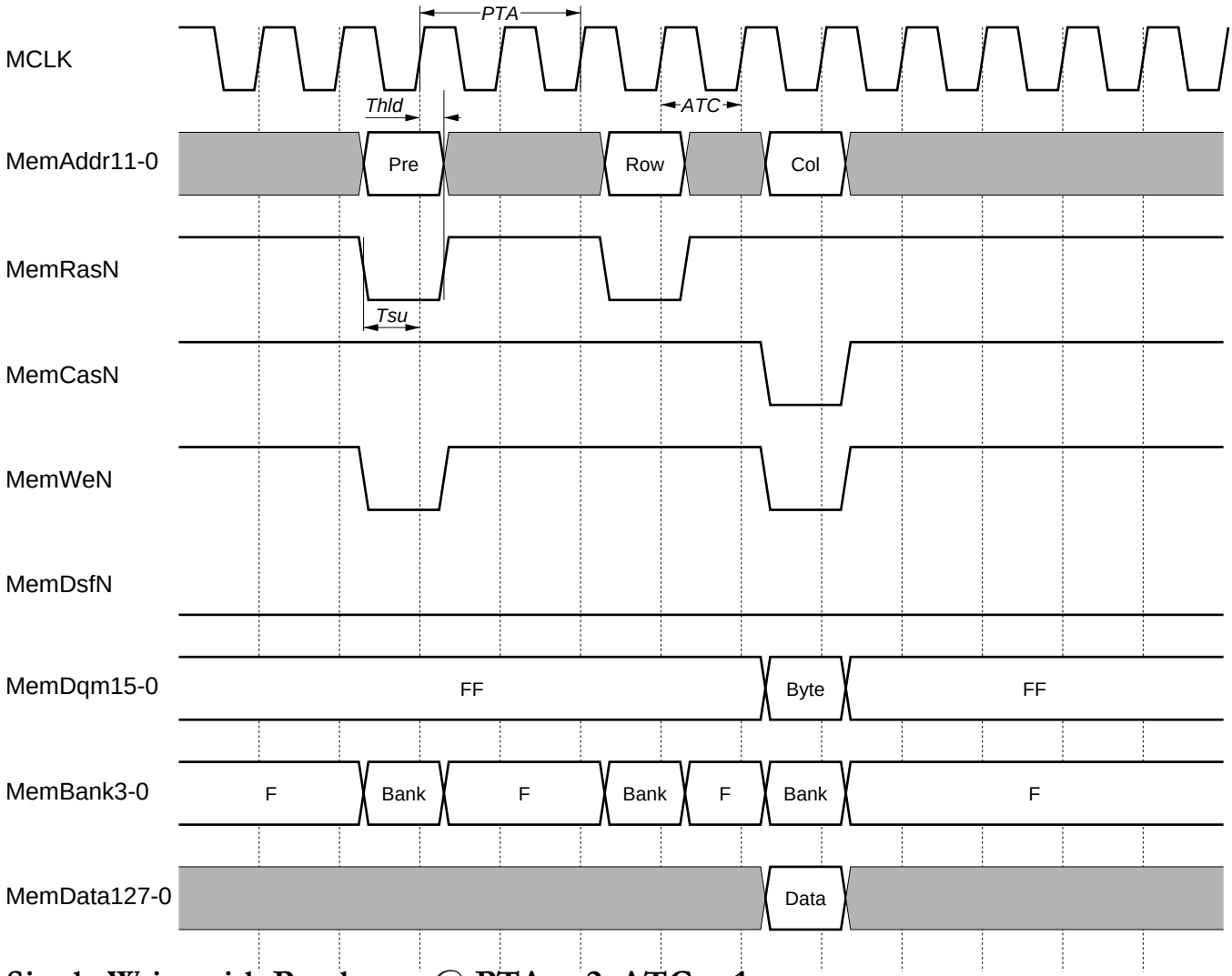
The following timing diagrams show specific operations of the memory controller.



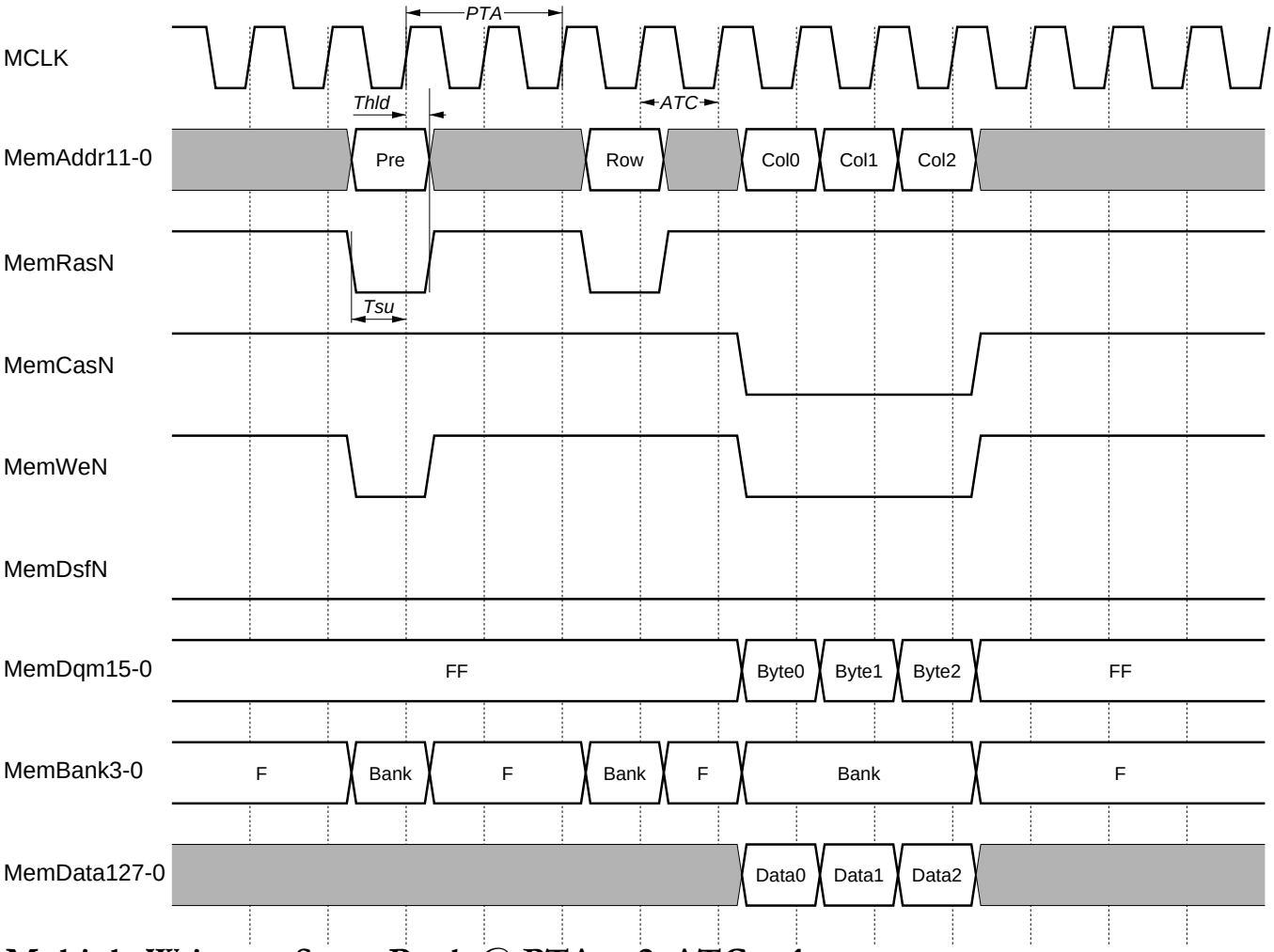
Single Read with Precharge @ CL = 2, PTA = 2 ATC = 1



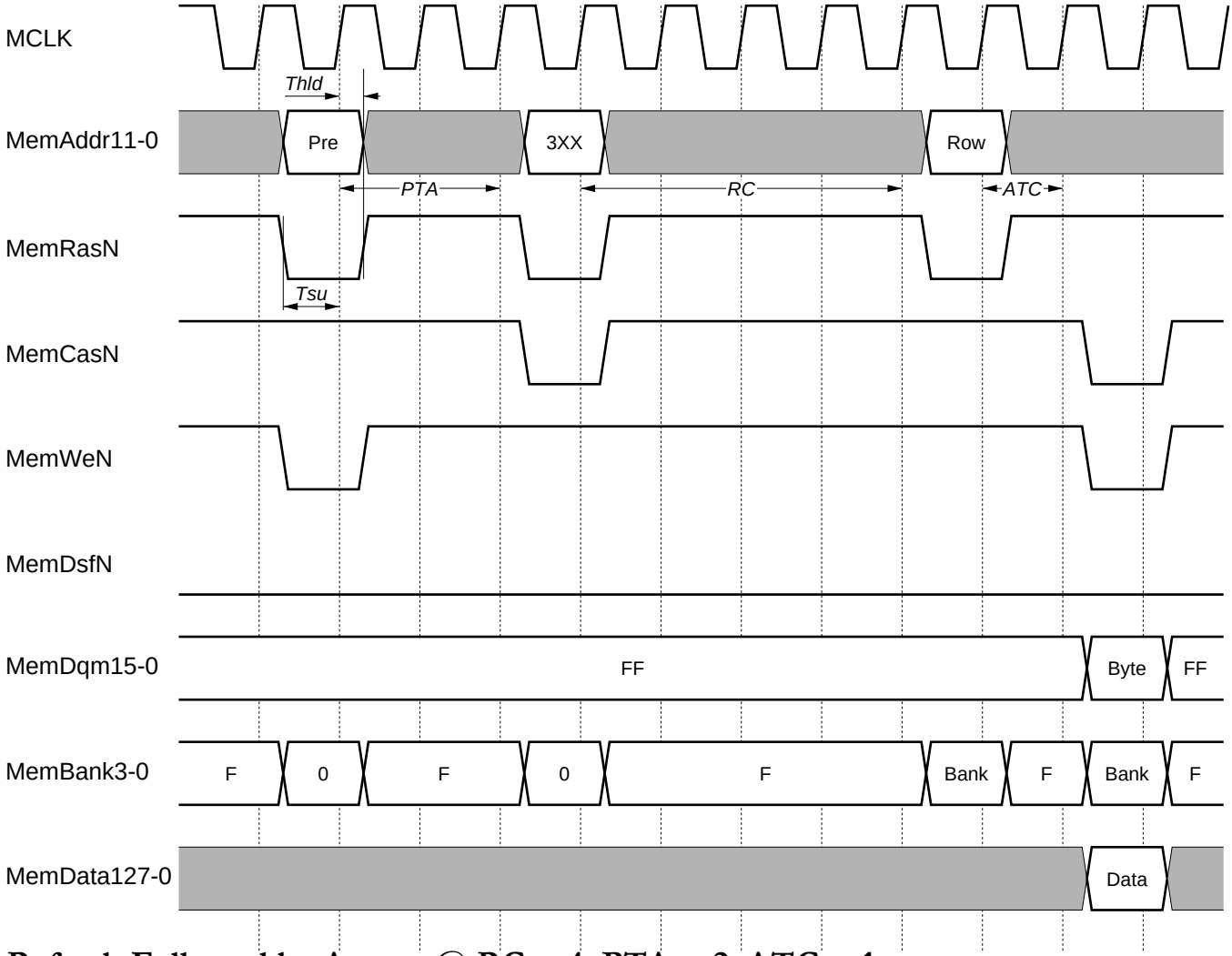
Multiple Reads to Same Bank @ CL = 2, PTA = 2 , ATC = 1



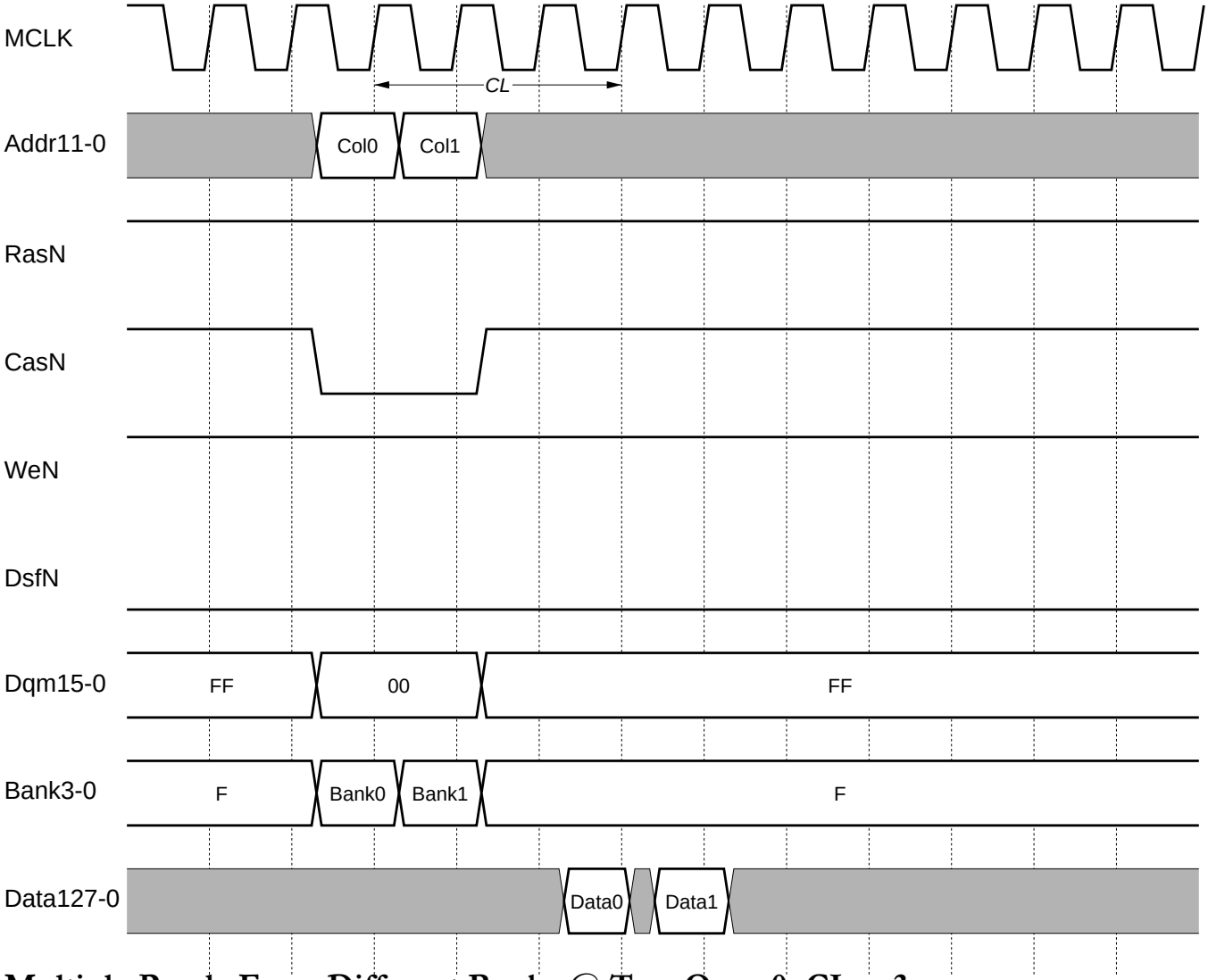
Single Write with Precharge @ PTA = 2, ATC = 1



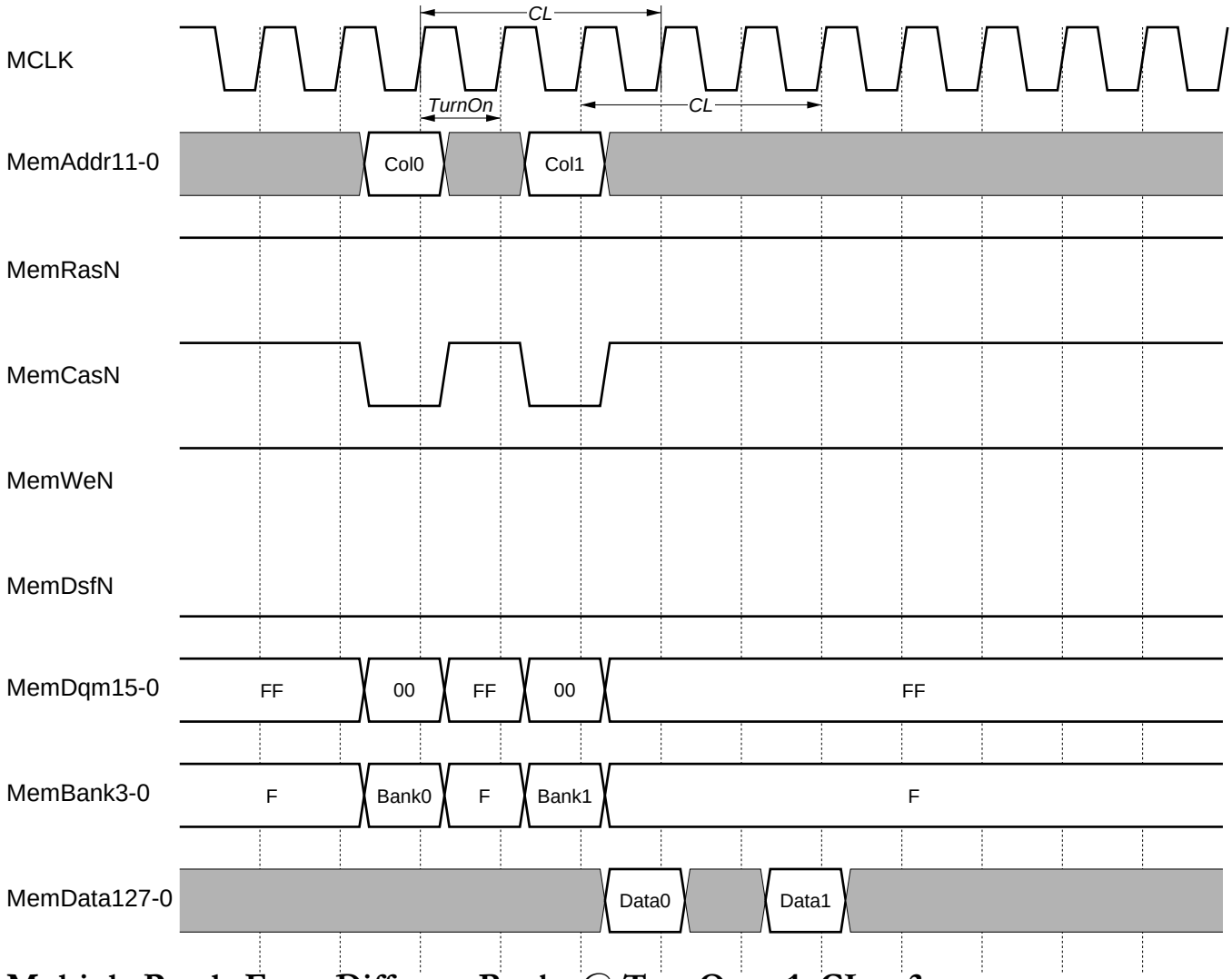
Multiple Writes to Same Bank @ PTA = 2, ATC = 1



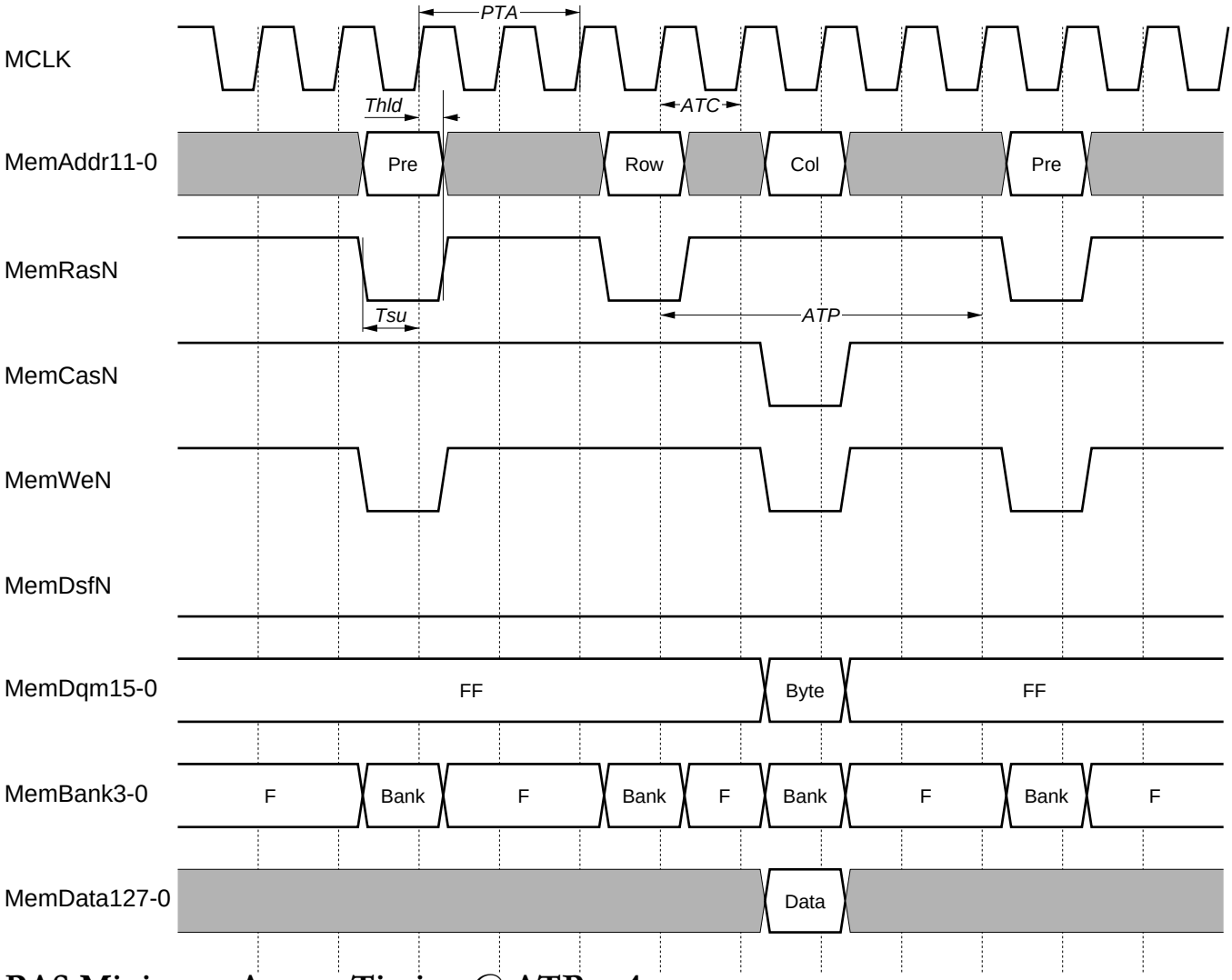
Refresh Followed by Access @ RC = 4, PTA = 2, ATC = 1



Multiple Reads From Different Banks @ TurnOn = 0, CL = 3

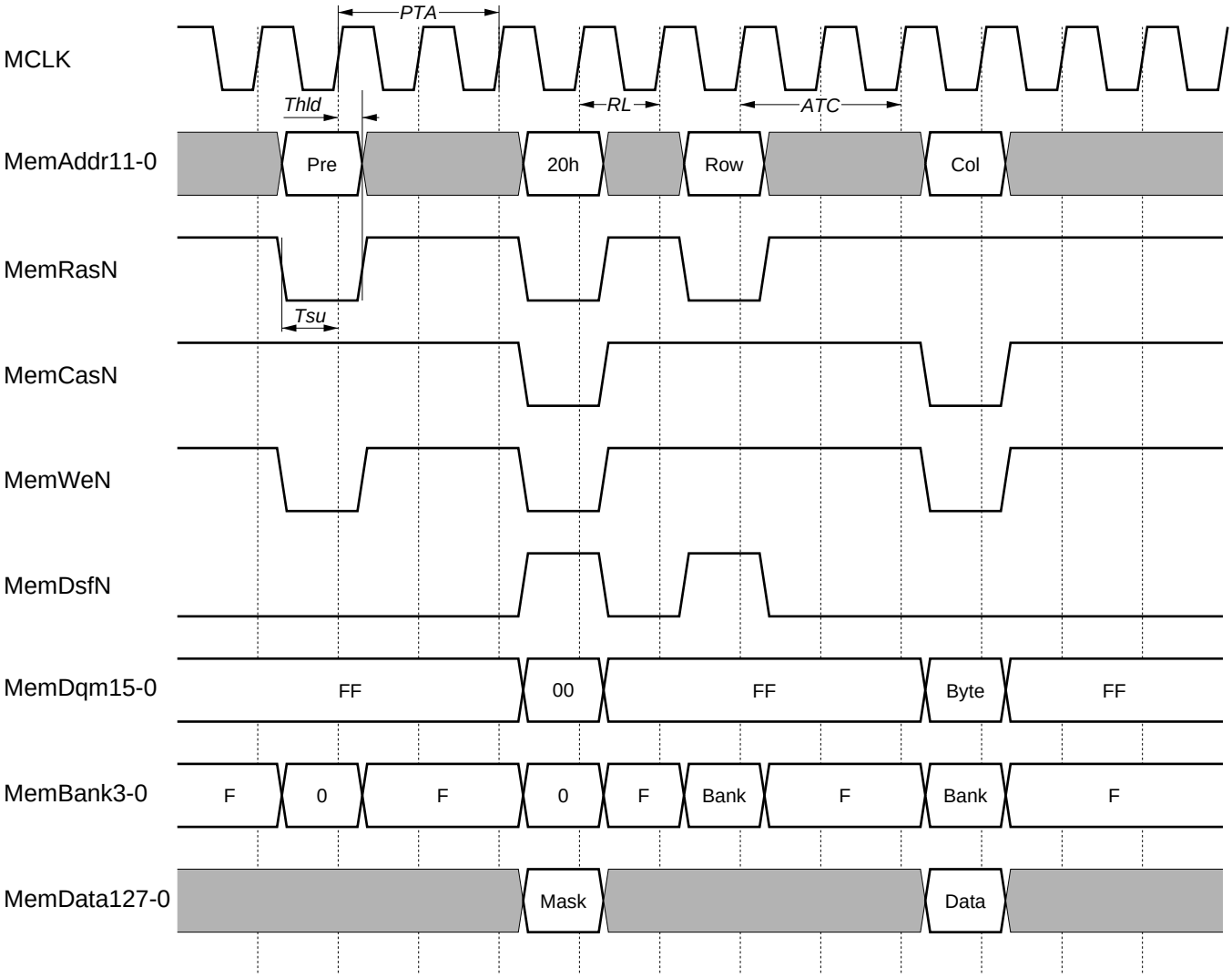


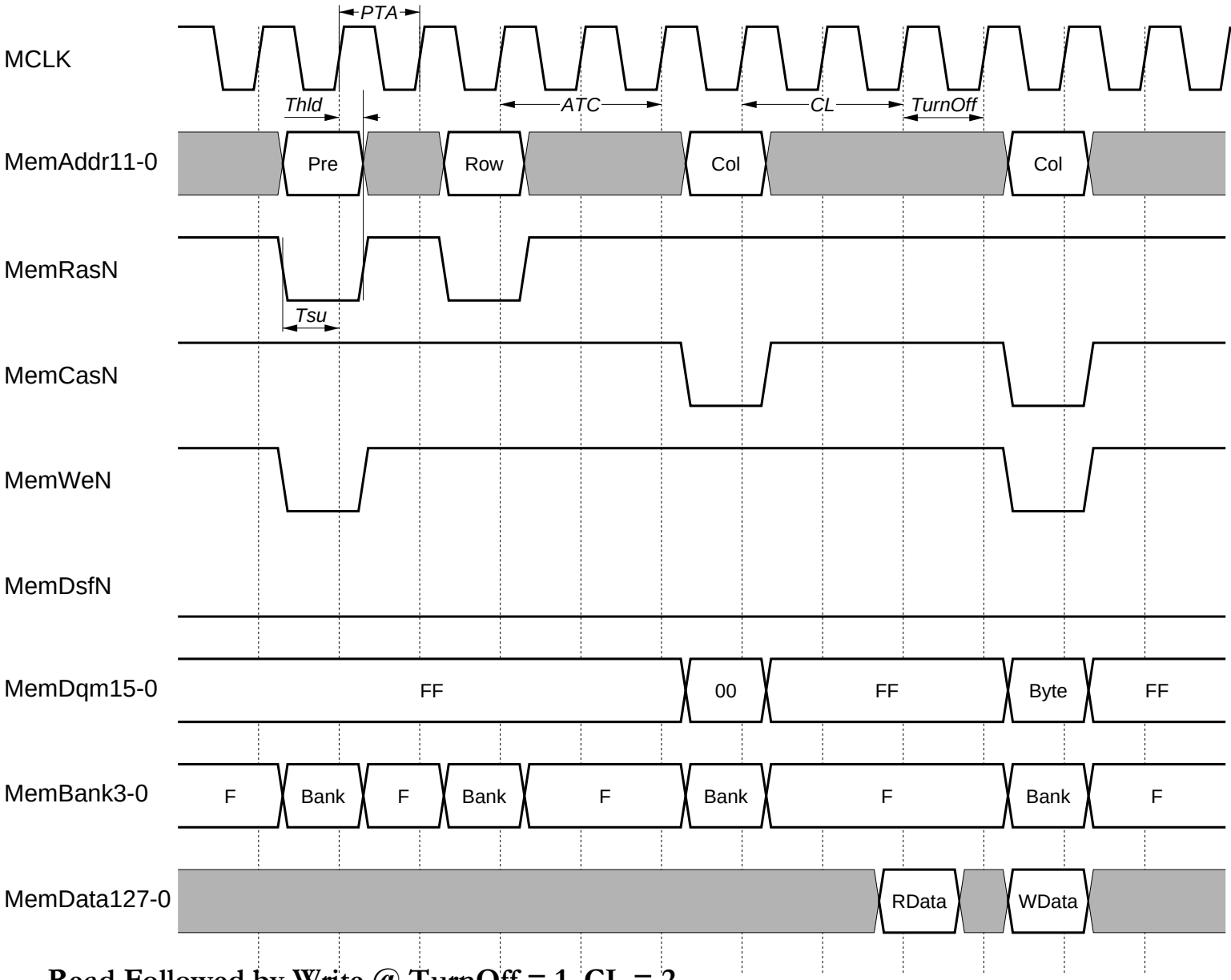
Multiple Reads From Different Banks @ TurnOn = 1, CL = 3



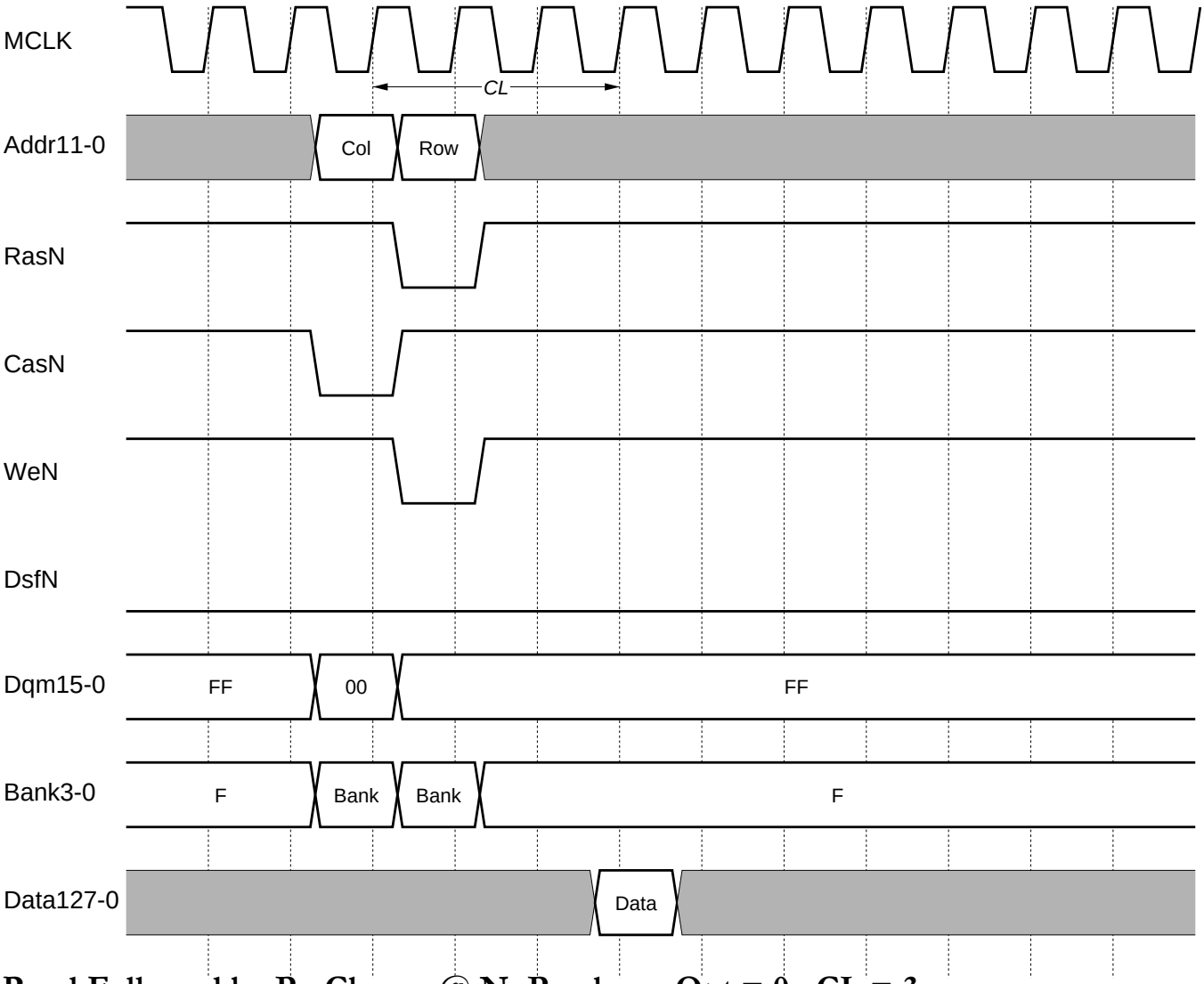
RAS Minimum Access Timing @ ATP = 4

Mask Load Followed by Masked Write @ RL = 1

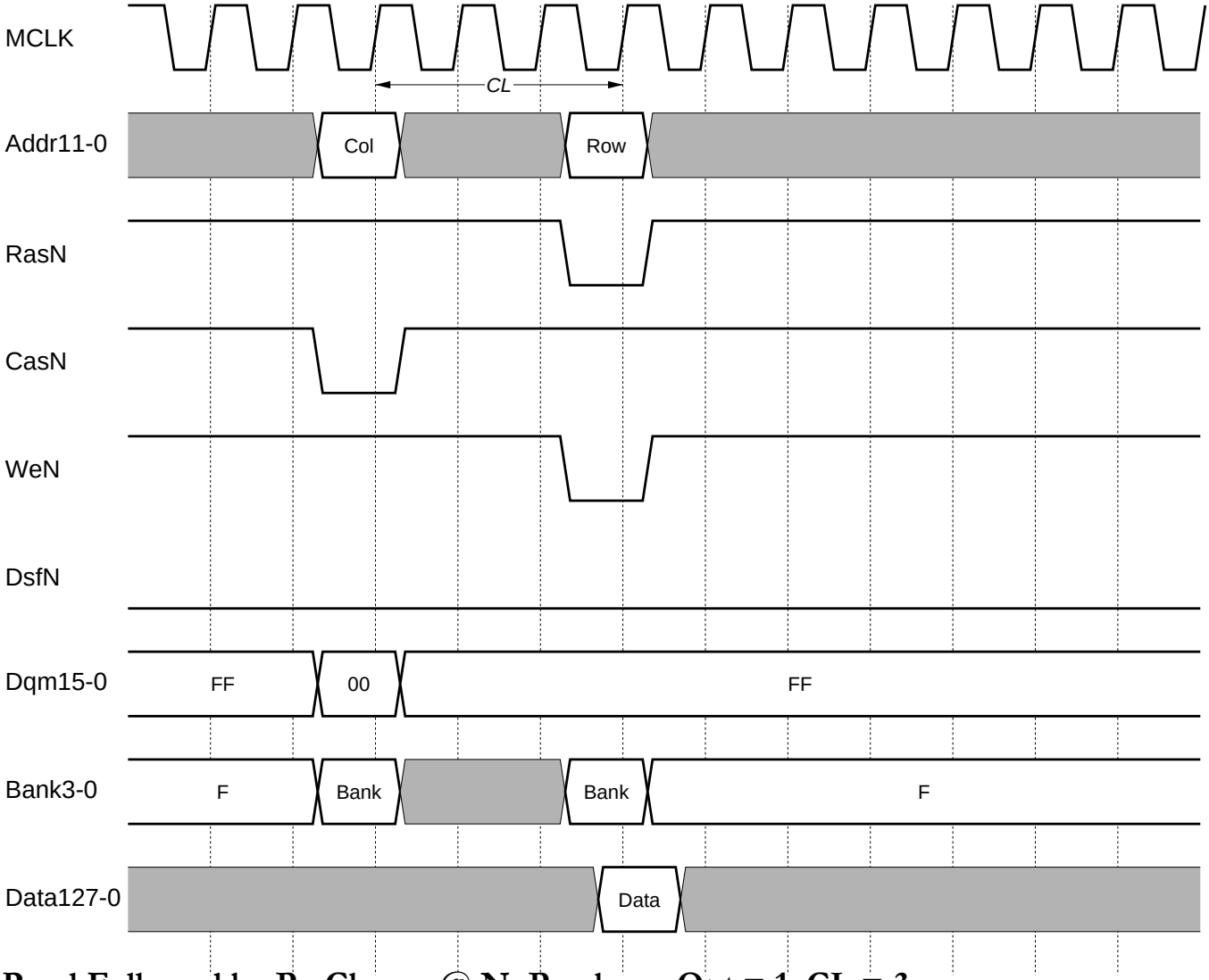




Read Followed by Write @ TurnOff = 1, CL = 2



Read Followed by PreCharge @ NoPrechargeOpt = 0 , CL = 3



Read Followed by PreCharge @ NoPrechargeOpt = 1, CL = 3

10 Reset

Specific signal pins are read on the trailing edge of a reset and the values present, due to pull-ups or pull-downs, are used to initialized bits of particular registers. Most of the sampled values from the I/O pins are read into the **ChipConfig** register - for details refer to volume II. In some cases they do not - e.g. **CfgMaxLat** and **CfgMinGrant** which directly update the hardware registers only. The configuration pins are mapped to real device pins as follows:

Table 10- 1 Reset Signal Pins

Name	Pin	Description
BaseClassZero	VSAData(0)	1 = force PCI Bass Class Code to be zero
VGAEnable	VSAData(1)	1 = internal VGA subsystem present
VGAFixed	VSAData(2)	1 = enable VGA fixed address decoding
RetryDisable	VSAData(3)	1 = disable PCI Retry using "Disconnect-Without-Data"
ShortReset	VSAData(4)	1 = generate short "AReset" pulse (BusReset + 64 clocks)
AGP1XCapable	VSAData(5)	1 = AGP 1XCapable
SBACapable	VSBData(0)	1 = AGP Sideband Addressing Capable
SubsystemFromRom	VSBData(1)	1 = Load subsystem Vendor ID and SubsystemID from ROM . 0 = leave as reset values
AGP2XCapable	VSAData(6)	1 = AGP 2X Capable
AGP4XCapable	VSAData(7)	1 = AGP 4XCapable - this should never be set on a P3, unless 4X drivers are added
IndirectIOEnable	VSBData(2)	1 = Indirect IO accesses using BaseAddress 3 are enabled
WCEnable	VSBData(3)	0 = Upper half of region Zero is byte-swapped 1= Upper half of region Zero flagged internally as write-combined
PrefetchEnable	VSBData(4)	1 = Base Address registers 1 and 2 marked as prefetchable

A hard configuration pin also exists (Table 10-2).

Table 10- 2 Hard Configuration Pin

Name	Pin	Description
PCIClk66	PCIClkSel	0 = up to 33MHz 1 = 66 MHz

Note: During Power-up resets the external frequency reference must be powered at the same time as the Permedia4 or before it, to ensure normal operation.

11 Thermal

The maximum junction temperature must be kept below Tj(max)and this can only be guaranteed by proper analysis of the operating environment and the thermal path between the die and the air surrounding it.

11.1 Device Characteristics

These are fixed characteristics of the device and are independent of the operating environment or the characteristics of any heatsink:-

(Eq: 11-1)

Maximum Junction Temperature	$T_{j(max)}$	= 125 °C.
Maximum Power Dissipation	Pd(max)	= 6.7 Watts
Nominal memory clock frequency	f_{MClk}	= 125 MHz
Nominal core clock frequency	f_{KClk}	= 125 MHz
Junction to case resistance	θ_{jt}	= 5.5 °C/Watt

11.2 Thermal Model

The formula used to calculate the junction temperature (Tj) is:

(Eq: 11-2)

$$Tj = Ta + Pd(\theta_{jt} + \theta_{cs} + \theta_{sa})$$
$$= Ta + Pd\theta_{ja}$$

Where:

(Eq: 11-3)

Tj = Junction temperature (°C)
Ta = Ambient temperature (°C)
Pd = Power dissipation (Watts)
θ_{jt} = Junction to top of case thermal resistance (°C/Watt)
θ_{cs} = Case to Heatsink thermal resistance (°C/Watt)
θ_{sa} = Heatsink to Air thermal resistance (°C/Watt)
θ_{ja} = Total Junction to Air thermal resistance (°C/Watt)

11.3 Cooling

Permedia4 should be operated with an attached heatsink or fan.

11.4 Operation with Heatsink

With a heatsink attached to the device the junction temperature will depend on qcs and qsa where qcs is the thermal resistance of the join between the heatsink and the case and qsa is the thermal resistance of the heatsink, which will be a function of system airflow. An ambient temperature of 40° C is assumed.

(Eq: 11-4)

Heatsink to air thermal resistance	θ_{sa}		
Maximum Junction Temperature	Tj(max)	=	125°C
Ambient Temperature	Ta	=	40°C
Maximum Power Dissipation	Pd(max)	=	6.7 Watts
Junction to case resistance	θ_{jt}	=	5.5°C/Watt
Heatsink to case resistance (EG 7655 epoxy - see below)	θ_{cs}	=	1.0°C/Watt

then:

$\theta_{sa} \leq [(125 - 40)/6.7] - 5.5 - 1.0$
≤ 6.2°C/Watt.

In this example a heatsink must be chosen which has a thermal resistance figure of no greater than 6.2°C/Watt at an airflow matching the expected airflow in the system.

11.4.1 Heatsink Attachment

The following method has been approved for the purpose of attaching a heatsink directly onto the surface of the PBGA package:

Thermally conductive epoxy using either Loctite Output 315 with Loctite 7386 or type EG 7655 from A.I. Technology Inc. The thickness of the epoxy layer should be between 0.05mm and 0.15mm with 95% coverage of the contact area.

Typical achievable θcs using this method is 1.0 ° C/Watt

12 Electrical

12.1 Absolute Maximum Ratings

Junction Temperature	**125°C**
Storage Temperature	-65°C to 150°C
VCC2.5 DC Supply Voltage	2.8V
VCC3.3 DC Supply Voltage	3.8V
I/O Pin Voltage with respect to GND	-0.5V to VCC3.3 + 0.5V

12.2 DC Specifications

Symbol	**Parameter**	**Min**	**Max**	**Unit**
VCC3.3	Supply Voltage	3.15	3.45	V
VCC2.5	Supply Voltage	2.25	2.75	V
LPIN	Pin Inductance		10 (sig); 8 (pwr)	nH
ICC (3V)	Power Supply Current		1	A
ICC (2.5V)	Power Supply Current		1.4	A

12.2.1 PCI Signal DC Specifications

Symbol	**Parameter**	**Min**	**Max**	**Unit**
V_{PIL}	Input Low Voltage		0.8	V
V^{PIH}	Input High Voltage	2.0		V
V_{POL}	Output Low Voltage		0.5	V
V_{POH}	Output High Voltage	2.4		V
I_{PIL}	Input Low Current		-20	uA
I_{PIH}	Input High Current		+20	uA
C_{PIN}	Input Capacitance		10	pF
C_{CLK}	PCI Clock Input Capacitance		10	pF
C_{IDSEL}	PCI Idsel Input Capacitance		8	pF

12.2.2 Non-PCI Signal DC Specifications

Symbol	**Parameter**	**Min**	**Max**	**Unit**
V_{IL}	Input Low Voltage		0.8	V
V_{IH}	Input High Voltage	2.0		V
V_{OL}	Output Low Voltage		0.5	V
V_{OH}	Output High Voltage	2.4		V
I_{IL}	Input Low Current		+10	uA

I_{IH}	Input High Current		-10	uA
I_{IHPD}	Pulldown Input High Current		250	uA
I_{ILPU}	Pullup Input Low Current		250	uA
C_{IN}	Input Capacitance		10	pF

12.3 AC Specifications

Pin Name	Capacitive Load
MADD[9:0]., MCAS[1:0], MDSF[1:0], MRAS[1:0], MWE[1:0].	80pF
PCIAD[31:0], PCICBEN[3:0], PCIPar, PCIFrameN,PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, PCIReqN, PCIGntN, PCIIntAN ,AGPPipeN, AGPRbfN, AGPSBA[7:0],	50pF in PCI 33 system 10pF in AGP system
MBANK[3:0], MBYTE[7:0], MEMCKE, MEMCKOUT[1:0], VidDDCClk, VidDDCData, VidRightEye, VidHSYNC, VidVSYNC,VSAResetN,VSBResetN,RenderSyncN	50pF
MDAT[63:0].	40pF
ROMSelectN, ROMWEN, SBClk, SBData, VSAData[7:0], VSBData[7:0], VSCtl[7:0], VSGPChipSelectN, VSGPDataAckN, VSGPDataStrobeN, VSGPReadWriteN.	30pF

12.3.1 Clock Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{PCyc}	PCIClk Cycle Time	15	-	ns	
T_{PHigh}	PCIClk High Time	-	-	ns	
T_{SLow}	PCIClk Low Time	-	-	ns	
T_{MCyc}	MClkin Cycle Time	8	-	ns	
T_{MHigh}	MClkin High Time	-	-	ns	
T_{MLow}	MClkin Low Time	-	-	ns	
T_{SCyc}	SClkin Cycle Time	15	-	ns	
T_{SHigh}	SClkin High Time	6	-	ns	
T_{SLow}	SClkin Low Time	6	-	ns	
T_{DCyc}	DClk Cycle Time	4	-	ns	
T_{DHigh}	DClk High Time	-	-	ns	
T_{DLow}	DClk Low Time	-	-	ns	

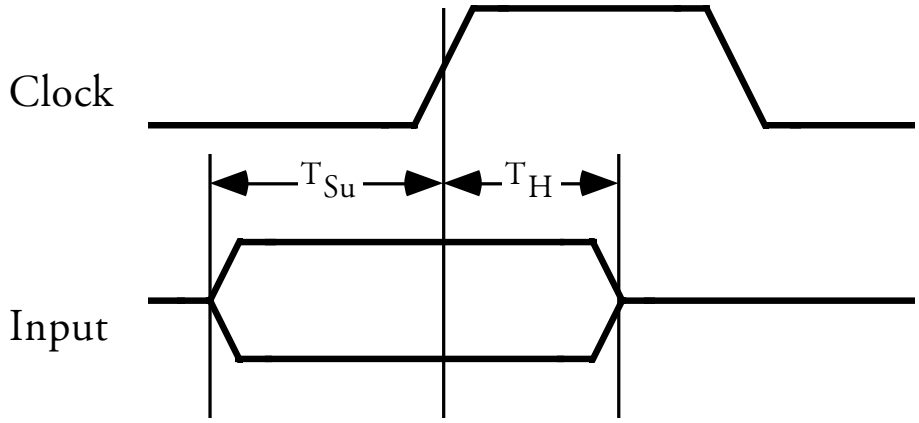


Figure 12.1 Input Timing Parameters

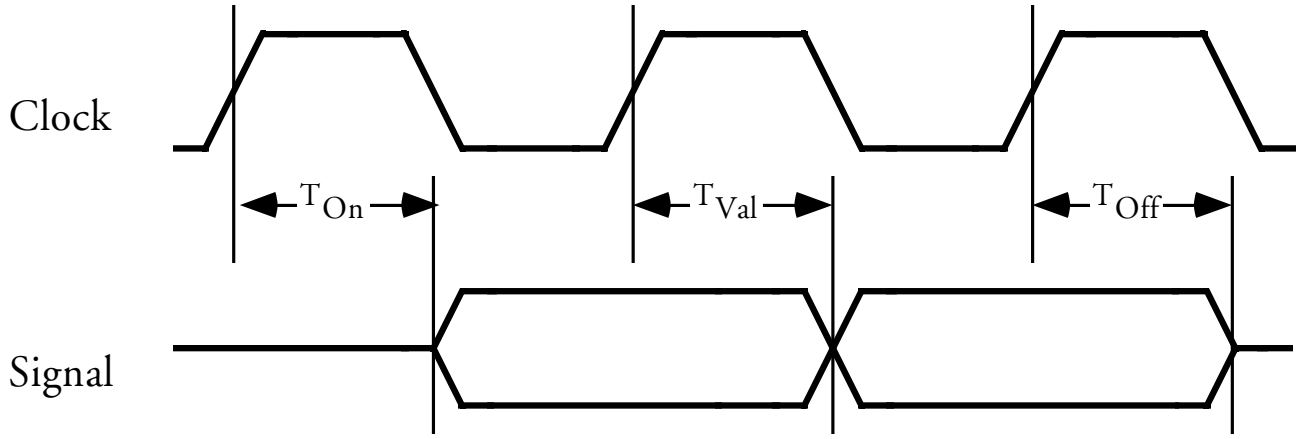


Figure 12.2 Output Timing Parameters

12.3.2 PCI Clock Referenced Input Timing

Parameter	T_{Su} Min	T_H Min	Units	Notes
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, AGPSt0-2	5	0	ns	
PCIGntN	5	0	ns	
PCIRstN	7	0	ns	1

Note 1: PCIRstN is resynchronised internally. The timings given, when met, ensure that the reset is detected in the current cycle.

12.3.3 PCI -Referenced Output Timing

	T_{Val}		T_{On}		T_{Off}			
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN	2	11	2	11	2	11	ns	
PCIReqN	2	12					ns	
PCIIntAN	2	11					ns	1

Note 1: Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

12.3.4 AGP Referenced Output Timing

	T_{Val}		T_{On}		T_{Off}			
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN	1.5	6	1.5	6	1.0	14	ns	
PCIReqN	1.5	6					ns	
PCIIntAN	1.5	6					ns	1

Note 1: Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

12.3.5 MEMClKOUT Referenced Input Timing

All timings below are with respect to MEMClKOUT, which is a delayed version of MClk.

Parameter	**TSu Min**	**TH Min**	**Units**	**Notes**
MDAT[63:0]	1	3	ns	

12.3.6 MEMClKOUT Referenced Output Timing

All timings below are with respect to MEMClKOUT, which is a delayed version of MClk.

	T_{Val}		T_{On}		T_{Off}			
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
All memory control, data and address lines[4]		8.5					ns	

[4] Ton and Toff are not applicable.

13

Errata and Alerts

Alerts are part of 3Dlabs commitment to providing comprehensive and useful information about chipset products. Alerts describe issues arising when the chip is used outside normal operating parameters and may be of interest to driver programmers.

13.1 ALERT001 - Control DMA/ Programmed IO Interaction Caution

13.1.1 Problem

The input fifo is not designed to cope with fast switching between Control DMA and writes to the input fifo. Normally, either one mechanism or the other (but not both) should be used. This advisory does not apply to mixing fifo/register space acesses and Hostin DMA.

13.1.2 Software Workaround

Where it is necessary to combine both write methods either (a) use HostIn DMA, or (b) ensure that the input fifo is completely empty after writing to the fifo/register space and before starting a new DMA transfer . The input FIFO must report 128 spaces available. Clamping to fewer than 128 spaces will produce unpredictable results.

13.2 ALERT002 - Texture Lockup when Cache Combining above 100MHz

13.2.1 Problem

When CombineCaches is enabled for texturing at frequencies above 100MHz, lockups may occur. When this happens check to see if the *CombineCaches* bit is set by reading back the **TextureFilterMode** register (refer to the *Permedia4 Reference Guide*).

13.2.2 Software Workaround

Since the Primary Cache Manager is the only texture read function which uses the *CombineCaches* bit, the workaround is to ensure that drivers do not set the *CombineCaches* bit in the **TextureReadMode0/1** and **TextureFilterMode** registers if clock speeds in excess of 100MHz are anticipated.

13.3 PEREN001 - Video Streams

13.3.1 Problem

Operation of input and output video streams is incorrect. Modes 1, 2, 3 and 4 of the VSConfiguration register mode field do not function correctly and should not be used. Access to the ROM (mode 0) and the flat panel display (mode 6) do function correctly and can be used.

13.3.2 Software Workaround

None

13.4 PEREN002 - YUV planar to packed through bypass

13.4.1 Problem

Data in the YUV planar format (the internal format of MPEG2 data) cannot be converted to packed YUV (the format used for processing) while being written to the framebuffer through the bypass.

13.4.2 Software Workaround

Planar data should be converted to packed before being written to the framebuffer. DirectX normally does the conversion so this errata should have no effect for DirectX systems.

13.5 PEREN003 - Memory frequency dependency

13.5.1 Problem

The memory and bypass clocks should not be set to run faster than the graphics processor clock. The graphics core may not function correctly if the frequency of the memory clock is greater than the frequency of the graphics processor clock. The memory clock is controlled by the MClkControl register, the bypass clock by the PclkControl register, and the graphics processor clock by KClkControl and associated PLL registers.

13.5.2 Software Workaround

Under normal conditions, the memory clock should be tied to the graphics processor clock. If slow speed memories are used, the memory clock may be run from, for example, an external clock with a frequency lower than the graphics processor clock. Care should be taken when using the power saving mode of the graphics processor clock as it may result in it having a lower frequency than the memory clock.

13.6 PEREN007 - Constant color 8 bpp span rendering

13.6.1 Problem

Constant color span operations on 8bpp framebuffers do not work correctly and omit some pixels.

13.6.2 Software Workaround

The normal workaround is to render a span aligned rectangle and set the UserScissor to clip it back to the desired size. In the places where this is not feasible (e.g. a polygon can change its alignment with every scanline), then the rendering is done with variable colour spans rather than constant colour spans as these do not suffer from the bug.

13.7 PEREN008 - Write DMA frequency dependency

13.7.1 Problem

The bypass write DMA controller is used to transfer data from the framebuffer to system memory. If the memory clock is operating at a higher frequency than the PCI clock, the DMA may not operate correctly. As the highest PCI clock is 66MHz, it is normal for the memory clock to be faster, so this DMA controller should not be used.

13.7.2 Software Workaround

Bypass write DMA should not be used. Instead, use the CPU to read from the framebuffer, or use the graphics processor to DMA data.

13.8 PEREN009 - GPOut write DMA

13.8.1 Problem

The GPOutDMA address register in region zero does not return the next DMA Address to be issued to the DMA arbiter when read. The PCIFeedbackCount register does not return the number of DWORDs transferred in the current DMA. This means that operations such as rectangular write DMA do not work correctly.

13.8.2 Software Workaround

Legacy output DMA, as used by PERMEDIA 2 drivers, should be used instead.

13.9 PEREN0015 - Render2D Register

13.9.1 Problem

The Render2D command does not always render the last pixel(s). This occurs under the following conditions:

- the Render2D command has the Operation field set to PatchOrderRendering,
- the rectangle width is less than the patch width in pixels (i.e. < 64 for 32 bpp, < 128 for 16 bpp or < 256 for 8 bpp)

- and the rectangle does not cross a patch boundary in X

The effect is that the last pixel(s) are not flushed out to memory. They will be by any subsequent rendering, but if no more rendering is done (for example while waiting for user input) then one or more pixels will not be visible on the screen.

13.9.2 Software Workaround

The simplest solution is to follow any Render2D command which might fall into this category with a ContinueNewSub (0) command which will do nothing, but as a side effect cause any pending pixels to be flushed out from the internal registers. If this proves to be too much of a performance burden then it is possible to do the flush only on an interrupt driven basis such as on a frame blank interrupt. This will flush the residual pixels 60 or more times per second, which is frequent enough to make the missing pixels invisible.

13.10 PEREN0016 - Invalidate Texture Cache

13.10.1 Problem

After sending an Invalidate Cache command, the texturing mapping hardware must wait for this to be fully processed before continuing with command processing. Failing to do so can result in the graphics processor locking up.

13.10.2 Software Workaround

One workaround is to send the Invalidate Cache command and then load a data value of 0 into the FogModeOr and TextureReadMode0Or registers. An alternative is to send WaitForCompletion (0) after the Invalidate Cache command.

PEREN0017 - Horizontal Display Resolution

1.1.1 Problem

The video unit imposes a 2048 pixel width constraint. Beyond this resolution the display is wrapped.

1.1.2 Software Workaround

None.

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