Permedia4®

Reference Guide - Volume I

DRAFT ONLY

PROPRIETARY AND CONFIDENTIAL INFORMATION

3D*labs*®

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Issue 4

Proprietary Notice

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Change History

Document	Issue	Date	Change
160.2.1	1	19 April 1999	Creation
160.2.1	2	16 June 1999	FBSourceData, FBData added; minor corrections
160.2.1	3	15 September 1999	New Package information, footer typography
160.2.1	4	20 Septmber 1999	Corrected offsets in PCI Configuration map

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1 Functional Overview

1.1 Introduction

Permedia4 is a high performance PCI/AGP graphics processor that balances high quality 3D polygon and textured graphics acceleration, windows acceleration and state-of-the-art MPEG1/MPEG2 playback with a fast integrated SVGA core, integrated RAMDAC and video ports.

Permedia4 offers significant advances over earlier members of the Permedia product family in both raw performance and functionality. New or improved functionality includes:

Permedia4 Enhancement Summary	
Memory Interface and Core	
Memory bus width (bits)	128
Core clock speed (MHz) – Provisional	125
Max. memory (MB)	32
AGP with sideband and pipelining	2x/4x dual protocol
Write-combined command FIFO	✔
Virtual texture management, logical texture addressing	✔
2k on-chip texture cache	✔
SGRAM/SDRAM incl. SGRAM block write	✔
3D Features	
Max. Z-buffer depth (bits)	32
Non-Linear 16 or 24-bit Z-buffer (Direct3D and OpenGL)	✔
W-Buffer Emulation with Non-Linear Z-buffer (Direct3D)	✔
Texture read units	2
Texture compositing units	✓
Single-pass dual texturing	✔
Single-pass bump mapping with surface texture	✔
Hardware texture paging	✔
Per polygon MIP mapping (single pass)	Tri-linear
Destination Alpha	✔

Permedia4 Enhancement Summary	
All OpenGL and Direct3D blend and depth modes	✔
Native support for DIRECT3D vertex formats	✔
OpenGL	1.2
Fog table	✔
Full hardware edge anti-aliasing	✔
Bilinear and trilinear filtering, emulated anisotropic filtering	✔
Specular and diffuse lighting support	✔
2D Features	
Logic Ops	✔
Single-register tag index setup for 2d primitives	✔
Font caching	✔
DMA Packing/unpacking on output/input	✔
32x32 stipple pattern	✔
Run-length encode/decode	✔
Buffer Formats	
Unified framebuffer/localbuffer	✔
Flexible GID, stencil and depth formats	✔
Stencil planes	8
GID bits	4
Simultaneoous framebuffer access	4
Any width framebuffer/localbuffer/texture	✔
2d buffer tiling	✔
Video/DVD	
Hardware video overlay	✔
Hardware scaling and filtering	✔
MPEG Motion compensation	✔
Memory to DVD accelerator DMA	✔
Flat panel LCD support	✔
Integrated 270MHz RAMDAC	✔
LUT Accuracy	8
Video overlay blend	2 bit
Video overlay with stretch and bilinear filtering	✔
Software	
SoftImage Compliant	✔

Permedia4 Enhancement Summary	
Power Management	
DPMS for monitors	✔
Memory array power-down	✔
Dynamic clock control	✔

Table 1-1 Permedia4 Enhancement Summary

1.2 P3/P4 Differences

The Permedia4 chipset removes a number of constraints found in the Permedia3, including those shown below. For more information see *Permedia3 Errata*:

Topic	P3	P4
HostIn DMA (P3 Errata 4)	DMACount=0 incorrect	Erratum cleared
	DMAContinue Double buffering incorrect	Erratum cleared
	Spurious DMA interrupts	Erratum cleared
Video Overlay (P3 Erratum 5)	Line length cannot be 4n-1	Erratum cleared
Video overlay (P3 Erratum 6)	Bob de-interlace incorrect	Erratum cleared
	1-pixel windows not supported	P4 supports single-pixel width wondows
Framebuffer Write (Erratum 7)	8bpp and 32bpp Constant Color Spans supported in software	SGRAM Block fills for 32bpp spans fully supported in hardware
Video Control (Erratum 13)	Line doubling with patching	Erratum cleared
RAMDAC Pan (Erratum 14)	Pan to 32 bit boundary incorrect	Erratum cleared
RAMDAC Cursor (Erratum 15)	Cannot disable	Erratum cleared
PCI Version	2.1	2.2
Dual AGP voltage	3.3VDC AGP 2X protocol	3.3VDC and 1.5VDC drivers (dual AGP2X and AGP4X protocol)
Direct access to DIRECT3D Native Data Structures without host intervention	Software support	Hardware backface cull, texture coordinate processing, texture wrap, per poly MIPmap and Scale by Q supported

1.3 Functional Blocks

The major functional blocks are shown in Figure 1-1.

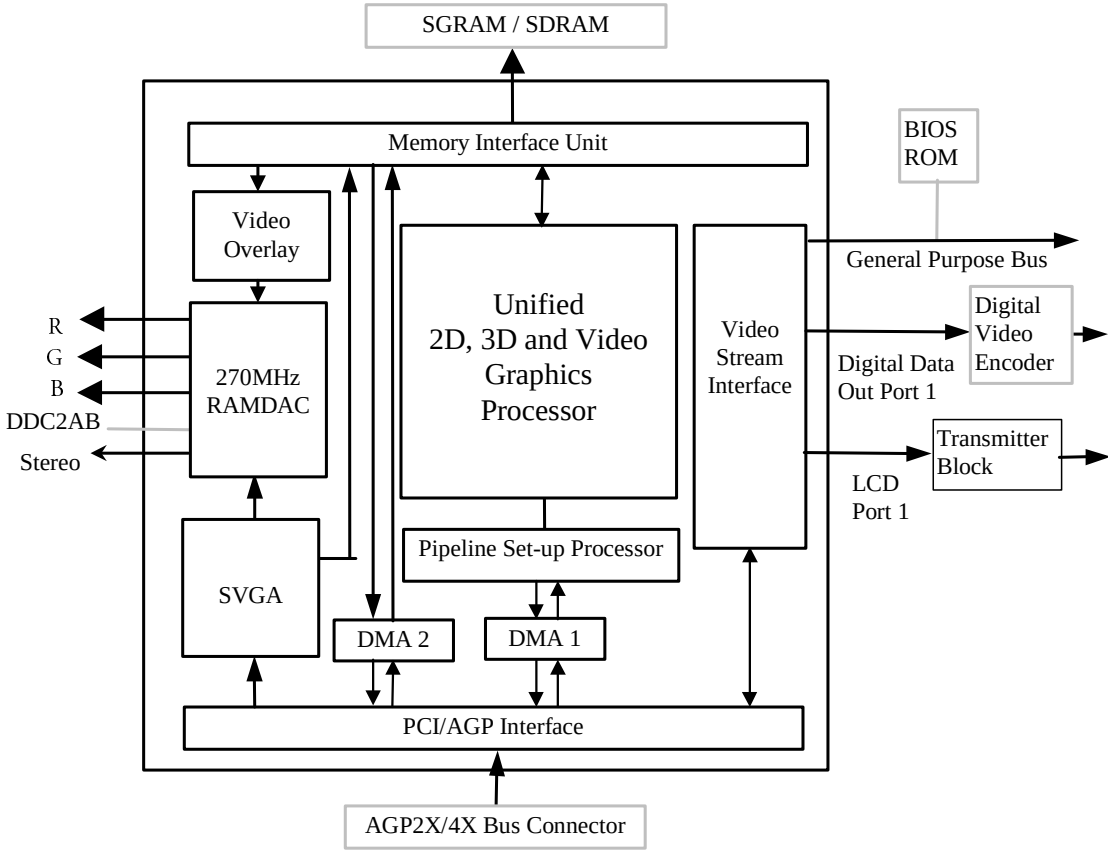

Figure 1-1 Chip Level Block Diagram

1.4 AGP/PCI Interface

The PCI interface conforms to the PCI Local Bus standard Revision 2.2. Permedia4 is a PCI Local Bus Target, a PCI Local Bus Read Master, and a PCILocal Bus Write Master. It is also an AGP read master with support for pipelined reads and sideband addressing.

The PCI interface has an input FIFO for passing data to the Graphics Core, and an output FIFO for buffering up data to be read from the Graphics Core. The input FIFO is 256 words deep, the output FIFO is 8 words deep. A DMA controller is provided in the PCI interface to allow Permedia4 to read data directly into the Graphics Core input FIFO or directly out of the output FIFO.

AGP 4X is Intel's high performance, component level interconnect targeted at 3D display applications, which uses a 66MHz PCI specification as an operation baseline and provides significant performance extensions to the PCI specification.

The specification for Permedia4's AGP implementation is:

- 266 MHz transfer rate
- DMA and execute mode support
- Sideband addressing

Implementing these features enables Permedia4 to achieve better than 1 GByte per second bandwidth from the host for instructions, textures, video data (limited by the host system throughput).

The add-in slot defined for AGP uses a connector body which is not compatible with the PCI connector. Boards designed for use in an AGP slot are not mechanically interchangeable with PCI boards.

Permedia4 is also still fully compliant with the AGP2X standard, including support for both 3.3VDC and 1.5VDC drivers.

1.4.1 Unified 2D/3D/Video Integrated Graphics Processor

The graphics core in PERMEDIA4 accelerates the key operations for 3D and 2D applications. For further information on the functionality of the graphics processor (GP), refer to chapter 5, Graphics Registers, in volume 2.

1.4.2 Memory Interface

The local memory is used to store color, depth, stencil, and texture data. For more information on the different data types and usage refer to Chapter 9 - Memory System.

The memory is organized as 1 to 4 blocks (blocks 0-3) of SGRAM or SDRAM. The memory interface is 128 bits wide with control lines for 4 blocks of memories (0-3). Block zero must always be fitted as the SVGA uses this area for local storage. Any other combination of banks may be fitted, but for contiguous memory banks should be added from 1 to 3.

Permedia4 will make use of special SGRAM features including block fill and write-per-bit masking. SDRAM may be used in place of SGRAM if it is identical to SGRAM except for missing block write and write per bit masks.

1.4.3 SVGA

The on-chip SVGA unit is register level compatible with standard VGA devices and requires no software emulation. It natively supports all standard VGA modes and certain VESA VBE extended modes.

The following standard VESA VBE extended video modes are supported - those not supportable by the SVGA unit may be supported using the Graphics Processor:

Table 1- 2 VESA VBE Graphics Modes

Mode (hex)	Pixels	Colors	Window-ed	Lin-ear	Support-able in SVGA	Support-able in GP
0x100	640x400	256	✓	✓	✓	✓
0x101	640x480	256	✓	✓	✓	✓
0x102	800x600	16	✓	✕	✓	✕
0x103	800x600	256	✓	✓	✕	✓
0x104	1024x768	16	✓	✕	✓	✕
0x105	1024x768	256	✓	✓	✕	✓
0x106	1280x1024	16	✓	✕	✓	✕
0x107	1280x1024	256	✓	✓	✕	✓
0x109	320x200	32K (5:5:5:1)	✓	✓	✕	✓
0x10D	320x200	64K (5:6:5)	✓	✓	✕	✓
0x10F	320x200	16.8M (8:8:8)	✓	✓	✕	✓
0x110	640x480	32K (5:5:5:1)	✓	✓	✕	✓
0x111	640x480	64K (5:6:5)	✓	✓	✕	✓
0x112	640x480	16.8M (8:8:8)	✓	✓	✕	✓
0x113	800x600	32K (5:5:5:1)	✓	✓	✕	✓
0x114	800x600	64K (5:6:5)	✓	✓	✕	✓
0x115	800x600	16.8M (8:8:8)	✓	✓	✕	✓
0x116	1024x768	32K (5:5:5:1)	✓	✓	✕	✓
0x117	1024x768	64K (5:6:5)	✓	✓	✕	✓
0x118	1024x768	16.8M (8:8:8)	✓	✓	✕	✓
0x119	1280x1024	32K (5:5:5:1)	✓	✓	✕	✓
0x11A	1280x1024	64K (5:6:5)	✓	✓	✕	✓
0x11B	1280x1024	16.8M (8:8:8)	✓	✓	✕	✓

The following VESA VBE text modes are supportable in the SVGA:

Table 1- 3 VESA VBE Text Modes

Mode (hex)	Characters (col/row)
0x108	80x60
0x109	132x25
0x10A	132x43
0x10B	132x50
0x10C	132x60

Permedia4 allows VESA bankswitching to be done through the bypass to enable additional VESA mode support. ModeX is also supported.

1.4.4 RAMDAC

Permedia4 incorporates a high performance 270MHz RAMDAC.

Its characteristics include a high resolution 270 MHz 128-bit RAMDAC. It supports screen resolutions up to 1600x1200 with refresh rates of 96Hz or 1920x1080 with refresh rates of 90Hz. It supports packed pixel formats, with color depths of 8, 16, and 32 bits per pixel. It has dot-clock phase locked loops (PLLs) and triple 8-bit D/A converters. The RAMDAC contains a 64x64x2 bit cursor array to support a 2, 4, or 16 color hardware cursor with cursor shapes cache.

1.4.5 Video Overlay

The video overlay is used to display incoming video data on screen. the overlay selection is based on a transparent color, the overlay key, which can be any RGB color or alpha value. Optionally, the overlay can be blended with the main image by using a 2-bit blend factor. A filter process supports zooming and shrinking at any rate. It combines four pixels into one by using bilinear filtering to achieve best results. Furthermore the filtered output is optionally converted from YUV to RGB color space format.

1.4.6 DMA1..DMA3

1.4.6.1 DMA1 Controller – System to Graphics Core and Graphics Core to System

- Autonomous - set-up/fetch parallelism
- No wait state - maximum transfer rate
- Programmable block size - large DMA buffers
- Separate DMA controllers for upload and download can run concurrently

1.4.6.2 DMA2 Controller - System to Memory and Memory to System

- Fast texture/image uploads and downloads
- Separate DMA controllers for upload and download can run concurrently
- DMA Controller supports scatter/gather
- Fast software MPEG2 download, fast frame capture

1.4.6.3 Interrupt Controller

- End-of-DMA - allows DMA chaining
- VSYNC - efficient double buffering
- Scanline - special effects
- Texture invalid
- Bypass DMA interrupt
- I2C start condition - alert host to start of I2C transfer
- Sync - indicates graphics core is idle
- Error - e.g. writing to a full FIFO

1.4.7 Video Streaming

Permedia4 supports digital video output. The 24-bit streamed output is designed to work with common PAL/NTSC encoders or flat panel controllers.

1.4.8 ROM support

Permedia4 supports a Flash ROM. This ROM may store code needed for device-specific initialization and the SVGA BIOS.

2

Address Maps and Regions

2.1 PCI Configuration Region

The PCI Configuration Region provides information that satisfies the needs of current and anticipated system configuration mechanisms.

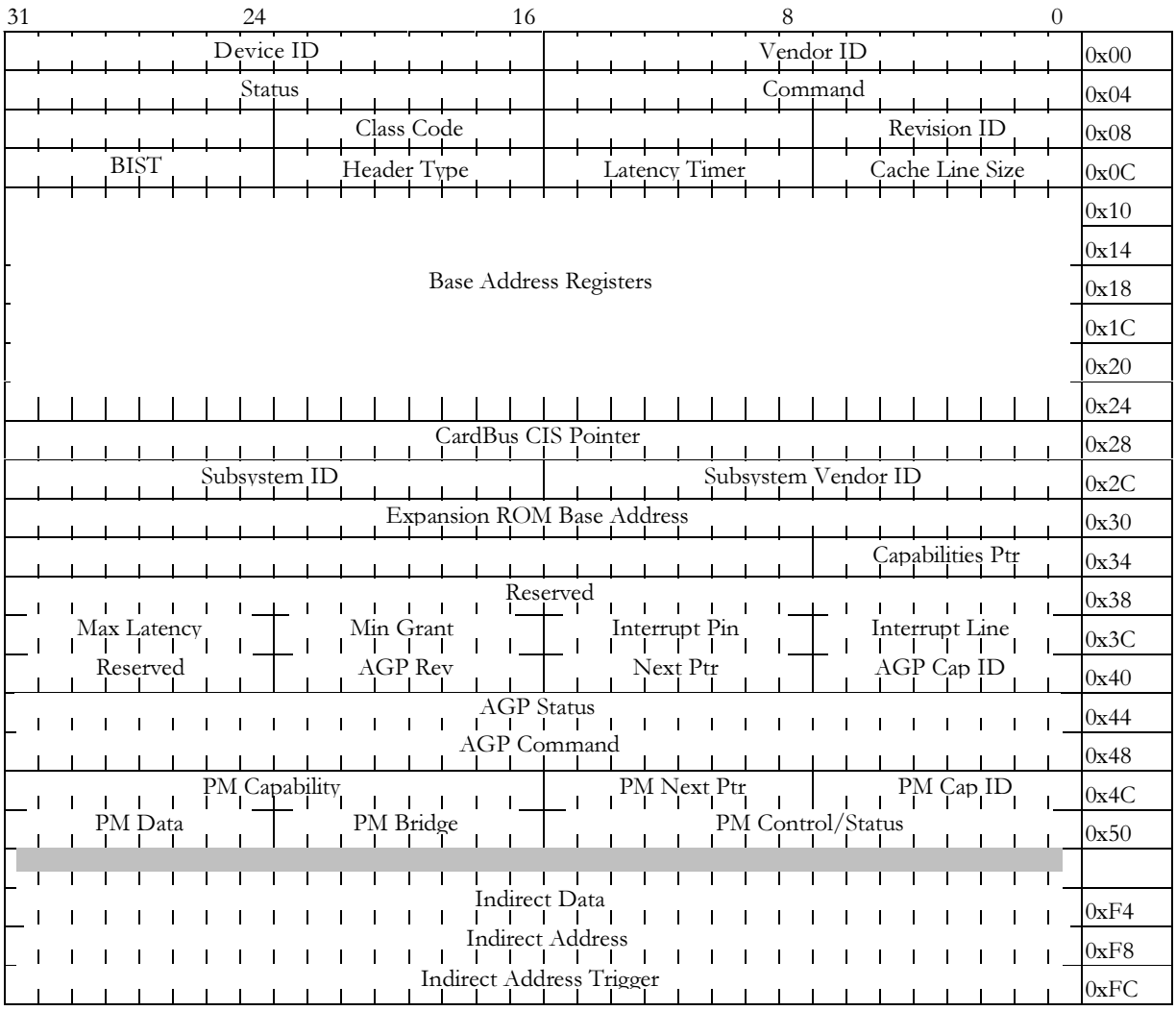

Figure 2-1 PCI Configuration Region

2.2 Region Zero Address Map

The Permedia4 region zero address map is shown in Table 2-1:

Address Range	Region Select	Byte Swap/ Write Combined
0000.0000 -> 0000.02FF	Control Status	No
0000.0300 -> 0000.03FF	Bypass Control	No
0000.0400 -> 0000.0FFF	Repeat of the Control and Bypass Decodes	No
0000.1000 -> 0000.1FFF	Memory Control	No
0000.2000 -> 0000.2FFF	GP FIFO Access	No
0000.3000 -> 0000.30FF	Video Control	No
0000.3100 -> 0000.3FFF	Video Overlay Control	No
0000.4000 -> 0000.4FFF	RAMDAC	No
0000.5000 -> 0000.57FF	VS GP	No
0000.5800 -> 0000.5FFF	VSCtl	No
0000.6000 -> 0000.6FFF	VGA Control	No
0000.7000 -> 0000.7FFF	TextureData FIFO	No
0000.8000 -> 0000.FFFF	GP Registers	No
0001.0000 -> 0001.01FF	Control Status	Yes
0001.0300 -> 0001.03FF	Bypass Control	Yes
0001.0400 -> 0001.0FFF	Repeat of the Control and Bypass Decodes	Yes
0001.1000 -> 0001.1FFF	Memory Control	Yes
0001.2000 -> 0001.2FFF	GP FIFO Access	Yes
0001.3000 -> 0001.37FF	Video Control	Yes
0001.3800 -> 0001.3FFF	Video Overlay Control	Yes
0001.4000 -> 0001.4FFF	RAMDAC	Yes
0001.5000 -> 0001.57FF	VS GP	Yes
0001.5800 -> 0001.5FFF	VSCtl	Yes
0001.6000 -> 0001.6FFF	VGA Control	Yes
0001.7000 -> 0001.7FFF	TextureData FIFO	Yes
0001.8000 -> 0001.FFFF	GP Registers	Yes

Table 2- 1 Region Zero Address Map

2.3 PCI Address Regions

Permedia4 has seven base address regions, as shown in Table 2-2:

Region	Address Space	Bytes	Description	Comments
Config	Configuration	256	PCI Configuration	PCI special
Zero	Memory	128 K	Control Registers	Relocatable
One	Memory	64M	Memory Aperture One	Relocatable
Two	Memory	64M	Memory Aperture Two	Relocatable
Three	I/O	16	Indirect Access I/O	Optional and Relocatable
ROM	Memory	64 K	Expansion ROM	Relocatable
VGA	Memory & I/O	—	VGA Access	Optional and Fixed

Table 2- 2 Permedia4 PCI Address Regions

3

Video Unit and RAMDAC

Permedia4 incorporates a high performance 270MHz RAMDAC The video unit and RAMDAC should be configured to display the framebuffer data with the format, resolution, and refresh frequency required.

3.1 RAMDAC Characteristics

- High resolution 270 MHz, 128-bit RAMDAC
- Supporting screen resolutions up to 1600x1200@96Hz or 1920x1200@82Hz refresh rate
- Supports packed pixel formats
- Color depths of 8, 16 and 32 bits/pixel
- Dot clock phase-locked loop (PLL)
- Triple 8-bit D/A converters
- 64x64x2-bit cursor array to support a 2, 4 or 16 color hardware cursor with cursor shapes cache

3.1.1 Display Resolutions

Permedia4 supports all the standard screen resolutions at ergonomic refresh rates. For each resolution and color depth in the table below, the frequency figure represents the refresh rate supported using the VESA generalized Timing formula with 50% of the memory bandwidth used for screen refresh and 50% for drawing assuming a pixel clock of 270MHz.

Resolution	8 bpp	16 bpp	32 bpp
320x200	220 Hz	220 Hz	220 Hz
640x480	220 Hz	220 Hz	220 Hz
800x600	220 Hz	220 Hz	220 Hz
1024x768	217 Hz	217 Hz	217 Hz
1152x864	176 Hz	176 Hz	176 Hz
1280x1024	137 Hz	137 Hz	137 Hz
1600x1200	96 Hz	96 Hz	96 Hz
1920x1080	90 Hz	90 Hz	90 Hz
1920x1200	82.3 Hz	82.3 Hz	82.3 Hz

Table 3.2 Display Resolutions

Resolutions are driver and memory limited. A 32MB framebuffer for example can support 2048x1200 @ 32bit colour, 32bit Z; or 2048x1536 @ 32bit colour, 16bit Z.

3.1.2 Display Data Channels (DDC)

Two control lines are dedicated on Permedia4 to support DDC1 and DDC2AB+ monitor configuration utilities. The DDC2 serial bus is independent of the serial bus in the video stream interface.

3.2 Display Timing Values

Table 3- 1 Timing Values for 640x480 16 BPP 75Hz

Parameter	Hex	Decimal
HTotal	0x065	101
HsStart	0x003	3
HsEnd	0x00B	11
HbEnd	0x016	22
HgEnd	0x016	22
VTotal	0x1F5	501
VsStart	0x000	0
VsEnd	0x003	3
VbEnd	0x016	22
ScreenStride	0x050	80
ScreenBase	0x000	0
VideoControl	0x029	41

Table 3- 2 Timing Values for 800x600 32 BPP 75Hz

Parameter	Hex	Decimal
HTotal	0x103	259
HsStart	0x00A	10
HsEnd	0x01E	30
HbEnd	0x03C	60
HgEnd	0x03C	60
VTotal	0x272	626
VsStart	0x000	0
VsEnd	0x003	3
VbEnd	0x01B	27
ScreenStride	0x0C8	200
ScreenBase	0x000	0
VideoControl	0x029	41

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