P9®

Reference Guide Volume IV -

Physical Features

DRAFT

PROPRIETARY AND CONFIDENTIAL INFORMATION

3D*labs*®

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Physical Features

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Issue 1

Proprietary Notice

Email: info@3dlabs.com
Web: http://www.3dlabs.com

3D*labs* Ltd.
Meadlake Place
Thorpe Lea Road, Egham
Surrey, TW20 8HE
United Kingdom
Tel: +44 (0) 1784 470555
Fax: +44 (0) 1784 470699

3D*labs* K.K.
Shiroyama JT Mori Bldg 16F
40301 Toranomon
Minato-ku, Tokyo, 105, Japan
Tel: +81-3-5403-4653
Fax: +91-3-5403-4646

3D*labs* Inc.
480 Potrero Avenue
Sunnyvale, CA 94086,
United States
Tel: +1 (408) 530-4700
Fax: +1 (408) 530-4701

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User Note

This manual uses hyperlinks (in MSWord DOC file distributions only) to improve ease of access to relevant information for online users. For correct operation of hyperlinks the complete set of *Reference Guide* and *Programmer's Guide* files should be in a single Windows directory or folder.

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Package Diagrams

P9 is a 644-ball thermally-enhanced HSBGA package with 100 thermal balls, in a 31mm package.

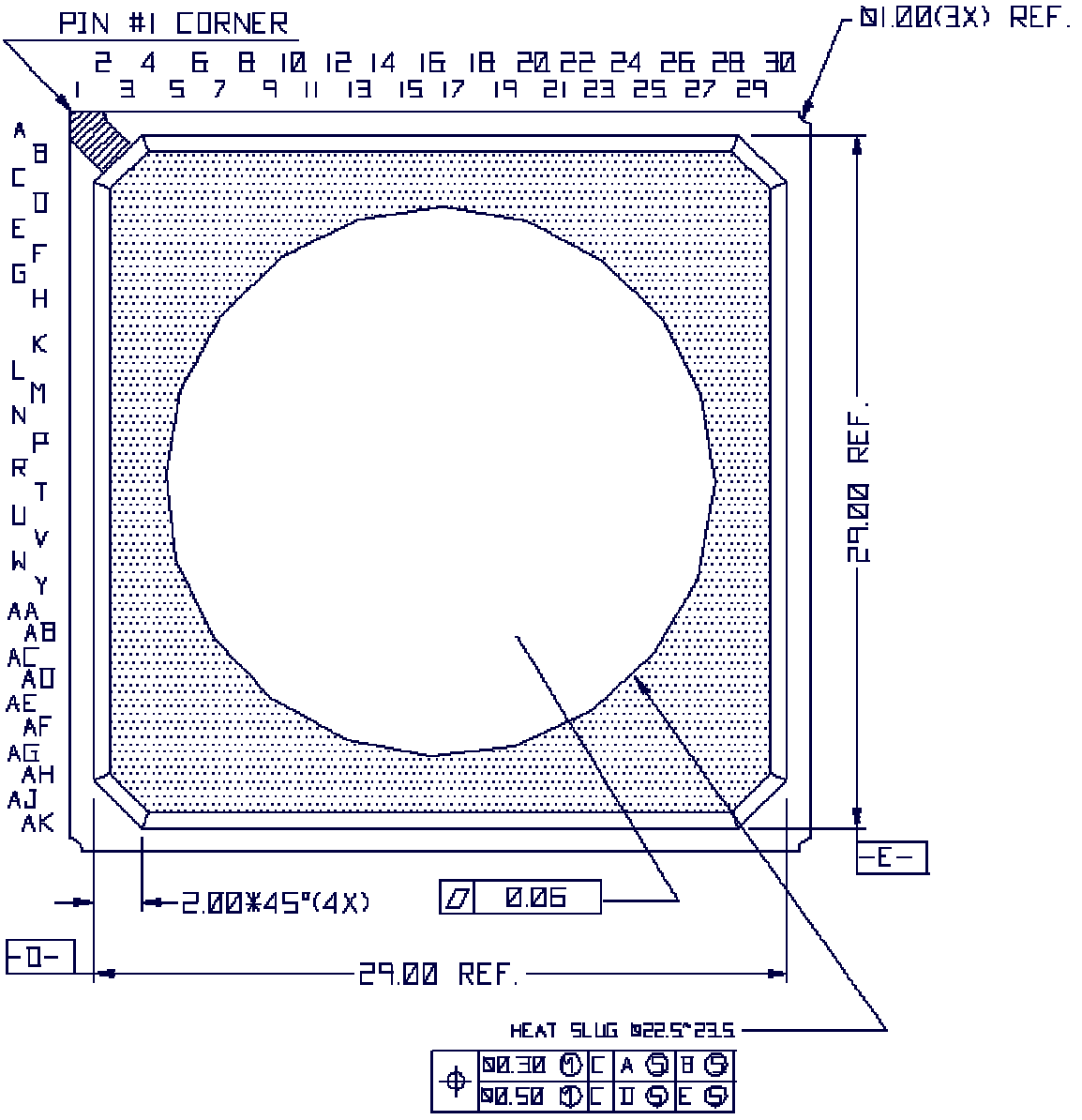

Figure 7-1 Package Diagram Top View

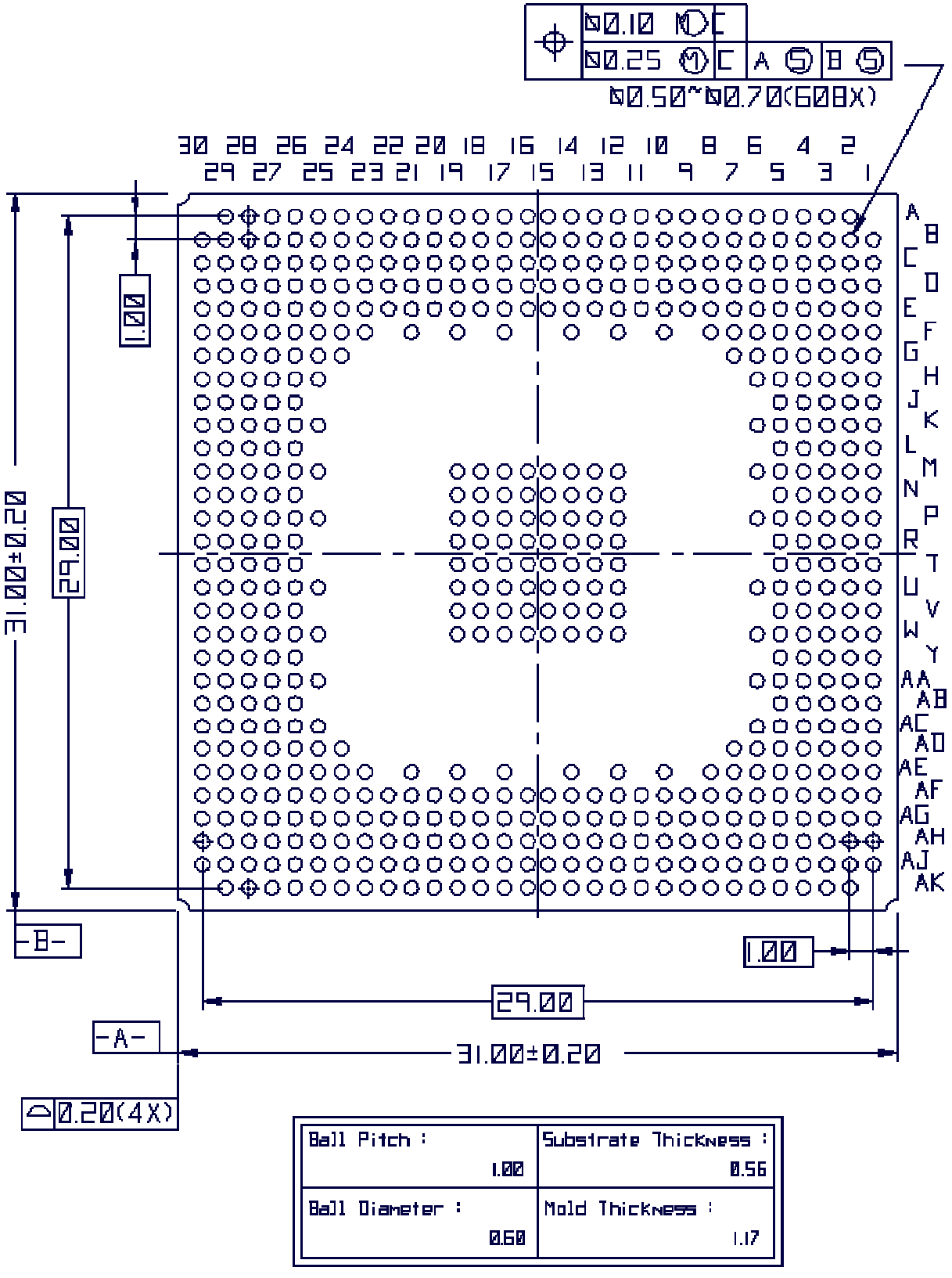

Figure 7-2 Ball pattern of 644L HSBGA

Figure 7-3 Package Profile Views

Description	Dimension
Package Size	31.0 x 31.0 mm
Die Size	10.7 x 10.7 mm
Type	HSBGA
Body Height	
Substrate Layer	4L (2 oz)
Ball pitch	1.00 mm
Ball pad opening	0.6 mm

Table 7-1 Package dimensions and characteristics

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Pin Assignment

8.1 Configuring AGP Pins for PCI boards

The table below shows pin configuration for AGP pins used in a PCI-bus environment.

Note: It is also usually recommended to tie ADSTB and ADSTBN to eliminate possible floating and noise.

Pin Name	Value
AGPSTB	NC
AGPSTBN	NC
AGPSBA[7:0]	NC
AGPST[2:0]	Pull high to 3.3V with 4.7K resistor
AGPADSTB[1:0]	Pull high to 3.3V with 4.7K resistor
AGPADSTBN[1:0]	Pull low to GND with 4.7K resistor
AGPIPEN	NC
AGPRBFN	NC
AGPWBFN	NC
VDDQ[5:0]	3.3V Plane
AGP3V3[4:0]	3.3V Plane
AGPVDet	GND
AGPVref	Set = PCI voltage/2
AGPZset	NC

8.2 Ground and Power Pins

8.2.1 Ground

At the following pins, Core and I/O ground supply = 0v:

A10, A22, A28, A3, A4, AA25, AA30, AA5, AA6, AB3, AB4, AB5, AC1, AC4, AD5, AE10, AE12, AE14, AE17, AE19, AE21, AE26, AE28, AE5, AE3, AE4, AF10, AF11, AF12, AF13, AF14, AF15, AF18, AF19, AF21, AF22, AF24, AF25, AF26, AG13, AG14, AG27, AG30, AG5, AG3, AG4, AH29, AH30, AH4, AJ14, AJ21, AJ28, AJ3, AJ9, AK20, AK3, AK4, B3, B7, C14, C17, C3, C30, E22, E28, E7, F10, F14, F17, F21, F26, F3, J1, J30, K25, K6, M1, M6, P25, P28, P6, R1, T28, U25, U28, U4, U5, U6, V1, V4, V5, W6, Y3, Y4, Y5.

8.2.2 VCC2V5 and VDD1V2

The following VCC2V5 pins are driven at 2.50vdc nominal:

F5, B1, A2, B2, E5, E8, A9, C12, F12, E15, E16, C19, F19, E23, A24, B26, A29, B30, B29, E26, H30, H26, M28, M25, R26, T26, W28, W25, AB30, AC26, AJ30, AK29, AJ29.

The following VDD1V2 pins are driven at 1.20vdc nominal:

AE6, AD6, AD7, AC6, H6, G6, F6, F7, G7, F8, F23, F24, F25, G25, G24, H25, AC25, AD25, AE25, AE24, AD24, AE23, AE8, AE7.

8.3 Pinlists

The tables below provides a brief description of each pin organized alphabetically by name and numerically by pin number.

All pins are listed here. For specifics of pin electrical characteristics refer to chapter 10, Electrical Characteristics.

The pin type definitions used are:

I/O: Input Signal (tolerates 2.5 and 3.3 VDC PCI and AGP4X standards)
PWR: Various power feed types
BIDIR: Bidirectional signals
IN, OUT Directional signals

Pins added since P10 are shown on a shaded background. There are numerous deletions, reflecting for example the use of only one DDC pair and one Sync pair per head (servicing both DFP and analog ports).

8.4 Pinlist by Name

PIN NAME	LOCATION		TYPE	DESCRIPTION
AGP3V3[0]	AK	21	PWR	3.30vdc nominal
AGP3V3[1]	AF	17	PWR	3.30vdc nominal
AGP3V3[2]	AK	28	PWR	3.30vdc nominal
AGP3V3[3]	AK	8	PWR	3.30vdc nominal
AGP3V3[4]	AK	14	PWR	3.30vdc nominal
AGPADSTB[0]	AJ	25	IN	AD_STB0 (agp only)
AGPADSTB[1]	AJ	17	IN	AD_STB0/1# (agp only) AD strobe - used in agp4x only (1.5v)
AGPADSTBN[0]	AH	25	IN	AD_STB0/1#(agp only)AD strobe-used in agp4x only[1.5V]
AGPADSTBN[1]	AH	17	IN	AD_STB0/1#(agp only)AD strobe-used in agp4x only[1.5V]
AGPPipeN	AH	10	OUT	PIPE#-Pipelined request(agp only)[3.3V]
AGPRbfN	AK	11	BIDIR	RGF# Read buffer full (AGP only) (3.3v)
AGPSBA[0]	AJ	11	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AGPSBA[1]	AH	11	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AGPSBA[2]	AK	12	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AGPSBA[3]	AG	11	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AGPSBA[4]	AK	13	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AGPSBA[5]	AG	12	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AGPSBA[6]	AJ	13	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AGPSBA[7]	AH	13	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]

PIN NAME	LOCATION		TYPE	DESCRIPTION
AGPSBSTB	AJ	12	OUT	SB_STB Sideband strobe (agp only)-(differential in AGP4x)[1.5V-3.3V]
AGPSBSTBN	AH	12	OUT	SB_STB# Sideband strobe (agp only) differential strobe used in agp4x only (1.5v).
AGPSt[0]	AK	10	BIDIR	ST Status bus (agp only) (1.5-3.3v)
AGPSt[1]	AG	9	BIDIR	ST Status bus(agp only)[3.3V]
AGPSt[2]	AJ	10	BIDIR	ST Status bus (agp only) [3.3V]
AGPVREF	AK	27	BIDIR	AGP I/O Reference voltage = VCCA 15/2 (1.67v or 0.75v)
AGPWbfN	AG	10	IN	Write Buffer Full signal
AGPZSET	AF	20	IN	Analog reference impedance(resistor)-connect to VDDQ via 37.5 ohms
DacAAG[0]	AH	3	PWR	DAC Head 0 analogue ground = 0v (isolated from GND)
DacAAG[1]	AG	2	PWR	DAC Head 0 Analogue Ground
DacAAG[2]	AD	2	PWR	DAC Head 0 Analogue Ground
DacAAG[3]	AD	4	PWR	DAC Head 0 Analogue Ground
DacABlue	AD	1	AN	DAC Head 0 Blue Out
DacAComp	AE	1	AN	DAC Head 0 Op-amp Compensation
DacAFSAdj	AD	3	AN	DAC Head 0 Full Scale Adjust
DacAGreen	AF	1	AN	DAC Head 0 Green Out
DacARed	AG	1	OUT	DAC Head 0 Red Out
DacAVAA[0]	AF	2	PWR	DAC Head 0 Analogue Power
DacAVAA[1]	AF	4	PWR	DAC Head 0 Analogue Power
DacAVAA[2]	AE	2	PWR	DAC Head 0 Analogue Power
DacAVref	AF	3	PWR	DAC Head 0 Voltage Reference signal
DacBAG[0]	AC	3	PWR	DAC Head 1 Analogue Ground
DacBAG[1]	AB	2	PWR	DAC Head 1 Analogue Ground
DacBAG[2]	W	2	PWR	DAC Head 1 Analogue Ground
DacBAG[3]	W	4	PWR	DAC Head 1 Analogue Ground
DacBBlue	W	1	AN	DAC Head 1 Blue Out
DacBComp	Y	1	AN	DAC Head 1 Op-amp Compensation
DacBFSAdj	W	3	AN	DAC Head 1 Full Scale Adjust
DacBGreen	AA	1	AN	DAC Head 1 Green Out
DacBRed	AB	1	AN	DAC Head 1 Red Out
DacBVAA[0]	AA	2	PWR	DAC Head 1 Analogue Power
DacBVAA[1]	AA	4	PWR	DAC Head 1 Analogue Power
DacBVAA[2]	Y	2	PWR	DAC Head 1 Analogue Power
DacBVref	AA	3	PWR	DAC Head 1 Voltage Reference
DfpABlank	K	1	OUT	DFP Blank signal Head 0
DfpAStrobe	J	5	OUT	DFP Data Strobe signal Head 0
DfpBBlank	N	2	OUT	DFP Blank signal Head 1
DfpBStrobe	N	1	OUT	DFP Strobe signal Head 1
DfpData[0]	F	2	BIDIR	Flat Panel Data signal / Interleave Data In signal

PIN NAME	LOCATION		TYPE	DESCRIPTION
DfpData[1]	F	1	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[10]	J	3	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[11]	J	4	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[12]	K	2	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[13]	K	3	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[14]	K	4	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[15]	L	1	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[16]	L	2	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[17]	L	3	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[18]	L	4	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[19]	L	5	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[2]	G	2	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[20]	M	2	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[21]	M	3	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[22]	M	4	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[23]	M	5	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[3]	G	3	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[4]	G	4	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[5]	H	1	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[6]	H	2	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[7]	H	3	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[8]	H	4	BIDIR	Flat Panel Data signal / Interleave Data In signal
DfpData[9]	H	5	BIDIR	Flat Panel Data signal / Interleave Data In signal
DFPVREF[0]	J	2	PWR	Supplied from SSTLDFP_Vref = VCC_DFP/2
DFPVREF[1]	N	3	PWR	Supplied from SSTLDFP_Vref = VCC_DFP/2
GenVSync	AG	7	IN	Genlock Vertical Sync signal for ExtVSync, enabled by GenLockControl register

PIN NAME	LOCATION		TYPE	DESCRIPTION
Lock	AG	6	BIDIR	Same as P10 VidLock signals
MAAddr[10]	A	18	OUT	Memory Controller A Address signal
MAAddr[0]	B	13	OUT	Memory Controller A Address signal
MAAddr[1]	A	15	OUT	Memory Controller A Address signal
MAAddr[2]	B	17	OUT	Memory Controller A Address signal
MAAddr[3]	B	18	OUT	Memory Controller A Address signal
MAAddr[4]	A	19	OUT	Memory Controller A Address signal
MAAddr[5]	B	19	OUT	Memory Controller A Address signal
MAAddr[6]	B	20	OUT	Memory Controller A Address signal
MAAddr[7]	A	17	OUT	Memory Controller A Address signal
MAAddr[8]	A	14	OUT	Memory Controller A Address signal
MAAddr[9]	B	15	OUT	Memory Controller A Address signal
MAAddrA	B	14	OUT	Memory Controller A Address ‘A’ signal
MAAddrB[0]	A	16	BIDIR	Memory Controller A Address ‘B’ signal
MAAddrB[1]	B	16	OUT	Memory Controller A Address ‘B’ signal
MABa[0]	B	12	OUT	Memory Controller A Bank Address signal
MABa[1]	A	13	OUT	Memory Controller A Bank Address signal
MACasN	B	11	OUT	Memory Controller A Column Address Strobe signal
MACke	B	21	OUT	Memory Controller A Clock Enable signal
MAClk	A	20	OUT	Memory Controller A Differential Clock signal
MAClkN	A	21	OUT	Memory Controller A Differential Clock signal
MAData[0]	F	4	BIDIR	Memory Controller A Data signal
MAData[1]	E	4	BIDIR	Memory Controller A Data signal
MAData[10]	B	4	BIDIR	Memory Controller A Data signal
MAData[11]	D	5	BIDIR	Memory Controller A Data signal
MAData[12]	C	5	BIDIR	Memory Controller A Data signal
MAData[13]	B	5	BIDIR	Memory Controller A Data signal
MAData[14]	A	5	BIDIR	Memory Controller A Data signal
MAData[15]	E	6	BIDIR	Memory Controller A Data signal
MAData[16]	D	6	BIDIR	Memory Controller A Data signal
MAData[17]	C	6	BIDIR	Memory Controller A Data signal
MAData[18]	D	7	BIDIR	Memory Controller A Data signal
MAData[19]	C	7	BIDIR	Memory Controller A Data signal
MAData[2]	E	3	BIDIR	Memory Controller A Data signal
MAData[20]	A	7	BIDIR	Memory Controller A Data signal
MAData[21]	D	8	BIDIR	Memory Controller A Data signal
MAData[22]	C	8	BIDIR	Memory Controller A Data signal
MAData[23]	E	9	BIDIR	Memory Controller A Data signal
MAData[24]	D	9	BIDIR	Memory Controller A Data signal
MAData[25]	C	9	BIDIR	Memory Controller A Data signal
MAData[26]	B	9	BIDIR	Memory Controller A Data signal

PIN NAME	LOCATION		TYPE	DESCRIPTION
MAData[27]	E	10	BIDIR	Memory Controller A Data signal
MAData[28]	D	10	BIDIR	Memory Controller A Data signal
MAData[29]	C	10	BIDIR	Memory Controller A Data signal
MAData[3]	E	2	BIDIR	Memory Controller A Data signal
MAData[30]	E	11	BIDIR	Memory Controller A Data signal
MAData[31]	E	12	BIDIR	Memory Controller A Data signal
MAData[32]	D	12	BIDIR	Memory Controller A Data signal
MAData[33]	E	13	BIDIR	Memory Controller A Data signal
MAData[34]	D	13	BIDIR	Memory Controller A Data signal
MAData[35]	C	13	BIDIR	Memory Controller A Data signal
MAData[36]	E	14	BIDIR	Memory Controller A Data signal
MAData[37]	D	14	BIDIR	Memory Controller A Data signal
MAData[38]	D	15	BIDIR	Memory Controller A Data signal
MAData[39]	C	15	BIDIR	Memory Controller A Data signal
MAData[4]	E	1	BIDIR	Memory Controller A Data signal
MAData[40]	E	17	BIDIR	Memory Controller A Data signal
MAData[41]	D	17	BIDIR	Memory Controller A Data signal
MAData[42]	E	18	BIDIR	Memory Controller A Data signal
MAData[43]	D	18	BIDIR	Memory Controller A Data signal
MAData[44]	C	18	BIDIR	Memory Controller A Data signal
MAData[45]	E	19	BIDIR	Memory Controller A Data signal
MAData[46]	D	19	BIDIR	Memory Controller A Data signal
MAData[47]	E	20	BIDIR	Memory Controller A Data signal
MAData[48]	E	21	BIDIR	Memory Controller A Data signal
MAData[49]	D	21	BIDIR	Memory Controller A Data signal
MAData[5]	D	3	BIDIR	Memory Controller A Data signal
MAData[50]	C	21	BIDIR	Memory Controller A Data signal
MAData[51]	D	22	BIDIR	Memory Controller A Data signal
MAData[52]	C	22	BIDIR	Memory Controller A Data signal
MAData[53]	D	23	BIDIR	Memory Controller A Data signal
MAData[54]	C	23	BIDIR	Memory Controller A Data signal
MAData[55]	E	24	BIDIR	Memory Controller A Data signal
MAData[56]	D	24	BIDIR	Memory Controller A Data signal
MAData[57]	C	24	BIDIR	Memory Controller A Data signal
MAData[58]	B	24	BIDIR	Memory Controller A Data signal
MAData[59]	E	25	BIDIR	Memory Controller A Data signal
MAData[6]	C	2	BIDIR	Memory Controller A Data signal
MAData[60]	D	25	BIDIR	Memory Controller A Data signal
MAData[61]	C	25	BIDIR	Memory Controller A Data signal
MAData[62]	D	26	BIDIR	Memory Controller A Data signal
MAData[63]	C	26	BIDIR	Memory Controller A Data signal
MAData[7]	C	1	BIDIR	Memory Controller A Data signal
MAData[8]	D	4	BIDIR	Memory Controller A Data signal
MAData[9]	C	4	BIDIR	Memory Controller A Data signal
MADm[0]	D	2	OUT	Memory controller A Data write mask signal
MADm[1]	B	6	OUT	Memory controller A Data write mask signal
MADm[2]	B	8	OUT	Memory controller A Data write

PIN NAME	LOCATION		TYPE	DESCRIPTION
				mask signal
MADm[3]	D	11	OUT	Memory controller A Data write mask signal
MADm[4]	D	16	OUT	Memory controller A Data write mask signal
MADm[5]	D	20	OUT	Memory controller A Data write mask signal
MADm[6]	B	23	OUT	Memory controller A Data write mask signal
MADm[7]	B	25	OUT	Memory controller A Data write mask signal
MADqs[0]	D	1	BIDIR	Memory Controller A Data Strobe signal
MADqs[1]	A	6	BIDIR	Memory Controller A Data Strobe signal
MADqs[2]	A	8	BIDIR	Memory Controller A Data Strobe signal
MADqs[3]	C	11	BIDIR	Memory Controller A Data Strobe signal
MADqs[4]	C	16	BIDIR	Memory Controller A Data Strobe signal
MADqs[5]	C	20	BIDIR	Memory Controller A Data Strobe signal
MADqs[6]	A	23	BIDIR	Memory Controller A Data Strobe signal
MADqs[7]	A	25	BIDIR	Memory Controller A Data Strobe signal
MARasN	A	12	OUT	Memory Controller A Row Address Strobe signal
MAWeN	A	11	OUT	Memory Controller A Write Enable signal
MBAddr[10]	U	30	OUT	Memory Controller B Address signal
MBAddr[0]	M	29	OUT	Memory Controller B Address signal
MBAddr[1]	P	30	OUT	Memory Controller B Address signal
MBAddr[2]	T	29	OUT	Memory Controller B Address signal
MBAddr[3]	U	29	OUT	Memory Controller B Address signal
MBAddr[4]	V	30	OUT	Memory Controller B Address signal
MBAddr[5]	V	29	OUT	Memory Controller B Address signal
MBAddr[6]	W	29	OUT	Memory Controller B Address signal
MBAddr[7]	T	30	OUT	Memory Controller B Address signal
MBAddr[8]	N	30	OUT	Memory Controller B Address signal
MBAddr[9]	P	29	OUT	Memory Controller B Address signal
MBAddrA	N	29	OUT	Memory Controller B Address ‘A’ signal
MBAddrB[0]	R	30	OUT	Memory Controller B Address ‘B’ signal
MBAddrB[1]	R	29	OUT	Memory Controller B Address ‘B’ signal
MBBa[0]	L	29	OUT	Memory Controller B Bank Address signal
MBBa[1]	M	30	OUT	Memory Controller B Bank Address signal

PIN NAME	LOCATION		TYPE	DESCRIPTION
MBCasN	K	29	OUT	Memory Controller B Column Address Strobe signal
MBCke	Y	29	OUT	Memory Controller B Clock Enable signal
MBClk	W	30	OUT	Memory Controller B Differential Clock signal
MBClkN	Y	30	OUT	Memory Controller B Differential Clock signal
MBData[0]	A	26	BIDIR	Memory Controller B Data signal
MBData[1]	C	27	BIDIR	Memory Controller B Data signal
MBData[10]	F	27	BIDIR	Memory Controller B Data signal
MBData[11]	F	28	BIDIR	Memory Controller B Data signal
MBData[12]	F	29	BIDIR	Memory Controller B Data signal
MBData[13]	F	30	BIDIR	Memory Controller B Data signal
MBData[14]	G	26	BIDIR	Memory Controller B Data signal
MBData[15]	G	27	BIDIR	Memory Controller B Data signal
MBData[16]	G	28	BIDIR	Memory Controller B Data signal
MBData[17]	G	29	BIDIR	Memory Controller B Data signal
MBData[18]	G	30	BIDIR	Memory Controller B Data signal
MBData[19]	H	27	BIDIR	Memory Controller B Data signal
MBData[2]	B	28	BIDIR	Memory Controller B Data signal
MBData[20]	H	28	BIDIR	Memory Controller B Data signal
MBData[21]	H	29	BIDIR	Memory Controller B Data signal
MBData[22]	J	26	BIDIR	Memory Controller B Data signal
MBData[23]	K	26	BIDIR	Memory Controller B Data signal
MBData[24]	K	27	BIDIR	Memory Controller B Data signal
MBData[25]	K	28	BIDIR	Memory Controller B Data signal
MBData[26]	L	26	BIDIR	Memory Controller B Data signal
MBData[27]	M	26	BIDIR	Memory Controller B Data signal
MBData[28]	M	27	BIDIR	Memory Controller B Data signal
MBData[29]	N	26	BIDIR	Memory Controller B Data signal
MBData[3]	C	28	BIDIR	Memory Controller B Data signal
MBData[30]	N	27	BIDIR	Memory Controller B Data signal
MBData[31]	N	28	BIDIR	Memory Controller B Data signal
MBData[32]	P	26	BIDIR	Memory Controller B Data signal
MBData[33]	P	27	BIDIR	Memory Controller B Data signal
MBData[34]	T	27	BIDIR	Memory Controller B Data signal
MBData[35]	U	26	BIDIR	Memory Controller B Data signal
MBData[36]	U	27	BIDIR	Memory Controller B Data signal
MBData[37]	V	26	BIDIR	Memory Controller B Data signal
MBData[38]	V	27	BIDIR	Memory Controller B Data signal
MBData[39]	V	28	BIDIR	Memory Controller B Data signal
MBData[4]	C	29	BIDIR	Memory Controller B Data signal
MBData[40]	W	26	BIDIR	Memory Controller B Data signal
MBData[41]	W	27	BIDIR	Memory Controller B Data signal
MBData[42]	Y	26	BIDIR	Memory Controller B Data signal
MBData[43]	AA	26	BIDIR	Memory Controller B Data signal
MBData[44]	AA	27	BIDIR	Memory Controller B Data signal
MBData[45]	AA	28	BIDIR	Memory Controller B Data signal

PIN NAME	LOCATION		TYPE	DESCRIPTION
MBData[46]	AB	26	BIDIR	Memory Controller B Data signal
MBData[47]	AB	27	BIDIR	Memory Controller B Data signal
MBData[48]	AB	28	BIDIR	Memory Controller B Data signal
MBData[49]	AB	29	BIDIR	Memory Controller B Data signal
MBData[5]	D	27	BIDIR	Memory Controller B Data signal
MBData[50]	AC	27	BIDIR	Memory Controller B Data signal
MBData[51]	AC	28	BIDIR	Memory Controller B Data signal
MBData[52]	AD	26	BIDIR	Memory Controller B Data signal
MBData[53]	AD	27	BIDIR	Memory Controller B Data signal
MBData[54]	AD	28	BIDIR	Memory Controller B Data signal
MBData[55]	AD	29	BIDIR	Memory Controller B Data signal
MBData[56]	AD	30	BIDIR	Memory Controller B Data signal
MBData[57]	AE	27	BIDIR	Memory Controller B Data signal
MBData[58]	AE	29	BIDIR	Memory Controller B Data signal
MBData[59]	AE	30	BIDIR	Memory Controller B Data signal
MBData[6]	D	28	BIDIR	Memory Controller B Data signal
MBData[60]	AF	27	BIDIR	Memory Controller B Data signal
MBData[61]	AF	28	BIDIR	Memory Controller B Data signal
MBData[62]	AG	28	BIDIR	Memory Controller B Data signal
MBData[63]	AG	29	BIDIR	Memory Controller B Data signal
MBData[7]	D	29	BIDIR	Memory Controller B Data signal
MBData[8]	D	30	BIDIR	Memory Controller B Data signal
MBData[9]	E	27	BIDIR	Memory Controller B Data signal
MBDm[0]	B	27	OUT	Memory Controller B Data wirte mask signal
MBDm[1]	E	29	OUT	Memory Controller B Data wirte mask signal
MBDm[2]	J	27	OUT	Memory Controller B Data wirte mask signal
MBDm[3]	L	27	OUT	Memory Controller B Data wirte mask signal
MBDm[4]	R	27	OUT	Memory Controller B Data wirte mask signal
MBDm[5]	Y	27	OUT	Memory Controller B Data wirte mask signal
MBDm[6]	AC	29	OUT	Memory Controller B Data wirte mask signal
MBDm[7]	AF	29	OUT	Memory Controller B Data wirte mask signal
MBDqs[0]	A	27	BIDIR	Memory Controller B Data Strobe signal
MBDqs[1]	E	30	BIDIR	Memory Controller B Data Strobe signal
MBDqs[2]	J	28	BIDIR	Memory Controller B Data Strobe signal
MBDqs[3]	L	28	BIDIR	Memory Controller B Data Strobe signal
MBDqs[4]	R	28	BIDIR	Memory Controller B Data Strobe signal
MBDqs[5]	Y	28	BIDIR	Memory Controller A Data Strobe signal

PIN NAME	LOCATION		TYPE	DESCRIPTION
MBDqs[6]	AC	30	BIDIR	Memory Controller B Data Strobe signal
MBDqs[7]	AF	30	BIDIR	Memory Controller B Data Strobe signal
MBRasN	L	30	OUT	Memory Controller B Row Address Strobe signal
MBWeN	K	30	OUT	Memory Controller B Write Enable signal
PCIAD[0]	AH	27	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[1]	AJ	27	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[10]	AJ	24	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[11]	AG	23	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[12]	AK	23	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[13]	AH	23	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[14]	AJ	23	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[15]	AG	22	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[16]	AG	19	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[17]	AJ	19	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[18]	AH	19	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[19]	AK	18	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[2]	AG	26	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[20]	AG	18	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[21]	AJ	18	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[22]	AH	18	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[23]	AK	17	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[24]	AG	16	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[25]	AK	16	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[26]	AH	16	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[27]	AJ	16	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[28]	AG	15	BIDIR	AD(31-0) address and data bus (1.5-3.3V)

PIN NAME	LOCATION		TYPE	DESCRIPTION
PCIAD[29]	AK	15	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[3]	AK	26	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[30]	AH	15	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[31]	AJ	15	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[4]	AH	26	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[5]	AJ	26	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[6]	AG	25	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[7]	AK	25	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[8]	AK	24	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCIAD[9]	AH	24	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
PCICBEN[0]	AG	24	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
PCICBEN[1]	AK	22	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
PCICBEN[2]	AK	19	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
PCICBEN[3]	AG	17	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
PCIClk	AJ	8	IN	Clk PciClk (3.3v)
PCIDevSelN	AJ	22	BIDIR	DEVSEL# Device select[1.5V-3.3V]
PCIFrameN	AH	20	BIDIR	Frame# Cycle Frame(3.3v)
PCIGntN	AH	9	IN	Gnt# Grant (3.3v)
PCIIdSel	AF	23	IN	Initialisation Device Select
PCIIntAN	AH	8	OUT	INTA# Interrupt A open drain
PCIIRdyN	AJ	20	BIDIR	IRDY# Initiator ready (3.3v)
PCIPar	AH	22	BIDIR	PAR Parity (3.3v)
PCIReqN	AK	9	OUT	REQ# Request[3.3v]
PCIRstN	AG	8	IN	RST# Reset (3.3v)
PCIStopN	AG	21	BIDIR	STOP# [3.3v]
PCITRdyN	AH	21	BIDIR	TRDY# Target Ready[3.3v]
PLLAG[0]	AJ	7	PWR	PLL analogue ground = 0v (islolated from GND)
PLLAG[1]	AJ	6	PWR	PLL analogue ground = 0v (isolated from GND)
PLLAG[2]	AJ	5	PWR	PLL analogue ground = 0v (isolated from GND)
PLLVAA[0]	AH	7	PWR	PLL analogue power = 3.3v
PLLVAA[1]	AH	6	PWR	PLL analogue power 3.3v
PLLVAA[2]	AH	5	PWR	PLL analogue power 3.3v
RefClk	AK	6	IN	Alternative External Reference Clock signal

PIN NAME	LOCATION		TYPE	DESCRIPTION
SBClk	AH	2	BIDIR	Serial Bus Clk signal (Open Collector) Controled from **ROMControl** register.
SBData	AH	1	BIDIR	Serial Bus Data signal (Open Collector) Controled from **ROMControl** register.
ScanEnable	AF	7	IN	Production Test Mode Scan Enable signal
SSTLVREF[0]	B	10	IN	Memory controller reference voltage signal
SSTLVREF[1]	B	22	IN	Memory controller reference voltage signal
SSTLVREF[2]	J	29	IN	Memory controller reference voltage signal
SSTLVREF[3]	AA	29	IN	Memory controller reference voltage signal
Stereo	AJ	4	OUT	Video Stereo signal
TestMode	AF	6	IN	Production test global enable (Active high)
VCC_DFP	P	1	PWR	2.50vdc nominal
VCC_DFP	P	4	PWR	2.50vdc nominal
VCC_DFP	K	5	PWR	2.50vdc nominal
VCC_DFP	G	1	PWR	2.50vdc nominal
VCC_DFP	G	5	PWR	2.50vdc nominal
VDD_TTL	AJ	1	PWR	3.30vdc nominal
VDD_TTL	AJ	2	PWR	3.30vdc nominal
VDD_TTL	AF	5	PWR	3.30vdc nominal
VDD_TTL	AC	2	PWR	3.30vdc nominal
VDD_TTL	AC	5	PWR	3.30vdc nominal
VDD_TTL	W	5	PWR	3.30 vdc nominal
VDD_TTL	U	1	PWR	3.30vdc nominal
VDD_TTL	P	5	PWR	3.30vdc nominal
VDD_TTL	AF	8	PWR	3.30vdc nominal
VDD_TTL	AK	7	PWR	3.30vdc nominal
VDD_TTL	AK	2	PWR	3.30vdc nominal
VDDQ	AH	28	PWR	3.30vdc nominal (1.50vdc nominal AGP4X)
VDDQ	AG	20	PWR	3.30vdc nominal (1.50vdc nominal AGP4X)
VDDQ	AF	16	PWR	3.30vdc nominal (1.50vdc nominal AGP4X)
VDDQ	AH	14	PWR	3.30vdc nominal (1.50vdc nominal AGP4X)
VDDQ	AF	9	PWR	3.30vdc nominal (1.50vdc nominal AGP4X)
VidADDCClk	U	2	BIDIR	DAC DDC Clk signal Head 0 (Open collector)
VidADDCData	U	3	BIDIR	DAC DDC Data signal Head 0 (Open collector)
VidAHSync	P	2	OUT	DAC Horizontal Sync signal Head 0

VidAVSync	P	3	OUT	DAC Vertical Sync signal Head 0
VidBDDCClk	V	2	BIDIR	Head 1 DDC Clk signal (Open Collector)
VidBDDCData	V	3	BIDIR	Head 1 DDC Data signal (Open Collector)
VidBHSync	N	4	OUT	DAC Horizontal Sync signal Head 1
VidBVSync	N	5	OUT	DAC Vertical Sync signal Head 1
VidInData[0]	R	3	IN	***Dual Function:*** DAC Horizontal Sync signal Head 1, and PCIClk 66MHz capable (Active High) – see Reset
VidInData[1]	R	4	IN	***Dual Function:*** Video Input Data signal, and Active High Boot from ROM (UseROMConfig) – see Reset
VidInData[2]	R	5	IN	***Dual Function:*** Video Input Data signal, and Active High Board is AGP Type – see Reset
VidInData[3]	T	1	IN	Video Input signal
VidInData[4]	T	2	IN	Video Input Data signal
VidInData[5]	T	3	IN	Video Input Data signal
VidInData[6]	T	4	IN	Video Input Data signal
VidInData[7]	T	5	IN	Video Input signal
VidInStrobe	R	2	IN	Video Input Data Strobe and Clock Source signal
Xtal	AK	5	BIDIR	External Reference Clock Source signal

8.5 Pinlist by Number

8.6 Schematics

Please refer to the supplied PDF or ZIP file for P9 Typical Board Layouts and Data.

9 Memory

The P9 memory system is intended for use with Double Data Rate (DDR) Synchronous Dynamic Memories. The memories can be SGRAM or SDRAM devices. Configuration is via memory control registers in region 0.:

The system system supports a 256 bit interface split into two 128 bit buses with replicated address and control lines. It can operate as a single 128 bit TQFP or CSP interface. Each interface has its own Address Bus, Control Signals and full register set.

9.1 Strobe Setup

Strobes are supplied from memory on data transitions and repositioned to give sufficient data setup time using delay chains. There is a register bitfield which selectively delays each of the Incoming and Outgoing strobes and the Clock Out. For a typical clock delay chain register set see *P9 Reference Guide* volume II:

- MV0Clock
- MV0StrobeInvert
- MV0StrobeOutDelay0
- MV0StrobeOutDelay1
- MV0StrobeInDelay0, and
- MV0StrobeInDelay1

The system can be configured to use Strobe per Byte or Strobe per Device.

Note: There is no clock In delay

9.1.1 DDR SDRAM

This configuration uses a full set of 4 individual strobes plus clock out. There is one delay register for each byte lane and controller. The memory device is a 32 bit CSP.

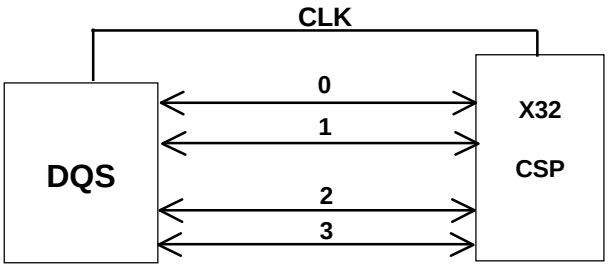

Figure 9.1 Non-common Strobes (DDR SDRAM)

9.1.2 DDR SGRAM

For sigle-strobe devices the strobe is replicated internally on input to supply the 4 strobe lines. DDR SGRAMs are not frequently encountered because they tend to use arbitrary blockfill without support for byte masking.

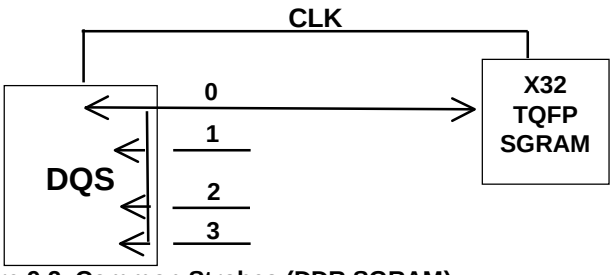

Figure 9.2 Common Strobes (DDR SGRAM)

9.1 System Parameters

The Memory System employs a comprehensive set of registers which allow for a wide range of memory configurations. The timing parameters used to control synchronous memories can be adjusted to allow for optimum performance depending on memory type, speed grade, data rate and the system clock frequency (MClk). Memory functionally can be enabled depending on the type fitted. Full addressing control is available so that virtually any memory configuration can be fitted.

The following parameters are used to control accesses to the memory. These values fall into three categories

- Addressing
- Functionality and Optimizations
- Timing and Mode

9.1.1 Addressing

These parameters are specified in the **MemoryControl** and **MVCaps** registers.

Note: On P9 the Column Address is always 0

9.1.2 Mode and Timing

These parameters are specified in the **MVMode**, **MVCaps** and delay chain registers registers.

9.1.3 Mode

The mode register stores the data for controlling the various operating modes of the DDR SGRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL Reset and various vendor specific options.

Bits	Name	Read	Write	Reset	Description
0…2	BL	✓	✓	0x XXXX .XXX X	Burst Length always = 4 (must be 4 dwords)
3	BT	✓	✓		Burst Type always = 0 (Sequential)
4…6	CAS	✓	✓		CAS Latency
7	TM	✓	✓		Test Mode
8	DLL	✓	✓		DLL Reset: 0= No, 1 = Yes
9…11	Reserved	✓	×		Reserved for future use
12	Mode	✓	✓		Mode/Extended Mode: 0 = Mode, 1 = Extended Mode.
13…15	Reserved	✓	×		
	Extended Mode	✓	✓		Bit pattern to load into extended mode register during initialization
16	DLL	✓	✓		DLL Enable (should be set = 1)
17	DS0	✓	✓		DriveStrength0: With DS1, sets drive strength and matched impedance mode.
18…21	Reserved	✓	×		
22	DS1	✓	✓		See DS0
23…27	Reserved	✓	×		
28	Extended Mode Access	✓	✓		0 = Mode 1 = Extended Mode

9.1.3.1 Burst Length

BL is always 4 dwords on P9

9.1.3.2 Burst Type

Burst Type is Sequential (=0)

9.1.3.3 CAS Latency (CL)

This parameter determines the CAS latency expected by the memory controller. The *CasLatency* parameter can be loaded directly with the appropriate value from the memory device data sheet plus 1. For example, if a CAS latency of 2 is required then the CasLatency parameter should be set to 3.

9.1.4 Extended Mode Parameters

These fields control the DLL enables, Driver Impedance control (DIC) and QFC. DLL and DIC are enabled, QFC is disabled. See the **MVMode** register mask details.

9.1.5 Memory Control

Refer to the **MemoryControl** register in Reference Guide Volume II for parameter information.

9.1.6 MVTimingA

9.1.6.1 Row Cycle (tRC)

The minimum time between Activate Commands to the same bank, calculated as tRC (in MClks) –1.

9.1.6.2 RAS to CAS Write (tRCDWR)

The delay from an Activate Command to a Write Command, calculated as: tRCDWR (in MClks) –1.

9.1.6.3 RAS to CAS Read (tRCDRD)

The delay from an Activate Command to a Read Command, calculated as: tRCDRD (in MClks) –1.

9.1.6.4 CAS to RAS Write (Write to Activate)

Delay from a Write Command to an Activate, defined as:

BL/2 (in Clocks) + 1 + tWR +tRD

Where +1 clock is to clear last data in.

9.1.6.5 CAS to RAS Read (Read to Activate)

Delay from Read Command to Activate, calculated as tRP + (BL/2)

9.1.6.6 Refresh Cycle (tRFC)

This parameter defines the minimum number of MClk cycles that need to be inserted between issuing a REFRESH and an ACTIVATE command, caculated as tRC (in MClk cycles) – 1. It must be enabled by setting the *RefreshEnable* bit in **MVTimingB.***RefreshEnable.*

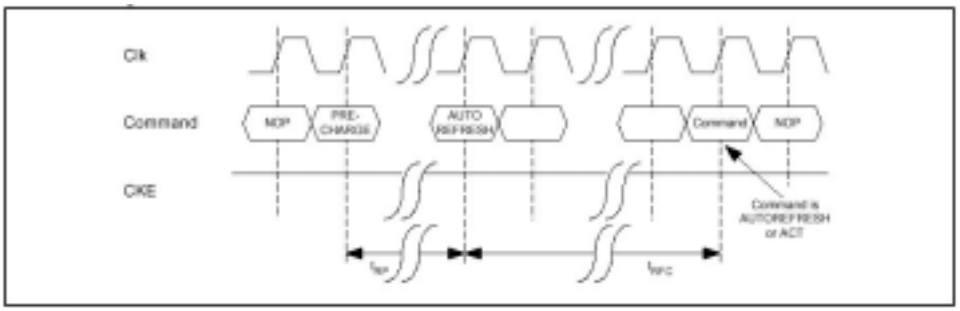

Figure 9.3 Refresh Cycle timing for Infineon HYB25D128323C 128Mbit DDR

9.1.7 MVTimingB

9.1.7.1 RefreshEnable

This flag should be set for Refresh commands to be issued by the memory controller (see MVTimingB).

9.1.7.2 RefreshCount (tRC)

This parameter defines the period between AUTO-REFRESH commands being issued to the memories. The count is in MClks. A delay between the Auto Refresh command and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the tRC(min).

9.1.7.3 ActivateToActivate (tRRD)

This parameter defines the number of MClk cycles that need to be inserted between issuing an ACTIVATE and a subsequent ACTIVATE command to another bank. This parameter is usually detailed in the memory device data sheet as tRRD. If tRRD is quoted including the ACTIVATE cycle, then ActivateToActivate should be calculated as tRRd (in MClk cycles) – 1.

9.1.7.4 Write to Read ()

A Burst Write can be interrupted by a Read command sent to any bank. Delay between a write and a read cycle, calculated as:

BL/2 + 1 + tWR

…where +1 is a clock to clear data from the last input operation.

9.1.7.5 Read to Write

Delay between a read and a write cycle, calculated as: CAS Latency + BL/2

9.1.8 MVCaps

Refer to the **MVCaps** register in *Reference Guide* Volume II for parameter information.

9.1.9 MV0Clock

The MV0 Clock registers refer to Memory Bus A. The MV1Clock registers are identical but refer to bus B.

The 4-bit field defines up to 16 taps at 220 picoseconds.

Refer to the **MV0Clock** or **MV1Clock** registers in the *P9 Reference Guide* Volume II for additional information.

9.1.10 MV0StrobeInvert

9.1.11 MV0StrobeOutDelay[0-1] and MV0StrobeInDelay[0-1] (tQDQSS / tDS)

Delay chain per strobe out or strobe in to configure for varying PCB layouts. The MV1 strobe delay chain registers are identical but apply to the second 128bit memory bus.

Figure 9.1 Typical Configuration for 128bit DD SDRAM

10 Reset

The P9 architecture loads all but the most critical initialisation information from the external Expansion ROM. Hard resets use three dual-function pins: VidInData(0), VidInData(1) and VidInData(2).

Note: These functionas are on different pins in P9 and P10.

VidInData(0) controls the PCI Clock speed (33MHz=1, 66MHz=0). VidInData(2) specifies whether the board is PCI or AGP (AGP=1, PCI=0).

Loading from the ROM is enabled using the single *UseROMConfig* configuration pin . This is a dual-function pin described as VidInData(1) on the pinlist and schematics. Default initialisation values are used for registers when ROM loading is disabled. For more information on the ROMController see the ROMControl section of the *Reference Guide*, volume II.

Following a hardware reset from the PCI Bus, the internal configuration state machine reads the 32-bit word at what would be the highest location in a 64KByte ROM, and interprets this as a pointer to a Configuration Table, as shown in the ROM Layout diagram below.

Note: The vector address is 0xFFFC but the offsets are in dwords.

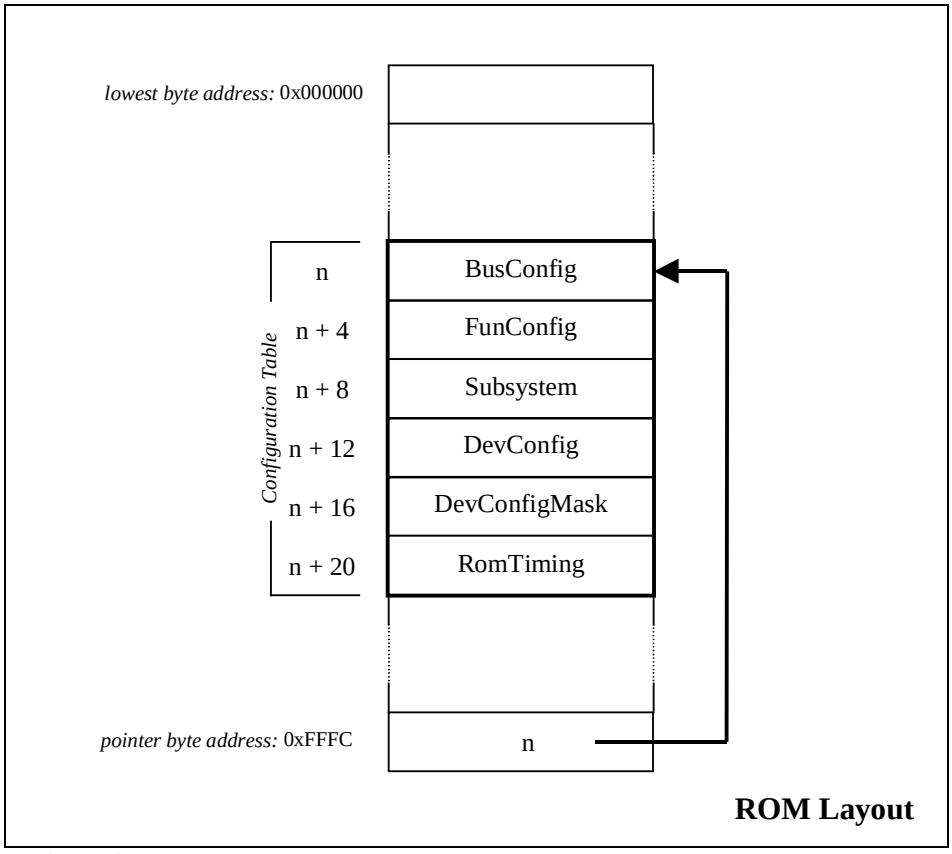

Figure 10.1 ROM Layout

Once the Configuration Table pointer has been read, a sequence of 32-bit words are loaded from it into configuration space registers in the PCI Config unit and control registers in the ROM Controller unit:

Table Offset	Table Field	Destination Unit	Destination Register
00h	BusConfig	PCI Config	CFGBusConfig
04h	FunConfig	PCI Config	CFGFunConfig
08h	Subsystem	PCI Config	CFGSubsystemID *and* CFGSubsystemVendorID
0Ch	DevConfig	PCI Config	CFGDevConfig
10h	DevConfigMask	PCI Config	CFGDevConfigMask
14h	RomTiming	ROM Controller	ROMTiming

The **CFGBusConfig**, **CFGFunConfig**, **CFGDevConfig**, and **CFGDevConfigMask** registers are described in volume II. Each of these four user-defined registers is shared between all functions in a multi-function device, and accesses through any function are mapped to the same underlying register hardware by the bus interface.

11

Thermal

During operation the P9 chip generates heat as a function of the power consumed, which in turn depends on frequency, the number of Texture pipes and other factors. This heat must be dissipated through the package to avoid exceeding the chip's design heat limit ($T_{j(max)}$, typically 125°C) and damaging the chip. In addition to dissipation throgh the pins and thermal balls to the PCB this can be accomplished by improving thermal flow:

- through the chip (junction to ambient air, or θj_a)
- from junction to top-of-case (θj_c).

These figures describe thermal resistance – lower is better. The top-of-case figure is significant where heatsinks and fans are considered.

11.1 Thermal Performance

The thermal performance of the chip is described in JEDEC standard JESD 51-2, 51-6:

$\theta_{ja} = (T_j - T_a) / P_h$

$\theta_{jc} = (T_j - T_c) / P_h$

where:

- Junction Temperature = Tj
- Ambient Temperature = Ta
- Top-of-case Temperature = Tc
- Power Dissipation = Ph

Working assumptions are:

Maximum Power Dissipation (provisional)	$P_{h(max)}$	=	[TBA] Watts (estimated)
Maximum Junction Temperature	$T_{j(max)}$	=	125 °C.
Nominal memory clock frequency	f_{MClk}	=	TBA
Nominal core clock frequency	f_{KClk}	=	TBA

11.2 Thermal Resistivity Equations

These are taken from Ellison's *Thermal Computations for Electronic Equipment.*[1]

11.2.1 Natural Convection

$$h_c = 0.83 \int \left(\frac{\Delta T}{L_{ch}} \right)^n (W / m^2 - {}^0C)$$

where ΔT is the temperature difference in C^0, and the constants f and n are given as

f =1.22 and n = 0.35 for a vertical plate;

f=1.00 and n = 0.33 for a horizontal plate facing upward; and

f =0.50 and n =0.33 for a horizontal plate facing downward

L_{ch} is the characteristic length in meters.

For a horizontal plate, $L_{ch} = \frac{WL}{2(W+L)}$

1 G. N. Ellison, Thermal Computations for Electronic Equipment, R. E. Krieger Publishing Company, Malabar, FL., 1989.

For a vertical plate, $L_{ch} = H$

where W, H and L are the width, height and length of the plate, respectively

11.2.2 Forced convection

$$h_c = 3.786(V/L)^{1/2} \quad (W/m^2 -^0 C)$$

where V is the air speed in m/s, and L is the total length in meters in the flow direction.

Data shown below are hypothetical based on typical package characteristics. Actual figures will be released when available.

608L HSBGA	Thermal Resistance				
	(deg.C/Watt) = θ_{ja}			Ψ_{jt}	θ_{jc}
	0 m/s	*1 m/s*	*2 m/s*	(C/W)	C/W
No heatsink, 4L PCB	12.9	11.2	9.7	1.9	3.1

Table 10-1 P9 Package (820L HSBGA) Thermal Performance

11.3 Cooling

From this analysis, relying on natural convection alone the junction temperature increases 14.8°C/W under normal operating conditions (12.9+1.9 = 14.8). In order not to exceed θ_{jt} the maximum ambient temperature would be 6.6°C at 8W. This would be inadequate and a heatsink would be recommended.

11.4 Operation with Heatsink

11.4.1 Heatsink Attachment

The following method has been approved for the purpose of attaching a heatsink directly onto the HSBGA package:

Thermally conductive epoxy using either Loctite Output 315 with Loctite 7386 or type EG 7655 from A.I. Technology Inc. The thickness of the epoxy layer should be between 0.05mm and 0.15mm with 95% coverage of the contact area.

Typical achievable θ_{cs} using this method is 1.0 °C/Watt

11.4.2 Calculating cooling requirements

With a heatsink attached to the device the junction temperature will depend on θjt, θcs and θsa, where θcs is the thermal resistance of the join between the heatsink and the case and θsa is the thermal resistance of the heatsink, which will be a function of heatsink and system airflow. These are shown as a combined package and heatsink $\theta_{ja,}$ a correction for junction to top of case (ψ_{jt}) and the bond resistance (θ_{cs}).

For a hypothetical 8 watts P_h in adiabatic conditions, junction temperature would be ambient plus 8(7.3 + 1.0 + 1.9) = ambient + 81.6 °C. The maximum ambient possible under this scenario would be 125-81.6=43.4 °C. This method allows easy calculation of cooling requirements under various operating conditions.

11.4.3 Temperature Range (Commercial/Embedded Applications)

P9 is operational in embedded use under a wide range of ambient air temperatures:

- Storage Range: -65°C to 150°C (suitably packed)
- Operating Range: 0°C to $T_{j(max)}$ [2]

[2] The operating range minima and maxima depend on the cooling configuration and whether any warm-up period is allowed. However with sufficient warmup or during continuous operation the thermal resistance would allow reliable operaton under much colder ambient conditions. Similarly with a suitable fan the ambient temperature could be considerably increased without exceeding $T_{j(max)}$.

12

Electrical

Provisional values may be subject to change and should be checked against current values on the 3Dlabs website[3].

Note: SSTL VCC2V5, P VDDQ and others are capable of dual voltage operation. This shows standard TTL levels for simplicity.

12.1 Absolute Maximum Ratings

Junction Temperature	**125°C**
Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to $T_{j(max)}$ (=125°C) [4]
VDD_TTL, VCC_DFP, VCC2.5 DC Supply Voltages	3.6vdc [5]
VCC1.2 DC Supply Voltage	1.32vdc
VDDQ, PLLVAA, DacVAA, AGP3V3 DC Supply Voltages	3.6vdc [6]
SSTL_Vref	VCC2V5/2
DFP_Vref	VCC_DFP/2
DacVREF, DacComp, DacFSAdj	Open
AGPVREF	VDDQ/2
I/O Pin Voltage with respect to GND	-0.5V to VDDQ + 0.3V

12.2 DC Specifications

Symbol/ PAD	**Parameter**	**Min**	**Nominal**	**Unit**
GND	Ground	0.00	0.00	Vdc
VCC1V2	Power at 1.20 vdc	1.08	1.20	Vdc
VDD_TTL	TTL Logic feed at 3.30 vdc	3.00	3.30	Vdc
VCC_DFP	DFP power at 2.5 vdc		2.50	Vdc
VCC2V5	Power at 2.5 vdc		2.50	Vdc
PLLVAA DacVAA AGP3V3	Power at 3.3 vdc		3.30	Vdc
SSTL_VRef	VCC2V5/2		1.25	Vdc
DFP_Vref	VCC_DFP/2		1.25	Vdc

[3] At: http://www.3dlabs.com

[4] This is the maximum junction temperature – normally maximum ambient temperature will be much lower. Maximum ambient temperature depends on thermal path characteristics such as heatsink and air flow.

[5] SSTL VCC2V5 is capable of dual voltage operation. This shows standard TTL level for simplicity.

[6] AGP VDDQ is capable of dual voltage operation. This shows standard TTL level for simplicity.

Symbol/ PAD	Parameter	Min	Nominal	Unit
DacVRef DacCOMP DacFSAdj		Open	Open 0.1 226	Vdc µF to DACVAA Ω to GND
AGPVRef	VDDQ / 2		VDDQ / 2	✓
LPIN	Pin Inductance		2.807	nH
	Pin Capacitance		0.6023	pF
	Pin Resistance		107	mOhm
ICC (3V)	Power Supply Current		TBA	A
ICC (2.5V)	Power Supply Current		TBA	A

12.2.1 PCI Signal DC Specifications

Symbol	Parameter	Min	Max	Unit
V_{PIL}	Input Low Voltage	-0.5	0.3Vcc	V
V^{PIH}	Input High Voltage	0.5Vcc	Vcc + 0.5	V
V_{POL}	Output Low Voltage		0.1Vcc	V
V_{POH}	Output High Voltage	0.9Vcc		V
I_{PIL}	Input Low Current	1500		UA
I_{PIH}	Input High Current	-500		UA
C_{PIN}	Input Capacitance		10	PF
C_{CLK}	PCI Clock Input Capacitance	5	12	PF
C_{IDSEL}	PCI Idsel Input Capacitance		8	PF

12.2.2 PCI Signal DC Specifications

Symbol	Parameter	Min	Max	Unit
V_{PIL}	Input Low Voltage	-0.5	0.3Vcc	V
V^{PIH}	Input High Voltage	0.5Vcc	Vcc + 0.5	V
V_{POL}	Output Low Voltage		0.1Vcc	V
V_{POH}	Output High Voltage	0.9Vcc		V
I_{PIL}	Input Low Current	1500		UA
I_{PIH}	Input High Current	-500		UA
C_{PIN}	Input Capacitance		10	PF
C_{CLK}	PCI Clock Input Capacitance	5	12	PF
C_{IDSEL}	PCI Idsel Input Capacitance		8	PF

12.2.3 Non-PCI Signal DC Specifications

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage		--	V
V_{IH}	Input High Voltage	-		V
V_{OL}	Output Low Voltage	0.4	0.4	V
V_{OH}	Output High Voltage	2.5	3.1	V
I_{OH}	Input Low Current	-4 [-8]	-4 [-8]	uA

12.3 SSTL_2 Class I Signals (DDR Memory Interface Only)

Symbol	Parameter	Min	Max	Units
IOL	Low Level Output Current	4 [8]	4 [8]	mA
IOH	High Level Output Current		16	mA
IIL	Low Level Input Current		2	uA
IIH	High Level Input Current		2	uA

Cin	Input Capacitance		20	pF

12.4 AC Specifications

Pin Name	Capacitive Load
PCIAD[31:0], PCICBEN[3:0], PCIPar, PCIFrameN,PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, PCIReqN, PCIGntN, PCIIntAN ,AGPPipeN, AGPRbfN, AGPSBA[7:0],	
All other outputs	

12.4.1 Clock Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{PCyc}	PCIClk Cycle Time	30	-	ns	
T_{PHigh}	PCIClk High Time	-11	-	ns	
T_{SLow}	PCIClk Low Time	-11	-	ns	
T_{MCyc}	MClkin Cycle Time		-	ns	
T_{MHigh}	MClkin High Time	-	-	ns	
T_{MLow}	MClkin Low Time	-	-	ns	
T_{SCyc}	SClkin Cycle Time		-	ns	
T_{SHigh}	SClkin High Time		-	ns	
T_{SLow}	SClkin Low Time		-	ns	
T_{DCyc}	DClk Cycle Time		3.3-	ns	
T_{DHigh}	DClk High Time	1.4	-	ns	
T_{DLow}	DClk Low Time	1.4	-	ns	

12.4.2 PCI Clock Referenced Input Timing

Parameter	T_{Su} Min	T_H Min	Units
PCIAD, PCICBEN	5.5	0	ns
PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, AGPSt0-2	6.0	0	
PCIGntN	6	0	ns
PCIRstN	5	0	ns

Note: PCIRstN is resynchronised internally. The timings given, when met, ensure that the reset is detected in the current cycle.

12.4.3 PCI-Referenced Output Timing

	T_{Val}		T_{On}		T_{Off}		
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
PCIAD[31::0], PCICBEN[3::0],		6 6					ns

PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN		5.5 5.5 5.5 5.5 5.5 5.5					ns
PCIReqN		5.5					ns
PCIIntAN		5.5					ns

Note: All signals are sampled on the rising edge of the clock. Each signal has a setup and hold aperture with respect to the rising clock edge, in which transitions are not allowed. Outside this aperture, signal values or transitions have no significance. Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

12.4.4 AGP Referenced Output Timing

As for PCI-Referenced Output Timing

12.4.5 MEMCKOUT Referenced Input and Output Timing

The **MV0Strobe** registers control the delay chain per strobe out or strobe in to configure for varying PCB layouts determines the Hold and Setup times. The MV1 strobe delay chain registers are identical to MV0 but apply to the second 128bit memory bus.

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13

Alerts and Errata

Alerts are part of 3Dlabs' commitment to providing comprehensive and useful information about chipset products. Alerts describe issues arising when the chip is used outside normal operating parameters and may be of interest to driver programmers.

13.1 ALERT001

13.1.1 Problem

When handling a page fault, the fault data is recovered from the MemoryPageControlFIFO with the **FaultID** in word 0, bit positions as follows:

0 – graphics process
1 – VGA
2 – Command
3 – Bypass
4 – Page handler
5 – Translation lookaside buffer
6 – Video 0
7 – Video 1

However the bitmask used to Suspend or Restart an addressing source has VGA as bit 2 and Command as bit 1.

13.1.2 Software Workaround

There are no functional implications if the programmer remembers to swap the Suspend mask *VGA* and *Command* bit positions.

13.2 P9ERN001

13.2.1 Problem

When using the **Restart** mask in operations such as Table Update Page DMA etc. where commands are sent to the memory controller's MemoryPageControlFifo, a **Suspend** mask must also be used. The **Suspend** mask must include reference to every currently suspended source.

13.2.2 Software Workaround

Use a Suspend mask as appropriate.

13.3 P9ERN002

13.3.1 Problem

If the circular buffer is filled (i.e. *WritePointer* is set equal to *ReadPointer*), then the *ReadPointer* and *Busy* flags do not get updated correctly.

13.3.2 Software Workaround

Do not completely fill the circular buffer - always leave at least 1 DWORD free. This also makes the software code easier as it doesn't have to worry about the buffer being full.

13.4 P9ERN003

13.4.1 Problem

If zero is written to the circular buffer the *Busy* flag is not updated correctly.

13.4.2 Software Workaround

Put a CommandID tag at the start of the circular buffer. i.e.

DWORD 0	CommandID_Tag
DWORD 1	ID
DWORD 2	First word of data.

This gives the host a way of tracking that the chip has started using the circular buffer and writes a 2 to the buffer *WritePointer* instead of 0, avoiding the problem entirely.

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