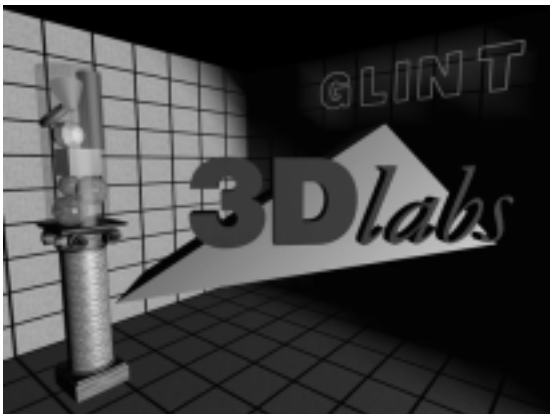
3Dlabs®

GLINT® Gamma

Hardware Reference Manual



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1. Contents

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2. Introduction

This document has been written as the reference for hardware and system designers who wish to develop hardware or software using the GLINT® Gamma geometry processor. A familiarity with the functionality of the GLINT rendering devices is assumed in this document.

2.1 What is the GLINT Gamma?

GLINT Gamma is a lighting and geometry processor, designed to break the 3D lighting and geometry bottleneck on PCs. GLINT Gamma implements the full 3D lighting and geometry pipeline for any 3Dlabs rendering device, e.g. GLINT 500TX, GLINT MX, etc. The lighting and geometry calculations in GLINT Gamma are general purpose and may be used to accelerate any 3D API, including OpenGL, Direct3D and Apple's QuickDraw 3D.

The GLINT Gamma contains two on-chip PCI Local Bus interfaces: the primary interface communicates with the host processor and the secondary interface communicates with other PCI devices such as GLINT 500TX, GLINT MX or an SVGA device.

GLINT Gamma functions as a AGP/PCI to PCI multi-function adapter. So, in addition to calculating the geometric information, the GLINT Gamma can act as a bridge between the PCI bus and multiple graphics devices. This capability may be used in various ways:

- Driving twin GLINT 500TX or GLINT MX devices for increased rendering speed;
- Driving a GLINT rendering device plus an SVGA device for 3D acceleration with on-board VGA.

2.2 The GLINT Family

The GLINT 500TX and MX graphics processors provide 100% OpenGL compliant rendering combined with state-of-the-art Windows acceleration. VRAM framebuffer support enables the high screen resolutions required by professional applications such as CAD and visualization.

The GLINT Gamma is completely compatible with GLINT 500TX and MX rendering devices providing a glueless hardware interface. The GLINT Gamma programming model is fully compatible with the other GLINT devices.

3. Functional Overview

The GLINT Gamma adds extra 3D graphics acceleration to the 3Dlabs' rendering devices by implementing the geometry, lighting, slope and setup calculations for 3D primitives in hardware. The processing required on the host is greatly reduced and much less data is passed from the host to the graphics subsystem.

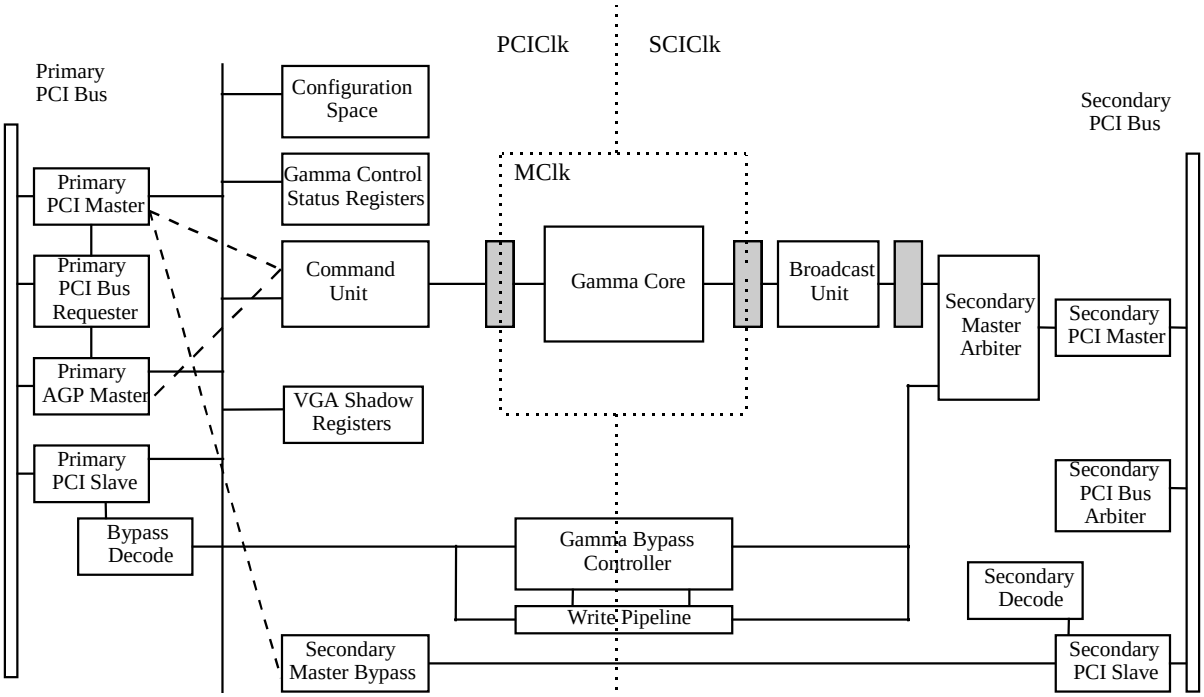

Figure 3-1 Functional Overview

For PCI accesses, if the access is for the Graphics Processor, it is directed towards the Command unit. If it is for a secondary target, the access is directed towards the Gamma Bypass Controller. The bus interface contains a number of PCI Configuration Registers and also various Control Status registers for the Gamma.

3.1 Reset Mode Control

A number of the parameters for the bus interface are set at reset time. There are two modes of reset configuration control in Gamma. The first mode is Delta compatible, the second uses a Serial EEPROM (Serial Mode) to allow greater configuration set-up control. In Delta compatible mode there are some hardwired mode pins. In both modes some of the reset state is configured using resistors connected to *configuration pins*. These pins normally form part of the Gamma operation, but are tri-state at reset. The state of *configuration pins* is sampled on the trailing edge of reset.

The resulting reset state is stored as Configuration bits within Gamma.

Configuration Bit	**Description**
PCI66MHzCapable	1 = 66MHz Capable
AGPCapable	1 = AGP Capable
SBACapable	1 = AGP Sideband Addressing Capable
BaseClassZero	1 = force PCI Base Class Code to be zero
PCIMinGnt[7:6]	top two bits of PCI Minimum Grant register
PCIMaxLat[7:6]	top two bits of PCI Maximum Latency register
ExtDevice1	1 = Enable external device 1
ExtDevice2	1 = Enable external device 2
ExtDevice3	1 = Enable external device 3
ExtVGAMode	0 = No VGA 1 = External device 1 is a VGA device 2 = External device 3 is a VGA device 3 = No VGA
VGANonAlias	See 2.6 VGA Support for definitions of the VGANonAlias
VGAControl	See 2.6 VGA Support for definitions of the VGA control bits
GlintEn1	1 = External Device 1 is a GLINT device 0 = External Device 1 is any other device
GlintEn2	1 = External Device 2 is a GLINT device 0 = External Device 2 is any other device

MultiGLINTAp	Multi GLINT aperture size control:
	if GlintEn1 = 1 and GlintEn2 = 1 then
	00 = 0M DISABLED
	01 = 16M
	10 = 32M
	11 = 64M
	else
	DISABLED

SubsystemVendorID[15:0]	Subsystem Vendor ID
SubsystemID[15:0]	Subsystem ID

Table 3-1 Gamma Configuration Bit Definitions

3.1.1 Delta compatible configuration mode

Delta compatible configuration mode is provided to allow a Gamma chip to be placed directly onto current Delta boards without any hardware changes. All new designs should use the Gamma serial configuration mode.

In Delta compatible mode, the configuration bits are loaded from mode and configuration pins, in exactly the same way as Delta. Some configuration bits are hard-coded and cannot be used in this mode of operation. To switch to Serial configuration mode the ExtFunc pins are set to 00b. This setting would never be used on any current Delta board design, so making the new mode backwards compatible with current Delta boards.

The configuration pins are listed in the tables below:

Mode Pin	Description	Mode
ExtFunc[1:0]	00b	Serial Configuration
	01b ExtDevice1 = 1 ExtDevice2 = 0 ExtDevice3 = 0	Delta Compatible
	10b ExtDevice1 = 0 ExtDevice2 = 1 ExtDevice3 = 0	Delta Compatible
	11b ExtDevice1 = 1 ExtDevice2 = 1 ExtDevice3 = 0	Delta Compatible

Table 3-2 External Function Enable Pins (Mode control for Gamma).

Mode Pin	Description
AGPSBA[0] (was ModeCtl[0])	1 = Report legacy PCI Base class BaseClassZero = 1b 0 = Report PCI 2.1 Base class BaseClassZero = 0b
AGPSBA[1] (was ModeCtl[1])	1 = PCIMaxLat[7:6] = 00b PCIMinGnt[7:6] = 11b 0 = PCIMaxLat[7:6] = 11b PCIMinGnt[7:6] = 11b
VGAEnable	1= External Device 1 is VGA device ExtVGAMode = 01b 0 = No VGA present ExtVGAMode = 00b Note: Delta compatibility mode only supports External Device 1 as VGA

Table 3-3 Delta compatible Mode Pins.

Configuration Pin	Description
GLINTInDis[0]	Target device 0 GLINT control Pull low (4K7) if GLINT GlintEn1 = 1 else Pull High (4K7) GlintEn1 = 0
GLINTInDis[1]	Target device 1 GLINT control Pull low (4K7) if GLINT GlintEn2 = 1 else Pull High (4K7) GlintEn2 = 0

Table 3-4 Delta compatible Configuration Pins

Configuration Bits	Value	Note
PCI66MHzCapable	0b	
AGPCapable	0b	
SBACapable	0b	
VGANonAlias	0b	
VGAControl	0000b	
SubsystemVendorID[15:0]	0000h	1
SubsystemID[15:0]	0000h	1

Table 3-5 Delta compatible Hard coded configuration bits.

Note 1: In Delta compatible mode the subsystem registers are Write-once, reset to 0000h.

3.1.2 Serial configuration mode

In serial configuration mode the Gamma configuration bits are set from configuration pins, and from a serial EEPROM. The EEPROM chosen for use with Gamma is the Xicor X84041-3 or X84041-2.7. For more information on this part please refer to the Xicor data sheet. Other serial EEPROMs may be usable if they are 100% compatible with the Xicor part.

Pin	Description
SerialCEN	Serial EEPROM Chip Enable
SerialOEN	Serial EEPROM Output Enable
SerialWEN	Serial EEPROM Write Enable
SerialData	Serial EEPROM Data bit

Table 3-6 Serial Mode Operation: EEPROM Pins.

Configuration Pin	Description
SerialData	Pull High (4k7) if external VGA target present else Pull Low (4k7)
SerialOEN:SerialWEN	Secondary PCI Bus Clock Control Set using 4k7 Pull-ups and pull-downs for following codes. 00b = SCIClk[0:3] = PCIClk 01b = SCIClk[0:3] = PCIClk 10b = SCIClk[0:3] = PCIClk/2 11b = SCIClk[0:3] = PCIClk/2
VGAEnable	In serial mode this pin is used to set the value of the 66MHz capable bit in the Configuration Status register. 0b = 66MHz capable bit not set 1b = 66MHz capable bit set

Table 3-7 Serial Mode Operation: Configuration Pins.

EEPROM Data Bit	Configuration Bits
0	**AGPCapable**
1	**SBACapable**
2	**BaseClassZero**
[4:3]	**PCIMinGnt[7:6]**
[6:5]	**PCIMaxLat[7:6]**
7	**ExtDevice1**
8	**ExtDevice2**
9	**ExtDevice3**
[11:10]	**ExtVGAMode**
12	**VGANonAlias**
[16:13]	**VGAControl**
17	**GlintEn1**
18	**GlintEn2**
[20:19]	**MultiGLINTAp**[1:0]
[47:32]	**SubsystemVendorID**[15:0]
[63:48]	**SubsystemID**[15:0]

Table 3-8 Serial Mode Operation: EEPROM Bit Definitions

Note That the ExtVGAMode bits are qualified by the configuration state on the SerialData pin. If the hardware configuration is set such that VGA target is defined to be absent, the EEPROM bits will be ignored, and ExtVGAMode will be set to 00b.

Bits 0 to 20 of the Gamma configuration are visible in the **ChipConfig** register. This register can be read back over the PCI bus. Some of the bits are writeable and may be modified by the host processor if required — see **ChipConfig** register specification in this

document. The PCI66MHzCapable, and subsystem Vendor ID, and subsystem ID are visible only in the appropriate PCI configuration register.

3.2 Gamma multi-function support

The GLINT Gamma includes circuitry to allow multiple single function PCI devices attached to its secondary bus to look like a single PCI multi-function device. To achieve this the Gamma device adjusts the results of certain secondary device configuration space accesses.

3.2.1 PCI Multi-function indication

To indicate a multi-function device all functions must return Bit 7 of the Header Type register set to a '1'. This bit is set by Gamma during a read of a secondary device Header Type register.

3.2.2 PCI 66MHz capable

To indicate 66MHz capability all functions must return Bit 5 of the Header Type register set to a '1'. This bit is set by Gamma during a read of a secondary device Status register if the Gamma PCI66MHzCapable configuration bit is set.

3.2.3 Force Legacy Class Codes

If BaseClassZero is set, GLINT Gamma will override the PCI base and sub class reported by devices on the secondary PCI bus. GLINT Gamma and any GLINT rendering device on the secondary PCI bus will have 00h reported as their PCI base class and 00h reported as their PCI sub-class. Any VGA device on the secondary PCI bus will have 00h reported as its PCI base class and 01h reported as its PCI sub-class.

3.3 PCI Address Regions

The Gamma PCI interface implements four PCI Address Regions, shown in Table 2-2.

The standard VGA-compatible Memory and I/O Space addresses are decoded when the Gamma has been suitably configured. These addresses do not form a single contiguous region, but are mentioned in the table for completeness.

Region	Address Space	Bytes	Description	Comments
Config	Configuration	256	PCI Configuration	PCI special
Zero	Memory	128K	Control Registers	relocatable
Two	Memory	Note 1.	Multi-GLINT aperture	relocatable
ROM	Memory	0K	Expansion ROM	No ROM
VGA	Memory & I/O	—	VGA Addresses	Note 2.

Table 3-9 Gamma PCI Address Regions.

Note 1: Multi-GLINT aperture size is variable. Size is set by EEPROM configuration bits at reset.

Note 2: VGA Addresses are decoded by Gamma when then VGA Present configuration bit is set to be processed by VGA chip on the secondary Bus.

3.4 PCI Configuration Space

The PCI Configuration Space provides a set of 'hooks' which satisfies the needs of current and anticipated system configuration mechanisms. The configuration registers are accessed and modified by the use of PCI Configuration Read and Write commands, and will normally be initialized by BIOS or similar low-level code at system power-up and reset.

Sixty four bytes of the Configuration Registers are predefined within the PCI Specification and are supported by the Gamma. These are defined in Section 28.2 of this document, and are all implemented within the PCI Bus Interface. Registers are provided for device identification, PCI control and status, and as base address registers for the relocatable memory regions. Registers are also provided to allow the reading and writing of the Gamma configuration serial EEPROM.

3.5 Gamma Control Registers

The Gamma Region Zero is a 128KByte region containing the control registers, and ports to and from the graphics processor. The control space is mapped in twice within the 128KByte region. In Delta compatible mode the second 64K the registers are mapped to be byte swapped for big endian hosts. For Dual GLINT systems when in Serial mode, Region zero can be configured to allow both GLINT control regions to be visible, the second GLINT being in the second 64K of this region.

A number of Control Status Registers are implemented within the PCI Bus Interface, including registers for interrupt and error handling, reporting graphics processor input FIFO status, and DMA control. All other registers on the Target GLINT are visible through the Gamma Control register space to allow for minimum software changes in supporting a Gamma Device.

3.6 VGA Support

The bus interface can be configured to respond to the standard VGA-compatible Memory and I/O Space addresses configuring ExtVGAMode. The interface will then respond to Memory addresses A0000h through BFFFFh.

Gamma can be configured to allow accesses to a number of I/O addresses to allow different types of VGA device to be used on the secondary bus.

3.6.1 VGA Aliasing

Aliases of the VGA I/O addresses will be decoded as defined below:

Decode Type	Address operation	VGANonAlias	VGAControl(3)
10 Bit aliasing	Bits 31-10 are ignored	0b	0b
partial aliasing	Bits 31-16 must be 0000h Bits 15-10 are ignored	0b	1b
Full decode	Bits 31-10 must be 000000h	1b	xb

Table 3-10 VGA Address Aliasing.

3.6.2 VGA decode control

The VGA address ranges to be decoded can be configured in Serial mode, as set out in the table below:

I/O Address range	Type	Configuration Control
3B0h - 3BBh, 3C0h - 3DFh	VGA	VGAControl(0) 1 = disabled 0 = enabled
2E8h, 2EAh - 2EFh	XGA	VGAControl(1) 1 = disabled 0 = enabled
102h	Special	VGAControl(2) 1 = disabled 0 = enabled

Table 3-11 VGA Address Regions.

In Delta compatible mode VGAControl(3-0) is set to 0h and VGANonAlias to set to 0b. This enables the decoding of all the I/O address ranges with full 10 bit address aliasing to make Gamma fully compatible with Delta in this mode.

3.7 VGA register shadowing

The GLINT Gamma shadows a number of the VGA I/O control registers to allow it to work transparently in all systems. These shadow registers ensure that Gamma only responds to the correct VGA memory addresses, and I/O addresses for the current VGA set-up.

This shadowing allows a Gamma to co-exist with a monochrome adapter which is something that was not possible with a GLINT Delta.

3.8 Multi-GLINT aperture

The Gamma Multi-GLINT aperture supports two GLINTS with non-shared framebuffers. Addresses into the aperture consist of a Y and an X component. To simplify calculations the X Span into the aperture is always a power of 2. The size of the Gamma aperture is set at reset.

The Aperture Address generator multiplies the Y address by the GLINT X span and then adds the result to the X address.

GLINT X spans supported are 320, 512, 640, 800, 1024, 1152, 1280, 1600, 1920

In 8 bits, 16 bits and 32 bits per pixel.

The address generator can hand GLINT framebuffer aperture sizes of 4M, 8M, 16M, and 32 Mbytes.

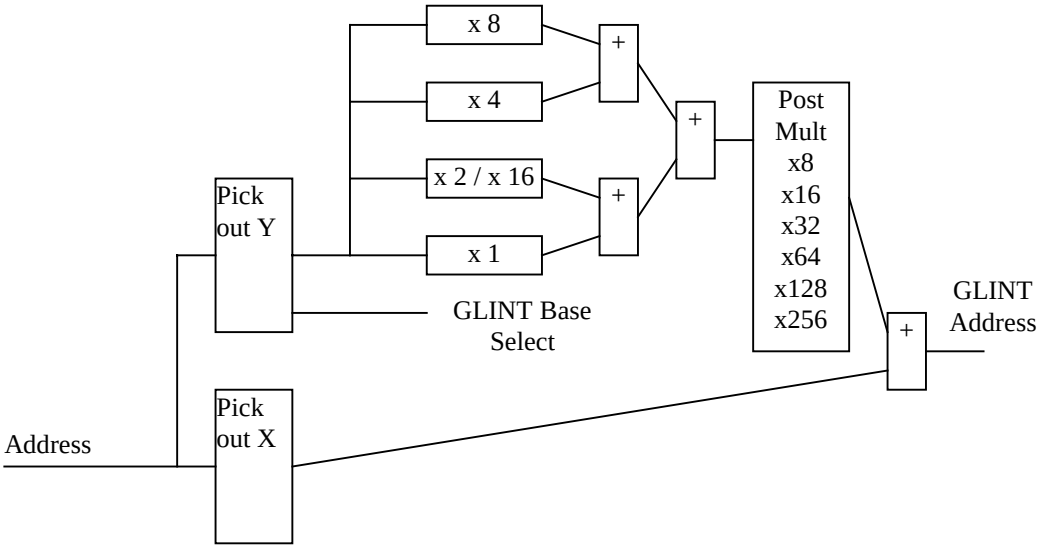

Figure 3-2 Address generation circuitry

Note: The Y address used in forming the GLINT address is ½ of the Input Y address, and the bottom bit of the Input Y address is used to select which GLINT Base address to use in the framebuffer access.

4. PCI Configuration Region

The PCI Configuration Region provides at set of 'hooks' which satisfies the needs of current and anticipated system configuration mechanisms. The configuration registers are accessed and modified by the use of Configuration Read and Write commands.

As GLINT Gamma is a multi-function device, the configuration space is split into eight 256 bytes blocks. GLINT Gamma has one internal function and up to 3 external functions.

GLINT Gamma will only respond to configuration space accesses for which devices exist. In Delta mode, hardware mode pins are used to indicate which of the external functions are populated in the system.

4.1 Internal Function Configuration Registers

64 bytes of the Configuration registers are predefined within the PCI Specification and are supported by GLINT Gamma. The remaining 192 Bytes are device specific AGP capabilities are configured in a number of registers in this device specific area. All other registers are unused by GLINT Gamma, returning the value zero.

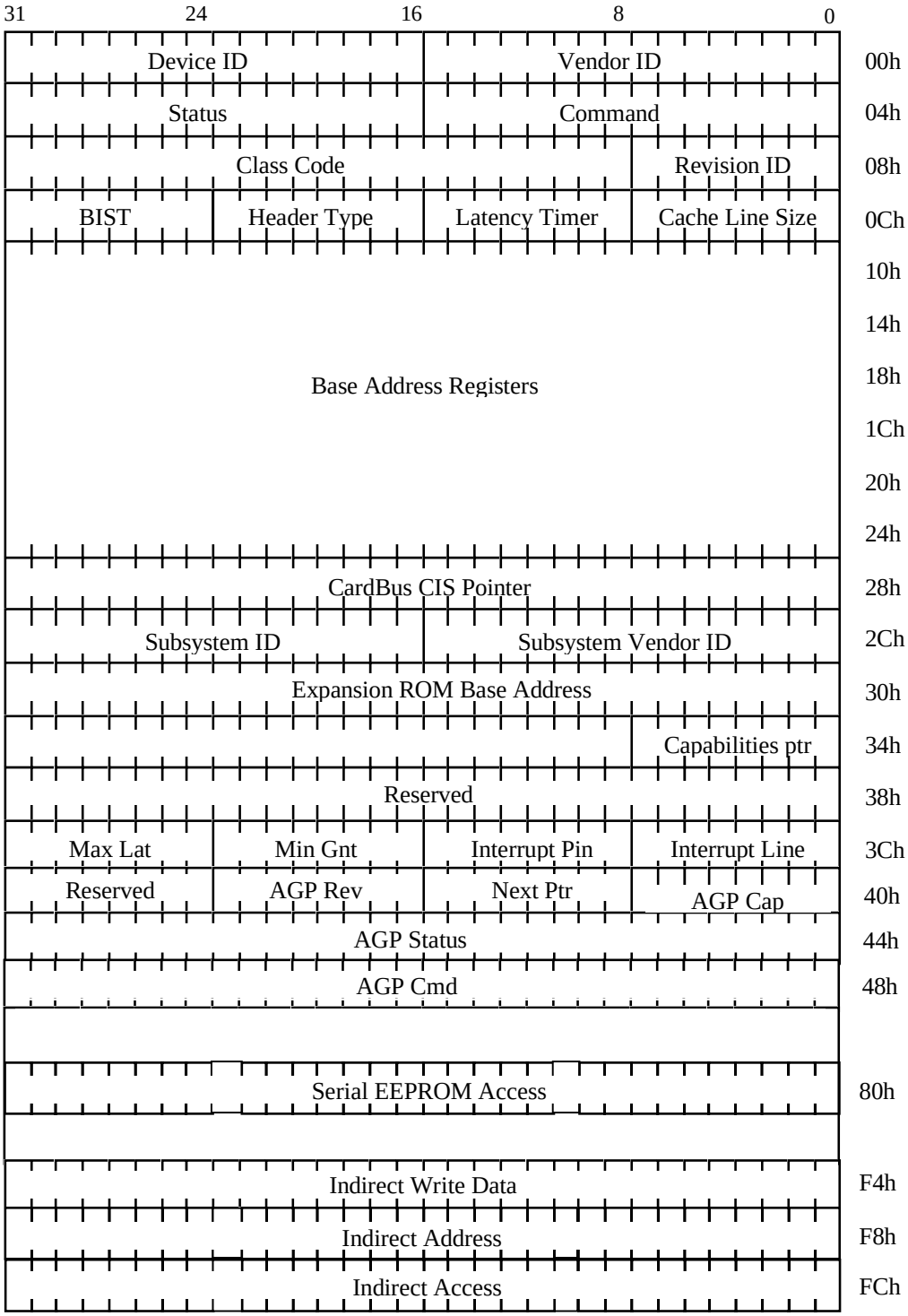

Figure 4-1 Configuration Region.

4.2 Device Identification

4.2.1 Vendor ID

Vendor identification number.

CFGVendorId

Region:	Config	Read Only	
Offset:	00h	**Reset Value:**	3D3Dh

Bits 0-15 3D3Dh
3Dlabs company code

4.2.2 Device ID

Device identification number.

CFGDeviceId

Region:	Config	Read Only	
Offset:	02h	**Reset Value:**	0008h

Bits 16-31 0008h
GLINT Gamma Device number

4.2.3 Revision ID

Revision identification number.

CFGRevisionId

Region:	Config	Read Only	
Offset:	08h	**Reset Value:**	Revision Number

The revision ID register returns the following code:

Bits 0-7 Revision
01h = Revision R01

4.2.4 Class Code Register

CFGClassCode

Region:	Config	Read Only	
Offset:	09h	**Reset Value:**	0B4000h

Bits 8-15 00h
Device class

Bits 16-23 40h
Sub class. PCI Definition: Co-Processor (unknown type)

Bits 24-31 0Bh
Base class. PCI Definition: Processor.

4.2.5 Header Type

CFGHeaderType

Region:	Config	Read Only	
Offset:	0Eh	**Reset Value:**	80h

Bits 16-23 80h
Header Type. PCI Definition: Multi- function device

4.3 Device Control

4.3.1 Command Register

The command register controls the ability of a device to generate and respond to PCI cycles. Writing zero to this register disconnects the device from the PCI for all except configuration accesses. All necessary bits within the command register are supported for the functionality contained in GLINT Gamma.

CFGCommand

Region: Config Read/Write

Offset: 04h **Reset Value:** 0000h

Bit 0 I/O access enable (Read Only)
0 = GLINT Gamma has no I/O space regions

Bit 1 Memory access enable
0 = Disable memory space accesses. (RESET)
1 = Enable memory space accesses

Bit 2 Master enable
0 = Disable master accesses. (RESET)
1 = Enable master accesses

Bit 3 Special Cycle access enable (Read Only)
0 = GLINT Gamma never responds to special cycle accesses.

Bit 4 Memory Write and Invalidate enable (Read Only)
0 = GLINT Gamma master never issues Memory Write and Invalidate accesses.

Bit 5 VGA palette snoop enable (Read Only)
0 = GLINT Gamma is not a VGA device.

Bit 6 Parity error report enable (Read Only)
0 = GLINT Gamma does not report parity errors.

Bit 7 Address/Data stepping enable (Read Only)
0 = GLINT Gamma does not do stepping.

Bit 8 SERR driver enable (Read Only)
0 = GLINT Gamma does not report parity errors.

Bit 9 Master Fast back-to-back enable (Read Only)
0 = The GLINT Gamma master does not implement fast back-to-back accesses.

Bits 10-15 Reserved
000000b

4.4 Device Status

4.4.1 Status Register

The Status Register is used to record status information for PCI related events. The definition for each bit is given below.

Reads to this register behave normally. Writes function differently in that bits can be reset but not set. A bit is reset whenever the register is written and the data in the corresponding bit location is a 1.

CFGStatus

Region: Config Read Only

Offset: 06h **Reset Value:** 00h

Bits 16-19 Reserved (Read Only)
0.0000b.

Bits 20 Cap_List (Read Only)
Configured by AGPCapable.
0 = no additional capabilities over PCI2.1
1 = AGP Capability

Bit 21 66 MHz Capable (Read Only)
Configured by 66MHz capable configuration pin
0 = Gamma is 33 MHz capable only.
1 = Gamma is 66 MHz capable (in an AGP system)

Bit 22 UDF Supported (Read Only)
0 = Gamma does not support user-definable configurations.

Bit 23 Fast Back-to-Back Capable (Read Only)
1 = Gamma can accept fast back-to-back PCI transactions.

Bit 24 Data Parity Error Detected (Read Only)
0 = Parity checking not implemented on the Gamma.

Bits 25-26 DEVSEL Timing (Read Only)
01b = The Gamma asserts DEVSEL# at medium speed.

Bit 27 Signaled Target Abort (Read Only)
0 = The Gamma never signals Target-Abort.

Bit 28 Received Target Abort
This bit is set by the Gamma bus master whenever its transaction is terminated with Target-Abort.

Bit 29 Received Master Abort
This bit is set by the Gamma bus master whenever its transaction is terminated with Master-Abort.

Bit 30 Signaled System Error (Read Only)
0 = The Gamma never asserts a system error.

Bit 31 Detected Parity Error (Read Only)
0 = Parity checking is not implemented by the Gamma.

4.5 Miscellaneous Functions

4.5.1 BIST

Optional register used for control and status of BIST (built-in self-test).

CFGBist

Region:	Config	Read Only	
Offset:	0Fh	**Reset Value:**	00h

Bits 24-31 BIST (Read only)
00h. BIST unsupported by GLINT Gamma over the PCI interface.

4.5.2 Latency Timer

This register specifies, in PCI bus clocks, the value of the Latency Timer for this PCI bus master.

CFGLatTimer

Region:	Config	Read/Write	
Offset:	**0Dh**	**Reset Value:**	00h

Bits 8-15 Latency Timer Count
Sets the maximum number of PCI clock cycles for master burst accesses.

4.5.3 Cache Line Size

This register specifies the cache line size in units of 32 bit words. It is only implemented for masters which use the 'Memory write and invalidate' command. GLINT Gamma does not use this command.

CFGCacheLine

Region:	Config	Read Only	
Offset:	**0Ch**	**Reset Value:**	00h

Bits 0-7 Cache Line Size
00h. Cache line size unsupported.

4.5.4 Maximum Latency

This register specifies how often the PCI device needs to gain access to the PCI bus. Two EEPROM bits are used to set the top two bits of this register, and the lower bits are always zero. (Possible register values are thus limited to 00h, 40h, 80h, and C0h.)

CFGMaxLat

Region:	Config	Read Only	
Offset:	3Fh	**Reset Value:**	80h

Bits 0-5	Maximum Latency **00.0000b**
Bit 6	Maximum Latency[6] **Set by the bit PCIMaxLat[0]**
Bit 7	Maximum Latency[7] **Set by the bit PCIMaxLat[1]**

4.5.5 Minimum Grant

This register specifies how long a burst period the PCI device needs. Two EEPROM bits are used to set the top two bits of this register, and the lower bits are always zero. (Possible register values are thus limited to 00h, 40h, 80h, and C0h.)

CFGMinGrant

Region:	Config	Read Only	
Offset:	3Eh	**Reset Value:**	Configured

Bits 0-5	Minimum Grant[5:0] **00.0000b**
Bit 6	Minimum Grant[6] **Set by the bit PCIMinGnt[0]**
Bit 7	Minimum Grant[7] **Set by the bit PCIMinGnt[1]**

4.5.6 Interrupt Pin

The Interrupt Pin register tells the BIOS which interrupt line GLINT Gamma uses.

CFGIntPin

Region:	Config	Read Only	
Offset:	3Dh	**Reset Value:**	001h

Bits 8-15 Interrupt Pin
01h GLINT Gamma uses Interrupt pin A

4.5.7 Interrupt Line

The Interrupt Line register is an 8 bit register used to communicate interrupt line routing information.

CFGIntLine

Region:	Config	Read/Write	
Offset:	3Ch	**Reset Value:**	00h

Bits 0-7 Interrupt Line

4.5.8 CardBus CIS Pointer

This optional register is not implemented by the Gamma.

CFGCardBus

Region:	Config	Read Only	
Offset:	028h	**Reset Value:**	0000.0000h

Bits 0-31 CardBus Pointer
0000.0000h = Not implemented

4.5.9 Subsystem Vendor ID

This register identifies the vendor of the add-in board on which the Gamma device resides.

In Delta Compatible reset mode it has a reset value of zero, and can only be written to once; all subsequent writes are discarded. Both bytes of this register should be initialized by the Gamma BIOS after a reset.

In Serial Mode the Subsystem ID is read only and is loaded from the Serial EEPROM.

CFGSubsystemVendorId

Region:	Config	Read Only / Write Once	
Offset:	02Ch	**Reset Value:**	configured

Bits 0-15 Subsystem Vendor ID

4.5.10 Subsystem ID

This register is used to identify the add-in board on which the Gamma device resides.

In Delta Compatible reset mode it has a reset value of zero, and can only be written to once; all subsequent writes are discarded. Both bytes of this register should be initialized by the Gamma BIOS after a reset.

In Serial Mode the Subsystem ID is read only and is loaded from the Serial EEPROM.

CFGSubsystemId

Region:	Config	Read Only / Write Once	
Offset:	02Eh	**Reset Value:**	configured

Bits 16-31 Subsystem ID

4.5.11 Capabilities Pointer

The Capabilities Pointer register is an eight bit register used to provide an offset into the configuration space for the first item in a capabilities list. It is used by the Gamma device in an AGP system to point to the AGP capability registers.

CFGCapPtr

Region:	Config	Read Only	
Offset:	34h	**Reset Value:**	configured

Bits 0-7 Capability Ptr
Configured by AGPCapable
00h. when AGPCapable = 0
40h when AGPCapable = 1

4.6 AGP Registers

4.6.1 Capability ID

This register specifies that the device has AGP capability

CFGCapID

Region:	Config	Read Only	
Offset:	40h	**Reset Value:**	configured

Bit 0-7 Capability ID
Configured by AGPCapable
00h if AGPCapable = 0
02h if AGPCapable = 1

4.6.2 Next Ptr

This register specifies the device has no next capability item.

CFGNextPtr

Region:	Config	Read Only	
Offset:	41h	**Reset Value:**	00h

Bit 8-15 Next Ptr
00h = no further capabilities in list

4.6.3 AGP Revision

This register specifies the revision of the AGP spec the device conforms to.

CFGAGPRev

Region:	Config	Read Only	
Offset:	42h	**Reset Value:**	configured

Bit 16-19 Minor Rev
Configured by AGPCapable
0h if AGPCapable = 0
0h if AGPCapable = 1

Bit 20-23 Major Rev
Configured at reset by AGPCapable
00h if AGPCapable = 0
01h if AGPCapable = 1

4.6.4 AGP status

This register describes the AGP capabilities of the device.

CFGAGPStatus

Region:	Config	Read Only	
Offset:	44h	**Reset Value:**	configured

Bit 0-1	Rate **Configured by AGPCapable** **0h if AGPCapable = 0** **1h if AGPCapable = 1**
Bit 2-8	Reserved
Bit 9	SBA **Configured by AGPCapable and SBACapable** **0 if AGPCapable = 0 or SBACapable = 1** **1 if AGPCapable = 1 and SBACapable =1**
Bit 10-23	Reserved
Bit 24-31	RQ **Maximum number of AGP requests supported** **Configured by AGPCapable** **00h if AGPCapable = 0** **1Fh if AGPCapable = 1**

4.6.5 AGP Command

This register specifies the revision of the AGP spec the device conforms to.

CFGAGPCommand

Region:	Config	Read/Write	
Offset:	48h	**Reset Value:**	00000000h

Bit 0-1	DataRate **0 = AGP disabled** **1 = 1X transfer rate**
Bit 2-7	Reserved
Bit 8	AGPEnable **0 = AGP Mastering Disabled** **1 = AGP Mastering Enabled**
Bit 9	SBAEnable **0 = sideband Addressing Disabled** **1 = sideband Addressing Enabled**
Bit 10-23	Reserved
Bit 24-31	RQDepth **Maximum number of AGP requests which can be queued**

4.7 Serial EEPROM Access

4.7.1 Serial EEPROM Access Register

This register is used to access the Configuration Serial EEPROM. Reads and writes of the EEPROM can be initiated by setting up the correct stream of read and write accesses to the bottom bit of this register. For details of the read / write patterns to be used, see the XICOR data sheet on the X84041 operation. Note the EEPROM is also programmable and readable through a region 0 register.

CFGSerialEnable

Region:	Config	Read/Write	
Offset:	80h	**Reset Value:**	00000000h

Bit 0	Serial EEPROM Data Pin
Bits 1-31	Reserved

4.8 Indirect Region 0 access though configuration space

Three configuration registers are provided to allow indirect accesses to region 0 through configuration space accesses. The offset to the region that is to be accessed is loaded into the Indirect Address register. For a write access, the data to be written is loaded into the Indirect Write Data register. The write access is then initiated by writing to the Indirect Access register. The data value written into the Indirect Access register is ignored. For a read access a read of the Indirect Access register returns the values at the current Indirect Address offset.

4.8.1 Indirect Write Data

The Indirect Write Data register holds data value which will be written with Indirect write access.

CFGIndirectWriteData

Region:	Config	Read/Write	
Offset:	F4h	**Reset Value:**	00000000h

Bits 0-31	Indirect write data

4.8.2 Indirect Address

The Indirect Address register holds the address offset for Indirect accesses.

CFGIndirectAddress

Region:	Config	Read/Write	
Offset:	F8h	**Reset Value:**	00000000h

Bit 0-22	Address offset within region
Bit 23-27	Reserved
Bit 28-31	Base Address select **0 = Base Address 0** **1 to 7 = Reserved**

4.8.3 Indirect Access

Accessing the Indirect access register initiates the indirect region 0 access.

CFGIndirectAccess

Region:	Config	Read/Write	
Offset:	FCh	**Reset Value:**	00000000h

Bits 0-31 Writes: Data value ignored
Reads: Indirect access read data value

Bit 0-31 Indirect data

4.9 Base Addresses

The base address registers allow the boot software to relocate PCI devices in the address spaces. At system power-up device independent software must be able to determine which devices are present, build a consistent address map, and determine if a device has an expansion ROM. All undefined Base address registers are read only and return the value 0000.0000h. GLINT Gamma does not have an expansion ROM and so the expansion ROM base address is also read only, returning the value 0000.0000h.

4.9.1 Base Address 0 Register

The Base Address 0 Register contains the GLINT Gamma control space offset. The control registers are in memory space. They are not prefetchable and can be located anywhere in 32 bit address space.

CFGBaseAddr0

Region:	Config	Read/Write	
Offset:	10h	**Reset Value:**	0000.0000h

Bits 0-3 Address Type Read Only
0h Memory Space, not prefetchable, in 32 bit address space

Bits 4-16 Size indication Read Only
000h Indicates that the control registers must be mapped into 128 KBytes.

Bits 17-31 Base offset
Loaded at boot time to set offset of the control register space.

4.9.2 Base Address 2 Register

The Base Address 2 Register contains the base address of the Gamma Multi GLINT aperture, and defines the size and type of this region.

CFGBaseAddr2

Region:	Config	Read/Write	
Offset:	18h	**Reset Value:**	0000.0000h

Bits 0-3 Address Type Read Only
0h Memory Space, not prefetchable, in 32 bit address space

Bits 4-xx Size Indication (Read Only)
These bits are zero, Region size set at configuration to 16M, 32M, 64M or disabled

Bits 31-xx Base Address
Loaded at boot time to set offset of the Multi GLINT aperture

4.10 Gamma Functions

As a PCI multi-function device Gamma can have up to 4 functions. If Gamma is configured as AGP capable the Gamma function is always the first function. This is because the AGP capable function is always assumed to be the first function in a multi-function device. When not AGP capable the order of the functions is affected by the **ExtVGAMode** mode bits.

PCI	AGP / No VGA	Device 1 VGA	Device 3 VGA
0	Gamma Function	External Device 1	External Device 3
1	External Device 1	Gamma Function	Gamma Function
2	External Device 2	External Device 2	External Device 1
3	External Device 3	External Device 3	External Device 2
4			
5			
6			
7			

Table 4-1 Gamma PCI Address Regions.

5. Region 0 - Control Registers

5.1 Region 0 Address Map

The Gamma Region Zero is a 128KByte region containing the control registers, and ports to and from the graphics processor. The control space is mapped in twice within the 128KByte region. In Delta compatible mode the second 64K the registers are mapped to be byte swapped for big endian hosts. Region zero can be configured in other ways for dual GLINT systems. See the **CSRAperture** register specification for details.

A large part of this region is not actually Gamma registers, but actually the registers of the Glint Target device sitting below Gamma. This allows Gamma to be a transparent as possible to the driver software.

Address Range	Region Select	Register Location
0000.0000 -> 0000.0FFF	Control Status	Gamma / Target
0000.1000 -> 0000.1FFF	Target Control	Target
0000.2000 -> 0000.2FFF	GP FIFO Access	Gamma / Target
0000.3000 -> 0000.7FFF	Target Control	Target
0000.8000 -> 0000.FFFF	GP Registers	Gamma / Target
0001.0000 -> 0001.0FFF	Control Status	Gamma / Target
0001.1000 -> 0001.1FFF	Target Control	Target
0001.2000 -> 0001.2FFF	GP FIFO Access	Gamma / Target
0001.3000 -> 0001.7FFF	Target Control	Target
0001.8000 -> 0001.FFFF	GP Registers	Gamma / Target

Table 5-1 Region Zero Address Map.

5.2 Control Status Registers

The GLINT Gamma Control Status Register region is split into two sections. The lower section allows direct access to the control status registers of the GLINT rendering device connected to GLINT Gamma. Some of the registers in this section are actually GLINT Gamma registers which are shadowing GLINT 500TX or MX operations for software compatibility with systems without GLINT Gamma.

The upper section has additional GLINT Gamma registers which are documented below. Refer to the appropriate GLINT 500TX or MX Hardware Reference Manual for details on registers in the lower region.

Writes to any reserved or undefined registers in the Control Status area will be discarded; reads will return the value zero.

For information on the target register definitions please refer to the appropriate target Hardware Reference Manual.

Address Range	Register	Register Location	Notes
0000.0000	ResetStatus	Gamma/Target	1
0000.0008	IntEnable	Target	2
0000.0010	IntFlags	Target	2
0000.0018	InFIFOSpace	Gamma	
0000.0020	OutFIFOWords	Target	2
0000.0028	DMAAddress	Gamma	
0000.0030	DMACount	Gamma	
0000.0038	ErrorFlags	Target	2
0000.0040	VClkCtl	Target	2
0000.0048	TestRegister	Target	2
0000.0050 - 0000.0058	Target Registers	Target	2
0000.0060	DMAControl	Gamma	
0000.0068	FIFODiscon	Target	2
0000.0070 - 0000.07F8	Target Registers	Target	2
0000.0080	OutDMA	Gamma	
0000.0088	OutDMACount	Gamma	
0000.0090 - 0000.03F8	Target Registers	Target	2
0000.0400 - 0000.07F8	Target Registers	Target	3
0000.0800	GResetStatus	Gamma	
0000.0808	GIntEnable	Gamma	
0000.0810	GIntFlags	Gamma	
0000.0818 - 0000.0830	Reserved	Gamma	
0000.0838	GErrorFlags	Gamma	
0000.0840	Reserved	Gamma	
0000.0848	GTestRegister	Gamma	
0000.0850 - 000.0860	Reserved	Gamma	
0000.0868	GFIFODis	Gamma	
0000.0870	GChipConfig	Gamma	
0000.0878	GCSRAperture	Gamma	
0000.0880 - 0000.0BF8	Reserved	Gamma	
0000.0C00	PageTableAddr	Gamma	
0000.0C08	PageTableLength	Gamma	
0000.0C10	Reserved	Gamma	
0000.0C18	Reserved	Gamma	
0000.0C20	Reserved	Gamma	
0000.0C28	Reserved	Gamma	
0000.0C30	Reserved	Gamma	
0000.0C38	DelayTimer	Gamma	
0000.0C40	CommandMode	Gamma	

0000.0C48	CommandIntEnable	Gamma	
0000.0C50	CommandIntFlags	Gamma	
0000.0C58	CommandErrorFlags	Gamma	
0000.0C60	CommandStatus	Gamma	
0000.0C68	CommandFaultingAddr	Gamma	
0000.0C70	VertexFaultingAddr	Gamma	
0000.0C78	Reserved	Gamma	
0000.0C80	Reserved	Gamma	
0000.0C88	WriteFaultingAddr	Gamma	
0000.0C90	Reserved	Gamma	
0000.0C98	FeedbackSelectCount	Gamma	
0000.0CA0	Reserved	Gamma	
0000.0CA8	Reserved	Gamma	
0000.0CB0	Reserved	Gamma	
0000.0CB8	GammaProcessorMode	Gamma	
0000.0CC0 - 0000.0CF8	Reserved	Gamma	
0000.0D00	VGAShadow	Gamma	
0000.0D08	MultiGLINTAperture	Gamma	
0000.0D10	MultiGLINT1	Gamma	
0000.0D18	MultiGLINT2	Gamma	
0000.0D20 - 0000.0EF8	Reserved	Gamma	
0000.0F00	SerialAccess	Gamma	
0000.0F08 - 0000.0FF8	Reserved	Gamma	

Table 5-2 Control Status Register Address Map.

Note 1: Writing to this register Resets both the Target device and Gamma. The access is sent to the target and snooped by Gamma

Note2: The specification for other Target Registers can be found in the appropriate Hardware Reference Manual

Note 3: The address offset range 0400h - 07F8h is passed through to the target device to allow visibility of the GLINT registers overlaid by Gamma registers. This is possible because not all address bits are used in the register space decode of GLINT chips.

5.2.1 Reset Status Register

Writing to the reset status register forces a software reset of the GLINT Gamma Graphics Core. The software reset does not reset the GLINT Gamma primary PCI interface. It is provided for software diagnostics in case an incorrect register set up locks up the GLINT Gamma internal GC.

The software reset takes a number of cycles and the GC must not be used during the reset. A flag in the register is provided which shows that the software reset is still in progress.

For more information on the operation of the GLINT Gamma at reset. Various mode pins are sampled at reset, these pins are described in section 2.1.

DResetStatus

Region:	Zero	Read/Write	
Offset:	00h	**Reset Value:**	0000.0000h

Bits 0-30 Reserved

Bit 31 Software Reset Flag

0 = GLINT Gamma is ready for use

1 = GLINT Gamma is being reset and must not be used

5.2.2 Input FIFO Space Register

The Input FIFO Space register shows the number of words that can currently be written to the input FIFO. This register can be read at any time.

InFIFOSpace

Region:	Zero	Read Only	
Offset:	18h	**Reset Value:**	0000.0021h

Bits 0-31 Input FIFO Space

The number of empty words in the input FIFO. This number of words can be written before checking "InFIFOSpace" again.

5.2.3 DMA Start Address

When using the legacy DMA controller to load the graphics processor, the DMA Start Address register should be loaded with the PCI address of the first word in the buffer to be transferred. In Queued DMA mode writes to this register are ignored.

Writing to the DMA Start Address register loads the address into the DMA address counter. Once a DMA has been initiated, the next DMA start address may be loaded. A read of this register returns the last start value loaded even if the DMA is already underway.

DMAAddress

Region:	Zero	Read/Write	
Offset:	28h	**Reset Value:**	0000.0000h

Bits 0-31 DMA Start Address
PCI start address for PCI master read transfer to the graphics processor core.

5.2.4 DMA Count

When using the legacy DMA controller to load the graphics processor, the DMA Count register should be loaded with the number of words to be transferred in the DMA operation. In Queued DMA mode writes to this register are ignored.

The action of loading a word greater than zero initiates the DMA operation. The value read back from this register indicates the current number of words left to be transferred. Writes to this register will be ignored if a DMA is in progress, but can be read at any time.

DMACount

Region:	Zero	Read/Write	
Offset:	30h	**Reset Value:**	0000.0000h

Bits 0-23 DMA Count
Number of words to be transferred in the DMA operation

Bits 24-31 Reserved

5.2.5 DMA Control Register

The DMA control register sets up the data transfer modes for the DMA controllers. Data transfer can be set to byte swapped for big endian hosts.

DMAControl

Region:	Zero	Read/Write	
Offset:	60h	**Reset Value:**	0000.0000h

Bit 0 InDMA Byte Swap Control
This field should only be changed when the InDMA controller is idle.
0 = Standard.
1 = Byte Swapped.

Bit 1 InDMA using AGP
0 = DMA uses PCI Master
1 = DMA uses AGP Master.

Bit 2 InDMA Data Throttle
0 = use AGP RBF# and IRDY# to throttle data.
1 = Only request data when space is available

Bit 3 AGP Long Read Disable
0 = AGP Long Read Requests may be generated.
1 = AGP Long Read Requests disabled.

Bit 4 OutDMA Byte Swap Control
This field should only be changed when the OutDMA controller is idle.
0 = Standard.
1 = Byte Swapped.

Bit 5 AGP Data Throttle
Applies to all AGP transfers
0 = Control data flow using bus protocols.
1 = Throttle Data requests based on FIFO space.

Bit 6 AGP High Priority
Applies to all AGP transferees
0 = Use AGP low priority reads.
1 = Use AGP high priority reads.

Bits 7-31 Reserved

5.2.6 OutDMA Start Address

When using the Out DMA controller to upload the graphics processor output FIFO, the Out DMA Start Address register should be loaded with the PCI address where the first word of the upload data is to be transferred.

Writing to the OutDMA Start Address register loads the address into the OutDMA address counter. Once a DMA has been initiated, the next DMA start address may be loaded. A read of this register returns the last start value loaded even if the DMA is already underway.

OutDMAAddress

Region:	Zero	Read/Write	
Offset:	80h	**Reset Value:**	0000.0000h

Bits 0-31 Out DMA Start Address
PCI start address for PCI master write transfer from the graphics processor core output FIFO .

5.2.7 Out DMA Count

The Out DMA Count register should be loaded with the number of words to be transferred in the DMA operation. The action of loading a word greater than zero initiates the DMA operation. The value read back from this register indicates the current number of words left to be transferred. Writes to this register will be ignored if it is non-zero, but can be read at any time.

OutDMACount

Region:	Zero	Read/Write	
Offset:	88h	**Reset Value:**	0000.0000h

Bits 0-23 Out DMA Count
Number of words to be transferred in the DMA operation.

Bits 16-31 Reserved

5.2.8 Gamma Reset Status Register

Writing to the reset status register causes a software reset of Gamma. The software reset does not reset the bus interface. The reset takes a number of cycles to complete during which the graphics processor should not be used. A flag in the register shows that the software reset is still in progress.

The GResetStatus register is different to the ResetStatus register in that only the Gamma device is reset, not the Target Device below Gamma. This register is normally for hardware diagnostic purposes only. The software operation is undefined if the Gamma is reset without resetting the Target Device.

GResetStatus

Region:	Zero	Read/Write	
Offset:	800h	**Reset Value:**	0000.0000h

Bits 0-30	Reserved
Bit 31	Software Reset Flag **0 = Gamma is ready for use.** **1 = Gamma is being reset and must not be used.**

5.2.9 Gamma Interrupt Enable Register

The Interrupt Enable Register selects which internal conditions are permitted to generate a bus interrupt. Three interrupt sources are defined below. At reset all interrupt sources are disabled.

GIntEnable

Region:	Zero	Read/Write	
Offset:	808h	**Reset Value:**	0000.0000h

Bit 0	DMA Interrupt Enable **0 = Disable interrupt.** **1 = Enable interrupt.**
Bit 1-2	Reserved
Bit 3	Error Interrupt Enable **0 = Disable interrupt.** **1 = Enable interrupt.**
Bits 4-12	Reserved
Bit 13	Command Interrupt Enable **0 = Disable interrupt.** **1 = Enable interrupt.**
Bits 14-31	Reserved

5.2.10 Gamma Interrupt Flags Register

The Interrupt Flags Register shows which interrupts are outstanding. Flag bits are reset by writing to this register with the corresponding bit set to a one. Flags at positions where the bits are set to zero will be unaffected by the write. The exception to this is bit 13, which is the Command interrupt Flag. This bit is cleared by clearing all bits the Command Unit Interrupt Flags Register **CommandIntFlags.**

GIntFlags

Region:	Zero	Read/Write	
Offset:	810h	**Reset Value:**	0000.0000h

Bit 0	DMA Flag **0 = No interrupt.** **1 = Interrupt outstanding.**
Bit 1-2	Reserved
Bit 3	Error Flag **0 = No interrupt.** **1 = Interrupt outstanding.**
Bits 4-12	Reserved
Bit 13	Command Interrupt Flag **Flag set when any bits set in the Command Interrupt Flags register** **0 = No interrupt.** **1 = Interrupt outstanding.**
Bits 14-31	Reserved

5.2.11 Gamma Error Flags Register

The Error Flags register shows which errors are outstanding in Gamma. Flag bits are reset by writing to this register with the corresponding bit set to a one. Flags at positions where the bits are set to zero will be unaffected by the write. The exception to this is bit 13, which is the Command Error Flag. This bit is cleared by clearing all bits the Command Unit Error Flags Register

GErrorFlags

Region: Zero Read/Write

Offset: 838h **Reset Value:** 0000.0000h

Bit 0 Input FIFO Error Flag
Flag set on write to full input FIFO.
0 = No error.
1 = Error outstanding.

Bits 1-2 Reserved

Bit 3 DMA Error Flag
Flag set for direct or register access to input FIFO while DMA is in progress (*i.e.* when the DMACount register is not zero).
0 = No error.
1 = Error outstanding.

Bit 4-6 Reserved

Bit 7 PCI Master Error Flag
Flag set when either Master abort or Target abort occurs while PCI Master access in progress. - The CFGStatus register can be read to determine the type of error.
0 = No error.
1 = Error outstanding.

Bit 8 Reserved

Bit 9 In DMA Overwrite Error Flag
Flag set in legacy mode if the InDMACount register is written when it is not zero
0 = No error.
1 = Error outstanding.

Bit 10 Out DMA Overwrite Error Flag
Flag set in legacy mode if the OutDMACount register is written when it is not zero
0 = No error.
1 = Error outstanding.

Bits 11-12 Reserved

Bit 13 Command Error Flag
Flag set when any bits set in the Command Error Flags register
0 = No error.
1 = Error outstanding.

Bits 14-31 Reserved

5.2.12 Gamma Test Register

For hardware test purposes only. Setting a bit in this register causes the corresponding unit to be put into test mode.

GTestRegister

Region:	Zero	Read/Write	
Offset:	848h	**Reset Value:**	0000.0000h

5.2.13 FIFO Disconnect Register

The FIFO Disconnect Register enables input FIFO disconnect on GLINT Gamma. Disconnect is disabled at reset.

DFIFODis

Region:	0	Read/Write	
Offset:	868h	**Reset Value:**	0000.0000h

Bit 0	Input FIFO Disconnect enable **0 = Disabled (RESET)** **1 = Enabled**
Bits 1-31	Reserved

5.2.14 Gamma Chip Configuration Register

Most of Gamma configuration bits are visible through the **GChipConfig**. This register can then be read back over the PCI bus, to allow the host to determine how the Gamma chip has been configured, and to modify various fields of the configuration if required.

GChipConfig

Region:	Zero	Read/Write	
Offset:	870h	**Reset Value:**	(configured)

Bit 0	AGPCapable **0 = AGP Capable** **1 = AGP Capable**	
Bit 1	SBACapable **0 = AGP sideband Addressing Disable** **1 = AGP sideband Addressing Enable**	
Bit 2	BaseClassZero **0 = use the correct PCI Base Class Code** **1 = force PCI Base Class Code to be zero**	
Bit 3-4	MinGrant[7:6] **Top 2 bits of the PCI Minimum Grant Configuration Register**	(Read Only)
Bit 5-6	MaxLat[7:6] **Top 2 bits of the PCI Minimum Grant Configuration Register**	(Read Only)
Bit 7	ExtDevice1 **Enable External device 1**	(Read Only)
Bit 8	ExtDevice2 **Enable External device2**	(Read Only)
Bit 9	ExtDevice3 **Enable External device 3**	(Read Only)
Bit 10-11	ExtVGAMode **0 = No VGA** **1 = External Device 1 is a VGA device** **2 = External Device 3 is a VGA device** **3 = No VGA**	
Bit 12	VGANonAlias **0 = enable VGA 10 bit address aliased decoding** **1 = disable VGA 10 bit address aliased decoding (Do 32bit decode)**	
Bit 13-16	VGAControl	
Bit 17	GlintEn1 **1 = External Device 1 is a GLINT device** **0 = External Device 1 is any other device**	(Read Only)
Bit 18	GlintEn2 **1 = External Device 2 is a GLINT device** **0 = External Device 2 is any other device**	(Read Only)
Bits 19-20	MultiGLINTAp **Indicates the MultiGLINT aperture size.** **0 = 0 MBytes.** **1 = 16 MBytes** **2 = 32 MBytes** **3 = 64 MBytes** **Note: If both GlintEn1 and GlintEn2 are not set then these bits are ignored and the Multi-GLINT aperture size is set to 0MBytes.**	(Read Only)
Bits 21-31	Reserved	

5.2.15 Gamma CSR Aperture Control Register

The Gamma CSR Aperture Control Register allows the accesses to Gamma and the GLINT chip behind to be configured in a number of different ways for a dual GLINT system. The register is reset to the Delta compatible configuration.

Note that this register has no effect on the region 0 space unless Gamma is controlling a dual GLINT system.

CSRAperture

Region:	Zero	Read/Write	
Offset:	878h	**Reset Value:**	0000.0000h

Bit 0 CSRViewDualGLINT
0 = Low CSR 64K accesses Master GLINT Little Endian
High CSR 64K accesses Master GLINT Big Endian
1 = Low CSR 64K accesses Master GLINT
High CSR 64K accesses Secondary GLINT
Endian set by CSRByteSwap

Bit 1 CSRByteSwap
This control bit has no effect unless the CSRViewDualGLINT bit is set
0 = All CSR accesses are little endian
1 = All CSR accesses are big endian

Bit 2 CSRGLINTSelect
This control bit has no effect except in a dual GLINT system as defined by the Gamma configuration bits.
0 = The Device 1 GLINT is the Master
1 = The Device 2 GLINT is the Master

Bits 3-31 Reserved (Read Only)
(all bits zero)

5.2.16 Page Table Address Register

The Page Table Address register holds the physical address of the page table used during the logical to physical mapping. The base address is given as a byte address, but must be on a 4K byte boundary.

PageTableAddr

Region:	Zero	Read/Write	
Offset:	C00h	**Reset Value:**	0000.0000h

Bits 0-11` Reserved

Bits 12-31` Page Table Address

5.2.17 Page Table Length Register

The Page Table Length register holds the length, in units of 4K bytes, of the page table. It is only used for some basic range checking.

PageTableLength

Region:	Zero	Read/Write	
Offset:	C08h	**Reset Value:**	0000.0000h

Bits 0-9	Page Table Length
Bits 10-31	Reserved

5.2.18 Delay Timer Register

The Delay Timer Register, when written to, starts a timer. When the timer reaches one an interrupt is generated and the timer stops. Writing zero aborts the timer with no interrupt being generated. Reading this register returns the current timer value.

DelayTimer

Region:	Zero	Read/Write	
Offset:	C38h	**Reset Value:**	0000.0000h

Bits 0-31	Delay Timer Count

5.2.19 Command Mode Register

The Command Mode Register controls the operation of the Command Unit.

CommandMode

Region:	Zero	Read/Write	
Offset:	C40h	**Reset Value:**	0000.0000h

Bits 0-1 Command Unit Operation
0 = Legacy DMA operation
1 = Queued DMA operation
2 = Reserved
3 = Reserved

Bit 2 Logical addressing
0 = Disable logical addressing
1 = Enable logical addressing

Bit 3 Abort Output DMA
0 = Normal operation
1 = Abort Output DMA

Bit 4-5 Reserved

Bit 6 Abort Input DMA
0 = Normal operation
1 = Abort Input DMA

Bits 7-31 Reserved

5.2.20 Command Interrupt Enable Register

The Command Interrupt Enable Register selects which command conditions are permitted to generate a bus interrupt. At reset all interrupt sources are disabled.

CommandIntEnable

Region: Zero Read/Write

Offset: C48h **Reset Value:** 0000.0000h

Bit 0 FIFO Queued Command DMA Interrupt Enable
0 = Interrupt disabled
1 = Interrupt enabled

Bit 1 Output DMA Interrupt Enable
0 = Interrupt disabled
1 = Interrupt enabled

Bit 2 Command Interrupt Enable
0 = Interrupt disabled
1 = Interrupt enabled

Bit 3 Timer Interrupt Enable
0 = Interrupt disabled
1 = Interrupt enabled

Bit 4 Command Error Interrupt Enable
0 = Interrupt disabled
1 = Interrupt enabled

Bit 5-7 Reserved

Bit 8 Page Fault Command Interrupt Enable
0 = Interrupt disabled
1 = Interrupt enabled

Bit 9 Page Fault Vertex Interrupt Enable
0 = Interrupt disabled
1 = Interrupt enabled

Bit 10-11 Reserved

Bit 12 Page Fault Write Interrupt Enable
0 = Interrupt disabled
1 = Interrupt enabled

Bits 13-31 Reserved

5.2.21 Command Interrupt Flags Register

The Command Interrupt Flags Register shows which Command interrupts are outstanding. Flag bits are reset by writing to this register with the corresponding bit set to a one. Flags at positions where the bits are set to zero will be unaffected by the write.

CommandIntFlags

Region: Zero Read/Write

Offset: C50h **Reset Value:** 0000.0000h

Bit 0	FIFO Queued Command DMA Flag **0 = No flag** **1 = flag**
Bit 1	Output DMA Flag **0 = No flag** **1 = flag**
Bit 2	Command Flag **0 = No flag** **1 = flag**
Bit 3	Timer Flag **0 = No flag** **1 = flag**
Bit 4	Command Error Flag **0 = No flag** **1 = flag**
Bits 5-7	Reserved
Bit 8	Page Fault Command Flag **0 = No flag** **1 = flag**
Bit 9	Page Fault Vertex Flag **0 = No flag** **1 = flag**
Bit 10-11	Reserved
Bit 12	Page Fault Write Flag **0 = No flag** **1 = flag**
Bits 13-31	Reserved

5.2.22 Command Error Flags Register

The Command Error Flags register shows which errors are outstanding in the Gamma Command Unit. Flag bits are reset by writing to this register with the corresponding bit set to a one. Flags at positions where the bits are set to zero will be unaffected by the write.

CommandErrorFlags

Region:	Zero	Read/Write	
Offset:	C58h	**Reset Value:**	0000.0000h

Bit 0	Stack underflow error **0 = No error** **1 = Error**
Bit 1	Stack overflow error **0 = No error** **1 = Error**
Bit 2	DMA overrun error **0 = No error** **1 = Error**
Bit 3	Reserved
Bit 4	Page Mapping Fault Command error **0 = No error** **1 = Error**
Bit 5	Page Mapping Fault Vertex error **0 = No error** **1 = Error**
Bits 6-7	Reserved
Bit 8	Page Mapping Fault Write error **0 = No error** **1 = Error**
Bit 9	Reserved
Bit 10	Page Fault Read Access Command error **0 = No error** **1 = Error**
Bit 11	Page Fault Read Access Vertex error **0 = No error** **1 = Error**
Bits 12-19	Reserved
Bit 20	Page Fault Write Access Write error **0 = No error** **1 = Error**
Bit 21	Reserved
Bit 22	Illegal DMA Tag error **0 = No error** **1 = Error**
Bits 23-31	Reserved

5.2.23 Command Status Register

The Command Status register is a read only register which gives information about the current Command unit status.

CommandStatus

Region:	Zero	Read Only	
Offset:	C60h	**Reset Value:**	0000.0004h

Bit 0	Command DMA busy **0 = Idle** **1 = Busy**
Bit 1	Output DMA Busy **0 = Idle** **1 = Busy**
Bit 2	Input FIFO Empty **0 = Not empty** **1 = Empty**
Bits 3-31	Reserved

5.2.24 Command Faulting Address Register

The Command Faulting Address register hold the logical address of an Input DMA access which caused a Command Fault interrupt, or caused one of the three possible logical to physical mapping errors.

CommandFaultingAddr

Region:	Zero	Read Only	
Offset:	C68h	**Reset Value:**	0000.0000h

Bits 0-31	Command Faulting Address

5.2.25 Vertex Faulting Address Register

The Vertex Faulting Address register hold the logical address of a Rectangle Read DMA access which caused a Vertex Fault interrupt, or caused one of the three possible logical to physical mapping errors.

VertexFaultingAddr

Region:	Zero	Read Only	
Offset:	C70h	**Reset Value:**	0000.0000h

Bits 0-31	Vertex Faulting Address

5.2.26 Write Faulting Address Register

The Write Faulting Address register hold the logical address of an Write DMA access which caused a Write Fault interrupt, or caused one of the three possible logical to physical mapping errors.

WriteFaultingAddr

Region:	Zero	Read Only	
Offset:	C88h	**Reset Value:**	0000.0000h

Bits 0-31	Write Faulting Address

5.2.27 Feedback Select Count Register

The operation of this register is currently defined in the Command Unit Specification.

FeedbackSelectCount

Region:	Zero	Read Only	
Offset:	C98h	**Reset Value:**	0000.0000h

Bits 0-23	Feedback Select Count
Bits 24-30	Reserved
Bit 31	Feedback Select Count Overflow **0 = No overflow** **1 = Overflow**

5.2.28 Gamma Processor Mode Register

The Gamma Processor Mode register allows the user to disable the Delta unit in Gamma. This is to allow a target chip Delta unit to be used instead.

GammaProcesorMode

Region:	Zero	Read/Write	
Offset:	CB8h	**Reset Value:**	0000.0000h

Bit 0	Delta Enable **0 = Delta unit enabled** **1 = Delta unit disabled**
Bits 1-31	Reserved

5.2.29 VGA Shadow Control Register

The VGA shadow control register allows the readback, and also writing of the VGA IO space shadow bits. This allows the VGA shadowing to be set without the use of IO space accesses.

VGAShadow

Region:	Zero	Read/Write	
Offset:	D00h	**Reset Value:**	0000.0001h

Bit 0	VGA IO Color decode **1 = Decode IO color space 3DXh** **0 = Decode VGA monochrome space 3BXh**
Bit 1	VGA Memory enable **0 = Disable VGA memory** **1 = Enable VGA memory**
Bits 2-3	VGA Memory region Select **00b = A0000h - BFFFFh (128K)** **01b = A0000h - AFFFFh (64K)** **10b = B0000h - B7FFFh (32K)** **11b = B8000h - BFFFFh (32K)**
Bits 4-31	Reserved

5.2.30 Multi-GLINT Aperture Control Register

The Multi-GLINT aperture control register controls the operation of the Multi-GLINT aperture. The control bits define X spans and Y multiply controls to allow the use of non shared framebuffer GLINT systems behind Gamma.

MultiGLINTAperture

Region:	Zero	Read/Write	
Offset:	D08h	**Reset Value:**	0000.0000h

Bit s 0-1	Input X Span **00b = Input X span is 1Kbytes** **01b = Input X span is 2Kbytes** **10b = Input X span is 4Kbytes** **11b = Input X span is 8Kbytes**
Bit 2	Product Select **0 = Use 2x product** **1 = Use 16x product (This is used for X Spans of 800 and 1600)**
Bit 3	1x Product Enable
Bit 4	16x / 2x Product Enable
Bit 5	4x Product Enable
Bit 6	8x Product Enable
Bits 7-9	Post Multiply **000b = x8.** **001b = x16.** **010b = x32.** **011b = x64.** **100b = x128.** **101b = x256** **All other values = x8**
Bits 10-11	GLINT Aperture Size **00b = 4M.** **01b = 8M.** **10b = 16M.** **11b = 32M**
Bits 12-31	Reserved

5.2.31 Multi-GLINT Base 1 Register

The Multi GLINT Base 1 Register should be loaded with the framebuffer base address of the First GLINT in a multi-GLINT system which uses the multi-GLINT aperture.

MultiGLINT1

Region:	Zero	Read/Write	
Offset:	D10h	**Reset Value:**	0000.0000h
Bits 0-21	Reserved		
Bits 22-31	GLINT 1 Base Address		

5.2.32 Multi-GLINT Base 2 Register

The Multi-GLINT Base 2 Register should be loaded with the framebuffer base address of the Second GLINT in a multi-GLINT system which uses the multi-GLINT aperture.

MultiGLINT2

Region:	Zero	Read/Write	
Offset:	D18h	**Reset Value:**	0000.0000h
Bits 0-21	Reserved		
Bits 22-31	GLINT 2 Base Address		

5.2.33 Serial EEPROM Access Register

This register is used to access the Configuration Serial EEPROM. Reads and writes of the EEPROM can be initiated by setting up the correct stream of read and write accesses to the bottom bit of this register. For details of the read / write patterns to be used, see the XICOR data sheet on the X84041 operation. Note the EEPROM is also programmable and readable through a configuration register.

SerialAccess

Region:	Zero	Read/Write	
Offset:	F00h	**Reset Value:**	0000.0000h

Bit 0	Serial EEPROM Data Pin
Bits 1-31	Reserved

5.3 Graphics Core Registers

All the Graphics Core registers in the GLINT Gamma, GLINT 500TX and MX are addressed in this part of region 0. The address for each register and associated data fields is defined in the appropriate Programmers Reference Manual.

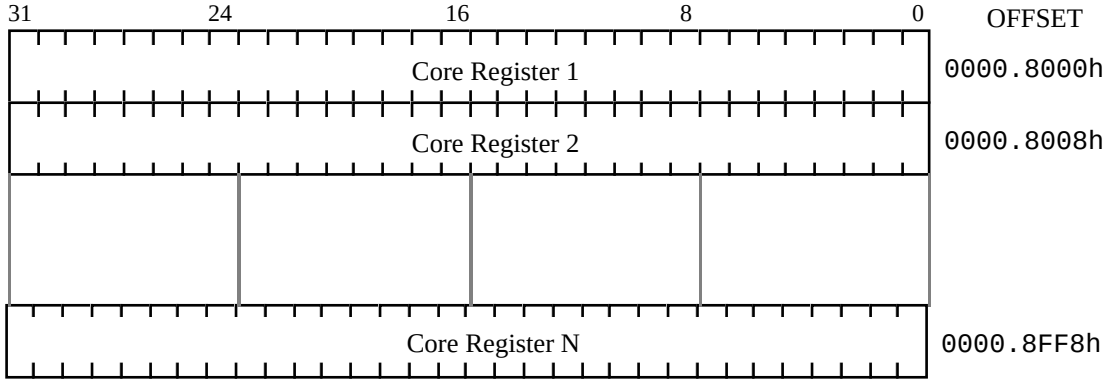

Figure 5-1 Graphics Core Registers

Note: Not all the available register locations are used within the Graphics Core. The registers are on 64 bit boundaries

5.4 Graphics Core FIFO Interface

The Graphics Core FIFO interface provides a port through which both GC register addresses and data can be sent to the input FIFO. A range of 4 KBytes of host space is provided although all data may be sent through one address in the range. ALL accesses go directly to the FIFO, the range is provided to allow for data transfer schemes which force the use of incrementing addresses. Before writing to the input FIFO the user must check that there is sufficient space by reading the InFIFOSpace register.

If the FIFO interface is used, then data is typically sent to the GLINT Gamma in pairs, an address word which addresses the register to be updated, followed by the data to be sent to the register.

Note: The GC registers can not be read through this interface. Command buffers generated to be sent to the input FIFO interface may be read directly by the GLINT Gamma by using the DMA controller.

A data formatting scheme is provided to allow for multiple data words to be sent with one address word where adjacent or grouped registers are being written, or where one register is to be written many times.

For more information on the direct FIFO interface data buffer formats please refer to the GLINT Gamma, GLINT 500TX and MX Programmers Reference Manuals.

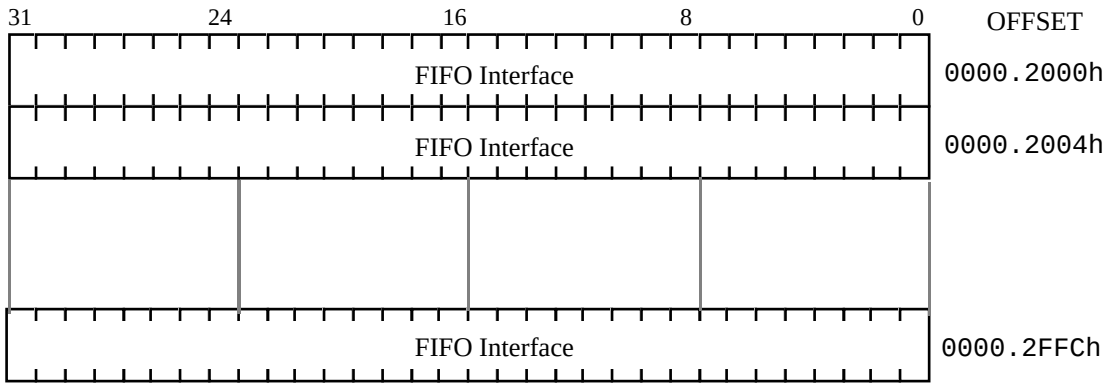

Figure 5-2 Graphics Core FIFO Interface

Note: The FIFO interface can be accessed at 32 bit boundaries. This is to allow a direct copy from a DMA format buffer.

6. Electrical Data

6.1 Absolute Maximum Ratings

Junction Temperature	100°C
Storage Temperature	-65°C to 150°C
DC Supply Voltage	3.8V
I/O Pin Voltage with respect to GND	-0.5V to 5.5V

Table 6-1 Absolute Maximum Ratings

6.2 DC Specifications

Symbol	Parameter	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
L_{PIN}	Pin Inductance		18.4	nH
I_{CC}	Power Supply Current			mA

Table 6-2 DC Specifications

Symbol	Parameter	Min	Max	Unit
V_{PIL}	Input Low Voltage		0.8	V
V_{PIH}	Input High Voltage	2.0		V
V_{POL}	Output Low Voltage		0.5	V
V_{POH}	Output High Voltage	2.4		V
I_{PIL}	Input Low Current		Note 1	mA
I_{PIH}	Input High Current		Note 1	mA
C_{PIN}	Input Capacitance		10	pF
C_{CLK}	PCI Clock Input Capacitance		12	pF
C_{IDSEL}	PCI Idsel Input Capacitance		8	pF

Table 6-3 PCI Signal DC Specifications

Note 1: This value is PCI 2.1 compliant

6.3 AC Specifications

Pin Name	Capacitive Load
PCIAD[31:0], PCICBEN[3:0], PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, PCIReqN, PCIGntN, PCIIntAN, AGPPipeN, AGPRbfN, AGPSBA[7:0], SCIAD[31:0], SCICBEN[3:0], SCIPar, SCIFrameN[1:0],SCIIRdyN[1:0], SCITRdyN[1:0],SCIStopN[1:0], SCIDevselN[1:0].	50pFin PCI 33 system. 10pF in AGP system
SCIClkOut[3:0],PCIFIFOInDis.	20pF

Table 6-4 Test Loads for AC Timing

6.3.1 Clock Timing

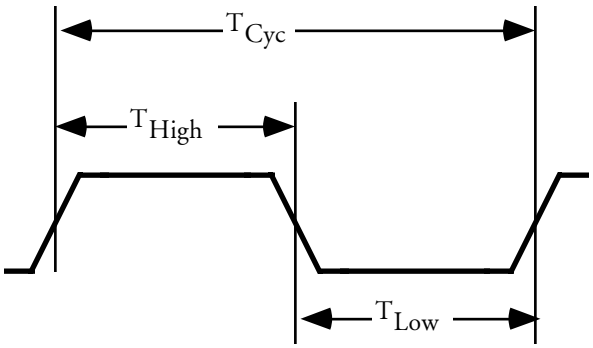

Figure 6-1 Clock Waveform Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{PCyc}	PCIClk Cycle Time	15		ns	
T_{PHigh}	PCIClk High Time			ns	
T_{PLow}	PCIClk Low Time			ns	
T_{MCyc}	MClk Cycle Time			ns	
T_{MHigh}	MClk High Time			ns	
T_{MLow}	MClk Low Time			ns	
T_{SCyc}	SCIClk Cycle Time	25		ns	
T_{SHigh}	SCIClk High Time			ns	
T_{SLow}	SCIClk Low Time			ns	

Table 6-5 Clock Waveform Timing

6.3.2 Input / Output Timing

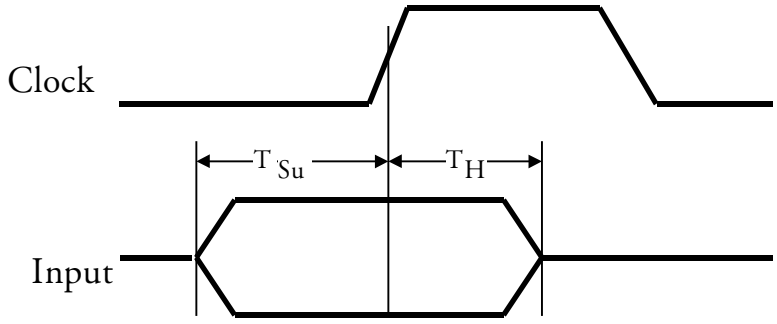

Figure 6-2 Clock Referenced Input Timing

Parameter	T_{Su} Min	T_H Min	Units	Notes
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, AGPSt[2:0]	5	0	ns	
PCIGntN	5	0	ns	
PCIRstN	7	0	ns	1

Table 6-6 PCIClk Referenced Input Timing

Note 1: PCIRstN is resynchronized internally. The given timings, when met, ensure that the reset is detected in the current cycle.

Parameter	T_{Su} Min	T_H Min	Units	Notes
SCIAD(31:0), SCICBEN(3:0), SCIPar, SCIIRdyN(1:0), SCITRdyN(1:0), SCIStopN(1:0), SCIDevselN(1:0), GLINTInDis(1:0),GLINTOutDis(1:0), SCIReqN	5	0.2	ns	
ModeCtl(1:0), VGAEn, ExtFuncEn(1:0)	10	2	ns	

Table 6-7 SCIClk Referenced Input Timing

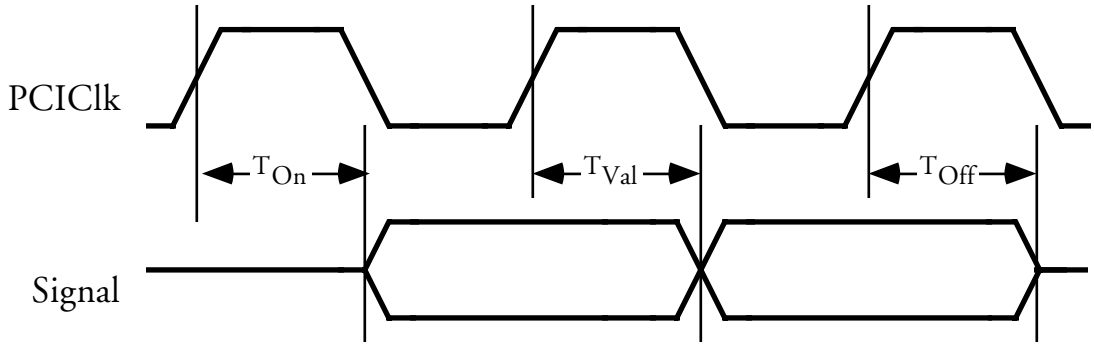

Figure 6-3 PCIClk Referenced Output Timing

	T_{Val}		T_{On}		T_{Off}			
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN	2	11	2	11	2	11	ns	
PCIReqN	2	12					ns	
PCIIntAN	2	15					ns	1

Table 6-8 PCIClk 33MHz Referenced Output Timing

Note 1: Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

	T_{Val}		T_{On}		T_{Off}			
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN	1.5	6	1.5	6	2	11	ns	
PCIReqN	1.5	6					ns	
PCIIntAN	1.5	6					ns	1

Table 6-9 PCIClk 66MHz Referenced Output Timing

Note 1: Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

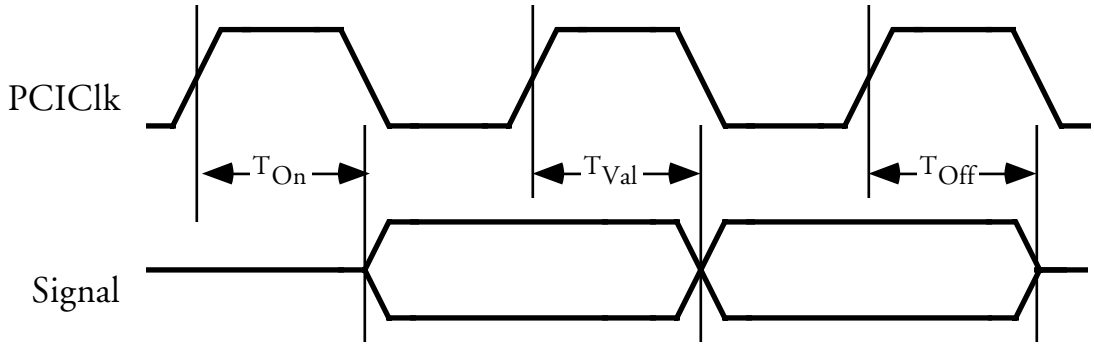

Figure 6-4 SCIClk Referenced Output Timing

	T_{val}		T_{On}		T_{Off}			
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
SCIAD(31:0), SCICBEN(3:0), SCIPar, SCIFrameN, SCIIRdyN, SCITRdyN, SCIStopN, SCIDevselN	1.5	7	1.5	7	1.5	7	ns	
SCIGntN	1.5	7					ns	

Table 6-10 SCIClk Referenced Output Timing

7. Pin Information

The GLINT Gamma comes in a 176 pin PQFP package.

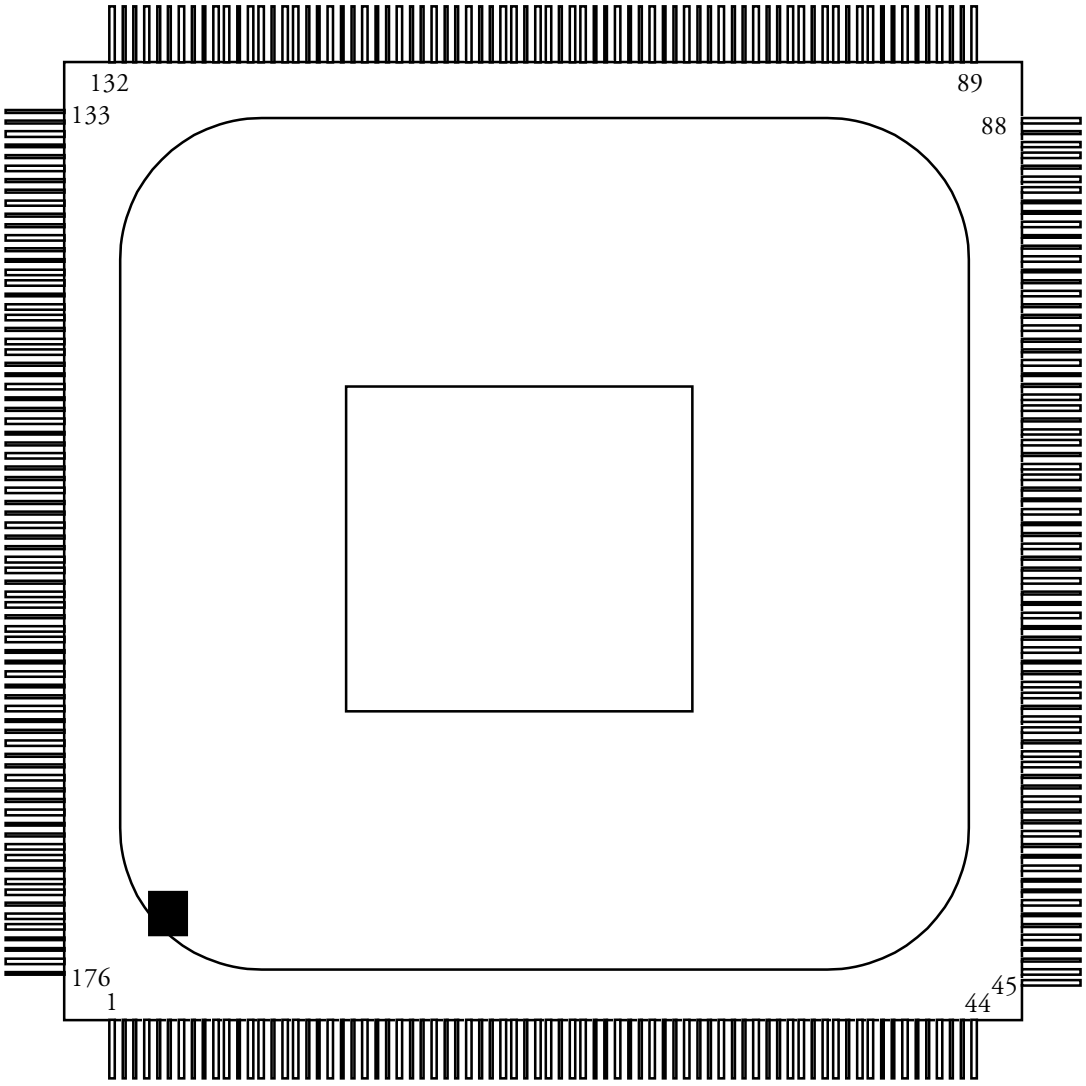

Figure 7-1 Pin Numbering

7.1 Alphabetical Pin Listing

Symbol		Pin Numbers
AGPPipeN	*	109
AGPRBFN	*	112
AGPSBA(0:7)	*	138,142,144,148,149,150,151,152
AGPST(0:2)	*	113,114,115
ExtFuncEn(0:1)		106,108
GLINTInDis(0:1)		146,147
GLINTOutDis(0:1)	*	90,100
GND		9,14,23,27,32,37,45,53,57,67,71,81,91,97,103,111,120,125, 130,141,155,160,164,169,172,176
MClk		126
PCIAD(31:0)		165,171,173-175,1-3,7,11-13,15-17,19,31,33-35,38-40,42,44, 46,47,49-51,54,55,
PCICBEN(3:0)		5,20,30,43
PCIClk		170
PCIDevselN		26
PCIFrameN		21
PCIGntN		166
PCIIdsel		6
PCIIntAN		161
PCIIRdyN		24
PCIPar		29
PCIReqN		167
PCIRstN		162
PCIStopN		28
PCITRdyN		25
SCIAD(0:31)		56,58-61,63-65,69,70,72-75,77,78,104,105,116-119,121,122, 129,131-134,136,137,143
SCICBEN(0:3)		68,79,102,128
SCIClk		139
SCIClkOut(3:0)		156-159
SCIDevselN(0:1)		87,88
SCIFrameN(0:1)		98,99
SCIGntN	*	107
SCIIntAN		127
SCIIRdyN(0:1)		92,93
SCIPar		84

SCIReqN	*	101
SCIRstN		123
SCIStopN(0:1)		82,83
SCITRdyN(0:1)		94,95
SerialCEN		10
SerialData	*	89
SerialOEN	*	85
SerialWEN	*	86
TestMode		153
VDD		4,8,18,22,36,41,48,52,62,66,76,80,96,110,124,135,140,145, 154,168
VGAEn		163

* indicates changes from GLINT Delta.

Table 7-1 Alphabetical Pin Listing

7.2 Numerical Pin Listing

Pin	Name
1	PCIAD26
2	PCIAD25
3	PCIAD24
4	VDD
5	PCICBEN3
6	PCIIdsel
7	PCIAD23
8	VDD
9	GND
10*	SerialCEN
11	PCIAD22
12	PCIAD21
13	PCIAD20
14	GND
15	PCIAD19
16	PCIAD18
17	PCIAD17
18	VDD
19	PCIAD16
20	PCICBEN2
21	PCIFrameN
22	VDD

Pin	Name
23	GND
24	PCIIRdyN
25	PCITRdyN
26	PCIDevselN
27	GND
28	PCIStopN
29	PCIPar
30	PCICBEN1
31	PCIAD15
32	GND
33	PCIAD14
34	PCIAD13
35	PCIAD12
36	VDD
37	GND
38	PCIAD11
39	PCIAD10
40	PCIAD9
41	VDD
42	PCIAD8
43	PCICBEN0
44	PCIAD7

45	GND
46	PCIAD6
47	PCIAD5
48	VDD
49	PCIAD4
50	PCIAD3
51	PCIAD2
52	VDD
53	GND
54	PCIAD1
55	PCIAD0
56	SCIAD0
57	GND
58	SCIAD1
59	SCIAD2
60	SCIAD3
61	SCIAD4
62	VDD
63	SCIAD5
64	SCIAD6
65	SCIAD7
66	VDD
67	GND

68	SCICBEN0
69	SCIAD8
70	SCIAD9
71	GND
72	SCIAD10
73	SCIAD11
74	SCIAD12
75	SCIAD13
76	VDD
77	SCIAD14
78	SCIAD15
79	SCICBEN1
80	VDD
81	GND
82	SCIStopN0
83	SCIStopN1
84	SCIPar
85*	SerialOEN
86*	SerialWEN
87	SCIDevselN0
88	SCIDevselN1
89*	SerialData
90*	GLINTOutDis0

91	GND	113*	AGPST0	135	VDD	157	SCIClkOut2
92	SCIIRdyN0	114*	AGPST1	136	SCIAD29	158	SCIClkOut1
93	SCIIRdyN1	115*	AGPST2	137	SCIAD30	159	SCIClkOut0
94	SCITRdyN0	116	SCIAD18	138*	AGPSBA0	160	GND
95	SCITRdyN1	117	SCIAD19	139	SCIClk	161	PCIIntAN
96	VDD	118	SCIAD20	140	VDD	162	PCIRstN
97	GND	119	SCIAD21	141	GND	163	VGAEn
98	SCIFrameN0	120	GND	142*	AGPSBA1	164	GND
99	SCIFrameN1	121	SCIAD22	143	SCIAD31	165	PCIAD31
100*	GLINTOutDis1	122	SCIAD23	144*	AGPSBA2	166	PCIGntN
101*	SCIReqN	123	SCIRstN	145	VDD	167	PCIReqN
102	SCICBEN2	124	VDD	146	GLINTInDis0	168	VDD
103	GND	125	GND	147	GLINTInDis1	169	GND
104	SCIAD16	126	MClk	148*	AGPSBA3	170	PCIClk
105	SCIAD17	127	SCIIntAN	149*	AGPSBA4	171	PCIAD30
106	ExtFuncEn0	128	SCICBEN3	150*	AGPSBA5	172	GND
107*	SCIGntN	129	SCIAD24	151*	AGPSBA6	173	PCIAD29
108	ExtFuncEn1	130	GND	152*	AGPSBA7	174	PCIAD28
109*	AGPPipeN	131	SCIAD25	153	TestMode	175	PCIAD27
110	VDD	132	SCIAD26	154	VDD	176	GND
111	GND	133	SCIAD27	155	GND		
112*	AGPRBFN	134	SCIAD28	156	SCIClkOut3		

* indicates changes from GLINT Delta.

Table 7-2 Numerical Pin Listing

8. Package Dimensions

LQFP 176

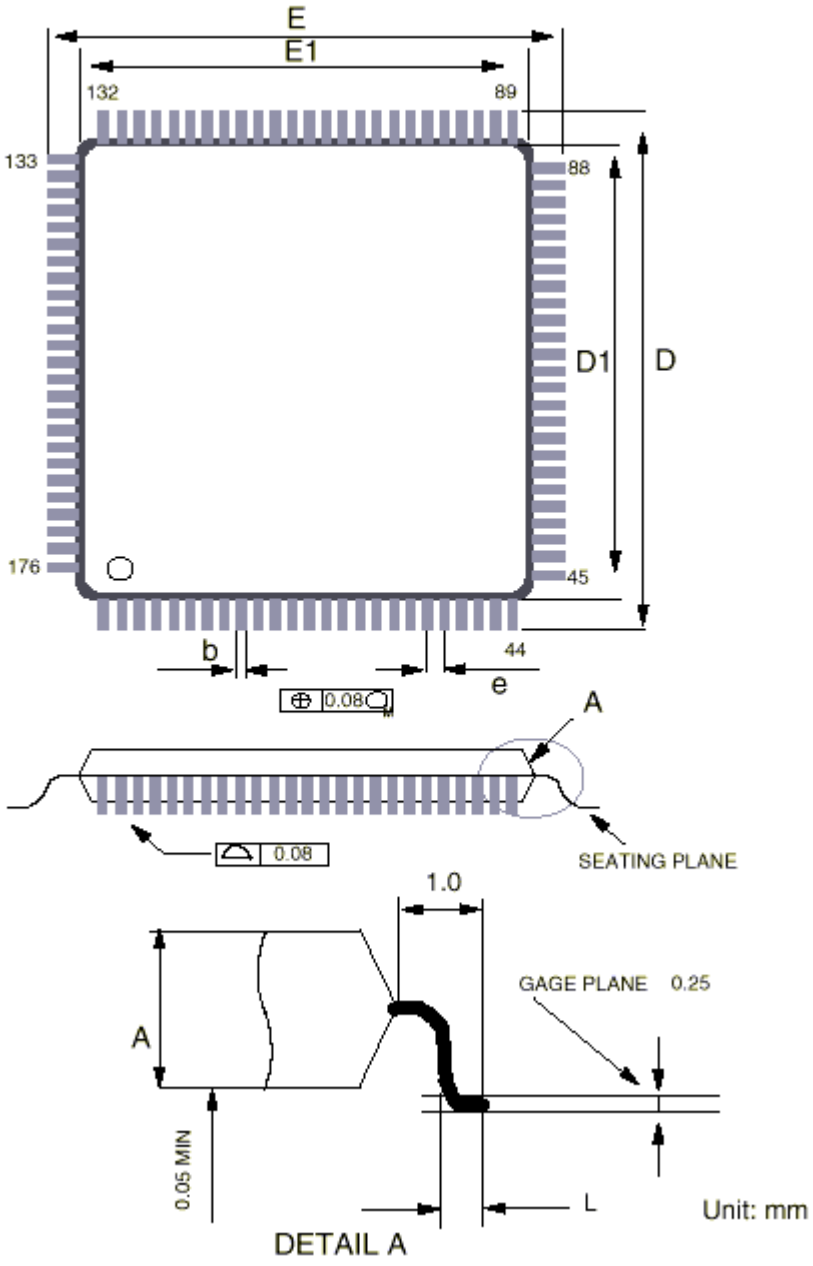

Figure 8-2 Mechanical Diagrams

Dimension		mm
a	Lead Pitch	0.5
b	Lead Width	0.22 ± 0.05
c	Foot Length	0.6 ± 0.15
d	Height	1.6
E	Width (toe to toe)	26.0
F	Body Width	24.0

Table 8-3 176 pin PQFP Package Dimensions

9. Gamma System Design

The following notes should be followed when designing systems which use the Gamma device.

9.1 Termination / Pull-ups

The signals SCIFrameN(0:1), SCIIRdyN(0:1), SCITRdyN(0:1), SCIStopN(0:1), SCIDevselN(0:1) are Tri-state signals which need to be held in their inactive state by 10K Ohm pull-up resistors.

SCIIntAN is an open drain signal which should all be pulled high with a 10K Ohm resistor.

The Testmode pin should be pulled low. Typically a 470 Ohm resistor would be used.

9.2 Secondary device IDSel wiring

Each secondary PCI device has an IDSel pin which must be wired up to allow Configuration space accesses to occur. On Gamma the IDSel lines on multiplexed onto the SCIAD bus. The IDSels should be wired as follows:

SCIAD28 should be connected to Idsel of a device fitted as secondary device 1.

SCIAD29 should be connected to Idsel of a device fitted as secondary device 2.

SCIAD30 should be connected to Idsel of a device fitted as secondary device 3.

9.3 GLINT side-band signals

GLINT devices have 2 sets of side-band signals for use after a Gamma device. These control data throttling into the input FIFO, and out of the output FIFO.

The Gamma GLINTInDis0 should be connected to PCIFIFOInDis of the GLINT rendering device fitted as secondary device 1.

The Gamma GLINTOutDis0 should be connected to PCIFIFOOutDis of the GLINT rendering device fitted as secondary device 1.

The Gamma GLINTInDis1 should be connected to PCIFIFOInDis of a GLINT rendering device fitted as secondary device 2.

The Gamma GLINTOutDis1 should be connected to PCIFIFOOutDis of the GLINT rendering device fitted as secondary device 2.

9.4 Using a secondary bus master

The Gamma device allows for one device to be a PCI bus master. To use PCI bus mastering the device must be connected to the second set of secondary bus PCI control signals. i.e. SCIFrameN(1), SCIIRdyN(1), SCITRdyN(1), SCIStopN(1), and SCIDevselN(1).

10. Thermal Characteristics

The maximum junction temperature must be kept below T_j(max) and this can only be guaranteed by proper analysis of the operating environment and the thermal path between the die and the air surrounding it.

10.1 Device Characteristics

These are fixed characteristics of the device and are independent of the operating environment or the characteristics of any heatsink:-

$T_{j(max)}$	=	125 °C.
Pd(max)	=	5.5 Watts @ Vdd(max), f_{MClk} = 66MHz.
θ_{jt}	=	3.0 °C/Watt.

10.2 Thermal Model

The formula used to calculate the junction temperature (T_j) is

$$T_j = T_a + Pd(\theta_{jt} + \theta_{cs} + \theta_{sa})$$
$$= T_a + Pd\theta_{ja}$$

Where:

T_j	=	Junction temperature (°C)
T_a	=	Ambient temperature (°C)
Pd	=	Power dissipation (Watts)
θ_{jt}	=	Junction to top of case thermal resistance (°C/Watt)
θ_{cs}	=	Case to Heatsink thermal resistance (°C/Watt)
θ_{sa}	=	Heatsink to Air thermal resistance (°C/Watt)
θ_{ja}	=	Total Junction to Air thermal resistance (°C/Watt)

The θ_{ja} form of the equation is more appropriate when there is no heatsink attached to the device.

10.3 Operation Without Heatsink

Gamma should not be operated without a heatsink attached.

10.4 Operation With Heatsink

With a heatsink attached to the device the junction temperature will depend on θ_{cs} and θ_{sa}. θ_{cs} is the thermal resistance of the join between the heatsink and the case. θ_{sa} is the thermal resistance of the heatsink and will be a function of system airflow.

The table below shows the calculated thermal figures for a 22mmx22mm heatsink with 10mm high fins.

Airflow lfpm		**θ_{ja} ° C/W**
0	(Convection Cooling)	16.4
50	(0.25m/sec)	12.3
100	(0.5m/sec)`	10.2
200	(1.0m/sec)`	8.6
400	(2.0m/sec)`	7.7

Table 10-1 Operation With Heatsink

This heatsink would be suitable for Gamma operation for ambient temperatures of up to 40°C. This heatsink would be suitable for Gamma operation for ambient temperatures of up to 35°C with zero airflow.

10.4.1 Heatsink Attachment

The heatsink should be attached with thermally conductive epoxy. Either Loctite Output 315 with Loctite 7387 or type EG 7655 from A.I. Technology Inc. are recommended. The thickness of the epoxy layer should be between 0.05mm and 0.15mm with 100% coverage of the attach area, and a maximum voiding in the bond area of 3%.

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