3Dlabs®

# GLINT® 500TX™

## *Hardware Reference Manual*

Version 1.0

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3Dlabs Inc.
2010 North First Street, Suite 403
San Jose, CA 95131
United States

Tel: (408) 436 3455
Fax: (408) 436 3458

3Dlabs Ltd.
Meadlake Place
Thorpe Lea Road. Egham
Surrey, TW20 8HE
United Kingdom

Tel: +44 (0) 784 470555
Fax: +44 (0) 784 470699

# Change History

| Issue | Date | Change |
|---|---|---|
| 1.0 | 1 April 96 | First Release |
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# Contents

# 1. GLINT 500TX Functional Overview

## 1.1 Introduction

The GLINT 500TX high performance graphics processor combines workstation class 3D graphics acceleration and state of the art 2D performance in a single chip. 3D rendering operations are accelerated by the GLINT 500TX, including Gouraud shading, depth buffering, antialiasing and alpha blending.

Implemented around a scalable memory architecture, the GLINT 500TX reduces the cost and complexity of delivering high performance 3D graphics within a windowing environment - making it ideal for a wide range of graphics products from PC boards to high end workstation accelerators.

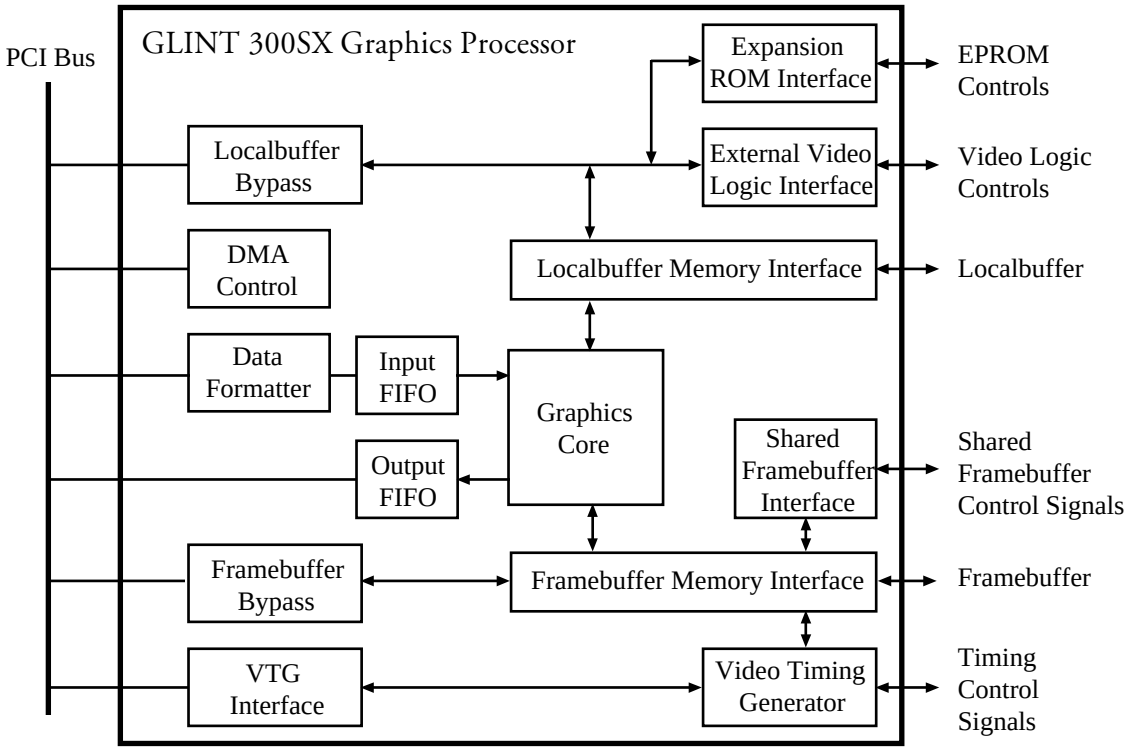



Figure 1-1. GLINT 500TX Functional Units

## 1.2 Notation

The following notational conventions are used in this book.

A signal name ending in N indicates an active low signal, eg PCIFrameN.

n-m indicates a bit field from bit n to bit m, eg. 7-0 specifies bits 7 through 0 inclusive.

Use of the letter h indicates a hexadecimal number, eg. 6Fh is a hexadecimal number.

Use of the letter b indicates a binary number, eg. 1010b is a binary number.

## 1.3 GLINT 500TX Graphics Core

The Graphics Core (GC) in the GLINT 500TX accelerates the key operations for 3D and 2D applications. For further information on the functionality of the GC refer to the GLINT Programmers Reference Manual.

## 1.3 PCI Interface

The PCI interface conforms to the PCI Local Bus standard Revision 2.1. The GLINT 500TX is a PCI Local Bus Target and a PCI Local Bus Read Master.

The host interface includes the configuration registers, the GLINT 500TX control registers, and two bypass paths: one to the GLINT 500TX Localbuffer memory and one to the Framebuffer memory.

The PCI interface has an input FIFO for passing data to the Graphics Core, and an output FIFO for buffering up data to be read from the Graphics Core. The input FIFO is 32 words deep. The output FIFO is 8 words deep.

A DMA controller is provided in the PCI interface to allow the GLINT 500TX to read data directly into the Graphics Core input FIFO.

## 1.4 Big-endian Processor support

The GLINT 500TX provides support for big-endian processors. A big-endian processor will generate byte swapped big-endian data on the PCI local bus, commonly known as gib-endian.

All the regions on the GLINT 500TX can accept gib-endian data. The configuration space is set by a control pin at reset time and the GLINT 500TX control registers are always visible little and gib-endian.

The Localbuffer and Framebuffer each have two PCI apertures whose endian is programmable.

## 1.5 Localbuffer Memory Interface

The Localbuffer memory is used to store off screen pixel associated information. This includes Depth (Z), Stencil, and Window support fields.

The Localbuffer consists of one or two banks of DRAM giving from 2 to 48 MBytes of storage. A Localbuffer pixel width of 0 to 48 bits is supported. The number of bits populated in any hardware implementation will depend on software requirements. The memory control signals are programmable to allow for optimum operation at different GLINT 500TX clock speeds with memory systems using -50 to -80 speed DRAM parts. Page sizes from 256 to 2048 are supported. EDO DRAM is also supported.

The Localbuffer interface provides a link to the PCI Local Bus to allow host accesses to bypass the Graphics Core.

Table 1-1. Localbuffer DRAM

| DRAM Generic types |
|---|
| 256K x 16/18 |
| 512k x8/9 |
| 1M x 4 |
| 1M x 16/18 |
| 2M x 8/9 |
| 4M x 4 |

DRAMs used must support fast page-mode or Extended-DataOut and CAS-BEFORE-RAS refresh.

## 1.6 Framebuffer Memory Interface

The GLINT 500TX can address a Framebuffer of between 2MByte and 32MBytes of VRAM. A Framebuffer data width of 64 bits is supported. The VRAMs supported include 256kx4, 256kx8 and 256kx16. The VRAMs must support split transfer cycles.

The memory control signals are programmable to allow for optimum operation at different GLINT 500TX clock speeds with a range of memory speeds allowing -60 to -80 VRAMs to be used. The GLINT 500TX can make use of VRAM write masks and block fill mode, if available, to improve performance.

LUT-DACs with 64 and 128 bit pixel buses are supported. For more information on LUT-DAC support refer to External Video Control (Section 5).

GLINT 500TX interfaces directly to most framebuffers, however framebuffers with greater than 16 memory parts require external buffering of the address and control lines.

The Framebuffer interface also provides a link to the PCI Local Bus to allow host accesses to bypass the Graphics Core.

The GLINT 500TX supports 32, 16, and 8 bit packed framestores.

## 1.7 Shared Framebuffer/Shared Localbuffer Interface

The GLINT 500TX provides a mechanism to share either the framebuffer or the localbuffer with another device. The GLINT 500TX can be programmed to either carry out the sharing arbitration (primary controller) or act as a slave (secondary controller).

## 1.8 Video Timing Generation

The GLINT 500TX has an internal timing generator and VRAM transfer controller for simple Framebuffer configurations. For more complex configurations an external timing generator and transfer controller is required.

The maximum video clock (VClk) for the GLINT 500TX is 80MHz. The video clock is derived from the video output pixel clock. The pixel clock is divided by the number of serial port interleaved banks. So if the pixel clock is 135MHz and there are 4 serial port interleaved banks, the video clock to the GLINT 500TX will be clocked at 33.75MHz.

Maximum GLINT 500TX video clock rates (assuming 50MHz VRAMs) are shown in table 1-2.

Table 1-2. Maximum Pixel Clock Support

| Pixel Width | Serial Interleave | Maximum Pixel Frequency |
|---|---|---|
| 32 bit | 4 | 200MHz |
| 16 bit | 8 | 400MHz |
| 8 bit | 16 | 800MHz |

## 1.9 External Video Logic Interface

The GLINT 500TX can control external video logic such as the video output LUT-DAC. The address and data lines for the control come from the Localbuffer interface. Control signals are provided to allow standard LUT-DACs to be connected directly to the GLINT 500TX. Some LUT-DACs will require a small amount of glue logic.

## 1.10 Reset Configuration Control

A number of parameters for the GLINT 500TX are set at reset time, such as Localbuffer and Framebuffer memory size and speed. The reset state is configured with resistors connected to the Localbuffer data pins. The state of the data pins is sampled on the rising edge of the reset line. See Reset Control (Section 12) for more details.

## 1.11 Expansion EPROM support

The GLINT 500TX supports an expansion EPROM. This EPROM may store code needed for device-specific initialization and expansion of the boot time code.

## 1.12 GLINT 500TX Address Map

The GLINT 500TX has six PCI base address regions:

Table 1-3. PCI Address Regions

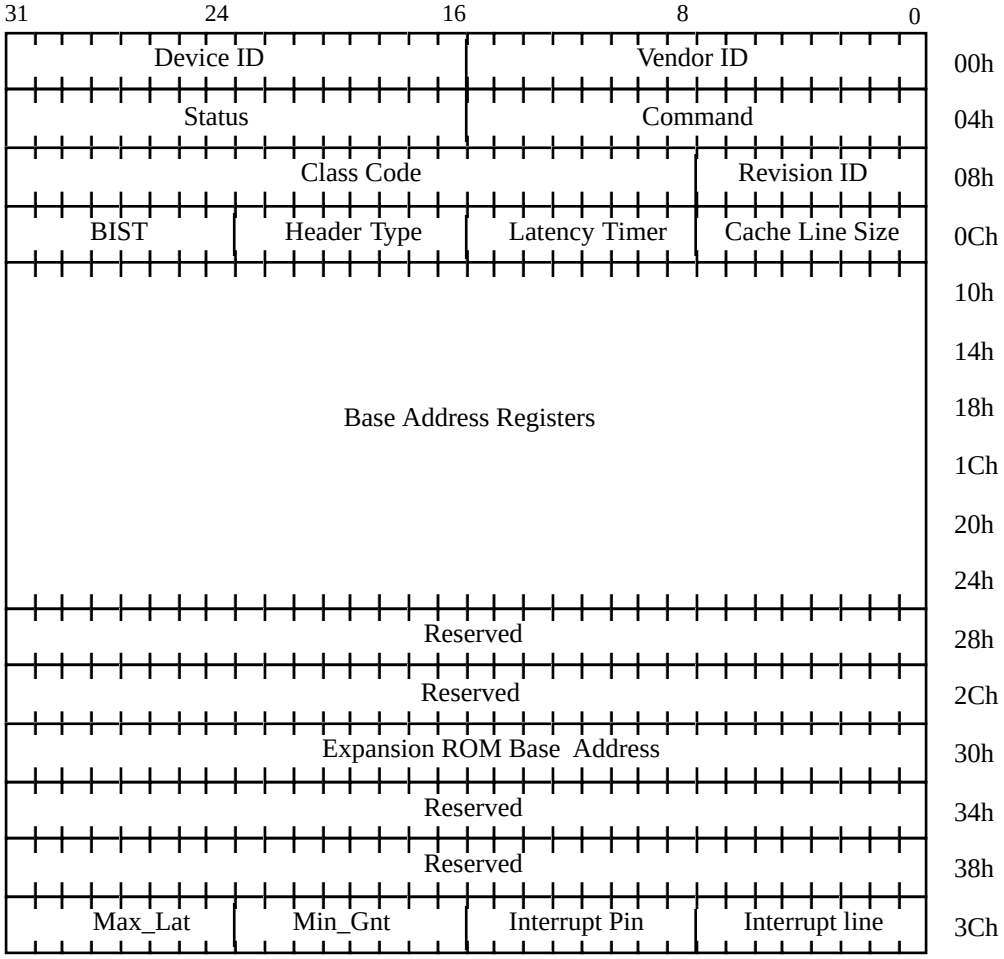
| Region | Description |
|---|---|
| Configuration | PCI configuration region |
| 0 | GC control region |
| 1 | Aperture 0 access to Localbuffer memory |
| 2 | Aperture 0 access to Framebuffer memory |
| 3 | Aperture 1 access to Localbuffer memory |
| 4 | Aperture 1 access to Framebuffer memory |
| ROM | Expansion ROM |

# 2. PCI Configuration Region

The PCI Configuration Region provides at set of 'hooks' which satisfies the needs of current and anticipated system configuration mechanisms. The configuration registers are accessed and modified by the use of Configuration Read and Write commands.

Sixty four bytes of the Configuration registers are predefined within the PCI Specification and are supported by the GLINT 500TX. The remaining 192 Bytes are device specific and are unused by the GLINT 500TX.

Table 2-1. Configuration Region.



## 2.1 Device Identification

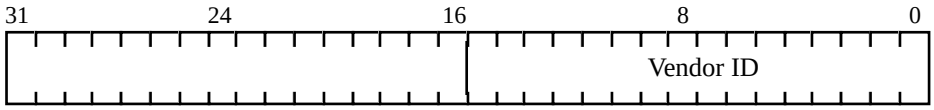
### 2.1.1 Vendor ID

Vendor identification number.

# CFGVendorId CFGVendorId

Region: Config Offset: 00h

Read Only Reset Value: 3D3D




Bits 15-0 3D3Dh

3Dlabs company code

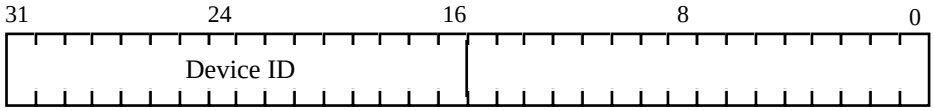
### 2.1.2 Device ID

Device identification number.

# CFGDeviceId CFGDeviceId

Region: Config Offset: 02h

Read Only Reset Value: 0002h




Bits 31-16 0002h

GLINT 500TX Device number

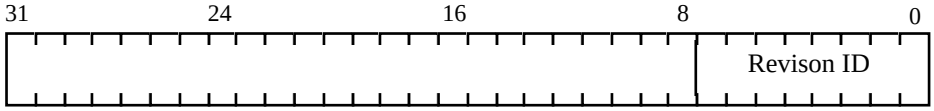
### 2.1.3 Revision ID

Revision identification number.

# CFGRevisionId CFGRevisionId

Region: Config Offset: 08h

Read Only Reset Value: Revision Number




The revision ID register returns the following code:

Bits 7 - 0 Revision

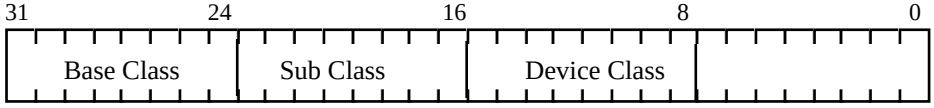
01h = Revision R01

### 2.1.4 Class Code Register

## CFGClassCode CFGClassCode

Region: Config Offset: 09h

Read Only Reset Value: 038000h




Bits 31-24 03h

Base class. PCI Definition: Display controller

Bits 23-16 80h

Sub class. PCI Definition: Other Display controller ( not VGA or XGA)

Bits 15-8 00h

Device class

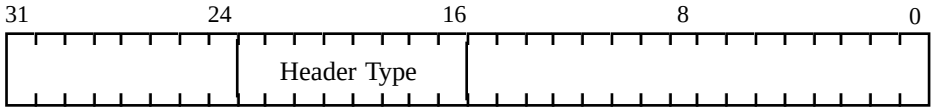
NB. Some OS can expect a device of Class 03h 80h to contain a VGA device and fail to boot correctly if no VGA device is present. GLINT 500 TX has no in-built VGA and this problem can occur. To avoid this problem, setting the 'Base Class Zero' field of the FBMemControl register using a configuration resistor causes the Class Code register to return 00h 00h (Backward Compatability Class). - see section 3.3.1

### 2.1.5 Header Type

## CFGHeaderType CFGHeaderType

Region: Config Offset: 0Eh

Read Only Reset Value: 00h




Bits 23-16 00h

Header Type. PCI Definition: Single function device

## 2.2 Device Control

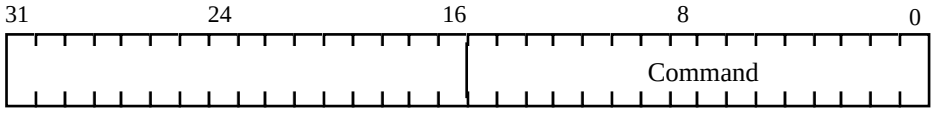
### 2.2.1 Command Register

The command register provides control over a device's ability to generate and respond to PCI cycles. Writing zero to this register disconnects the device from the PCI for all except configuration accesses. The GLINT 500TX supports all necessary bits within the command register for the functionality it contains.

# CFGCommand CFGCommand

Region: Config Offset: 04h

Read/Write Reset Value: 0000h




| | |
|---|---|
| Bit 0 | I/O access enable ( Read Only )<br>0 = GLINT 500TX has no I/O space regions |
| Bit 1 | Memory access enable<br>0 = Disable memory space accesses. ( RESET)<br>1 = Enable memory space accesses |
| Bit 2 | Master enable<br>0 = Disable master accesses. ( RESET)<br>1 = Enable master accesses |
| Bit 3 | Special Cycle access enable ( Read Only )<br>0 = The GLINT 500TX never responds to special cycle accesses. |
| Bit 4 | Memory Write and Invalidate enable ( Read Only )<br>0 = The GLINT 500TX master never issues Memory Write and Invalidate accesses. |
| Bit 5 | VGA palette snoop enable ( Read Only )<br>0 = The GLINT 500TX is not a VGA device. |
| Bit 6 | Parity error report enable ( Read Only )<br>0 = The GLINT 500TX does not report parity error s. |
| Bit 7 | Address/Data stepping enable ( Read Only )<br>0 = The GLINT 500TX does not do stepping. |
| Bit 8 | SERR driver enable( Read Only)<br>0 = The GLINT 500TX does not report parity error s. |
| Bit 9 | Master Fast back-to-back enable( Read Only)<br>0 = The GLINT 500TX master doesn't implement fast back-to-back accesses. |
| Bits 15-10 | Reserved<br>000000b |

## 2.3 Device Status

### 2.3.1 Status Register

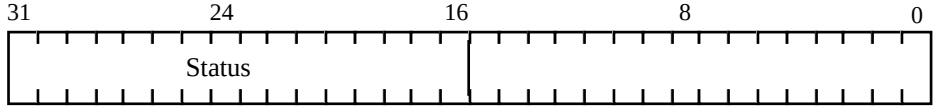
The Status Register is used to record status information for PCI related events. The definition for each bit is given below.

Reads to this register behave normally . Writes function differently in that bits can be reset but not set. A bit is reset whenever the register is written and the data in the corresponding bit location is a 1.

CFGStatus CFGStatus

Region: Config Offset: 06h

Read Only Reset Value: 00h




| | |
|---|---|
| Bits 22-16 | Reserved ( Read Only )<br>0000000b. |
| Bit 23 | Fast back-to-back Transactions ( Read Only)<br>1 = Indicates support for fast back-to-back PCI transactions . |
| Bit 24 | Master Parity check flag ( Read Only)<br>0 = Parity checking not implemented on the GLINT 500TX. |
| Bits 26-25 | 10b ( Read Only )<br>Indicates that the GLINT 500TX asserts DevselN at medium speed. |
| Bit 27 | Target Abort flag( Read Only)<br>0 = The GLINT 500TX never issues a target abort. |
| Bit 28 | Master Target Abort flag<br>Set by master when transaction terminates with target abort. |
| Bit 29 | Master Abort flag<br>Set by master when it terminates transaction with master abort. |
| Bit 30 | SERR flag ( Read Only)<br>0 = Parity checking not implemented on the GLINT 500TX. |
| Bit 31 | PERR flag ( Read Only)<br>0 = Parity checking not implemented on the GLINT 500TX. |

## 2.4 Miscellaneous Functions

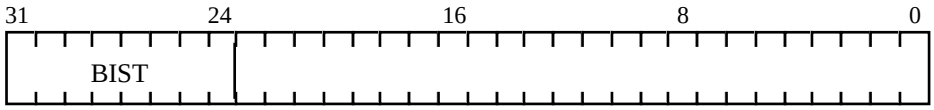
### 2.4.1 BIST

Optional register used for control and status of BIST.

#### CFGBist CFGBist

Region: Config Offset: 0Fh

Read Only Reset Value: 00h




Bits 31-24 BIST

00h. BIST unsupported by GLINT 500TX over the PCI interface.

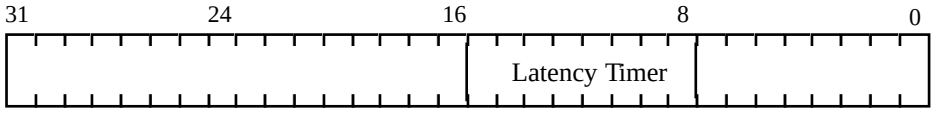
### 2.4.2 Latency Timer

This register specifies, in PCI bus clocks, the value of the Latency Timer for this PCI bus master.

#### CFGLatTimer CFGLatTimer

Region: Config Offset: 0Dh

Read/Write Reset Value: 00h




Bits 15-8 Latency Timer Count

Sets the maximum number of PCI clock cycles for master burst accesses.

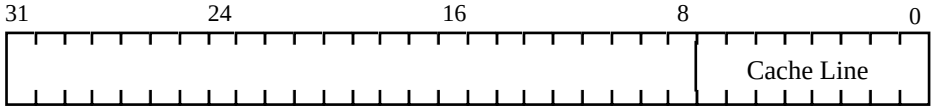
### 2.4.3 Cache Line Size

This register specifies the cache line size in units of 32 bit words. It is only implemented for masters which use the 'Memory write and invalidate' command. The GLINT 500TX does not use this command.

## CFGCacheLine CFGCacheLine

Region: Config Offset: 0Ch

Read Only Reset Value: 00h




Bits 7-0 Cache Line Size

00h. Cache line size unsupported.

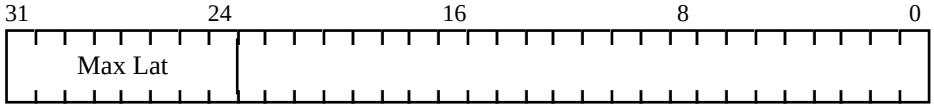
### 2.4.4 Maximum Latency

This register specifies how often the PCI device needs to gain access to the PCI bus.

## CFGMaxLat CFGMaxLat

Region: Config Offset: 3Fh

Read Only Reset Value: Determined by Localbuffer data pins




Bits 31-24 Maximum Latency LB Reset Bits 21-20

Set by the reset value of Localbuffer data pins.
Possible values are: 00h, 40h, 80h, and C0h.

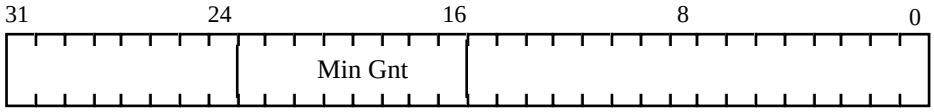
### 2.4.5 Minimum Grant

This register specifies how long a burst period the PCI device needs.

## CFGMinGrant CFGMinGrant

Region: Config Offset: 3Eh

Read Only Reset Value: Determined by Localbuffer data pins




Bits 23-16 Minimum Grant LB Reset Bits 23-22

Set by the reset value of Localbuffer data pins.
Possible values are: 00h, 40h, 80h, and C0h.

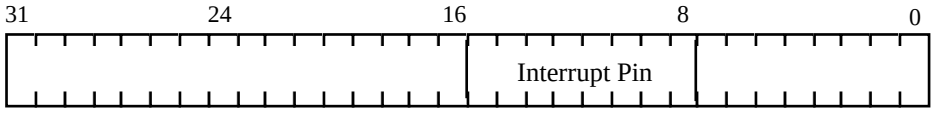
### 2.4.6 Interrupt Pin

The Interrupt Pin register tells the BIOS which interrupt line the GLINT 500TX uses.

## CFGIntPin CFGIntPin

Region: Config Offset: 3Dh

Read Only Reset Value: 01h




Bits 15-8 Interrupt Pin

01h The GLINT 500TX uses Interrupt pin A

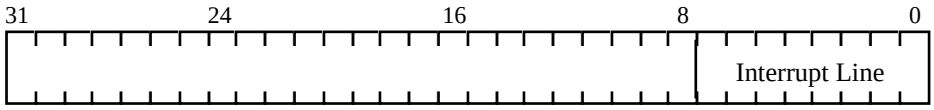
### 2.4.7 Interrupt Line

The Interupt Line register is an 8 bit register used to communicate interrupt line routing information.

## CFGIntLine CFGIntLine

Region: Config Offset: 3Ch

Read/Write Reset Value: 00h




Bits 7-0 Interrupt Line

## 2.5 Base Addresses

The base address registers allow the boot software to relocate PCI devices in the address spaces. At system power-up device independent software must be able to determine what devices are present, build a consistent address map, and determine if a device has an expansion ROM.

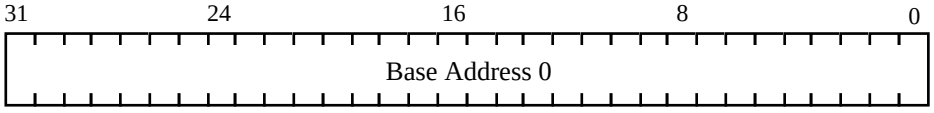
### 2.5.1 Base Address 0 Register

The Base Address 0 Register contains the GLINT 500TX control space offset. The control registers are in memory space. They are not prefetchable and can be located anywhere in 32 bit address space.

# CFGBaseAddr0 CFGBaseAddr0

Region: Config Offset: 10h

Read/Write Reset Value: 0000.0000h




| | | |
|---|---|---|
| Bits 31-17 | Base offset | |
| | Loaded at boot time to set offset of the control register space. | |
| Bits 16-4 | Size indication | Read Only |
| | 000h | Indicates that the control registers must be mapped into 128KBytes. |
| Bits 3-0 | Address Type | Read Only |
| | 0h | Memory Space, not prefetchable, in 32 bit address space |

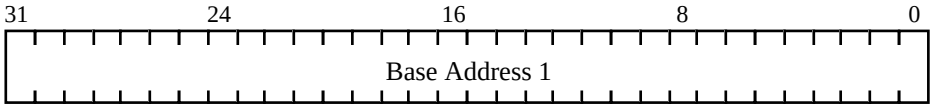
### 2.5.2 Base Address 1 Register

The Base Address 1 Register contains the GLINT 500TX aperture 0 Localbuffer offset. The Localbuffer is in memory space. It is prefetchable and can be located anywhere in 32 bit address space.

## CFGBaseAddr1 CFGBaseAddr1

Region: Config Offset: 14h

Read/Write Reset Value: 0000.0000h




Bits 31-xx Base offset

Loaded at boot time to set offset of the Localbuffer space.

Bits xx-4 Size indication Read Only LB Reset Bits 26-24

0000h Set at reset time by the Localbuffer data pins.
The following sizes are possible: 0M, 1M, 2M, 4M, 8M, 16M, 32M, and 64M Bytes.

Bits 3-0 Address Type Read Only

8h Memory Space, prefetchable, in 32 bit address space

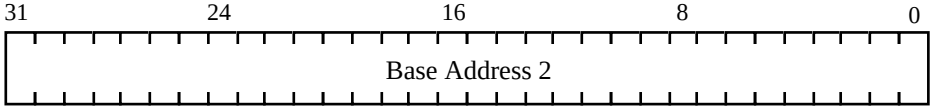
### 2.5.3 Base Address 2 Register

The Base Address 1 register contains the GLINT 500TX aperture 0 Framebuffer offset. The Framebuffer is in memory space. It is prefetchable and can be located anywhere in 32 bit address space.

## CFGBaseAddr2 CFGBaseAddr2

Region: Config Offset: 18h

Read/Write Reset Value: 0000.0000h




Bits 31-xx Base offset

Loaded at boot time to set offset of the Framebuffer space.

Bits xx-4 Size indication Read Only FB Reset Bits 31-29

0000h Set at reset time by the Framebuffer data pins.
The following sizes are possible: 0M, 1M, 2M, 4M, 8M, 16M, and 32M Bytes.

Bits 3-0 Address Type Read Only

8h Memory Space, prefetchable, in 32 bit address space.

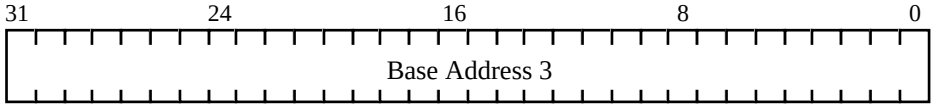
### 2.5.4 Base Address 3 Register

The Base Address 3 Register contains the GLINT 500TX aperture 1 Localbuffer offset. Aperture 1 is always the same size as aperture 0.

## CFGBaseAddr3 CFGBaseAddr3

Region: Config Offset: 1Ch

Read/Write Reset Value: 0000.0000h




Bits 31-xx Base offset

Loaded at boot time to set offset of the Localbuffer space.

Bits xx-4 Size indication Read Only LB Reset Bits 26-24

0000h Set at reset time by the Localbuffer data pins.
The following sizes are possible: 0M, 1M, 2M, 4M, 8M, 16M, 32M, and 64M Bytes.

Bits 3-0 Address Type Read Only

8h Memory Space, prefetchable, in 32 bit address space.

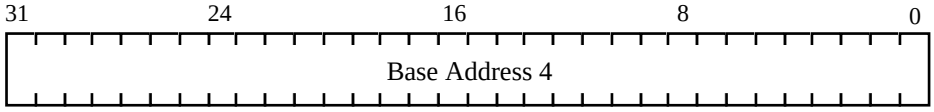
### 2.5.5 Base Address 4 Register

The Base Address 4 register contains the GLINT 500TX aperture 1 Framebuffer offset. Aperture 1 is always the same size as aperture 0.

## CFGBaseAddr4 CFGBaseAddr4

Region: Config Offset: 20h

Read/Write Reset Value: 0000.0000h




Bits 31-xx Base offset

Loaded at boot time to set offset of the Framebuffer space.

Bits xx-4 Size indication Read Only FB Reset Bits 31-29

0000h Set at reset time by the Framebuffer data pins.
The following sizes are possible: 0M, 1M, 2M, 4M, 8M, 16M, and 32M Bytes.

Bits 3-0 Address Type Read Only

8h Memory Space, prefetchable, in 32 bit address space.

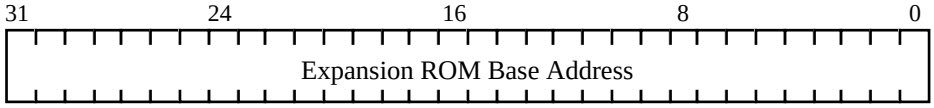
### 2.5.6 Expansion ROM Base Address

The Expansion ROM Base register is the offset address for the expansion ROM. The ROM is in memory space.

## CFGRomAddr CFGRomAddr

Region: Config Offset: 30h

Read/Write Reset Value: 0000.0000h




| | | |
|---|---|---|
| Bits 31-16 | Base offset | |
| | Loaded at boot time to set offset of the Expansion ROM. | |
| Bits 15-11 | Size indication | Read Only |
| | 00h Indicates that the Expansion ROM must be mapped into 64KBytes. | |
| Bits 10-1 | Reserved | Read Only |
| | 000h PCI reserved register bits. | |
| Bit 0 | Access enable | |
| | 0 = Expansion ROM accesses disabled<br>1 = Expansion ROM accesses enabled | |

## 2.6 Expansion ROM Interface

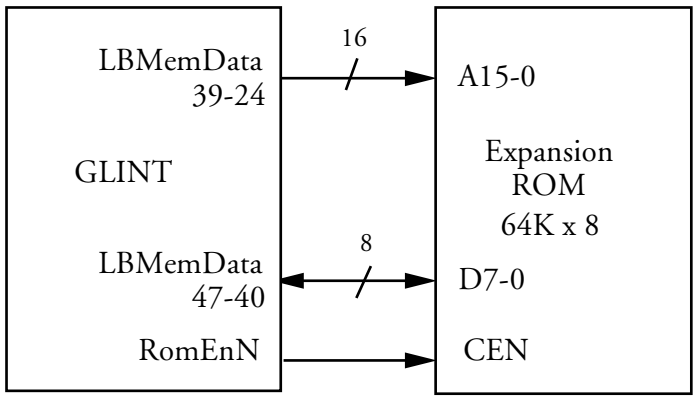
A 64K x 8 bit interface is provided for an expansion ROM. This interface is read only from the PCI .The address and data lines share pins with the localbuffer data bus as defined in table 2-2.

Table 2-2. Expansion ROM Connections

| Signal | Pins used | Description |
|---|---|---|
| RomAddr(15-0) | LBMemData(39-24) | Expansion ROM Address lines. |
| RomData(7-0) | LBMemData(47-40) | Expansion ROM Data bus. |
| RomEnN | RomEnN | Expansion ROM read strobe (negative active) |

Figure 2-1 Expansion ROM interface

Error! Cannot open file.



# 3. Region 0 - Control Registers

## 3.1 Region 0 Address Map

The GLINT 500TX region 0 is a 128KByte region containing the control registers and ports to and from the Graphics Core.

The control space is mapped in twice in the 128KByte region. In the second 64K the registers are mapped to be byte swapped for big endian hosts.

| Offset | Function | Byte Swap Offset |
|---|---|---|
| 0000.0000h<br>-<br>0000.0FFFh | Control Status Registers | 0001.0000h<br>-<br>0001.0FFFh |
| 0000.1000h<br>-<br>0000.17FFh | Localbuffer Registers | 0001.1000h<br>-<br>0001.17FFh |
| 0000.1800h<br>-<br>0000.1FFFh | Framebuffer Registers | 0001.1800h<br>-<br>0001.1FFFh |
| 0000.2000h<br>-<br>0000.2FFFh | GC FIFO Interface | 0001.2000h<br>-<br>0001.2FFFh |
| 0000.3000h<br>-<br>0000.3FFFh | Internal Video Registers | 0001.3000h<br>-<br>0001.3FFFh |
| 0000.3000h<br>-<br>0000.7FFFh | External Video Registers | 0001.3000h<br>-<br>0001.7FFFh |
| 0000.8000h<br>-<br>0000.FFFFh | GC Register Access<br>( Through FIFO ) | 0001.8000h<br>-<br>0001.FFFFh |

Figure 3-1. Region 0 Address Map

### 3.1.1 Reset Status Register

Writing to the reset status register forces a software reset of the GLINT 500TX Graphics Core. The software reset does not reset the PCI interface. It is provided for software diagnostics in case an incorrect register set up locks up the internal GC.

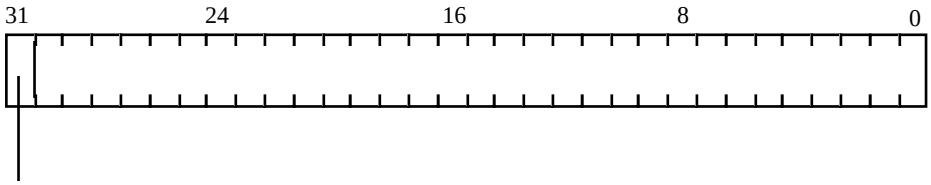
The software reset takes a number of cycles and the GC must not be used during the reset. A flag in the register is provided which shows that the software reset is still in progress.

For more information on the operation of the GLINT 500TX at reset please refer to Reset Control (Section 12).

## ResetStatus ResetStatus

Region: 0 Offset: 0000.0000h

Read/Write Reset Value: 0000.0000h




Software Reset Flag

Bits 30-0 Reserved

Bit 31 Software Reset Flag

0 = The GLINT 500TX is ready for use
1 = The GLINT 500TX is being reset and must not be used

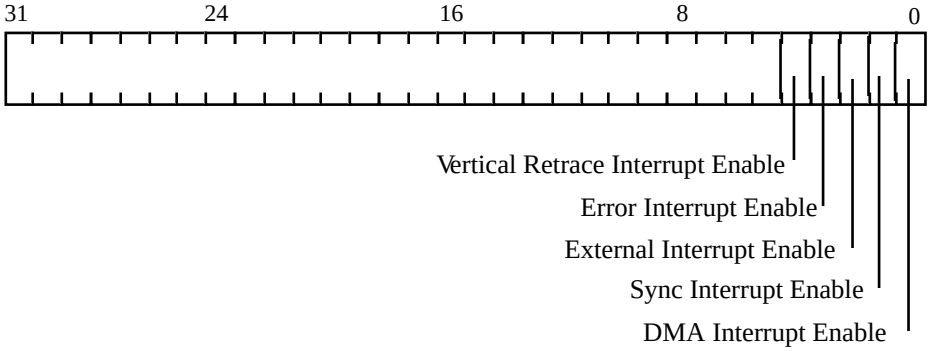
### 3.1.2 Interrupt Enable Register

The Interrupt Enable Register allows for a number of GLINT 500TX flags to generate a PCI interrupt. Five interrupt sources are defined below. At reset all interrupts sources are disabled.

## IntEnable IntEnable

Region: 0 Offset: 0000.0008h

Read/Write Reset Value: 0000.0000h




Bit 0 DMA interrupt enable

0 = Disable interrupt (RESET)
1 = Enable interrupt

Bit 1 Sync interrupt enable

0 = Disable interrupt (RESET)
1 = Enable interrupt

Bit 2 External interrupt enable

0 = Disable interrupt (RESET)
1 = Enable interrupt

Bit 3 Error interrupt enable

0 = Disable interrupt (RESET)
1 = Enable interrupt

Bit 4 Vertical retrace interrupt enable

0 = Disable interrupt (RESET)
1 = Enable interrupt

### 3.1.3 Interrupt Flags Register

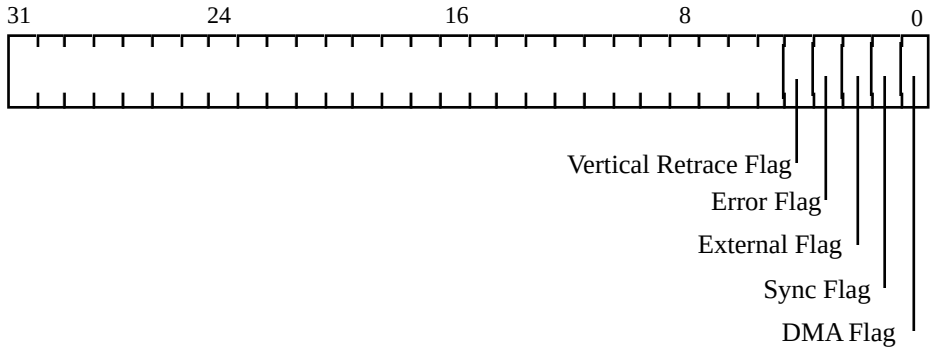
The Interrupt Flags Register shows which interrupts are outstanding on the GLINT 500TX.

Flag bits are reset by writing to this register with the corresponding bit set to a 1. Flags at positions where the bits are set to 0 will be unaffected by the write.

# IntFlags IntFlags

Region: 0 Offset: 0000.0010h

Read/Write Reset Value: 0000.0000h




Bit 0 DMA Flag

0 = No interrupt (RESET)
1 = Interrupt outstanding

Bit 1 Sync Flag

0 = No interrupt (RESET)
1 = Interrupt outstanding

Bit 2 External Flag

0 = No interrupt (RESET)
1 = Interrupt outstanding

Bit 3 Error Flag

0 = No interrupt (RESET)
1 = Interrupt outstanding

Bit 4 Vertical Retrace Flag

0 = No interrupt (RESET)
1 = Interrupt outstanding

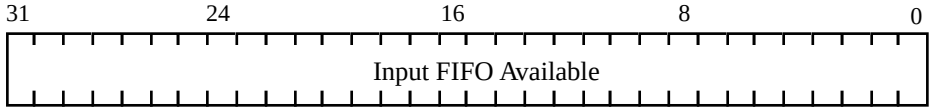
### 3.1.4 Input FIFO Space Register

The input FIFO space register indicates the number of words that can currently be written to the input FIFO. This register can be read at any time and used to allow the controlling software to efficiently send data to the GLINT 500TX. If the DMA controller for the FIFO is in use, the value read is a snapshot of the current FIFO status.

## InFIFOSpace InFIFOSpace

Region: 0 Offset: 0000.0018h

Read Only Reset Value: 0000.0010h




Bits 31-0 Input FIFO Space

Valid range: 0 to 16.
The number of empty words in the input FIFO. This number of words can be written before checking again for FIFO space availability. Although th input FIFO is 32 words deep, the maximum Input FIFO space returned is 16 for compatability with GLINT 300SX.

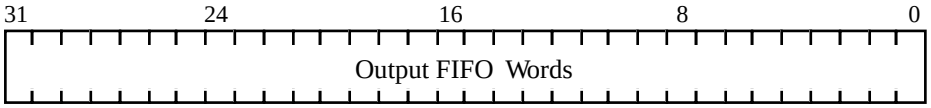
### 3.1.5 Output FIFO Words Register

The output FIFO words register indicates the number of words currently in the output FIFO. This register can be read at any time and used to allow the controlling software to efficiently read output data from the GLINT 500TX.

## OutFIFOWords OutFIFOWords

Region: .0 Offset: 0000.0020h

Read Only Reset Value: 0000.0000h




Bits 31-0 Output FIFO Words

Valid range: 0 to 8.
The number of valid words in the output FIFO. This number of words can be read before checking for more words.

### 3.1.6 DMA Start Address

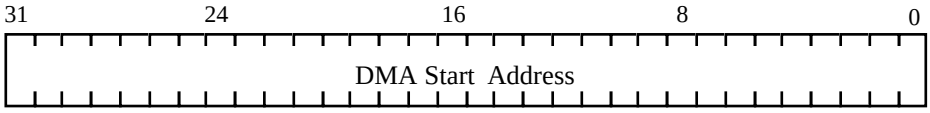
The DMA address should be loaded with the first PCI address for the buffer to be transfered to the GC when using the DMA controller.

Writing to the DMA start address register loads the address into the DMA address counter. Once a DMA has been set off the next DMA start address may be loaded. A read of this register returns the last start value loaded even if the DMA is underway.

## DMAAddress DMAAddress

Region: 0 Offset: 0000.0028h

Read/Write Reset Value: 0000.0000h




Bits 31-0 DMA Start Address

PCI start address for PCI master read transfer to the Graphics Core.

### 3.1.7 DMA Count

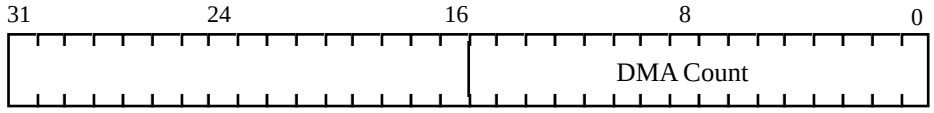
The DMA count register should be loaded with the number of words to be transfered in the DMA operation. The action of loading a word count greater than zero sets off the DMA operation. The value read back from this register indicates the current number of words left to be transfered.

This register should only be written to if the count is zero. It can be read at any time.

## DMACount DMACount

Region: 0 Offset: 0000.0030h

Read/Write Reset Value: 0000.0000h




Bits 15-0 DMA Count

Valid Range: 0 to 65535
Number of words to be transfered in DMA operation.
Undefined action if this register is written to when it is not zero.

### 3.1.8 Error Flags Register

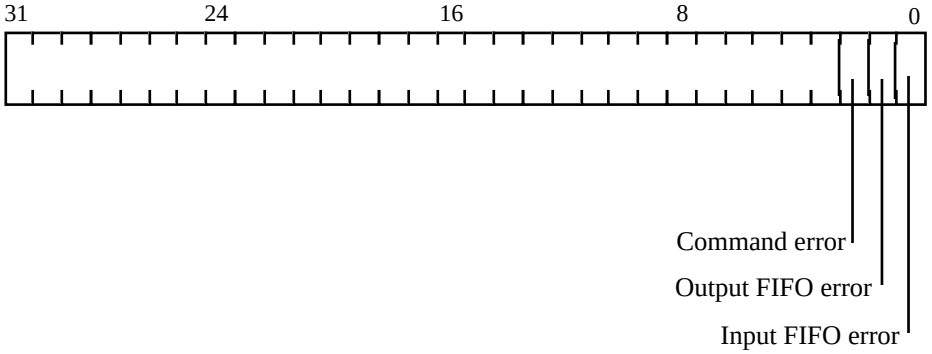
The Error Flags Register shows which errors are outstanding on the GLINT 500TX.

Flag bits are reset by writing to this register with the corresponding bit set to a 1. Flags at positions where the bits are set to 0 will be unaffected by the write.

## ErrorFlags ErrorFlags

Region: 0 Offset: 0000.0038h

Read/Write Reset Value: 0000.0000h




Bit 0 Input FIFO Error Flag

Flag set on write to full input FIFO
0 = No error (RESET)
1 = Error outstanding

Bit 1 Output FIFO Error Flag

Flag set on read from empty output FIFO
0 = No error (RESET)
1 = Error outstanding

Bit 2 Command Error Flag

Flag set on incorrect mixing of accesses to the input FIFO space and the GC register space
0 = No error (RESET)
1 = Error outstanding

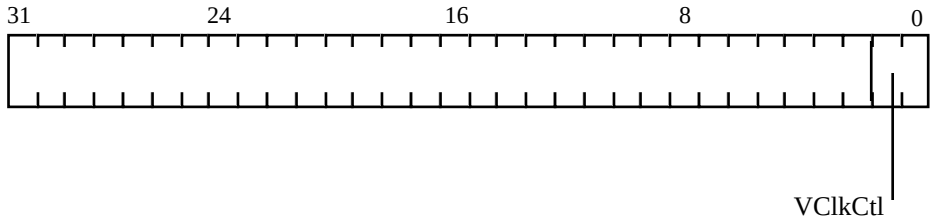
### 3.1.9 Video Clock Control Register

The video clock control Register drives two physical pins on the GLINT 500TX. These pins are used to program the video clock PLL chip.

VClkCtl VClkCtl

Region: 0 Offset: 0000.0040h

Read/Write Reset Value: 0000.0000h




| | |
|---|---|
| Bit 0 | VClkCtl (0) |
| Bit 1 | VClkCtl (1) |

### 3.1.10 Test Register

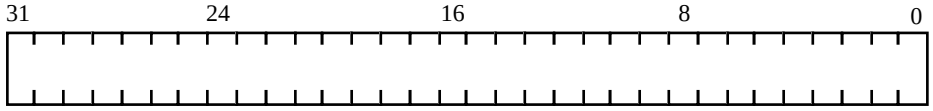
The test register is not to be used by any user software. Writes to this register have an undefined effect.

The GLINT 500TX powers up in functional mode.

## TestRegister TestRegister

Region: 0 Offset: 0000.0048h

Read/Write Reset Value: 0000.0000h




| | |
|---|---|
| Bit 0 | Rasterizer |
| Bit 1 | Scissor Stipple |
| Bit 2 | Color DDA |
| Bit 3 | Fog |
| Bit 4 | Alpha test |
| Bit 5 | LB read |
| Bit 6 | GID Stencil Depth |
| Bit 7 | LB write |
| Bit 8 | FB read |
| Bit 9 | Alpha blend |
| Bit 10 | Dither |
| Bit 11 | Logicops |
| Bit 12 | FB Write |
| Bit 13 | Host out |
| Bit 14 | Texture Address |
| Bit 15 | Texture Read |
| Bit 16 | Texture Color |
| Bit 17 | Router |

### 3.1.11 Aperture 0 Control Register

The aperture 0 control Register sets up the data transfer modes for the Localbuffer visible in region 1 and the Framebuffer in region 2.

The Localbuffer can be set to be byte swapped for big endian hosts.

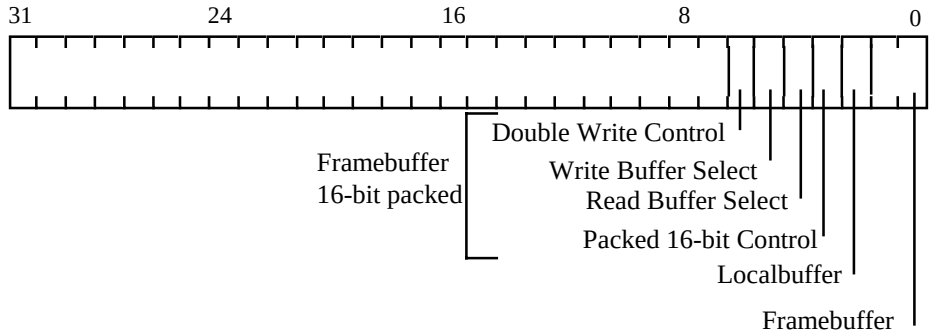
The Framebuffer can be set to be byte swapped and half word swapped for big endian hosts.

The Framebuffer can be used in a mode whereby two 16-bit buffers (A and B) are interleaved together on a per-pixel basis. Each 32bit word contains a 16 bit pixel from buffer A and the equivalent pixel from buffer B. Control bits are provided to allow reading and writing of Buffers A and B as contiguous 16-bit packed buffers, despite their being pixel-interleaved within memory. Each 32-bit read or write access over the PCI bus thus transfers two 16-bit pixels to either Buffer A or Buffer B as selected by the fileds below.

Aperture0 Aperture0

Region: 0 Offset: 0000.0050h

Read/Write Reset Value: 0000.0000h




Bits 1-0 Framebuffer Byte Control

0 = Standard
1 = Byte Swapped
2 = Half Word Swapped
3 = Reserved

Bit 2 Localbuffer Byte control

0 = Standard
1 = Byte Swapped

Bit 3 Packed 16-bit (1:5:5:5:5) Framebuffer Control

Turns on 16-bit packed accesses.

0 = disable packed 16-bit framebuffer
1 = enable packed 16-bit framebuffer

Bit 4 Packed 16-bit Read Buffer Select

0 = select Buffer A for read accesses
1 = select Buffer B for read accesses

Bit 5 Packed 16-bit Write Buffer Select

0 = select Buffer A for write accesses

1 = select Buffer B for write accesses

Bit 6 Packed 16-bit Double Write Control

Allows a write access to be performed to both Buffer A and Buffer B simultaneously.

0 = disable double writes

1 = enable double writes

### 3.1.12 Aperture 1 Control Register

The aperture 1 control Register sets up the data transfer modes for the Localbuffer visible in region 3 and the Framebuffer in region 4.

The Localbuffer can be set to be byte swapped for big endian hosts.

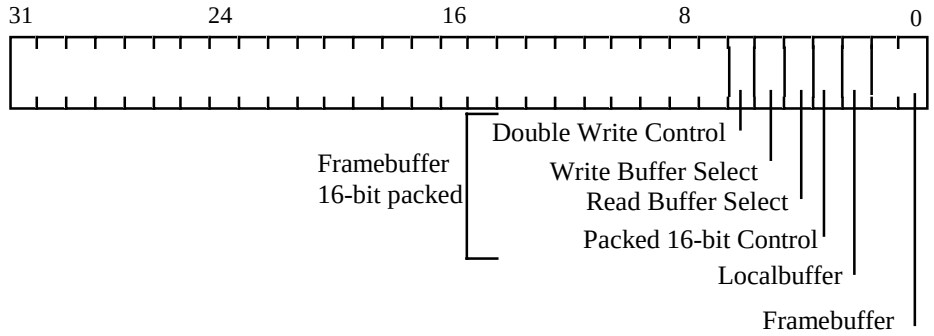
The Framebuffer can be set to be byte swapped and half word swapped for big endian hosts.

The Framebuffer can be used in a mode whereby two 16-bit buffers (A and B) are interleaved together on a per-pixel basis. Each 32bit word contains a 16 bit pixel from buffer A and the equivalent pixel from buffer B. Control bits are provided to allow reading and writing of Buffers A and B as contiguous 16-bit packed buffers, despite their being pixel-interleaved within memory. Each 32-bit read or write access over the PCI bus thus transfers two 16-bit pixels to either Buffer A or Buffer B as selected by the fileds below.

## Aperture1 Aperture1

Region: 0 Offset: 0000.0058h

Read/Write Reset Value: 0000.0000h




Bits 1-0 Framebuffer Byte Control

0 = Standard
1 = Byte Swapped
2 = Half Word Swapped
3 = Reserved

Bit 2 Localbuffer Byte control

0 = Standard
1 = Byte Swapped

Bit 3 Packed 16-bit (1:5:5:5:5) Framebuffer Control

Turns on 16-bit packed accesses.

0 = disable packed 16-bit framebuffer
1 = enable packed 16-bit framebuffer

Bit 4 Packed 16-bit Read Buffer Select

0 = select Buffer A for read accesses
1 = select Buffer B for read accesses

Bit 5 Packed 16-bit Write Buffer Select

0 = select Buffer A for write accesses

1 = select Buffer B for write accesses

Bit 6 Packed 16-bit Double Write Control

Allows a write access to be performed to both Buffer A and Buffer B simultaneously.

0 = disable double writes

1 = enable double writes

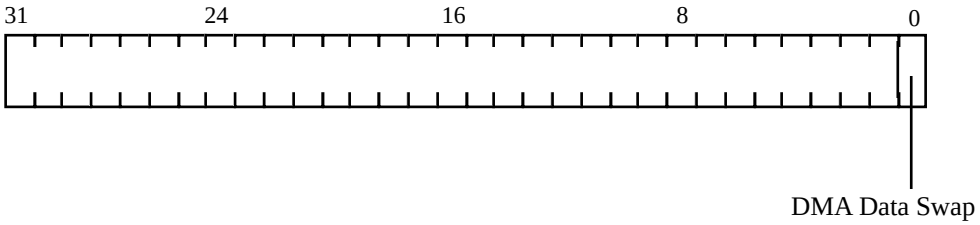
### 3.1.13 DMA Control Register

The DMA control Register sets up the data transfer modes for the DMA controller. Data transfer can be set to byte swapped for big endian hosts.

## DMAControl DMAControl

Region: 0 Offset: 0000.0060h

Read/Write Reset Value: 0000.0000h




Bit 0 DMA Byte Swap Control

0 = Standard

1 = Byte Swapped

## 3.2 Localbuffer Registers

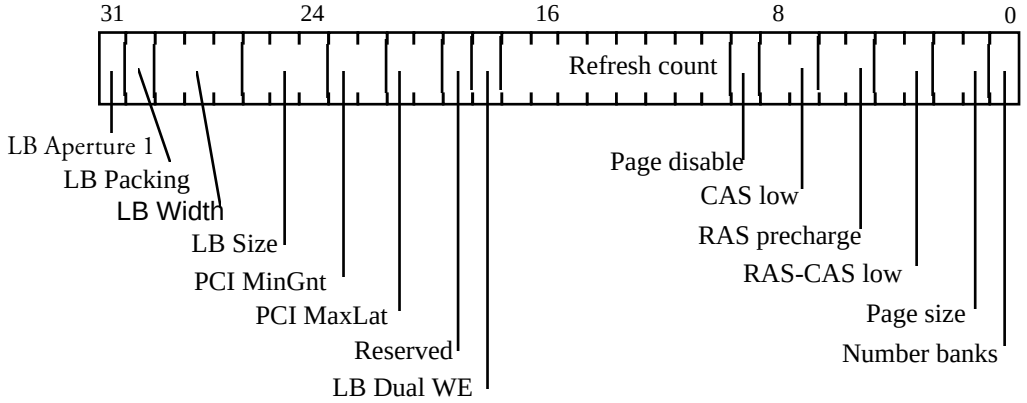
### 3.2.1 Localbuffer Memory Control

The Localbuffer memory control register sets the characteristics of the Localbuffer DRAM. The register is initialised at reset time by setting values on Localbuffer data pins (see Reset Control, Section 12). Care must be taken when modifying this register to ensure that the DRAM will function within its worst case timings.

# LBMemoryCtl LBMemoryCtl

Region: 0 Offset: 0000.1000h

Read/Write Reset Value: Determined by Localbuffer data pins




Bit 0 Number of banks LB Reset Bit 0

Defines the number of banks of CAS interleaved memory in the localbuffer.

0 = 1 bank
1 = 2 banks

Bits 2-1 Page size LB Reset Bits 2-1

Defines the page size of the DRAM of the memory in the localbuffer. If there are 2 banks of memory, the effective page size is twice this value.

0 = 256 pixels
1 = 512 pixels
2 = 1024 pixels
3 = 2048 pixels

Bits 4-3 RAS-CAS low LB Reset Bits 4-3

Defines the number of MClks that RAS is asserted before CAS is asserted during a memory access.

0 = 2 clocks
1 = 3 clocks
2 = 4 clocks
3 = 5 clocks

Bits 6-5 RAS precharge LB Reset Bits 6-5

Defines the RAS prechareg time in terms of MClk periods.

0 = 2 clocks
1 = 3 clocks

2 = 4 clocks
3 = 5 clocks

| | | | |
|---|---|---|---|
| Bits 8-7 | CAS low | | LB Reset Bits 8-7 |

Defines the CAS low time during a localbuffer access in terms of MClk periods.

0 = 1 clock
1 = 2 clocks
2 = 3 clocks
3 = 4 clocks

| | | | |
|---|---|---|---|
| Bit 9 | Page mode disable | | LB Reset Bit 9 |

Asserting this bit will cause all localbuffer accesses to perform a full DRAM memory cycle. i.e. Fast Page mode is never used.

0 = Page mode enabled
1 = Page mode disabled

| | | | |
|---|---|---|---|
| Bits 17-10 | Refresh count | | |

This field can be used to optimise the DRAM refresh period to the system MClk and the DRAM used for the localbuffer. The refresh period is the value of this field x 16 x MClk period . The Reset value is 20h.

| | | | |
|---|---|---|---|
| Bit 18 | Localbuffer dual Write enables | Read Only | LB Reset Bit 18 |

x16 DRAM parts come with either 2CAS line and 1 WE line or 1CAS line and 2 WE. The preferred memory parts for GLINT dual CAS lines, however asserting this bit field allows Dual WE parts to be used. In this case, the LBMemCasN lines should be connected to the DRAM WE lines, and the LBMemWeN lines should be connected to the DRAM CAS lines. When x4 or x8 parts are used, this bit should not be set.

0 = Dual CAS
1 = Dual Write Enables

| | | | |
|---|---|---|---|
| Bit 19 | Reserved | Read Only | LB Reset Bit 19 |
| Bits 21-20 | PCI Maximum Latency | Read Only | LB Reset Bits 21-20 |

Form the top 2 bits of the configuration space Maximum Latency register

| | | | |
|---|---|---|---|
| Bits 23-22 | PCI Minimum Grant | Read Only | LB Reset Bits 23-22 |

Form the top 2 bits of the configuration space Minimum Grant register

| | | | |
|---|---|---|---|
| Bits 26-24 | Localbuffer visible region size | Read Only | LB Reset Bits 26-24 |

0 = 1 MByte
1 = 2 MBytes
2 = 4 MBytes
3 = 8 MBytes
4 = 16 MBytes
5 = 32 MBytes
6 = 64 MBytes
7 = 0 MBytes

| | | | |
|---|---|---|---|
| Bits 29-27 | Localbuffer width | Read Only | LB Reset Bits 29-27 |

0 = 16 Bit
1 = 18 Bit
2 = 24 Bit
3 = 32 Bit
4 = 36 Bit
5 = 40 Bit
6 = 48 Bit
7 = Other width

| | | | |
|---|---|---|---|
| Bit 30 | Localbuffer Bypass Packing<br>0 = 64 bit Localbuffer bypass step<br>1 = 32 bit Localbuffer bypass step | Read Only | LB Reset Bit 30 |
| Bit 31 | Second Localbuffer aperture<br>0 = Disabled<br>1 = Enabled | Read Only | LB Reset Bit 31 |

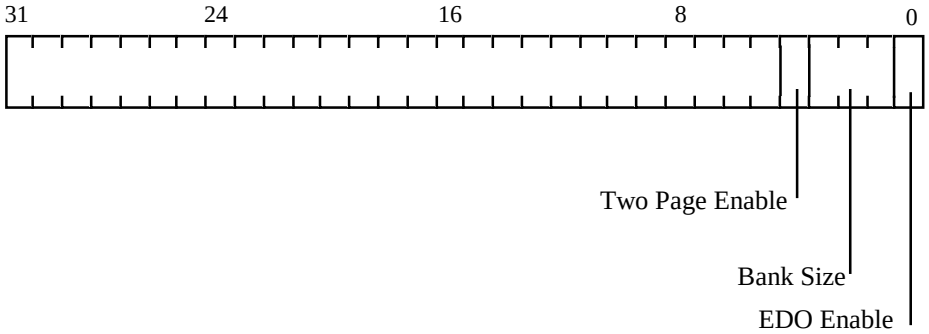
### 3.2.1 Localbuffer Memory EDO

The Localbuffer memory EDO register enables and controls the use of EDO DRAM for the Localbuffer and controls the number of page detectors used to control the Localbuffer.

## LBMemoryEDO LBMemoryEDO

Region: 0 Offset: 0000.1008h

Read/Write Reset Value: 0000.0000h




Bit 0 EDO enable

Enables EDO functionality in the localbuffer.

0 = EDO disabled (RESET)
1 = EDO enabled

Bits 2-1 Bank Size

Defines the page size of the DRAM of the memory in the localbuffer. If there are 2 banks of memory, the effective page size is twice this value.

0 = Second memory bank disabled (RESET)
1 = Second bank starts at 256K pixels
2 = Second bank starts at 512K pixels
3 = Second bank starts at 1M pixels
4 = Second bank starts at 2M pixels
5 = Second bank starts at 4M pixels
6 = Second bank starts at 8M pixels
7 = Reserved

Bit 3 Two Page enable

Enables a separate page detectors for each bank of memory .

0 = Single Page detector (RESET)
1 = Two Page Detectors Enabled

Note bits 31 to 20 of this register return bits 31 to 20 of the LBMemoryCtl register when read.

## 3.3 Framebuffer Registers

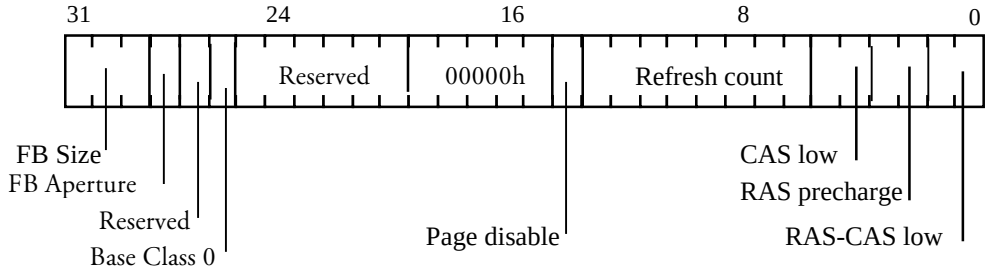
### 3.3.1 Framebuffer Memory Control

The Framebuffer memory control register sets the characteristics of the Framebuffer VRAM. The register is initialised at reset time by setting values on Localbuffer data pins (see Reset Control, Section 12). Care must be taken when modifying this register to ensure that the VRAM will function within its worst case timings.

# FBMemoryCtl FBMemoryCtl

Region: 0 Offset: 0000.1800h

Read/Write Reset Value: Determined by Framebuffer data pins




Bits 1-0 RAS-CAS low FB Reset Bits 1-0

Defines the period from RAS asserted to CAS asserted during a framebuffer access in terms of MClks.

0 = 2 clocks
1 = 3 clocks
2 = 4 clocks
3 = 5 clocks

Bits 3-2 RAS precharge FB Reset Bits 3-2

Defines the RAS precharge period in MClks.

0 = 2 clocks
1 = 3 clocks
2 = 4 clocks
3 = 5 clocks

Bits 5-4 CAS low FB Reset Bits 5-4

Determines the CAS active time during a framebuffer memory access.

0 = 1 clock
1 = 2 clocks
2 = 3 clocks
3 = 4 clocks

Bit 13-6 Refresh count

This field can be used to optimise the VRAM refresh period to the system MClk and the VRAM used for the framebuffer. The refresh period is the value of this field x 16 x MClk period.

Reset value 20h

| | | | |
|---|---|---|---|
| Bit 14 | Page mode disable | | FB Reset Bit 6 |
| | Asserting this bit will cause all framebuffer accesses to perform a full VRAM memory cycle. i.e. Fast Page mode is never used.<br>0 = Page mode enabled<br>1 = Page mode disabled | | |
| Bits 19-15 | 00000h Read only | | |
| Bits 21-20 | Reserved | | |
| Bit 22 | EDO DRAM | | FB Reset Bit 22 |
| | This field is for informational purposes only and can be used to correctly configure the Localbuffer through sotfware.<br>0 = Fast Page Mode DRAM fitted for Localbuffer<br>1 = EDO DRAM fitted for Localbuffer | | |
| Bits 25-23 | Reserved | FB Reset Bits 25-23 | |
| Bit 26 | Base Class Zero | Read only | FB Reset Bit 26 |
| | 0 = GLINT 500TX returns a PCI Base class and sub-class of 03h 80h<br>1 = GLINT 500 TX returns a PCI Base Class and sub-Class of 00h 00h<br>See section 2.1.4 | | |
| Bit 27 | Reserved | Read only | FB Reset Bit 27 |
| Bit 28 | Framebuffer Aperture 1 Enable | Read only | FB Reset Bit 28 |
| Bits 31-29 | Framebuffer Visible Region Size | Read only | FB Reset Bits 31-29 |
| | 0 = 1 MByte<br>1 = 2 MBytes<br>2 = 4 MBytes<br>3 = 8 MBytes<br>4 = 16 MBytes<br>5 = 32 MBytes<br>6 = Reserved<br>7 = 0 MBytes | | |

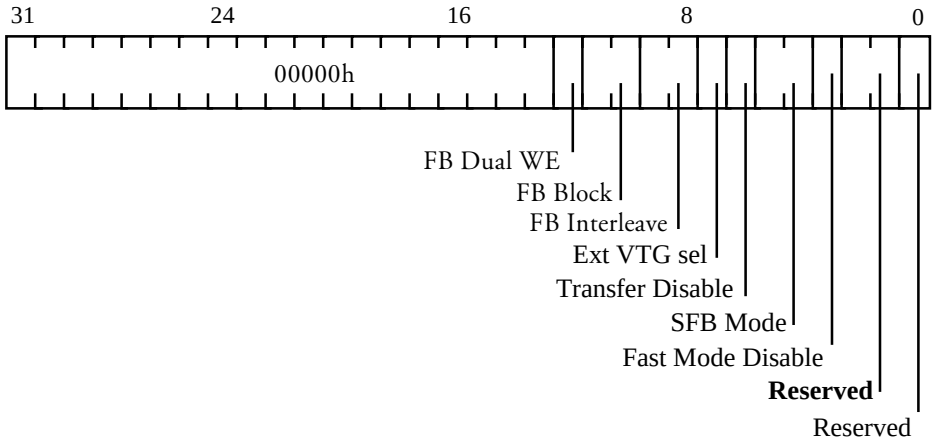
### 3.3.2 Framebuffer Mode Select

The Framebuffer mode select register sets the mode of the Framebuffer VRAM. The register is initialised at reset time by setting values on Localbuffer data pins (see Reset Control, Section 12).

## FBModeSel FBModeSel

Region: 0 Offset: 0000.1808h

Read/Write Reset Value: Determined by Framebuffer data bits




Bit 0 Framebuffer Width Read Only

This field always returns the value 1 indicating that the Framebuffer width is 64 bits for backward compatibility with the GLINT 300SX.

Bits 2-1 Reserved

This field always returns the value 3.

Bit 3 Fast Mode Disable FB Reset Bit 10

Setting this field turns off some of the memory access optimisations.

0 = Fast mode enabled
1 = Fast mode disabled

Bit 5-4 Shared Framebuffer Mode Read only FB Reset Bits 12-11

If TX Enhanced mode is not set, this 2 bit field detimes the Shared Framebuffer mode.

0 = Disabled
1 = Arbiter ( Primary controller)
2 = Requester ( Secondary controller)
3 = Reserved

This is compatible with GLINT 300SX.

In TX enhanced mode is set , then this field is used in conjunction with the TX Enhanced Shared Memory and SFBModeSwap fields of the TX Shared Memory Control register to determine Shared memory control. See section XXX for more details

Bit 6 Transfer disable FB Reset Bit 13

0 = Video memory transfer cycles enabled
1 = Video memory transfer cycles disabled

| | | |
|---|---|---|
| Bit 7 | External VTG Select | FB Reset Bit 14 |

0 = Select internal Video Timing Generator
1 = Select external Video Timing Generator

| | | |
|---|---|---|
| Bits 9-8 | Framebuffer interleave | FB Reset Bits 16-15 |

This field determines how many interleaved banks of memory are available. e.g. Framebuffer Width = 1 and Framebuffer Interleave = 1 means 2 x64bit banks of memory interleaved by CAS.

0 = 1 way
1 = 2 way
2 = 4 way
3 = Reserved

| | | |
|---|---|---|
| Bits 11-10 | Framebuffer block fill size | FB Reset Bits 18-17 |

The field is used by the memory controller to perform VRAM block fill and relects the block fill size of an individual VRAM. It can be used by the software in conjunction with the values in the Framebuffer Width field and the Framebuffer Interleave field to determine the actual block fill size available to GLINT.

. 0 = Block fill unsupported
1 = 4 pixel per VRAM block fill
2 = 8 pixel per VRAM block fill
3 = Reserved

| | | |
|---|---|---|
| Bit 12 | Framebuffer Dual Write Enables | FB Reset Bit 19 |

x16 VRAM parts come with either 2 CAS line and 1 WE line or 1CAS line and 2 WE. The preferred memory parts for GLINT have dual CAS lines, however asserting this bit field allows Dual WE parts to be used. In this case, the FBMemCasN lines should be connected to the VRAM WE lines, and the FBMemWeN lines should be connected to the VRAM CAS lines. When x4 or x8 parts are used, this bit should not be set.

0 = Dual CAS VRAMs
1 = Dual WE VRAMs

Bits 31-13 00000h

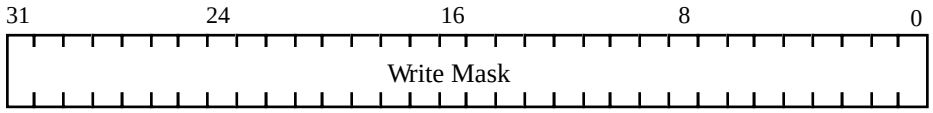
### 3.3.3 Framebuffer Graphics Core Write Mask

The Framebuffer GC write mask register is a read only register to allow the current Graphics Core write mask to be read. This register is for diagnostic purposes only.

FBGCWrMask FBGCWrMask

Region: 0 Offset: 0000.1810h

Read Reset Value: FFFF.FFFFh




Bits 31-0 Graphics Core Write Mask

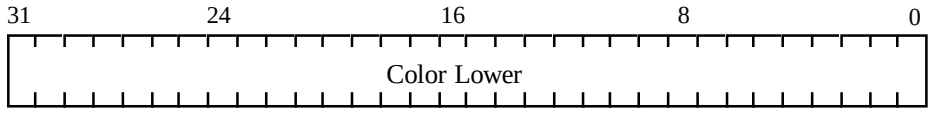
### 3.3.4 Framebuffer Graphics Core Color Lower

The Framebuffer GC color lower register is a read only register to allow the current Graphics Core color low 32 bits to be read. This register is for diagnostic purposes only.

FBGCColorLower FBGCColorLower

Region: 0 Offset: 0000.1818h

Read Reset Value: XXXX.XXXXh




Bits 31-0 Graphics Core Color Mask

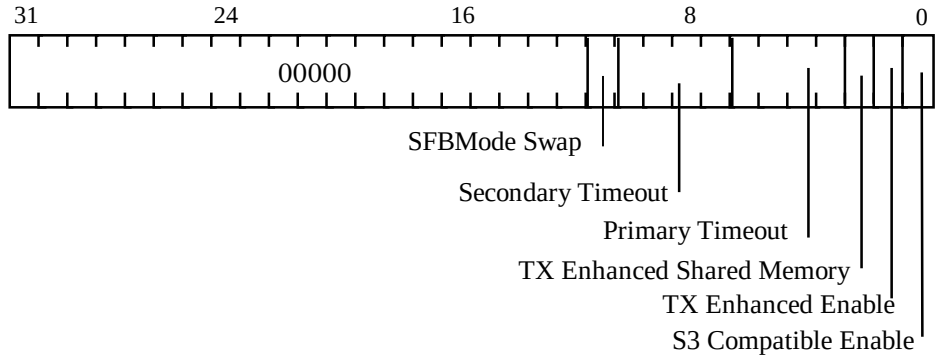
### 3.3.5 Framebuffer TX Shared Memory Control

The Framebuffer TX shared memory control register sets the characteristics of shared framebuffer interface for the GLINT 500TX..

## FBTXMemCtl FBTXMemCtl

Region: 0 Offset: 0000.1820h

Read/Write Reset Value: Determined by TX Control Pin




Bit 0 S3 Compatible Enable

Sets the Framebuffer memory controller to be compatible with the S3 964/968

Bit 1 TX Enhanced Enable Read Only TX Control Pin

Indicates that certain GLINT 500TX enhanced features are available

Bit 2 TX Enhanced Shared Memory Read Only FB Reset Bit 20

This bit can only be set if the TXEnhanced pin is pulled high.

In TX enhanced mode this value is used together with the Shared Framebuffer Mode bits in the FBModeSel register and the SFBModeSwap field to determine the Shared Memory configuration.See Section XXXX.

Bits 6-3 Primary Timeout

This 4 bit field provides a timeout count for the Shared Memory arbiter. When GLINT 500TX is a primary controller it will ignore requests from the secondary controller until the timeout counter has reached zero. The timeout period is Mclk x 16 .

Reset value 0h

Bits 10-7 Secondary Timeout

This 4 bit field provides a timeout counter for the Shared Memory arbiter. When GLINT 500TX is a primary controller, the timout counter is used to gate requests from the GLINT 500TX for the memory bus when the secondary controller has the bus. The timeout period is Mclk x 16.

Reset value 0h

Bit 11 SFBModeSwap Read Only FB Reset Bit 21

In TX enhanced mode this value is used together with the Shared Framebuffer Mode bits in the FBModeSel register and the TXEnhanced SharedMemory field to determine the Shared Memory configuration.See Section XXXX.

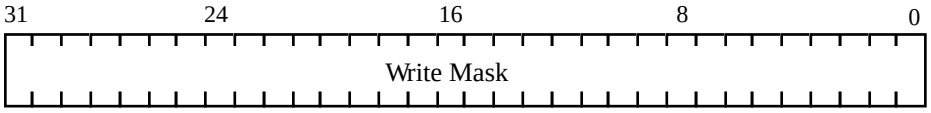
### 3.3.6 FramebufferBypass Write Mask

The Framebuffer write mask register defines the hardware write used for bypass accesses.

## FBWrMask FBWrMask

Region: 0 Offset: 0000.1830h

Read Reset Value: FFFF.FFFFh




Bits 31-0 Graphics Core Write Mask

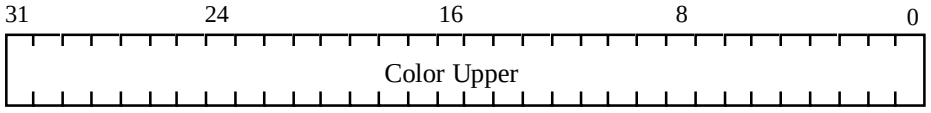
### 3.3.7 Framebuffer Graphics Core Color Upper

The Framebuffer GC color upper register is a read only register to allow the current Graphics Core color high 32 bits to be read. This register is for diagnostic purposes only.

## FBGCColorUpper FBGCColorUpper

Region: 0 Offset: 0000.1838h

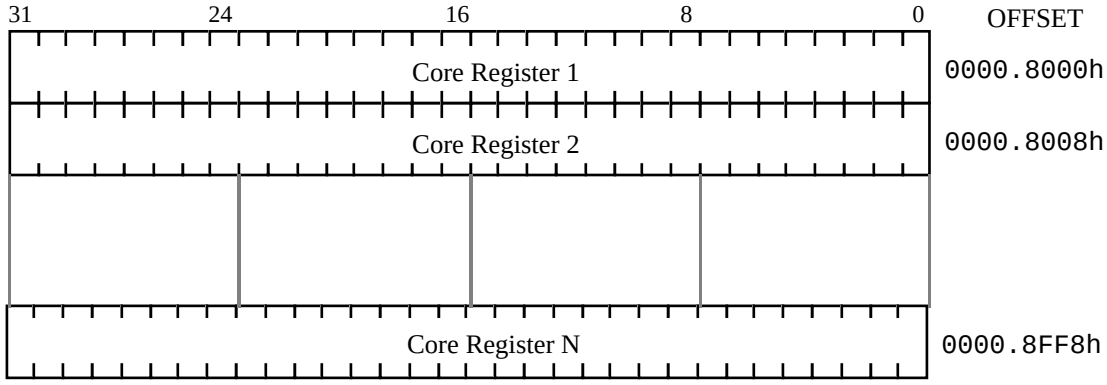
Read Reset Value: XXXX.XXXXh




Bits 31-0 Graphics Core Color Upper

## 3.4 Graphics Core Registers

All the Graphics Core registers in the GLINT 500TX are addressed in this part of region 0. The address for each register and associated data fields is defined in the GLINT Programmers Reference Manual.




Note. Not all the available register locations are used within the Graphics Core. The registers are on 64 bit boundaries.

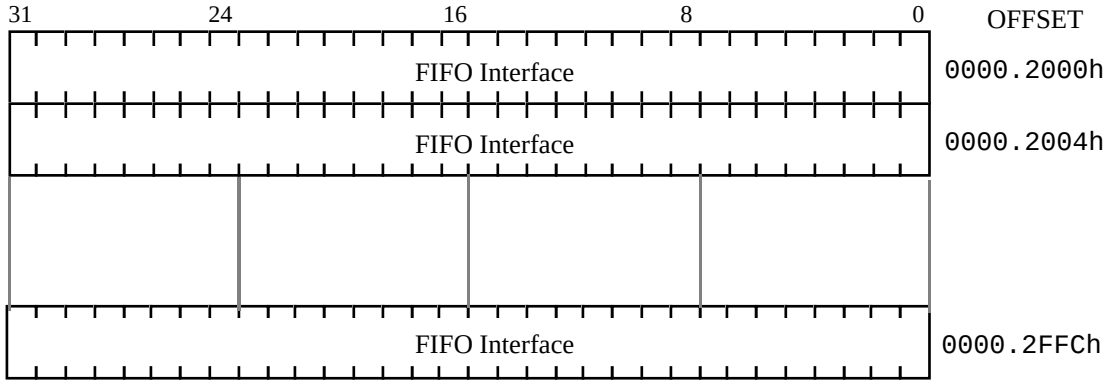
## 3.5 Graphics Core FIFO Interface

The Graphics Core FIFO interface provides a port through which both GC register addresses and data can be sent to the input FIFO. A range of 4 KBytes of host space is provided although all data may be sent through one address in the range. ALL accesses go directly to the FIFO, the range is provided to allow for data transfer schemes which force the use of incrementing addresses. Before writing to the input FIFO the user must check that there is sufficient space by reading the InFIFOSpace register.

If the FIFO interface is used, then data is typically sent to the GLINT 500TX in pairs, an address word which addresses the register to be updated, followed by the data to be sent to the register. Note that the GC registers can not be read through this interface. Command buffers generated to be sent to the input FIFO interface may be read directly by the GLINT 500TX by using the DMA controller.

A data formatting scheme is provided to allow for multiple data words to be sent with one address word where adjacent or grouped registers are being written, or where one register is to be written many times.

For more information on the direct FIFO interface data buffer formats please refer to the GLINT Programmers Reference Manual.




Note. The FIFO interface can be accessed at 32 bit boundaries. This is to allow a direct copy from a DMA format buffer.

Error! Cannot open file.

# 4. Internal Video Timing Generator

GLINT 500TX provides a timing generator to enable a complete framebuffer to be implemented with just the addition of VRAM , video clock generator and a suitable RAMDAC. The timing generator produces appropriate Horizontal and Vertical Syncs and Blanks from an external video clock. It controls the instigation of VRAM transfer cycles in the FrameBuffer Interface and provides the VRAM transfer addresses. It also controls the VRAM serial clocks and serial output enables.

It is anticipated that GLINT 500TX will be used with more complex framebuffers than the internal timing generator can drive. For this reason, the timing generator can be disabled and the FrameBuffer Interface can be controlled by external circuitry to generate VRAM transfer cycles.

The timing generator is controlled through a series of registers accessible from the PCI bus. There is no access to the timing generator from the GLINT 500TX core.

The timing generator operates entirely from a video clk (VClk). Suitable internal resynchronisation occurs between the timing generator and both the PCI interface (PCIClk) and the FrameBuffer Interface (MClk).

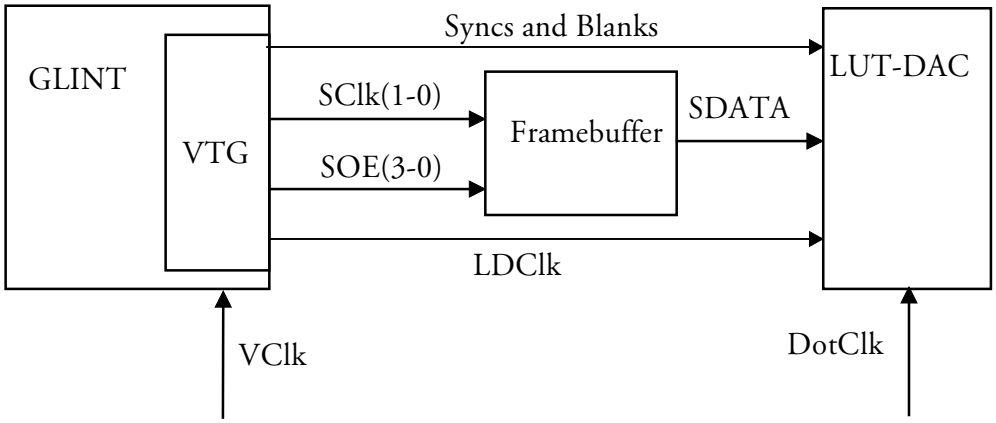



Figure 4-1. Video Timing Generator

## 4.1 Overview of Internal VTG features

- Generates VSync, HSync, CompositeBlank, CompositeSync, all with programmmable polarity.
- 12 bit horizontal and vertical counters.
- Video clock of up to 80 MHz.
- Linearly mapped framebuffer.
- VRAMs with split transfer required.
- VRAMs with and without QSF.
- Programmable size of VRAM split register - 128 or 256.

- Programmable transfer address at start of frame for double buffering support.
- 1, 2 or 4 way Interleaving of VRAM serial outputs.

## 4.2 Internal VTG Register Set

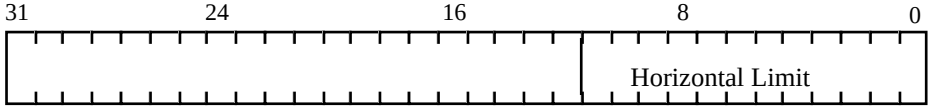
### 4.2.1 Horizontal Limit

The Horizontal Limit register defines the horizontal period of the video display. The internal horizontal counter is clocked by VClk. This counter starts at 1 , counts to the value set in the Horizontal Count limit register and resets to 1 again.

VTGHLimit VTGHLimit

Region: 0 Offset: 0000.3000h

Read/Write Reset Value: 001h




Bits 11-0 Horizontal Limit

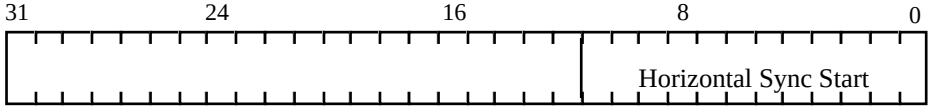
### 4.2.2 Horizontal Sync Start Register

The Horizontal Sync starts when the internal Horizontal Counter reaches the value stored in the Horizontal Sync Start register.

VTGHSyncStart VTGHSyncStart

Region: 0 Offset: 0000.3008h

Read/Write Reset Value: XXXh




Bits 11-0 Horizontal Sync Start

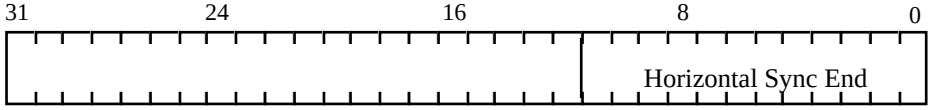
### 4.2.3 Horizontal Sync End

The Horizontal Sync ends when the internal Horizontal Counter reaches the value stored in the Horizontal Sync End register.

VTGHSyncEnd VTGHSyncEnd

Region: 0 Offset: 0000.3010h

Read/Write Reset Value: XXXh




Bits 11-0 Horizontal Sync End

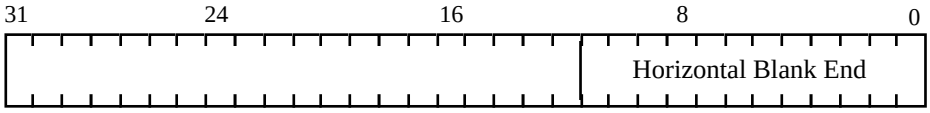
### 4.2.4 Horizontal Blank End

The Horizontal Blank starts when the internal Counter is reset to 1. The Horizontal Blank ends when the internal Horizontal Counter reaches the value stored in the Horizontal Blank End register.

## VTGHBlankEnd VTGHBlankEnd

Region: 0 Offset: 0000.3018h

Read/Write Reset Value: XXXh




Bits 11-0 Horizontal Blank End

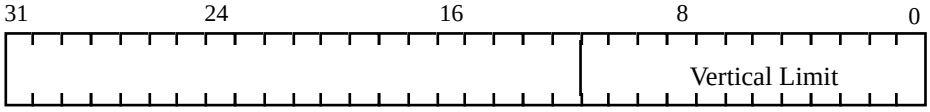
### 4.2.5 Vertical Limit

The Vertical Limit register defines the vertical period of the video display. The internal vertical counter is clocked by VClk at the start of every Horizonal line. This counter starts at 1 , counts to the value set in the Vertical Count limit register and resets to 1 again.

## VTGVLimit VTGVLimit

Region: 0 Offset: 0000.3020h

Read/Write Reset Value: 001h




Bits 11-0 Vertical Count

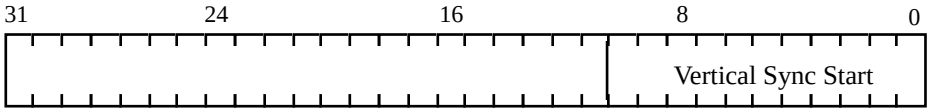
### 4.2.6 Vertical SyncStart

The Vertical Sync starts when the internal Vertical Counter reaches the value stored in the Vertical Sync Start register.

## VTGVSyncStart VTGVSyncStart

Region: 0 Offset: 0000.3028h

Read/Write Reset Value: XXXh




Bits 11-0 Vertical Sync Start

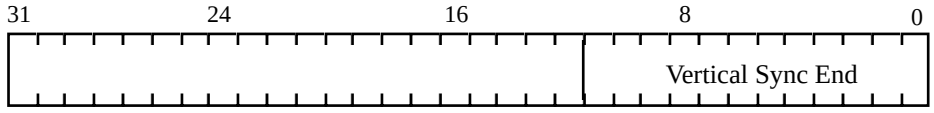
### 4.2.7 Vertical Sync End

The Vertical Sync ends when the internal Vertical Counter reaches the value stored in the Vertical Sync End register.

## VTGVSyncEnd VTGVSyncEnd

Region: 0 Offset: 0000.3030h

Read/Write Reset Value: XXXh




Bits 11-0 Vertical Sync End

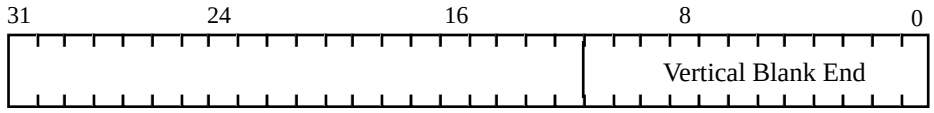
### 4.2.8 Vertical Blank End

The Vertical Blank ends when the internal Vertical Counter reaches the value stored in the Vertical Blank End register.

## VTGVBlankEnd VTGVBlankEnd

Region: 0 Offset: 0000.3038h

Read/Write Reset Value: XXXh




Bits 11-0 Vertical Blank End

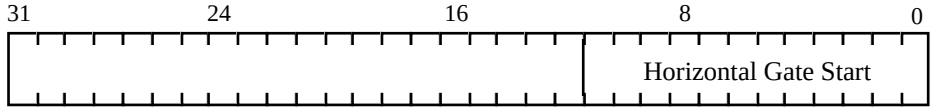
### 4.2.9 Horizontal Gate Start

The Horizontal Gate is an internal signal used to gate the VRAM serial clocks SClk0 and SClk1. Between HGate Start and HGate End, the serial clocks are enabled. The Horizontal Gate is typically set to the inverse of Horizontal Blank with a possible shift to allow for external delays in the Blank and serial clock/data paths. The internal Horizontal Gate signal starts when the internal Horizontal Counter matches Horizontal Gate Start register.

## VTGHGateStart VTGHGateStart

Region: 0 Offset: 0000.3040h

Read/Write Reset Value: XXXh




Bits 11-0 Horizontal Gate Start

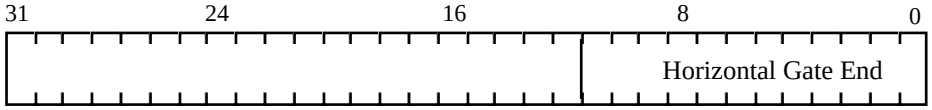
### 4.2.10 Horizontal Gate End

The internal Horizontal Gate signal ends when the internal Horizontal Counter matches the Horizontal Gate End register.

## VTGHGateEnd VTGHGateEnd

Region: 0 Offset: 0000.3048h

Read/Write Reset Value: XXXh




Bits 11-0 Horizontal Gate End

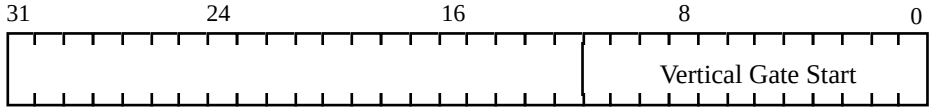
### 4.2.11 Vertical Gate Start

The internal Vertical Gate signal is used to reset the VRAM transfer cycle controller to perform a full transfer at the start of a frame. It is typically active for the Horzontal line before the end of vertical blank. The internal Vertical Gate signal starts when the internal Vertical Counter matches Vertical Gate Start register.

## VTGVGateStart VTGVGateStart

Region: 0 Offset: 0000.3050h

Read/Write Reset Value: XXXh




Bits 11-0 Vertical Gate Start

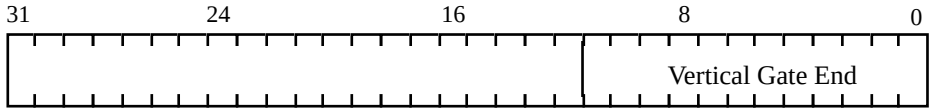
### 4.2.12 Vertical Gate End

The internal Vertical Gate signal ends when the internal Vertical Counter matches the Vertical Gate End register.

## VTGVGateEnd VTGVGateEnd

Region: 0 Offset: 0000.3058h

Read/Write Reset Value: XXXh




Bits 11-0 Vertical Gate End

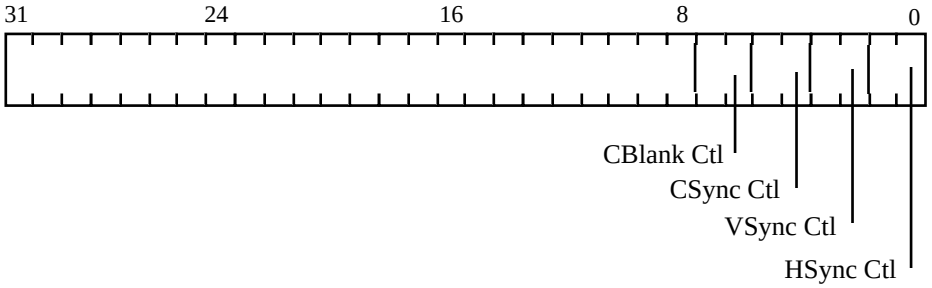
### 4.2.13 Polarity Control

The Polarity Control Register determines the polarities of the output signals HSync, VSync, CBlank and CompSync.

## VTGPolarity VTGPolarity

Region: 0 Offset: 0000.3060h

Read/Write Reset Value: D5h




Bits 1-0 HSync Ctl

0 = Active High
1 = Forced High
2 = Active Low
3 = Forced Low

Bits 3-2 VSync Ctl

0 = Active High
1 = Forced High
2 = Active Low
3 = Forced Low

Bits 5-4 CSync Ctl

0 = Active High
1 = Forced High
2 = Active Low
3 = Forced Low

Bits 7-6 CBlank Ctl

0 = Active High
1 = Forced High
2 = Active Low
3 = Forced Low

### 4.2.14 Frame Row Address register

The contents of the Frame Row Address register determines the VRAM row loaded into the VRAM shift register at the start of frame. While the frame is active, VRAM split transfers are generated to reload the VRAM shift register. The transfer addresses required are automatically generated internally, starting from this value. At the start of the next frame, a full transfer reloads the shift register with the row specified by this register again. The full transfer split register start address is always zero.

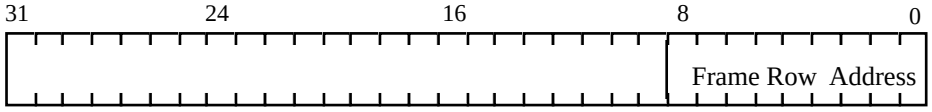
This register can be programmed for double-buffering, if the framebuffer is large enough, by starting the buffers on two different rows and altering the value to swap buffers.

To avoid any possible display artifact, this register should not be changed at the time the VRAM full transfer cycle is occuring at the start of frame. It is recommended that the register is updated during the active vertical period.

## VTGFrameRowAddr VTGFrameRowAddr

Region: 0 Offset: 0000.3068h

Read/Write Reset Value: 00h




Bits 8-0 Frame Row Address

### 4.2.15 Vertical Line Number

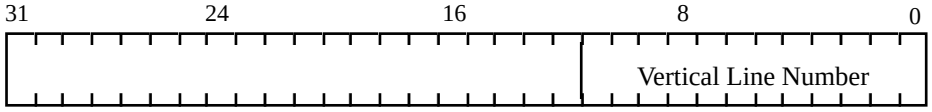
This read only register returns the value of the internal Vertical counter. It can be used to determine when the display is in the vertical blanking interval.

The display is in vertical blanking if the Vertical Line Number is between 1 and the value in the Vertical Blank End register. The display is active if the Vertical Line number is greater than the Vertical Blank End value.

## VTGVLineNumber VTGVLineNumber

Region: 0 Offset: 0000.3070h

Read Reset Value: 001h



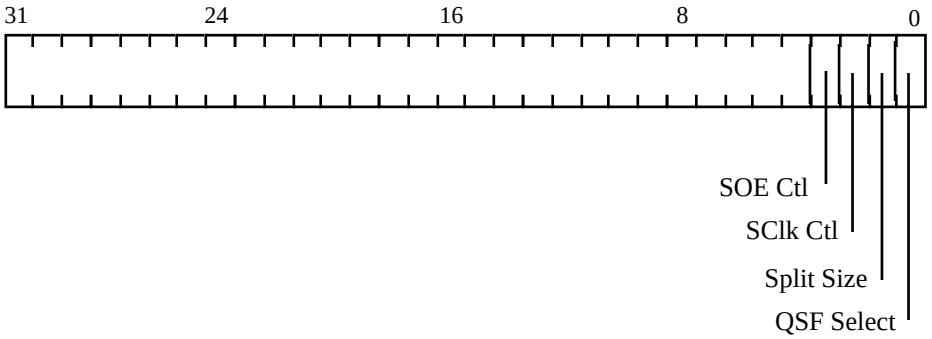

Bits 11-0 Vertical Line Number

### 4.2.16 Serial Clock Control

VTGSerialClk VTGSerialClk

Region: 0 Offset: 0000.3078h

Read/Write Reset Value: XXh




Bit 0 QSF Select

0 = External QSF
1 = Internal QSF

When this bit is asserted, the transfer address generator counts VRAM serial clocks and generates an internal QSF signal to initiate VRAM transfer cycles. When this bit is negated, the QSF pin is used to initiate transfer cycles. ( IBM 4M VRAM do not generate QSF, so an internal QSF must be generated).

Bit 1 Split Size

0 = 128 word split transfer register
1 = 256 word split transfer register

This bit is set to reflect the size of the VRAM transfer register in split transfer mode. 0 = 128 , 1 = 256. Most 256Kx4 and 256K x 8 VRAMs have a split register of 256. IBM 4M VRAMs have a split register size of 128. This field is used in the generation of the internal QSF.

Bit 2 SClk Ctl

This field is used to control the generation of SCLK0 and SCLK1 as described in section 4.4 below

Bit 3 SOE Ctl

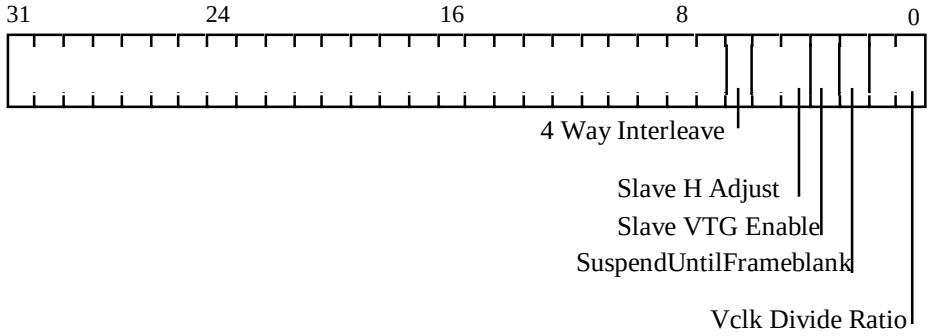
This field is used to control the generation of SOE , SOE1, SOE2 and SOE3 as described in section 4.4 below.

### 4.2.17 Mode Control

# VTGModeCtl VTGModeCtl

Region: 0 Offset: 0000.3080h

Read/Write Reset Value: 0000h




Bits 1-0 VCLK Divide Ratio

0 = Use VCLK undivided
1 = Use VClk/2
2 = Use VClk/4
3 = Use VClk/8

GLINT 500TX can generate a LDClk which is divided down from the incoming VCLK. The VClk Divide ratio is used to select the division .The SClk and SOE signals are derived from the LDClk. Normal usage has this field at 0.

Bit 2 SuspendUntilFrameBlank Enable

0 = Complete immediatly

1 = wait for VBLANK

GLINT 500TX has a mechanism in the Graphics core to flush outstanding writes to the framebuffer and then suspend any succeding reads or writes until the next vertical blank period. This field is used to enable this feature in the timing generator. If the field is not set then no suspension occurs. This is the reset condition. The field should not be set until the timing generator is running to avoid the possibility of suspending the Graphics Core when no VBLANK will occur.

Bit 3 Slave VTG Enable

0 = Disable

1 = Enable

This field enables the syncing of the timing generator to an external VSYNC. The master VSYNC is input to the GLINT 500TX on the QSF pin. The polarity of the VSYNC is taken to be the polarity of the internal VSYNC defined in the VTGPolarity register.

Bits 5-4 Slave Hadjust

0 = adjust by 0 VClks

1 = adjust by 1 VClks

2 = adjust by 2 VClks

3 = adjust by 3 VClks

This field allows the internal timing generator to be adjusted by a number of VClks relative to the incoming master VSYNC.

Bit 6 4-way Interleave Enable

0 = Disable

1 = Enable

When this bit is set, and the TXEnhanced pin is pulled high, then two additional Serial O/p enables are generated allowing 4 banks of memory to be interleaved into the RAMDAC.

## 4.3 VTG Configuration

### 4.3.1 Horizontal Timing Specifications.

A Horizontal counter (VTGHCount) runs off VClk. The counter starts at 1 and counts to the value in VTGHLimit and then reloads. This defines the Horizontal period. i.e. VTGHLimit x VClkPeriod. The horizontal blank and sync timing is derived from this counter and the values stored in the parameter registers.

At reset VTGHLimit is reset with '1'. This effectivly freezes the counter until the VTGHLimit register is loaded.

Horizontal blank starts at VTGHCount = 1.

Horizontal blank ends at VTGHCount = VTGHBlankEnd.

Horizontal blank width = VTGHBlankEnd x VClkPeriod.

Horizontal sync. starts at VTGHcount = VTGHSyncStart and ends at VTGHSyncEnd.

Horizontal sync. width = (VTGHsyncEnd - VTGHSyncStart) x VClkperiod.

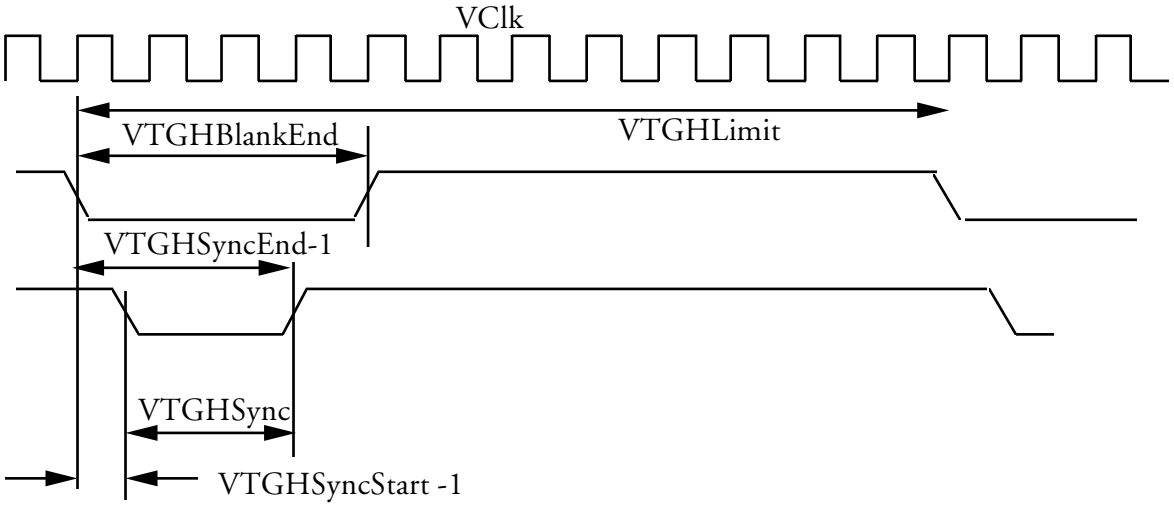



Figure 4-2. Horizontal Timing.

### 4.3.2 Vertical Timing Specifications.

The vertical signals are specified in terms of numbers of lines. A vertical counter (VTGVCount) counts lines starting at 1 and counts to the value in VTGVLimit and then reloads. The vertical period or frame rate is defined as VTGVLimit x Horizontal period. This is VTGVLimit x VTGHLimit x VClkPeriod. The vertical blank and sync timing is derived from this counter and the values stored in the parameter registers.

At reset VTGVLimit is reset with '1'. This effectivly freezes the counter until the VTGVLimit register is loaded.

Vertical Blank is asserted on the active edge of Horizontal blank

Vertical blank starts at VTGVCount = 1 and

Vertical blank ends at VTGVCount = VTGVBlankEnd.

Vertical blank width = VTGVBlankEnd x HorizontalPeriod.

The Vertical sync is asserted on the active edge of Horizontal sync.

Vertical sync starts at (VTGVCount = VTGVSyncStart -1)

Vertical sync ends at VTGVSyncEnd - 1

Vertical sync. width = (VTGVsyncEnd - VTGVSync start) x HorizontalPeriod

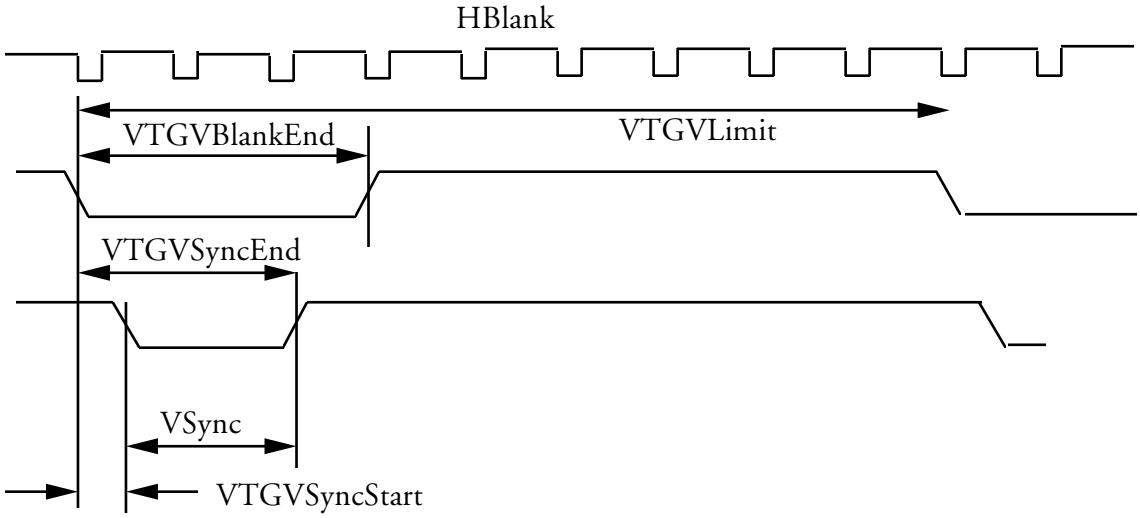



Fig. 4-3. Vertical Timing.

### 4.3.3 Sync and Blank Generation

Composite Sync (CompSync.) is the logical OR of HSync and VSync.

Composite Blank (CBlank) is the logical OR of HBlank and VBlank.

VSync, HSync, CompSync and CBlank are all outputs from GLINT 500TX. The polarity of these signals is controlled by the Polarity Control Register.

### 4.3.4 Vertical and Horizontal Gate Specification

Hgate is generated from VTGHGateStart and VTGHGateEnd in the same way as Hsync. i.e.

Hgate = (VTGHGateEnd - VTGHGateStart) x VClkPeriod

Similarly VGate is generated from VTGVGateStart and VTGVGateEnd

VGate = (VTGVGateEnd - VTGVGateStart) x HorizontalPeriod.

VGate and HGate are used to control the VRAM transfer requester and to gate the VRAM serial clock. HGate is typically set to be the inverse of HBlank with a shift of a number of clocks to allow the VRAM serial data to reach the RAMDAC synchronised correctly to the blanking signal. VGate is typically set during the line before the end of Vertical Blank.

### 4.3.5 VRAM Transfer Control

The video display from GLINT 500TX is generated by connecting the framebuffer VRAM serial ports to the RAMDAC. The VRAM serial shift registers must be kept loaded with the correct data to generate the display. The framebuffer must be linearly mapped to use the internal timing generator/transfer address controller.

At the end of the vertical blanking, a VRAM full transfer cycle is performed using the addressloaded in the Frame Row Address register. This defines the VRAM RAS address start point.

The VRAM serial clock (SClk ) is gated with HGate and VGate to only clock during the active part of active lines. If an external QSF signal is available which indicates when the VRAM shift register is half empty, split transfer cycles are performed which reload the empty half of the shift register. This continues until the end of the frame.

If no external QSF signal is available then the Internal QSF bit of the Serial Clock Control register must be set. An internal QSF is generated by effectivly counting SClks until the size of the VRAM split register is reached and QSF is toggled. Split register sizes of both 256 bits and 128 bits are supported by setting the Split RegisterSize bit of the Serial Clock Control register appropriately.

For a split register size of 256, the row address and column address bit 8 is incremented every time QSF toggles. For a split register size of 128, the row address and column address bits 8 and 7 are incremented every time QSF toggles.

## 4.4 VRAM Serial Port Control

There are numerous ways of controlling the framebuffer serial port to generate the display. The serial port interleave may be one,two or four way depending on the number of banks of memory and the RAMDAC port width. The register settings for these different interleaves is listed in Table 4.1 below.

| 4way | TX Enhanced | SOE Ctl | SClk Ctl | Display source | Sclk freq. | serial port interleave |
|---|---|---|---|---|---|---|
| X | 0 | 0 | 0 | SOE0 | LDCLK | 1-way bank0 |
| X | 0 | 1 | 0 | SOE1 | LDCLK | 1-way bank1 |
| X | 0 | X | 1 | SOE0,1 | LDCLK/2 | 2-way bank0,1 |
| 0 | 1 | 0 | 1 | SOE0,1 | LDCLK/2 | 2-way bank0,1 |
| 0 | 1 | 1 | 1 | SOE2,3 | LDCLK/2 | 2-way bank2,3 |
| 1 | 1 | X | X | SOE0,1,2,3 | LDCLK/4 | 4way |

**Table 4.1 Options for serial port control**

The first 3 modes are compatible with GLINT 300SX. The latter 3 modes are new to GLINT 500TX.

### 4.4.1 One-way Interleaved

Serial data is clocked out of either Bank 0 or Bank 1. This is controlled using the SOE Ctl field of the Serial Clock Control register. There is no dynamic switching from bank 0 to bank 1.

SClk0 and SClk1 are identical in this case and are gated versions of the RAMDAC LDClk.

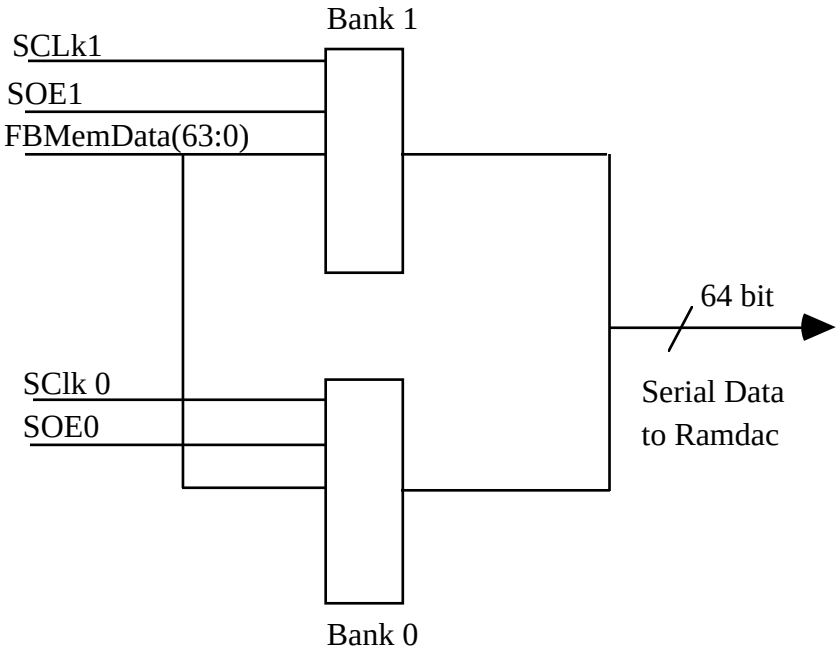



Fig 4.4 Serial Control of 1-way interleaved display.

### 4.4.2 Two-way Interleaved

In this mode, Bank 0 and Bank 1 are interleaved, and the display is taked alternatly from each using SOE0 and SOE1. SCLK0 and SCLK1 are again gated on during the active scan line and run at RAMDAC LDClk/2. This is compatible with GLINT 300SX.

If the GLINT 500TX has the TXEnhanced pin pulled high, then the SOE2 and SOE3 pins are activated. These can be used to allow display from an additional 2 banks of memory. In two-way interleaved mode the SOE Ctl field of the Serial Clock Control

register is used to select whether the Bank 0 and Bank 1 are outputting data onto the Serial data bus, or whether Bank 2 and Bank 3 are used.

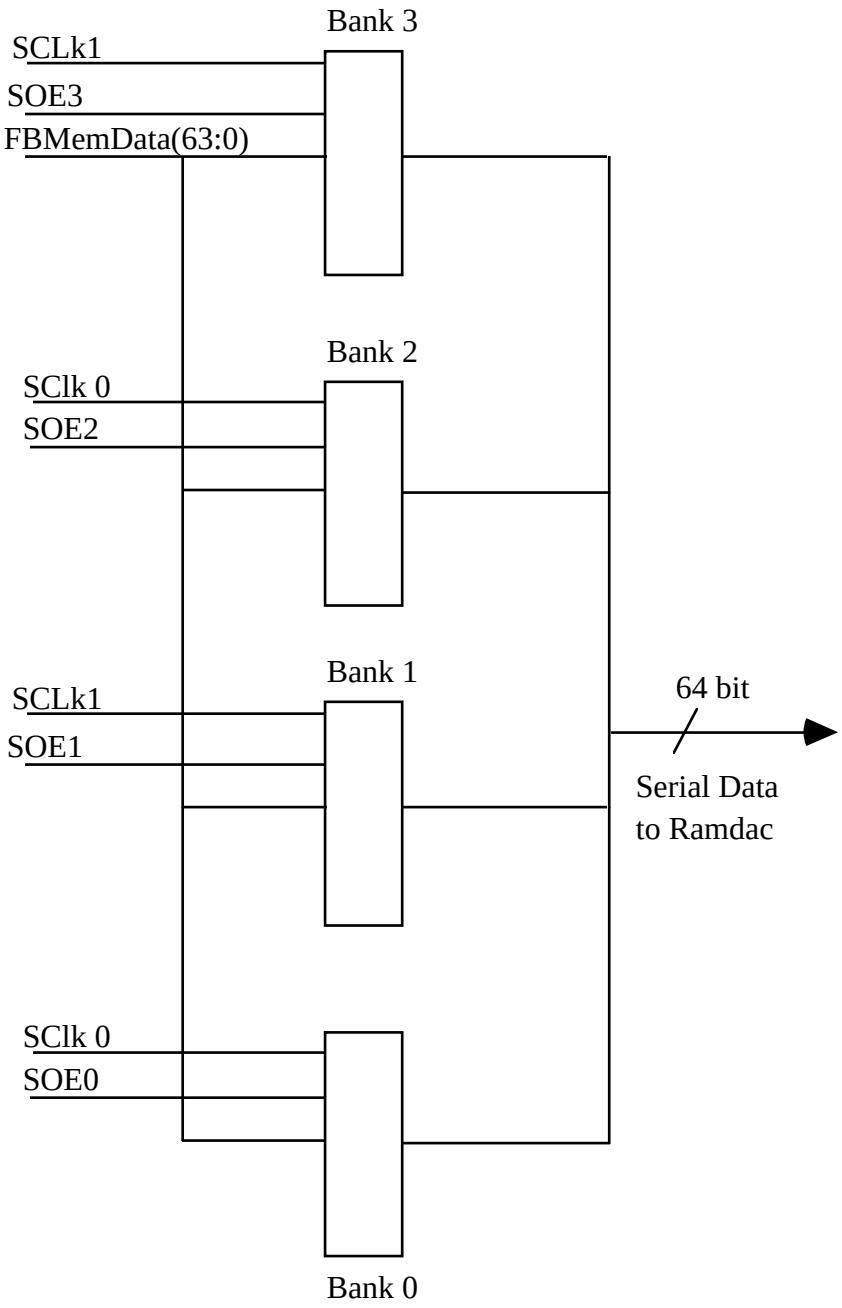



Fig 4.5 2-way or 4-way interleaved serial port with 64bit RAMDAC.

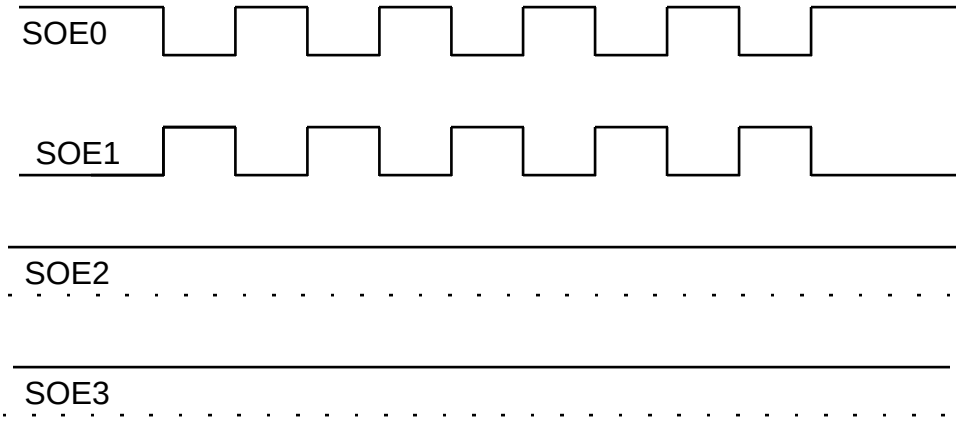



Fig 4.6 2-way Interleaved with TX Enhanced = 1 , SOE Ctl = 0.

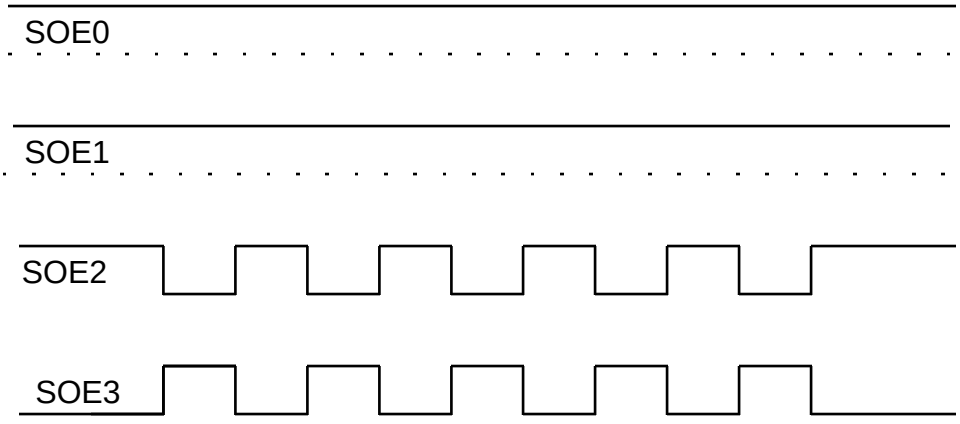



Fig 4.7 2-way Interleaved with TX Enhanced = 1 , SOE Ctl = 1.

### 4.4.3 Four-way Interleaved

This mode is connected to the VRAM serial port exactly the same way as the two-way interleaved mode. The GLINT 500TX drives the SOE of each of the 4 banks low in turn. Note that banks 0 and 2 are connected to SCLK0 and banks 1 and 3 to SCLK1.

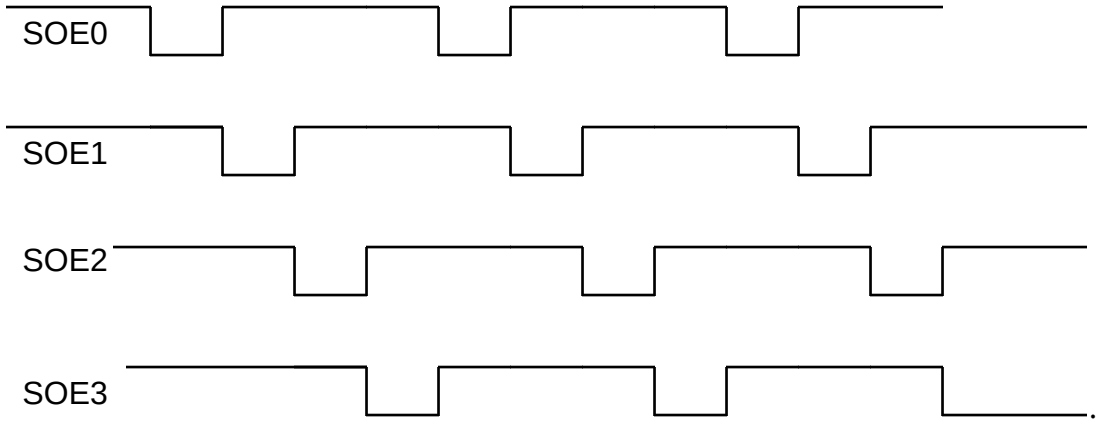



Fig 4.8 4-way interleaved serial port.

If using a 64-bit RAMDAC, the interleave of the VRAM serial port must match the interleave of the VRAM random port as defined in the Interleave field of the FBModeSel register.

If a 128-bit RAMDAC is used, the interleave of the VRAM serial port must be half the interleave of the VRAM random port.

In general, the higher the interleave value of the serial port, the faster the pixel rate that can be displayed and hence the higher the resolution . However, more banks of memory must be fitted.

▪

## 4.5 VTG Example

The timing specification for the VESA 800 x 600 at 60 Hz mode 6Ah are as follows :-

| | Horizontal Time | Characters | Vertical Time | Lines |
|---|---|---|---|---|
| Dot Clock | 40 MHz | | | |
| Sync. Polarity | Positive | | Positive | |
| Frequency | 37.879 KHz | | 60.3165 Hz | |
| Period | 26.4 uS | 132 | 16.579 mS | 628 lines |
| Blanking Time | 6.4 uS | 32 | 0.739 mS | 28 lines |
| Sync Width | 3.2 uS | 16 | 0.106 mS | 4 lines |
| Back Porch | 2.2 uS | 11 | 0.607 mS | 23 lines |
| Active Time | 20.0 uS | 100 | 15.840 mS | 600 lines |
| Front Porch | 1.0 uS | 5 | 0.026 mS | 1 line |

For a system with 32 bits per pixel and a 2 to 1 interleave on the serial data ie VLCK = Dot Clock /2 then the the following register values can be used .

| Register Name | Value | Explanation |
|---|---|---|
| VTGHLimit | 528 | 132 x 8 pixel chars. 2 pixels per VCLK |
| VTGHSyncStart | 20 | Front porch *8 /2 |
| VTGHSyncEnd | 84 | (FrontPorch + SyncWidth)*8/2 |
| VTGHBlankEnd | 128 | (Blanking time ) *8/2 |
| VTGVLimit | 628 | Vertical Period |
| VTGVSyncStart | 2 | Front Porch +1 |
| VTGVSyncEnd | 6 | Front Porch + SyncWidth +1 |
| VTGVBlankEnd | 28 | Blanking Time |
| VTGHGateStart | HBlankEnd -2 | Example value ( system dependent) |
| VTGHGateEnd | HLimit -2 | Example value ( system dependent) |
| VTGVGateStart | VBlankEnd -1 | |
| VTGVGateEnd | VBlankEnd | |

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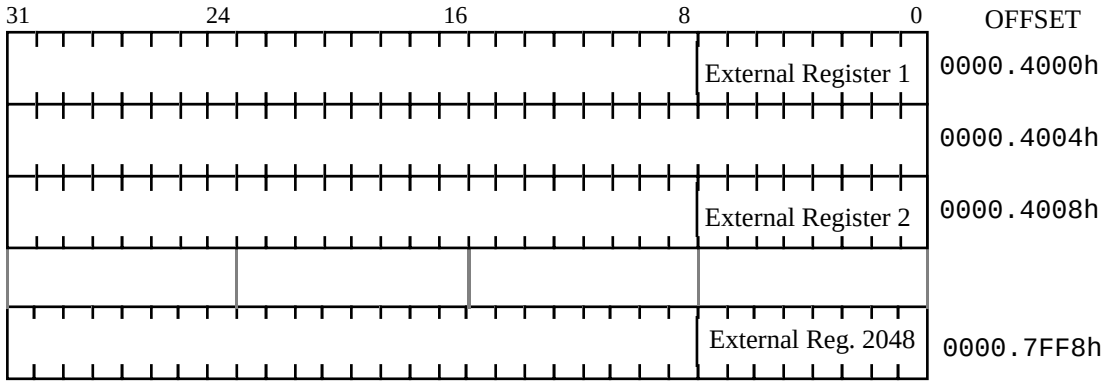
# 5. External Video Control Registers

GLINT 500TX provides an 8 bit general purpose interface to allow external devices to be addressed from the PCI. This interface has a 16Kbyte address space and is specified as the external video control register region. It allows up to 2048 x 8bit registers to be accessed on 64 bit boundaries. On a typical system, this interface is used to address the LUT-DAC. On more advanced designs, when an external video timing generator or other controllable video circuitry is used, these can also be addressed through this regster space. The interface consists of address, data and two control lines. The address and data lines share pins with the Localbuffer data pins.




## 5.1 External Video Interface Signal Definitons

The follwing signals are defined for the External Video Interface, together with the GLINT 500TX pins that the signals appear on.

Table 5-1. External Video Signals

| Signal | Pins used | Description |
|---|---|---|
| Ext VidAddress(13-3) | LBMemData(37-27) | External Video register Address lines. Note that the registers are on 64 bit PCI boundaries. |
| ExtVidData(7-0) | LBMemData(47-40) | External Video Data bus. |
| DacRdN | DacRdN | External Video register read strobe (negative active) |
| DacWrN | DacWrN | External Video register write strobe (negative active) |

See Chapter 9 for signal waveforms and timing.

## 5.2 LUT-DAC Interface.

A typical LUT-DAC would be connected to GLINT 500TX through the External Video Interface as shown in figure 5-1.

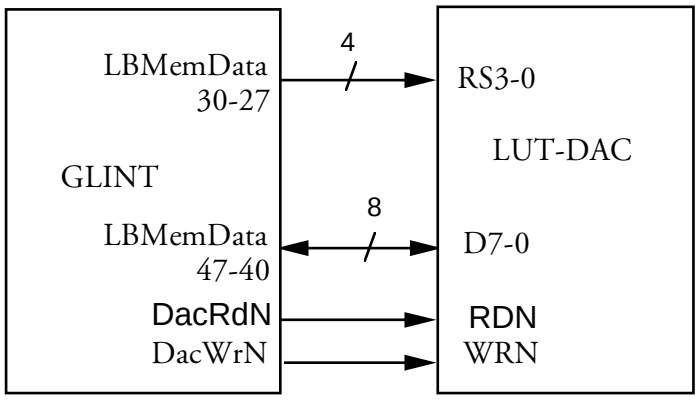



Figure 5-1 Typical LUT-DAC Interface.

When additional External Video circuitry is required, the the DacRdN, DacWrN and ExtVidAddress must be externally decoded to generate any required select or control lines.

## 5.3 Reseting External Circuitry

External circuitry connected to GLINT may need a reset signal. This cannot be obtained directly from the PCI reset line as this can only have one load, the GLINT chip itself. GLINT uses two of its external ciruitry control pins, RomEnN and DacWrN, when asserted together to indicate a reset. The pins are asserted when either the PCIRstN line to GLINT is asserted or when GLINT is reset by software.

Reset is indicated for the full length of a PCI reset and for 64 MClk cycles when a soft reset is initiated.

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# 8. GLINT 500TX Register Set

Table 8-1. GLINT 500TX Configuration Region Registers

| Register | Type | Offset | Section | Description |
|---|---|---|---|---|
| **Device Identification** | | | | |
| CFGVendorId | R | 00h | 2.1.1 | Vendor identification number |
| CFGDeviceID | R | 02h | 2.1.2 | Device identification number |
| CFGRevisionID | R | 08h | 2.1.3 | Revision identification number |
| CFGClassCode | R | 09h | 2.1.4 | Class code register |
| CFGHeaderType | R | 0Eh | 2.1.5 | Header type |
| **Device Control/Status** | | | | |
| CFGCommand | R/W | 04h | 2.2.1 | PCI command register |
| CFGStatus | | 06h | 2.3.1 | PCI status register |
| **Miscellaneous Functions** | | | | |
| CFGBist | R | 0Fh | 2.4.1 | BIST |
| CFGLatTimer | R/W | 0Dh | 2.4.2 | Latency timer value |
| CFGCacheLine | R | 0Ch | 2.4.3 | Cache line size |
| CFGMaxLat | R | 3Fh | 2.4.4 | Maximum latency period |
| CFGMinGrant | R | 3Eh | 2.4.5 | Minimum grant period |
| CFGIntPin | R | 3Dh | 2.4.6 | Interrupt pin being used |
| CFGIntLine | R/W | 3Ch | 2.4.7 | Interrupt line routing information |
| **Base Addresses** | | | | |
| CFGBaseAddr0 | R/W | 10h | 2.5.1 | Control space offset |
| CFGBaseAddr1 | R/W | 14h | 2.5.2 | Aperture 0 Localbuffer offset |
| CFGBaseAddr2 | R/W | 18h | 2.5.3 | Aperture 0 Framebuffer offset |
| CFGBaseAddr3 | R/W | 1Ch | 2.5.4 | Aperture 1 Localbuffer offset |
| CFGBaseAddr4 | R/W | 20h | 2.5.5 | Aperture 1 Framebuffer offset |
| CFGRomAddr | R/W | 30h | 2.5.6 | Expansion ROM offset |

Table 8-2. GLINT 500TX Region 0 Registers

| Register | Type | Offset | Section | Description |
|---|---|---|---|---|
| **Control Status Registers** | | | | |
| ResetStatus | R/W | 0000h | 3.1.1 | Reset status and software reset |
| IntEnable | R/W | 0008h | 3.1.2 | Interrupt enable |
| IntFlags | R/W | 0010h | 3.1.3 | Interrupt flags |
| InFIFOSpace | R | 0018h | 3.1.4 | Input FIFO space |
| OutFIFOWords | R | 0020h | 3.1.5 | Number of words in the output FIFO |
| DMAAddress | R/W | 0028h | 3.1.6 | DMA start address |
| DMACount | R/W | 0030h | 3.1.7 | DMA word count |
| ErrorFlags | R/W | 0038h | 3.1.8 | Error flags |
| VClkCtl | R/W | 0040h | 3.1.9 | Video clock control |
| TestRegister | R/W | 0048h | 3.1.10 | Test register (Diagnostic) |
| Aperture0 | R/W | 0050h | 3.1.11 | Aperture 0 control |
| Aperture1 | R/W | 0058h | 3.1.12 | Aperture 1 control |
| DMAControl | R/W | 0060h | 3.1.13 | DMA control |
| **Localbuffer Registers** | | | | |
| LBMemoryCtl | R/W | 1000h | 3.2.1 | Localbuffer memory control register |
| LBMemoryEDO | R/W | 1008h | 3.2.2 | Localbuffer EDO memory control |
| **Framebuffer Registers** | | | | |
| FBMemoryCtl | R/W | 1800h | 3.3.1 | Framebuffer memory control register |
| FBModeSel | R/W | 1808h | 3.3.2 | Framebuffer mode select |
| FBGCWrMask | R | 1810h | 3.3.3 | Framebuffer GC write mask (Diagnostic) |
| FBGCColorLower | R | 1818h | 3.3.4 | Framebuffer GC color lower (Diagnostic) |
| FBTXMemCtl | R/W | 1820h | 3.3.5 | Framebuffer TX Shared Memory Control |
| FBWrMask | R/W | 1830h | 3.3.6 | Framebuffer Bypass Write mask |
| FBGCColorUpper | R/W | 1838h | 3.3.7 | Framebuffer GC color upper (Diagnostic) |

| Register | Type | Offset | Section | Description |
|---|---|---|---|---|

Internal Video Registers

| | | | | |
|---|---|---|---|---|
| VTGHLimit | R/W | 3000h | 4.2.1 | Horizontal VClk count limit |
| VTGHSyncStart | R/W | 3008h | 4.2.2 | Horizontal sync pulse start |
| VTGHSyncEnd | R/W | 3010h | 4.2.3 | Horizontal sync pulse end |
| VTGHBlankEnd | R/W | 3018h | 4.2.4 | Horizontal blanking period end |
| VTGVLimit | R/W | 3020h | 4.2.5 | Vertical line count limit |
| VTGVSyncStart | R/W | 3028h | 4.2.6 | Vertical sync pulse start |
| VTGVSyncEnd | R/W | 3030h | 4.2.7 | Vertical sync pulse end |
| VTGVBlankEnd | R/W | 3038h | 4.2.8 | Vertical blanking period end |
| VTGHGateStart | R/W | 3040h | 4.2.9 | Horizontal gate pulse start |
| VTGHGateEnd | R/W | 3048h | 4.2.10 | Horizontal gate pulse end |
| VTGVGateStart | R/W | 3050h | 4.2.11 | Vertical gate pulse start |
| VTGVGateEnd | R/W | 3058h | 4.2.12 | Vertical gate pulse end |
| VTGPolarity | R/W | 3060h | 4.2.13 | Output signal polarity control |
| VTGFrameRowAddr | R/W | 3068h | 4.2.14 | Frame row address |
| VTGVLineNumber | R | 3070h | 4.2.15 | Vertical line number |
| VTGSerialClk | R/W | 3078h | 4.2.16 | Serial clock control |
| VTGModeCtl | R/W | 3080h | 4.2.17 | Mode Control |

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# 9. Electrical Data

## 9.1 Absolute Maximum Ratings

Table 9-1 Absolute Maximum Ratings

| | |
|---|---|
| Junction Temperature | 100°C |
| Storage Temperature | -65°C to 150°C |
| DC Supply Voltage | 3.8V |
| I/O Pin Voltage with respect to GND | -0.5V to 5.5V |

## 9.2 DC Specifications

Table 9-2 DC Specifications

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| VDD | Supply Voltage | 3.0 | 3.6 | V |
| $L_{PIN}$ | Pin Inductance | | 18.4 | nH |
| $I_{CC}$ | Power Supply Current | | TBD | mA |

Table 9-3 PCI Signal DC Specifications

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{PIL}$ | Input Low Voltage | | TBD | V |
| $V_{PIH}$ | Input High Voltage | TBD | | V |
| $V_{POL}$ | Output Low Voltage | | 0.5 | V |
| $V_{POH}$ | Output High Voltage | 2.4 | | V |
| $I_{PIL}$ | Input Low Current | | TBD | mA |
| $I_{PIH}$ | Input High Current | | TBD | mA |
| $C_{PIN}$ | Input Capacitance | | TBD | pF |
| $C_{CLK}$ | PCI Clock Input Capacitance | | TBD | pF |
| $C_{IDSEL}$ | PCI Idsel Input Capacitance | | TBD | pF |

Table 9-4 Non PCI Signal DC Specifications

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | 2.0 | | V |
| $V_{OL}$ | Output Low Voltage | | 0.5 | V |
| $V_{OH}$ | Output High Voltage | 2.4 | | V |
| $I_{OL12}$ | Output Low Current | 12 | | mA |
| $I_{OH12}$ | Output High Current | -8 | | mA |
| $I_{OL8}$ | Output Low Current | 8 | | mA |
| $I_{OH8}$ | Output High Current | -6 | | mA |
| $I_{IL}$ | Input Low Current | | 1 | uA |
| $I_{IH}$ | Input High Current | | 1 | uA |
| $I_{IHPD}$ | Pulldown Input High Current | | 250 | uA |
| $I_{ILPU}$ | Pullup Input Low Current | | 250 | uA |
| $C_{IN}$ | Input Capacitance | | TBD | pF |

## 9.3 AC Specifications

Table 9-5 Test Loads for AC Timing

| Pin Name | Capacitive Load |
|---|---|
| PCIAD[31:0], PCICBEN[3:0], PCIPar, PCIFrameN,PCIIRdyN, PCITRdyN, PCIStopN, PCILockN, PCIIdsel, PCIDevselN, PCIReqN, PCIGntN, PCIIntAN, LBMemAddr[11:0], LBRasN[1:0], LBCasN[5:0], LBMemOeN[1:0], LBMemWeN, LBMemData[47:0], FBMemAddr[8:0], FBMemRas[3:0], FBMemCas[7:0], FBMemOeN[3:0], FBMemWeN[3:0], FBMemDSF[1:0], FBMemData[63:0], LDClk, SClk[1:0], SOE[3:0]. | 50pF |
| CompSync, DacWrN, DacRdN, HSync/ExtTxCmd[0], VSync/ExtTxCmd[1], CBlank/ExtTxSplit, FBGnt, FBReq, FBSelOE, VClkCtl[1:0], RomEnN. | 20pF |

### 9.3.1 Clock Timing

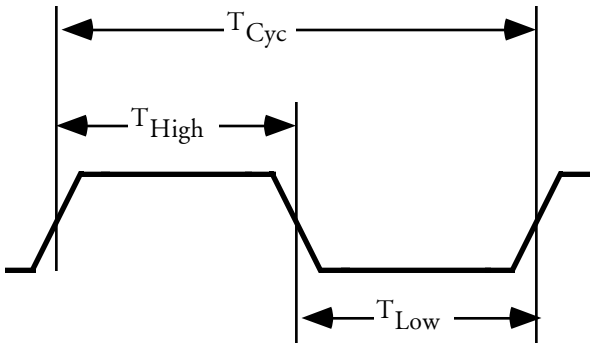


Figure 9-1 Clock Waveform Timing

Table 9-6 Clock Waveform Timing

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $T_{PCyc}$ | PCIClk Cycle Time | 30 | | nS | |
| $T_{PHigh}$ | PCIClk High Time | 8 | | nS | |
| $T_{VLow}$ | PCIClk Low Time | 8 | | nS | |
| $T_{MCyc}$ | MClk Cycle Time | 25 | 40 | nS | |
| $T_{MHigh}$ | MClk High Time | 8 | | nS | |
| $T_{MLow}$ | MClk Low Time | 8 | | nS | |
| $T_{VCyc}$ | VClk Cycle Time | 20 | | nS | |
| $T_{VHigh}$ | VClk High Time | 6 | | nS | |
| $T_{VLow}$ | VClk Low Time | 6 | | nS | |

### 9.3.1 Input / Output Timing

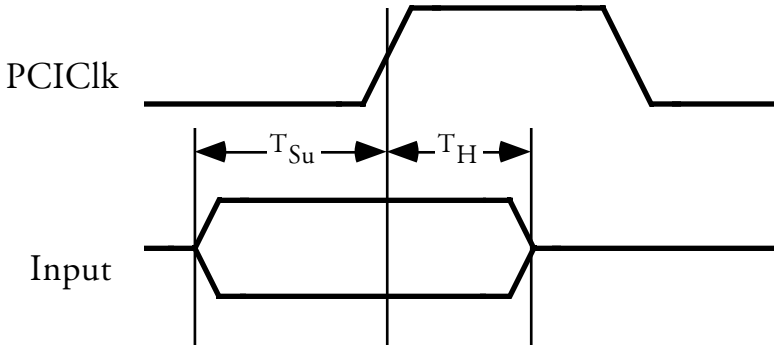


Figure 9-2 PCIClk Referenced Input Timing

Table 9-7 PCIClk Referenced Input Timing

| Parameter | $T_{Su}$ Min | $T_H$ Min | Units | Notes |
|---|---|---|---|---|
| PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCILockN, PCIIdsel, PCIDevselN | 7 | 0 | nS | |
| PCIGntN | 10 | 0 | nS | |
| PCIRstN | 7 | 0 | nS | 1 |

Notes:

1 PCIRstN is resynchronised internally. The timings given, when met, ensure that the reset is detected in the current cycle.

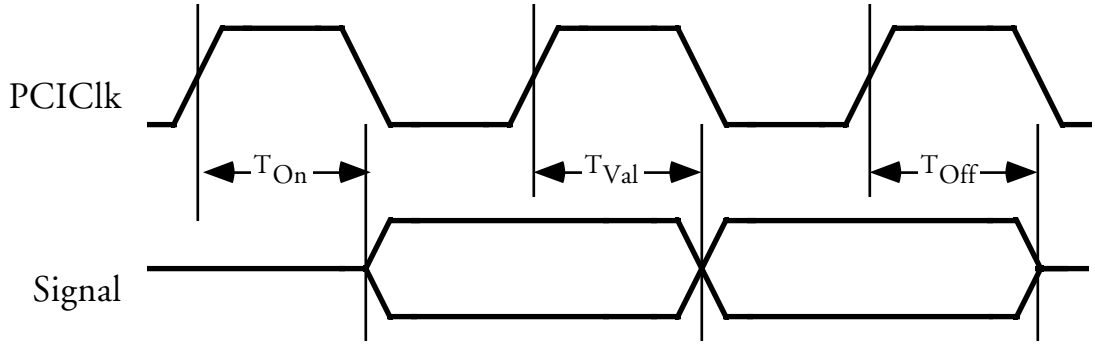


Figure 9-3 PCIClk Referenced Output Timing

Table 9-8 PCIClk Referenced Output Timing

| | $T_{Val}$ | | $T_{On}$ | | $T_{Off}$ | | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Min | Max | Min | Max | Min | Max | Units | Notes |
| PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCILockN, PCIIdsel, PCIDevselN | 2 | 11 | 2 | 11 | 2 | 11 | nS | |
| PCIReqN | 2 | 12 | | | | | nS | |
| PCIIntAN | TBD | TBD | | | | | nS | 1 |

Notes:

1. Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

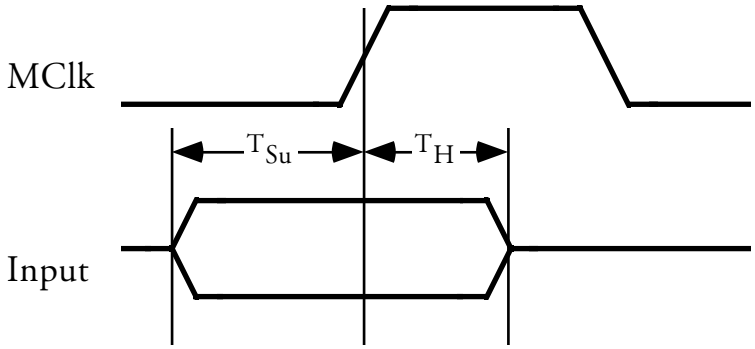


Figure 9-4 MClk Referenced Input Timing

Table 9-9 MClk Referenced Input Timing

| Parameter | $T_{Su}$ Min | $T_H$ Min | Units | Notes |
|---|---|---|---|---|
| FBReqN | - | - | nS | 1 |
| FBGntN | - | - | nS | 2 |
| QSF/ExtTxReq | - | - | nS | 3 |
| CBlank/ExtTxSplit | - | - | nS | 3 |
| ExtIntN | TBD | TBD | nS | 4 |

Notes:

1. This signal is an input when GLINT 500TX is a Shared Framebuffer Primary Controller. It is resynchronised internally.
2. This signal is an input when GLINT 500TX is a Shared Framebuffer Secondary Controller. It is resynchronised internally.
3. These signals are inputs when GLINT 500TX has an external video timing controller.These are resynchronised internally.
4. ExtIntN is resynchronised internally. The timings given,when met, ensure that the interrupt is detected in the current cycle.

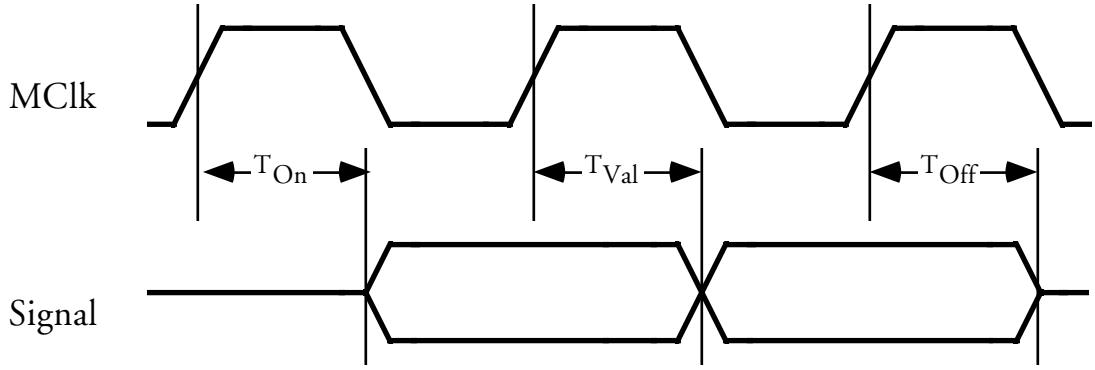


Figure 9-5 MClk Referenced Output Timing

Table 9-10 MClk Referenced Output Timing

| | $T_{Val}$ | | $T_{On}$ | | $T_{Off}$ | | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Min | Max | Min | Max | Min | Max | Units | Notes |
| LBMemAddr(11:0) | 7 | 23 | - | - | - | - | nS | |
| LBMemRasN(1:0) | 5 | 17 | | | | | nS | |
| LBMemCasN(5:0) | 5 | 17 | | | | | nS | |
| LBMemOeN(1:0) | 5 | 17 | | | | | nS | |
| LBMemWeN(1:0) | 5 | 17 | | | | | nS | |
| LBMemData(63:0) | 5 | 20 | 7 | 20 | 7 | 20 | nS | |
| FBMemAddr(8:0) | 7 | 25 | 5 | 25 | 5 | 15 | nS | |
| FBMemRasN(3:0) | 5 | 16 | 5 | 17 | 5 | 17 | nS | |
| FBMemCasN(7:0) | 5 | 17 | 5 | 17 | 5 | 17 | nS | |
| FBMemOeN(3:0) | 5 | 17 | 5 | 17 | 5 | 17 | nS | |
| FBMemWeN(3:0) | 5 | 17 | 5 | 17 | 5 | 17 | nS | |
| FBMemDSF(1:0) | 5 | 17 | 5 | 17 | 5 | 17 | nS | |
| FBMemData(63:0) | 6 | 24 | 7 | 27 | 7 | 27 | nS | |
| FBReq | 7 | 25 | | | | | nS | |
| FBGnt | 7 | 25 | | | | | nS | |
| FBSelOEN | 6 | 20 | | | | | nS | |
| HSync/ExtTxCmd1 | 7 | 24 | | | | | nS | |
| VSync/ExtTxCmd0 | 7 | 24 | | | | | nS | |
| DacWrN | 5 | 20 | | | | | nS | |
| DacRdN | 5 | 20 | | | | | nS | |
| RomEnN | 5 | 20 | | | | | nS | |

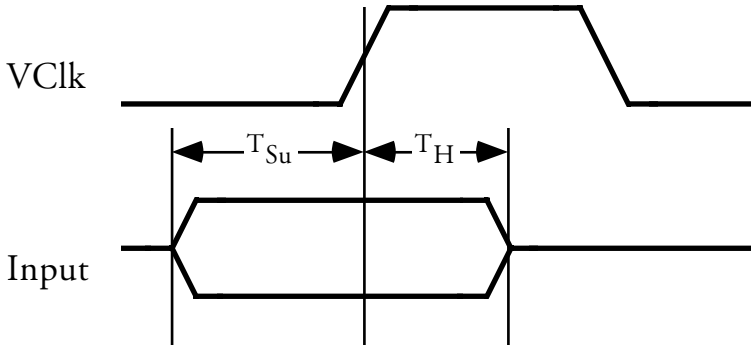


Figure 9-6 VClk Referenced Input Timing

Table 9-11 VClk Referenced Input Timing

| Parameter | $T_{Su}$ Min | $T_H$ Min | Units | Notes |
|---|---|---|---|---|
| QSF/ExtTxReq | 3 | 3 | nS | 1 |

Notes:

1. QSF/ExtTxReq is only timed against VClk when the GLINT 500TX is set to use the internal timing generator.

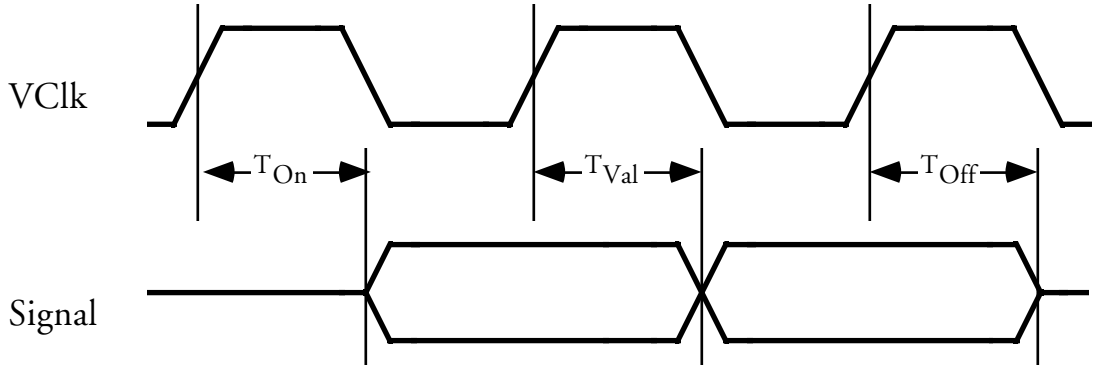


Figure 9-7 VClk Referenced Output Timing

Table 9-12 VClk Referenced Output Timing

| | $T_{Val}$ | | $T_{On}$ | | $T_{Off}$ | | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Min | Max | Min | Max | Min | Max | Units | Notes |
| SClk(1:0) | 4.5 | 15 | | | | | nS | |
| SOE(3:0) | 4.5 | 19 | | | | | nS | |
| LDClk | 4 | 15 | | | | | nS | |
| CBlank/ExtTxSplit | 7 | 21 | | | | | nS | 1 |
| HSync/ExtTxCmd1 | 7 | 21 | | | | | nS | 1 |
| VSync/ExtTxCmd0 | 7 | 21 | | | | | nS | 1 |
| CompSync | 7 | 21 | | | | | nS | |

Notes:

1. These signals are only timed against VClk when the GLINT 500TX is set to use the internal timing generator.

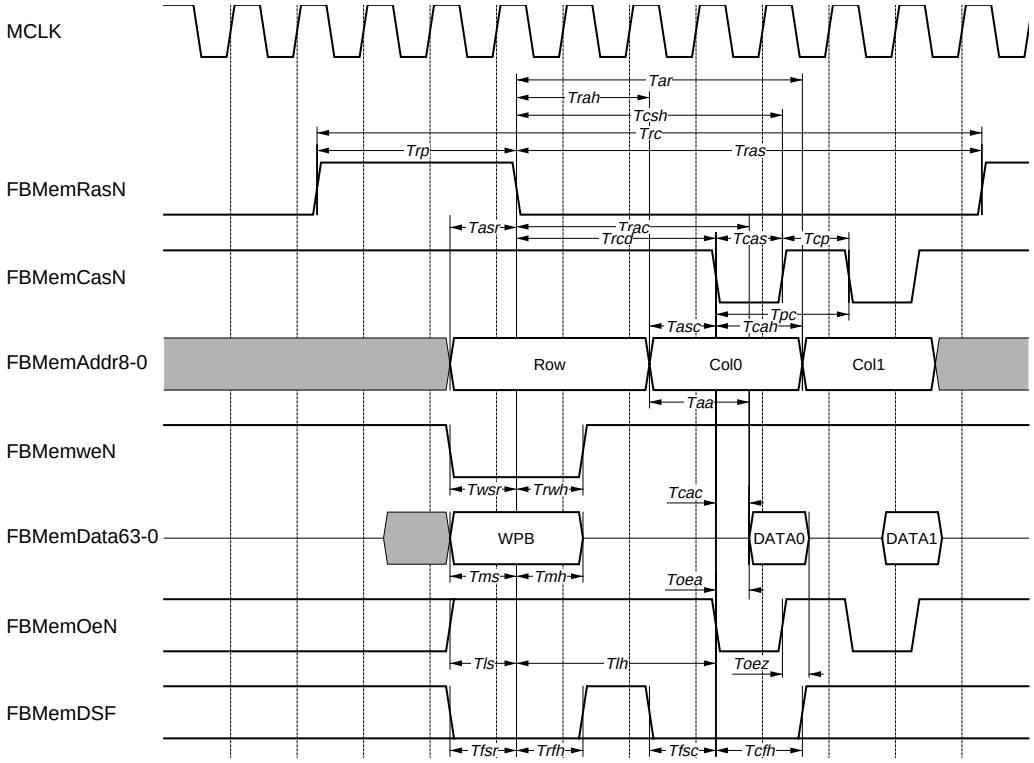


Figure 9-8 Framebuffer Read Timings

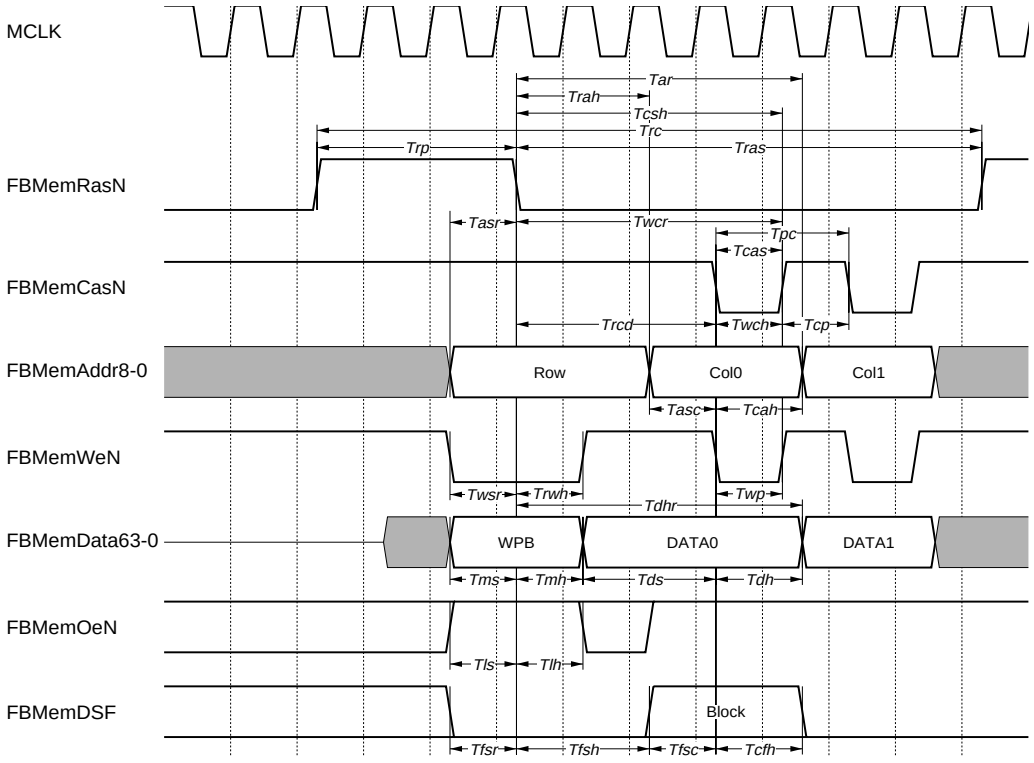


Figure 9-9 Framebuffer Write Timing

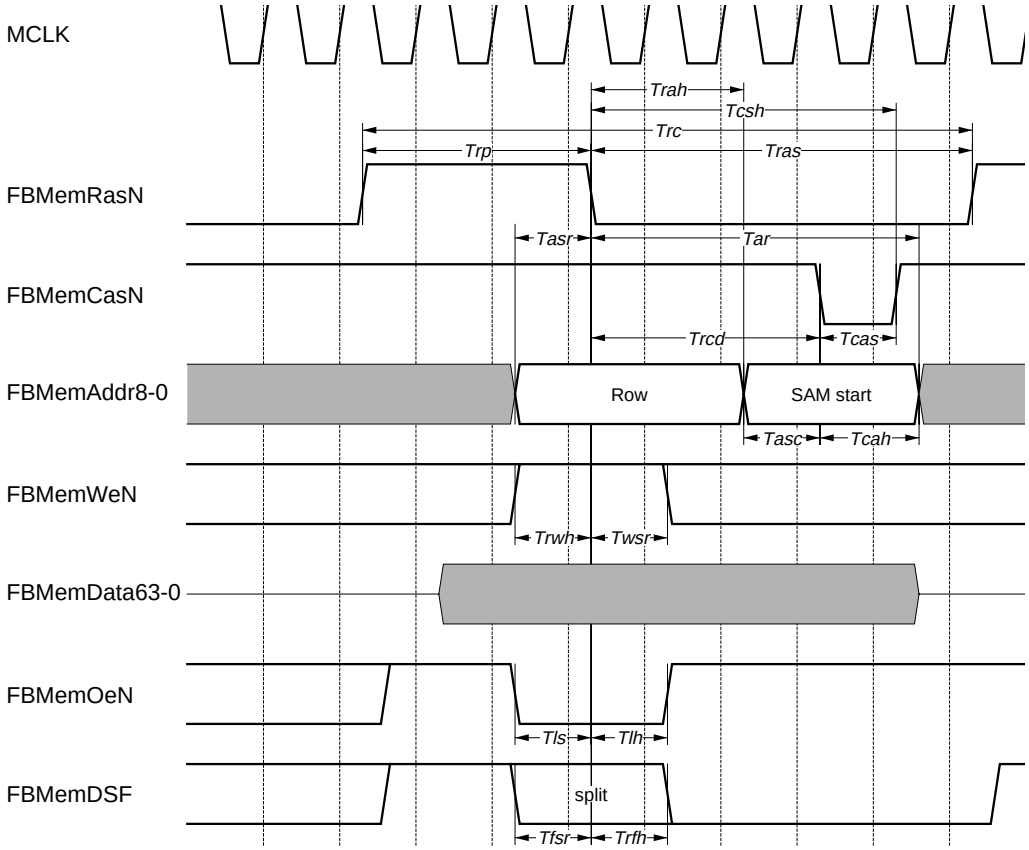


Figure 9-10 Frambuffer Transfer Cycle Timing

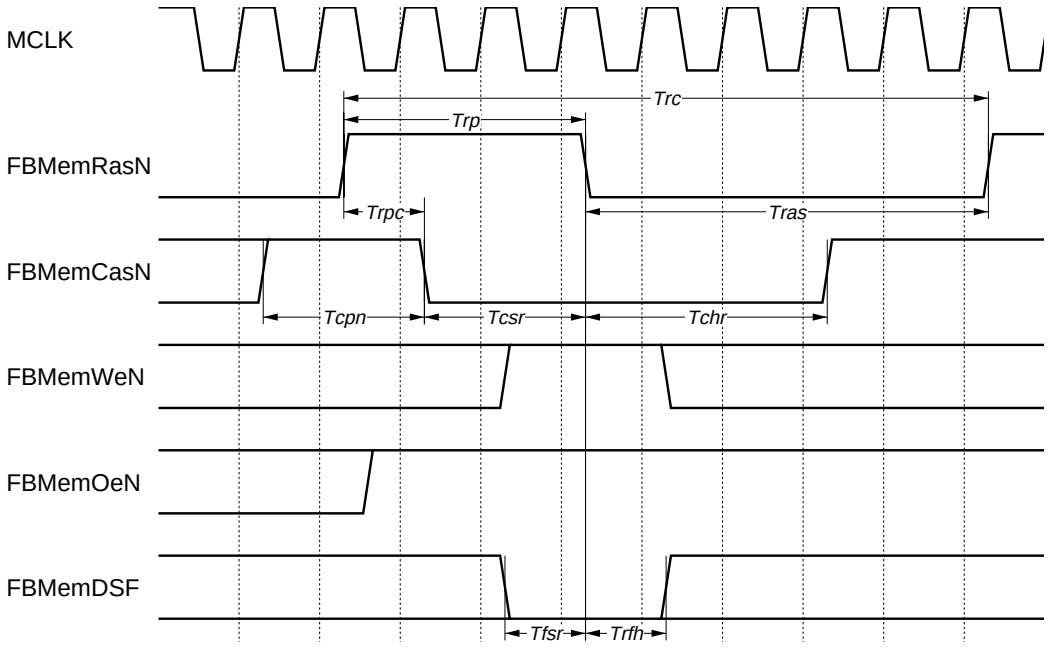


Figure 9-11 Framebuffer CAS-before-RAS refresh timings

Table 9-13 Framebuffer Timing

| Symbol | Parameter | Nominal timing in system clocks | Nominal timing at 50MHz |
|---|---|---|---|
| $t_{cas}$ | CAS Pulse Width | CL | 20*CL |
| $t_{crp}$ | CAS to RAS Precharge | CL | 20*CL |
| $t_{csh}$ | CAS hold time | RL+CL | 20*(RL+CL) |
| $t_{pc}$ | Page-mode cycle time | CL + 1 | 20*(CL+1) |
| $t_{cp}$ | CAS precharge time | 1 | 20 |
| $t_{rp}$ | RAS precharge time | RP | 20*RP |
| $t_{rc}$ | Random read /write Cycle time | RL + RP+CL | 20*(RL+RP+CL) |
| $t_{ras}$ | RAS pulse Width | RL+CL | 20*(RL+CL) |
| $t_{rcd}$ | RAS to CAS delay time | RL+CL | 20*(RL+CL) |
| $t_{rah}$ | Row Addres hold time | 1 | 20 |
| $t_{ar}$ | Column address Hold time (referenced to RAS) | RL+CL | 20*(RL+CL) |
| $t_{asc}$ | Column Address setup time | 1 | 20 |
| $t_{cah}$ | Column Address Hold time | CL | 20*CL |
| $t_{wch}$ | Write Command hold time | 1 | 20 |
| $t_{wcr}$ | Write Command hold time (referenced to RAS) | RL+CL | 20*(RL+CL) |
| $t_{wp}$ | Write Command pulse width | CL | 20*CL |
| $t_{ds}$ | Data setup time | 1 | 20 |
| $t_{dh}$ | Data hold time | CL | 20*CL |
| $t_{dhr}$ | Data hold time ( to RAS) | RL+CL | 20*(RL+CL) |
| $t_{rpc}$ | RAS precharge to CAS active | 1 | 20 |
| $t_{csr}$ | CAS setup time for CAS-before-RAS refresh | 1 | 20 |
| $t_{chr}$ | CAS hold time for CAS-before-RAS refresh | RL+CL | 20*(RL+CL) |
| $t_{asr}$ | Row Address setup time | 1 | 20 |
| $t_{tls}$ | DT/OE setup time to RAS | 1 | 20 |
| $t_{tlh}$ | DT/OE hold time to RAS | 1 | 20 |
| $t_{fsc}$ | DSF setup time referenced to CAS | 1 | 20 |
| $t_{cfh}$ | DSF hold time (to CAS) | CL | 20*CL |
| $t_{fsr}$ | DSF setup time referenced to RAS | 1 | 20 |
| $t_{rfh}$ | DSF hold time referenced to RAS | 1 | 20 |

| | | | |
|---|---|---|---|
| $t_{tp}$ | DT/OE precharge time | 1 | 20 |
| $t_{trp}$ | DT/OE to RAS precharge time | RP + 2 | 20*(RP+2) |

VRAM Access times required.

The following table gives the access times required to read from VRAM into the GLINT 500TX.

A CAS access time of 15 ns or better is required for a system clock of 50MHz with the CAS-low parameter set to 1 clock.

Table 9-14. VRAM Access Time Requirements.

| Symbol | Parameter | Nominal timing in system clocks | Nominal timing at 50MHz |
|---|---|---|---|
| $t_{cpa}$ | Access time from CAS precharge | CL + 1 | 20*(CL+1) -5 |
| $t_{rac}$ | Access time from RAS | RL+CL | 20*(RL+CL) -5 |
| $t_{cac}$ | Access time from CAS | CL | 20*CL -5 |
| $t_{oea}$ | Access time from OE | CL | 20*CL -5 |
| $t_{caa}$ | Access time from Column Address | CL + 1 | 20*(CL+1) -5 |

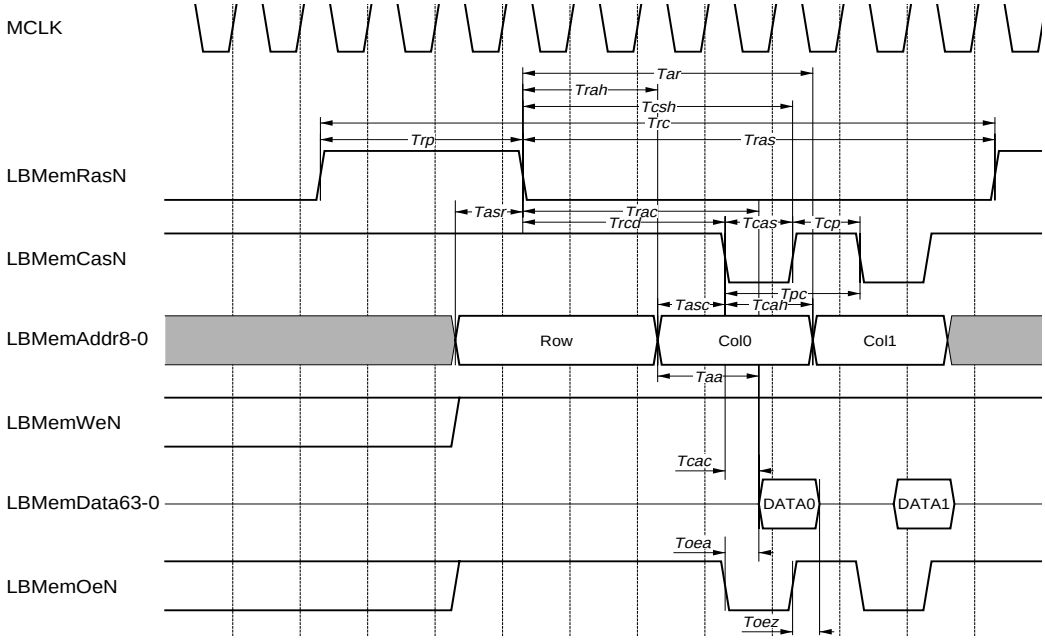


Figure 9-12 Localbuffer Read Timings - Fast-page mode

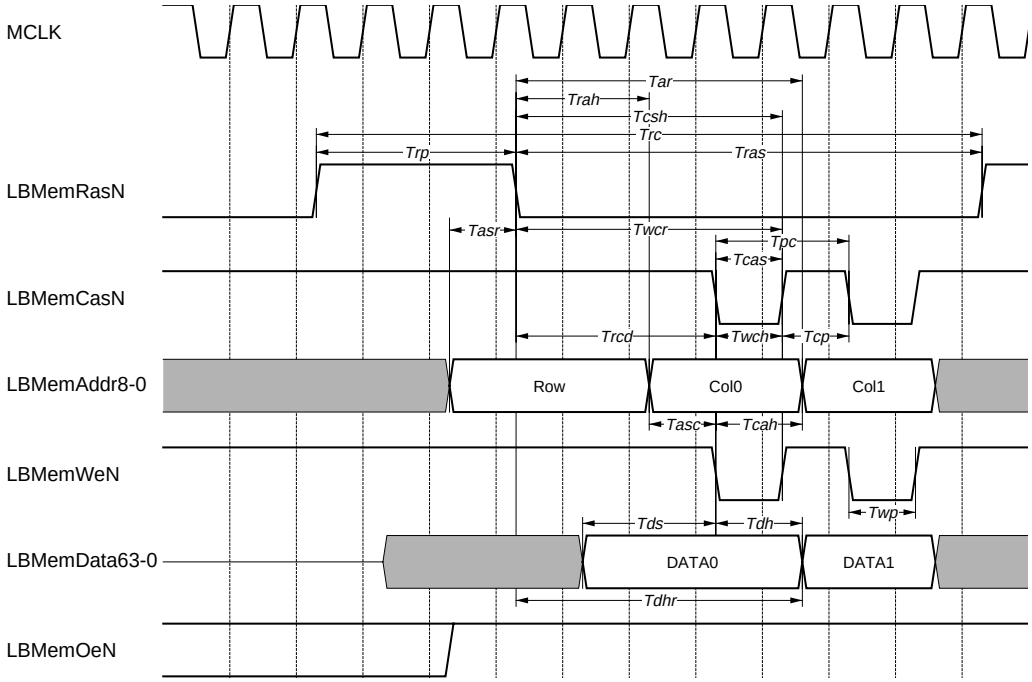


Fig 9-13 Localbuffer Write Timings - Fast-page mode

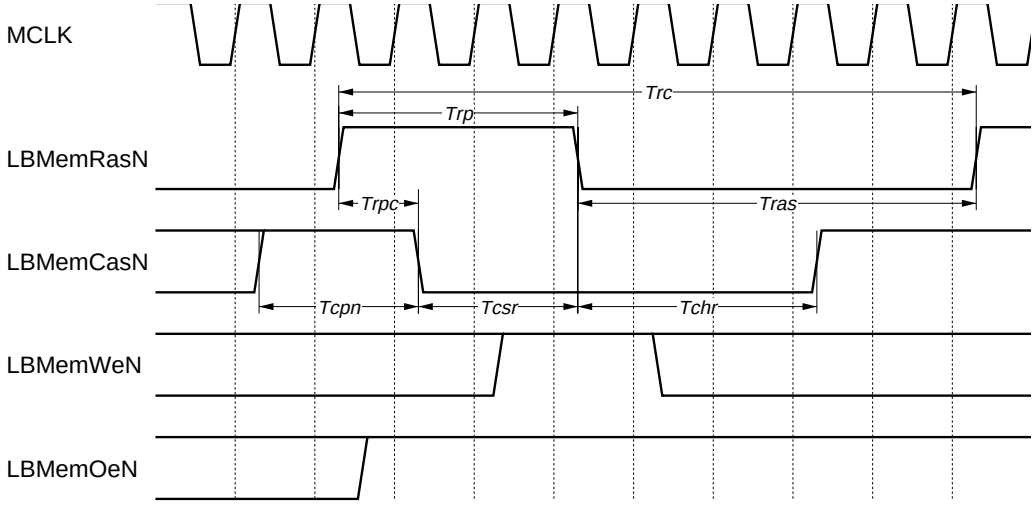


Figure 9-14 Localbuffer CAS-before-RAS Refresh Timings

Table 9-15 Localbuffer Timing - Fast-page mode

| Symbol | Parameter | Nominal timing in system clocks | Nominal timing at 50MHz |
|---|---|---|---|
| $t_{cas}$ | CAS Pulse Width | CL | 20*CL |
| $t_{crp}$ | CAS to RAS Precharge | CL | 20*CL |
| $t_{csh}$ | CAS hold time | RL+CL | 20*(RL+CL) |
| $t_{pc}$ | Page-mode cycle time | CL + 1 | 20*(CL+1) |
| $t_{cp}$ | CAS precharge time | 1 | 20 |
| $t_{rp}$ | RAS precharge time | RP | 20*RP |
| $t_{rc}$ | Random read or write Cycle time | RL + RP+CL | 20*(RL+RP+CL) |
| $t_{ras}$ | RAS pulse Width | RL+CL | 20*(RL+CL) |
| $t_{rcd}$ | RAS to CAS delay time | RL+CL | 20*(RL+CL) |
| $t_{rah}$ | Row Addres hold time | 1 | 20 |
| $t_{ar}$ | Column address Hold time (referenced to RAS) | RL+CL | 20*(RL+CL) |
| $t_{asc}$ | Column Address setup time | 1 | 20 |
| $t_{cah}$ | Column Address Hold time | CL | 20*CL |
| $t_{wch}$ | Write Command hold time | 1 | 20 |
| $t_{wcr}$ | Write Command hold time (referenced to RAS) | RL+CL | 20*(RL+CL) |
| $t_{wp}$ | Write Command pulse width | CL | 20*CL |
| $t_{ds}$ | Data setup time | 1 | 20 |
| $t_{dh}$ | Data hold time | CL | 20*CL |
| $t_{dhr}$ | Data hold time (referenced to RAS) | RL+CL | 20*(RL+CL) |
| $t_{rpc}$ | RAS precharge to CAS active | 1 | 20 |
| $t_{csr}$ | CAS setup time for CAS-before-RAS refresh | 1 | 20 |
| $t_{chr}$ | CAS hold time for CAS-before-RAS refresh | RL+CL | 20*(RL+CL) |
| $t_{asr}$ | Row Address setup time | 1 | 20 |

DRAM Access times required - Fast-page mode.

The following table gives the access times required to read from DRAM into the GLINT 500TX.

A CAS access time of 15 ns or better is required for a system clock of 50MHz with the CAS-low parameter set to 1 clock.

Table 9-16. Localbuffer Access Time Requirements - Fast Page Mode.

| Symbol | Parameter | Nominal timing in system clocks | Nominal timing at 50MHz |
|---|---|---|---|
| $t_{cpa}$ | Access time from CAS precharge | CL + 1 | 20*(CL+1) -5 |
| $t_{rac}$ | Access time from RAS | RL+CL | 20*(RL+CL) -5 |
| $t_{cac}$ | Access time from CAS | CL | 20*CL -5 |
| $t_{oea}$ | Access time from OE | CL | 20*CL -5 |
| $t_{caa}$ | Access time from Column Address | CL + 1 | 20*(CL+1) -5 |

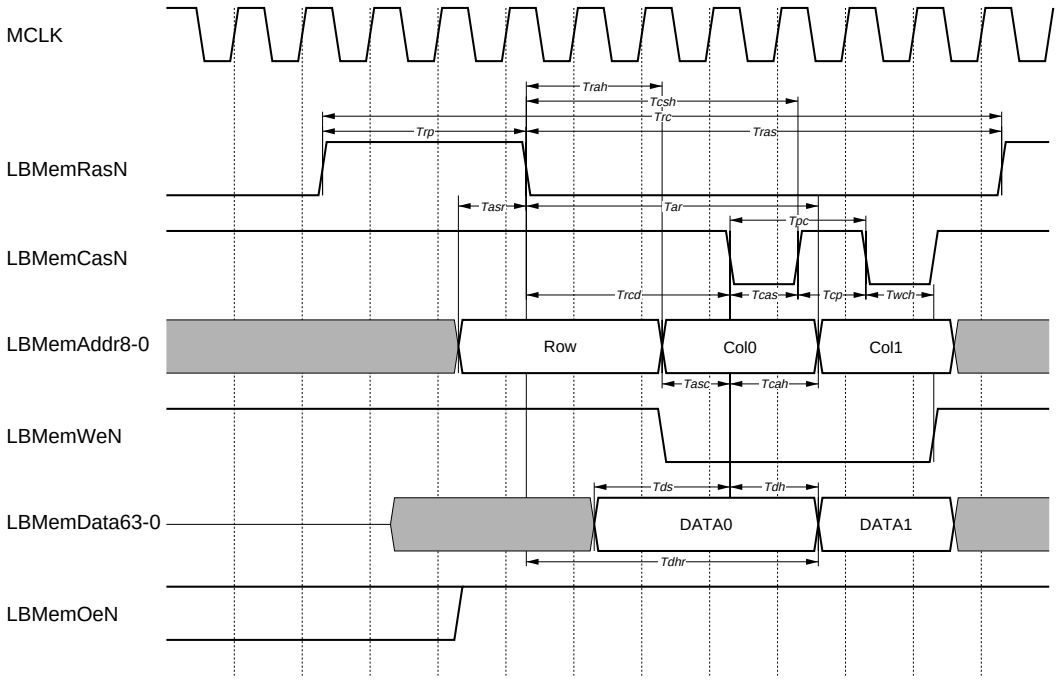


Figure 9-15 Localbuffer Write Timings - EDO mode

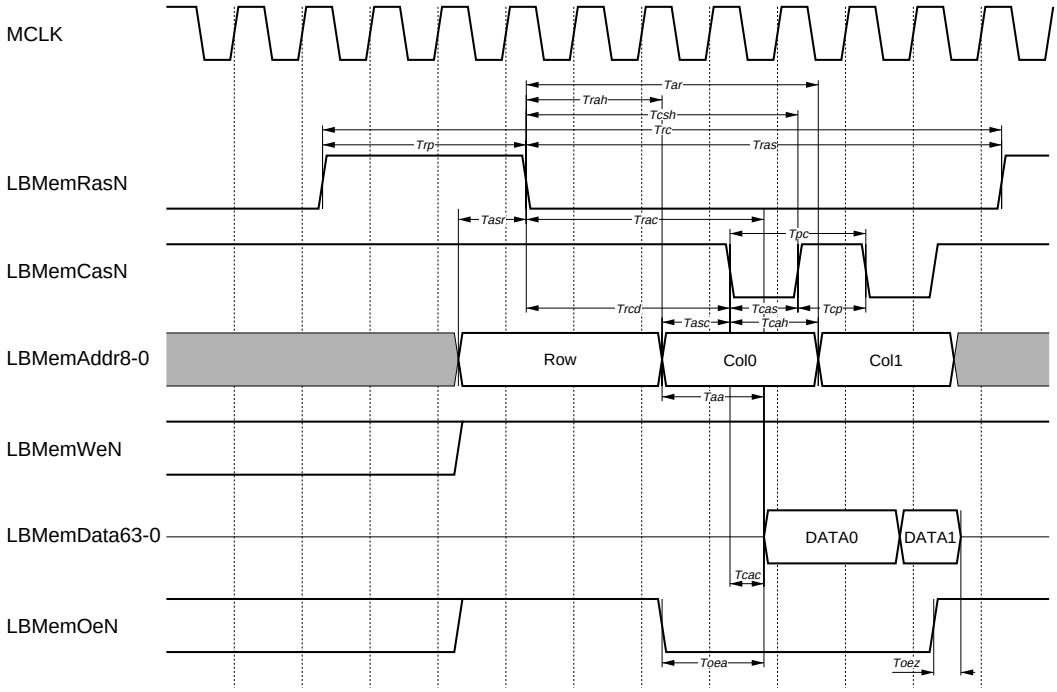


Figure 9-16 Localbuffer Read Timings - EDO mode

Table 9-17 Localbuffer Timing - EDO mode

| Symbol | Parameter | Nominal timing in system clocks | Nominal timing at 50MHz |
|---|---|---|---|
| $t_{cas}$ | CAS Pulse Width | 0.5 | 10 |
| $t_{crp}$ | CAS to RAS Precharge | 1.5 | 30 |
| $t_{csh}$ | CAS hold time | RL+1 | 20*(RL+1) |
| $t_{pc}$ | Page-mode cycle time | 1 | 20 |
| $t_{cp}$ | CAS precharge time | 0.5 | 10 |
| $t_{rp}$ | RAS precharge time | RP | 20*RP |
| $t_{rc}$ | Random read or write Cycle time | RL + RP+1 | 20*(RL+RP+1) |
| $t_{ras}$ | RAS pulse Width | RL+1 | 20*(RL+1) |
| $t_{rcd}$ | RAS to CAS delay time | RL+0.5 | 20*(RL+0.5) |
| $t_{rah}$ | Row Addres hold time | 1 | 20 |
| $t_{ar}$ | Column address Hold time (referenced to RAS) | RL+CL | 20*(RL+CL) |
| $t_{asc}$ | Column Address setup time | 1 | 20 |
| $t_{cah}$ | Column Address Hold time | 0.5 | 10 |
| $t_{wch}$ | Write Command hold time | 0.5 | 10 |
| $t_{wcr}$ | Write Command hold time (referenced to RAS) | RL+CL | 20*(RL+CL) |
| $t_{ds}$ | Data setup time | 0.5 | 10 |
| $t_{dh}$ | Data hold time | 0.5 | 10 |
| $t_{dhr}$ | Data hold time (referenced to RAS) | RL+1 | 20*(RL+1) |
| $t_{rpc}$ | RAS precharge to CAS active | 1 | 20 |
| $t_{csr}$ | CAS setup time for CAS-before-RAS refresh | 1 | 20 |
| $t_{chr}$ | CAS hold time for CAS-before-RAS refresh | RL+CL | 20*(RL+CL) |
| $t_{asr}$ | Row Address setup time | 1 | 20 |

DRAM Access times required - EDO mode.

The following table gives the access times required to read from DRAM into the GLINT 500TX.

A HyperPage Mode cycle time of 20 ns or better is required for a system clock of 50MHz.

Table 9-18. Localbuffer Access Time Requirements - EDO Mode.

| Symbol | Parameter | Nominal timing in system clocks | Nominal timing at 50MHz |
|---|---|---|---|
| $t_{cpa}$ | Access time from CAS precharge | 1.5 | 30 |
| $t_{rac}$ | Access time from RAS | RL+1.5 | 20*(RL+ 1.5) |
| $t_{cac}$ | Access time from CAS | 1 | 20 |
| $t_{oea}$ | Access time from OE | 1.5 | 30 |
| $t_{caa}$ | Access time from Column Address | 1.5 | 30 |

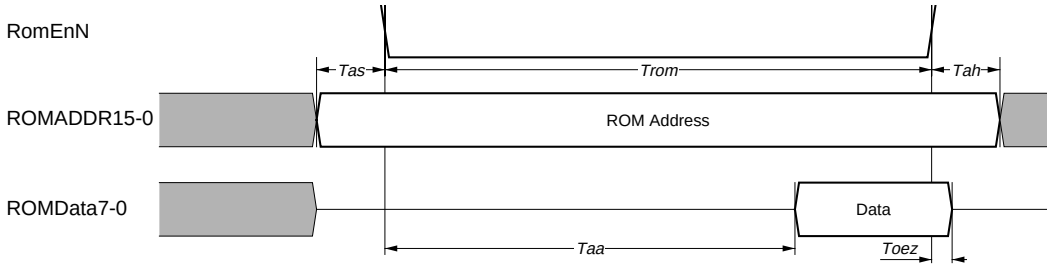


Figure 9-17 ROM Read Timings

Table 9-19. ROM Read Timings.

| Symbol | Parameter | Nominal timing in system clocks | Nominal timing at 50MHz |
|---|---|---|---|
| $t_{rom}$ | ROMEN low time | 8 | 160 ns |
| $t_{as}$ | Address setup time | 1 | 20 ns |
| $t_{ah}$ | Address hold time | 1 | 20 ns |

Table 9-20. ROM Access Times.

| Symbol | Parameter | Nominal timing in system clocks | Nominal timing at 50MHz |
|---|---|---|---|
| $t_{aa}$ | Access time from ROMEN | - | 150 ns min. |
| $t_{oez}$ | Access time from Column Address | - | 20 ns min. |

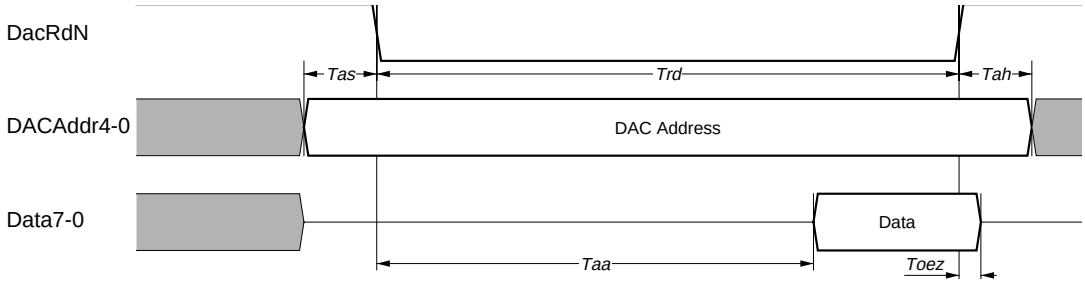


Figure 9-18 LUT-DAC Read Timings

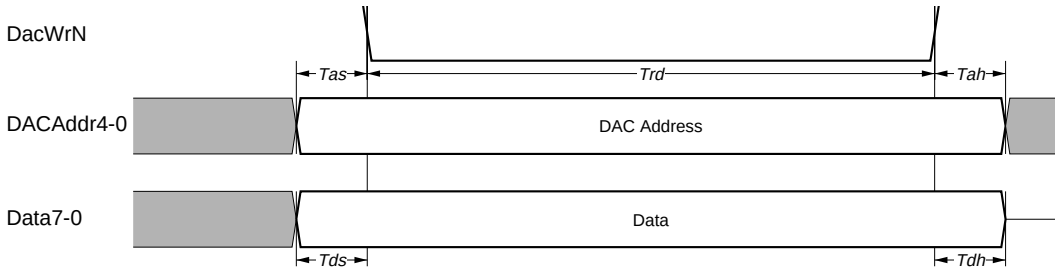


Figure 9-19 LUT-DAC Write Timings

Table 9-21. LUT-DAC Timings.

| Symbol | Parameter | Nominal timing in system clocks | Nominal timing at 50MHz |
|---|---|---|---|
| $t_{rd}$ | DACRDN low time | 8 | 160 ns |
| $t_{as}$ | Address setup time | 1 | 20 ns |
| $t_{ah}$ | Address hold time | 1 | 20 ns |
| $t_{ds}$ | Data setup time | 1 | 20 ns |
| $t_{dh}$ | Data hold time | 1 | 20 ns |

Table 9-22. LUT-DAC Access Times.

| Symbol | Parameter | Nominal timing in system clocks | Nominal timing at 50MHz |
|---|---|---|---|
| $t_{aa}$ | Access time from DACRDN | - | 150 ns min. |
| $t_{oez}$ | Access time from Column Address | - | 20 ns min. |

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# 10. Pin Information.

## 10.1 Package Pinout

The GLINT 500TX comes in a 304 pin QFP package. The pin numbering is shown in figure 10-1.

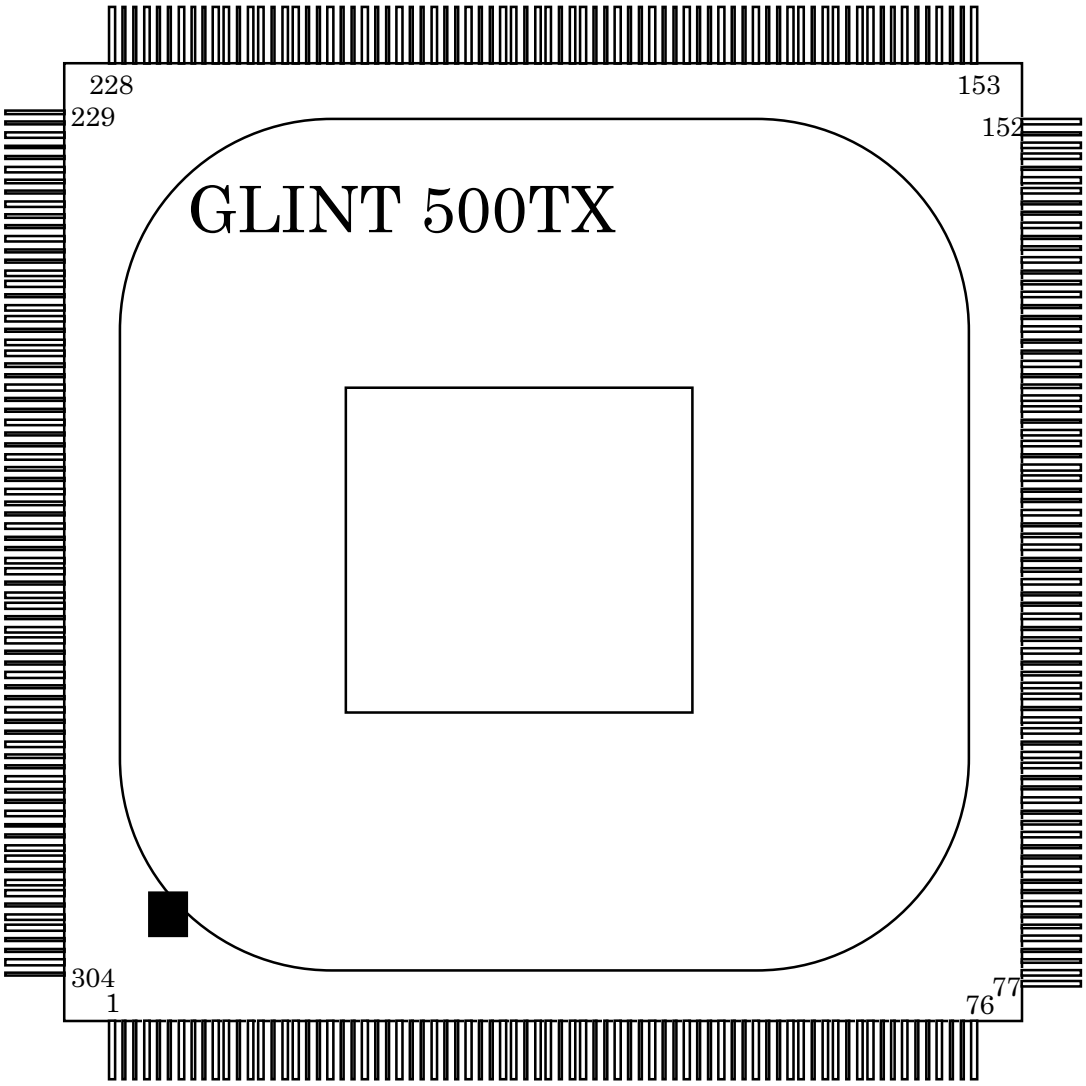


Figure 10-1. GLINT 500TX Pin Numbering.

## 10.2 Pin Descriptions

Table 10-1 provides a brief description of each pin. The following pin type definitions are used.

I Input signal
O Output signal
I/O Bidirectional signal

Output power ratings are marked as 4, 8, or 12 for the milliamp current rating or P indicating a PCI compatible output.

Table 10-1. Pin Descriptions

| Symbol | Type | Power | Pin Number(s) | Description |
|---|---|---|---|---|
| **Clocks** | | | | |
| PCIClk | I | | 11 | PCI clock. |
| MClk | I | | 262 | System clock. Used for all internally clocked functions on the chip and by the memory controllers. |
| VClk | I | | 296 | Video clock. Used by internal video rate circuitry. Typically connected to a divided pixel clock. |
| LDClk | O | 12 | 304 | LUT-DAC Load clock. |
| **PCI Interface** | | | | |
| PCIAD(31:0) | I/O | P | 14-15, 17-22, 27-28, 30-32, 34-36, 51, 54-57, 59-61, 64-67, 73-76 | PCI Address and Data bus. |
| PCICBEN(3:0) | I/O | P | 23, 37, 50, 62 | PCI command and bytes enables. |
| PCIPar | I/O | P | 49 | PCI parity bit. |
| PCIFrameN | I/O | P | 40 | PCI frame control line. |
| PCIIRdyN | I/O | P | 41 | PCI Initiator Ready. |
| PCITRdyN | I/O | P | 42 | PCI Target Ready. |
| PCIStopN | I/O | P | 44 | PCI Target Stop control. |
| PCIIdsel | I | | 26 | PCI slot configuration select line. |
| PCIDevselN | I/O | P | 43 | PCI Target selected. |
| PCIReqN | O | P | 13 | PCI Master request line. |
| PCIGntN | I | | 12 | PCI Master Grant line. |
| PCIFifoIndis | O | P | 47 | PCI Input Fifo Disconnect |
| PCIFifoOutDis | O | P | 48 | PCI OutputFifo Disconnect. |
| PCIIntAN | OD | P | 5 | PCI interrupt line. |

| Symbol | Type | Power | Pin Number(s) | Description |
|---|---|---|---|---|

## Localbuffer Interface

| | | | | |
|---|---|---|---|---|
| LBMemAddr(11:0) | O | 12 | 140-141, 144-145, 84-85, 88-93 | Localbuffer Address bus. |
| LBMemRasN(1:0) | O | 12 | 109, 113 | Localbuffer DRAM RAS control lines. These lines are electrically equivalent. Two lines are provided for buffering purposes. |
| LBMemCasN(5:0) | O | 12 | 110-111, 112, 116-118 | Localbuffer DRAM CAS control lines.<br>These lines are used as byte enables for localbuffer accesses |
| LBMemOeN(1:0) | O | 12 | 158-159 | Localbuffer DRAM Output Enable Lines. These lines Select between 2 banks of memory for reads. For 1 bank only LBMemOEN(0) is used. |
| LBMemWeN(1:0) | O | 12 | 162-163 | Localbuffer DRAM Write Enable Lines. These lines are used to select between 2 banks of memory for writes. For 1 bank only LBMemWEN(0) is used. |
| LBMemData(47:0) | I/O | 12 | 77-80, 82-83, 95-101,<br>104-108, 122-125, 128-133, 136-139, 146-157, 164-167 | Localbuffer Data Bus. Also used at reset time to initialise internal registers.<br>LBMemData(47:0) are also used as Data(7:0) for External Video/LUT-DAC and Expansion Rom.<br>LBMemData(39:24) are also used as Address(15:0) for External Video and Expansion ROM. |

## Framebuffer Interface

| | | | | |
|---|---|---|---|---|
| FBMemAddr(8:0) | O | 12 | 217-219, 222, 224-228 | Framebuffer Address Bus. |
| FBMemRasN(3:0) | O | 12 | 264-265, 259-260 | Framebuffer VRAM RAS control lines. |
| FBMemCasN(7:0) | O | 12 | 186-189, 192-195 | Framebuffer VRAM CAS control lines. |
| FBMemOeN(3:0) | O | 12 | 253, 256-258 | Framebuffer VRAM Output Enable lines. |
| FBMemWeN(3:0) | O | 12 | 249-252 | Framebuffer VRAM Write Enable lines. |
| FBMemDSF(1:0) | O | 12 | 269, 271 | Framebuffer VRAM DSF lines. These lines are electrically the same. Two DSF lines are provided for buffering purposes.<br>NB. These DSF lines do NOT equate to the DSF0 and DSF1 lines of hyperpipelined VRAMs such as Toshiba TC528267 |

| Symbol | Type | Power | Pin Number(s) | Description |
|---|---|---|---|---|
| FBMemData(63:0) | I/O | 12 | 170-175, 178-182, 184-185, 196-203, 206-211, 213-216, 229-237, 240-245, 248, 272-277, 280-286, 288-291 | Framebuffer Data Bus. |
| FBGnt | I/O | 8 | 4 | Shared Framebuffer grant. This line is an output when GLINT 300SX is a shared framebuffer primary controller. This line is an input when a secondary controller. |
| FBSelOE/SOE2 | I/O | 8 | 2 | When TX Enhanced function pin is pulled high, this pin is VRAM serial output Enable 2 , otherwise it is the Shared Framebuffer output enable which can be used to control memory control signal buffers when a secondary shared framebuffer controller. |

## Video Control

| | | | | |
|---|---|---|---|---|
| VClkCtl(1:0) | O | 8 | 70-71 | Pixel clock select lines. Can be used to control multi-rate Pixel clock generation chips. |
| HSync/ExtTxCmd1 | O | 8 | 292 | Video Horizontal Sync line / Controls the external transfer address generator and acknowledges an ExtTxReq |
| VSync/ExtTxCmd0 | O | 8 | 293 | Video Vertical Sync line / Controls the external transfer address generator and acknowledges an ExtTxReq |
| QSF/ExtTxReq | I | | 297 | Input from VRAM QSF pin or External Timing generator to control VRAM transfer cycles |
| CBlank/ExtTxSplit | I/O | 8 | 298 | Video Composite Blank line / Qualifies ExtTxReq as a split transfer (instead of full transfer) |
| CompSync | O | 8 | 1 | Video Composite Sync line. |
| DacWrN | O | 8 | 120 | LUT-DAC / External VideoWrite line. |
| DacRdN | O | 8 | 121 | LUT-DAC / External VideoRead line. |
| SClk(1:0) | O | 12 | 299, 301 | Video serial clocks. |
| SOE(1:0) | O | 12 | 302-303 | Video serial output enable. |
| SOE3 | O | 12 | 46 | When the TX Enhanced function pin is pulled high, this pin is VRAM serial output enable 3, otherwise the pin is tri-state. |

| Symbol | Type | Power | Pin Number(s) | Description |
|---|---|---|---|---|

Misc.

| | | | | |
|---|---|---|---|---|
| TXEnhanced | I | | 270 | TX Enhanced Function pin.<br>When this pin is pulled low, the GLINT 500TX pin functionality remains consistent with GLINT 300 SX. When this pin is pulled high, the SOE2 and SOE3 functionality is enabled. The new shared Localbuffer/Framebuffer functionality and S3 compatible framebuffer modes are enabled. |
| PCIRstN | I | | 10 | Power On and Hardware reset. |
| ExtIntN | I | | 223 | Ext Interrupt Internal Pullup |
| RomEnN | O | 8 | 119 | Expansion ROM enable |
| TestMode | I | | 263 | Test mode control. |
| TestAClk | I | | 6 | Test clock A. Internal Pulldown |
| TestBClk | I | | 7 | Test clock B. Internal Pulldown |
| TestCClk | I | | 268 | Test clock C. Internal Pulldown |
| DI1 | I | | 58 | Test Driver Inhibit. This pin must be pulled high in functional mode. |
| DI2 | I | | 134 | Test Driver Inhibit. This pin must be pulled high in functional mode. |
| VDD | I | | 8, 24, 38, 52, 68, 86, 102, 114, 126, 142, 160, 168, 176, 190, 204, 220, 238, 246, 254, 266, 278, 294 | Vdd pins. All must be used |
| GND | I | | 9, 16, 25, 29, 33, 39, 45, 53, 63, 69, 72, 81, 87, 94, 103, 115, 127, 135, 143, 161, 169, 177, 183, 191, 205, 212, 221, 239, 247, 255, 261, 267, 279, 287, 295, 300 | Ground pins. All must be used. |

## 10.3 Pin Lists.

Table 10-2. Alphabetical Pin Listing

| Symbol | Pin Numbers |
|---|---|
| CBlank/ExtTxSplit | 298 |
| CompSync | 1 |
| DacRdN | 121 |
| DacWrN | 120 |
| DI1 | 58 |
| DI2 | 134 |
| ExtIntN | 223 |
| FBGntN | 4 |
| FBMemAddr(8:0) | 217-219, 222, 224-228 |
| FBMemCasN(7:0) | 186-189, 192-195 |
| FBMemData(63:0) | 170-175, 178-182, 184-185, 196-203, 206-211, 213-216, 229-237, 240-245, 248, 272-277, 280-286, 288-291 |
| FBMemDSF(1:0) | 269, 271 |
| FBMemOeN(3:0) | 253, 256-258 |
| FBMemRasN(3:0) | 264-265, 259-260 |
| FBMemWeN(3:0) | 249-252 |
| FBReqN | 3 |
| FBSelOEN/SOE2 | 2 |
| GND | 9, 16, 25, 29, 33, 39, 45, 53, 63, 69, 72, 81, 87, 94, 103, 115, 127, 135, 143, 161, 169, 177, 183, 191, 205, 212, 221, 239, 247, 255, 261, 267, 279, 287, 295, 300 |
| HSync/ExtTxCmd1 | 292 |
| LBMemAddr(11:0) | 140-141, 144-145, 84-85, 88-93 |
| LBMemCasN(5:0) | 110-111, 112, 116-118 |
| LBMemData(47:0) | 77-80, 82-83, 95-101, 104-108, 122-125, 128-133, 136-139, 146-157, 164-167 |
| LBMemOeN(1:0) | 158-159 |
| LBMemRasN(1:0) | 109, 113 |
| LBMemWeN | 162-163 |
| LDClk | 304 |
| MClk | 262 |
| PCIAD(31:0) | 14-15, 17-22, 27-28, 30-32, 34-36, 51, 54-57, 59-61, 64-67, 73-76 |
| PCICBEN(3:0) | 23, 37, 50, 62 |
| PCIClk | 11 |
| PCIDevselN | 43 |
| PCIFifoInDis | 47 |
| PCIFifoOutDis | 48 |
| PCIFrameN | 40 |
| PCIGntN | 12 |
| PCIIdsel | 26 |
| PCIIntAN | 5 |
| PCIIRdyN | 41 |

Table 10-2. Alphabetical Pin Listing (Continued)

| Symbol | Pin Numbers |
|---|---|
| PCIPar | 49 |
| PCIPerrN | 47 |
| PCIReqN | 13 |
| PCIRstN | 10 |
| PCISerrN | 48 |
| PCIStopN | 44 |
| PCITRdyN | 42 |
| VClkCtl(1:0) | 70-71 |
| QSF/ExtTxReq | 297 |
| RomEnN | 119 |
| SClk(1:0) | 299, 301 |
| SOE(1:0) | 302-303 |
| SOE3 | 46 |
| TestAClk | 6 |
| TestBClk | 7 |
| TestCClk | 268 |
| TestMode | 263 |
| TXEnhanced | 270 |
| VClk | 296 |
| VDD | 8, 24, 38, 52, 68, 86, 102, 114, 126, 142, 160, 168, 176, 190, 204, 220, 238, 246, 254, 266, 278, 294 |
| VSync/ExtTxCmd0 | 293 |

Table 10-3. Numerical Pin Listing

| Pin | Name |
|---|---|
| 1 | CompSync |
| 2 | FBSelOEN/SOE2 |
| 3 | FBReqN |
| 4 | FBGntN |
| 5 | PCIIntAN |
| 6 | TestAClk |
| 7 | TestBClk |
| 8 | VDD |
| 9 | GND |
| 10 | PCIRstN |
| 11 | PCIClk |
| 12 | PCIGntN |
| 13 | PCIReqN |
| 14 | PCIAD31 |
| 15 | PCIAD30 |
| 16 | GND |
| 17 | PCIAD29 |
| 18 | PCIAD28 |
| 19 | PCIAD27 |
| 20 | PCIAD26 |
| 21 | PCIAD25 |
| 22 | PCIAD24 |
| 23 | PCICBEN3 |
| 24 | VDD |
| 25 | GND |
| 26 | PCIIdsel |
| 27 | PCIAD23 |
| 28 | PCIAD22 |
| 29 | GND |
| 30 | PCIAD21 |
| 31 | PCIAD20 |
| 32 | PCIAD19 |
| 33 | GND |
| 34 | PCIAD18 |
| 35 | PCIAD17 |
| 36 | PCIAD16 |
| 37 | PCICBEN2 |
| 38 | VDD |

| Pin | Name |
|---|---|
| 39 | GND |
| 40 | PCIFrameN |
| 41 | PCIIRdyN |
| 42 | PCITRdyN |
| 43 | PCIDevselN |
| 44 | PCIStopN |
| 45 | GND |
| 46 | SOE3 |
| 47 | PCIFifoInDis |
| 48 | PCIFifoOutDis |
| 49 | PCIPar |
| 50 | PCICBEN1 |
| 51 | PCIAD15 |
| 52 | VDD |
| 53 | GND |
| 54 | PCIAD14 |
| 55 | PCIAD13 |
| 56 | PCIAD12 |
| 57 | PCIAD11 |
| 58 | DI1 |
| 59 | PCIAD10 |
| 60 | PCIAD9 |
| 61 | PCIAD8 |
| 62 | PCICBEN0 |
| 63 | GND |
| 64 | PCIAD7 |
| 65 | PCIAD6 |
| 66 | PCIAD5 |
| 67 | PCIAD4 |
| 68 | VDD |
| 69 | GND |
| 70 | VClkCtl1 |
| 71 | VClkCtl0 |
| 72 | GND |
| 73 | PCIAD3 |
| 74 | PCIAD2 |
| 75 | PCIAD1 |
| 76 | PCIAD0 |

Table 10-3. Numerical Pin Listing (Continued)

| Pin | Name |
|---|---|
| 77 | LBMemData47 |
| 78 | LBMemData46 |
| 79 | LBMemData45 |
| 80 | LBMemData44 |
| 81 | GND |
| 82 | LBMemData43 |
| 83 | LBMemData42 |
| 84 | LBMemAddr7 |
| 85 | LBMemAddr6 |
| 86 | VDD |
| 87 | GND |
| 88 | LBMemAddr5 |
| 89 | LBMemAddr4 |
| 90 | LBMemAddr3 |
| 91 | LBMemAddr2 |
| 92 | LBMemAddr1 |
| 93 | LBMemAddr0 |
| 94 | GND |
| 95 | LBMemData41 |
| 96 | LBMemData40 |
| 97 | LBMemData39 |
| 98 | LBMemData38 |
| 99 | LBMemData37 |
| 100 | LBMemData36 |
| 101 | LBMemData35 |
| 102 | VDD |
| 103 | GND |
| 104 | LBMemData34 |
| 105 | LBMemData33 |
| 106 | LBMemData32 |
| 107 | LBMemData31 |
| 108 | LBMemData30 |
| 109 | LBMemRasN1 |
| 110 | LBMemCasN5 |
| 111 | LBMemCasN4 |
| 112 | LBMemCasN3 |
| 113 | LBMemRasN0 |
| 114 | VDD |

| Pin | Name |
|---|---|
| 115 | GND |
| 116 | LBMemCasN2 |
| 117 | LBMemCasN1 |
| 118 | LBMemCasN0 |
| 119 | RomEnN |
| 120 | DacWrN |
| 121 | DacRdN |
| 122 | LBMemData29 |
| 123 | LBMemData28 |
| 124 | LBMemData27 |
| 125 | LBMemData26 |
| 126 | VDD |
| 127 | GND |
| 128 | LBMemData25 |
| 129 | LBMemData24 |
| 130 | LBMemData23 |
| 131 | LBMemData22 |
| 132 | LBMemData21 |
| 133 | LBMemData20 |
| 134 | DI2 |
| 135 | GND |
| 136 | LBMemData19 |
| 137 | LBMemData18 |
| 138 | LBMemData17 |
| 139 | LBMemData16 |
| 140 | LBMemAddr11 |
| 141 | LBMemAddr10 |
| 142 | VDD |
| 143 | GND |
| 144 | LBMemAddr9 |
| 145 | LBMemAddr8 |
| 146 | LBMemData15 |
| 147 | LBMemData14 |
| 148 | LBMemData13 |
| 149 | LBMemData12 |
| 150 | LBMemData11 |
| 151 | LBMemData10 |
| 152 | LBMemData9 |

Table 10-3 Numerical Pin Listing (Continued)

| Pin | Name |
|---|---|
| 153 | LBMemData8 |
| 154 | LBMemData7 |
| 155 | LBMemData6 |
| 156 | LBMemData5 |
| 157 | LBMemData4 |
| 158 | LBMemOeN1 |
| 159 | LBMemOeN0 |
| 160 | VDD |
| 161 | GND |
| 162 | LBMemWeN1 |
| 163 | LBMemWeN0 |
| 164 | LBMemData3 |
| 165 | LBMemData2 |
| 166 | LBMemData1 |
| 167 | LBMemData0 |
| 168 | VDD |
| 169 | GND |
| 170 | FBMemData63 |
| 171 | FBMemData62 |
| 172 | FBMemData61 |
| 173 | FBMemData60 |
| 174 | FBMemData59 |
| 175 | FBMemData58 |
| 176 | VDD |
| 177 | GND |
| 178 | FBMemData57 |
| 179 | FBMemData56 |
| 180 | FBMemData55 |
| 181 | FBMemData54 |
| 182 | FBMemData53 |
| 183 | GND |
| 184 | FBMemData52 |
| 185 | FBMemData51 |
| 186 | FBMemCasN7 |
| 187 | FBMemCasN6 |
| 188 | FBMemCasN5 |
| 189 | FBMemCasN4 |
| 190 | VDD |

| Pin | Name |
|---|---|
| 191 | GND |
| 192 | FBMemCasN3 |
| 193 | FBMemCasN2 |
| 194 | FBMemCasN1 |
| 195 | FBMemCasN0 |
| 196 | FBMemData50 |
| 197 | FBMemData49 |
| 198 | FBMemData48 |
| 199 | FBMemData47 |
| 200 | FBMemData46 |
| 201 | FBMemData45 |
| 202 | FBMemData44 |
| 203 | FBMemData43 |
| 204 | VDD |
| 205 | GND |
| 206 | FBMemData42 |
| 207 | FBMemData41 |
| 208 | FBMemData40 |
| 209 | FBMemData39 |
| 210 | FBMemData38 |
| 211 | FBMemData37 |
| 212 | GND |
| 213 | FBMemData36 |
| 214 | FBMemData35 |
| 215 | FBMemData34 |
| 216 | FBMemData33 |
| 217 | FBMemAddr8 |
| 218 | FBMemAddr7 |
| 219 | FBMemAddr6 |
| 220 | VDD |
| 221 | GND |
| 222 | FBMemAddr5 |
| 223 | ExtIntN |
| 224 | FBMemAddr4 |
| 225 | FBMemAddr3 |
| 226 | FBMemAddr2 |
| 227 | FBMemAddr1 |
| 228 | FBMemAddr0 |

Table 10-3. Numerical Pin Listing (Continued)

| Pin | Name |
|---|---|
| 229 | FBMemData32 |
| 230 | FBMemData31 |
| 231 | FBMemData30 |
| 232 | FBMemData29 |
| 233 | FBMemData28 |
| 234 | FBMemData27 |
| 235 | FBMemData26 |
| 236 | FBMemData25 |
| 237 | FBMemData24 |
| 238 | VDD |
| 239 | GND |
| 240 | FBMemData23 |
| 241 | FBMemData22 |
| 242 | FBMemData21 |
| 243 | FBMemData20 |
| 244 | FBMemData19 |
| 245 | FBMemData18 |
| 246 | VDD |
| 247 | GND |
| 248 | FBMemData17 |
| 249 | FBMemWeN3 |
| 250 | FBMemWeN2 |
| 251 | FBMemWeN1 |
| 252 | FBMemWeN0 |
| 253 | FBMemOeN3 |
| 254 | VDD |
| 255 | GND |
| 256 | FBMemOeN2 |
| 257 | FBMemOeN1 |
| 258 | FBMemOeN0 |
| 259 | FBMemRasN1 |
| 260 | FBMemRasN0 |
| 261 | GND |
| 262 | MClk |
| 263 | TestMode |
| 264 | FBMemRasN3 |
| 265 | FBMemRasN2 |
| 266 | VDD |

| Pin | Name |
|---|---|
| 267 | GND |
| 268 | TestCClk |
| 269 | FBMemDSF1 |
| 270 | TXEnhanced |
| 271 | FBMemDSF0 |
| 272 | FBMemData16 |
| 273 | FBMemData15 |
| 274 | FBMemData14 |
| 275 | FBMemData13 |
| 276 | FBMemData12 |
| 277 | FBMemData11 |
| 278 | VDD |
| 279 | GND |
| 280 | FBMemData10 |
| 281 | FBMemData9 |
| 282 | FBMemData8 |
| 283 | FBMemData7 |
| 284 | FBMemData6 |
| 285 | FBMemData5 |
| 286 | FBMemData4 |
| 287 | GND |
| 288 | FBMemData3 |
| 289 | FBMemData2 |
| 290 | FBMemData1 |
| 291 | FBMemData0 |
| 292 | HSync/ExtTxCmd1 |
| 293 | VSync/ExtTxCmd0 |
| 294 | VDD |
| 295 | GND |
| 296 | VClk |
| 297 | QSF/ExtTxReq |
| 298 | CBlank/ExtTxSplit |
| 299 | SClk1 |
| 300 | GND |
| 301 | SClk0 |
| 302 | SOE1 |
| 303 | SOE0 |
| 304 | LDClk |

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# 11. Thermal Management

The maximum junction temperature must be kept below $T_j$(max)and this can only be guaranteed by proper analysis of the operating environment and the thermal path between the die and the air surrounding it.

## 11.1 Device Characteristics

These are fixed characteristics of the device and are independent of the operating environment or the characteristics of any heatsink:-

| | | |
|---|---|---|
| $T_{j(max)}$ | = | 100 °C. |
| Pd(max) | = | 3.7 Watts @ Vdd(max), $f_{MClk}$ = 50MHz. |
| $\theta_{jc}$ | = | 0 °C/Watt.<br>(there is no case to consider here, so this resistance is negligible) |

## 11.2 Thermal Model

The formula used to calculate the junction temperature ($T_j$) is

$$T_j = T_a + Pd \times ( \theta_{jc} + \theta_{cs} + \theta_{sa} )$$

$$= T_a + Pd \times \theta_{ja}$$

Where:-

| | | |
|---|---|---|
| $T_j$ | = | Junction temperature (°C) |
| $T_a$ | = | Ambient temperature (°C) |
| Pd | = | Power dissipation (Watts) |
| $\theta_{jc}$ | = | Junction to Case thermal resistance (°C/Watt) |
| $\theta_{cs}$ | = | Case to Heatsink thermal resistance (°C/Watt) |
| $\theta_{sa}$ | = | Heatsink to Air thermal resistance (°C/Watt) |
| $\theta_{ja}$ | = | Total Junction to Air thermal resistance (°C/Watt) |

The $\theta_{ja}$ form of the equation is more appropriate when there is no heatsink attached to the device (see below).

## 11.3 Operation Without Heatsink

Generally it is not recommended that this device is operated without a heatsink due to the high airflow rates which must be maintained to keep $T_j$ below $T_j$(max).

The 304 CQFP package with the die exposed on the top surface and no attached heatsink has the following $\theta_{ja}$ characteristic as a function of airflow:-

Table 11-1. 304 pin CQFP Package Thermal Characteristics

| Airflow (lfpm) | | $\theta_{ja}$ (° C/W) |
|---|---|---|
| 0 | (Convection Cooling) | 30 |
| 50 | (0.25m/sec) | 26 |
| 100 | (0.5m/sec) | 23 |
| 200 | (1m/sec) | 20 |
| 400 | (2m/sec) | 18 |

Example:-
Ta = 30 ° C
Airflow = 400 lfpm
$T_j$ = 30 + 3.7 x (18)
= 96.6 ° C

## 11.4 Operation With Heatsink

With a heatsink attached to the device the junction temperature will depend on $\theta_{cs}$ and $\theta_{sa}$. $\theta_{cs}$ is the thermal resistance of the join between the heatsink and the exposed back surface of the die. $\theta_{sa}$ is the thermal resistance of the heatsink and will be a function of system airflow.

Example:-
Ta = 40 ° C
$\theta_{cs}$ = 1.0 ° C/Watt (EG 7655 epoxy - see below)
$\theta_{sa}$ $\leq$ (100 - 40)/3.7 - 1.0
$\leq$ 15.2 ° C/Watt.

In this example a heatsink must be chosen which has a thermal resistance figure of no greater than 15.2 ° C/Watt at an airflow matching the expected airflow in the system.

## 11.5 Heatsink Attachment

Two methods have been approved for the purpose of attaching a heatsink directly onto the exposed die surface and the Urethane conformal coating material covering the top of the CQFP package.

### 11.5.1 Attachment Method 1

Thermally conductive epoxy type EG 7655 from A.I. Technology Inc. The thickness of the epoxy layer should be between 0.05mm and 0.15mm with 100% coverage of the exposed die area, and a maximum voiding in the bond area of 3%. This epoxy should not be used outside the die area.

Typical achievable $\theta_{cs}$ using this method is 1.0 ° C/Watt.

### 11.5.2 Attachment Method 2

Chomerics Thermattach 405 thermally conductive tape when used with an additional adhesive, such as Loctite Output 315, for structural support outside the die area.

Typical achievable $\theta_{cs}$ using this method is 2.2 ° C/Watt.

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# 12. Reset Control and Test Mode

## 12.1 Reset

A number of parameters for the GLINT 500TX are set at reset , such as Localbuffer and Framebuffer memory size and speed. The reset state is configured with resistors connected to the Localbuffer data pins. The state of the data pins is sampled on the rising edge of the reset line. Various parameters may be configured e.g.

- Framebuffer and Localbuffer sizes.
- Framebuffer and Localbuffer RAS and CAS timings
- Framebuffer and Localbuffer widths.

To set a bit to 1 the relevant data pin should be tied to $V_{DD}$ (3.3V) with a 10K resistor.

To set a bit to 0 the relevant data pin should be tied to ground with a 4K7 resistor.

## 12.2 Clock Operation at Reset

The GLINT 500TX is a synchronous device. For correct reset operation the clocks must be running during the reset pulse. At power-up care must be taken to ensure that MClk and VClk are running before the system reset pulse completes.

## 12.3 Reset Localbuffer Configuration

This is determined as follows by the reset state of the Localbuffer data pins:

Bit 0 Number of Banks

| | |
|---|---|
| 0 | 1 Bank |
| 1 | 2 Banks |

Bits 2-1 Page Size

| | |
|---|---|
| 0 | 256 Pixels |
| 1 | 512 Pixels |
| 2 | 1024 Pixels |
| 3 | 2048 Pixels |

Bits 4-3 RAS-CAS low

| | |
|---|---|
| 0 | 2 Clocks |
| 1 | 3 Clocks |
| 2 | 4 Clocks |
| 3 | 5 Clocks |

Bits 6-5 RAS Precharge

| | |
|---|---|
| 0 | 2 Clocks |
| 1 | 3 Clocks |
| 2 | 4 Clocks |
| 3 | 5 Clocks |

### Bits 8-7 CAS Low

0 1 Clocks
1 2 Clocks
2 3 Clocks
3 4 Clocks

### Bit 9 Page Mode Disable

0 Page mode Enabled
1 Page mode Disabled

### Bit 18 Dual Write Enables

0 2 WE and 6 CAS pins
1 6 WE and 2 CAS pins

### Bits 21-20 PCI Maximum Latency

Forms the top 2 bits of the configuration space Maximum Latency register

### Bits 23-22 PCI Minimum Grant

Forms the top 2 bits of the configuration space Minimum Grant register

### Bits 26-24 Localbuffer Visible Region Size

0 1 Mbyte
1 2 Mbytes
2 4 Mbytes
3 8 Mbytes
4 16 Mbytes
5 32 Mbytes
6 64 Mbytes
7 0 Mbytes

### Bits 29-27 Localbuffer width

0 16 bits
1 18 bits
2 24 bits
3 32 bits
4 36 bits
5 40 bits
6 48 bits
7 Other width

### Bit 30 Localbuffer Bypass Packing

0 64 bit Localbuffer bypass step
1 32 bit Localbuffer bypass step

### Bit 31 Aperture 1 Enable

0 Aperture 1 disabled
1 Aperture 1 enabled

## 12.4 Reset Framebuffer Configuration

This is determined as follows by the reset state of the Framebuffer data lines:

Bits 1-0 RAS-CAS low

| | |
|---|---|
| 0 | 2 Clocks |
| 1 | 3 Clocks |
| 2 | 4 Clocks |
| 3 | 5 Clocks |

Bits 3-2 RAS Precharge

| | |
|---|---|
| 0 | 2 Clocks |
| 1 | 3 Clocks |
| 2 | 4 Clocks |
| 3 | 5 Clocks |

Bits 5-4 CAS Low

| | |
|---|---|
| 0 | 1 Clocks |
| 1 | 2 Clocks |
| 2 | 3 Clocks |
| 3 | 4 Clocks |

Bit 6 Page Mode Disable

| | |
|---|---|
| 0 | Page mode Enabled |
| 1 | Page mode Disabled |

Bit 10 Fast Mode Disable

| | |
|---|---|
| 0 | Enabled |
| 1 | Disabled |

Bits 12-11 Shared Framebuffer Mode

| | |
|---|---|
| 0 | Disabled |
| 1 | Arbiter |
| 2 | Requester |
| 3 | Reserved |

Bit 13 Video Transfer Disable

| | |
|---|---|
| 0 | Transfer Cycles Enabled |
| 1 | Transfer Cycles Disabled |

Bit 14 External VTG Select

0 Internal VTG
1 External VTG

Bits 16-15 Framebuffer Interleave

0 1 way
1 2 way
2 4 way
3 Reserved

Bits18-17 Block Fill Size

0 Disabled
1 4 Pixels
2 8 Pixels
3 Reserved

Bit 19 Dual Write Enables

0 4 WE and 8 CAS pins
1 8 WE and 4 CAS pins

Bit 20 TX Enhanced Shared Memory

0 GLINT 300SX compatible Shared Framebuffer control
1 Enhanced SharedMemory Control

Bit 21 SFBModeSwap

0 SFBMode field has default action
1 invert action of SFBMode field

Bit 22 EDO DRAM Localbuffer

0 Fast Page Mode DRAM fitted for Local buffer
1 EDO Dram fitted for Local Buffer

( This field has no direct effect on the hardware)

Bit 26 Base Class Zero

0 = GLINT 500TX returns a PCI Base class and sub-class of 03h 80h
1 = GLINT 500 TX returns a PCI Base Class and sub-Class of 00h 00h

Bit 27 Reserved

Bit 28 Aperture 1 Enable

0 Aperture 1 disabled
1 Aperture 1 enabled

Bits 31-29 Framebuffer Visible Region Size

0 1 Mbyte
1 2 Mbytes

| | |
|---|---|
| 2 | 4 Mbytes |
| 3 | 8 Mbytes |
| 4 | 16 Mbytes |
| 5 | 32 Mbytes |
| 6 | Reserved |
| 7 | 0 Mbytes |

## 12.5 Production Test Mode

This section describes how to place GLINT 500TX into a mode suitable for board production test. In Board ATE mode, all GLINT drivers are tristated. In order to do this, the DI1 and DI2 pins must be pulled low.

Table 12-1. GLINT 500TX Functional Mode

| Pin | |
|---|---|
| DI2 | high |
| DI1 | high |
| TestAClk | low |
| TestBClk | low |
| TestCClk | low |

Table 12-2. GLINT 500TX Board ATE Mode

| Pin | |
|---|---|
| DI1 | low |
| DI2 | low |
| TestAClk | low |
| TestBClk | low |
| TestCClk | low |

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# 13. Package Drawings

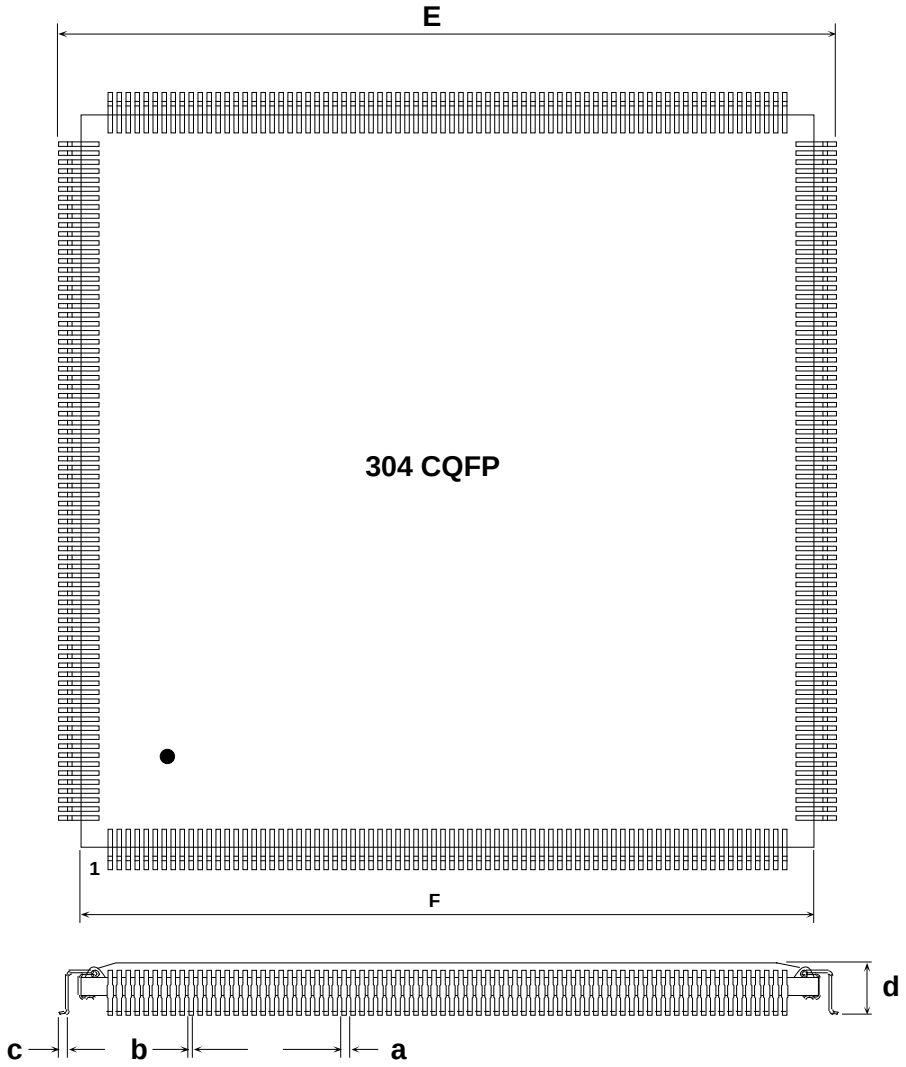


Figure 13-1 Mechanical Diagrams

Table 13-1. 304 pin CQFP Package Dimensions

| Dimension | | mm |
|---|---|---|
| a | Lead Pitch | 0.5 |
| b | Lead Width | 0.23 ± 0.05 |
| c | Foot Length | 0.5 ± 0.1 |
| d | Height | 3.1 max |
| E | Width (toe to toe) | 42.6 ± 0.2 |
| F | Body Width | 40.0 ± 0.2 |

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