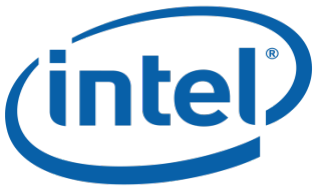

Intel® Xeon® Scalable Processor

Instruction Throughput and Latency

July 2017

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Date: July 2017
Intel® Xeon® Scalable Processor Instruction Throughput and Latency
The table describes throughput and latency for processors with two FMA units.
Memory latencies are assuming Data Cache Unit (DCU) hit

IFORM	Instruction Example	Latency [Cycles]	Throughput [Cycles/Instruction]
XED_IFORM_ADC_MEMb_IMMb_82r2	adc [rdi], 1	8	1
XED_IFORM_ADC_MEMb_IMMb_80r2	adc [rdi], 1	8	1
XED_IFORM_ADC_MEMv_IMMb	adc [rdi], 1	8	1
XED_IFORM_ADC_MEMv_IMMz	adc [rdi], 1	8	1
XED_IFORM_ADC_MEMb_GPR8	adc [rdi], al	8	1
XED_IFORM_ADC_MEMv_GPRv	adc [rdi], rax	8	1
XED_IFORM_ADC_GPR8_MEMb	adc al, [rdi]	6	0.5
XED_IFORM_ADC_GPR8_IMMb_80r2	adc al, 1	2	0.5
XED_IFORM_ADC_GPR8_IMMb_82r2	adc al, 1	2	0.5
XED_IFORM_ADC_AL_IMMb	adc al, 1	2	0.5
XED_IFORM_ADC_GPR8_GPR8_10	adc al, cl	1	0.5
XED_IFORM_ADC_GPR8_GPR8_12	adc al, cl	1	0.5
XED_IFORM_ADC_OrAX_IMMz	adc ax, 1	1	0.5
XED_IFORM_ADC_GPRv_MEMv	adc rax, [rdi]	6	0.5
XED_IFORM_ADC_GPRv_IMMz	adc rax, 1	1	0.5
XED_IFORM_ADC_GPRv_IMMb	adc rax, 1	1	0.5
XED_IFORM_ADC_GPRv_GPRv_13	adc rax, rcx	1	0.5
XED_IFORM_ADC_GPRv_GPRv_11	adc rax, rcx	1	0.5
XED_IFORM_ADCX_GPR32d_MEMd	adcx eax, [rdi]	6	0.5
XED_IFORM_ADCX_GPR32d_GPR32d	adcx eax, ecx	1	0.5
XED_IFORM_ADCX_GPR64q_MEMq	adcx rax, [rdi]	6	0.5
XED_IFORM_ADCX_GPR64q_GPR64q	adcx rax, rcx	1	0.5
XED_IFORM_ADD_MEMb_IMMb_80r0	add [rdi], 1	6	1
XED_IFORM_ADD_MEMv_IMMb	add [rdi], 1	6	1
XED_IFORM_ADD_MEMb_IMMb_82r0	add [rdi], 1	6	1
XED_IFORM_ADD_MEMv_IMMz	add [rdi], 1	6	1
XED_IFORM_ADD_MEMb_GPR8	add [rdi], al	6	1
XED_IFORM_ADD_MEMv_GPRv	add [rdi], rax	6	1
XED_IFORM_ADD_GPR8_MEMb	add al, [rdi]	6	0.5
XED_IFORM_ADD_AL_IMMb	add al, 1	1	0.25
XED_IFORM_ADD_GPR8_IMMb_82r0	add al, 1	1	0.25
XED_IFORM_ADD_GPR8_IMMb_80r0	add al, 1	1	0.25
XED_IFORM_ADD_GPR8_GPR8_02	add al, cl	1	0.25
XED_IFORM_ADD_GPR8_GPR8_00	add al, cl	1	0.25
XED_IFORM_ADD_OrAX_IMMz	add ax, 1	1	0.25
XED_IFORM_ADD_GPRv_MEMv	add rax, [rdi]	6	0.5
XED_IFORM_ADD_GPRv_IMMz	add rax, 1	1	0.25
XED_IFORM_ADD_GPRv_IMMb	add rax, 1	1	0.25
XED_IFORM_ADD_GPRv_GPRv_01	add rax, rcx	1	0.25
XED_IFORM_ADD_GPRv_GPRv_03	add rax, rcx	1	0.25
XED_IFORM_JECXZ_RELBRb	addr32 jecxz 0xd	2	0.5
XED_IFORM_ADOX_GPR32d_MEMd	adox eax, [rdi]	6	0.5
XED_IFORM_ADOX_GPR32d_GPR32d	adox eax, ecx	1	0.5
XED_IFORM_ADOX_GPR64q_MEMq	adox rax, [rdi]	6	0.5
XED_IFORM_ADOX_GPR64q_GPR64q	adox rax, rcx	1	0.5
XED_IFORM_AND_MEMb_IMMb_80r4	and [rdi], 1	6	1
XED_IFORM_AND_MEMv_IMMb	and [rdi], 1	6	1
XED_IFORM_AND_MEMv_IMMz	and [rdi], 1	6	1
XED_IFORM_AND_MEMb_IMMb_82r4	and [rdi], 1	6	1
XED_IFORM_AND_MEMb_GPR8	and [rdi], al	6	1
XED_IFORM_AND_MEMv_GPRv	and [rdi], rax	6	1
XED_IFORM_AND_GPR8_MEMb	and al, [rdi]	6	0.5
XED_IFORM_AND_AL_IMMb	and al, 1	1	0.25
XED_IFORM_AND_GPR8_IMMb_80r4	and al, 1	1	0.25
XED_IFORM_AND_GPR8_IMMb_82r4	and al, 1	1	0.25
XED_IFORM_AND_GPR8_GPR8_20	and al, cl	1	0.25
XED_IFORM_AND_GPR8_GPR8_22	and al, cl	1	0.25
XED_IFORM_AND_OrAX_IMMz	and ax, 1	1	0.25
XED_IFORM_AND_GPRv_MEMv	and rax, [rdi]	6	0.5
XED_IFORM_AND_GPRv_IMMb	and rax, 1	1	0.25
XED_IFORM_AND_GPRv_IMMz	and rax, 1	1	0.25
XED_IFORM_AND_GPRv_GPRv_23	and rax, rcx	1	0.25
XED_IFORM_AND_GPRv_GPRv_21	and rax, rcx	1	0.25
XED_IFORM_ANDN_VGPR32d_VGPR32d_MEMd	andn eax, ecx, [rdi]	6	0.5
XED_IFORM_ANDN_VGPR32d_VGPR32d_VGPR32d	andn eax, ecx, edx	1	0.5
XED_IFORM_ANDN_VGPR64q_VGPR64q_MEMq	andn rax, rcx, [rdi]	6	0.5
XED_IFORM_ANDN_VGPR64q_VGPR64q_VGPR64q	andn rax, rcx, rdx	1	0.5
XED_IFORM_BEXTR_VGPR32d_MEMd_VGPR32d	bextr eax, [rdi], ecx	7	0.5
XED_IFORM_BEXTR_VGPR32d_VGPR32d_VGPR32d	bextr eax, ecx, edx	2	0.5
XED_IFORM_BEXTR_VGPR64q_MEMq_VGPR64q	bextr rax, [rdi], rcx	7	0.5
XED_IFORM_BEXTR_VGPR64q_VGPR64q_VGPR64q	bextr rax, rcx, rdx	2	0.5
XED_IFORM_BLSI_VGPR32d_MEMd	blsi eax, [rdi]	6	0.5
XED_IFORM_BLSI_VGPR32d_VGPR32d	blsi eax, ecx	1	0.5

XED_IFORM_BLSI_VGPR64q_MEMq	blsi rax, [rdi]	6	0.5
XED_IFORM_BLSI_VGPR64q_VGPR64q	blsi rax, rcx	1	0.5
XED_IFORM_BLSMSK_VGPR32d_MEMd	blsmsk eax, [rdi]	6	0.5
XED_IFORM_BLSMSK_VGPR32d_VGPR32d	blsmsk eax, ecx	1	0.5
XED_IFORM_BLSMSK_VGPR64q_MEMq	blsmsk rax, [rdi]	6	0.5
XED_IFORM_BLSMSK_VGPR64q_VGPR64q	blsmsk rax, rcx	1	0.5
XED_IFORM_BLSR_VGPR32d_MEMd	blsr eax, [rdi]	6	0.5
XED_IFORM_BLSR_VGPR32d_VGPR32d	blsr eax, ecx	1	0.5
XED_IFORM_BLSR_VGPR64q_MEMq	blsr rax, [rdi]	6	0.5
XED_IFORM_BLSR_VGPR64q_VGPR64q	blsr rax, rcx	1	0.5
XED_IFORM_BSF_GPRv_MEMv	bsf rax, [rdi]	8	1
XED_IFORM_BSF_GPRv_GPRv	bsf rax, rcx	3	1
XED_IFORM_BSR_GPRv_MEMv	bsr rax, [rdi]	8	1
XED_IFORM_BSR_GPRv_GPRv	bsr rax, rcx	3	1
XED_IFORM_BSWAP_GPRv	bswap rax	2	0.5
XED_IFORM_BT_MEMv_IMMb	bt [rdi], 1	6	0.5
XED_IFORM_BT_GPRv_IMMb	bt rax, 1	1	0.5
XED_IFORM_BT_GPRv_GPRv	bt rax, rcx	1	0.5
XED_IFORM_BTC_MEMv_IMMb	btc [rdi], 1	6	1
XED_IFORM_BTC_GPRv_IMMb	btc rax, 1	1	0.5
XED_IFORM_BTC_GPRv_GPRv	btc rax, rcx	1	0.5
XED_IFORM_BTR_MEMv_IMMb	btr [rdi], 1	6	1
XED_IFORM_BTR_GPRv_IMMb	btr rax, 1	1	0.5
XED_IFORM_BTR_GPRv_GPRv	btr rax, rcx	1	0.5
XED_IFORM_BTS_MEMv_IMMb	bts [rdi], 1	6	1
XED_IFORM_BTS_GPRv_IMMb	bts rax, 1	1	0.5
XED_IFORM_BTS_GPRv_GPRv	bts rax, rcx	1	0.5
XED_IFORM_BZHI_VGPR32d_MEMd_VGPR32d	bzhi eax, [rdi], ecx	6	0.5
XED_IFORM_BZHI_VGPR32d_VGPR32d_VGPR32d	bzhi eax, ecx, edx	1	0.5
XED_IFORM_BZHI_VGPR64q_MEMq_VGPR64q	bzhi rax, [rdi], rcx	6	0.5
XED_IFORM_BZHI_VGPR64q_VGPR64q_VGPR64q	bzhi rax, rcx, rdx	1	0.5
XED_IFORM_CALL_NEAR_MEMv	call [rdi]	7	1
XED_IFORM_CALL_FAR_MEMp2	call [rdi]	7	1
XED_IFORM_CALL_NEAR_RELBRd	call 0xf	7	1
XED_IFORM_CALL_NEAR_RELBRz	call 0xf	7	1
XED_IFORM_CALL_NEAR_GPRv	call rax	7	1
XED_IFORM_CDQ	cdq	1	0.5
XED_IFORM_CDQE	cdqe	1	0.25
XED_IFORM_CLAC	clac	1	0.5
XED_IFORM_CLC	clc	1	0.25
XED_IFORM_CLD	cld	3	1
XED_IFORM_CLFLUSH_MEMmprefetch	clflush [rdi]	2	1
XED_IFORM_CMC	cmc	1	0.25
XED_IFORM_CMOVB_GPRv_MEMv	cmovb rax, [rdi]	6	0.5
XED_IFORM_CMOVB_GPRv_GPRv	cmovb rax, rcx	1	0.5
XED_IFORM_CMOVBE_GPRv_MEMv	cmovbe rax, [rdi]	7	1
XED_IFORM_CMOVBE_GPRv_GPRv	cmovbe rax, rcx	2	1
XED_IFORM_CMOVL_GPRv_MEMv	cmovl rax, [rdi]	6	0.5
XED_IFORM_CMOVL_GPRv_GPRv	cmovl rax, rcx	1	0.5
XED_IFORM_CMOVLE_GPRv_MEMv	cmovle rax, [rdi]	6	0.5
XED_IFORM_CMOVLE_GPRv_GPRv	cmovle rax, rcx	1	0.5
XED_IFORM_CMOVNB_GPRv_MEMv	cmovnb rax, [rdi]	6	0.5
XED_IFORM_CMOVNB_GPRv_GPRv	cmovnb rax, rcx	1	0.5
XED_IFORM_CMOVNBE_GPRv_MEMv	cmovnbe rax, [rdi]	7	1
XED_IFORM_CMOVNBE_GPRv_GPRv	cmovnbe rax, rcx	2	1
XED_IFORM_CMOVNL_GPRv_MEMv	cmovnl rax, [rdi]	6	0.5
XED_IFORM_CMOVNL_GPRv_GPRv	cmovnl rax, rcx	1	0.5
XED_IFORM_CMOVNLE_GPRv_MEMv	cmovnle rax, [rdi]	6	0.5
XED_IFORM_CMOVNLE_GPRv_GPRv	cmovnle rax, rcx	1	0.5
XED_IFORM_CMOVNO_GPRv_MEMv	cmovno rax, [rdi]	6	0.5
XED_IFORM_CMOVNO_GPRv_GPRv	cmovno rax, rcx	1	0.5
XED_IFORM_CMOVNP_GPRv_MEMv	cmovnp rax, [rdi]	6	0.5
XED_IFORM_CMOVNP_GPRv_GPRv	cmovnp rax, rcx	1	0.5
XED_IFORM_CMOVNS_GPRv_MEMv	cmovns rax, [rdi]	6	0.5
XED_IFORM_CMOVNS_GPRv_GPRv	cmovns rax, rcx	1	0.5
XED_IFORM_CMOVNZ_GPRv_MEMv	cmovnz rax, [rdi]	6	0.5
XED_IFORM_CMOVNZ_GPRv_GPRv	cmovnz rax, rcx	1	0.5
XED_IFORM_CMOVO_GPRv_MEMv	cmovo rax, [rdi]	6	0.5
XED_IFORM_CMOVO_GPRv_GPRv	cmovo rax, rcx	1	0.5
XED_IFORM_CMOVP_GPRv_MEMv	cmovp rax, [rdi]	6	0.5
XED_IFORM_CMOVP_GPRv_GPRv	cmovp rax, rcx	1	0.5
XED_IFORM_CMOVS_GPRv_MEMv	cmovs rax, [rdi]	6	0.5
XED_IFORM_CMOVS_GPRv_GPRv	cmovs rax, rcx	1	0.5
XED_IFORM_CMOVZ_GPRv_MEMv	cmovz rax, [rdi]	6	0.5
XED_IFORM_CMOVZ_GPRv_GPRv	cmovz rax, rcx	1	0.5
XED_IFORM_CMP_MEMb_IMMb_80r7	cmp [rdi], 1	6	0.5
XED_IFORM_CMP_MEMv_IMMz	cmp [rdi], 1	6	0.5
XED_IFORM_CMP_MEMb_IMMb_82r7	cmp [rdi], 1	6	0.5
XED_IFORM_CMP_MEMv_IMMb	cmp [rdi], 1	6	0.5

XED_IFORM_CMP_MEMb_GPR8	cmp [rdi], al	6	0.5
XED_IFORM_CMP_MEMv_GPRv	cmp [rdi], rax	6	0.5
XED_IFORM_CMP_GPR8_MEMb	cmp al, [rdi]	6	0.5
XED_IFORM_CMP_AL_IMMb	cmp al, 1	1	0.25
XED_IFORM_CMP_GPR8_IMMb_82r7	cmp al, 1	1	0.25
XED_IFORM_CMP_GPR8_IMMb_80r7	cmp al, 1	1	0.25
XED_IFORM_CMP_GPR8_GPR8_3A	cmp al, cl	1	0.25
XED_IFORM_CMP_GPR8_GPR8_38	cmp al, cl	1	0.25
XED_IFORM_CMP_OrAX_IMMz	cmp ax, 1	1	0.25
XED_IFORM_CMP_GPRv_MEMv	cmp rax, [rdi]	6	0.5
XED_IFORM_CMP_GPRv_IMMz	cmp rax, 1	1	0.25
XED_IFORM_CMP_GPRv_IMMb	cmp rax, 1	1	0.25
XED_IFORM_CMP_GPRv_GPRv_3B	cmp rax, rcx	1	0.25
XED_IFORM_CMP_GPRv_GPRv_39	cmp rax, rcx	1	0.25
XED_IFORM_CMPXCHG_MEMb_GPR8	cmpxchg [rdi], al	8	1
XED_IFORM_CMPXCHG_MEMv_GPRv	cmpxchg [rdi], rax	8	1
XED_IFORM_CMPXCHG_GPR8_GPR8	cmpxchg al, cl	5	1.25
XED_IFORM_CMPXCHG_GPRv_GPRv	cmpxchg rax, rcx	5	1.25
XED_IFORM_CMPXCHG16B_MEMdq	cmpxchg16b [rdi]	23	4
XED_IFORM_CMPXCHG8B_MEMq	cmpxchg8b [rdi]	16	2.75
XED_IFORM_CPUID	cpuid	18	2
XED_IFORM_CQO	cqo	1	0.5
XED_IFORM_CVTPD2PI_MMXq_MEMpd	cvtpd2pi mmx0, [rdi]	11	1
XED_IFORM_CVTPD2PI_MMXq_XMMpd	cvtpd2pi mmx0, xmm1	5	1
XED_IFORM_CVTPI2PD_XMMpd_MEMq	cvtpi2pd xmm1, [rdi]	10	1
XED_IFORM_CVTPI2PD_XMMpd_MMXq	cvtpi2pd xmm1, mmx0	5	1
XED_IFORM_CVTPI2PS_XMMq_MEMq	cvtpi2ps xmm1, [rdi]	9	1
XED_IFORM_CVTPI2PS_XMMq_MMXq	cvtpi2ps xmm1, mmx0	6	2
XED_IFORM_CVTPS2PI_MMXq_MEMq	cvtps2pi mmx0, [rdi]	9	0.5
XED_IFORM_CVTPS2PI_MMXq_XMMq	cvtps2pi mmx0, xmm1	5	1
XED_IFORM_CVTSD2SI_GPR32d_MEMsd	cvtsd2si eax, [rdi]	7	1
XED_IFORM_CVTSD2SI_GPR64q_MEMsd	cvtsd2si rax, [rdi]	7	1
XED_IFORM_CVTSS2SI_GPR32d_MEMss	cvtss2si eax, [rdi]	7	1
XED_IFORM_CVTSS2SI_GPR64q_MEMss	cvtss2si rax, [rdi]	7	1
XED_IFORM_CVTTPD2PI_MMXq_MEMpd	cvttpd2pi mmx0, [rdi]	11	1
XED_IFORM_CVTTPD2PI_MMXq_XMMpd	cvttpd2pi mmx0, xmm1	5	1
XED_IFORM_CVTTPS2PI_MMXq_MEMq	cvttps2pi mmx0, [rdi]	9	0.5
XED_IFORM_CVTTPS2PI_MMXq_XMMq	cvttps2pi mmx0, xmm1	5	1
XED_IFORM_CVTTSD2SI_GPR32d_MEMsd	cvttsd2si eax, [rdi]	11	1
XED_IFORM_CVTTSD2SI_GPR64q_MEMsd	cvttsd2si rax, [rdi]	11	1
XED_IFORM_CVTTSS2SI_GPR32d_MEMss	cvttss2si eax, [rdi]	11	1
XED_IFORM_CVTTSS2SI_GPR64q_MEMss	cvttss2si rax, [rdi]	12	1
XED_IFORM_CWDE	cwde	1	0.25
XED_IFORM_CBW	data16 cbw	1	0.25
XED_IFORM_CWD	data16 cwd	2	0.5
XED_IFORM_INSW	data16 insw	20	1.25
XED_IFORM_PUSHF	data16 pushf	9	1
XED_IFORM_DEC_MEMv	dec [rdi]	6	1
XED_IFORM_DEC_MEMb	dec [rdi]	6	1
XED_IFORM_DEC_GPR8	dec al	1	0.25
XED_IFORM_DEC_GPRv_FFr1	dec rax	1	0.25
XED_IFORM_DEC_GPRv_48	dec rax	1	0.25
XED_IFORM_DIV_GPRv	div rax	76	8
XED_IFORM_ENTER_IMMw_IMMb	enter 1, 1	11	1.5
XED_IFORM_F2XM1_ST0	f2xm1 st0	23	3
XED_IFORM_FABS_ST0	fabs st0	1	1
XED_IFORM_FADD_ST0_MEMmem32real	fadd st0, [rdi]	10	1
XED_IFORM_FADD_ST0_MEMm64real	fadd st0, [rdi]	10	1
XED_IFORM_FADDP_X87_ST0	faddp st1, st0	3	1
XED_IFORM_FADD_X87_ST0	faddp st1, st0	3	1
XED_IFORM_FADD_ST0_X87	faddp st1, st0	3	1
XED_IFORM_FBSTP_MEMmem80dec_ST0	fbstp ptr [rdi], st0	5	1
XED_IFORM_FCHS_ST0	fchs st0	1	1
XED_IFORM_FCOM_ST0_MEMmem32real	fcom st0, [rdi]	8	1
XED_IFORM_FCOM_ST0_MEMm64real	fcom st0, [rdi]	8	1
XED_IFORM_FCOM_ST0_X87_DCD0	fcom st0, st1	1	1
XED_IFORM_FCOM_ST0_X87	fcom st0, st1	1	1
XED_IFORM_FCOMP_ST0_MEMmem32real	fcomp st0, [rdi]	8	1
XED_IFORM_FCOMP_ST0_MEMm64real	fcomp st0, [rdi]	8	1
XED_IFORM_FCOMP_ST0_X87_DCD1	fcomp st0, st1	1	1
XED_IFORM_FCOMP_ST0_X87_DED0	fcomp st0, st1	1	1
XED_IFORM_FCOMP_ST0_X87	fcomp st0, st1	1	1
XED_IFORM_FCOMPP_ST0_ST1	fcompp st0, st1	2	1
XED_IFORM_FCOS_ST0	fcos st0		7
XED_IFORM_FDECSTP	fdecstp	2	1
XED_IFORM_FDIV_ST0_MEMmem32real	fdiv st0, [rdi]	22	1
XED_IFORM_FDIV_ST0_MEMm64real	fdiv st0, [rdi]	22	1
XED_IFORM_FDIV_ST0_X87	fdivp st1, st0		1
XED_IFORM_FDIVR_ST0_MEMmem32real	fdivr st0, [rdi]	27	1

XED_IFORM_FDIVR_ST0_MEMm64real	fdivr st0, [rdi]	27	1
XED_IFORM_FDIVR_ST0_X87	fdivrp st1, st0	15	1
XED_IFORM_FDIVRP_X87_ST0	fdivrp st1, st0	15	1
XED_IFORM_FDIVR_X87_ST0	fdivrp st1, st0	15	1
XED_IFORM_FIADD_ST0_MEMmem32int	fiadd st0, [rdi]	13	2
XED_IFORM_FIADD_ST0_MEMmem16int	fiadd st0, [rdi]	13	2
XED_IFORM_FICOM_ST0_MEMmem16int	ficom st0, [rdi]	11	2
XED_IFORM_FICOM_ST0_MEMmem32int	ficom st0, [rdi]	11	2
XED_IFORM_FICOMP_ST0_MEMmem16int	ficomp st0, [rdi]	11	2
XED_IFORM_FICOMP_ST0_MEMmem32int	ficomp st0, [rdi]	11	2
XED_IFORM_FIDIV_ST0_MEMmem32int	fidiv st0, [rdi]	25	1
XED_IFORM_FIDIV_ST0_MEMmem16int	fidiv st0, [rdi]	25	1
XED_IFORM_FIDIVR_ST0_MEMmem32int	fidivr st0, [rdi]	30	1
XED_IFORM_FIDIVR_ST0_MEMmem16int	fidivr st0, [rdi]	30	1
XED_IFORM_FILD_ST0_MEMm64int	fild st0, [rdi]	10	1
XED_IFORM_FILD_ST0_MEMmem16int	fild st0, [rdi]	10	1
XED_IFORM_FILD_ST0_MEMmem32int	fild st0, [rdi]	10	1
XED_IFORM_FIMUL_ST0_MEMmem32int	fimul st0, [rdi]	14	1
XED_IFORM_FIMUL_ST0_MEMmem16int	fimul st0, [rdi]	14	1
XED_IFORM_FINCSTP	fincstp	1	0.5
XED_IFORM_FIST_MEMmem32int_ST0	fist [rdi], st0	8	1
XED_IFORM_FIST_MEMmem16int_ST0	fist [rdi], st0	8	1
XED_IFORM_FISTP_MEMmem32int_ST0	fistp [rdi], st0	8	1
XED_IFORM_FISTP_MEMm64int_ST0	fistp [rdi], st0	8	1
XED_IFORM_FISTP_MEMmem16int_ST0	fistp [rdi], st0	8	1
XED_IFORM_FISTTP_MEMmem16int_ST0	fisttp [rdi], st0	8	1
XED_IFORM_FISTTP_MEMm64int_ST0	fisttp [rdi], st0	8	1
XED_IFORM_FISTTP_MEMmem32int_ST0	fisttp [rdi], st0	8	1
XED_IFORM_FISUB_ST0_MEMmem32int	fisub st0, [rdi]	13	2
XED_IFORM_FISUB_ST0_MEMmem16int	fisub st0, [rdi]	13	2
XED_IFORM_FISUBR_ST0_MEMmem16int	fisubr st0, [rdi]	13	2
XED_IFORM_FISUBR_ST0_MEMmem32int	fisubr st0, [rdi]	13	2
XED_IFORM_FLD_ST0_MEMmem80real	fld st0, [rdi]	7	0.5
XED_IFORM_FLD_ST0_MEMm64real	fld st0, [rdi]	7	0.5
XED_IFORM_FLD_ST0_MEMmem32real	fld st0, [rdi]	7	0.5
XED_IFORM_FLD1_ST0	fld1 st0	2	1
XED_IFORM_FLDCW_MEMmem16	fldcw [rdi]	7	1
XED_IFORM_FLDENV_MEMmem28	fldenv ptr [rdi]	62	14
XED_IFORM_FLDENV_MEMmem14	fldenv ptr [rdi]	62	14
XED_IFORM_FLDL2E_ST0	fldl2e st0	4	1
XED_IFORM_FLDL2T_ST0	fldl2t st0	4	1
XED_IFORM_FLDLG2_ST0	fldlg2 st0	4	1
XED_IFORM_FLDLN2_ST0	fldln2 st0	4	1
XED_IFORM_FLDPI_ST0	fldpi st0	4	1
XED_IFORM_FLDZ_ST0	fldz st0	1	0.5
XED_IFORM_FMUL_ST0_MEMmem32real	fmul st0, [rdi]	11	1
XED_IFORM_FMUL_ST0_MEMm64real	fmul st0, [rdi]	11	1
XED_IFORM_FMULP_X87_ST0	fmulp st1, st0	4	1
XED_IFORM_FMUL_ST0_X87	fmulp st1, st0	4	1
XED_IFORM_FMUL_X87_ST0	fmulp st1, st0	4	1
XED_IFORM_FNCLEX	fnclex	4	1
XED_IFORM_FNINIT	fninit	75	6
XED_IFORM_FNOP	fnop	1	0.5
XED_IFORM_FNSTCW_MEMmem16	fnstcw [rdi]	6	1
XED_IFORM_FNSTENV_MEMmem28	fnstenv ptr [rdi]	110	19.5
XED_IFORM_FNSTENV_MEMmem14	fnstenv ptr [rdi]	110	19.5
XED_IFORM_FNSTSW_MEMmem16	fnstsw [rdi]	7	1
XED_IFORM_FNSTSW_AX	fnstsw ax	3	1
XED_IFORM_FPATAN_ST0_ST1	fpatan st0, st1	1	26
XED_IFORM_FPREM_ST0_ST1	fprem st0, st1	59	2
XED_IFORM_FPREM1_ST0_ST1	fprem1 st0, st1	56	1
XED_IFORM_FPTAN_ST0_ST1	fptan st0, st1	124	4
XED_IFORM_FRNDINT_ST0	frndint st0	29	6.5
XED_IFORM_FSCALE_ST0_ST1	fscale st0, st1	26	2
XED_IFORM_FSIN_ST0	fsin st0	32	8
XED_IFORM_FSINCOS_ST0_ST1	fsincos st0, st1	104	3
XED_IFORM_FSTP_MEMmem32real_ST0	fstp [rdi], st0	5	1
XED_IFORM_FSTP_MEMmem80real_ST0	fstp [rdi], st0	5	1
XED_IFORM_FSTP_MEMm64real_ST0	fstp [rdi], st0	5	1
XED_IFORM_FSUB_ST0_MEMmem32real	fsub st0, [rdi]	10	1
XED_IFORM_FSUB_ST0_MEMm64real	fsub st0, [rdi]	10	1
XED_IFORM_FSUB_ST0_X87	fsubp st1, st0	3	1
XED_IFORM_FSUBP_X87_ST0	fsubp st1, st0	3	1
XED_IFORM_FSUB_X87_ST0	fsubp st1, st0	3	1
XED_IFORM_FSUBR_ST0_MEMm64real	fsubr st0, [rdi]	10	1
XED_IFORM_FSUBR_ST0_MEMmem32real	fsubr st0, [rdi]	10	1
XED_IFORM_FSUBR_X87_ST0	fsubrp st1, st0	3	1
XED_IFORM_FSUBRP_X87_ST0	fsubrp st1, st0	3	1
XED_IFORM_FSUBR_ST0_X87	fsubrp st1, st0	3	1

XED_IFORM_FTST_ST0	ftst st0	1	1
XED_IFORM_FUCOM_ST0_X87	fucom st0, st1	1	1
XED_IFORM_FUCOMP_ST0_X87	fucomp st0, st1	1	1
XED_IFORM_FUCOMPP_ST0_ST1	fucompp st0, st1	2	1
XED_IFORM_FWAIT	fwait	2	0.5
XED_IFORM_FXAM_ST0	fxam st0	6	2
XED_IFORM_FXCH_ST0_X87_DDC1	fxch st0, st1	17	4
XED_IFORM_FXCH_ST0_X87	fxch st0, st1	17	4
XED_IFORM_FXCH_ST0_X87_DFC1	fxch st0, st1	17	4
XED_IFORM_FXRSTOR_MEMmfpxenv	fxrstor ptr [rdi]	63	14.25
XED_IFORM_FXRSTOR64_MEMmfpxenv	fxrstor64 ptr [rdi]	63	14.25
XED_IFORM_FXTRACT_ST0_ST1	fxtract st0, st1	34	2
XED_IFORM_FYL2X_ST0_ST1	fyl2x st0, st1	17	3.5
XED_IFORM_IDIV_MEMv	idiv [rdi]	28	4
XED_IFORM_IDIV_MEMb	idiv [rdi]	28	4
XED_IFORM_IDIV_GPRv	idiv rax	102	16.5
XED_IFORM_IMUL_MEMb	imul [rdi]	8	1
XED_IFORM_IMUL_MEMv	imul [rdi]	8	1
XED_IFORM_IMUL_GPR8	imul al	3	1
XED_IFORM_IMUL_GPRv	imul rax	4	1
XED_IFORM_IMUL_GPRv_MEMv	imul rax, [rdi]	8	1
XED_IFORM_IMUL_GPRv_MEMv_IMMb	imul rax, [rdi], 1	8	1
XED_IFORM_IMUL_GPRv_MEMv_IMMz	imul rax, [rdi], 1	8	1
XED_IFORM_IMUL_GPRv_GPRv	imul rax, rcx	3	1
XED_IFORM_IMUL_GPRv_GPRv_IMMz	imul rax, rcx, 1	3	1
XED_IFORM_IMUL_GPRv_GPRv_IMMb	imul rax, rcx, 1	3	1
XED_IFORM_INC_MEMb	inc [rdi]	6	1
XED_IFORM_INC_MEMv	inc [rdi]	6	1
XED_IFORM_INC_GPR8	inc al	1	0.25
XED_IFORM_INC_GPRv_FFr0	inc rax	1	0.25
XED_IFORM_INC_GPRv_40	inc rax	1	0.25
XED_IFORM_INSB	insb	20	1.25
XED_IFORM_INSD	insd	20	1.25
XED_IFORM_JB_RELBRb	jb 0xc	1	0.5
XED_IFORM_JB_RELBRd	jb 0xc	1	0.5
XED_IFORM_JB_RELBRz	jb 0xc	1	0.5
XED_IFORM_JBE_RELBRd	jbe 0xc	1	0.5
XED_IFORM_JBE_RELBRb	jbe 0xc	1	0.5
XED_IFORM_JBE_RELBRz	jbe 0xc	1	0.5
XED_IFORM_JL_RELBRz	jl 0xc	1	0.5
XED_IFORM_JL_RELBRb	jl 0xc	1	0.5
XED_IFORM_JL_RELBRd	jl 0xc	1	0.5
XED_IFORM_JLE_RELBRz	jle 0xc	1	0.5
XED_IFORM_JLE_RELBRb	jle 0xc	1	0.5
XED_IFORM_JLE_RELBRd	jle 0xc	1	0.5
XED_IFORM_JMP_MEMv	jmp [rdi]	6	1
XED_IFORM_JMP_FAR_MEMp2	jmp [rdi]	6	1
XED_IFORM_JMP_RELBRz	jmp 0xc	1	0.5
XED_IFORM_JMP_RELBRb	jmp 0xc	1	0.5
XED_IFORM_JMP_RELBRd	jmp 0xc	1	0.5
XED_IFORM_JMP_GPRv	jmp rax	1	1
XED_IFORM_JNB_RELBRz	jnb 0xc	1	0.5
XED_IFORM_JNB_RELBRd	jnb 0xc	1	0.5
XED_IFORM_JNB_RELBRb	jnb 0xc	1	0.5
XED_IFORM_JNBE_RELBRd	jnbe 0xc	1	0.5
XED_IFORM_JNBE_RELBRz	jnbe 0xc	1	0.5
XED_IFORM_JNBE_RELBRb	jnbe 0xc	1	0.5
XED_IFORM_JNL_RELBRz	jnl 0xc	1	0.5
XED_IFORM_JNL_RELBRb	jnl 0xc	1	0.5
XED_IFORM_JNL_RELBRd	jnl 0xc	1	0.5
XED_IFORM_JNLE_RELBRz	jnle 0xc	1	0.5
XED_IFORM_JNLE_RELBRd	jnle 0xc	1	0.5
XED_IFORM_JNLE_RELBRb	jnle 0xc	1	0.5
XED_IFORM_JNO_RELBRd	jno 0xc	1	0.5
XED_IFORM_JNO_RELBRb	jno 0xc	1	0.5
XED_IFORM_JNO_RELBRz	jno 0xc	1	0.5
XED_IFORM_JNP_RELBRd	jnp 0xc	1	0.5
XED_IFORM_JNP_RELBRz	jnp 0xc	1	0.5
XED_IFORM_JNP_RELBRb	jnp 0xc	1	0.5
XED_IFORM_JNS_RELBRd	jns 0xc	1	0.5
XED_IFORM_JNS_RELBRz	jns 0xc	1	0.5
XED_IFORM_JNS_RELBRb	jns 0xc	1	0.5
XED_IFORM_JNZ_RELBRb	jnz 0xc	1	0.5
XED_IFORM_JNZ_RELBRz	jnz 0xc	1	0.5
XED_IFORM_JNZ_RELBRd	jnz 0xc	1	0.5
XED_IFORM_JO_RELBRd	jo 0xc	1	0.5
XED_IFORM_JO_RELBRb	jo 0xc	1	0.5
XED_IFORM_JO_RELBRz	jo 0xc	1	0.5
XED_IFORM_JP_RELBRb	jp 0xc	1	0.5

XED_IFORM_JP_RELBRz	jp 0xc	1	0.5
XED_IFORM_JP_RELBRd	jp 0xc	1	0.5
XED_IFORM_JRCXZ_RELBRb	jrcxz 0xc	2	0.5
XED_IFORM_JS_RELBRd	js 0xc	1	0.5
XED_IFORM_JS_RELBRz	js 0xc	1	0.5
XED_IFORM_JS_RELBRb	js 0xc	1	0.5
XED_IFORM_JZ_RELBRd	jz 0xc	1	0.5
XED_IFORM_JZ_RELBRz	jz 0xc	1	0.5
XED_IFORM_JZ_RELBRb	jz 0xc	1	0.5
XED_IFORM_KADDB_MASKmskw_MASKmskw_MASKmskw_AVX512	kaddb k1, k1, k1	3	1
XED_IFORM_KADDD_MASKmskw_MASKmskw_MASKmskw_AVX512	kaddd k1, k1, k1	3	1
XED_IFORM_KADDQ_MASKmskw_MASKmskw_MASKmskw_AVX512	kaddq k1, k1, k1	3	1
XED_IFORM_KADDW_MASKmskw_MASKmskw_MASKmskw_AVX512	kaddw k1, k1, k1	3	1
XED_IFORM_KANDB_MASKmskw_MASKmskw_MASKmskw_AVX512	kandb k1, k1, k1	1	1
XED_IFORM_KANDD_MASKmskw_MASKmskw_MASKmskw_AVX512	kandd k1, k1, k1	1	1
XED_IFORM_KANDNB_MASKmskw_MASKmskw_MASKmskw_AVX512	kandnb k1, k1, k1	1	1
XED_IFORM_KANDND_MASKmskw_MASKmskw_MASKmskw_AVX512	kandnd k1, k1, k1	1	1
XED_IFORM_KANDNQ_MASKmskw_MASKmskw_MASKmskw_AVX512	kandnq k1, k1, k1	1	1
XED_IFORM_KANDNW_MASKmskw_MASKmskw_MASKmskw_AVX512	kandnw k1, k1, k1	1	1
XED_IFORM_KANDQ_MASKmskw_MASKmskw_MASKmskw_AVX512	kandq k1, k1, k1	1	1
XED_IFORM_KANDW_MASKmskw_MASKmskw_MASKmskw_AVX512	kandw k1, k1, k1	1	1
XED_IFORM_KMOVB_MEMu8_MASKmskw_AVX512	kmovb [rdi], k1	5	1
XED_IFORM_KMOVB_GPR32u32_MASKmskw_AVX512	kmovb eax, k1	3	1
XED_IFORM_KMOVB_MASKmskw_MEMu8_AVX512	kmovb k1, [rdi]	7	1
XED_IFORM_KMOVB_MASKmskw_GPR32u32_AVX512	kmovb k1, eax	1	1
XED_IFORM_KMOVB_MASKmskw_MASKu8_AVX512	kmovb k1, k1	1	1
XED_IFORM_KMOVD_MEMu32_MASKmskw_AVX512	kmovd [rdi], k1	5	1
XED_IFORM_KMOVD_GPR32u32_MASKmskw_AVX512	kmovd eax, k1	3	1
XED_IFORM_KMOVD_MASKmskw_MEMu32_AVX512	kmovd k1, [rdi]	7	1
XED_IFORM_KMOVD_MASKmskw_GPR32u32_AVX512	kmovd k1, eax	1	1
XED_IFORM_KMOVD_MASKmskw_MASKu32_AVX512	kmovd k1, k1	1	1
XED_IFORM_KMOVQ_MEMu64_MASKmskw_AVX512	kmovq [rdi], k1	5	1
XED_IFORM_KMOVQ_MASKmskw_MEMu64_AVX512	kmovq k1, [rdi]	7	1
XED_IFORM_KMOVQ_MASKmskw_MASKu64_AVX512	kmovq k1, k1	1	1
XED_IFORM_KMOVQ_MASKmskw_GPR64u64_AVX512	kmovq k1, rax	1	1
XED_IFORM_KMOVQ_GPR64u64_MASKmskw_AVX512	kmovq rax, k1	3	1
XED_IFORM_KMOVW_MEMu16_MASKmskw_AVX512	kmovw [rdi], k1	5	1
XED_IFORM_KMOVW_GPR32u32_MASKmskw_AVX512	kmovw eax, k1	3	1
XED_IFORM_KMOVW_MASKmskw_MEMu16_AVX512	kmovw k1, [rdi]	7	1
XED_IFORM_KMOVW_MASKmskw_GPR32u32_AVX512	kmovw k1, eax	1	1
XED_IFORM_KMOVW_MASKmskw_MASKu16_AVX512	kmovw k1, k1	1	1
XED_IFORM_KNOTB_MASKmskw_MASKmskw_AVX512	knotb k1, k1	1	1
XED_IFORM_KNOTD_MASKmskw_MASKmskw_AVX512	knotd k1, k1	1	1
XED_IFORM_KNOTQ_MASKmskw_MASKmskw_AVX512	knotq k1, k1	1	1
XED_IFORM_KNOTW_MASKmskw_MASKmskw_AVX512	knotw k1, k1	1	1
XED_IFORM_KORB_MASKmskw_MASKmskw_MASKmskw_AVX512	korb k1, k1, k1	1	1
XED_IFORM_KORD_MASKmskw_MASKmskw_MASKmskw_AVX512	kord k1, k1, k1	1	1
XED_IFORM_KORQ_MASKmskw_MASKmskw_MASKmskw_AVX512	korq k1, k1, k1	1	1
XED_IFORM_KORTESTB_MASKmskw_MASKmskw_AVX512	kortestb k1, k1	3	1
XED_IFORM_KORTESTD_MASKmskw_MASKmskw_AVX512	kortestd k1, k1	3	1
XED_IFORM_KORTESTQ_MASKmskw_MASKmskw_AVX512	kortestq k1, k1	3	1
XED_IFORM_KORTESTW_MASKmskw_MASKmskw_AVX512	kortestw k1, k1	3	1
XED_IFORM_KORW_MASKmskw_MASKmskw_MASKmskw_AVX512	korw k1, k1, k1	1	1
XED_IFORM_KSHIFTLB_MASKmskw_MASKmskw_IMM8_AVX512	kshiftlb k1, k1, 1	3	1
XED_IFORM_KSHIFTLD_MASKmskw_MASKmskw_IMM8_AVX512	kshiftld k1, k1, 1	3	1
XED_IFORM_KSHIFTLQ_MASKmskw_MASKmskw_IMM8_AVX512	kshiftlq k1, k1, 1	3	1
XED_IFORM_KSHIFTLW_MASKmskw_MASKmskw_IMM8_AVX512	kshiftlw k1, k1, 1	3	1
XED_IFORM_KSHIFTRB_MASKmskw_MASKmskw_IMM8_AVX512	kshiftrb k1, k1, 1	3	1
XED_IFORM_KSHIFTRD_MASKmskw_MASKmskw_IMM8_AVX512	kshiftrd k1, k1, 1	3	1
XED_IFORM_KSHIFTRQ_MASKmskw_MASKmskw_IMM8_AVX512	kshiftrq k1, k1, 1	3	1
XED_IFORM_KSHIFTRW_MASKmskw_MASKmskw_IMM8_AVX512	kshiftrw k1, k1, 1	3	1
XED_IFORM_KTESTB_MASKmskw_MASKmskw_AVX512	ktestb k1, k1	3	1
XED_IFORM_KTESTD_MASKmskw_MASKmskw_AVX512	ktestd k1, k1	3	1
XED_IFORM_KTESTQ_MASKmskw_MASKmskw_AVX512	ktestq k1, k1	3	1
XED_IFORM_KTESTW_MASKmskw_MASKmskw_AVX512	ktestw k1, k1	3	1
XED_IFORM_KUNPCKBW_MASKmskw_MASKmskw_MASKmskw_AVX512	kunpckbw k1, k1, k1	3	1
XED_IFORM_KUNPCKDQ_MASKmskw_MASKmskw_MASKmskw_AVX512	kunpckdq k1, k1, k1	3	1
XED_IFORM_KUNPCKWD_MASKmskw_MASKmskw_MASKmskw_AVX512	kunpckwd k1, k1, k1	3	1
XED_IFORM_KXNORB_MASKmskw_MASKmskw_MASKmskw_AVX512	kxnorb k1, k1, k1	1	1
XED_IFORM_KXNORD_MASKmskw_MASKmskw_MASKmskw_AVX512	kxnord k1, k1, k1	1	1
XED_IFORM_KXNORQ_MASKmskw_MASKmskw_MASKmskw_AVX512	kxnorq k1, k1, k1	1	1
XED_IFORM_KXNORW_MASKmskw_MASKmskw_MASKmskw_AVX512	kxnorw k1, k1, k1	1	1
XED_IFORM_KXORB_MASKmskw_MASKmskw_MASKmskw_AVX512	kxorb k1, k1, k1	1	1
XED_IFORM_KXORD_MASKmskw_MASKmskw_MASKmskw_AVX512	kxord k1, k1, k1	1	1
XED_IFORM_KXORQ_MASKmskw_MASKmskw_MASKmskw_AVX512	kxorq k1, k1, k1	1	1
XED_IFORM_KXORW_MASKmskw_MASKmskw_MASKmskw_AVX512	kxorw k1, k1, k1	1	1
XED_IFORM_LAHF	lahf	1	0.25
XED_IFORM_LAR_GPRv_MEMw	lar rax, [rdi]	9	2
XED_IFORM_LAR_GPRv_GPRv	lar rax, rcx	4	1

XED_IFORM_LEA_GPRv_AGEN	lea rax, ptr [rdi]	1	0.5
XED_IFORM_LEAVE	leave	7	0.5
XED_IFORM_LFENCE	lfence	2	0.5
XED_IFORM_ADC_LOCK_MEMb_GPR8	lock : adc [rdi], al	12	2
XED_IFORM_ADC_LOCK_MEMv_GPRv	lock adc [rdi], rax	12	2
XED_IFORM_ADD_LOCK_MEMb_IMMb_82r0	lock add [rdi], 1	10	1.25
XED_IFORM_ADD_LOCK_MEMv_IMMb	lock add [rdi], 1	10	1.25
XED_IFORM_ADD_LOCK_MEMv_IMMz	lock add [rdi], 1	10	1.25
XED_IFORM_ADD_LOCK_MEMb_IMMb_80r0	lock add [rdi], 1	10	1.25
XED_IFORM_ADD_LOCK_MEMb_GPR8	lock add [rdi], al	10	1.25
XED_IFORM_ADD_LOCK_MEMv_GPRv	lock add [rdi], rax	10	1.25
XED_IFORM_AND_LOCK_MEMv_IMMb	lock and [rdi], 1	10	1.25
XED_IFORM_AND_LOCK_MEMb_IMMb_80r4	lock and [rdi], 1	10	1.25
XED_IFORM_AND_LOCK_MEMb_IMMb_82r4	lock and [rdi], 1	10	1.25
XED_IFORM_AND_LOCK_MEMv_IMMz	lock and [rdi], 1	10	1.25
XED_IFORM_AND_LOCK_MEMb_GPR8	lock and [rdi], al	10	1.25
XED_IFORM_AND_LOCK_MEMv_GPRv	lock and [rdi], rax	10	1.25
XED_IFORM_BTC_LOCK_MEMv_IMMb	lock btc [rdi], 1	10	1.5
XED_IFORM_BTR_LOCK_MEMv_IMMb	lock btr [rdi], 1	10	1.5
XED_IFORM_BTS_LOCK_MEMv_IMMb	lock bts [rdi], 1	10	1.5
XED_IFORM_CMPXCHG_LOCK_MEMb_GPR8	lock cmpxchg [rdi], al	12	2
XED_IFORM_CMPXCHG_LOCK_MEMv_GPRv	lock cmpxchg [rdi], rax	12	2
XED_IFORM_CMPXCHG16B_LOCK_MEMdq	lock cmpxchg16b [rdi]	23	4
XED_IFORM_CMPXCHG8B_LOCK_MEMq	lock cmpxchg8b [rdi]	20	3.75
XED_IFORM_DEC_LOCK_MEMv	lock dec [rdi]	10	1.25
XED_IFORM_DEC_LOCK_MEMb	lock dec [rdi]	10	1.25
XED_IFORM_INC_LOCK_MEMv	lock inc [rdi]	10	1.25
XED_IFORM_INC_LOCK_MEMb	lock inc [rdi]	10	1.25
XED_IFORM_NEG_LOCK_MEMb	lock neg [rdi]	10	1.25
XED_IFORM_NEG_LOCK_MEMv	lock neg [rdi]	10	1.25
XED_IFORM_NOT_LOCK_MEMv	lock not [rdi]	10	1.25
XED_IFORM_NOT_LOCK_MEMb	lock not [rdi]	10	1.25
XED_IFORM_OR_LOCK_MEMb_IMMb_82r1	lock or [rdi], 1	10	1.25
XED_IFORM_OR_LOCK_MEMv_IMMz	lock or [rdi], 1	10	1.25
XED_IFORM_OR_LOCK_MEMv_IMMb	lock or [rdi], 1	10	1.25
XED_IFORM_OR_LOCK_MEMb_IMMb_80r1	lock or [rdi], 1	10	1.25
XED_IFORM_OR_LOCK_MEMb_GPR8	lock or [rdi], al	10	1.25
XED_IFORM_OR_LOCK_MEMv_GPRv	lock or [rdi], rax	10	1.25
XED_IFORM_SBB_LOCK_MEMb_GPR8	lock sbb [rdi], al	12	2
XED_IFORM_SBB_LOCK_MEMv_GPRv	lock sbb [rdi], rax	12	2
XED_IFORM_SUB_LOCK_MEMb_IMMb_82r5	lock sub [rdi], 1	10	1.25
XED_IFORM_SUB_LOCK_MEMv_IMMb	lock sub [rdi], 1	10	1.25
XED_IFORM_SUB_LOCK_MEMv_IMMz	lock sub [rdi], 1	10	1.25
XED_IFORM_SUB_LOCK_MEMb_IMMb_80r5	lock sub [rdi], 1	10	1.25
XED_IFORM_SUB_LOCK_MEMb_GPR8	lock sub [rdi], al	10	1.25
XED_IFORM_SUB_LOCK_MEMv_GPRv	lock sub [rdi], rax	10	1.25
XED_IFORM_XADD_LOCK_MEMb_GPR8	lock xadd [rdi], al	11	1.5
XED_IFORM_XADD_LOCK_MEMv_GPRv	lock xadd [rdi], rax	11	1.5
XED_IFORM_XOR_LOCK_MEMv_IMMb	lock xor [rdi], 1	10	1.25
XED_IFORM_XOR_LOCK_MEMb_IMMb_80r6	lock xor [rdi], 1	10	1.25
XED_IFORM_XOR_LOCK_MEMv_IMMz	lock xor [rdi], 1	10	1.25
XED_IFORM_XOR_LOCK_MEMb_IMMb_82r6	lock xor [rdi], 1	10	1.25
XED_IFORM_XOR_LOCK_MEMb_GPR8	lock xor [rdi], al	10	1.25
XED_IFORM_XOR_LOCK_MEMv_GPRv	lock xor [rdi], rax	10	1.25
XED_IFORM_LOOP_RELBRb	loop 0xc	7	2
XED_IFORM_LOOPE_RELBRb	loope 0xc	11	2.75
XED_IFORM_LOOPNE_RELBRb	loopne 0xc	11	2.75
XED_IFORM_LSL_GPRv_MEMw	lsl rax, [rdi]	9	2
XED_IFORM_LZCNT_GPRv_MEMv	lzcnt rax, [rdi]	8	1
XED_IFORM_LZCNT_GPRv_GPRv	lzcnt rax, rcx	3	1
XED_IFORM_MASKMOVQ_MMXq_MMXq	maskmovq mmx0, mmx0	1	1
XED_IFORM_MOV_MEMb_IMMb	mov [rdi], 1	5	1
XED_IFORM_MOV_MEMv_IMMz	mov [rdi], 1	5	1
XED_IFORM_MOV_MEMb_AL	mov [rdi], al	5	1
XED_IFORM_MOV_MEMb_GPR8	mov [rdi], al	5	1
XED_IFORM_MOV_MEMv_OrAX	mov [rdi], ax	5	1
XED_IFORM_MOV_MEMv_GPRv	mov [rdi], rax	5	1
XED_IFORM_MOV_AL_MEMb	mov al, [rdi]	5	0.5
XED_IFORM_MOV_GPR8_MEMb	mov al, [rdi]	5	0.5
XED_IFORM_MOV_GPR8_IMMb_C6r0	mov al, 1	1	0.25
XED_IFORM_MOV_GPR8_IMMb_D0	mov al, 1	1	0.25
XED_IFORM_MOV_GPR8_GPR8_8A	mov al, cl	1	0.25
XED_IFORM_MOV_GPR8_GPR8_88	mov al, cl	1	0.25
XED_IFORM_MOV_OrAX_MEMv	mov ax, [rdi]	5	0.5
XED_IFORM_MOV_GPRv_MEMv	mov rax, [rdi]	5	0.5
XED_IFORM_MOV_GPRv_IMMz	mov rax, 1	1	0.25
XED_IFORM_MOV_GPRv_IMMv	mov rax, 1	1	0.25
XED_IFORM_MOV_GPRv_GPRv_8B	mov rax, rcx	0	0.25
XED_IFORM_MOV_GPRv_GPRv_89	mov rax, rcx	0	0.25

XED_IFORM_MOVBE_MEMv_GPRv	movbe [rdi], rax	6	1
XED_IFORM_MOVBE_GPRv_MEMv	movbe rax, [rdi]	6	0.5
XED_IFORM_MOVD_MEMd_MMXd	movd [rdi], mmx0	5	1
XED_IFORM_MOVD_GPR32_MMXd	movd eax, mmx0	2	1
XED_IFORM_MOVD_MMXq_MEMd	movd mmx0, [rdi]	5	0.5
XED_IFORM_MOVD_MMXq_GPR32	movd mmx0, eax	1	1
XED_IFORM_MOVDQ2Q_MMXq_XMMq	movdq2q mmx0, xmm1	2	1
XED_IFORM_MOVNTI_MEMd_GPR32	movnti [rdi], eax	5	1
XED_IFORM_MOVNTI_MEMq_GPR64	movnti [rdi], rax	5	1
XED_IFORM_MOVNTQ_MEMq_MMXq	movntq [rdi], mmx0	5	1
XED_IFORM_MOVQ_MEMq_MMXq_0F7F	movq [rdi], mmx0	5	1
XED_IFORM_MOVQ_MEMq_MMXq_0F7E	movq [rdi], mmx0	5	1
XED_IFORM_MOVQ_MMXq_MEMq_0F6E	movq mmx0, [rdi]	5	0.5
XED_IFORM_MOVQ_MMXq_MEMq_0F6F	movq mmx0, [rdi]	5	0.5
XED_IFORM_MOVQ_MMXq_MMXq_0F6F	movq mmx0, mmx0	1	0.5
XED_IFORM_MOVQ_MMXq_MMXq_0F7F	movq mmx0, mmx0	1	0.5
XED_IFORM_MOVQ_MMXq_GPR64	movq mmx0, rax	1	1
XED_IFORM_MOVQ_GPR64_MMXq	movq rax, mmx0	2	1
XED_IFORM_MOVQ2DQ_XMMdq_MMXq	movq2dq xmm1, mmx0	2	2
XED_IFORM_MOVSX_GPRv_MEMb	movsx rax, [rdi]	5	0.5
XED_IFORM_MOVSX_GPRv_MEMw	movsx rax, [rdi]	5	0.5
XED_IFORM_MOVSX_GPRv_GPR8	movsx rax, al	1	0.25
XED_IFORM_MOVSX_GPRv_GPR16	movsx rax, ax	1	0.25
XED_IFORM_MOVSXD_GPRv_MEMd	movsxd rax, [rdi]	5	0.5
XED_IFORM_MOVSXD_GPRv_GPR32	movsxd rax, eax	1	0.25
XED_IFORM_MOVZX_GPRv_MEMb	movzx rax, [rdi]	5	0.5
XED_IFORM_MOVZX_GPRv_MEMw	movzx rax, [rdi]	5	0.5
XED_IFORM_MOVZX_GPRv_GPR8	movzx rax, al	0	0.25
XED_IFORM_MOVZX_GPRv_GPR16	movzx rax, ax	0	0.25
XED_IFORM_MUL_MEMv	mul [rdi]	8	1
XED_IFORM_MUL_MEMb	mul [rdi]	8	1
XED_IFORM_MUL_GPR8	mul al	3	1
XED_IFORM_MUL_GPRv	mul rax	4	1
XED_IFORM_MULX_VGPR32d_VGPR32d_MEMd	mulx eax, ecx, [rdi]	10	1
XED_IFORM_MULX_VGPR32d_VGPR32d_VGPR32d	mulx eax, ecx, edx	5	1
XED_IFORM_MULX_VGPR64q_VGPR64q_MEMq	mulx rax, rcx, [rdi]	9	1
XED_IFORM_MULX_VGPR64q_VGPR64q_VGPR64q	mulx rax, rcx, rdx	4	1
XED_IFORM_NEG_MEMv	neg [rdi]	6	1
XED_IFORM_NEG_MEMb	neg [rdi]	6	1
XED_IFORM_NEG_GPR8	neg al	1	0.25
XED_IFORM_NEG_GPRv	neg rax	1	0.25
XED_IFORM_NOP_90	nop	1	0.25
XED_IFORM_NOT_MEMv	not [rdi]	6	1
XED_IFORM_NOT_MEMb	not [rdi]	6	1
XED_IFORM_NOT_GPR8	not al	1	0.25
XED_IFORM_NOT_GPRv	not rax	1	0.25
XED_IFORM_OR_MEMv_IMMb	or [rdi], 1	6	1
XED_IFORM_OR_MEMv_IMMz	or [rdi], 1	6	1
XED_IFORM_OR_MEMb_IMMb_80r1	or [rdi], 1	6	1
XED_IFORM_OR_MEMb_IMMb_82r1	or [rdi], 1	6	1
XED_IFORM_OR_MEMb_GPR8	or [rdi], al	6	1
XED_IFORM_OR_MEMv_GPRv	or [rdi], rax	6	1
XED_IFORM_OR_GPR8_MEMb	or al, [rdi]	6	0.5
XED_IFORM_OR_GPR8_IMMb_80r1	or al, 1	1	0.25
XED_IFORM_OR_AL_IMMb	or al, 1	1	0.25
XED_IFORM_OR_GPR8_IMMb_82r1	or al, 1	1	0.25
XED_IFORM_OR_GPR8_GPR8_08	or al, cl	1	0.25
XED_IFORM_OR_GPR8_GPR8_0A	or al, cl	1	0.25
XED_IFORM_OR_OrAX_IMMz	or ax, 1	1	0.25
XED_IFORM_OR_GPRv_MEMv	or rax, [rdi]	6	0.5
XED_IFORM_OR_GPRv_IMMz	or rax, 1	1	0.25
XED_IFORM_OR_GPRv_IMMb	or rax, 1	1	0.25
XED_IFORM_OR_GPRv_GPRv_0B	or rax, rcx	1	0.25
XED_IFORM_OR_GPRv_GPRv_09	or rax, rcx	1	0.25
XED_IFORM_PABSB_MMXq_MEMq	pabsb mmx0, [rdi]	6	0.5
XED_IFORM_PABSB_MMXq_MMXq	pabsb mmx0, mmx0	1	0.5
XED_IFORM_PABSD_MMXq_MEMq	pabsd mmx0, [rdi]	6	0.5
XED_IFORM_PABSD_MMXq_MMXq	pabsd mmx0, mmx0	1	0.5
XED_IFORM_PABSW_MMXq_MEMq	pabsw mmx0, [rdi]	6	0.5
XED_IFORM_PABSW_MMXq_MMXq	pabsw mmx0, mmx0	1	0.5
XED_IFORM_PACKSSDW_MMXq_MEMq	packssdw mmx0, [rdi]	7	2
XED_IFORM_PACKSSDW_MMXq_MMXq	packssdw mmx0, mmx0	3	2
XED_IFORM_PACKSSWB_MMXq_MEMq	packsswb mmx0, [rdi]	7	2
XED_IFORM_PACKSSWB_MMXq_MMXq	packsswb mmx0, mmx0	3	2
XED_IFORM_PACKUSWB_MMXq_MEMq	packuswb mmx0, [rdi]	7	2
XED_IFORM_PACKUSWB_MMXq_MMXq	packuswb mmx0, mmx0	3	2
XED_IFORM_PADDB_MMXq_MEMq	paddb mmx0, [rdi]	6	0.5
XED_IFORM_PADDB_MMXq_MMXq	paddb mmx0, mmx0	1	0.5
XED_IFORM_PADDD_MMXq_MEMq	paddd mmx0, [rdi]	6	0.5

XED_IFORM_PADDD_MMXq_MMXq	paddd mmx0, mmx0	1	0.5
XED_IFORM_PADDQ_MMXq_MEMq	paddq mmx0, [rdi]	6	0.5
XED_IFORM_PADDQ_MMXq_MMXq	paddq mmx0, mmx0	1	0.5
XED_IFORM_PADDSB_MMXq_MEMq	paddsb mmx0, [rdi]	6	1
XED_IFORM_PADDSB_MMXq_MMXq	paddsb mmx0, mmx0	1	1
XED_IFORM_PADDSW_MMXq_MEMq	paddsw mmx0, [rdi]	6	1
XED_IFORM_PADDSW_MMXq_MMXq	paddsw mmx0, mmx0	1	1
XED_IFORM_PADDUSB_MMXq_MEMq	paddusb mmx0, [rdi]	6	1
XED_IFORM_PADDUSB_MMXq_MMXq	paddusb mmx0, mmx0	1	1
XED_IFORM_PADDUSW_MMXq_MEMq	paddusw mmx0, [rdi]	6	1
XED_IFORM_PADDUSW_MMXq_MMXq	paddusw mmx0, mmx0	1	1
XED_IFORM_PADDW_MMXq_MEMq	paddw mmx0, [rdi]	6	0.5
XED_IFORM_PADDW_MMXq_MMXq	paddw mmx0, mmx0	1	0.5
XED_IFORM_PALIGNR_MMXq_MEMq_IMMb	palignr mmx0, [rdi], 1	6	1
XED_IFORM_PALIGNR_MMXq_MMXq_IMMb	palignr mmx0, mmx0, 1	1	1
XED_IFORM_PAND_MMXq_MEMq	pand mmx0, [rdi]	6	0.5
XED_IFORM_PAND_MMXq_MMXq	pand mmx0, mmx0	1	0.5
XED_IFORM_PANDN_MMXq_MEMq	pandn mmx0, [rdi]	6	0.5
XED_IFORM_PANDN_MMXq_MMXq	pandn mmx0, mmx0	1	0.5
XED_IFORM_PAUSE	pause	140	140
XED_IFORM_PAVGB_MMXq_MEMq	pavgb mmx0, [rdi]	6	1
XED_IFORM_PAVGB_MMXq_MMXq	pavgb mmx0, mmx0	1	1
XED_IFORM_PAVGW_MMXq_MEMq	pavgw mmx0, [rdi]	6	1
XED_IFORM_PAVGW_MMXq_MMXq	pavgw mmx0, mmx0	1	1
XED_IFORM_PCMPEQB_MMXq_MEMq	pcmpeqb mmx0, [rdi]	6	1
XED_IFORM_PCMPEQB_MMXq_MMXq	pcmpeqb mmx0, mmx0	1	1
XED_IFORM_PCMPEQD_MMXq_MEMq	pcmpeqd mmx0, [rdi]	6	1
XED_IFORM_PCMPEQD_MMXq_MMXq	pcmpeqd mmx0, mmx0	1	1
XED_IFORM_PCMPEQW_MMXq_MEMq	pcmpeqw mmx0, [rdi]	6	1
XED_IFORM_PCMPEQW_MMXq_MMXq	pcmpeqw mmx0, mmx0	1	1
XED_IFORM_PCMPGTB_MMXq_MEMq	pcmpgtb mmx0, [rdi]	6	1
XED_IFORM_PCMPGTB_MMXq_MMXq	pcmpgtb mmx0, mmx0	1	1
XED_IFORM_PCMPGTD_MMXq_MEMq	pcmpgtd mmx0, [rdi]	6	1
XED_IFORM_PCMPGTD_MMXq_MMXq	pcmpgtd mmx0, mmx0	1	1
XED_IFORM_PCMPGTW_MMXq_MEMq	pcmpgtw mmx0, [rdi]	6	1
XED_IFORM_PCMPGTW_MMXq_MMXq	pcmpgtw mmx0, mmx0	1	1
XED_IFORM_PDEP_VGPR32d_VGPR32d_MEMd	pdep eax, ecx, [rdi]	8	1
XED_IFORM_PDEP_VGPR32d_VGPR32d_VGPR32d	pdep eax, ecx, edx	3	1
XED_IFORM_PDEP_VGPR64q_VGPR64q_MEMq	pdep rax, rcx, [rdi]	8	1
XED_IFORM_PDEP_VGPR64q_VGPR64q_VGPR64q	pdep rax, rcx, rdx	3	1
XED_IFORM_PEXT_VGPR32d_VGPR32d_MEMd	pext eax, ecx, [rdi]	8	1
XED_IFORM_PEXT_VGPR32d_VGPR32d_VGPR32d	pext eax, ecx, edx	3	1
XED_IFORM_PEXT_VGPR64q_VGPR64q_MEMq	pext rax, rcx, [rdi]	8	1
XED_IFORM_PEXT_VGPR64q_VGPR64q_VGPR64q	pext rax, rcx, rdx	3	1
XED_IFORM_PEXTRW_GPR32_MMXq_IMMb	pextrw eax, mmx0, 1	3	1
XED_IFORM_PHADDD_MMXq_MEMq	phaddd mmx0, [rdi]	8	2
XED_IFORM_PHADDD_MMXq_MMXq	phaddd mmx0, mmx0	3	2
XED_IFORM_PHADDSW_MMXq_MEMq	phaddsw mmx0, [rdi]	8	2
XED_IFORM_PHADDSW_MMXq_MMXq	phaddsw mmx0, mmx0	3	2
XED_IFORM_PHADDW_MMXq_MEMq	phaddw mmx0, [rdi]	8	2
XED_IFORM_PHADDW_MMXq_MMXq	phaddw mmx0, mmx0	3	2
XED_IFORM_PHSUBD_MMXq_MEMq	phsubd mmx0, [rdi]	8	2
XED_IFORM_PHSUBD_MMXq_MMXq	phsubd mmx0, mmx0	3	2
XED_IFORM_PHSUBSW_MMXq_MEMq	phsubsw mmx0, [rdi]	8	2
XED_IFORM_PHSUBSW_MMXq_MMXq	phsubsw mmx0, mmx0	3	2
XED_IFORM_PHSUBW_MMXq_MEMq	phsubw mmx0, [rdi]	8	2
XED_IFORM_PHSUBW_MMXq_MMXq	phsubw mmx0, mmx0	3	2
XED_IFORM_PINSRW_MMXq_MEMw_IMMb	pinsrw mmx0, [rdi], 1	6	1
XED_IFORM_PINSRW_MMXq_GPR32_IMMb	pinsrw mmx0, eax, 1	2	2
XED_IFORM_PMADDUBSW_MMXq_MEMq	pmaddubsw mmx0, [rdi]	9	1
XED_IFORM_PMADDUBSW_MMXq_MMXq	pmaddubsw mmx0, mmx0	4	1
XED_IFORM_PMADDWD_MMXq_MEMq	pmaddwd mmx0, [rdi]	9	1
XED_IFORM_PMADDWD_MMXq_MMXq	pmaddwd mmx0, mmx0	4	1
XED_IFORM_PMAXSW_MMXq_MEMq	pmaxsw mmx0, [rdi]	6	1
XED_IFORM_PMAXSW_MMXq_MMXq	pmaxsw mmx0, mmx0	1	1
XED_IFORM_PMAXUB_MMXq_MEMq	pmaxub mmx0, [rdi]	6	1
XED_IFORM_PMAXUB_MMXq_MMXq	pmaxub mmx0, mmx0	1	1
XED_IFORM_PMINSW_MMXq_MEMq	pminsw mmx0, [rdi]	6	1
XED_IFORM_PMINSW_MMXq_MMXq	pminsw mmx0, mmx0	1	1
XED_IFORM_PMINUB_MMXq_MEMq	pminub mmx0, [rdi]	6	1
XED_IFORM_PMINUB_MMXq_MMXq	pminub mmx0, mmx0	1	1
XED_IFORM_PMOVMSKB_GPR32_MMXq	pmovmskb eax, mmx0	2	1
XED_IFORM_PMULHRSW_MMXq_MEMq	pmulhrsw mmx0, [rdi]	9	1
XED_IFORM_PMULHRSW_MMXq_MMXq	pmulhrsw mmx0, mmx0	4	1
XED_IFORM_PMULHUW_MMXq_MEMq	pmulhuw mmx0, [rdi]	9	1
XED_IFORM_PMULHUW_MMXq_MMXq	pmulhuw mmx0, mmx0	4	1
XED_IFORM_PMULHW_MMXq_MEMq	pmulhw mmx0, [rdi]	9	1
XED_IFORM_PMULHW_MMXq_MMXq	pmulhw mmx0, mmx0	4	1
XED_IFORM_PMULLW_MMXq_MEMq	pmullw mmx0, [rdi]	9	1

XED_IFORM_PMULLW_MMXq_MMXq	pmullw mmx0, mmx0	4	1
XED_IFORM_PMULUDQ_MMXq_MEMq	pmuludq mmx0, [rdi]	9	1
XED_IFORM_PMULUDQ_MMXq_MMXq	pmuludq mmx0, mmx0	4	1
XED_IFORM_POP_MEMv	pop [rdi]	6	1
XED_IFORM_POP_GPRv_8F	pop rax	6	0.5
XED_IFORM_POP_GPRv_51	pop rax	6	0.5
XED_IFORM_POPCNT_GPRv_MEMv	popcnt rax, [rdi]	8	1
XED_IFORM_POPCNT_GPRv_GPRv	popcnt rax, rcx	3	1
XED_IFORM_POR_MMXq_MEMq	por mmx0, [rdi]	6	0.5
XED_IFORM_POR_MMXq_MMXq	por mmx0, mmx0	1	0.5
XED_IFORM_PREFETCHNTA_MEMmprefetch	prefetchnta [rdi]	5	0.5
XED_IFORM_PREFETCHT0_MEMmprefetch	prefetcht0 [rdi]	5	0.5
XED_IFORM_PREFETCHT1_MEMmprefetch	prefetcht1 [rdi]	5	0.5
XED_IFORM_PREFETCHT2_MEMmprefetch	prefetcht2 [rdi]	5	0.5
XED_IFORM_PSADBW_MMXq_MEMq	psadbw mmx0, [rdi]	8	1
XED_IFORM_PSADBW_MMXq_MMXq	psadbw mmx0, mmx0	3	1
XED_IFORM_PSHUFB_MMXq_MEMq	pshufb mmx0, [rdi]	6	1
XED_IFORM_PSHUFB_MMXq_MMXq	pshufb mmx0, mmx0	1	1
XED_IFORM_PSHUFW_MMXq_MEMq_IMMb	pshufw mmx0, [rdi], 1	6	1
XED_IFORM_PSHUFW_MMXq_MMXq_IMMb	pshufw mmx0, mmx0, 1	1	1
XED_IFORM_PSIGNB_MMXq_MEMq	psignb mmx0, [rdi]	6	0.5
XED_IFORM_PSIGNB_MMXq_MMXq	psignb mmx0, mmx0	1	0.5
XED_IFORM_PSIGND_MMXq_MEMq	psignd mmx0, [rdi]	6	0.5
XED_IFORM_PSIGND_MMXq_MMXq	psignd mmx0, mmx0	1	0.5
XED_IFORM_PSIGNW_MMXq_MEMq	psignw mmx0, [rdi]	6	0.5
XED_IFORM_PSIGNW_MMXq_MMXq	psignw mmx0, mmx0	1	0.5
XED_IFORM_PSLLD_MMXq_MEMq	pslld mmx0, [rdi]	6	1
XED_IFORM_PSLLD_MMXq_IMMb	pslld mmx0, 1	1	1
XED_IFORM_PSLLD_MMXq_MMXq	pslld mmx0, mmx0	1	1
XED_IFORM_PSLLQ_MMXq_MEMq	psllq mmx0, [rdi]	6	1
XED_IFORM_PSLLQ_MMXq_IMMb	psllq mmx0, 1	1	1
XED_IFORM_PSLLQ_MMXq_MMXq	psllq mmx0, mmx0	1	1
XED_IFORM_PSLLW_MMXq_MEMq	psllw mmx0, [rdi]	6	1
XED_IFORM_PSLLW_MMXq_IMMb	psllw mmx0, 1	1	1
XED_IFORM_PSLLW_MMXq_MMXq	psllw mmx0, mmx0	1	1
XED_IFORM_PSRAD_MMXq_MEMq	psrad mmx0, [rdi]	6	1
XED_IFORM_PSRAD_MMXq_IMMb	psrad mmx0, 1	1	1
XED_IFORM_PSRAD_MMXq_MMXq	psrad mmx0, mmx0	1	1
XED_IFORM_PSRAW_MMXq_MEMq	psraw mmx0, [rdi]	6	1
XED_IFORM_PSRAW_MMXq_IMMb	psraw mmx0, 1	1	1
XED_IFORM_PSRAW_MMXq_MMXq	psraw mmx0, mmx0	1	1
XED_IFORM_PSRLD_MMXq_MEMq	psrld mmx0, [rdi]	6	1
XED_IFORM_PSRLD_MMXq_IMMb	psrld mmx0, 1	1	1
XED_IFORM_PSRLD_MMXq_MMXq	psrld mmx0, mmx0	1	1
XED_IFORM_PSRLQ_MMXq_MEMq	psrlq mmx0, [rdi]	6	1
XED_IFORM_PSRLQ_MMXq_IMMb	psrlq mmx0, 1	1	1
XED_IFORM_PSRLQ_MMXq_MMXq	psrlq mmx0, mmx0	1	1
XED_IFORM_PSRLW_MMXq_MEMq	psrlw mmx0, [rdi]	6	1
XED_IFORM_PSRLW_MMXq_IMMb	psrlw mmx0, 1	1	1
XED_IFORM_PSRLW_MMXq_MMXq	psrlw mmx0, mmx0	1	1
XED_IFORM_PSUBB_MMXq_MEMq	psubb mmx0, [rdi]	6	0.5
XED_IFORM_PSUBB_MMXq_MMXq	psubb mmx0, mmx0	1	0.5
XED_IFORM_PSUBD_MMXq_MEMq	psubd mmx0, [rdi]	6	0.5
XED_IFORM_PSUBD_MMXq_MMXq	psubd mmx0, mmx0	1	0.5
XED_IFORM_PSUBQ_MMXq_MEMq	psubq mmx0, [rdi]	6	0.5
XED_IFORM_PSUBQ_MMXq_MMXq	psubq mmx0, mmx0	1	0.5
XED_IFORM_PSUBSB_MMXq_MEMq	psubsb mmx0, [rdi]	6	1
XED_IFORM_PSUBSB_MMXq_MMXq	psubsb mmx0, mmx0	1	1
XED_IFORM_PSUBSW_MMXq_MEMq	psubsw mmx0, [rdi]	6	1
XED_IFORM_PSUBSW_MMXq_MMXq	psubsw mmx0, mmx0	1	1
XED_IFORM_PSUBUSB_MMXq_MEMq	psubusb mmx0, [rdi]	6	1
XED_IFORM_PSUBUSB_MMXq_MMXq	psubusb mmx0, mmx0	1	1
XED_IFORM_PSUBUSW_MMXq_MEMq	psubusw mmx0, [rdi]	6	1
XED_IFORM_PSUBUSW_MMXq_MMXq	psubusw mmx0, mmx0	1	1
XED_IFORM_PSUBW_MMXq_MEMq	psubw mmx0, [rdi]	6	0.5
XED_IFORM_PSUBW_MMXq_MMXq	psubw mmx0, mmx0	1	0.5
XED_IFORM_PUNPCKHBW_MMXq_MEMq	punpckhbw mmx0, [rdi]	6	1
XED_IFORM_PUNPCKHBW_MMXq_MMXd	punpckhbw mmx0, mmx0	1	1
XED_IFORM_PUNPCKHDQ_MMXq_MEMq	punpckhdq mmx0, [rdi]	6	1
XED_IFORM_PUNPCKHDQ_MMXq_MMXd	punpckhdq mmx0, mmx0	1	1
XED_IFORM_PUNPCKHWD_MMXq_MEMq	punpckhwd mmx0, [rdi]	6	1
XED_IFORM_PUNPCKHWD_MMXq_MMXd	punpckhwd mmx0, mmx0	1	1
XED_IFORM_PUNPCKLBW_MMXq_MEMd	punpcklbw mmx0, [rdi]	6	1
XED_IFORM_PUNPCKLBW_MMXq_MMXd	punpcklbw mmx0, mmx0	1	1
XED_IFORM_PUNPCKLDQ_MMXq_MEMd	punpckldq mmx0, [rdi]	6	1
XED_IFORM_PUNPCKLDQ_MMXq_MMXd	punpckldq mmx0, mmx0	1	1
XED_IFORM_PUNPCKLWD_MMXq_MEMd	punpcklwd mmx0, [rdi]	6	1
XED_IFORM_PUNPCKLWD_MMXq_MMXd	punpcklwd mmx0, mmx0	1	1
XED_IFORM_PUSH_MEMv	push [rdi]	6	1

XED_IFORM_PUSH_IMMb	push 1	6	1
XED_IFORM_PUSH_IMMz	push 1	6	1
XED_IFORM_PUSH_GPRv_FFr6	push rax	6	1
XED_IFORM_PUSH_GPRv_50	push rax	6	1
XED_IFORM_PUSHFQ	pushfq	9	1
XED_IFORM_PXOR_MMXq_MEMq	pxor mmx0, [rdi]	6	0.5
XED_IFORM_PXOR_MMXq_MMXq	pxor mmx0, mmx0	1	0.5
XED_IFORM_RCL_MEMv_IMMb	rcl [rdi], 1	8	1
XED_IFORM_RCL_MEMb_ONE	rcl [rdi], 1	8	1
XED_IFORM_RCL_MEMb_IMMb	rcl [rdi], 1	8	1
XED_IFORM_RCL_MEMv_ONE	rcl [rdi], 1	8	1
XED_IFORM_RCL_MEMv_CL	rcl [rdi], cl	15	2.5
XED_IFORM_RCL_MEMb_CL	rcl [rdi], cl	15	2.5
XED_IFORM_RCL_GPR8_ONE	rcl al, 1	3	0.75
XED_IFORM_RCL_GPR8_IMMb	rcl al, 1	3	0.75
XED_IFORM_RCL_GPR8_CL	rcl al, cl	11	2.5
XED_IFORM_RCL_GPRv_ONE	rcl rax, 1	3	0.75
XED_IFORM_RCL_GPRv_IMMb	rcl rax, 1	3	0.75
XED_IFORM_RCL_GPRv_CL	rcl rax, cl	11	2
XED_IFORM_RCR_MEMb_IMMb	rcr [rdi], 1	8	1
XED_IFORM_RCR_MEMb_ONE	rcr [rdi], 1	8	1
XED_IFORM_RCR_MEMv_IMMb	rcr [rdi], 1	8	1
XED_IFORM_RCR_MEMv_ONE	rcr [rdi], 1	8	1
XED_IFORM_RCR_MEMb_CL	rcr [rdi], cl	18	2.31
XED_IFORM_RCR_MEMv_CL	rcr [rdi], cl	18	2.31
XED_IFORM_RCR_GPR8_IMMb	rcr al, 1	3	0.75
XED_IFORM_RCR_GPR8_ONE	rcr al, 1	3	0.75
XED_IFORM_RCR_GPR8_CL	rcr al, cl	14	2.5
XED_IFORM_RCR_GPRv_IMMb	rcr rax, 1	3	0.75
XED_IFORM_RCR_GPRv_ONE	rcr rax, 1	3	0.75
XED_IFORM_RCR_GPRv_CL	rcr rax, cl	11	2
XED_IFORM_RDTSC	rdtsc	18	2
XED_IFORM_RDTSCP	rdtscp	42	5.5
XED_IFORM_REPE_SCASB	rep scasb [rdi]	22	4.25
XED_IFORM_REPE_SCASD	rep scasd [rdi]	22	4.25
XED_IFORM_REPE_SCASQ	rep scasq [rdi]	22	4.25
XED_IFORM_REPE_SCASW	rep scasw [rdi]	22	4.25
XED_IFORM_REPNE_SCASB	repne scasb [rdi]	34	7.75
XED_IFORM_RET_FAR	ret	7	1
XED_IFORM_RET_NEAR	ret	7	1
XED_IFORM_RET_NEAR_IMMw	ret 1	8	2
XED_IFORM_RET_FAR_IMMw	ret 1	8	2
XED_IFORM_ROL_MEMv_ONE	rol [rdi], 1	7	1
XED_IFORM_ROL_MEMb_ONE	rol [rdi], 1	7	1
XED_IFORM_ROL_MEMv_IMMb	rol [rdi], 1	7	1
XED_IFORM_ROL_MEMb_IMMb	rol [rdi], 1	7	1
XED_IFORM_ROL_MEMb_CL	rol [rdi], cl	8	1.5
XED_IFORM_ROL_MEMv_CL	rol [rdi], cl	8	1.5
XED_IFORM_ROL_GPR8_ONE	rol al, 1	2	1
XED_IFORM_ROL_GPR8_IMMb	rol al, 1	2	1
XED_IFORM_ROL_GPR8_CL	rol al, cl	3	1.5
XED_IFORM_ROL_GPRv_ONE	rol rax, 1	2	1
XED_IFORM_ROL_GPRv_IMMb	rol rax, 1	2	1
XED_IFORM_ROL_GPRv_CL	rol rax, cl	3	1.5
XED_IFORM_ROR_MEMv_IMMb	ror [rdi], 1	7	1
XED_IFORM_ROR_MEMb_IMMb	ror [rdi], 1	7	1
XED_IFORM_ROR_MEMv_ONE	ror [rdi], 1	7	1
XED_IFORM_ROR_MEMb_ONE	ror [rdi], 1	7	1
XED_IFORM_ROR_MEMb_CL	ror [rdi], cl	8	1.5
XED_IFORM_ROR_MEMv_CL	ror [rdi], cl	8	1.5
XED_IFORM_ROR_GPR8_IMMb	ror al, 1	2	1
XED_IFORM_ROR_GPR8_ONE	ror al, 1	2	1
XED_IFORM_ROR_GPR8_CL	ror al, cl	3	1.5
XED_IFORM_ROR_GPRv_ONE	ror rax, 1	2	1
XED_IFORM_ROR_GPRv_IMMb	ror rax, 1	2	1
XED_IFORM_ROR_GPRv_CL	ror rax, cl	3	1.5
XED_IFORM_RORX_VGPR32d_MEMd_IMMb	rorx eax, [rdi], 1	6	0.5
XED_IFORM_RORX_VGPR32d_VGPR32d_IMMb	rorx eax, ecx, 1	1	0.5
XED_IFORM_RORX_VGPR64q_MEMq_IMMb	rorx rax, [rdi], 1	6	0.5
XED_IFORM_RORX_VGPR64q_VGPR64q_IMMb	rorx rax, rcx, 1	1	0.5
XED_IFORM_SAHF	sahf	1	0.25
XED_IFORM_SAR_MEMb_ONE	sar [rdi], 1	6	1
XED_IFORM_SAR_MEMv_ONE	sar [rdi], 1	6	1
XED_IFORM_SAR_MEMb_IMMb	sar [rdi], 1	6	1
XED_IFORM_SAR_MEMv_IMMb	sar [rdi], 1	6	1
XED_IFORM_SAR_MEMv_CL	sar [rdi], cl	8	1.5
XED_IFORM_SAR_MEMb_CL	sar [rdi], cl	8	1.5
XED_IFORM_SAR_GPR8_ONE	sar al, 1	1	0.5
XED_IFORM_SAR_GPR8_IMMb	sar al, 1	1	0.5

XED_IFORM_SAR_GPR8_CL	sar al, cl	3	1.5
XED_IFORM_SAR_GPRv_ONE	sar rax, 1	1	0.5
XED_IFORM_SAR_GPRv_IMMb	sar rax, 1	1	0.5
XED_IFORM_SAR_GPRv_CL	sar rax, cl	3	1.5
XED_IFORM_SARX_VGPR32d_MEMd_VGPR32d	sarx eax, [rdi], ecx	6	0.5
XED_IFORM_SARX_VGPR32d_VGPR32d_VGPR32d	sarx eax, ecx, edx	1	0.5
XED_IFORM_SARX_VGPR64q_MEMq_VGPR64q	sarx rax, [rdi], rcx	6	0.5
XED_IFORM_SARX_VGPR64q_VGPR64q_VGPR64q	sarx rax, rcx, rdx	1	0.5
XED_IFORM_SBB_MEMb_IMMb_80r3	sbb [rdi], 1	8	1
XED_IFORM_SBB_MEMv_IMMb	sbb [rdi], 1	8	1
XED_IFORM_SBB_MEMv_IMMz	sbb [rdi], 1	8	1
XED_IFORM_SBB_MEMb_IMMb_82r3	sbb [rdi], 1	8	1
XED_IFORM_SBB_MEMb_GPR8	sbb [rdi], al	8	1
XED_IFORM_SBB_MEMv_GPRv	sbb [rdi], rax	8	1
XED_IFORM_SBB_GPR8_MEMb	sbb al, [rdi]	6	0.5
XED_IFORM_SBB_GPR8_IMMb_82r3	sbb al, 1	2	0.5
XED_IFORM_SBB_GPR8_IMMb_80r3	sbb al, 1	2	0.5
XED_IFORM_SBB_AL_IMMb	sbb al, 1	2	0.5
XED_IFORM_SBB_GPR8_GPR8_18	sbb al, cl	1	0.5
XED_IFORM_SBB_GPR8_GPR8_1A	sbb al, cl	1	0.5
XED_IFORM_SBB_OrAX_IMMz	sbb ax, 1	1	0.5
XED_IFORM_SBB_GPRv_MEMv	sbb rax, [rdi]	6	0.5
XED_IFORM_SBB_GPRv_IMMz	sbb rax, 1	1	0.5
XED_IFORM_SBB_GPRv_IMMb	sbb rax, 1	1	0.5
XED_IFORM_SBB_GPRv_GPRv_19	sbb rax, rcx	1	0.5
XED_IFORM_SBB_GPRv_GPRv_1B	sbb rax, rcx	1	0.5
XED_IFORM_SCASB	scasb [rdi]	7	0.5
XED_IFORM_SCASD	scasd [rdi]	7	0.5
XED_IFORM_SCASQ	scasq [rdi]	7	0.5
XED_IFORM_SCASW	scasw [rdi]	7	0.5
XED_IFORM_SETB_MEMb	setb [rdi]	6	1
XED_IFORM_SETB_GPR8	setb al	1	0.5
XED_IFORM_SETBE_MEMb	setbe [rdi]	7	1
XED_IFORM_SETBE_GPR8	setbe al	2	1
XED_IFORM_SETL_MEMb	setl [rdi]	6	1
XED_IFORM_SETL_GPR8	setl al	1	0.5
XED_IFORM_SETLE_MEMb	setle [rdi]	6	1
XED_IFORM_SETLE_GPR8	setle al	1	0.5
XED_IFORM_SETNB_MEMb	setnb [rdi]	6	1
XED_IFORM_SETNB_GPR8	setnb al	1	0.5
XED_IFORM_SETNBE_MEMb	setnbe [rdi]	7	1
XED_IFORM_SETNBE_GPR8	setnbe al	2	1
XED_IFORM_SETNL_MEMb	setnl [rdi]	6	1
XED_IFORM_SETNL_GPR8	setnl al	1	0.5
XED_IFORM_SETNLE_MEMb	setnle [rdi]	6	1
XED_IFORM_SETNLE_GPR8	setnle al	1	0.5
XED_IFORM_SETNO_MEMb	setno [rdi]	6	1
XED_IFORM_SETNO_GPR8	setno al	1	0.5
XED_IFORM_SETNP_MEMb	setnp [rdi]	6	1
XED_IFORM_SETNP_GPR8	setnp al	1	0.5
XED_IFORM_SETNS_MEMb	setns [rdi]	6	1
XED_IFORM_SETNS_GPR8	setns al	1	0.5
XED_IFORM_SETNZ_MEMb	setnz [rdi]	6	1
XED_IFORM_SETNZ_GPR8	setnz al	1	0.5
XED_IFORM_SETO_MEMb	seto [rdi]	6	1
XED_IFORM_SETO_GPR8	seto al	1	0.5
XED_IFORM_SETP_MEMb	setp [rdi]	6	1
XED_IFORM_SETP_GPR8	setp al	1	0.5
XED_IFORM_SETS_MEMb	sets [rdi]	6	1
XED_IFORM_SETS_GPR8	sets al	1	0.5
XED_IFORM_SETZ_MEMb	setz [rdi]	6	1
XED_IFORM_SETZ_GPR8	setz al	1	0.5
XED_IFORM_SGDT_MEMs	sgdt ptr [rdi]	1	0.25
XED_IFORM_SGDT_MEMs64	sgdt ptr [rdi]	1	0.25
XED_IFORM_SHL_MEMv_IMMb_C1r4	shl [rdi], 1	6	1
XED_IFORM_SHL_MEMv_ONE_D1r6	shl [rdi], 1	6	1
XED_IFORM_SHL_MEMb_IMMb_C0r4	shl [rdi], 1	6	1
XED_IFORM_SHL_MEMb_IMMb_C0r6	shl [rdi], 1	6	1
XED_IFORM_SHL_MEMv_IMMb_C1r6	shl [rdi], 1	6	1
XED_IFORM_SHL_MEMv_ONE_D1r4	shl [rdi], 1	6	1
XED_IFORM_SHL_MEMb_ONE_D0r6	shl [rdi], 1	6	1
XED_IFORM_SHL_MEMb_ONE_D0r4	shl [rdi], 1	6	1
XED_IFORM_SHL_MEMb_CL_D2r4	shl [rdi], cl	8	1.5
XED_IFORM_SHL_MEMv_CL_D3r4	shl [rdi], cl	8	1.5
XED_IFORM_SHL_MEMb_CL_D2r6	shl [rdi], cl	8	1.5
XED_IFORM_SHL_MEMv_CL_D3r6	shl [rdi], cl	8	1.5
XED_IFORM_SHL_GPR8_ONE_D0r6	shl al, 1	1	0.5
XED_IFORM_SHL_GPR8_IMMb_C0r4	shl al, 1	1	0.5
XED_IFORM_SHL_GPR8_IMMb_C0r6	shl al, 1	1	0.5

XED_IFORM_SHL_GPR8_ONE_D0r4	shl al, 1	1	0.5
XED_IFORM_SHL_GPR8_CL_D2r4	shl al, cl	3	1.5
XED_IFORM_SHL_GPR8_CL_D2r6	shl al, cl	3	1.5
XED_IFORM_SHL_GPRv_ONE_D1r4	shl rax, 1	1	0.5
XED_IFORM_SHL_GPRv_IMMb_C1r6	shl rax, 1	1	0.5
XED_IFORM_SHL_GPRv_ONE_D1r6	shl rax, 1	1	0.5
XED_IFORM_SHL_GPRv_IMMb_C1r4	shl rax, 1	1	0.5
XED_IFORM_SHL_GPRv_CL_D3r6	shl rax, cl	3	1.5
XED_IFORM_SHL_GPRv_CL_D3r4	shl rax, cl	3	1.5
XED_IFORM_SHLD_MEMv_GPRv_IMMb	shld [rdi], rax, 1	9	1
XED_IFORM_SHLD_MEMv_GPRv_CL	shld [rdi], rax, cl	11	1
XED_IFORM_SHLD_GPRv_GPRv_IMMb	shld rax, rcx, 1	3	1
XED_IFORM_SHLD_GPRv_GPRv_CL	shld rax, rcx, cl	6	1
XED_IFORM_SHLX_VGPR32d_MEMd_VGPR32d	shlx eax, [rdi], ecx	6	0.5
XED_IFORM_SHLX_VGPR32d_VGPR32d_VGPR32d	shlx eax, ecx, edx	1	0.5
XED_IFORM_SHLX_VGPR64q_MEMq_VGPR64q	shlx rax, [rdi], rcx	6	0.5
XED_IFORM_SHLX_VGPR64q_VGPR64q_VGPR64q	shlx rax, rcx, rdx	1	0.5
XED_IFORM_SHR_MEMv_ONE	shr [rdi], 1	6	1
XED_IFORM_SHR_MEMv_IMMb	shr [rdi], 1	6	1
XED_IFORM_SHR_MEMb_IMMb	shr [rdi], 1	6	1
XED_IFORM_SHR_MEMb_ONE	shr [rdi], 1	6	1
XED_IFORM_SHR_MEMb_CL	shr [rdi], cl	8	1.5
XED_IFORM_SHR_MEMv_CL	shr [rdi], cl	8	1.5
XED_IFORM_SHR_GPR8_ONE	shr al, 1	1	0.5
XED_IFORM_SHR_GPR8_IMMb	shr al, 1	1	0.5
XED_IFORM_SHR_GPR8_CL	shr al, cl	3	1.5
XED_IFORM_SHR_GPRv_IMMb	shr rax, 1	1	0.5
XED_IFORM_SHR_GPRv_ONE	shr rax, 1	1	0.5
XED_IFORM_SHR_GPRv_CL	shr rax, cl	3	1.5
XED_IFORM_SHRD_MEMv_GPRv_IMMb	shrd [rdi], rax, 1	9	1
XED_IFORM_SHRD_MEMv_GPRv_CL	shrd [rdi], rax, cl	11	1
XED_IFORM_SHRD_GPRv_GPRv_IMMb	shrd rax, rcx, 1	3	1
XED_IFORM_SHRD_GPRv_GPRv_CL	shrd rax, rcx, cl	6	1
XED_IFORM_SHRX_VGPR32d_MEMd_VGPR32d	shrx eax, [rdi], ecx	6	0.5
XED_IFORM_SHRX_VGPR32d_VGPR32d_VGPR32d	shrx eax, ecx, edx	1	0.5
XED_IFORM_SHRX_VGPR64q_MEMq_VGPR64q	shrx rax, [rdi], rcx	6	0.5
XED_IFORM_SHRX_VGPR64q_VGPR64q_VGPR64q	shrx rax, rcx, rdx	1	0.5
XED_IFORM_SIDT_MEMs64	sidt ptr [rdi]	1	0.25
XED_IFORM_SIDT_MEMs	sidt ptr [rdi]	1	0.25
XED_IFORM_SLDT_MEMw	sldt [rdi]	1	0.25
XED_IFORM_SLDT_GPRv	sldt rax	6	1
XED_IFORM_SMSW_MEMw	smsw [rdi]	1	0.25
XED_IFORM_STAC	stac	1	0.5
XED_IFORM_STC	stc	1	0.25
XED_IFORM_STD	std	6	1.5
XED_IFORM_STOSB	stosb [rdi]	6	1
XED_IFORM_STOSD	stosd [rdi]	6	1
XED_IFORM_STOSQ	stosq [rdi]	6	1
XED_IFORM_STOSW	stosw [rdi]	6	1
XED_IFORM_STR_MEMw	str [rdi]	1	0.25
XED_IFORM_STR_GPRv	str rax	5	1
XED_IFORM_SUB_MEMb_IMMb_82r5	sub [rdi], 1	6	1
XED_IFORM_SUB_MEMv_IMMb	sub [rdi], 1	6	1
XED_IFORM_SUB_MEMv_IMMz	sub [rdi], 1	6	1
XED_IFORM_SUB_MEMb_IMMb_80r5	sub [rdi], 1	6	1
XED_IFORM_SUB_MEMb_GPR8	sub [rdi], al	6	1
XED_IFORM_SUB_MEMv_GPRv	sub [rdi], rax	6	1
XED_IFORM_SUB_GPR8_MEMb	sub al, [rdi]	6	0.5
XED_IFORM_SUB_GPR8_IMMb_82r5	sub al, 1	1	0.25
XED_IFORM_SUB_GPR8_IMMb_80r5	sub al, 1	1	0.25
XED_IFORM_SUB_AL_IMMb	sub al, 1	1	0.25
XED_IFORM_SUB_GPR8_GPR8_28	sub al, cl	0	0.25
XED_IFORM_SUB_GPR8_GPR8_2A	sub al, cl	0	0.25
XED_IFORM_SUB_OrAX_IMMz	sub ax, 1	1	0.25
XED_IFORM_SUB_GPRv_MEMv	sub rax, [rdi]	6	0.5
XED_IFORM_SUB_GPRv_IMMb	sub rax, 1	1	0.25
XED_IFORM_SUB_GPRv_IMMz	sub rax, 1	1	0.25
XED_IFORM_SUB_GPRv_GPRv_29	sub rax, rcx	0	0.25
XED_IFORM_SUB_GPRv_GPRv_2B	sub rax, rcx	0	0.25
XED_IFORM_SYSCALL	syscall	1	0.25
XED_IFORM_TEST_MEMv_IMMz_F7r0	test [rdi], 1	6	0.5
XED_IFORM_TEST_MEMv_IMMz_F7r1	test [rdi], 1	6	0.5
XED_IFORM_TEST_MEMb_IMMb_F6r0	test [rdi], 1	6	0.5
XED_IFORM_TEST_MEMb_IMMb_F6r1	test [rdi], 1	6	0.5
XED_IFORM_TEST_MEMb_GPR8	test [rdi], al	6	0.5
XED_IFORM_TEST_MEMv_GPRv	test [rdi], rax	6	0.5
XED_IFORM_TEST_GPR8_IMMb_F6r0	test al, 1	1	0.25
XED_IFORM_TEST_GPR8_IMMb_F6r1	test al, 1	1	0.25
XED_IFORM_TEST_AL_IMMb	test al, 1	1	0.25

XED_IFORM_TEST_OrAX_IMMz	test ax, 1	1	0.25
XED_IFORM_TEST_GPR8_GPR8	test cl, al	1	0.25
XED_IFORM_TEST_GPRv_IMMz_F7r0	test rax, 1	1	0.25
XED_IFORM_TEST_GPRv_IMMz_F7r1	test rax, 1	1	0.25
XED_IFORM_TEST_GPRv_GPRv	test rcx, rax	1	0.25
XED_IFORM_TZCNT_GPRv_MEMv	tzcnt rax, [rdi]	8	1
XED_IFORM_TZCNT_GPRv_GPRv	tzcnt rax, rcx	3	1
XED_IFORM_ADDPD_XMMpd_MEMpd	vaddpd xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_ADDPD_XMMpd_XMMpd	vaddpd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VADDPD_XMMdq_XMMdq_MEMdq	vaddpd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VADDPD_XMMdq_XMMdq_XMMdq	vaddpd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VADDPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vaddpd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VADDPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vaddpd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VADDPD_YMMqq_YMMqq_MEMqq	vaddpd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VADDPD_YMMqq_YMMqq_YMMqq	vaddpd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VADDPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vaddpd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VADDPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vaddpd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VADDPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vaddpd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VADDPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vaddpd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_ADDPS_XMMps_MEMps	vaddps xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_ADDPS_XMMps_XMMps	vaddps xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VADDPS_XMMdq_XMMdq_MEMdq	vaddps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VADDPS_XMMdq_XMMdq_XMMdq	vaddps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VADDPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vaddps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VADDPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vaddps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VADDPS_YMMqq_YMMqq_MEMqq	vaddps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VADDPS_YMMqq_YMMqq_YMMqq	vaddps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VADDPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vaddps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VADDPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vaddps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VADDPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vaddps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VADDPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vaddps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_ADDSD_XMMsd_MEMsd	vaddsd xmm1, xmm1, [rdi]	9	0.5
XED_IFORM_ADDSD_XMMsd_XMMsd	vaddsd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VADDSD_XMMdq_XMMdq_MEMq	vaddsd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VADDSD_XMMdq_XMMdq_XMMq	vaddsd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VADDSD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vaddsd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VADDSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vaddsd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_ADDSS_XMMss_MEMss	vaddss xmm1, xmm1, [rdi]	9	0.5
XED_IFORM_ADDSS_XMMss_XMMss	vaddss xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VADDSS_XMMdq_XMMdq_MEMd	vaddss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VADDSS_XMMdq_XMMdq_XMMd	vaddss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VADDSS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vaddss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VADDSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vaddss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_ADDSUBPD_XMMpd_MEMpd	vaddsubpd xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_ADDSUBPD_XMMpd_XMMpd	vaddsubpd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VADDSUBPD_XMMdq_XMMdq_MEMdq	vaddsubpd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VADDSUBPD_XMMdq_XMMdq_XMMdq	vaddsubpd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VADDSUBPD_YMMqq_YMMqq_MEMqq	vaddsubpd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VADDSUBPD_YMMqq_YMMqq_YMMqq	vaddsubpd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_ADDSUBPS_XMMps_MEMps	vaddsubps xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_ADDSUBPS_XMMps_XMMps	vaddsubps xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VADDSUBPS_XMMdq_XMMdq_MEMdq	vaddsubps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VADDSUBPS_XMMdq_XMMdq_XMMdq	vaddsubps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VADDSUBPS_YMMqq_YMMqq_MEMqq	vaddsubps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VADDSUBPS_YMMqq_YMMqq_YMMqq	vaddsubps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_AESDEC_XMMdq_MEMdq	vaesdec xmm1, xmm1, [rdi]	10	1
XED_IFORM_AESDEC_XMMdq_XMMdq	vaesdec xmm1, xmm1, xmm2	4	1
XED_IFORM_VAESDEC_XMMdq_XMMdq_MEMdq	vaesdec xmm1, xmm2, [rdi]	10	1
XED_IFORM_VAESDEC_XMMdq_XMMdq_XMMdq	vaesdec xmm1, xmm2, xmm3	4	1
XED_IFORM_AESDECLAST_XMMdq_MEMdq	vaesdeclast xmm1, xmm1, [rdi]	10	1
XED_IFORM_AESDECLAST_XMMdq_XMMdq	vaesdeclast xmm1, xmm1, xmm2	4	1
XED_IFORM_VAESDECLAST_XMMdq_XMMdq_MEMdq	vaesdeclast xmm1, xmm2, [rdi]	10	1
XED_IFORM_VAESDECLAST_XMMdq_XMMdq_XMMdq	vaesdeclast xmm1, xmm2, xmm3	4	1
XED_IFORM_AESENC_XMMdq_MEMdq	vaesenc xmm1, xmm1, [rdi]	10	1
XED_IFORM_AESENC_XMMdq_XMMdq	vaesenc xmm1, xmm1, xmm2	4	1
XED_IFORM_VAESENC_XMMdq_XMMdq_MEMdq	vaesenc xmm1, xmm2, [rdi]	10	1
XED_IFORM_VAESENC_XMMdq_XMMdq_XMMdq	vaesenc xmm1, xmm2, xmm3	4	1
XED_IFORM_AESENCLAST_XMMdq_MEMdq	vaesenclast xmm1, xmm1, [rdi]	10	1
XED_IFORM_AESENCLAST_XMMdq_XMMdq	vaesenclast xmm1, xmm1, xmm2	4	1
XED_IFORM_VAESENCLAST_XMMdq_XMMdq_MEMdq	vaesenclast xmm1, xmm2, [rdi]	10	1
XED_IFORM_VAESENCLAST_XMMdq_XMMdq_XMMdq	vaesenclast xmm1, xmm2, xmm3	4	1
XED_IFORM_AESIMC_XMMdq_MEMdq	vaesimc xmm1, [rdi]	14	2
XED_IFORM_VAESIMC_XMMdq_MEMdq	vaesimc xmm1, [rdi]	14	2
XED_IFORM_VAESIMC_XMMdq_XMMdq	vaesimc xmm1, xmm2	8	2
XED_IFORM_AESIMC_XMMdq_XMMdq	vaesimc xmm1, xmm2	8	2
XED_IFORM_VAESKEYGENASSIST_XMMdq_MEMdq_IMMb	vaeskeygenassist xmm1, [rdi], 1	25	6
XED_IFORM_AESKEYGENASSIST_XMMdq_MEMdq_IMMb	vaeskeygenassist xmm1, [rdi], 1	25	6
XED_IFORM_VALIGND_XMMu32_MASKmskw_XMMu32_MEMu32_IMM8_AVX512	valignd xmm1{k1}, xmm2, [rdi], 1	9	1
XED_IFORM_VALIGND_XMMu32_MASKmskw_XMMu32_XMMu32_IMM8_AVX512	valignd xmm1{k1}, xmm2, xmm3, 1	3	1

XED_IFORM_VALIGND_YMMu32_MASKmskw_YMMu32_MEMu32_IMM8_AVX512	valignd ymm1{k1}, ymm2, [rdi], 1	3	1
XED_IFORM_VALIGND_YMMu32_MASKmskw_YMMu32_YMMu32_IMM8_AVX512	valignd ymm1{k1}, ymm2, ymm3, 1	3	1
XED_IFORM_VALIGND_ZMMu32_MASKmskw_ZMMu32_MEMu32_IMM8_AVX512	valignd zmm1{k1}, zmm2, [rdi], 1	10	1
XED_IFORM_VALIGND_ZMMu32_MASKmskw_ZMMu32_ZMMu32_IMM8_AVX512	valignd zmm1{k1}, zmm2, zmm3, 1	3	1
XED_IFORM_VALIGNQ_XMMu64_MASKmskw_XMMu64_MEMu64_IMM8_AVX512	valignq xmm1{k1}, xmm2, [rdi], 1	9	1
XED_IFORM_VALIGNQ_XMMu64_MASKmskw_XMMu64_XMMu64_IMM8_AVX512	valignq xmm1{k1}, xmm2, xmm3, 1	3	1
XED_IFORM_VALIGNQ_YMMu64_MASKmskw_YMMu64_MEMu64_IMM8_AVX512	valignq ymm1{k1}, ymm2, [rdi], 1	3	1
XED_IFORM_VALIGNQ_YMMu64_MASKmskw_YMMu64_YMMu64_IMM8_AVX512	valignq ymm1{k1}, ymm2, ymm3, 1	3	1
XED_IFORM_VALIGNQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_IMM8_AVX512	valignq zmm1{k1}, zmm2, [rdi], 1	10	1
XED_IFORM_VALIGNQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_IMM8_AVX512	valignq zmm1{k1}, zmm2, zmm3, 1	3	1
XED_IFORM_ANDNPD_XMMpd_MEMpd	vandnpd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_ANDNPD_XMMpd_XMMpd	vandnpd xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VANDNPD_XMMdq_XMMdq_MEMdq	vandnpd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VANDNPD_XMMdq_XMMdq_XMMdq	vandnpd xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VANDNPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vandnpd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VANDNPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vandnpd xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VANDNPD_YMMqq_YMMqq_MEMqq	vandnpd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VANDNPD_YMMqq_YMMqq_YMMqq	vandnpd ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VANDNPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vandnpd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VANDNPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vandnpd ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VANDNPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vandnpd zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VANDNPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vandnpd zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_ANDNPS_XMMps_MEMps	vandnps xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_ANDNPS_XMMps_XMMps	vandnps xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VANDNPS_XMMdq_XMMdq_MEMdq	vandnps xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VANDNPS_XMMdq_XMMdq_XMMdq	vandnps xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VANDNPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vandnps xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VANDNPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vandnps xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VANDNPS_YMMqq_YMMqq_MEMqq	vandnps ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VANDNPS_YMMqq_YMMqq_YMMqq	vandnps ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VANDNPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vandnps ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VANDNPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vandnps ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VANDNPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vandnps zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VANDNPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vandnps zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_ANDPD_XMMpd_MEMpd	vandpd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_ANDPD_XMMpd_XMMpd	vandpd xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VANDPD_XMMdq_XMMdq_MEMdq	vandpd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VANDPD_XMMdq_XMMdq_XMMdq	vandpd xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VANDPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vandpd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VANDPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vandpd xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VANDPD_YMMqq_YMMqq_MEMqq	vandpd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VANDPD_YMMqq_YMMqq_YMMqq	vandpd ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VANDPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vandpd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VANDPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vandpd ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VANDPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vandpd zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VANDPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vandpd zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_ANDPS_XMMps_MEMps	vandps xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_ANDPS_XMMps_XMMps	vandps xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VANDPS_XMMdq_XMMdq_MEMdq	vandps xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VANDPS_XMMdq_XMMdq_XMMdq	vandps xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VANDPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vandps xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VANDPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vandps xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VANDPS_YMMqq_YMMqq_MEMqq	vandps ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VANDPS_YMMqq_YMMqq_YMMqq	vandps ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VANDPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vandps ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VANDPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vandps ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VANDPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vandps zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VANDPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vandps zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VBLENDMPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vblendmpd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VBLENDMPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vblendmpd xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VBLENDMPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vblendmpd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VBLENDMPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vblendmpd ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VBLENDMPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vblendmpd zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VBLENDMPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vblendmpd zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VBLENDMPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vblendmps xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VBLENDMPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vblendmps xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VBLENDMPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vblendmps ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VBLENDMPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vblendmps ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VBLENDMPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vblendmps zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VBLENDMPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vblendmps zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_BLENDPD_XMMdq_MEMdq_IMMb	vblendpd xmm1, xmm1, [rdi], 1	7	0.5
XED_IFORM_BLENDPD_XMMdq_XMMdq_IMMb	vblendpd xmm1, xmm1, xmm2, 1	1	0.33
XED_IFORM_VBLENDPD_XMMdq_XMMdq_MEMdq_IMMb	vblendpd xmm1, xmm2, [rdi], 1	7	0.5
XED_IFORM_VBLENDPD_XMMdq_XMMdq_XMMdq_IMMb	vblendpd xmm1, xmm2, xmm3, 1	1	0.33
XED_IFORM_VBLENDPD_YMMqq_YMMqq_MEMqq_IMMb	vblendpd ymm1, ymm2, [rdi], 1	1	0.5
XED_IFORM_VBLENDPD_YMMqq_YMMqq_YMMqq_IMMb	vblendpd ymm1, ymm2, ymm3, 1	1	0.33
XED_IFORM_BLENDPS_XMMdq_MEMdq_IMMb	vblendps xmm1, xmm1, [rdi], 1	7	0.5
XED_IFORM_BLENDPS_XMMdq_XMMdq_IMMb	vblendps xmm1, xmm1, xmm2, 1	1	0.33
XED_IFORM_VBLENDPS_XMMdq_XMMdq_MEMdq_IMMb	vblendps xmm1, xmm2, [rdi], 1	7	0.5

XED_IFORM_VBLENDPS_XMMdq_XMMdq_XMMdq_IMMb	vblendps xmm1, xmm2, xmm3, 1	1	0.33
XED_IFORM_VBLENDPS_YMMqq_YMMqq_MEMqq_IMMb	vblendps ymm1, ymm2, [rdi], 1	1	0.5
XED_IFORM_VBLENDPS_YMMqq_YMMqq_YMMqq_IMMb	vblendps ymm1, ymm2, ymm3, 1	1	0.33
XED_IFORM_BLENDVPD_XMMdq_MEMdq	vblendvpd xmm1, xmm1, [rdi], xmm0	8	0.66
XED_IFORM_BLENDVPD_XMMdq_XMMdq	vblendvpd xmm1, xmm1, xmm2, xmm0	2	0.66
XED_IFORM_VBLENDVPD_XMMdq_XMMdq_MEMdq_XMMdq	vblendvpd xmm1, xmm2, [rdi], xmm3	8	0.66
XED_IFORM_VBLENDVPD_XMMdq_XMMdq_XMMdq_XMMdq	vblendvpd xmm1, xmm2, xmm3, xmm4	2	0.66
XED_IFORM_VBLENDVPD_YMMqq_YMMqq_MEMqq_YMMqq	vblendvpd ymm1, ymm2, [rdi], ymm3	2	0.66
XED_IFORM_VBLENDVPD_YMMqq_YMMqq_YMMqq_YMMqq	vblendvpd ymm1, ymm2, ymm3, ymm4	2	0.66
XED_IFORM_BLENDVPS_XMMdq_MEMdq	vblendvps xmm1, xmm1, [rdi], xmm0	8	0.66
XED_IFORM_BLENDVPS_XMMdq_XMMdq	vblendvps xmm1, xmm1, xmm2, xmm0	2	0.66
XED_IFORM_VBLENDVPS_XMMdq_XMMdq_MEMdq_XMMdq	vblendvps xmm1, xmm2, [rdi], xmm3	8	0.66
XED_IFORM_VBLENDVPS_XMMdq_XMMdq_XMMdq_XMMdq	vblendvps xmm1, xmm2, xmm3, xmm4	2	0.66
XED_IFORM_VBLENDVPS_YMMqq_YMMqq_MEMqq_YMMqq	vblendvps ymm1, ymm2, [rdi], ymm3	2	0.66
XED_IFORM_VBLENDVPS_YMMqq_YMMqq_YMMqq_YMMqq	vblendvps ymm1, ymm2, ymm3, ymm4	2	0.66
XED_IFORM_VBROADCASTF128_YMMqq_MEMdq	vbroadcastf128 ymm1, [rdi]	0	0.5
XED_IFORM_VBROADCASTF32X2_YMMf32_MASKmskw_MEMf32_AVX512	vbroadcastf32x2 ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VBROADCASTF32X2_YMMf32_MASKmskw_XMMf32_AVX512	vbroadcastf32x2 ymm1{k1}, xmm2	3	1
XED_IFORM_VBROADCASTF32X2_ZMMf32_MASKmskw_MEMf32_AVX512	vbroadcastf32x2 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VBROADCASTF32X2_ZMMf32_MASKmskw_XMMf32_AVX512	vbroadcastf32x2 zmm1{k1}, xmm2	3	1
XED_IFORM_VBROADCASTF32X4_YMMf32_MASKmskw_MEMf32_AVX512	vbroadcastf32x4 ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VBROADCASTF32X4_ZMMf32_MASKmskw_MEMf32_AVX512	vbroadcastf32x4 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VBROADCASTF32X8_ZMMf32_MASKmskw_MEMf32_AVX512	vbroadcastf32x8 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VBROADCASTF64X2_YMMf64_MASKmskw_MEMf64_AVX512	vbroadcastf64x2 ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VBROADCASTF64X2_ZMMf64_MASKmskw_MEMf64_AVX512	vbroadcastf64x2 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VBROADCASTF64X4_ZMMf64_MASKmskw_MEMf64_AVX512	vbroadcastf64x4 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VBROADCASTI128_YMMqq_MEMdq	vbroadcasti128 ymm1, [rdi]	0	0.5
XED_IFORM_VBROADCASTI32X2_XMMu32_MASKmskw_MEMu32_AVX512	vbroadcasti32x2 xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VBROADCASTI32X2_XMMu32_MASKmskw_XMMu32_AVX512	vbroadcasti32x2 xmm1{k1}, xmm2	1	1
XED_IFORM_VBROADCASTI32X2_YMMu32_MASKmskw_MEMu32_AVX512	vbroadcasti32x2 ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VBROADCASTI32X2_YMMu32_MASKmskw_XMMu32_AVX512	vbroadcasti32x2 ymm1{k1}, xmm2	3	1
XED_IFORM_VBROADCASTI32X2_ZMMu32_MASKmskw_MEMu32_AVX512	vbroadcasti32x2 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VBROADCASTI32X2_ZMMu32_MASKmskw_XMMu32_AVX512	vbroadcasti32x2 zmm1{k1}, xmm2	3	1
XED_IFORM_VBROADCASTI32X4_YMMu32_MASKmskw_MEMu32_AVX512	vbroadcasti32x4 ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VBROADCASTI32X4_ZMMu32_MASKmskw_MEMu32_AVX512	vbroadcasti32x4 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VBROADCASTI32X8_ZMMu32_MASKmskw_MEMu32_AVX512	vbroadcasti32x8 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VBROADCASTI64X2_YMMu64_MASKmskw_MEMu64_AVX512	vbroadcasti64x2 ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VBROADCASTI64X2_ZMMu64_MASKmskw_MEMu64_AVX512	vbroadcasti64x2 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VBROADCASTI64X4_ZMMu64_MASKmskw_MEMu64_AVX512	vbroadcasti64x4 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VBROADCASTSD_YMMqq_MEMq	vbroadcastsd ymm1, [rdi]	0	0.5
XED_IFORM_VBROADCASTSD_YMMqq_XMMdq	vbroadcastsd ymm1, xmm2	3	1
XED_IFORM_VBROADCASTSD_YMMf64_MASKmskw_MEMf64_AVX512	vbroadcastsd ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VBROADCASTSD_YMMf64_MASKmskw_XMMf64_AVX512	vbroadcastsd ymm1{k1}, xmm2	3	1
XED_IFORM_VBROADCASTSD_ZMMf64_MASKmskw_MEMf64_AVX512	vbroadcastsd zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VBROADCASTSD_ZMMf64_MASKmskw_XMMf64_AVX512	vbroadcastsd zmm1{k1}, xmm2	3	1
XED_IFORM_VBROADCASTSS_XMMdq_MEMd	vbroadcastss xmm1, [rdi]	6	0.5
XED_IFORM_VBROADCASTSS_XMMdq_XMMdq	vbroadcastss xmm1, xmm2	1	1
XED_IFORM_VBROADCASTSS_XMMf32_MASKmskw_MEMf32_AVX512	vbroadcastss xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VBROADCASTSS_XMMf32_MASKmskw_XMMf32_AVX512	vbroadcastss xmm1{k1}, xmm2	3	1
XED_IFORM_VBROADCASTSS_YMMqq_MEMd	vbroadcastss ymm1, [rdi]	0	0.5
XED_IFORM_VBROADCASTSS_YMMqq_XMMdq	vbroadcastss ymm1, xmm2	3	1
XED_IFORM_VBROADCASTSS_YMMf32_MASKmskw_MEMf32_AVX512	vbroadcastss ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VBROADCASTSS_YMMf32_MASKmskw_XMMf32_AVX512	vbroadcastss ymm1{k1}, xmm2	3	1
XED_IFORM_VBROADCASTSS_ZMMf32_MASKmskw_MEMf32_AVX512	vbroadcastss zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VBROADCASTSS_ZMMf32_MASKmskw_XMMf32_AVX512	vbroadcastss zmm1{k1}, xmm2	3	1
XED_IFORM_VCMPPD_MASKmskw_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vcmppd k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VCMPPD_MASKmskw_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vcmppd k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VCMPPD_MASKmskw_MASKmskw_YMMf64_MEMf64_IMM8_AVX512	vcmppd k1{k1}, ymm1, [rdi], 1	3	1
XED_IFORM_VCMPPD_MASKmskw_MASKmskw_YMMf64_YMMf64_IMM8_AVX512	vcmppd k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VCMPPD_MASKmskw_MASKmskw_ZMMf64_MEMf64_IMM8_AVX512	vcmppd k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VCMPPD_MASKmskw_MASKmskw_ZMMf64_ZMMf64_IMM8_AVX512	vcmppd k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_CMPPD_XMMpd_MEMpd_IMMb	vcmppd xmm1, xmm1, [rdi], 1	10	0.5
XED_IFORM_CMPPD_XMMpd_XMMpd_IMMb	vcmppd xmm1, xmm1, xmm2, 1	4	0.5
XED_IFORM_VCMPPD_XMMdq_XMMdq_MEMdq_IMMb	vcmppd xmm1, xmm2, [rdi], 1	10	0.5
XED_IFORM_VCMPPD_XMMdq_XMMdq_XMMdq_IMMb	vcmppd xmm1, xmm2, xmm3, 1	4	0.5
XED_IFORM_VCMPPD_YMMqq_YMMqq_MEMqq_IMMb	vcmppd ymm1, ymm2, [rdi], 1	4	0.5
XED_IFORM_VCMPPD_YMMqq_YMMqq_YMMqq_IMMb	vcmppd ymm1, ymm2, ymm3, 1	4	0.5
XED_IFORM_VCMPPS_MASKmskw_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vcmpps k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VCMPPS_MASKmskw_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vcmpps k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VCMPPS_MASKmskw_MASKmskw_YMMf32_MEMf32_IMM8_AVX512	vcmpps k1{k1}, ymm1, [rdi], 1	3	1
XED_IFORM_VCMPPS_MASKmskw_MASKmskw_YMMf32_YMMf32_IMM8_AVX512	vcmpps k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VCMPPS_MASKmskw_MASKmskw_ZMMf32_MEMf32_IMM8_AVX512	vcmpps k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VCMPPS_MASKmskw_MASKmskw_ZMMf32_ZMMf32_IMM8_AVX512	vcmpps k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_CMPPS_XMMps_MEMps_IMMb	vcmpps xmm1, xmm1, [rdi], 1	10	0.5
XED_IFORM_CMPPS_XMMps_XMMps_IMMb	vcmpps xmm1, xmm1, xmm2, 1	4	0.5
XED_IFORM_VCMPPS_XMMdq_XMMdq_MEMdq_IMMb	vcmpps xmm1, xmm2, [rdi], 1	10	0.5
XED_IFORM_VCMPPS_XMMdq_XMMdq_XMMdq_IMMb	vcmpps xmm1, xmm2, xmm3, 1	4	0.5
XED_IFORM_VCMPPS_YMMqq_YMMqq_MEMqq_IMMb	vcmpps ymm1, ymm2, [rdi], 1	4	0.5
XED_IFORM_VCMPPS_YMMqq_YMMqq_YMMqq_IMMb	vcmpps ymm1, ymm2, ymm3, 1	4	0.5

XED_IFORM_VCMPSD_MASKmskw_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vcmpsd k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VCMPSD_MASKmskw_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vcmpsd k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_CMPSD_XMM_XMMsd_MEMsd_IMMb	vcmpsd xmm1, xmm1, [rdi], 1	9	0.5
XED_IFORM_CMPSD_XMM_XMMsd_XMMsd_IMMb	vcmpsd xmm1, xmm1, xmm2, 1	4	0.5
XED_IFORM_VCMPSD_XMMdq_XMMdq_MEMq_IMMb	vcmpsd xmm1, xmm2, [rdi], 1	9	0.5
XED_IFORM_VCMPSD_XMMdq_XMMdq_XMMq_IMMb	vcmpsd xmm1, xmm2, xmm3, 1	4	0.5
XED_IFORM_VCMPSS_MASKmskw_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vcmpss k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VCMPSS_MASKmskw_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vcmpss k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_CMPSS_XMMss_MEMss_IMMb	vcmpss xmm1, xmm1, [rdi], 1	9	0.5
XED_IFORM_CMPSS_XMMss_XMMss_IMMb	vcmpss xmm1, xmm1, xmm2, 1	4	0.5
XED_IFORM_VCMPSS_XMMdq_XMMdq_MEMd_IMMb	vcmpss xmm1, xmm2, [rdi], 1	9	0.5
XED_IFORM_VCMPSS_XMMdq_XMMdq_XMMd_IMMb	vcmpss xmm1, xmm2, xmm3, 1	4	0.5
XED_IFORM_VCOMISD_XMMf64_MEMf64_AVX512	vcomisd xmm1, [rdi]	7	1
XED_IFORM_COMISD_XMMsd_MEMsd	vcomisd xmm1, [rdi]	7	1
XED_IFORM_VCOMISD_XMMq_MEMq	vcomisd xmm1, [rdi]	7	1
XED_IFORM_VCOMISD_XMMq_XMMq	vcomisd xmm1, xmm2	2	1
XED_IFORM_COMISD_XMMsd_XMMsd	vcomisd xmm1, xmm2	2	1
XED_IFORM_VCOMISD_XMMf64_XMMf64_AVX512	vcomisd xmm1, xmm2	2	1
XED_IFORM_COMISS_XMMss_MEMss	vcomiss xmm1, [rdi]	7	1
XED_IFORM_VCOMISS_XMMd_MEMd	vcomiss xmm1, [rdi]	7	1
XED_IFORM_VCOMISS_XMMf32_MEMf32_AVX512	vcomiss xmm1, [rdi]	7	1
XED_IFORM_VCOMISS_XMMd_XMMd	vcomiss xmm1, xmm2	2	1
XED_IFORM_VCOMISS_XMMf32_XMMf32_AVX512	vcomiss xmm1, xmm2	2	1
XED_IFORM_COMISS_XMMss_XMMss	vcomiss xmm1, xmm2	2	1
XED_IFORM_VCOMPRESSPD_MEMf64_MASKmskw_XMMf64_AVX512	vcompresspd [rdi]{k1}, xmm1	11	2
XED_IFORM_VCOMPRESSPD_MEMf64_MASKmskw_YMMf64_AVX512	vcompresspd [rdi]{k1}, ymm1	11	2
XED_IFORM_VCOMPRESSPD_MEMf64_MASKmskw_ZMMf64_AVX512	vcompresspd [rdi]{k1}, zmm1	11	2
XED_IFORM_VCOMPRESSPD_XMMf64_MASKmskw_XMMf64_AVX512	vcompresspd xmm1{k1}, xmm2	6	2
XED_IFORM_VCOMPRESSPD_YMMf64_MASKmskw_YMMf64_AVX512	vcompresspd ymm1{k1}, ymm2	6	2
XED_IFORM_VCOMPRESSPD_ZMMf64_MASKmskw_ZMMf64_AVX512	vcompresspd zmm1{k1}, zmm2	6	2
XED_IFORM_VCOMPRESSPS_MEMf32_MASKmskw_XMMf32_AVX512	vcompressps [rdi]{k1}, xmm1	11	2
XED_IFORM_VCOMPRESSPS_MEMf32_MASKmskw_YMMf32_AVX512	vcompressps [rdi]{k1}, ymm1	11	2
XED_IFORM_VCOMPRESSPS_MEMf32_MASKmskw_ZMMf32_AVX512	vcompressps [rdi]{k1}, zmm1	11	2
XED_IFORM_VCOMPRESSPS_XMMf32_MASKmskw_XMMf32_AVX512	vcompressps xmm1{k1}, xmm2	6	2
XED_IFORM_VCOMPRESSPS_YMMf32_MASKmskw_YMMf32_AVX512	vcompressps ymm1{k1}, ymm2	6	2
XED_IFORM_VCOMPRESSPS_ZMMf32_MASKmskw_ZMMf32_AVX512	vcompressps zmm1{k1}, zmm2	6	2
XED_IFORM_CVTDQ2PD_XMMpd_MEMq	vcvtdq2pd xmm1, [rdi]	11	1
XED_IFORM_VCVTDQ2PD_XMMdq_MEMq	vcvtdq2pd xmm1, [rdi]	11	1
XED_IFORM_VCVTDQ2PD_XMMdq_XMMq	vcvtdq2pd xmm1, xmm2	5	1
XED_IFORM_CVTDQ2PD_XMMpd_XMMq	vcvtdq2pd xmm1, xmm2	5	1
XED_IFORM_VCVTDQ2PD_XMMf64_MASKmskw_MEMi32_AVX512	vcvtdq2pd xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTDQ2PD_XMMf64_MASKmskw_XMMi32_AVX512	vcvtdq2pd xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTDQ2PD_YMMqq_MEMdq	vcvtdq2pd ymm1, [rdi]	13	1
XED_IFORM_VCVTDQ2PD_YMMqq_XMMdq	vcvtdq2pd ymm1, xmm2	7	1
XED_IFORM_VCVTDQ2PD_YMMf64_MASKmskw_MEMi32_AVX512	vcvtdq2pd ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTDQ2PD_YMMf64_MASKmskw_XMMi32_AVX512	vcvtdq2pd ymm1{k1}, xmm2	7	1
XED_IFORM_VCVTDQ2PD_ZMMf64_MASKmskw_MEMi32_AVX512	vcvtdq2pd zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTDQ2PD_ZMMf64_MASKmskw_YMMi32_AVX512	vcvtdq2pd zmm1{k1}, ymm2	7	1
XED_IFORM_VCVTDQ2PS_XMMdq_MEMdq	vcvtdq2ps xmm1, [rdi]	10	0.5
XED_IFORM_CVTDQ2PS_XMMps_MEMdq	vcvtdq2ps xmm1, [rdi]	10	0.5
XED_IFORM_CVTDQ2PS_XMMps_XMMdq	vcvtdq2ps xmm1, xmm2	4	0.5
XED_IFORM_VCVTDQ2PS_XMMdq_XMMdq	vcvtdq2ps xmm1, xmm2	4	0.5
XED_IFORM_VCVTDQ2PS_XMMf32_MASKmskw_MEMi32_AVX512	vcvtdq2ps xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTDQ2PS_XMMf32_MASKmskw_XMMi32_AVX512	vcvtdq2ps xmm1{k1}, xmm2	4	0.5
XED_IFORM_VCVTDQ2PS_YMMqq_MEMqq	vcvtdq2ps ymm1, [rdi]	4	0.5
XED_IFORM_VCVTDQ2PS_YMMqq_YMMqq	vcvtdq2ps ymm1, ymm2	4	0.5
XED_IFORM_VCVTDQ2PS_YMMf32_MASKmskw_MEMi32_AVX512	vcvtdq2ps ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTDQ2PS_YMMf32_MASKmskw_YMMi32_AVX512	vcvtdq2ps ymm1{k1}, ymm2	4	0.5
XED_IFORM_VCVTDQ2PS_ZMMf32_MASKmskw_MEMi32_AVX512	vcvtdq2ps zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTDQ2PS_ZMMf32_MASKmskw_ZMMi32_AVX512	vcvtdq2ps zmm1{k1}, zmm2	4	0.5
XED_IFORM_CVTPD2DQ_XMMdq_MEMpd	vcvtpd2dq xmm1, [rdi]	11	0
XED_IFORM_CVTPD2DQ_XMMdq_XMMpd	vcvtpd2dq xmm1, xmm2	5	1
XED_IFORM_VCVTPD2DQ_XMMdq_XMMdq	vcvtpd2dq xmm1, xmm2	5	1
XED_IFORM_VCVTPD2DQ_XMMdq_YMMqq	vcvtpd2dq xmm1, ymm2	7	1
XED_IFORM_VCVTPD2DQ_XMMi32_MASKmskw_XMMf64_AVX512_VL128	vcvtpd2dq xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTPD2DQ_XMMi32_MASKmskw_YMMf64_AVX512_VL256	vcvtpd2dq xmm1{k1}, ymm2	7	1
XED_IFORM_VCVTPD2DQ_YMMi32_MASKmskw_MEMf64_AVX512_VL512	vcvtpd2dq ymm1{k1}, [rdi]	14	1
XED_IFORM_VCVTPD2DQ_YMMi32_MASKmskw_ZMMf64_AVX512_VL512	vcvtpd2dq ymm1{k1}, zmm2	7	1
XED_IFORM_CVTPD2PS_XMMps_MEMpd	vcvtpd2ps xmm1, [rdi]	11	0
XED_IFORM_VCVTPD2PS_XMMdq_XMMdq	vcvtpd2ps xmm1, xmm2	5	1
XED_IFORM_CVTPD2PS_XMMps_XMMpd	vcvtpd2ps xmm1, xmm2	5	1
XED_IFORM_VCVTPD2PS_XMMdq_YMMqq	vcvtpd2ps xmm1, ymm2	7	1
XED_IFORM_VCVTPD2PS_XMMf32_MASKmskw_XMMf64_AVX512_VL128	vcvtpd2ps xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTPD2PS_XMMf32_MASKmskw_YMMf64_AVX512_VL256	vcvtpd2ps xmm1{k1}, ymm2	7	1
XED_IFORM_VCVTPD2PS_YMMf32_MASKmskw_MEMf64_AVX512_VL512	vcvtpd2ps ymm1{k1}, [rdi]	14	1
XED_IFORM_VCVTPD2PS_YMMf32_MASKmskw_ZMMf64_AVX512_VL512	vcvtpd2ps ymm1{k1}, zmm2	7	1
XED_IFORM_VCVTPD2QQ_XMMi64_MASKmskw_MEMf64_AVX512	vcvtpd2qq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTPD2QQ_XMMi64_MASKmskw_XMMf64_AVX512	vcvtpd2qq xmm1{k1}, xmm2	4	0.5
XED_IFORM_VCVTPD2QQ_YMMi64_MASKmskw_MEMf64_AVX512	vcvtpd2qq ymm1{k1}, [rdi]	4	0.5

XED_IFORM_VCVTPD2QQ_YMMi64_MASKmskw_YMMf64_AVX512	vcvtpd2qq ymm1{k1}, ymm2	4	0.5
XED_IFORM_VCVTPD2QQ_ZMMi64_MASKmskw_MEMf64_AVX512	vcvtpd2qq zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTPD2QQ_ZMMi64_MASKmskw_ZMMf64_AVX512	vcvtpd2qq zmm1{k1}, zmm2	4	0.5
XED_IFORM_VCVTPD2UDQ_XMMu32_MASKmskw_XMMf64_AVX512_VL128	vcvtpd2udq xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTPD2UDQ_XMMu32_MASKmskw_YMMf64_AVX512_VL256	vcvtpd2udq xmm1{k1}, ymm2	7	1
XED_IFORM_VCVTPD2UDQ_YMMu32_MASKmskw_MEMf64_AVX512_VL512	vcvtpd2udq ymm1{k1}, [rdi]	14	1
XED_IFORM_VCVTPD2UDQ_YMMu32_MASKmskw_ZMMf64_AVX512_VL512	vcvtpd2udq ymm1{k1}, zmm2	7	1
XED_IFORM_VCVTPD2UQQ_XMMu64_MASKmskw_MEMf64_AVX512	vcvtpd2uqq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTPD2UQQ_XMMu64_MASKmskw_XMMf64_AVX512	vcvtpd2uqq xmm1{k1}, xmm2	4	0.5
XED_IFORM_VCVTPD2UQQ_YMMu64_MASKmskw_MEMf64_AVX512	vcvtpd2uqq ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTPD2UQQ_YMMu64_MASKmskw_YMMf64_AVX512	vcvtpd2uqq ymm1{k1}, ymm2	4	0.5
XED_IFORM_VCVTPD2UQQ_ZMMu64_MASKmskw_MEMf64_AVX512	vcvtpd2uqq zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTPD2UQQ_ZMMu64_MASKmskw_ZMMf64_AVX512	vcvtpd2uqq zmm1{k1}, zmm2	4	0.5
XED_IFORM_VCVTPH2PS_XMMdq_MEMq	vcvtph2ps xmm1, [rdi]	9	0.5
XED_IFORM_VCVTPH2PS_XMMdq_XMMq	vcvtph2ps xmm1, xmm2	5	1
XED_IFORM_VCVTPH2PS_XMMf32_MASKmskw_MEMf16_AVX512	vcvtph2ps xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTPH2PS_XMMf32_MASKmskw_XMMf16_AVX512	vcvtph2ps xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTPH2PS_YMMqq_MEMdq	vcvtph2ps ymm1, [rdi]	10	0.5
XED_IFORM_VCVTPH2PS_YMMqq_XMMdq	vcvtph2ps ymm1, xmm2	7	1
XED_IFORM_VCVTPH2PS_YMMf32_MASKmskw_MEMf16_AVX512	vcvtph2ps ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTPH2PS_YMMf32_MASKmskw_XMMf16_AVX512	vcvtph2ps ymm1{k1}, xmm2	7	1
XED_IFORM_VCVTPH2PS_ZMMf32_MASKmskw_MEMf16_AVX512	vcvtph2ps zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTPH2PS_ZMMf32_MASKmskw_YMMf16_AVX512	vcvtph2ps zmm1{k1}, ymm2	7	1
XED_IFORM_VCVTPS2DQ_XMMdq_MEMdq	vcvtps2dq xmm1, [rdi]	10	0.5
XED_IFORM_CVTPS2DQ_XMMdq_MEMps	vcvtps2dq xmm1, [rdi]	10	0.5
XED_IFORM_CVTPS2DQ_XMMdq_XMMps	vcvtps2dq xmm1, xmm2	4	0.5
XED_IFORM_VCVTPS2DQ_XMMdq_XMMdq	vcvtps2dq xmm1, xmm2	4	0.5
XED_IFORM_VCVTPS2DQ_XMMi32_MASKmskw_MEMf32_AVX512	vcvtps2dq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTPS2DQ_XMMi32_MASKmskw_XMMf32_AVX512	vcvtps2dq xmm1{k1}, xmm2	4	0.5
XED_IFORM_VCVTPS2DQ_YMMqq_MEMqq	vcvtps2dq ymm1, [rdi]	4	0.5
XED_IFORM_VCVTPS2DQ_YMMqq_YMMqq	vcvtps2dq ymm1, ymm2	4	0.5
XED_IFORM_VCVTPS2DQ_YMMi32_MASKmskw_MEMf32_AVX512	vcvtps2dq ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTPS2DQ_YMMi32_MASKmskw_YMMf32_AVX512	vcvtps2dq ymm1{k1}, ymm2	4	0.5
XED_IFORM_VCVTPS2DQ_ZMMi32_MASKmskw_MEMf32_AVX512	vcvtps2dq zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTPS2DQ_ZMMi32_MASKmskw_ZMMf32_AVX512	vcvtps2dq zmm1{k1}, zmm2	4	0.5
XED_IFORM_VCVTPS2PD_XMMdq_MEMq	vcvtps2pd xmm1, [rdi]	9	0.5
XED_IFORM_CVTPS2PD_XMMpd_MEMq	vcvtps2pd xmm1, [rdi]	9	0.5
XED_IFORM_VCVTPS2PD_XMMdq_XMMq	vcvtps2pd xmm1, xmm2	5	1
XED_IFORM_CVTPS2PD_XMMpd_XMMq	vcvtps2pd xmm1, xmm2	5	1
XED_IFORM_VCVTPS2PD_XMMf64_MASKmskw_MEMf32_AVX512	vcvtps2pd xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTPS2PD_XMMf64_MASKmskw_XMMf32_AVX512	vcvtps2pd xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTPS2PD_YMMqq_MEMdq	vcvtps2pd ymm1, [rdi]	4	0.5
XED_IFORM_VCVTPS2PD_YMMqq_XMMdq	vcvtps2pd ymm1, xmm2	7	1
XED_IFORM_VCVTPS2PD_YMMf64_MASKmskw_MEMf32_AVX512	vcvtps2pd ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTPS2PD_YMMf64_MASKmskw_XMMf32_AVX512	vcvtps2pd ymm1{k1}, xmm2	7	1
XED_IFORM_VCVTPS2PD_ZMMf64_MASKmskw_MEMf32_AVX512	vcvtps2pd zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTPS2PD_ZMMf64_MASKmskw_YMMf32_AVX512	vcvtps2pd zmm1{k1}, ymm2	7	1
XED_IFORM_VCVTPS2PH_MEMq_XMMdq_IMMb	vcvtps2ph [rdi], xmm1, 1	10	1
XED_IFORM_VCVTPS2PH_MEMdq_YMMqq_IMMb	vcvtps2ph [rdi], ymm1, 1	12	1
XED_IFORM_VCVTPS2PH_MEMf16_MASKmskw_XMMf32_IMM8_AVX512	vcvtps2ph [rdi]{k1}, xmm1, 1	9	1
XED_IFORM_VCVTPS2PH_MEMf16_MASKmskw_YMMf32_IMM8_AVX512	vcvtps2ph [rdi]{k1}, ymm1, 1	9	1
XED_IFORM_VCVTPS2PH_MEMf16_MASKmskw_ZMMf32_IMM8_AVX512	vcvtps2ph [rdi]{k1}, zmm1, 1	9	1
XED_IFORM_VCVTPS2PH_XMMq_XMMdq_IMMb	vcvtps2ph xmm1, xmm2, 1	5	1
XED_IFORM_VCVTPS2PH_XMMdq_YMMqq_IMMb	vcvtps2ph xmm1, ymm2, 1	7	1
XED_IFORM_VCVTPS2PH_XMMf16_MASKmskw_XMMf32_IMM8_AVX512	vcvtps2ph xmm1{k1}, xmm2, 1	5	1
XED_IFORM_VCVTPS2PH_XMMf16_MASKmskw_YMMf32_IMM8_AVX512	vcvtps2ph xmm1{k1}, ymm2, 1	7	1
XED_IFORM_VCVTPS2PH_YMMf16_MASKmskw_ZMMf32_IMM8_AVX512	vcvtps2ph ymm1{k1}, zmm2, 1	7	1
XED_IFORM_VCVTPS2QQ_XMMi64_MASKmskw_MEMf32_AVX512	vcvtps2qq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTPS2QQ_XMMi64_MASKmskw_XMMf32_AVX512	vcvtps2qq xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTPS2QQ_YMMi64_MASKmskw_MEMf32_AVX512	vcvtps2qq ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTPS2QQ_YMMi64_MASKmskw_XMMf32_AVX512	vcvtps2qq ymm1{k1}, xmm2	7	1
XED_IFORM_VCVTPS2QQ_ZMMi64_MASKmskw_MEMf32_AVX512	vcvtps2qq zmm1{k1}, [rdi]	12	1
XED_IFORM_VCVTPS2QQ_ZMMi64_MASKmskw_YMMf32_AVX512	vcvtps2qq zmm1{k1}, ymm2	7	1
XED_IFORM_VCVTPS2UDQ_XMMu32_MASKmskw_MEMf32_AVX512	vcvtps2udq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTPS2UDQ_XMMu32_MASKmskw_XMMf32_AVX512	vcvtps2udq xmm1{k1}, xmm2	4	0.5
XED_IFORM_VCVTPS2UDQ_YMMu32_MASKmskw_MEMf32_AVX512	vcvtps2udq ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTPS2UDQ_YMMu32_MASKmskw_YMMf32_AVX512	vcvtps2udq ymm1{k1}, ymm2	4	0.5
XED_IFORM_VCVTPS2UDQ_ZMMu32_MASKmskw_MEMf32_AVX512	vcvtps2udq zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTPS2UDQ_ZMMu32_MASKmskw_ZMMf32_AVX512	vcvtps2udq zmm1{k1}, zmm2	4	0.5
XED_IFORM_VCVTPS2UQQ_XMMu64_MASKmskw_MEMf32_AVX512	vcvtps2uqq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTPS2UQQ_XMMu64_MASKmskw_XMMf32_AVX512	vcvtps2uqq xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTPS2UQQ_YMMu64_MASKmskw_MEMf32_AVX512	vcvtps2uqq ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTPS2UQQ_YMMu64_MASKmskw_XMMf32_AVX512	vcvtps2uqq ymm1{k1}, xmm2	7	1
XED_IFORM_VCVTPS2UQQ_ZMMu64_MASKmskw_MEMf32_AVX512	vcvtps2uqq zmm1{k1}, [rdi]	12	1
XED_IFORM_VCVTPS2UQQ_ZMMu64_MASKmskw_YMMf32_AVX512	vcvtps2uqq zmm1{k1}, ymm2	7	1
XED_IFORM_VCVTQQ2PD_XMMi64_MASKmskw_MEMf64_AVX512	vcvtqq2pd xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTQQ2PD_XMMi64_MASKmskw_XMMf64_AVX512	vcvtqq2pd xmm1{k1}, xmm2	4	0.5
XED_IFORM_VCVTQQ2PD_YMMi64_MASKmskw_MEMf64_AVX512	vcvtqq2pd ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTQQ2PD_YMMi64_MASKmskw_YMMf64_AVX512	vcvtqq2pd ymm1{k1}, ymm2	4	0.5

XED_IFORM_VCVTQQ2PD_ZMMi64_MASKmskw_MEMf64_AVX512	vcvtqq2pd zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTQQ2PD_ZMMi64_MASKmskw_ZMMf64_AVX512	vcvtqq2pd zmm1{k1}, zmm2	4	0.5
XED_IFORM_VCVTQQ2PS_XMMf32_MASKmskw_XMMu64_AVX512_VL128	vcvtqq2ps xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTQQ2PS_XMMf32_MASKmskw_YMMu64_AVX512_VL256	vcvtqq2ps xmm1{k1}, ymm2	7	1
XED_IFORM_VCVTQQ2PS_YMMf32_MASKmskw_MEMu64_AVX512_VL512	vcvtqq2ps ymm1{k1}, [rdi]	14	1
XED_IFORM_VCVTQQ2PS_YMMf32_MASKmskw_ZMMu64_AVX512_VL512	vcvtqq2ps ymm1{k1}, zmm2	7	1
XED_IFORM_VCVTSD2SI_GPR32d_MEMq	vcvtsd2si eax, [rdi]	7	1
XED_IFORM_VCVTSD2SI_GPR32i32_MEMf64_AVX512	vcvtsd2si eax, [rdi]	7	1
XED_IFORM_VCVTSD2SI_GPR32i32_XMMf64_AVX512	vcvtsd2si eax, xmm1	7	1
XED_IFORM_VCVTSD2SI_GPR32d_XMMq	vcvtsd2si eax, xmm1	7	1
XED_IFORM_CVTSD2SI_GPR32d_XMMsd	vcvtsd2si eax, xmm1	7	1
XED_IFORM_VCVTSD2SI_GPR64q_MEMq	vcvtsd2si rax, [rdi]	7	1
XED_IFORM_VCVTSD2SI_GPR64i64_MEMf64_AVX512	vcvtsd2si rax, [rdi]	7	1
XED_IFORM_VCVTSD2SI_GPR64q_XMMq	vcvtsd2si rax, xmm1	7	1
XED_IFORM_CVTSD2SI_GPR64q_XMMsd	vcvtsd2si rax, xmm1	7	1
XED_IFORM_VCVTSD2SI_GPR64i64_XMMf64_AVX512	vcvtsd2si rax, xmm1	7	1
XED_IFORM_CVTSD2SS_XMMss_MEMsd	vcvtsd2ss xmm1, xmm1, [rdi]	10	1
XED_IFORM_CVTSD2SS_XMMss_XMMsd	vcvtsd2ss xmm1, xmm1, xmm2	5	1
XED_IFORM_VCVTSD2SS_XMMdq_XMMdq_MEMq	vcvtsd2ss xmm1, xmm2, [rdi]	10	1
XED_IFORM_VCVTSD2SS_XMMdq_XMMdq_XMMq	vcvtsd2ss xmm1, xmm2, xmm3	5	1
XED_IFORM_VCVTSD2SS_XMMf32_MASKmskw_XMMf64_MEMf64_AVX512	vcvtsd2ss xmm1{k1}, xmm2, [rdi]	11	1
XED_IFORM_VCVTSD2SS_XMMf32_MASKmskw_XMMf64_XMMf64_AVX512	vcvtsd2ss xmm1{k1}, xmm2, xmm3	5	1
XED_IFORM_VCVTSD2USI_GPR32u32_MEMf64_AVX512	vcvtsd2usi eax, [rdi]	12	1
XED_IFORM_VCVTSD2USI_GPR32u32_XMMf64_AVX512	vcvtsd2usi eax, xmm1	6	1
XED_IFORM_VCVTSD2USI_GPR64u64_MEMf64_AVX512	vcvtsd2usi rax, [rdi]	11	1
XED_IFORM_VCVTSD2USI_GPR64u64_XMMf64_AVX512	vcvtsd2usi rax, xmm1	6	1
XED_IFORM_CVTSI2SD_XMMsd_GPR32d	vcvtsi2sd xmm1, xmm1, eax	7	1
XED_IFORM_CVTSI2SD_XMMsd_GPR64q	vcvtsi2sd xmm1, xmm1, rax	7	1
XED_IFORM_VCVTSI2SD_XMMdq_XMMdq_GPR32d	vcvtsi2sd xmm1, xmm2, eax	7	1
XED_IFORM_VCVTSI2SD_XMMf64_XMMf64_GPR32i32_AVX512	vcvtsi2sd xmm1, xmm2, eax	7	1
XED_IFORM_VCVTSI2SD_XMMdq_XMMdq_GPR64q	vcvtsi2sd xmm1, xmm2, rax	7	1
XED_IFORM_VCVTSI2SD_XMMf64_XMMf64_GPR64i64_AVX512	vcvtsi2sd xmm1, xmm2, rax	7	1
XED_IFORM_CVTSI2SS_XMMss_GPR32d	vcvtsi2ss xmm1, xmm1, eax	7	1
XED_IFORM_CVTSI2SS_XMMss_GPR64q	vcvtsi2ss xmm1, xmm1, rax	7	2
XED_IFORM_VCVTSI2SS_XMMf32_XMMf32_GPR32i32_AVX512	vcvtsi2ss xmm1, xmm2, eax	7	1
XED_IFORM_VCVTSI2SS_XMMdq_XMMdq_GPR32d	vcvtsi2ss xmm1, xmm2, eax	7	1
XED_IFORM_VCVTSI2SS_XMMf32_XMMf32_GPR64i64_AVX512	vcvtsi2ss xmm1, xmm2, rax	7	2
XED_IFORM_VCVTSI2SS_XMMdq_XMMdq_GPR64q	vcvtsi2ss xmm1, xmm2, rax	7	2
XED_IFORM_CVTSS2SD_XMMsd_MEMss	vcvtss2sd xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_CVTSS2SD_XMMsd_XMMss	vcvtss2sd xmm1, xmm1, xmm2	5	1
XED_IFORM_VCVTSS2SD_XMMdq_XMMdq_MEMd	vcvtss2sd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VCVTSS2SD_XMMdq_XMMdq_XMMd	vcvtss2sd xmm1, xmm2, xmm3	5	1
XED_IFORM_VCVTSS2SD_XMMf64_MASKmskw_XMMf32_MEMf32_AVX512	vcvtss2sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VCVTSS2SD_XMMf64_MASKmskw_XMMf32_XMMf32_AVX512	vcvtss2sd xmm1{k1}, xmm2, xmm3	5	1
XED_IFORM_VCVTSS2SI_GPR32d_MEMd	vcvtss2si eax, [rdi]	7	1
XED_IFORM_VCVTSS2SI_GPR32i32_MEMf32_AVX512	vcvtss2si eax, [rdi]	7	1
XED_IFORM_VCVTSS2SI_GPR32d_XMMd	vcvtss2si eax, xmm1	7	1
XED_IFORM_CVTSS2SI_GPR32d_XMMss	vcvtss2si eax, xmm1	7	1
XED_IFORM_VCVTSS2SI_GPR32i32_XMMf32_AVX512	vcvtss2si eax, xmm1	7	1
XED_IFORM_VCVTSS2SI_GPR64q_MEMd	vcvtss2si rax, [rdi]	7	1
XED_IFORM_VCVTSS2SI_GPR64i64_MEMf32_AVX512	vcvtss2si rax, [rdi]	7	1
XED_IFORM_VCVTSS2SI_GPR64q_XMMd	vcvtss2si rax, xmm1	7	1
XED_IFORM_CVTSS2SI_GPR64q_XMMss	vcvtss2si rax, xmm1	7	1
XED_IFORM_VCVTSS2SI_GPR64i64_XMMf32_AVX512	vcvtss2si rax, xmm1	7	1
XED_IFORM_VCVTSS2USI_GPR32u32_MEMf32_AVX512	vcvtss2usi eax, [rdi]	11	1
XED_IFORM_VCVTSS2USI_GPR32u32_XMMf32_AVX512	vcvtss2usi eax, xmm1	6	1
XED_IFORM_VCVTSS2USI_GPR64u64_MEMf32_AVX512	vcvtss2usi rax, [rdi]	12	1
XED_IFORM_VCVTSS2USI_GPR64u64_XMMf32_AVX512	vcvtss2usi rax, xmm1	7	1
XED_IFORM_CVTTPD2DQ_XMMdq_MEMpd	vcvttpd2dq xmm1, [rdi]	11	0
XED_IFORM_CVTTPD2DQ_XMMdq_XMMpd	vcvttpd2dq xmm1, xmm2	5	1
XED_IFORM_VCVTTPD2DQ_XMMdq_XMMdq	vcvttpd2dq xmm1, xmm2	5	1
XED_IFORM_VCVTTPD2DQ_XMMdq_YMMqq	vcvttpd2dq xmm1, ymm2	7	1
XED_IFORM_VCVTTPD2DQ_XMMi32_MASKmskw_XMMf64_AVX512_VL128	vcvttpd2dq xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTTPD2DQ_XMMi32_MASKmskw_YMMf64_AVX512_VL256	vcvttpd2dq xmm1{k1}, ymm2	7	1
XED_IFORM_VCVTTPD2DQ_YMMi32_MASKmskw_MEMf64_AVX512_VL512	vcvttpd2dq ymm1{k1}, [rdi]	14	1
XED_IFORM_VCVTTPD2DQ_YMMi32_MASKmskw_ZMMf64_AVX512_VL512	vcvttpd2dq ymm1{k1}, zmm2	7	1
XED_IFORM_VCVTTPD2QQ_XMMi64_MASKmskw_MEMf64_AVX512	vcvttpd2qq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTTPD2QQ_XMMi64_MASKmskw_XMMf64_AVX512	vcvttpd2qq xmm1{k1}, xmm2	4	0.5
XED_IFORM_VCVTTPD2QQ_YMMi64_MASKmskw_MEMf64_AVX512	vcvttpd2qq ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTTPD2QQ_YMMi64_MASKmskw_YMMf64_AVX512	vcvttpd2qq ymm1{k1}, ymm2	4	0.5
XED_IFORM_VCVTTPD2QQ_ZMMi64_MASKmskw_MEMf64_AVX512	vcvttpd2qq zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTTPD2QQ_ZMMi64_MASKmskw_ZMMf64_AVX512	vcvttpd2qq zmm1{k1}, zmm2	4	0.5
XED_IFORM_VCVTTPD2UDQ_XMMu32_MASKmskw_XMMf64_AVX512_VL128	vcvttpd2udq xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTTPD2UDQ_XMMu32_MASKmskw_YMMf64_AVX512_VL256	vcvttpd2udq xmm1{k1}, ymm2	7	1
XED_IFORM_VCVTTPD2UDQ_YMMu32_MASKmskw_MEMf64_AVX512_VL512	vcvttpd2udq ymm1{k1}, [rdi]	14	1
XED_IFORM_VCVTTPD2UDQ_YMMu32_MASKmskw_ZMMf64_AVX512_VL512	vcvttpd2udq ymm1{k1}, zmm2	7	1
XED_IFORM_VCVTTPD2UQQ_XMMu64_MASKmskw_MEMf64_AVX512	vcvttpd2uqq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTTPD2UQQ_XMMu64_MASKmskw_XMMf64_AVX512	vcvttpd2uqq xmm1{k1}, xmm2	4	0.5
XED_IFORM_VCVTTPD2UQQ_YMMu64_MASKmskw_MEMf64_AVX512	vcvttpd2uqq ymm1{k1}, [rdi]	4	0.5

XED_IFORM_VCVTTPD2UQQ_YMMu64_MASKmskw_YMMf64_AVX512	vcvttpd2uqq ymm1{k1}, ymm2	4	0.5
XED_IFORM_VCVTTPD2UQQ_ZMMu64_MASKmskw_MEMf64_AVX512	vcvttpd2uqq zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTTPD2UQQ_ZMMu64_MASKmskw_ZMMf64_AVX512	vcvttpd2uqq zmm1{k1}, zmm2	4	0.5
XED_IFORM_CVTTPS2DQ_XMMdq_MEMps	vcvttps2dq xmm1, [rdi]	10	0.5
XED_IFORM_VCVTTPS2DQ_XMMdq_MEMdq	vcvttps2dq xmm1, [rdi]	10	0.5
XED_IFORM_VCVTTPS2DQ_XMMdq_XMMdq	vcvttps2dq xmm1, xmm2	4	0.5
XED_IFORM_CVTTPS2DQ_XMMdq_XMMps	vcvttps2dq xmm1, xmm2	4	0.5
XED_IFORM_VCVTTPS2DQ_XMMi32_MASKmskw_MEMf32_AVX512	vcvttps2dq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTTPS2DQ_XMMi32_MASKmskw_XMMf32_AVX512	vcvttps2dq xmm1{k1}, xmm2	4	0.5
XED_IFORM_VCVTTPS2DQ_YMMqq_MEMqq	vcvttps2dq ymm1, [rdi]	4	0.5
XED_IFORM_VCVTTPS2DQ_YMMqq_YMMqq	vcvttps2dq ymm1, ymm2	4	0.5
XED_IFORM_VCVTTPS2DQ_YMMi32_MASKmskw_MEMf32_AVX512	vcvttps2dq ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTTPS2DQ_YMMi32_MASKmskw_YMMf32_AVX512	vcvttps2dq ymm1{k1}, ymm2	4	0.5
XED_IFORM_VCVTTPS2DQ_ZMMi32_MASKmskw_MEMf32_AVX512	vcvttps2dq zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTTPS2DQ_ZMMi32_MASKmskw_ZMMf32_AVX512	vcvttps2dq zmm1{k1}, zmm2	4	0.5
XED_IFORM_VCVTTPS2QQ_XMMi64_MASKmskw_MEMf32_AVX512	vcvttps2qq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTTPS2QQ_XMMi64_MASKmskw_XMMf32_AVX512	vcvttps2qq xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTTPS2QQ_YMMi64_MASKmskw_MEMf32_AVX512	vcvttps2qq ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTTPS2QQ_YMMi64_MASKmskw_XMMf32_AVX512	vcvttps2qq ymm1{k1}, xmm2	7	1
XED_IFORM_VCVTTPS2QQ_ZMMi64_MASKmskw_MEMf32_AVX512	vcvttps2qq zmm1{k1}, [rdi]	12	1
XED_IFORM_VCVTTPS2QQ_ZMMi64_MASKmskw_YMMf32_AVX512	vcvttps2qq zmm1{k1}, ymm2	7	1
XED_IFORM_VCVTTPS2UDQ_XMMu32_MASKmskw_MEMf32_AVX512	vcvttps2udq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTTPS2UDQ_XMMu32_MASKmskw_XMMf32_AVX512	vcvttps2udq xmm1{k1}, xmm2	4	0.5
XED_IFORM_VCVTTPS2UDQ_YMMu32_MASKmskw_MEMf32_AVX512	vcvttps2udq ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTTPS2UDQ_YMMu32_MASKmskw_YMMf32_AVX512	vcvttps2udq ymm1{k1}, ymm2	4	0.5
XED_IFORM_VCVTTPS2UDQ_ZMMu32_MASKmskw_MEMf32_AVX512	vcvttps2udq zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTTPS2UDQ_ZMMu32_MASKmskw_ZMMf32_AVX512	vcvttps2udq zmm1{k1}, zmm2	4	0.5
XED_IFORM_VCVTTPS2UQQ_XMMu64_MASKmskw_MEMf32_AVX512	vcvttps2uqq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTTPS2UQQ_XMMu64_MASKmskw_XMMf32_AVX512	vcvttps2uqq xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTTPS2UQQ_YMMu64_MASKmskw_MEMf32_AVX512	vcvttps2uqq ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTTPS2UQQ_YMMu64_MASKmskw_XMMf32_AVX512	vcvttps2uqq ymm1{k1}, xmm2	7	1
XED_IFORM_VCVTTPS2UQQ_ZMMu64_MASKmskw_MEMf32_AVX512	vcvttps2uqq zmm1{k1}, [rdi]	12	1
XED_IFORM_VCVTTPS2UQQ_ZMMu64_MASKmskw_YMMf32_AVX512	vcvttps2uqq zmm1{k1}, ymm2	7	1
XED_IFORM_VCVTTSD2SI_GPR32d_MEMq	vcvttsd2si eax, [rdi]	11	1
XED_IFORM_VCVTTSD2SI_GPR32i32_MEMf64_AVX512	vcvttsd2si eax, [rdi]	11	1
XED_IFORM_CVTTSD2SI_GPR32d_XMMsd	vcvttsd2si eax, xmm1	6	1
XED_IFORM_VCVTTSD2SI_GPR32i32_XMMf64_AVX512	vcvttsd2si eax, xmm1	6	1
XED_IFORM_VCVTTSD2SI_GPR32d_XMMq	vcvttsd2si eax, xmm1	6	1
XED_IFORM_VCVTTSD2SI_GPR64i64_MEMf64_AVX512	vcvttsd2si rax, [rdi]	11	1
XED_IFORM_VCVTTSD2SI_GPR64q_MEMq	vcvttsd2si rax, [rdi]	11	1
XED_IFORM_VCVTTSD2SI_GPR64i64_XMMf64_AVX512	vcvttsd2si rax, xmm1	6	1
XED_IFORM_CVTTSD2SI_GPR64q_XMMsd	vcvttsd2si rax, xmm1	6	1
XED_IFORM_VCVTTSD2SI_GPR64q_XMMq	vcvttsd2si rax, xmm1	6	1
XED_IFORM_VCVTTSD2USI_GPR32u32_MEMf64_AVX512	vcvttsd2usi eax, [rdi]	12	1
XED_IFORM_VCVTTSD2USI_GPR32u32_XMMf64_AVX512	vcvttsd2usi eax, xmm1	6	1
XED_IFORM_VCVTTSD2USI_GPR64u64_MEMf64_AVX512	vcvttsd2usi rax, [rdi]	11	1
XED_IFORM_VCVTTSD2USI_GPR64u64_XMMf64_AVX512	vcvttsd2usi rax, xmm1	6	1
XED_IFORM_VCVTTSS2SI_GPR32d_MEMd	vcvttss2si eax, [rdi]	11	1
XED_IFORM_VCVTTSS2SI_GPR32i32_MEMf32_AVX512	vcvttss2si eax, [rdi]	11	1
XED_IFORM_CVTTSS2SI_GPR32d_XMMss	vcvttss2si eax, xmm1	7	1
XED_IFORM_VCVTTSS2SI_GPR32i32_XMMf32_AVX512	vcvttss2si eax, xmm1	7	1
XED_IFORM_VCVTTSS2SI_GPR32d_XMMd	vcvttss2si eax, xmm1	7	1
XED_IFORM_VCVTTSS2SI_GPR64q_MEMd	vcvttss2si rax, [rdi]	11	1
XED_IFORM_VCVTTSS2SI_GPR64i64_MEMf32_AVX512	vcvttss2si rax, [rdi]	11	1
XED_IFORM_VCVTTSS2SI_GPR64i64_XMMf32_AVX512	vcvttss2si rax, xmm1	7	1
XED_IFORM_CVTTSS2SI_GPR64q_XMMss	vcvttss2si rax, xmm1	7	1
XED_IFORM_VCVTTSS2SI_GPR64q_XMMd	vcvttss2si rax, xmm1	7	1
XED_IFORM_VCVTTSS2USI_GPR32u32_MEMf32_AVX512	vcvttss2usi eax, [rdi]	11	1
XED_IFORM_VCVTTSS2USI_GPR32u32_XMMf32_AVX512	vcvttss2usi eax, xmm1	6	1
XED_IFORM_VCVTTSS2USI_GPR64u64_MEMf32_AVX512	vcvttss2usi rax, [rdi]	12	1
XED_IFORM_VCVTTSS2USI_GPR64u64_XMMf32_AVX512	vcvttss2usi rax, xmm1	7	1
XED_IFORM_VCVTUDQ2PD_XMMf64_MASKmskw_MEMu32_AVX512	vcvtudq2pd xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTUDQ2PD_XMMf64_MASKmskw_XMMu32_AVX512	vcvtudq2pd xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTUDQ2PD_YMMf64_MASKmskw_MEMu32_AVX512	vcvtudq2pd ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTUDQ2PD_YMMf64_MASKmskw_XMMu32_AVX512	vcvtudq2pd ymm1{k1}, xmm2	7	1
XED_IFORM_VCVTUDQ2PD_ZMMf64_MASKmskw_MEMu32_AVX512	vcvtudq2pd zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTUDQ2PD_ZMMf64_MASKmskw_YMMu32_AVX512	vcvtudq2pd zmm1{k1}, ymm2	7	1
XED_IFORM_VCVTUDQ2PS_XMMf32_MASKmskw_MEMu32_AVX512	vcvtudq2ps xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTUDQ2PS_XMMf32_MASKmskw_XMMu32_AVX512	vcvtudq2ps xmm1{k1}, xmm2	4	0.5
XED_IFORM_VCVTUDQ2PS_YMMf32_MASKmskw_MEMu32_AVX512	vcvtudq2ps ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTUDQ2PS_YMMf32_MASKmskw_YMMu32_AVX512	vcvtudq2ps ymm1{k1}, ymm2	4	0.5
XED_IFORM_VCVTUDQ2PS_ZMMf32_MASKmskw_MEMu32_AVX512	vcvtudq2ps zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTUDQ2PS_ZMMf32_MASKmskw_ZMMu32_AVX512	vcvtudq2ps zmm1{k1}, zmm2	4	0.5
XED_IFORM_VCVTUQQ2PD_XMMf64_MASKmskw_MEMu64_AVX512	vcvtuqq2pd xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VCVTUQQ2PD_XMMf64_MASKmskw_XMMu64_AVX512	vcvtuqq2pd xmm1{k1}, xmm2	4	0.5
XED_IFORM_VCVTUQQ2PD_YMMf64_MASKmskw_MEMu64_AVX512	vcvtuqq2pd ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VCVTUQQ2PD_YMMf64_MASKmskw_YMMu64_AVX512	vcvtuqq2pd ymm1{k1}, ymm2	4	0.5
XED_IFORM_VCVTUQQ2PD_ZMMf64_MASKmskw_MEMu64_AVX512	vcvtuqq2pd zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VCVTUQQ2PD_ZMMf64_MASKmskw_ZMMu64_AVX512	vcvtuqq2pd zmm1{k1}, zmm2	4	0.5

XED_IFORM_VCVTUQQ2PS_XMMf32_MASKmskw_XMMu64_AVX512_VL128	vcvtuqq2ps xmm1{k1}, xmm2	5	1
XED_IFORM_VCVTUQQ2PS_XMMf32_MASKmskw_YMMu64_AVX512_VL256	vcvtuqq2ps xmm1{k1}, ymm2	7	1
XED_IFORM_VCVTUQQ2PS_YMMf32_MASKmskw_MEMu64_AVX512_VL512	vcvtuqq2ps ymm1{k1}, [rdi]	14	1
XED_IFORM_VCVTUQQ2PS_YMMf32_MASKmskw_ZMMu64_AVX512_VL512	vcvtuqq2ps ymm1{k1}, zmm2	7	1
XED_IFORM_VCVTUSI2SD_XMMf64_XMMf64_GPR32u32_AVX512	vcvtusi2sd xmm1, xmm2, eax	5	1
XED_IFORM_VCVTUSI2SD_XMMf64_XMMf64_GPR64u64_AVX512	vcvtusi2sd xmm1, xmm2, rax	5	1
XED_IFORM_VCVTUSI2SS_XMMf32_XMMf32_GPR32u32_AVX512	vcvtusi2ss xmm1, xmm2, eax	5	1
XED_IFORM_VCVTUSI2SS_XMMf32_XMMf32_GPR64u64_AVX512	vcvtusi2ss xmm1, xmm2, rax	6	2
XED_IFORM_VDBPSADBW_XMMu16_MASKmskw_XMMu8_MEMu8_IMM8_AVX512	vdbpsadbw xmm1{k1}, xmm2, [rdi], 1	9	1
XED_IFORM_VDBPSADBW_XMMu16_MASKmskw_XMMu8_XMMu8_IMM8_AVX512	vdbpsadbw xmm1{k1}, xmm2, xmm3, 1	3	1
XED_IFORM_VDBPSADBW_YMMu16_MASKmskw_YMMu8_MEMu8_IMM8_AVX512	vdbpsadbw ymm1{k1}, ymm2, [rdi], 1	3	1
XED_IFORM_VDBPSADBW_YMMu16_MASKmskw_YMMu8_YMMu8_IMM8_AVX512	vdbpsadbw ymm1{k1}, ymm2, ymm3, 1	3	1
XED_IFORM_VDBPSADBW_ZMMu16_MASKmskw_ZMMu8_MEMu8_IMM8_AVX512	vdbpsadbw zmm1{k1}, zmm2, [rdi], 1	10	1
XED_IFORM_VDBPSADBW_ZMMu16_MASKmskw_ZMMu8_ZMMu8_IMM8_AVX512	vdbpsadbw zmm1{k1}, zmm2, zmm3, 1	3	1
XED_IFORM_DIVPD_XMMpd_MEMpd	vdivpd xmm1, xmm1, [rdi]	20	4
XED_IFORM_DIVPD_XMMpd_XMMpd	vdivpd xmm1, xmm1, xmm2	14	4
XED_IFORM_VDIVPD_XMMdq_XMMdq_MEMdq	vdivpd xmm1, xmm2, [rdi]	20	4
XED_IFORM_VDIVPD_XMMdq_XMMdq_XMMdq	vdivpd xmm1, xmm2, xmm3	14	4
XED_IFORM_VDIVPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vdivpd xmm1{k1}, xmm2, [rdi]	20	4
XED_IFORM_VDIVPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vdivpd xmm1{k1}, xmm2, xmm3	14	4
XED_IFORM_VDIVPD_YMMqq_YMMqq_MEMqq	vdivpd ymm1, ymm2, [rdi]	14	8
XED_IFORM_VDIVPD_YMMqq_YMMqq_YMMqq	vdivpd ymm1, ymm2, ymm3	14	8
XED_IFORM_VDIVPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vdivpd ymm1{k1}, ymm2, [rdi]	14	8
XED_IFORM_VDIVPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vdivpd ymm1{k1}, ymm2, ymm3	14	8
XED_IFORM_VDIVPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vdivpd zmm1{k1}, zmm2, [rdi]	30	16
XED_IFORM_VDIVPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vdivpd zmm1{k1}, zmm2, zmm3	23	16
XED_IFORM_DIVPS_XMMps_MEMps	vdivps xmm1, xmm1, [rdi]	17	3
XED_IFORM_DIVPS_XMMps_XMMps	vdivps xmm1, xmm1, xmm2	11	3
XED_IFORM_VDIVPS_XMMdq_XMMdq_MEMdq	vdivps xmm1, xmm2, [rdi]	17	3
XED_IFORM_VDIVPS_XMMdq_XMMdq_XMMdq	vdivps xmm1, xmm2, xmm3	11	3
XED_IFORM_VDIVPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vdivps xmm1{k1}, xmm2, [rdi]	17	3
XED_IFORM_VDIVPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vdivps xmm1{k1}, xmm2, xmm3	11	3
XED_IFORM_VDIVPS_YMMqq_YMMqq_MEMqq	vdivps ymm1, ymm2, [rdi]	11	5
XED_IFORM_VDIVPS_YMMqq_YMMqq_YMMqq	vdivps ymm1, ymm2, ymm3	11	5
XED_IFORM_VDIVPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vdivps ymm1{k1}, ymm2, [rdi]	11	5
XED_IFORM_VDIVPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vdivps ymm1{k1}, ymm2, ymm3	11	5
XED_IFORM_VDIVPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vdivps zmm1{k1}, zmm2, [rdi]	24	10
XED_IFORM_VDIVPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vdivps zmm1{k1}, zmm2, zmm3	23	10
XED_IFORM_DIVSD_XMMsd_MEMsd	vdivsd xmm1, xmm1, [rdi]	19	4
XED_IFORM_DIVSD_XMMsd_XMMsd	vdivsd xmm1, xmm1, xmm2	14	4
XED_IFORM_VDIVSD_XMMdq_XMMdq_MEMq	vdivsd xmm1, xmm2, [rdi]	19	4
XED_IFORM_VDIVSD_XMMdq_XMMdq_XMMq	vdivsd xmm1, xmm2, xmm3	14	4
XED_IFORM_VDIVSD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vdivsd xmm1{k1}, xmm2, [rdi]	20	4
XED_IFORM_VDIVSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vdivsd xmm1{k1}, xmm2, xmm3	14	4
XED_IFORM_DIVSS_XMMss_MEMss	vdivss xmm1, xmm1, [rdi]	16	3
XED_IFORM_DIVSS_XMMss_XMMss	vdivss xmm1, xmm1, xmm2	11	3
XED_IFORM_VDIVSS_XMMdq_XMMdq_MEMd	vdivss xmm1, xmm2, [rdi]	16	3
XED_IFORM_VDIVSS_XMMdq_XMMdq_XMMd	vdivss xmm1, xmm2, xmm3	11	3
XED_IFORM_VDIVSS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vdivss xmm1{k1}, xmm2, [rdi]	17	3
XED_IFORM_VDIVSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vdivss xmm1{k1}, xmm2, xmm3	11	3
XED_IFORM_DPPD_XMMdq_MEMdq_IMMb	vdppd xmm1, xmm1, [rdi], 1	15	1
XED_IFORM_DPPD_XMMdq_XMMdq_IMMb	vdppd xmm1, xmm1, xmm2, 1	9	1
XED_IFORM_VDPPD_XMMdq_XMMdq_MEMdq_IMMb	vdppd xmm1, xmm2, [rdi], 1	15	1
XED_IFORM_VDPPD_XMMdq_XMMdq_XMMdq_IMMb	vdppd xmm1, xmm2, xmm3, 1	9	1
XED_IFORM_DPPS_XMMdq_MEMdq_IMMb	vdpps xmm1, xmm1, [rdi], 1	19	1.5
XED_IFORM_DPPS_XMMdq_XMMdq_IMMb	vdpps xmm1, xmm1, xmm2, 1	13	1.5
XED_IFORM_VDPPS_XMMdq_XMMdq_MEMdq_IMMb	vdpps xmm1, xmm2, [rdi], 1	19	1.5
XED_IFORM_VDPPS_XMMdq_XMMdq_XMMdq_IMMb	vdpps xmm1, xmm2, xmm3, 1	13	1.5
XED_IFORM_VDPPS_YMMqq_YMMqq_MEMqq_IMMb	vdpps ymm1, ymm2, [rdi], 1	13	1.5
XED_IFORM_VDPPS_YMMqq_YMMqq_YMMqq_IMMb	vdpps ymm1, ymm2, ymm3, 1	13	1.5
XED_IFORM_VEXPANDPD_XMMf64_MASKmskw_MEMf64_AVX512	vexpandpd xmm1{k1}, [rdi]	10	2
XED_IFORM_VEXPANDPD_XMMf64_MASKmskw_XMMf64_AVX512	vexpandpd xmm1{k1}, xmm2	4	2
XED_IFORM_VEXPANDPD_YMMf64_MASKmskw_MEMf64_AVX512	vexpandpd ymm1{k1}, [rdi]	4	2
XED_IFORM_VEXPANDPD_YMMf64_MASKmskw_YMMf64_AVX512	vexpandpd ymm1{k1}, ymm2	4	2
XED_IFORM_VEXPANDPD_ZMMf64_MASKmskw_MEMf64_AVX512	vexpandpd zmm1{k1}, [rdi]	11	2
XED_IFORM_VEXPANDPD_ZMMf64_MASKmskw_ZMMf64_AVX512	vexpandpd zmm1{k1}, zmm2	4	2
XED_IFORM_VEXPANDPS_XMMf32_MASKmskw_MEMf32_AVX512	vexpandps xmm1{k1}, [rdi]	10	2
XED_IFORM_VEXPANDPS_XMMf32_MASKmskw_XMMf32_AVX512	vexpandps xmm1{k1}, xmm2	4	2
XED_IFORM_VEXPANDPS_YMMf32_MASKmskw_MEMf32_AVX512	vexpandps ymm1{k1}, [rdi]	4	2
XED_IFORM_VEXPANDPS_YMMf32_MASKmskw_YMMf32_AVX512	vexpandps ymm1{k1}, ymm2	4	2
XED_IFORM_VEXPANDPS_ZMMf32_MASKmskw_MEMf32_AVX512	vexpandps zmm1{k1}, [rdi]	11	2
XED_IFORM_VEXPANDPS_ZMMf32_MASKmskw_ZMMf32_AVX512	vexpandps zmm1{k1}, zmm2	4	2
XED_IFORM_VEXTRACTF128_MEMdq_YMMdq_IMMb	vextractf128 [rdi], ymm1, 1	5	1
XED_IFORM_VEXTRACTF128_XMMdq_YMMdq_IMMb	vextractf128 xmm1, ymm2, 1	3	1
XED_IFORM_VEXTRACTF32X4_MEMf32_MASKmskw_YMMf32_IMM8_AVX512	vextractf32x4 [rdi]{k1}, ymm1, 1	5	1
XED_IFORM_VEXTRACTF32X4_MEMf32_MASKmskw_ZMMf32_IMM8_AVX512	vextractf32x4 [rdi]{k1}, zmm1, 1	5	1
XED_IFORM_VEXTRACTF32X4_XMMf32_MASKmskw_YMMf32_IMM8_AVX512	vextractf32x4 xmm1{k1}, ymm2, 1	3	1
XED_IFORM_VEXTRACTF32X4_XMMf32_MASKmskw_ZMMf32_IMM8_AVX512	vextractf32x4 xmm1{k1}, zmm2, 1	3	1
XED_IFORM_VEXTRACTF32X8_MEMf32_MASKmskw_ZMMf32_IMM8_AVX512	vextractf32x8 [rdi]{k1}, zmm1, 1	5	1

XED_IFORM_VEXTRACTF32X8_YMMf32_MASKmskw_ZMMf32_IMM8_AVX512	vextractf32x8 ymm1{k1}, zmm2, 1	3	1
XED_IFORM_VEXTRACTF64X2_MEMf64_MASKmskw_YMMf64_IMM8_AVX512	vextractf64x2 [rdi]{k1}, ymm1, 1	5	1
XED_IFORM_VEXTRACTF64X2_MEMf64_MASKmskw_ZMMf64_IMM8_AVX512	vextractf64x2 [rdi]{k1}, zmm1, 1	5	1
XED_IFORM_VEXTRACTF64X2_XMMf64_MASKmskw_YMMf64_IMM8_AVX512	vextractf64x2 xmm1{k1}, ymm2, 1	3	1
XED_IFORM_VEXTRACTF64X2_XMMf64_MASKmskw_ZMMf64_IMM8_AVX512	vextractf64x2 xmm1{k1}, zmm2, 1	3	1
XED_IFORM_VEXTRACTF64X4_MEMf64_MASKmskw_ZMMf64_IMM8_AVX512	vextractf64x4 [rdi]{k1}, zmm1, 1	5	1
XED_IFORM_VEXTRACTF64X4_YMMf64_MASKmskw_ZMMf64_IMM8_AVX512	vextractf64x4 ymm1{k1}, zmm2, 1	3	1
XED_IFORM_VEXTRACTI128_MEMdq_YMMqq_IMMb	vextracti128 [rdi], ymm1, 1	5	1
XED_IFORM_VEXTRACTI128_XMMdq_YMMqq_IMMb	vextracti128 xmm1, ymm2, 1	3	1
XED_IFORM_VEXTRACTI32X4_MEMu32_MASKmskw_YMMu32_IMM8_AVX512	vextracti32x4 [rdi]{k1}, ymm1, 1	5	1
XED_IFORM_VEXTRACTI32X4_MEMu32_MASKmskw_ZMMu32_IMM8_AVX512	vextracti32x4 [rdi]{k1}, zmm1, 1	5	1
XED_IFORM_VEXTRACTI32X4_XMMu32_MASKmskw_YMMu32_IMM8_AVX512	vextracti32x4 xmm1{k1}, ymm2, 1	3	1
XED_IFORM_VEXTRACTI32X4_XMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vextracti32x4 xmm1{k1}, zmm2, 1	3	1
XED_IFORM_VEXTRACTI32X8_MEMu32_MASKmskw_ZMMu32_IMM8_AVX512	vextracti32x8 [rdi]{k1}, zmm1, 1	5	1
XED_IFORM_VEXTRACTI32X8_YMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vextracti32x8 ymm1{k1}, zmm2, 1	3	1
XED_IFORM_VEXTRACTI64X2_MEMu64_MASKmskw_YMMu64_IMM8_AVX512	vextracti64x2 [rdi]{k1}, ymm1, 1	5	1
XED_IFORM_VEXTRACTI64X2_MEMu64_MASKmskw_ZMMu64_IMM8_AVX512	vextracti64x2 [rdi]{k1}, zmm1, 1	5	1
XED_IFORM_VEXTRACTI64X2_XMMu64_MASKmskw_YMMu64_IMM8_AVX512	vextracti64x2 xmm1{k1}, ymm2, 1	3	1
XED_IFORM_VEXTRACTI64X2_XMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vextracti64x2 xmm1{k1}, zmm2, 1	3	1
XED_IFORM_VEXTRACTI64X4_MEMu64_MASKmskw_ZMMu64_IMM8_AVX512	vextracti64x4 [rdi]{k1}, zmm1, 1	5	1
XED_IFORM_VEXTRACTI64X4_YMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vextracti64x4 ymm1{k1}, zmm2, 1	3	1
XED_IFORM_VEXTRACTPS_MEMf32_XMMf32_IMM8_AVX512	vextractps [rdi], xmm1, 1	6	1
XED_IFORM_VEXTRACTPS_MEMd_XMMdq_IMMb	vextractps [rdi], xmm1, 1	6	1
XED_IFORM_EXTRACTPS_MEMd_XMMps_IMMb	vextractps [rdi], xmm1, 1	6	1
XED_IFORM_EXTRACTPS_GPR32d_XMMdq_IMMb	vextractps eax, xmm1, 1	3	1
XED_IFORM_VEXTRACTPS_GPR32f32_XMMf32_IMM8_AVX512	vextractps eax, xmm1, 1	3	1
XED_IFORM_VEXTRACTPS_GPR32_XMMdq_IMMb	vextractps eax, xmm1, 1	3	1
XED_IFORM_VFIXUPIMMPD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vfixupimmpd xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VFIXUPIMMPD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vfixupimmpd xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VFIXUPIMMPD_YMMf64_MASKmskw_YMMf64_MEMf64_IMM8_AVX512	vfixupimmpd ymm1{k1}, ymm2, [rdi], 1	4	0.5
XED_IFORM_VFIXUPIMMPD_YMMf64_MASKmskw_YMMf64_YMMf64_IMM8_AVX512	vfixupimmpd ymm1{k1}, ymm2, ymm3, 1	4	0.5
XED_IFORM_VFIXUPIMMPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_IMM8_AVX512	vfixupimmpd zmm1{k1}, zmm2, [rdi], 1	11	0.5
XED_IFORM_VFIXUPIMMPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_IMM8_AVX512	vfixupimmpd zmm1{k1}, zmm2, zmm3, 1	4	0.5
XED_IFORM_VFIXUPIMMPS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vfixupimmps xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VFIXUPIMMPS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vfixupimmps xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VFIXUPIMMPS_YMMf32_MASKmskw_YMMf32_MEMf32_IMM8_AVX512	vfixupimmps ymm1{k1}, ymm2, [rdi], 1	4	0.5
XED_IFORM_VFIXUPIMMPS_YMMf32_MASKmskw_YMMf32_YMMf32_IMM8_AVX512	vfixupimmps ymm1{k1}, ymm2, ymm3, 1	4	0.5
XED_IFORM_VFIXUPIMMPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_IMM8_AVX512	vfixupimmps zmm1{k1}, zmm2, [rdi], 1	11	0.5
XED_IFORM_VFIXUPIMMPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_IMM8_AVX512	vfixupimmps zmm1{k1}, zmm2, zmm3, 1	4	0.5
XED_IFORM_VFIXUPIMMSD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vfixupimmsd xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VFIXUPIMMSD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vfixupimmsd xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VFIXUPIMMSS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vfixupimmss xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VFIXUPIMMSS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vfixupimmss xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VFMADD132PD_XMMdq_XMMdq_MEMdq	vfmadd132pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD132PD_XMMdq_XMMdq_XMMdq	vfmadd132pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD132PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmadd132pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD132PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmadd132pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD132PD_YMMqq_YMMqq_MEMqq	vfmadd132pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADD132PD_YMMqq_YMMqq_YMMqq	vfmadd132pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMADD132PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfmadd132pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADD132PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfmadd132pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMADD132PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfmadd132pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMADD132PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfmadd132pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMADD132PS_XMMdq_XMMdq_MEMdq	vfmadd132ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD132PS_XMMdq_XMMdq_XMMdq	vfmadd132ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD132PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmadd132ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD132PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmadd132ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD132PS_YMMqq_YMMqq_MEMqq	vfmadd132ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADD132PS_YMMqq_YMMqq_YMMqq	vfmadd132ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMADD132PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfmadd132ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADD132PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfmadd132ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMADD132PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfmadd132ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMADD132PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfmadd132ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMADD132SD_XMMdq_XMMq_MEMq	vfmadd132sd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFMADD132SD_XMMdq_XMMq_XMMq	vfmadd132sd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD132SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmadd132sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD132SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmadd132sd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD132SS_XMMdq_XMMd_MEMd	vfmadd132ss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFMADD132SS_XMMdq_XMMd_XMMd	vfmadd132ss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD132SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmadd132ss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD132SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmadd132ss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD213PD_XMMdq_XMMdq_MEMdq	vfmadd213pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD213PD_XMMdq_XMMdq_XMMdq	vfmadd213pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD213PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmadd213pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD213PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmadd213pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD213PD_YMMqq_YMMqq_MEMqq	vfmadd213pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADD213PD_YMMqq_YMMqq_YMMqq	vfmadd213pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMADD213PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfmadd213pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADD213PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfmadd213pd ymm1{k1}, ymm2, ymm3	4	0.5

XED_IFORM_VFMADD213PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfmadd213pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMADD213PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfmadd213pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMADD213PS_XMMdq_XMMdq_MEMdq	vfmadd213ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD213PS_XMMdq_XMMdq_XMMdq	vfmadd213ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD213PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmadd213ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD213PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmadd213ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD213PS_YMMqq_YMMqq_MEMqq	vfmadd213ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADD213PS_YMMqq_YMMqq_YMMqq	vfmadd213ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMADD213PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfmadd213ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADD213PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfmadd213ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMADD213PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfmadd213ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMADD213PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfmadd213ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMADD213SD_XMMdq_XMMq_MEMq	vfmadd213sd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFMADD213SD_XMMdq_XMMq_XMMq	vfmadd213sd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD213SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmadd213sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD213SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmadd213sd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD213SS_XMMdq_XMMd_MEMd	vfmadd213ss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFMADD213SS_XMMdq_XMMd_XMMd	vfmadd213ss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD213SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmadd213ss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD213SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmadd213ss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD231PD_XMMdq_XMMdq_MEMdq	vfmadd231pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD231PD_XMMdq_XMMdq_XMMdq	vfmadd231pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD231PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmadd231pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD231PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmadd231pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD231PD_YMMqq_YMMqq_MEMqq	vfmadd231pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADD231PD_YMMqq_YMMqq_YMMqq	vfmadd231pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMADD231PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfmadd231pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADD231PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfmadd231pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMADD231PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfmadd231pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMADD231PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfmadd231pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMADD231PS_XMMdq_XMMdq_MEMdq	vfmadd231ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD231PS_XMMdq_XMMdq_XMMdq	vfmadd231ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD231PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmadd231ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD231PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmadd231ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD231PS_YMMqq_YMMqq_MEMqq	vfmadd231ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADD231PS_YMMqq_YMMqq_YMMqq	vfmadd231ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMADD231PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfmadd231ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADD231PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfmadd231ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMADD231PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfmadd231ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMADD231PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfmadd231ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMADD231SD_XMMdq_XMMq_MEMq	vfmadd231sd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFMADD231SD_XMMdq_XMMq_XMMq	vfmadd231sd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD231SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmadd231sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD231SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmadd231sd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD231SS_XMMdq_XMMd_MEMd	vfmadd231ss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFMADD231SS_XMMdq_XMMd_XMMd	vfmadd231ss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADD231SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmadd231ss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADD231SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmadd231ss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB132PD_XMMdq_XMMdq_MEMdq	vfmaddsub132pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADDSUB132PD_XMMdq_XMMdq_XMMdq	vfmaddsub132pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB132PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmaddsub132pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADDSUB132PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmaddsub132pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB132PD_YMMqq_YMMqq_MEMqq	vfmaddsub132pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADDSUB132PD_YMMqq_YMMqq_YMMqq	vfmaddsub132pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMADDSUB132PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfmaddsub132pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADDSUB132PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfmaddsub132pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMADDSUB132PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfmaddsub132pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMADDSUB132PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfmaddsub132pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMADDSUB132PS_XMMdq_XMMdq_MEMdq	vfmaddsub132ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADDSUB132PS_XMMdq_XMMdq_XMMdq	vfmaddsub132ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB132PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmaddsub132ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADDSUB132PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmaddsub132ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB132PS_YMMqq_YMMqq_MEMqq	vfmaddsub132ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADDSUB132PS_YMMqq_YMMqq_YMMqq	vfmaddsub132ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMADDSUB132PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfmaddsub132ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADDSUB132PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfmaddsub132ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMADDSUB132PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfmaddsub132ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMADDSUB132PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfmaddsub132ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMADDSUB213PD_XMMdq_XMMdq_MEMdq	vfmaddsub213pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADDSUB213PD_XMMdq_XMMdq_XMMdq	vfmaddsub213pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB213PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmaddsub213pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADDSUB213PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmaddsub213pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB213PD_YMMqq_YMMqq_MEMqq	vfmaddsub213pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADDSUB213PD_YMMqq_YMMqq_YMMqq	vfmaddsub213pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMADDSUB213PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfmaddsub213pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADDSUB213PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfmaddsub213pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMADDSUB213PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfmaddsub213pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMADDSUB213PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfmaddsub213pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMADDSUB213PS_XMMdq_XMMdq_MEMdq	vfmaddsub213ps xmm1, xmm2, [rdi]	10	0.5

XED_IFORM_VFMADDSUB213PS_XMMdq_XMMdq_XMMdq	vfmaddsub213ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB213PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmaddsub213ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADDSUB213PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmaddsub213ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB213PS_YMMqq_YMMqq_MEMqq	vfmaddsub213ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADDSUB213PS_YMMqq_YMMqq_YMMqq	vfmaddsub213ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMADDSUB213PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfmaddsub213ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADDSUB213PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfmaddsub213ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMADDSUB213PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfmaddsub213ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMADDSUB213PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfmaddsub213ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMADDSUB231PD_XMMdq_XMMdq_MEMdq	vfmaddsub231pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADDSUB231PD_XMMdq_XMMdq_XMMdq	vfmaddsub231pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB231PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmaddsub231pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADDSUB231PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmaddsub231pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB231PD_YMMqq_YMMqq_MEMqq	vfmaddsub231pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADDSUB231PD_YMMqq_YMMqq_YMMqq	vfmaddsub231pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMADDSUB231PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfmaddsub231pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADDSUB231PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfmaddsub231pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMADDSUB231PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfmaddsub231pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMADDSUB231PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfmaddsub231pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMADDSUB231PS_XMMdq_XMMdq_MEMdq	vfmaddsub231ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADDSUB231PS_XMMdq_XMMdq_XMMdq	vfmaddsub231ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB231PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmaddsub231ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMADDSUB231PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmaddsub231ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMADDSUB231PS_YMMqq_YMMqq_MEMqq	vfmaddsub231ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADDSUB231PS_YMMqq_YMMqq_YMMqq	vfmaddsub231ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMADDSUB231PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfmaddsub231ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMADDSUB231PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfmaddsub231ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMADDSUB231PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfmaddsub231ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMADDSUB231PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfmaddsub231ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMSUB132PD_XMMdq_XMMdq_MEMdq	vfmsub132pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB132PD_XMMdq_XMMdq_XMMdq	vfmsub132pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB132PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmsub132pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB132PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmsub132pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB132PD_YMMqq_YMMqq_MEMqq	vfmsub132pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUB132PD_YMMqq_YMMqq_YMMqq	vfmsub132pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUB132PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfmsub132pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUB132PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfmsub132pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUB132PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfmsub132pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMSUB132PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfmsub132pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMSUB132PS_XMMdq_XMMdq_MEMdq	vfmsub132ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB132PS_XMMdq_XMMdq_XMMdq	vfmsub132ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB132PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmsub132ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB132PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmsub132ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB132PS_YMMqq_YMMqq_MEMqq	vfmsub132ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUB132PS_YMMqq_YMMqq_YMMqq	vfmsub132ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUB132PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfmsub132ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUB132PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfmsub132ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUB132PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfmsub132ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMSUB132PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfmsub132ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMSUB132SD_XMMdq_XMMq_MEMq	vfmsub132sd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFMSUB132SD_XMMdq_XMMq_XMMq	vfmsub132sd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB132SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmsub132sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB132SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmsub132sd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB132SS_XMMdq_XMMd_MEMd	vfmsub132ss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFMSUB132SS_XMMdq_XMMd_XMMd	vfmsub132ss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB132SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmsub132ss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB132SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmsub132ss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB213PD_XMMdq_XMMdq_MEMdq	vfmsub213pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB213PD_XMMdq_XMMdq_XMMdq	vfmsub213pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB213PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmsub213pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB213PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmsub213pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB213PD_YMMqq_YMMqq_MEMqq	vfmsub213pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUB213PD_YMMqq_YMMqq_YMMqq	vfmsub213pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUB213PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfmsub213pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUB213PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfmsub213pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUB213PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfmsub213pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMSUB213PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfmsub213pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMSUB213PS_XMMdq_XMMdq_MEMdq	vfmsub213ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB213PS_XMMdq_XMMdq_XMMdq	vfmsub213ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB213PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmsub213ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB213PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmsub213ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB213PS_YMMqq_YMMqq_MEMqq	vfmsub213ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUB213PS_YMMqq_YMMqq_YMMqq	vfmsub213ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUB213PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfmsub213ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUB213PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfmsub213ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUB213PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfmsub213ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMSUB213PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfmsub213ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMSUB213SD_XMMdq_XMMq_MEMq	vfmsub213sd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFMSUB213SD_XMMdq_XMMq_XMMq	vfmsub213sd xmm1, xmm2, xmm3	4	0.5

XED_IFORM_VFMSUB213SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmsub213sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB213SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmsub213sd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB213SS_XMMdq_XMMd_MEMd	vfmsub213ss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFMSUB213SS_XMMdq_XMMd_XMMd	vfmsub213ss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB213SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmsub213ss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB213SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmsub213ss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB231PD_XMMdq_XMMdq_MEMdq	vfmsub231pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB231PD_XMMdq_XMMdq_XMMdq	vfmsub231pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB231PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmsub231pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB231PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmsub231pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB231PD_YMMqq_YMMqq_MEMqq	vfmsub231pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUB231PD_YMMqq_YMMqq_YMMqq	vfmsub231pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUB231PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfmsub231pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUB231PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfmsub231pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUB231PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfmsub231pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMSUB231PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfmsub231pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMSUB231PS_XMMdq_XMMdq_MEMdq	vfmsub231ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB231PS_XMMdq_XMMdq_XMMdq	vfmsub231ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB231PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmsub231ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB231PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmsub231ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB231PS_YMMqq_YMMqq_MEMqq	vfmsub231ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUB231PS_YMMqq_YMMqq_YMMqq	vfmsub231ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUB231PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfmsub231ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUB231PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfmsub231ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUB231PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfmsub231ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMSUB231PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfmsub231ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMSUB231SD_XMMdq_XMMq_MEMq	vfmsub231sd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFMSUB231SD_XMMdq_XMMq_XMMq	vfmsub231sd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB231SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmsub231sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB231SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmsub231sd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB231SS_XMMdq_XMMd_MEMd	vfmsub231ss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFMSUB231SS_XMMdq_XMMd_XMMd	vfmsub231ss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUB231SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmsub231ss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUB231SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmsub231ss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD132PD_XMMdq_XMMdq_MEMdq	vfmsubadd132pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUBADD132PD_XMMdq_XMMdq_XMMdq	vfmsubadd132pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD132PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmsubadd132pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUBADD132PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmsubadd132pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD132PD_YMMqq_YMMqq_MEMqq	vfmsubadd132pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUBADD132PD_YMMqq_YMMqq_YMMqq	vfmsubadd132pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUBADD132PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfmsubadd132pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUBADD132PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfmsubadd132pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUBADD132PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfmsubadd132pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMSUBADD132PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfmsubadd132pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMSUBADD132PS_XMMdq_XMMdq_MEMdq	vfmsubadd132ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUBADD132PS_XMMdq_XMMdq_XMMdq	vfmsubadd132ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD132PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmsubadd132ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUBADD132PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmsubadd132ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD132PS_YMMqq_YMMqq_MEMqq	vfmsubadd132ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUBADD132PS_YMMqq_YMMqq_YMMqq	vfmsubadd132ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUBADD132PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfmsubadd132ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUBADD132PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfmsubadd132ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUBADD132PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfmsubadd132ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMSUBADD132PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfmsubadd132ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMSUBADD213PD_XMMdq_XMMdq_MEMdq	vfmsubadd213pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUBADD213PD_XMMdq_XMMdq_XMMdq	vfmsubadd213pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD213PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmsubadd213pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUBADD213PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmsubadd213pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD213PD_YMMqq_YMMqq_MEMqq	vfmsubadd213pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUBADD213PD_YMMqq_YMMqq_YMMqq	vfmsubadd213pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUBADD213PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfmsubadd213pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUBADD213PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfmsubadd213pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUBADD213PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfmsubadd213pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMSUBADD213PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfmsubadd213pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMSUBADD213PS_XMMdq_XMMdq_MEMdq	vfmsubadd213ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUBADD213PS_XMMdq_XMMdq_XMMdq	vfmsubadd213ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD213PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmsubadd213ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUBADD213PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmsubadd213ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD213PS_YMMqq_YMMqq_MEMqq	vfmsubadd213ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUBADD213PS_YMMqq_YMMqq_YMMqq	vfmsubadd213ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUBADD213PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfmsubadd213ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUBADD213PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfmsubadd213ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUBADD213PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfmsubadd213ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMSUBADD213PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfmsubadd213ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMSUBADD231PD_XMMdq_XMMdq_MEMdq	vfmsubadd231pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUBADD231PD_XMMdq_XMMdq_XMMdq	vfmsubadd231pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD231PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfmsubadd231pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUBADD231PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfmsubadd231pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD231PD_YMMqq_YMMqq_MEMqq	vfmsubadd231pd ymm1, ymm2, [rdi]	4	0.5

XED_IFORM_VFMSUBADD231PD_YMMqq_YMMqq_YMMqq	vfmsubadd231pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUBADD231PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfmsubadd231pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUBADD231PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfmsubadd231pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUBADD231PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfmsubadd231pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMSUBADD231PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfmsubadd231pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFMSUBADD231PS_XMMdq_XMMdq_MEMdq	vfmsubadd231ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUBADD231PS_XMMdq_XMMdq_XMMdq	vfmsubadd231ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD231PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfmsubadd231ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFMSUBADD231PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfmsubadd231ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFMSUBADD231PS_YMMqq_YMMqq_MEMqq	vfmsubadd231ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUBADD231PS_YMMqq_YMMqq_YMMqq	vfmsubadd231ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUBADD231PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfmsubadd231ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFMSUBADD231PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfmsubadd231ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFMSUBADD231PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfmsubadd231ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFMSUBADD231PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfmsubadd231ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMADD132PD_XMMdq_XMMdq_MEMdq	vfnmadd132pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD132PD_XMMdq_XMMdq_XMMdq	vfnmadd132pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD132PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfnmadd132pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD132PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfnmadd132pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD132PD_YMMqq_YMMqq_MEMqq	vfnmadd132pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMADD132PD_YMMqq_YMMqq_YMMqq	vfnmadd132pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFNMADD132PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfnmadd132pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMADD132PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfnmadd132pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFNMADD132PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfnmadd132pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFNMADD132PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfnmadd132pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMADD132PS_XMMdq_XMMdq_MEMdq	vfnmadd132ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD132PS_XMMdq_XMMdq_XMMdq	vfnmadd132ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD132PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfnmadd132ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD132PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfnmadd132ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD132PS_YMMqq_YMMqq_MEMqq	vfnmadd132ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMADD132PS_YMMqq_YMMqq_YMMqq	vfnmadd132ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFNMADD132PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfnmadd132ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMADD132PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfnmadd132ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFNMADD132PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfnmadd132ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFNMADD132PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfnmadd132ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMADD132SD_XMMdq_XMMq_MEMq	vfnmadd132sd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFNMADD132SD_XMMdq_XMMq_XMMq	vfnmadd132sd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD132SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfnmadd132sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD132SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfnmadd132sd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD132SS_XMMdq_XMMd_MEMd	vfnmadd132ss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFNMADD132SS_XMMdq_XMMd_XMMd	vfnmadd132ss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD132SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfnmadd132ss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD132SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfnmadd132ss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD213PD_XMMdq_XMMdq_MEMdq	vfnmadd213pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD213PD_XMMdq_XMMdq_XMMdq	vfnmadd213pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD213PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfnmadd213pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD213PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfnmadd213pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD213PD_YMMqq_YMMqq_MEMqq	vfnmadd213pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMADD213PD_YMMqq_YMMqq_YMMqq	vfnmadd213pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFNMADD213PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfnmadd213pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMADD213PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfnmadd213pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFNMADD213PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfnmadd213pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFNMADD213PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfnmadd213pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMADD213PS_XMMdq_XMMdq_MEMdq	vfnmadd213ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD213PS_XMMdq_XMMdq_XMMdq	vfnmadd213ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD213PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfnmadd213ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD213PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfnmadd213ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD213PS_YMMqq_YMMqq_MEMqq	vfnmadd213ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMADD213PS_YMMqq_YMMqq_YMMqq	vfnmadd213ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFNMADD213PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfnmadd213ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMADD213PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfnmadd213ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFNMADD213PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfnmadd213ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFNMADD213PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfnmadd213ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMADD213SD_XMMdq_XMMq_MEMq	vfnmadd213sd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFNMADD213SD_XMMdq_XMMq_XMMq	vfnmadd213sd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD213SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfnmadd213sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD213SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfnmadd213sd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD213SS_XMMdq_XMMd_MEMd	vfnmadd213ss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFNMADD213SS_XMMdq_XMMd_XMMd	vfnmadd213ss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD213SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfnmadd213ss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD213SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfnmadd213ss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD231PD_XMMdq_XMMdq_MEMdq	vfnmadd231pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD231PD_XMMdq_XMMdq_XMMdq	vfnmadd231pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD231PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfnmadd231pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD231PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfnmadd231pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD231PD_YMMqq_YMMqq_MEMqq	vfnmadd231pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMADD231PD_YMMqq_YMMqq_YMMqq	vfnmadd231pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFNMADD231PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfnmadd231pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMADD231PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfnmadd231pd ymm1{k1}, ymm2, ymm3	4	0.5

XED_IFORM_VFNMADD231PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfnmadd231pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFNMADD231PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfnmadd231pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMADD231PS_XMMdq_XMMdq_MEMdq	vfnmadd231ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD231PS_XMMdq_XMMdq_XMMdq	vfnmadd231ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD231PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfnmadd231ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD231PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfnmadd231ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD231PS_YMMqq_YMMqq_MEMqq	vfnmadd231ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMADD231PS_YMMqq_YMMqq_YMMqq	vfnmadd231ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFNMADD231PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfnmadd231ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMADD231PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfnmadd231ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFNMADD231PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfnmadd231ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFNMADD231PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfnmadd231ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMADD231SD_XMMdq_XMMq_MEMq	vfnmadd231sd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFNMADD231SD_XMMdq_XMMq_XMMq	vfnmadd231sd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD231SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfnmadd231sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD231SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfnmadd231sd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD231SS_XMMdq_XMMd_MEMd	vfnmadd231ss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFNMADD231SS_XMMdq_XMMd_XMMd	vfnmadd231ss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMADD231SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfnmadd231ss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMADD231SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfnmadd231ss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB132PD_XMMdq_XMMdq_MEMdq	vfnmsub132pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB132PD_XMMdq_XMMdq_XMMdq	vfnmsub132pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB132PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfnmsub132pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB132PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfnmsub132pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB132PD_YMMqq_YMMqq_MEMqq	vfnmsub132pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMSUB132PD_YMMqq_YMMqq_YMMqq	vfnmsub132pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFNMSUB132PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfnmsub132pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMSUB132PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfnmsub132pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFNMSUB132PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfnmsub132pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFNMSUB132PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfnmsub132pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMSUB132PS_XMMdq_XMMdq_MEMdq	vfnmsub132ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB132PS_XMMdq_XMMdq_XMMdq	vfnmsub132ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB132PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfnmsub132ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB132PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfnmsub132ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB132PS_YMMqq_YMMqq_MEMqq	vfnmsub132ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMSUB132PS_YMMqq_YMMqq_YMMqq	vfnmsub132ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFNMSUB132PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfnmsub132ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMSUB132PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfnmsub132ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFNMSUB132PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfnmsub132ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFNMSUB132PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfnmsub132ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMSUB132SD_XMMdq_XMMq_MEMq	vfnmsub132sd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFNMSUB132SD_XMMdq_XMMq_XMMq	vfnmsub132sd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB132SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfnmsub132sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB132SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfnmsub132sd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB132SS_XMMdq_XMMd_MEMd	vfnmsub132ss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFNMSUB132SS_XMMdq_XMMd_XMMd	vfnmsub132ss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB132SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfnmsub132ss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB132SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfnmsub132ss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB213PD_XMMdq_XMMdq_MEMdq	vfnmsub213pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB213PD_XMMdq_XMMdq_XMMdq	vfnmsub213pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB213PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfnmsub213pd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB213PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfnmsub213pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB213PD_YMMqq_YMMqq_MEMqq	vfnmsub213pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMSUB213PD_YMMqq_YMMqq_YMMqq	vfnmsub213pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFNMSUB213PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfnmsub213pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMSUB213PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfnmsub213pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFNMSUB213PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfnmsub213pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFNMSUB213PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfnmsub213pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMSUB213PS_XMMdq_XMMdq_MEMdq	vfnmsub213ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB213PS_XMMdq_XMMdq_XMMdq	vfnmsub213ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB213PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfnmsub213ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB213PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfnmsub213ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB213PS_YMMqq_YMMqq_MEMqq	vfnmsub213ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMSUB213PS_YMMqq_YMMqq_YMMqq	vfnmsub213ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFNMSUB213PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfnmsub213ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMSUB213PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfnmsub213ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFNMSUB213PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfnmsub213ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFNMSUB213PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfnmsub213ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMSUB213SD_XMMdq_XMMq_MEMq	vfnmsub213sd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFNMSUB213SD_XMMdq_XMMq_XMMq	vfnmsub213sd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB213SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfnmsub213sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB213SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfnmsub213sd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB213SS_XMMdq_XMMd_MEMd	vfnmsub213ss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFNMSUB213SS_XMMdq_XMMd_XMMd	vfnmsub213ss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB213SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfnmsub213ss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB213SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfnmsub213ss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB231PD_XMMdq_XMMdq_MEMdq	vfnmsub231pd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB231PD_XMMdq_XMMdq_XMMdq	vfnmsub231pd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB231PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfnmsub231pd xmm1{k1}, xmm2, [rdi]	10	0.5

XED_IFORM_VFNMSUB231PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfnmsub231pd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB231PD_YMMqq_YMMqq_MEMqq	vfnmsub231pd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMSUB231PD_YMMqq_YMMqq_YMMqq	vfnmsub231pd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFNMSUB231PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vfnmsub231pd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMSUB231PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vfnmsub231pd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFNMSUB231PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vfnmsub231pd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFNMSUB231PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vfnmsub231pd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMSUB231PS_XMMdq_XMMdq_MEMdq	vfnmsub231ps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB231PS_XMMdq_XMMdq_XMMdq	vfnmsub231ps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB231PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfnmsub231ps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB231PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfnmsub231ps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB231PS_YMMqq_YMMqq_MEMqq	vfnmsub231ps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMSUB231PS_YMMqq_YMMqq_YMMqq	vfnmsub231ps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VFNMSUB231PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vfnmsub231ps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VFNMSUB231PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vfnmsub231ps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VFNMSUB231PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vfnmsub231ps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VFNMSUB231PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vfnmsub231ps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VFNMSUB231SD_XMMdq_XMMq_MEMq	vfnmsub231sd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFNMSUB231SD_XMMdq_XMMq_XMMq	vfnmsub231sd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB231SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vfnmsub231sd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB231SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vfnmsub231sd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB231SS_XMMdq_XMMd_MEMd	vfnmsub231ss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VFNMSUB231SS_XMMdq_XMMd_XMMd	vfnmsub231ss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VFNMSUB231SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vfnmsub231ss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VFNMSUB231SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vfnmsub231ss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VFPCLASSPD_MASKmskw_MASKmskw_XMMf64_IMM8_AVX512	vfpclasspd k1{k1}, xmm1, 1	3	1
XED_IFORM_VFPCLASSPD_MASKmskw_MASKmskw_YMMf64_IMM8_AVX512	vfpclasspd k1{k1}, ymm1, 1	3	1
XED_IFORM_VFPCLASSPD_MASKmskw_MASKmskw_ZMMf64_IMM8_AVX512	vfpclasspd k1{k1}, zmm1, 1	3	1
XED_IFORM_VFPCLASSPS_MASKmskw_MASKmskw_XMMf32_IMM8_AVX512	vfpclassps k1{k1}, xmm1, 1	3	1
XED_IFORM_VFPCLASSPS_MASKmskw_MASKmskw_YMMf32_IMM8_AVX512	vfpclassps k1{k1}, ymm1, 1	3	1
XED_IFORM_VFPCLASSPS_MASKmskw_MASKmskw_ZMMf32_IMM8_AVX512	vfpclassps k1{k1}, zmm1, 1	3	1
XED_IFORM_VFPCLASSSD_MASKmskw_MASKmskw_MEMf64_IMM8_AVX512	vfpclasssd k1{k1}, [rdi], 1	8	1
XED_IFORM_VFPCLASSSD_MASKmskw_MASKmskw_XMMf64_IMM8_AVX512	vfpclasssd k1{k1}, xmm1, 1	3	1
XED_IFORM_VFPCLASSSS_MASKmskw_MASKmskw_MEMf32_IMM8_AVX512	vfpclassss k1{k1}, [rdi], 1	9	1
XED_IFORM_VFPCLASSSS_MASKmskw_MASKmskw_XMMf32_IMM8_AVX512	vfpclassss k1{k1}, xmm1, 1	3	1
XED_IFORM_VGATHERDPD_XMMf64_MEMdq_XMMi64_VL128	vgatherdpd xmm1, [rdi+xmm2*1], xmm3	22	2
XED_IFORM_VGATHERDPD_XMMf64_MASKmskw_MEMf64_AVX512_VL128	vgatherdpd xmm1{k1}, [rdi+xmm2*1]	22	2
XED_IFORM_VGATHERDPD_YMMf64_MEMqq_YMMi64_VL256	vgatherdpd ymm1, [rdi+xmm2*1], ymm3	25	4
XED_IFORM_VGATHERDPD_YMMf64_MASKmskw_MEMf64_AVX512_VL256	vgatherdpd ymm1{k1}, [rdi+xmm2*1]	25	4
XED_IFORM_VGATHERDPD_ZMMf64_MASKmskw_MEMf64_AVX512_VL512	vgatherdpd zmm1{k1}, [rdi+ymm2*1]	26	5
XED_IFORM_VGATHERDPS_YMMf32_MEMqq_YMMi32_VL256	vgatherdps ymm1, [rdi+ymm2*1], ymm3	27	5
XED_IFORM_VGATHERDPS_YMMf32_MASKmskw_MEMf32_AVX512_VL256	vgatherdps ymm1{k1}, [rdi+ymm2*1]	27	5
XED_IFORM_VGATHERDPS_ZMMf32_MASKmskw_MEMf32_AVX512_VL512	vgatherdps zmm1{k1}, [rdi+zmm2*1]	30	9.75
XED_IFORM_VGATHERQPD_XMMf64_MEMdq_XMMi64_VL128	vgatherqpd xmm1, [rdi+xmm2*1], xmm3	22	2
XED_IFORM_VGATHERQPD_XMMf64_MASKmskw_MEMf64_AVX512_VL128	vgatherqpd xmm1{k1}, [rdi+xmm2*1]	22	2
XED_IFORM_VGATHERQPD_YMMf64_MEMqq_YMMi64_VL256	vgatherqpd ymm1, [rdi+ymm2*1], ymm3	25	4
XED_IFORM_VGATHERQPD_YMMf64_MASKmskw_MEMf64_AVX512_VL256	vgatherqpd ymm1{k1}, [rdi+ymm2*1]	25	4
XED_IFORM_VGATHERQPD_ZMMf64_MASKmskw_MEMf64_AVX512_VL512	vgatherqpd zmm1{k1}, [rdi+zmm2*1]	26	5
XED_IFORM_VGATHERQPS_XMMf32_MEMq_XMMi32_VL128	vgatherqps xmm1, [rdi+xmm2*1], xmm3	20	2
XED_IFORM_VGATHERQPS_XMMf32_MEMdq_XMMi32_VL256	vgatherqps xmm1, [rdi+xmm2*1], xmm3	20	2
XED_IFORM_VGATHERQPS_XMMf32_MASKmskw_MEMf32_AVX512_VL256	vgatherqps xmm1{k1}, [rdi+xmm2*1]	20	2
XED_IFORM_VGATHERQPS_XMMf32_MASKmskw_MEMf32_AVX512_VL128	vgatherqps xmm1{k1}, [rdi+xmm2*1]	20	2
XED_IFORM_VGETEXPPD_XMMf64_MASKmskw_MEMf64_AVX512	vgetexppd xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VGETEXPPD_XMMf64_MASKmskw_XMMf64_AVX512	vgetexppd xmm1{k1}, xmm2	4	0.5
XED_IFORM_VGETEXPPD_YMMf64_MASKmskw_MEMf64_AVX512	vgetexppd ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VGETEXPPD_YMMf64_MASKmskw_YMMf64_AVX512	vgetexppd ymm1{k1}, ymm2	4	0.5
XED_IFORM_VGETEXPPD_ZMMf64_MASKmskw_MEMf64_AVX512	vgetexppd zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VGETEXPPD_ZMMf64_MASKmskw_ZMMf64_AVX512	vgetexppd zmm1{k1}, zmm2	4	0.5
XED_IFORM_VGETEXPPS_XMMf32_MASKmskw_MEMf32_AVX512	vgetexpps xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VGETEXPPS_XMMf32_MASKmskw_XMMf32_AVX512	vgetexpps xmm1{k1}, xmm2	4	0.5
XED_IFORM_VGETEXPPS_YMMf32_MASKmskw_MEMf32_AVX512	vgetexpps ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VGETEXPPS_YMMf32_MASKmskw_YMMf32_AVX512	vgetexpps ymm1{k1}, ymm2	4	0.5
XED_IFORM_VGETEXPPS_ZMMf32_MASKmskw_MEMf32_AVX512	vgetexpps zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VGETEXPPS_ZMMf32_MASKmskw_ZMMf32_AVX512	vgetexpps zmm1{k1}, zmm2	4	0.5
XED_IFORM_VGETEXPSD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vgetexpsd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VGETEXPSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vgetexpsd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VGETEXPSS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vgetexpss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VGETEXPSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vgetexpss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VGETMANTPD_XMMf64_MASKmskw_MEMf64_IMM8_AVX512	vgetmantpd xmm1{k1}, [rdi], 1	10	0.5
XED_IFORM_VGETMANTPD_XMMf64_MASKmskw_XMMf64_IMM8_AVX512	vgetmantpd xmm1{k1}, xmm2, 1	4	0.5
XED_IFORM_VGETMANTPD_YMMf64_MASKmskw_MEMf64_IMM8_AVX512	vgetmantpd ymm1{k1}, [rdi], 1	4	0.5
XED_IFORM_VGETMANTPD_YMMf64_MASKmskw_YMMf64_IMM8_AVX512	vgetmantpd ymm1{k1}, ymm2, 1	4	0.5
XED_IFORM_VGETMANTPD_ZMMf64_MASKmskw_MEMf64_IMM8_AVX512	vgetmantpd zmm1{k1}, [rdi], 1	11	0.5
XED_IFORM_VGETMANTPD_ZMMf64_MASKmskw_ZMMf64_IMM8_AVX512	vgetmantpd zmm1{k1}, zmm2, 1	4	0.5
XED_IFORM_VGETMANTPS_XMMf32_MASKmskw_MEMf32_IMM8_AVX512	vgetmantps xmm1{k1}, [rdi], 1	10	0.5
XED_IFORM_VGETMANTPS_XMMf32_MASKmskw_XMMf32_IMM8_AVX512	vgetmantps xmm1{k1}, xmm2, 1	4	0.5
XED_IFORM_VGETMANTPS_YMMf32_MASKmskw_MEMf32_IMM8_AVX512	vgetmantps ymm1{k1}, [rdi], 1	4	0.5
XED_IFORM_VGETMANTPS_YMMf32_MASKmskw_YMMf32_IMM8_AVX512	vgetmantps ymm1{k1}, ymm2, 1	4	0.5
XED_IFORM_VGETMANTPS_ZMMf32_MASKmskw_MEMf32_IMM8_AVX512	vgetmantps zmm1{k1}, [rdi], 1	11	0.5

XED_IFORM_VGETMANTPS_ZMMf32_MASKmskw_ZMMf32_IMM8_AVX512	vgetmantps zmm1{k1}, zmm2, 1	4	0.5
XED_IFORM_VGETMANTSD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vgetmantsd xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VGETMANTSD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vgetmantsd xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VGETMANTSS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vgetmantss xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VGETMANTSS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vgetmantss xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_HADDPD_XMMpd_MEMpd	vhaddpd xmm1, xmm1, [rdi]	12	2
XED_IFORM_HADDPD_XMMpd_XMMpd	vhaddpd xmm1, xmm1, xmm2	6	2
XED_IFORM_VHADDPD_XMMdq_XMMdq_MEMdq	vhaddpd xmm1, xmm2, [rdi]	12	2
XED_IFORM_VHADDPD_XMMdq_XMMdq_XMMdq	vhaddpd xmm1, xmm2, xmm3	6	2
XED_IFORM_VHADDPD_YMMqq_YMMqq_MEMqq	vhaddpd ymm1, ymm2, [rdi]	6	2
XED_IFORM_VHADDPD_YMMqq_YMMqq_YMMqq	vhaddpd ymm1, ymm2, ymm3	6	2
XED_IFORM_HADDPS_XMMps_MEMps	vhaddps xmm1, xmm1, [rdi]	12	2
XED_IFORM_HADDPS_XMMps_XMMps	vhaddps xmm1, xmm1, xmm2	6	2
XED_IFORM_VHADDPS_XMMdq_XMMdq_MEMdq	vhaddps xmm1, xmm2, [rdi]	12	2
XED_IFORM_VHADDPS_XMMdq_XMMdq_XMMdq	vhaddps xmm1, xmm2, xmm3	6	2
XED_IFORM_VHADDPS_YMMqq_YMMqq_MEMqq	vhaddps ymm1, ymm2, [rdi]	6	2
XED_IFORM_VHADDPS_YMMqq_YMMqq_YMMqq	vhaddps ymm1, ymm2, ymm3	6	2
XED_IFORM_HSUBPD_XMMpd_MEMpd	vhsubpd xmm1, xmm1, [rdi]	12	2
XED_IFORM_HSUBPD_XMMpd_XMMpd	vhsubpd xmm1, xmm1, xmm2	6	2
XED_IFORM_VHSUBPD_XMMdq_XMMdq_MEMdq	vhsubpd xmm1, xmm2, [rdi]	12	2
XED_IFORM_VHSUBPD_XMMdq_XMMdq_XMMdq	vhsubpd xmm1, xmm2, xmm3	6	2
XED_IFORM_VHSUBPD_YMMqq_YMMqq_MEMqq	vhsubpd ymm1, ymm2, [rdi]	6	2
XED_IFORM_VHSUBPD_YMMqq_YMMqq_YMMqq	vhsubpd ymm1, ymm2, ymm3	6	2
XED_IFORM_HSUBPS_XMMps_MEMps	vhsubps xmm1, xmm1, [rdi]	12	2
XED_IFORM_HSUBPS_XMMps_XMMps	vhsubps xmm1, xmm1, xmm2	6	2
XED_IFORM_VHSUBPS_XMMdq_XMMdq_MEMdq	vhsubps xmm1, xmm2, [rdi]	12	2
XED_IFORM_VHSUBPS_XMMdq_XMMdq_XMMdq	vhsubps xmm1, xmm2, xmm3	6	2
XED_IFORM_VHSUBPS_YMMqq_YMMqq_MEMqq	vhsubps ymm1, ymm2, [rdi]	6	2
XED_IFORM_VHSUBPS_YMMqq_YMMqq_YMMqq	vhsubps ymm1, ymm2, ymm3	6	2
XED_IFORM_VINSERTF128_YMMqq_YMMqq_MEMdq_IMMb	vinsertf128 ymm1, ymm2, [rdi], 1	7	0.5
XED_IFORM_VINSERTF128_YMMqq_YMMqq_XMMdq_IMMb	vinsertf128 ymm1, ymm2, xmm3, 1	3	1
XED_IFORM_VINSERTF32X4_YMMf32_MASKmskw_YMMf32_MEMf32_IMM8_AVX512	vinsertf32x4 ymm1{k1}, ymm2, [rdi], 1	1	0.5
XED_IFORM_VINSERTF32X4_YMMf32_MASKmskw_YMMf32_XMMf32_IMM8_AVX512	vinsertf32x4 ymm1{k1}, ymm2, xmm3, 1	3	1
XED_IFORM_VINSERTF32X4_ZMMf32_MASKmskw_ZMMf32_MEMf32_IMM8_AVX512	vinsertf32x4 zmm1{k1}, zmm2, [rdi], 1	8	0.5
XED_IFORM_VINSERTF32X4_ZMMf32_MASKmskw_ZMMf32_XMMf32_IMM8_AVX512	vinsertf32x4 zmm1{k1}, zmm2, xmm3, 1	3	1
XED_IFORM_VINSERTF32X8_ZMMf32_MASKmskw_ZMMf32_MEMf32_IMM8_AVX512	vinsertf32x8 zmm1{k1}, zmm2, [rdi], 1	8	0.5
XED_IFORM_VINSERTF32X8_ZMMf32_MASKmskw_ZMMf32_YMMf32_IMM8_AVX512	vinsertf32x8 zmm1{k1}, zmm2, ymm3, 1	3	1
XED_IFORM_VINSERTF64X2_YMMf64_MASKmskw_YMMf64_MEMf64_IMM8_AVX512	vinsertf64x2 ymm1{k1}, ymm2, [rdi], 1	1	0.5
XED_IFORM_VINSERTF64X2_YMMf64_MASKmskw_YMMf64_XMMf64_IMM8_AVX512	vinsertf64x2 ymm1{k1}, ymm2, xmm3, 1	3	1
XED_IFORM_VINSERTF64X2_ZMMf64_MASKmskw_ZMMf64_MEMf64_IMM8_AVX512	vinsertf64x2 zmm1{k1}, zmm2, [rdi], 1	8	0.5
XED_IFORM_VINSERTF64X2_ZMMf64_MASKmskw_ZMMf64_XMMf64_IMM8_AVX512	vinsertf64x2 zmm1{k1}, zmm2, xmm3, 1	3	1
XED_IFORM_VINSERTF64X4_ZMMf64_MASKmskw_ZMMf64_MEMf64_IMM8_AVX512	vinsertf64x4 zmm1{k1}, zmm2, [rdi], 1	8	0.5
XED_IFORM_VINSERTF64X4_ZMMf64_MASKmskw_ZMMf64_YMMf64_IMM8_AVX512	vinsertf64x4 zmm1{k1}, zmm2, ymm3, 1	3	1
XED_IFORM_VINSERTI128_YMMqq_YMMqq_MEMdq_IMMb	vinserti128 ymm1, ymm2, [rdi], 1	7	0.5
XED_IFORM_VINSERTI128_YMMqq_YMMqq_XMMdq_IMMb	vinserti128 ymm1, ymm2, xmm3, 1	3	1
XED_IFORM_VINSERTI32X4_YMMu32_MASKmskw_YMMu32_MEMu32_IMM8_AVX512	vinserti32x4 ymm1{k1}, ymm2, [rdi], 1	1	0.5
XED_IFORM_VINSERTI32X4_YMMu32_MASKmskw_YMMu32_XMMu32_IMM8_AVX512	vinserti32x4 ymm1{k1}, ymm2, xmm3, 1	3	1
XED_IFORM_VINSERTI32X4_ZMMu32_MASKmskw_ZMMu32_MEMu32_IMM8_AVX512	vinserti32x4 zmm1{k1}, zmm2, [rdi], 1	8	0.5
XED_IFORM_VINSERTI32X4_ZMMu32_MASKmskw_ZMMu32_XMMu32_IMM8_AVX512	vinserti32x4 zmm1{k1}, zmm2, xmm3, 1	3	1
XED_IFORM_VINSERTI32X8_ZMMu32_MASKmskw_ZMMu32_MEMu32_IMM8_AVX512	vinserti32x8 zmm1{k1}, zmm2, [rdi], 1	8	0.5
XED_IFORM_VINSERTI32X8_ZMMu32_MASKmskw_ZMMu32_YMMu32_IMM8_AVX512	vinserti32x8 zmm1{k1}, zmm2, ymm3, 1	3	1
XED_IFORM_VINSERTI64X2_YMMu64_MASKmskw_YMMu64_MEMu64_IMM8_AVX512	vinserti64x2 ymm1{k1}, ymm2, [rdi], 1	1	0.5
XED_IFORM_VINSERTI64X2_YMMu64_MASKmskw_YMMu64_XMMu64_IMM8_AVX512	vinserti64x2 ymm1{k1}, ymm2, xmm3, 1	3	1
XED_IFORM_VINSERTI64X2_ZMMu64_MASKmskw_ZMMu64_MEMu64_IMM8_AVX512	vinserti64x2 zmm1{k1}, zmm2, [rdi], 1	8	0.5
XED_IFORM_VINSERTI64X2_ZMMu64_MASKmskw_ZMMu64_XMMu64_IMM8_AVX512	vinserti64x2 zmm1{k1}, zmm2, xmm3, 1	3	1
XED_IFORM_VINSERTI64X4_ZMMu64_MASKmskw_ZMMu64_MEMu64_IMM8_AVX512	vinserti64x4 zmm1{k1}, zmm2, [rdi], 1	8	0.5
XED_IFORM_VINSERTI64X4_ZMMu64_MASKmskw_ZMMu64_YMMu64_IMM8_AVX512	vinserti64x4 zmm1{k1}, zmm2, ymm3, 1	3	1
XED_IFORM_INSERTPS_XMMps_MEMd_IMMb	vinsertps xmm1, xmm1, [rdi], 1	7	1
XED_IFORM_INSERTPS_XMMps_XMMps_IMMb	vinsertps xmm1, xmm1, xmm2, 1	1	1
XED_IFORM_VINSERTPS_XMMf32_XMMf32_MEMf32_IMM8_AVX512	vinsertps xmm1, xmm2, [rdi], 1	7	1
XED_IFORM_VINSERTPS_XMMdq_XMMdq_MEMd_IMMb	vinsertps xmm1, xmm2, [rdi], 1	7	1
XED_IFORM_VINSERTPS_XMMdq_XMMdq_XMMdq_IMMb	vinsertps xmm1, xmm2, xmm3, 1	1	1
XED_IFORM_VINSERTPS_XMMf32_XMMf32_XMMf32_IMM8_AVX512	vinsertps xmm1, xmm2, xmm3, 1	1	1
XED_IFORM_VLDDQU_XMMdq_MEMdq	vlddqu xmm1, [rdi]	6	0.5
XED_IFORM_LDDQU_XMMpd_MEMdq	vlddqu xmm1, [rdi]	6	0.5
XED_IFORM_VLDDQU_YMMqq_MEMqq	vlddqu ymm1, [rdi]	0	0.5
XED_IFORM_VLDMXCSR_MEMd	vldmxcsr [rdi]	7	1
XED_IFORM_LDMXCSR_MEMd	vldmxcsr [rdi]	7	1
XED_IFORM_MASKMOVDQU_XMMdq_XMMdq	vmaskmovdqu xmm1, xmm2	6	1
XED_IFORM_VMASKMOVDQU_XMMdq_XMMdq	vmaskmovdqu xmm1, xmm2	6	1
XED_IFORM_VMASKMOVPD_MEMdq_XMMdq_XMMdq	vmaskmovpd [rdi], xmm1, xmm2	6	1
XED_IFORM_VMASKMOVPD_MEMqq_YMMqq_YMMqq	vmaskmovpd [rdi], ymm1, ymm2	6	1
XED_IFORM_VMASKMOVPD_XMMdq_XMMdq_MEMdq	vmaskmovpd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VMASKMOVPD_YMMqq_YMMqq_MEMqq	vmaskmovpd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VMASKMOVPS_MEMdq_XMMdq_XMMdq	vmaskmovps [rdi], xmm1, xmm2	6	1
XED_IFORM_VMASKMOVPS_MEMqq_YMMqq_YMMqq	vmaskmovps [rdi], ymm1, ymm2	6	1
XED_IFORM_VMASKMOVPS_XMMdq_XMMdq_MEMdq	vmaskmovps xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VMASKMOVPS_YMMqq_YMMqq_MEMqq	vmaskmovps ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_MAXPD_XMMpd_MEMpd	vmaxpd xmm1, xmm1, [rdi]	10	0.5

XED_IFORM_MAXPD_XMMpd_XMMpd	vmaxpd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VMAXPD_XMMdq_XMMdq_MEMdq	vmaxpd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VMAXPD_XMMdq_XMMdq_XMMdq	vmaxpd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VMAXPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vmaxpd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VMAXPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vmaxpd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VMAXPD_YMMqq_YMMqq_MEMqq	vmaxpd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VMAXPD_YMMqq_YMMqq_YMMqq	vmaxpd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VMAXPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vmaxpd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VMAXPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vmaxpd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VMAXPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vmaxpd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VMAXPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vmaxpd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_MAXPS_XMMps_MEMps	vmaxps xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_MAXPS_XMMps_XMMps	vmaxps xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VMAXPS_XMMdq_XMMdq_MEMdq	vmaxps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VMAXPS_XMMdq_XMMdq_XMMdq	vmaxps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VMAXPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vmaxps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VMAXPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vmaxps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VMAXPS_YMMqq_YMMqq_MEMqq	vmaxps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VMAXPS_YMMqq_YMMqq_YMMqq	vmaxps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VMAXPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vmaxps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VMAXPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vmaxps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VMAXPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vmaxps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VMAXPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vmaxps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_MAXSD_XMMsd_MEMsd	vmaxsd xmm1, xmm1, [rdi]	9	0.5
XED_IFORM_MAXSD_XMMsd_XMMsd	vmaxsd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VMAXSD_XMMdq_XMMdq_MEMq	vmaxsd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VMAXSD_XMMdq_XMMdq_XMMq	vmaxsd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VMAXSD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vmaxsd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VMAXSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vmaxsd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_MAXSS_XMMss_MEMss	vmaxss xmm1, xmm1, [rdi]	9	0.5
XED_IFORM_MAXSS_XMMss_XMMss	vmaxss xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VMAXSS_XMMdq_XMMdq_MEMd	vmaxss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VMAXSS_XMMdq_XMMdq_XMMd	vmaxss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VMAXSS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vmaxss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VMAXSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vmaxss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VMCLEAR_MEMq	vmclear [rdi]	40	3.75
XED_IFORM_MINPD_XMMpd_MEMpd	vminpd xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_MINPD_XMMpd_XMMpd	vminpd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VMINPD_XMMdq_XMMdq_MEMdq	vminpd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VMINPD_XMMdq_XMMdq_XMMdq	vminpd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VMINPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vminpd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VMINPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vminpd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VMINPD_YMMqq_YMMqq_MEMqq	vminpd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VMINPD_YMMqq_YMMqq_YMMqq	vminpd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VMINPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vminpd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VMINPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vminpd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VMINPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vminpd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VMINPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vminpd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_MINPS_XMMps_MEMps	vminps xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_MINPS_XMMps_XMMps	vminps xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VMINPS_XMMdq_XMMdq_MEMdq	vminps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VMINPS_XMMdq_XMMdq_XMMdq	vminps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VMINPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vminps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VMINPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vminps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VMINPS_YMMqq_YMMqq_MEMqq	vminps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VMINPS_YMMqq_YMMqq_YMMqq	vminps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VMINPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vminps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VMINPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vminps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VMINPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vminps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VMINPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vminps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_MINSD_XMMsd_MEMsd	vminsd xmm1, xmm1, [rdi]	9	0.5
XED_IFORM_MINSD_XMMsd_XMMsd	vminsd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VMINSD_XMMdq_XMMdq_MEMq	vminsd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VMINSD_XMMdq_XMMdq_XMMq	vminsd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VMINSD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vminsd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VMINSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vminsd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_MINSS_XMMss_MEMss	vminss xmm1, xmm1, [rdi]	9	0.5
XED_IFORM_MINSS_XMMss_XMMss	vminss xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VMINSS_XMMdq_XMMdq_MEMd	vminss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VMINSS_XMMdq_XMMdq_XMMd	vminss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VMINSS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vminss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VMINSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vminss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VMOVAPD_MEMdq_XMMdq	vmovapd [rdi], xmm1	5	1
XED_IFORM_MOVAPD_MEMpd_XMMpd	vmovapd [rdi], xmm1	5	1
XED_IFORM_VMOVAPD_MEMqq_YMMqq	vmovapd [rdi], ymm1	5	1
XED_IFORM_VMOVAPD_MEMf64_MASKmskw_XMMf64_AVX512	vmovapd [rdi]{k1}, xmm1	5	1
XED_IFORM_VMOVAPD_MEMf64_MASKmskw_YMMf64_AVX512	vmovapd [rdi]{k1}, ymm1	5	1
XED_IFORM_VMOVAPD_MEMf64_MASKmskw_ZMMf64_AVX512	vmovapd [rdi]{k1}, zmm1	5	1
XED_IFORM_MOVAPD_XMMpd_MEMpd	vmovapd xmm1, [rdi]	6	0.5

XED_IFORM_VMOVAPD_XMMdq_MEMdq	vmovapd xmm1, [rdi]	6	0.5
XED_IFORM_VMOVAPD_XMMdq_XMMdq_28	vmovapd xmm1, xmm2	0	0.25
XED_IFORM_MOVAPD_XMMpd_XMMpd_0F29	vmovapd xmm1, xmm2	0	0.25
XED_IFORM_MOVAPD_XMMpd_XMMpd_0F28	vmovapd xmm1, xmm2	0	0.25
XED_IFORM_VMOVAPD_XMMdq_XMMdq_29	vmovapd xmm1, xmm2	0	0.25
XED_IFORM_VMOVAPD_XMMf64_MASKmskw_MEMf64_AVX512	vmovapd xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVAPD_XMMf64_MASKmskw_XMMf64_AVX512	vmovapd xmm1{k1}, xmm2	1	0.33
XED_IFORM_VMOVAPD_YMMqq_MEMqq	vmovapd ymm1, [rdi]	0	0.5
XED_IFORM_VMOVAPD_YMMqq_YMMqq_29	vmovapd ymm1, ymm2	0	0.25
XED_IFORM_VMOVAPD_YMMqq_YMMqq_28	vmovapd ymm1, ymm2	0	0.25
XED_IFORM_VMOVAPD_YMMf64_MASKmskw_MEMf64_AVX512	vmovapd ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVAPD_YMMf64_MASKmskw_YMMf64_AVX512	vmovapd ymm1{k1}, ymm2	1	0.33
XED_IFORM_VMOVAPD_ZMMf64_MASKmskw_MEMf64_AVX512	vmovapd zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VMOVAPD_ZMMf64_MASKmskw_ZMMf64_AVX512	vmovapd zmm1{k1}, zmm2	1	0.5
XED_IFORM_VMOVAPS_MEMdq_XMMdq	vmovaps [rdi], xmm1	5	1
XED_IFORM_MOVAPS_MEMps_XMMps	vmovaps [rdi], xmm1	5	1
XED_IFORM_VMOVAPS_MEMqq_YMMqq	vmovaps [rdi], ymm1	5	1
XED_IFORM_VMOVAPS_MEMf32_MASKmskw_XMMf32_AVX512	vmovaps [rdi]{k1}, xmm1	5	1
XED_IFORM_VMOVAPS_MEMf32_MASKmskw_YMMf32_AVX512	vmovaps [rdi]{k1}, ymm1	5	1
XED_IFORM_VMOVAPS_MEMf32_MASKmskw_ZMMf32_AVX512	vmovaps [rdi]{k1}, zmm1	5	1
XED_IFORM_MOVAPS_XMMps_MEMps	vmovaps xmm1, [rdi]	6	0.5
XED_IFORM_VMOVAPS_XMMdq_MEMdq	vmovaps xmm1, [rdi]	6	0.5
XED_IFORM_MOVAPS_XMMps_XMMps_0F29	vmovaps xmm1, xmm2	0	0.25
XED_IFORM_MOVAPS_XMMps_XMMps_0F28	vmovaps xmm1, xmm2	0	0.25
XED_IFORM_VMOVAPS_XMMdq_XMMdq_29	vmovaps xmm1, xmm2	0	0.25
XED_IFORM_VMOVAPS_XMMdq_XMMdq_28	vmovaps xmm1, xmm2	0	0.25
XED_IFORM_VMOVAPS_XMMf32_MASKmskw_MEMf32_AVX512	vmovaps xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVAPS_XMMf32_MASKmskw_XMMf32_AVX512	vmovaps xmm1{k1}, xmm2	1	0.33
XED_IFORM_VMOVAPS_YMMqq_MEMqq	vmovaps ymm1, [rdi]	0	0.5
XED_IFORM_VMOVAPS_YMMqq_YMMqq_28	vmovaps ymm1, ymm2	0	0.25
XED_IFORM_VMOVAPS_YMMqq_YMMqq_29	vmovaps ymm1, ymm2	0	0.25
XED_IFORM_VMOVAPS_YMMf32_MASKmskw_MEMf32_AVX512	vmovaps ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVAPS_YMMf32_MASKmskw_YMMf32_AVX512	vmovaps ymm1{k1}, ymm2	1	0.33
XED_IFORM_VMOVAPS_ZMMf32_MASKmskw_MEMf32_AVX512	vmovaps zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VMOVAPS_ZMMf32_MASKmskw_ZMMf32_AVX512	vmovaps zmm1{k1}, zmm2	1	0.5
XED_IFORM_VMOVD_MEMu32_XMMu32_AVX512	vmovd [rdi], xmm1	5	1
XED_IFORM_MOVD_MEMd_XMMd	vmovd [rdi], xmm1	5	1
XED_IFORM_VMOVD_MEMd_XMMd	vmovd [rdi], xmm1	5	1
XED_IFORM_MOVD_GPR32_XMMd	vmovd eax, xmm1	2	1
XED_IFORM_VMOVD_GPR32u32_XMMu32_AVX512	vmovd eax, xmm1	2	1
XED_IFORM_VMOVD_GPR32d_XMMd	vmovd eax, xmm1	2	1
XED_IFORM_VMOVD_XMMdq_MEMd	vmovd xmm1, [rdi]	5	0.5
XED_IFORM_MOVD_XMMdq_MEMd	vmovd xmm1, [rdi]	5	0.5
XED_IFORM_VMOVD_XMMu32_MEMu32_AVX512	vmovd xmm1, [rdi]	5	0.5
XED_IFORM_VMOVD_XMMdq_GPR32d	vmovd xmm1, eax	1	1
XED_IFORM_MOVD_XMMdq_GPR32	vmovd xmm1, eax	1	1
XED_IFORM_VMOVD_XMMu32_GPR32u32_AVX512	vmovd xmm1, eax	1	1
XED_IFORM_MOVDDUP_XMMdq_MEMq	vmovddup xmm1, [rdi]	5	0.5
XED_IFORM_VMOVDDUP_XMMdq_MEMq	vmovddup xmm1, [rdi]	5	0.5
XED_IFORM_MOVDDUP_XMMdq_XMMq	vmovddup xmm1, xmm2	1	1
XED_IFORM_VMOVDDUP_XMMdq_XMMdq	vmovddup xmm1, xmm2	1	1
XED_IFORM_VMOVDDUP_XMMf64_MASKmskw_MEMf64_AVX512	vmovddup xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVDDUP_XMMf64_MASKmskw_XMMf64_AVX512	vmovddup xmm1{k1}, xmm2	1	1
XED_IFORM_VMOVDDUP_YMMqq_MEMqq	vmovddup ymm1, [rdi]	0	0.5
XED_IFORM_VMOVDDUP_YMMqq_YMMqq	vmovddup ymm1, ymm2	1	1
XED_IFORM_VMOVDDUP_YMMf64_MASKmskw_MEMf64_AVX512	vmovddup ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVDDUP_YMMf64_MASKmskw_YMMf64_AVX512	vmovddup ymm1{k1}, ymm2	1	1
XED_IFORM_VMOVDDUP_ZMMf64_MASKmskw_MEMf64_AVX512	vmovddup zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VMOVDDUP_ZMMf64_MASKmskw_ZMMf64_AVX512	vmovddup zmm1{k1}, zmm2	1	1
XED_IFORM_VMOVDQA_MEMdq_XMMdq	vmovdqa [rdi], xmm1	5	1
XED_IFORM_MOVDQA_MEMdq_XMMdq	vmovdqa [rdi], xmm1	5	1
XED_IFORM_VMOVDQA_MEMqq_YMMqq	vmovdqa [rdi], ymm1	5	1
XED_IFORM_VMOVDQA_XMMdq_MEMdq	vmovdqa xmm1, [rdi]	6	0.5
XED_IFORM_MOVDQA_XMMdq_MEMdq	vmovdqa xmm1, [rdi]	6	0.5
XED_IFORM_MOVDQA_XMMdq_XMMdq_0F6F	vmovdqa xmm1, xmm2	0	0.25
XED_IFORM_VMOVDQA_XMMdq_XMMdq_7F	vmovdqa xmm1, xmm2	0	0.25
XED_IFORM_MOVDQA_XMMdq_XMMdq_0F7F	vmovdqa xmm1, xmm2	0	0.25
XED_IFORM_VMOVDQA_XMMdq_XMMdq_6F	vmovdqa xmm1, xmm2	0	0.25
XED_IFORM_VMOVDQA_YMMqq_MEMqq	vmovdqa ymm1, [rdi]	0	0.5
XED_IFORM_VMOVDQA_YMMqq_YMMqq_6F	vmovdqa ymm1, ymm2	0	0.25
XED_IFORM_VMOVDQA_YMMqq_YMMqq_7F	vmovdqa ymm1, ymm2	0	0.25
XED_IFORM_VMOVDQA32_MEMu32_MASKmskw_XMMu32_AVX512	vmovdqa32 [rdi]{k1}, xmm1	5	1
XED_IFORM_VMOVDQA32_MEMu32_MASKmskw_YMMu32_AVX512	vmovdqa32 [rdi]{k1}, ymm1	5	1
XED_IFORM_VMOVDQA32_MEMu32_MASKmskw_ZMMu32_AVX512	vmovdqa32 [rdi]{k1}, zmm1	5	1
XED_IFORM_VMOVDQA32_XMMu32_MASKmskw_MEMu32_AVX512	vmovdqa32 xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVDQA32_XMMu32_MASKmskw_XMMu32_AVX512	vmovdqa32 xmm1{k1}, xmm2	1	0.33
XED_IFORM_VMOVDQA32_YMMu32_MASKmskw_MEMu32_AVX512	vmovdqa32 ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVDQA32_YMMu32_MASKmskw_YMMu32_AVX512	vmovdqa32 ymm1{k1}, ymm2	1	0.33
XED_IFORM_VMOVDQA32_ZMMu32_MASKmskw_MEMu32_AVX512	vmovdqa32 zmm1{k1}, [rdi]	8	0.5

XED_IFORM_VMOVDQA32_ZMMu32_MASKmskw_ZMMu32_AVX512	vmovdqa32 zmm1{k1}, zmm2	1	0.5
XED_IFORM_VMOVDQA64_MEMu64_MASKmskw_XMMu64_AVX512	vmovdqa64 [rdi]{k1}, xmm1	5	1
XED_IFORM_VMOVDQA64_MEMu64_MASKmskw_YMMu64_AVX512	vmovdqa64 [rdi]{k1}, ymm1	5	1
XED_IFORM_VMOVDQA64_MEMu64_MASKmskw_ZMMu64_AVX512	vmovdqa64 [rdi]{k1}, zmm1	5	1
XED_IFORM_VMOVDQA64_XMMu64_MASKmskw_MEMu64_AVX512	vmovdqa64 xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVDQA64_XMMu64_MASKmskw_XMMu64_AVX512	vmovdqa64 xmm1{k1}, xmm2	1	0.33
XED_IFORM_VMOVDQA64_YMMu64_MASKmskw_MEMu64_AVX512	vmovdqa64 ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVDQA64_YMMu64_MASKmskw_YMMu64_AVX512	vmovdqa64 ymm1{k1}, ymm2	1	0.33
XED_IFORM_VMOVDQA64_ZMMu64_MASKmskw_MEMu64_AVX512	vmovdqa64 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VMOVDQA64_ZMMu64_MASKmskw_ZMMu64_AVX512	vmovdqa64 zmm1{k1}, zmm2	1	0.5
XED_IFORM_VMOVDQU_MEMdq_XMMdq	vmovdqu [rdi], xmm1	5	1
XED_IFORM_MOVDQU_MEMdq_XMMdq	vmovdqu [rdi], xmm1	5	1
XED_IFORM_VMOVDQU_MEMqq_YMMqq	vmovdqu [rdi], ymm1	5	1
XED_IFORM_VMOVDQU_XMMdq_MEMdq	vmovdqu xmm1, [rdi]	6	0.5
XED_IFORM_MOVDQU_XMMdq_MEMdq	vmovdqu xmm1, [rdi]	6	0.5
XED_IFORM_MOVDQU_XMMdq_XMMdq_0F7F	vmovdqu xmm1, xmm2	0	0.25
XED_IFORM_VMOVDQU_XMMdq_XMMdq_7F	vmovdqu xmm1, xmm2	0	0.25
XED_IFORM_VMOVDQU_XMMdq_XMMdq_6F	vmovdqu xmm1, xmm2	0	0.25
XED_IFORM_MOVDQU_XMMdq_XMMdq_0F6F	vmovdqu xmm1, xmm2	0	0.25
XED_IFORM_VMOVDQU_YMMqq_MEMqq	vmovdqu ymm1, [rdi]	0	0.5
XED_IFORM_VMOVDQU_YMMqq_YMMqq_7F	vmovdqu ymm1, ymm2	0	0.25
XED_IFORM_VMOVDQU_YMMqq_YMMqq_6F	vmovdqu ymm1, ymm2	0	0.25
XED_IFORM_VMOVDQU16_MEMu16_MASKmskw_XMMu16_AVX512	vmovdqu16 [rdi]{k1}, xmm1	5	1
XED_IFORM_VMOVDQU16_MEMu16_MASKmskw_YMMu16_AVX512	vmovdqu16 [rdi]{k1}, ymm1	5	1
XED_IFORM_VMOVDQU16_MEMu16_MASKmskw_ZMMu16_AVX512	vmovdqu16 [rdi]{k1}, zmm1	5	1
XED_IFORM_VMOVDQU16_XMMu16_MASKmskw_MEMu16_AVX512	vmovdqu16 xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVDQU16_XMMu16_MASKmskw_XMMu16_AVX512	vmovdqu16 xmm1{k1}, xmm2	1	0.33
XED_IFORM_VMOVDQU16_YMMu16_MASKmskw_MEMu16_AVX512	vmovdqu16 ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVDQU16_YMMu16_MASKmskw_YMMu16_AVX512	vmovdqu16 ymm1{k1}, ymm2	1	0.33
XED_IFORM_VMOVDQU16_ZMMu16_MASKmskw_MEMu16_AVX512	vmovdqu16 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VMOVDQU16_ZMMu16_MASKmskw_ZMMu16_AVX512	vmovdqu16 zmm1{k1}, zmm2	1	0.5
XED_IFORM_VMOVDQU32_MEMu32_MASKmskw_XMMu32_AVX512	vmovdqu32 [rdi]{k1}, xmm1	5	1
XED_IFORM_VMOVDQU32_MEMu32_MASKmskw_YMMu32_AVX512	vmovdqu32 [rdi]{k1}, ymm1	5	1
XED_IFORM_VMOVDQU32_MEMu32_MASKmskw_ZMMu32_AVX512	vmovdqu32 [rdi]{k1}, zmm1	5	1
XED_IFORM_VMOVDQU32_XMMu32_MASKmskw_MEMu32_AVX512	vmovdqu32 xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVDQU32_XMMu32_MASKmskw_XMMu32_AVX512	vmovdqu32 xmm1{k1}, xmm2	1	0.33
XED_IFORM_VMOVDQU32_YMMu32_MASKmskw_MEMu32_AVX512	vmovdqu32 ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVDQU32_YMMu32_MASKmskw_YMMu32_AVX512	vmovdqu32 ymm1{k1}, ymm2	1	0.33
XED_IFORM_VMOVDQU32_ZMMu32_MASKmskw_MEMu32_AVX512	vmovdqu32 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VMOVDQU32_ZMMu32_MASKmskw_ZMMu32_AVX512	vmovdqu32 zmm1{k1}, zmm2	1	0.5
XED_IFORM_VMOVDQU64_MEMu64_MASKmskw_XMMu64_AVX512	vmovdqu64 [rdi]{k1}, xmm1	5	1
XED_IFORM_VMOVDQU64_MEMu64_MASKmskw_YMMu64_AVX512	vmovdqu64 [rdi]{k1}, ymm1	5	1
XED_IFORM_VMOVDQU64_MEMu64_MASKmskw_ZMMu64_AVX512	vmovdqu64 [rdi]{k1}, zmm1	5	1
XED_IFORM_VMOVDQU64_XMMu64_MASKmskw_MEMu64_AVX512	vmovdqu64 xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVDQU64_XMMu64_MASKmskw_XMMu64_AVX512	vmovdqu64 xmm1{k1}, xmm2	1	0.33
XED_IFORM_VMOVDQU64_YMMu64_MASKmskw_MEMu64_AVX512	vmovdqu64 ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVDQU64_YMMu64_MASKmskw_YMMu64_AVX512	vmovdqu64 ymm1{k1}, ymm2	1	0.33
XED_IFORM_VMOVDQU64_ZMMu64_MASKmskw_MEMu64_AVX512	vmovdqu64 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VMOVDQU64_ZMMu64_MASKmskw_ZMMu64_AVX512	vmovdqu64 zmm1{k1}, zmm2	1	0.5
XED_IFORM_VMOVDQU8_MEMu8_MASKmskw_XMMu8_AVX512	vmovdqu8 [rdi]{k1}, xmm1	5	1
XED_IFORM_VMOVDQU8_MEMu8_MASKmskw_YMMu8_AVX512	vmovdqu8 [rdi]{k1}, ymm1	5	1
XED_IFORM_VMOVDQU8_MEMu8_MASKmskw_ZMMu8_AVX512	vmovdqu8 [rdi]{k1}, zmm1	6	1
XED_IFORM_VMOVDQU8_XMMu8_MASKmskw_MEMu8_AVX512	vmovdqu8 xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVDQU8_XMMu8_MASKmskw_XMMu8_AVX512	vmovdqu8 xmm1{k1}, xmm2	1	0.33
XED_IFORM_VMOVDQU8_YMMu8_MASKmskw_MEMu8_AVX512	vmovdqu8 ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVDQU8_YMMu8_MASKmskw_YMMu8_AVX512	vmovdqu8 ymm1{k1}, ymm2	1	0.33
XED_IFORM_VMOVDQU8_ZMMu8_MASKmskw_MEMu8_AVX512	vmovdqu8 zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VMOVDQU8_ZMMu8_MASKmskw_ZMMu8_AVX512	vmovdqu8 zmm1{k1}, zmm2	1	0.5
XED_IFORM_MOVHLPS_XMMq_XMMq	vmovhlps xmm1, xmm1, xmm2	1	1
XED_IFORM_VMOVHLPS_XMMdq_XMMdq_XMMdq	vmovhlps xmm1, xmm2, xmm3	1	1
XED_IFORM_VMOVHLPS_XMMf32_XMMf32_XMMf32_AVX512	vmovhlps xmm1, xmm2, xmm3	1	1
XED_IFORM_VMOVHPD_MEMq_XMMdq	vmovhpd [rdi], xmm1	5	1
XED_IFORM_VMOVHPD_MEMf64_XMMf64_AVX512	vmovhpd [rdi], xmm1	5	1
XED_IFORM_MOVHPD_MEMq_XMMsd	vmovhpd [rdi], xmm1	5	1
XED_IFORM_MOVHPD_XMMsd_MEMq	vmovhpd xmm1, xmm1, [rdi]	6	1
XED_IFORM_VMOVHPD_XMMf64_XMMf64_MEMf64_AVX512	vmovhpd xmm1, xmm2, [rdi]	6	1
XED_IFORM_VMOVHPD_XMMdq_XMMq_MEMq	vmovhpd xmm1, xmm2, [rdi]	6	1
XED_IFORM_VMOVHPS_MEMq_XMMdq	vmovhps [rdi], xmm1	5	1
XED_IFORM_MOVHPS_MEMq_XMMps	vmovhps [rdi], xmm1	5	1
XED_IFORM_VMOVHPS_MEMf32_XMMf32_AVX512	vmovhps [rdi], xmm1	5	1
XED_IFORM_MOVHPS_XMMq_MEMq	vmovhps xmm1, xmm1, [rdi]	6	1
XED_IFORM_VMOVHPS_XMMdq_XMMq_MEMq	vmovhps xmm1, xmm2, [rdi]	6	1
XED_IFORM_VMOVHPS_XMMf32_XMMf32_MEMf32_AVX512	vmovhps xmm1, xmm2, [rdi]	6	1
XED_IFORM_MOVLHPS_XMMq_XMMq	vmovlhps xmm1, xmm1, xmm2	1	1
XED_IFORM_VMOVLHPS_XMMf32_XMMf32_XMMf32_AVX512	vmovlhps xmm1, xmm2, xmm3	1	1
XED_IFORM_VMOVLHPS_XMMdq_XMMq_XMMq	vmovlhps xmm1, xmm2, xmm3	1	1
XED_IFORM_MOVLPD_MEMq_XMMsd	vmovlpd [rdi], xmm1	5	1
XED_IFORM_VMOVLPD_MEMf64_XMMf64_AVX512	vmovlpd [rdi], xmm1	5	1
XED_IFORM_VMOVLPD_MEMq_XMMq	vmovlpd [rdi], xmm1	5	1

XED_IFORM_MOVLPD_XMMsd_MEMq	vmovlpd xmm1, xmm1, [rdi]	6	1
XED_IFORM_VMOVLPD_XMMf64_XMMf64_MEMf64_AVX512	vmovlpd xmm1, xmm2, [rdi]	6	1
XED_IFORM_VMOVLPD_XMMdq_XMMdq_MEMq	vmovlpd xmm1, xmm2, [rdi]	6	1
XED_IFORM_MOVLPS_MEMq_XMMps	vmovlps [rdi], xmm1	5	1
XED_IFORM_VMOVLPS_MEMq_XMMq	vmovlps [rdi], xmm1	5	1
XED_IFORM_VMOVLPS_MEMf32_XMMf32_AVX512	vmovlps [rdi], xmm1	5	1
XED_IFORM_MOVLPS_XMMq_MEMq	vmovlps xmm1, xmm1, [rdi]	6	1
XED_IFORM_VMOVLPS_XMMdq_XMMdq_MEMq	vmovlps xmm1, xmm2, [rdi]	6	1
XED_IFORM_VMOVLPS_XMMf32_XMMf32_MEMf32_AVX512	vmovlps xmm1, xmm2, [rdi]	6	1
XED_IFORM_MOVMSKPD_GPR32_XMMpd	vmovmskpd eax, xmm1	2	1
XED_IFORM_VMOVMSKPD_GPR32d_XMMdq	vmovmskpd eax, xmm1	2	1
XED_IFORM_VMOVMSKPD_GPR32d_YMMqq	vmovmskpd eax, ymm1	2	1
XED_IFORM_MOVMSKPS_GPR32_XMMps	vmovmskps eax, xmm1	2	1
XED_IFORM_VMOVMSKPS_GPR32d_XMMdq	vmovmskps eax, xmm1	2	1
XED_IFORM_VMOVMSKPS_GPR32d_YMMqq	vmovmskps eax, ymm1	2	1
XED_IFORM_MOVNTDQ_MEMdq_XMMdq	vmovntdq [rdi], xmm1	5	1
XED_IFORM_VMOVNTDQ_MEMdq_XMMdq	vmovntdq [rdi], xmm1	5	1
XED_IFORM_VMOVNTDQ_MEMu32_XMMu32_AVX512	vmovntdq [rdi], xmm1	5	1
XED_IFORM_VMOVNTDQ_MEMu32_YMMu32_AVX512	vmovntdq [rdi], ymm1	5	1
XED_IFORM_VMOVNTDQ_MEMqq_YMMqq	vmovntdq [rdi], ymm1	5	1
XED_IFORM_VMOVNTDQ_MEMu32_ZMMu32_AVX512	vmovntdq [rdi], zmm1	5	1
XED_IFORM_VMOVNTDQA_XMMdq_MEMdq	vmovntdqa xmm1, [rdi]	6	0.5
XED_IFORM_MOVNTDQA_XMMdq_MEMdq	vmovntdqa xmm1, [rdi]	6	0.5
XED_IFORM_VMOVNTDQA_XMMu32_MEMu32_AVX512	vmovntdqa xmm1, [rdi]	6	0.5
XED_IFORM_VMOVNTDQA_YMMu32_MEMu32_AVX512	vmovntdqa ymm1, [rdi]	0	0.5
XED_IFORM_VMOVNTDQA_YMMqq_MEMqq	vmovntdqa ymm1, [rdi]	0	0.5
XED_IFORM_VMOVNTDQA_ZMMu32_MEMu32_AVX512	vmovntdqa zmm1, [rdi]	7	0.5
XED_IFORM_MOVNTPD_MEMdq_XMMpd	vmovntpd [rdi], xmm1	5	1
XED_IFORM_VMOVNTPD_MEMdq_XMMdq	vmovntpd [rdi], xmm1	5	1
XED_IFORM_VMOVNTPD_MEMf64_XMMf64_AVX512	vmovntpd [rdi], xmm1	5	1
XED_IFORM_VMOVNTPD_MEMf64_YMMf64_AVX512	vmovntpd [rdi], ymm1	5	1
XED_IFORM_VMOVNTPD_MEMqq_YMMqq	vmovntpd [rdi], ymm1	5	1
XED_IFORM_VMOVNTPD_MEMf64_ZMMf64_AVX512	vmovntpd [rdi], zmm1	5	1
XED_IFORM_VMOVNTPS_MEMdq_XMMdq	vmovntps [rdi], xmm1	5	1
XED_IFORM_VMOVNTPS_MEMf32_XMMf32_AVX512	vmovntps [rdi], xmm1	5	1
XED_IFORM_MOVNTPS_MEMdq_XMMps	vmovntps [rdi], xmm1	5	1
XED_IFORM_VMOVNTPS_MEMf32_YMMf32_AVX512	vmovntps [rdi], ymm1	5	1
XED_IFORM_VMOVNTPS_MEMqq_YMMqq	vmovntps [rdi], ymm1	5	1
XED_IFORM_VMOVNTPS_MEMf32_ZMMf32_AVX512	vmovntps [rdi], zmm1	5	1
XED_IFORM_MOVQ_MEMq_XMMq_0FD6	vmovq [rdi], xmm1	5	1
XED_IFORM_VMOVQ_MEMq_XMMq_7E	vmovq [rdi], xmm1	5	1
XED_IFORM_VMOVQ_MEMq_XMMq_D6	vmovq [rdi], xmm1	5	1
XED_IFORM_VMOVQ_MEMu64_XMMu64_AVX512	vmovq [rdi], xmm1	5	1
XED_IFORM_MOVQ_MEMq_XMMq_0F7E	vmovq [rdi], xmm1	5	1
XED_IFORM_VMOVQ_GPR64q_XMMq	vmovq rax, xmm1	2	1
XED_IFORM_MOVQ_GPR64_XMMq	vmovq rax, xmm1	2	1
XED_IFORM_VMOVQ_GPR64u64_XMMu64_AVX512	vmovq rax, xmm1	2	1
XED_IFORM_MOVQ_XMMdq_MEMq_0F6E	vmovq xmm1, [rdi]	5	0.5
XED_IFORM_VMOVQ_XMMdq_MEMq_7E	vmovq xmm1, [rdi]	5	0.5
XED_IFORM_MOVQ_XMMdq_MEMq_0F7E	vmovq xmm1, [rdi]	5	0.5
XED_IFORM_VMOVQ_XMMdq_MEMq_6E	vmovq xmm1, [rdi]	5	0.5
XED_IFORM_VMOVQ_XMMu64_MEMu64_AVX512	vmovq xmm1, [rdi]	5	0.5
XED_IFORM_MOVQ_XMMdq_GPR64	vmovq xmm1, rax	1	1
XED_IFORM_VMOVQ_XMMdq_GPR64q	vmovq xmm1, rax	1	1
XED_IFORM_VMOVQ_XMMu64_GPR64u64_AVX512	vmovq xmm1, rax	1	1
XED_IFORM_VMOVQ_XMMdq_XMMq_7E	vmovq xmm1, xmm2	1	0.33
XED_IFORM_MOVQ_XMMdq_XMMq_0F7E	vmovq xmm1, xmm2	1	0.33
XED_IFORM_MOVQ_XMMdq_XMMq_0FD6	vmovq xmm1, xmm2	1	0.33
XED_IFORM_VMOVQ_XMMu64_XMMu64_AVX512	vmovq xmm1, xmm2	1	0.33
XED_IFORM_VMOVQ_XMMdq_XMMq_D6	vmovq xmm1, xmm2	1	0.33
XED_IFORM_MOVSD_XMM_MEMsd_XMMsd	vmovsd [rdi], xmm1	5	1
XED_IFORM_VMOVSD_MEMq_XMMq	vmovsd [rdi], xmm1	5	1
XED_IFORM_VMOVSD_MEMf64_MASKmskw_XMMf64_AVX512	vmovsd [rdi]{k1}, xmm1	5	1
XED_IFORM_VMOVSD_XMMdq_MEMq	vmovsd xmm1, [rdi]	5	0.5
XED_IFORM_MOVSD_XMM_XMMdq_MEMsd	vmovsd xmm1, [rdi]	5	0.5
XED_IFORM_MOVSD_XMM_XMMsd_XMMsd_0F10	vmovsd xmm1, xmm1, xmm2	1	1
XED_IFORM_MOVSD_XMM_XMMsd_XMMsd_0F11	vmovsd xmm1, xmm1, xmm2	1	1
XED_IFORM_VMOVSD_XMMdq_XMMdq_XMMq_10	vmovsd xmm1, xmm2, xmm3	1	1
XED_IFORM_VMOVSD_XMMdq_XMMdq_XMMq_11	vmovsd xmm1, xmm2, xmm3	1	1
XED_IFORM_VMOVSD_XMMf64_MASKmskw_MEMf64_AVX512	vmovsd xmm1{k1}, [rdi]	7	1
XED_IFORM_VMOVSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vmovsd xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VMOVSHDUP_XMMdq_MEMdq	vmovshdup xmm1, [rdi]	6	0.5
XED_IFORM_MOVSHDUP_XMMps_MEMps	vmovshdup xmm1, [rdi]	6	0.5
XED_IFORM_MOVSHDUP_XMMps_XMMps	vmovshdup xmm1, xmm2	1	1
XED_IFORM_VMOVSHDUP_XMMdq_XMMdq	vmovshdup xmm1, xmm2	1	1
XED_IFORM_VMOVSHDUP_XMMf32_MASKmskw_MEMf32_AVX512	vmovshdup xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVSHDUP_XMMf32_MASKmskw_XMMf32_AVX512	vmovshdup xmm1{k1}, xmm2	1	1
XED_IFORM_VMOVSHDUP_YMMqq_MEMqq	vmovshdup ymm1, [rdi]	0	0.5
XED_IFORM_VMOVSHDUP_YMMqq_YMMqq	vmovshdup ymm1, ymm2	1	1

XED_IFORM_VMOVSHDUP_YMMf32_MASKmskw_MEMf32_AVX512	vmovshdup ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVSHDUP_YMMf32_MASKmskw_YMMf32_AVX512	vmovshdup ymm1{k1}, ymm2	1	1
XED_IFORM_VMOVSHDUP_ZMMf32_MASKmskw_MEMf32_AVX512	vmovshdup zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VMOVSHDUP_ZMMf32_MASKmskw_ZMMf32_AVX512	vmovshdup zmm1{k1}, zmm2	1	1
XED_IFORM_VMOVSLDUP_XMMdq_MEMdq	vmovsldup xmm1, [rdi]	6	0.5
XED_IFORM_MOVSLDUP_XMMps_MEMps	vmovsldup xmm1, [rdi]	6	0.5
XED_IFORM_VMOVSLDUP_XMMdq_XMMdq	vmovsldup xmm1, xmm2	1	1
XED_IFORM_MOVSLDUP_XMMps_XMMps	vmovsldup xmm1, xmm2	1	1
XED_IFORM_VMOVSLDUP_XMMf32_MASKmskw_MEMf32_AVX512	vmovsldup xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVSLDUP_XMMf32_MASKmskw_XMMf32_AVX512	vmovsldup xmm1{k1}, xmm2	1	1
XED_IFORM_VMOVSLDUP_YMMqq_MEMqq	vmovsldup ymm1, [rdi]	0	0.5
XED_IFORM_VMOVSLDUP_YMMqq_YMMqq	vmovsldup ymm1, ymm2	1	1
XED_IFORM_VMOVSLDUP_YMMf32_MASKmskw_MEMf32_AVX512	vmovsldup ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVSLDUP_YMMf32_MASKmskw_YMMf32_AVX512	vmovsldup ymm1{k1}, ymm2	1	1
XED_IFORM_VMOVSLDUP_ZMMf32_MASKmskw_MEMf32_AVX512	vmovsldup zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VMOVSLDUP_ZMMf32_MASKmskw_ZMMf32_AVX512	vmovsldup zmm1{k1}, zmm2	1	1
XED_IFORM_VMOVSS_MEMd_XMMd	vmovss [rdi], xmm1	5	1
XED_IFORM_MOVSS_MEMss_XMMss	vmovss [rdi], xmm1	5	1
XED_IFORM_VMOVSS_MEMf32_MASKmskw_XMMf32_AVX512	vmovss [rdi]{k1}, xmm1	5	1
XED_IFORM_VMOVSS_XMMdq_MEMd	vmovss xmm1, [rdi]	5	0.5
XED_IFORM_MOVSS_XMMdq_MEMss	vmovss xmm1, [rdi]	5	0.5
XED_IFORM_MOVSS_XMMss_XMMss_0F11	vmovss xmm1, xmm1, xmm2	1	0.33
XED_IFORM_MOVSS_XMMss_XMMss_0F10	vmovss xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VMOVSS_XMMdq_XMMdq_XMMd_11	vmovss xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VMOVSS_XMMdq_XMMdq_XMMd_10	vmovss xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VMOVSS_XMMf32_MASKmskw_MEMf32_AVX512	vmovss xmm1{k1}, [rdi]	7	1
XED_IFORM_VMOVSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vmovss xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_MOVUPD_MEMpd_XMMpd	vmovupd [rdi], xmm1	5	1
XED_IFORM_VMOVUPD_MEMdq_XMMdq	vmovupd [rdi], xmm1	5	1
XED_IFORM_VMOVUPD_MEMqq_YMMqq	vmovupd [rdi], ymm1	5	1
XED_IFORM_VMOVUPD_MEMf64_MASKmskw_XMMf64_AVX512	vmovupd [rdi]{k1}, xmm1	5	1
XED_IFORM_VMOVUPD_MEMf64_MASKmskw_YMMf64_AVX512	vmovupd [rdi]{k1}, ymm1	5	1
XED_IFORM_VMOVUPD_MEMf64_MASKmskw_ZMMf64_AVX512	vmovupd [rdi]{k1}, zmm1	5	1
XED_IFORM_VMOVUPD_XMMdq_MEMdq	vmovupd xmm1, [rdi]	6	0.5
XED_IFORM_MOVUPD_XMMpd_MEMpd	vmovupd xmm1, [rdi]	6	0.5
XED_IFORM_VMOVUPD_XMMdq_XMMdq_11	vmovupd xmm1, xmm2	0	0.25
XED_IFORM_VMOVUPD_XMMdq_XMMdq_10	vmovupd xmm1, xmm2	0	0.25
XED_IFORM_MOVUPD_XMMpd_XMMpd_0F11	vmovupd xmm1, xmm2	0	0.25
XED_IFORM_MOVUPD_XMMpd_XMMpd_0F10	vmovupd xmm1, xmm2	0	0.25
XED_IFORM_VMOVUPD_XMMf64_MASKmskw_MEMf64_AVX512	vmovupd xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVUPD_XMMf64_MASKmskw_XMMf64_AVX512	vmovupd xmm1{k1}, xmm2	1	0.33
XED_IFORM_VMOVUPD_YMMqq_MEMqq	vmovupd ymm1, [rdi]	0	0.5
XED_IFORM_VMOVUPD_YMMqq_YMMqq_10	vmovupd ymm1, ymm2	0	0.25
XED_IFORM_VMOVUPD_YMMqq_YMMqq_11	vmovupd ymm1, ymm2	0	0.25
XED_IFORM_VMOVUPD_YMMf64_MASKmskw_MEMf64_AVX512	vmovupd ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVUPD_YMMf64_MASKmskw_YMMf64_AVX512	vmovupd ymm1{k1}, ymm2	1	0.33
XED_IFORM_VMOVUPD_ZMMf64_MASKmskw_MEMf64_AVX512	vmovupd zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VMOVUPD_ZMMf64_MASKmskw_ZMMf64_AVX512	vmovupd zmm1{k1}, zmm2	1	0.5
XED_IFORM_VMOVUPS_MEMdq_XMMdq	vmovups [rdi], xmm1	5	1
XED_IFORM_MOVUPS_MEMps_XMMps	vmovups [rdi], xmm1	5	1
XED_IFORM_VMOVUPS_MEMqq_YMMqq	vmovups [rdi], ymm1	5	1
XED_IFORM_VMOVUPS_MEMf32_MASKmskw_XMMf32_AVX512	vmovups [rdi]{k1}, xmm1	5	1
XED_IFORM_VMOVUPS_MEMf32_MASKmskw_YMMf32_AVX512	vmovups [rdi]{k1}, ymm1	5	1
XED_IFORM_VMOVUPS_MEMf32_MASKmskw_ZMMf32_AVX512	vmovups [rdi]{k1}, zmm1	5	1
XED_IFORM_MOVUPS_XMMps_MEMps	vmovups xmm1, [rdi]	6	0.5
XED_IFORM_VMOVUPS_XMMdq_MEMdq	vmovups xmm1, [rdi]	6	0.5
XED_IFORM_MOVUPS_XMMps_XMMps_0F10	vmovups xmm1, xmm2	0	0.25
XED_IFORM_VMOVUPS_XMMdq_XMMdq_10	vmovups xmm1, xmm2	0	0.25
XED_IFORM_MOVUPS_XMMps_XMMps_0F11	vmovups xmm1, xmm2	0	0.25
XED_IFORM_VMOVUPS_XMMdq_XMMdq_11	vmovups xmm1, xmm2	0	0.25
XED_IFORM_VMOVUPS_XMMf32_MASKmskw_MEMf32_AVX512	vmovups xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VMOVUPS_XMMf32_MASKmskw_XMMf32_AVX512	vmovups xmm1{k1}, xmm2	1	0.33
XED_IFORM_VMOVUPS_YMMqq_MEMqq	vmovups ymm1, [rdi]	0	0.5
XED_IFORM_VMOVUPS_YMMqq_YMMqq_10	vmovups ymm1, ymm2	0	0.25
XED_IFORM_VMOVUPS_YMMqq_YMMqq_11	vmovups ymm1, ymm2	0	0.25
XED_IFORM_VMOVUPS_YMMf32_MASKmskw_MEMf32_AVX512	vmovups ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VMOVUPS_YMMf32_MASKmskw_YMMf32_AVX512	vmovups ymm1{k1}, ymm2	1	0.33
XED_IFORM_VMOVUPS_ZMMf32_MASKmskw_MEMf32_AVX512	vmovups zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VMOVUPS_ZMMf32_MASKmskw_ZMMf32_AVX512	vmovups zmm1{k1}, zmm2	1	0.5
XED_IFORM_MPSADBW_XMMdq_MEMdq_IMMb	vmpsadbw xmm1, xmm1, [rdi], 1	10	2
XED_IFORM_MPSADBW_XMMdq_XMMdq_IMMb	vmpsadbw xmm1, xmm1, xmm2, 1	4	2
XED_IFORM_VMPSADBW_XMMdq_XMMdq_MEMdq_IMMb	vmpsadbw xmm1, xmm2, [rdi], 1	10	2
XED_IFORM_VMPSADBW_XMMdq_XMMdq_XMMdq_IMMb	vmpsadbw xmm1, xmm2, xmm3, 1	4	2
XED_IFORM_VMPSADBW_YMMqq_YMMqq_MEMqq_IMMb	vmpsadbw ymm1, ymm2, [rdi], 1	4	2
XED_IFORM_VMPSADBW_YMMqq_YMMqq_YMMqq_IMMb	vmpsadbw ymm1, ymm2, ymm3, 1	4	2
XED_IFORM_VMPTRST_MEMq	vmptrst [rdi]	5	1
XED_IFORM_MULPD_XMMpd_MEMpd	vmulpd xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_MULPD_XMMpd_XMMpd	vmulpd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VMULPD_XMMdq_XMMdq_MEMdq	vmulpd xmm1, xmm2, [rdi]	10	0.5

XED_IFORM_VMULPD_XMMdq_XMMdq_XMMdq	vmulpd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VMULPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vmulpd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VMULPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vmulpd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VMULPD_YMMqq_YMMqq_MEMqq	vmulpd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VMULPD_YMMqq_YMMqq_YMMqq	vmulpd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VMULPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vmulpd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VMULPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vmulpd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VMULPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vmulpd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VMULPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vmulpd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_MULPS_XMMps_MEMps	vmulps xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_MULPS_XMMps_XMMps	vmulps xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VMULPS_XMMdq_XMMdq_MEMdq	vmulps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VMULPS_XMMdq_XMMdq_XMMdq	vmulps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VMULPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vmulps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VMULPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vmulps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VMULPS_YMMqq_YMMqq_MEMqq	vmulps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VMULPS_YMMqq_YMMqq_YMMqq	vmulps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VMULPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vmulps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VMULPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vmulps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VMULPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vmulps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VMULPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vmulps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_MULSD_XMMsd_MEMsd	vmulsd xmm1, xmm1, [rdi]	9	0.5
XED_IFORM_MULSD_XMMsd_XMMsd	vmulsd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VMULSD_XMMdq_XMMdq_MEMq	vmulsd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VMULSD_XMMdq_XMMdq_XMMq	vmulsd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VMULSD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vmulsd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VMULSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vmulsd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_MULSS_XMMss_MEMss	vmulss xmm1, xmm1, [rdi]	9	0.5
XED_IFORM_MULSS_XMMss_XMMss	vmulss xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VMULSS_XMMdq_XMMdq_MEMd	vmulss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VMULSS_XMMdq_XMMdq_XMMd	vmulss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VMULSS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vmulss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VMULSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vmulss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_ORPD_XMMpd_MEMpd	vorpd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_ORPD_XMMpd_XMMpd	vorpd xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VORPD_XMMdq_XMMdq_MEMdq	vorpd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VORPD_XMMdq_XMMdq_XMMdq	vorpd xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VORPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vorpd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VORPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vorpd xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VORPD_YMMqq_YMMqq_MEMqq	vorpd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VORPD_YMMqq_YMMqq_YMMqq	vorpd ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VORPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vorpd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VORPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vorpd ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VORPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vorpd zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VORPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vorpd zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_ORPS_XMMps_MEMps	vorps xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_ORPS_XMMps_XMMps	vorps xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VORPS_XMMdq_XMMdq_MEMdq	vorps xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VORPS_XMMdq_XMMdq_XMMdq	vorps xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VORPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vorps xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VORPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vorps xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VORPS_YMMqq_YMMqq_MEMqq	vorps ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VORPS_YMMqq_YMMqq_YMMqq	vorps ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VORPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vorps ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VORPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vorps ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VORPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vorps zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VORPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vorps zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPABSB_XMMdq_MEMdq	vpabsb xmm1, [rdi]	7	0.5
XED_IFORM_PABSB_XMMdq_MEMdq	vpabsb xmm1, [rdi]	7	0.5
XED_IFORM_PABSB_XMMdq_XMMdq	vpabsb xmm1, xmm2	1	0.5
XED_IFORM_VPABSB_XMMdq_XMMdq	vpabsb xmm1, xmm2	1	0.5
XED_IFORM_VPABSB_XMMi8_MASKmskw_MEMi8_AVX512	vpabsb xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VPABSB_XMMi8_MASKmskw_XMMi8_AVX512	vpabsb xmm1{k1}, xmm2	1	0.5
XED_IFORM_VPABSB_YMMqq_MEMqq	vpabsb ymm1, [rdi]	1	0.5
XED_IFORM_VPABSB_YMMqq_YMMqq	vpabsb ymm1, ymm2	1	0.5
XED_IFORM_VPABSB_YMMi8_MASKmskw_MEMi8_AVX512	vpabsb ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VPABSB_YMMi8_MASKmskw_YMMi8_AVX512	vpabsb ymm1{k1}, ymm2	1	0.5
XED_IFORM_VPABSB_ZMMi8_MASKmskw_MEMi8_AVX512	vpabsb zmm1{k1}, [rdi]	8	1
XED_IFORM_VPABSB_ZMMi8_MASKmskw_ZMMi8_AVX512	vpabsb zmm1{k1}, zmm2	1	1
XED_IFORM_PABSD_XMMdq_MEMdq	vpabsd xmm1, [rdi]	7	0.5
XED_IFORM_VPABSD_XMMdq_MEMdq	vpabsd xmm1, [rdi]	7	0.5
XED_IFORM_VPABSD_XMMdq_XMMdq	vpabsd xmm1, xmm2	1	0.5
XED_IFORM_PABSD_XMMdq_XMMdq	vpabsd xmm1, xmm2	1	0.5
XED_IFORM_VPABSD_XMMi32_MASKmskw_MEMi32_AVX512	vpabsd xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VPABSD_XMMi32_MASKmskw_XMMi32_AVX512	vpabsd xmm1{k1}, xmm2	1	0.5
XED_IFORM_VPABSD_YMMqq_MEMqq	vpabsd ymm1, [rdi]	1	0.5
XED_IFORM_VPABSD_YMMqq_YMMqq	vpabsd ymm1, ymm2	1	0.5
XED_IFORM_VPABSD_YMMi32_MASKmskw_MEMi32_AVX512	vpabsd ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VPABSD_YMMi32_MASKmskw_YMMi32_AVX512	vpabsd ymm1{k1}, ymm2	1	0.5

XED_IFORM_VPABSD_ZMMi32_MASKmskw_MEMi32_AVX512	vpabsd zmm1{k1}, [rdi]	8	1
XED_IFORM_VPABSD_ZMMi32_MASKmskw_ZMMi32_AVX512	vpabsd zmm1{k1}, zmm2	1	1
XED_IFORM_VPABSQ_XMMi64_MASKmskw_MEMi64_AVX512	vpabsq xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VPABSQ_XMMi64_MASKmskw_XMMi64_AVX512	vpabsq xmm1{k1}, xmm2	1	0.5
XED_IFORM_VPABSQ_YMMi64_MASKmskw_MEMi64_AVX512	vpabsq ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VPABSQ_YMMi64_MASKmskw_YMMi64_AVX512	vpabsq ymm1{k1}, ymm2	1	0.5
XED_IFORM_VPABSQ_ZMMi64_MASKmskw_MEMi64_AVX512	vpabsq zmm1{k1}, [rdi]	8	1
XED_IFORM_VPABSQ_ZMMi64_MASKmskw_ZMMi64_AVX512	vpabsq zmm1{k1}, zmm2	1	1
XED_IFORM_VPABSW_XMMdq_MEMdq	vpabsw xmm1, [rdi]	7	0.5
XED_IFORM_PABSW_XMMdq_MEMdq	vpabsw xmm1, [rdi]	7	0.5
XED_IFORM_VPABSW_XMMdq_XMMdq	vpabsw xmm1, xmm2	1	0.5
XED_IFORM_PABSW_XMMdq_XMMdq	vpabsw xmm1, xmm2	1	0.5
XED_IFORM_VPABSW_XMMi16_MASKmskw_MEMi16_AVX512	vpabsw xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VPABSW_XMMi16_MASKmskw_XMMi16_AVX512	vpabsw xmm1{k1}, xmm2	1	0.5
XED_IFORM_VPABSW_YMMqq_MEMqq	vpabsw ymm1, [rdi]	1	0.5
XED_IFORM_VPABSW_YMMqq_YMMqq	vpabsw ymm1, ymm2	1	0.5
XED_IFORM_VPABSW_YMMi16_MASKmskw_MEMi16_AVX512	vpabsw ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VPABSW_YMMi16_MASKmskw_YMMi16_AVX512	vpabsw ymm1{k1}, ymm2	1	0.5
XED_IFORM_VPABSW_ZMMi16_MASKmskw_MEMi16_AVX512	vpabsw zmm1{k1}, [rdi]	8	1
XED_IFORM_VPABSW_ZMMi16_MASKmskw_ZMMi16_AVX512	vpabsw zmm1{k1}, zmm2	1	1
XED_IFORM_PACKSSDW_XMMdq_MEMdq	vpackssdw xmm1, xmm1, [rdi]	7	1
XED_IFORM_PACKSSDW_XMMdq_XMMdq	vpackssdw xmm1, xmm1, xmm2	1	1
XED_IFORM_VPACKSSDW_XMMdq_XMMdq_MEMdq	vpackssdw xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPACKSSDW_XMMdq_XMMdq_XMMdq	vpackssdw xmm1, xmm2, xmm3	1	1
XED_IFORM_VPACKSSDW_XMMi16_MASKmskw_XMMi32_MEMi32_AVX512	vpackssdw xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPACKSSDW_XMMi16_MASKmskw_XMMi32_XMMi32_AVX512	vpackssdw xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPACKSSDW_YMMqq_YMMqq_MEMqq	vpackssdw ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPACKSSDW_YMMqq_YMMqq_YMMqq	vpackssdw ymm1, ymm2, ymm3	1	1
XED_IFORM_VPACKSSDW_YMMi16_MASKmskw_YMMi32_MEMi32_AVX512	vpackssdw ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPACKSSDW_YMMi16_MASKmskw_YMMi32_YMMi32_AVX512	vpackssdw ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPACKSSDW_ZMMi16_MASKmskw_ZMMi32_MEMi32_AVX512	vpackssdw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPACKSSDW_ZMMi16_MASKmskw_ZMMi32_ZMMi32_AVX512	vpackssdw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PACKSSWB_XMMdq_MEMdq	vpacksswb xmm1, xmm1, [rdi]	7	1
XED_IFORM_PACKSSWB_XMMdq_XMMdq	vpacksswb xmm1, xmm1, xmm2	1	1
XED_IFORM_VPACKSSWB_XMMdq_XMMdq_MEMdq	vpacksswb xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPACKSSWB_XMMdq_XMMdq_XMMdq	vpacksswb xmm1, xmm2, xmm3	1	1
XED_IFORM_VPACKSSWB_XMMi8_MASKmskw_XMMi16_MEMi16_AVX512	vpacksswb xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPACKSSWB_XMMi8_MASKmskw_XMMi16_XMMi16_AVX512	vpacksswb xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPACKSSWB_YMMqq_YMMqq_MEMqq	vpacksswb ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPACKSSWB_YMMqq_YMMqq_YMMqq	vpacksswb ymm1, ymm2, ymm3	1	1
XED_IFORM_VPACKSSWB_YMMi8_MASKmskw_YMMi16_MEMi16_AVX512	vpacksswb ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPACKSSWB_YMMi8_MASKmskw_YMMi16_YMMi16_AVX512	vpacksswb ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPACKSSWB_ZMMi8_MASKmskw_ZMMi16_MEMi16_AVX512	vpacksswb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPACKSSWB_ZMMi8_MASKmskw_ZMMi16_ZMMi16_AVX512	vpacksswb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PACKUSDW_XMMdq_MEMdq	vpackusdw xmm1, xmm1, [rdi]	7	1
XED_IFORM_PACKUSDW_XMMdq_XMMdq	vpackusdw xmm1, xmm1, xmm2	1	1
XED_IFORM_VPACKUSDW_XMMdq_XMMdq_MEMdq	vpackusdw xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPACKUSDW_XMMdq_XMMdq_XMMdq	vpackusdw xmm1, xmm2, xmm3	1	1
XED_IFORM_VPACKUSDW_XMMu16_MASKmskw_XMMu32_MEMu32_AVX512	vpackusdw xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPACKUSDW_XMMu16_MASKmskw_XMMu32_XMMu32_AVX512	vpackusdw xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPACKUSDW_YMMqq_YMMqq_MEMqq	vpackusdw ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPACKUSDW_YMMqq_YMMqq_YMMqq	vpackusdw ymm1, ymm2, ymm3	1	1
XED_IFORM_VPACKUSDW_YMMu16_MASKmskw_YMMu32_MEMu32_AVX512	vpackusdw ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPACKUSDW_YMMu16_MASKmskw_YMMu32_YMMu32_AVX512	vpackusdw ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPACKUSDW_ZMMu16_MASKmskw_ZMMu32_MEMu32_AVX512	vpackusdw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPACKUSDW_ZMMu16_MASKmskw_ZMMu32_ZMMu32_AVX512	vpackusdw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PACKUSWB_XMMdq_MEMdq	vpackuswb xmm1, xmm1, [rdi]	7	1
XED_IFORM_PACKUSWB_XMMdq_XMMdq	vpackuswb xmm1, xmm1, xmm2	1	1
XED_IFORM_VPACKUSWB_XMMdq_XMMdq_MEMdq	vpackuswb xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPACKUSWB_XMMdq_XMMdq_XMMdq	vpackuswb xmm1, xmm2, xmm3	1	1
XED_IFORM_VPACKUSWB_XMMu8_MASKmskw_XMMu16_MEMu16_AVX512	vpackuswb xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPACKUSWB_XMMu8_MASKmskw_XMMu16_XMMu16_AVX512	vpackuswb xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPACKUSWB_YMMqq_YMMqq_MEMqq	vpackuswb ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPACKUSWB_YMMqq_YMMqq_YMMqq	vpackuswb ymm1, ymm2, ymm3	1	1
XED_IFORM_VPACKUSWB_YMMu8_MASKmskw_YMMu16_MEMu16_AVX512	vpackuswb ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPACKUSWB_YMMu8_MASKmskw_YMMu16_YMMu16_AVX512	vpackuswb ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPACKUSWB_ZMMu8_MASKmskw_ZMMu16_MEMu16_AVX512	vpackuswb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPACKUSWB_ZMMu8_MASKmskw_ZMMu16_ZMMu16_AVX512	vpackuswb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PADDB_XMMdq_MEMdq	vpaddb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PADDB_XMMdq_XMMdq	vpaddb xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPADDB_XMMdq_XMMdq_MEMdq	vpaddb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDB_XMMdq_XMMdq_XMMdq	vpaddb xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPADDB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpaddb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpaddb xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPADDB_YMMqq_YMMqq_MEMqq	vpaddb ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDB_YMMqq_YMMqq_YMMqq	vpaddb ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPADDB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpaddb ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpaddb ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPADDB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpaddb zmm1{k1}, zmm2, [rdi]	8	0.5

XED_IFORM_VPADDB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpaddb zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PADDD_XMMdq_MEMdq	vpaddd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PADDD_XMMdq_XMMdq	vpaddd xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPADDD_XMMdq_XMMdq_MEMdq	vpaddd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDD_XMMdq_XMMdq_XMMdq	vpaddd xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPADDD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpaddd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpaddd xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPADDD_YMMqq_YMMqq_MEMqq	vpaddd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDD_YMMqq_YMMqq_YMMqq	vpaddd ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPADDD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpaddd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpaddd ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPADDD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpaddd zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPADDD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpaddd zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PADDQ_XMMdq_MEMdq	vpaddq xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PADDQ_XMMdq_XMMdq	vpaddq xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPADDQ_XMMdq_XMMdq_MEMdq	vpaddq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDQ_XMMdq_XMMdq_XMMdq	vpaddq xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPADDQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpaddq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpaddq xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPADDQ_YMMqq_YMMqq_MEMqq	vpaddq ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDQ_YMMqq_YMMqq_YMMqq	vpaddq ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPADDQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpaddq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpaddq ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPADDQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpaddq zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPADDQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpaddq zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PADDSB_XMMdq_MEMdq	vpaddsb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PADDSB_XMMdq_XMMdq	vpaddsb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPADDSB_XMMdq_XMMdq_MEMdq	vpaddsb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDSB_XMMdq_XMMdq_XMMdq	vpaddsb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPADDSB_XMMi8_MASKmskw_XMMi8_MEMi8_AVX512	vpaddsb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDSB_XMMi8_MASKmskw_XMMi8_XMMi8_AVX512	vpaddsb xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPADDSB_YMMqq_YMMqq_MEMqq	vpaddsb ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDSB_YMMqq_YMMqq_YMMqq	vpaddsb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPADDSB_YMMi8_MASKmskw_YMMi8_MEMi8_AVX512	vpaddsb ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDSB_YMMi8_MASKmskw_YMMi8_YMMi8_AVX512	vpaddsb ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPADDSB_ZMMi8_MASKmskw_ZMMi8_MEMi8_AVX512	vpaddsb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPADDSB_ZMMi8_MASKmskw_ZMMi8_ZMMi8_AVX512	vpaddsb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PADDSW_XMMdq_MEMdq	vpaddsw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PADDSW_XMMdq_XMMdq	vpaddsw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPADDSW_XMMdq_XMMdq_MEMdq	vpaddsw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDSW_XMMdq_XMMdq_XMMdq	vpaddsw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPADDSW_XMMi16_MASKmskw_XMMi16_MEMi16_AVX512	vpaddsw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDSW_XMMi16_MASKmskw_XMMi16_XMMi16_AVX512	vpaddsw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPADDSW_YMMqq_YMMqq_MEMqq	vpaddsw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDSW_YMMqq_YMMqq_YMMqq	vpaddsw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPADDSW_YMMi16_MASKmskw_YMMi16_MEMi16_AVX512	vpaddsw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDSW_YMMi16_MASKmskw_YMMi16_YMMi16_AVX512	vpaddsw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPADDSW_ZMMi16_MASKmskw_ZMMi16_MEMi16_AVX512	vpaddsw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPADDSW_ZMMi16_MASKmskw_ZMMi16_ZMMi16_AVX512	vpaddsw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PADDUSB_XMMdq_MEMdq	vpaddusb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PADDUSB_XMMdq_XMMdq	vpaddusb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPADDUSB_XMMdq_XMMdq_MEMdq	vpaddusb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDUSB_XMMdq_XMMdq_XMMdq	vpaddusb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPADDUSB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpaddusb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDUSB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpaddusb xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPADDUSB_YMMqq_YMMqq_MEMqq	vpaddusb ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDUSB_YMMqq_YMMqq_YMMqq	vpaddusb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPADDUSB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpaddusb ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDUSB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpaddusb ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPADDUSB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpaddusb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPADDUSB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpaddusb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PADDUSW_XMMdq_MEMdq	vpaddusw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PADDUSW_XMMdq_XMMdq	vpaddusw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPADDUSW_XMMdq_XMMdq_MEMdq	vpaddusw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDUSW_XMMdq_XMMdq_XMMdq	vpaddusw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPADDUSW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpaddusw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDUSW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpaddusw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPADDUSW_YMMqq_YMMqq_MEMqq	vpaddusw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDUSW_YMMqq_YMMqq_YMMqq	vpaddusw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPADDUSW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpaddusw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDUSW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpaddusw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPADDUSW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpaddusw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPADDUSW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpaddusw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PADDW_XMMdq_MEMdq	vpaddw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PADDW_XMMdq_XMMdq	vpaddw xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPADDW_XMMdq_XMMdq_MEMdq	vpaddw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDW_XMMdq_XMMdq_XMMdq	vpaddw xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPADDW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpaddw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPADDW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpaddw xmm1{k1}, xmm2, xmm3	1	0.33

XED_IFORM_VPADDW_YMMqq_YMMqq_MEMqq	vpaddw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDW_YMMqq_YMMqq_YMMqq	vpaddw ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPADDW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpaddw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPADDW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpaddw ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPADDW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpaddw zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPADDW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpaddw zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PALIGNR_XMMdq_MEMdq_IMMb	vpalignr xmm1, xmm1, [rdi], 1	7	1
XED_IFORM_PALIGNR_XMMdq_XMMdq_IMMb	vpalignr xmm1, xmm1, xmm2, 1	1	1
XED_IFORM_VPALIGNR_XMMdq_XMMdq_MEMdq_IMMb	vpalignr xmm1, xmm2, [rdi], 1	7	1
XED_IFORM_VPALIGNR_XMMdq_XMMdq_XMMdq_IMMb	vpalignr xmm1, xmm2, xmm3, 1	1	1
XED_IFORM_VPALIGNR_XMMu8_MASKmskw_XMMu8_MEMu8_IMM8_AVX512	vpalignr xmm1{k1}, xmm2, [rdi], 1	7	1
XED_IFORM_VPALIGNR_XMMu8_MASKmskw_XMMu8_XMMu8_IMM8_AVX512	vpalignr xmm1{k1}, xmm2, xmm3, 1	1	1
XED_IFORM_VPALIGNR_YMMqq_YMMqq_MEMqq_IMMb	vpalignr ymm1, ymm2, [rdi], 1	1	1
XED_IFORM_VPALIGNR_YMMqq_YMMqq_YMMqq_IMMb	vpalignr ymm1, ymm2, ymm3, 1	1	1
XED_IFORM_VPALIGNR_YMMu8_MASKmskw_YMMu8_MEMu8_IMM8_AVX512	vpalignr ymm1{k1}, ymm2, [rdi], 1	1	1
XED_IFORM_VPALIGNR_YMMu8_MASKmskw_YMMu8_YMMu8_IMM8_AVX512	vpalignr ymm1{k1}, ymm2, ymm3, 1	1	1
XED_IFORM_VPALIGNR_ZMMu8_MASKmskw_ZMMu8_MEMu8_IMM8_AVX512	vpalignr zmm1{k1}, zmm2, [rdi], 1	8	1
XED_IFORM_VPALIGNR_ZMMu8_MASKmskw_ZMMu8_ZMMu8_IMM8_AVX512	vpalignr zmm1{k1}, zmm2, zmm3, 1	1	1
XED_IFORM_PAND_XMMdq_MEMdq	vpand xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PAND_XMMdq_XMMdq	vpand xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPAND_XMMdq_XMMdq_MEMdq	vpand xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPAND_XMMdq_XMMdq_XMMdq	vpand xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPAND_YMMqq_YMMqq_MEMqq	vpand ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPAND_YMMqq_YMMqq_YMMqq	vpand ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPANDD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpandd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPANDD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpandd xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPANDD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpandd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPANDD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpandd ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPANDD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpandd zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPANDD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpandd zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PANDN_XMMdq_MEMdq	vpandn xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PANDN_XMMdq_XMMdq	vpandn xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPANDN_XMMdq_XMMdq_MEMdq	vpandn xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPANDN_XMMdq_XMMdq_XMMdq	vpandn xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPANDN_YMMqq_YMMqq_MEMqq	vpandn ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPANDN_YMMqq_YMMqq_YMMqq	vpandn ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPANDND_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpandnd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPANDND_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpandnd xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPANDND_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpandnd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPANDND_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpandnd ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPANDND_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpandnd zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPANDND_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpandnd zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPANDNQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpandnq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPANDNQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpandnq xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPANDNQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpandnq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPANDNQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpandnq ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPANDNQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpandnq zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPANDNQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpandnq zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPANDQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpandq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPANDQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpandq xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPANDQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpandq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPANDQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpandq ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPANDQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpandq zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPANDQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpandq zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PAVGB_XMMdq_MEMdq	vpavgb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PAVGB_XMMdq_XMMdq	vpavgb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPAVGB_XMMdq_XMMdq_MEMdq	vpavgb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPAVGB_XMMdq_XMMdq_XMMdq	vpavgb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPAVGB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpavgb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPAVGB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpavgb xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPAVGB_YMMqq_YMMqq_MEMqq	vpavgb ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPAVGB_YMMqq_YMMqq_YMMqq	vpavgb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPAVGB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpavgb ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPAVGB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpavgb ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPAVGB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpavgb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPAVGB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpavgb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PAVGW_XMMdq_MEMdq	vpavgw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PAVGW_XMMdq_XMMdq	vpavgw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPAVGW_XMMdq_XMMdq_MEMdq	vpavgw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPAVGW_XMMdq_XMMdq_XMMdq	vpavgw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPAVGW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpavgw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPAVGW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpavgw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPAVGW_YMMqq_YMMqq_MEMqq	vpavgw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPAVGW_YMMqq_YMMqq_YMMqq	vpavgw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPAVGW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpavgw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPAVGW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpavgw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPAVGW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpavgw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPAVGW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpavgw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPBLENDD_XMMdq_XMMdq_MEMdq_IMMb	vpblendd xmm1, xmm2, [rdi], 1	7	0.5

XED_IFORM_VPBLENDD_XMMdq_XMMdq_XMMdq_IMMb	vpblendd xmm1, xmm2, xmm3, 1	1	0.33
XED_IFORM_VPBLENDD_YMMqq_YMMqq_MEMqq_IMMb	vpblendd ymm1, ymm2, [rdi], 1	1	0.5
XED_IFORM_VPBLENDD_YMMqq_YMMqq_YMMqq_IMMb	vpblendd ymm1, ymm2, ymm3, 1	1	0.33
XED_IFORM_VPBLENDMB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpblendmb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPBLENDMB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpblendmb xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPBLENDMB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpblendmb ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPBLENDMB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpblendmb ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPBLENDMB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpblendmb zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPBLENDMB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpblendmb zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPBLENDMD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpblendmd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPBLENDMD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpblendmd xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPBLENDMD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpblendmd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPBLENDMD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpblendmd ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPBLENDMD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpblendmd zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPBLENDMD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpblendmd zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPBLENDMQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpblendmq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPBLENDMQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpblendmq xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPBLENDMQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpblendmq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPBLENDMQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpblendmq ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPBLENDMQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpblendmq zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPBLENDMQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpblendmq zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPBLENDMW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpblendmw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPBLENDMW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpblendmw xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPBLENDMW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpblendmw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPBLENDMW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpblendmw ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPBLENDMW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpblendmw zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPBLENDMW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpblendmw zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PBLENDVB_XMMdq_MEMdq	vpblendvb xmm1, xmm1, [rdi], xmm0	8	0.66
XED_IFORM_PBLENDVB_XMMdq_XMMdq	vpblendvb xmm1, xmm1, xmm2, xmm0	2	0.66
XED_IFORM_VPBLENDVB_XMMdq_XMMdq_MEMdq_XMMdq	vpblendvb xmm1, xmm2, [rdi], xmm3	8	0.66
XED_IFORM_VPBLENDVB_XMMdq_XMMdq_XMMdq_XMMdq	vpblendvb xmm1, xmm2, xmm3, xmm4	2	0.66
XED_IFORM_VPBLENDVB_YMMqq_YMMqq_MEMqq_YMMqq	vpblendvb ymm1, ymm2, [rdi], ymm3	8	0.66
XED_IFORM_VPBLENDVB_YMMqq_YMMqq_YMMqq_YMMqq	vpblendvb ymm1, ymm2, ymm3, ymm4	2	0.66
XED_IFORM_PBLENDW_XMMdq_MEMdq_IMMb	vpblendw xmm1, xmm1, [rdi], 1	7	1
XED_IFORM_PBLENDW_XMMdq_XMMdq_IMMb	vpblendw xmm1, xmm1, xmm2, 1	1	1
XED_IFORM_VPBLENDW_XMMdq_XMMdq_MEMdq_IMMb	vpblendw xmm1, xmm2, [rdi], 1	7	1
XED_IFORM_VPBLENDW_XMMdq_XMMdq_XMMdq_IMMb	vpblendw xmm1, xmm2, xmm3, 1	1	1
XED_IFORM_VPBLENDW_YMMqq_YMMqq_MEMqq_IMMb	vpblendw ymm1, ymm2, [rdi], 1	1	1
XED_IFORM_VPBLENDW_YMMqq_YMMqq_YMMqq_IMMb	vpblendw ymm1, ymm2, ymm3, 1	1	1
XED_IFORM_VPBROADCASTB_XMMdq_MEMb	vpbroadcastb xmm1, [rdi]	7	1
XED_IFORM_VPBROADCASTB_XMMdq_XMMb	vpbroadcastb xmm1, xmm2	3	1
XED_IFORM_VPBROADCASTB_XMMu8_MASKmskw_MEMu8_AVX512	vpbroadcastb xmm1{k1}, [rdi]	7	1
XED_IFORM_VPBROADCASTB_XMMu8_MASKmskw_GPR32u8_AVX512	vpbroadcastb xmm1{k1}, eax	3	1
XED_IFORM_VPBROADCASTB_XMMu8_MASKmskw_XMMu8_AVX512	vpbroadcastb xmm1{k1}, xmm2	3	1
XED_IFORM_VPBROADCASTB_YMMqq_MEMb	vpbroadcastb ymm1, [rdi]	1	1
XED_IFORM_VPBROADCASTB_YMMqq_XMMb	vpbroadcastb ymm1, xmm2	3	1
XED_IFORM_VPBROADCASTB_YMMu8_MASKmskw_MEMu8_AVX512	vpbroadcastb ymm1{k1}, [rdi]	1	1
XED_IFORM_VPBROADCASTB_YMMu8_MASKmskw_GPR32u8_AVX512	vpbroadcastb ymm1{k1}, eax	3	1
XED_IFORM_VPBROADCASTB_YMMu8_MASKmskw_XMMu8_AVX512	vpbroadcastb ymm1{k1}, xmm2	3	1
XED_IFORM_VPBROADCASTB_ZMMu8_MASKmskw_MEMu8_AVX512	vpbroadcastb zmm1{k1}, [rdi]	8	1
XED_IFORM_VPBROADCASTB_ZMMu8_MASKmskw_GPR32u8_AVX512	vpbroadcastb zmm1{k1}, eax	3	1
XED_IFORM_VPBROADCASTB_ZMMu8_MASKmskw_XMMu8_AVX512	vpbroadcastb zmm1{k1}, xmm2	3	1
XED_IFORM_VPBROADCASTD_XMMdq_MEMd	vpbroadcastd xmm1, [rdi]	6	0.5
XED_IFORM_VPBROADCASTD_XMMdq_XMMd	vpbroadcastd xmm1, xmm2	1	1
XED_IFORM_VPBROADCASTD_XMMu32_MASKmskw_MEMu32_AVX512	vpbroadcastd xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VPBROADCASTD_XMMu32_MASKmskw_GPR32u32_AVX512	vpbroadcastd xmm1{k1}, eax	3	1
XED_IFORM_VPBROADCASTD_XMMu32_MASKmskw_XMMu32_AVX512	vpbroadcastd xmm1{k1}, xmm2	3	1
XED_IFORM_VPBROADCASTD_YMMqq_MEMd	vpbroadcastd ymm1, [rdi]	0	0.5
XED_IFORM_VPBROADCASTD_YMMqq_XMMd	vpbroadcastd ymm1, xmm2	3	1
XED_IFORM_VPBROADCASTD_YMMu32_MASKmskw_MEMu32_AVX512	vpbroadcastd ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VPBROADCASTD_YMMu32_MASKmskw_GPR32u32_AVX512	vpbroadcastd ymm1{k1}, eax	3	1
XED_IFORM_VPBROADCASTD_YMMu32_MASKmskw_XMMu32_AVX512	vpbroadcastd ymm1{k1}, xmm2	3	1
XED_IFORM_VPBROADCASTD_ZMMu32_MASKmskw_MEMu32_AVX512	vpbroadcastd zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VPBROADCASTD_ZMMu32_MASKmskw_GPR32u32_AVX512	vpbroadcastd zmm1{k1}, eax	3	1
XED_IFORM_VPBROADCASTD_ZMMu32_MASKmskw_XMMu32_AVX512	vpbroadcastd zmm1{k1}, xmm2	3	1
XED_IFORM_VPBROADCASTQ_XMMdq_MEMq	vpbroadcastq xmm1, [rdi]	6	0.5
XED_IFORM_VPBROADCASTQ_XMMdq_XMMq	vpbroadcastq xmm1, xmm2	1	1
XED_IFORM_VPBROADCASTQ_XMMu64_MASKmskw_MEMu64_AVX512	vpbroadcastq xmm1{k1}, [rdi]	7	0.5
XED_IFORM_VPBROADCASTQ_XMMu64_MASKmskw_GPR64u64_AVX512	vpbroadcastq xmm1{k1}, rax	3	1
XED_IFORM_VPBROADCASTQ_XMMu64_MASKmskw_XMMu64_AVX512	vpbroadcastq xmm1{k1}, xmm2	3	1
XED_IFORM_VPBROADCASTQ_YMMqq_MEMq	vpbroadcastq ymm1, [rdi]	0	0.5
XED_IFORM_VPBROADCASTQ_YMMqq_XMMq	vpbroadcastq ymm1, xmm2	3	1
XED_IFORM_VPBROADCASTQ_YMMu64_MASKmskw_MEMu64_AVX512	vpbroadcastq ymm1{k1}, [rdi]	1	0.5
XED_IFORM_VPBROADCASTQ_YMMu64_MASKmskw_GPR64u64_AVX512	vpbroadcastq ymm1{k1}, rax	3	1
XED_IFORM_VPBROADCASTQ_YMMu64_MASKmskw_XMMu64_AVX512	vpbroadcastq ymm1{k1}, xmm2	3	1
XED_IFORM_VPBROADCASTQ_ZMMu64_MASKmskw_MEMu64_AVX512	vpbroadcastq zmm1{k1}, [rdi]	8	0.5
XED_IFORM_VPBROADCASTQ_ZMMu64_MASKmskw_GPR64u64_AVX512	vpbroadcastq zmm1{k1}, rax	3	1
XED_IFORM_VPBROADCASTQ_ZMMu64_MASKmskw_XMMu64_AVX512	vpbroadcastq zmm1{k1}, xmm2	3	1
XED_IFORM_VPBROADCASTW_XMMdq_MEMw	vpbroadcastw xmm1, [rdi]	7	1

XED_IFORM_VPBROADCASTW_XMMdq_XMMw	vpbroadcastw xmm1, xmm2	3	1
XED_IFORM_VPBROADCASTW_XMMu16_MASKmskw_MEMu16_AVX512	vpbroadcastw xmm1{k1}, [rdi]	7	1
XED_IFORM_VPBROADCASTW_XMMu16_MASKmskw_GPR32u16_AVX512	vpbroadcastw xmm1{k1}, eax	3	1
XED_IFORM_VPBROADCASTW_XMMu16_MASKmskw_XMMu16_AVX512	vpbroadcastw xmm1{k1}, xmm2	3	1
XED_IFORM_VPBROADCASTW_YMMqq_MEMw	vpbroadcastw ymm1, [rdi]	1	1
XED_IFORM_VPBROADCASTW_YMMqq_XMMw	vpbroadcastw ymm1, xmm2	3	1
XED_IFORM_VPBROADCASTW_YMMu16_MASKmskw_MEMu16_AVX512	vpbroadcastw ymm1{k1}, [rdi]	1	1
XED_IFORM_VPBROADCASTW_YMMu16_MASKmskw_GPR32u16_AVX512	vpbroadcastw ymm1{k1}, eax	3	1
XED_IFORM_VPBROADCASTW_YMMu16_MASKmskw_XMMu16_AVX512	vpbroadcastw ymm1{k1}, xmm2	3	1
XED_IFORM_VPBROADCASTW_ZMMu16_MASKmskw_MEMu16_AVX512	vpbroadcastw zmm1{k1}, [rdi]	8	1
XED_IFORM_VPBROADCASTW_ZMMu16_MASKmskw_GPR32u16_AVX512	vpbroadcastw zmm1{k1}, eax	3	1
XED_IFORM_VPBROADCASTW_ZMMu16_MASKmskw_XMMu16_AVX512	vpbroadcastw zmm1{k1}, xmm2	3	1
XED_IFORM_PCLMULQDQ_XMMdq_MEMdq_IMMb	vpclmulqdq xmm1, xmm1, [rdi], 1	12	1
XED_IFORM_PCLMULQDQ_XMMdq_XMMdq_IMMb	vpclmulqdq xmm1, xmm1, xmm2, 1	6	1
XED_IFORM_VPCLMULQDQ_XMMdq_XMMdq_MEMdq_IMMb	vpclmulqdq xmm1, xmm2, [rdi], 1	12	1
XED_IFORM_VPCLMULQDQ_XMMdq_XMMdq_XMMdq_IMMb	vpclmulqdq xmm1, xmm2, xmm3, 1	6	1
XED_IFORM_VPCMPB_MASKmskw_MASKmskw_XMMi8_MEMi8_IMM8_AVX512	vpcmpb k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VPCMPB_MASKmskw_MASKmskw_XMMi8_XMMi8_IMM8_AVX512	vpcmpb k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VPCMPB_MASKmskw_MASKmskw_YMMi8_MEMi8_IMM8_AVX512	vpcmpb k1{k1}, ymm1, [rdi], 1	3	1
XED_IFORM_VPCMPB_MASKmskw_MASKmskw_YMMi8_YMMi8_IMM8_AVX512	vpcmpb k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VPCMPB_MASKmskw_MASKmskw_ZMMi8_MEMi8_IMM8_AVX512	vpcmpb k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPB_MASKmskw_MASKmskw_ZMMi8_ZMMi8_IMM8_AVX512	vpcmpb k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCMPD_MASKmskw_MASKmskw_XMMi32_MEMi32_IMM8_AVX512	vpcmpd k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VPCMPD_MASKmskw_MASKmskw_XMMi32_XMMi32_IMM8_AVX512	vpcmpd k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VPCMPD_MASKmskw_MASKmskw_YMMi32_MEMi32_IMM8_AVX512	vpcmpd k1{k1}, ymm1, [rdi], 1	3	1
XED_IFORM_VPCMPD_MASKmskw_MASKmskw_YMMi32_YMMi32_IMM8_AVX512	vpcmpd k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VPCMPD_MASKmskw_MASKmskw_ZMMi32_MEMi32_IMM8_AVX512	vpcmpd k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPD_MASKmskw_MASKmskw_ZMMi32_ZMMi32_IMM8_AVX512	vpcmpd k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCMPEQB_MASKmskw_MASKmskw_XMMu8_MEMu8_AVX512	vpcmpeqb k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPCMPEQB_MASKmskw_MASKmskw_XMMu8_XMMu8_AVX512	vpcmpeqb k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPCMPEQB_MASKmskw_MASKmskw_YMMu8_MEMu8_AVX512	vpcmpeqb k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPCMPEQB_MASKmskw_MASKmskw_YMMu8_YMMu8_AVX512	vpcmpeqb k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPCMPEQB_MASKmskw_MASKmskw_ZMMu8_MEMu8_AVX512	vpcmpeqb k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPCMPEQB_MASKmskw_MASKmskw_ZMMu8_ZMMu8_AVX512	vpcmpeqb k1{k1}, zmm1, zmm2	3	1
XED_IFORM_PCMPEQB_XMMdq_MEMdq	vpcmpeqb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PCMPEQB_XMMdq_XMMdq	vpcmpeqb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPCMPEQB_XMMdq_XMMdq_MEMdq	vpcmpeqb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPCMPEQB_XMMdq_XMMdq_XMMdq	vpcmpeqb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPCMPEQB_YMMqq_YMMqq_MEMqq	vpcmpeqb ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPCMPEQB_YMMqq_YMMqq_YMMqq	vpcmpeqb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPCMPEQD_MASKmskw_MASKmskw_XMMu32_MEMu32_AVX512	vpcmpeqd k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPCMPEQD_MASKmskw_MASKmskw_XMMu32_XMMu32_AVX512	vpcmpeqd k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPCMPEQD_MASKmskw_MASKmskw_YMMu32_MEMu32_AVX512	vpcmpeqd k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPCMPEQD_MASKmskw_MASKmskw_YMMu32_YMMu32_AVX512	vpcmpeqd k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPCMPEQD_MASKmskw_MASKmskw_ZMMu32_MEMu32_AVX512	vpcmpeqd k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPCMPEQD_MASKmskw_MASKmskw_ZMMu32_ZMMu32_AVX512	vpcmpeqd k1{k1}, zmm1, zmm2	3	1
XED_IFORM_PCMPEQD_XMMdq_MEMdq	vpcmpeqd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PCMPEQD_XMMdq_XMMdq	vpcmpeqd xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPCMPEQD_XMMdq_XMMdq_MEMdq	vpcmpeqd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPCMPEQD_XMMdq_XMMdq_XMMdq	vpcmpeqd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPCMPEQD_YMMqq_YMMqq_MEMqq	vpcmpeqd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPCMPEQD_YMMqq_YMMqq_YMMqq	vpcmpeqd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPCMPEQQ_MASKmskw_MASKmskw_XMMu64_MEMu64_AVX512	vpcmpeqq k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPCMPEQQ_MASKmskw_MASKmskw_XMMu64_XMMu64_AVX512	vpcmpeqq k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPCMPEQQ_MASKmskw_MASKmskw_YMMu64_MEMu64_AVX512	vpcmpeqq k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPCMPEQQ_MASKmskw_MASKmskw_YMMu64_YMMu64_AVX512	vpcmpeqq k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPCMPEQQ_MASKmskw_MASKmskw_ZMMu64_MEMu64_AVX512	vpcmpeqq k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPCMPEQQ_MASKmskw_MASKmskw_ZMMu64_ZMMu64_AVX512	vpcmpeqq k1{k1}, zmm1, zmm2	3	1
XED_IFORM_PCMPEQQ_XMMdq_MEMdq	vpcmpeqq xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PCMPEQQ_XMMdq_XMMdq	vpcmpeqq xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPCMPEQQ_XMMdq_XMMdq_MEMdq	vpcmpeqq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPCMPEQQ_XMMdq_XMMdq_XMMdq	vpcmpeqq xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPCMPEQQ_YMMqq_YMMqq_MEMqq	vpcmpeqq ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPCMPEQQ_YMMqq_YMMqq_YMMqq	vpcmpeqq ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPCMPEQW_MASKmskw_MASKmskw_XMMu16_MEMu16_AVX512	vpcmpeqw k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPCMPEQW_MASKmskw_MASKmskw_XMMu16_XMMu16_AVX512	vpcmpeqw k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPCMPEQW_MASKmskw_MASKmskw_YMMu16_MEMu16_AVX512	vpcmpeqw k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPCMPEQW_MASKmskw_MASKmskw_YMMu16_YMMu16_AVX512	vpcmpeqw k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPCMPEQW_MASKmskw_MASKmskw_ZMMu16_MEMu16_AVX512	vpcmpeqw k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPCMPEQW_MASKmskw_MASKmskw_ZMMu16_ZMMu16_AVX512	vpcmpeqw k1{k1}, zmm1, zmm2	3	1
XED_IFORM_PCMPEQW_XMMdq_MEMdq	vpcmpeqw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PCMPEQW_XMMdq_XMMdq	vpcmpeqw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPCMPEQW_XMMdq_XMMdq_MEMdq	vpcmpeqw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPCMPEQW_XMMdq_XMMdq_XMMdq	vpcmpeqw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPCMPEQW_YMMqq_YMMqq_MEMqq	vpcmpeqw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPCMPEQW_YMMqq_YMMqq_YMMqq	vpcmpeqw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_PCMPESTRI_XMMdq_MEMdq_IMMb	vpcmpestri xmm1, [rdi], 1	24	4
XED_IFORM_VPCMPESTRI_XMMdq_MEMdq_IMMb	vpcmpestri xmm1, [rdi], 1	24	4
XED_IFORM_VPCMPESTRI_XMMdq_XMMdq_IMMb	vpcmpestri xmm1, xmm2, 1	18	4

XED_IFORM_PCMPESTRI_XMMdq_XMMdq_IMMb	vpcmpestri xmm1, xmm2, 1	18	4
XED_IFORM_VPCMPESTRM_XMMdq_MEMdq_IMMb	vpcmpestrm xmm1, [rdi], 1	25	4
XED_IFORM_PCMPESTRM_XMMdq_MEMdq_IMMb	vpcmpestrm xmm1, [rdi], 1	25	4
XED_IFORM_VPCMPESTRM_XMMdq_XMMdq_IMMb	vpcmpestrm xmm1, xmm2, 1	19	4
XED_IFORM_PCMPESTRM_XMMdq_XMMdq_IMMb	vpcmpestrm xmm1, xmm2, 1	19	4
XED_IFORM_VPCMPGTB_MASKmskw_MASKmskw_XMMu8_MEMu8_AVX512	vpcmpgtb k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPCMPGTB_MASKmskw_MASKmskw_XMMu8_XMMu8_AVX512	vpcmpgtb k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPCMPGTB_MASKmskw_MASKmskw_YMMu8_MEMu8_AVX512	vpcmpgtb k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPCMPGTB_MASKmskw_MASKmskw_YMMu8_YMMu8_AVX512	vpcmpgtb k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPCMPGTB_MASKmskw_MASKmskw_ZMMu8_MEMu8_AVX512	vpcmpgtb k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPCMPGTB_MASKmskw_MASKmskw_ZMMu8_ZMMu8_AVX512	vpcmpgtb k1{k1}, zmm1, zmm2	3	1
XED_IFORM_PCMPGTB_XMMdq_MEMdq	vpcmpgtb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PCMPGTB_XMMdq_XMMdq	vpcmpgtb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPCMPGTB_XMMdq_XMMdq_MEMdq	vpcmpgtb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPCMPGTB_XMMdq_XMMdq_XMMdq	vpcmpgtb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPCMPGTB_YMMqq_YMMqq_MEMqq	vpcmpgtb ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPCMPGTB_YMMqq_YMMqq_YMMqq	vpcmpgtb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPCMPGTD_MASKmskw_MASKmskw_XMMi32_MEMi32_AVX512	vpcmpgtd k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPCMPGTD_MASKmskw_MASKmskw_XMMi32_XMMi32_AVX512	vpcmpgtd k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPCMPGTD_MASKmskw_MASKmskw_YMMi32_MEMi32_AVX512	vpcmpgtd k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPCMPGTD_MASKmskw_MASKmskw_YMMi32_YMMi32_AVX512	vpcmpgtd k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPCMPGTD_MASKmskw_MASKmskw_ZMMi32_MEMi32_AVX512	vpcmpgtd k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPCMPGTD_MASKmskw_MASKmskw_ZMMi32_ZMMi32_AVX512	vpcmpgtd k1{k1}, zmm1, zmm2	3	1
XED_IFORM_PCMPGTD_XMMdq_MEMdq	vpcmpgtd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PCMPGTD_XMMdq_XMMdq	vpcmpgtd xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPCMPGTD_XMMdq_XMMdq_MEMdq	vpcmpgtd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPCMPGTD_XMMdq_XMMdq_XMMdq	vpcmpgtd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPCMPGTD_YMMqq_YMMqq_MEMqq	vpcmpgtd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPCMPGTD_YMMqq_YMMqq_YMMqq	vpcmpgtd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPCMPGTQ_MASKmskw_MASKmskw_XMMi64_MEMi64_AVX512	vpcmpgtq k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPCMPGTQ_MASKmskw_MASKmskw_XMMi64_XMMi64_AVX512	vpcmpgtq k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPCMPGTQ_MASKmskw_MASKmskw_YMMi64_MEMi64_AVX512	vpcmpgtq k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPCMPGTQ_MASKmskw_MASKmskw_YMMi64_YMMi64_AVX512	vpcmpgtq k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPCMPGTQ_MASKmskw_MASKmskw_ZMMi64_MEMi64_AVX512	vpcmpgtq k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPCMPGTQ_MASKmskw_MASKmskw_ZMMi64_ZMMi64_AVX512	vpcmpgtq k1{k1}, zmm1, zmm2	3	1
XED_IFORM_PCMPGTQ_XMMdq_MEMdq	vpcmpgtq xmm1, xmm1, [rdi]	9	1
XED_IFORM_PCMPGTQ_XMMdq_XMMdq	vpcmpgtq xmm1, xmm1, xmm2	3	1
XED_IFORM_VPCMPGTQ_XMMdq_XMMdq_MEMdq	vpcmpgtq xmm1, xmm2, [rdi]	9	1
XED_IFORM_VPCMPGTQ_XMMdq_XMMdq_XMMdq	vpcmpgtq xmm1, xmm2, xmm3	3	1
XED_IFORM_VPCMPGTQ_YMMqq_YMMqq_MEMqq	vpcmpgtq ymm1, ymm2, [rdi]	3	1
XED_IFORM_VPCMPGTQ_YMMqq_YMMqq_YMMqq	vpcmpgtq ymm1, ymm2, ymm3	3	1
XED_IFORM_VPCMPGTW_MASKmskw_MASKmskw_XMMu16_MEMu16_AVX512	vpcmpgtw k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPCMPGTW_MASKmskw_MASKmskw_XMMu16_XMMu16_AVX512	vpcmpgtw k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPCMPGTW_MASKmskw_MASKmskw_YMMu16_MEMu16_AVX512	vpcmpgtw k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPCMPGTW_MASKmskw_MASKmskw_YMMu16_YMMu16_AVX512	vpcmpgtw k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPCMPGTW_MASKmskw_MASKmskw_ZMMu16_MEMu16_AVX512	vpcmpgtw k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPCMPGTW_MASKmskw_MASKmskw_ZMMu16_ZMMu16_AVX512	vpcmpgtw k1{k1}, zmm1, zmm2	3	1
XED_IFORM_PCMPGTW_XMMdq_MEMdq	vpcmpgtw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PCMPGTW_XMMdq_XMMdq	vpcmpgtw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPCMPGTW_XMMdq_XMMdq_MEMdq	vpcmpgtw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPCMPGTW_XMMdq_XMMdq_XMMdq	vpcmpgtw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPCMPGTW_YMMqq_YMMqq_MEMqq	vpcmpgtw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPCMPGTW_YMMqq_YMMqq_YMMqq	vpcmpgtw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPCMPISTRI_XMMdq_MEMdq_IMMb	vpcmpistri xmm1, [rdi], 1	16	3
XED_IFORM_PCMPISTRI_XMMdq_MEMdq_IMMb	vpcmpistri xmm1, [rdi], 1	16	3
XED_IFORM_VPCMPISTRM_XMMdq_MEMdq_IMMb	vpcmpistrm xmm1, [rdi], 1	16	3
XED_IFORM_PCMPISTRM_XMMdq_MEMdq_IMMb	vpcmpistrm xmm1, [rdi], 1	16	3
XED_IFORM_VPCMPQ_MASKmskw_MASKmskw_XMMi64_MEMi64_IMM8_AVX512	vpcmpq k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VPCMPQ_MASKmskw_MASKmskw_XMMi64_XMMi64_IMM8_AVX512	vpcmpq k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VPCMPQ_MASKmskw_MASKmskw_YMMi64_MEMi64_IMM8_AVX512	vpcmpq k1{k1}, ymm1, [rdi], 1	3	1
XED_IFORM_VPCMPQ_MASKmskw_MASKmskw_YMMi64_YMMi64_IMM8_AVX512	vpcmpq k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VPCMPQ_MASKmskw_MASKmskw_ZMMi64_MEMi64_IMM8_AVX512	vpcmpq k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPQ_MASKmskw_MASKmskw_ZMMi64_ZMMi64_IMM8_AVX512	vpcmpq k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCMPUB_MASKmskw_MASKmskw_XMMu8_MEMu8_IMM8_AVX512	vpcmpub k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VPCMPUB_MASKmskw_MASKmskw_XMMu8_XMMu8_IMM8_AVX512	vpcmpub k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VPCMPUB_MASKmskw_MASKmskw_YMMu8_MEMu8_IMM8_AVX512	vpcmpub k1{k1}, ymm1, [rdi], 1	3	1
XED_IFORM_VPCMPUB_MASKmskw_MASKmskw_YMMu8_YMMu8_IMM8_AVX512	vpcmpub k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VPCMPUB_MASKmskw_MASKmskw_ZMMu8_MEMu8_IMM8_AVX512	vpcmpub k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPUB_MASKmskw_MASKmskw_ZMMu8_ZMMu8_IMM8_AVX512	vpcmpub k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCMPUD_MASKmskw_MASKmskw_XMMu32_MEMu32_IMM8_AVX512	vpcmpud k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VPCMPUD_MASKmskw_MASKmskw_XMMu32_XMMu32_IMM8_AVX512	vpcmpud k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VPCMPUD_MASKmskw_MASKmskw_YMMu32_MEMu32_IMM8_AVX512	vpcmpud k1{k1}, ymm1, [rdi], 1	3	1
XED_IFORM_VPCMPUD_MASKmskw_MASKmskw_YMMu32_YMMu32_IMM8_AVX512	vpcmpud k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VPCMPUD_MASKmskw_MASKmskw_ZMMu32_MEMu32_IMM8_AVX512	vpcmpud k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPUD_MASKmskw_MASKmskw_ZMMu32_ZMMu32_IMM8_AVX512	vpcmpud k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCMPUQ_MASKmskw_MASKmskw_XMMu64_MEMu64_IMM8_AVX512	vpcmpuq k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VPCMPUQ_MASKmskw_MASKmskw_XMMu64_XMMu64_IMM8_AVX512	vpcmpuq k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VPCMPUQ_MASKmskw_MASKmskw_YMMu64_MEMu64_IMM8_AVX512	vpcmpuq k1{k1}, ymm1, [rdi], 1	3	1
XED_IFORM_VPCMPUQ_MASKmskw_MASKmskw_YMMu64_YMMu64_IMM8_AVX512	vpcmpuq k1{k1}, ymm1, ymm2, 1	3	1

XED_IFORM_VPCMPUQ_MASKmskw_MASKmskw_ZMMu64_MEMu64_IMM8_AVX512	vpcmpuq k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPUQ_MASKmskw_MASKmskw_ZMMu64_ZMMu64_IMM8_AVX512	vpcmpuq k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCMPUW_MASKmskw_MASKmskw_XMMu16_MEMu16_IMM8_AVX512	vpcmpuw k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VPCMPUW_MASKmskw_MASKmskw_XMMu16_XMMu16_IMM8_AVX512	vpcmpuw k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VPCMPUW_MASKmskw_MASKmskw_YMMu16_MEMu16_IMM8_AVX512	vpcmpuw k1{k1}, ymm1, [rdi], 1	3	1
XED_IFORM_VPCMPUW_MASKmskw_MASKmskw_YMMu16_YMMu16_IMM8_AVX512	vpcmpuw k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VPCMPUW_MASKmskw_MASKmskw_ZMMu16_MEMu16_IMM8_AVX512	vpcmpuw k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPUW_MASKmskw_MASKmskw_ZMMu16_ZMMu16_IMM8_AVX512	vpcmpuw k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCMPW_MASKmskw_MASKmskw_XMMi16_MEMi16_IMM8_AVX512	vpcmpw k1{k1}, xmm1, [rdi], 1	9	1
XED_IFORM_VPCMPW_MASKmskw_MASKmskw_XMMi16_XMMi16_IMM8_AVX512	vpcmpw k1{k1}, xmm1, xmm2, 1	3	1
XED_IFORM_VPCMPW_MASKmskw_MASKmskw_YMMi16_MEMi16_IMM8_AVX512	vpcmpw k1{k1}, ymm1, [rdi], 1	3	1
XED_IFORM_VPCMPW_MASKmskw_MASKmskw_YMMi16_YMMi16_IMM8_AVX512	vpcmpw k1{k1}, ymm1, ymm2, 1	3	1
XED_IFORM_VPCMPW_MASKmskw_MASKmskw_ZMMi16_MEMi16_IMM8_AVX512	vpcmpw k1{k1}, zmm1, [rdi], 1	10	1
XED_IFORM_VPCMPW_MASKmskw_MASKmskw_ZMMi16_ZMMi16_IMM8_AVX512	vpcmpw k1{k1}, zmm1, zmm2, 1	3	1
XED_IFORM_VPCOMPRESSD_MEMu32_MASKmskw_XMMu32_AVX512	vpcompressd [rdi]{k1}, xmm1	11	2
XED_IFORM_VPCOMPRESSD_MEMu32_MASKmskw_YMMu32_AVX512	vpcompressd [rdi]{k1}, ymm1	11	2
XED_IFORM_VPCOMPRESSD_MEMu32_MASKmskw_ZMMu32_AVX512	vpcompressd [rdi]{k1}, zmm1	11	2
XED_IFORM_VPCOMPRESSD_XMMu32_MASKmskw_XMMu32_AVX512	vpcompressd xmm1{k1}, xmm2	6	2
XED_IFORM_VPCOMPRESSD_YMMu32_MASKmskw_YMMu32_AVX512	vpcompressd ymm1{k1}, ymm2	6	2
XED_IFORM_VPCOMPRESSD_ZMMu32_MASKmskw_ZMMu32_AVX512	vpcompressd zmm1{k1}, zmm2	6	2
XED_IFORM_VPCOMPRESSQ_MEMu64_MASKmskw_XMMu64_AVX512	vpcompressq [rdi]{k1}, xmm1	11	2
XED_IFORM_VPCOMPRESSQ_MEMu64_MASKmskw_YMMu64_AVX512	vpcompressq [rdi]{k1}, ymm1	11	2
XED_IFORM_VPCOMPRESSQ_MEMu64_MASKmskw_ZMMu64_AVX512	vpcompressq [rdi]{k1}, zmm1	11	2
XED_IFORM_VPCOMPRESSQ_XMMu64_MASKmskw_XMMu64_AVX512	vpcompressq xmm1{k1}, xmm2	6	2
XED_IFORM_VPCOMPRESSQ_YMMu64_MASKmskw_YMMu64_AVX512	vpcompressq ymm1{k1}, ymm2	6	2
XED_IFORM_VPCOMPRESSQ_ZMMu64_MASKmskw_ZMMu64_AVX512	vpcompressq zmm1{k1}, zmm2	6	2
XED_IFORM_VPCONFLICTD_XMMu32_MASKmskw_MEMu32_AVX512	vpconflictd xmm1{k1}, [rdi]	15	2.31
XED_IFORM_VPCONFLICTD_XMMu32_MASKmskw_XMMu32_AVX512	vpconflictd xmm1{k1}, xmm2	22	5
XED_IFORM_VPCONFLICTD_YMMu32_MASKmskw_MEMu32_AVX512	vpconflictd ymm1{k1}, [rdi]	37	9
XED_IFORM_VPCONFLICTD_YMMu32_MASKmskw_YMMu32_AVX512	vpconflictd ymm1{k1}, ymm2	37	9
XED_IFORM_VPCONFLICTD_ZMMu32_MASKmskw_MEMu32_AVX512CD	vpconflictd zmm1{k1}, [rdi]	74	17.5
XED_IFORM_VPCONFLICTD_ZMMu32_MASKmskw_ZMMu32_AVX512CD	vpconflictd zmm1{k1}, zmm2	67	17.5
XED_IFORM_VPCONFLICTQ_XMMu64_MASKmskw_MEMu64_AVX512	vpconflictq xmm1{k1}, [rdi]	11	2
XED_IFORM_VPCONFLICTQ_XMMu64_MASKmskw_XMMu64_AVX512	vpconflictq xmm1{k1}, xmm2	5	2
XED_IFORM_VPCONFLICTQ_YMMu64_MASKmskw_MEMu64_AVX512	vpconflictq ymm1{k1}, [rdi]	22	5
XED_IFORM_VPCONFLICTQ_YMMu64_MASKmskw_YMMu64_AVX512	vpconflictq ymm1{k1}, ymm2	22	5
XED_IFORM_VPCONFLICTQ_ZMMu64_MASKmskw_MEMu64_AVX512CD	vpconflictq zmm1{k1}, [rdi]	44	10.5
XED_IFORM_VPCONFLICTQ_ZMMu64_MASKmskw_ZMMu64_AVX512CD	vpconflictq zmm1{k1}, zmm2	37	10.5
XED_IFORM_VPERM2F128_YMMqq_YMMqq_MEMqq_IMMb	vperm2f128 ymm1, ymm2, [rdi], 1	3	1
XED_IFORM_VPERM2F128_YMMqq_YMMqq_YMMqq_IMMb	vperm2f128 ymm1, ymm2, ymm3, 1	3	1
XED_IFORM_VPERM2I128_YMMqq_YMMqq_MEMqq_IMMb	vperm2i128 ymm1, ymm2, [rdi], 1	3	1
XED_IFORM_VPERM2I128_YMMqq_YMMqq_YMMqq_IMMb	vperm2i128 ymm1, ymm2, ymm3, 1	3	1
XED_IFORM_VPERMD_YMMqq_YMMqq_MEMqq	vpermd ymm1, ymm2, [rdi]	3	1
XED_IFORM_VPERMD_YMMqq_YMMqq_YMMqq	vpermd ymm1, ymm2, ymm3	3	1
XED_IFORM_VPERMD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpermd ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPERMD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpermd ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpermd zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpermd zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMI2D_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpermi2d xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMI2D_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpermi2d xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMI2D_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpermi2d ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPERMI2D_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpermi2d ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMI2D_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpermi2d zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMI2D_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpermi2d zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMI2PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vpermi2pd xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMI2PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vpermi2pd xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMI2PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vpermi2pd ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPERMI2PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vpermi2pd ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMI2PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vpermi2pd zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMI2PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vpermi2pd zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMI2PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vpermi2ps xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMI2PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vpermi2ps xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMI2PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vpermi2ps ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPERMI2PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vpermi2ps ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMI2PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vpermi2ps zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMI2PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vpermi2ps zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMI2Q_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpermi2q xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMI2Q_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpermi2q xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMI2Q_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpermi2q ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPERMI2Q_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpermi2q ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMI2Q_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpermi2q zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMI2Q_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpermi2q zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMI2W_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpermi2w xmm1{k1}, xmm2, [rdi]	13	2
XED_IFORM_VPERMI2W_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpermi2w xmm1{k1}, xmm2, xmm3	7	2
XED_IFORM_VPERMI2W_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpermi2w ymm1{k1}, ymm2, [rdi]	7	2
XED_IFORM_VPERMI2W_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpermi2w ymm1{k1}, ymm2, ymm3	7	2
XED_IFORM_VPERMI2W_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpermi2w zmm1{k1}, zmm2, [rdi]	14	2
XED_IFORM_VPERMI2W_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpermi2w zmm1{k1}, zmm2, zmm3	7	2
XED_IFORM_VPERMILPD_XMMdq_MEMdq_IMMb	vpermilpd xmm1, [rdi], 1	7	1

XED_IFORM_VPERMILPD_XMMdq_XMMdq_MEMdq	vpermilpd xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPERMILPD_XMMdq_XMMdq_IMMb	vpermilpd xmm1, xmm2, 1	1	1
XED_IFORM_VPERMILPD_XMMdq_XMMdq_XMMdq	vpermilpd xmm1, xmm2, xmm3	1	1
XED_IFORM_VPERMILPD_XMMf64_MASKmskw_MEMf64_IMM8_AVX512	vpermilpd xmm1{k1}, [rdi], 1	7	1
XED_IFORM_VPERMILPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vpermilpd xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPERMILPD_XMMf64_MASKmskw_XMMf64_IMM8_AVX512	vpermilpd xmm1{k1}, xmm2, 1	1	1
XED_IFORM_VPERMILPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vpermilpd xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPERMILPD_YMMqq_MEMqq_IMMb	vpermilpd ymm1, [rdi], 1	1	1
XED_IFORM_VPERMILPD_YMMqq_YMMqq_MEMqq	vpermilpd ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPERMILPD_YMMqq_YMMqq_IMMb	vpermilpd ymm1, ymm2, 1	1	1
XED_IFORM_VPERMILPD_YMMqq_YMMqq_YMMqq	vpermilpd ymm1, ymm2, ymm3	1	1
XED_IFORM_VPERMILPD_YMMf64_MASKmskw_MEMf64_IMM8_AVX512	vpermilpd ymm1{k1}, [rdi], 1	1	1
XED_IFORM_VPERMILPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vpermilpd ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPERMILPD_YMMf64_MASKmskw_YMMf64_IMM8_AVX512	vpermilpd ymm1{k1}, ymm2, 1	1	1
XED_IFORM_VPERMILPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vpermilpd ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPERMILPD_ZMMf64_MASKmskw_MEMf64_IMM8_AVX512	vpermilpd zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPERMILPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vpermilpd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPERMILPD_ZMMf64_MASKmskw_ZMMf64_IMM8_AVX512	vpermilpd zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPERMILPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vpermilpd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPERMILPS_XMMdq_MEMdq_IMMb	vpermilps xmm1, [rdi], 1	7	1
XED_IFORM_VPERMILPS_XMMdq_XMMdq_MEMdq	vpermilps xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPERMILPS_XMMdq_XMMdq_IMMb	vpermilps xmm1, xmm2, 1	1	1
XED_IFORM_VPERMILPS_XMMdq_XMMdq_XMMdq	vpermilps xmm1, xmm2, xmm3	1	1
XED_IFORM_VPERMILPS_XMMf32_MASKmskw_MEMf32_IMM8_AVX512	vpermilps xmm1{k1}, [rdi], 1	7	1
XED_IFORM_VPERMILPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vpermilps xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPERMILPS_XMMf32_MASKmskw_XMMf32_IMM8_AVX512	vpermilps xmm1{k1}, xmm2, 1	1	1
XED_IFORM_VPERMILPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vpermilps xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPERMILPS_YMMqq_MEMqq_IMMb	vpermilps ymm1, [rdi], 1	1	1
XED_IFORM_VPERMILPS_YMMqq_YMMqq_MEMqq	vpermilps ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPERMILPS_YMMqq_YMMqq_IMMb	vpermilps ymm1, ymm2, 1	1	1
XED_IFORM_VPERMILPS_YMMqq_YMMqq_YMMqq	vpermilps ymm1, ymm2, ymm3	1	1
XED_IFORM_VPERMILPS_YMMf32_MASKmskw_MEMf32_IMM8_AVX512	vpermilps ymm1{k1}, [rdi], 1	1	1
XED_IFORM_VPERMILPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vpermilps ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPERMILPS_YMMf32_MASKmskw_YMMf32_IMM8_AVX512	vpermilps ymm1{k1}, ymm2, 1	1	1
XED_IFORM_VPERMILPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vpermilps ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPERMILPS_ZMMf32_MASKmskw_MEMf32_IMM8_AVX512	vpermilps zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPERMILPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vpermilps zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPERMILPS_ZMMf32_MASKmskw_ZMMf32_IMM8_AVX512	vpermilps zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPERMILPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vpermilps zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPERMPD_YMMqq_MEMqq_IMMb	vpermpd ymm1, [rdi], 1	3	1
XED_IFORM_VPERMPD_YMMqq_YMMqq_IMMb	vpermpd ymm1, ymm2, 1	3	1
XED_IFORM_VPERMPD_YMMf64_MASKmskw_MEMf64_IMM8_AVX512	vpermpd ymm1{k1}, [rdi], 1	3	1
XED_IFORM_VPERMPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vpermpd ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPERMPD_YMMf64_MASKmskw_YMMf64_IMM8_AVX512	vpermpd ymm1{k1}, ymm2, 1	3	1
XED_IFORM_VPERMPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vpermpd ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMPD_ZMMf64_MASKmskw_MEMf64_IMM8_AVX512	vpermpd zmm1{k1}, [rdi], 1	10	1
XED_IFORM_VPERMPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vpermpd zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMPD_ZMMf64_MASKmskw_ZMMf64_IMM8_AVX512	vpermpd zmm1{k1}, zmm2, 1	3	1
XED_IFORM_VPERMPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vpermpd zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMPS_YMMqq_YMMqq_MEMqq	vpermps ymm1, ymm2, [rdi]	3	1
XED_IFORM_VPERMPS_YMMqq_YMMqq_YMMqq	vpermps ymm1, ymm2, ymm3	3	1
XED_IFORM_VPERMPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vpermps ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPERMPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vpermps ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vpermps zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vpermps zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMQ_YMMqq_MEMqq_IMMb	vpermq ymm1, [rdi], 1	3	1
XED_IFORM_VPERMQ_YMMqq_YMMqq_IMMb	vpermq ymm1, ymm2, 1	3	1
XED_IFORM_VPERMQ_YMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpermq ymm1{k1}, [rdi], 1	3	1
XED_IFORM_VPERMQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpermq ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPERMQ_YMMu64_MASKmskw_YMMu64_IMM8_AVX512	vpermq ymm1{k1}, ymm2, 1	3	1
XED_IFORM_VPERMQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpermq ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMQ_ZMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpermq zmm1{k1}, [rdi], 1	10	1
XED_IFORM_VPERMQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpermq zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMQ_ZMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vpermq zmm1{k1}, zmm2, 1	3	1
XED_IFORM_VPERMQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpermq zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMT2D_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpermt2d xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMT2D_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpermt2d xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMT2D_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpermt2d ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPERMT2D_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpermt2d ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMT2D_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpermt2d zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMT2D_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpermt2d zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMT2PD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vpermt2pd xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMT2PD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vpermt2pd xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMT2PD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vpermt2pd ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPERMT2PD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vpermt2pd ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMT2PD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vpermt2pd zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMT2PD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vpermt2pd zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMT2PS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vpermt2ps xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMT2PS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vpermt2ps xmm1{k1}, xmm2, xmm3	3	1

XED_IFORM_VPERMT2PS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vpermt2ps ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPERMT2PS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vpermt2ps ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMT2PS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vpermt2ps zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMT2PS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vpermt2ps zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMT2Q_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpermt2q xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPERMT2Q_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpermt2q xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPERMT2Q_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpermt2q ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPERMT2Q_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpermt2q ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPERMT2Q_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpermt2q zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPERMT2Q_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpermt2q zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPERMT2W_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpermt2w xmm1{k1}, xmm2, [rdi]	13	2
XED_IFORM_VPERMT2W_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpermt2w xmm1{k1}, xmm2, xmm3	7	2
XED_IFORM_VPERMT2W_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpermt2w ymm1{k1}, ymm2, [rdi]	7	2
XED_IFORM_VPERMT2W_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpermt2w ymm1{k1}, ymm2, ymm3	7	2
XED_IFORM_VPERMT2W_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpermt2w zmm1{k1}, zmm2, [rdi]	14	2
XED_IFORM_VPERMT2W_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpermt2w zmm1{k1}, zmm2, zmm3	7	2
XED_IFORM_VPERMW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpermw xmm1{k1}, xmm2, [rdi]	12	2
XED_IFORM_VPERMW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpermw xmm1{k1}, xmm2, xmm3	6	2
XED_IFORM_VPERMW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpermw ymm1{k1}, ymm2, [rdi]	6	2
XED_IFORM_VPERMW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpermw ymm1{k1}, ymm2, ymm3	6	2
XED_IFORM_VPERMW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpermw zmm1{k1}, zmm2, [rdi]	13	2
XED_IFORM_VPERMW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpermw zmm1{k1}, zmm2, zmm3	6	2
XED_IFORM_VPEXPANDD_XMMu32_MASKmskw_MEMu32_AVX512	vpexpandd xmm1{k1}, [rdi]	10	2
XED_IFORM_VPEXPANDD_XMMu32_MASKmskw_XMMu32_AVX512	vpexpandd xmm1{k1}, xmm2	4	2
XED_IFORM_VPEXPANDD_YMMu32_MASKmskw_MEMu32_AVX512	vpexpandd ymm1{k1}, [rdi]	4	2
XED_IFORM_VPEXPANDD_YMMu32_MASKmskw_YMMu32_AVX512	vpexpandd ymm1{k1}, ymm2	4	2
XED_IFORM_VPEXPANDD_ZMMu32_MASKmskw_MEMu32_AVX512	vpexpandd zmm1{k1}, [rdi]	11	2
XED_IFORM_VPEXPANDD_ZMMu32_MASKmskw_ZMMu32_AVX512	vpexpandd zmm1{k1}, zmm2	4	2
XED_IFORM_VPEXPANDQ_XMMu64_MASKmskw_MEMu64_AVX512	vpexpandq xmm1{k1}, [rdi]	10	2
XED_IFORM_VPEXPANDQ_XMMu64_MASKmskw_XMMu64_AVX512	vpexpandq xmm1{k1}, xmm2	4	2
XED_IFORM_VPEXPANDQ_YMMu64_MASKmskw_MEMu64_AVX512	vpexpandq ymm1{k1}, [rdi]	4	2
XED_IFORM_VPEXPANDQ_YMMu64_MASKmskw_YMMu64_AVX512	vpexpandq ymm1{k1}, ymm2	4	2
XED_IFORM_VPEXPANDQ_ZMMu64_MASKmskw_MEMu64_AVX512	vpexpandq zmm1{k1}, [rdi]	11	2
XED_IFORM_VPEXPANDQ_ZMMu64_MASKmskw_ZMMu64_AVX512	vpexpandq zmm1{k1}, zmm2	4	2
XED_IFORM_VPEXTRB_MEMb_XMMdq_IMMb	vpextrb [rdi], xmm1, 1	6	1
XED_IFORM_PEXTRB_MEMb_XMMdq_IMMb	vpextrb [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRB_MEMu8_XMMu8_IMM8_AVX512	vpextrb [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRB_GPR32u8_XMMu8_IMM8_AVX512	vpextrb eax, xmm1, 1	3	1
XED_IFORM_PEXTRB_GPR32d_XMMdq_IMMb	vpextrb eax, xmm1, 1	3	1
XED_IFORM_VPEXTRB_GPR32d_XMMdq_IMMb	vpextrb eax, xmm1, 1	3	1
XED_IFORM_VPEXTRD_MEMu32_XMMu32_IMM8_AVX512	vpextrd [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRD_MEMd_XMMdq_IMMb	vpextrd [rdi], xmm1, 1	6	1
XED_IFORM_PEXTRD_MEMd_XMMdq_IMMb	vpextrd [rdi], xmm1, 1	6	1
XED_IFORM_PEXTRD_GPR32d_XMMdq_IMMb	vpextrd eax, xmm1, 1	3	1
XED_IFORM_VPEXTRD_GPR32d_XMMdq_IMMb	vpextrd eax, xmm1, 1	3	1
XED_IFORM_VPEXTRD_GPR32u32_XMMu32_IMM8_AVX512	vpextrd eax, xmm1, 1	3	1
XED_IFORM_VPEXTRQ_MEMu64_XMMu64_IMM8_AVX512	vpextrq [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRQ_MEMq_XMMdq_IMMb	vpextrq [rdi], xmm1, 1	6	1
XED_IFORM_PEXTRQ_MEMq_XMMdq_IMMb	vpextrq [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRQ_GPR64u64_XMMu64_IMM8_AVX512	vpextrq rax, xmm1, 1	3	1
XED_IFORM_VPEXTRQ_GPR64q_XMMdq_IMMb	vpextrq rax, xmm1, 1	3	1
XED_IFORM_PEXTRQ_GPR64q_XMMdq_IMMb	vpextrq rax, xmm1, 1	3	1
XED_IFORM_VPEXTRW_MEMu16_XMMu16_IMM8_AVX512	vpextrw [rdi], xmm1, 1	6	1
XED_IFORM_PEXTRW_SSE4_MEMw_XMMdq_IMMb	vpextrw [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRW_MEMw_XMMdq_IMMb	vpextrw [rdi], xmm1, 1	6	1
XED_IFORM_VPEXTRW_GPR32d_XMMdq_IMMb_C5	vpextrw eax, xmm1, 1	3	1
XED_IFORM_PEXTRW_GPR32_XMMdq_IMMb	vpextrw eax, xmm1, 1	3	1
XED_IFORM_VPEXTRW_GPR32u16_XMMu16_IMM8_AVX512	vpextrw eax, xmm1, 1	3	1
XED_IFORM_VPEXTRW_GPR32d_XMMdq_IMMb_15	vpextrw eax, xmm1, 1	3	1
XED_IFORM_PEXTRW_SSE4_GPR32_XMMdq_IMMb	vpextrw eax, xmm1, 1	3	1
XED_IFORM_VPGATHERDD_YMMu32_MEMqq_YMMi32_VL256	vpgatherdd ymm1, [rdi+ymm2*1], ymm3	27	5
XED_IFORM_VPGATHERDD_YMMu32_MASKmskw_MEMu32_AVX512_VL256	vpgatherdd ymm1{k1}, [rdi+ymm2*1]	27	5
XED_IFORM_VPGATHERDD_ZMMu32_MASKmskw_MEMu32_AVX512_VL512	vpgatherdd zmm1{k1}, [rdi+zmm2*1]	30	9.75
XED_IFORM_VPGATHERDQ_XMMu64_MEMdq_XMMi64_VL128	vpgatherdq xmm1, [rdi+xmm2*1], xmm3	22	2
XED_IFORM_VPGATHERDQ_XMMu64_MASKmskw_MEMu64_AVX512_VL128	vpgatherdq xmm1{k1}, [rdi+xmm2*1]	22	2
XED_IFORM_VPGATHERDQ_YMMu64_MEMqq_YMMi64_VL256	vpgatherdq ymm1, [rdi+xmm2*1], ymm3	25	4
XED_IFORM_VPGATHERDQ_YMMu64_MASKmskw_MEMu64_AVX512_VL256	vpgatherdq ymm1{k1}, [rdi+xmm2*1]	25	4
XED_IFORM_VPGATHERDQ_ZMMu64_MASKmskw_MEMu64_AVX512_VL512	vpgatherdq zmm1{k1}, [rdi+ymm2*1]	26	5
XED_IFORM_VPGATHERQD_XMMu32_MEMq_XMMi32_VL128	vpgatherqd xmm1, [rdi+ymm2*1], xmm3	20	2
XED_IFORM_VPGATHERQD_XMMu32_MEMdq_XMMi32_VL256	vpgatherqd xmm1, [rdi+ymm2*1], xmm3	20	2
XED_IFORM_VPGATHERQD_XMMu32_MASKmskw_MEMu32_AVX512_VL128	vpgatherqd xmm1{k1}, [rdi+ymm2*1]	20	2
XED_IFORM_VPGATHERQD_XMMu32_MASKmskw_MEMu32_AVX512_VL256	vpgatherqd xmm1{k1}, [rdi+ymm2*1]	20	2
XED_IFORM_VPGATHERQD_YMMu32_MASKmskw_MEMu32_AVX512_VL512	vpgatherqd ymm1{k1}, [rdi+zmm2*1]	25	4
XED_IFORM_VPGATHERQQ_XMMu64_MEMdq_XMMi64_VL128	vpgatherqq xmm1, [rdi+xmm2*1], xmm3	22	2
XED_IFORM_VPGATHERQQ_XMMu64_MASKmskw_MEMu64_AVX512_VL128	vpgatherqq xmm1{k1}, [rdi+xmm2*1]	22	2
XED_IFORM_VPGATHERQQ_YMMu64_MASKmskw_MEMu64_AVX512_VL256	vpgatherqq ymm1{k1}, [rdi+ymm2*1]	25	4
XED_IFORM_VPGATHERQQ_ZMMu64_MASKmskw_MEMu64_AVX512_VL512	vpgatherqq zmm1{k1}, [rdi+zmm2*1]	26	5
XED_IFORM_PHADDD_XMMdq_MEMdq	vphaddd xmm1, xmm1, [rdi]	9	2
XED_IFORM_PHADDD_XMMdq_XMMdq	vphaddd xmm1, xmm1, xmm2	3	2

XED_IFORM_VPHADDD_XMMdq_XMMdq_MEMdq	vphaddd xmm1, xmm2, [rdi]	9	2
XED_IFORM_VPHADDD_XMMdq_XMMdq_XMMdq	vphaddd xmm1, xmm2, xmm3	3	2
XED_IFORM_VPHADDD_YMMqq_YMMqq_MEMqq	vphaddd ymm1, ymm2, [rdi]	3	2
XED_IFORM_VPHADDD_YMMqq_YMMqq_YMMqq	vphaddd ymm1, ymm2, ymm3	3	2
XED_IFORM_PHADDSW_XMMdq_MEMdq	vphaddsw xmm1, xmm1, [rdi]	9	2
XED_IFORM_PHADDSW_XMMdq_XMMdq	vphaddsw xmm1, xmm1, xmm2	3	2
XED_IFORM_VPHADDSW_XMMdq_XMMdq_MEMdq	vphaddsw xmm1, xmm2, [rdi]	9	2
XED_IFORM_VPHADDSW_XMMdq_XMMdq_XMMdq	vphaddsw xmm1, xmm2, xmm3	3	2
XED_IFORM_VPHADDSW_YMMqq_YMMqq_MEMqq	vphaddsw ymm1, ymm2, [rdi]	3	2
XED_IFORM_VPHADDSW_YMMqq_YMMqq_YMMqq	vphaddsw ymm1, ymm2, ymm3	3	2
XED_IFORM_PHADDW_XMMdq_MEMdq	vphaddw xmm1, xmm1, [rdi]	9	2
XED_IFORM_PHADDW_XMMdq_XMMdq	vphaddw xmm1, xmm1, xmm2	3	2
XED_IFORM_VPHADDW_XMMdq_XMMdq_MEMdq	vphaddw xmm1, xmm2, [rdi]	9	2
XED_IFORM_VPHADDW_XMMdq_XMMdq_XMMdq	vphaddw xmm1, xmm2, xmm3	3	2
XED_IFORM_VPHADDW_YMMqq_YMMqq_MEMqq	vphaddw ymm1, ymm2, [rdi]	3	2
XED_IFORM_VPHADDW_YMMqq_YMMqq_YMMqq	vphaddw ymm1, ymm2, ymm3	3	2
XED_IFORM_PHMINPOSUW_XMMdq_MEMdq	vphminposuw xmm1, [rdi]	10	0.5
XED_IFORM_VPHMINPOSUW_XMMdq_MEMdq	vphminposuw xmm1, [rdi]	10	0.5
XED_IFORM_VPHMINPOSUW_XMMdq_XMMdq	vphminposuw xmm1, xmm2	4	0.33
XED_IFORM_PHMINPOSUW_XMMdq_XMMdq	vphminposuw xmm1, xmm2	4	0.33
XED_IFORM_PHSUBD_XMMdq_MEMdq	vphsubd xmm1, xmm1, [rdi]	9	2
XED_IFORM_PHSUBD_XMMdq_XMMdq	vphsubd xmm1, xmm1, xmm2	3	2
XED_IFORM_VPHSUBD_XMMdq_XMMdq_MEMdq	vphsubd xmm1, xmm2, [rdi]	9	2
XED_IFORM_VPHSUBD_XMMdq_XMMdq_XMMdq	vphsubd xmm1, xmm2, xmm3	3	2
XED_IFORM_VPHSUBD_YMMqq_YMMqq_MEMqq	vphsubd ymm1, ymm2, [rdi]	3	2
XED_IFORM_VPHSUBD_YMMqq_YMMqq_YMMqq	vphsubd ymm1, ymm2, ymm3	3	2
XED_IFORM_PHSUBSW_XMMdq_MEMdq	vphsubsw xmm1, xmm1, [rdi]	9	2
XED_IFORM_PHSUBSW_XMMdq_XMMdq	vphsubsw xmm1, xmm1, xmm2	3	2
XED_IFORM_VPHSUBSW_XMMdq_XMMdq_MEMdq	vphsubsw xmm1, xmm2, [rdi]	9	2
XED_IFORM_VPHSUBSW_XMMdq_XMMdq_XMMdq	vphsubsw xmm1, xmm2, xmm3	3	2
XED_IFORM_VPHSUBSW_YMMqq_YMMqq_MEMqq	vphsubsw ymm1, ymm2, [rdi]	3	2
XED_IFORM_VPHSUBSW_YMMqq_YMMqq_YMMqq	vphsubsw ymm1, ymm2, ymm3	3	2
XED_IFORM_PHSUBW_XMMdq_MEMdq	vphsubw xmm1, xmm1, [rdi]	9	2
XED_IFORM_PHSUBW_XMMdq_XMMdq	vphsubw xmm1, xmm1, xmm2	3	2
XED_IFORM_VPHSUBW_XMMdq_XMMdq_MEMdq	vphsubw xmm1, xmm2, [rdi]	9	2
XED_IFORM_VPHSUBW_XMMdq_XMMdq_XMMdq	vphsubw xmm1, xmm2, xmm3	3	2
XED_IFORM_VPHSUBW_YMMqq_YMMqq_MEMqq	vphsubw ymm1, ymm2, [rdi]	3	2
XED_IFORM_VPHSUBW_YMMqq_YMMqq_YMMqq	vphsubw ymm1, ymm2, ymm3	3	2
XED_IFORM_PINSRB_XMMdq_MEMb_IMMb	vpinsrb xmm1, xmm1, [rdi], 1	6	1
XED_IFORM_PINSRB_XMMdq_GPR32d_IMMb	vpinsrb xmm1, xmm1, eax, 1	2	2
XED_IFORM_VPINSRB_XMMu8_XMMu8_MEMu8_IMM8_AVX512	vpinsrb xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRB_XMMdq_XMMdq_MEMb_IMMb	vpinsrb xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRB_XMMu8_XMMu8_GPR32u8_IMM8_AVX512	vpinsrb xmm1, xmm2, eax, 1	2	2
XED_IFORM_VPINSRB_XMMdq_XMMdq_GPR32d_IMMb	vpinsrb xmm1, xmm2, eax, 1	2	2
XED_IFORM_PINSRD_XMMdq_MEMd_IMMb	vpinsrd xmm1, xmm1, [rdi], 1	6	1
XED_IFORM_PINSRD_XMMdq_GPR32d_IMMb	vpinsrd xmm1, xmm1, eax, 1	2	2
XED_IFORM_VPINSRD_XMMdq_XMMdq_MEMd_IMMb	vpinsrd xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRD_XMMu32_XMMu32_MEMu32_IMM8_AVX512	vpinsrd xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRD_XMMu32_XMMu32_GPR32u32_IMM8_AVX512	vpinsrd xmm1, xmm2, eax, 1	2	2
XED_IFORM_VPINSRD_XMMdq_XMMdq_GPR32d_IMMb	vpinsrd xmm1, xmm2, eax, 1	2	2
XED_IFORM_PINSRQ_XMMdq_MEMq_IMMb	vpinsrq xmm1, xmm1, [rdi], 1	6	1
XED_IFORM_PINSRQ_XMMdq_GPR64q_IMMb	vpinsrq xmm1, xmm1, rax, 1	2	2
XED_IFORM_VPINSRQ_XMMdq_XMMdq_MEMq_IMMb	vpinsrq xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRQ_XMMu64_XMMu64_MEMu64_IMM8_AVX512	vpinsrq xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRQ_XMMdq_XMMdq_GPR64q_IMMb	vpinsrq xmm1, xmm2, rax, 1	2	2
XED_IFORM_VPINSRQ_XMMu64_XMMu64_GPR64u64_IMM8_AVX512	vpinsrq xmm1, xmm2, rax, 1	2	2
XED_IFORM_PINSRW_XMMdq_MEMw_IMMb	vpinsrw xmm1, xmm1, [rdi], 1	6	1
XED_IFORM_PINSRW_XMMdq_GPR32_IMMb	vpinsrw xmm1, xmm1, eax, 1	2	2
XED_IFORM_VPINSRW_XMMdq_XMMdq_MEMw_IMMb	vpinsrw xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRW_XMMu16_XMMu16_MEMu16_IMM8_AVX512	vpinsrw xmm1, xmm2, [rdi], 1	6	1
XED_IFORM_VPINSRW_XMMdq_XMMdq_GPR32d_IMMb	vpinsrw xmm1, xmm2, eax, 1	2	2
XED_IFORM_VPINSRW_XMMu16_XMMu16_GPR32u16_IMM8_AVX512	vpinsrw xmm1, xmm2, eax, 1	2	2
XED_IFORM_VPLZCNTD_XMMu32_MASKmskw_MEMu32_AVX512	vplzcntd xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VPLZCNTD_XMMu32_MASKmskw_XMMu32_AVX512	vplzcntd xmm1{k1}, xmm2	4	0.5
XED_IFORM_VPLZCNTD_YMMu32_MASKmskw_MEMu32_AVX512	vplzcntd ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VPLZCNTD_YMMu32_MASKmskw_YMMu32_AVX512	vplzcntd ymm1{k1}, ymm2	4	0.5
XED_IFORM_VPLZCNTD_ZMMu32_MASKmskw_MEMu32_AVX512CD	vplzcntd zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VPLZCNTD_ZMMu32_MASKmskw_ZMMu32_AVX512CD	vplzcntd zmm1{k1}, zmm2	4	0.5
XED_IFORM_VPLZCNTQ_XMMu64_MASKmskw_MEMu64_AVX512	vplzcntq xmm1{k1}, [rdi]	10	0.5
XED_IFORM_VPLZCNTQ_XMMu64_MASKmskw_XMMu64_AVX512	vplzcntq xmm1{k1}, xmm2	4	0.5
XED_IFORM_VPLZCNTQ_YMMu64_MASKmskw_MEMu64_AVX512	vplzcntq ymm1{k1}, [rdi]	4	0.5
XED_IFORM_VPLZCNTQ_YMMu64_MASKmskw_YMMu64_AVX512	vplzcntq ymm1{k1}, ymm2	4	0.5
XED_IFORM_VPLZCNTQ_ZMMu64_MASKmskw_MEMu64_AVX512CD	vplzcntq zmm1{k1}, [rdi]	11	0.5
XED_IFORM_VPLZCNTQ_ZMMu64_MASKmskw_ZMMu64_AVX512CD	vplzcntq zmm1{k1}, zmm2	4	0.5
XED_IFORM_PMADDUBSW_XMMdq_MEMdq	vpmaddubsw xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_PMADDUBSW_XMMdq_XMMdq	vpmaddubsw xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMADDUBSW_XMMdq_XMMdq_MEMdq	vpmaddubsw xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VPMADDUBSW_XMMdq_XMMdq_XMMdq	vpmaddubsw xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMADDUBSW_XMMi16_MASKmskw_XMMi16_MEMi16_AVX512	vpmaddubsw xmm1{k1}, xmm2, [rdi]	10	0.5

XED_IFORM_VPMADDUBSW_XMMi16_MASKmskw_XMMi16_XMMi16_AVX512	vpmaddubsw xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMADDUBSW_YMMqq_YMMqq_MEMqq	vpmaddubsw ymm1, ymm2, [rdi]	5	0.5
XED_IFORM_VPMADDUBSW_YMMqq_YMMqq_YMMqq	vpmaddubsw ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMADDUBSW_YMMi16_MASKmskw_YMMi16_MEMi16_AVX512	vpmaddubsw ymm1{k1}, ymm2, [rdi]	11	0.5
XED_IFORM_VPMADDUBSW_YMMi16_MASKmskw_YMMi16_YMMi16_AVX512	vpmaddubsw ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMADDUBSW_ZMMi16_MASKmskw_ZMMi16_MEMi16_AVX512	vpmaddubsw zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VPMADDUBSW_ZMMi16_MASKmskw_ZMMi16_ZMMi16_AVX512	vpmaddubsw zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_PMADDWD_XMMdq_MEMdq	vpmaddwd xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_PMADDWD_XMMdq_XMMdq	vpmaddwd xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMADDWD_XMMdq_XMMdq_MEMdq	vpmaddwd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VPMADDWD_XMMdq_XMMdq_XMMdq	vpmaddwd xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMADDWD_XMMi32_MASKmskw_XMMi16_MEMi16_AVX512	vpmaddwd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VPMADDWD_XMMi32_MASKmskw_XMMi16_XMMi16_AVX512	vpmaddwd xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMADDWD_YMMqq_YMMqq_MEMqq	vpmaddwd ymm1, ymm2, [rdi]	11	0.5
XED_IFORM_VPMADDWD_YMMqq_YMMqq_YMMqq	vpmaddwd ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMADDWD_YMMi32_MASKmskw_YMMi16_MEMi16_AVX512	vpmaddwd ymm1{k1}, ymm2, [rdi]	11	0.5
XED_IFORM_VPMADDWD_YMMi32_MASKmskw_YMMi16_YMMi16_AVX512	vpmaddwd ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMADDWD_ZMMi32_MASKmskw_ZMMi16_MEMi16_AVX512	vpmaddwd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VPMADDWD_ZMMi32_MASKmskw_ZMMi16_ZMMi16_AVX512	vpmaddwd zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_VPMASKMOVD_MEMdq_XMMdq_XMMdq	vpmaskmovd [rdi], xmm1, xmm2	6	1
XED_IFORM_VPMASKMOVD_MEMqq_YMMqq_YMMqq	vpmaskmovd [rdi], ymm1, ymm2	6	1
XED_IFORM_VPMASKMOVD_XMMdq_XMMdq_MEMdq	vpmaskmovd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMASKMOVD_YMMqq_YMMqq_MEMqq	vpmaskmovd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMASKMOVQ_MEMdq_XMMdq_XMMdq	vpmaskmovq [rdi], xmm1, xmm2	6	1
XED_IFORM_VPMASKMOVQ_MEMqq_YMMqq_YMMqq	vpmaskmovq [rdi], ymm1, ymm2	6	1
XED_IFORM_VPMASKMOVQ_XMMdq_XMMdq_MEMdq	vpmaskmovq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMASKMOVQ_YMMqq_YMMqq_MEMqq	vpmaskmovq ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_PMAXSB_XMMdq_MEMdq	vpmaxsb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMAXSB_XMMdq_XMMdq	vpmaxsb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMAXSB_XMMdq_XMMdq_MEMdq	vpmaxsb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXSB_XMMdq_XMMdq_XMMdq	vpmaxsb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXSB_XMMi8_MASKmskw_XMMi8_MEMi8_AVX512	vpmaxsb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXSB_XMMi8_MASKmskw_XMMi8_XMMi8_AVX512	vpmaxsb xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXSB_YMMqq_YMMqq_MEMqq	vpmaxsb ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMAXSB_YMMqq_YMMqq_YMMqq	vpmaxsb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXSB_YMMi8_MASKmskw_YMMi8_MEMi8_AVX512	vpmaxsb ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPMAXSB_YMMi8_MASKmskw_YMMi8_YMMi8_AVX512	vpmaxsb ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXSB_ZMMi8_MASKmskw_ZMMi8_MEMi8_AVX512	vpmaxsb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMAXSB_ZMMi8_MASKmskw_ZMMi8_ZMMi8_AVX512	vpmaxsb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMAXSD_XMMdq_MEMdq	vpmaxsd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMAXSD_XMMdq_XMMdq	vpmaxsd xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMAXSD_XMMdq_XMMdq_MEMdq	vpmaxsd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXSD_XMMdq_XMMdq_XMMdq	vpmaxsd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXSD_XMMi32_MASKmskw_XMMi32_MEMi32_AVX512	vpmaxsd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXSD_XMMi32_MASKmskw_XMMi32_XMMi32_AVX512	vpmaxsd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXSD_YMMqq_YMMqq_MEMqq	vpmaxsd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMAXSD_YMMqq_YMMqq_YMMqq	vpmaxsd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXSD_YMMi32_MASKmskw_YMMi32_MEMi32_AVX512	vpmaxsd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPMAXSD_YMMi32_MASKmskw_YMMi32_YMMi32_AVX512	vpmaxsd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXSD_ZMMi32_MASKmskw_ZMMi32_MEMi32_AVX512	vpmaxsd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMAXSD_ZMMi32_MASKmskw_ZMMi32_ZMMi32_AVX512	vpmaxsd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPMAXSQ_XMMi64_MASKmskw_XMMi64_MEMi64_AVX512	vpmaxsq xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPMAXSQ_XMMi64_MASKmskw_XMMi64_XMMi64_AVX512	vpmaxsq xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPMAXSQ_YMMi64_MASKmskw_YMMi64_MEMi64_AVX512	vpmaxsq ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPMAXSQ_YMMi64_MASKmskw_YMMi64_YMMi64_AVX512	vpmaxsq ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPMAXSQ_ZMMi64_MASKmskw_ZMMi64_MEMi64_AVX512	vpmaxsq zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPMAXSQ_ZMMi64_MASKmskw_ZMMi64_ZMMi64_AVX512	vpmaxsq zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_VPMAXSW_XMMdq_MEMdq	vpmaxsw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_VPMAXSW_XMMdq_XMMdq	vpmaxsw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMAXSW_XMMdq_XMMdq_MEMdq	vpmaxsw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXSW_XMMdq_XMMdq_XMMdq	vpmaxsw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXSW_XMMi16_MASKmskw_XMMi16_MEMi16_AVX512	vpmaxsw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXSW_XMMi16_MASKmskw_XMMi16_XMMi16_AVX512	vpmaxsw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXSW_YMMqq_YMMqq_MEMqq	vpmaxsw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMAXSW_YMMqq_YMMqq_YMMqq	vpmaxsw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXSW_YMMi16_MASKmskw_YMMi16_MEMi16_AVX512	vpmaxsw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPMAXSW_YMMi16_MASKmskw_YMMi16_YMMi16_AVX512	vpmaxsw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXSW_ZMMi16_MASKmskw_ZMMi16_MEMi16_AVX512	vpmaxsw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMAXSW_ZMMi16_MASKmskw_ZMMi16_ZMMi16_AVX512	vpmaxsw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMAXUB_XMMdq_MEMdq	vpmaxub xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMAXUB_XMMdq_XMMdq	vpmaxub xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMAXUB_XMMdq_XMMdq_MEMdq	vpmaxub xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXUB_XMMdq_XMMdq_XMMdq	vpmaxub xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXUB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpmaxub xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXUB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpmaxub xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXUB_YMMqq_YMMqq_MEMqq	vpmaxub ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMAXUB_YMMqq_YMMqq_YMMqq	vpmaxub ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXUB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpmaxub ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPMAXUB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpmaxub ymm1{k1}, ymm2, ymm3	1	0.5

XED_IFORM_VPMAXUB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpmaxub zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMAXUB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpmaxub zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMAXUD_XMMdq_MEMdq	vpmaxud xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMAXUD_XMMdq_XMMdq	vpmaxud xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMAXUD_XMMdq_XMMdq_MEMdq	vpmaxud xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXUD_XMMdq_XMMdq_XMMdq	vpmaxud xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXUD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpmaxud xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXUD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpmaxud xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXUD_YMMqq_YMMqq_MEMqq	vpmaxud ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMAXUD_YMMqq_YMMqq_YMMqq	vpmaxud ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXUD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpmaxud ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPMAXUD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpmaxud ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXUD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpmaxud zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMAXUD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpmaxud zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPMAXUQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpmaxuq xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPMAXUQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpmaxuq xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPMAXUQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpmaxuq ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPMAXUQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpmaxuq ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPMAXUQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpmaxuq zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPMAXUQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpmaxuq zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_PMAXUW_XMMdq_MEMdq	vpmaxuw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMAXUW_XMMdq_XMMdq	vpmaxuw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMAXUW_XMMdq_XMMdq_MEMdq	vpmaxuw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXUW_XMMdq_XMMdq_XMMdq	vpmaxuw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXUW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpmaxuw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMAXUW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpmaxuw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMAXUW_YMMqq_YMMqq_MEMqq	vpmaxuw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMAXUW_YMMqq_YMMqq_YMMqq	vpmaxuw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXUW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpmaxuw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPMAXUW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpmaxuw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMAXUW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpmaxuw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMAXUW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpmaxuw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMINSB_XMMdq_MEMdq	vpminsb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMINSB_XMMdq_XMMdq	vpminsb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMINSB_XMMdq_XMMdq_MEMdq	vpminsb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINSB_XMMdq_XMMdq_XMMdq	vpminsb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMINSB_XMMi8_MASKmskw_XMMi8_MEMi8_AVX512	vpminsb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINSB_XMMi8_MASKmskw_XMMi8_XMMi8_AVX512	vpminsb xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMINSB_YMMqq_YMMqq_MEMqq	vpminsb ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMINSB_YMMqq_YMMqq_YMMqq	vpminsb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMINSB_YMMi8_MASKmskw_YMMi8_MEMi8_AVX512	vpminsb ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPMINSB_YMMi8_MASKmskw_YMMi8_YMMi8_AVX512	vpminsb ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMINSB_ZMMi8_MASKmskw_ZMMi8_MEMi8_AVX512	vpminsb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMINSB_ZMMi8_MASKmskw_ZMMi8_ZMMi8_AVX512	vpminsb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMINSD_XMMdq_MEMdq	vpminsd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMINSD_XMMdq_XMMdq	vpminsd xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMINSD_XMMdq_XMMdq_MEMdq	vpminsd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINSD_XMMdq_XMMdq_XMMdq	vpminsd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMINSD_XMMi32_MASKmskw_XMMi32_MEMi32_AVX512	vpminsd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINSD_XMMi32_MASKmskw_XMMi32_XMMi32_AVX512	vpminsd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMINSD_YMMqq_YMMqq_MEMqq	vpminsd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMINSD_YMMqq_YMMqq_YMMqq	vpminsd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMINSD_YMMi32_MASKmskw_YMMi32_MEMi32_AVX512	vpminsd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPMINSD_YMMi32_MASKmskw_YMMi32_YMMi32_AVX512	vpminsd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMINSD_ZMMi32_MASKmskw_ZMMi32_MEMi32_AVX512	vpminsd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMINSD_ZMMi32_MASKmskw_ZMMi32_ZMMi32_AVX512	vpminsd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPMINSQ_XMMi64_MASKmskw_XMMi64_MEMi64_AVX512	vpminsq xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPMINSQ_XMMi64_MASKmskw_XMMi64_XMMi64_AVX512	vpminsq xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPMINSQ_YMMi64_MASKmskw_YMMi64_MEMi64_AVX512	vpminsq ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPMINSQ_YMMi64_MASKmskw_YMMi64_YMMi64_AVX512	vpminsq ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPMINSQ_ZMMi64_MASKmskw_ZMMi64_MEMi64_AVX512	vpminsq zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPMINSQ_ZMMi64_MASKmskw_ZMMi64_ZMMi64_AVX512	vpminsq zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_PMINSW_XMMdq_MEMdq	vpminsw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMINSW_XMMdq_XMMdq	vpminsw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMINSW_XMMdq_XMMdq_MEMdq	vpminsw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINSW_XMMdq_XMMdq_XMMdq	vpminsw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMINSW_XMMi16_MASKmskw_XMMi16_MEMi16_AVX512	vpminsw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINSW_XMMi16_MASKmskw_XMMi16_XMMi16_AVX512	vpminsw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMINSW_YMMqq_YMMqq_MEMqq	vpminsw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMINSW_YMMqq_YMMqq_YMMqq	vpminsw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMINSW_YMMi16_MASKmskw_YMMi16_MEMi16_AVX512	vpminsw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPMINSW_YMMi16_MASKmskw_YMMi16_YMMi16_AVX512	vpminsw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMINSW_ZMMi16_MASKmskw_ZMMi16_MEMi16_AVX512	vpminsw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMINSW_ZMMi16_MASKmskw_ZMMi16_ZMMi16_AVX512	vpminsw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMINUB_XMMdq_MEMdq	vpminub xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMINUB_XMMdq_XMMdq	vpminub xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMINUB_XMMdq_XMMdq_MEMdq	vpminub xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINUB_XMMdq_XMMdq_XMMdq	vpminub xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMINUB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpminub xmm1{k1}, xmm2, [rdi]	7	0.5

XED_IFORM_VPMINUB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpminub xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMINUB_YMMqq_YMMqq_MEMqq	vpminub ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMINUB_YMMqq_YMMqq_YMMqq	vpminub ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMINUB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpminub ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPMINUB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpminub ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMINUB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpminub zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMINUB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpminub zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PMINUD_XMMdq_MEMdq	vpminud xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMINUD_XMMdq_XMMdq	vpminud xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMINUD_XMMdq_XMMdq_MEMdq	vpminud xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINUD_XMMdq_XMMdq_XMMdq	vpminud xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMINUD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpminud xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINUD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpminud xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMINUD_YMMqq_YMMqq_MEMqq	vpminud ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMINUD_YMMqq_YMMqq_YMMqq	vpminud ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMINUD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpminud ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPMINUD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpminud ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMINUD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpminud zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMINUD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpminud zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPMINUQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpminuq xmm1{k1}, xmm2, [rdi]	9	1
XED_IFORM_VPMINUQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpminuq xmm1{k1}, xmm2, xmm3	3	1
XED_IFORM_VPMINUQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpminuq ymm1{k1}, ymm2, [rdi]	3	1
XED_IFORM_VPMINUQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpminuq ymm1{k1}, ymm2, ymm3	3	1
XED_IFORM_VPMINUQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpminuq zmm1{k1}, zmm2, [rdi]	10	1
XED_IFORM_VPMINUQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpminuq zmm1{k1}, zmm2, zmm3	3	1
XED_IFORM_PMINUW_XMMdq_MEMdq	vpminuw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PMINUW_XMMdq_XMMdq	vpminuw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPMINUW_XMMdq_XMMdq_MEMdq	vpminuw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINUW_XMMdq_XMMdq_XMMdq	vpminuw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPMINUW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpminuw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPMINUW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpminuw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPMINUW_YMMqq_YMMqq_MEMqq	vpminuw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPMINUW_YMMqq_YMMqq_YMMqq	vpminuw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPMINUW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpminuw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPMINUW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpminuw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPMINUW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpminuw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPMINUW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpminuw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPMOVB2M_MASKmskw_XMMu8_AVX512	vpmovb2m k1, xmm1	1	1
XED_IFORM_VPMOVB2M_MASKmskw_YMMu8_AVX512	vpmovb2m k1, ymm1	1	1
XED_IFORM_VPMOVB2M_MASKmskw_ZMMu8_AVX512	vpmovb2m k1, zmm1	1	1
XED_IFORM_VPMOVD2M_MASKmskw_XMMu32_AVX512	vpmovd2m k1, xmm1	1	1
XED_IFORM_VPMOVD2M_MASKmskw_YMMu32_AVX512	vpmovd2m k1, ymm1	1	1
XED_IFORM_VPMOVD2M_MASKmskw_ZMMu32_AVX512	vpmovd2m k1, zmm1	1	1
XED_IFORM_VPMOVDB_MEMu8_MASKmskw_XMMu32_AVX512	vpmovdb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVDB_MEMu8_MASKmskw_YMMu32_AVX512	vpmovdb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVDB_MEMu8_MASKmskw_ZMMu32_AVX512	vpmovdb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVDB_XMMu8_MASKmskw_XMMu32_AVX512	vpmovdb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVDB_XMMu8_MASKmskw_YMMu32_AVX512	vpmovdb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVDB_XMMu8_MASKmskw_ZMMu32_AVX512	vpmovdb xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVDW_MEMu16_MASKmskw_XMMu32_AVX512	vpmovdw [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVDW_MEMu16_MASKmskw_YMMu32_AVX512	vpmovdw [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVDW_MEMu16_MASKmskw_ZMMu32_AVX512	vpmovdw [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVDW_XMMu16_MASKmskw_XMMu32_AVX512	vpmovdw xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVDW_XMMu16_MASKmskw_YMMu32_AVX512	vpmovdw xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVDW_YMMu16_MASKmskw_ZMMu32_AVX512	vpmovdw ymm1{k1}, zmm2	4	2
XED_IFORM_PMOVMSKB_GPR32_XMMdq	vpmovmskb eax, xmm1	2	1
XED_IFORM_VPMOVMSKB_GPR32d_XMMdq	vpmovmskb eax, xmm1	2	1
XED_IFORM_VPMOVMSKB_GPR32d_YMMqq	vpmovmskb eax, ymm1	2	1
XED_IFORM_VPMOVQ2M_MASKmskw_XMMu64_AVX512	vpmovq2m k1, xmm1	1	1
XED_IFORM_VPMOVQ2M_MASKmskw_YMMu64_AVX512	vpmovq2m k1, ymm1	1	1
XED_IFORM_VPMOVQ2M_MASKmskw_ZMMu64_AVX512	vpmovq2m k1, zmm1	1	1
XED_IFORM_VPMOVQB_MEMu8_MASKmskw_XMMu64_AVX512	vpmovqb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVQB_MEMu8_MASKmskw_YMMu64_AVX512	vpmovqb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVQB_MEMu8_MASKmskw_ZMMu64_AVX512	vpmovqb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVQB_XMMu8_MASKmskw_XMMu64_AVX512	vpmovqb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVQB_XMMu8_MASKmskw_YMMu64_AVX512	vpmovqb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVQB_XMMu8_MASKmskw_ZMMu64_AVX512	vpmovqb xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVQD_MEMu32_MASKmskw_XMMu64_AVX512	vpmovqd [rdi]{k1}, xmm1	8	1
XED_IFORM_VPMOVQD_MEMu32_MASKmskw_YMMu64_AVX512	vpmovqd [rdi]{k1}, ymm1	8	1
XED_IFORM_VPMOVQD_MEMu32_MASKmskw_ZMMu64_AVX512	vpmovqd [rdi]{k1}, zmm1	8	1
XED_IFORM_VPMOVQD_XMMu32_MASKmskw_XMMu64_AVX512	vpmovqd xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVQD_XMMu32_MASKmskw_YMMu64_AVX512	vpmovqd xmm1{k1}, ymm2	3	1
XED_IFORM_VPMOVQD_YMMu32_MASKmskw_ZMMu64_AVX512	vpmovqd ymm1{k1}, zmm2	3	1
XED_IFORM_VPMOVQW_MEMu16_MASKmskw_XMMu64_AVX512	vpmovqw [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVQW_MEMu16_MASKmskw_YMMu64_AVX512	vpmovqw [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVQW_MEMu16_MASKmskw_ZMMu64_AVX512	vpmovqw [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVQW_XMMu16_MASKmskw_XMMu64_AVX512	vpmovqw xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVQW_XMMu16_MASKmskw_YMMu64_AVX512	vpmovqw xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVQW_XMMu16_MASKmskw_ZMMu64_AVX512	vpmovqw xmm1{k1}, zmm2	4	2

XED_IFORM_VPMOVSDB_MEMi8_MASKmskw_XMMi32_AVX512	vpmovsdb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVSDB_MEMi8_MASKmskw_YMMi32_AVX512	vpmovsdb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVSDB_MEMi8_MASKmskw_ZMMi32_AVX512	vpmovsdb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVSDB_XMMi8_MASKmskw_XMMi32_AVX512	vpmovsdb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVSDB_XMMi8_MASKmskw_YMMi32_AVX512	vpmovsdb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVSDB_XMMi8_MASKmskw_ZMMi32_AVX512	vpmovsdb xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSDW_MEMi16_MASKmskw_XMMi32_AVX512	vpmovsdw [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVSDW_MEMi16_MASKmskw_YMMi32_AVX512	vpmovsdw [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVSDW_MEMi16_MASKmskw_ZMMi32_AVX512	vpmovsdw [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVSDW_XMMi16_MASKmskw_XMMi32_AVX512	vpmovsdw xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVSDW_XMMi16_MASKmskw_YMMi32_AVX512	vpmovsdw xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVSDW_YMMi16_MASKmskw_ZMMi32_AVX512	vpmovsdw ymm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSQB_MEMi8_MASKmskw_XMMi64_AVX512	vpmovsqb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVSQB_MEMi8_MASKmskw_YMMi64_AVX512	vpmovsqb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVSQB_MEMi8_MASKmskw_ZMMi64_AVX512	vpmovsqb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVSQB_XMMi8_MASKmskw_XMMi64_AVX512	vpmovsqb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVSQB_XMMi8_MASKmskw_YMMi64_AVX512	vpmovsqb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVSQB_XMMi8_MASKmskw_ZMMi64_AVX512	vpmovsqb xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSQD_MEMi32_MASKmskw_XMMi64_AVX512	vpmovsqd [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVSQD_MEMi32_MASKmskw_YMMi64_AVX512	vpmovsqd [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVSQD_MEMi32_MASKmskw_ZMMi64_AVX512	vpmovsqd [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVSQD_XMMi32_MASKmskw_XMMi64_AVX512	vpmovsqd xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVSQD_XMMi32_MASKmskw_YMMi64_AVX512	vpmovsqd xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVSQD_YMMi32_MASKmskw_ZMMi64_AVX512	vpmovsqd ymm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSQW_MEMi16_MASKmskw_XMMi64_AVX512	vpmovsqw [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVSQW_MEMi16_MASKmskw_YMMi64_AVX512	vpmovsqw [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVSQW_MEMi16_MASKmskw_ZMMi64_AVX512	vpmovsqw [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVSQW_XMMi16_MASKmskw_XMMi64_AVX512	vpmovsqw xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVSQW_XMMi16_MASKmskw_YMMi64_AVX512	vpmovsqw xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVSQW_XMMi16_MASKmskw_ZMMi64_AVX512	vpmovsqw xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSWB_MEMi8_MASKmskw_XMMi16_AVX512	vpmovswb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVSWB_MEMi8_MASKmskw_YMMi16_AVX512	vpmovswb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVSWB_MEMi8_MASKmskw_ZMMi16_AVX512	vpmovswb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVSWB_XMMi8_MASKmskw_XMMi16_AVX512	vpmovswb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVSWB_XMMi8_MASKmskw_YMMi16_AVX512	vpmovswb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVSWB_YMMi8_MASKmskw_ZMMi16_AVX512	vpmovswb ymm1{k1}, zmm2	4	2
XED_IFORM_VPMOVSXBD_XMMdq_MEMd	vpmovsxbd xmm1, [rdi]	6	1
XED_IFORM_PMOVSXBD_XMMdq_MEMd	vpmovsxbd xmm1, [rdi]	6	1
XED_IFORM_VPMOVSXBD_XMMdq_XMMd	vpmovsxbd xmm1, xmm2	1	1
XED_IFORM_PMOVSXBD_XMMdq_XMMd	vpmovsxbd xmm1, xmm2	1	1
XED_IFORM_VPMOVSXBD_XMMi32_MASKmskw_MEMi8_AVX512	vpmovsxbd xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVSXBD_XMMi32_MASKmskw_XMMi8_AVX512	vpmovsxbd xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBD_YMMqq_MEMq	vpmovsxbd ymm1, [rdi]	8	1
XED_IFORM_VPMOVSXBD_YMMqq_XMMq	vpmovsxbd ymm1, xmm2	3	1
XED_IFORM_VPMOVSXBD_YMMi32_MASKmskw_MEMi8_AVX512	vpmovsxbd ymm1{k1}, [rdi]	3	1
XED_IFORM_VPMOVSXBD_YMMi32_MASKmskw_XMMi8_AVX512	vpmovsxbd ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBD_ZMMi32_MASKmskw_MEMi8_AVX512	vpmovsxbd zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXBD_ZMMi32_MASKmskw_XMMi8_AVX512	vpmovsxbd zmm1{k1}, xmm2	3	1
XED_IFORM_PMOVSXBQ_XMMdq_MEMw	vpmovsxbq xmm1, [rdi]	6	1
XED_IFORM_VPMOVSXBQ_XMMdq_MEMw	vpmovsxbq xmm1, [rdi]	6	1
XED_IFORM_VPMOVSXBQ_XMMdq_XMMw	vpmovsxbq xmm1, xmm2	1	1
XED_IFORM_PMOVSXBQ_XMMdq_XMMw	vpmovsxbq xmm1, xmm2	1	1
XED_IFORM_VPMOVSXBQ_XMMi64_MASKmskw_MEMi8_AVX512	vpmovsxbq xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVSXBQ_XMMi64_MASKmskw_XMMi8_AVX512	vpmovsxbq xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBQ_YMMqq_MEMd	vpmovsxbq ymm1, [rdi]	8	1
XED_IFORM_VPMOVSXBQ_YMMqq_XMMd	vpmovsxbq ymm1, xmm2	3	1
XED_IFORM_VPMOVSXBQ_YMMi64_MASKmskw_MEMi8_AVX512	vpmovsxbq ymm1{k1}, [rdi]	3	1
XED_IFORM_VPMOVSXBQ_YMMi64_MASKmskw_XMMi8_AVX512	vpmovsxbq ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBQ_ZMMi64_MASKmskw_MEMi8_AVX512	vpmovsxbq zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXBQ_ZMMi64_MASKmskw_XMMi8_AVX512	vpmovsxbq zmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBW_XMMdq_MEMq	vpmovsxbw xmm1, [rdi]	6	1
XED_IFORM_PMOVSXBW_XMMdq_MEMq	vpmovsxbw xmm1, [rdi]	6	1
XED_IFORM_PMOVSXBW_XMMdq_XMMq	vpmovsxbw xmm1, xmm2	1	1
XED_IFORM_VPMOVSXBW_XMMdq_XMMq	vpmovsxbw xmm1, xmm2	1	1
XED_IFORM_VPMOVSXBW_XMMi16_MASKmskw_MEMi8_AVX512	vpmovsxbw xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVSXBW_XMMi16_MASKmskw_XMMi8_AVX512	vpmovsxbw xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBW_YMMqq_MEMdq	vpmovsxbw ymm1, [rdi]	9	1
XED_IFORM_VPMOVSXBW_YMMqq_XMMdq	vpmovsxbw ymm1, xmm2	3	1
XED_IFORM_VPMOVSXBW_YMMi16_MASKmskw_MEMi8_AVX512	vpmovsxbw ymm1{k1}, [rdi]	3	1
XED_IFORM_VPMOVSXBW_YMMi16_MASKmskw_XMMi8_AVX512	vpmovsxbw ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXBW_ZMMi16_MASKmskw_MEMi8_AVX512	vpmovsxbw zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXBW_ZMMi16_MASKmskw_YMMi8_AVX512	vpmovsxbw zmm1{k1}, ymm2	3	1
XED_IFORM_PMOVSXDQ_XMMdq_MEMq	vpmovsxdq xmm1, [rdi]	6	1
XED_IFORM_VPMOVSXDQ_XMMdq_MEMq	vpmovsxdq xmm1, [rdi]	6	1
XED_IFORM_PMOVSXDQ_XMMdq_XMMq	vpmovsxdq xmm1, xmm2	1	1
XED_IFORM_VPMOVSXDQ_XMMdq_XMMq	vpmovsxdq xmm1, xmm2	1	1
XED_IFORM_VPMOVSXDQ_XMMi64_MASKmskw_MEMi32_AVX512	vpmovsxdq xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVSXDQ_XMMi64_MASKmskw_XMMi32_AVX512	vpmovsxdq xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXDQ_YMMqq_MEMdq	vpmovsxdq ymm1, [rdi]	9	1

XED_IFORM_VPMOVSXDQ_YMMqq_XMMdq	vpmovsxdq ymm1, xmm2	3	1
XED_IFORM_VPMOVSXDQ_YMMi64_MASKmskw_MEMi32_AVX512	vpmovsxdq ymm1{k1}, [rdi]	3	1
XED_IFORM_VPMOVSXDQ_YMMi64_MASKmskw_XMMi32_AVX512	vpmovsxdq ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXDQ_ZMMi64_MASKmskw_MEMi32_AVX512	vpmovsxdq zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXDQ_ZMMi64_MASKmskw_YMMi32_AVX512	vpmovsxdq zmm1{k1}, ymm2	3	1
XED_IFORM_PMOVSXWD_XMMdq_MEMq	vpmovsxwd xmm1, [rdi]	6	1
XED_IFORM_VPMOVSXWD_XMMdq_MEMq	vpmovsxwd xmm1, [rdi]	6	1
XED_IFORM_VPMOVSXWD_XMMdq_XMMq	vpmovsxwd xmm1, xmm2	1	1
XED_IFORM_PMOVSXWD_XMMdq_XMMq	vpmovsxwd xmm1, xmm2	1	1
XED_IFORM_VPMOVSXWD_XMMi32_MASKmskw_MEMi16_AVX512	vpmovsxwd xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVSXWD_XMMi32_MASKmskw_XMMi16_AVX512	vpmovsxwd xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXWD_YMMqq_MEMdq	vpmovsxwd ymm1, [rdi]	9	1
XED_IFORM_VPMOVSXWD_YMMqq_XMMdq	vpmovsxwd ymm1, xmm2	3	1
XED_IFORM_VPMOVSXWD_YMMi32_MASKmskw_MEMi16_AVX512	vpmovsxwd ymm1{k1}, [rdi]	3	1
XED_IFORM_VPMOVSXWD_YMMi32_MASKmskw_XMMi16_AVX512	vpmovsxwd ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXWD_ZMMi32_MASKmskw_MEMi16_AVX512	vpmovsxwd zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXWD_ZMMi32_MASKmskw_YMMi16_AVX512	vpmovsxwd zmm1{k1}, ymm2	3	1
XED_IFORM_VPMOVSXWQ_XMMdq_MEMd	vpmovsxwq xmm1, [rdi]	6	1
XED_IFORM_PMOVSXWQ_XMMdq_MEMd	vpmovsxwq xmm1, [rdi]	6	1
XED_IFORM_PMOVSXWQ_XMMdq_XMMd	vpmovsxwq xmm1, xmm2	1	1
XED_IFORM_VPMOVSXWQ_XMMdq_XMMd	vpmovsxwq xmm1, xmm2	1	1
XED_IFORM_VPMOVSXWQ_XMMi64_MASKmskw_MEMi16_AVX512	vpmovsxwq xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVSXWQ_XMMi64_MASKmskw_XMMi16_AVX512	vpmovsxwq xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXWQ_YMMqq_MEMq	vpmovsxwq ymm1, [rdi]	8	1
XED_IFORM_VPMOVSXWQ_YMMqq_XMMq	vpmovsxwq ymm1, xmm2	3	1
XED_IFORM_VPMOVSXWQ_YMMi64_MASKmskw_MEMi16_AVX512	vpmovsxwq ymm1{k1}, [rdi]	3	1
XED_IFORM_VPMOVSXWQ_YMMi64_MASKmskw_XMMi16_AVX512	vpmovsxwq ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVSXWQ_ZMMi64_MASKmskw_MEMi16_AVX512	vpmovsxwq zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVSXWQ_ZMMi64_MASKmskw_XMMi16_AVX512	vpmovsxwq zmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVUSDB_MEMu8_MASKmskw_XMMu32_AVX512	vpmovusdb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVUSDB_MEMu8_MASKmskw_YMMu32_AVX512	vpmovusdb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVUSDB_MEMu8_MASKmskw_ZMMu32_AVX512	vpmovusdb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVUSDB_XMMu8_MASKmskw_XMMu32_AVX512	vpmovusdb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVUSDB_XMMu8_MASKmskw_YMMu32_AVX512	vpmovusdb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVUSDB_XMMu8_MASKmskw_ZMMu32_AVX512	vpmovusdb xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVUSDW_MEMu16_MASKmskw_XMMu32_AVX512	vpmovusdw [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVUSDW_MEMu16_MASKmskw_YMMu32_AVX512	vpmovusdw [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVUSDW_MEMu16_MASKmskw_ZMMu32_AVX512	vpmovusdw [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVUSDW_XMMu16_MASKmskw_XMMu32_AVX512	vpmovusdw xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVUSDW_XMMu16_MASKmskw_YMMu32_AVX512	vpmovusdw xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVUSDW_YMMu16_MASKmskw_ZMMu32_AVX512	vpmovusdw ymm1{k1}, zmm2	4	2
XED_IFORM_VPMOVUSQB_MEMu8_MASKmskw_XMMu64_AVX512	vpmovusqb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVUSQB_MEMu8_MASKmskw_YMMu64_AVX512	vpmovusqb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVUSQB_MEMu8_MASKmskw_ZMMu64_AVX512	vpmovusqb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVUSQB_XMMu8_MASKmskw_XMMu64_AVX512	vpmovusqb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVUSQB_XMMu8_MASKmskw_YMMu64_AVX512	vpmovusqb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVUSQB_XMMu8_MASKmskw_ZMMu64_AVX512	vpmovusqb xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVUSQD_MEMu32_MASKmskw_XMMu64_AVX512	vpmovusqd [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVUSQD_MEMu32_MASKmskw_YMMu64_AVX512	vpmovusqd [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVUSQD_MEMu32_MASKmskw_ZMMu64_AVX512	vpmovusqd [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVUSQD_XMMu32_MASKmskw_XMMu64_AVX512	vpmovusqd xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVUSQD_XMMu32_MASKmskw_YMMu64_AVX512	vpmovusqd xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVUSQD_YMMu32_MASKmskw_ZMMu64_AVX512	vpmovusqd ymm1{k1}, zmm2	4	2
XED_IFORM_VPMOVUSQW_MEMu16_MASKmskw_XMMu64_AVX512	vpmovusqw [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVUSQW_MEMu16_MASKmskw_YMMu64_AVX512	vpmovusqw [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVUSQW_MEMu16_MASKmskw_ZMMu64_AVX512	vpmovusqw [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVUSQW_XMMu16_MASKmskw_XMMu64_AVX512	vpmovusqw xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVUSQW_XMMu16_MASKmskw_YMMu64_AVX512	vpmovusqw xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVUSQW_XMMu16_MASKmskw_ZMMu64_AVX512	vpmovusqw xmm1{k1}, zmm2	4	2
XED_IFORM_VPMOVUSWB_MEMu8_MASKmskw_XMMu16_AVX512	vpmovuswb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVUSWB_MEMu8_MASKmskw_YMMu16_AVX512	vpmovuswb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVUSWB_MEMu8_MASKmskw_ZMMu16_AVX512	vpmovuswb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVUSWB_XMMu8_MASKmskw_XMMu16_AVX512	vpmovuswb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVUSWB_XMMu8_MASKmskw_YMMu16_AVX512	vpmovuswb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVUSWB_YMMu8_MASKmskw_ZMMu16_AVX512	vpmovuswb ymm1{k1}, zmm2	4	2
XED_IFORM_VPMOVW2M_MASKmskw_XMMu16_AVX512	vpmovw2m k1, xmm1	1	1
XED_IFORM_VPMOVW2M_MASKmskw_YMMu16_AVX512	vpmovw2m k1, ymm1	1	1
XED_IFORM_VPMOVW2M_MASKmskw_ZMMu16_AVX512	vpmovw2m k1, zmm1	1	1
XED_IFORM_VPMOVWB_MEMu8_MASKmskw_XMMu16_AVX512	vpmovwb [rdi]{k1}, xmm1	9	2
XED_IFORM_VPMOVWB_MEMu8_MASKmskw_YMMu16_AVX512	vpmovwb [rdi]{k1}, ymm1	9	2
XED_IFORM_VPMOVWB_MEMu8_MASKmskw_ZMMu16_AVX512	vpmovwb [rdi]{k1}, zmm1	9	2
XED_IFORM_VPMOVWB_XMMu8_MASKmskw_XMMu16_AVX512	vpmovwb xmm1{k1}, xmm2	4	2
XED_IFORM_VPMOVWB_XMMu8_MASKmskw_YMMu16_AVX512	vpmovwb xmm1{k1}, ymm2	4	2
XED_IFORM_VPMOVWB_YMMu8_MASKmskw_ZMMu16_AVX512	vpmovwb ymm1{k1}, zmm2	4	2
XED_IFORM_PMOVZXBD_XMMdq_MEMd	vpmovzxbd xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXBD_XMMdq_MEMd	vpmovzxbd xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXBD_XMMdq_XMMd	vpmovzxbd xmm1, xmm2	1	1
XED_IFORM_PMOVZXBD_XMMdq_XMMd	vpmovzxbd xmm1, xmm2	1	1
XED_IFORM_VPMOVZXBD_XMMi32_MASKmskw_MEMi8_AVX512	vpmovzxbd xmm1{k1}, [rdi]	9	1

XED_IFORM_VPMOVZXBD_XMMi32_MASKmskw_XMMi8_AVX512	vpmovzxbd xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBD_YMMqq_MEMq	vpmovzxbd ymm1, [rdi]	3	1
XED_IFORM_VPMOVZXBD_YMMqq_XMMq	vpmovzxbd ymm1, xmm2	3	1
XED_IFORM_VPMOVZXBD_YMMi32_MASKmskw_MEMi8_AVX512	vpmovzxbd ymm1{k1}, [rdi]	3	1
XED_IFORM_VPMOVZXBD_YMMi32_MASKmskw_XMMi8_AVX512	vpmovzxbd ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBD_ZMMi32_MASKmskw_MEMi8_AVX512	vpmovzxbd zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXBD_ZMMi32_MASKmskw_XMMi8_AVX512	vpmovzxbd zmm1{k1}, xmm2	3	1
XED_IFORM_PMOVZXBQ_XMMdq_MEMw	vpmovzxbq xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXBQ_XMMdq_MEMw	vpmovzxbq xmm1, [rdi]	6	1
XED_IFORM_PMOVZXBQ_XMMdq_XMMw	vpmovzxbq xmm1, xmm2	1	1
XED_IFORM_VPMOVZXBQ_XMMdq_XMMw	vpmovzxbq xmm1, xmm2	1	1
XED_IFORM_VPMOVZXBQ_XMMi64_MASKmskw_MEMi8_AVX512	vpmovzxbq xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVZXBQ_XMMi64_MASKmskw_XMMi8_AVX512	vpmovzxbq xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBQ_YMMqq_MEMd	vpmovzxbq ymm1, [rdi]	3	1
XED_IFORM_VPMOVZXBQ_YMMqq_XMMd	vpmovzxbq ymm1, xmm2	3	1
XED_IFORM_VPMOVZXBQ_YMMi64_MASKmskw_MEMi8_AVX512	vpmovzxbq ymm1{k1}, [rdi]	3	1
XED_IFORM_VPMOVZXBQ_YMMi64_MASKmskw_XMMi8_AVX512	vpmovzxbq ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBQ_ZMMi64_MASKmskw_MEMi8_AVX512	vpmovzxbq zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXBQ_ZMMi64_MASKmskw_XMMi8_AVX512	vpmovzxbq zmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBW_XMMdq_MEMq	vpmovzxbw xmm1, [rdi]	6	1
XED_IFORM_PMOVZXBW_XMMdq_MEMq	vpmovzxbw xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXBW_XMMdq_XMMq	vpmovzxbw xmm1, xmm2	1	1
XED_IFORM_PMOVZXBW_XMMdq_XMMq	vpmovzxbw xmm1, xmm2	1	1
XED_IFORM_VPMOVZXBW_XMMi16_MASKmskw_MEMi8_AVX512	vpmovzxbw xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVZXBW_XMMi16_MASKmskw_XMMi8_AVX512	vpmovzxbw xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBW_YMMqq_MEMdq	vpmovzxbw ymm1, [rdi]	3	1
XED_IFORM_VPMOVZXBW_YMMqq_XMMdq	vpmovzxbw ymm1, xmm2	3	1
XED_IFORM_VPMOVZXBW_YMMi16_MASKmskw_MEMi8_AVX512	vpmovzxbw ymm1{k1}, [rdi]	3	1
XED_IFORM_VPMOVZXBW_YMMi16_MASKmskw_XMMi8_AVX512	vpmovzxbw ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXBW_ZMMi16_MASKmskw_MEMi8_AVX512	vpmovzxbw zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXBW_ZMMi16_MASKmskw_YMMi8_AVX512	vpmovzxbw zmm1{k1}, ymm2	3	1
XED_IFORM_VPMOVZXDQ_XMMdq_MEMq	vpmovzxdq xmm1, [rdi]	6	1
XED_IFORM_PMOVZXDQ_XMMdq_MEMq	vpmovzxdq xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXDQ_XMMdq_XMMq	vpmovzxdq xmm1, xmm2	1	1
XED_IFORM_PMOVZXDQ_XMMdq_XMMq	vpmovzxdq xmm1, xmm2	1	1
XED_IFORM_VPMOVZXDQ_XMMi64_MASKmskw_MEMi32_AVX512	vpmovzxdq xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVZXDQ_XMMi64_MASKmskw_XMMi32_AVX512	vpmovzxdq xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXDQ_YMMqq_MEMdq	vpmovzxdq ymm1, [rdi]	3	1
XED_IFORM_VPMOVZXDQ_YMMqq_XMMdq	vpmovzxdq ymm1, xmm2	3	1
XED_IFORM_VPMOVZXDQ_YMMi64_MASKmskw_MEMi32_AVX512	vpmovzxdq ymm1{k1}, [rdi]	3	1
XED_IFORM_VPMOVZXDQ_YMMi64_MASKmskw_XMMi32_AVX512	vpmovzxdq ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXDQ_ZMMi64_MASKmskw_MEMi32_AVX512	vpmovzxdq zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXDQ_ZMMi64_MASKmskw_YMMi32_AVX512	vpmovzxdq zmm1{k1}, ymm2	3	1
XED_IFORM_VPMOVZXWD_XMMdq_MEMq	vpmovzxwd xmm1, [rdi]	6	1
XED_IFORM_PMOVZXWD_XMMdq_MEMq	vpmovzxwd xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXWD_XMMdq_XMMq	vpmovzxwd xmm1, xmm2	1	1
XED_IFORM_PMOVZXWD_XMMdq_XMMq	vpmovzxwd xmm1, xmm2	1	1
XED_IFORM_VPMOVZXWD_XMMi32_MASKmskw_MEMi16_AVX512	vpmovzxwd xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVZXWD_XMMi32_MASKmskw_XMMi16_AVX512	vpmovzxwd xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXWD_YMMqq_MEMdq	vpmovzxwd ymm1, [rdi]	9	1
XED_IFORM_VPMOVZXWD_YMMqq_XMMdq	vpmovzxwd ymm1, xmm2	3	1
XED_IFORM_VPMOVZXWD_YMMi32_MASKmskw_MEMi16_AVX512	vpmovzxwd ymm1{k1}, [rdi]	3	1
XED_IFORM_VPMOVZXWD_YMMi32_MASKmskw_XMMi16_AVX512	vpmovzxwd ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXWD_ZMMi32_MASKmskw_MEMi16_AVX512	vpmovzxwd zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXWD_ZMMi32_MASKmskw_YMMi16_AVX512	vpmovzxwd zmm1{k1}, ymm2	3	1
XED_IFORM_VPMOVZXWQ_XMMdq_MEMd	vpmovzxwq xmm1, [rdi]	6	1
XED_IFORM_PMOVZXWQ_XMMdq_MEMd	vpmovzxwq xmm1, [rdi]	6	1
XED_IFORM_VPMOVZXWQ_XMMdq_XMMd	vpmovzxwq xmm1, xmm2	1	1
XED_IFORM_PMOVZXWQ_XMMdq_XMMd	vpmovzxwq xmm1, xmm2	1	1
XED_IFORM_VPMOVZXWQ_XMMi64_MASKmskw_MEMi16_AVX512	vpmovzxwq xmm1{k1}, [rdi]	9	1
XED_IFORM_VPMOVZXWQ_XMMi64_MASKmskw_XMMi16_AVX512	vpmovzxwq xmm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXWQ_YMMqq_MEMq	vpmovzxwq ymm1, [rdi]	3	1
XED_IFORM_VPMOVZXWQ_YMMqq_XMMq	vpmovzxwq ymm1, xmm2	3	1
XED_IFORM_VPMOVZXWQ_YMMi64_MASKmskw_MEMi16_AVX512	vpmovzxwq ymm1{k1}, [rdi]	3	1
XED_IFORM_VPMOVZXWQ_YMMi64_MASKmskw_XMMi16_AVX512	vpmovzxwq ymm1{k1}, xmm2	3	1
XED_IFORM_VPMOVZXWQ_ZMMi64_MASKmskw_MEMi16_AVX512	vpmovzxwq zmm1{k1}, [rdi]	10	1
XED_IFORM_VPMOVZXWQ_ZMMi64_MASKmskw_XMMi16_AVX512	vpmovzxwq zmm1{k1}, xmm2	3	1
XED_IFORM_PMULDQ_XMMdq_MEMdq	vpmuldq xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_PMULDQ_XMMdq_XMMdq	vpmuldq xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMULDQ_XMMdq_XMMdq_MEMdq	vpmuldq xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VPMULDQ_XMMdq_XMMdq_XMMdq	vpmuldq xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMULDQ_XMMi64_MASKmskw_XMMi32_MEMi32_AVX512	vpmuldq xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VPMULDQ_XMMi64_MASKmskw_XMMi32_XMMi32_AVX512	vpmuldq xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMULDQ_YMMqq_YMMqq_MEMqq	vpmuldq ymm1, ymm2, [rdi]	11	0.5
XED_IFORM_VPMULDQ_YMMqq_YMMqq_YMMqq	vpmuldq ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMULDQ_YMMi64_MASKmskw_YMMi32_MEMi32_AVX512	vpmuldq ymm1{k1}, ymm2, [rdi]	11	0.5
XED_IFORM_VPMULDQ_YMMi64_MASKmskw_YMMi32_YMMi32_AVX512	vpmuldq ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMULDQ_ZMMi64_MASKmskw_ZMMi32_MEMi32_AVX512	vpmuldq zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VPMULDQ_ZMMi64_MASKmskw_ZMMi32_ZMMi32_AVX512	vpmuldq zmm1{k1}, zmm2, zmm3	5	0.5

XED_IFORM_PMULHRSW_XMMdq_MEMdq	vpmulhrsw xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_PMULHRSW_XMMdq_XMMdq	vpmulhrsw xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMULHRSW_XMMdq_XMMdq_MEMdq	vpmulhrsw xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VPMULHRSW_XMMdq_XMMdq_XMMdq	vpmulhrsw xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMULHRSW_XMMi16_MASKmskw_XMMi16_MEMi16_AVX512	vpmulhrsw xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VPMULHRSW_XMMi16_MASKmskw_XMMi16_XMMi16_AVX512	vpmulhrsw xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMULHRSW_YMMqq_YMMqq_MEMqq	vpmulhrsw ymm1, ymm2, [rdi]	11	0.5
XED_IFORM_VPMULHRSW_YMMqq_YMMqq_YMMqq	vpmulhrsw ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMULHRSW_YMMi16_MASKmskw_YMMi16_MEMi16_AVX512	vpmulhrsw ymm1{k1}, ymm2, [rdi]	11	0.5
XED_IFORM_VPMULHRSW_YMMi16_MASKmskw_YMMi16_YMMi16_AVX512	vpmulhrsw ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMULHRSW_ZMMi16_MASKmskw_ZMMi16_MEMi16_AVX512	vpmulhrsw zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VPMULHRSW_ZMMi16_MASKmskw_ZMMi16_ZMMi16_AVX512	vpmulhrsw zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_PMULHUW_XMMdq_MEMdq	vpmulhuw xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_PMULHUW_XMMdq_XMMdq	vpmulhuw xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMULHUW_XMMdq_XMMdq_MEMdq	vpmulhuw xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VPMULHUW_XMMdq_XMMdq_XMMdq	vpmulhuw xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMULHUW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpmulhuw xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VPMULHUW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpmulhuw xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMULHUW_YMMqq_YMMqq_MEMqq	vpmulhuw ymm1, ymm2, [rdi]	11	0.5
XED_IFORM_VPMULHUW_YMMqq_YMMqq_YMMqq	vpmulhuw ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMULHUW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpmulhuw ymm1{k1}, ymm2, [rdi]	11	0.5
XED_IFORM_VPMULHUW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpmulhuw ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMULHUW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpmulhuw zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VPMULHUW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpmulhuw zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_PMULHW_XMMdq_MEMdq	vpmulhw xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_PMULHW_XMMdq_XMMdq	vpmulhw xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMULHW_XMMdq_XMMdq_MEMdq	vpmulhw xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VPMULHW_XMMdq_XMMdq_XMMdq	vpmulhw xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMULHW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpmulhw xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VPMULHW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpmulhw xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMULHW_YMMqq_YMMqq_MEMqq	vpmulhw ymm1, ymm2, [rdi]	11	0.5
XED_IFORM_VPMULHW_YMMqq_YMMqq_YMMqq	vpmulhw ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMULHW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpmulhw ymm1{k1}, ymm2, [rdi]	11	0.5
XED_IFORM_VPMULHW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpmulhw ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMULHW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpmulhw zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VPMULHW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpmulhw zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_PMULLD_XMMdq_MEMdq	vpmulld xmm1, xmm1, [rdi]	14	0.66
XED_IFORM_PMULLD_XMMdq_XMMdq	vpmulld xmm1, xmm1, xmm2	8	0.66
XED_IFORM_VPMULLD_XMMdq_XMMdq_MEMdq	vpmulld xmm1, xmm2, [rdi]	14	0.66
XED_IFORM_VPMULLD_XMMdq_XMMdq_XMMdq	vpmulld xmm1, xmm2, xmm3	8	0.66
XED_IFORM_VPMULLD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpmulld xmm1{k1}, xmm2, [rdi]	14	0.66
XED_IFORM_VPMULLD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpmulld xmm1{k1}, xmm2, xmm3	8	0.66
XED_IFORM_VPMULLD_YMMqq_YMMqq_MEMqq	vpmulld ymm1, ymm2, [rdi]	8	0.66
XED_IFORM_VPMULLD_YMMqq_YMMqq_YMMqq	vpmulld ymm1, ymm2, ymm3	8	0.66
XED_IFORM_VPMULLD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpmulld ymm1{k1}, ymm2, [rdi]	8	0.66
XED_IFORM_VPMULLD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpmulld ymm1{k1}, ymm2, ymm3	8	0.66
XED_IFORM_VPMULLD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpmulld zmm1{k1}, zmm2, [rdi]	15	1
XED_IFORM_VPMULLD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpmulld zmm1{k1}, zmm2, zmm3	8	1
XED_IFORM_VPMULLQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpmullq xmm1{k1}, xmm2, [rdi]	18	1
XED_IFORM_VPMULLQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpmullq xmm1{k1}, xmm2, xmm3	12	1
XED_IFORM_VPMULLQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpmullq ymm1{k1}, ymm2, [rdi]	12	1
XED_IFORM_VPMULLQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpmullq ymm1{k1}, ymm2, ymm3	12	1
XED_IFORM_VPMULLQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpmullq zmm1{k1}, zmm2, [rdi]	19	1.5
XED_IFORM_VPMULLQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpmullq zmm1{k1}, zmm2, zmm3	12	1.5
XED_IFORM_PMULLW_XMMdq_MEMdq	vpmullw xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_PMULLW_XMMdq_XMMdq	vpmullw xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMULLW_XMMdq_XMMdq_MEMdq	vpmullw xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VPMULLW_XMMdq_XMMdq_XMMdq	vpmullw xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMULLW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpmullw xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VPMULLW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpmullw xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMULLW_YMMqq_YMMqq_MEMqq	vpmullw ymm1, ymm2, [rdi]	11	0.5
XED_IFORM_VPMULLW_YMMqq_YMMqq_YMMqq	vpmullw ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMULLW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpmullw ymm1{k1}, ymm2, [rdi]	11	0.5
XED_IFORM_VPMULLW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpmullw ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMULLW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpmullw zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VPMULLW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpmullw zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_PMULUDQ_XMMdq_MEMdq	vpmuludq xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_PMULUDQ_XMMdq_XMMdq	vpmuludq xmm1, xmm1, xmm2	5	0.5
XED_IFORM_VPMULUDQ_XMMdq_XMMdq_MEMdq	vpmuludq xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VPMULUDQ_XMMdq_XMMdq_XMMdq	vpmuludq xmm1, xmm2, xmm3	5	0.5
XED_IFORM_VPMULUDQ_XMMu64_MASKmskw_XMMu32_MEMu32_AVX512	vpmuludq xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VPMULUDQ_XMMu64_MASKmskw_XMMu32_XMMu32_AVX512	vpmuludq xmm1{k1}, xmm2, xmm3	5	0.5
XED_IFORM_VPMULUDQ_YMMqq_YMMqq_MEMqq	vpmuludq ymm1, ymm2, [rdi]	11	0.5
XED_IFORM_VPMULUDQ_YMMqq_YMMqq_YMMqq	vpmuludq ymm1, ymm2, ymm3	5	0.5
XED_IFORM_VPMULUDQ_YMMu64_MASKmskw_YMMu32_MEMu32_AVX512	vpmuludq ymm1{k1}, ymm2, [rdi]	11	0.5
XED_IFORM_VPMULUDQ_YMMu64_MASKmskw_YMMu32_YMMu32_AVX512	vpmuludq ymm1{k1}, ymm2, ymm3	5	0.5
XED_IFORM_VPMULUDQ_ZMMu64_MASKmskw_ZMMu32_MEMu32_AVX512	vpmuludq zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VPMULUDQ_ZMMu64_MASKmskw_ZMMu32_ZMMu32_AVX512	vpmuludq zmm1{k1}, zmm2, zmm3	5	0.5
XED_IFORM_POR_XMMdq_MEMdq	vpor xmm1, xmm1, [rdi]	7	0.5

XED_IFORM_POR_XMMdq_XMMdq	vpor xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPOR_XMMdq_XMMdq_MEMdq	vpor xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPOR_XMMdq_XMMdq_XMMdq	vpor xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPOR_YMMqq_YMMqq_MEMqq	vpor ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPOR_YMMqq_YMMqq_YMMqq	vpor ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPORD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpord xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPORD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpord xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPORD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpord ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPORD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpord ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPORD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpord zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPORD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpord zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPORQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vporq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPORQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vporq xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPORQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vporq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPORQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vporq ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPORQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vporq zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPORQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vporq zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPROLD_XMMu32_MASKmskw_MEMu32_IMM8_AVX512	vprold xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPROLD_XMMu32_MASKmskw_XMMu32_IMM8_AVX512	vprold xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPROLD_YMMu32_MASKmskw_MEMu32_IMM8_AVX512	vprold ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPROLD_YMMu32_MASKmskw_YMMu32_IMM8_AVX512	vprold ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPROLD_ZMMu32_MASKmskw_MEMu32_IMM8_AVX512	vprold zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPROLD_ZMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vprold zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPROLQ_XMMu64_MASKmskw_MEMu64_IMM8_AVX512	vprolq xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPROLQ_XMMu64_MASKmskw_XMMu64_IMM8_AVX512	vprolq xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPROLQ_YMMu64_MASKmskw_MEMu64_IMM8_AVX512	vprolq ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPROLQ_YMMu64_MASKmskw_YMMu64_IMM8_AVX512	vprolq ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPROLQ_ZMMu64_MASKmskw_MEMu64_IMM8_AVX512	vprolq zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPROLQ_ZMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vprolq zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPROLVD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vprolvd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPROLVD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vprolvd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPROLVD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vprolvd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPROLVD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vprolvd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPROLVD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vprolvd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPROLVD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vprolvd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPROLVQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vprolvq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPROLVQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vprolvq xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPROLVQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vprolvq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPROLVQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vprolvq ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPROLVQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vprolvq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPROLVQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vprolvq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPRORD_XMMu32_MASKmskw_MEMu32_IMM8_AVX512	vprord xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPRORD_XMMu32_MASKmskw_XMMu32_IMM8_AVX512	vprord xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPRORD_YMMu32_MASKmskw_MEMu32_IMM8_AVX512	vprord ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPRORD_YMMu32_MASKmskw_YMMu32_IMM8_AVX512	vprord ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPRORD_ZMMu32_MASKmskw_MEMu32_IMM8_AVX512	vprord zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPRORD_ZMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vprord zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPRORQ_XMMu64_MASKmskw_MEMu64_IMM8_AVX512	vprorq xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPRORQ_XMMu64_MASKmskw_XMMu64_IMM8_AVX512	vprorq xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPRORQ_YMMu64_MASKmskw_MEMu64_IMM8_AVX512	vprorq ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPRORQ_YMMu64_MASKmskw_YMMu64_IMM8_AVX512	vprorq ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPRORQ_ZMMu64_MASKmskw_MEMu64_IMM8_AVX512	vprorq zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPRORQ_ZMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vprorq zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPRORVD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vprorvd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPRORVD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vprorvd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPRORVD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vprorvd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPRORVD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vprorvd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPRORVD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vprorvd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPRORVD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vprorvd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPRORVQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vprorvq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPRORVQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vprorvq xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPRORVQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vprorvq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPRORVQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vprorvq ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPRORVQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vprorvq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPRORVQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vprorvq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSADBW_XMMdq_MEMdq	vpsadbw xmm1, xmm1, [rdi]	9	1
XED_IFORM_PSADBW_XMMdq_XMMdq	vpsadbw xmm1, xmm1, xmm2	3	1
XED_IFORM_VPSADBW_XMMdq_XMMdq_MEMdq	vpsadbw xmm1, xmm2, [rdi]	9	1
XED_IFORM_VPSADBW_XMMu16_XMMu8_MEMu8_AVX512	vpsadbw xmm1, xmm2, [rdi]	9	1
XED_IFORM_VPSADBW_XMMdq_XMMdq_XMMdq	vpsadbw xmm1, xmm2, xmm3	3	1
XED_IFORM_VPSADBW_XMMu16_XMMu8_XMMu8_AVX512	vpsadbw xmm1, xmm2, xmm3	3	1
XED_IFORM_VPSADBW_YMMqq_YMMqq_MEMqq	vpsadbw ymm1, ymm2, [rdi]	3	1
XED_IFORM_VPSADBW_YMMu16_YMMu8_MEMu8_AVX512	vpsadbw ymm1, ymm2, [rdi]	3	1
XED_IFORM_VPSADBW_YMMu16_YMMu8_YMMu8_AVX512	vpsadbw ymm1, ymm2, ymm3	3	1
XED_IFORM_VPSADBW_YMMqq_YMMqq_YMMqq	vpsadbw ymm1, ymm2, ymm3	3	1
XED_IFORM_VPSADBW_ZMMu16_ZMMu8_MEMu8_AVX512	vpsadbw zmm1, zmm2, [rdi]	10	1
XED_IFORM_VPSADBW_ZMMu16_ZMMu8_ZMMu8_AVX512	vpsadbw zmm1, zmm2, zmm3	3	1
XED_IFORM_VPSCATTERDD_MEMu32_MASKmskw_XMMu32_AVX512_VL128	vpscatterdd [rdi+xmm1*1]{k1}, xmm2	12	4
XED_IFORM_VPSCATTERDD_MEMu32_MASKmskw_YMMu32_AVX512_VL256	vpscatterdd [rdi+ymm1*1]{k1}, ymm2	12	8

XED_IFORM_VPSCATTERDD_MEMu32_MASKmskw_ZMMu32_AVX512_VL512	vpscatterdd [rdi+zmm1*1]{k1}, zmm2	12	16.75
XED_IFORM_VPSCATTERDQ_MEMu64_MASKmskw_XMMu64_AVX512_VL128	vpscatterdq [rdi+xmm1*1]{k1}, xmm2	11	2
XED_IFORM_VPSCATTERDQ_MEMu64_MASKmskw_YMMu64_AVX512_VL256	vpscatterdq [rdi+xmm1*1]{k1}, ymm2	11	4
XED_IFORM_VPSCATTERDQ_MEMu64_MASKmskw_ZMMu64_AVX512_VL512	vpscatterdq [rdi+ymm1*1]{k1}, zmm2	11	8
XED_IFORM_VPSCATTERQD_MEMu32_MASKmskw_XMMu32_AVX512_VL256	vpscatterqd [rdi+xmm1*1]{k1}, xmm2	12	4
XED_IFORM_VPSCATTERQD_MEMu32_MASKmskw_XMMu32_AVX512_VL128	vpscatterqd [rdi+xmm1*1]{k1}, xmm2	12	4
XED_IFORM_VPSCATTERQQ_MEMu64_MASKmskw_XMMu64_AVX512_VL128	vpscatterqq [rdi+xmm1*1]{k1}, xmm2	11	2
XED_IFORM_VPSCATTERQQ_MEMu64_MASKmskw_YMMu64_AVX512_VL256	vpscatterqq [rdi+ymm1*1]{k1}, ymm2	11	4
XED_IFORM_VPSCATTERQQ_MEMu64_MASKmskw_ZMMu64_AVX512_VL512	vpscatterqq [rdi+zmm1*1]{k1}, zmm2	11	8
XED_IFORM_PSHUFB_XMMdq_MEMdq	vpshufb xmm1, xmm1, [rdi]	7	1
XED_IFORM_PSHUFB_XMMdq_XMMdq	vpshufb xmm1, xmm1, xmm2	1	1
XED_IFORM_VPSHUFB_XMMdq_XMMdq_MEMdq	vpshufb xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPSHUFB_XMMdq_XMMdq_XMMdq	vpshufb xmm1, xmm2, xmm3	1	1
XED_IFORM_VPSHUFB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpshufb xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPSHUFB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpshufb xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPSHUFB_YMMqq_YMMqq_MEMqq	vpshufb ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPSHUFB_YMMqq_YMMqq_YMMqq	vpshufb ymm1, ymm2, ymm3	1	1
XED_IFORM_VPSHUFB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpshufb ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPSHUFB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpshufb ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPSHUFB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpshufb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSHUFB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpshufb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSHUFD_XMMdq_MEMdq_IMMb	vpshufd xmm1, [rdi], 1	7	1
XED_IFORM_PSHUFD_XMMdq_MEMdq_IMMb	vpshufd xmm1, [rdi], 1	7	1
XED_IFORM_VPSHUFD_XMMdq_XMMdq_IMMb	vpshufd xmm1, xmm2, 1	1	1
XED_IFORM_PSHUFD_XMMdq_XMMdq_IMMb	vpshufd xmm1, xmm2, 1	1	1
XED_IFORM_VPSHUFD_XMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpshufd xmm1{k1}, [rdi], 1	7	1
XED_IFORM_VPSHUFD_XMMu32_MASKmskw_XMMu32_IMM8_AVX512	vpshufd xmm1{k1}, xmm2, 1	1	1
XED_IFORM_VPSHUFD_YMMqq_MEMqq_IMMb	vpshufd ymm1, [rdi], 1	1	1
XED_IFORM_VPSHUFD_YMMqq_YMMqq_IMMb	vpshufd ymm1, ymm2, 1	1	1
XED_IFORM_VPSHUFD_YMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpshufd ymm1{k1}, [rdi], 1	1	1
XED_IFORM_VPSHUFD_YMMu32_MASKmskw_YMMu32_IMM8_AVX512	vpshufd ymm1{k1}, ymm2, 1	1	1
XED_IFORM_VPSHUFD_ZMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpshufd zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSHUFD_ZMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vpshufd zmm1{k1}, zmm2, 1	1	1
XED_IFORM_PSHUFHW_XMMdq_MEMdq_IMMb	vpshufhw xmm1, [rdi], 1	7	1
XED_IFORM_VPSHUFHW_XMMdq_MEMdq_IMMb	vpshufhw xmm1, [rdi], 1	7	1
XED_IFORM_PSHUFHW_XMMdq_XMMdq_IMMb	vpshufhw xmm1, xmm2, 1	1	1
XED_IFORM_VPSHUFHW_XMMdq_XMMdq_IMMb	vpshufhw xmm1, xmm2, 1	1	1
XED_IFORM_VPSHUFHW_XMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpshufhw xmm1{k1}, [rdi], 1	7	1
XED_IFORM_VPSHUFHW_XMMu16_MASKmskw_XMMu16_IMM8_AVX512	vpshufhw xmm1{k1}, xmm2, 1	1	1
XED_IFORM_VPSHUFHW_YMMqq_MEMqq_IMMb	vpshufhw ymm1, [rdi], 1	1	1
XED_IFORM_VPSHUFHW_YMMqq_YMMqq_IMMb	vpshufhw ymm1, ymm2, 1	1	1
XED_IFORM_VPSHUFHW_YMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpshufhw ymm1{k1}, [rdi], 1	1	1
XED_IFORM_VPSHUFHW_YMMu16_MASKmskw_YMMu16_IMM8_AVX512	vpshufhw ymm1{k1}, ymm2, 1	1	1
XED_IFORM_VPSHUFHW_ZMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpshufhw zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSHUFHW_ZMMu16_MASKmskw_ZMMu16_IMM8_AVX512	vpshufhw zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSHUFLW_XMMdq_MEMdq_IMMb	vpshuflw xmm1, [rdi], 1	7	1
XED_IFORM_PSHUFLW_XMMdq_MEMdq_IMMb	vpshuflw xmm1, [rdi], 1	7	1
XED_IFORM_PSHUFLW_XMMdq_XMMdq_IMMb	vpshuflw xmm1, xmm2, 1	1	1
XED_IFORM_VPSHUFLW_XMMdq_XMMdq_IMMb	vpshuflw xmm1, xmm2, 1	1	1
XED_IFORM_VPSHUFLW_XMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpshuflw xmm1{k1}, [rdi], 1	7	1
XED_IFORM_VPSHUFLW_XMMu16_MASKmskw_XMMu16_IMM8_AVX512	vpshuflw xmm1{k1}, xmm2, 1	1	1
XED_IFORM_VPSHUFLW_YMMqq_MEMqq_IMMb	vpshuflw ymm1, [rdi], 1	1	1
XED_IFORM_VPSHUFLW_YMMqq_YMMqq_IMMb	vpshuflw ymm1, ymm2, 1	1	1
XED_IFORM_VPSHUFLW_YMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpshuflw ymm1{k1}, [rdi], 1	1	1
XED_IFORM_VPSHUFLW_YMMu16_MASKmskw_YMMu16_IMM8_AVX512	vpshuflw ymm1{k1}, ymm2, 1	1	1
XED_IFORM_VPSHUFLW_ZMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpshuflw zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSHUFLW_ZMMu16_MASKmskw_ZMMu16_IMM8_AVX512	vpshuflw zmm1{k1}, zmm2, 1	1	1
XED_IFORM_PSIGNB_XMMdq_MEMdq	vpsignb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSIGNB_XMMdq_XMMdq	vpsignb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSIGNB_XMMdq_XMMdq_MEMdq	vpsignb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSIGNB_XMMdq_XMMdq_XMMdq	vpsignb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSIGNB_YMMqq_YMMqq_MEMqq	vpsignb ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSIGNB_YMMqq_YMMqq_YMMqq	vpsignb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_PSIGND_XMMdq_MEMdq	vpsignd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSIGND_XMMdq_XMMdq	vpsignd xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSIGND_XMMdq_XMMdq_MEMdq	vpsignd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSIGND_XMMdq_XMMdq_XMMdq	vpsignd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSIGND_YMMqq_YMMqq_MEMqq	vpsignd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSIGND_YMMqq_YMMqq_YMMqq	vpsignd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_PSIGNW_XMMdq_MEMdq	vpsignw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSIGNW_XMMdq_XMMdq	vpsignw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSIGNW_XMMdq_XMMdq_MEMdq	vpsignw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSIGNW_XMMdq_XMMdq_XMMdq	vpsignw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSIGNW_YMMqq_YMMqq_MEMqq	vpsignw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSIGNW_YMMqq_YMMqq_YMMqq	vpsignw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_PSLLD_XMMdq_MEMdq	vpslld xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSLLD_XMMdq_IMMb	vpslld xmm1, xmm1, 1	1	0.5
XED_IFORM_PSLLD_XMMdq_XMMdq	vpslld xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSLLD_XMMdq_XMMdq_MEMdq	vpslld xmm1, xmm2, [rdi]	7	0.5

XED_IFORM_VPSLLD_XMMdq_XMMdq_IMMb	vpslld xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSLLD_XMMdq_XMMdq_XMMdq	vpslld xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSLLD_XMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpslld xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSLLD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpslld xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLD_XMMu32_MASKmskw_XMMu32_IMM8_AVX512	vpslld xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSLLD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpslld xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSLLD_YMMqq_YMMqq_MEMdq	vpslld ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSLLD_YMMqq_YMMqq_IMMb	vpslld ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSLLD_YMMqq_YMMqq_XMMq	vpslld ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSLLD_YMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpslld ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPSLLD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpslld ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSLLD_YMMu32_MASKmskw_YMMu32_IMM8_AVX512	vpslld ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSLLD_YMMu32_MASKmskw_YMMu32_XMMu32_AVX512	vpslld ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSLLD_ZMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpslld zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSLLD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpslld zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSLLD_ZMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vpslld zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSLLD_ZMMu32_MASKmskw_ZMMu32_XMMu32_AVX512	vpslld zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_VPSLLDQ_XMMu8_MEMu8_IMM8_AVX512	vpslldq xmm1, [rdi], 1	7	1
XED_IFORM_PSLLDQ_XMMdq_IMMb	vpslldq xmm1, xmm1, 1	1	1
XED_IFORM_VPSLLDQ_XMMu8_XMMu8_IMM8_AVX512	vpslldq xmm1, xmm2, 1	1	1
XED_IFORM_VPSLLDQ_XMMdq_XMMdq_IMMb	vpslldq xmm1, xmm2, 1	1	1
XED_IFORM_VPSLLDQ_YMMu8_MEMu8_IMM8_AVX512	vpslldq ymm1, [rdi], 1	1	1
XED_IFORM_VPSLLDQ_YMMqq_YMMqq_IMMb	vpslldq ymm1, ymm2, 1	1	1
XED_IFORM_VPSLLDQ_YMMu8_YMMu8_IMM8_AVX512	vpslldq ymm1, ymm2, 1	1	1
XED_IFORM_VPSLLDQ_ZMMu8_MEMu8_IMM8_AVX512	vpslldq zmm1, [rdi], 1	8	1
XED_IFORM_VPSLLDQ_ZMMu8_ZMMu8_IMM8_AVX512	vpslldq zmm1, zmm2, 1	1	1
XED_IFORM_PSLLQ_XMMdq_MEMdq	vpsllq xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSLLQ_XMMdq_IMMb	vpsllq xmm1, xmm1, 1	1	0.5
XED_IFORM_PSLLQ_XMMdq_XMMdq	vpsllq xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSLLQ_XMMdq_XMMdq_MEMdq	vpsllq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLQ_XMMdq_XMMdq_IMMb	vpsllq xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSLLQ_XMMdq_XMMdq_XMMdq	vpsllq xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSLLQ_XMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsllq xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSLLQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsllq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLQ_XMMu64_MASKmskw_XMMu64_IMM8_AVX512	vpsllq xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSLLQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsllq xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSLLQ_YMMqq_YMMqq_MEMdq	vpsllq ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSLLQ_YMMqq_YMMqq_IMMb	vpsllq ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSLLQ_YMMqq_YMMqq_XMMq	vpsllq ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSLLQ_YMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsllq ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPSLLQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsllq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSLLQ_YMMu64_MASKmskw_YMMu64_IMM8_AVX512	vpsllq ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSLLQ_YMMu64_MASKmskw_YMMu64_XMMu64_AVX512	vpsllq ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSLLQ_ZMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsllq zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSLLQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsllq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSLLQ_ZMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vpsllq zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSLLQ_ZMMu64_MASKmskw_ZMMu64_XMMu64_AVX512	vpsllq zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_VPSLLVD_XMMdq_XMMdq_MEMdq	vpsllvd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLVD_XMMdq_XMMdq_XMMdq	vpsllvd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSLLVD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpsllvd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLVD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpsllvd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSLLVD_YMMqq_YMMqq_MEMqq	vpsllvd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSLLVD_YMMqq_YMMqq_YMMqq	vpsllvd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSLLVD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpsllvd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSLLVD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpsllvd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSLLVD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpsllvd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSLLVD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpsllvd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSLLVQ_XMMdq_XMMdq_MEMdq	vpsllvq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLVQ_XMMdq_XMMdq_XMMdq	vpsllvq xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSLLVQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsllvq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLVQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsllvq xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSLLVQ_YMMqq_YMMqq_MEMqq	vpsllvq ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSLLVQ_YMMqq_YMMqq_YMMqq	vpsllvq ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSLLVQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsllvq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSLLVQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpsllvq ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSLLVQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsllvq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSLLVQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpsllvq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSLLVW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsllvw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLVW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsllvw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSLLVW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsllvw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSLLVW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpsllvw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSLLVW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsllvw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSLLVW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpsllvw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSLLW_XMMdq_MEMdq	vpsllw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSLLW_XMMdq_IMMb	vpsllw xmm1, xmm1, 1	1	0.5
XED_IFORM_PSLLW_XMMdq_XMMdq	vpsllw xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSLLW_XMMdq_XMMdq_MEMdq	vpsllw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLW_XMMdq_XMMdq_IMMb	vpsllw xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSLLW_XMMdq_XMMdq_XMMdq	vpsllw xmm1, xmm2, xmm3	2	1

XED_IFORM_VPSLLW_XMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsllw xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSLLW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsllw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSLLW_XMMu16_MASKmskw_XMMu16_IMM8_AVX512	vpsllw xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSLLW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsllw xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSLLW_YMMqq_YMMqq_MEMdq	vpsllw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSLLW_YMMqq_YMMqq_IMMb	vpsllw ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSLLW_YMMqq_YMMqq_XMMq	vpsllw ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSLLW_YMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsllw ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPSLLW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsllw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSLLW_YMMu16_MASKmskw_YMMu16_IMM8_AVX512	vpsllw ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSLLW_YMMu16_MASKmskw_YMMu16_XMMu16_AVX512	vpsllw ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSLLW_ZMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsllw zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSLLW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsllw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSLLW_ZMMu16_MASKmskw_ZMMu16_IMM8_AVX512	vpsllw zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSLLW_ZMMu16_MASKmskw_ZMMu16_XMMu16_AVX512	vpsllw zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_PSRAD_XMMdq_MEMdq	vpsrad xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSRAD_XMMdq_IMMb	vpsrad xmm1, xmm1, 1	1	0.5
XED_IFORM_PSRAD_XMMdq_XMMdq	vpsrad xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSRAD_XMMdq_XMMdq_MEMdq	vpsrad xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAD_XMMdq_XMMdq_IMMb	vpsrad xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSRAD_XMMdq_XMMdq_XMMdq	vpsrad xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSRAD_XMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpsrad xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSRAD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpsrad xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAD_XMMu32_MASKmskw_XMMu32_IMM8_AVX512	vpsrad xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSRAD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpsrad xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSRAD_YMMqq_YMMqq_MEMdq	vpsrad ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRAD_YMMqq_YMMqq_IMMb	vpsrad ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSRAD_YMMqq_YMMqq_XMMq	vpsrad ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSRAD_YMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpsrad ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPSRAD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpsrad ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRAD_YMMu32_MASKmskw_YMMu32_IMM8_AVX512	vpsrad ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSRAD_YMMu32_MASKmskw_YMMu32_XMMu32_AVX512	vpsrad ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSRAD_ZMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpsrad zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSRAD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpsrad zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRAD_ZMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vpsrad zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSRAD_ZMMu32_MASKmskw_ZMMu32_XMMu32_AVX512	vpsrad zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_VPSRAQ_XMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsraq xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSRAQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsraq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAQ_XMMu64_MASKmskw_XMMu64_IMM8_AVX512	vpsraq xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSRAQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsraq xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSRAQ_YMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsraq ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPSRAQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsraq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRAQ_YMMu64_MASKmskw_YMMu64_IMM8_AVX512	vpsraq ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSRAQ_YMMu64_MASKmskw_YMMu64_XMMu64_AVX512	vpsraq ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSRAQ_ZMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsraq zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSRAQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsraq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRAQ_ZMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vpsraq zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSRAQ_ZMMu64_MASKmskw_ZMMu64_XMMu64_AVX512	vpsraq zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_VPSRAVD_XMMdq_XMMdq_MEMdq	vpsravd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAVD_XMMdq_XMMdq_XMMdq	vpsravd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSRAVD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpsravd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAVD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpsravd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSRAVD_YMMqq_YMMqq_MEMqq	vpsravd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRAVD_YMMqq_YMMqq_YMMqq	vpsravd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSRAVD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpsravd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRAVD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpsravd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSRAVD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpsravd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRAVD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpsravd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSRAVQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsravq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAVQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsravq xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSRAVQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsravq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRAVQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpsravq ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSRAVQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsravq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRAVQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpsravq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSRAVW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsravw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAVW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsravw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSRAVW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsravw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRAVW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpsravw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSRAVW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsravw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRAVW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpsravw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSRAW_XMMdq_MEMdq	vpsraw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSRAW_XMMdq_IMMb	vpsraw xmm1, xmm1, 1	1	0.5
XED_IFORM_PSRAW_XMMdq_XMMdq	vpsraw xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSRAW_XMMdq_XMMdq_MEMdq	vpsraw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAW_XMMdq_XMMdq_IMMb	vpsraw xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSRAW_XMMdq_XMMdq_XMMdq	vpsraw xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSRAW_XMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsraw xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSRAW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsraw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRAW_XMMu16_MASKmskw_XMMu16_IMM8_AVX512	vpsraw xmm1{k1}, xmm2, 1	1	0.5

XED_IFORM_VPSRAW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsraw xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSRAW_YMMqq_YMMqq_MEMdq	vpsraw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRAW_YMMqq_YMMqq_IMMb	vpsraw ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSRAW_YMMqq_YMMqq_XMMq	vpsraw ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSRAW_YMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsraw ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPSRAW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsraw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRAW_YMMu16_MASKmskw_YMMu16_IMM8_AVX512	vpsraw ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSRAW_YMMu16_MASKmskw_YMMu16_XMMu16_AVX512	vpsraw ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSRAW_ZMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsraw zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSRAW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsraw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRAW_ZMMu16_MASKmskw_ZMMu16_IMM8_AVX512	vpsraw zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSRAW_ZMMu16_MASKmskw_ZMMu16_XMMu16_AVX512	vpsraw zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_PSRLD_XMMdq_MEMdq	vpsrld xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSRLD_XMMdq_IMMb	vpsrld xmm1, xmm1, 1	1	0.5
XED_IFORM_PSRLD_XMMdq_XMMdq	vpsrld xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSRLD_XMMdq_XMMdq_MEMdq	vpsrld xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLD_XMMdq_XMMdq_IMMb	vpsrld xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSRLD_XMMdq_XMMdq_XMMdq	vpsrld xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSRLD_XMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpsrld xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSRLD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpsrld xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLD_XMMu32_MASKmskw_XMMu32_IMM8_AVX512	vpsrld xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSRLD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpsrld xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSRLD_YMMqq_YMMqq_MEMdq	vpsrld ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRLD_YMMqq_YMMqq_IMMb	vpsrld ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSRLD_YMMqq_YMMqq_XMMq	vpsrld ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSRLD_YMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpsrld ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPSRLD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpsrld ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRLD_YMMu32_MASKmskw_YMMu32_IMM8_AVX512	vpsrld ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSRLD_YMMu32_MASKmskw_YMMu32_XMMu32_AVX512	vpsrld ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSRLD_ZMMu32_MASKmskw_MEMu32_IMM8_AVX512	vpsrld zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSRLD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpsrld zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRLD_ZMMu32_MASKmskw_ZMMu32_IMM8_AVX512	vpsrld zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSRLD_ZMMu32_MASKmskw_ZMMu32_XMMu32_AVX512	vpsrld zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_VPSRLDQ_XMMu8_MEMu8_IMM8_AVX512	vpsrldq xmm1, [rdi], 1	7	1
XED_IFORM_PSRLDQ_XMMdq_IMMb	vpsrldq xmm1, xmm1, 1	1	1
XED_IFORM_VPSRLDQ_XMMdq_XMMdq_IMMb	vpsrldq xmm1, xmm2, 1	1	1
XED_IFORM_VPSRLDQ_XMMu8_XMMu8_IMM8_AVX512	vpsrldq xmm1, xmm2, 1	1	1
XED_IFORM_VPSRLDQ_YMMu8_MEMu8_IMM8_AVX512	vpsrldq ymm1, [rdi], 1	1	1
XED_IFORM_VPSRLDQ_YMMqq_YMMqq_IMMb	vpsrldq ymm1, ymm2, 1	1	1
XED_IFORM_VPSRLDQ_YMMu8_YMMu8_IMM8_AVX512	vpsrldq ymm1, ymm2, 1	1	1
XED_IFORM_VPSRLDQ_ZMMu8_MEMu8_IMM8_AVX512	vpsrldq zmm1, [rdi], 1	8	1
XED_IFORM_VPSRLDQ_ZMMu8_ZMMu8_IMM8_AVX512	vpsrldq zmm1, zmm2, 1	1	1
XED_IFORM_PSRLQ_XMMdq_MEMdq	vpsrlq xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSRLQ_XMMdq_IMMb	vpsrlq xmm1, xmm1, 1	1	0.5
XED_IFORM_PSRLQ_XMMdq_XMMdq	vpsrlq xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSRLQ_XMMdq_XMMdq_MEMdq	vpsrlq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLQ_XMMdq_XMMdq_IMMb	vpsrlq xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSRLQ_XMMdq_XMMdq_XMMdq	vpsrlq xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSRLQ_XMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsrlq xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSRLQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsrlq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLQ_XMMu64_MASKmskw_XMMu64_IMM8_AVX512	vpsrlq xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSRLQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsrlq xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSRLQ_YMMqq_YMMqq_MEMdq	vpsrlq ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRLQ_YMMqq_YMMqq_IMMb	vpsrlq ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSRLQ_YMMqq_YMMqq_XMMq	vpsrlq ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSRLQ_YMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsrlq ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPSRLQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsrlq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRLQ_YMMu64_MASKmskw_YMMu64_IMM8_AVX512	vpsrlq ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSRLQ_YMMu64_MASKmskw_YMMu64_XMMu64_AVX512	vpsrlq ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSRLQ_ZMMu64_MASKmskw_MEMu64_IMM8_AVX512	vpsrlq zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSRLQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsrlq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRLQ_ZMMu64_MASKmskw_ZMMu64_IMM8_AVX512	vpsrlq zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSRLQ_ZMMu64_MASKmskw_ZMMu64_XMMu64_AVX512	vpsrlq zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_VPSRLVD_XMMdq_XMMdq_MEMdq	vpsrlvd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLVD_XMMdq_XMMdq_XMMdq	vpsrlvd xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSRLVD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpsrlvd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLVD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpsrlvd xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSRLVD_YMMqq_YMMqq_MEMqq	vpsrlvd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRLVD_YMMqq_YMMqq_YMMqq	vpsrlvd ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSRLVD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpsrlvd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRLVD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpsrlvd ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSRLVD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpsrlvd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRLVD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpsrlvd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSRLVQ_XMMdq_XMMdq_MEMdq	vpsrlvq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLVQ_XMMdq_XMMdq_XMMdq	vpsrlvq xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSRLVQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsrlvq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLVQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsrlvq xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSRLVQ_YMMqq_YMMqq_MEMqq	vpsrlvq ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRLVQ_YMMqq_YMMqq_YMMqq	vpsrlvq ymm1, ymm2, ymm3	1	0.5

XED_IFORM_VPSRLVQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsrlvq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRLVQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpsrlvq ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSRLVQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsrlvq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRLVQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpsrlvq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_VPSRLVW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsrlvw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLVW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsrlvw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSRLVW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsrlvw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRLVW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpsrlvw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSRLVW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsrlvw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRLVW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpsrlvw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSRLW_XMMdq_MEMdq	vpsrlw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSRLW_XMMdq_IMMb	vpsrlw xmm1, xmm1, 1	1	0.5
XED_IFORM_PSRLW_XMMdq_XMMdq	vpsrlw xmm1, xmm1, xmm2	2	1
XED_IFORM_VPSRLW_XMMdq_XMMdq_MEMdq	vpsrlw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLW_XMMdq_XMMdq_IMMb	vpsrlw xmm1, xmm2, 1	1	0.5
XED_IFORM_VPSRLW_XMMdq_XMMdq_XMMdq	vpsrlw xmm1, xmm2, xmm3	2	1
XED_IFORM_VPSRLW_XMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsrlw xmm1{k1}, [rdi], 1	7	0.5
XED_IFORM_VPSRLW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsrlw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSRLW_XMMu16_MASKmskw_XMMu16_IMM8_AVX512	vpsrlw xmm1{k1}, xmm2, 1	1	0.5
XED_IFORM_VPSRLW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsrlw xmm1{k1}, xmm2, xmm3	2	1
XED_IFORM_VPSRLW_YMMqq_YMMqq_MEMdq	vpsrlw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRLW_YMMqq_YMMqq_IMMb	vpsrlw ymm1, ymm2, 1	1	0.5
XED_IFORM_VPSRLW_YMMqq_YMMqq_XMMq	vpsrlw ymm1, ymm2, xmm3	4	1
XED_IFORM_VPSRLW_YMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsrlw ymm1{k1}, [rdi], 1	1	0.5
XED_IFORM_VPSRLW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsrlw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSRLW_YMMu16_MASKmskw_YMMu16_IMM8_AVX512	vpsrlw ymm1{k1}, ymm2, 1	1	0.5
XED_IFORM_VPSRLW_YMMu16_MASKmskw_YMMu16_XMMu16_AVX512	vpsrlw ymm1{k1}, ymm2, xmm3	4	1
XED_IFORM_VPSRLW_ZMMu16_MASKmskw_MEMu16_IMM8_AVX512	vpsrlw zmm1{k1}, [rdi], 1	8	1
XED_IFORM_VPSRLW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsrlw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSRLW_ZMMu16_MASKmskw_ZMMu16_IMM8_AVX512	vpsrlw zmm1{k1}, zmm2, 1	1	1
XED_IFORM_VPSRLW_ZMMu16_MASKmskw_ZMMu16_XMMu16_AVX512	vpsrlw zmm1{k1}, zmm2, xmm3	4	1
XED_IFORM_PSUBB_XMMdq_MEMdq	vpsubb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBB_XMMdq_XMMdq	vpsubb xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPSUBB_XMMdq_XMMdq_MEMdq	vpsubb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBB_XMMdq_XMMdq_XMMdq	vpsubb xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpsubb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpsubb xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBB_YMMqq_YMMqq_MEMqq	vpsubb ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBB_YMMqq_YMMqq_YMMqq	vpsubb ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpsubb ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpsubb ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpsubb zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPSUBB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpsubb zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PSUBD_XMMdq_MEMdq	vpsubd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBD_XMMdq_XMMdq	vpsubd xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPSUBD_XMMdq_XMMdq_MEMdq	vpsubd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBD_XMMdq_XMMdq_XMMdq	vpsubd xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpsubd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpsubd xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBD_YMMqq_YMMqq_MEMqq	vpsubd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBD_YMMqq_YMMqq_YMMqq	vpsubd ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpsubd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpsubd ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpsubd zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPSUBD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpsubd zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PSUBQ_XMMdq_MEMdq	vpsubq xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBQ_XMMdq_XMMdq	vpsubq xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPSUBQ_XMMdq_XMMdq_MEMdq	vpsubq xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBQ_XMMdq_XMMdq_XMMdq	vpsubq xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpsubq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpsubq xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBQ_YMMqq_YMMqq_MEMqq	vpsubq ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBQ_YMMqq_YMMqq_YMMqq	vpsubq ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpsubq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpsubq ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpsubq zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPSUBQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpsubq zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_PSUBSB_XMMdq_MEMdq	vpsubsb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBSB_XMMdq_XMMdq	vpsubsb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSUBSB_XMMdq_XMMdq_MEMdq	vpsubsb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBSB_XMMdq_XMMdq_XMMdq	vpsubsb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBSB_XMMi8_MASKmskw_XMMi8_MEMi8_AVX512	vpsubsb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBSB_XMMi8_MASKmskw_XMMi8_XMMi8_AVX512	vpsubsb xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBSB_YMMqq_YMMqq_MEMqq	vpsubsb ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBSB_YMMqq_YMMqq_YMMqq	vpsubsb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBSB_YMMi8_MASKmskw_YMMi8_MEMi8_AVX512	vpsubsb ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBSB_YMMi8_MASKmskw_YMMi8_YMMi8_AVX512	vpsubsb ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBSB_ZMMi8_MASKmskw_ZMMi8_MEMi8_AVX512	vpsubsb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSUBSB_ZMMi8_MASKmskw_ZMMi8_ZMMi8_AVX512	vpsubsb zmm1{k1}, zmm2, zmm3	1	1

XED_IFORM_PSUBSW_XMMdq_MEMdq	vpsubsw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBSW_XMMdq_XMMdq	vpsubsw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSUBSW_XMMdq_XMMdq_MEMdq	vpsubsw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBSW_XMMdq_XMMdq_XMMdq	vpsubsw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBSW_XMMi16_MASKmskw_XMMi16_MEMi16_AVX512	vpsubsw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBSW_XMMi16_MASKmskw_XMMi16_XMMi16_AVX512	vpsubsw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBSW_YMMqq_YMMqq_MEMqq	vpsubsw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBSW_YMMqq_YMMqq_YMMqq	vpsubsw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBSW_YMMi16_MASKmskw_YMMi16_MEMi16_AVX512	vpsubsw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBSW_YMMi16_MASKmskw_YMMi16_YMMi16_AVX512	vpsubsw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBSW_ZMMi16_MASKmskw_ZMMi16_MEMi16_AVX512	vpsubsw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSUBSW_ZMMi16_MASKmskw_ZMMi16_ZMMi16_AVX512	vpsubsw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSUBUSB_XMMdq_MEMdq	vpsubusb xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBUSB_XMMdq_XMMdq	vpsubusb xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSUBUSB_XMMdq_XMMdq_MEMdq	vpsubusb xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBUSB_XMMdq_XMMdq_XMMdq	vpsubusb xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBUSB_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpsubusb xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBUSB_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpsubusb xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBUSB_YMMqq_YMMqq_MEMqq	vpsubusb ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBUSB_YMMqq_YMMqq_YMMqq	vpsubusb ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBUSB_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpsubusb ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBUSB_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpsubusb ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBUSB_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpsubusb zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSUBUSB_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpsubusb zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSUBUSW_XMMdq_MEMdq	vpsubusw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBUSW_XMMdq_XMMdq	vpsubusw xmm1, xmm1, xmm2	1	0.5
XED_IFORM_VPSUBUSW_XMMdq_XMMdq_MEMdq	vpsubusw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBUSW_XMMdq_XMMdq_XMMdq	vpsubusw xmm1, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBUSW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsubusw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBUSW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsubusw xmm1{k1}, xmm2, xmm3	1	0.5
XED_IFORM_VPSUBUSW_YMMqq_YMMqq_MEMqq	vpsubusw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBUSW_YMMqq_YMMqq_YMMqq	vpsubusw ymm1, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBUSW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsubusw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBUSW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpsubusw ymm1{k1}, ymm2, ymm3	1	0.5
XED_IFORM_VPSUBUSW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsubusw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPSUBUSW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpsubusw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PSUBW_XMMdq_MEMdq	vpsubw xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PSUBW_XMMdq_XMMdq	vpsubw xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPSUBW_XMMdq_XMMdq_MEMdq	vpsubw xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBW_XMMdq_XMMdq_XMMdq	vpsubw xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBW_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpsubw xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPSUBW_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpsubw xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPSUBW_YMMqq_YMMqq_MEMqq	vpsubw ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBW_YMMqq_YMMqq_YMMqq	vpsubw ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBW_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpsubw ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPSUBW_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpsubw ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPSUBW_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpsubw zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPSUBW_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpsubw zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPTERNLOGD_XMMu32_MASKmskw_XMMu32_MEMu32_IMM8_AVX512	vpternlogd xmm1{k1}, xmm2, [rdi], 1	7	0.5
XED_IFORM_VPTERNLOGD_XMMu32_MASKmskw_XMMu32_XMMu32_IMM8_AVX512	vpternlogd xmm1{k1}, xmm2, xmm3, 1	1	0.33
XED_IFORM_VPTERNLOGD_YMMu32_MASKmskw_YMMu32_MEMu32_IMM8_AVX512	vpternlogd ymm1{k1}, ymm2, [rdi], 1	1	0.5
XED_IFORM_VPTERNLOGD_YMMu32_MASKmskw_YMMu32_YMMu32_IMM8_AVX512	vpternlogd ymm1{k1}, ymm2, ymm3, 1	1	0.33
XED_IFORM_VPTERNLOGD_ZMMu32_MASKmskw_ZMMu32_MEMu32_IMM8_AVX512	vpternlogd zmm1{k1}, zmm2, [rdi], 1	8	0.5
XED_IFORM_VPTERNLOGD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_IMM8_AVX512	vpternlogd zmm1{k1}, zmm2, zmm3, 1	1	0.5
XED_IFORM_VPTERNLOGQ_XMMu64_MASKmskw_XMMu64_MEMu64_IMM8_AVX512	vpternlogq xmm1{k1}, xmm2, [rdi], 1	7	0.5
XED_IFORM_VPTERNLOGQ_XMMu64_MASKmskw_XMMu64_XMMu64_IMM8_AVX512	vpternlogq xmm1{k1}, xmm2, xmm3, 1	1	0.33
XED_IFORM_VPTERNLOGQ_YMMu64_MASKmskw_YMMu64_MEMu64_IMM8_AVX512	vpternlogq ymm1{k1}, ymm2, [rdi], 1	1	0.5
XED_IFORM_VPTERNLOGQ_YMMu64_MASKmskw_YMMu64_YMMu64_IMM8_AVX512	vpternlogq ymm1{k1}, ymm2, ymm3, 1	1	0.33
XED_IFORM_VPTERNLOGQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_IMM8_AVX512	vpternlogq zmm1{k1}, zmm2, [rdi], 1	8	0.5
XED_IFORM_VPTERNLOGQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_IMM8_AVX512	vpternlogq zmm1{k1}, zmm2, zmm3, 1	1	0.5
XED_IFORM_PTEST_XMMdq_MEMdq	vptest xmm1, [rdi]	9	1
XED_IFORM_VPTEST_XMMdq_MEMdq	vptest xmm1, [rdi]	9	1
XED_IFORM_PTEST_XMMdq_XMMdq	vptest xmm1, xmm2	3	1
XED_IFORM_VPTEST_XMMdq_XMMdq	vptest xmm1, xmm2	3	1
XED_IFORM_VPTEST_YMMqq_MEMqq	vptest ymm1, [rdi]	3	1
XED_IFORM_VPTEST_YMMqq_YMMqq	vptest ymm1, ymm2	3	1
XED_IFORM_VPTESTMB_MASKmskw_MASKmskw_XMMu8_MEMu8_AVX512	vptestmb k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTMB_MASKmskw_MASKmskw_XMMu8_XMMu8_AVX512	vptestmb k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTMB_MASKmskw_MASKmskw_YMMu8_MEMu8_AVX512	vptestmb k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPTESTMB_MASKmskw_MASKmskw_YMMu8_YMMu8_AVX512	vptestmb k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTMB_MASKmskw_MASKmskw_ZMMu8_MEMu8_AVX512	vptestmb k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTMB_MASKmskw_MASKmskw_ZMMu8_ZMMu8_AVX512	vptestmb k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTMD_MASKmskw_MASKmskw_XMMu32_MEMu32_AVX512	vptestmd k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTMD_MASKmskw_MASKmskw_XMMu32_XMMu32_AVX512	vptestmd k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTMD_MASKmskw_MASKmskw_YMMu32_MEMu32_AVX512	vptestmd k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPTESTMD_MASKmskw_MASKmskw_YMMu32_YMMu32_AVX512	vptestmd k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTMD_MASKmskw_MASKmskw_ZMMu32_MEMu32_AVX512	vptestmd k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTMD_MASKmskw_MASKmskw_ZMMu32_ZMMu32_AVX512	vptestmd k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTMQ_MASKmskw_MASKmskw_XMMu64_MEMu64_AVX512	vptestmq k1{k1}, xmm1, [rdi]	9	1

XED_IFORM_VPTESTMQ_MASKmskw_MASKmskw_XMMu64_XMMu64_AVX512	vptestmq k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTMQ_MASKmskw_MASKmskw_YMMu64_MEMu64_AVX512	vptestmq k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPTESTMQ_MASKmskw_MASKmskw_YMMu64_YMMu64_AVX512	vptestmq k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTMQ_MASKmskw_MASKmskw_ZMMu64_MEMu64_AVX512	vptestmq k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTMQ_MASKmskw_MASKmskw_ZMMu64_ZMMu64_AVX512	vptestmq k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTMW_MASKmskw_MASKmskw_XMMu16_MEMu16_AVX512	vptestmw k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTMW_MASKmskw_MASKmskw_XMMu16_XMMu16_AVX512	vptestmw k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTMW_MASKmskw_MASKmskw_YMMu16_MEMu16_AVX512	vptestmw k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPTESTMW_MASKmskw_MASKmskw_YMMu16_YMMu16_AVX512	vptestmw k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTMW_MASKmskw_MASKmskw_ZMMu16_MEMu16_AVX512	vptestmw k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTMW_MASKmskw_MASKmskw_ZMMu16_ZMMu16_AVX512	vptestmw k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTNMB_MASKmskw_MASKmskw_XMMu8_MEMu8_AVX512	vptestnmb k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTNMB_MASKmskw_MASKmskw_XMMu8_XMMu8_AVX512	vptestnmb k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTNMB_MASKmskw_MASKmskw_YMMu8_MEMu8_AVX512	vptestnmb k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPTESTNMB_MASKmskw_MASKmskw_YMMu8_YMMu8_AVX512	vptestnmb k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTNMB_MASKmskw_MASKmskw_ZMMu8_MEMu8_AVX512	vptestnmb k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTNMB_MASKmskw_MASKmskw_ZMMu8_ZMMu8_AVX512	vptestnmb k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTNMD_MASKmskw_MASKmskw_XMMu32_MEMu32_AVX512	vptestnmd k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTNMD_MASKmskw_MASKmskw_XMMu32_XMMu32_AVX512	vptestnmd k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTNMD_MASKmskw_MASKmskw_YMMu32_MEMu32_AVX512	vptestnmd k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPTESTNMD_MASKmskw_MASKmskw_YMMu32_YMMu32_AVX512	vptestnmd k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTNMD_MASKmskw_MASKmskw_ZMMu32_MEMu32_AVX512	vptestnmd k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTNMD_MASKmskw_MASKmskw_ZMMu32_ZMMu32_AVX512	vptestnmd k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTNMQ_MASKmskw_MASKmskw_XMMu64_MEMu64_AVX512	vptestnmq k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTNMQ_MASKmskw_MASKmskw_XMMu64_XMMu64_AVX512	vptestnmq k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTNMQ_MASKmskw_MASKmskw_YMMu64_MEMu64_AVX512	vptestnmq k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPTESTNMQ_MASKmskw_MASKmskw_YMMu64_YMMu64_AVX512	vptestnmq k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTNMQ_MASKmskw_MASKmskw_ZMMu64_MEMu64_AVX512	vptestnmq k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTNMQ_MASKmskw_MASKmskw_ZMMu64_ZMMu64_AVX512	vptestnmq k1{k1}, zmm1, zmm2	3	1
XED_IFORM_VPTESTNMW_MASKmskw_MASKmskw_XMMu16_MEMu16_AVX512	vptestnmw k1{k1}, xmm1, [rdi]	9	1
XED_IFORM_VPTESTNMW_MASKmskw_MASKmskw_XMMu16_XMMu16_AVX512	vptestnmw k1{k1}, xmm1, xmm2	3	1
XED_IFORM_VPTESTNMW_MASKmskw_MASKmskw_YMMu16_MEMu16_AVX512	vptestnmw k1{k1}, ymm1, [rdi]	3	1
XED_IFORM_VPTESTNMW_MASKmskw_MASKmskw_YMMu16_YMMu16_AVX512	vptestnmw k1{k1}, ymm1, ymm2	3	1
XED_IFORM_VPTESTNMW_MASKmskw_MASKmskw_ZMMu16_MEMu16_AVX512	vptestnmw k1{k1}, zmm1, [rdi]	10	1
XED_IFORM_VPTESTNMW_MASKmskw_MASKmskw_ZMMu16_ZMMu16_AVX512	vptestnmw k1{k1}, zmm1, zmm2	3	1
XED_IFORM_PUNPCKHBW_XMMdq_MEMdq	vpunpckhbw xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKHBW_XMMdq_XMMq	vpunpckhbw xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKHBW_XMMdq_XMMdq_MEMdq	vpunpckhbw xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHBW_XMMdq_XMMdq_XMMdq	vpunpckhbw xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHBW_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpunpckhbw xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHBW_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpunpckhbw xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHBW_YMMqq_YMMqq_MEMqq	vpunpckhbw ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKHBW_YMMqq_YMMqq_YMMqq	vpunpckhbw ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHBW_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpunpckhbw ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKHBW_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpunpckhbw ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHBW_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpunpckhbw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKHBW_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpunpckhbw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKHDQ_XMMdq_MEMdq	vpunpckhdq xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKHDQ_XMMdq_XMMq	vpunpckhdq xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKHDQ_XMMdq_XMMdq_MEMdq	vpunpckhdq xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHDQ_XMMdq_XMMdq_XMMdq	vpunpckhdq xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHDQ_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpunpckhdq xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHDQ_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpunpckhdq xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHDQ_YMMqq_YMMqq_MEMqq	vpunpckhdq ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKHDQ_YMMqq_YMMqq_YMMqq	vpunpckhdq ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHDQ_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpunpckhdq ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKHDQ_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpunpckhdq ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHDQ_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpunpckhdq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKHDQ_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpunpckhdq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKHQDQ_XMMdq_MEMdq	vpunpckhqdq xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKHQDQ_XMMdq_XMMq	vpunpckhqdq xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKHQDQ_XMMdq_XMMdq_MEMdq	vpunpckhqdq xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHQDQ_XMMdq_XMMdq_XMMdq	vpunpckhqdq xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHQDQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpunpckhqdq xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHQDQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpunpckhqdq xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHQDQ_YMMqq_YMMqq_MEMqq	vpunpckhqdq ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKHQDQ_YMMqq_YMMqq_YMMqq	vpunpckhqdq ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHQDQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpunpckhqdq ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKHQDQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpunpckhqdq ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHQDQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpunpckhqdq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKHQDQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpunpckhqdq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKHWD_XMMdq_MEMdq	vpunpckhwd xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKHWD_XMMdq_XMMq	vpunpckhwd xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKHWD_XMMdq_XMMdq_MEMdq	vpunpckhwd xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHWD_XMMdq_XMMdq_XMMdq	vpunpckhwd xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHWD_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpunpckhwd xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKHWD_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpunpckhwd xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKHWD_YMMqq_YMMqq_MEMqq	vpunpckhwd ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKHWD_YMMqq_YMMqq_YMMqq	vpunpckhwd ymm1, ymm2, ymm3	1	1

XED_IFORM_VPUNPCKHWD_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpunpckhwd ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKHWD_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpunpckhwd ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKHWD_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpunpckhwd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKHWD_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpunpckhwd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKLBW_XMMdq_MEMdq	vpunpcklbw xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKLBW_XMMdq_XMMq	vpunpcklbw xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKLBW_XMMdq_XMMdq_MEMdq	vpunpcklbw xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLBW_XMMdq_XMMdq_XMMdq	vpunpcklbw xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLBW_XMMu8_MASKmskw_XMMu8_MEMu8_AVX512	vpunpcklbw xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLBW_XMMu8_MASKmskw_XMMu8_XMMu8_AVX512	vpunpcklbw xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLBW_YMMqq_YMMqq_MEMqq	vpunpcklbw ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKLBW_YMMqq_YMMqq_YMMqq	vpunpcklbw ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLBW_YMMu8_MASKmskw_YMMu8_MEMu8_AVX512	vpunpcklbw ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKLBW_YMMu8_MASKmskw_YMMu8_YMMu8_AVX512	vpunpcklbw ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLBW_ZMMu8_MASKmskw_ZMMu8_MEMu8_AVX512	vpunpcklbw zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKLBW_ZMMu8_MASKmskw_ZMMu8_ZMMu8_AVX512	vpunpcklbw zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKLDQ_XMMdq_MEMdq	vpunpckldq xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKLDQ_XMMdq_XMMq	vpunpckldq xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKLDQ_XMMdq_XMMdq_MEMdq	vpunpckldq xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLDQ_XMMdq_XMMdq_XMMdq	vpunpckldq xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLDQ_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpunpckldq xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLDQ_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpunpckldq xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLDQ_YMMqq_YMMqq_MEMqq	vpunpckldq ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKLDQ_YMMqq_YMMqq_YMMqq	vpunpckldq ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLDQ_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpunpckldq ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKLDQ_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpunpckldq ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLDQ_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpunpckldq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKLDQ_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpunpckldq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKLQDQ_XMMdq_MEMdq	vpunpcklqdq xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKLQDQ_XMMdq_XMMq	vpunpcklqdq xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKLQDQ_XMMdq_XMMdq_MEMdq	vpunpcklqdq xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLQDQ_XMMdq_XMMdq_XMMdq	vpunpcklqdq xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLQDQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpunpcklqdq xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLQDQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpunpcklqdq xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLQDQ_YMMqq_YMMqq_MEMqq	vpunpcklqdq ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKLQDQ_YMMqq_YMMqq_YMMqq	vpunpcklqdq ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLQDQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpunpcklqdq ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKLQDQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpunpcklqdq ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLQDQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpunpcklqdq zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKLQDQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpunpcklqdq zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PUNPCKLWD_XMMdq_MEMdq	vpunpcklwd xmm1, xmm1, [rdi]	7	1
XED_IFORM_PUNPCKLWD_XMMdq_XMMq	vpunpcklwd xmm1, xmm1, xmm2	1	1
XED_IFORM_VPUNPCKLWD_XMMdq_XMMdq_MEMdq	vpunpcklwd xmm1, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLWD_XMMdq_XMMdq_XMMdq	vpunpcklwd xmm1, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLWD_XMMu16_MASKmskw_XMMu16_MEMu16_AVX512	vpunpcklwd xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VPUNPCKLWD_XMMu16_MASKmskw_XMMu16_XMMu16_AVX512	vpunpcklwd xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VPUNPCKLWD_YMMqq_YMMqq_MEMqq	vpunpcklwd ymm1, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKLWD_YMMqq_YMMqq_YMMqq	vpunpcklwd ymm1, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLWD_YMMu16_MASKmskw_YMMu16_MEMu16_AVX512	vpunpcklwd ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VPUNPCKLWD_YMMu16_MASKmskw_YMMu16_YMMu16_AVX512	vpunpcklwd ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VPUNPCKLWD_ZMMu16_MASKmskw_ZMMu16_MEMu16_AVX512	vpunpcklwd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VPUNPCKLWD_ZMMu16_MASKmskw_ZMMu16_ZMMu16_AVX512	vpunpcklwd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_PXOR_XMMdq_MEMdq	vpxor xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_PXOR_XMMdq_XMMdq	vpxor xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VPXOR_XMMdq_XMMdq_MEMdq	vpxor xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VPXOR_XMMdq_XMMdq_XMMdq	vpxor xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VPXOR_YMMqq_YMMqq_MEMqq	vpxor ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VPXOR_YMMqq_YMMqq_YMMqq	vpxor ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VPXORD_XMMu32_MASKmskw_XMMu32_MEMu32_AVX512	vpxord xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPXORD_XMMu32_MASKmskw_XMMu32_XMMu32_AVX512	vpxord xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPXORD_YMMu32_MASKmskw_YMMu32_MEMu32_AVX512	vpxord ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPXORD_YMMu32_MASKmskw_YMMu32_YMMu32_AVX512	vpxord ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPXORD_ZMMu32_MASKmskw_ZMMu32_MEMu32_AVX512	vpxord zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPXORD_ZMMu32_MASKmskw_ZMMu32_ZMMu32_AVX512	vpxord zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VPXORQ_XMMu64_MASKmskw_XMMu64_MEMu64_AVX512	vpxorq xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VPXORQ_XMMu64_MASKmskw_XMMu64_XMMu64_AVX512	vpxorq xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VPXORQ_YMMu64_MASKmskw_YMMu64_MEMu64_AVX512	vpxorq ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VPXORQ_YMMu64_MASKmskw_YMMu64_YMMu64_AVX512	vpxorq ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VPXORQ_ZMMu64_MASKmskw_ZMMu64_MEMu64_AVX512	vpxorq zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VPXORQ_ZMMu64_MASKmskw_ZMMu64_ZMMu64_AVX512	vpxorq zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VRANGEPD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vrangepd xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VRANGEPD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vrangepd xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VRANGEPD_YMMf64_MASKmskw_YMMf64_MEMf64_IMM8_AVX512	vrangepd ymm1{k1}, ymm2, [rdi], 1	4	0.5
XED_IFORM_VRANGEPD_YMMf64_MASKmskw_YMMf64_YMMf64_IMM8_AVX512	vrangepd ymm1{k1}, ymm2, ymm3, 1	4	0.5
XED_IFORM_VRANGEPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_IMM8_AVX512	vrangepd zmm1{k1}, zmm2, [rdi], 1	11	0.5
XED_IFORM_VRANGEPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_IMM8_AVX512	vrangepd zmm1{k1}, zmm2, zmm3, 1	4	0.5
XED_IFORM_VRANGEPS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vrangeps xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VRANGEPS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vrangeps xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VRANGEPS_YMMf32_MASKmskw_YMMf32_MEMf32_IMM8_AVX512	vrangeps ymm1{k1}, ymm2, [rdi], 1	4	0.5

XED_IFORM_VRANGEPS_YMMf32_MASKmskw_YMMf32_YMMf32_IMM8_AVX512	vrangeps ymm1{k1}, ymm2, ymm3, 1	4	0.5
XED_IFORM_VRANGEPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_IMM8_AVX512	vrangeps zmm1{k1}, zmm2, [rdi], 1	11	0.5
XED_IFORM_VRANGEPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_IMM8_AVX512	vrangeps zmm1{k1}, zmm2, zmm3, 1	4	0.5
XED_IFORM_VRANGESD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vrangesd xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VRANGESD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vrangesd xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VRANGESS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vrangess xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VRANGESS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vrangess xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VRCP14PD_XMMf64_MASKmskw_MEMf64_AVX512	vrcp14pd xmm1{k1}, [rdi]	10	1
XED_IFORM_VRCP14PD_XMMf64_MASKmskw_XMMf64_AVX512	vrcp14pd xmm1{k1}, xmm2	4	1
XED_IFORM_VRCP14PD_YMMf64_MASKmskw_MEMf64_AVX512	vrcp14pd ymm1{k1}, [rdi]	4	1
XED_IFORM_VRCP14PD_YMMf64_MASKmskw_YMMf64_AVX512	vrcp14pd ymm1{k1}, ymm2	4	1
XED_IFORM_VRCP14PD_ZMMf64_MASKmskw_MEMf64_AVX512	vrcp14pd zmm1{k1}, [rdi]	16	2
XED_IFORM_VRCP14PD_ZMMf64_MASKmskw_ZMMf64_AVX512	vrcp14pd zmm1{k1}, zmm2	9	2
XED_IFORM_VRCP14PS_XMMf32_MASKmskw_MEMf32_AVX512	vrcp14ps xmm1{k1}, [rdi]	10	1
XED_IFORM_VRCP14PS_XMMf32_MASKmskw_XMMf32_AVX512	vrcp14ps xmm1{k1}, xmm2	4	1
XED_IFORM_VRCP14PS_YMMf32_MASKmskw_MEMf32_AVX512	vrcp14ps ymm1{k1}, [rdi]	4	1
XED_IFORM_VRCP14PS_YMMf32_MASKmskw_YMMf32_AVX512	vrcp14ps ymm1{k1}, ymm2	4	1
XED_IFORM_VRCP14PS_ZMMf32_MASKmskw_MEMf32_AVX512	vrcp14ps zmm1{k1}, [rdi]	16	2
XED_IFORM_VRCP14PS_ZMMf32_MASKmskw_ZMMf32_AVX512	vrcp14ps zmm1{k1}, zmm2	9	2
XED_IFORM_VRCP14SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vrcp14sd xmm1{k1}, xmm2, [rdi]	10	1
XED_IFORM_VRCP14SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vrcp14sd xmm1{k1}, xmm2, xmm3	4	1
XED_IFORM_VRCP14SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vrcp14ss xmm1{k1}, xmm2, [rdi]	10	1
XED_IFORM_VRCP14SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vrcp14ss xmm1{k1}, xmm2, xmm3	4	1
XED_IFORM_RCPPS_XMMps_MEMps	vrcpps xmm1, [rdi]	10	1
XED_IFORM_VRCPPS_XMMdq_MEMdq	vrcpps xmm1, [rdi]	10	1
XED_IFORM_RCPPS_XMMps_XMMps	vrcpps xmm1, xmm2	4	1
XED_IFORM_VRCPPS_XMMdq_XMMdq	vrcpps xmm1, xmm2	4	1
XED_IFORM_VRCPPS_YMMqq_MEMqq	vrcpps ymm1, [rdi]	4	1
XED_IFORM_VRCPPS_YMMqq_YMMqq	vrcpps ymm1, ymm2	4	1
XED_IFORM_RCPSS_XMMss_MEMss	vrcpss xmm1, xmm1, [rdi]	9	1
XED_IFORM_RCPSS_XMMss_XMMss	vrcpss xmm1, xmm1, xmm2	4	1
XED_IFORM_VRCPSS_XMMdq_XMMdq_MEMd	vrcpss xmm1, xmm2, [rdi]	9	1
XED_IFORM_VRCPSS_XMMdq_XMMdq_XMMd	vrcpss xmm1, xmm2, xmm3	4	1
XED_IFORM_VREDUCEPD_XMMf64_MASKmskw_MEMf64_IMM8_AVX512	vreducepd xmm1{k1}, [rdi], 1	10	0.5
XED_IFORM_VREDUCEPD_XMMf64_MASKmskw_XMMf64_IMM8_AVX512	vreducepd xmm1{k1}, xmm2, 1	4	0.5
XED_IFORM_VREDUCEPD_YMMf64_MASKmskw_MEMf64_IMM8_AVX512	vreducepd ymm1{k1}, [rdi], 1	4	0.5
XED_IFORM_VREDUCEPD_YMMf64_MASKmskw_YMMf64_IMM8_AVX512	vreducepd ymm1{k1}, ymm2, 1	4	0.5
XED_IFORM_VREDUCEPD_ZMMf64_MASKmskw_MEMf64_IMM8_AVX512	vreducepd zmm1{k1}, [rdi], 1	11	0.5
XED_IFORM_VREDUCEPD_ZMMf64_MASKmskw_ZMMf64_IMM8_AVX512	vreducepd zmm1{k1}, zmm2, 1	4	0.5
XED_IFORM_VREDUCEPS_XMMf32_MASKmskw_MEMf32_IMM8_AVX512	vreduceps xmm1{k1}, [rdi], 1	10	0.5
XED_IFORM_VREDUCEPS_XMMf32_MASKmskw_XMMf32_IMM8_AVX512	vreduceps xmm1{k1}, xmm2, 1	4	0.5
XED_IFORM_VREDUCEPS_YMMf32_MASKmskw_MEMf32_IMM8_AVX512	vreduceps ymm1{k1}, [rdi], 1	4	0.5
XED_IFORM_VREDUCEPS_YMMf32_MASKmskw_YMMf32_IMM8_AVX512	vreduceps ymm1{k1}, ymm2, 1	4	0.5
XED_IFORM_VREDUCEPS_ZMMf32_MASKmskw_MEMf32_IMM8_AVX512	vreduceps zmm1{k1}, [rdi], 1	11	0.5
XED_IFORM_VREDUCEPS_ZMMf32_MASKmskw_ZMMf32_IMM8_AVX512	vreduceps zmm1{k1}, zmm2, 1	4	0.5
XED_IFORM_VREDUCESD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vreducesd xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VREDUCESD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vreducesd xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VREDUCESS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vreducess xmm1{k1}, xmm2, [rdi], 1	10	0.5
XED_IFORM_VREDUCESS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vreducess xmm1{k1}, xmm2, xmm3, 1	4	0.5
XED_IFORM_VRNDSCALEPD_XMMf64_MASKmskw_MEMf64_IMM8_AVX512	vrndscalepd xmm1{k1}, [rdi], 1	14	1
XED_IFORM_VRNDSCALEPD_XMMf64_MASKmskw_XMMf64_IMM8_AVX512	vrndscalepd xmm1{k1}, xmm2, 1	8	1
XED_IFORM_VRNDSCALEPD_YMMf64_MASKmskw_MEMf64_IMM8_AVX512	vrndscalepd ymm1{k1}, [rdi], 1	8	1
XED_IFORM_VRNDSCALEPD_YMMf64_MASKmskw_YMMf64_IMM8_AVX512	vrndscalepd ymm1{k1}, ymm2, 1	8	1
XED_IFORM_VRNDSCALEPD_ZMMf64_MASKmskw_MEMf64_IMM8_AVX512	vrndscalepd zmm1{k1}, [rdi], 1	15	1
XED_IFORM_VRNDSCALEPD_ZMMf64_MASKmskw_ZMMf64_IMM8_AVX512	vrndscalepd zmm1{k1}, zmm2, 1	8	1
XED_IFORM_VRNDSCALEPS_XMMf32_MASKmskw_MEMf32_IMM8_AVX512	vrndscaleps xmm1{k1}, [rdi], 1	14	1
XED_IFORM_VRNDSCALEPS_XMMf32_MASKmskw_XMMf32_IMM8_AVX512	vrndscaleps xmm1{k1}, xmm2, 1	8	1
XED_IFORM_VRNDSCALEPS_YMMf32_MASKmskw_MEMf32_IMM8_AVX512	vrndscaleps ymm1{k1}, [rdi], 1	8	1
XED_IFORM_VRNDSCALEPS_YMMf32_MASKmskw_YMMf32_IMM8_AVX512	vrndscaleps ymm1{k1}, ymm2, 1	8	1
XED_IFORM_VRNDSCALEPS_ZMMf32_MASKmskw_MEMf32_IMM8_AVX512	vrndscaleps zmm1{k1}, [rdi], 1	15	1
XED_IFORM_VRNDSCALEPS_ZMMf32_MASKmskw_ZMMf32_IMM8_AVX512	vrndscaleps zmm1{k1}, zmm2, 1	8	1
XED_IFORM_VRNDSCALESD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vrndscalesd xmm1{k1}, xmm2, [rdi], 1	14	1
XED_IFORM_VRNDSCALESD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vrndscalesd xmm1{k1}, xmm2, xmm3, 1	8	1
XED_IFORM_VRNDSCALESS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vrndscaless xmm1{k1}, xmm2, [rdi], 1	14	1
XED_IFORM_VRNDSCALESS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vrndscaless xmm1{k1}, xmm2, xmm3, 1	8	1
XED_IFORM_ROUNDPD_XMMpd_MEMpd_IMMb	vroundpd xmm1, [rdi], 1	14	1
XED_IFORM_VROUNDPD_XMMdq_MEMdq_IMMb	vroundpd xmm1, [rdi], 1	14	1
XED_IFORM_VROUNDPD_XMMdq_XMMdq_IMMb	vroundpd xmm1, xmm2, 1	8	1
XED_IFORM_ROUNDPD_XMMpd_XMMpd_IMMb	vroundpd xmm1, xmm2, 1	8	1
XED_IFORM_VROUNDPD_YMMqq_MEMqq_IMMb	vroundpd ymm1, [rdi], 1	8	1
XED_IFORM_VROUNDPD_YMMqq_YMMqq_IMMb	vroundpd ymm1, ymm2, 1	8	1
XED_IFORM_ROUNDPS_XMMps_MEMps_IMMb	vroundps xmm1, [rdi], 1	14	1
XED_IFORM_VROUNDPS_XMMdq_MEMdq_IMMb	vroundps xmm1, [rdi], 1	14	1
XED_IFORM_VROUNDPS_XMMdq_XMMdq_IMMb	vroundps xmm1, xmm2, 1	8	1
XED_IFORM_ROUNDPS_XMMps_XMMps_IMMb	vroundps xmm1, xmm2, 1	8	1
XED_IFORM_VROUNDPS_YMMqq_MEMqq_IMMb	vroundps ymm1, [rdi], 1	8	1
XED_IFORM_VROUNDPS_YMMqq_YMMqq_IMMb	vroundps ymm1, ymm2, 1	8	1
XED_IFORM_ROUNDSD_XMMq_MEMq_IMMb	vroundsd xmm1, xmm1, [rdi], 1	14	1
XED_IFORM_ROUNDSD_XMMq_XMMq_IMMb	vroundsd xmm1, xmm1, xmm2, 1	8	1

XED_IFORM_VROUNDSD_XMMdq_XMMdq_MEMq_IMMb	vroundsd xmm1, xmm2, [rdi], 1	14	1
XED_IFORM_VROUNDSD_XMMdq_XMMdq_XMMq_IMMb	vroundsd xmm1, xmm2, xmm3, 1	8	1
XED_IFORM_ROUNDSS_XMMd_MEMd_IMMb	vroundss xmm1, xmm1, [rdi], 1	14	1
XED_IFORM_ROUNDSS_XMMd_XMMd_IMMb	vroundss xmm1, xmm1, xmm2, 1	8	1
XED_IFORM_VROUNDSS_XMMdq_XMMdq_MEMd_IMMb	vroundss xmm1, xmm2, [rdi], 1	14	1
XED_IFORM_VROUNDSS_XMMdq_XMMdq_XMMd_IMMb	vroundss xmm1, xmm2, xmm3, 1	8	1
XED_IFORM_VRSQRT14PD_XMMf64_MASKmskw_MEMf64_AVX512	vrsqrt14pd xmm1{k1}, [rdi]	10	1
XED_IFORM_VRSQRT14PD_XMMf64_MASKmskw_XMMf64_AVX512	vrsqrt14pd xmm1{k1}, xmm2	4	1
XED_IFORM_VRSQRT14PD_YMMf64_MASKmskw_MEMf64_AVX512	vrsqrt14pd ymm1{k1}, [rdi]	4	1
XED_IFORM_VRSQRT14PD_YMMf64_MASKmskw_YMMf64_AVX512	vrsqrt14pd ymm1{k1}, ymm2	4	1
XED_IFORM_VRSQRT14PD_ZMMf64_MASKmskw_MEMf64_AVX512	vrsqrt14pd zmm1{k1}, [rdi]	16	2
XED_IFORM_VRSQRT14PD_ZMMf64_MASKmskw_ZMMf64_AVX512	vrsqrt14pd zmm1{k1}, zmm2	9	2
XED_IFORM_VRSQRT14PS_XMMf32_MASKmskw_MEMf32_AVX512	vrsqrt14ps xmm1{k1}, [rdi]	10	1
XED_IFORM_VRSQRT14PS_XMMf32_MASKmskw_XMMf32_AVX512	vrsqrt14ps xmm1{k1}, xmm2	4	1
XED_IFORM_VRSQRT14PS_YMMf32_MASKmskw_MEMf32_AVX512	vrsqrt14ps ymm1{k1}, [rdi]	4	1
XED_IFORM_VRSQRT14PS_YMMf32_MASKmskw_YMMf32_AVX512	vrsqrt14ps ymm1{k1}, ymm2	4	1
XED_IFORM_VRSQRT14PS_ZMMf32_MASKmskw_MEMf32_AVX512	vrsqrt14ps zmm1{k1}, [rdi]	16	2
XED_IFORM_VRSQRT14PS_ZMMf32_MASKmskw_ZMMf32_AVX512	vrsqrt14ps zmm1{k1}, zmm2	9	2
XED_IFORM_VRSQRT14SD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vrsqrt14sd xmm1{k1}, xmm2, [rdi]	10	1
XED_IFORM_VRSQRT14SD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vrsqrt14sd xmm1{k1}, xmm2, xmm3	4	1
XED_IFORM_VRSQRT14SS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vrsqrt14ss xmm1{k1}, xmm2, [rdi]	10	1
XED_IFORM_VRSQRT14SS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vrsqrt14ss xmm1{k1}, xmm2, xmm3	4	1
XED_IFORM_RSQRTPS_XMMps_MEMps	vrsqrtps xmm1, [rdi]	10	1
XED_IFORM_VRSQRTPS_XMMdq_MEMdq	vrsqrtps xmm1, [rdi]	10	1
XED_IFORM_RSQRTPS_XMMps_XMMps	vrsqrtps xmm1, xmm2	4	1
XED_IFORM_VRSQRTPS_XMMdq_XMMdq	vrsqrtps xmm1, xmm2	4	1
XED_IFORM_VRSQRTPS_YMMqq_MEMqq	vrsqrtps ymm1, [rdi]	4	1
XED_IFORM_VRSQRTPS_YMMqq_YMMqq	vrsqrtps ymm1, ymm2	4	1
XED_IFORM_RSQRTSS_XMMss_MEMss	vrsqrtss xmm1, xmm1, [rdi]	9	1
XED_IFORM_RSQRTSS_XMMss_XMMss	vrsqrtss xmm1, xmm1, xmm2	4	1
XED_IFORM_VRSQRTSS_XMMdq_XMMdq_MEMd	vrsqrtss xmm1, xmm2, [rdi]	9	1
XED_IFORM_VRSQRTSS_XMMdq_XMMdq_XMMd	vrsqrtss xmm1, xmm2, xmm3	4	1
XED_IFORM_VSCALEFPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vscalefpd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSCALEFPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vscalefpd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VSCALEFPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vscalefpd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VSCALEFPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vscalefpd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VSCALEFPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vscalefpd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VSCALEFPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vscalefpd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VSCALEFPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vscalefps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSCALEFPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vscalefps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VSCALEFPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vscalefps ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VSCALEFPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vscalefps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VSCALEFPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vscalefps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VSCALEFPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vscalefps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_VSCALEFSD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vscalefsd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSCALEFSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vscalefsd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VSCALEFSS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vscalefss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSCALEFSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vscalefss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VSCATTERDPD_MEMf64_MASKmskw_XMMf64_AVX512_VL128	vscatterdpd [rdi+xmm1*1]{k1}, xmm2	11	2
XED_IFORM_VSCATTERDPD_MEMf64_MASKmskw_YMMf64_AVX512_VL256	vscatterdpd [rdi+xmm1*1]{k1}, ymm2	11	4
XED_IFORM_VSCATTERDPD_MEMf64_MASKmskw_ZMMf64_AVX512_VL512	vscatterdpd [rdi+ymm1*1]{k1}, zmm2	11	8
XED_IFORM_VSCATTERDPS_MEMf32_MASKmskw_XMMf32_AVX512_VL128	vscatterdps [rdi+xmm1*1]{k1}, xmm2	12	4
XED_IFORM_VSCATTERDPS_MEMf32_MASKmskw_YMMf32_AVX512_VL256	vscatterdps [rdi+ymm1*1]{k1}, ymm2	12	8
XED_IFORM_VSCATTERDPS_MEMf32_MASKmskw_ZMMf32_AVX512_VL512	vscatterdps [rdi+zmm1*1]{k1}, zmm2	11	16.75
XED_IFORM_VSCATTERQPD_MEMf64_MASKmskw_XMMf64_AVX512_VL128	vscatterqpd [rdi+xmm1*1]{k1}, xmm2	11	2
XED_IFORM_VSCATTERQPD_MEMf64_MASKmskw_YMMf64_AVX512_VL256	vscatterqpd [rdi+ymm1*1]{k1}, ymm2	11	4
XED_IFORM_VSCATTERQPD_MEMf64_MASKmskw_ZMMf64_AVX512_VL512	vscatterqpd [rdi+zmm1*1]{k1}, zmm2	11	8
XED_IFORM_VSCATTERQPS_MEMf32_MASKmskw_XMMf32_AVX512_VL256	vscatterqps [rdi+xmm1*1]{k1}, xmm2	12	4
XED_IFORM_VSCATTERQPS_MEMf32_MASKmskw_XMMf32_AVX512_VL128	vscatterqps [rdi+xmm1*1]{k1}, xmm2	12	4
XED_IFORM_VSHUFF32X4_YMMf32_MASKmskw_YMMf32_MEMf32_IMM8_AVX512	vshuff32x4 ymm1{k1}, ymm2, [rdi], 1	3	1
XED_IFORM_VSHUFF32X4_YMMf32_MASKmskw_YMMf32_YMMf32_IMM8_AVX512	vshuff32x4 ymm1{k1}, ymm2, ymm3, 1	3	1
XED_IFORM_VSHUFF32X4_ZMMf32_MASKmskw_ZMMf32_MEMf32_IMM8_AVX512	vshuff32x4 zmm1{k1}, zmm2, [rdi], 1	10	1
XED_IFORM_VSHUFF32X4_ZMMf32_MASKmskw_ZMMf32_ZMMf32_IMM8_AVX512	vshuff32x4 zmm1{k1}, zmm2, zmm3, 1	3	1
XED_IFORM_VSHUFF64X2_YMMf64_MASKmskw_YMMf64_MEMf64_IMM8_AVX512	vshuff64x2 ymm1{k1}, ymm2, [rdi], 1	3	1
XED_IFORM_VSHUFF64X2_YMMf64_MASKmskw_YMMf64_YMMf64_IMM8_AVX512	vshuff64x2 ymm1{k1}, ymm2, ymm3, 1	3	1
XED_IFORM_VSHUFF64X2_ZMMf64_MASKmskw_ZMMf64_MEMf64_IMM8_AVX512	vshuff64x2 zmm1{k1}, zmm2, [rdi], 1	10	1
XED_IFORM_VSHUFF64X2_ZMMf64_MASKmskw_ZMMf64_ZMMf64_IMM8_AVX512	vshuff64x2 zmm1{k1}, zmm2, zmm3, 1	3	1
XED_IFORM_VSHUFI32X4_YMMu32_MASKmskw_YMMu32_MEMu32_IMM8_AVX512	vshufi32x4 ymm1{k1}, ymm2, [rdi], 1	3	1
XED_IFORM_VSHUFI32X4_YMMu32_MASKmskw_YMMu32_YMMu32_IMM8_AVX512	vshufi32x4 ymm1{k1}, ymm2, ymm3, 1	3	1
XED_IFORM_VSHUFI32X4_ZMMu32_MASKmskw_ZMMu32_MEMu32_IMM8_AVX512	vshufi32x4 zmm1{k1}, zmm2, [rdi], 1	10	1
XED_IFORM_VSHUFI32X4_ZMMu32_MASKmskw_ZMMu32_ZMMu32_IMM8_AVX512	vshufi32x4 zmm1{k1}, zmm2, zmm3, 1	3	1
XED_IFORM_VSHUFI64X2_YMMu64_MASKmskw_YMMu64_MEMu64_IMM8_AVX512	vshufi64x2 ymm1{k1}, ymm2, [rdi], 1	3	1
XED_IFORM_VSHUFI64X2_YMMu64_MASKmskw_YMMu64_YMMu64_IMM8_AVX512	vshufi64x2 ymm1{k1}, ymm2, ymm3, 1	3	1
XED_IFORM_VSHUFI64X2_ZMMu64_MASKmskw_ZMMu64_MEMu64_IMM8_AVX512	vshufi64x2 zmm1{k1}, zmm2, [rdi], 1	10	1
XED_IFORM_VSHUFI64X2_ZMMu64_MASKmskw_ZMMu64_ZMMu64_IMM8_AVX512	vshufi64x2 zmm1{k1}, zmm2, zmm3, 1	3	1
XED_IFORM_SHUFPD_XMMpd_MEMpd_IMMb	vshufpd xmm1, xmm1, [rdi], 1	7	1
XED_IFORM_SHUFPD_XMMpd_XMMpd_IMMb	vshufpd xmm1, xmm1, xmm2, 1	1	1
XED_IFORM_VSHUFPD_XMMdq_XMMdq_MEMdq_IMMb	vshufpd xmm1, xmm2, [rdi], 1	7	1
XED_IFORM_VSHUFPD_XMMdq_XMMdq_XMMdq_IMMb	vshufpd xmm1, xmm2, xmm3, 1	1	1

XED_IFORM_VSHUFPD_XMMf64_MASKmskw_XMMf64_MEMf64_IMM8_AVX512	vshufpd xmm1{k1}, xmm2, [rdi], 1	7	1
XED_IFORM_VSHUFPD_XMMf64_MASKmskw_XMMf64_XMMf64_IMM8_AVX512	vshufpd xmm1{k1}, xmm2, xmm3, 1	1	1
XED_IFORM_VSHUFPD_YMMqq_YMMqq_MEMqq_IMMb	vshufpd ymm1, ymm2, [rdi], 1	1	1
XED_IFORM_VSHUFPD_YMMqq_YMMqq_YMMqq_IMMb	vshufpd ymm1, ymm2, ymm3, 1	1	1
XED_IFORM_VSHUFPD_YMMf64_MASKmskw_YMMf64_MEMf64_IMM8_AVX512	vshufpd ymm1{k1}, ymm2, [rdi], 1	1	1
XED_IFORM_VSHUFPD_YMMf64_MASKmskw_YMMf64_YMMf64_IMM8_AVX512	vshufpd ymm1{k1}, ymm2, ymm3, 1	1	1
XED_IFORM_VSHUFPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_IMM8_AVX512	vshufpd zmm1{k1}, zmm2, [rdi], 1	8	1
XED_IFORM_VSHUFPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_IMM8_AVX512	vshufpd zmm1{k1}, zmm2, zmm3, 1	1	1
XED_IFORM_SHUFPS_XMMps_MEMps_IMMb	vshufps xmm1, xmm1, [rdi], 1	7	1
XED_IFORM_SHUFPS_XMMps_XMMps_IMMb	vshufps xmm1, xmm1, xmm2, 1	1	1
XED_IFORM_VSHUFPS_XMMdq_XMMdq_MEMdq_IMMb	vshufps xmm1, xmm2, [rdi], 1	7	1
XED_IFORM_VSHUFPS_XMMdq_XMMdq_XMMdq_IMMb	vshufps xmm1, xmm2, xmm3, 1	1	1
XED_IFORM_VSHUFPS_XMMf32_MASKmskw_XMMf32_MEMf32_IMM8_AVX512	vshufps xmm1{k1}, xmm2, [rdi], 1	7	1
XED_IFORM_VSHUFPS_XMMf32_MASKmskw_XMMf32_XMMf32_IMM8_AVX512	vshufps xmm1{k1}, xmm2, xmm3, 1	1	1
XED_IFORM_VSHUFPS_YMMqq_YMMqq_MEMqq_IMMb	vshufps ymm1, ymm2, [rdi], 1	1	1
XED_IFORM_VSHUFPS_YMMqq_YMMqq_YMMqq_IMMb	vshufps ymm1, ymm2, ymm3, 1	1	1
XED_IFORM_VSHUFPS_YMMf32_MASKmskw_YMMf32_MEMf32_IMM8_AVX512	vshufps ymm1{k1}, ymm2, [rdi], 1	1	1
XED_IFORM_VSHUFPS_YMMf32_MASKmskw_YMMf32_YMMf32_IMM8_AVX512	vshufps ymm1{k1}, ymm2, ymm3, 1	1	1
XED_IFORM_VSHUFPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_IMM8_AVX512	vshufps zmm1{k1}, zmm2, [rdi], 1	8	1
XED_IFORM_VSHUFPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_IMM8_AVX512	vshufps zmm1{k1}, zmm2, zmm3, 1	1	1
XED_IFORM_SQRTPD_XMMpd_MEMpd	vsqrtpd xmm1, [rdi]	24	6
XED_IFORM_VSQRTPD_XMMdq_MEMdq	vsqrtpd xmm1, [rdi]	24	6
XED_IFORM_VSQRTPD_XMMdq_XMMdq	vsqrtpd xmm1, xmm2	18	6
XED_IFORM_SQRTPD_XMMpd_XMMpd	vsqrtpd xmm1, xmm2	18	6
XED_IFORM_VSQRTPD_XMMf64_MASKmskw_MEMf64_AVX512	vsqrtpd xmm1{k1}, [rdi]	24	6
XED_IFORM_VSQRTPD_XMMf64_MASKmskw_XMMf64_AVX512	vsqrtpd xmm1{k1}, xmm2	18	6
XED_IFORM_VSQRTPD_YMMqq_MEMqq	vsqrtpd ymm1, [rdi]	18	12
XED_IFORM_VSQRTPD_YMMqq_YMMqq	vsqrtpd ymm1, ymm2	18	12
XED_IFORM_VSQRTPD_YMMf64_MASKmskw_MEMf64_AVX512	vsqrtpd ymm1{k1}, [rdi]	18	12
XED_IFORM_VSQRTPD_YMMf64_MASKmskw_YMMf64_AVX512	vsqrtpd ymm1{k1}, ymm2	18	12
XED_IFORM_VSQRTPD_ZMMf64_MASKmskw_MEMf64_AVX512	vsqrtpd zmm1{k1}, [rdi]	38	24
XED_IFORM_VSQRTPD_ZMMf64_MASKmskw_ZMMf64_AVX512	vsqrtpd zmm1{k1}, zmm2	31	24
XED_IFORM_SQRTPS_XMMps_MEMps	vsqrtps xmm1, [rdi]	18	3
XED_IFORM_VSQRTPS_XMMdq_MEMdq	vsqrtps xmm1, [rdi]	18	3
XED_IFORM_SQRTPS_XMMps_XMMps	vsqrtps xmm1, xmm2	12	3
XED_IFORM_VSQRTPS_XMMdq_XMMdq	vsqrtps xmm1, xmm2	12	3
XED_IFORM_VSQRTPS_XMMf32_MASKmskw_MEMf32_AVX512	vsqrtps xmm1{k1}, [rdi]	18	3
XED_IFORM_VSQRTPS_XMMf32_MASKmskw_XMMf32_AVX512	vsqrtps xmm1{k1}, xmm2	12	3
XED_IFORM_VSQRTPS_YMMqq_MEMqq	vsqrtps ymm1, [rdi]	12	6
XED_IFORM_VSQRTPS_YMMqq_YMMqq	vsqrtps ymm1, ymm2	12	6
XED_IFORM_VSQRTPS_YMMf32_MASKmskw_MEMf32_AVX512	vsqrtps ymm1{k1}, [rdi]	12	6
XED_IFORM_VSQRTPS_YMMf32_MASKmskw_YMMf32_AVX512	vsqrtps ymm1{k1}, ymm2	12	6
XED_IFORM_VSQRTPS_ZMMf32_MASKmskw_MEMf32_AVX512	vsqrtps zmm1{k1}, [rdi]	26	12
XED_IFORM_VSQRTPS_ZMMf32_MASKmskw_ZMMf32_AVX512	vsqrtps zmm1{k1}, zmm2	19	12
XED_IFORM_SQRTSD_XMMsd_MEMsd	vsqrtsd xmm1, xmm1, [rdi]	23	6
XED_IFORM_SQRTSD_XMMsd_XMMsd	vsqrtsd xmm1, xmm1, xmm2	18	6
XED_IFORM_VSQRTSD_XMMdq_XMMdq_MEMq	vsqrtsd xmm1, xmm2, [rdi]	23	6
XED_IFORM_VSQRTSD_XMMdq_XMMdq_XMMq	vsqrtsd xmm1, xmm2, xmm3	18	6
XED_IFORM_VSQRTSD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vsqrtsd xmm1{k1}, xmm2, [rdi]	24	6
XED_IFORM_VSQRTSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vsqrtsd xmm1{k1}, xmm2, xmm3	18	6
XED_IFORM_SQRTSS_XMMss_MEMss	vsqrtss xmm1, xmm1, [rdi]	17	3
XED_IFORM_SQRTSS_XMMss_XMMss	vsqrtss xmm1, xmm1, xmm2	12	3
XED_IFORM_VSQRTSS_XMMdq_XMMdq_MEMd	vsqrtss xmm1, xmm2, [rdi]	17	3
XED_IFORM_VSQRTSS_XMMdq_XMMdq_XMMd	vsqrtss xmm1, xmm2, xmm3	12	3
XED_IFORM_VSQRTSS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vsqrtss xmm1{k1}, xmm2, [rdi]	18	3
XED_IFORM_VSQRTSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vsqrtss xmm1{k1}, xmm2, xmm3	12	3
XED_IFORM_VSTMXCSR_MEMd	vstmxcsr [rdi]	6	1
XED_IFORM_STMXCSR_MEMd	vstmxcsr [rdi]	6	1
XED_IFORM_SUBPD_XMMpd_MEMpd	vsubpd xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_SUBPD_XMMpd_XMMpd	vsubpd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VSUBPD_XMMdq_XMMdq_MEMdq	vsubpd xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VSUBPD_XMMdq_XMMdq_XMMdq	vsubpd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VSUBPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vsubpd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSUBPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vsubpd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VSUBPD_YMMqq_YMMqq_MEMqq	vsubpd ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VSUBPD_YMMqq_YMMqq_YMMqq	vsubpd ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VSUBPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vsubpd ymm1{k1}, ymm2, [rdi]	4	0.5
XED_IFORM_VSUBPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vsubpd ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VSUBPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vsubpd zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VSUBPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vsubpd zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_SUBPS_XMMps_MEMps	vsubps xmm1, xmm1, [rdi]	10	0.5
XED_IFORM_SUBPS_XMMps_XMMps	vsubps xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VSUBPS_XMMdq_XMMdq_MEMdq	vsubps xmm1, xmm2, [rdi]	10	0.5
XED_IFORM_VSUBPS_XMMdq_XMMdq_XMMdq	vsubps xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VSUBPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vsubps xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSUBPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vsubps xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VSUBPS_YMMqq_YMMqq_MEMqq	vsubps ymm1, ymm2, [rdi]	4	0.5
XED_IFORM_VSUBPS_YMMqq_YMMqq_YMMqq	vsubps ymm1, ymm2, ymm3	4	0.5
XED_IFORM_VSUBPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vsubps ymm1{k1}, ymm2, [rdi]	4	0.5

XED_IFORM_VSUBPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vsubps ymm1{k1}, ymm2, ymm3	4	0.5
XED_IFORM_VSUBPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vsubps zmm1{k1}, zmm2, [rdi]	11	0.5
XED_IFORM_VSUBPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vsubps zmm1{k1}, zmm2, zmm3	4	0.5
XED_IFORM_SUBSD_XMMsd_MEMsd	vsubsd xmm1, xmm1, [rdi]	9	0.5
XED_IFORM_SUBSD_XMMsd_XMMsd	vsubsd xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VSUBSD_XMMdq_XMMdq_MEMq	vsubsd xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VSUBSD_XMMdq_XMMdq_XMMq	vsubsd xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VSUBSD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vsubsd xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSUBSD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vsubsd xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_SUBSS_XMMss_MEMss	vsubss xmm1, xmm1, [rdi]	9	0.5
XED_IFORM_SUBSS_XMMss_XMMss	vsubss xmm1, xmm1, xmm2	4	0.5
XED_IFORM_VSUBSS_XMMdq_XMMdq_MEMd	vsubss xmm1, xmm2, [rdi]	9	0.5
XED_IFORM_VSUBSS_XMMdq_XMMdq_XMMd	vsubss xmm1, xmm2, xmm3	4	0.5
XED_IFORM_VSUBSS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vsubss xmm1{k1}, xmm2, [rdi]	10	0.5
XED_IFORM_VSUBSS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vsubss xmm1{k1}, xmm2, xmm3	4	0.5
XED_IFORM_VTESTPD_XMMdq_MEMdq	vtestpd xmm1, [rdi]	8	1
XED_IFORM_VTESTPD_XMMdq_XMMdq	vtestpd xmm1, xmm2	2	1
XED_IFORM_VTESTPD_YMMqq_MEMqq	vtestpd ymm1, [rdi]	2	1
XED_IFORM_VTESTPD_YMMqq_YMMqq	vtestpd ymm1, ymm2	2	1
XED_IFORM_VTESTPS_XMMdq_MEMdq	vtestps xmm1, [rdi]	8	1
XED_IFORM_VTESTPS_XMMdq_XMMdq	vtestps xmm1, xmm2	2	1
XED_IFORM_VTESTPS_YMMqq_MEMqq	vtestps ymm1, [rdi]	2	1
XED_IFORM_VTESTPS_YMMqq_YMMqq	vtestps ymm1, ymm2	2	1
XED_IFORM_UCOMISD_XMMsd_MEMsd	vucomisd xmm1, [rdi]	7	1
XED_IFORM_VUCOMISD_XMMf64_MEMf64_AVX512	vucomisd xmm1, [rdi]	7	1
XED_IFORM_VUCOMISD_XMMdq_MEMq	vucomisd xmm1, [rdi]	7	1
XED_IFORM_VUCOMISD_XMMf64_XMMf64_AVX512	vucomisd xmm1, xmm2	2	1
XED_IFORM_UCOMISD_XMMsd_XMMsd	vucomisd xmm1, xmm2	2	1
XED_IFORM_VUCOMISD_XMMdq_XMMq	vucomisd xmm1, xmm2	2	1
XED_IFORM_VUCOMISS_XMMf32_MEMf32_AVX512	vucomiss xmm1, [rdi]	7	1
XED_IFORM_UCOMISS_XMMss_MEMss	vucomiss xmm1, [rdi]	7	1
XED_IFORM_VUCOMISS_XMMdq_MEMd	vucomiss xmm1, [rdi]	7	1
XED_IFORM_VUCOMISS_XMMf32_XMMf32_AVX512	vucomiss xmm1, xmm2	2	1
XED_IFORM_VUCOMISS_XMMdq_XMMd	vucomiss xmm1, xmm2	2	1
XED_IFORM_UCOMISS_XMMss_XMMss	vucomiss xmm1, xmm2	2	1
XED_IFORM_UNPCKHPD_XMMpd_MEMdq	vunpckhpd xmm1, xmm1, [rdi]	7	1
XED_IFORM_UNPCKHPD_XMMpd_XMMq	vunpckhpd xmm1, xmm1, xmm2	1	1
XED_IFORM_VUNPCKHPD_XMMdq_XMMdq_MEMdq	vunpckhpd xmm1, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKHPD_XMMdq_XMMdq_XMMdq	vunpckhpd xmm1, xmm2, xmm3	1	1
XED_IFORM_VUNPCKHPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vunpckhpd xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKHPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vunpckhpd xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VUNPCKHPD_YMMqq_YMMqq_MEMqq	vunpckhpd ymm1, ymm2, [rdi]	1	1
XED_IFORM_VUNPCKHPD_YMMqq_YMMqq_YMMqq	vunpckhpd ymm1, ymm2, ymm3	1	1
XED_IFORM_VUNPCKHPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vunpckhpd ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VUNPCKHPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vunpckhpd ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VUNPCKHPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vunpckhpd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VUNPCKHPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vunpckhpd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_UNPCKHPS_XMMps_MEMdq	vunpckhps xmm1, xmm1, [rdi]	7	1
XED_IFORM_UNPCKHPS_XMMps_XMMdq	vunpckhps xmm1, xmm1, xmm2	1	1
XED_IFORM_VUNPCKHPS_XMMdq_XMMdq_MEMdq	vunpckhps xmm1, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKHPS_XMMdq_XMMdq_XMMdq	vunpckhps xmm1, xmm2, xmm3	1	1
XED_IFORM_VUNPCKHPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vunpckhps xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKHPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vunpckhps xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VUNPCKHPS_YMMqq_YMMqq_MEMqq	vunpckhps ymm1, ymm2, [rdi]	1	1
XED_IFORM_VUNPCKHPS_YMMqq_YMMqq_YMMqq	vunpckhps ymm1, ymm2, ymm3	1	1
XED_IFORM_VUNPCKHPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vunpckhps ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VUNPCKHPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vunpckhps ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VUNPCKHPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vunpckhps zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VUNPCKHPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vunpckhps zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_UNPCKLPD_XMMpd_MEMdq	vunpcklpd xmm1, xmm1, [rdi]	7	1
XED_IFORM_UNPCKLPD_XMMpd_XMMq	vunpcklpd xmm1, xmm1, xmm2	1	1
XED_IFORM_VUNPCKLPD_XMMdq_XMMdq_MEMdq	vunpcklpd xmm1, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKLPD_XMMdq_XMMdq_XMMdq	vunpcklpd xmm1, xmm2, xmm3	1	1
XED_IFORM_VUNPCKLPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vunpcklpd xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKLPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vunpcklpd xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VUNPCKLPD_YMMqq_YMMqq_MEMqq	vunpcklpd ymm1, ymm2, [rdi]	1	1
XED_IFORM_VUNPCKLPD_YMMqq_YMMqq_YMMqq	vunpcklpd ymm1, ymm2, ymm3	1	1
XED_IFORM_VUNPCKLPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vunpcklpd ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VUNPCKLPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vunpcklpd ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VUNPCKLPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vunpcklpd zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VUNPCKLPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vunpcklpd zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_UNPCKLPS_XMMps_MEMdq	vunpcklps xmm1, xmm1, [rdi]	7	1
XED_IFORM_UNPCKLPS_XMMps_XMMq	vunpcklps xmm1, xmm1, xmm2	1	1
XED_IFORM_VUNPCKLPS_XMMdq_XMMdq_MEMdq	vunpcklps xmm1, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKLPS_XMMdq_XMMdq_XMMdq	vunpcklps xmm1, xmm2, xmm3	1	1
XED_IFORM_VUNPCKLPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vunpcklps xmm1{k1}, xmm2, [rdi]	7	1
XED_IFORM_VUNPCKLPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vunpcklps xmm1{k1}, xmm2, xmm3	1	1
XED_IFORM_VUNPCKLPS_YMMqq_YMMqq_MEMqq	vunpcklps ymm1, ymm2, [rdi]	1	1
XED_IFORM_VUNPCKLPS_YMMqq_YMMqq_YMMqq	vunpcklps ymm1, ymm2, ymm3	1	1

XED_IFORM_VUNPCKLPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vunpcklps ymm1{k1}, ymm2, [rdi]	1	1
XED_IFORM_VUNPCKLPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vunpcklps ymm1{k1}, ymm2, ymm3	1	1
XED_IFORM_VUNPCKLPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vunpcklps zmm1{k1}, zmm2, [rdi]	8	1
XED_IFORM_VUNPCKLPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vunpcklps zmm1{k1}, zmm2, zmm3	1	1
XED_IFORM_XORPD_XMMpd_MEMpd	vxorpd xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_XORPD_XMMpd_XMMpd	vxorpd xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VXORPD_XMMdq_XMMdq_MEMdq	vxorpd xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VXORPD_XMMdq_XMMdq_XMMdq	vxorpd xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VXORPD_XMMf64_MASKmskw_XMMf64_MEMf64_AVX512	vxorpd xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VXORPD_XMMf64_MASKmskw_XMMf64_XMMf64_AVX512	vxorpd xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VXORPD_YMMqq_YMMqq_MEMqq	vxorpd ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VXORPD_YMMqq_YMMqq_YMMqq	vxorpd ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VXORPD_YMMf64_MASKmskw_YMMf64_MEMf64_AVX512	vxorpd ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VXORPD_YMMf64_MASKmskw_YMMf64_YMMf64_AVX512	vxorpd ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VXORPD_ZMMf64_MASKmskw_ZMMf64_MEMf64_AVX512	vxorpd zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VXORPD_ZMMf64_MASKmskw_ZMMf64_ZMMf64_AVX512	vxorpd zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_XORPS_XMMps_MEMps	vxorps xmm1, xmm1, [rdi]	7	0.5
XED_IFORM_XORPS_XMMps_XMMps	vxorps xmm1, xmm1, xmm2	1	0.33
XED_IFORM_VXORPS_XMMdq_XMMdq_MEMdq	vxorps xmm1, xmm2, [rdi]	7	0.5
XED_IFORM_VXORPS_XMMdq_XMMdq_XMMdq	vxorps xmm1, xmm2, xmm3	1	0.33
XED_IFORM_VXORPS_XMMf32_MASKmskw_XMMf32_MEMf32_AVX512	vxorps xmm1{k1}, xmm2, [rdi]	7	0.5
XED_IFORM_VXORPS_XMMf32_MASKmskw_XMMf32_XMMf32_AVX512	vxorps xmm1{k1}, xmm2, xmm3	1	0.33
XED_IFORM_VXORPS_YMMqq_YMMqq_MEMqq	vxorps ymm1, ymm2, [rdi]	1	0.5
XED_IFORM_VXORPS_YMMqq_YMMqq_YMMqq	vxorps ymm1, ymm2, ymm3	1	0.33
XED_IFORM_VXORPS_YMMf32_MASKmskw_YMMf32_MEMf32_AVX512	vxorps ymm1{k1}, ymm2, [rdi]	1	0.5
XED_IFORM_VXORPS_YMMf32_MASKmskw_YMMf32_YMMf32_AVX512	vxorps ymm1{k1}, ymm2, ymm3	1	0.33
XED_IFORM_VXORPS_ZMMf32_MASKmskw_ZMMf32_MEMf32_AVX512	vxorps zmm1{k1}, zmm2, [rdi]	8	0.5
XED_IFORM_VXORPS_ZMMf32_MASKmskw_ZMMf32_ZMMf32_AVX512	vxorps zmm1{k1}, zmm2, zmm3	1	0.5
XED_IFORM_VZEROALL	vzeroall	16	4
XED_IFORM_VZEROUPPER	vzeroupper	4	1
XED_IFORM_XADD_MEMb_GPR8	xadd [rdi], al	7	1
XED_IFORM_XADD_MEMv_GPRv	xadd [rdi], rax	7	1
XED_IFORM_XADD_GPR8_GPR8	xadd al, cl	3	0.75
XED_IFORM_XADD_GPRv_GPRv	xadd rax, rcx	3	0.75
XED_IFORM_XCHG_MEMb_GPR8	xchg [rdi], al	10	1.25
XED_IFORM_XCHG_MEMv_GPRv	xchg [rdi], rax	10	1.25
XED_IFORM_XCHG_GPR8_GPR8	xchg cl, al	3	0.75
XED_IFORM_XCHG_GPRv_GPRv	xchg rcx, rax	1	0.25
XED_IFORM_XGETBV	xgetbv	2	0.5
XED_IFORM_XOR_MEMb_IMMb_80r6	xor [rdi], 1	6	1
XED_IFORM_XOR_MEMv_IMMz	xor [rdi], 1	6	1
XED_IFORM_XOR_MEMv_IMMb	xor [rdi], 1	6	1
XED_IFORM_XOR_MEMb_IMMb_82r6	xor [rdi], 1	6	1
XED_IFORM_XOR_MEMb_GPR8	xor [rdi], al	6	1
XED_IFORM_XOR_MEMv_GPRv	xor [rdi], rax	6	1
XED_IFORM_XOR_GPR8_MEMb	xor al, [rdi]	6	0.5
XED_IFORM_XOR_GPR8_IMMb_80r6	xor al, 1	1	0.25
XED_IFORM_XOR_GPR8_IMMb_82r6	xor al, 1	1	0.25
XED_IFORM_XOR_AL_IMMb	xor al, 1	1	0.25
XED_IFORM_XOR_GPR8_GPR8_30	xor al, cl	0	0.25
XED_IFORM_XOR_GPR8_GPR8_32	xor al, cl	0	0.25
XED_IFORM_XOR_OrAX_IMMz	xor ax, 1	1	0.25
XED_IFORM_XOR_GPRv_MEMv	xor rax, [rdi]	6	0.5
XED_IFORM_XOR_GPRv_IMMz	xor rax, 1	1	0.25
XED_IFORM_XOR_GPRv_IMMb	xor rax, 1	1	0.25
XED_IFORM_XOR_GPRv_GPRv_31	xor rax, rcx	0	0.25
XED_IFORM_XOR_GPRv_GPRv_33	xor rax, rcx	0	0.25
XED_IFORM_XRSTOR_MEMmxsave	xrstor ptr [rdi]	37	8
XED_IFORM_XRSTOR64_MEMmxsave	xrstor64 ptr [rdi]	37	8
XED_IFORM_XSAVE_MEMmxsave	xsave ptr [rdi]	42	11
XED_IFORM_XSAVE64_MEMmxsave	xsave64 ptr [rdi]	41	10
XED_IFORM_XSAVEOPT_MEMmxsave	xsaveopt ptr [rdi]	46	11
XED_IFORM_XSAVEOPT64_MEMmxsave	xsaveopt64 ptr [rdi]	46	11
XED_IFORM_XSETBV	xsetbv	5	1.25