National Semiconductor

PRODUCT BRIEF
September 2000

Geode™ SC3200 WebPAD™ on a Chip

General Description

The Geode SC3200 device is a member of the National IA on a Chip family of fully integrated x86 system chips. The Geode SC3200 includes a Geode GX1™ 32-bit x86 compatible processor, TFT video processor, Core Logic, and a SuperI/O block.

These features, combined with the device's small form factor and low power consumption, make it ideal as the core of a Personal Access Device (PAD).

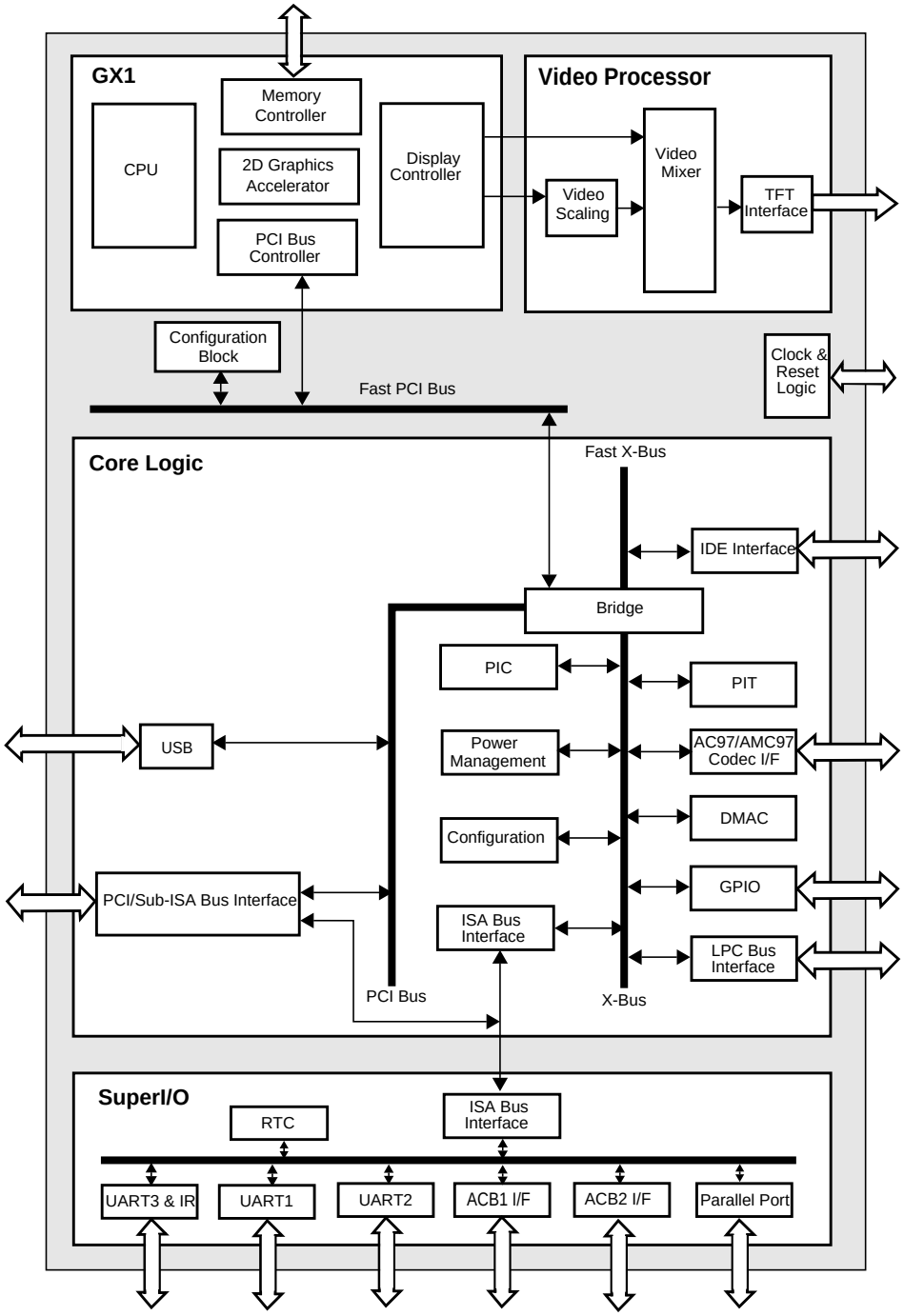
The Geode SC3200 integrated architecture simplifies system design by reducing the component count, the number of traces on the main system board, and the overall system power requirements. It can significantly lower overall system costs while improving time-to-market.

Primary Components of the Geode SC3200

- The Geode GX1 combines advanced CPU performance with MMX™ support, fully accelerated 2D graphics, a 64-bit synchronous DRAM (SDRAM) interface, a PCI bus controller, and a display controller.
- The low-power TFT video processor has a hardware video accelerator for scaling, filtering, and color space conversion.
- Core Logic of the SC3200 device includes: PC AT functionality, a USB interface, an IDE interface, a PCI bus interface, an LPC bus interface, ACPI 1.0 compliant power managementand an audio codec interface.
- Other primary components include: three serial ports (UART1, UART2, UART3 with fast Infrared), a parallel port, two ACCESS.bus (ACB) interfaces, and a Real-Time Clock (RTC).

The block diagram on the following page shows the relationships between the functional blocks in the SC3200.

Block Diagram



Features

Outstanding Features

- 32-bit x86 processor, up to 233 MHz, with MMX instruction set support
- Memory controller with 64-bit SDRAM interface
- 2D graphics accelerator
- TFT controller with hardware video accelerator
- PC AT functionality
- PCI bus controller
- IDE interface
- USB, three ports, OpenHCI 1.0 compliant
- Audio, AC97/AMC97 2.0 compliant
- Virtual System Architecture (VSA™) support
- Power management, ACPI 1.0 compliant
- EBGA package

GX1

CPU

- 32-bit x86, up to 266 MHz, with MMX compatible instruction set support
- 16 KB unified L1 cache
- Integrated Floating Point Unit (FPU)
- Re-entrant SMM enhanced for VSA

2D Graphics Accelerator

- Accelerates BitBLTs, line draw and text
- Supports all 256 raster operations
- Supports transparent BLTs
- Runs at core clock frequency

Memory Controller

- 64-bit SDRAM interface
- 66 MHz to 100 MHz frequency range
- Direct interface with CPU/cache, display controller and 2D graphic accelerator
- Supports clock suspend and power-down/self-refresh
- Up to 8 SDRAM devices or one DIMM/SODIMM

Display Controller

- Hardware graphics frame buffer compress/decompress
- Hardware cursor, 32 x 32 pixels

Video Processor

Video Accelerator

- Hardware video accelerator with video shaping and image enhancing
- Flexible video scaling support of up to 800% (horizontally and vertically)
- Bilinear interpolation filters (with two taps, and eight phases) to smooth output video
- Video/Graphics mixer using color key
- TFT Interface
  - 800 x 600 non-interlaced TFT @ 16 bpp Graphics, up to 75 Hz 18 bpp interface
  - 1024 x 768 non-interlaced TFT @ 16 bpp Graphics, up to 75 Hz 18 bpp interface

Core Logic

Audio

- AC97/AMC97 (Rev. 2.0) codec interface
- Legacy audio emulation using XpressAUDIO™
- 6 DMA channels

PC AT Functionality

- Programmable Interrupt Controller (PIC), 8259A-equivalent
- Programmable Interval Timer (PIT), 8254-equivalent
- DMA Controller (DMAC), 8237-equivalent

Power Management

- ACPI 1.0 compliant
- Sx state control of three power planes
- Cx/Sx state control of clocks and PLLs
- Thermal event input
- Wake-up event support:
  - Three general-purpose events
  - AC97 codec event
  - UART2 $\overline{RI}$ signal
  - Infrared (IR) event

General Purpose I/O (GPIO) Ports

- 27 multiplexed GPIO signals

Low Pin Count (LPC) Bus Interface

- Specification Rev. 1.0 compatible

PCI Bus Interface

- PCI 2.1 compliant with wake-up capability
- 32-bit data path, up to 33 MHz
- Glueless interface for an external PCI device
- Fixed priority
- 3.3V signal support only

Sub-ISA Bus Interface

- Up to 16 MB addressing
- Supports a chip select for ROM or Flash EPROM boot device
- Supports either:
  - DiskOnChip® DOC2000 Flash file system
  - NAND E^2PROM

Features (Continued)

- Supports up to two chip selects for external I/O devices
- 8-bit (optional 16-bit) data bus width
- Shares balls with PCI signals

IDE Interface

- IDE channel for up to two external IDE devices
- Supports ATA-33 synchronous DMA mode transfers, up to 33 MB/s

Universal Serial Bus (USB)

- USB OpenHCI 1.0 compliant
- Three ports

SuperI/O

Real-Time Clock (RTC)

- DS1287, MC146818 and PC87911 compatible
- Multi-century calendar

ACCESS.bus (ACB) Interface

- Two ACB interface ports

Parallel Port

- EPP 1.9 compliant
- IEEE1284 ECP compliant, including level 2

Serial Port (UART)

- UART1, 16550A compatible (SIN, SOUT, BOUT pins), used for smart card interface
- UART2, 16550A compatible
- Enhanced UART with fast Infrared (IR)

Other Features

High Resolution Timer

- 32-bit counter with 0.92593 µS count interval

WATCHDOG

- Interfaces to INTR, SMI, Reset

Clocks

- Input:
  - 32.768 KHz (internal clock oscillator)
  - 25 MHz (internal clock oscillator)
- Output:
  - AC97 clock (24.576 MHz)
  - Memory controller clock (66 MHz to 100 MHz)
  - Ethernet clock (25 MHz)
  - PCI clock (33 MHz)

JTAG Testability

- Bypass, Extest, Sample/Preload, IDcode, Clamp, Hiz

Voltages

- Internal logic:
  - CPU frequency up to 266 MHz: 2.0V
  - CPU frequency up to 200 MHz: 1.8V
- Battery: 3V
- I/O: 3.3V
- Standby: 3.3V
- Internal standby: 1.8V

Package

- EBGA, 432 balls
- Footprint: 40 x 40 mm,1.27 mm pitch

1.0 Signal Definitions

This section defines the signals and describes the external interface of the SC3200 device. Figure 2-1 shows the signals organized by their functional groups. Where signals are multiplexed, the default signal name is listed first and is separated by a slash (/) from other signal names.

The overline (¯) symbol above a signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. Otherwise, the signal is asserted when at a high voltage level.

1.1 Signal Groups

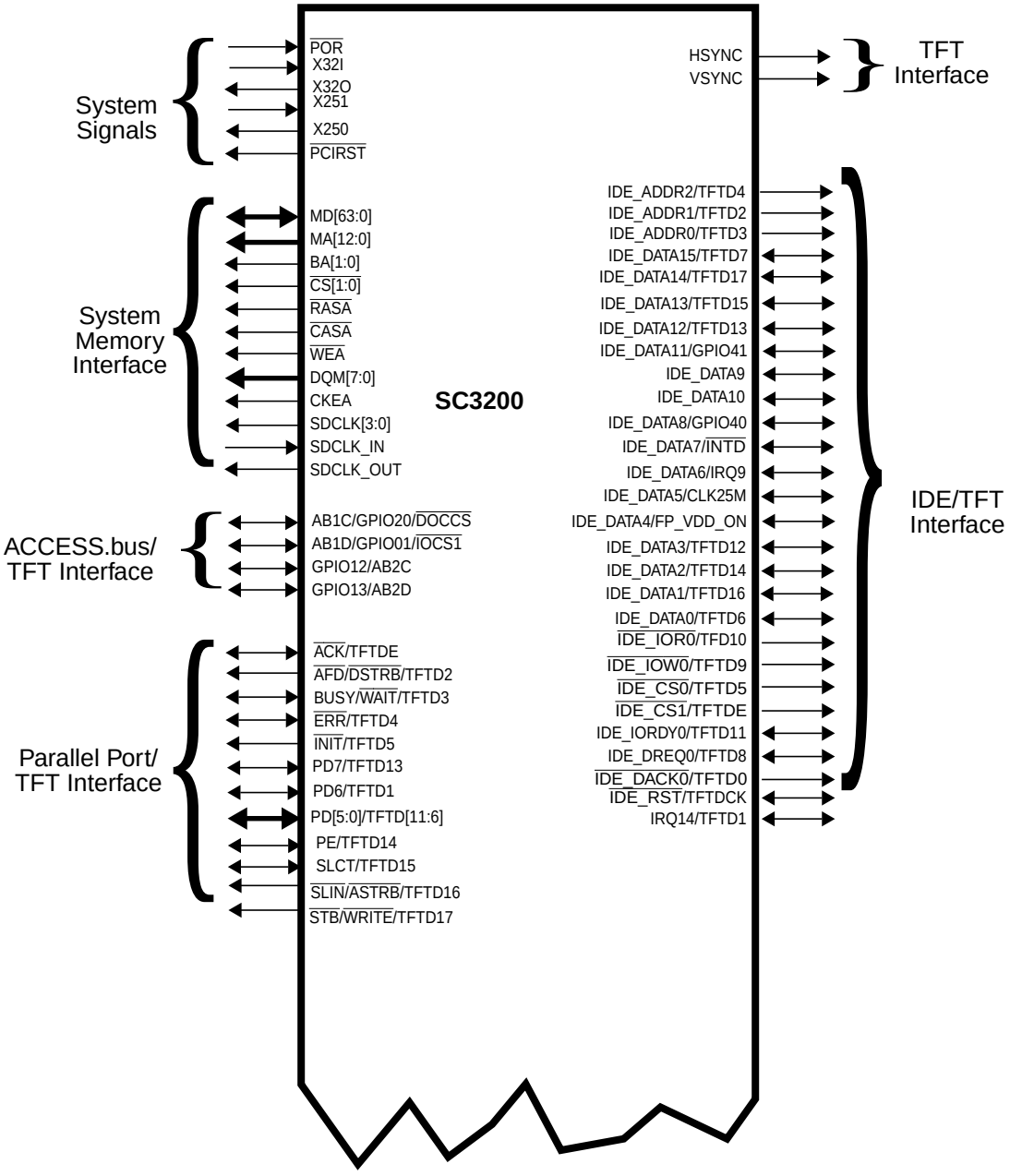


Figure 1 SC3200 Signal Groups

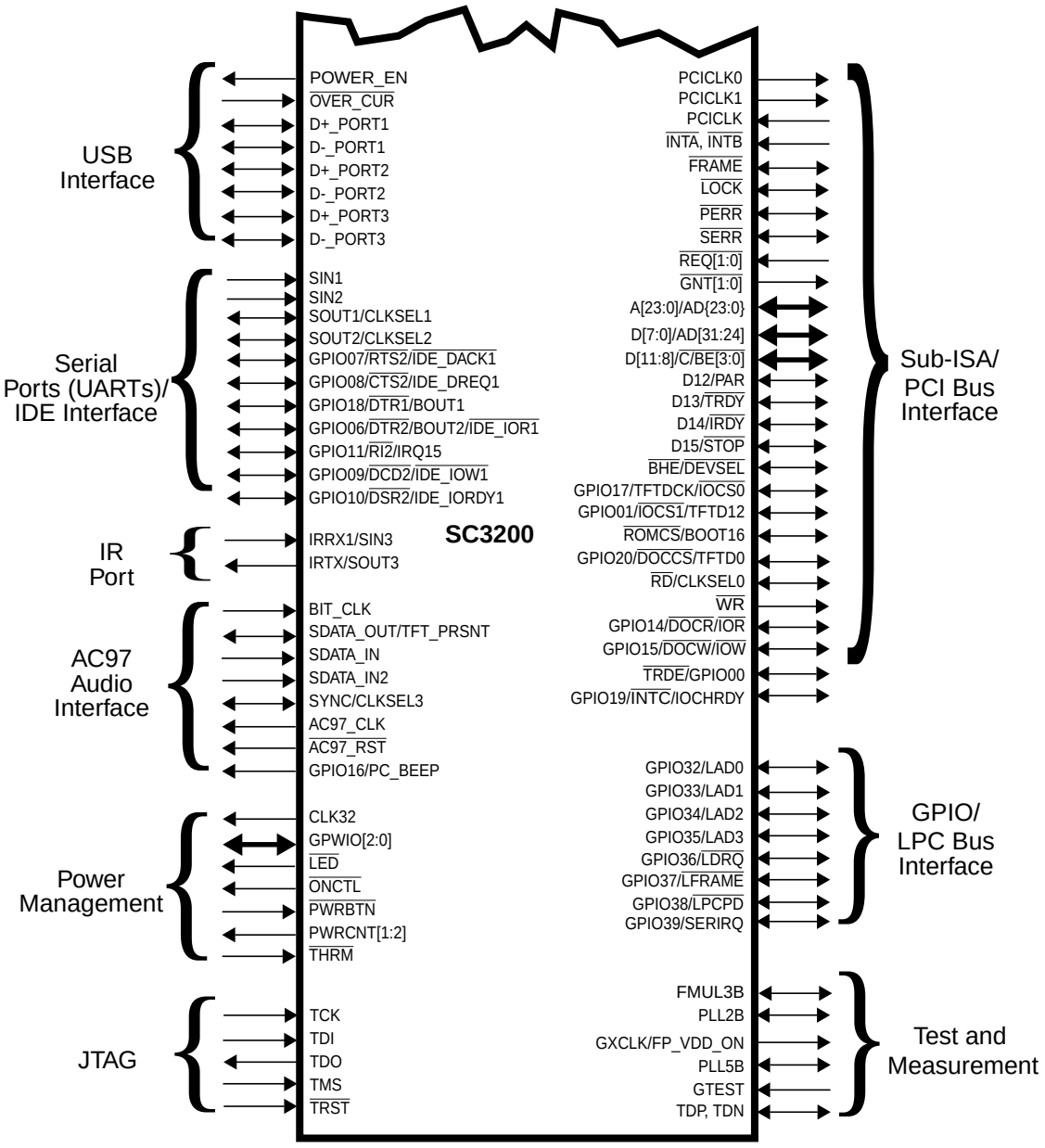


Figure 1. SC3200 Signal Groups (Cont'd)

1.1.1 Functional Pin Summary

Module	Pin Count
System Signals	6
System Memory Interface	99
IDE Interface (channel 1)	28
IDE Interface (channel 2, multiplexed))	(6)
TFT Interface (multiplexed)	(21)
ACCESS.bus Interface	4
PCI Bus Interface	54
Sub-ISA Interface (including NAND E^2PROM)	10
LPC Interface	8
Universal Serial Bus (USB)	8
UART1 (for smart card)	3
UART2	8
Parallel Port Interface (IEEE 1284)	17
Fast Infrared (IR) Port / UART3	2
AC97 Audio Interface	8
Power Management	10
Miscellaneous/Test/JTAG	12
GPIO Ports (multiplexed)	(27)
Total	277

1.1.2 Signal Descriptions

The following tables contain descriptions of each signal of the SC3200 device.

1.1.3 System Signals

Name	Type	Description	MUX
CLKSEL[1:0]	I	**Fast PCI Clock Select.** These strap signals are used to set the internal fast PCI clock. 00: 33.3 MHz 01: 48 MHz 10: 66.7 MHz 11: 33.3 MHz During system reset, an internal pull-down resistor of 100 KΩ exists on these pins. If needed, an external pull-up resistor of 15 KΩ should be placed.[1]	
CLKSEL[3:2]	I	**Maximum Core Clock Multiplier.** These strap signals are used to set the maximum allowed multiplier value for the core clock. During system reset, an internal pull-down resistor of 100 KΩ exists on these pins. If needed, an external pull-up resistor of 15 KΩ should be placed.[1]	
BOOT16	I	**16-Bit Wide Boot ROM.** This strap signal enables the optional 16-bit wide Sub-ISA bus. During system reset, an internal pull-down resistor of 100 KΩ exists on this pin. If needed, an external pull-up resistor of 15 KΩ should be placed.[1]	
$\overline{\text{POR}}$	I	**Power On Reset.** $\overline{\text{POR}}$ is the system reset signal generated from the power supply to indicate that the system should be reset.	
X32I, X32O	I/O	**Crystal.** Connected directly to a 32.768 KHz crystal. This clock input is required even if the internal RTC is not being used. Some of the internal clocks are derived from this clock. If an external clock is used, it should be connected to X32I, (X32O should remain unconnected), using a voltage level of 0 volts to V_{CORE}.	
X25I, X25O	I/O	**Crystal.** Connected directly to a 25 MHz crystal. This clock input is used for video circuits. Some of the internal clocks are derived from this clock. If an external clock is used, it should be connected to X25I, and X250, using a voltage level of 0 volts to V_{IO}. X25O should remain unconnected.	
CLK25M	O	25 **MHz Output Clock**	
$\overline{\text{PCIRST}}$	O	**PCI and System Reset.** $\overline{\text{PCIRST}}$ is the reset signal for the PCI bus and system. It is asserted for approximately 100 µS after $\overline{\text{POR}}$ is negated.	

1. An external pull-up or pull-down resistor may be needed for these pins if external components have an input DC current. This resistor should have a resistance of at least 1KΩ.

1.1.4 System Memory Interface

Name	Type	Description	
MD[63:0]	I/O	**Memory Data Bus.** The data bus lines driven to/from system memory.	
MA[12:0]	O	**Memory Address Bus.** The multiplexed row/column address lines driven to the system memory. Supports 256 Mbit SDRAM.	
BA[1:0]	O	**Bank Address Bits.** These bits are used to select the component bank within the SDRAM.	
$\overline{\text{CS}}$[1:0]	O	**Chip Selects.** These bits are used to select the module bank within system memory. Each chip select corresponds to a specific module bank. If $\overline{\text{CS}}$ is high, the bank(s) do not respond to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ until the bank is selected again.	
$\overline{\text{RASA}}$	O	**Row Address Strobe.** $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and CKE are encoded to support the different SDRAM commands. $\overline{\text{RASA}}$ is used with $\overline{\text{CS}}$[1:0].	
$\overline{\text{CASA}}$	O	**Column Address Strobe.** $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and CKE are encoded to support the different SDRAM commands. $\overline{\text{CASA}}$ is used with $\overline{\text{CS}}$[1:0].	
$\overline{\text{WEA}}$	O	**Write Enable.** $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and CKE are encoded to support the different SDRAM commands. $\overline{\text{WEA}}$ is used with $\overline{\text{CS}}$[1:0].	
DQM[7:0]	O	**Data Mask Control Bits** During memory read cycles, these outputs control whether SDRAM output buffers are driven on the MD bus or not. All DQM signals are asserted during read cycles. During memory write cycles, these outputs control whether or not MD data will be written into SDRAM. DQM[7:0] connect directly to the [DQM7:0] pins of each DIMM connector.	
CKEA	O	**Clock Enable.** These signals are used to enter Suspend/power-down mode. If CKE goes low when no read or write cycle is in progress, the SDRAM enters power-down mode. To ensure that SDRAM data remains valid, the self-refresh command is executed. To exit this mode and return to normal oepration, drive CKE high. These signals should have an external pull-down resistor of 33 KΩ .	
SDCLK[3:0]	O	**SDRAM Clocks.** SDRAM uses these clocks to sample all control, address, and data lines. To ensure that the Suspend mode functions correctly, SDCLK3 and SDCLK1 should be used with $\overline{\text{CS1}}$. SDCLK2 and SDCLK0 should be used together with $\overline{\text{CS0}}$.	
SDCLK_IN	I	**SDRAM Clock Input.** The SC3200 samples the memory read data on this clock. Works in conjunction with the SDCLK_OUT signal.	
SDCLK_OUT	O	**SDRAM Clock Output.** This output is routed back to SDCLK_IN. The board designer should vary the length of the board trace to control skew between SDCLK_IN and SDCLK.	

1.1.5 TFT Interface

Name	Type	Description	
HSYNC	O	**Horizontal Sync**	
VSYNC	O	**Vertical Sync**	

Name	Type	Description	
TFTDCK	O	**TFT Clock.** Clock to external CRT DACs or TFT.	
TFTDE	O	**TFT Data Enable.** Can be used as blank signal to external CRT DACs.	
FP_VDD_ON	O	**TFT Power Control.** Used to enable power to the Flat Panel display, with power sequence timing.	
TFTD[17:0]	O	**Digital RGB Data to TFT** TFTD[5:0] are connected to the Blue TFT inputs. TFTD[11:6 are connected to the Green TFT inputs. TFTD[17:12] are connected to the Red TFT inputs.	
TFT_PRSNT	I	**TFT Present.** A strap used to select Multiplexing of TFT signals at power-up. Enables using TFT instead of Parallel Port, ACB1, and GPIO17. During system reset, an internal pull-down resistor of 100 KΩ exists on this pin. If needed, an external pull-up resistor of 15 KΩ should be placed.	

1.1.6 ACCESS.bus Interface

Name	Type	Description	
AB1C	I/O	**ACCESS.bus 1 Serial Clock.** This is the serial clock for the interface.	
AB1D	I/O	**ACCESS.bus 1 Serial Data.** This is the bidirectional serial data signal for the interface.	
AB2C	I/O	**ACCESS.bus 2 Serial Clock.** This is the serial clock for the interface.	
AB2D	I/O	**ACCESS.bus 2 Serial Data.** This is the bidirectional serial data signal for the interface.	

1.1.7 PCI Bus Interface

Name	Type	Description	
PCICLK	I	**PCI Clock.** PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge.	
PCICLK0, PCICLK1	O	**PCI Clock Output.** PCICLK0 and PCICLK1 provide clock drives for the system at 33 MHz. These clocks are asynchronous to PCI signals. There is low skew between all outputs. One of these clock signals should be connected to PCICLK input. All PCI clock users in the system (including PCICLK) should receive the clock with as low a skew as possible.	
AD[31:0]	I/O	**Multiplexed Address and Data.** A bus transaction consists of an address phase in the cycle in which $\overline{\text{FRAME}}$ is asserted followed by one or more data phases. During the address phase, AD[31:0] contain a physical 32-bit address. For I/O, this is a byte address. For configuration and memory, it is a DWORD address. During data phases, AD[7:0] contain the least significant byte (LSB) and AD[31:24] contain the most significant byte (MSB).	
$\overline{\text{C/BE[3:0]}}$	I/O	**Multiplexed Command and Byte Enables.** During the address phase of a transaction when $\overline{\text{FRAME}}$ is active, $\overline{\text{C/BE[3:0]}}$ define the bus command. During the data phase, $\overline{\text{C/BE[3:0]}}$ are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data. $\overline{\text{C/BE0}}$ applies to byte 0 (LSB) and $\overline{\text{C/BE3}}$ applies to byte 3 (MSB).	
$\overline{\text{INTA}}$, $\overline{\text{INTB}}$, $\overline{\text{INTC}}$, $\overline{\text{INTD}}$	I	**PCI Interrupt.** The SC3200 provides inputs for the optional "level-sensitive" PCI interrupts (also known in industry terms as $\overline{\text{PIRQx}}$). These interrupts can be mapped to IRQs of the internal 8259 interrupt controllers using PCI Interrupt Steering Registers 1 and 2 (F0 Index 5Ch and 5Dh).	
PAR	I/O	**Parity.** Parity generation is required by all PCI agents. The master drives PAR for address- and write-data phases. The target drives PAR for read-data phases. Parity is even across AD[31:0] and $\overline{\text{C/BE[3:0]}}$. For address phases, PAR is stable and valid one PCI clock after the address phase. It has the same timing as AD[31:0] but is delayed by one PCI clock. For data phases, PAR is stable and valid one PCI clock after either $\overline{\text{IRDY}}$ is asserted on a write transaction or after $\overline{\text{TRDY}}$ is asserted on a read transaction. Once PAR is valid, it remains valid until one PCI clock after the completion of the data phase. (Also see $\overline{\text{PERR}}$.)	
$\overline{\text{FRAME}}$	I/O	**Frame Cycle.** Frame is driven by the current master to indicate the beginning and duration of an access. $\overline{\text{FRAME}}$ is asserted to indicate the beginning of a bus transaction. While $\overline{\text{FRAME}}$ is asserted, data transfers continue. $\overline{\text{FRAME}}$ is deasserted when the transaction is in the final data phase. This pin is internally connected to a pull-up resistor.	
$\overline{\text{IRDY}}$	I/O	**Initiator Ready.** $\overline{\text{IRDY}}$ is asserted to indicate that the bus master is able to complete the current data phase of the transaction. $\overline{\text{IRDY}}$ is used in conjunction with $\overline{\text{TRDY}}$. A data phase is completed on any PCI clock in which both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are sampled as asserted. During a write, $\overline{\text{IRDY}}$ indicates that valid data is present on AD[31:0]. During a read, it indicates that the master is prepared to accept data. Wait cycles are inserted until both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted together. This pin is internally connected to a pull-up resistor.	

Name	Type	Description	
TRDY	I/O	**Target Ready.** TRDY is asserted to indicate that the target agent is able to complete the current data phase of the transaction. TRDY is used in conjunction with IRDY. A data phase is complete on any PCI clock in which both TRDY and IRDY are sampled as asserted. During a read, TRDY indicates that valid data is present on AD[31:0]. During a write, it indicates that the target is prepared to accept data. Wait cycles are inserted until both IRDY and TRDY are asserted together. This pin is internally connected to a pull-up resistor.	
STOP	I/O	**Target Stop.** STOP is asserted to indicate that the current target is requesting that the master stop the current transaction. This signal is used with DEVSEL to indicate retry, disconnect, or target abort. If STOP is sampled active by the master, FRAME is deasserted and the cycle is stopped within three PCI clock cycles. As an input, STOP can be asserted in the following cases: 1) If a PCI master tries to access memory that has been locked by another master. This condition is detected if FRAME and LOCK are asserted during an address phase. 2) If the PCI write buffers are full or if a previously buffered cycle has not completed. 3) On read cycles that cross cache line boundaries. This is conditional based upon the programming of bit 1 in PCI Control Function 2 Register. This pin is internally connected to a pull-up resistor.	
LOCK	I/O	**Lock Operation.** LOCK indicates an atomic operation that may require multiple transactions to complete. When LOCK is asserted, nonexclusive transactions may proceed to an address that is not currently locked (at least 16 bytes must be locked). A grant to start a transaction on PCI does not guarantee control of LOCK. Control of LOCK is obtained under its own protocol in conjunction with GNT. It is possible for different agents to use PCI while a single master retains ownership of LOCK. The arbiter can implement a complete system lock. In this mode, if LOCK is active, no other master can gain access to the system until the LOCK is deasserted. This signal is internally connected to a pull-up resistor.	
DEVSEL	I/O	**Device Select.** DEVSEL indicates that the driving device has decoded its address as the target of the current access. As an input, DEVSEL indicates whether any device on the bus has been selected. DEVSEL is also driven by any agent that has the ability to accept cycles on a subtractive decode basis. As a master, if no DEVSEL is detected within and up to the subtractive decode clock, a master abort cycle will be initiated (except for special cycles which do not expect a DEVSEL returned). This signal is internally connected to a pull-up resistor.	
PERR	I/O	**Parity Error.** PERR is used for reporting data parity errors during all PCI transactions except a Special Cycle. The PERR line is driven two PCI clocks after the data in which the error was detected. This is one PCI clock after the PAR that is attached to the data. The minimum duration of PERR is one PCI clock for each data phase in which a data parity error is detected. PERR must be driven high for one PCI clock before being placed in TRISTATE. A target asserts PERR on write cycles if it has claimed the cycle with DEVSEL. The master asserts PERR on read cycles. This signal is internally connected to a pull-up resistor.	

Name	Type	Description	
$\overline{SERR}$	I/O	**System Error.** $\overline{SERR}$ can be asserted by any agent for reporting errors other than PCI parity, so that the PCI central agent notifies the processor. When the Parity Enable bit is set in the Memory Controller Configuration register, $\overline{SERR}$ is asserted upon detection of a parity error in read operations from DRAM.	
$\overline{REQ[1:0]}$	I	**Request Lines.** $\overline{REQ[1:0]}$ indicate to the arbiter that an agent requires the bus. Each master has its own $\overline{REQ}$ line. $\overline{REQ}$ priorities are based on the specified arbitration scheme. Each of these pins is internally connected to a pull-up resistor.	
$\overline{GNT[1:0]}$	O	**Grant Lines.** $\overline{GNT[1:0]}$ indicate to the requesting master that it has been granted access to the bus. Each master has its own $\overline{GNT}$ line. $\overline{GNT}$ can be retracted at any time a higher $\overline{REQ}$ is received or if the master does not begin a cycle within a minimum period of time (16 PCI clocks). These signals must be connected to a 15 KΩ pull-up resistor.	

1.1.8 Sub-ISA Interface

Name	Type	Description	
A[23:0]	O	**Address Lines**	
D[15:0]	I/O	**Data Bus**	
$\overline{BHE}$	O	**Byte High Enable.** With A0, defines byte accessed for 16-bit wide bus cycles.	
$\overline{IOCS[1:0]}$	O	**I/O Chip Selects**	
$\overline{ROMCS}$	O	**ROM or Flash ROM Chip Select**	
$\overline{DOCCS}$	O	**DiskOnChip or NAND Flash Chip Select**	
$\overline{TRDE}$	O	**Transceiver Data Enable Control.** Active low for Sub-ISA data transfers.	
$\overline{RD}$	O	**Memory or I/O Read.** Active on any read cycle.	
$\overline{WR}$	O	**Memory or I/O Write.** Active on any write cycle.	
$\overline{IOR}$	O	**I/O Read.** Active on any I/O read cycle.	
$\overline{IOW}$	O	**I/O Write.** Active on any I/O write cycle.	
$\overline{DOCR}$	O	**DiskOnChip or NAND Flash Read.** Active on any memory read cycle to DiskOnChip.	
$\overline{DOCW}$	O	**DiskOnChip or NAND Flash Write.** Active on any memory write cycle to DiskOnChip.	
IRQ9	I	**Interrupt 9 Request Input.** Active High.	
IOCHRDY	I	**I/O Channel Ready**	

1.1.9 Low Pin Count (LPC) Bus Interface

Name	Type	Description	
LAD[3:0]	I/O	**LPC Address-Data.** Multiplexed command, address, bidirectional data, and cycle status.	
$\overline{\text{LDRQ}}$	I	**LPC DMA Request.** Encoded DMA request for LPC I/F.	
$\overline{\text{LFRAME}}$	O	**LPC Frame.** A low pulse indicates the beginning of a new LPC cycle or termination of a broken cycle.	
$\overline{\text{LPCPD}}$	O	**LPC Power-Down.** Signals the LPC device to prepare for power shut-down on the LPC interface.	
SERIRQ	I/O	**Serial IRQ.** The interrupt requests are serialized over a single pin, where each IRQ level is delivered during a designated time slot.	

1.1.10 IDE Interface

Name	Type	Description	
$\overline{\text{IDE\_RST}}$	O	**IDE Reset.** This signal resets all the devices that are attached to the IDE interface.	
IDE_ADDR[2:0]	O	**IDE Address Bits.** These address bits are used to access a register or data port in a device on the IDE bus.	
IDE_DATA[15:0]	I/O	**IDE Data Lines.** IDE_DATA[15:0] transfers data to/from the IDE devices.	
$\overline{\text{IDE\_IOR0}}$, $\overline{\text{IDE\_IOR1}}$	O	**IDE I/O Read Channels 0 and 1.** $\overline{\text{IDE\_IOR0}}$ is the read signal for Channel 0 and $\overline{\text{IDE\_IOR1}}$ is the read signal for Channel 1. Each signal is asserted at read accesses to the corresponding IDE port addresses.	
$\overline{\text{IDE\_IOW0}}$, $\overline{\text{IDE\_IOW1}}$	O	**IDE I/O Write Channels 0 and 1.** $\overline{\text{IDE\_IOW0}}$ is the write signal for Channel 0. $\overline{\text{IDE\_IOW1}}$ is the write signal for Channel 1. Each signal is asserted at write accesses to corresponding IDE port addresses.	
$\overline{\text{IDE\_CS0}}$, $\overline{\text{IDE\_CS1}}$	O	**IDE Chip Selects 0 and 1.** These signals are used to select the command block registers in an IDE device.	
IDE_IORDY0, IDE_IORDY1	I	**I/O Ready Channels 0 and 1.** When deasserted, these signals extend the transfer cycle of any host register access if the required device is not ready to respond to the data transfer request.	
IDE_DREQ0, IDE_DREQ1	I	**DMA Request Channels 0 and 1.** The IDE_DREQ signals are used to request a DMA transfer from the SC3200. The direction of transfer is determined by the $\overline{\text{IDE\_IOR/IOW}}$ signals.	
$\overline{\text{IDE\_DACK0}}$, $\overline{\text{IDE\_DACK1}}$	O	**DMA Acknowledge Channels 0 and 1.** The $\overline{\text{IDE\_DACK}}$ signals acknowledge the DREQ request to initiate DMA transfers.	
IRQ14, IRQ15	I	**Interrupt Request Channels 0 and 1.** These input signals are edge-sensitive interrupts that indicate when the IDE device is requesting a CPU interrupt service.	

1.0 Signal Definitions (Continued)

1.1.11 Universal Serial Bus (USB)

Name	Type	Description	
POWER_EN	O	**Power Enable.** This pin enables the power to a self-powered USB hub.	
$\overline{\text{OVER\_CUR}}$	I	**Overcurrent.** This pin indicates that the USB hub has detected an overcurrent on the USB.	
D+_PORT1	I/O	**USB Port 1 Data Positive.** This pin is the Universal Serial Bus Data Positive for port 1.	
D−_PORT1	I/O	**USB Port 1 Data Negative.** This pin is the Universal Serial Bus Data Negative for port 1.	
D+_PORT2	I/O	**USB Port 2 Data Positive.** This pin is the Universal Serial Bus Data Positive for port 2.	
D−_PORT2	I/O	**USB Port 2 Data Negative.** This pin is the Universal Serial Bus Data Negative for port 2.	
D+_PORT3	I/O	**USB Port 3 Data Positive.** This pin is the Universal Serial Bus Data Positive for port 3.	
D−_PORT3	I/O	**USB Port 3 Data Negative.** This pin is the Universal Serial Bus Data Negative for port 3.	

1.1.12 Serial Ports (UARTs)

Name	Type	Description	
SIN1 SIN2 SIN3	I	**Serial Input.** Receive composite serial data from the communications link (peripheral device, modem or other data transfer device).	
SOUT1 SOUT2 SOUT3	O	**Serial Output.** Send composite serial data to the communications link (peripheral device, modem or other data transfer device). These signals are set active high after a system reset.	
$\overline{\text{RTS2}}$	O	**Request to Send.** When low, indicate to the modem or other data transfer device that the corresponding UART is ready to exchange data. A system reset sets these signals to inactive high, and loopback operation holds them inactive.	
$\overline{\text{CTS2}}$	I	**Clear to Send.** When low, indicate that the modem or other data transfer device is ready to exchange data.	
$\overline{\text{DTR1}}$/ BOUT1 $\overline{\text{DTR2}}$/ BOUT2	O	**Data Terminal Ready (DTRx).** When low, indicate to the modem or other data transfer device that the UART is ready to establish a communications link. After a system reset, these pins provide the $\overline{\text{DTR}}$ function and set these signals to inactive high. Loopback operation drives them inactive. **Baud Output (BOUTx).** Provides the associated serial channel baud rate generator output signal if test mode is selected, i.e., bit 7 of the EXCR1 Register is set.	
$\overline{\text{RI2}}$	I	**Ring Indicator.** When low, indicates to the modem that a telephone ring signal has been received by the modem. They are monitored during power-off for wake-up event detection.	
$\overline{\text{DCD2}}$	I	**Data Carrier Detected.** When low, indicates that the data transfer device, e.g., modem, is ready to establish a communications link.	
$\overline{\text{DSR2}}$	I	**Data SetReady.** When low, indicates that the data transfer device, e.g., modem, is ready to establish a communications link.	

1.1.13 Parallel Port

Signal	I/O	Description	MUX
$\overline{\text{ACK}}$	I	**Acknowledge.** Pulsed low by the printer to indicate that it has received data from the Parallel Port.	
$\overline{\text{AFD}}$/$\overline{\text{DSTRB}}$	O	**AFD - Automatic Feed.** When low, instructs the printer to automatically feed a line after printing each line. This pin is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be attached to this pin. **DSTRB - Data Strobe (EPP).** Active low, used in EPP mode to denote a data cycle. When the cycle is aborted, $\overline{\text{DSTRB}}$ becomes inactive (high).	
BUSY/$\overline{\text{WAIT}}$	I	**BUSY.** Set high by the printer when it cannot accept another character. **$\overline{\text{WAIT}}$.** In EPP mode, the Parallel Port device uses this active low signal to extend its access cycle.	
$\overline{\text{ERR}}$	I	**Error.** Set active low by the printer when it detects an error.	
$\overline{\text{INIT}}$	O	**Initialize.** When low, initializes the printer. This signal is in TRI-STATE after a 1 is loaded into the corresponding control register bit. Use an external 4.7 KΩ pull-up resistor.	
PD[7:0]	I/O	**Parallel Port Data.** Transfer data to and from the peripheral data bus and the appropriate Parallel Port data register. These signals have a high current drive capability.	
PE	I	**Paper End.** Set high by the printer when it is out of paper. This pin has an internal weak pull-up or pull-down resistor.	
SLCT	I	**Select.** Set active high by the printer when the printer is selected.	
$\overline{\text{SLIN}}$/$\overline{\text{ASTRB}}$	O	**$\overline{\text{SLIN}}$ - Select Input.** When low, selects the printer. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. Uses an external 4.7 KΩ pull-up resistor. **$\overline{\text{ASTRB}}$ - Address Strobe (EPP).** Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, $\overline{\text{ASTRB}}$ becomes inactive (high).	
$\overline{\text{STB}}$/$\overline{\text{WRITE}}$	O	**$\overline{\text{STB}}$ - Data Strobe.** When low, Indicates to the printer that valid data is available at the printer port. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be employed. **$\overline{\text{WRITE}}$ - Write Strobe.** Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, $\overline{\text{WRITE}}$ becomes inactive (high).	

1.1.14 Fast Infrared (IR) Port

Name	Type	Description	
IRRX1	I	**IR Receive.** Primary input to receive serial data from the IR transceiver. Monitored during power-off for wake-up event detection.	
IRRX2	I	**IRRX2 - IR Receive 2**. Auxiliary IR receiver input to support a second transceiver. This input signal can be used when GPIO38 is selected using PMR[14], and when AUX_IRRX bit in register IRCR2 of the IR module in internal SuperI/O is set.	
IRTX	O	**IR Transmit.** IR serial output data.	

1.1.15 AC97 Audio Interface

Name	Type	Description	
BIT_CLK	I	**Audio Bit Clock.** The serial bit clock from the codec.	
SDATA_OUT	O	**Serial Data Output.** This output transmits audio serial data to the codec.	
SDATA_IN	I	**Serial Data Input.** This input receives serial data from the primary codec.	
SDATA_IN2	I	**Serial Data Input 2.** This input receives serial data from the secondary codec. This pin has wake-up capability.	
SYNC	O	**Serial Bus Synchronization.** This bit is asserted to synchronize the transfer of data between the SC3200 and the AC97 codec.	
AC97_CLK	O	**Codec Clock.** It is twice the frequency of the Audio Bit Clock.	
$\overline{\text{AC97\_RST}}$	O	**Codec Reset**	
PC_BEEP	O	**PC Beep.** Legacy PC/AT speaker output.	

1.1.16 Power Management

Name	Type	Description	
CLK32	O	**32.768 KHz Output Clock**	
GPWIO[0:2]	I/O	**General Purpose Wake-up I/O Signals**	
$\overline{\text{LED}}$	O	**LED Control.** Drives an externally connected LED (on, off or a 1 Hz blink). Sleeping / Working indicator. This signal is an open-drain output.	
$\overline{\text{ONCTL}}$	O	**On / Off Control.** This signal indicates to the main power supply that power should be turned on. This signal is an open-drain output.	
$\overline{\text{PWRBTN}}$	I	**Power Button.** Input used by the power management logic to monitor external system events, most typically a system on/off button or switch. The pin has an internal pull-up of 100 KΩ, a schmitt-trigger input buffer and debounce protection of at least 16 msec.	
PWRCNT[1:2]	O	**Suspend Power Plane Control 1 and 2.** Control signal asserted during power management suspend states. These signals are open-drain outputs.	
$\overline{\text{THRM}}$	I	**Thermal Event.** Active low signal generated by external hardware indicating that the system temperature is too high.	

1.1.17 General Purpose (GPIO) Ports

Name	Type	Description	
GPIO[00:01], and [06:20]	I/O	**GPIO Port 0**. Each signal is configured independently as input or I/O, with or without static pull-up, and with either open-drain or totem-pole output type. A debouncer and an interrupt can be enabled or masked for each of signals GPIO[00:01] and [06:15] independently.	
GPIO[32:41]	I/O	**GPIO Port 1.** Same as Port 0. A debouncer and an interrupt can be enabled or masked for each of signals GPIO[32:41] independently.	

1.1.18 JTAG

Name	Type	Description	
TCK	I	**Test Clock**	
TDI	I	**Test Data Input**	
TDO	O	**Test Data Output**	
TMS	I	**Test Mode Select**	
$\overline{\text{TRST}}$	I	**Test Reset.** This pin has an internal weak pull-up resistor. • For normal JTAG operation, this signal should be active at power-up. • If the JTAG interface is not being used, this signal can be tied low.	

1.1.19 Test and Measurement

Name	Type	Description	
FMUL3B	I/O	For internal test only.	
PLL2B	I/O	**PLL2 bypass input.** Graphics dot clock generator	
GXCLK	O	For internal test only.	
PLL5B	I/O	**PLL5 bypass input.** For internal test only.	
GTEST	I	For internal test only.	
TDP, TDN	I/O	**Thermal Diode.** For test only.	

1.1.20 Power and Ground

Note: All power sources must be connected to the SC3200, even if the function is not used.

Name	Type	Description
AV_{SSPLL2}	GND	**Analog PLL2 Ground Connection**
AV_{SSPLL3}	GND	**Analog PLL3 Ground Connection**
AV_{CCUSB}	PWR	**3.3V Analog USB Power Connection.** Low noise power
AV_{SSUSB}	GND	**Analog USB Ground Connection**
AV_{CC}	PWR	**3.3V Analog Power Connection**.
AV_{SS}	GND	**Analog Ground Connection.**
V_{BAT}		**Battery.** Provides battery back-up to the Real-Time Clock (RTC) and ACPI registers. The ball is connected to the internal logic through a series resistor for UL protection.
V_{CORE}	PWR	**1.8V or 2.0V Core processor Power Connection**
V_{IO}	PWR	**3.3V I/O Power Connection**
V_{PLL2}	PWR	**3.3V PLL2 Analog Power Connection**. Low noise power
V_{PLL3}	PWR	**3.3V PLL3 Analog Power Connection.** Low noise power
V_{SB}	PWR	**3.3V Standby Power Supply.** Provides power to the Real-Time Clock (RTC) and ACPI circuitry while the main power supply is turned off.
V_{SBL}	PWR	**1.8 V or 2.0V Standby Power Supply.** Provides power to the internal logic while the main power supply is turned off. This pin requires a 0.1 µF bypass capacitor to V_{SS}.
V_{SS}	GND	**Ground Connection**

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