Z86318

Z8® MCU 8-BIT MICROCONTROLLER

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86318	124	14	21	0V to 6.0V

Note: *General-Purpose

- –40°C to +105°C Operating Temperature Range
- Low-Power Consumption: 33 mW (Typical)
- ROM Mask Options:
  - Permanent Watch-Dog Timer
  - ROM Protect
  - Low-Voltage Protection
  - Pull-Up/Pull-Down I/O Pins (Nibble Programmable)
  - Feedback Resistor on the On-Chip Oscillator
- On-Chip Oscillator (Crystal, Ceramic Resonator, LC, or External Clock Drive)
- Fast Instruction Pointer: 1.5 µs @ 4 MHz
- ESD Protection Circuitry

GENERAL DESCRIPTION

The Z86318 is a member of the Z8® MCU family of CMOS microcontrollers. This device offers on-board pull-up and pull-down resistors (ROM mask-option programmable on a nibble basis), a scalable trip-point buffer to accommodate opto-transistor outputs, and high drive ports capable of up to 20 mA current sinking per pin (3 pins maximum).

The Z86318 features I/O Ports (IOL = 20 mA at VOL = 0.8V, 3 pins max.) to provide increased current sinking capabilities. These devices also offer users a selection of ROM mask options, which include a permanently enabled Watch-Dog Timer that ensures operational reliability across a broad range of application environments.

For applications requiring powerful I/O capabilities, the Z86318 provides dedicated input and output lines that are grouped into three ports. These ports can be configured by means of ROM mask options (nibble-programmable) as pull ups, pull downs, or neither. There are two basic address spaces available. Program Memory, and 124 bytes of general-purpose registers.

The Z86318 devices provide two on-chip 8-bit programmable counter/timers with a large number of user-selectable modes. Each counter/timer is driven by its own 6-bit programmable prescaler. The Z86318 counter/timers off-load system real-time tasks such as counting/timing and input/output data communications for increased system efficiency.

Notes: All Signals with a preceding front slash, "/", are active Low, e.g.; B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	VCC	VDD
Ground	GND	VSS

GENERAL DESCRIPTION (Continued)

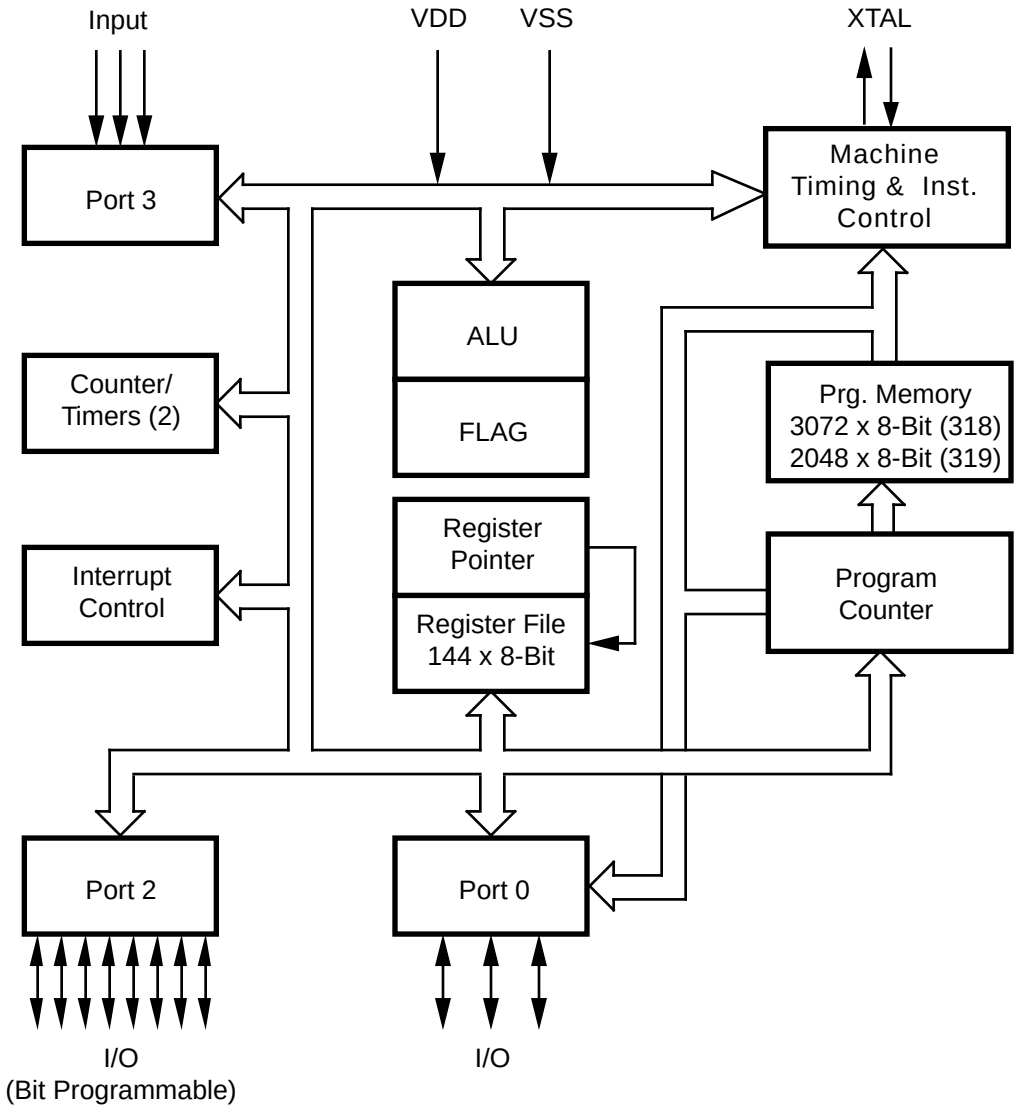


Figure 1. Z86318 Functional Block Diagram

PIN DESCRIPTIONS

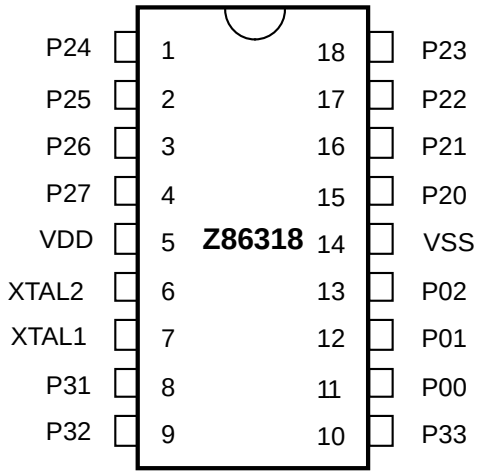


Figure 2. Z86318 18-Pin DIP/SOIC Pin Configuration

Table 1. Z86318 18 Pin DIP/SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{DD}	Power Supply	Input
6	XTAL2	XTAL Osc. Clock	Output
7	XTAL1	XTAL Osc. Clock	Input
8	P31	Port 3, Pin 1	Input
9	P32	Port 3, Pin 2	Input
10	P33	Port 3, Pin 3	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	V_{SS}	Ground	
15-18	P20-P23	Port 2, Pins 0, 1, 2, 3	In/Output

ABSOLUTE MAXIMUM RATINGS

Sym.	Parameter	Min.	Max.	Units
V_{DD}	Supply Voltage*	–0.3	+7	V
T_{STG}	Storage Temp.	–65°	+150°	C
T_A	Oper. Ambient Temp.	†	†	C

Note:
*Voltages on all pins with respect to Ground.
†See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground.Positive current flows into the referenced pin (Figure 3).

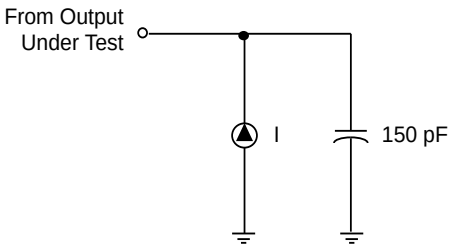


Figure 3. Test Load Diagram

CAPACITANCE

TA = GND = 0V, f = 1.0 MHz, unmeasured pins returned to Ground.

Parameter	Min.	Max.
Input Capacitance	0	10 pF
Output Capacitance	0	20 pF
I/O Capacitance	0	25 pF

V_{CC} SPECIFICATION

V_{CC} = 4.0V to 6.0V

DC ELECTRICAL CHARACTERISTICS

			T_A= 0°C to +70°C		Typical		
Sym	**Parameter**	**V_{DD}**	**Min**	**Max**	**@ 25°C**	**Units**	**Conditions**
	Max Input Voltage	4.0V		12		V	V_{IN} < 250 µA (Port Pins Only)
V_{CH}	Clock Input High Voltage	4.0V	0.7 V_{DD}	V_{DD} + 0.3	2.0	V	Driven by External Clock Generator
		6.0V	0.7 V_{DD}	V_{DD} + 0.3	3.0	V	
V_{CL}	Clock Input Low Voltage	4.0V	V_{SS} – 0.3	0.2 V_{DD}	0.8	V	Driven by External Clock Generator
		6.0V	V_{SS} – 0.3	0.2 V_{DD}	1.5	V	
V_{IH}	Input High Voltage Schmitt-Triggered	4.0V	0.7 V_{DD}	V_{DD} + 0.3	1.6	V	
		6.0V	0.7 V_{DD}	V_{DD} + 0.3	2.6	V	
V_{IH}	Input High Voltage CMOS Input	4.0V	0.7 V_{DD}	V_{DD} + 0.3	1.4	V	
		6.0V	0.7 V_{DD}	V_{DD} + 0.3	2.6	V	
V_{IL}	Input Low Voltage Schmitt-Triggered	4.0V	V_{SS} – 0.3	0.2 V_{DD}	0.8	V	
		6.0V	V_{SS} – 0.3	0.2 V_{DD}	1.5	V	
V_{IL}	Input Low Voltage CMOS Input	4.0V	V_{SS} – 0.3	0.2 V_{DD}	1.3	V	
		6.0V	V_{SS} – 0.3	0.2 V_{DD}	2.4	V	
V_{OH}	Output High Voltage	4.0V	V_{DD} – 0.4		2.8	V	I_{OH} = –2.0 mA
		4.5V	V_{DD} – 0.4		4.4	V	
V_{OL1}	Output Low Voltage	4.0V		0.6	0.2	V	I_{OL} = +4.0 mA
		6.0V		0.4	0.1	V	
V_{OL2}	Output Low Voltage	4.0V		1.5	0.8	V	I_{OL} = 20.0 mA, 3 Pin Max
		6.0V		0.8	0.3	V	$_{OL}$ = 10.0 mA, 6 Pin Max
V_{LV}	VCC Low-Voltage Protection*		1.6	2.7	2.3	V	@ 2 MHz Max
V_{TP}	Trip-Point Voltage*	4.0V		0.4 V_{DD}		V	P24-P27
		4.5V	1.5	2.1	1.8	V	
		5.5V	1.9	2.5	2.2	V	
		6.0V	2.1	2.7	2.4	V	
V_{OC}	Input Open-Circuit Voltage	4.5V	0.95	1.15	1.04	V	No Off-Chip Resistance
		5.0V	1.05	1.25	1.15	V	
		5.5V	1.15	1.39	1.27	V	
		6.0V	1.25	1.49	1.37	V	
I_{IL}	Input Leakage	3.0V	–1.0	1.0	0.4	µA	V_{IN} = 0V, VCC
		5.5V	–1.0	1.0	0.4	µA	
		6.0V	–1.0	1.0	0.4	µA	
I_{OL}	Output Leakage	4.0V	–1.0	1.0	0.4	µA	V_{IN} = 0V, VCC
		5.5V	–1.0	1.0	0.4	µA	
		6.0V	–1.0	1.0	0.4	µA	

Note:
*The Z86318 is functional to V_{LV} voltage. The minimum operational V_{DD} is determined by the value of the V_{LV} voltage at ambient temperature. The V_{LV} voltage increases as temperature decreases.

DC ELECTRICAL CHARACTERISTICS (Continued)

			T_A= 0°C to +70°C		Typical			
Sym.	**Parameter**	**V_{DD}**	**Min.**	**Max.**	**@ 25°C**	**Units**	**Conditions**	**Notes**
I_{DD}	Supply Current	4.0V		1.5	0.41	mA	@ 1 MHz	[1]
		4.0V		2.0	0.93	mA	@ 2 MHz	[1]
		4.0V		3.0	1.64	mA	@ 4 MHz	[1]
		6.0V		3.0	1.44	mA	@ 1 MHz	[1]
		6.0V		4.0	2.60	mA	@ 2 MHz	[1]
		6.0V		6.0	4.28	mA	@ 4 MHz	[1]
I_{DD1}	Standby Current	4.0V		0.6	0.15	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz	
		4.0V		0.8	0.20	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	
		4.0V		1.0	0.3	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz	
		6.0V		1.3	0.70	mA	HALT mode V_{IN} = 0V, V_{CC} @ 1 MHz	
		6.0V		1.5	0.80	mA	HALT mode V_{IN} = 0V, V_{CC} @ 2 MHz	
		6.0V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 4 MHz	
I_{DD2}	Standby Current	6.0V		10	1.5	mA	STOP mode V_{IN} = 0V, V_{CC}	
I_{PU}	Pull-Up Current (100K) Port P00–P02; Port P22, P23; Port P31–P33	4.5V	-20			µA	V_{IH} @ 1V	
		6.0V		105			V_{IH} @ 1V	
I_{PD}	Pull-Down Current (100K) Port P00–P02; Port P22, P23; Port P31–P33	4.5V	20			µA	V_{IL} @ 3V	
		6.0V		114			V_{IL} @ 4V	
I_{PU}	Pull-Up Current (10K) Port P20, P21	4.5V	208			µA	V_{IH} @ 0V	
		6.0V		870			V_{IH} @ 0V	
I_{PD}	Pull-Down Current (10K) Port P20, P21	4.5V	170			µA	V_{IH} @ 3V	
		6.0V		870			V_{IH} @ 3V	

Note: [1] All outputs unloaded, I/O pins floating, inputs at rail.

AC ELECTRICAL CHARACTERISTICS

Timing Diagrams

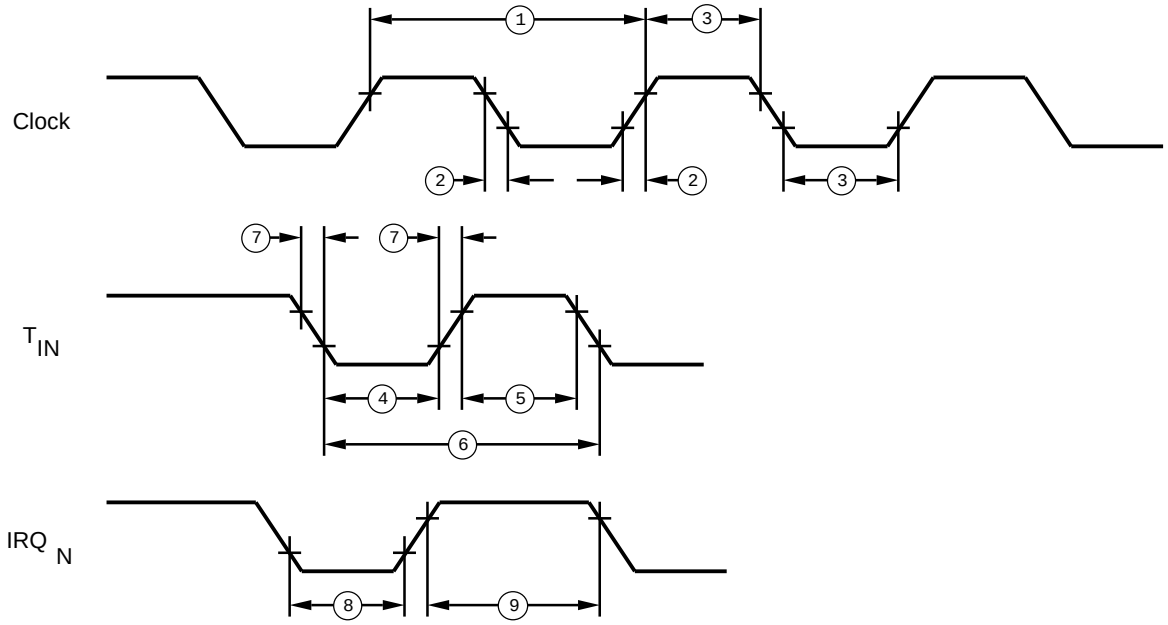


Figure 4. Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 4V to 6V ±10%, T_A = 0°C to +70°C, unless otherwise specified)

				T_A = 0°C to +70°C					
				1 MHz		4 MHz			
No.	**Symbol**	**Parameter**	**V_{DD}**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Notes**
1	TpC	Input Clock Period	6.0V	1,000	100,000	250	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	6.0V		25		25	ns	
3	TwC	Input Clock Width	6.0V		475		100	ns	[1]
4	TwTinL	Timer Input Low Width	6.0V		70		70	ns	[1]
5	TwTinH	Timer Input High Width	6.0V	2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	6.0V	4TpC		4TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	6.0V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	6.0V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	6.0V	2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer	6.0V	24		24		ms	
11	T_{POR}	Power-On Reset Time	6.0V	6		6		ms	[1]

Notes:

1. Timing Reference uses 0.9 VDD for a logic 1 and 0.1 VDD for a logic 0.
2. Interrupt request through Port 3 (P33-P31).

PIN FUNCTIONS

XTAL1, XTAL2. Crystal in, crystal out (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (4 MHz Max.) to the on-chip clock oscillator and buffer. **Note:** XTAL1 has a pull-down resistor.

Port 0 (P02-P00). Port 0 is a 3-bit, I/O programmable, bi-directional, CMOS-compatible I/O port. These three I/O lines can be configured under software control to be input or output (see Figure 5). When Port 0 is configured as an input port, all lines have the capability to be globally configured (ROM mask option) for a 100K pull-down or pull-up resistor. The pull-up/pull-down resistor can be disabled as well. (No current is drawn if disabled.) Graphs showing current versus pin voltage are shown in Figures 6 and 7.

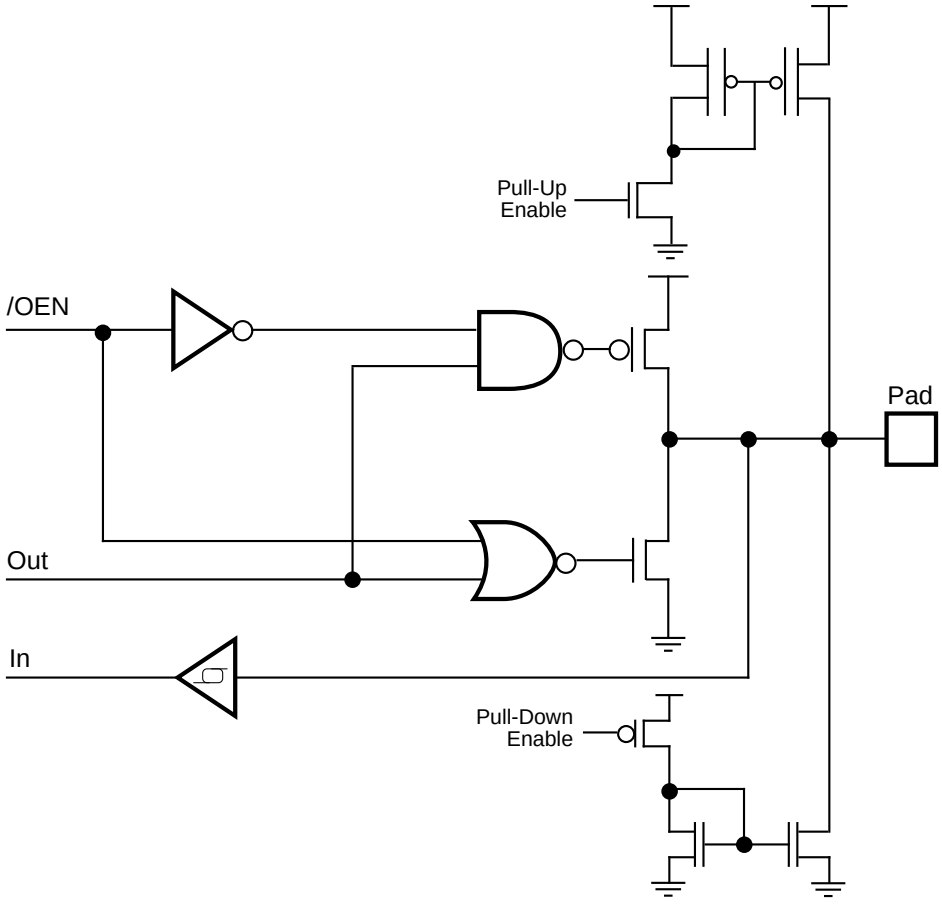


Figure 5. Port 0 Configuration

PIN FUNCTIONS (Continued)

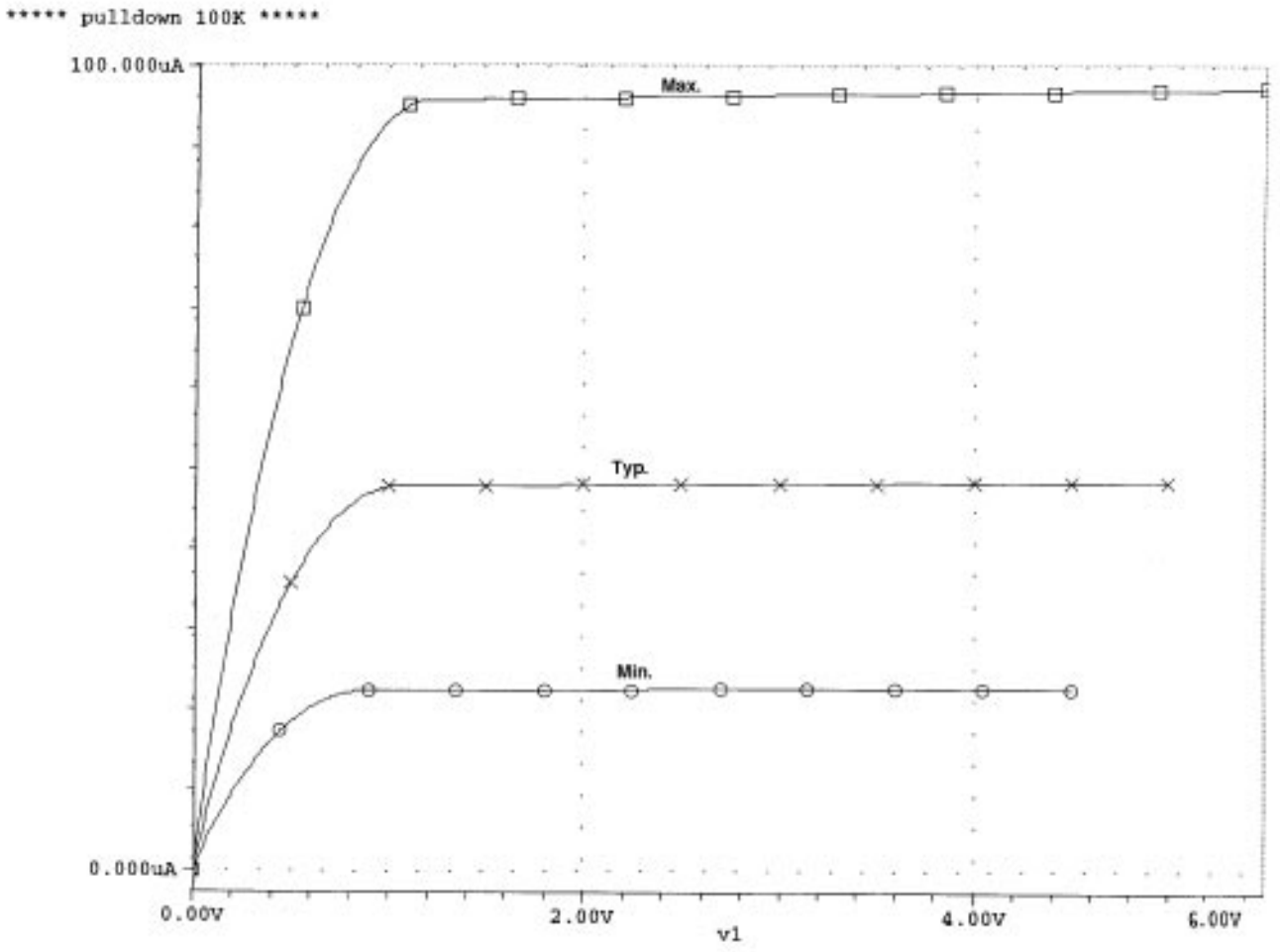


Figure 6. Typical Current Versus Pin Voltage Values

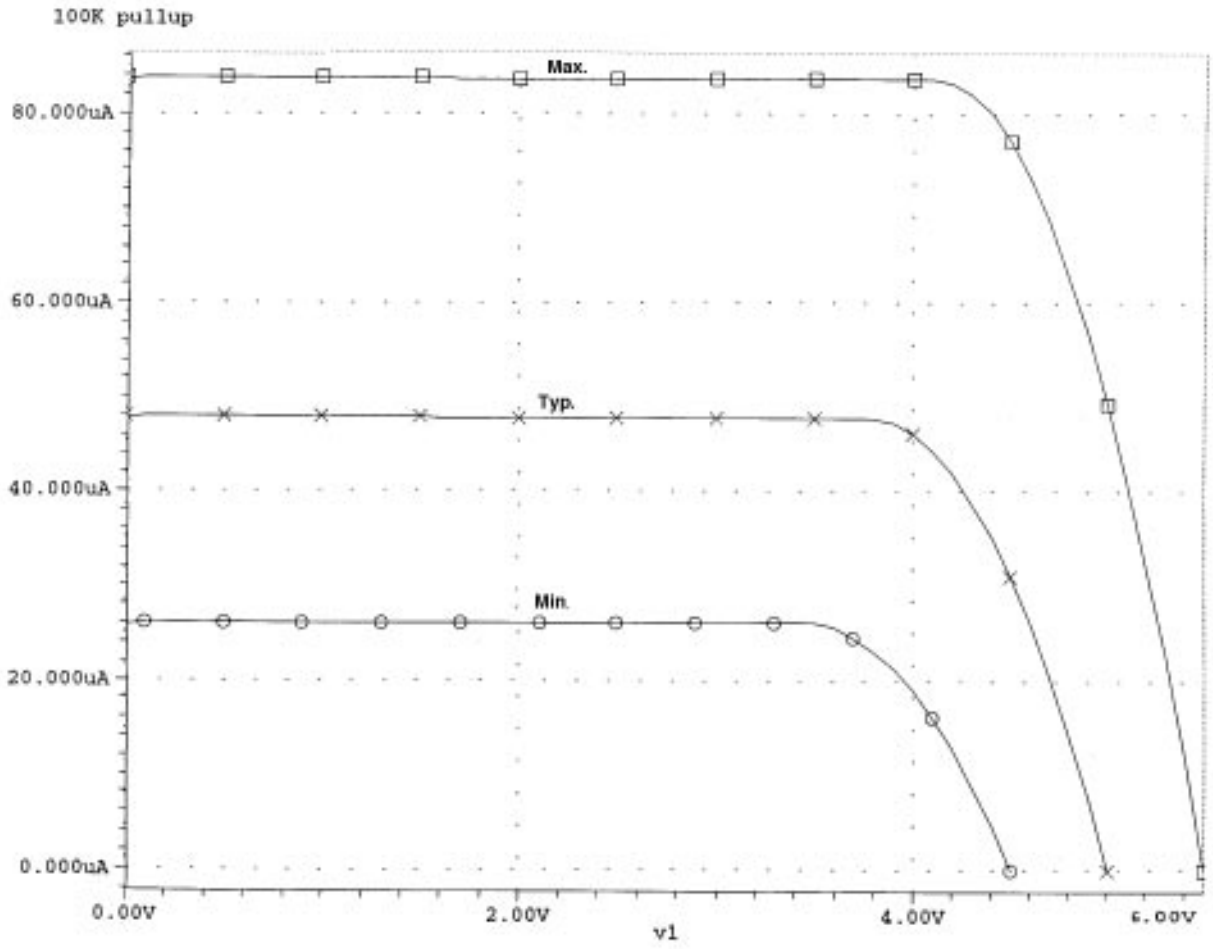


Figure 7. Typical Current Versus Pin Voltage Values

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, bit-programmable, bidirectional, CMOS-compatible I/O port. P23-P20 can be configured under software control to be input or output, independently. Note: Bits D3 and D4 of POIM register must be set to 0. Bits programmed as outputs may be globally programmed as either push-pull or open-drain via bit D0, P3M register. P20 and P21 can be configured with a ROM mask option for 10 Kohm pull-up/pull-down, or none. P22 and P23 can be configured with a ROM mask option for 100 Kohm pull-up/pull-down, or none (Figure 8). No current is drawn if pull-up/pull-down is disabled. **Note:** P23-20 are configured for pull-up/pull-down/none globally.

P24-P27 can be configured as a voltage divider. The voltage divider consists of an internal 25K pull-up resistor (Figure 9), and a 7.5K pull-down resistor. The zero trip-point input levels on P24-P27 are adjusted for connection to the emitters of opto-transistors and switch at a voltage level of 0.4 VDD. All four of the voltage dividers are globally configured as enabled or disabled.

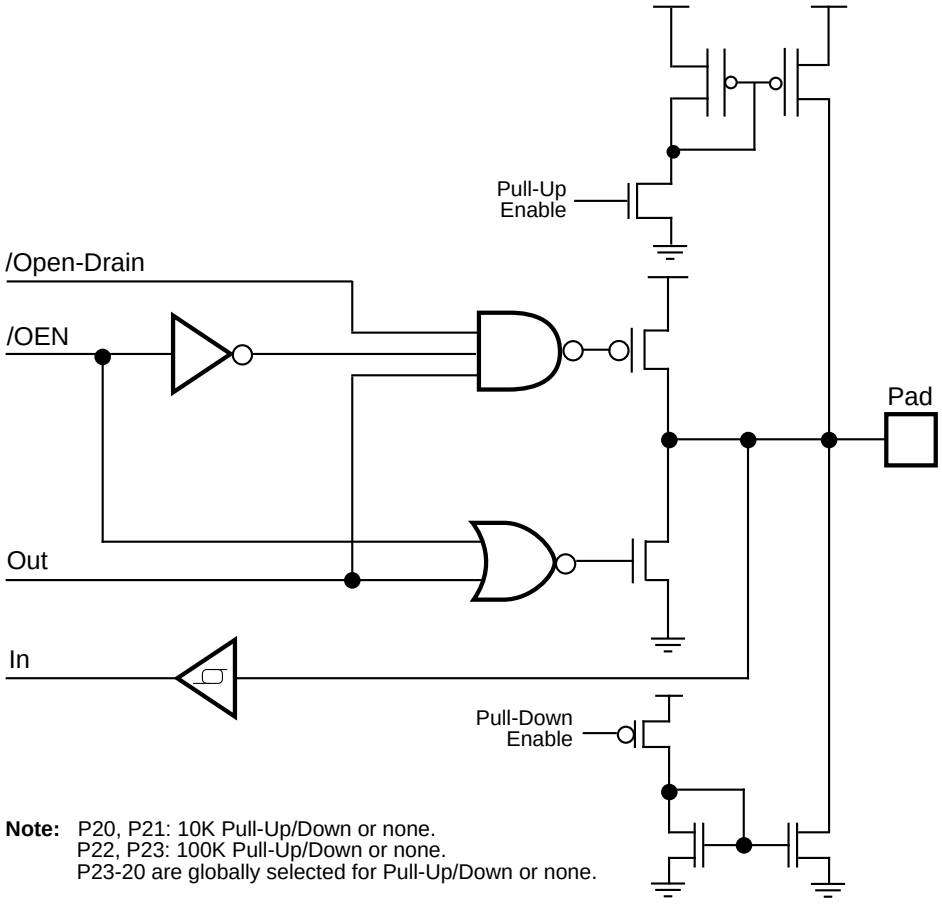


Figure 8. Port 2 P20-P23 Configuration

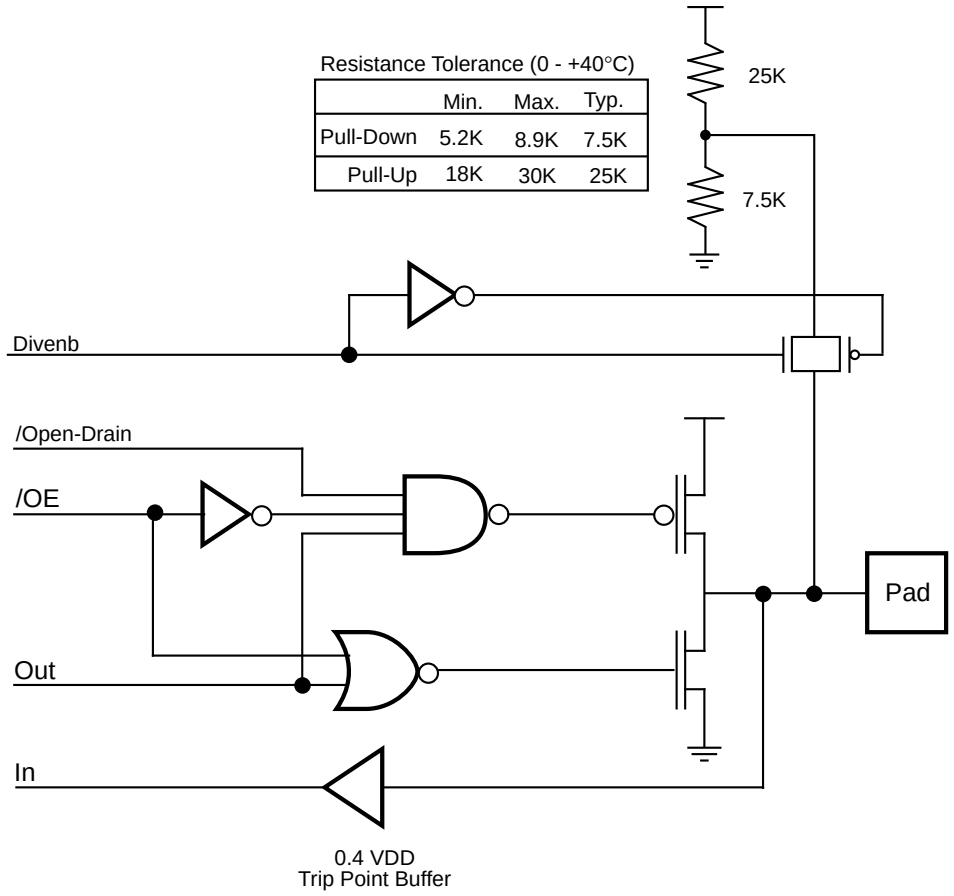


Figure 9. Port 2 P27-P24 Configuration

Port 3 (P33, P32, P31). Port 3 is a 3-bit, CMOS-compatible port with three fixed input lines (P33–P31). These three lines can also be used as the interrupt sources IRQ2, IRQ1, and IRQ0. P31 can also be configured as a timer input.

All three lines can be configured globally by means of ma ROM mask option for a 100 Kohm pull-up or pull-down resistor (Figure 10), or no pull-up/pull-down. No current is drawn if pull-up/pull-down is disabled.

PIN FUNCTIONS (Continued)

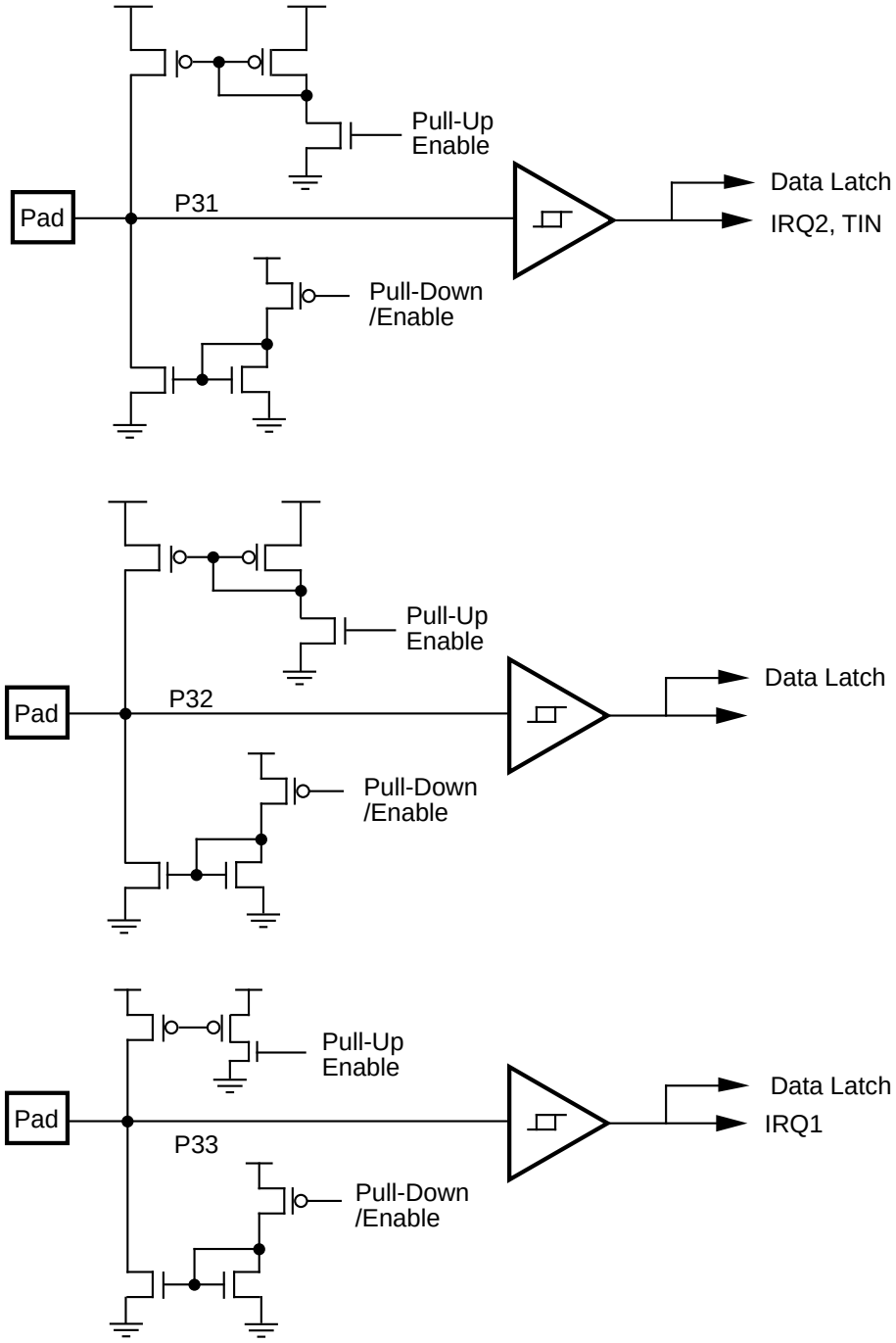


Figure 10. Port 3 P31-P33 Configuration

The Z86318 MCU incorporates the following special features to enhance the Z8® architectural core for use in mouse and trackball applications.

Reset. The Z86318 is reset in one of the following conditions: 1) Power-On Reset (POR), 2) Watch-Dog Timer (WDT) Mode, 3) Stop-Mode Recovery source, and 4) Low-Voltage Recovery. Other sources of Reset, ports are configured in an input mode, asynchronous of the clock. However, a clock is required to generate the internal reset that resets the internal registers.

Auto POR circuitry is built into the Z86318, eliminating the need for an external reset circuit to reset on power-on.

Table 2. Z86318 Control Registers

		Reset Values								
Addr.	**Reg.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F7*	P3M	U	U	U	U	U	U	1	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	
FB	IMR	0	U	U	U	U	U	U	U	
FC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	U	U	U	U	U	U	U	U	
FF	SPL	U	U	U	U	U	U	U	U	

Notes: *
A reset after a Low on P27 to exit STOP mode may affect device reliability.

Program Memory. The Z86318 device can address up to 3 KB of internal program memory (Figure 11). The first 12 bytes of Program Memory are reserved for the interrupt vectors. These locations contain four 16-bit vectors that correspond to the four available interrupts. Bytes 0-3064 are programmed on-chip by means of a ROM mask option.

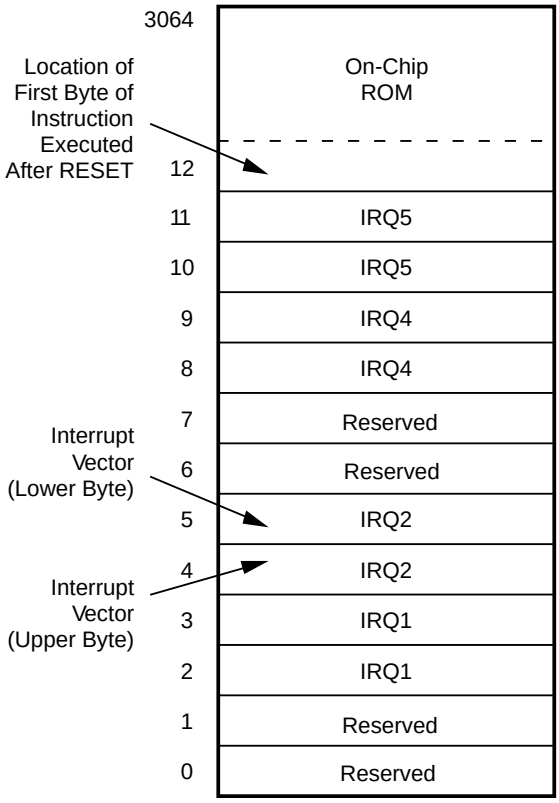


Figure 11. Program Memory Map

FUNCTIONAL DESCRIPTION

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 15 control and status registers, R0-R3, R4-R127 and R241-R255, respectively (see Figure 12). The Z86318 instructions can access registers directly or indirectly via an 8-bit address field. This allows short, 4-bit register addressing using the Register Pointer.

In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group (Figures 13 and 14).

LOCATION		IDENTIFIERS
R255	Stack Pointer (Bits 7-0)	SPL
R254	General-Purpose	GPR
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Ports 0-1 Mode	P01M
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PRE0
R244	Timer/Counter0	T0
R243	T1 Prescaler	PRE1
R242	Timer/Counter1	T1
R241	Timer Mode	TMR
R128	Not Implemented	
R127	General-Purpose Registers	
R4		
R3	Port 3	P3
R2	Port 2	P2
R1	Reserved	
R0	Port 0	P0

Figure 12. Register File

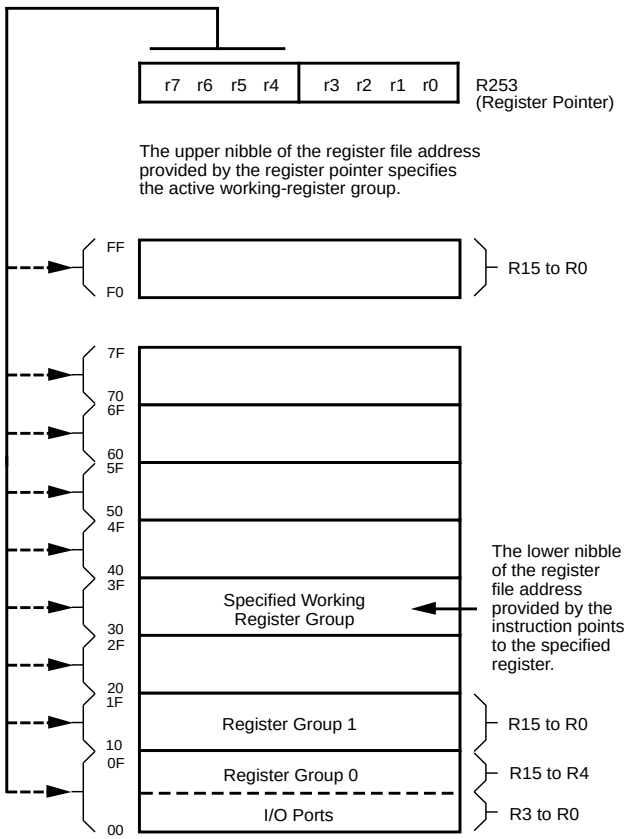


Figure 13. Register Pointer

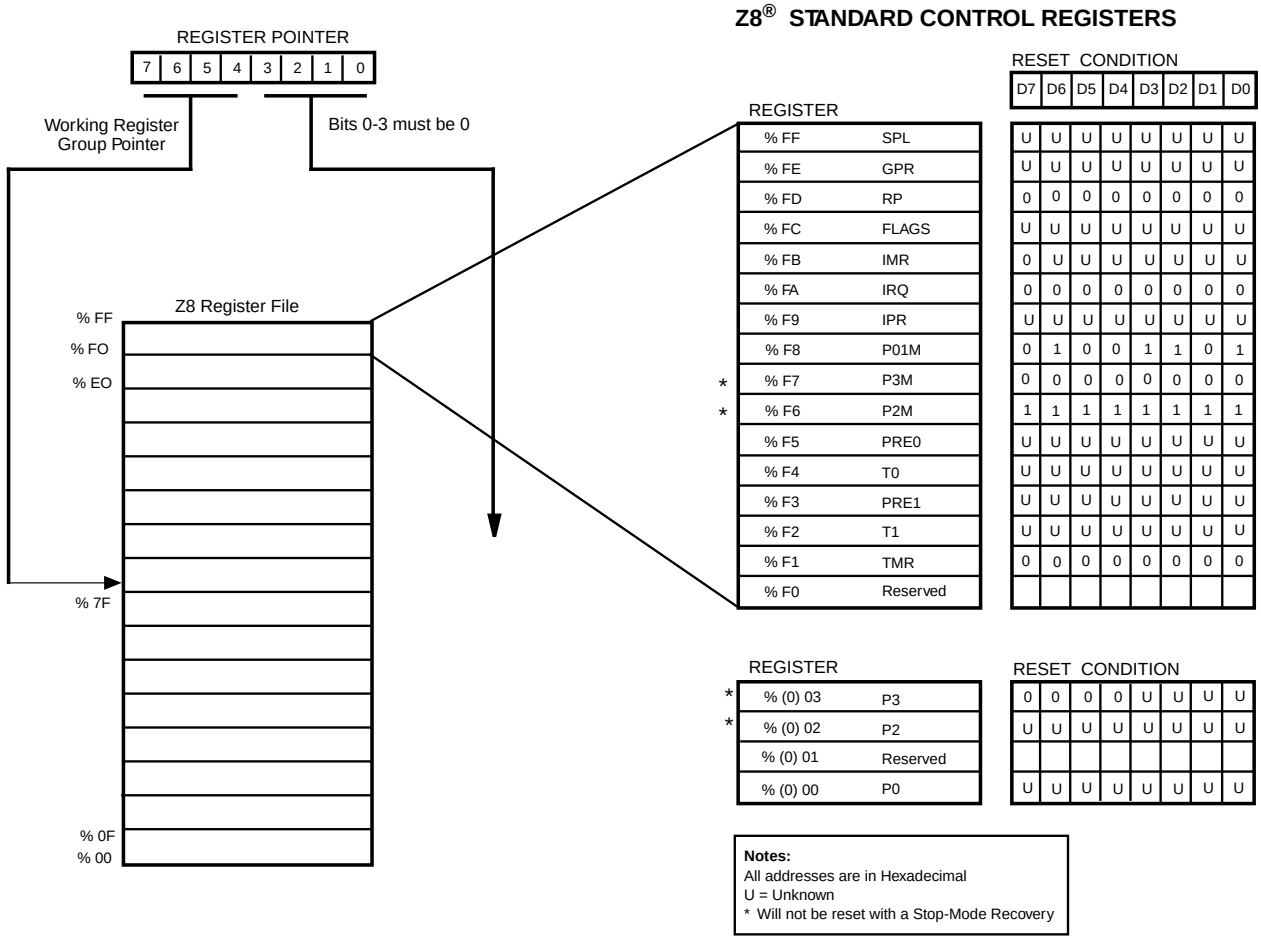


Figure 14. Register File Architecture

ROM Protect. A ROM Protect feature prevents “dumping” of the ROM contents without inhibiting execution of LDC, LDCI, LDE, and LDEI instructions. This feature is mask-programmable.

Stack Pointer. The Z86318 features an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however, the T0 can be driven by the internal clock source only (see Figure 15).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

FUNCTIONAL DESCRIPTION (Continued)

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, may be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or not retriggerable, or as a gate input for the internal clock.

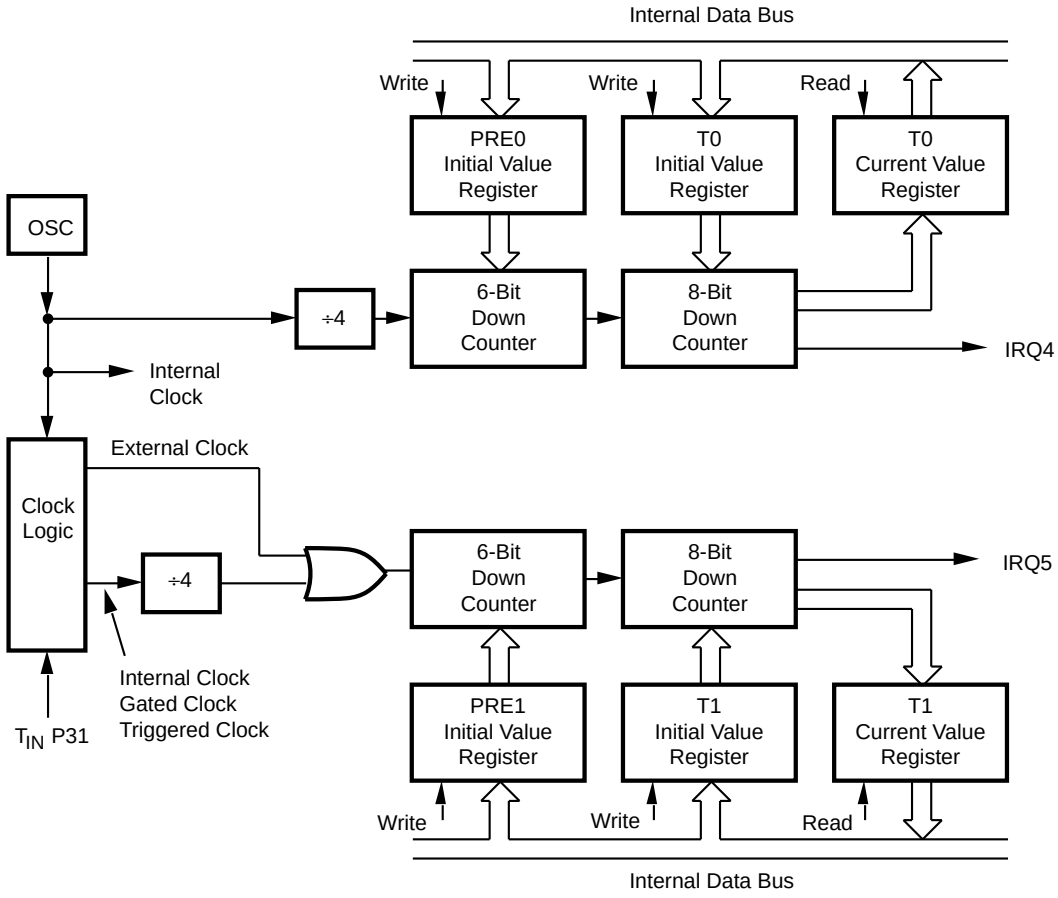


Figure 15. Counter/Timers Block Diagram

Interrupts. The Z86318 features four interrupts from four different sources. These interrupts are maskable and prioritized (Figure 16). The four sources are divided as follows: the falling edge of P31, P33, and the two counter/timers. The Interrupt Mask Register globally or individually enables or disables the four interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86318 interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the Interrupt Service Routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register is polled to determine which of the interrupt requests needs service.

Table 3. Interrupt Types, Sources, and Vectors

Source	Name	Vector	Location	Comments
P33	IRQ1	2,3	External	(F)Edge
P31	IRQ2	4,5	External	(F)Edge
T0	IRQ4	8,9	Internal	
T1	IRQ5	10,11	Internal	

Notes:
F = Falling edge triggered
R = Rising edge triggered

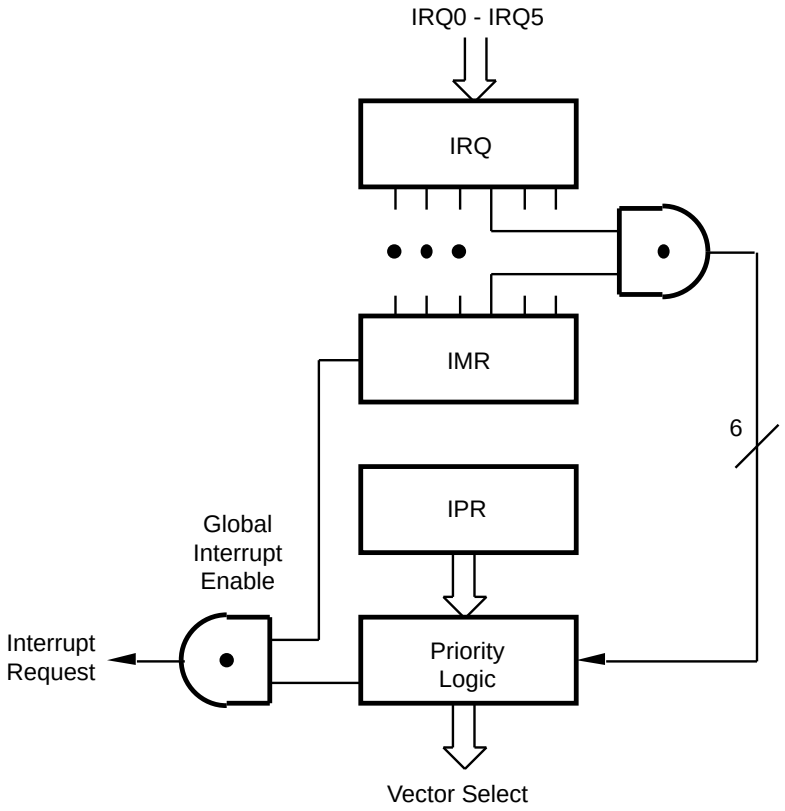


Figure 16. Interrupt Block Diagram

Clock. The Z86318 on-chip oscillator has a parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 4 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance is between 10 pF to 250 pF and is specified by the crystal manufacturer, ceramic resonator and PCB layout) from each pin to ground (see Figure 17).

FUNCTIONAL DESCRIPTION (Continued)

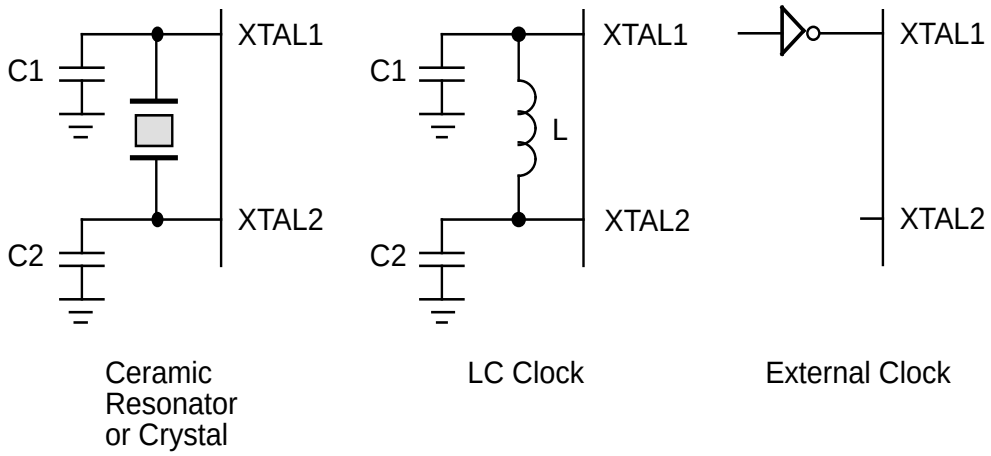


Figure 17. Oscillator Configuration

HALT Mode. This instruction turns off the internal CPU clock but not the on-chip oscillation circuit. The counter/timers and external interrupts IRQ1 and IRQ2 remain active. The device can be recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT. The HALT mode may also be exited via POR/RESET activation or a WDT time-out. In this case, the program execution begins at location 000CH. The WDH instruction is used to enable the Watch-Dog Timer in HALT mode.

STOP Mode. This instruction turns off the internal clock and reduces the standby current. The STOP mode can be released by the following methods: 1) Power-On Reset (POR) and 2) P27 is configured as an input line when the device executes the STOP instruction. A low input condition on P27 that meets a minimum pulse width (TWSM) releases the STOP mode. **Note:** WDT is disabled in STOP mode.

Upon reset, program execution begins at location 000C (hex). However, when P27 is used to release the STOP mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as an output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

LDP2M, #1XXX XXXXB(X = user's choice)

NOP

STOP

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, such as the following:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter the STOP mode
                or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter the HALT mode
```

In STOP or HALT mode, the value of each output line prior to the HALT or STOP instruction is retained during execution.

Watch-Dog Timer (WDT). The WDT is initially enabled by executing the WDT instruction and it is refreshed by subsequent WDT instruction executions. Note: Once the WDT has been enabled, it cannot be disabled. The time-out period of the WDT is 24 ms. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags. The WDT can be permanently enabled (ROM mask option) upon MCU power-up.

Opcode WDT (5FH). Execution of WDT clears the WDT counter. This must be done at least every 24 ms, otherwise, the WDT times out and generates a reset. This generated reset is the same as a power-on reset of 6.0 ms, plus 18 clock cycles.

Low-Voltage Protection (V_{LV}). The device will function normally between 6.0V and 4.0V under all specified conditions. Below 4.0V, the device is still internally functional until the Low Voltage trip point (V_{LV}) is reached; however, it is not guaranteed to meet all AC and DC Characteristics. When the supply voltage drops below V_{LV}, an automatic hardware reset occurs, re-initializing the Z86318. The Low-Voltage Protection feature may be selected as a ROM mask option.

The actual V_{LV} is a function of temperature, operating frequency and process parameters. A typical example of the V_{LV} trip-point function at ambient temperature for a frequency of 4 MHz is illustrated in Figure 18.

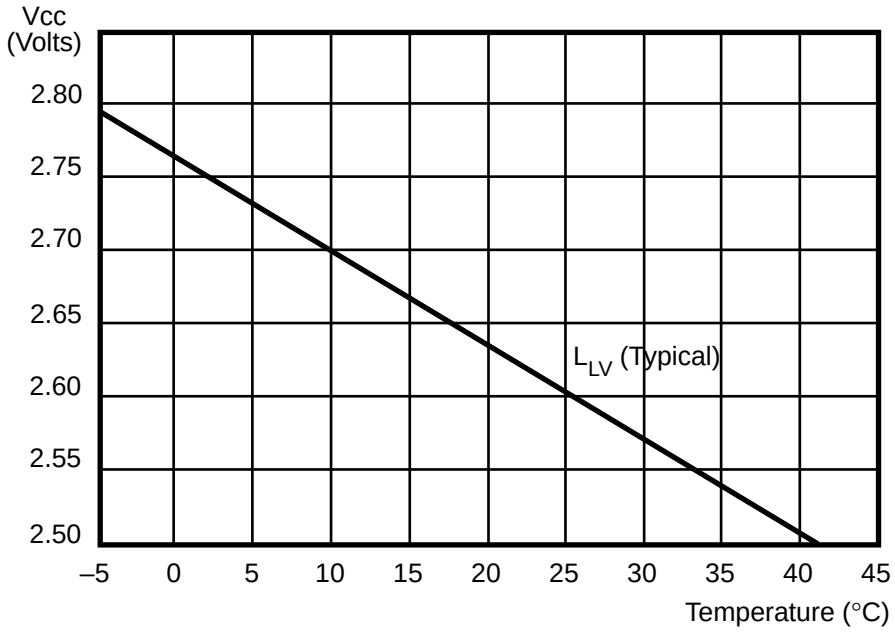


Figure 18. Typical Z86318 V_{LV} Versus Temperature

Z8 CONTROL REGISTERS

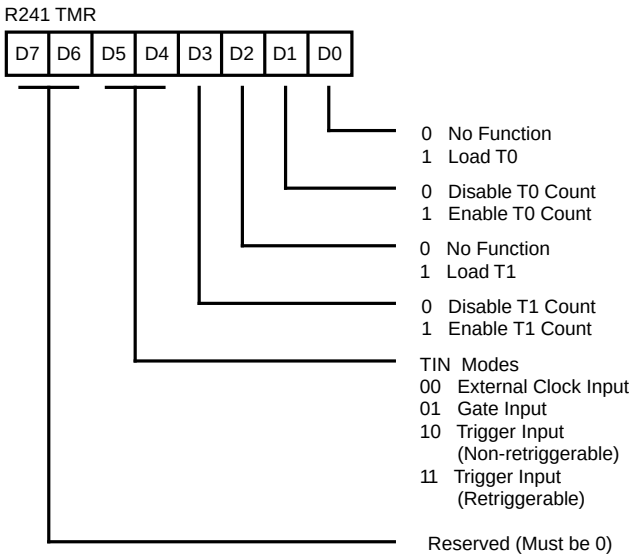


Figure 19. Timer Mode Register ($F1_H$:Read/Write)

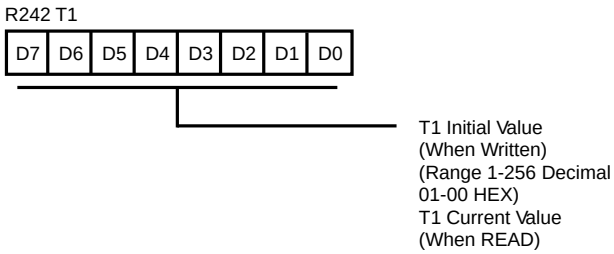


Figure 20. Counter Timer 1 Register ($F2_H$: Read/Write)

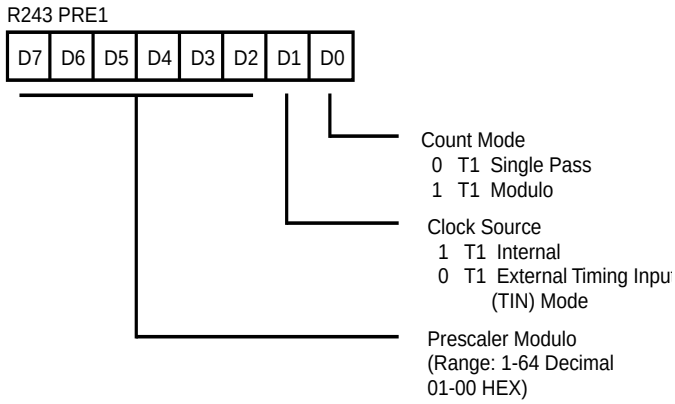


Figure 21. Prescaler 1 Register ($F3_H$:Write Only)

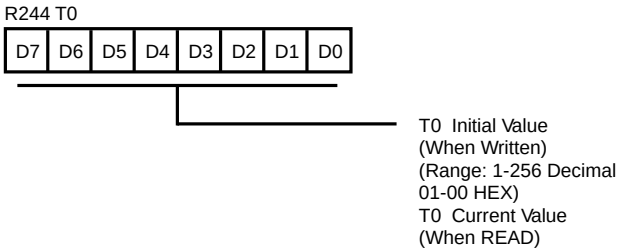


Figure 22. Counter Timer 0 Register ($F4_H$: Read/Write)

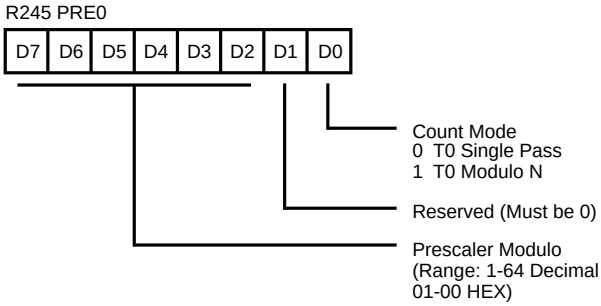


Figure 23. Prescaler 0 Register ($F5_H$: Write Only)

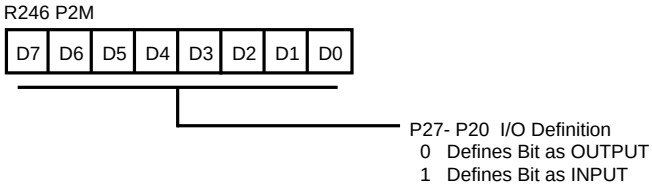


Figure 24. Port 2 Mode Register ($F6_H$: Write Only)

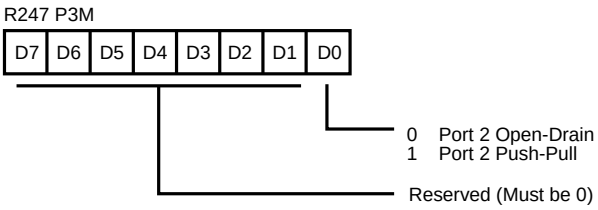


Figure 25. Port 3 Mode Register ($F7_H$: Write Only)

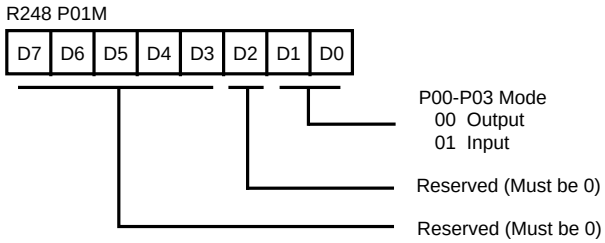


Figure 26. Port 0 and 1 Mode Register ($F8_H$: Write Only)

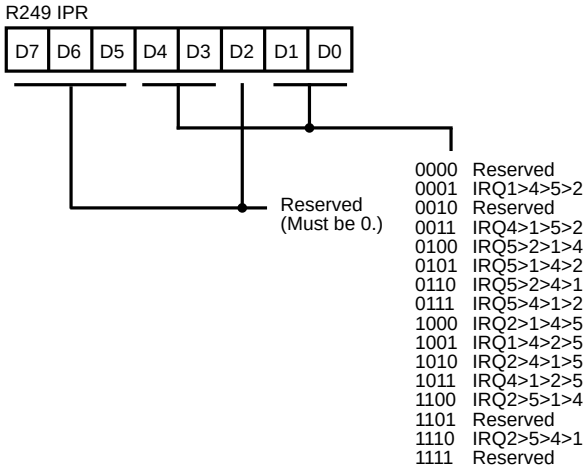


Figure 27. Interrupt Priority Register ($F9_H$: Write Only)

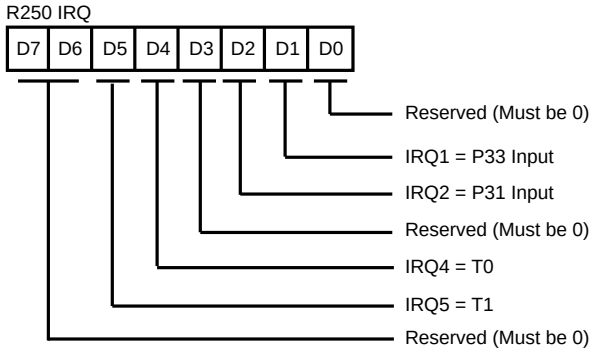


Figure 28. Interrupt Request Register (FA_H: Read/Write)

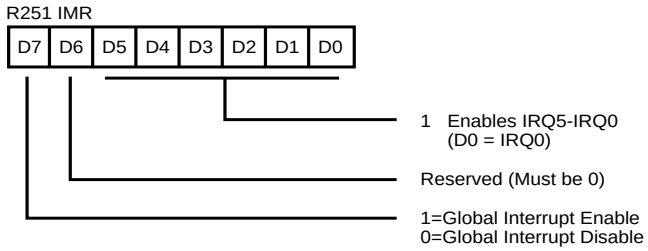


Figure 29. Interrupt Mask Register (FB_H: Read/Write)

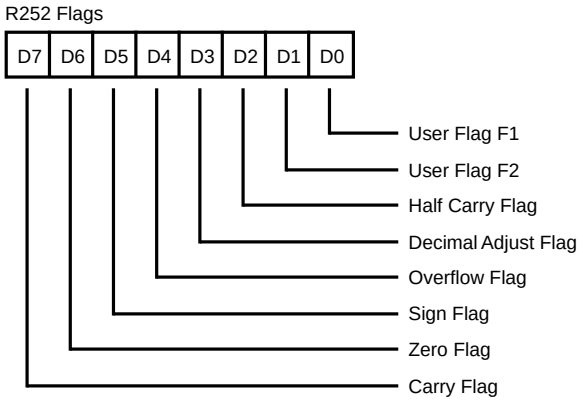


Figure 30. Flag Register (FC_H: Read/Write)

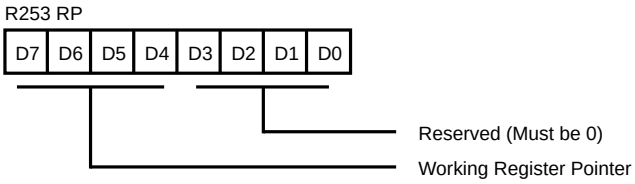


Figure 31. Register Pointer (FD_H: Read/Write)

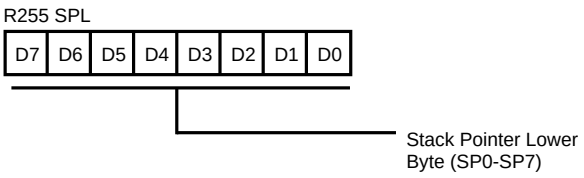
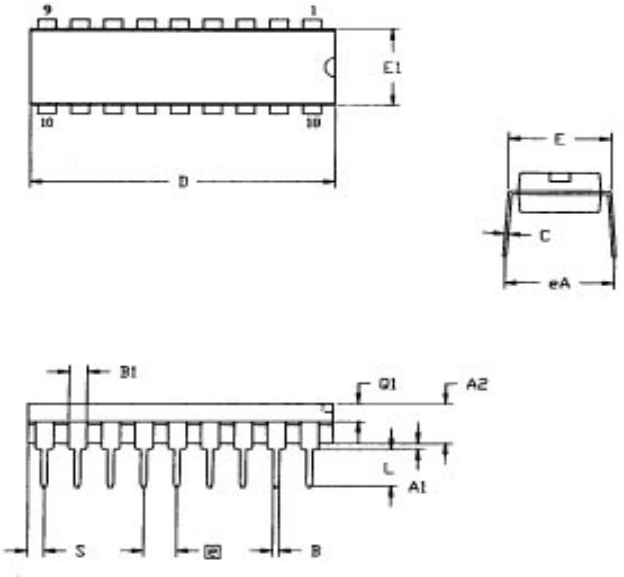


Figure 32. Stack Pointer (FFH: Read/Write)

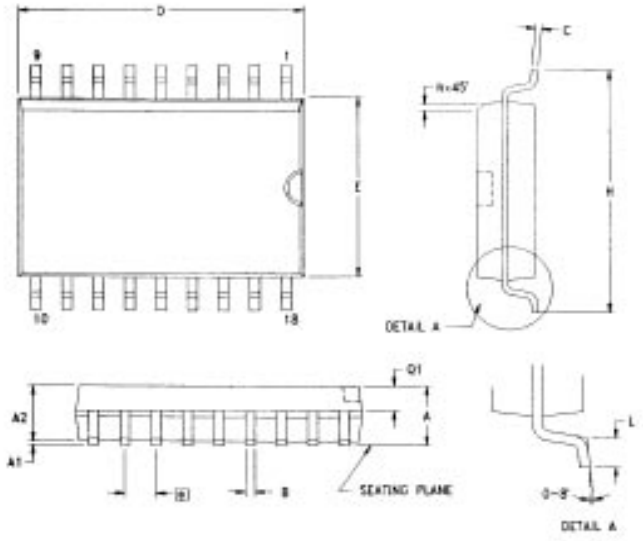
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 33. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 34. 18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86318	
18-Pin DIP	**18-Pin SOIC**
Z8631804PSC	Z8631804SSC
Z8631804PEC	Z8631804SEC

For fast results, contact your local Zilog sales offices for assistance in ordering the part desired.

Codes

Preferred Package
P = DIP

Longer Lead Time
S = SOIC

Temperature
S = 0°C to +70°C

Speed
04 = 4 MHz

Environmental
C = Plastic Standard

Example:

Z 86318 04 P S C is a Z86318, 4 MHz, DIP, 0°C to +70°C, Plastic Standard Flow