VIA C3 Nehemiah Processor

Datasheet

Revision 1.13

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VIA TECHNOLOGIES, INC.

This is **Version 1.13** of the VIA C3 Nehemiah Processor Datasheet.

LIFE SUPPORT POLICY

VIA processor products are not authorized for use as components in life support or other medical devices or systems (hereinafter life support devices) unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of VIA.

1. **Life support devices are devices which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **This policy covers any component of a life support device or system whose failure to perform can cause the failure of the life support device or system, or to affect its safety or effectiveness.**

Revision History

Document Release	Date	Revision	Initials
1.0	11/26/03	Initial external release	EY
1.10	3/11/04	Updated table 5-3	JW
1.11	07/30/04	Updated POWERGOOD information in figures 4-5, 4-6 and table 3-3	JW
1.12	9/1/04	Updated table 4-13	JW
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1

INTRODUCTION

The VIA C3 Nehemiah processor is based on a unique internal architecture and is manufactured using an advanced 0.13µ CMOS technology. This architecture and process technology provides a highly compatible, high-performance, low-cost and low-power solution for the desktop PC, notebook and Internet Appliance markets. The VIA Nehemiah family also provides Padlock, a suite a security technologies. The VIA C3 Nehemiah processor is available in several GHz versions.

When considered individually, the compatibility, function, performance, cost and power dissipation of the VIA C3 Nehemiah processor family are all very competitive. When considered as a whole, the VIA C3 Nehemiah processor family offers a breakthrough level of *value.*

1.1 DATASHEET OUTLINE

The intent of this datasheet is to make it easy for a direct user—a board designer, a system designer, or a BIOS developer—to use the VIA C3 Nehemiah processor.

In the datasheet, Section 1 summarizes the key features of the VIA C3 Nehemiah processor. Section 2 specifies the primary programming interface and Section 3 does the same for the bus interface. Sections 4, 5, and 6 specify the classical datasheet topics of AC timings, pinouts and mechanical specifications.

Appendix A documents the VIA C3 Nehemiah processor machine specific registers (MSRs).

1.2 BASIC FEATURES

The VIA C3 Nehemiah processor family currently consists of two basic models with several different GHz versions. Due to its low power dissipation, the two models are ideally suited for both desktop and mobile applications. All versions share the following common features (except as noted):

- Padlock Advanced Cryptography Engine (available in Stepping 8 and higher).
- Padlock Random Number Generator (available in Stepping 3 and higher).
- Plug-compatible with Socket 370 processors in terms of bus protocol, electrical interface, and physical package
- Software-compatible with thousands of x86 software applications available
- MMX-compatible instructions
- SSE-compatible instructions
- Two large (64-KB each, 4-way) on-chip caches (2-way in Stepping 8 and higher)
- 64-KB Level 2 victim cache (16-way)
- Two large TLBs (128 entries each, 8-way)
- Branch Target Address Cache with 1k entries each identifying 2 branches
- Unique and sophisticated branch prediction mechanisms
- Bus speeds up to 133 MHz
- Extremely low power dissipation
- Very small die-52 mm^2 in TSMC 0.13µ technology (47 mm^2 for Stepping 8 and higher)

1.3 PROCESSOR VERSIONS

Typically, there are five specification parameters that characterize different versions of a processor family: package, voltage, maximum case temperature, external bus speed and internal MHz.

The VIA C3 Nehemiah processor family is offered in a variety of packages: a Universal370-compatible ceramic PGA and an enhanced BGA (EBGA). The current nominal voltage is defined based on the different versions available. The Universal370 VID pins define the voltage.

The internal MHz of a particular VIA C3 Nehemiah processor chip is defined by two parameters: the specified external bus speed and the internal bus-clock multiplier. VIA C3 Nehemiah processors operate the bus at 133 MHz bus. (VIA C3 Nehemiah can also operate at 66 or 100 MHz bus speeds.) Bus frequency select pins (BSEL 0 and BSEL 1) identify the appropriate bus speed.

The bus-clock multiplier is hardwired into each VIA C3 Nehemiah processor chip. That is, the ratio of the internal processor clock speed to the externally supplied bus clock is frozen for a particular chip[1]. Several different clock-multiplier versions are currently offered.

More information on these topics is included in Sections 4, 5, and 6 of this datasheet

- The VIA C3 Nehemiah processor is initially available with a variety of speeds:
  - 1.00 GHz (7.5 x 133-MHz bus)
  - 1.13 GHz (8.5 x 133-MHz bus)
  - 1.20 GHz (9.0 x 133-MHz bus)
- The VIA C3 Nehemiah processor will provide other speed grades, bus speed combinations and different core voltages for the future.

[1] Actually, it is semi-frozen. A VIA-unique machine specific register allows programming to temporarily change the hard-wired multiplier. This capability, documented in Appendix A, is intended for special BIOS situations as well as test and debug usage.

1.4 COMPATIBILITY

A VIA C3 Nehemiah processor can plug into existing Socket 370 motherboards and it can operate without any changes on the system. No special jumper or different board wiring is required. In some cases, however, a special BIOS is needed. Currently, BIOS support for the VIA C3 Nehemiah processor is available from Award, AMI, Phoenix and Insyde.

The VIA C3 Nehemiah processor integrates external termination of bus signals. Physical and bus compatibility is covered in more detail in Section 4 of this datasheet.

The VIA C3 Nehemiah processor supports SSE instructions. The VIA C3 Nehemiah processor currently does not support multiple processors; however future versions may implement dual processors support. These functions are defined as optional by, and are identified to software via, the CPUID instruction. The VIA C3 Nehemiah processor carefully follows the protocol for defining the availability of these optional features. Both the additional and omitted optional features are described in detail in Section 2 of this datasheet.

To verify compatibility of the VIA C3 Nehemiah processor with real PC applications and hardware, VIA has performed extensive testing of hundreds of PC boards and peripherals, thousands of software applications and all known operating systems.

SECTION

2

PROGRAMMING INTERFACE

2.1 GENERAL

The VIA C3 Nehemiah processor's functions include:

- All basic x86 instructions, registers, and functions
- All floating-point (numeric processor) instructions, registers and functions
- All basic operating modes: real mode, protect mode, virtual-8086 mode
- System Management Interrupt (SMI) and the associated System Management Mode (SMM)
- All interrupt and exception functions
- All debug functions (including the new I/O breakpoint function)
- All input/output functions
- All tasking functions (TSS, task switch, etc.)
- Processor initialization behavior
- Page Global Enable feature

Besides the MMX instructions, the VIA C3 Nehemiah processor also includes SSE instructions to boost the performance of 3D graphics.

However, there are some differences between the VIA C3 Nehemiah processor and the Celeron processor. These differences fall into three groups:

- **Implementation-specific differences**. Examples are cache and TLB testing features, and performance monitoring features that expose the internal implementation features. These types of functions are incompatible among *all* different x86 implementations.
- **Omitted functions**. Some Intel Celeron processor functions are not provided on the VIA C3 Nehemiah processor because they are not used or unnecessary for the targeted PC systems. Examples of some specific bus functions: functional redundancy checking and performance monitoring. Other examples of architectural extensions: support for Physical Address Extensions and JTAG boundary scan.

  These types of differences are similar to those among various versions of the processors. With the CPUID instruction, the system software can determine whether these features are supported.
- **Low-level behavioral differences**. A few low-level VIA C3 Nehemiah processor functions are different from Intel Celeron because the results are (1) documented in the documentation as *undefined*, and (2) known to be different for different x86 implementations. That is, compatibility with the Intel Celeron processor for these functions is clearly not needed for software compatibility (or they would not be different across different implementations).

This chapter summarizes the first three types of differences: additional functions, implementation-specific functions, and omitted functions. *Appendix A* contains more details on machine-specific functions.

2.2 ADDITIONAL FUNCTIONS

Virtual 8086 Mode Enhancements: VME

VME has been added to VIA C3 Nehemiah stepping ID 8 and above. The function is omitted in VIA C3 Nehemiah stepping ID 7 and below. The CPUID feature flag bit 1 will indicate if Virtual Mode Enhancements are present.

SYSENTER and SYSEXIT: SEP

This function has been added to VIA C3 Nehemiah stepping ID 8 and above. The function is omitted in VIA C3 Nehemiah stepping ID 7 and below. The CPUID feature flag bit 11 will indicate if SYSENTER/SYSEXIT instructions are present.

Page Attribute Table: PAT

PAT function has been added to VIA C3 Nehemiah stepping ID 8 and above. The function is omitted in VIA C3 Nehemiah stepping ID 7 and below. The CPUID feature flag bit 16 will indicate if a Page Attribute Table is present.

Padlock

The VIA Eden-N processor includes a suite of security technologies called Padlock. One Padlock feature is called the Advanced Cryptography Engine (ACE) and provides a high performance implementation of the Advanced Encryption Standard (AES), as specified by the US Government. VIA Eden-N processors also extend Padlock by including two separate Random Number Generators.

Advanced Cryptography Engine: ACE

Padlock's Advanced Cryptography Engine provides the world’s fastest AES encryption implementation. Wherever AES software encryption implementations are used today, it can be optimized for ACE with minimal effort. World class AES performance is a user-level instruction away as only one opcode handles encrypt and decrypt functions. See the Padlock ACE programming guide for further details.

Random Number Generator: RNG

VIA Eden-N processors incorporate two random number generators on the processors die for a fast source of entropy. See the Padlock RNG programming guide for further details.

2.3 ACHINE-SPECIFIC FUNCTIONS

2.3.1 GENERAL

All x86 processor implementations provide a variety of *machine-specific functions*. Examples are cache and TLB testing features and performance monitoring features that expose the internal implementation features.

This section describes the VIA C3 Nehemiah processor machine-specific functions that are most likely used by software, and compares them to related processors where applicable. *Appendix A* documents the VIA C3 Nehemiah processor machine-specific registers (*MSRs*).

This section covers those features of Intel Pentium-compatible processors that are used to commonly identify and control processor features. All Pentium-compatible processors have the same mechanisms, but the bit-specific data values often differ.

2.3.2 STANDARD CPUID INSTRUCTION FUNCTIONS

The CPUID instruction is available on all contemporary x86 processors. The CPUID instruction has two standard functions requested via the EAX register. The first function returns a vendor identification string in registers EBX, ECX, and EDX. The second CPUID function returns an assortment of bits in EAX and EDX that identify the chip version and describe the specific features available.

The EAX:EBX:ECX:EDX return values of the CPUID instruction executed with EAX == 0 are:

Table 3-1. CPUID Return Values (EAX = 0)

REGISTER[BITS] – MEANING	*VIA C3 NEHEMIAH*
EAX (highest EAX input value understood by CPUID)	1
EBX:EDX:ECX (vendor ID string)	"Centaur Hauls"

The EAX return values of the CPUID instruction executed with EAX == 1 are:

Table 3-2. CPUID EAX Return Values (EAX = 1)

EAX BITS – MEANING	*VIA C3 NEHEMIAH*
3:0 - Stepping ID	
7:4 - Model ID	Same as the return value in EDX after Reset (see next section)
11:8 - Family ID	
13:12 – Type ID	

The EDX return values of the CPUID instruction with EAX == 1 are:

Table 3-3 CPUID EDX Return Values (EAX = 1)

EDX BITS – MEANING	*VIA C3 NEHEMIAH (Stepping 0-7)*	*VIA C3 NEHEMIAH (Stepping 8-15)*	*NOTES*
0 – FPU present	1	1	
1 - Virtual Mode Extension	0	1	
2 - Debugging Extensions	1	1	
3 - Page Size Extensions (4MB)	1	1	
4 – Time Stamp Counter (TSC) supported	1	1	
5 - Model Specific Registers present	1	1	
6 - Physical Address Extension	0	0	
7 - Machine Check Exception	0	0	
8 - CMPXCHG8B instruction	1	1	1
9 – APIC supported	0	1	2
10- Reserved			
11- Fast System Call	0	1	
12- Memory Range Registers	1	1	
13 - PTE Global Bit supported	1/0	1/0	3
14- Machine Check Architecture supported	0	0	
15- Conditional Move supported	1	1	
16- Page Attribute Table	0	1	
17- 36-bit Page Size Extension	0	0	
18- Processor serial number	0	0	
19:22 - Reserved			
23- MMX supported	1	1	
24- FXSR	1	1	
25- Streaming SIMD Extension supported	1	1	
26:31 - Reserved			

Notes On CPUID Feature Flags:

General: an "x/y" entry means that the default setting of this bit is x but the bit (and the underlying function) can be set to y using the FCR MSR.

1. The CMPXCHG8B instruction is provided and always enabled, however, it can be disabled in the corresponding CPUID function bit 8 to avoid a bug in an early version of Windows NT. However, this default can be changed via bit 1 in the FCR MSR.
2. APIC will be available in future steppings.
3. The VIA C3 Nehemiah processor's support for Page Global Enable can be enabled or disabled by a bit in the FCR. The CPUID bit reports the current setting of this enable control.

2.3.3 EXTENDED CPUID INSTRUCTION FUNCTIONS

The VIA C3 Nehemiah processor supports extended CPUID functions that provide additional information about the VIA C3 Nehemiah processor. Extended CPUID functions are requested by executing CPUID with EAX set to any value in the range 0x80000000 through 0x80000006.

The following table summarizes the extended CPUID functions.

Table 3-4. Extended CPUID Functions

EAX	*TITLE*	*OUTPUT*
80000000	Largest Extended Function Input Value	EAX=80000006 EBX,ECX,EDX=Reserved
80000001	Processor Signature and Feature Flags	EAX=Processor Signature EBX,ECX=Reserved EDX=Extended Feature Flags
80000002	Processor Name String	EAX,EBX,ECX,EDX
80000003	Processor Name String	EAX,EBX,ECX,EDX
80000004	Processor Name String	EAX,EBX,ECX,EDX
80000005	TLB and L1 Cache Information	EAX = Reserved EBX = TLB Information ECX = L1 Data Cache Information EDX = L1 Instruction Cache Information
80000006	L2 Cache Information	EAX, EBX, EDX = Reserved ECX = L2 Cache Information

Largest Extended Function Input Value (EAX==0x80000000)

Returns 0x80000006 in EAX, the largest extended function input value.

Processor Signature and Feature Flags (EAX==0x80000001)

Returns processor version information in EAX.

Processor Name String (EAX==0x80000002–0x80000004)

Returns the name of the processor, suitable for BIOS to display on the screen (ASCII). The string can be up to 48 characters in length. If the string is shorter, the rightmost characters are padded with zero. The leftmost characters go in EAX, then EBX, ECX, and EDX. The leftmost character goes in least significant byte (little endian).

For example, the string "VIA C3 Nehemiah*"* would be returned by extended function EAX=0x80000002 as follows:

EAX = 0x20414956

EBX = 0x6568654E

ECX = 0x6861696D

EDX = 0x00000000

Since the string is less than 17 bytes, the extended functions EAX=0x80000003 and EAX=0x80000004 return zero in EAX, EBX, ECX, and EDX.

L1 Cache Information (EAX == 0x80000005)

Returns information about the implementation of the TLBs and caches:

Table 3-5. L1 Cache & TLB Configuration Encoding

REGISTER	*DESCRIPTION*	*VALUE*
EAX	Reserved	
EBX	TLB Information	
EBX[31:24]	D-TLB associativity	8
EBX[23:16]	D-TLB # entries	128
EBX[15: 8]	I-TLB associativity	8
EBX[7: 0]	I-TLB # entries	128
ECX	L1 Data Cache Information	
ECX[31:24]	Size (Kbytes)	64
ECX[23:16]	Associativity	4/2
ECX[15: 8]	Lines per Tag	1
ECX[7: 0]	Line Size (bytes)	32
EDX	L1 Instruction Cache Information	
EDX[31:24]	Size (Kbytes)	64
EDX[23:16]	Associativity	4/2
EDX[15: 8]	Lines per Tag	1
EDX[7: 0]	Line Size (bytes)	32

Notes On CPUID L1 Cache Associativity:

Steppings 0 through 7 have a 4-way L1 Data and Instruction caches. Steppings 8 and higher have 2-way L1 Data and Instruction caches. Stepping 8 has an erratum that will inadvertently report 4-way L1 caches instead of the proper 2-way L1 caches. The erratum is fixed in future steppings.

L2 Cache Information (EAX == 0x80000006)

Returns information about the implementation of the L2 cache:

Table 3-6. L2 Cache Configuration Encoding

REGISTER	*DESCRIPTION*	*VALUE*
EAX, EBX, EDX	Reserved	
ECX	L2 Data Cache Information	
ECX[31:16]	Size (Kbytes)	64
ECX[15:12]	Associativity	16
ECX[11: 8]	Lines per Tag	1
ECX[7: 0]	Line Size (bytes)	32

2.3.4 CENTAUR EXTENDED CPUID INSTRUCTION FUNCTIONS

The VIA C3 Nehemiah processor supports special CPUID functions that provide additional information about the VIA C3 Nehemiah processor. Centaur CPUID functions are requested by executing CPUID with EAX set to 0xC0000000 or 0xC0000001.

EAX INPUT	*TITLE*	*OUTPUT*
0xC0000000	Largest Centaur Extended Function Input Value	EAX=0xC0000001
0xC0000001	Centaur Extended Feature Flags	EDX=Centaur Extended Feature Flags EAX,EBX,ECX=Reserved

EDX BIT	*VALUE*
0	EDX[0]=0 Alternate Instruction Set (AIS) not supported EDX[0]=1 Alternate Instruction Set (AIS) supported
1	EDX[1]=0 AIS Disabled EDX[1]=1 AIS Enabled
2	EDX[2]=0 Random Number Generator (RNG) Present EDX[2]=1 Random Number Generator (RNG) Not Present
3	EDX[3]=0 RNG Disabled EDX[3]=1 RNG Enabled
4	EDX[4]=0 Longhaul MSR 0x110A not available EDX[4]=1 Longhaul MSR 0x110A available
5	EDX[5]=0 FEMMS instruction (opcode 0x0F0E) Not Present EDX[5]=1 FEMMS instruction (opcode 0x0F0E) Present
6	EDX[6]=0 Advanced Cryptography Engine (ACE) Present EDX[6]=1 Advanced Cryptography Engine (ACE) Not Present
7	EDX[6]=0 ACE Disabled EDX[6]=1 ACE Enabled
31:8	Reserved

2.3.5 PROCESSOR IDENTIFICATION

The VIA C3 Nehemiah processor provides several machine-specific features. These features are identified by the standard CPUID function EAX=1. Other machine-specific features are controlled by VIA C3 Nehemiah MSRs. Some of these features are not backward compatible with the predecessors in the VIA C3 family.

System software must not assume that all future processors in the VIA processor family will implement all of the same machine-specific features, or even that these features will be implemented in a backward-compatible manner. In order to determine if the processor supports particular machine-specific features, system software should follow the following procedure.

Identify the processor as a member of the VIA processor family by checking for a Vendor Identification String of "CentaurHauls" using CPUID with EAX=0. Once this has been verified, system software must determine the processor version in order to properly configure the machine-specific registers.

In general, system software can determine the processor version by comparing the Family and Model Identification fields returned by the CPUID standard function EAX=1.

If the processor version is not recognized then system software must not attempt to activate any machine-specific feature.

2.3.6 EDX VALUE AFTER RESET

After reset the EDX register holds a component identification number as follows:

	31:14	13:12	11:8	7:4	3:0
EDX	Reserved	Type ID	Family ID	Model ID	Stepping ID
	18	2	4	4	4

The specific values for the VIA C3 Nehemiah processor are listed in the chart. There are two stepping ID available for the Via C3 Nehemiah processor with different features available based on the stepping. The first stepping ID is 7 and below, while the second stepping ID is 8 and above. Differences in features are noted in the data sheet.

PROCESSOR	*TYPE ID*	*FAMILY ID*	*MODEL ID*	*STEPPING ID*
VIA C3 Nehemiah	0	6	9	Begins at 0

2.3.7 CONTROL REGISTER 4 (CR4)

Control register 4 (CR4) controls some of the advanced features of the Celeron processor. The VIA C3 Nehemiah processor provides a CR4 with the following specifics:

Table 3-7. CR4 Bits

CR4 BITS - MEANING	*VIA C3 NEHEMIAH*	*CELERON MODEL 6*	*CELERON MODEL 8*	*NOTES*
0: VME: Enables VME feature	0/1	0/1	0/1	1
1: PVI: Enables PVI feature	0/1	0/1	0/1	1
2: TSD: Makes RDTSC inst privileged	0/1	0/1	0/1	
3: DE: Enables I/O breakpoints	0/1	0/1	0/1	
4: PSE: Enables 4-MB pages	0/1	0/1	0/1	
5: PAE: Enables address extensions	r	r	r	
6: MCE: Enables machine check exception	0/1	0/1	0/1	2
7: PGE: Enables global page feature	0/1	0/1	0/1	
8: PCE: Enables RDPMC for all levels	0/1	0/1	0/1	
9: OSFXSR: Enables FXSAVE//FXRSTOR Support	0/1	r	0/1	
10: OSXMMEXCPT: O/S Unmasked Exception Support	0/1	r	0/1	
31:11 – reserved	r	r	r	

Notes On CR4

General: a "0/1" means that the default setting of this bit is 0 but the bit can be set to (1). A "0" means that the bit is always 0; it cannot be set. An "r" means that this bit is reserved. It appears as a 0 when read, and a GP exception is signaled if an attempt is made to write a 1 to this bit.

1. The VIA C3 Nehemiah processor stepping 7 and below do not provide this "Appendix H" function and this CR4 bit cannot be set. However, no GP exception occurs if an attempt is made to set this bit. The VIA C3 Nehemiah processor steppings 8 and above do provide function and the CR4 bit can be set.
2. The VIA C3 Nehemiah processor Machine Check has different specifics than the Machine Check function of compatible processors.

2.3.8 MACHINE-SPECIFIC REGISTERS

The VIA C3 Nehemiah processor implements the concept of Machine Specific Registers (MSRs). RDMSR and WRMSR instructions are provided and the CPUID instruction identifies that the VIA C3 Nehemiah processor supports MSRs.

In general, the MSRs have no usefulness to application or operating system software and are not used. (This is to be expected since the MSRs are different on each processor.) *Appendix A* contains a detailed description of the VIA C3 Nehemiah processor's MSRs.

2.4 OMITTED FUNCTIONS

This section summarizes those functions that are not in the VIA C3 Nehemiah processor. A bit in the CPUID feature flags indicates whether these feature are present or not.

Physical Address Extensions: PAE

This function is omitted since the target market for the VIA C3 Nehemiah processor is portables and typical desktop systems. These systems do not use 2 MB paging and have greater than 4 GB of system memory.

Page Size Extensions: PSE-36

This function is omitted since the target operating systems for the VIA C3 Nehemiah do not require greater than 4 GB of system memory.

Other Functions

Model specific registers pertaining to Machine Check, and Debug, Performance Monitoring, and Trace features are not supported.

SECTION

3

HARDWARE INTERFACE

3.1 BUS INTERFACE

The VIA C3 Nehemiah processor bus interface is commonly referred to as the Socket 370 interface.

The majority of the pins within the bus interface are involved with the physical memory and I/O interface. The remaining pins are power and ground pins, test and debug support pins, and various ancillary control functions. The pins and associated functions are listed and described in this section.

3.1.1 DIFFERENCES

The areas where the VIA C3 Nehemiah processor differs from compatible processors should not cause operational compatibility issues. These differences are:

- Bus-to-core Ratio Control
- Bus Frequency Control
- Probe Mode / JTAG / TAP Port (see *Test and Debug Section*)

Bus-to-Core Frequency Ratio Control

The VIA C3 Nehemiah processor supports both fused and software control of the bus-to-core frequency ratio. At reset, the factory-set, fused ratio is used. This ratio can then be adjusted via software. This adjustment lasts until the next reset.

Software can adjust the bus-to-core ratio using the VIA C3 Nehemiah processor's LongHaul extensions. These are documented separately in the VIA C3 LongHaul Specification.

Bus Frequency Selection

The VIA C3 Nehemiah processor supports automated bus frequency selection through the BSEL pins. The BSEL pins are used as a mechanism whereby the processor and the system board can negotiate to support high frequency bus frequencies. The standard BSEL decoding is shown in Table 3-1.

While the VIA C3 Nehemiah processor is designed to operate at bus frequencies of 66, 100, or 133 MHz, performance is improved by running at higher bus frequencies. Various speed bins preclude 133 MHz operation because the available bus-to-core ratios do not permit operation at the desired core MHz.

Processors from these speed bins indicate this by shorting the BSEL[1] pin to ground internal to the package. For these processors the BSEL[0] pin is left floating. Processors from speed bins which permit 133 MHz bus operation indicate this by allowing both BSEL[1] and BSEL[0] to float.

It is anticipated that motherboards will pull up both BSEL pins. The resulting BSEL-indicated bus frequency will then be either 100 MHz or 133 MHz according to speed bin. Bus operation at 66MHz is not desirable.

Table 3-1. BSEL Frequency Mapping

BSEL[1]	*BSEL[0]*	*BUS FREQUENCY*
0	0	66 MHz
0	1	100 MHz
1	0	Reserved
1	1	133 MHz

3.1.2 CLARIFICATIONS

Power Supply Voltage

The VIA C3 Nehemiah processor automatically controls its core processor power supply voltage with the VID pins.

The VID mapping for CPGA-packaged VIA C3 Nehemiah processors is in Table 3-2. This mapping corresponds to the VRM8.5 specification.

Table 3-2. Core Voltage Settings

VID4	*VID3*	*VID2*	*VID1*	*VID0*	*VCORE*
0	0	1	0	0	1.050V
1	0	1	0	0	1.075V
0	0	0	1	1	1.100V
1	0	0	1	1	1.125
0	0	0	1	0	1.150V
1	0	0	1	0	1.175V
0	0	0	0	1	1.200V
1	0	0	0	1	1.225V
0	0	0	0	0	1.250V
1	0	0	0	0	1.275V
0	1	1	1	1	1.300V
1	1	1	1	1	1.325V
0	1	1	1	0	1.350V
1	1	1	1	0	1.375V
0	1	1	0	1	1.400V
1	1	1	0	1	1.425V
0	1	1	0	0	1.450V
1	1	1	0	0	1.475V
0	1	0	1	1	1.500V
1	1	0	1	1	1.525V
0	1	0	1	0	1.550V
1	1	0	1	0	1.575V
0	1	0	0	1	1.600V
1	1	0	0	1	1.625V
0	1	0	0	0	1.650V
1	1	0	0	0	1.675V
0	0	1	1	1	1.700V
1	0	1	1	1	1.725V
0	0	1	1	0	1.750V
1	0	1	1	0	1.775V
0	0	1	0	1	1.800V
1	0	1	0	1	1.825V

NOTE: VID4 may be referred as VID25mV.

VCCCMOS

The VIA C3 Nehemiah processor routes the $VCC_{1.5}$ pin to the VCC_{CMOS} pin via the package. This signal is not used by the processor, but is intended for the system as the power supply for CMOS level signals. VCC_{CMOS} should not be expected to source more than 250mA.

RESET#

The VIA C3 Nehemiah processor is reset by the assertion of the RESET# pin. Current versions of the VIA C3 Nehemiah processor connect this pin to AH-4 in the Socket370 pinout.

Board designers should always connect RESET# to both AH-4 and X-4 to ensure compatibility with all VIA processors.

Thermal Monitoring

The VIA C3 Nehemiah processor supports thermal monitoring via the THERMDN and THERMDP pins. However, it does not support the THERMTRIP# pin. The THERMTRIP# pin should be treated as reserved.

Advanced Peripheral Interrupt Controller (APIC)

The APIC is currently not supported by the VIA C3 Nehemiah processor. Future steppings of the VIA C3 Nehemiah will support the APIC. The APIC pins (PICCLK, PICD0, and PICD1) are specified as reserved, but should be connected on the motherboard for compatibility with future processors.

3.1.3 OMISSIONS

VTT_PWRGD

The VTT_PWRGD signal is not used. Care should be taken to prevent the VCC plane from powering up before the VTT plane.

Breakpoint and Performance Monitoring Signals

The VIA C3 Nehemiah processor internally supports instruction and data breakpoints. However, the VIA C3 Nehemiah processor does not support the external indication of breakpoint matches via the BP3-BP0 pins. Similarly, the VIA C3 Nehemiah processor contains performance monitoring hooks internally, but it does not support the indication of performance monitoring events on PM1-PM0. The associated pins are unconnected on the VIA C3 Nehemiah processor package.

Error Checking

The VIA C3 Nehemiah processor does not support error checking. The BERR#, BINIT#, AERR#, AP#[1:0], DEP#[7:0], IERR#, RP#, and RSP# pins do not exist and should be treated as reserved.

$V_{COREDET}$

The VIA C3 Nehemiah processor does not connect to the VCOREDET pin.

SLEWCTRL

The VIA C3 Nehemiah processor does not connect to the SLEWCTRL pin. Future VIA processors may connect to the SLEWCTRL pin.

3.2 PIN DESCRIPTION

Table 3-3. Pin Descriptions

Pin Name	*Description*	*I/O*	*Clock*
A[31:3]#	The address Bus provides addresses for physical memory and external I/O devices. During cache inquiry cycles, A31#-A3# are used as inputs to perform snoop cycles.	I/O	BCLK
A20M#	A20 Mask causes the CPU to make (force to 0) the A20 address bit when driving the external address bus or performing an internal cache access. A20M# is provided to emulate the 1 MByte address wrap-around that occurs on the 8086. Snoop addressing is not affected.	I(1.5V)	ASYNC
ADS#	Address Strobe begins a memory/I/O cycle and indicates the address bus (A31#-A3#) and transaction request signals (REQ#) are valid.	I/O	BCLK
BCLK	Bus Clock provides the fundamental timing for the VIA C3 Nehemiah CPU. The frequency of the VIA C3 Nehemiah CPU input clock determines the operating frequency of the CPU's bus. External timing is defined referenced to the rising edge of CLK.	I(2.5V)	--
BNR#	Block Next Request signals a bus stall by a bus agent unable to accept new transactions.	I/O	BCLK
BPRI#	Priority Agent Bus Request arbitrates for ownership of the system bus.	I	BCLK
BSEL[1:0]	Bus Selection Bus provides system bus frequency data to the CPU.	O	BCLK
BR[1:0]#	BR0# drives the BREQ[0]# signal in the system to request access to the system bus. BR1# drives the BREQ[1]# signal in the system to request access to the system bus.	I/O	None
CPUPRES#	CPU Present is grounded inside the processor to indicate to the system that a processor is present.	O	None
D[63:0]#	Data Bus signals are bi-directional signals which provide the data path between the VIA C3 Nehemiah CPU and external memory and I/O devices. The data bus must assert DRDY# to indicate valid data transfer.	I/O	BCLK
DBSY#	Data Bus Busy is asserted by the data bus driver to indicate data bus is in use.	I/O	BCLK
DEFER#	Defer is asserted by target agent (e.g., north bridge) and indicates the transaction cannot be guaranteed as an in-order completion.	I	BCLK
DRDY#	Data Ready is asserted by data driver to indicate that a valid signal is on the data bus.	I/O	BCLK
FERR#	FPU Error Status indicates an unmasked floating-point error has occurred. FERR# is asserted during execution of the FPU instruction that caused the error.	O(1.5V)	ASYNC
FLUSH#	Flush Internal Caches writing back all data in the modified state.	I(1.5V)	ASYNC
HIT#	Snoop Hit indicates that the current cache inquiry address has been found in the cache (exclusive or shared states).	I/O	BCLK
HITM#	Snoop Hit Modified indicates that the current cache inquiry address has been found in the cache and dirty data exists in the cache line (modified state).	I/O	BCLK
IGNNE#	Ignore Numeric Error forces the VIA C3 Nehemiah CPU to ignore any pending unmasked FPU errors and allows continued execution of floating point instructions.	I(1.5V)	ASYNC
INIT#	Initialization resets integer registers and does not affect internal cache or floating point registers.	I(1.5V)	ASYNC
INTR / LINT0	Maskable Interrupt / Signal become LINT0 when APIC is enabled	I(1.5V)	ASYNC
NCHCTRL	Control integrated I/O pull-ups. Connect this signal to VTT with a 14Ω resistor.	I	ASYNC
NMI / LINT1	Non-Maskable Interrupt / Signal become LINT1 when APIC is enabled	I(1.5V)	ASYNC
LOCK#	Lock Status is used by the CPU to signal to the target that the operation is atomic.	I/O	BCLK
PICCLK	APIC clock for operation with the system I/O APIC	I	APIC

Pin Name	Description	I/O	Clock
PICD[1:0]	Bi-directional serial pins for communicating APIC messages to the system	I/0	APIC
PWRGD	Indicates that the processor's VCC is stable.	I (1.5V)	ASYNC
REQ[4:0]#	Request Command is asserted by bus driver to define current transaction type.	I/O	BCLK
RESET#	Resets the processor and invalidates internal cache without writing back.	I	BCLK
RS[2:0]#	Response Status signals the completion status of the current transaction when the CPU is the response agent.	I	BCLK
RTTCTRL	Control the output impedance on the on-die termination resistance. Connect this signal to VSS with a 56Ω resistor if relying upon on-die termination. Connect this signal to VSS with a 110Ω resistor if relying upon board termination.	I	ASYNC
SLP#	Sleep, when asserted in the stop grant state, causes the CPU to enter the sleep state.	I(1.5V)	ASYNC
SMI#	System Management (SMM) Interrupt forces the processor to save the CPU state to the top of SMM memory and to begin execution of the SMI services routine at the beginning of the defined SMM memory space. An SMI is a high-priority interrupt than NMI.	I(1.5V)	ASYNC
STPCLK#	Stop Clock causes the CPU to enter the stop grant state.	I(1.5V)	ASYNC
TRDY#	Target Ready indicates that the target is ready to receive a write or write-back transfer from the CPU.	I	BCLK
VID[4:0]	Voltage Identification Bus informs the regulatory system on the motherboard of the CPU Core voltage requirements.	O(1.5V)	ASYNC

Table 3-4. BGA only Pin Descriptions

Pin Name	Description	I/O	Clock
BR[4:0]	Hardware strapping options for setting the processors internal clock multiplier. VIA C3 Nehemiah processors do not have their clock multiplier set to a factory default value. Use jumpers or populate 0Ω resistors to select the rated multiplier. The BR[4:0] balls should be wired to VSS for a value of "0" or wired to OPEN for setting of "1." See Table 3-5 for ratio values.	I	

Table 3-5. Clock Ratio

BR[4]	BR[3]	BR[2]	BR[1]	BR[0]	Bus Ratio
0	0	0	0	0	9.0X
0	0	0	0	1	3.0X
0	0	0	1	0	4.0X
0	0	0	1	1	10.0X
0	0	1	0	0	5.5X
0	0	1	0	1	3.5X
0	0	1	1	0	4.5X
0	0	1	1	1	9.5X
0	1	0	0	0	5.0X
0	1	0	0	1	7.0X
0	1	0	1	0	8.0X
0	1	0	1	1	6.0X
0	1	1	0	0	12.0X
0	1	1	0	1	7.5X
0	1	1	1	0	8.5X
0	1	1	1	1	6.5X
1	0	0	0	0	Reserved
1	0	0	0	1	11.0X
1	0	0	1	0	12.0X
1	0	0	1	1	Reserved
1	0	1	0	0	13.5X
1	0	1	0	1	11.5X
1	0	1	1	0	12.5X
1	0	1	1	1	10.5X
1	1	0	0	0	13.0X
1	1	0	0	1	15.0X
1	1	0	1	0	16.0X
1	1	0	1	1	14.0X
1	1	1	0	0	Reserved
1	1	1	0	1	15.5X
1	1	1	1	0	Reserved
1	1	1	1	1	14.5X

3.3 POWER MANAGEMENT

The VIA C3 Nehemiah processor provides both static and dynamic power management.

The VIA C3 Nehemiah processor supports five power management states: NORMAL, QUICKSTART, SLEEP, DEEP SLEEP and DEEPER SLEEP.

The VIA C3 Nehemiah processor uses dynamic power management techniques to reduce power consumption in the NORMAL state. In NORMAL state, the on-chip arrays, selected datapaths and the associated control logic are powered down when not in use. Also, units that are in use attempt to minimize switching of inactive nodes.

- NORMAL state is the normal operating state for the processor.
- QUICKSTART state is the low power state where most of the processor clocks do not toggle. It is entered when the STPCLK# signal is asserted or when the processor executes the HALT instruction. Snoop cycles are supported in this state.
- SLEEP state is the low power state where only the processor's PLL (phase lock loop) toggles. It is entered from QUICKSTART state when the processor samples the SLP# signal asserted. Snoop cycles that occur while in SLEEP state or during a transition into or out of SLEEP state will cause unpredictable behavior.
- DEEP SLEEP state is a very low power state. It is entered when the BCLK signal is stopped while the processor is in the SLEEP state. Snoop cycles are completely ignored in this state.
- DEEPER SLEEP state is the lowest power state. It is entered when the processor core voltage is lowered while the processor is in the DEEP SLEEP state. Snoop cycles are completely ignored in this state.

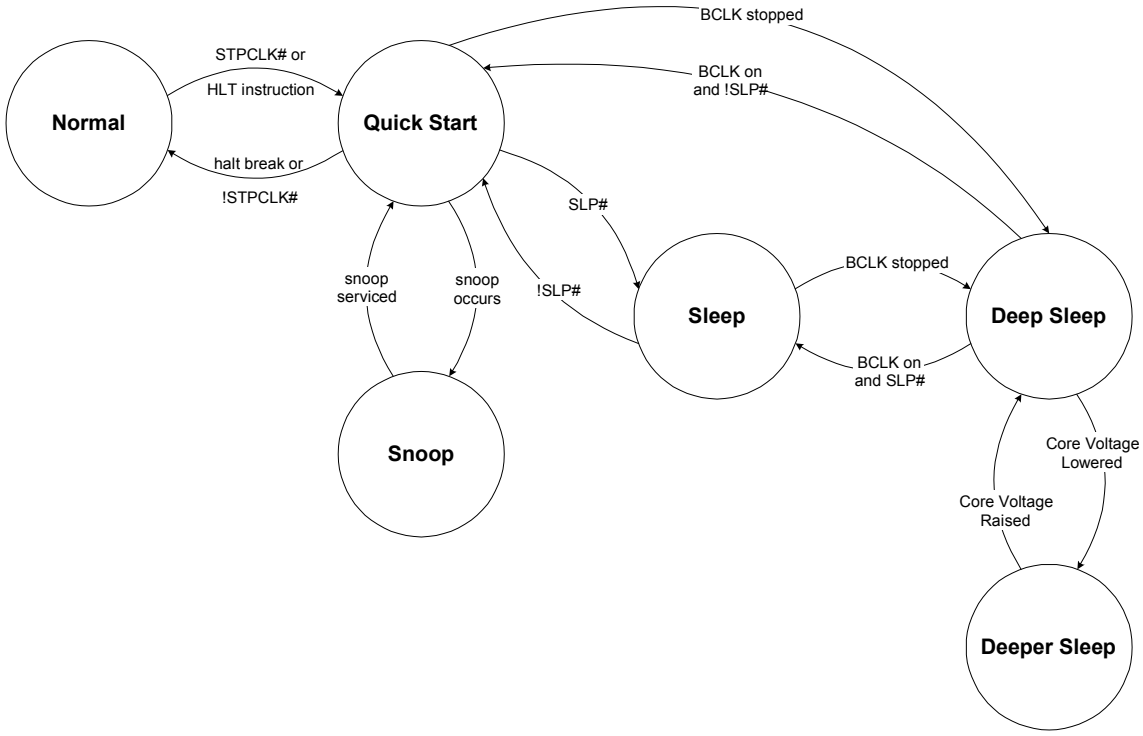


Figure 3-1. Power Management State Diagram

3.4 TEST & DEBUG

3.4.1 BIST

A Built-in Self-Test (BIST) can be requested as part of the VIA C3 Nehemiah processor reset sequence by holding INIT# asserted as RESET# is de-asserted.

The VIA C3 Nehemiah processor BIST performs the following general functions:

- A hardware-implemented exhaustive test of (1) all internal microcode ROM, and (2) the X86 instruction decode, instruction generation, and entry point generation logic.
- An extensive microcode test of all internal registers and datapaths.
- An extensive microcode test of data and instruction caches, their tags, and associated TLBs.

BIST requires about four million internal clocks.

EAX Value After Reset

The result of a BIST is indicated by a code in EAX. Normally EAX is zero after reset. If a BIST is requested as part of the Reset sequence, EAX contains the BIST results. A 0 in EAX after BIST Reset means that no failures were detected. Any value other than zero indicates an error has occurred during BIST.

3.4.2 JTAG

The VIA C3 Nehemiah processor has a JTAG scan interface that is used for test functions and the proprietary Debug Port. However, the VIA C3 Nehemiah processor does not provide a fully compatible IEEE 1149.1 JTAG function.

From a practical user viewpoint, JTAG does not exist and the associated pins (TCLK, and so forth) should not be used.

3.4.3 DEBUG PORT

Certain processors have a proprietary Debug Port that uses the JTAG scan mechanism to control internal debug features (“probe mode”). These interfaces are not documented and are available (if at all) only under a non-disclosure agreement.

The VIA C3 Nehemiah processor does not have a debug interface.

SECTION

4

ELECTRICAL SPECIFICATIONS

4.1 AC TIMING TABLES

Table 4-1: System Bus Clock AC Specifications (133 MHz)[1]

SYMBOL	*PARAMETER*	*MIN*	*MAX*	*UNIT*	*FIGURE*	*NOTES*
	System Bus Frequency		133	MHz		
T_{1S}	BCLK Period	7.5	7.65	ns	Figure 4-1	(2)
T_{1Sabs}	BCLK Period – Instantaneous Minimum	7.25				(2)
T_{2S}	BCLK Period Stability		$\pm$250	ps		(2),(3),(4)
T_{3S}	BCLK High Time	1.4		ns	Figure 4-1	at>2.0V
T_{4S}	BCLK Low Time	1.4		ns	Figure 4-1	at<0.5V
T_{5S}	BCLK Rise Time	0.4	1.6	ns	Figure 4-1	(5)
T_{6S}	BCLK Fall Time	0.4	1.6	ns	Figure 4-1	(5)

Notes:

1. All AC timings for bus and CMOS signals are referenced to the BCLK rising edge at 1.25V.
2. Period, jitter, skew and offset measured at 1.25V.
3. Not 100% tested. Specified by design/characterization.
4. Measured on the rising edge of adjacent BCLKs at 1.25V. The jitter present must be accounted for as a component of BCLK skew between devices.
5. Measured between 0.5V and 2.0V.

Table 4-2. System Bus Clock AC Specifications (100 MHz)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
	System Bus Frequency		100	MHz		
T_{1S1}	BCLK Period		10	ns	Figure 4-1	(2)
T_{1S1abs}	BCLK Period – Instantaneous Minimum	9.75		ns		(2)
T_{2S1}	BCLK Period Stability			ps	Figure 4-1	(2),(3),(4)
T_{3S1}	BCLK High Time	2.70		ns	Figure 4-1	At >2.0V
T_{4S1}	BCLK Fall Time	2.45		ns	Figure 4-1	At <0.5V
T_{5S1}	BCLK Rise Time	0.4		ns	Figure 4-1	(5)
T_{6S1}	BCLK Fall Time	0.4		ns	Figure 4-1	(5)

Notes:

1. All AC timings for bus and CMOS signals are referenced to the BCLK rising edge at 1.25V.
2. Period, jitter, skew and offset measured at 1.25V.
3. Not 100% tested. Specified by design/characterization
4. Measured on the rising edge of adjacent BCLKs at 1.25V. The jitter present must be accounted for as a component of BCLK skew between devices.
5. Measured between 0.5V and 2.0V.

Table 4-3. Bus Signal Groups AC Specifications[1,8]

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
T_7	Bus Output Valid Delay	0.40	3.25	ns	Figure 4-2	
T_8	Bus Input Setup Time	0.95 1.30		ns	Figure 4-3, Figure 4-4	(2),(3),(6) (7)
T_9	Bus Input Hold Time	1		ns	Figure 4-3, Figure 4-4	(4)
T_{10}	RESET# Pulse Width	1		ms	Figure 4-4	(5)

Notes:

1. All AC timings for bus and CMOS signals are referenced to the BCLK rising edge at 1.25V. All bus signals are referenced at VREF. Unless specified, all timings apply to both 100 MHz and 133 MHz bus frequencies.
2. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
3. Specification is for a minimum 0.4V swing from VREF-200 mV to VREF+200 mV.
4. Specification is for a maximum 0.8V swing from VTT-0.8V to VTT.
5. After VCC, VTT and BCLK become stable and PWRGOOD is asserted.
6. Applies to processors supporting 133 MHz bus clock frequency.
7. Applies to processors supporting 100 MHz bus clock frequency.
8. Rtt=56Ω internally terminated to VTT; VREF=2/3 VTT; Load = 50Ω

Table 4-4. CMOS and Open-drain Signal GROUPS AC Specifications[1,2]

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
T_{14}	1.5V Input Pulse Width, except PWRGOOD and LINT[1:0]	2		BCLKs	Figure 4-2	Active and inactive states
T_{14B}	LINT[1:0] Input Pulse Width	6		BCLKs	Figure 4-2	(3)
T_{15}	PWRGOOD Inactive Pulse Width	2		µs	Figure 4-5	(4)

Notes:

1. All AC timings for CMOS and Open-drain signals are referenced to the rising edge of BCLK at 1.25V. All CMOS and Open-drain signals are referenced at 1.0V.
2. Minimum output pulse width on CMOS outputs is 2 BCLKs.
3. This specification only applies when the APIC is enabled and the LINT[1:0] signals are configured as edge triggered interrupts with fixed delivery, otherwise specification T14 applies.
4. When driven inactive, or after VCC, VTT and BCLK become stable. PWRGOOD must remain below VIL18,MAX until all the voltage planes meet the voltage tolerance specifications in Table 4-8 through Table 4-10 and BCLK have met the BCLK AC specifications in Table 4-1 and Table 4-2 for a least 2 µs. PWRGOOD must rise error-free and monotonically.

Table 4-5. Reset Configuration AC Specifications and Power On/Power Down Timings

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	FIGURE	NOTES
T_{16}	Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Setup Time	4			BCLKs	Figure 4-4	Before deassertion of RESET#
T_{17}	Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Hold Time	2		20	BCLKs	Figure 4-4	After clock that deasserts RESET#
T_{18}	RESET#/PWRGOOD Setup Time	1			ms	Figure 4-5	Before deassertion of RESET#[1]
T_{18B}	VCC to PWRGOOD Setup Time		10		ms	Figure 4-5	
T_{18D}	RESET# inactive to Valid Outputs	1			BCLK	Figure 4-4	
T_{18E}	RESET# inactive to Drive Signals	4			BCLKs	Figure 4-4	
T_{19A}	Time from VCC(nominal)-12% to PWRGOOD low			0	ns	Figure 4-6	VCC(nominal) is the VID voltage setting
T_{19B}	All outputs valid after PWRGOOD low	0			ns	Figure 4-6	
T_{19C}	All inputs required valid after PWRGOOD low	0			ns	Figure 4-6	
T_{20B}	All outputs valid after VTT-12%	0			ns	Figure 4-7	
T_{20C}	All inputs required valid after VTT-12%	0			ns	Figure 4-7	
T_{20D}	VID, BSEL signals valid after VTT-12%	0			ns	Figure 4-7	

Notes:

1. At least 1 ms must pass after PWRGOOD rises above VIH18min and BCLK meet their AC timing specification until RESET# may be deasserted.

Table 4-6. APIC Bus Signal AC Specifications[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
T_{21}	PICCLK Frequency	2	33.3	MHz		(2)
T_{22}	PICCLK Period	30	500	ns	Figure 4-1	
T_{23}	PICCLK High Time	10.5		ns	Figure 4-1	at>1.6V
T_{24}	PICCLK Low Time	10.5		ns	Figure 4-1	at<0.4V
T_{25}	PICCLK Rise Time	0.25	3.0	ns	Figure 4-1	(0.4V-1.6V)
T_{26}	PICCLK Fall Time	0.25	3.0	ns	Figure 4-1	(1.6V-0.4V)
T_{27}	PICD[1:0] Setup Time	8.0		ns	Figure 4-3	(3)
T_{28}	PICD[1:0] Hold Time	2.5		ns	Figure 4-3	(3)
T_{29}	PICD[1:0] Valid Delay (Rising Edge)	1.5	8.7	ns	Figure 4-2	(3),(4)
	PICD[1:0] Valid Delay (Falling Edge)	1.5	12.0	ns		

Notes:

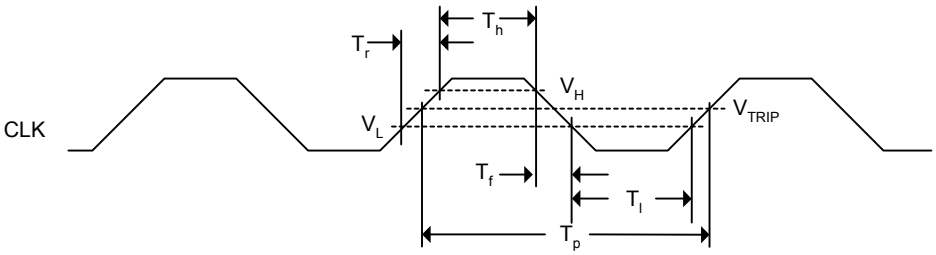
1. All AC timing for APIC signals referenced to the PICCLK rising edge at 1.0V. All CMOS signals are referenced at 1.0V.
2. The minimum frequency is 2MHz when PICD0 is at 1.5V at reset referenced to PICCLK Rising Edge.
3. For open-drain signals, Valid Delay is synonymous with Float Delay.
4. Valid delay timings for these signals are specified into 150Ω to 1.5V and 0pF of external load. For real system timings, these specifications must be derated for external capacitance at 105ps/pF.

Table 4-7. StopGrant / Sleep / Deep Sleep AC Specifications[1, 3, 4]

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
T_{45}	Stop Grant Cycle Completion to SLP# assertion or BCLK Stopped	100		BCLKs	Figure 4-8, Figure 4-9	
T_{46}	Stop Grant Cycle Completion to Input Signals Stable		0	µs	Figure 4-8, Figure 4-9	
T_{47}	Sleep PLL Lock Latency	0	30	µs	Figure 4-8, Figure 4-9	(2)
T_{48}	STPCLK# Hold Time from PLL Lock	0		µs	Figure 4-8, Figure 4-9	
T_{49}	Input Signal Hold Time from STPCLK# Deassertion	8		BCLKs	Figure 4-8, Figure 4-9	
T_{60}	BCLK Settling Time		150	ns		

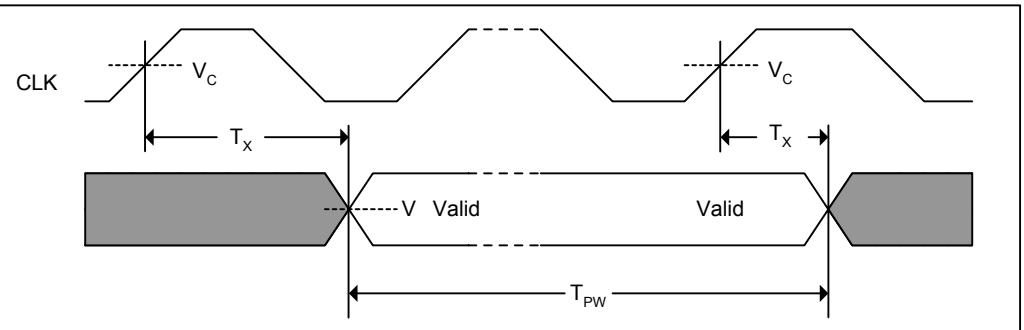
Notes:

1. Input Signals other than RESET# and BPRI# must be held constant in the Stop Grant state.
2. The BCLK Settling Time specification (T60) applies to all sleep state exits under all conditions.
3. In Figure 4-8 after SLP# is asserted, BCLK can be stopped and the processor will enter the Deep Sleep state. To exit the Deep Sleep state all timings shown in Figure 4-9 will need to be observed.
4. Vcore must be at nominal stable voltage before Deep Sleep exit after a Deeper Sleep transition.



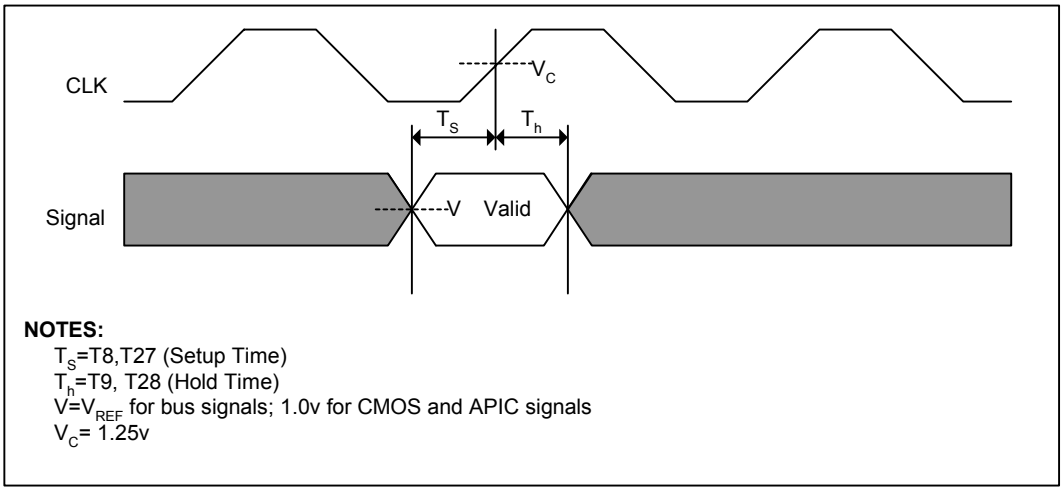
NOTES:
T_r=T5S, T5S1, T25 (Rise Time)
T_f=T6S, T6S1, T26 (Fall Time)
T_h=T3S, T3S1, T23 (High Time)
T_l=T4S, T4S1, T24 (Low Time)
T_p=T1S, T1S1, T22 (Period)
V_{TRIP}=1.25v for BCLK; 1.0V for PICCLK
V_L=0.5v for BCLK; 0.4V for PICCLK
V_H=2.0v for BCLK; 1.6V for PICCLK

Figure 4-1. BCLK Generic Clock Timing Waveform



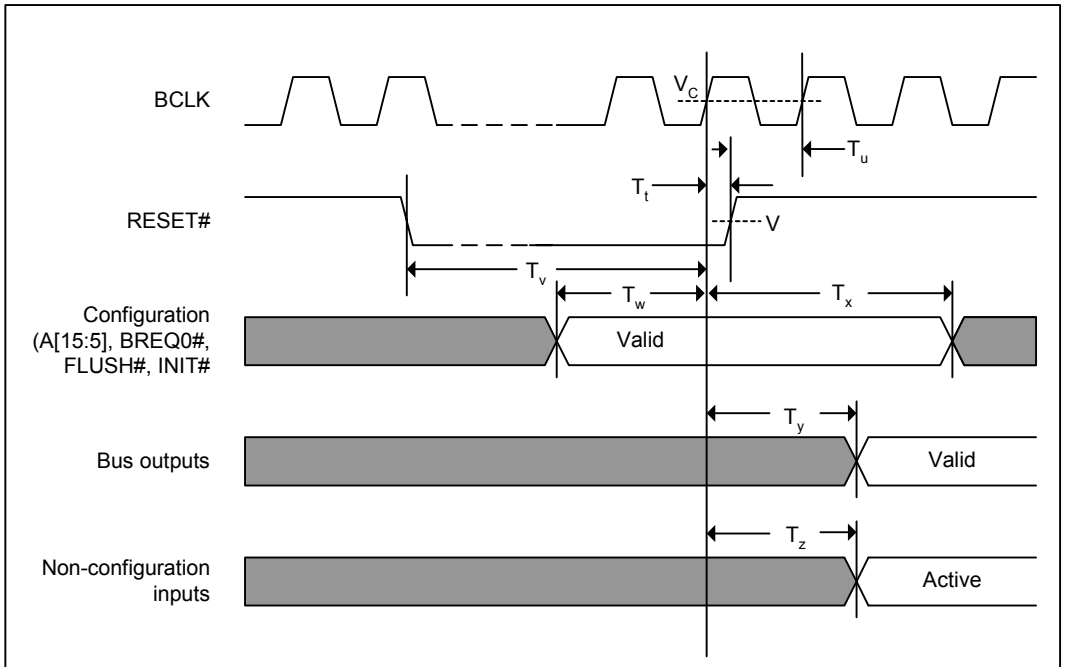
NOTES:
T_X=T7, T29 (Valid Delay)
T_{PW}=T14, T14B (Pulse Width)
V=V_{REF} for bus signal group; 1.0v for CMOS, Open-drain, and APIC signal groups
V_C= 1.25v

Figure 4-2. Valid Delay Timings



NOTES:
T_S=T8,T27 (Setup Time)
T_h=T9, T28 (Hold Time)
$V=V_{REF}$ for bus signals; 1.0v for CMOS and APIC signals
V_C= 1.25v

Figure 4-3. Setup and Hold Timings



NOTES:
T_t=T9 (Bus Input Hold Time)
T_u=T8 (Bus Input Setup Time)
T_v=T10 (RESET# Pulse Width)
T_w=T16 (Reset Configuration Signals (A[15:5#, BREQ0#, FLUSH#, INIT#) Setup Time)
T_x=T17 (Reset Configuration Signals (A[15:5#, BREQ0#, FLUSH#, INIT#) Hold Time)
T_y=T18D (RESET# inactive to Valid Outputs)
T_z=T18E (RESET# inactive to Drive Signals)
V_C=1.25v

Figure 4-4. Cold/Warm Reset and Configuration Timings

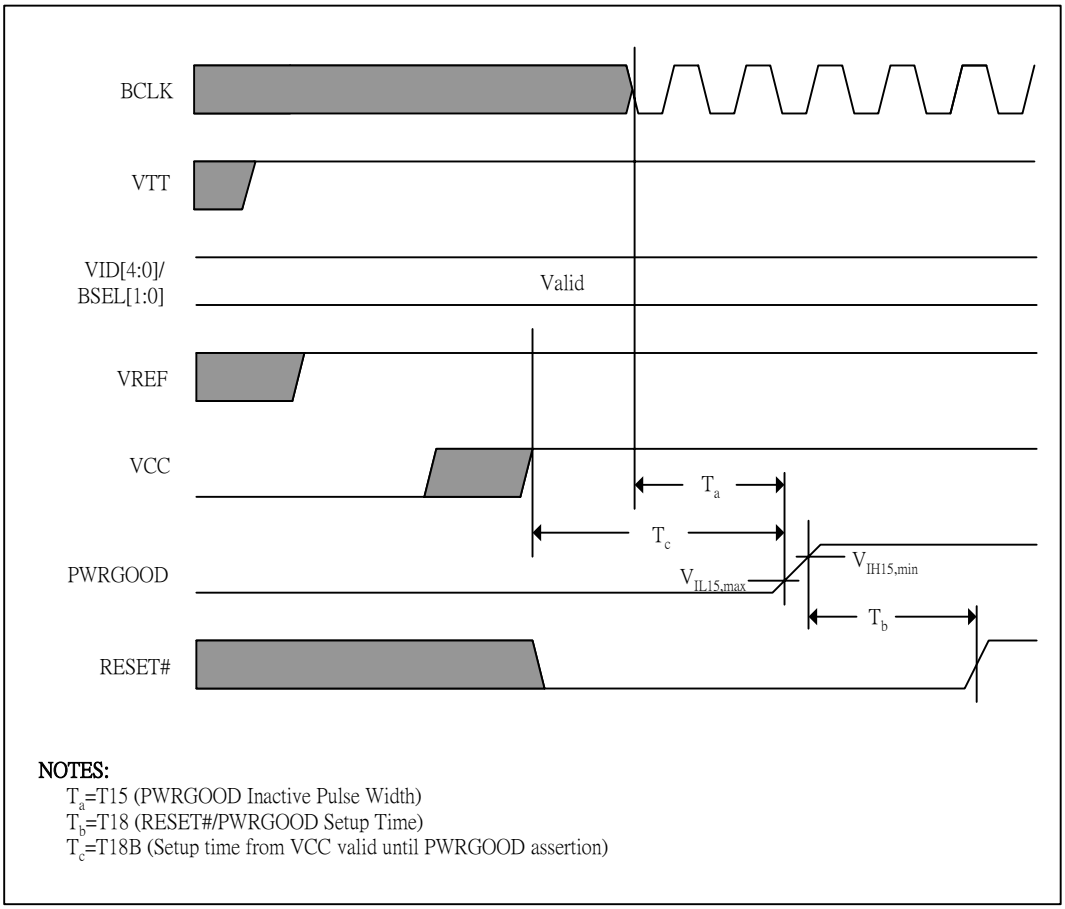


Figure 4-5. Power-on Sequence and Reset Timings

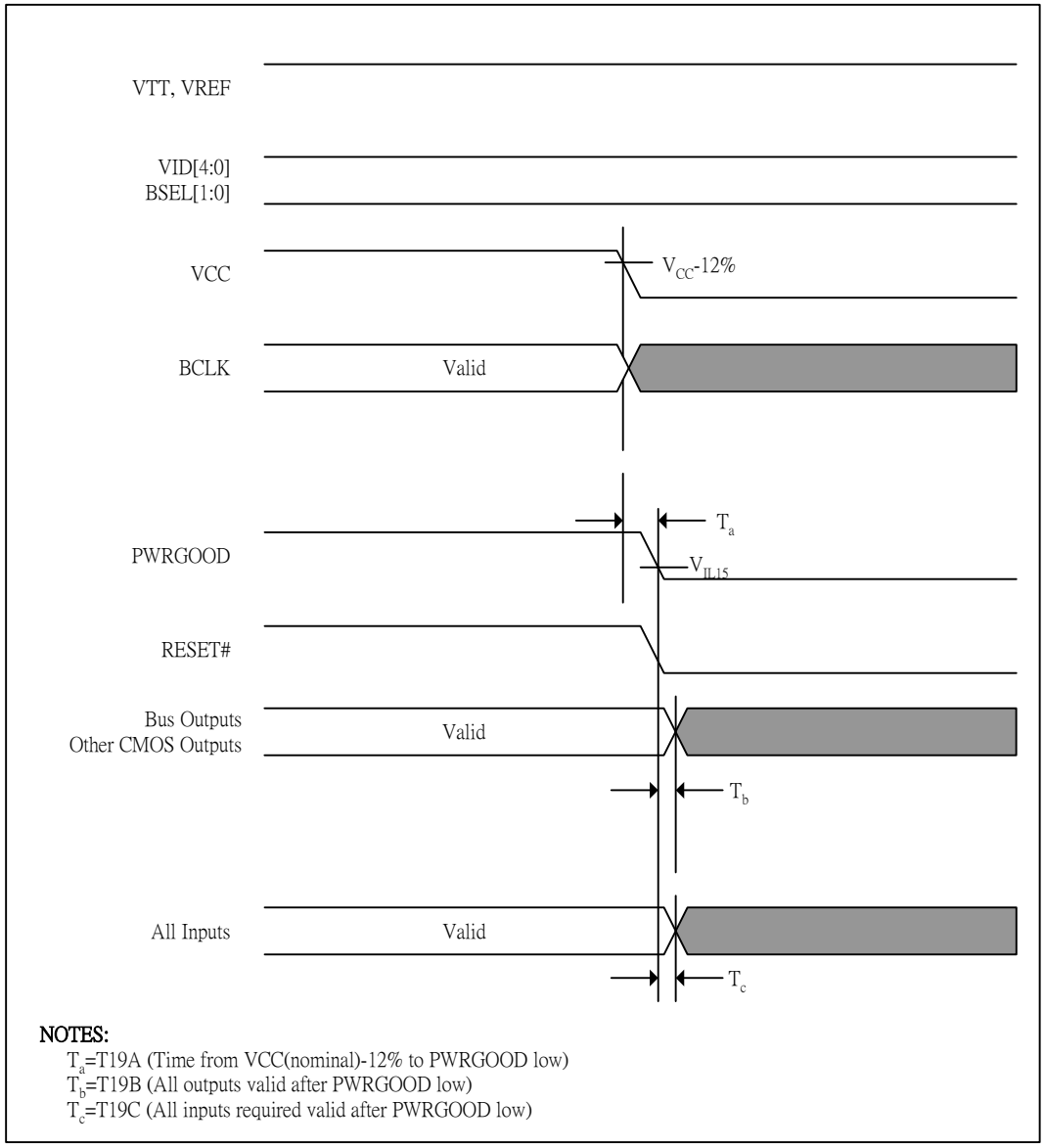


Figure 4-6. Power Down Sequencing and Timings (VCC Leading)

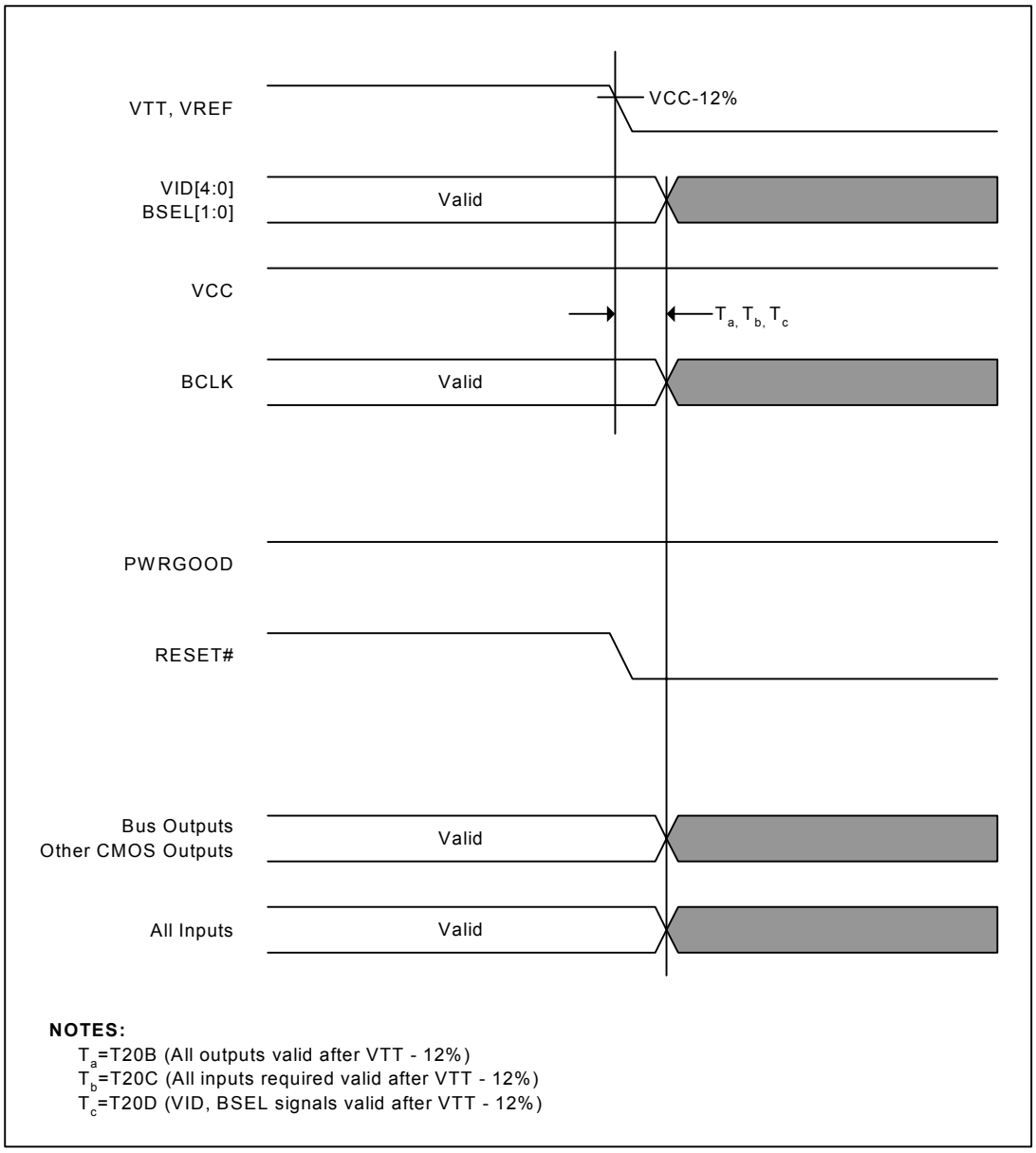
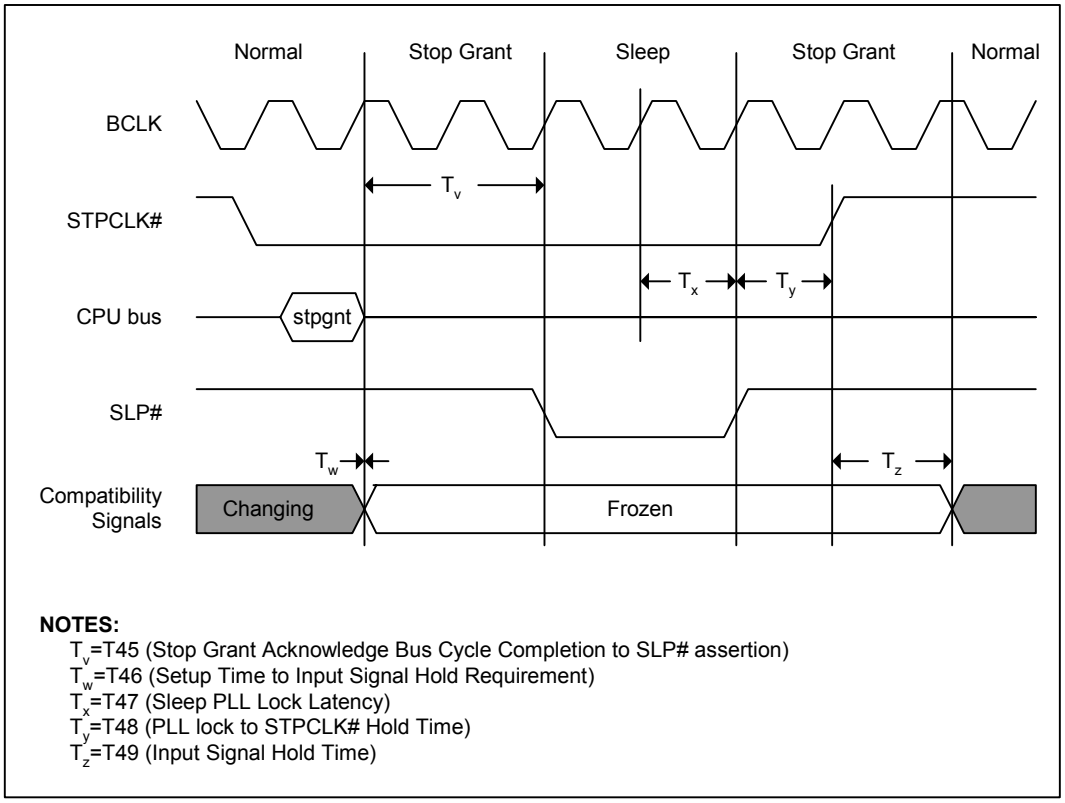
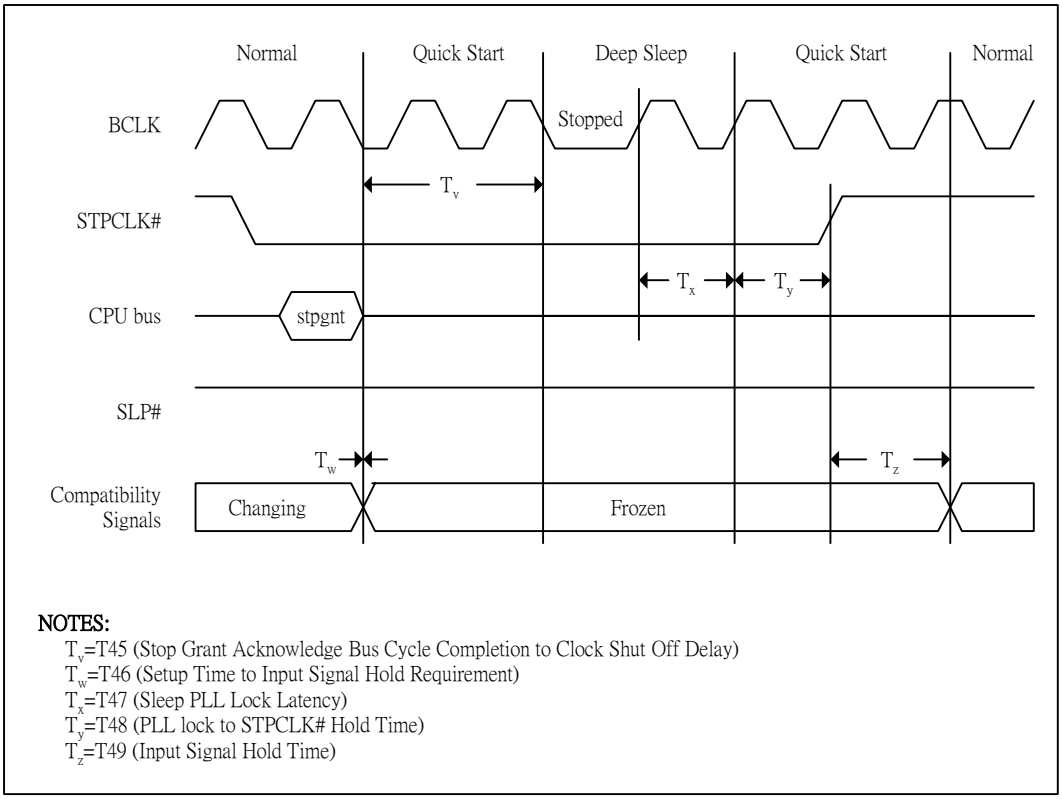


Figure 4-7. Power Down Sequencing and Timings (VTT Leading)



NOTES:
T_v=T45 (Stop Grant Acknowledge Bus Cycle Completion to SLP# assertion)
T_w=T46 (Setup Time to Input Signal Hold Requirement)
T_x=T47 (Sleep PLL Lock Latency)
T_y=T48 (PLL lock to STPCLK# Hold Time)
T_z=T49 (Input Signal Hold Time)

Figure 4-8. Stop Grant/Sleep Timing (SLP# assertion method)



NOTES:
T_v=T45 (Stop Grant Acknowledge Bus Cycle Completion to Clock Shut Off Delay)
T_w=T46 (Setup Time to Input Signal Hold Requirement)
T_x=T47 (Sleep PLL Lock Latency)
T_y=T48 (PLL lock to STPCLK# Hold Time)
T_z=T49 (Input Signal Hold Time)

Figure 4-9. Stop Grant/Deep Sleep Timing (BCLK Stopping method)

4.2 DC SPECIFICATIONS

4.2.1 RECOMMENDED OPERATING CONDITIONS

Functional operation of the VIA C3 Nehemiah processor is guaranteed if the conditions in Table 4-8 are met. Sustained operation outside of the recommended operating conditions may damage the device.

Table 4-8. Recommended Operating Conditions

PARAMETER	*MIN*	*NOM*	*MAX*	*UNITS*	*NOTES*
Operating Case Temperature	0		70	°C	CPGA
Operating Case Temperature	0		85	°C	EBGA
V_{CORE} Voltage		1.40		V	EBGA
V_{CORE} Voltage		1.45		V	CPGA
V_{CORE} Static Tolerance	See Table 4-9			V	(1)
V_{CORE} Dynamic Tolerance				V	(2)
V_{TT} Voltage		1.25		V	1.25V±3% (3)
V_{TT} Voltage	1.365	1.5	1.635	V	(4)
IV_{TT} Termination Supply Current			800	mA	(5)
V_{REF}	-2%	2/3 V_{TT}	+2%	V	
R_{TT}	50	56	115	Ω	(6)
$V_{1.5}$ – 1.5V Supply Voltage	1.365		1.635	V	

Notes:

1. DC measurement
2. AC noise measured with bandwidth limited to 20MHz
3. Universal Socket370 boards must hold VTT to 1.25V ±9% while the bus is active and 1.25V ±3% when bus is idle.
4. Legacy Socket370 boards
5. DC measurement. Measured with 250 µs sampling rate.
6. RTT is controlled by RTTCTRL pin. RTTCTRL should be 56Ω when relying upon on-die bus termination. RTTCTRL should be 110Ω when relying upon board termination.

Table 4-9. V_{CC} Static and Transient Tolerance

Icc (A)	Voltage Deviation from VID Setting (mV)			
	Static Tolerance		Transient Tolerance	
	Min	Max	Min	Max
0	**15**	**65**	**5**	**85**
2	**5**	**55**	**-5**	**74**
4	**-5**	**45**	**-15**	**62**
6	**-15**	**35**	**-25**	**51**
8	**-25**	**25**	**-35**	**40**
10	**-35**	**15**	**-45**	**28**
12	**-45**	**5**	**-55**	**17**
14	**-55**	**-5**	**-65**	**6**
16	**-65**	**-15**	**-76**	**-5**
18	**-75**	**-25**	**-87**	**-15**
20	**-85**	**-35**	**-98**	**-25**
22	**-95**	**-45**	**-110**	**-35**
24	**-105**	**-55**	**-121**	**-45**
26	**-115**	**-65**	**-132**	**-55**
28	**-125**	**-75**	**-144**	**-65**
30	**-135**	**-85**	**-155**	**-75**

4.2.2 MAXIMUM RATINGS

While functional operation is not guaranteed beyond the operating ranges listed in Table 4-8, the device may be subjected to the limits specified in Table 4-10 without causing long-term damage.

These conditions must not be imposed on the device for a sustained period—any such sustained imposition may damage the device. Likewise exposure to conditions in excess of the maximum ratings may damage the device.

Table 4-10. Maximum Ratings

PARAMETER	*MIN*	*MAX*	*UNITS*	*NOTES*
Storage Temperature	-65	150	°C	
Supply Voltage (V_{CC})	-0.5	1.7	V	
CMOS I/O Voltage	-0.5	V_{CMOS} +0.5	V	
I/O Voltage	-0.5	V_{TT} +0.5	V	

4.2.3 DC CHARACTERISTICS

Table 4-11. DC Characteristics

PARAMETER	*MIN*	*MAX*	*UNITS*	*NOTES*
I_{OL} – Low level output current	-9.0		mA	@ V = $V_{OL(max)}$
V_{OH} – High Level Output Voltage		V_{TT}	V	
V_{OL} – Low Level Output Voltage	0	0.4	V	@ I_{ol} = -8mA
I_L – Input Leakage Current		± 15	µA	
I_{LU} – Input Leakage Current for inputs with pull-ups		200	µA	
I_{LD} – Input Leakage Current for inputs with pull-downs		-400	µA	

Table 4-12. CMOS DC Characteristics

PARAMETER	*MIN*	*MAX*	*UNITS*	*NOTES*
V_{IL} -- Input Low Voltage	-0.58	0.700	V	
$V_{IH1.5}$ – Input High Voltage	V_{REF} + 0.2	V_{TT}	V	(2)
$V_{IH2.5}$ – Input High Voltage	2.0	3.18	V	(3)
V_{OL} – Low Level Output Voltage		0.40	V	@ I_{OL}
V_{OH} – High Level Output Voltage		V_{CMOS}	V	(1)
I_{OL} – Low Level Output Current	9		mA	@ V_{OL}
I_{LI} – Input Leakage Current		±100	µA	(4)
I_{LO} – Output Leakage Current		±100	µA	(4)

Notes:

1. All CMOS signals are open drain.
2. Applies to all CMOS signals except **BCLK**.
3. Applies only to **BCLK**.
4. Leakage current is specified for the range between VSS and VCC. I/O's are diode clamped to the VCC and VSS rails. **BCLK** has three series diodes between the input and VCC and a single diode between the input and VSS. All other signals have a single diode between the signal and VCC and another single diode between the signal and VSS.

4.2.4 POWER DISSIPATION

Table 4-13 gives the core power consumption for the VIA C3 Nehemiah processor at the various operating frequencies and voltages. Note that this does not include the power consumed by the I/O pads.

Table 4-13. Thermal Design Power Information

PARAMETER	TDP MAX[1,2]	UNITS	NOTES
Normal Mode			
Nehemiah 1.00 GHz (CPGA) 1.45V	15.0	W	
Nehemiah 1.13 GHz (CPGA) 1.45V	15.0	W	70°C, 3, 5
Nehemiah 1.20 GHz (CPGA) 1.45V	19.0	W	

Notes:

1. Maximum power is generated from running publicly available application software that consumes the most power. Synthetic applications or "thermal virus" applications may consume more power.
2. TDP Max is average value of all processors while running the worst case instruction sequence. Not 100% guaranteed or tested. Consider these power numbers as an average of all parts and some deviation is expected.
3. The above power consumption is preliminary and based on case temperature as noted.
4. All normal mode frequencies use 133MHz as the CPU clock frequency.
5. Conservative thermal solutions must be designed to account for worst-case core and I/O power consumption.

Table 4-14. $V_{TT-I/O}$ Power Consumption

PARAMETER	TYPICAL	MAX	UNITS	NOTES
$P_{TT-I/O}$ – I/O Operating Power Consumption	0.3	1.2	W	

SECTION

5

MECHANICAL SPECIFICATIONS

5.1 CPGA PACKAGE

The VIA C3 Nehemiah processor is available in a Ceramic Pin Grid Array (CPGA) package for Socket 370 motherboards.

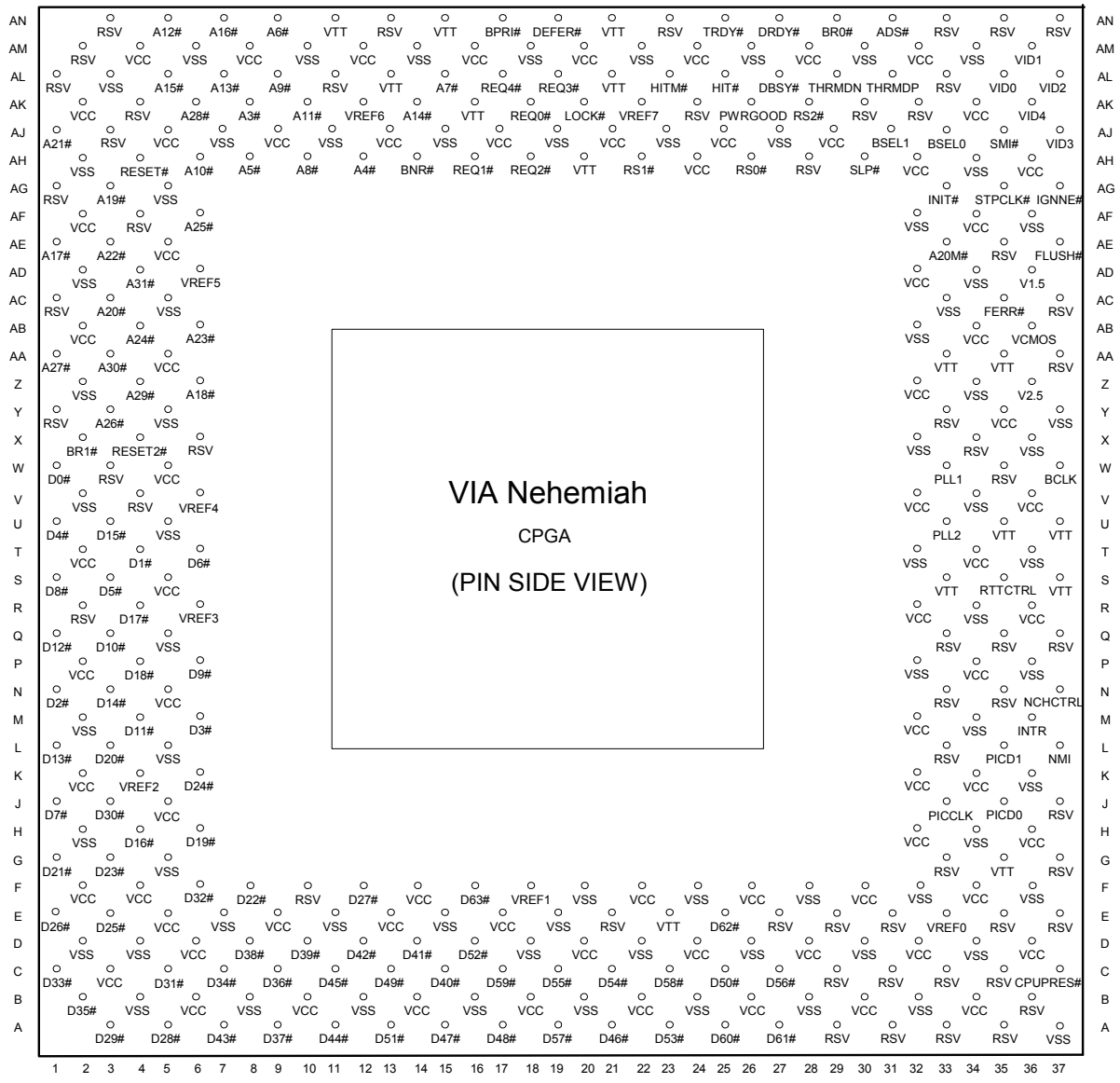


Figure 5-1. CPGA Pinout (Pinside View)

Table 5-1. CPGA Pin Cross Reference

Address		Data		Control		Power/other		VCC	VTT	VSS	Reserved
Name	Ball	Name	Ball	Name	Ball	Name	Ball	Ball	Ball	Ball	Ball
A3#	AK-8	D0#	W-1	A20M#	AE-33	CPUPRES#	C-37	AA-5	AH-20	AM-22	AK-24
A4#	AH-12	D1#	T-4	ADS#	AN-31	PLL1	W-33	AB-2	AK-16	AM-26	AL-11
A5#	AH-8	D2#	N-1	BCLK	W-37	PLL2	U-33	AB-34	AL-13	AM-30	AN-13
A6#	AN-9	D3#	M-6	BNR#	AH-14	$V_{1.5}$	AD-36	AD-32	AL-21	AM-34	V-4
A7#	AL-15	D4#	U-1	BPRI#	AN-17	$V_{2.5}$	Z-36	AE-5	AN-11	AM-6	B-36
A8#	AH-10	D5#	S-3	BR0#	AN-29	V_{CMOS}	AB-36	E-5	AN-15	B-12	G-33
A9#	AL-9	D6#	T-6	BR1#	X-2	VID0	AL-35	E-9	G-35	B-16	E-37
A10#	AH-6	D7#	J-1	BSEL0	AJ-33	VID1	AM-36	F-14	AA-33	B-20	C-35
A11#	AK-10	D8#	S-1	BSEL1	AJ-31	VID2	AL-37	F-2	AA-35	B-24	E-35
A12#	AN-5	D9#	P-6	DBSY#	AL-27	VID3	AJ-37	F-22	AN-21	B-28	C-33
A13#	AL-7	D10#	Q-3	DEFER#	AN-19	VID4	AK-36	F-26	E-23	B-32	C-31
A14#	AK-14	D11#	M-4	DRDY#	AN-27	V_{REF0}	E-33	F-30	S-33	B-4	A-33
A15#	AL-5	D12#	Q-1	FERR#	AC-35	V_{REF1}	F-18	F-34	S-37	B-8	A-31
A16#	AN-7	D13#	L-1	FLUSH#	AE-37	V_{REF2}	K-4	F-4	U-35	D-18	E-31
A17#	AE-1	D14#	N-3	HIT#	AL-25	V_{REF3}	R-6	H-32	U-37	D-2	C-29
A18#	Z-6	D15#	U-3	HITM#	AL-23	V_{REF4}	V-6	H-36		D-22	E-29
A19#	AG-3	D16#	H-4	IGNNE#	AG-37	V_{REF5}	AD-6	J-5		D-26	A-29
A20#	AC-3	D17#	R-4	INIT#	AG-33	V_{REF6}	AK-12	K-2		D-30	A-35
A21#	AJ-1	D18#	P-4	INTR	M-36	V_{REF7}	AK-22	K-32		D-34	G-37
A22#	AE-3	D19#	H-6	NMI	L-37	THERMDN	AL-29	K-34		D-4	L-33
A23#	AB-6	D20#	L-3	LOCK#	AK-20	THERMDP	AL-31	M-32		Z-34	N-33
A24#	AB-4	D21#	G-1	PWRGOOD	AK-26			N-5		E-11	N-35
A25#	AF-6	D22#	F-8	REQ0#	AK-18			P-2		E-15	Q-33
A26#	Y-3	D23#	G-3	REQ1#	AH-16			P-34		E-19	Q-35
A27#	AA-1	D24#	K-6	REQ2#	AH-18			R-32		E-7	Q-37
A28#	AK-6	D25#	E-3	REQ3#	AL-19			R-36		F-20	R-2
A29#	Z-4	D26#	E-1	REQ4#	AL-17			S-5		F-24	W-35
A30#	AA-3	D27#	F-12	RESET#	AH-4			T-2		F-28	Y-1
A31#	AD-4	D28#	A-5	RESET2#	X-4			T-34		F-32	AK-30
		D29#	A-3	RS0#	AH-26			V-32		F-36	AM-2
		D30#	J-3	RS1#	AH-22			V-36		G-5	F-10
		D31#	C-5	RS2#	AK-28			W-5		H-2	AN-23
		D32#	F-6	SLP#	AH-30			Y-35		H-34	AC-37
		D33#	C-1	SMI#	AJ-35			Z-32		K-36	AL-33
		D34#	C-7	STPCLK#	AG-35			AF-2		L-5	AN-35
		D35#	B-2	TRDY#	AN-25			AH-24		M-2	AN-37

Address		Data		Control		Power/other		VCC	VTT	VSS	Reserved
Name	Ball	Name	Ball	Name	Ball	Name	Ball	Ball	Ball	Ball	Ball
		D36#	C-9	RTTCTRL	S-35			AH-32		M-34	AH-28
		D37#	A-9	NCHCTRL	N-37			AH-36		P-32	AK-32
		D38#	D-8	PICCLK	J-33			AJ-13		P-36	AN-33
		D39#	D-10	PICD0	J-35			AJ-17		A-37	E-27
		D40#	C-15	PICD1	L-35			AJ-21		AB-32	AG-1
		D41#	D-14					AJ-25		AC-33	E-21
		D42#	D-12					AJ-29		AC-5	AC-1
		D43#	A-7					AJ-5		AD-2	W-3
		D44#	A-11					AK-2		AD-34	AF-4
		D45#	C-11					AK-34		AF-32	X-6
		D46#	A-21					AM-12		AF-36	Y-33
		D47#	A-15					AM-16		AG-5	J-37
		D48#	A-17					AM-20		AH-2	AE-35
		D49#	C-13					AM-24		AH-34	AA-37
		D50#	C-25					AM-28		AJ-11	AJ-3
		D51#	A-13					AM-32		AJ-15	AK-4
		D52#	D-16					AM-4		AJ-19	AL-1
		D53#	A-23					AM-8		AJ-23	X-34
		D54#	C-21					B-10		AJ-27	AN-3
		D55#	C-19					B-14		AJ-7	
		D56#	C-27					B-18		AL-3	
		D57#	A-19					B-22		AM-10	
		D58#	C-23					B-26		AM-14	
		D59#	C-17					B-30		AM-18	
		D60#	A-25					B-34		Q-5	
		D61#	A-27					B-6		R-34	
		D62#	E-25					C-3		T-32	
		D63#	F-16					D-20		T-36	
								D-24		U-5	
								D-32		V-2	
								D-36		V-34	
								D-6		X-32	
								E-13		X-36	
								E-17		Y-37	
								AJ-9		Y-5	
								D-28		Z-2	
								AF-34			

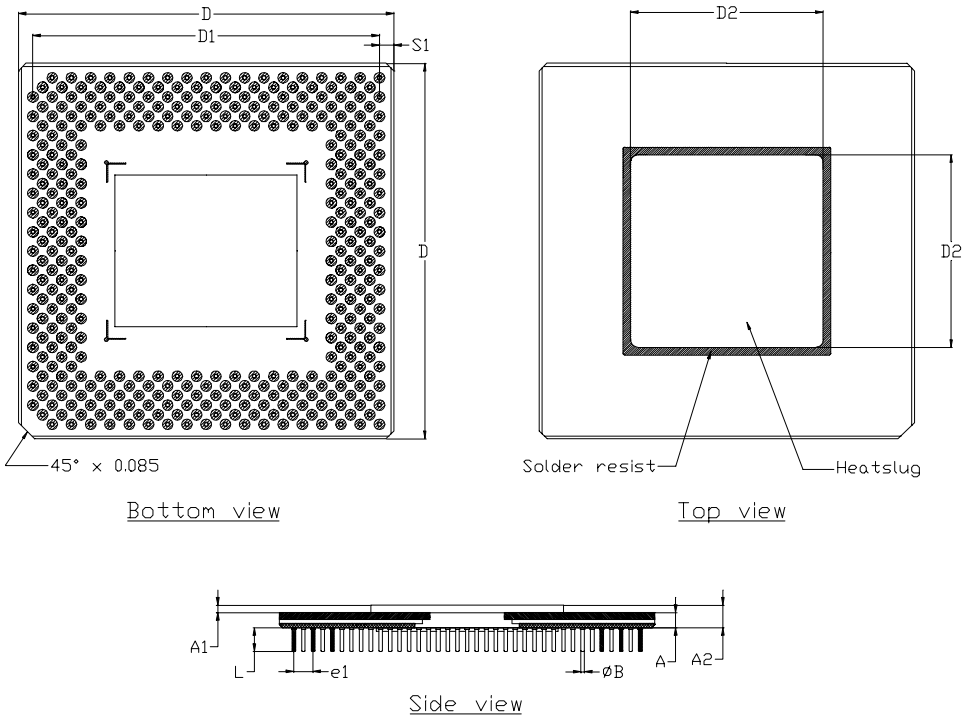
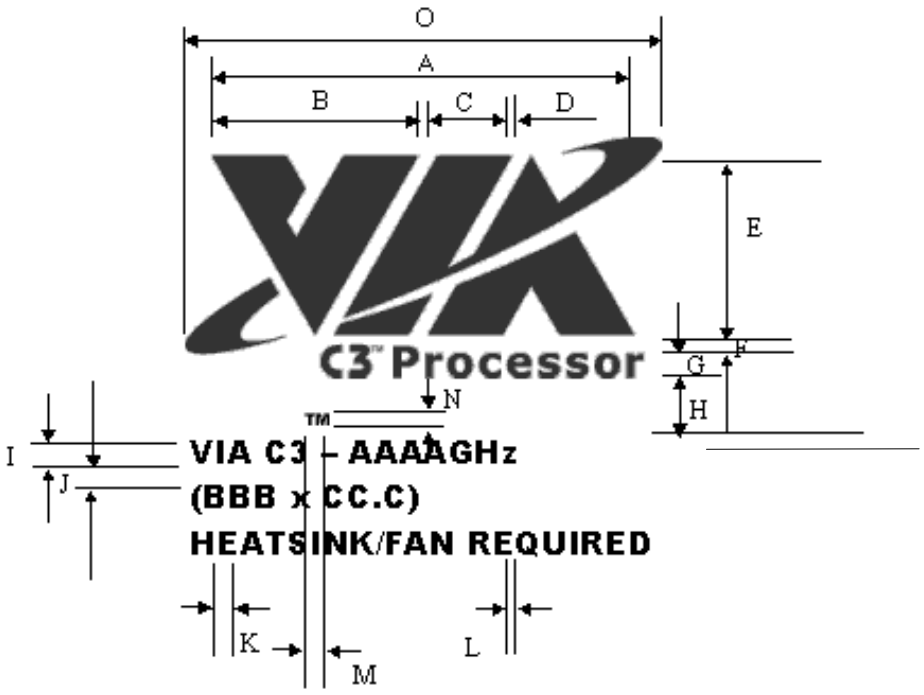


Figure 5-2. CPGA with Heat Slug Dimensions

Table 5-2. CPGA Package Dimensions

Symbol	Millimeters				Inches			
	Typical	Min	Max	Notes	Typical	Min	Max	Notes
A	1.96	1.76	2.16		0.077	0.069	0.085	
A1	1.00 typical				0.039 typical			
A2	2.96	2.72	3.33		0.116	0.107	0.131	
ϕB	0.046	0.41	0.51		0.018	0.016	0.020	
D	49.53	49.28	49.83		1.950	1.940	1.962	
D1	45.72	45.47	45.97		1.8	1.790	1.810	
D2	25.4	25.02	25.78		1.00	0.985	1.015	
e1	2.54	2.41	2.67		0.100	0.095	0.105	
L	3.18	2.98	3.38		0.125	0.117	0.133	
N	370			Lead count	370			Lead count
S1	1.905	1.65	2.16		0.075	0.065	0.085	



	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
Dimension	**18.40**	**9.18**	**3.24**	**0.81**	**7.74**	**0.50**	**1.15**	**1.75**	**1.28**	**0.65**	**0.78**	**0.22**	**1.54**	**0.96**	**19.70**

Units: MM

Speed Code: Core Speed and FSB Speed

AAA	BBB	CC.C	Description
1.4	100	14.0	**1.4AGHz**
1.4	133	10.5	**1.4AGHz**
1.3	133	10.0	**1.3AGHz**
1.3	100	13.0	**1.3AGHz**
1.2	100	12.0	**1.2AGHz**
1.2	133	9.0	**1.2AGHz**
1.1	100	11.0	**1.1AGHz**
1.0	100	10.0	**1.0AGHz**
1.0	133	7.5	**1.0AGHz**

Figure 5-3. CPGA Top Marking Design

5.2 EBGA PACKAGE

The VIA C3 Nehemiah in EBGA is packaged in a unique enhanced ball grid array that facilitates compact and economical surface mounting. The VIA C3 Nehemiah in EBGA bus is functionally similar to Socket 370 used by conventional CPGA VIA C3 Nehemiah's but is obviously not mechanically compatible.

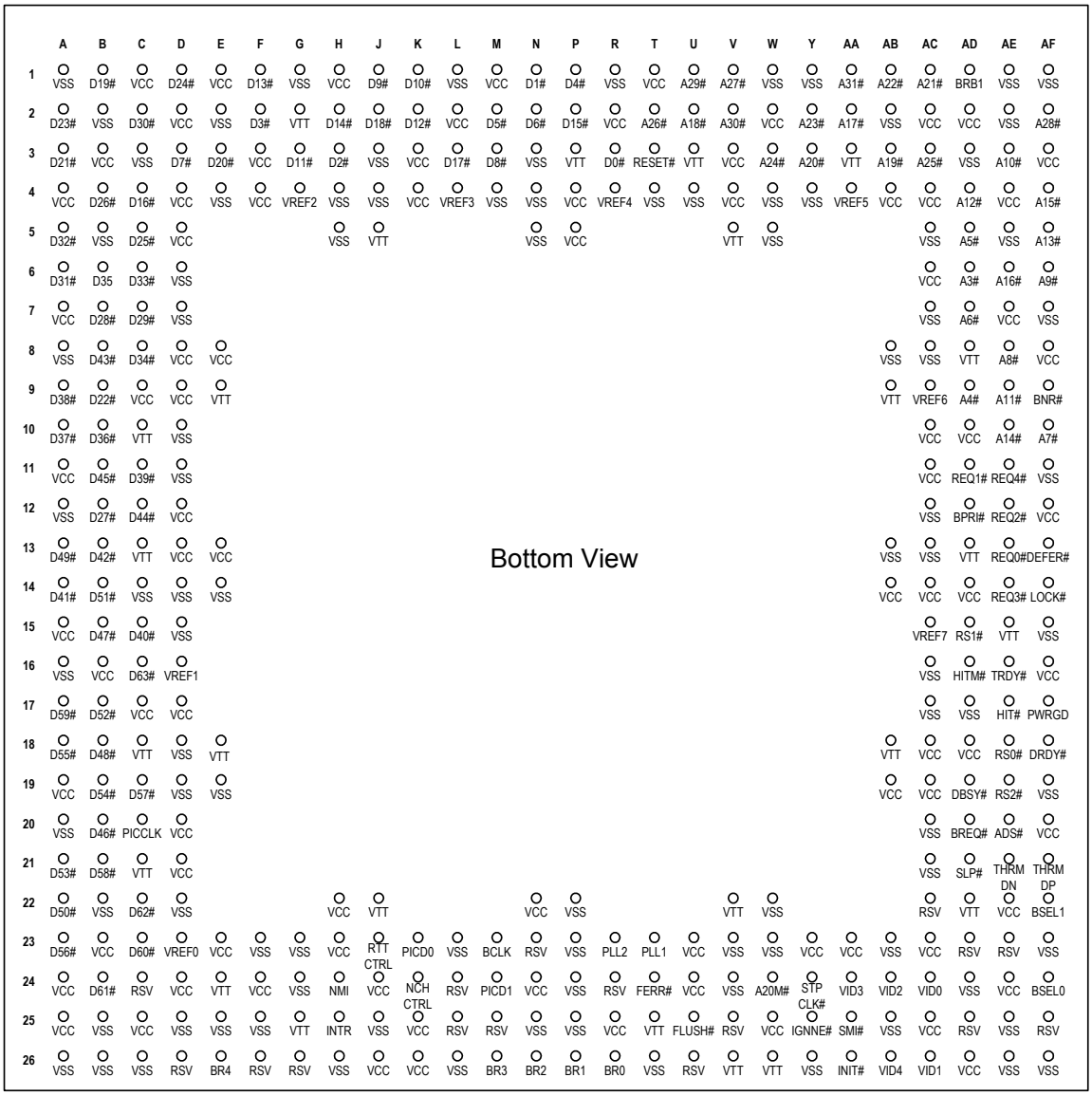


Figure 5-4. EBGA Ball Diagram (Bottom View)

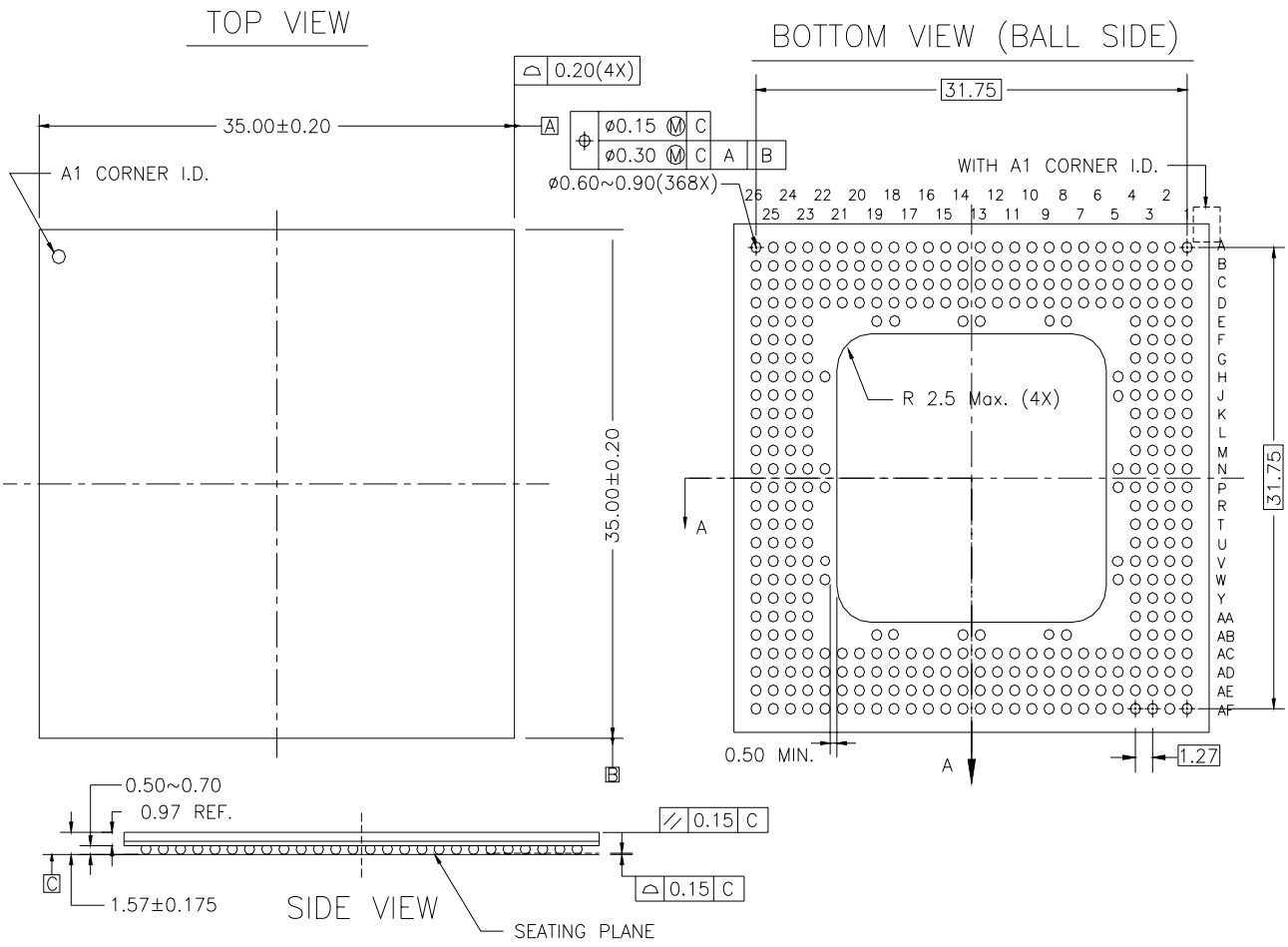
Table 5-3. EBGA Ball Cross Reference

Address		Data		Control		Power/other		VCC	VTT	VSS	Reserved
Name	Ball	Name	Ball	Name	Ball	Name	Ball	Ball	Ball	Ball	Ball
A3#	AD-6	D0#	R-3	A20M#	W-24	PLL1	T-23	A-11	AA-3 [1]	A-1	R-24
A4#	AD-9	D1#	N-1	ADS#	AE-20	PLL2	R-23	A-15	AD-13 [1]	A-12	AC-22
A5#	AD-5	D2#	H-3	BCLK	M-23	THERMDN	AE-21	A-19	AD-22 [1]	A-16	AE-23
A6#	AD-7	D3#	F-2	BNR#	AF-9	THERMDP	AF-21	A-24	AD-8 [1]	A-20	AD-25
A7#	AF-10	D4#	P-1	BPRI#	AD-12	VID0	AC-24	A-25	AE-15 [1]	A-26	AD-23
A8#	AE-8	D5#	M-2	BREQ#	AD-20	VID1	AC-26	A-4	C-10 [1]	A-8	AF-25
A9#	AF-6	D6#	N-2	BSEL0	AF-24	VID2	AB-24	A-7	C-13 [1]	AB-13	G-26
A10#	AE-3	D7#	D-3	BSEL1	AF-22	VID3	AA-24	AA-23	C-18 [1]	AB-2	D-26
A11#	AE-9	D8#	M-3	DBSY#	AD-19	VID4	AB-26	AB-19	C-21 [1]	AB-23	F-26
A12#	AD-4	D9#	J-1	DEFER#	AF-13	VREF0	D-23	AB-4	E-24 [1]	AB-25	L-25
A13#	AF-5	D10#	K-1	DRDY#	AF-18	VREF1	D-16	AB-14	G-2 [1]	AB-8	M-25
A14#	AE-10	D11#	G-3	FERR#	T-24	VREF2	G-4	AC-10	G-25 [1]	AC-12	V-25
A15#	AF-4	D12#	K-2	FLUSH#	U-25	VREF3	L-4	AC-11	P-3 [1]	AC-13	U-26
A16#	AE-6	D13#	F-1	HIT#	AE-17	VREF4	R-4	AC-14	T-25 [1]	AC-16	C-24
A17#	AA-2	D14#	H-2	HITM#	AD-16	VREF5	AA-4	AC-18	U-3 [1]	AC-17	L-24
A18#	U-2	D15#	P-2	IGNNE#	Y-25	VREF6	AC-9	AC-19	W-26 [1]	AC-20	N-23
A19#	AB-3	D16#	C-4	INIT#	AA-26	VREF7	AC-15	AC-2	V-26 [1]	AC-21	
A20#	Y-3	D17#	L-3	INTR	H-25			AC-23	AB-9	AC-5	
A21#	AC-1	D18#	J-2	LOCK#	AF-14			AC-25	AB-18	AC-7	
A22#	AB-1	D19#	B-1	NMI	H-24			AC-4	V-5	AC-8	
A23#	Y-2	D20#	E-3	PWRGD	AF-17			AC-6	V-22	AD-17	
A24#	W-3	D21#	A-3	REQ0#	AE-13			AD-10	J-5	AD-24	
A25#	AC-3	D22#	B-9	REQ1#	AD-11			AD-14	J-22	AD-3	
A26#	T-2	D23#	A-2	REQ2#	AE-12			AD-18	E-9	AE-1	
A27#	V-1	D24#	D-1	REQ3#	AE-14			AD-26	E-18	AE-2	
A28#	AF-2	D25#	C-5	REQ4#	AE-11			AD-2		AE-25	
A29#	U-1	D26#	B-4	RESET#	T-3			AE-22		AE-26	
A30#	V-2	D27#	B-12	RS0#	AE-18			AE-24		AE-5	
A31#	AA-1	D28#	B-7	RS1#	AD-15			AE-4		AF-1	

Address		Data		Control		Power/other		V_{CC}	VTT	VSS	Reserved
		D29#	C-7	RS2#	AE-19			AF-20		AF-23	
		D30#	C-2	SMI#	AA-25			AF-3		AF-26	
		D31#	A-6	STPCLK#	Y-24			AF-8		AF-7	
		D32#	A-5	TRDY#	AE-16			B-16		B-2	
		D33#	C-6	BR0	R-26			B-23		B-22	
		D34#	C-8	BR1	P-26			B-3		B-25	
		D35#	B-6	BR2	N-26			C-1		B-26	
		D36#	B-10	BR3	M-26			C-17		B-5	
		D37#	A-10	BR4	E-26			C-25		C-14	
		D38#	A-9	NCHCTRL	K-24			C-9		C-3	
		D39#	C-11	PICCLK	C-20			D-12		C-26	
		D40#	C-15	PICD0	K-23			D-13		D-10	
		D41#	A-14	PICD1	M-24			D-17		D-11	
		D42#	B-13	BRB1	AD-1			D-2		D-14	
		D43#	B-8					D-20		D-15	
		D44#	C-12					D-21		D-18	
		D45#	B-11					D-24		D-19	
		D46#	B-20					D-4		D-22	
		D47#	B-15					D-5		D25	
		D48#	B-18					D-8		D-6	
		D49#	A-13					D-9		D-7	
		D50#	A-22					E-1		E-14	
		D51#	B-14					E-13		E-19	
		D52#	B-17					E-23		E-2	
		D53#	A-21					E-8		E-25	
		D54#	B-19					F-24		E-4	
		D55#	A-18					F-3		F-23	
		D56#	A-23					F-4		F-25	
		D57#	C-19					H-1		G-1	
		D58#	B-21					H-22		G-23	
		D59#	A-17					H-23		G-24	
		D60#	C-23					J-24		H-26	

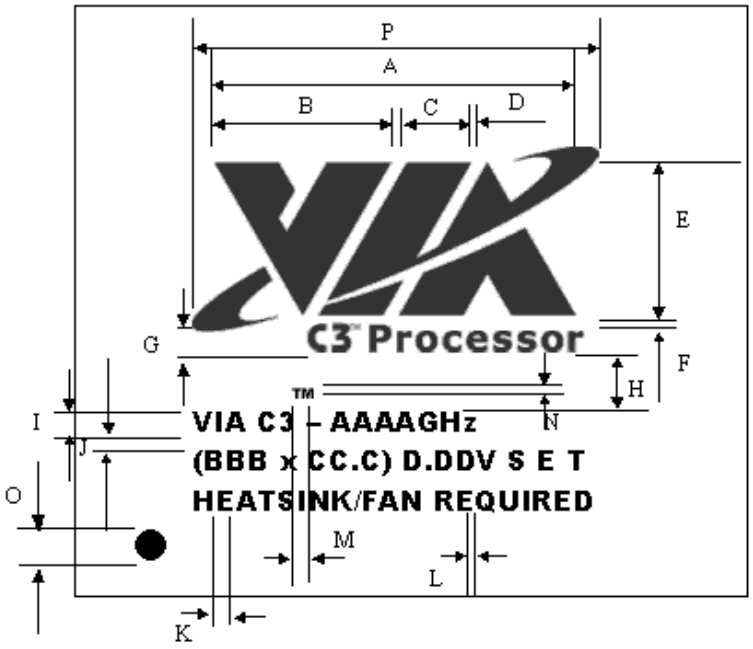
Address		Data		Control		Power/other		V_{CC}	VTT	VSS	Reserved
		D61#	B-24					J-26		H-4	
		D62#	C-22					K-25		H-5	
		D63#	C-16					K-26		J-25	
								K-3		J-3	
								K-4		J-4	
								L-2		L-1	
								M-1		L-23	
								N-22		L-26	
								N-24		M-4	
								P-4		N-25	
								P-5		N-3	
								R-2		N-4	
								R-25		N-5	
								T-1		P-22	
								U-23		P-23	
								U-24		P-24	
								V-3		P-25	
								V-4		R-1	
								W-2		T-26	
								W-25		T-4	
								Y-23		U-4	
								AE-7		V-23	
								AF-12		V-24	
								AF-16		W-1	
								AF-20		W-4	
										W-5	
										W-22	
										W-23	
										Y-1	
										Y-4	
										Y-26	

Address		Data		Control		Power/other		V_{CC}	VTT	VSS	Reserved
										AF-11	
										AF-15	
										AF-19	



Allowable Pressure on the top of the package is 800 kPa (116 Psi)

Figure 5-5. EBGA Mechanical Specification



Remark:

1.The "S" means the clock ratio can be adjusted by M/B jumper.

2.The "E" means the temperature of case will not be higher than 85℃.

3.The "T" means termination on die.

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
Dimension	**18.40**	**9.18**	**3.24**	**0.81**	**7.74**	**0.50**	**1.15**	**1.75**	**1.28**	**0.65**	**0.78**	**0.22**	**1.54**	**0.96**	**1.30**	**19.70**

Units: MM

Speed Code: Core Speed and FSB Speed

AAA	BBB	CC.C	Description
1.4	100	14.0	**1.4AGHz**
1.4	133	10.5	**1.4AGHz**
1.3	133	10.0	**1.3AGHz**
1.3	100	13.0	**1.3AGHz**
1.2	100	12.0	**1.2AGHz**
1.2	133	9.0	**1.2AGHz**
1.1	100	11.0	**1.1AGHz**
1.0	100	10.0	**1.0AGHz**
1.0	133	7.5	**1.0AGHz**

Figure 5-6. EBGA Top Marking Design

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SECTION

6

THERMAL SPECIFICATIONS

6.1 INTRODUCTION

The VIA C3 Nehemiah is specified for operation with device case temperatures in the range of 0°C to 70°C (85°C for EBGA). Operation outside of this range will result in functional failures and may potentially damage the device.

Care must be taken to ensure that the case temperature remains within the specified range at all times during operation. An effective heat sink with adequate airflow is therefore a requirement during operation.

6.2 TYPICAL ENVIRONMENTS

Typical thermal solutions involve three components: a heat sink, an interface material between the heat sink and the package, and a source of airflow. The best thermal solutions rely on the use of all three components. To the extent that any of these components are not used, the other components must be improved to compensate for such omission. In particular, the use of interface material such as thermal grease, silicone paste, or graphite paper can make a 40°C difference in the case temperature. Likewise, the imposition of airflow is realistically a requirement.

6.3 MEASURING T_C

The case temperature (T_C) should be measured by attaching a thermocouple to the center of the VIA C3 Nehemiah package. The heat produced by the processor is very localized so measuring the case temperature anywhere else will underestimate the case temperature.

The presence of a thermocouple is inherently invasive; effort must be taken to minimize the effect of the measurement. The thermocouple should be attached to the processor through a small hole drilled in the heat sink. Thermal grease should be used to ensure that the thermocouple makes good contact with the package, but the thermocouple should not come in direct contact with the heat sink.

Physical Test Conditions

Case temperature measurements should be made in the worst case operating environments. Ideally, systems should be maximally configured, and tested at the worst-case ambient temperature.

Test Patterns

During normal operation the processor attempts to minimize power consumption. Consequently, normal power consumption is much lower than the maximum power consumption. Thermal testing should be done while running software which causes the processor to operate at its thermal limits.

6.4 MEASURING T_J

The junction temperature of the die can be measured by using the processor's on-chip diode.

6.5 ESTIMATING T_C

The VIA C3 Nehemiah processor's case temperature can be estimated based on the general characteristics of the thermal environment. This estimate is not intended as a replacement for actual measurement.

Case temperature can be estimated where,

$T_A \equiv$ Ambient Temperature

$T_C \equiv$ Case Temperature

$\theta_{CA} \equiv$ case-to-ambient thermal resistance

$\theta_{JA} \equiv$ junction-to-ambient thermal resistance

$\theta_{JC} \equiv$ junction-to-case thermal resistance

$P \equiv$ power consumption (Watts)

and,

$T_J = T_C + (P * \theta_{JC})$

$T_A = T_J - (P * \theta_{JA})$

$T_A = T_C - (P * \theta_{CA})$

$\theta_{CA} = \theta_{JA} - \theta_{JC}$

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APPENDIX

A

MACHINE SPECIFIC REGISTERS

A.1 GENERAL

Tables A-1 and A-2 summarize the VIA C3 Nehemiah processor machine-specific registers (MSRs). Further description of each MSR follows the table. MSRs are read using the RDMSR instruction and written using the WRMSR instruction.

There are four basic groups of MSRs (not necessarily with contiguous addresses). Other than as defined below, a reference to an undefined MSR causes a General Protection exception.

1. Generally these registers can have some utility to low-level programs (like BIOS).

   Note that some of the MSRs (address 0 to 0x4FF) have no function in the VIA C3 Nehemiah processor. These MSRs do not cause a GP when used on the VIA C3 Nehemiah processor; instead, reads to these MSRs return zero, and writes are ignored. Some of these undocumented MSRs may have ill side effects when written to indiscriminately. Do not write to undocumented MSRs.

2. There are some undocumented internal-use MSRs used for low-level hardware testing purposes. Attempts to read or write these undocumented MSRs cause unpredictable and disastrous results; so don't use MSRs that are not documented in this datasheet!

3. MSRs used for cache and TLB testing. These use MSR addresses that are not used on compatible processor. These test functions are very low-level and complicated to use. They are not documented in this datasheet but the information will be provided to customers given an appropriate justification

MSRs are not reinitialized by the bus INIT interrupt; the setting of MSRs is preserved across INIT.

Table A-1. Category 1 MSRs

MSR	*MSR NAME*	*ECX*	*EDX*	*EAX*	*TYPE*	*NOTES*
TSC	Time Stamp Counter	10h	TSC[63:32]	TSC[31:0]	RW	
EBL_CR_POWERON	EBL_CR_POWERON	2Ah	n/a	Control bits	RW	
PERFCTR0	Performance counter 0	C1h	TSC[39:32]	TSC[31:0]	RW	1
PERFCTR1	Performance counter 1	C2h	0	Count[31:0]	RW	
BBL_CR_CTL3	L2 Hardware Disabled	11Eh	n/a	00800000h	RO	
EVNTSEL0	Event counter 0 select	186h	n/a	00470079h	RO	1
EVNTSEL1	Event counter 1 select	187h	n/a	Control bits	RW	
MTRR	MTRRphysBase0	200h	Control bits	Control bits	RW	
MTRR	MTRRphysMask0	201h	Control bits	Control bits	RW	
MTRR	MTRRphysBase1	202h	Control bits	Control bits	RW	
MTRR	MTRRphysMask1	203h	Control bits	Control bits	RW	
MTRR	MTRRphysBase2	204h	Control bits	Control bits	RW	
MTRR	MTRRphysMask2	205h	Control bits	Control bits	RW	
MTRR	MTRRphysBase3	206h	Control bits	Control bits	RW	
MTRR	MTRRphysMask3	207h	Control bits	Control bits	RW	
MTRR	MTRRphysBase4	208h	Control bits	Control bits	RW	
MTRR	MTRRphysMask4	209h	Control bits	Control bits	RW	
MTRR	MTRRphysBase5	20Ah	Control bits	Control bits	RW	
MTRR	MTRRphysMask5	20Bh	Control bits	Control bits	RW	
MTRR	MTRRphysBase6	20Ch	Control bits	Control bits	RW	
MTRR	MTRRphysMask6	20Dh	Control bits	Control bits	RW	
MTRR	MTRRphysBase7	20Eh	Control bits	Control bits	RW	
MTRR	MTRRphysMask7	20Fh	Control bits	Control bits	RW	
MTRR	MTRRfix64K_00000	250h	Control bits	Control bits	RW	
MTRR	MTRRfix16K_80000	258h	Control bits	Control bits	RW	
MTRR	MTRRfix16K_A0000	259h	Control bits	Control bits	RW	
MTRR	MTRRfix4K_C0000	268h	Control bits	Control bits	RW	
MTRR	MTRRfix4K_C8000	269h	Control bits	Control bits	RW	
MTRR	MTRRfix4K_D0000	26Ah	Control bits	Control bits	RW	
MTRR	MTRRfix4K_D8000	26Bh	Control bits	Control bits	RW	
MTRR	MTRRfix4K_E0000	26Ch	Control bits	Control bits	RW	
MTRR	MTRRfix4K_E8000	26Dh	Control bits	Control bits	RW	
MTRR	MTRRfix4K_F0000	26Eh	Control bits	Control bits	RW	
MTRR	MTRRfix4K_F8000	26Fh	Control bits	Control bits	RW	
MTRR	MTRRdefType	2FFh	Control bits	Control bits	RW	

Notes:

1. PERFCTR0 is an alias for the lower 40 bits of the Time Stamp Counter. EVNTSEL0 is a read only MSR that reflects this limitation.

Table A-2. Category 2 MSRs

MSR	*MSR NAME*	*ECX*	*EDX*	*EAX*	*TYPE*	*NOTES*
FCR	Feature Control Reg	1107h	n/a	FCR value	RW	
FCR2	Feature Control Reg 2	1108h	FCR2_Hi	FCR2 value	RW	1
FCR3	Feature Control Reg 3	1109h	FCR3_Hi	FCR3 value	WO	1

Notes:

1. FCR2 and FCR3 provide system software with the ability to specify the Vendor ID string returned by the CPUID instruction.

A.2 CATEGORY 1 MSRS

10H: TSC (TIME STAMP COUNTER)

VIA C3 Nehemiah processor has a 64-bit MSR that materializes the Time Stamp Counter (TSC). System increments the TSC once per processor clock. The TSC is incremented even during AutoHalt or Stop-Clock. A WRMSR to the TSC will clear the upper 32 bits of the TSC.

2AH: EBL_CR_POWERON

31:27	27	26	25:22	21:20	19:18	17:15	14	13	12:0
Res '11000'	BF4	Low-PowerEn '1'	BF[3:0]	*Res*	BSEL	*Res*	1MPOV	IOQDepth	*Reserved (Ignored on write; returns 0 on read)*
5	1	1	4	2	2	3	1	1	13

IOQDepth: 0 = In Order Queue Depth with up to 8 transactions
1 = 1 transaction

1MPOV: 0 = Power on Reset Vector at 0xFFFFFFF0 (4Gbytes)
1 = Power on Reset Vector at 0x000FFFF0 (1 Mbyte)

BSEL: 01 = 133 MHz Bus
10 = 100 MHz Bus

BF[4:0]: Bus Clock Frequency Ratio

Nehemiah	MSR 0x2A [27]	MSR 0x2A [25:22]
5.0	0	0000b
16.0	0	0001b
Reserved	0	0010b
10.0	0	0011b
5.5	0	0100b
Reserved	0	0101b
Reserved	0	0110b
9.5	0	0111b
9.0	0	1000b
7.0	0	1001b
8.0	0	1010b
6.0	0	1011b
12.0	0	1100b
7.5	0	1101b
8.5	0	1110b
6.5	0	1111b
9.0	1	0000b
Reserved in Steppings 0 &1 11.0 otherwise	1	0001b
12.0	1	0010b
10.0	1	0011b
13.5	1	0100b
11.5	1	0101b
12.5	1	0110b
10.5	1	0111b
13.0	1	1000b
15.0	1	1001b
16.0	1	1010b
14.0	1	1011b
12.0	1	1100b
15.5	1	1101b
Reserved	1	1110b
14.5	1	1111b

LowPowerEn: This bit always set to '1'

C1H-C2H: PERFCTR0 & PERFCTR1

These are events counters 0 and 1. VIA C3 Nehemiah processor's PERFCTR0 is an alias for the lower 40 bits of the TSC.

11EH: BBL_CR_CTL3

31:24	23	22:0
Reserved	L2_Hdw_Disable '1'	*Reserved* *(Ignored on write;* *returns 0 on read)*
8	1	23

The VIA C3 Nehemiah processor does contain an L2 cache. For compatibility, this read-only MSR indicates to the BIOS or system software that the L2 is disabled even if the L2 is enabled.

L2_Hdw_Disable: This bit always set to '1'

186H: EVNTSEL0 (EVENT COUNTER 0 SELECT)

31:24	23:16	15:9	8:0
Reserved	*Reserved*	*Reserved*	CTR0 Event Select = 79h
8	8	7	9

PERFCTR0 is an alias for the lower 40 bits of the Time Stamp Counter. EVNTSEL0 is a read only MSR which reflects this limitation. The CTR0_Event Select field always returns 0x0079, which corresponds to counting of processor clocks.

187H: EVNTSEL1 (EVENT COUNTER 1 SELECT)

31:24	23:16	15:9	8:0
Reserved	*Reserved*	*Reserved*	CTR1 Event Select
8	8	7	9

VIA C3 Nehemiah processor have two MSRs that contain bits defining the behavior of the two hardware event counters: PERFCTR0 and PERFCTR1.

The CTR1_Event_Select control field defines which of several possible events is counted. The possible Event Select values for PERFCTR1 are listed in the table below. Note that CTR1_Event_Select is a 9-bit field.

The EVNTSEL1 register should be written before PERFCTR1 is written to initialize the counter. The counts are not necessarily perfectly exact; the counters are intended for use over a large number of events and may differ by one or two counts from what might be expected.

Most counter events are internal implementation-dependent debug functions, having no meaning to software. The counters that can have end-user utility are:

EVENT	***DESCRIPTION***
C0h	Instructions executed
1C0h	Instructions executed and string iterations
79h	Internal clocks (default event for CTR0)

A.3 CATEGORY 2 MSRS

1107H: FCR (FEATURE CONTROL REGISTER)

The FCR controls the major optional feature capabilities of the VIA C3 Nehemiah processor. Table A-3 contains the bit values for the FCR. The default settings shown for the FCR bits are not necessarily exact. The actual settings can be changed as part of the manufacturing process and thus a particular VIA C3 Nehemiah processor version can have slightly different default settings than shown here. All reserved bit values of the FCR must be preserved by using a read-modify-write sequence to update the FCR.

Table A-3. FCR Bit Assignments

BIT	NAME	DESCRIPTION	DEFAULT
0	ALTINST	*Reserved for test & special uses*	0
1	ECX8	Enables CPUID reporting CX8	1
2		*Reserved*	1
3		*Reserved*	0
4		*Reserved*	0
5	DSTPCLK	Disables supporting STPCLK	0
6		*Reserved*	0
7	EPGE	Enables CR4.PGE and CPUID.PGE (Page Global Enable)	1
8	DL2	Disables L2 Cache	0
9		*Reserved*	1
10		*Reserved*	0
11		*Reserved*	0
12	EBRPRED	Enables Branch Prediction	1
13	DIC	Disables I-Cache	0
14	DDC	Disables D-Cache	0
31:15		*Reserved*	0/1

ALTINST: 0 = Normal x86 instruction execution.

1 = Alternate instruction set execution is enabled (see details below)

ECX8: 0 = The CPUID instruction does not report the presence of the CMPXCHG8B instruction (CX8 = 0). The instruction actually exists and operates correctly, however.

1 = The CPUID instruction reports that the CMPXCHG8B instruction is supported (CX8 = 1).

DSTPCLK: 0 = STPCLK interrupt properly supported.

1 = Ignores SPCLK interrupt.

EPGE: 0 = The processor does not support Page Global Enable and therefore CPUID Feature Flags reports EDX[13]=0; attempts to set CR4.PGE are ignored.

1 = The processor supports Page Global Enable and therefore CPUID Feature Flags reports EDX[13]=1; CR4.PGE can be set to 1.

DL2: 0 = L2 Cache enabled.

1 = L2 Cache disabled.

EBRPRED: 0 = Disables branch prediction function.

1 = Enables branch prediction function.

DIC: 0 = Enables use of I-Cache.

1 = Disables use of I-Cache: cache misses are performed as single transfer bus cycles, PCD is de-asserted. This overrides any setting of CR0.CD and CR0.NW.

DDC: 0 = Enables use of D-Cache.

1 = Disables use of D-Cache: same semantics as for DIC except for D-Cache.

ALTERNATE INSTRUCTION EXECUTION

When set to 1, the ALTINST bit in the FCR enables execution of an alternate (not x86) instruction set. While setting this FCR bit is a privileged operation, executing the alternate instructions can be done from any protection level.

This alternate instruction set includes an extended set of integer, MMX, floating-point, and 3DNow! instructions along with additional registers and some more powerful instruction forms over the x86 instruction architecture. For example, in the alternate instruction set, privileged functions can be used from any protection level, memory descriptor checking can be bypassed, and many x86 exceptions such as alignment check can be bypassed.

This alternate instruction set is intended for testing, debug, and special application usage. Accordingly, it is not documented for general usage. If you have a justified need for access to these instructions, contact your VIA representative.

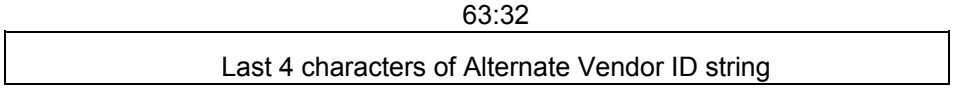
The mechanism for initiating execution of this alternate set of instructions is as follows:

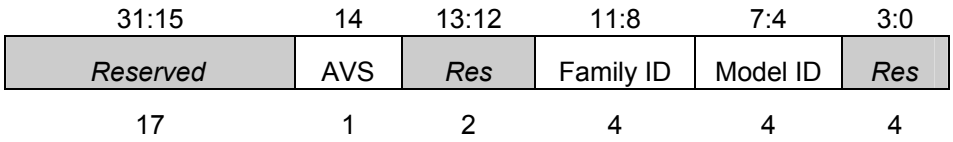
1. Set the FCR ALTINST bit to 1 using WRMSR instruction (this is a privileged instruction). This should be done using a read-modify-write sequence to preserve the values of other FCR bits.
2. The ALTINST bit enables execution of a new x86 jump instruction that starts execution of alternate instructions. This new jump instruction can be executed from any privilege level at any time that ALTINST is 1. The new jump instruction is a two-byte instruction: 0x0F3F. If ALTINST is 0, the execution of 0x0F3F causes an Invalid Instruction exception.
3. When executed, the new 0x0F3F x86 instruction causes a near branch to CS:EAX. That is, the branch function is the same as the existing x86 instruction
   - jmp [eax]
- In addition to the branch, the 0x0F3F instruction sets the processor into an internal mode where the target bytes are not interpreted as x86 instructions but rather as alternate instruction set instructions.
4. The alternate instructions fetched following the 0x0F3F branch should be of the form
   - 0x8D8400XXXXXXXX where 0xXXXXXXXX is the 32-bit alternate instruction
- That is, the alternate instructions are presented as the 32-bit displacement of a
   - LEA [EAX+EAX+disp]
- instruction. This example assumes that the current code segment size is 32-bits, if it is 16-bits, then an address size prefix (0x67) must be placed in front of the LEA opcode.
5. Upon fetching, the LEA “wrapper” is stripped off and the 32-bit alternate instruction contained in the displacement field is executed.
6. The alternate instruction set contains a special branch instruction that returns control to x86 fetch and execute mode. The x86 state upon return is not necessarily what it was when alternate instruction execution is entered since the alternate instructions can completely modify the x86 state.

While all VIA C3 processor processors contain this alternate instruction feature, the invocation details (e.g., the 0x8D8400 “prefix”) may be different between processors. Check the appropriate processor datasheet for details.

1108H: FCR2 (FEATURE CONTROL REGISTER 2)

This MSR contains more feature control bits — many of which are undefined. It is important that all reserved bits are preserved by using a read-modify-write sequence to update the MSR.





AVS: 0 = The CPUID instruction vendor ID is "CentaurHauls"

1 = The CPUID instruction returns the alternate Vendor ID. The first 8 characters of the alternate Vendor ID are stored in FCR3 and the last 4 characters in FCR2[63:32]. These 12 characters are undefined after RESET and may be loaded by system software using WRMSR.

Family ID: This field will be returned as the family ID field by subsequent uses of the CPUID instruction

Model ID: This field will be returned as the model ID field by subsequent uses of the CPUID instruction

1109H: FCR (FEATURE CONTROL REGISTER 3)

This MSR contains the first 8 characters of the alternate Vendor ID. The alternate Vendor ID is returned by the CPUID instruction when FCR2[AVS] is set to '1'. FCR3 is a write-only MSR.