Application Note 130
Cyrix III CPU Layout Guidelines for 133 MHz Bus Operation

Cyrix Processors

REVISION HISTORY

Date	Version	Revision
3/31/99	0.3	Page 4 Added paragraph under Introduction.
3/29/99	0.2	Removed notes 3 and 4 from Table 3. Restored subscripts on page 7. Minor typos corrected on page 27.
2/18/99	0.1	Initial Version C:\documentation\joshua\appnotes\cIII_layout.fm

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APPLICATION NOTE 130

Cyrix III Layout Guideline for 133 MHz Operation

1 Introduction

The Cyrix III processor is a next generation Cyrix processor. Cyrix III employs a Socket 370 package, P6 bus protocol and operates with front side bus speeds of 66 MHz, 100 MHz, and 133 MHz. The Cyrix III processor system bus uses GTL+ signaling interface. The objective of this layout guideline is to provide the system designer with the information needed to achieve stable operation with 133 MHz front side bus. A Cyrix III IBIS model is available if the system designer would like to verify his design, but signal integrity analysis is not a requirement if the design falls within the specifications of this guideline.

This document is to serve as a reference design to help new board designers meet the 133 MHz specification. The Guidelines in this document are for reference only, and are not a requirement for Cyrix motherboard certification.

2. *Printed Circuit Board Stack-Up*

Either a four-layer or six-layer stack-up can be used. In either case, it is important to control the characteristic impedance to be 60 ohms within +/-10% for a 6 mil-wide trace. This characteristic impedance improves signal integrity in many respects. Firstly, it improves signal integrity because it is close to the value of the termination, 56 ohms. Secondly, it reduces overshoots and under-shoots. Table 1 and Figure 1 describes a four-layer stack-up which would meets the characteristic impedance requirement:

STACK-UP PARAMETER	VALUE
Height of Outer Dielectric	4.5 mil
Dielectric constant	4.5
Microstrip Base Cu Thickness	0.5 oz.
Microstrip Plating Cu Thickness	0.5 oz.
Power Plane Cu Thickness	1 oz.
Zo Typical	60 ohms

Table 1. Recommended Four Layer Stack-Up Parameters

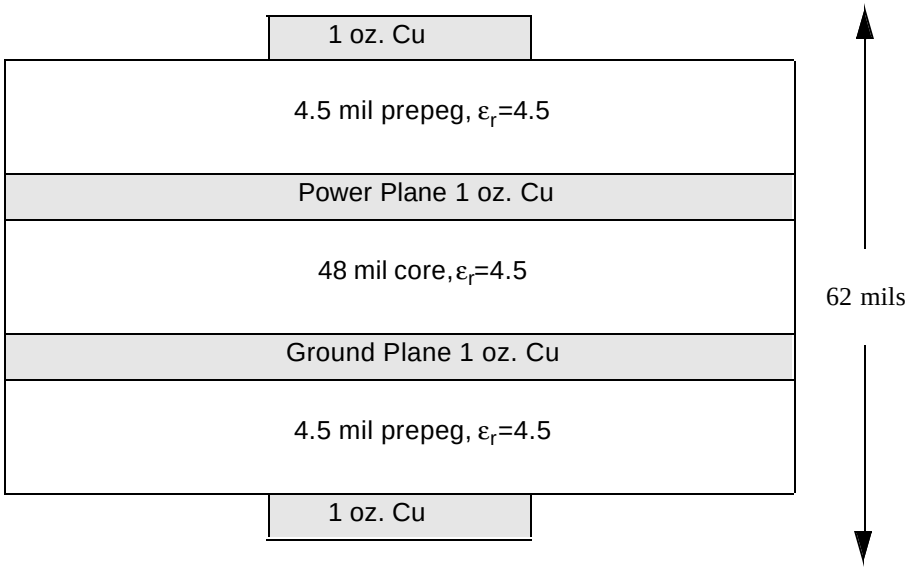

Figure 1. Recommended Four Layer Stack-Up

Table 2 and Figure 2 describe the recommended six layer stack-up which meets the characteristic impedance requirements.

STACK-UP PARAMETER	VALUE
Height of Outer Dielectric	4.5 mil
Dielectric constant for Microstrip Core	4.5
Dielectric constant for Stripline Traces	4.3
Microstrip Base Cu Thickness	0.5 oz
Microstrip Plating Cu Thickness	0.5 oz
Stripline Base Cu Thickness	0.5 oz.
Power Plane Cu Thickness	1 oz.
Zo Typical	60 ohms

Table 2. Recommended Four Layer Stack-Up Parameters

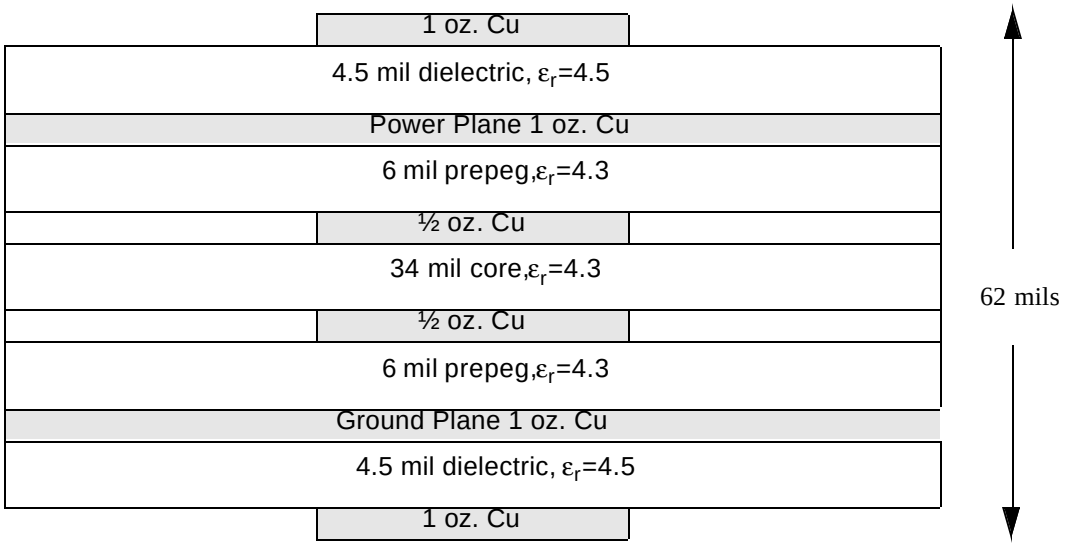

Figure 2. Recommended Six Layer Stack-Up.

The previous two stack-ups are recommendations only. The system designer may chose other possible stack-ups. If so, he should only aim for maintaining a characteristic impedance between 60 ohms +/-10%.

3. GTL+ Bus Timing Analysis

Before discussing timing analysis, it is important to clarify all the terminology. Some of these terms have been made specific to Cyrix III by including the voltage levels and temperatures. Be aware that documentation from other companies may define these terms differently with respect to the voltage levels and temperatures.

1. Clock Period (T_{PERIOD}) – the ideal clock period at which the bus clock is running.

2. Clock Jitter (T_{JIT}) – the maximum amount of variation from the clock period from one cycle to the consecutive cycle coming from the clock chip.

3. Clock Misrepresentation (T_{MIS}) – the time difference between when the clock reaches Vih on a rising edge and when it reaches Vil on a rising edge. This time accounts for time differences in the time that devices get clocked due to a slower edge rate. This effect can be seen in long clock lines and is very much dependent on the pcb layout. For analysis, the worst-case trace length and stack-up are assumed.

4. Maximum Clock to Output Time (T_{CO-MAX}) – the maximum time difference between when the bus clock crosses Vref and the output crosses Vref with the Test Load connected. This is measured at 0ºC for Cyrix III.

5. Minimum Clock to Output Time (T_{CO-MIN}) – the minimum time difference between when the bus clock crosses Vref and the output crosses Vref with the Test Load connected. This is measured at 110ºC for Cyrix III.

6. Maximum Flight Time ($T_{FLT-MAX}$) – the maximum of {Maximum Flight Time on rising edge, Maximum Flight Time on falling edge}

7. Maximum Flight Time, rise – this is the maximum time difference between when a rising edge crosses V_{ref} on the Test Load and when it crosses V_{ref} + dV_{ref} at the receiver. This generally occurs on the longest trace.

8. Maximum Flight Time, fall - this is the maximum time difference between when a falling edge crosses V_{ref} on the Test Load and when it crosses V_{ref} - dV_{ref} at the receiver. This generally occurs on the longest trace.

9. Minimum Flight Time ($T_{FLT-MIN}$) – the minimum of {Minimum Flight Time on rising edge, Minimum Flight Time on falling edge}

10. Minimum Flight Time, rise – this is the minimum time difference between when a rising edge crosses V_{ref} on the Test Load and when it crosses V_{ref} - dV_{ref} at the receiver. This generally occurs on the shortest trace.

11. Minimum Flight Time, fall - this is the minimum time difference between when a falling edge crosses V_{ref} on the Test Load and when it crosses V_{ref} + dV_{ref} at the receiver. This generally occurs on the shortest trace.

12. Minimum Hold Time (T_{HOLD}) – the time for which the input data must remain valid after the input clock.

13. Minimum Setup Time (T_{SU}) - time for which the input data must be valid prior to the input clock.

14. Maximum Clock Generator Skew – the maximum time difference between the switching of two different outputs from the same clock generator. This time is not included in the equations and analysis, because there is a method of significantly reducing this skew which will be described in the next section.

15. Maximum PCB Clock Skew ($T_{MAX\text{-}PCB\text{-}SKEW}$) – the maximum propagation delay of the bus clock to the processor minus the propagation delay of the bus clock to the chipset.

16. Minimum PCB Clock Skew ($T_{MIN\text{-}PCB\text{-}SKEW}$) – the minimum propagation delay of the bus clock to the processor minus the propagation delay of the bus clock to the chipset.

17. Reference Voltage (V_{ref}) – This is the GTL+ reference voltage and is equivalent to 1 volt. An electrical high is a voltage level above this voltage and an electrical low is a voltage level below this voltage.

18. Reference Voltage Noise Margin (dV_{ref}) – noise margin for the reference voltage (V_{ref}). This noise margin accounts for noise both on the reference voltage (V_{ref}) and the termination voltage V_{TT}.

19. Simultaneous Switching Pull-In Time ($T_{PULL\text{-}IN}$) – the amount of time that the switching time is decreased on account of neighboring traces switching in the same direction. As this is greatly dependent on the board topology, the worst-case stack-up and spacing are used to determine this number.

20. Simultaneous Switching Pull-Out Time ($T_{PULL\text{-}OUT}$) – the amount of time that the switching time is increased on account of neighboring traces switching in the opposite direction. As this is greatly dependent on the board topology, the worst-case trace length, stack-up, and spacing are used to determine this number.

21. Test Load – This is a 56 ohm resistor pulled up to 1.5 volts.

In doing timing analysis, a systems engineer has basically two timing constraints to meet for each receiver: setup time and hold time. The system architecture for this design guide has two receivers – the processor and the chipset. Thus, there are basically four different timing

equations to verify. The four conditional equations which must hold true are listed below. In addition to satisfying the conditional equations, you should also maintain a timing margin of at least 1 nsec for setup time and at least 0.5ns for hold time in your design. The equations for the timing margins are also shown below. Mathematically, a timing margin is a measure of how well the corresponding conditional equation is met. When the timing margin is greater, your design will be more reliable. It is not advisable to proceed with a design that has timing margins less than 0.5 nsec.

Equations 1 through 4 describe the timing constraints for the receiver at the processor. Equations 2 and 4 describe the timing margin for the setup and hold time for the processor. Note that a subscript 'PROC' indicates that this value is derived from a timing analysis of the processor whereas a subscript 'CH' indicates that this value is derived from a timing analysis of the chipset.

Equation 1. Set-up Time Equation for the Receiver at the Processor.

$$(T_{CO\text{-}MAX})_{CH} + (T_{FLT\text{-}MAX})_{CH} + (T_{SU})_{PROC} + (T_{PULLOUT})_{CH} <= T_{PERIOD} - T_{JIT} - T_{MIS} + T_{MIN\text{-}PCB\text{-}SKEW}$$

Equation 2. Timing Margin for Set-Up Time at the Processor.

$$(T_{M\text{-}SU})_{PROC} = T_{PERIOD} - T_{JIT} - T_{MIS} - (T_{CO\text{-}MAX})_{CH} - (T_{FLT\text{-}MAX})_{CH} - (T_{SU})_{PROC} + T_{MIN\text{-}PCB\text{-}SKEW} - (T_{PULLOUT})_{CH}$$

Equation 3. Hold Time Equation for the Receiver at the Processor.

$$(T_{CO\text{-}MIN})_{CH} + (T_{FLT\text{-}MIN})_{CH} - T_{MAX\text{-}PCB\text{-}SKEW} - (T_{PULL\text{-}IN})_{CH} >= (T_{HOLD})_{PROC} + T_{MIS}$$

Equation 4. Timing Margin for Hold Time at the Processor.

$$(T_{M\text{-}HOLD})_{PROC} = (T_{CO\text{-}MIN})_{CH} + (T_{FLT\text{-}MIN})_{CH} - T_{MAX\text{-}PCB\text{-}SKEW} - (T_{PULL\text{-}IN})_{CH} - (T_{HOLD})_{PROC} - T_{MIS}$$

Equations 5 through 8 describe the timing constraints for the receiver at the chipset. Equations 6 and 8 describe the timing margin for the setup and hold time for the chipset.

Equation 5. Set-up Time Equation for the Receiver at the Chipset.

$$(T_{CO\text{-}MAX})_{PROC} + (T_{FLT\text{-}MAX})_{PROC} + (T_{SU})_{CH} + (T_{PULLOUT})_{PROC} <= T_{PERIOD} - T_{JIT} - T_{MIS} - T_{MAX\text{-}PCB\text{-}SKEW}$$

Equation 6. Timing Margin for Set-Up Time at the Chipset.

$$(T_{M\text{-}SU})_{CH} = T_{PERIOD} - T_{JIT} - T_{MIS} - (T_{CO\text{-}MAX})_{PROC} - (T_{FLT\text{-}MAX})_{PROC} - (T_{SU})_{CH} - T_{MAX\text{-}PCB\text{-}SKEW} - (T_{PULLOUT})_{PROC}$$

Equation 7. Hold Time Equation for the Receiver at the Chipset.

$(T_{CO\text{-}MIN})_{PROC} + (T_{FLT\text{-}MIN})_{PROC} + T_{MIN\text{-}PCB\text{-}SKEW} - (T_{PULL\text{-}IN})_{PROC} >= (T_{HOLD})_{CH} + T_{MIS}$

Equation 8. Timing Margin for Hold Time at the Chipset.

$(T_{M\text{-}HOLD})_{CH} =$
$(T_{CO\text{-}MIN})_{PROC} + (T_{FLT\text{-}MIN})_{PROC} + T_{MIN\text{-}PCB\text{-}SKEW} - (T_{PULL\text{-}IN})_{PROC} - (T_{HOLD})_{CH} - T_{MIS}$

Now that the pertinent terminology has been defined and the equations listed, we can list the timing data for the processor, the timing data for the 440BX, and the recommended timing data for a 133MHz North Bridge. Table 3 is a compendium of this information.

SYMBOL	PHRASE	CLOCK (NSEC)	CYRIX III (NSEC)	INTEL 440BX (NSEC)	REQUIRED NORTH BRIDGE CHARACTER-ISTICS (NSEC)	PCB LAYOUT (NSEC)
T_{PERIOD}	Clock Period	7.50				
T_{JIT}	Clock Jitter	0.25[1]				
T_{MIS}	Clock Misregistration	0.34[2]				
$T_{CO\text{-}MAX}$	Maximum Clock to Output Time		1.50	4.45	4.30	
$T_{CO\text{-}MIN}$	Minimum Clock to Output Time		0.95	0.80	2.00	
T_{HOLD}	Minimum Hold Time		0.50[3]	-0.10	0.20	
T_{SU}	Minimum Setup Time		1.00[4]	3.00	2.90	
$T_{MIN\text{-}PCB\text{-}SKEW}$	Minimum PCB Clock Skew					0.40
$T_{MAX\text{-}PCB\text{-}SKEW}$	Maximum PCB Clock Skew					0.50
$T_{FLT\text{-}MAX}$	Maximum Flight Time		0.77[5]	0.77[5]	0.77[5]	
$T_{FLT\text{-}MIN}$	Minimum Flight Time		0.22[6]	0.22[6]	0.22[6]	

Table 3. AC Characteristics of Cyrix III, Intel™ 440BX, recommended, and layout.

SYMBOL	PHRASE	CLOCK (NSEC)	CYRIX III (NSEC)	INTEL 440BX (NSEC)	REQUIRED NORTH BRIDGE CHARACTER-ISTICS (NSEC)	PCB LAYOUT (NSEC)
$T_{PULL-IN}$	Simultaneous Switching Pull-In Time					0.05
$T_{PULL-OUT}$	Simultaneous Switching Pull-Out Time					0.15

Table 3. AC Characteristics of Cyrix III, Intel™ 440BX, recommended, and layout.

Notes:

[1] This number is based on the maximum jitter as specified in the datasheets of many clock chips, but in reality it is unlikely that you will see this much jitter.

[2] Based on IBIS simulations with ICS clock chip ICS9250-10 with a series termination of 10 ohms, a trace length of 7 inches, and a characteristic impedance of 67 ohms. Measurement taken from the crossing of 0.7V to 1.7V on rising edge.

[3] This number takes into account PLL skew within the part.

[4] From datasheet.

[5] This is the propagation delay of a 5 in. microstrip trace with 54 ohm. The actual flight time could be slightly longer.

[6] This is the propagation delay of a 2 in. microstrip trace with 67 ohm. The actual flight time could be slightly shorter.

Now we can use Table 3 and Equations 2, 4, 6 and 8 to find the timing margins in your design. The timing margins for Cyrix III and a chipset with the recommended AC characteristics are as follows:

$(T_{M\text{-}SU})_{PROC}$ =
$T_{PERIOD} - T_{JIT} - T_{MIS} - (T_{CO\text{-}MAX})_{CH} - (T_{FLT\text{-}MAX})_{CH} - (T_{SU})_{PROC} + T_{MIN\text{-}PCB\text{-}SKEW} - (T_{PULLOUT})_{CH}$

= 7.50 – 0.25 – 0.34 – 4.30 – 0.77 – 1.00 + 0.40 – 0.15
= 1.09 nsec

$(T_{M\text{-}HOLD})_{PROC} = (T_{CO\text{-}MIN})_{CH} + (T_{FLT\text{-}MIN})_{CH} - T_{MAX\text{-}PCB\text{-}SKEW} - (T_{PULL\text{-}IN})_{CH} - (T_{HOLD})_{PROC} - T_{MIS}$

= 2.00 + 0.22 – 0.5 – 0.05 – 0.5 – 0.34
= 0.83 nsec

$(T_{M\text{-}SU})_{CH} = T_{PERIOD} - T_{JIT} - T_{MIS} - (T_{CO\text{-}MAX})_{PROC} - (T_{FLT\text{-}MAX})_{PROC} - (T_{SU})_{CH} - T_{MAX\text{-}PCB\text{-}SKEW} - (T_{PULLOUT})_{CH}$

= 7.50 – 0.25 – 0.34 – 1.50 – 0.77 – 2.90 – 0.5 – 0.15
= 1.09 nsec

$(T_{M\text{-}HOLD})_{CH} = (T_{CO\text{-}MIN})_{PROC} + (T_{FLT\text{-}MIN})_{PROC} + T_{MIN\text{-}PCB\text{-}SKEW} - (T_{PULL\text{-}IN})_{PROC} - (T_{HOLD})_{CH} - T_{MIS}$

= 0.95 + 0.22 + 0.40 – 0.05 – 0.2 – 0.34
= 0.98 nsec

4. Clock Layout Recommendations

Before proceeding with the layout of a clock, the system designer has many things to be concerned about. The following is a list of items to consider before laying out a clock trace:

1. Choice of termination for the clock chip. Series termination is very effective method for reducing reflections and EMI simultaneously. A large value (> 47 ohms) for the termination is very effective at dampening out reflections; however, it can also cause a significant increase in the rise time which adds some error into the time when a device is clocked. A small value (<22 ohms) improves the rise time, although it is not very good at dampening out reflections if the trace is long (> 3 inches). With the ICS9248-73 clock chip, a good choice for the series termination is 33 ohms. This is approximately equal to the difference between the transmission line characteristic impedance and the output impedance of the clock chips buffers; hence, reflections will be greatly reduced and the rise time will not be significantly increased. The series termination should be less than 250 mils from the output pin.

2. Meeting signal integrity requirements. Two important signal integrity requirements are reducing crosstalk to an acceptable level and minimizing ringing at the receiver pins. In order to reduce ringing, the clock trace to the processor should be less than 6.5 inches. In addition, there should be a minimum spacing of 24 mils between the clock and all other traces to reduce the crosstalk to an acceptable level. If this spacing rule is not adhered to, your board may exhibit stability problems which are very difficult to resolve. GTL+ signals are particular sensitive to crosstalk. As an illustration, Figure 3 shows a picture of the crosstalk injected on a 6 inch trace which has a spacing of 24 mils from the CPU clock buffer of an ICS9250-10. A series termination of 33 ohms is used on both the CPU clock trace and the victim trace. The transmission line characteristic impedance in this simulation is 67 ohms.

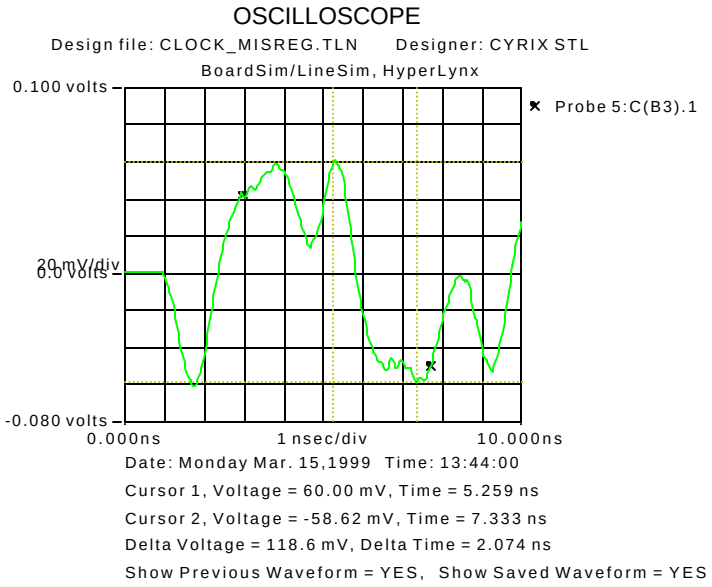

Figure 3. Crosstalk Injected On a Victim Net Due to Nearby 133 MHz Clock.

3. Meeting timing requirements. As shown in the previous timing analysis section, skewing the clock can balance out the four timing margins – the processor's setup time, the processor's hold time, the chipset's setup time, and the chipset's hold time. In the previous section, the amount of clock skew that was used to balance the timing margins was an additional clock delay of between 400 psec and 500 psec on the clock trace to the processor. If your board design is a four layer board, then the clock trace to the processor should be longer than the clock length to the chipset by a length between 2.64 and 3.26 inches.

In addition to skewing the clock, reducing the amount of unpredictable skew between the clock trace to the chipset and the clock trace to the processor can improve the timing margins and add more reliability to your design. Unpredictable skew between the clocks can be reduced by connecting the two outputs together. Figure 4 shows the recommended topology for the clock and Table 4 lists the length requirements assuming microstrip traces.

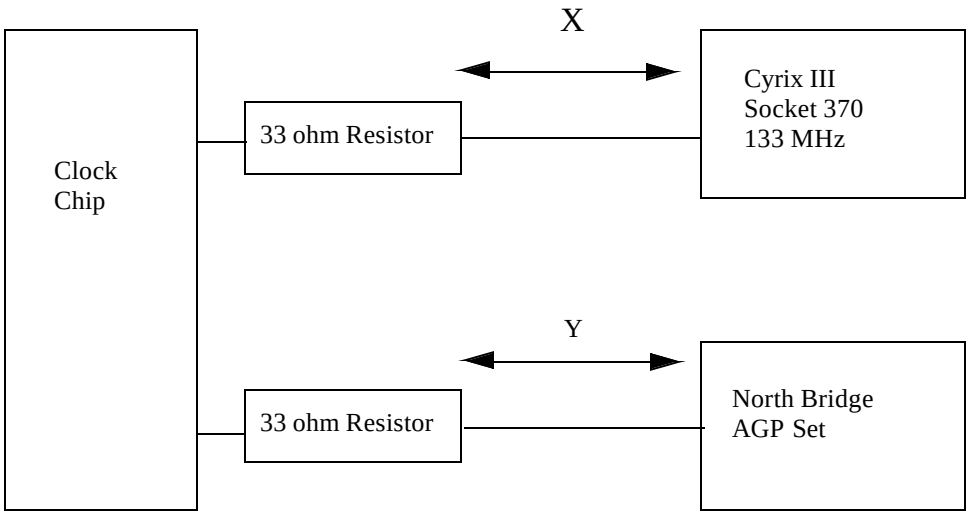

Figure 4. Diagram of Clock Layout Topology.

PARAMETERS FOR CLOCK LAYOUT FOR FOUR LAYER BOARD			
DESCRIPTION	RECOMMENDED	MINIMUM	MAXIMUM
X – Trace length from clock chip to processor	As short as possible but longer than 2.84”	2.84”	6.5”
Y – Trace length from clock chip to chipset	X-2.95”	X-3.26”	X-2.64”
Termination	33 ohms		
Spacing between clock trace and other traces	24 mils		

Table 4. Parameters for Clock Layout for a Four Layer Board

It is recommended that the trace the chipset be routed first. Use as few vias as possible (three or less) and make the trace as short as possible. Then, route the trace to the processor. If the trace to the processor is longer than the trace to the chipset by more than 3.26 inches, you may need to move the clock chip or lengthen the trace to the chipset by adding extra loops. Be sure to route with 45º angles and each segment of trace should be at least 15 mils in length.

Finding the best clock chip placement and the routing of the clocks may take several iterations. It is important to think about the clock routing starting from the initial placement and to verify that the routing meets this guideline before releasing the board. Negligence in this area may make the board unreliable at 133 MHz.

5. GTL+ Layout Recommendations

Before discussing signal integrity, it is helpful to have a description of the GTL+ bus. The GTL+ output buffers are primarily open-drain, although there is a small p-channel drive to improve the rise time. Pull-up resistors exist on all GTL+ lines and serve two purposes. They pull the line high when the buffer is released. They also act as termination to dampen out reflections. Each GTL+ line is pulled up to a termination voltage V_{TT} equal to 1.5 volts with a 56 ohm resistor.

On the receiver end, the signal is compared to V_{REF}, which is two-thirds of V_{TT}, to determine whether the signal is high or low. A logic high is an electrically low signal and a logic low is an electrically high signal. There are eight pins for V_{REF} on the processor. A simple resistor divider network using 1% resistors can be used to create V_{REF}. Resistor values of 75 and 150 ohms are suggested. This provides a stiff voltage divider network. A 0.1uF capacitor should be used to provide adequate decoupling to two V_{REF} pins and should be placed as close to both pins as possible. V_{REF} should be routed with a 10 mil wide trace. Table 5 gives the acceptable range for the V_{REF} voltage.

VOLTAGE	MINIMUM	TYPICAL	MAXIMUM
V_{REF}	0.98V	1.00V	1.02V

Table 5. Specifications for Reference Voltage, VREF

Definitions 1 through 4 relate to signal integrity without consideration for mutual inductance and capacitance between traces. Definitions 6 through 9 are for crosstalk and related terminology.

1. Overshoot – The maximum peak voltage on a low to high transition.

2. Undershoot – The minimum peak voltage on a high to low transition.

3. Rising-Edge Ringback – The minimum value of the voltage after it has reached its initial peak value on the rising edge.

4. Falling-Edge Ringback – The maximum value of the voltage after it has reached its initial peak value on the falling edge.

5. Crosstalk – Injection of noise on a victim net resulting from the inductive and capacitive coupling between the victim net and an aggressor net when it is switching.

6. Aggressor net – In crosstalk analysis, the net which is switching and inducing noise on a victim net is called the aggressor net.

7. Victim net – In crosstalk analysis, this is the net which is receiving the noise. To simplify analysis, this net is usually held at a steady voltage level, V_{OL} or V_{OH}.

8. Odd Crosstalk – This occurs when the aggressor is switching to a voltage level different than the victim net.

9. Even Crosstalk – This occurs when parallel nets are switching in the same direction.

10. Trace-to-trace spacing – This is the distance between the edge of one trace to the edge of another. Note that “spacing” is NOT a measure from the center of one trace to the center of another.

Table 6 lists the GTL+ layout requirements which were derived in the Timing Analysis section as timing requirements. The timing requirements translate into different length requirements, depending on whether the trace is microstrip or stripline.

PARAMETER	MIN	MAX
Propagation Delay	0.22 nsec	0.77 nsec
Length (Microstrip)	1.5 in	5 in
Length (Stripline)	1.3 in	4.4 in

Table 6. Trace Length Constraints Derived from Timing Requirements.

Although the length requirements have been derived by the timing requirements, there are still open issues to be addressed. They are described as follows:

1. Proper Trace-to-Trace Spacing
It is important to maintain proper spacing to ensure that crosstalk does not become an issue. Crosstalk increases when the spacing is reduced and when a trace is long. Crosstalk occurs on all systems to some extent. Crosstalk which results in a signal's logic being non-deterministic or which violates the electrical specifications of a device is termed "harmful crosstalk". Extensive modeling and simulation of both the output buffers and realistic board topologies have been done. The result of these crosstalk simulations is that there is a possibility that harmful crosstalk will occur when an electrically low trace is surrounded on either side by neighboring aggressor nets which are spaced 6 mils away, five inches in length, and switching high. In order to provide a good noise margin, it is recommended that a spacing of 10 mils be used with all GTL+ lines if they are longer than two inches. There are times when it is impossible to route lines with that much space between them due to small package sizes. In that case, smaller spacing can be used for short distances to breakout from a package and then the larger spacing can be used for the rest of the routing. Thus, the requirement can be broken down into possible guidelines from which the system designer can choose. Table 7 breaks down the spacing requirement into four options.

GUIDELINE	SPACING RECOMMENDATION
#1: 10 mil spacing only	Route all GTL+ traces with 10 mil spacing. All GTL+ traces 5 inches or less. Traces should be no longer than 5 inches total.
#2: 4 mil and 10 mil spacing	Route all GTL+ traces with 4 mil spacing for no more than 0.25 inches and 10 mil spacing for no more that 4.75 inches. Traces should be no longer than 5 inches total.
#3: 6 mil and 10 mil spacing	Route all GTL+ traces with 6 mil spacing for no more than 0.75 inches and 10 mil spacing for no more that 4.25 inches. Traces should be no longer than 5 inches total.
#4: 6 mil spacing	Route all GTL+ traces with 6 mil spacing for no more than 2 inches. Traces should be no longer than 2 inches total.

Table 7. Guidelines for Spacing Neighboring GTL+ Signals.

Note that the GTL+ lines do not need to be separated into groups of control, data, and address as is the case for some bus architectures. All output buffers from a device switch synchronously, so their purpose is irrelevant as far as signal integrity is concerned.
As CMOS lines create even more crosstalk on GTL+ lines, there should be 25 mil separation between CMOS lines and GTL+ lines.

2. Optimization of Termination Topology.
There are two types of topologies that can be used with GTL+ lines. Each topology is the ideal topology depending whether the trace will only be driven from one end or could be driven from both ends. For this reason, the GTL+ signals have been split into two groups: GTL+ input only and GTL+ I/O.

A. Daisy Chain Topology
This topology should be used for all GTL+ signals which are input-only with respect to the processor. Route each GTL+ trace from chipset to processor and then from the processor to the pull-up termination. This particular topology results in a clean signal if the receiver is at the processor. If the signal received is at the chipset, it will exhibit much more ringing. At a frequency of 133MHz, the signal integrity for this topology is poor when signals are driven from the processor and received at the chipset. For this reason, this topology is a sensible choice only for signals which are input-only at the processor. Table 8 describes all the GTL+ signals which are input-only. Figure 5 describes the topology that should be used with these signals and Table 9 describes the restrictions on this topology assuming that the traces are microstrip.

TABLE OF CYRIX III GTL+ INPUT SIGNALS			
SIGNAL NAME	PIN NUMBER	ACTIVE LEVEL	CLOCK
BPRI#	AN17	Low	BCLK
DEFER#	AN19	Low	BCLK
RESET#	X4	Low	BCLK
RS[0]#	AH26	Low	BCLK
RS[1]#	AH22	Low	BCLK
RS[2]#	AK28	Low	BCLK
TRDY#	AN25	Low	BCLK

Table 8. Cyrix III GTL+ Input-Only signals.

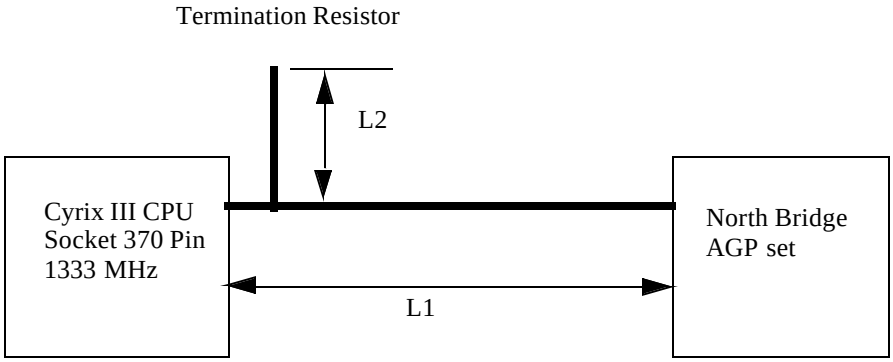

Figure 5. Recommended Topology for GTL+ Input-Only Signals.

Topology Length Requirements for Figure 5		
	Min Length	Max Length
L1	1.5”	5.0”
L2	0”	1.0”

Table 9. Table of the Length Requirements for Figure 5 for Microstrip Traces.

B. Middle Termination Topology

This topology should be used for all GTL+ signals except the input-only signals listed in Table 8. Route each GTL+ I/O trace from the chipset to the processor. Connect the trace to a 56 ohm resistor pulled up to V_{TT} (1.5 volts) with a via somewhere midway between the processor and the chipset. For simplicity, we will assume that this topology is routed with microstrip traces. This topology improves signal quality for both the processor and the chipset. Make sure that the via is no more than 3 inches from the pins of either device. The stub from the via to the pull-up resistor can be as much as 3 inches long. Figure 6 depicts this topology and Table 10 lists the length requirements for this topology assuming microstrip traces.

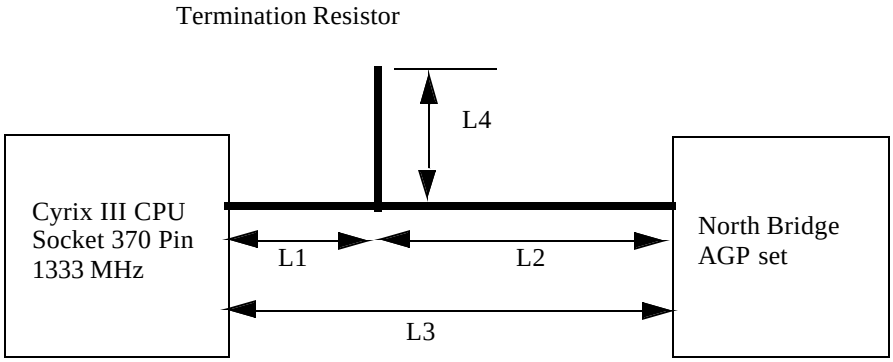

Figure 6. Diagram of Recommended Topology for all GTL+ I/O Signals.

Topology Length Requirements for Figure 6		
	Min Length	Max Length
L1	0”	3.0”
L2	0”	3.0”
L3	1.5”	5”
L4	0”	3”

Table 10. **Table of the Length Requirements for Figure 6 for Microstrip Traces**

Other layout recommendations for routing the GTL+ lines:

- The best place to put the via is exactly midway between both the processor and the chipset for middle-terminated lines, although this is not a requirement.
- Each net should have no more than three vias on it.

- GTL+ lines should be separated from CMOS lines by a distance of 25 mils.
- Contrary to popular belief, it is not necessary to minimize the length L4. For example, if L4 is three inches instead of 50 mils, the termination will be just as effective. On the other hand, a good reason for keeping L4 short would be to reduce EMI.
- Trace lengths L1 and L2 should be made as short as possible.

3. Supplying V_{TT} Current for GTL+.
In addition to supplying current for the GTL+ lines, the termination voltage V_{TT} must also maintain a stable voltage. The specification for this voltage is shown in Table 11.

VOLTAGE	MINIMUM	TYPICAL	MAXIMUM
V_{TT}	1.365V	1.50V	1.635V

Table 11. Range for Termination Voltage V_{TT}.

There are two methods of making sure that the termination voltage V_{TT} can supply the GTL+ lines with adequate current and maintain a voltage of 1.5 volts. Firstly, you can improve the stability of the termination voltage V_{TT} to by increasing the trace width of V_{TT}. Secondly, high frequency decoupling capacitors can be used to both supply the necessary switching current and help maintain a steady V_{TT} voltage.

Before designing the power distribution of V_{TT}, it might be beneficial to review how the current fluctuates for each GTL+ buffer. Starting from an electrically high state, there is practically no current flowing. There are no buffers driving the line and the termination resistor is holding the line at a constant voltage of 1.5V. When a buffer pulls the line low, there is an instantaneous amount of current which flows from V_{TT} through the terminating resistor, through the trace, and into the buffer. Knowing how much current will be switching and how fast it will switch is important for choosing the right size capacitor and number of capacitors. After the traces switches low, there is a steady-state DC current which will flow from V_{TT} through the termination resistor. If you know the worst-case DC steady-state current, you can determine the appropriate width of the V_{TT} trace. When the buffer drives the line high, the current stops flowing from V_{TT} and the buffer actually drives a small amount of current into V_{TT}. Although this is not the purpose of the p-channel drive, this current recharges the decoupling capacitors to some extent when the buffer first switches high. Table 12 lists the typical and maximum currents through one terminating resistor during the different phases of the switching.

TABLE OF CURRENTS SUPPLIED FROM V_{TT} FOR ONE GTL+ BUFFER		
TYPES OF CURRENT THROUGH TERMINATING RESISTOR $I(R_{TT})$	TYPICAL VALUE (MA)	MAXIMUM VALUE (MA)
DC Steady-State on Low Signal	20	23
Maximum AC Current on High-to-Low Switching	23	28
Maximum change in current in 1ns Interval	7	12
Maximum Current driven into V_{TT} on Low-to-High Switching	4.5	5.7

Table 12. Currents through a GTL+ Termination Resistor

Before calculating the correct width of the V_{TT} trace, Table 13 defines some terms.

SYMBOL	UNITS	DESCRIPTION	VALUE
I_{DC}	A	Maximum DC steady-state current flowing through terminating resistor when line is held low	0.023
L	in.	Total length of V_{TT} trace (small stubs should not be included)	variable
R	ohms/in.	DC steady-state resistance of trace per inch	variable
V_D	V	Maximum voltage drop on V_{TT}	variable
N_{SW}	none	Maximum number of GTL+ lines that could be low simultaneously	~100

Table 13. Definitions of Terms used in Equation 9.

Equation 9 calculates the approximate worst-case voltage drop of V_{TT} due to the steady-state DC currents.

Equation 9. Worst-Case Voltage Drop on V_{TT} due to Steady-State Currents.

$$V_D = ½*L*I_{DC}*N_{SW}*R$$

The termination voltage should not drop by more than 135mV according to the specification. However, there will be a small voltage drop in V_{TT} due to instantaneous switching, so it is recommended that only 2% of 1.5 volts or 30mV should be budgeted toward the voltage drop in V_{TT} due to steady-state currents. In addition any voltage drop on V_{TT} will result in a voltage drop on V_{REF}. Significant drops in V_{REF} add more error into the timing analysis, so proper layout is important for both V_{REF} and V_{TT}. Table 14 describes possible solutions using different trace widths. The lengths in this table refer to the length of the main trunk. This is meant as a guideline only. It is left to the system designer to tailor the layout requirements in accordance with his particular board design.

SOLUTION	TRACE WIDTH OF TRUNK (MILS)	RESISTANCE/IN (OHMS/IN.)	LENGTH (IN.)	WORST-CASE VOLTAGE DROP (V)
1	40	0.013	2.00	30mV
2	50	0.010	2.61	30mV
3	60	0.008	3.26	30mV
4	70	0.007	3.73	30mV

Table 14. Possible Routing Solutions for V_{TT}

In addition to making V_{TT} a wide trace, it is also necessary to provide high frequency decoupling capacitors. It is recommended that one 0.1uF capacitor be placed for every two resistor packs. It is important that each capacitor be placed in the proximity of connection between the termination voltage and the resistor pack; otherwise, the capacitors become ineffective for high-frequency decoupling. If these guidelines are not followed for the placement of capacitors, then you will get slower rising edges on your GTL+ lines. The end result is that your design may become unreliable at 133MHz as the timing margins are decreased.

4. Verification of Signal Integrity Requirements.

In particular, the overshoot, undershoot, ringback, and settling time must all be within the GTL+ specification. Detailed modeling of the buffer, the package, and the board have been done to verify that would be no signal integrity issues if this guideline was followed. Table 15 lists the worst-case signal integrity measurements for the entire range of stack-ups and topologies listed in this guideline using a fast process model at 0ºC. In addition, it lists the GTL+ specifications from the Intel's *100 MHz GTL+ Layout Guidelines for the Pentium II Processor and Intel 440BX AGPset*.

SIGNAL INTEGRITY PARAMETER	WORST-CASE SIMULATION VALUE (VOLTS)	MAXIMUM SPECIFIED (VOLTS)	NOISE MARGIN (VOLTS)
Overshoot	2.21	2.50	0.29
Undershoot	-0.28	-0.70	0.42
Rising-Edge Ringback	1.46	1.12	0.34
Falling-Edge Ringback	0.56	0.88	0.32

Table 15. Signal Integrity Parameters for 133 MHz Operation

It is clear from the results in Table 15 that there is a good noise margin with regards to the signal integrity requirements for even the fastest possible process and a low temperature if the layout recommendations in this guideline are followed. Still, it is recommended that you gather actual lab measurements of both the bus clock and the GTL+ signals on your board to ensure adequate signal integrity.

6. Differences between Cyrix III and Intel™ Celeron™ Design Guides

There are a number of important, although small differences between Celeron and Cyrix III. A few are discussed below:

♦ Connection of 1.5V. Celeron running at 66MHz does not need 1.5V connected; however, Cyrix III does. Please make sure that pin AD36 is connected to 1.5 volts. It will still be compatible with Celeron if 1.5 volts is connected.

♦ Clock ratio. Celeron hard-wires the clock ratio; however, Cyrix III will be able to have the clock ratio changed in BIOS. Until this feature is implemented, the Pentium II method of determining the clock ratio is suggested.

♦ VID[4]. Cyrix III has five voltage identification pins, where as Celeron has four. The extra VID pin (AK36) on Cyrix III is a ground pin on Celeron. Thus, VID[4] on the voltage regulator module can be connected to this pin. In this fashion, the board will be compatible with both Celeron and Cyrix III.

♦ BSEL1. This pin is not present on Celeron. This is an active high signal which selects 133MHz. In order to achieve 133MHz, BSEL0 must also be high.

Please refer to Cyrix *Application Note 127 Cyrix III Board Design Considerations and AC/DC Specifications* for additional details on Cyrix III.

Printed in the United States of America

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Richardson, Texas 75080-2010

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