Application Note 127
Cyrix III CPU MotherBoard Design Considerations

Cyrix Processors

REVISION HISTORY

Date	Version	Revision
5/20/99	1.0	Added Diagrams
4/5/99	0.54	Page 5, Table 1, Pin AK30 Description. Changed description. Page 5, Table 1, Moved third column and changed heading. Other minor editing on pages 7, 8, 9,and 13 .
4/2/99	0.53	Typo Page 5, AK30 pin BSEL1 changed to 1 = 133 MHz, 0 =100 MHz
3/22/99	0.52	Changed MXs processor name to Cyrix III.
3/15/99	0.51	Corrected typos.
3/12/99	0.5	Added paragraphs to pages 4, 7, 8 and 9 Renamed document to include the word “Considerations”
3/11/99	0.4	Renamed document to better reflect the content.
2/26/99	0.3	Repaired Table 1-4. BSEL0 and BSEL1 columns were reversed.
2/26/99	0.2	Changed BSEL66# to BSEL0, Changed BSEL133# to BSEL1. BSEL1 now requires pull-down 10K resistor instead of 200 ohm pull-up resistor. Pins now listed in Table 1-2. Bus speed signals redefined in Table 1-4.
2/25/99	0.1	Initial Version C:\documentation\joshua\appnotes\cIII_board.fm

Application Note 127

Cyrix III Board Design Considerations and AC/DC Specifications

1. Introduction

The Cyrix III is the next generation processor from Cyrix. This application note describes board design considerations unique to the Cyrix III processor. In this document, pin differences are described and design considerations are discussed. Also the AC/DC Specifications are presented to a aid in proper timing design.

The Cyrix III CPU is designed to be compatible with the Intel Celeron CPU. It is a socket 370 compatible processor and thus is intended to work with the common Socket 370 motherboards. There are however some differences between the Cyrix III as the Intel Celeron that impact mother-board design.

There are four major differences between the Cyrix III and Celeron CPUs that are important to motherboard designers:

1) Core voltages: the Cyrix III operates at 2.2 volts and the Celeron operates at 2.0 volts. It thus requires the VID4 pin to be tied to cpu and VR.

2) Bus speed: the Cyrix III can run with a bus at high as 133 MHz bus whereas the Celeron can run with a bus as high as 100 MHz.

3) Clock multiplier: the Cyrix III built in default clock multiplier can be changed (either by jumpers or by BIOS), whereas the Celeron has a inflexible built-in clock multiplier.

4) BIOS update: BIOS needs to be programmed to identify Cyrix III cpu and set up all cpu registers. Performance Rating must be added to CPU name.

Operating the Cyrix III processor at 100 MHz and 133 MHz bus speeds requires careful board design. Signal timing analysis and signal integrity analysis must be done to ensure reliable operation. Factors such as clock skew, board and connector parasitics, and signal overshoot and ringback must be considered. Refer to *100MHz GTL+ Layout Guidelines* (Intel document 243330-001) and Cyrix Application Notes 101 and 113 for implementation suggestions.

2. PPGA 370 Package Pinout Differences

The Cyrix III processor has some advanced features which are not supported by the Intel® Celeron™ processor. Refer to the *Cyrix III Databook chapter 5* for information on pin numbering and package footprint. Table 1 lists the pins that are defined differently for the Cyrix III and Celeron processors.

Table 1. Cyrix III and Intel Celeron Pin Differences

PINS	CYRIX III SIGNAL	CELERON SIGNAL	TYPE	DESCRIPTION
AK36	VID[4]	GND	O	Voltage ID bit 4. Used by Cyrix III when signaling 2.2 V operation (VID[4-0] = 11101). Connecting AK36 to the voltage regulator will be compatible with both Cyrix III and Celeron since VID4 will be grounded by Celeron.
AK30	BSEL1	Reserved	I	Used with BSEL0 to select system bus frequency. This is legacy Cyrix III pin. New Celeron has defined a different pin for its BSEL1 signal, which Cyrix III also supports. Motherboard may use either pin for Cyrix III.
AJ31	BSEL1	BSEL1	I	AK30 and AJ31 are tied together internally to Cyrix III to be compatible with both legacy Cyrix III and new Celeron boards.
AB2	EXTRATIOPIN#	Vdd	I	When low, Cyrix III samples clock multiplier pins from jumpers, when high external jumpers are ignored and default clock multiplier is selected.
The following signals are not supported by Cyrix III, but may be connected the same as Celeron.				
C35, E35	Reserved	BPM[1-0]#	I/O	Output driven by Celeron to indicate the status of breakpoints and programmable counters used for monitoring processor performance.
AE35	Reserved	IERR#	O	Asserted by Celeron as a result of an internal error.
A35	Reserved	PRDY#	O	Probe ready. This output signal is used to determines Celeron debug readiness and is not supported.
J37	Reserved	PREQ#	I	Probe request. This input signal is used by Intel debug tools to request debug operation of the Celeron processor.
AH28	Reserved	THERMTRIP#	I	Thermal trip. Output from the Celeron processor to signal severe over-temperature operation. The Cyrix III CPU always drives this signal high.

3. Voltage ID Signaling

The Cyrix III processor uses a 5-pin VID bus to signal its core voltage requirement as shown below:

The Cyrix III CPU currently operates at 2.2 volts. The Intel Celeron currently operates at 2.0 volts. Due to the voltage regulator protocol, Cyrix III CPU requires an additional voltage identification signal—VID4.

Table 2. Core Voltage Requirement Bus Signaling

VID[4]	VID[3]	VID[2]	VID[1]	VID[0]	VDD_{CORE}
L	L	H	L	H	1.80 V
L	L	H	L	L	1.85 V
L	L	L	H	H	1.90 V
L	L	L	H	L	1.95 V
L	L	L	L	H	2.00 V
L	L	L	L	L	2.05 V
H	H	H	H	L	2.10 V
H	H	H	L	H	2.20 V

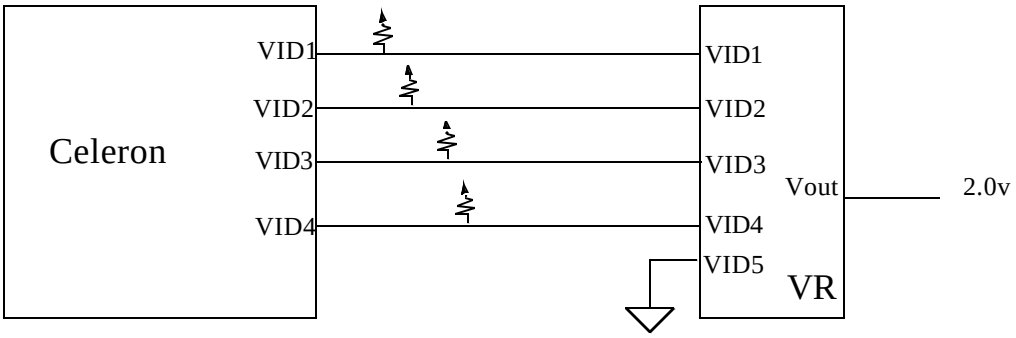
NOTES:
L = processor pin connected to GND.
H = open on processor. The board must provide pull-up resistors to 2.5 V on VID[4-0].
The VID encodings are the same as for Celeron for voltages at or below 2.05 V.
All other VID encodings are reserved.

The Cyrix III expands the VID bus by defining pin AK36 as VID4. Pin AK36 is defined as GND on the Celeron processor. By connecting the AK36 CPU pin to the VID4 voltage-regulator input pin makes the motherboard compatible with both Cyrix III and Intel Celeron processors.

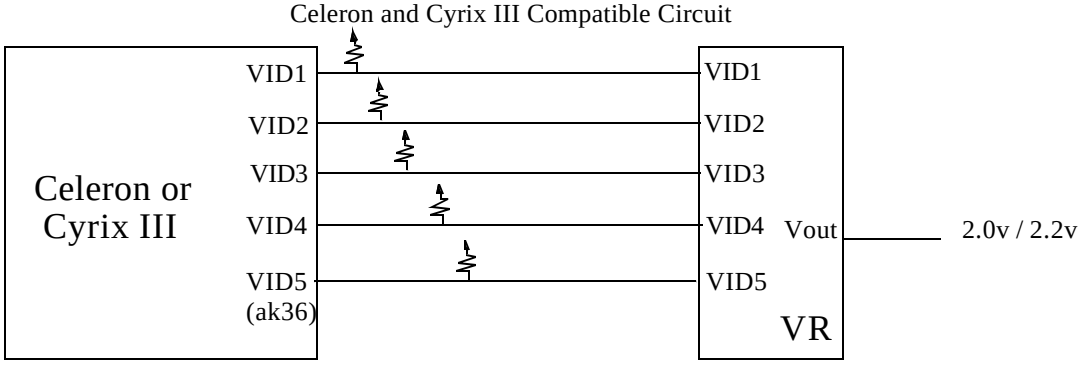
The following schematic diagrams explain how to make a standard socket 370 motherboard compatible with the Cyrix III cpu.

Figure 3.1: VID4 Signal Implementation

Celeron Only Circuit



Celeron and Cyrix III Compatible Circuit



*ak36 is VID4 for Cyrix III, and GND for Celeron

Note: VID pins are open-drain cmos meaning the motherboard must provide pullups to Vdd_cmos on all VID signals.

4. Bus Speed Signaling

The Cyrix III processor supports 66 MHz, 100 MHz and 133 MHz bus frequencies through the use of BSEL0 and BSEL1. The CPU must be informed of the bus frequency in order to properly generate its internal clocks and to tune its I/O performance. Bus speed signaling is defined in the following table:

Table 3. Speed Bus Signaling

BSEL1	BSEL0	BUS FREQUENCY
L	L	66 MHz
L	H	100 MHz
H	H	133 MHz
H	L	Reserved

The Celeron CPU drives the clock chip with the signal BSEL# instead of BSEL0 and BSEL1. The BSEL# output signal (pin AJ33) directs the clock chip to generate either a 66 or 100 MHz bus clock frequency. Almost all motherboards have a provision to override the BSEL# signal with a jumper selection.

The flexible Cyrix III CPU supplies two input signals, BSEL0 (pin AJ33) and BSEL1 (pin AK30), allowing the selection of up to four different bus speeds. Since these signals are inputs when using the Cyrix III, two motherboard jumpers may be used to select the correct bus speed. When no jumpers are employed, the Cyrix III will drive the clock chip to the Cyrix III default bus speed.

The Celeron BSEL# (pin AJ33) is defined on the Cyrix III CPU as BSEL0. The Celeron reserved pin (AK30) is defined on the Cyrix III as BSEL1.

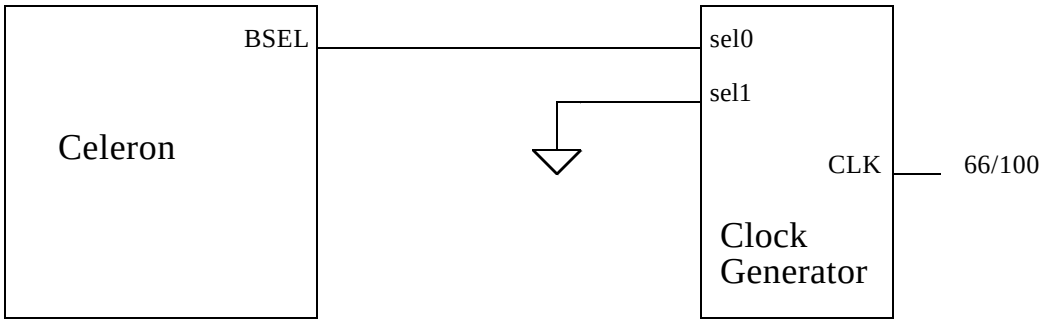
IMPORTANT: The new Celeron Specification defines its own BSEL1 pin which is pin AJ31. To be compatible, Cyrix III connects AJ31 to AK30 internally to the cpu. So the motherboard may use either pin as BSEL1. The only problem occurs when a legacy Celeron (no BSEL1 defined) is updated for Cyrix III (BSEL1=AK30). Since old celeron defines AJ31 as GND (BSEL1 in new celeron), if GND is connected to AJ31 and BSEL1 is connected to AK30, then BSEL1 will be grounded through the cpu. This will disable 133 Mhz. (66 and 100 Mhz will work fine). If this type of board wants to run 133 Mhz, then AJ31 should be disconnected, or else use I2C to program clock chip to 133 Mhz.

To make a motherboard compatible for both Celeron and the Cyrix III, connect the BSEL0 pins on the clock chip and CPU together. Do the same for the BSEL1 pins. Also connect each line to a jumper, so that the lines can be jumpered high or low.

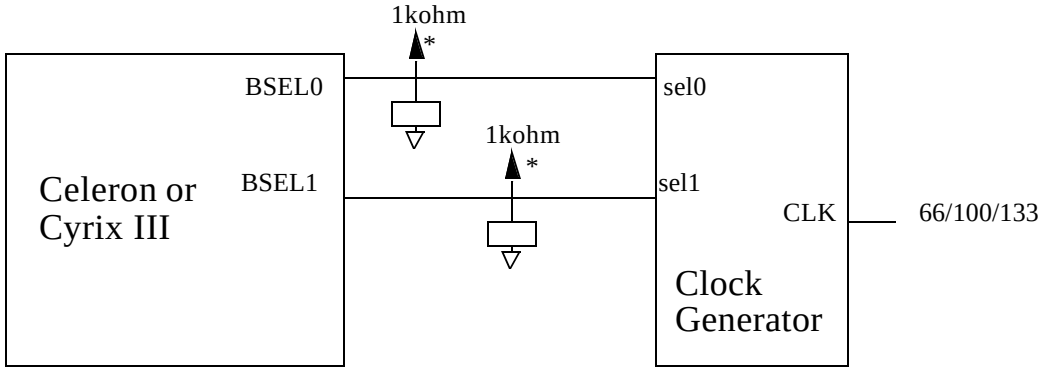
JUMPERLESS: If no jumpers are used on the BSEL lines, Cyrix III defaults to its proper bus speed, but then the BIOS may use I2C to program the clock chip to any Mhz, providing a jumperless solution.

Figure 4.1: BSEL Signal Implementation

Celeron Only Circuit



Celeron and Cyrix III Compatible Circuit



*1kohm pullup to Vcc_cmos, and jumpers to GND are required for user setting.

5. *CPU Core Clock Ratio Signaling*

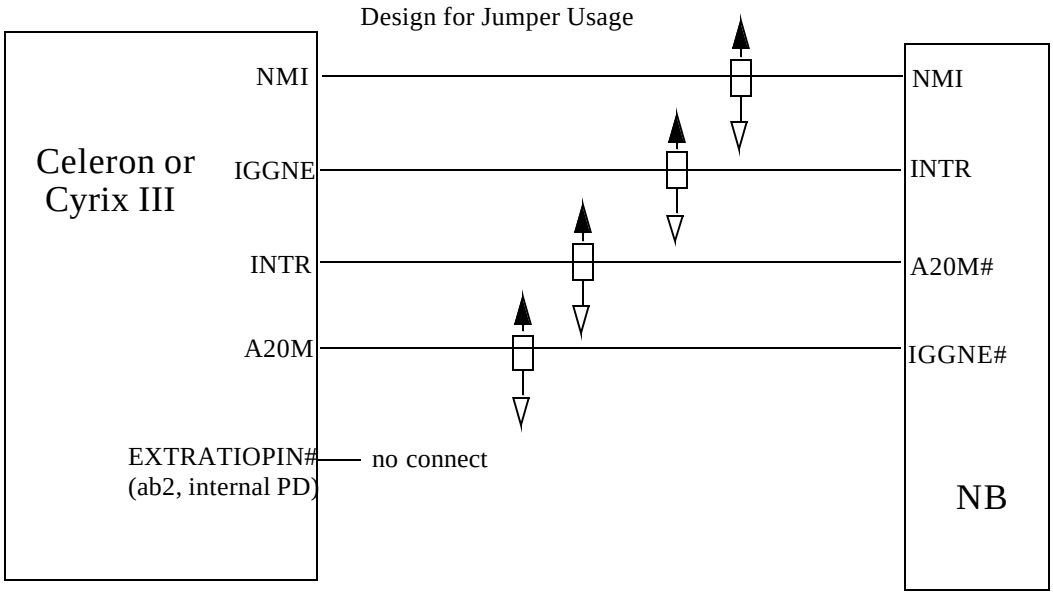
Like the Intel Celeron processor, the Cyrix III processor has a built in clock multiplier, but Cyrix III can also use the original Pentium II method for setting the core clock ratio to override the built in value. Cyrix III samples NMI, INTR, A20M# and IGNNE# while RESET# is asserted (low) and latches the values at the rising edge of RESET#. These signals must be stable for 1 ms prior to the rising edge of RESET# to ensure proper operation. This solution requires four jumpers to be placed on the motherboard so that these signals may be driven high or low. The use of these jumpers requires EXTRATIOPIN# to be unconnected (It defaults to low pull down inside cpu).

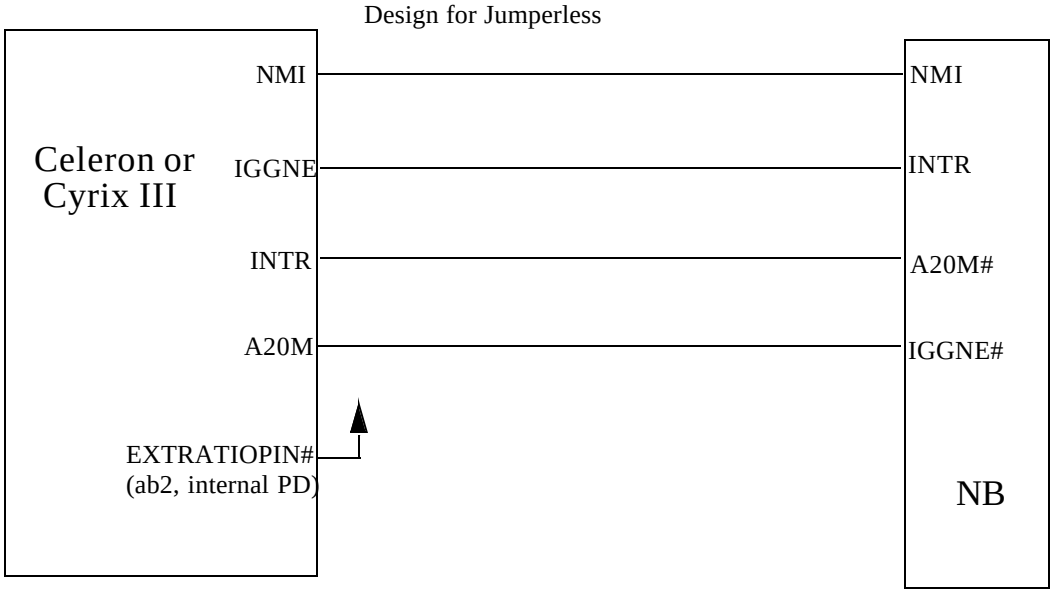
Table 4. Clock Ratio Signaling

RATIO	NMI	INTR]	A20M#	IGGNE#	CORE CLOCK		
					66 MHZ BUS	100 MHZ BUS	133 MHZ BUS
2:5	L	H	L	L			333 MHz
3:1	L	L	L	H		300 MHz	400 MHz
3.5:1	L	H	L	H		350 MHz	466 MHz
4:1	L	L	H	L		400 MHz	
4.5:1	L	H	H	L	300 MHz	450 MHz	
5:1	L	L	H	H	333 MHz	500 MHz	
5.5:1	L	H	H	H	366 MHz		
6:1	H	L	L	L	400 MHz		
6.5:1	H	H	L	L	433 MHz		
7:1	H	L	L	H	466 MHz		
7.5:1	H	H	L	H	500 MHz		

JUMPERLESS: the Cyrix III has a built in clock multiplier that will run the cpu at the proper frequency. Also the BIOS can override the built in value by setting the Clock Multiplier Configuration Register during bootup. This alternative eliminates the need for clock multiplier jumper pins on the motherboard. See the Cyrix III BIOS Writer's Guide, or Cyrix III Data Book for complete information.

If there are no jumpers on the board to set the clock multiplier, so that the board is relying on the built in multiplier or the BIOS to program the Cyrix III clock multiplier, the pin EXTRATIO# should be tied high (2.5v). This will make sure the Cyrix III does not latch in an invalid clock multiplier from the NMI-INTR-A20M#-IGGNE# pins. Instead the Cyrix III will boot up in default mode and the new clock multiplier can be programmed by BIOS. EXTRATIO# pin is a Vdd pin for Celeron so this pin will be high by default on most motherboards.


Design for Jumper Usage
Celeron or
Cyrix III
NMI
IGGNE
INTR
A20M
EXTRATIOPIN#
(ab2, internal PD)
no connect
NMI
INTR
A20M#
IGGNE#
NB


Design for Jumperless
Celeron or
Cyrix III
NMI
IGGNE
INTR
A20M
EXTRATIOPIN#
(ab2, internal PD)
NMI
INTR
A20M#
IGGNE#
NB

6. BUS SIGNAL GROUPS

The GTL+ signals are applied to open-drain receivers that differentially compare input signals to a reference voltage V_{REF} and determine if the input signals are logically high or low. Termination resistors are needed to pull the signal high. The high termination voltage, V_{TT}, is a typical value of 1.5 V. The reference voltage is typically 2/3 of V_{TT}.

The following table defines which signals are GTL+ and which are CMOS levels.

Table 5. Bus Signal Groups

SIGNAL TYPE	PARAMETER
GTL+ Input	BPRI#, DEFER#, RESET#, RS[2-0]#, TRDY#
GTL+ I/O	A[31-3]#, ADS#, BNR#, BUSSEL66#, BUSSEL133#, D[63-0]#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, REQ[4-0]#
CMOS Input	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK#
CMOS Output	FERR#, VID[4-0],

7. DC Characteristics

Below are the preliminary DC characteristics for the Cyrix III bus signals, and the GTL+ termination specifications that should be followed in order to design to this bus interface.

Table 6. GTL+ DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
V_{IL}	Input Low Voltage	-0.3	0.82	V	
V_{IH}	Input High Voltage	1.22	V_{TT}	V	See bus termination table
V_{OL}	Output Low Voltage		0.60	V	Measured into 25 ohm resistor to 1.5v
V_{OH}	Output High Voltage		V_{TT}	V	See bus termination table
I_{OL}	Output Low Current	36	48	mA	
I_L	Leakage Current		+/- 100	uA	
I_{LO}	Output Leakage Current		+/- 15	uA	

Table 7. GTL+ Termination Specifications

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNIT
V_{TT}	Bus Termination Voltage	1.365	1.5	1.635	V
B_{TT}	Bus Termination Resistance		56		Ohms
V_{REF}	Input Reference Voltage	2/3 V_{TT}–2%	2/3 V_{TT}	2/3 V_{TT}+2%	V

Table 8. CMOS DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
V_{IL}	Input Low Voltage	-0.3	0.7	V	
V_{IH}	Input High Voltage	1.7	2.625	V	
V_{OL}	Output Low Voltage		0.4	V	
V_{OH}	Output High Voltage		2.625	V	
I_{OL}	Output Low Current	14		mA	
I_L	Leakage Current		+/- 100	uA	
I_{LO}	Output Leakage Current		+/- 10	uA	

8. AC Characteristics

Below are the preliminary AC characteristics for the system bus clock, BCLK, and the Cyrix III GTL+ and CMOS signals at different bus clock speeds.

Table 9. 66 MHz System Bus AC Characteristics

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNIT	NOTES
BCLK	System Bus Frequency		66.67		MHz	
T1	BCLK Period		15.0		ns	
T2	BCLK Period Stability			+/- 300	ps	
T3	BCLK High Time	3.6			ns	
T4	BCLK Low Time	3.6			ns	
T5	BCLK Rise Time	0.34		1.40	ns	0.5 V to 2.0 V
T6	BCLK Fall Time	0.34		1.40	ns	2.0 V to 0.5 V

Table 10. 100 MHz System Bus AC Characteristics

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNIT	NOTES
BCLK	System Bus Frequency		100.00		MHz	
T1	BCLK Period		10.0		ns	
T2	BCLK Period Stability			+/- 250	ps	
T3	BCLK High Time	2.4			ns	
T4	BCLK Low Time	2.4			ns	
T5	BCLK Rise Time	0.34		1.40	ns	
T6	BCLK Fall Time	0.34		1.40	ns	

Table 11. 133 MHz System Bus AC Characteristics

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNIT	NOTES
BCLK	System Bus Frequency		133.00		MHz	
T1	BCLK Period		7.5		ns	
T2	BCLK Period Stability			+/- 200	ps	
T3	BCLK High Time	1.8			ns	
T4	BCLK Low Time	1.8			ns	
T5	BCLK Rise Time	0.34		1.40	ns	
T6	BCLK Fall Time	0.34		1.40	ns	

Table 12. GTL+ Bus AC Specifications

PARAMETER	66 MHz BUS		100 MHz BUS		133 MHz BUS		UNIT	NOTES
	MIN	MAX	MIN	MAX	MIN	MAX		
GTL+ Output Valid Delay	0.17	4.40	0.17	3.45	0.17	3.00	ns	1, 2
GTL+ Input Setup Time	1.60		1.60		1.40		ns	1
GTL+ Input Hold Time	0.90		0.90		0.90		ns	1
RESET# pulse width	1.00		1.00		1.00		ms	3

Notes:

1. All timings are referenced from the rising edge of BCLK at 1.25 V and are measured to the GTL+ signal when it crosses 1.00 V.
2. Valid delay timings are specified for a 25Ω resistance to V_{TT} and with V_{REF} at 1.0 V.
3. RESET# must remain asserted for the time specified after VDDCORE and BCLK are stable.

Table 13. CMOS Signal AC Characteristics

Parameter	66 MHz		100 MHz		133 MHz		Unit	Notes
	Min	Max	Min	Max	Min	Max		
2.5 V Output Valid Delay	0	8.0	0	8.0	0	7.0	ns	
2.5 V Input Setup Time	4.0		4.0		4.0		ns	See Note
2.5 V Input Hold Time	1.3		1.3		1.3		ns	See Note

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