Overcoming Barriers to Semiconductor Technology Scaling

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July 12, 2005

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Outline

- Background
- Challenges to Semiconductor Scaling
  - Transistor Leakage
  - V_t (Threshold Voltage) Variation
- New Approaches: Dynamic V_t Control
- Early results
- Conclusions

Background: About Transmeta

Transmeta develops efficient computing technologies that increase semiconductor performance and reduce power consumption

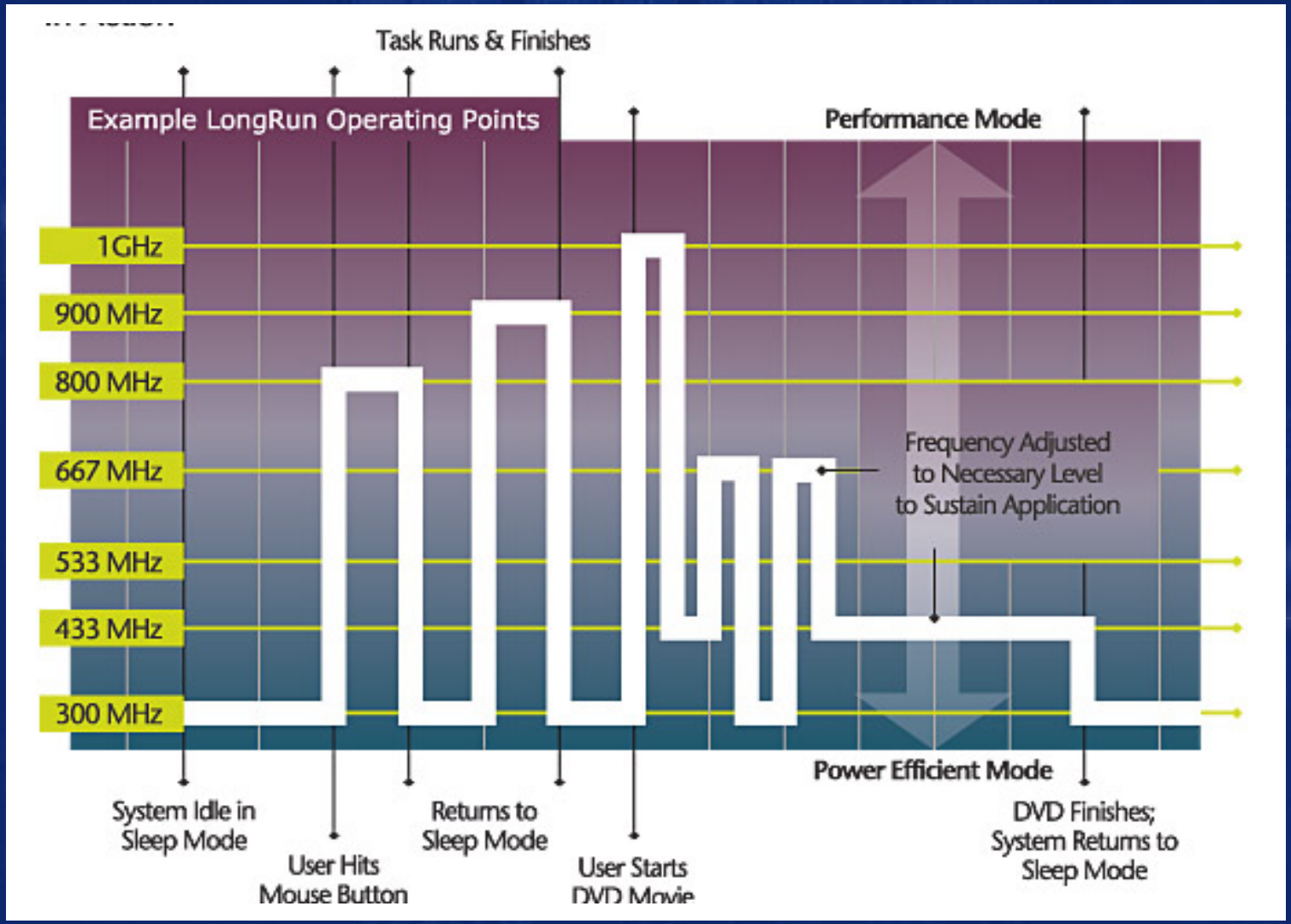
- **Transmeta Business Model**
  - Low Power x86 Processors
  - Customized Processor Development
  - Technology and IP Licensing
  - Synergistic Engineering Services
- **Serves Industry Leading Customers**
  - Sony, Fujitsu, NEC, Microsoft …
- **Headquartered in Santa Clara, CA**
  - Founded 1995
  - Publicly traded NASDAQ:TMTA
  - 200+ employees

Background:
Transmeta Power Management Technologies

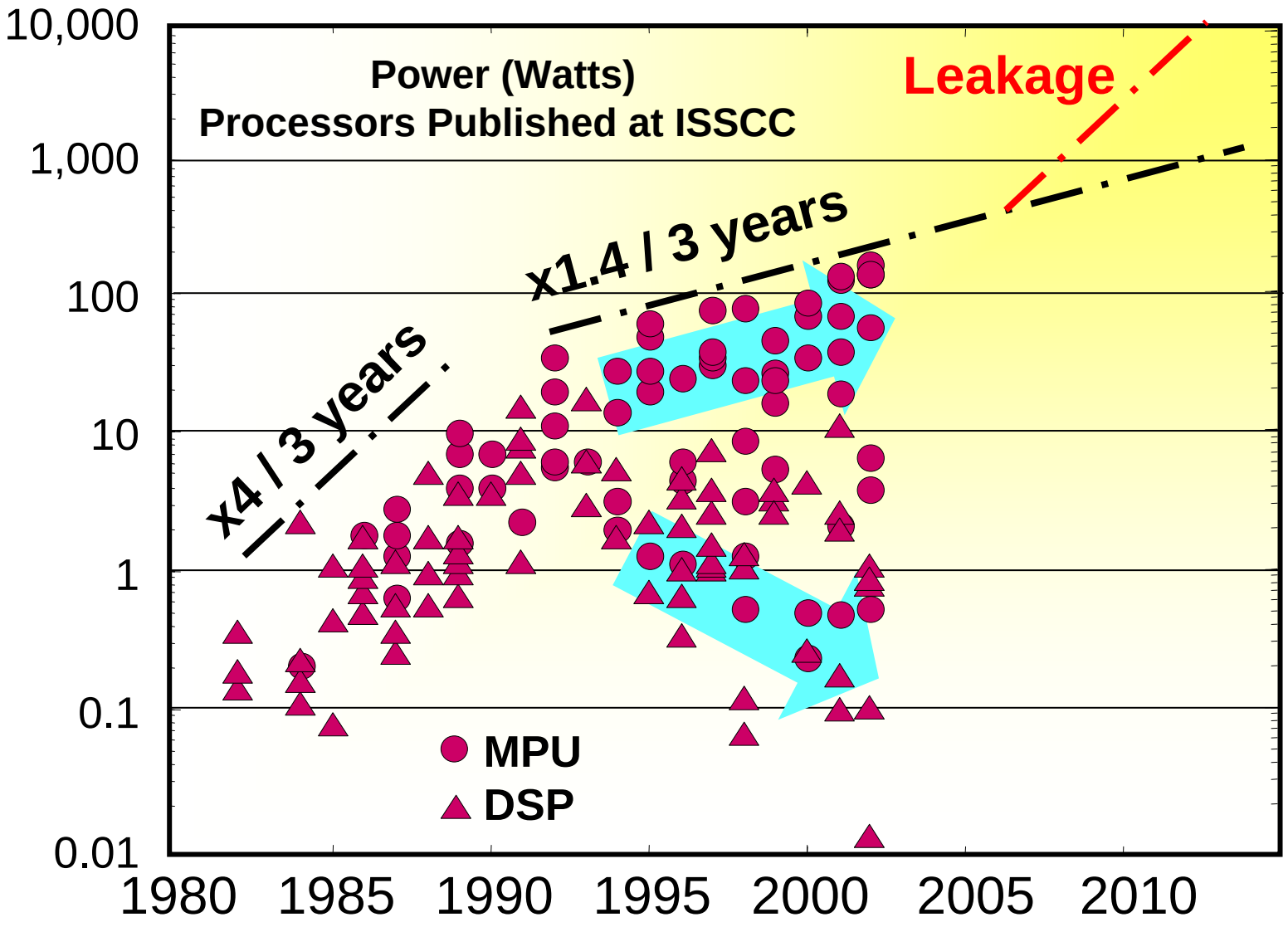
- Transmeta led the industry with a focus on energy efficient x86-compatible processing using innovations in:
  - **Processor Design** – VLIW processor + Code Morphing Software
  - **Power Management** – LongRun™ (version 1) Technology

- **LongRun Technology:**
  - Dynamically scales V_{dd} and frequency as demands change
  - Enables cubic reduction in power vs. linear gains if V_{dd} is constant
    - Power = Capacitance x Voltage^2 x Frequency
    - LongRun adjusts Voltage and frequency to reduce active power
  - This technique, now popular, was pioneered by Transmeta

Transmeta LongRun Technology: Dynamic MHz & V_{dd} Control



Power Consumption Trends & Leakage



Source: Professor T. Sakurai, University of Tokyo

Challenge to Technology Scaling: Widespread Concern Over Transistor Leakage

"Moore's law drives the industry for higher performance and lower cost, but…The leakage power explosion and Vt fluctuation will be big stumbling blocks for Moore's law."

Professor Takayasu Sakurai, Ph.D., University of Tokyo

"Scaling died at 130-nm"

Bernie Meyerson, CTO, IBM Systems & Technology
(Semico Conf.,1/19/04 & In-Stat/MDR Forum, 10/5/04)

"Leakage threatens CMOS scaling, panel warns"

Silicon Strategies Headline (EDA Industry Panel, 6/8/2004)

"Power cliff, performance wall"

EE Times Headline (2/5/2004)

"Semiconductor firms find leakage a problem at 90nm"

Electronics Weekly Headline (2/8/2004)

"Power is a growing concern at 90, 65-nm nodes"

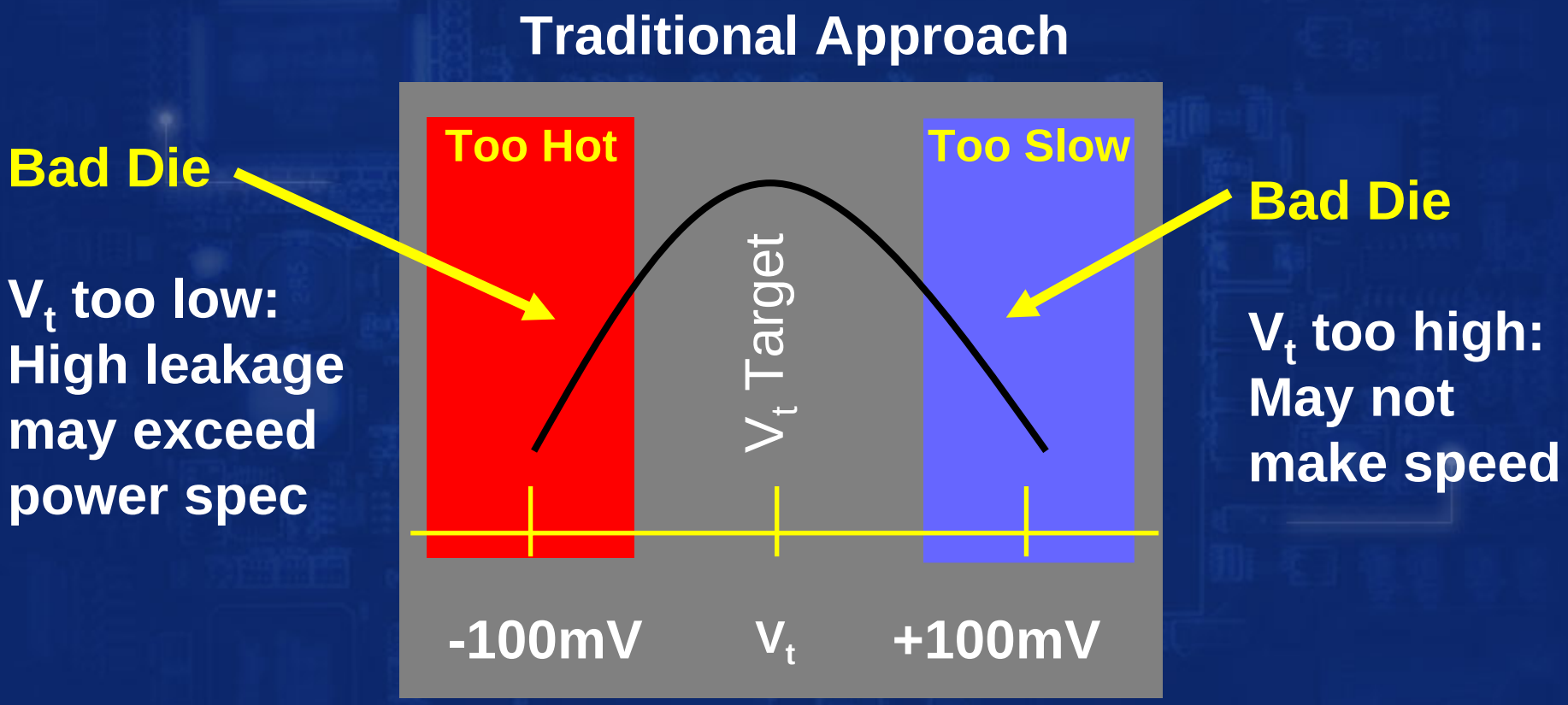
Silicon Strategies Headline (2/5/2004)

And many more headlines, papers, articles, panels and seminars...

Dealing with Transistor Leakage: Two Camps

- **Camp #1: Maintaining High V_{dd} (>1.0V)**
  - Raise threshold voltage (V_t) to decrease severity of leakage
  - Keep supply voltage roughly constant, > 1.0 V to maintain speed
  - **Result:**
    - **Leakage power is minimized, but active power remains high**
    - **Limited performance gains from new technology generations**
    - **Primary gain from new technology is die area reduction**
- **Camp #2: Following Technology Scaling towards 0.5 Volts**
  - Aggressively reduce V_{dd} and V_t each generation
  - V_t variation is a major concern
  - **Result:**
    - **Performance improvement and area gains from new technology**
    - **Need new solutions to address leakage power that comes with low V_t**

Challenge to Continued Scaling: V_t (Threshold Voltage) Variation

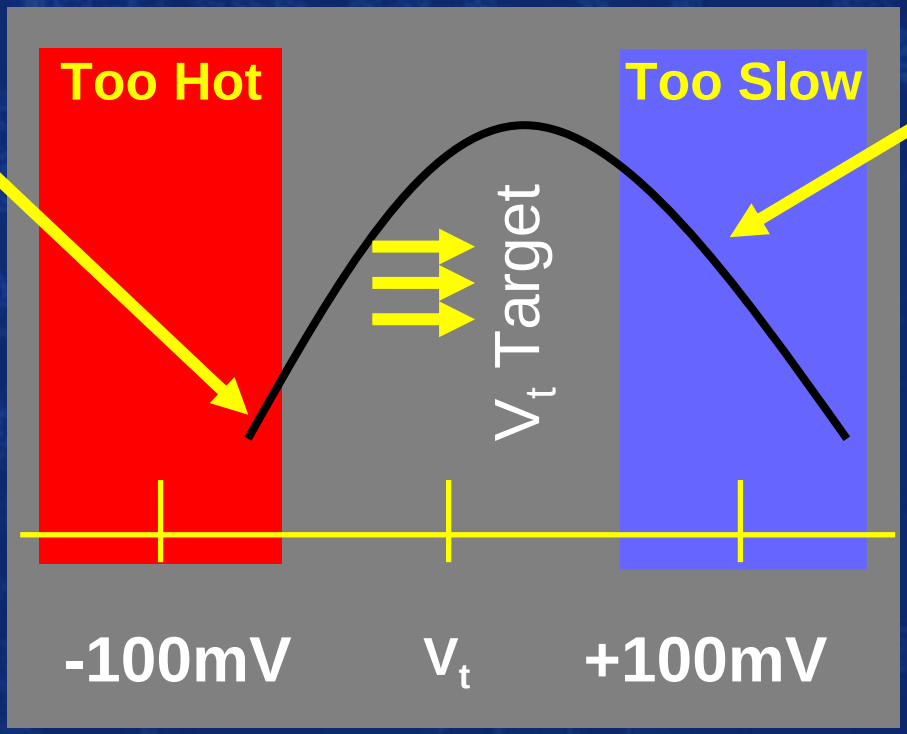


Challenge to Continued Scaling: V_t (Threshold Voltage) Variation

Some may shift their distribution to save power:

Fewer Bad Die

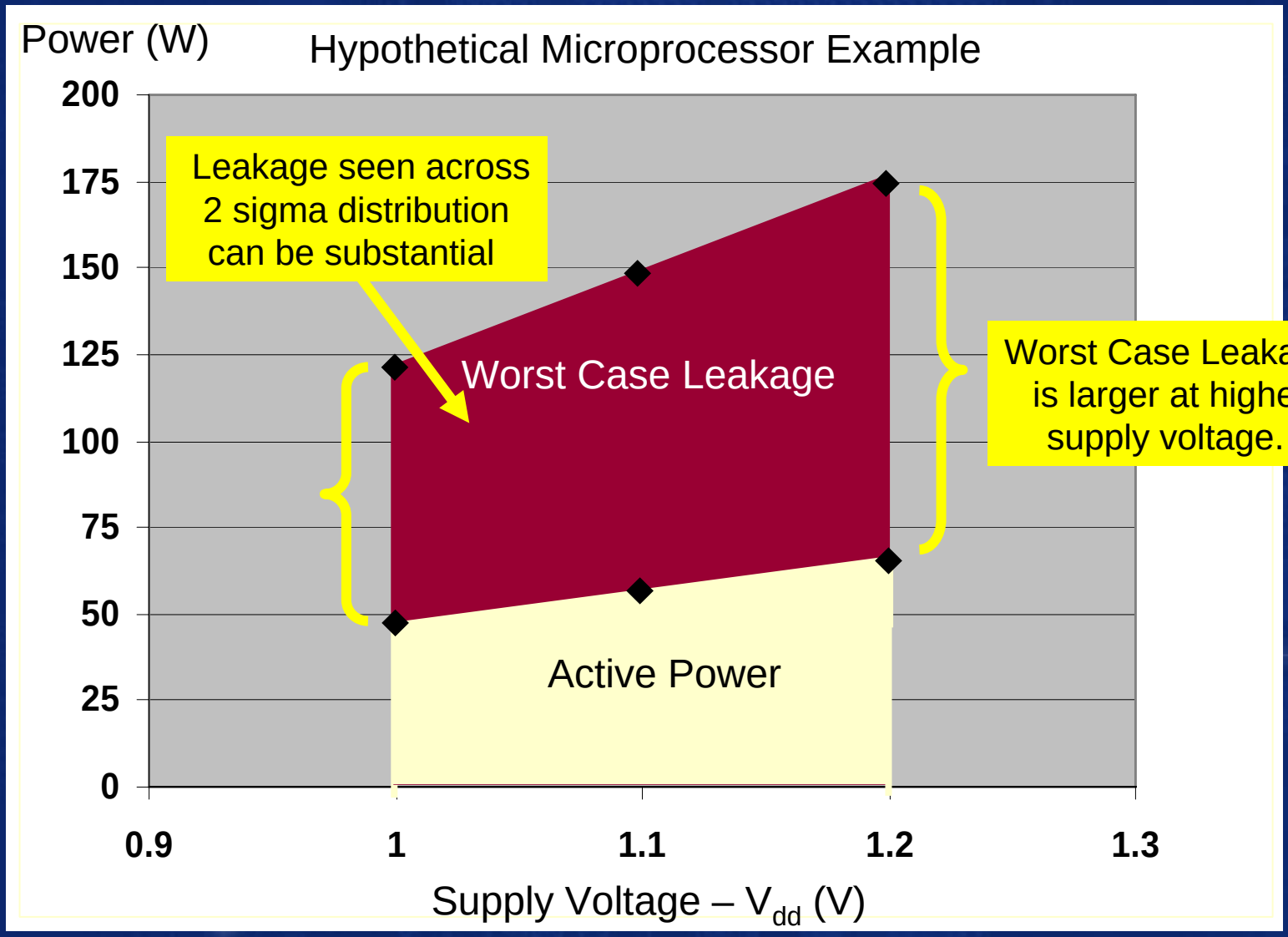
Minimize bad die caused by high leakage



Many Bad Die

Many die may fail to make speed

Leakage Power Is Sensitive to Distribution



Some Proposed Solutions to Leakage and V_t Variations

- Process solutions
  - Aligned transistor poly, multiple threshold voltages, OPC, …
- Materials solutions
  - High-k gate dielectric, SOI, …
- Thermal solutions
  - Reduce maximum allowed junction temperature/active control
- More robust circuit approaches, multiple V_{dd} , …

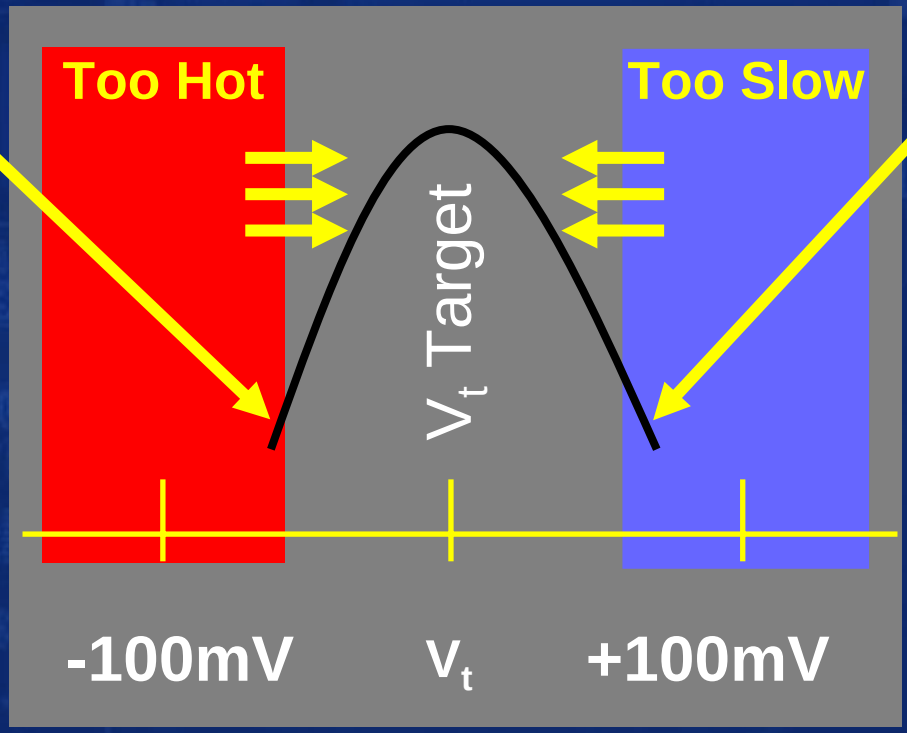
Many of these solutions can be costly

Even with these techniques, variation and leakage challenges still remain

Transmeta's Solution: Dynamic V_t Scaling with LongRun2™ Technologies

- Reduce variation and leakage with multi-prong strategy
- Incorporates a number of key technologies:
  - Implement Dynamic V_t control in a new way
  - Complementary to other power and leakage control
  - Can be retrofitted into existing "bulk silicon" designs
  - Technologies to help reduce minimum operating voltage (V_{min})
- Current LongRun2 Licensees: NEC, Fujitsu and Sony
- First prototype demonstrated on Efficeon™ Processor, in October 2003

Dynamic V_t Control with LongRun2: Adjust Distribution to Reach Goals



Few Bad Die

Minimize die exceeding power spec

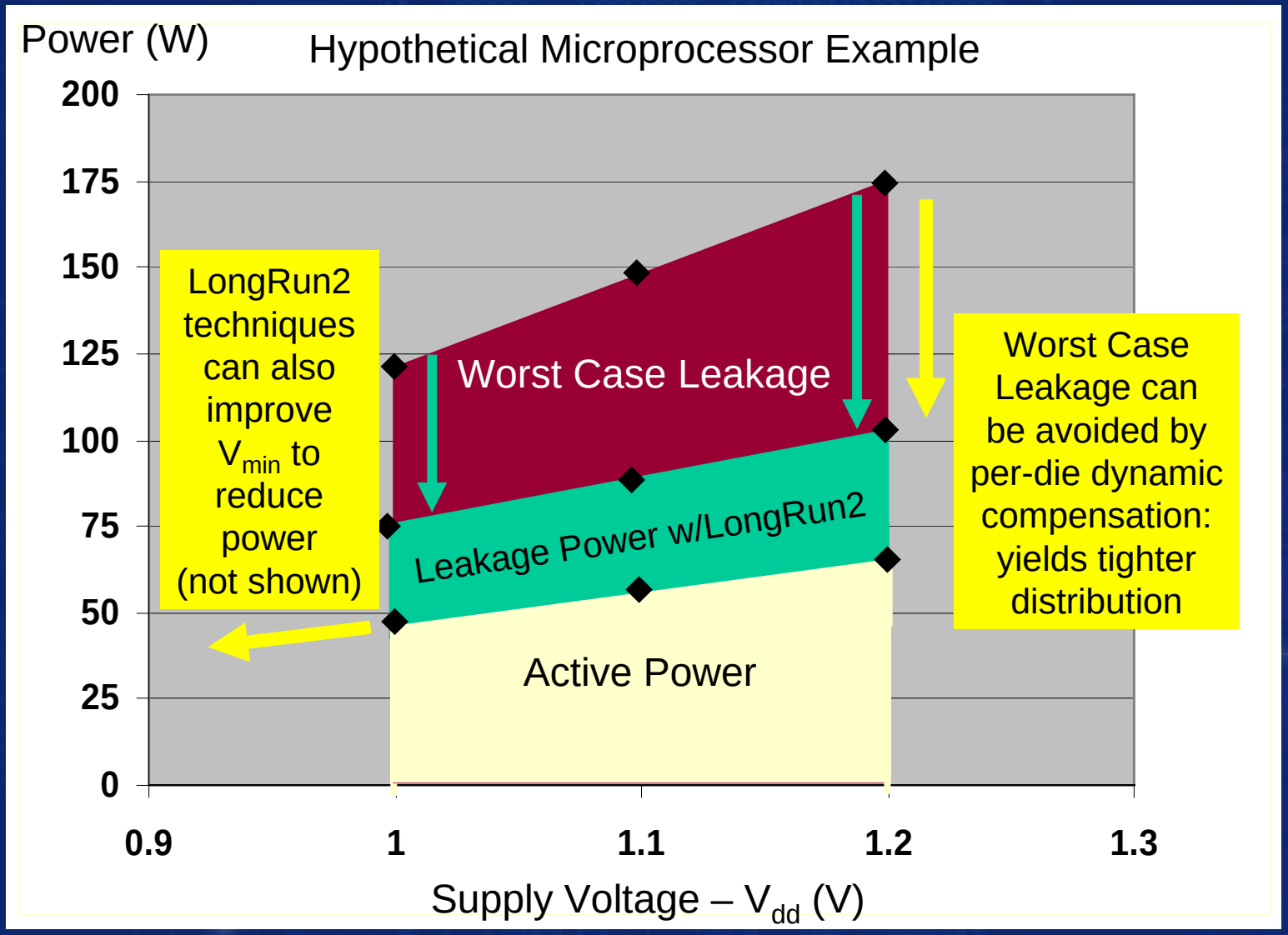
Few Bad Die

Minimize die not meeting speed

LongRun2 allows tuning of each die to meet specs

Result: Increased yield, better distribution, lower variation

Leakage Power Is Sensitive to Distribution



Early Results: NEC Cuts 65nm Standby Power by Two Orders of Magnitude

- NEC (LongRun2 Licensee) reported standby current leakage reduced by 30X to 100X using:
  - Transmeta's LongRun2
  - High-k gate dielectric

- As stated in the article, most of the power and leakage reduction is from LongRun2.

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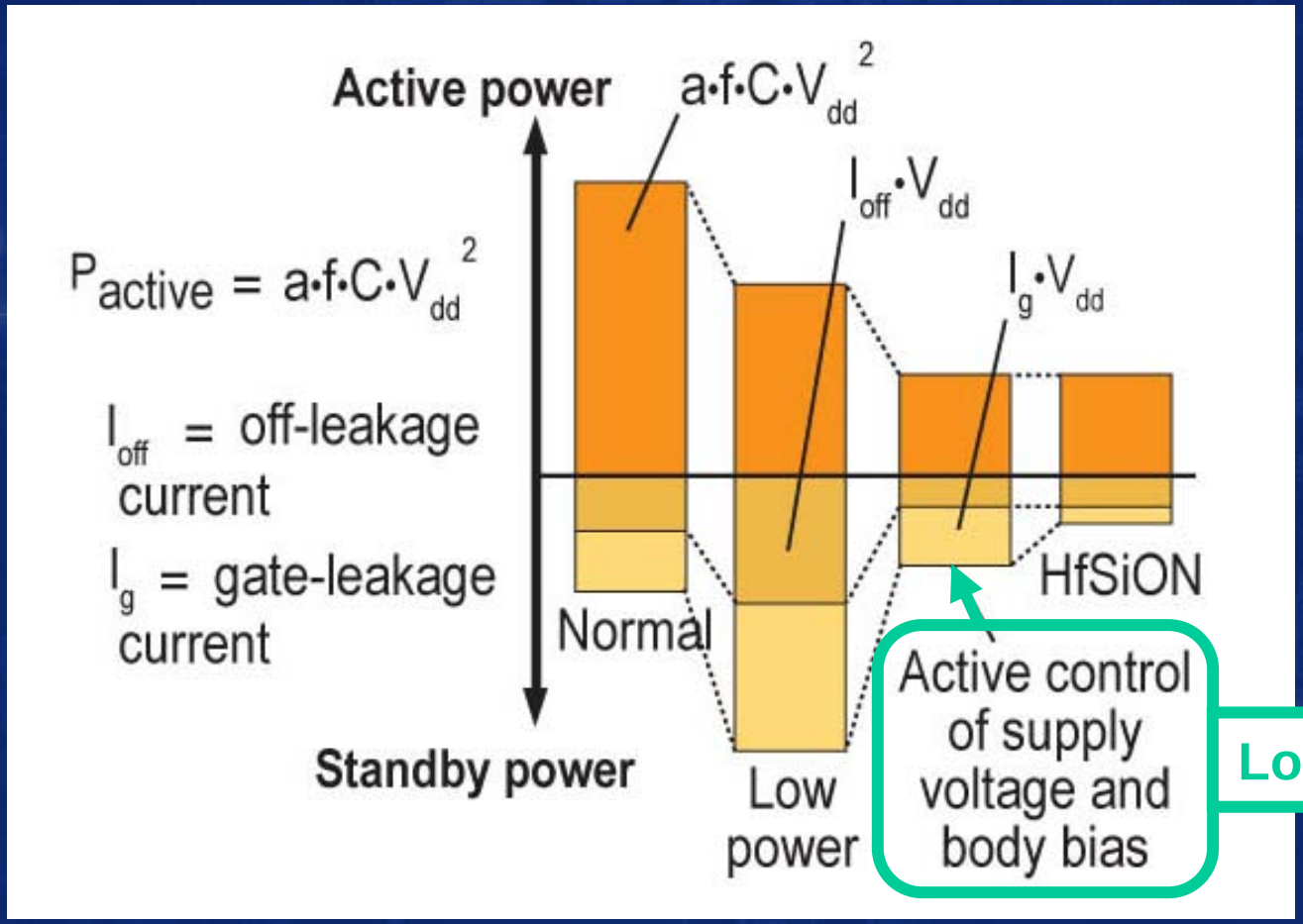
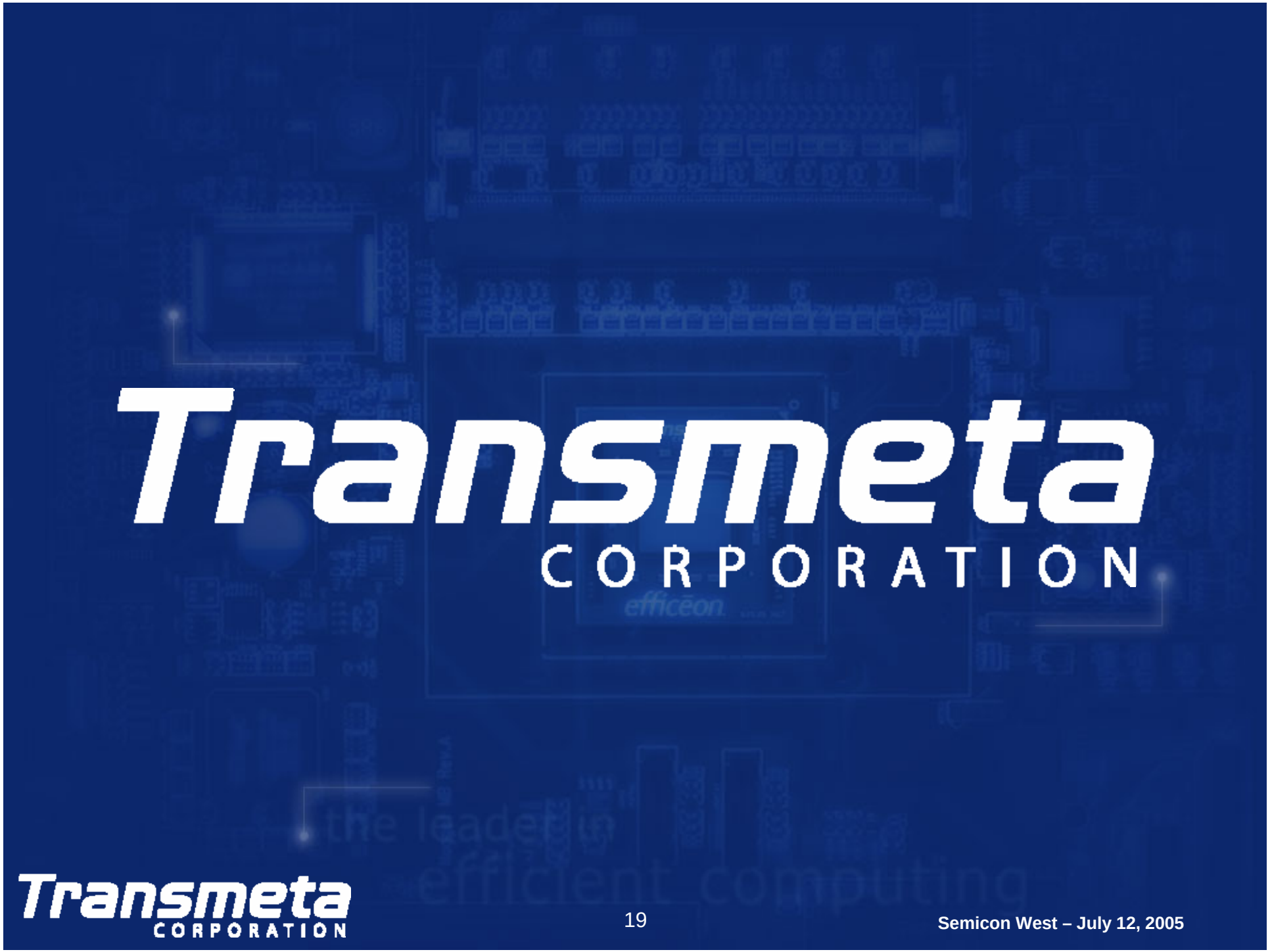


Source: **Yasushi Yamagata and Kiyotaka Imai**
NEC Electronics Corp., Advanced Device Development Div.,
***Solid State Technology*, November, 2004**

Conclusions

- **Continued innovation is required to maintain semiconductor scaling into the future**
- **LongRun2 is a practical solution to key challenges**:
  - Simper new approaches to dynamic Vt control
  - Can reduce Transistor Leakage
  - Can reduce Threshold Voltage Variation
- **Advantages**:
  - Applicable to existing CMOS designs
  - Complementary to other solutions like high-k gate dielectrics
  - May offer increased yield by reducing wafer to wafer V_t variation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