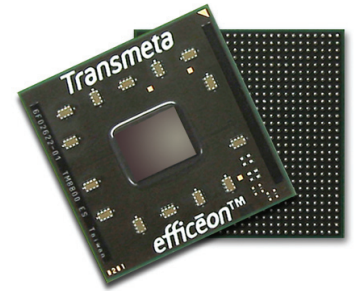![efficēon PROCESSOR]

Transmeta CORPORATION

Transmeta™ Efficeon™ TM8800 Processor

The Transmeta Efficeon TM8800 processor offers a compelling balance of low power consumption for long battery life, high performance x86-compatible processing for multimedia applications and reduced heat for quiet, fanless operation.

It features a 256-bit wide VLIW engine that can issue up to 8 instructions per clock cycle, a large 1 MB L2 cache, and support for MMX, SSE, SSE2 and SSE3 instructions for a powerful multimedia experience. It is built upon Fujitsu's next-generation 90nm silicon technology that can produce transistors with an industry-leading 40nm gate length, yielding higher frequencies with lower power requirements.

The Efficeon TM8800 processor combines the processor and Northbridge functionality into a single integrated circuit, creating a single package that reduces board space by eliminating the need for a dedicated Northbridge chip. Integrated functionality includes a high-performance DDR memory interface, a 1.6 GB/s HyperTransport™ I/O interconnect, and an AGP 4X graphics interface.

Featuring an advanced design with LongRun™ advanced dynamic power management technology, The Efficeon TM8800 is a highly integrated, reliable, antivirus enhanced processor that delivers high-performance for low power mobile, blade server and embedded designs.

Transmeta EfficeonTM8800 Processor

Lead-Free Packaging

The Efficeon TM8820 processor is Transmeta's first Lead-Free Packaging processor to be developed in accordance with industrywide initiatives. By adhering to the Restriction of Hazardous Substances (RoHS) and Waste Electronic Equipment (WEEE) initiatives, Transmeta has removed lead and other hazardous materials from processor packaging. Transmeta's adherence to environmental packaging also meets the Lead-Free Packaging standards requirements for consumer electronic devices put forth by the Japanese legislation and the European Union (EU).

Streaming SIMD Extensions (SSE3)

The Efficeon processor now contains support for Streaming SIMD Exentsions 3 (SSE3), a set of 13 new instructions that build upon SSE and SSE2. SSE3 improves performance for complex arithmetic, graphics and video encoding and provides performance at lower power consumption. SSE3 is compatible with existing software and operating systems.

Specifications	Efficeon TM8800
Processor Speed	Up to 1.7 GHz
On-die L1 Instruction Cache	128 KB
On-die L1 Data Cache	64 KB
On-die L2 Write-Back Cache	1 MB
HyperTransport System Bus Speed	400MHz
Aggregate HyperTransport Link Bandwidth	1.6 GB/s
MMX, SSE, SSE2 and SSE3 Instruction Support	Yes
Fully Integrated Northbridge Functionality	Yes
Support for DDR-266, 333 and 400 memory	Yes
Support for ECC memory	Yes
Integrated AGP 4X graphics interface	Yes
Integrated Low Pin Count Bus (LPC)	Yes
Full x86 Software and OS Compatibility	Yes
Enhanced LongRun Thermal Management	Yes
Enhanced LongRun Power Management	Yes
AntiVirusNX Technology	Yes
Process Geometry	90nm
Package Size	29mm x 29mm
Junction Temperature (Tj)	Up to 100° C
Package Type	783-pin OBGA 1mm ball pitch

AntiVirusNX TECHNOLOGY

AntiVirusNX Technology

In response to the escalating threat of computer virus attacks, Transmeta has introduced a new feature — called AntiVirusNX — that can detect common viruses and render them harmless in Efficeon processor-based computers. AntiVirusNX works in conjunction with Microsoft's Data Execution Protection (DEP) technology in Windows XP Service Pack 2, detecting and preventing attempts by attackers to overflow memory buffers with malicious virus content. AntiVirusNX represents a significant deterent to the ever increasing threat of computer viruses, including the recent Sasser, Blaster, CodeRed and BugBear worms, that leverage buffer overflows as a means of entry onto a computer operating system.

HIGH PERFORMANCE

8 Instruction Issue, 256-Bit VLIW Engine

- Fully Pentium 4-ISA compatible
- Up to eight instructions issued per clock cycle
- Up to 50% improvement in integer applications
- SSE, SSE2 and SSE3 multimedia extensions enables multimedia applications to run up to 80% faster per clock cycle than previous generation processors from Transmeta
- Large 1 MB L2 cache improves processor performance

Advanced Code Morphing Software

- Improves performance and responsiveness over 1st generation Transmeta Crusoe technology
- Unique software based architecture is key to reducing power consumption and enabling future scalability and flexibility
- New generation Code Morphing Software technology leverages 256-bit VLIW hardware advances
- Enables quick, low cost improvements to performance and power consumption with updates of Code Morphing Software

HIGHLY INTEGRATED ARCHITECTURE

Fully Integrated Northbridge Core Logic

- On-chip DDR memory interface
- Integrated AGP 2.0 compliant graphics interface for industry standard, high performance graphics solutions at 1X, 2X & 4X data rates
- On-chip 400 MHz HyperTransport interface, 8-bits wide in each direction, provides 12x the I/O throughput (1.6 GB/sec aggregate bandwidth) compared to 32-bit, 33 MHz PCI
- Full support for ECC in L2 cache and northbridge memory controller

Enables Small Form Factor Designs

- Northbridge integration reduces system chip count, power consumption and printed circuit board size

ENERGY EFFICIENT DESIGN

Enhanced LongRun Dynamic Power Management

- Enables longer battery life by dynamically adjusting operating frequency and voltage to match the performance requirements of application workloads
- Provides higher performance within smaller, thermally constrained environments

Enhanced LongRun Thermal Management

- Maximizes performance within a thermal envelope
- Low thermal characteristics enable fanless designs for quieter and more reliable systems

ADVANCED ANTIVIRUS PROTECTION

AntiVirusNX Technology

- Works in conjunction with Microsoft's Data Execution Protection (DEP) to detect and prevent attempts by attackers to overflow memory buffers with malicious virus and worm content.
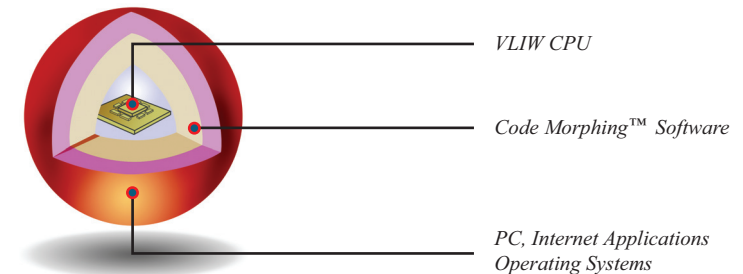
Transmeta Efficeon Processor Core

To maximize performance and responsiveness, the Efficeon processor features a state-of-the-art 256-bit-wide VLIW (Very Long Instruction Word) engine that can issue up to 8 instructions per clock cycle. A large 1 MB L2 cache and support for SSE - SSE3 instructions help make for a compelling multimedia experience.

Transmeta Code Morphing™ Software

Transmeta's proprietary Code Morphing Software (CMS) runs at the heart of the Efficeon processor, dynamically optimizing and translating x86 instructions into VLIW native code. This unique combination of hardware and software allows the processor to be more efficient, adding intelligence to the Efficeon proessor to manage power consumption and heat dissipation not found in other x86 microprocessors.

With the new Code Morphing Software for the Efficeon processor, Transmeta extends its leadership in power management, offering a solution that provides high performance while consuming less power for the same work.

VLIW CPU

Code Morphing™ Software

PC, Internet Applications Operating Systems

Transmeta Enhanced LongRun™ Power Management

LongRun power management technology provides Code Morphing software with the ability to adjust the Efficeon processor core operating voltage and clock frequency dynamically, depending on the demands placed on the processor by software. Because power varies linearly with clock speed and by the square of voltage, adjusting both processor voltage and clock frequency can produce cubic reductions in power consumption. Conventional processors can adjust power linearly, by adjusting the effective operating frequency.

LongRun power management policies are implemented within Code Morphing software, and can detect different workload scenarios based on runtime performance information, and then exploit these by adapting processor power usage accordingly. This ensures the processor delivers high performance when necessary and conserves power when demand on the processor is low.

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For more information, visit www.transmeta.com