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TRANSMETA™

Product Brief

Transmeta Efficeon Processor

The Transmeta Efficeon™ x86 compatible processor ushers in a new era of energy efficient computing. The processor was designed from the start to address the ever-growing demand for power-efficient x86 solutions. To maximize performance and responsiveness, the Efficeon processor features a 256-bit wide VLIW engine that can issue up to 8 instructions per clock cycle, a large 1 MB L2 cache, and support for SSE & SSE2 instructions for a compelling multimedia experience. The I/O features built into the Efficeon processor's integrated northbridge were selected to provide the highest system performance. These new I/O interfaces include support for DDR 400 DRAM, a 1.6 GB/s HyperTransport™ interconnect, and an AGP 4X graphics interface. With the new Code Morphing™ Software for the Efficeon processor, Transmeta extends its leadership in power management by offering a solution that provides high performance while consuming less power for the same work. The result is a highly efficient x86 solution suitable for notebook computers, Tablet PC's and many other applications where an integrated, low power x86 processor is desirable.

HIGH PERFORMANCE

8 Instruction Issue, 256-Bit VLIW Engine

- Fully x86 compatible (P4-ISA)
- Up to eight instructions issued per clock cycle
- Up to 50% improvement in integer applications
- SSE and SSE2 multimedia extensions enables multimedia applications to run up to 80% faster per clock cycle than previous generation processors from Transmeta
- Large 1 MB L2 cache improves processor performance

Advanced Code Morphing Software

- Improves performance and responsiveness over 1st generation Transmeta Crusoe technology
- New generation Code Morphing Software technology leverages 256-bit VLIW hardware advances
- Unique software based architecture is key to reducing power consumption and enabling future scalability and flexibility
- Enables quick, low cost improvements to performance and power consumption with updates of Code Morphing Software

HIGHLY INTEGRATED ARCHITECTURE

Fully Integrated Northbridge Core Logic

- On-chip DDR-400 memory interface
- Integrated AGP 2.0 compliant graphics interface for industry standard, high performance graphics solutions at 1X, 2X & 4X data rates
- On-chip 400 MHz HyperTransport interface, 8-bits wide in each direction, provides 12x the I/O throughput compared to 32-bit, 33 MHz PCI.
- Full support for ECC in L2 cache and northbridge memory controller enables expansion into the server market.

Enables Small Form Factor Designs

- Northbridge integration reduces system chip count, power consumption and PCB size

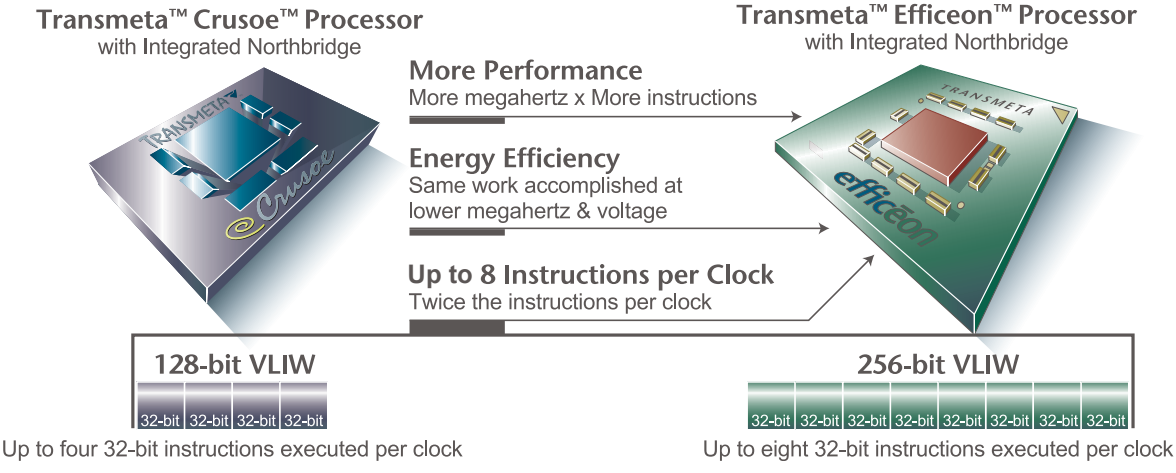
ENERGY EFFICIENT DESIGN

Enhanced LongRun™ Dynamic Power Management

- Enables longer battery life by continually adjusting operating frequency and voltage to match the performance requirements of application workloads
- More efficient than typical duty cycle clock throttling power management schemes

Enhanced LongRun Thermal Management

- Maximizes performance within a thermal envelope
- Low thermal characteristics enable fanless designs for quieter and more reliable systems



Transmeta™ Efficeon™ Processor

Transmeta Efficeon Processor Core

At the heart of the Transmeta Efficeon processor is a state-of-the-art VLIW (Very Long Instruction Word) hardware engine. This hardware engine processes instructions like a conventional processor, but runs a custom, efficient instruction set. Running on the processor is Transmeta's proprietary Code Morphing Software (CMS), the Efficeon software component that dynamically optimizes and translates x86 instructions into VLIW native code. This unique combination of hardware and software adds intelligence not found in other x86 microprocessors, allowing the Efficeon processor to manage power consumption and heat.

Transmeta Enhanced LongRun Power Management

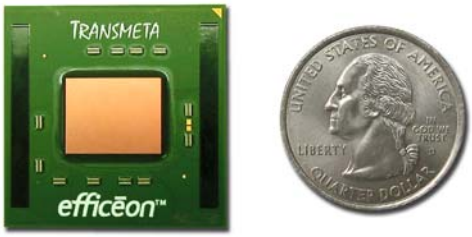
Unlike conventional x86 processors, Transmeta's Enhanced LongRun power management technology is part of the Efficeon processor's Code Morphing Software. This combination allows the Efficeon processor to seamlessly adjust its operating frequency and voltage up to hundreds of times per second — dramatically extending battery life, limiting heat dissipation and providing rapid system responsiveness.

Smallest Solution Footprint

	Component	Package
CPU / Northbridge	Efficeon (included)	841mm^2
	Total	841mm^2
CPU	Pentium-M	1232mm^2
Northbridge	855PM	1406mm^2
	Total	2638mm^2

Efficeon is less than 1/3 the size of Pentium-M and 855PM

Source: *http://www.intel.com — Intel® Pentium® M Processor Datasheet, June 2003; Intel® 855PM Chipset Memory Controller Hub (MCH) DDR 200/266 MHz Datasheet, March 2003*



Quarter used to show relative size.

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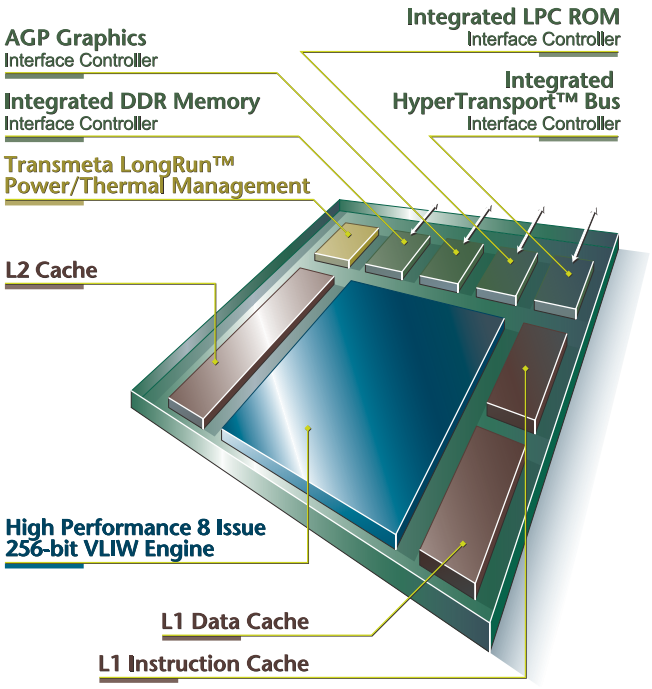
Block Diagram



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Specifications	
On-die L1 Instruction Cache	128 KB
On-die L1 Data Cache	64 KB
On-die L2 Write-Back Cache	1 MB
HyperTransport System Bus Speed	800 Megatransfers/s
Aggregate HyperTransport Link Bandwidth	1.6 GB/s
MMX, SSE, SSE2 Instruction Support	Yes
Fully Integrated Northbridge Functionality	Yes
Integrated AGP 1X, 2X, and 4X graphics interface	Yes
Support for DDR-266, 333, 400 memory	Yes
Support for ECC memory	Yes
Integrated Low Pin Count Bus (LPC)	Yes
Full x86 Software and OS Compatibility	Yes
Enhanced LongRun Thermal Management	Yes
Enhanced LongRun Power Management	Yes
Package Size	29mmx29mm

For more information, visit **www.transmeta.com**

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