efficēon PROCESSOR

Transmeta CORPORATION

Product Sheet

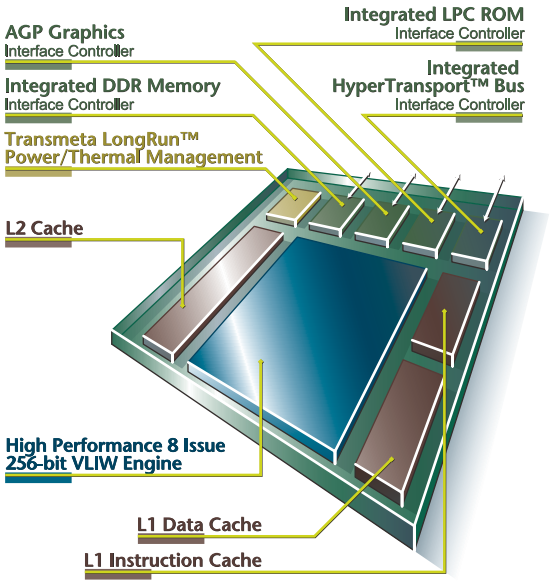
Transmeta™ Efficeon™ TM8600 Processor

The Transmeta Efficeon x86 compatible processor ushers in a new era of energy efficient computing. The processor was designed from the start to address the ever-growing demand for power-efficient x86 solutions. To maximize performance and responsiveness, the Efficeon processor features a 256-bit wide VLIW engine that can execute up to 8 instructions per clock cycle, a large 1 MB L2 cache, and support for SSE & SSE2 instructions for a compelling multimedia experience. The I/O interfaces built into the Efficeon processor's integrated Northbridge are matched with its high performance core featuring support for DDR-400 DRAM, a 1.6 GB/s HyperTransport™ interconnect, and an AGP 4X graphics interface. With the new Code Morphing Software for the Efficeon processor, Transmeta extends its leadership in power management, offering a solution that provides high performance while consuming less power for the same work. The result is a highly efficient x86 solution suitable for notebook computers, Tablet PC's and many other applications where an integrated, low power x86 processor is desirable.

Specifications	
Processor Speed	1.0 GHz - 1.1 GHz
On-die L1 Instruction Cache	128 KB
On-die L1 Data Cache	64 KB
On-die L2 Write-Back Cache	1 MB
HyperTransport System Bus Speed	400 MHz
Aggregate HyperTransport Link Bandwidth	1.6 GB/s
MMX, SSE and SSE2 Instruction Support	Yes
Fully Integrated Northbridge Functionality	Yes
Support for DDR-266, 333 memory	Yes
Support for ECC memory	Yes
Integrated AGP 4X graphics interface	Yes
Integrated Low Pin Count Bus (LPC)	Yes
Full x86 Software and OS Compatibility	Yes
Enhanced LongRun Thermal Management	Yes
Enhanced LongRun Power Management	Yes
Process Geometry	TSMC 130nm
Package Size	29mm x 29mm
Junction Temperature (Tj)	Up to 100° C
Package Type	783-pin OBGA with 1mm ball pitch

Transmeta™ Efficeon™ Processor

Block Diagram



Smallest Solution Footprint

	Component	Package
CPU	Efficeon	841mm²
Northbridge	(included)	
	Total	841mm²
CPU	Pentium-M	1232mm²
Northbridge	855PM	1406mm²
	Total	2638mm²

Efficeon is less than 1/3 the size of Pentium-M and 855PM

Source: *http://www.intel.com — Intel® Pentium® M Processor Datasheet, June 2003; Intel® 855PM Chipset Memory Controller Hub (MCH) DDR 200/266 MHz Datasheet, March 2003*

Transmeta Efficeon TM8600 Processor

HIGH PERFORMANCE

8 Instruction Issue, 256-Bit VLIW Engine

- Fully Pentium 4-ISA compatible
- Up to eight instructions issued per clock cycle
- Up to 50% improvement in integer applications
- SSE and SSE2 multimedia extensions enables multimedia applications to run up to 80% faster per clock cycle than previous generation processors from Transmeta
- Large 1 MB L2 cache improves processor performance

Advanced Code Morphing Software

- Improves performance and responsiveness over 1st generation Transmeta Crusoe technology
- Unique software based architecture is key to reducing power consumption and enabling future scalability and flexibility
- New generation Code Morphing Software technology leverages 256-bit VLIW hardware advances
- Enables quick, low cost improvements to performance and power consumption with updates of Code Morphing Software

HIGHLY INTEGRATED ARCHITECTURE

Fully Integrated Northbridge Core Logic

- On-chip DDR-266/333 memory interface
- Integrated AGP 2.0 compliant graphics interface for industry standard, high performance graphics solutions at 1X, 2X & 4X data rates
- On-chip 400 MHz HyperTransport interface, 8-bits wide in each direction, provides 12x the I/O throughput (1.6 GB/sec aggregate bandwidth) compared to 32-bit, 33 MHz PCI
- Full support for ECC in L2 cache and northbridge memory controller enables expansion into the server market

Enables Small Form Factor Designs

- Northbridge integration reduces system chip count, power consumption and PCB size

ENERGY EFFICIENT DESIGN

Enhanced LongRun Dynamic Power Management

- Enables longer battery life by dynamically adjusting operating frequency and voltage to match the performance requirements of application workloads
- Provides higher performance within smaller, thermally constrained environments

Enhanced LongRun Thermal Management

- Maximizes performance within a thermal envelope
- Low thermal characteristics enable fanless designs for quieter and more reliable systems

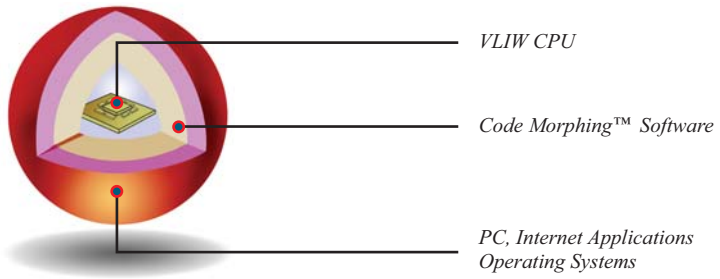
Transmeta Efficeon Processor Core

To maximize performance and responsiveness, the Efficeon processor features a state-of-the-art 256-bit-wide VLIW (Very Long Instruction Word) engine that can issue up to 8 instructions per clock cycle. A large 1 MB L2 cache and support for SSE & SSE2 instructions help make for a compelling multimedia experience.

Transmeta Code Morphing™ Software

Transmeta's proprietary Code Morphing Software (CMS) runs at the heart of the Efficeon processor, dynamically optimizing and translating x86 instructions into VLIW native code. This unique combination of hardware and software allows the processor to be more efficient, adding intelligence to the Efficeon proessor to manage power consumption and heat dissipation not found in other x86 microprocessors.

With the new Code Morphing Software for the Efficeon processor, Transmeta extends its leadership in power management, offering a solution that provides high performance while consuming less power for the same work.



Transmeta Enhanced LongRun™ Power Management

LongRun power management technology provides Code Morphing software with the ability to adjust the Efficeon processor core operating voltage and clock frequency dynamically, depending on the demands placed on the processor by software. Because power varies linearly with clock speed and by the square of voltage, adjusting both processor voltage and clock frequency can produce cubic reductions in power consumption. Conventional processors can adjust power linearly, by adjusting the effective operating frequency.

LongRun power management policies are implemented within Code Morphing software, and can detect different workload scenarios based on runtime performance information, and then exploit these by adapting processor power usage accordingly. This ensures the processor delivers high performance when necessary and conserves power when demand on the processor is low.

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For more information, visit **www.transmeta.com**

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QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO 9001:2000

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