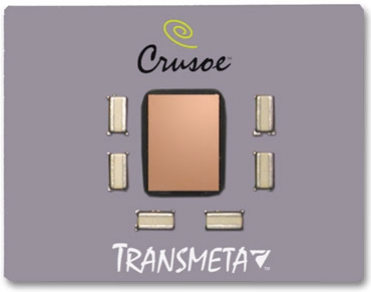
Crusoe™ Processor Product Brief
Model TM5500



Crusoe™ Processor Model TM5500 Features

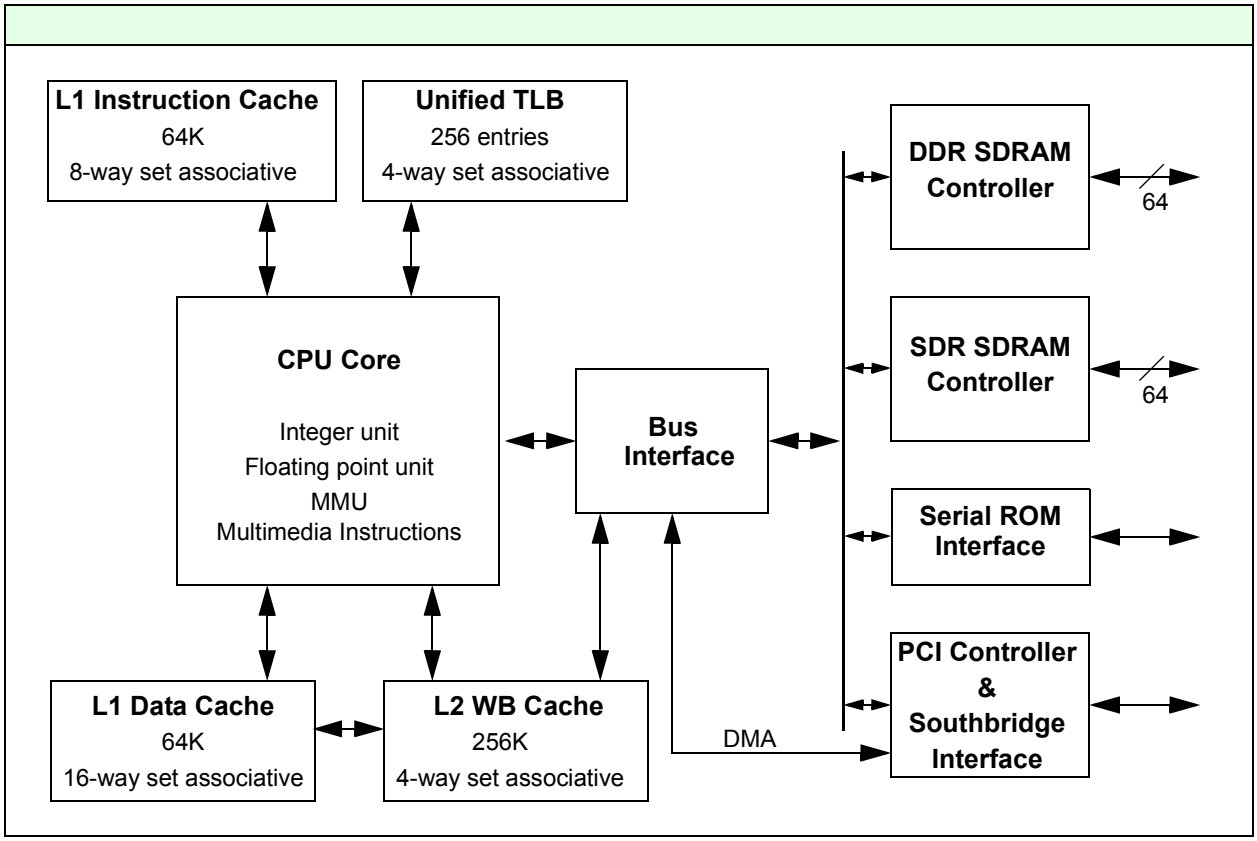
- VLIW processor and x86 Code Morphing™ software provide x86-compatible mobile platform solution
- Processors fabricated in latest 0.13µ process technology operate up to 1000 MHz at very low power levels
- Standard product speed of 800 MHz
- Integrated 64 KByte L1 instruction cache, 64 KByte L1 data cache, and 256 KByte L2 write-back cache
- Integrated northbridge core logic features facilitate compact system designs
  - DDR SDRAM memory controller with 100-133 MHz, 2.5V interface
  - SDR SDRAM memory controller with 100-133 MHz, 3.3V interface
  - PCI bus controller (PCI 2.1 compliant) with 33 MHz, 3.3V interface
- LongRun™ advanced power management with low-power operation extends battery life
  - 0.5-1.5 W @ 300-800 MHz, 0.9-1.3V running typical multimedia applications
  - 250 mW typical in deep sleep
- Full System Management Mode (SMM) support
- Compact 474-pin ceramic BGA package

Transmeta Crusoe TM5500 processors are low-power, high-speed microprocessors, based on an advanced VLIW core architecture. When used in conjunction with Transmeta's x86 Code Morphing software, these Crusoe processors provide x86-compatible software execution using dynamic binary code translation, without requiring code recompilation. In addition to the VLIW core, these processors incorporate separate 64 KByte instruction and data caches, a large 256 KByte L2 write-back cache, 64-bit DDR SDRAM memory controller, 64-bit SDR SDRAM memory controller, and 32-bit PCI controller. These additional functional units, which are typically part of the core system logic that surrounds the microprocessor, allow Crusoe TM5500 processors to provide highly integrated and cost effective platform solutions for x86 software-compatible mobile and low-power applications. The processor core operates from a 0.9-1.3 V supply, resulting in extremely low power consumption, even at high operating frequencies. With power consumption during typical operation as low as 250 mW, Crusoe TM5500 processors are among the most energy efficient high-performance x86-compatible mobile solutions available today.

1.0 Architecture

Crusoe TM5500 processors incorporate integer and floating point execution units, separate instruction and data caches, a level-2 write-back cache, memory management unit, and multimedia instructions. In addition to these traditional processor features, the devices integrate a DDR SDRAM controller, SDR SDRAM controller, PCI bus controller and serial ROM interface controller. These additional units are usually part of the core system logic that surrounds the microprocessor. The VLIW processor, in combination with Code Morphing software and the additional system core logic units, allow the Crusoe TM5500 processor to provide a highly integrated, low-power, high performance platform solution for the x86 mobile market. The Crusoe TM5500 processor block diagram is shown in Figure 1.

Figure 1 Crusoe TM5500 Processor Block Diagram



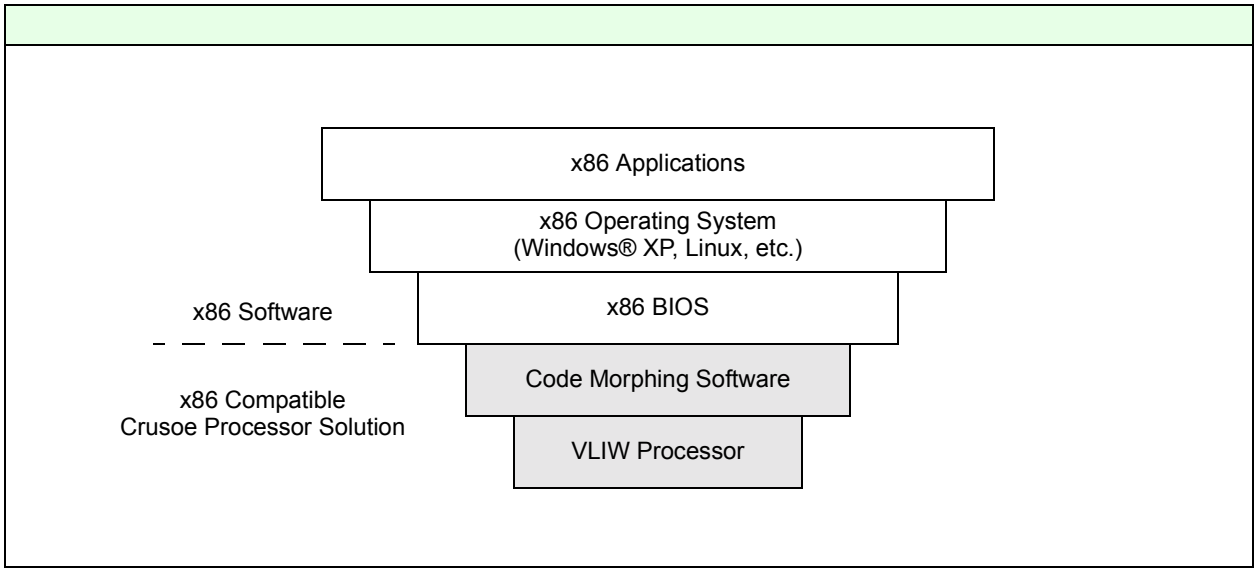
2.0 Processor Core

The Crusoe TM5500 processor core architecture is relatively simple compared to conventional x86 processors. It is based on a very long instruction word (VLIW) 128-bit instruction set. Within this VLIW architecture, the control logic of the processor is kept very simple and software is used to control the scheduling of instructions. This allows a simplified and very straightforward hardware implementation with an in-order 7-stage integer pipeline and a 10-stage floating point pipeline. By streamlining the processor hardware and reducing the control logic transistor count, the performance-to-power consumption ratio (energy efficiency) can be greatly improved over conventional x86 architectures.

Crusoe TM5500 processors include a 64 KByte 8-way set-associative level 1 (L1) instruction cache, and a 64 KByte 16-way set associative L1 data cache. These processors also include an integrated 256 KByte level 2 (L2) write-back cache for improved effective memory bandwidth and enhanced performance. This cache architecture assures maximum internal memory bandwidth for performance intensive applications, while maintaining the same low-power implementation that provides superior energy efficiency relative to previous x86 processors.

Other than having execution hardware for logical, arithmetic, shift, and floating point instructions, as in conventional processors, Crusoe TM5500 processors have very distinctive features from traditional x86 processor designs. To ease the translation process from x86 to the core VLIW instruction set, the hardware generates the same condition codes as conventional x86 processors and operates on the same 80-bit floating point numbers. Also, the translation look-aside buffer (TLB) has the same protection bits and address mapping as other x86 processors. The software component of this solution is used to emulate all other features of the x86 architecture. The software that converts x86 programs into the core VLIW instructions is called Code Morphing software. The combination of Code Morphing software and the VLIW core together act as an x86-compatible solution, as shown in Figure 2.

Figure 2 Crusoe Processor Software Hierarchy



The typical behavior of Code Morphing software is to execute a loop that decodes and executes x86 instructions. The first few times a specific x86 code sequence is executed, Code Morphing software interprets the code by decoding the instructions one byte at time, and then dispatching execution to corresponding VLIW native instruction subroutines. Once the x86 code has been executed several times, Code Morphing software translates the x86 instructions into highly optimized and extremely fast VLIW native instructions, executes the translated code, and caches the native instruction translations for future use. If the same x86 code is required to execute again, the high-performance cached translations are executed immediately and no re-translation is required.

2.1 Integrated DDR SDRAM Memory Controller

The DDR SDRAM interface is the highest performance memory interface available on Crusoe TM5500 processors. The DDR SDRAM controller supports only double data rate (DDR) SDRAM and transfers data at a rate twice the clock frequency of the interface. The DDR SDRAM controller supports a single bank of memory, depending on the memory configuration selected, using a 64-bit wide interface. This is equivalent to a single small outline dual In-line memory module (SODIMM) of DDR SDRAM.

The DDR SDRAM memory can be populated with 64 Mbit, 128 Mbit, 256 Mbit, or 512 Mbit devices. To reduce signal loading, only x8 or x16 devices should be used. The table below shows supported DDR SDRAM configurations.

Table 1 DDR SDRAM Interface Memory Configurations

DDR Device Size	DDR Device Configuration	DDR Devices per Bank	Memory Size per Bank	Maximum Banks	Maximum Memory Size
64 Mbit	4M x 16	4	32 MBytes	1	32 MBytes
	8M x 8	8	64 MBytes	1	64 MBytes
128 Mbit	8M x 16	4	64 MBytes	1	
	16M x 8	8	128 MBytes	1	128 MBytes
256 Mbit	16M x 16	4	128 MBytes	1	
	32M x 8	8	256 MBytes	1	256 MBytes
512 Mbit	32M x 16	4	256 MBytes	1	
	64M x 8	8	512 MBytes	1	512 MBytes

The frequency setting for the DDR SDRAM interface is initialized during the power-on boot sequence. The DDR SDRAM interface can be configured to operate over a frequency range of 83-133 MHz. DDR SDRAM interface frequency settings can vary at each LongRun power management operating point, as shown in the LongRun power management operating point table.

2.2 Integrated SDR SDRAM Memory Controller

The SDR SDRAM memory controller supports up to four banks, equivalent to two small outline dual In-line memory modules (SODIMMS), of single data rate (SDR) SDRAM that can be configured as 64-bit SODIMMs. These SODIMMs can be populated with 64 Mbit, 128 Mbit, 256 Mbit, or 512 Mbit devices. All SODIMMs must use the same frequency SDRAMs, but there are no restrictions on mixing different SODIMM configurations into each SODIMM slot. The table below shows supported SDR SDRAM configurations.

Table 2 SDR SDRAM Interface Memory Configurations

DDR Device Size	DDR Device Configuration	DDR Devices per Bank	Memory Size per Bank	Maximum Banks	Maximum Memory Size
64 Mbit	4M x 16	4	32 MBytes	4	128 MBytes
	8M x 8	8	64 MBytes	2	
	16M x 4	16	128 MBytes	1	
128 Mbit	8M x 16	4	64 MBytes	4	256 MBytes
	16M x 8	8	128 MBytes	2	
	32M x 4	16	256 MBytes	1	
256 Mbit	16M x 16	4	128 MBytes	4	512 MBytes
	32M x 8	8	256 MBytes	2	
	64M x 4	16	512 MBytes	1	
512 Mbit	32M x 16	4	256 MBytes	4	1024 MBytes
	64M x 8	8	512 MBytes	2	

The frequency setting for the SDR SDRAM interface is initialized during the power-on boot sequence. The SDR SDRAM interface can be configured to operate over a frequency range of 66-133 MHz. SDR SDRAM interface frequency settings can vary at each LongRun power management operating point, as shown in the LongRun power management operating point table. Each SDR SDRAM SODIMM should be limited to a maximum of 8 memory devices in order to operate at the required frequency with the proper signal integrity.

2.3 Integrated PCI Controller

Crusoe TM5500 processors include a PCI bus controller that is PCI 2.1 compliant. The PCI bus is 32 bits wide, operates at 33 MHz, and is compatible with 3.3 V signal levels. The PCI bus interface is not 5 V tolerant. The PCI controller on the processor provides a PCI host bridge, the PCI bus arbiter, and a DMA controller.

The PCI bus can sustain 132 Mbyte per second bursts for reads and writes on 4 KByte blocks. The PCI controller snoops ahead on PCI-to-DRAM reads and writes. The 16-Dword processor-to-PCI write buffer converts sequential memory mapped I/O writes to PCI bursts. The DMA controller handles PCI-to-DRAM reads and writes. The 16-Dword PCI-to-DRAM write buffer converts one 16-Dword burst to eight separate address/data pairs. The 16-Dword DRAM-to-PCI read ahead buffer permits continuation of read ahead activity after hitting in the buffer. The PCI controller tri-states the PCI bus when hot docking.

2.4 Serial ROM Interface

The Crusoe TM5500 processor 5-pin serial ROM interface is used to read data from a serial flash ROM. The flash ROM is 1 MByte in size and provides non-volatile storage for Code Morphing software. During the boot process, Code Morphing software code is copied from the ROM to the Code Morphing memory space in SDRAM. Once transferred, the Code Morphing software code requires 16 MBytes of memory space. The portion of SDRAM space reserved for Code Morphing software is not visible to x86 code. This interface can also be used for in-system reprogramming of the flash ROM.

3.0 Software Compatibility

When used in conjunction with Transmeta's x86 Code Morphing software, Crusoe TM5500 processors provide x86-compatible software execution without requiring code recompilation. Systems based on this solution are capable of executing all standard x86-compatible operating systems and applications, including Microsoft® Windows® 9x, Windows® ME, Windows® NT, Windows® 2000, Windows® XP, and Linux.

4.0 Power and Thermal Management

Crusoe TM5500 processors operate from a 0.9-1.3 V core voltage supply at very low power levels, even while delivering high application performance. These processors incorporate LongRun adaptive power and thermal management technologies. LongRun power management dynamically reduces the core processor power consumption to near-optimal levels in response to application workload requirements. LongRun thermal management intelligently adapts Crusoe TM5500 processor operation to system thermal environments.

4.1 Power Management States

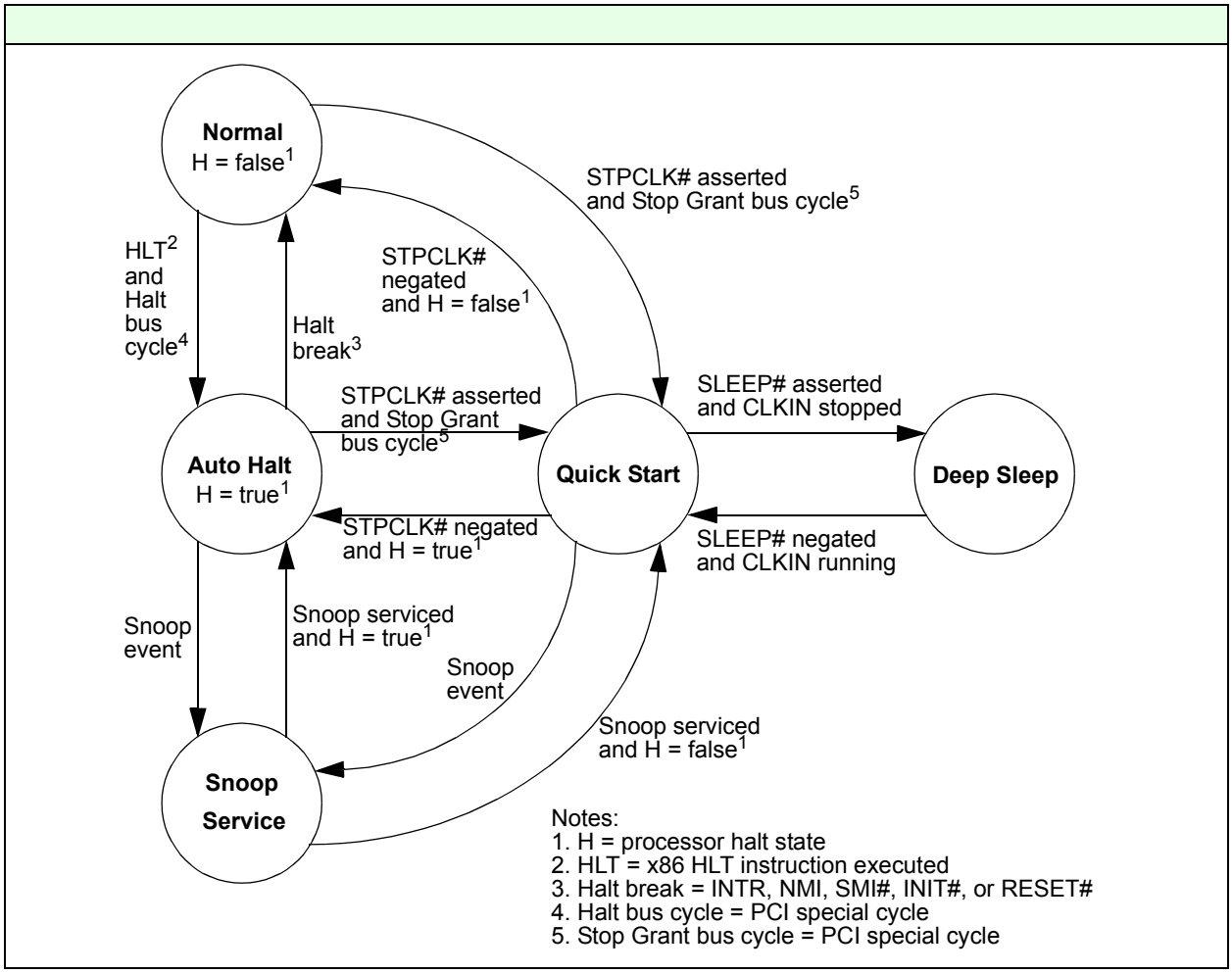
Crusoe TM5500 processors, in conjunction with Code Morphing software, support industry standard ACPI-compliant power management modes, with five distinct processor power states: *Normal*, *Auto Halt*, *Quick Start*, *Deep Sleep*, and *Off*. These power states may be used to reduce the operating power of the processor during system states that require little or no processor activity. Table 3 lists the state of the processor for each of the ACPI global system states.

Table 3 Crusoe Processor Power Management System States

ACPI System State		Processor State	SDRAM	Clock Generator
G0 / S0 / C0	Working	Normal	Normal	Running
G0 / S0 / C1	Auto Halt	Auto Halt	Normal/Self Refresh	Running
G0 / S0 / C2	Quick Start	Quick Start	Self Refresh	Running
G0 / S0 / C3	Deep Sleep	Deep Sleep	Self Refresh	Clocks Stopped
G1 / S1	Sleeping	Deep Sleep	Self Refresh	PLL Shut Down
G1 / S3	Suspend-to-RAM	Off	Self Refresh	PLL Shut Down
G1 / S4	Suspend-to-Disk	Off	Off	Off
G2 / S5	Soft Off	Off	Off	Off
G3	Mechanical Off	Off	Off	Off

The Crusoe TM5500 processor power management state diagram, Figure 3 below, shows the state transitions between the various processor power management states and the conditions driving these transitions.

Figure 3 Power Management State Diagram

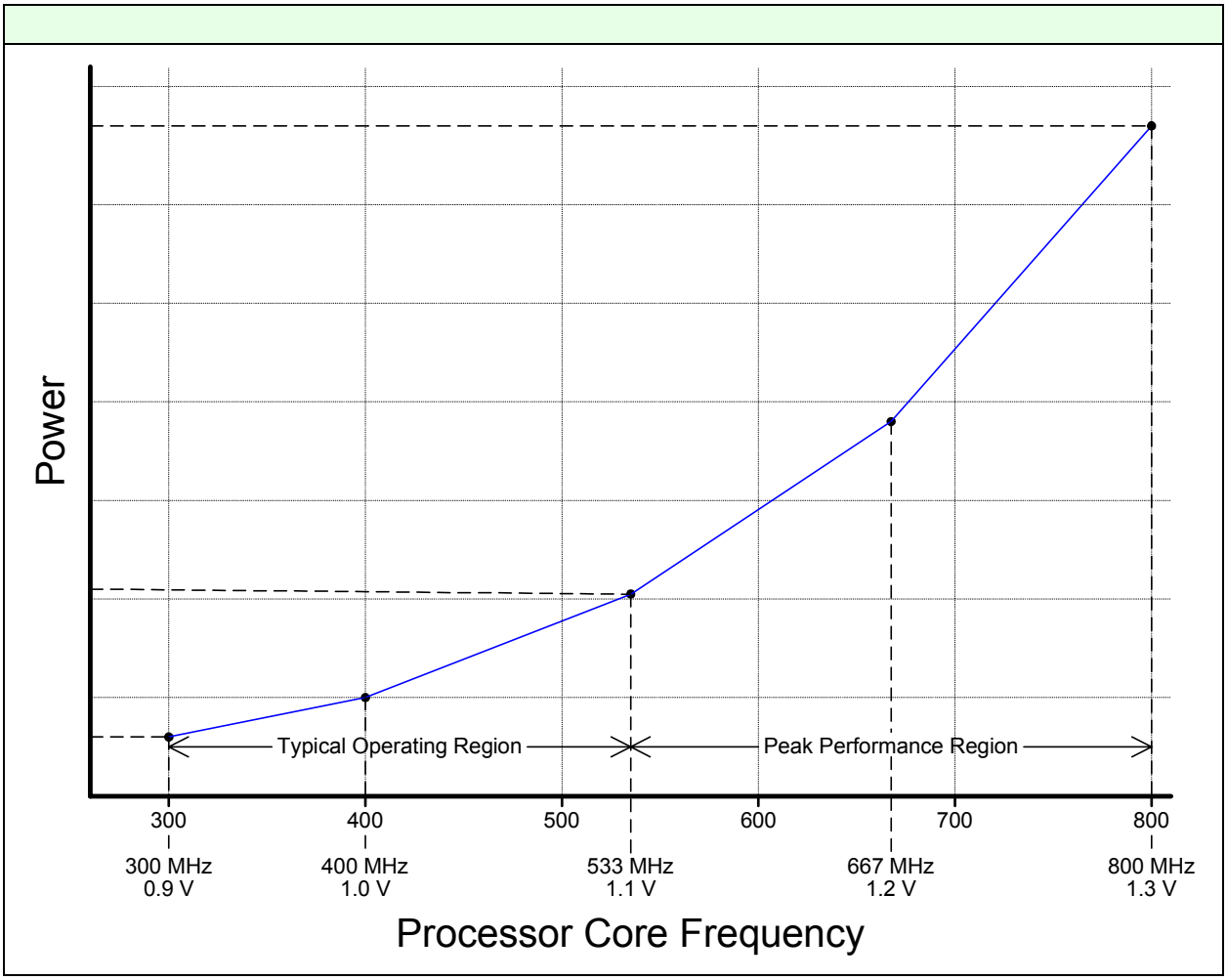


4.2 LongRun Power Management

LongRun power management provides Code Morphing software with the ability to adjust the Crusoe TM5500 processor core operating voltage and clock frequency dynamically, depending on the demands placed on the processor by application software. Because power varies linearly with clock speed and by the square of voltage, adjusting both processor voltage and clock frequency can produce cubic reductions in power consumption, whereas conventional processors can adjust power only linearly by adjusting the effective operating frequency.

LongRun power management policies are implemented within Code Morphing software and can detect different workload scenarios based on runtime performance information, and then exploit these by adapting processor power usage accordingly. This ensures the processor delivers high performance when necessary and conserves power when demand on the processor is low. All power adjustments are transparent to the operating system, power management controller, and the user. LongRun power management uses a number of core frequency/voltage operating points, allowing Crusoe TM5500 processors to optimize for the lowest power and maximum performance along this operating curve, as shown in Figure 4 below.

Figure 4 LongRun Power Management Operating Points - 800 MHz TM5500 Processors



Processor core frequency, core voltage, DDR and SDR memory interface frequency, and thermal design power (TDP) at the standard LongRun power management operating points are provided in Table 4 below.

Table 4 Crusoe TM5500 LongRun Power Management Operating Points and Power

Processor				Memory Interface		Power
	Core			DDR-266	SDR-133	
SKU	MHz	V	T_j Max	MHz	MHz	TDP
TM5500-800-1.0	800	1.30	100 °C	133	133	8.0 W
	667	1.20		133	133	
	533	1.10		133	133	
	400	1.00		133	133	
	300	0.90		100	100	

Most conventional x86 processors utilize ACPI policies to regulate their power consumption, with the processor rapidly alternating between running at full speed and being effectively turned off (called clock-throttling). This approach can potentially disable the processor just when a critical application needs it. In contrast, LongRun power management dynamically selects the optimal clock speed and operating voltage needed to run the application, thereby allowing maximum energy efficiency. LongRun power management works in conjunction with ACPI. When the processor frequency and voltage scaling reaches the minimum LongRun power management operating point, the processor transparently switches over to traditional power models, allowing policies such as ACPI to handle power management at very low-power operating points.

4.3 LongRun Thermal Management

Thermal management of Crusoe TM5500 processors is integrated into the LongRun power management dynamic operating point policies. LongRun thermal management policy manages the processor thermal environment by using frequency/voltage operating point shifts as a substitute for thermal throttling. In contrast to conventional thermal management techniques, LongRun thermal management delivers higher performance at the same die temperature, or the same performance at a lower die temperature. LongRun thermal management essentially expands the thermal budget of the processor. LongRun thermal management maximizes system performance and maintains safe processor operating temperatures within constrained thermal environments. LongRun thermal management is recommended for all Crusoe TM5500 processor-based systems.

Crusoe TM5500 processors provide an integrated on-die thermal diode. The thermal diode can be connected to an external temperature sensor and the processor junction temperature monitored by system BIOS and application software.

4.4 Typical Operating Power

Table 5 below shows typical Crusoe TM5500 processor power consumption for each of the processor power management states.

Table 5 Crusoe TM5500 Typical Power Consumption (300-800 MHz 0.9-1.3 V)

Application Workload	ACPI State	Typical Processor Power	Notes
DVD Playback	C0-C3	1.5 W	1, 2
MP3 Playback	C0-C3	0.75 W	1, 3
Auto Halt	C1	0.45 W	1
Quick Start	C2	0.35 W	1
Deep Sleep	C3	0.25 W	1

1. All power supplies at their nominal operating values. Full system power management enabled, including LongRun power management.
2. Typical DVD power is measured while running the Win DVD® 2000 player under Windows® 2000.
3. Typical MP3 power measured while running MMJukebox under Windows® 2000.