Crusoe™

TM5700/TM5900 Data Book

Crusoe Processors Described in this Document

Processor							Memory
SKU	Package Marking	L2 Cache	Max Core Frequency	Core Voltage	T_j Max	TDP	DDR
TM5900-1000-6.5 CoolRun80	5900A100010	512 KBytes	1000 MHz	0.80-1.25 V	80/100 °C	6.5 W	133 MHz
TM5900-1000-7.5 CoolRun80	5900B100010	512 KBytes	1000 MHz	0.80-1.30 V	80/100 °C	7.5 W	133 MHz
TM5900-1000-8.5 CoolRun80	5900C100010	512 KBytes	1000 MHz	0.80-1.35 V	80/100 °C	8.5 W	133 MHz
TM5900-1000-9.5 CoolRun80	5900D100010	512 KBytes	1000 MHz	0.80-1.40 V	80/100 °C	9.5 W	133 MHz
TM5900-933-8.5 CoolRun80	5900C093310	512 KBytes	933 MHz	0.80-1.35 V	80/100 °C	8.5 W	133 MHz
TM5900-800-6.6 CoolRun80	5900A080010	512 KBytes	800 MHz	0.80-1.25 V	80/100 °C	6.6 W	133 MHz
TM5700-667-5.0 CoolRun80	5700E066710	256 KBytes	667 MHz	0.80-1.15 V	80/100 °C	5.0 W	133 MHz

Crusoe™ Processor Model TM5700/TM5900
Data Book
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Property of:

Transmeta Corporation
3990 Freedom Circle
Santa Clara, CA 95054
USA
(408) 919-3000
http://www.transmeta.com

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Introduction

The Transmeta Crusoe™ processor model TM5700/TM5900 is a high performance, low power microprocessor based on a VLIW core architecture. When combined with Transmeta's x86 Code Morphing™ software, the TM5700/TM5900 processor provides x86-compatible code execution. TM5700/TM5900 processors deliver highly integrated, cost-effective processor solutions, incorporating L2 cache, support for double data rate (DDR) SDRAM, and a PCI controller. TM5700/TM5900 processors also provide power management controls, SMM and thermal monitoring capabilities, and operate at very voltage levels, making them ideal for mobile applications.

Crusoe™ Processor Model TM5700/TM5900 Features

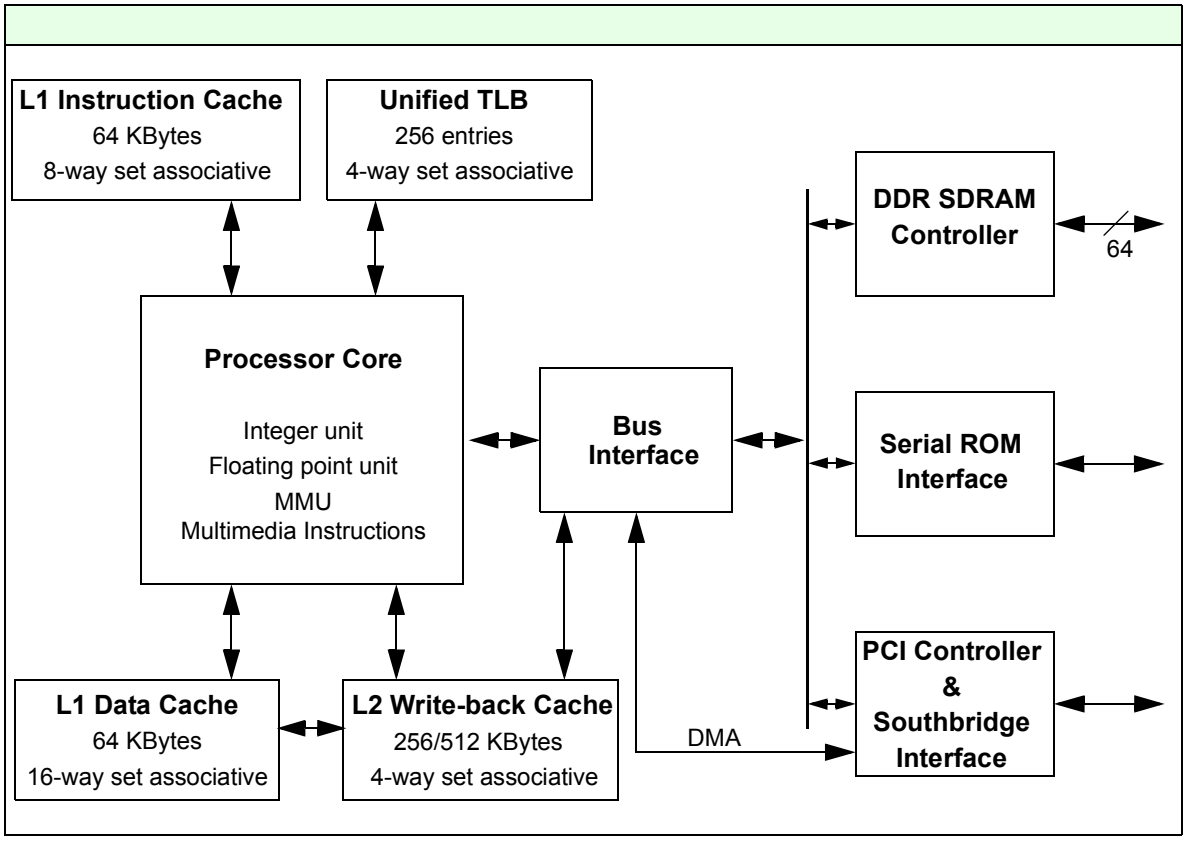
- VLIW processor and x86 Code Morphing™ software provides x86-compatible mobile platform solution
- Core operating frequencies up to 1000 MHz
- Integrated 64 KByte L1 instruction and data caches, and 256 KByte (TM5700) or 512 KByte (TM5900) L2 write-back cache
- Integrated northbridge core logic features facilitate compact system designs
  - DDR SDRAM memory controller with 83-133 MHz, 2.5 V interface
  - PCI bus controller (PCI 2.1 compliant) with 33 MHz, 3.3 V interface
- LongRun™ advanced power management with ultra-low power operation extends battery life
  - < 1 W running typical multimedia applications
  - < 150 mW typical in Deep Sleep
- LongRun™ thermal management (CoolRun) dynamically adapts to system thermal environment
- Power management controls for ACPI-compliant modes
- Full System Management Mode (SMM) support
- Compact (21 mm x 21 mm) 399-contact flip-chip organic ball-grid array (FC-OBGA) package

The processor core operates from a 0.80-1.40 V supply, resulting in extremely low power consumption even at high operating frequencies. The processor typically consumes below 1 Watt under normal operating conditions. When operating in Deep Sleep, power consumption typically drops below 150 mW.

Architectural Overview

The Transmeta Crusoe processor model TM5700/TM5900 is an ultra-low power, high-speed microprocessor based on an advanced VLIW core architecture. When used in conjunction with Transmeta's x86 Code Morphing software, the TM5700/TM5900 processor provides x86-compatible software execution using dynamic binary code translation, without requiring code recompilation. In addition to the VLIW core, the processor incorporates separate 64 KByte L1 instruction and data caches, a large L2 write-back cache (256 KBytes on TM5700, 512 KBytes on TM5900), a 64-bit DDR SDRAM memory controller, and a 32-bit PCI controller. These additional functional units, which are typically part of the chipset system logic that surrounds the microprocessor, allow the TM5700/TM5900 processor to provide a highly-integrated, cost-effective solution for x86 platforms requiring superior energy efficiency, low power consumption, and low thermal generation. Figure 1 shows a block diagram of the Crusoe TM5700/TM5900 processor.

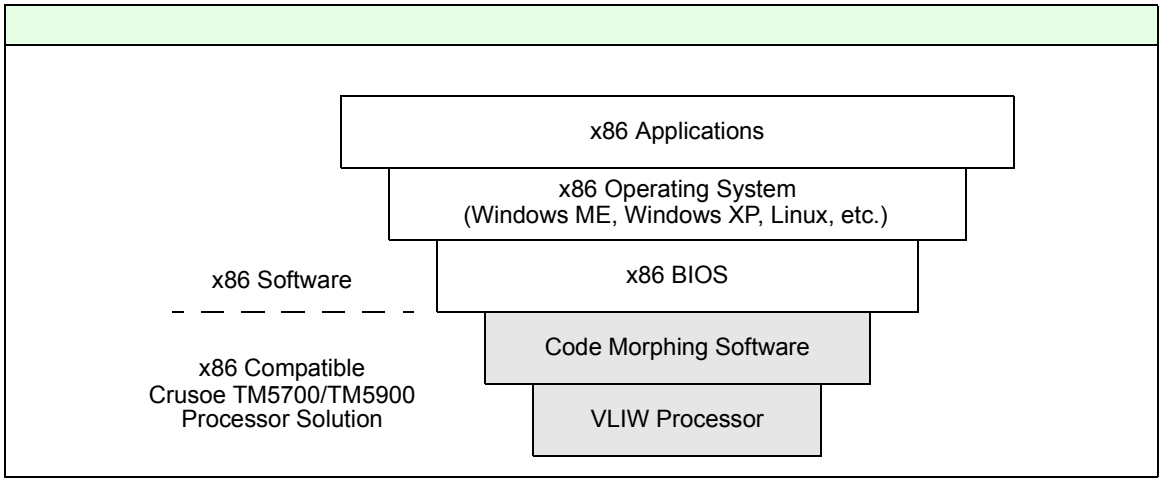
Figure 1: Crusoe TM5700/TM5900 Processor Block Diagram



The TM5700/TM5900 processor core is based on a Very Long Instruction Word (VLIW) instruction set of 64 or 128 bits. Within this VLIW architecture, the control logic of the processor is kept very simple, and software is used to control the scheduling of instructions. This allows a simplified and very straightforward hardware implementation with an in-order 7-stage integer pipeline and a 10-stage floating point pipeline. By streamlining the processor hardware and reducing control logic transistor count, the performance-to-power consumption ratio (energy efficiency) can be greatly improved over traditional x86 architectures.

In addition to having the execution hardware for logical, arithmetic, shift, and floating point instructions, as in conventional processors, the TM5700/TM5900 processor uses a combination of software and hardware to offer full x86 compatibility. The processor hardware generates the same condition codes as conventional x86 processors and operates on the same 80-bit floating point numbers. Also, the translation look-aside buffer (TLB) has the same protection bits and address mapping as x86 processors. The software component of this processor solution is used to emulate all other features of the x86 architecture. The software that converts x86 programs into the core VLIW instructions is called Code Morphing software. The combination of Code Morphing software and the VLIW core together act as an x86-compatible processor solution, as shown in Figure 2.

Figure 2: Crusoe TM5700/TM5900 Processor Software Hierarchy



The typical behavior of Code Morphing software is to execute a loop, which decodes and executes x86 instructions. The first few times a specific x86 code sequence is executed, Code Morphing software interprets the code by decoding the instructions one at a time and then dispatching execution to corresponding VLIW native instruction subroutines. Once the x86 code has been executed several times, Code Morphing software translates the x86 instructions into highly optimized and extremely fast native VLIW instructions, executes the translated code, and caches the native instruction translations for future use. If the same x86 code is required to execute again, the high-performance cached translations are executed immediately and no re-translation is required.

Reference Documents

The following documents should be used in conjunction with this specification:

- *TM5700/TM5900 System Design Guide*
- *TM5700/TM5900 Development and Manufacturing Guide*
- *TM5700/TM5900 BSDL Test File*
- *TM5700/TM5900 IBIS Models*
- *TM5x00/Code Morphing Software Version 4.5 BIOS Programmer's Guide*
- *TM5700/TM5900/Code Morphing Software Version 4.5 Release Notes*
- *TM5700/TM5900/Code Morphing Software Version 4.5 Errata*
- *Transmeta Processor Thermal Design Guide*
- *PCI Local Bus Specification*

Chapter 1

Functional Interface Description

1.1 Power and Thermal Management

1.1.1 Power Management States

TM5700/TM5900 processors, in conjunction with Code Morphing software, support ACPI-compliant power management modes. Table 1 lists the state of the TM5700/TM5900 processor for each of the ACPI global system states. The power management states listed in Table 1 are defined in greater detail in Table 2 and the following paragraphs. TM5700/TM5900 processor power management states and state transitions are shown in Figure 3.

Table 1: System Power Management States

ACPI System State		Processor State	SDRAM	Clock Generator	Delay to Return to C0 State [1]
G0 / S0 / C0	Working	Normal	Normal	Running	-
G0 / S0 / C1	Auto Halt	Auto Halt	Normal	Running	< 260 nS
G0 / S0 / C2	Quick Start	Quick Start	Self-refresh	Running	< 2.8 µS
G0 / S0 / C3	Deep Sleep	Deep Sleep	Self-refresh	CLKIN stopped	< 20 µS
		DSX			< 25 µS
G1 / S1	Sleeping	Deep Sleep	Self-refresh	PLL shut down	< 20 µS
		DSX			< 25 µS
G1 / S3	Suspend-to-RAM	Off	Self-refresh	PLL shut down	10 mS + BIOS
G1 / S4	Suspend-to-Disk	Off	Off	Off	< 30 S
G2 / S5	Soft Off	Off	Off	Off	-
G3	Mechanical Off	Off	Off	Off	-

1. Delay times specified may vary depending on core operating frequency, memory type and speed, and system device response times.

Table 2: Processor Power Management States

Processor		SDRAM	PCI Controller	Entry Trigger	Snoops	Interrupts
State	Core					
Normal	Running	Running	Running	Normal operation	Serviced	Serviced
Auto Halt	Stopped	Running	Running	Executing a HLT instruction	Serviced	Serviced
Quick Start	Stopped	Self refresh	Running	Asserting STPCLK#	Serviced	Latched
Deep Sleep	Stopped	Self refresh	Stopped	Asserting SLEEP# and stopping CLKIN while in Quick Start state	Not allowed	Not allowed
DSX	Stopped	Self refresh	Stopped	Reduce CVDD while in Deep Sleep	Not allowed	Not allowed

Auto Halt

The Auto Halt state is a low-power mode entered through the execution of the HLT instruction. The Auto Halt state is exited upon an interrupt (INTR, INIT#, SMI# or NMI) or assertion of RESET#. Snoops are serviced while in the Auto Halt state.

Quick Start

The Quick Start state is entered with the assertion of the STPCLK# input signal. While in Quick Start, snoops are serviced and interrupts are latched. Latched interrupts are serviced once the processor returns to the Normal state. Only one occurrence of an interrupt is latched while in Quick Start. If RESET# is asserted while in Quick Start, processor initialization occurs and then the processor returns to the Quick Start state if STPCLK# is still asserted.

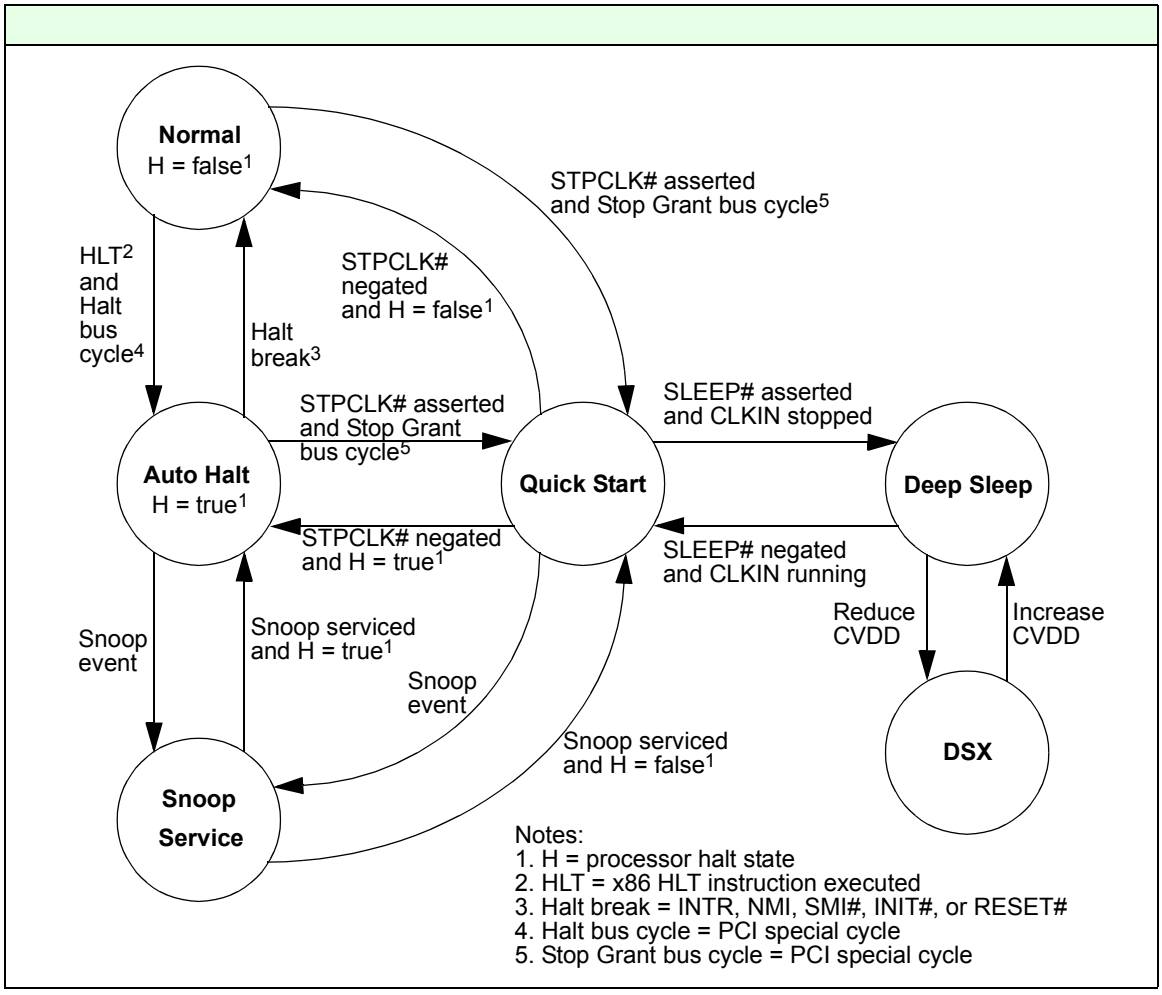
Deep Sleep

The Deep Sleep state is a very low power state that the processor can enter while still maintaining its context. After entering the Quick Start state, the processor enters Deep Sleep when SLEEP# is asserted and the master clock input (CLKIN) is stopped. The PCI clock input (P_PCLK) may also be stopped. The processor internal PLL is shutdown while in Deep Sleep. Therefore, when the clocks are restarted to exit Deep Sleep, the system must allow time for PLL resynchronization. Snoops are not serviced and interrupts are neither serviced nor latched while in Deep Sleep. RESET# is ignored while in Deep Sleep.

Deep Sleep Extended (DSX)

DSX is the lowest power state the processor can enter while still maintaining context. DSX is an extended Deep Sleep state with the processor core voltage (CVDD) reduced to a minimal sustaining level.

Figure 3: Power Management State Diagram

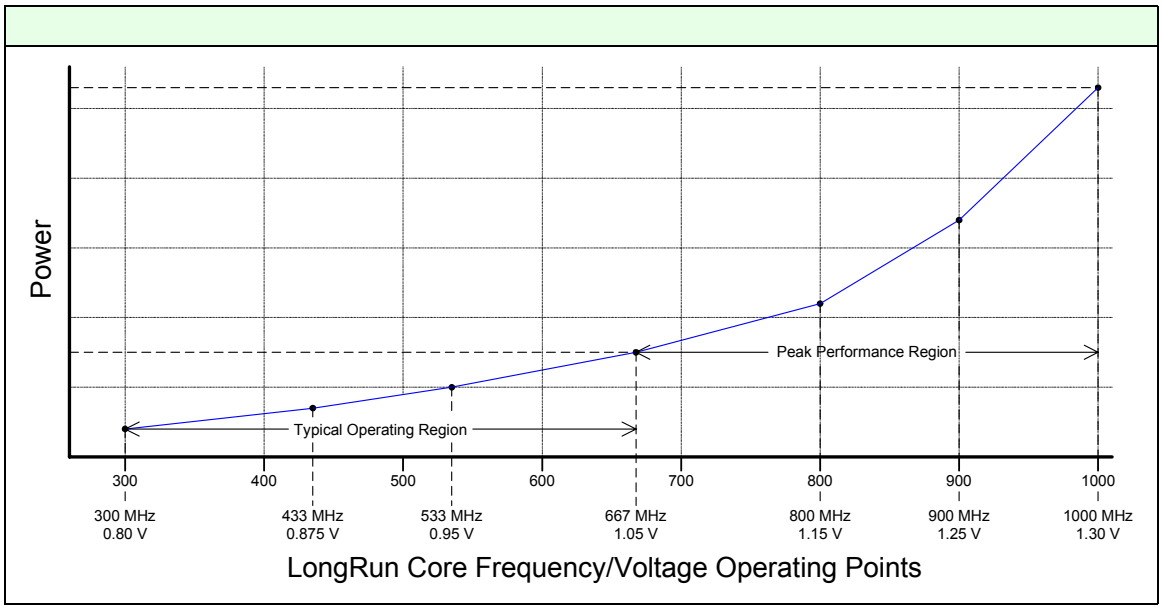


1.1.2 LongRun Power Management

LongRun power management technology provides Code Morphing software with the ability to adjust the TM5700/TM5900 processor core operating voltage and clock frequency dynamically, depending on the demands placed on the processor by software. Because power varies linearly with clock speed and by the square of voltage, adjusting both processor voltage and clock frequency can produce cubic reductions in power consumption, whereas conventional processors can adjust power linearly only by adjusting the effective operating frequency.

The LongRun policies are implemented within the Code Morphing software and can detect different workload scenarios based on runtime performance information, and then exploit these by adapting processor power usage accordingly. This ensures the processor delivers high performance when necessary and conserves power when demand on the processor is low. All power adjustments are transparent to the operating system, power management controller, and the user. LongRun power management uses a number of core frequency/voltage operating points, allowing TM5700/TM5900 processors to optimize for the lowest power and maximum performance along this curve, as shown in the figure below.

Figure 4: LongRun Power Management Operating Points



Most conventional x86 processors utilize ACPI policies to regulate their power consumption, the processor rapidly alternating between running at full-speed and being effectively turned off (called clock-throttling). This approach can potentially disable the processor just when a critical application needs it. In contrast, LongRun power management dynamically picks just the right clock speed and operating voltage needed to run the application, thereby allowing maximum energy efficiency. LongRun power management works in conjunction with ACPI. When the processor frequency and voltage scaling reaches the minimum LongRun power management setpoint, the processor transparently switches over to traditional power models, allowing policies such as ACPI to handle power management at very low power operating points.

During LongRun power management operation, the processor memory interface frequencies are also changed dynamically to keep the memory interfaces synchronized with the core frequency. LongRun power management core frequency, core voltage, and memory interface frequency configurations are provided in Table 3. Information on LongRun power management configuration is provided in *TM5700/TM5900 Development and Manufacturing Guide*.

Table 3: LongRun Power Management Specifications

Processor				Memory Interface	
	Core			DDR-266	DDR-200
SKU	MHz	V	T_j max	MHz	MHz
TM5900-1000-6.5 CoolRun80	1000	1.250	80 °C	125	100
	900	1.200	100 °C	129	100
	800	1.100		133	100
	667	1.000		133	95
	567	0.900		113	94
	433	0.800		108	87
TM5900-1000-7.5 CoolRun80	1000	1.300	80 °C	125	100
	900	1.250	100 °C	129	100
	800	1.150		133	100
	667	1.050		133	95
	533	0.950		133	89
	433	0.875		108	87
	300	0.800		100	100
TM5900-1000-8.5 CoolRun80	1000	1.350	80 °C	125	100
	900	1.300	100 °C	129	100
	800	1.200		133	100
	667	1.100		133	95
	533	1.000		133	89
	433	0.925		108	87
	300	0.800		100	100
TM5900-1000-9.5 CoolRun80	1000	1.400	80 °C	125	100
	900	1.350	100 °C	129	100
	800	1.250		133	100
	667	1.150		133	95
	533	1.050		133	89
	433	0.950		108	87
	300	0.800		100	100
TM5900-933-8.5 CoolRun80	933	1.350	80 °C	133	93
	800	1.250	100 °C	133	100
	667	1.150		133	95
	533	1.050		133	89
	433	0.950		108	87
	300	0.800		100	100
TM5900-800-6.6 CoolRun80	800	1.250	80 °C	133	100
	667	1.150	100 °C	133	95
	533	1.050		133	89
	433	0.950		108	87
	300	0.800		100	100

Table 3: LongRun Power Management Specifications (Continued)

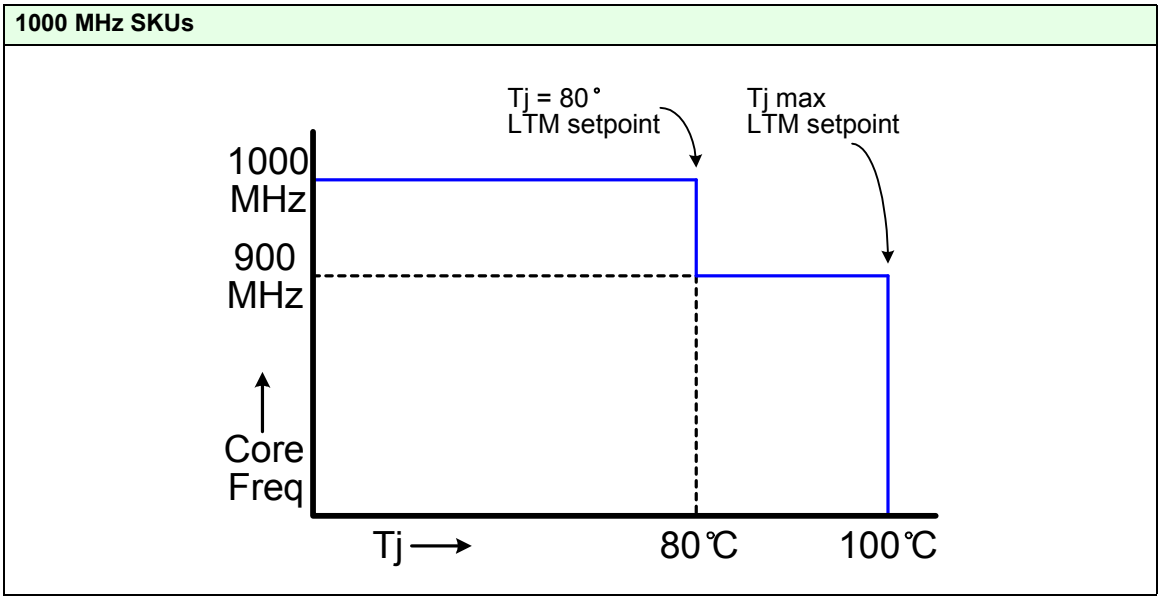
Processor				Memory Interface	
	Core			DDR-266	DDR-200
SKU	MHz	V	T_j max	MHz	MHz
TM5700-667-5.0 CoolRun80	667	1.150	80 °C	133	95
	533	1.050	100 °C	133	89
	433	0.950		108	87
	300	0.800		100	100

1.1.3 LongRun Thermal Management

Thermal management of TM5700/TM5900 processors is integrated into the LongRun power management frequency/voltage ramp policies. The LongRun thermal management policy manages the TM5700/TM5900 processor thermal environment by using frequency/voltage shifts as a substitute for thermal throttling. In contrast to conventional thermal management techniques, LongRun thermal management delivers higher performance at the same die temperature, or the same performance at a lower die temperature. LongRun thermal management essentially expands the thermal budget of the processor. LongRun thermal management maximizes system performance and maintains safe processor operating temperatures within constrained thermal environments.

LongRun thermal management must be implemented for all TM5700/TM5900 CoolRun80 processor-based system designs. LongRun thermal management is recommended for all TM5700/TM5900 (non-CoolRun80) processor-based systems. Implementation details for LongRun thermal management are described in the TM5500/TM5800 technical bulletin *LongRun Thermal Management Implementation Guide*. The figure below shows LongRun thermal management operating points for 1000 MHz TM5700/TM5900 CoolRun80 processors. The operating curves for other SKUs is similar, with the processor operating at the top LongRun frequency until the processor junction temperature reaches 80 °C, after which the operating frequency drops to the second and lower LongRun points with junction temperatures above 80 °C.

Figure 5: LongRun Thermal Management (LTM) Operating Curves



1.1.4 Processor Thermal Monitoring

TM5700/TM5900 processors provide an integrated on-die thermal diode. This 2-terminal (DIODE_ANODE, DIODE_CATHODE) thermal diode can be connected to an external temperature sensor and the processor junction temperature monitored by system BIOS and application software.

Thermal Diode Accuracy

The TM5700/TM5900 processor on-die thermal diode, when used in conjunction with a Maxim MAX1617MEE (standard part) temperature sensor, will provide a temperature accuracy of ± 3°C from 0 to 100°C.

1.1.5 DDR SDRAM Power Saving Modes

In addition to the power management states defined in previous sections, TM5700/TM5900 processors provide additional power saving modes for DDR SDRAM. These power saving modes can be enabled during normal operation by programming processor-specific PSR configuration registers (CD_MISC). In these power saving modes, the clock enable lines to the SDRAM are active only when the SDRAM is being accessed or refreshed. This decreases power dissipation, but increases the latency for a memory cycle by one SDRAM clock. Refer to the *TM5700/TM5900 BIOS Programmer's Guide* and the *TM5700/TM5900 Development and Manufacturing Guide* for power saving mode programming information.

1.2 DDR Memory Interface

TM5700/TM5900 processors include an integrated high performance DDR (double data-rate) SDRAM controller and interface. The DDR controller supports only DDR SDRAM and transfers data at a rate that is twice the clock frequency of the interface. The DDR SDRAM controller supports the equivalent of two DIMMs (up to four ranks) of DDR SDRAM using a 64-bit wide interface. The DDR SDRAM interface does not support parity bits.

Systems based on TM5700/TM5900 processors require careful consideration of the memory subsystem design. There are unique characteristics of the TM5700/TM5900 memory controller that place specific constraints on the allowable system memory configurations, as described in the sections below. The design guidelines provided below allow system designs that provide robust memory configurations that support a variety of memory upgrade scenarios.

Ranks Not Banks - A Note on Terminology
Memory chip vendors and system designers have historically used slightly different terminology to describe memory configurations. To avoid confusion, this document uses the terminology employed by memory chip vendors in describing memory configurations. For example, the grouping of sections of memory on system boards, commonly referred to by designers as ‘sides’ or ‘banks’, will be referred to by the proper name of ‘rank’, as this is the term recognized by the memory industry. A rank describes the memory chips connected to a common ‘chip select’ signal. Use of term ‘bank’ to describe memory organization can be confusing because modern memory chips use ‘bank’ select signals in addition to row and column address signals. It is important not to confuse single- and dual-rank memory with single- and dual-sided memory, since the physical location of memory chips on memory modules is not a reliable indicator of the actual memory configuration on the module. For example, it is possible for single-rank memory modules to contain memory chips on both sides of the module.

1.2.1 Supported Memory Types

TM5700/TM5900 processors support only non-buffered/non-registered/non-ECC DDR SDRAM memory. SDR (single data rate) SDRAM memory, buffered/registered memory, and ECC memory are not supported.

TM5700/TM5900 memory subsystems can be populated with 64-Mbit (4M x 16 or 8M x 8), 128-Mbit (8M x 16 or 16M x 8), 256-Mbit (16M x 16 or 32M x 8), or 512-Mbit (32M x 16 or 64M x 8) devices. Note that only x8 and x16 memory devices are supported.

1.2.2 Memory Speed (Frequency)

For memory configurations with up to 8 loads per interface signal, TM5700/TM5900 processors support DDR interface frequencies up to 133 MHz (DDR-266). With memory configurations having more than 8 loads per signal, the DDR interface frequency must be reduced below 133 MHz. The amount of reduction depends on the actual interface signal loading, layout and routing, PCB quality, etc. For the highest performance, it is recommended that the DDR memory devices be soldered down to the circuit board, rather than incorporated on DIMMs. Careful memory subsystem designs using SODIMMs can be nearly as good as soldered-down memory designs.

The frequency setting for the DDR memory interface is initialized during the processor boot sequence from data stored in the configuration ROM. Although the processor can be configured for a DDR interface frequency in the range of 1/2 to 1/15 of the core frequency, the supported interface frequency is restricted to a minimum of 83 MHz and a maximum of 133 MHz. DDR frequency settings vary at each LongRun power

management step. DDR interface frequencies at various LongRun power management steps are shown in Table 3.

With LongRun power management enabled, the processor core frequency is lowered during times when peak performance is not required. When the core frequency changes, the DDR interface frequency is recalculated to match the new core frequency setting. For example, a 1000 MHz device with a 125 MHz memory interface may have a LongRun setting of 667 MHz with a 133 MHz memory interface. Therefore, systems that use LongRun power management must support the entire DDR SDRAM interface frequency range of 83 MHz to 133 MHz.

1.2.3 Memory Interface Constraints

TM5700/TM5900 processors have a quad-rank memory controller implementation. In a quad-rank memory controller, only one register is available to describe and store all of the parameters of the memory types used in the system. This implies that each individual rank of memory must be identical. Also, in this memory controller implementation, memory is assumed to be contiguous, so sequential placement of memory in each rank is required.

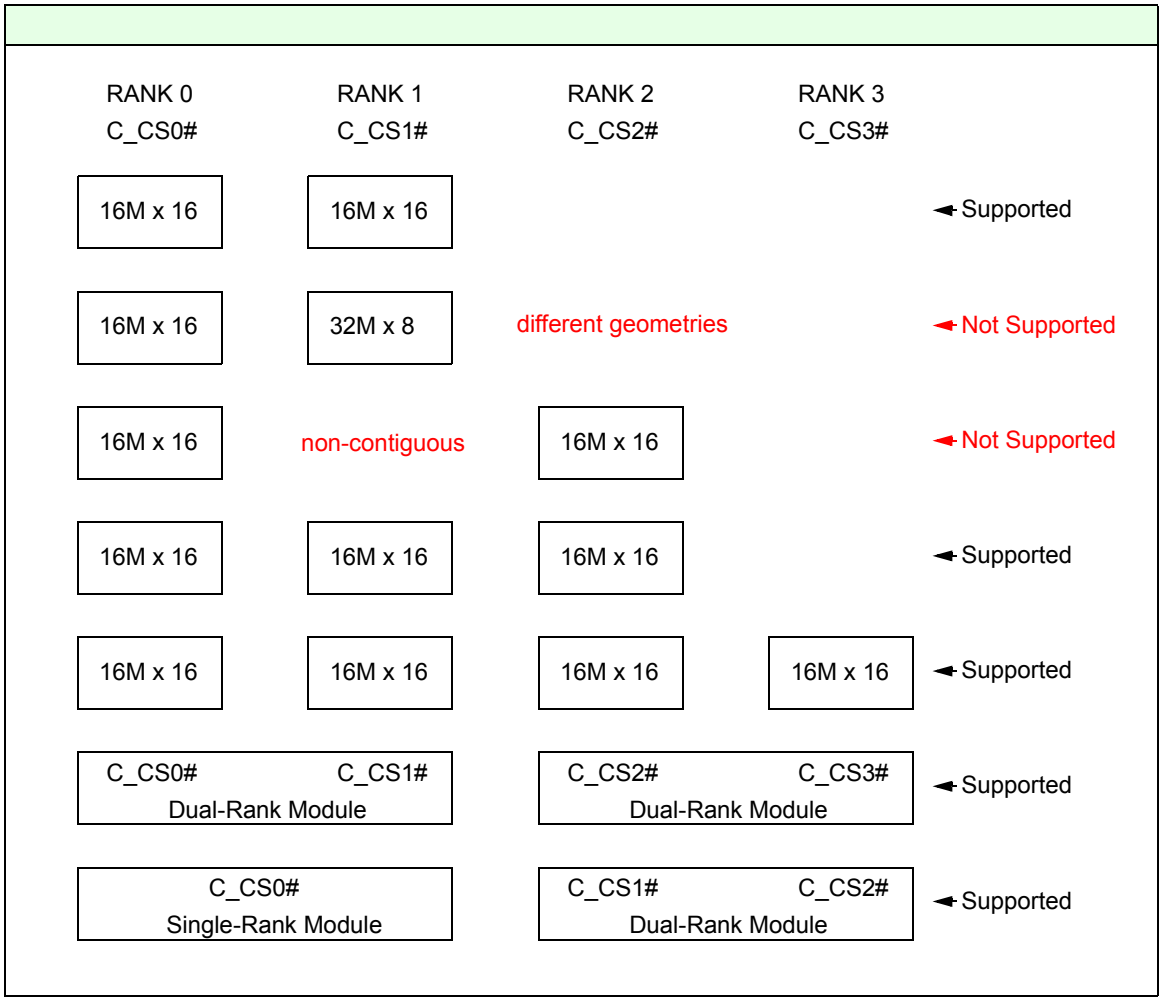
By taking into consideration the memory subsystem constraints described below for TM5700/TM5900 processor-based systems, and following a few simple guidelines, designers can be assured of reliable high-performance memory operation, and system memory upgrades can be supported in a straightforward manner.

- Memory must be placed in ranks in equal capacities (sizes).
- Memory must be of the same density and organization (geometry).
- Memory must be populated sequentially and contiguously so that a rank is not skipped and left open.
- All memory devices must be the same speed. The memory interface operating frequency must be set for the lowest speed memory in the system.
- The DDR interface cannot drive more than eight unbuffered loads (devices) at the maximum interface frequency of 133 MHz. For memory configurations that exceed eight loads, the interface must be reduced from 133 MHz.
- Placing the DDR devices down on the motherboard is recommended for best high-speed signal integrity. Follow the DDR interface layout and routing guidelines in the *TM5700/TM5900 System Design Guide*.
- See Table 4 for allowable and recommended DDR memory configurations. Choose configurations that minimize the number of loads. Use the largest capacity devices possible for a given total memory size.

1.2.4 Memory Rank and Chip Select Examples

As described previously, a rank describes the memory chips connected to a common chip select signal. Once populated, each of the four memory ranks is controlled through one of the four DDR interface chip select signals (C_CS0#, C_CS1#, C_CS2#, C_CS3#). These chip selects are used by the memory controller to manage accesses between the connected memories. Typically, memory controllers support distinct dual-rank DIMMs, but for the quad rank controller implemented in TM5700/TM5900 processors, system memory must be configured in a specific way, as shown in Figure 6 below.

Figure 6: Memory Rank and Chip Select Examples



If different sizes and geometries of memory are paired up, the organization of the memory addressing will become incompatible and the system will become non-functional. If identical memory of the same size and geometry is populated on a system board so that a rank is skipped, such as placing memory in Rank 0 and Rank 2 and not in Rank 1, only the memory located in the first rank will be recognized and available to the system, while the second rank of memory will not be recognized.

The same memory interface constraints previously described apply for memory modules (e.g. SODIMMs) as well as soldered down memory. Assuring the memory constraints are not violated when using expansion memory on modules requires careful selection and review of the memory module specifications. Memory modules are typically manufactured as single-rank or dual-rank. Determining the difference between the two types typically requires the memory module manufacturer's specification sheet, due to the number of different chip types and configurations available.

1.2.5 Supported Memory Configurations

Table 4 below shows allowable memory configurations for TM5700/TM5900 processors, with recommended configurations **highlighted**. Note that only configurations with contiguous memory ranks populated, using identical geometries for each rank, are supported. Also note that all installed memory will operate at the same interface frequency, and will be limited to the maximum frequency of the slowest installed memory devices. Board layout and signal loading may limit memory frequency to below 133 MHz, as described previously.

Table 4: DDR SDRAM Memory Configurations

Device Density (Mbits)	Device Organization (Geometry)	Rank 0 C_CS0#	Rank 1 C_CS1#	Rank 2 C_CS2#	Rank 3 C_CS3#	Loads	Total Memory (MBytes)	Maximum Interface Frequency (MHz)
64	4M x 16	X				4	32	133
		X	X			8	64	133
		X	X	X		12	96	< 133
		X	X	X	X	16	128	< 133
	8M x 8	X				8	64	133
		X	X			16	128	< 133
128	8M x 16	X				4	64	133
		X	X			8	128	133
		X	X	X		12	192	< 133
		X	X	X	X	16	256	< 133
	16M x 8	X				8	128	133
		X	X			16	256	< 133
256	16M x 16	**X**				**4**	**128**	**133**
		X	**X**			**8**	**256**	**133**
		X	X	X		12	384	< 133
		X	X	X	X	16	512	< 133
	32M x 8	X				8	256	133
		X	X			16	512	< 133
512	32M x 16	**X**				**4**	**256**	**133**
		X	**X**			**8**	**512**	**133**
		X	X	X		12	768	< 133
		X	X	X	X	16	1024	< 133
	64M x 8	X				8	512	133
		X	X			16	1024	< 133

1.2.6 Example Memory Configurations

Notebook PC

The memory requirements of the latest industry standard operating systems, in combination with the widespread availability of low-cost DDR memory, has resulted in base system memory configurations of 128-256 MBytes for notebook PCs. Additional memory expansion slots are usually provided for user-installed expansion memory. A typical TM5700/TM5900 processor-based notebook memory sub-system design configuration would be:

- Four 133 MHz (DDR-266) 256 Mbit (16M x 16) DDR SDRAM devices soldered down to the system motherboard, providing 128 MBytes of high-performance base system memory. This rank of memory should be connected to C_CS0#.
- Two single-rank DDR memory expansion µDIMM sockets. The first and second of these µDIMM sockets must be connected to C_CS1# and C_CS2# respectively. These can be populated with two 128 MByte single-rank µDIMM memory modules (must use 16M x16 devices on modules), allowing incremental memory expansion of 128 or 256 MBytes. This allows the base 128 MBytes of memory to be incrementally expanded to 256 or 384 Mbytes. Note that when both memory expansion modules are installed, the memory will operate at less than 133 MHz.

Embedded Controller

Embedded controller memory requirements typically favor small memory configurations. An example embedded controller memory sub-system design configuration would be:

- Four 133 MHz (DDR-266) 256 Mbit (16M x 16) DDR SDRAM devices soldered down to the system motherboard, providing 128 MBytes of high-performance system memory. This rank of memory should be connected to C_CS0#.

1.2.7 Code Morphing Software Memory

Code Morphing software uses a portion (typically 16-24 MBytes) of the installed system memory for its working area and to store code translations. This portion of memory is completely isolated from the operating system-accessible (x86) memory area.

Code Morphing software memory is statically configured in the OEM configuration table. See the *TM5700/TM5900 Development and Manufacturing Guide* for detailed information on Code Morphing software memory configuration.

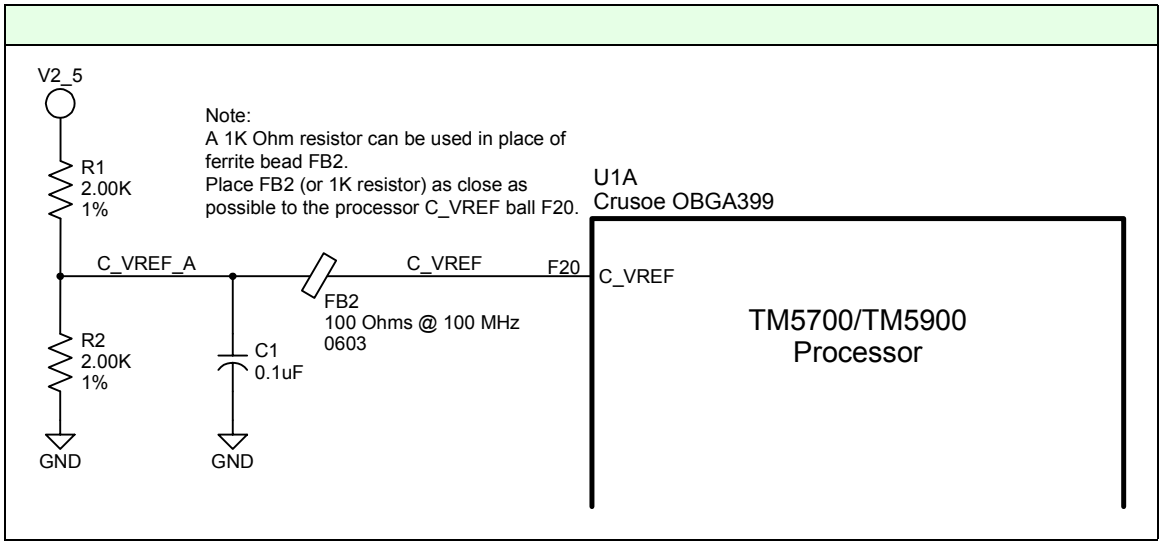
1.2.8 SPD ROM Devices

If system memory expansion modules (e.g. SODIMMS) are required for the system design, SPD (serial presence detect) ROM devices must be connected to the system southbridge SM (system management) bus. This is required so the BIOS code can read the SPD ROM data to correctly determine the system memory configuration (speed, size, geometry), and for Code Morphing software to calculate the number of device loads and select an appropriate memory frequency.

1.2.9 DDR Interface Reference Voltage Circuit

TM5700/TM5900 processors require a ferrite bead (or 1K resistor) noise filter on the C_VREF DDR interface reference voltage signal. C_VREF is derived from IOVDD25 (2.5 V I/O power supply) using a resistive voltage divider. The recommended noise filter circuit is shown below.

Figure 7: Recommended C_VREF Circuit with Noise Filter



1.3 PCI Interface

The TM5700/TM5900 processor PCI bus is revision 2.1 compliant. The PCI bus is 32 bits wide, operates at 33 MHz and is compatible with 3.3 V levels (but is not 5 V tolerant). The PCI controller on the TM5700/TM5900 provides a PCI host bridge, the central resource and a DMA controller.

The TM5700/TM5900 PCI bus can sustain 132 Mbytes/sec bursts for reads and writes on 4 KByte blocks. The PCI controller snoops ahead on PCI-to-DRAM reads and writes. The 16 DWORD processor-to-PCI write buffer converts sequential memory mapped I/O writes to PCI bursts. The DMA controller handles PCI-to-DRAM reads and writes. The 16 DWORD PCI-to-DRAM write buffer converts one 16 DWORD burst to eight separate address/data pairs. The 16 DWORD DRAM-to-PCI read ahead buffer permits continuation of read ahead after hitting in the buffer. The PCI controller tri-states the PCI bus when hot docking.

1.3.1 PCI Bus Commands

The TM5700/TM5900 PCI controller, in conjunction with the Code Morphing software, supports the PCI bus commands listed in Table 5. If the processor generates a shutdown, halt or stop grant condition, a PCI special cycle is generated. The shutdown cycle is propagated with 0000h in the message field, the halt cycle is propagated with 0001h in the message field, and the stop grant cycle is propagated with 0002h in the message field and 0012h in the message dependent data field.

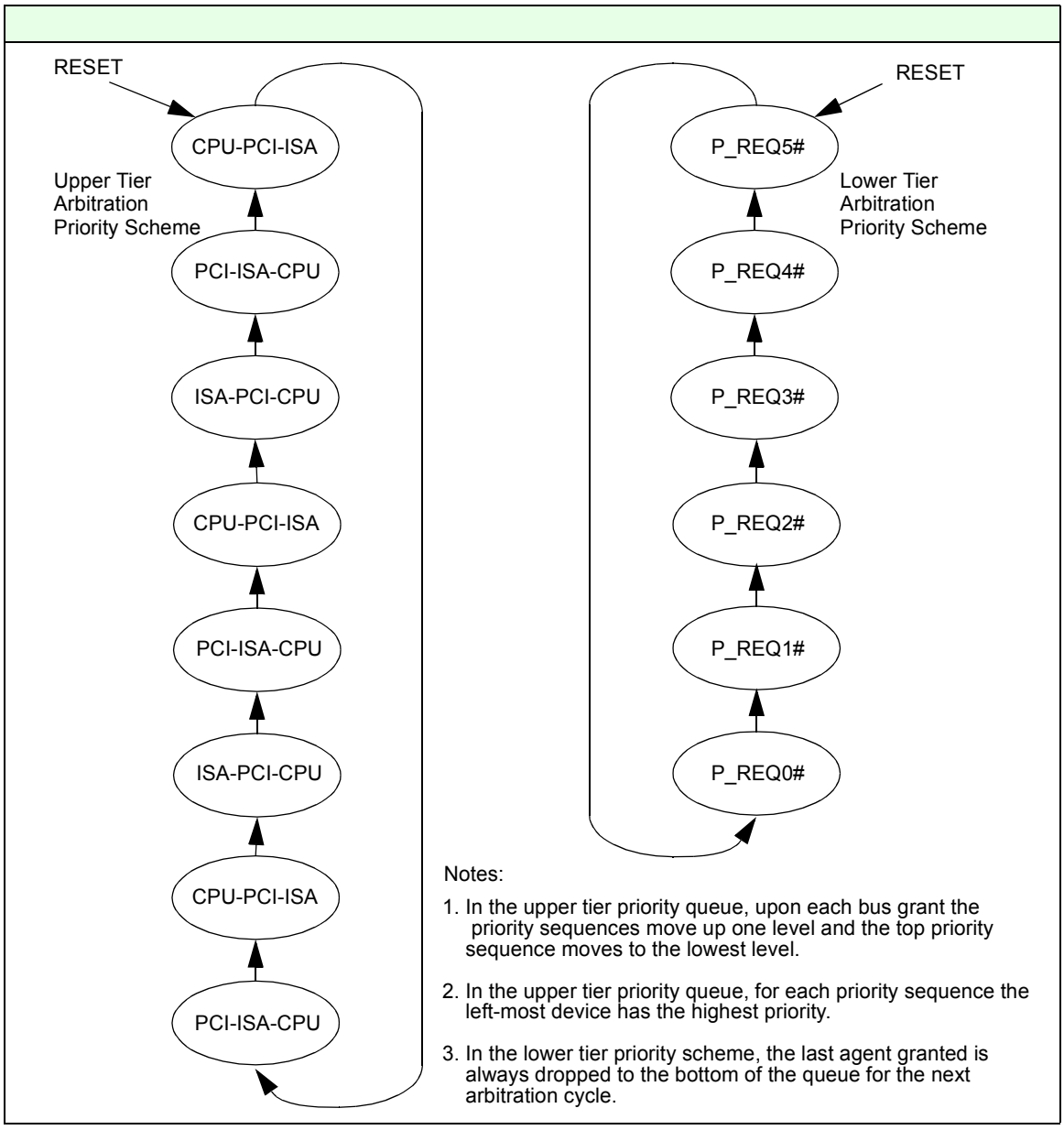
Table 5: PCI Bus Commands Supported

Command Encoding (P_CBE#)	Command Type	Initiator Support	Target Support
0000	Interrupt Acknowledge	Yes	No
0001	Special Cycle	Yes	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0100	-	-	-
0101	-	-	-
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	-	-	-
1001	-	-	-
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	No	As a memory read
1101	Dual Address Cycle	No	No
1110	Memory Read Line	No	As a memory read
1111	Memory Write and Invalidate	No	As a memory write

1.3.2 Bus Arbitration

The PCI controller central resource includes an integrated arbiter which supports up to seven PCI masters, including a PCI-to-ISA bridge. The arbiter, in conjunction with Code Morphing software, implements a two-tier rotating priority-based scheme. The upper tier arbitrates among the three bus master categories of processor (CPU), PCI devices, and PCI-to-ISA bridge. The lower tier arbitrates among the requesting PCI devices. The arbitration priority scheme is shown in Figure 8.

Figure 8: PCI Arbitration Priority Scheme



When the PCI bus becomes idle, the arbiter “parks” the PCI bus on the processor. If the bus is parked and the processor and one or more other bus masters request the bus simultaneously, the processor is granted the bus regardless of the state of the upper tier priority queue.

P_REQ[5:0]# and P_GNT[5:0]# are the arbitration handshake signals used by PCI masters other than the PCI-to-ISA bridge. The PCI-to-ISA bridge uses the P_HOLD# and P_HLDA# signals.

1.4 Southbridge Sideband Signals

TM5700/TM5900 processors provide a variety of southbridge sideband signals: INIT#, RESET#, INTR, NMI, SMI#, FERR#, IGNNE#, STPCLK#, and SLEEP#. These signals are driven/monitored by a system southbridge device on the base platform and are used to guarantee PC-compatible functionality for resets, interrupts, floating point errors, processor clock control, and power management.

1.5 Serial Interfaces

TM5700/TM5900 processors incorporate three separate serial interfaces:

Debug Serial Interface

The two-signal (S_SCLK, S_SDATA) debug interface can be used for debug purposes. Note that the serial debug interface is NOT an I2C or SMBus interface.

Configuration (Mode-Bit) ROM Serial Interface

The two-signal (CFG_SCLK, CFG_SDATA) configuration ROM interface is used to read data from a required serial ROM device. The serial configuration ROM contains hardware data that is used to initialize TM5700/TM5900 processors at power-up, and must be provided in the system design. The contents of the configuration ROM determines the settings for the processor and the SDRAM clocks, and the memory and PCI interface timing parameters. Once the PCI and SDRAM interfaces have been initialized, the configuration ROM controls the transfer of the Code Morphing software from the Code Morphing software flash memory to the SDRAM. Control is then transferred to the Code Morphing software and the configuration ROM is disabled. Programming information for the configuration ROM is available from Transmeta. The recommended ROM device is the 93LC56B-I/SN from Microchip Technology, Inc.

Code Morphing Software Boot ROM Serial Interface

The 5-signal (SROM_CS0#, SROM_CS1#, SROM_SCLK, SROM_SIN, SROM_SOUT) Code Morphing software boot ROM interface is used to read data from an optional serial flash ROM. This interface may also be used for in-system reprogramming. When used, the serial flash ROM device stores the Code Morphing software. During the boot process, the Code Morphing software is copied from the flash memory to the SDRAM. The Code Morphing software boot ROM interface supports up to 1 MByte of total storage using either two 512 KByte devices or a single 1 MByte device. Programming information for the Code Morphing software boot ROM is available from Transmeta.

1.6 Clocks

The TM5700/TM5900 processor input clock (CLKIN) is multiplied by the processor clock multiplier to generate the processor core clock. For currently defined TM5700/TM5900 SKUs, CLKIN is assumed to be 66.6 MHz. The CLKIN multipliers used for each available SKU and LongRun power management core clock frequency are provided in Table 6.

The processor core clock is divided down by the DDR clock divider to generate the DDR SDRAM interface clocks. See DDR Memory Interface on page 20 for additional information on DDR frequency settings.

There is also a clock divider that must be initialized for the PCI interface. The PCI interface operates at 33.3 MHz. The processor core frequency divisors used to generate the 33.3 MHz PCI interface clock are shown in Table 6. The clock multiplier and divider values are programmed into the TM5700/TM5900 processor during initialization from data stored in the configuration ROM.

Table 6: Core Clock Multipliers and PCI Interface Divisors

Processor		66.6 MHz CLKIN Multiplier	33.3 MHz PCI Interface Divisor
SKU	Core Freq (MHz)		
TM5900-1000-6.5	1000	15	30
	900	13.5	27
	800	12	24
	667	10	20
	567	8.5	17
	433	6.5	13
TM5900-1000-7.5 TM5900-1000-8.5 TM5900-1000-9.5	1000	15	30
	900	13.5	27
	800	12	24
	667	10	20
	533	8	16
	433	6.5	13
	300	4.5	9
TM5900-933-8.5	933	14	28
	800	12	24
	667	10	20
	533	8	16
	433	6.5	13
	300	4.5	9
TM5900-800-6.6	800	12	24
	667	10	20
	533	8	16
	433	6.5	13
	300	4.5	9
TM5700-667-5.0	667	10	20
	533	8	16
	433	6.5	13
	300	4.5	9

1.7 JTAG Test Interface

TM5700/TM5900 processors provide a 5-signal JTAG interface that can be used for processor testing. This interface supports IEEE 1149.1, EXTEST, SAMPLE/PRELOAD, BYPASS, and HiZ instructions. The JTAG interface operates up to 50 MHz.

1.8 Supply Voltages

TM5700/TM5900 processors require four supply voltages. The core supply voltage (CVDD) varies from 0.80-1.40 V (nominal), depending on the SKU and the LongRun power management voltage setting. Two I/O supply voltages are required: IOVDD is 3.3 V (nominal), and IOVDD25 is 2.5 V (nominal). There is also a single supply connection for the PLL circuit, with a supply voltage (PLLVDD) that tracks the core supply voltage. See Recommended Operating Conditions on page 56 for detailed power supply specifications.

1.9 Core Voltage Regulator VRDA Interface

TM5700/TM5900 processors provide a 5-signal open-drain interface (VRDA[4:0]) that is used by Code Morphing software LongRun power management to control the output voltage (CVDD) of the processor core voltage regulator. The power-on default values for the VRDA signals are provided in Table 7.

Table 7: Power-On Default VRDA Output Values

VRDA Value						Low-Range Regulator [1] Output	High-Range Regulator Output
VRDA[4]	VRDA[3]	VRDA[2]	VRDA[1]	VRDA[0]	VRDA[4:0]		
0	1	1	1	0	0x0E	1.05 V	1.30 V

1. Low-range voltage regulators, such as the Maxim MAX1718, are recommended for the TM5700/TM5900 core regulator device. See *TM5700/TM5900 System Design Guide* for more information on core regulator circuit recommendations.

1.10 Power-On Sequence

The sequence of operations required to power-on TM5700/TM5900 processors is provided below.

1. **Apply power to the system.** Allow PLLVDD and CVDD to ramp up to their minimum operating levels. After CVDD reaches its minimum operating level, ramp up IOVDD and IOVDD25 to their respective minimum operating levels. The IOVDD and IOVDD25 supplies must not begin ramping up until CVDD has reached its minimum operating level or excessive surge currents can result on the I/O supply lines. See Power On Specifications on page 64 for additional information. RESET#, P_PCI_RST# and PWRGOOD should all be held low during this time. With PWRGOOD at a low level, the processor is in a self-protecting mode.

2. **Assert PWRGOOD.** Assert PWRGOOD after all power supplies reach their specified operating voltage levels following the required sequencing described in Power On Specifications on page 64.

3. **Begin toggling CLKIN.** At or before the assertion of PWRGOOD, begin toggling CLKIN.

4. **Deassert P_PCI_RST# and RESET#.** P_PCI_RST# must be held low until at least 1 ms after CLKIN begins to toggle. It also must be held low until at least 1 mS after the PWRGOOD rising edge.

5. **Processor mode bits are loaded from the configuration ROM.** Once P_PCI_RST# is deasserted, the processor begins reading data from the off-chip configuration ROM using the CFG_SCLK and CFG_SDATA signals. The frequency of CFG_SCLK is 920 KHz (CLKIN/72). The processor begins reading the configuration ROM by sending an eleven-bit sequence of 11000000000. This sequence tells the configuration ROM to begin supplying data starting at address 0. There is a 1 clock delay to allow the direction of the CFG_SDATA signal to change from driving to receiving. The processor then issues 112 CFG_SCLKs to read the contents of the configuration ROM. The entire sequence completes in approximately 130 µS.

6. **Complete internal reset sequence.** The processor internal reset sequence continues for approximately 800 ms plus an additional 64 internal clock cycles after the rising edge of RESET#. The processor then fetches its first instruction from either the serial boot ROM or from the PCI bus as determined by an internal mode bit.

Chapter 2

Signal Descriptions and Ballouts

This chapter contains signal descriptions, package footprint, and ballout assignments for TM5700/TM5900 processors.

2.1 Signal Descriptions

Table 8 provides a summary of the processor signals. Table 9 through Table 18 describe the function of each signal on the processor. Signals that are designated as **Reserved** may have internal electrical connections. Unless specified otherwise in Table 17, there should be no external electrical connection to the reserved signals.

Table 8: Signal Summary

Signal Group	Quantity
DDR SDRAM Interface	109
PCI Interface	62
Southbridge Sideband Interface	8
Serial Interfaces	9
Thermal/Power/System Management	14
JTAG Interface and Debug	7
Reserved and No Connection	23
Core Voltage Sniff	1
Power	80
Ground	86
TOTAL	399

Table 9: DDR SDRAM Interface Signals

Signal Name	Type	Qty	Description
C_A[12:0]	O	13	**Memory Address** These signals carry row and column addressing information.
C_BA[1:0]	O	2	**Bank Address** These signals carry the bank address for the DDR SDRAM devices.
C_CAS#	O	1	**Column Address Strobe** When asserted low, enables latching of the column address on the positive edge of the next clock.
C_CKE[1:0]	O	2	**Clock Enable** When deasserted, the DDR SDRAMs enter power down mode. C_CKE[1] and C_CKE[0] are identical, and are provided to support loading requirements; each drives one block.
C_CLKA, C_CLKA#, C_CLKB, C_CLKB#	O	4	**SDRAM Clocks** Differential clocks for the multiple ranks of DDR SDRAM. All DDR SDRAM operations are synchronized to the clock.
C_CS[3:0]#	O	4	**Chip Select** A DDR SDRAM row is selected when its C_CS# signal is asserted low.
C_DQ[63:0]	I/O	64	**Memory Data** This is the 64-bit data bus to the DDR SDRAMs.
C_DQMB[7:0]	O	8	**Data Mask** Used during read or write operations, one C_DQMB signal per data byte.
C_DQS[7:0]	I/O	8	**Data Strobe** Used to capture data at the processor and DDR SDRAM. When sending data to a DDR SDRAM, the strobe signal is aligned to the center of the data window to maintain timing margins. When receiving data from a DDR SDRAM, the strobe edge is aligned to the data at the processor pins.
C_RAS#	O	1	**Row Address Strobe** When asserted low, enables latching of the row address on the positive edge of the next clock.
C_VREF	I	1	**Voltage Reference** Reference voltage for the DDR SDRAM interface inputs. Used for SSTL-2 interface.
C_WE#	O	1	**Memory Write Enable** Enables write operations to the DDR SDRAMs.
Total Signals		109	

Table 10: Logical Alignment of DDR Byte Enables, Data Strobes and Data Bits

Byte Enable C_DQMB[7:0]	Data Strobe C_DQS[7:0]	Data Bits C_DQ[63:0]
C_DQMB0	C_DQS0	C_DQ[7:0]
C_DQMB1	C_DQS1	C_DQ[15:8]
C_DQMB2	C_DQS2	C_DQ[23:16]
C_DQMB3	C_DQS3	C_DQ[31:24]
C_DQMB4	C_DQS4	C_DQ[39:32]
C_DQMB5	C_DQS5	C_DQ[47:40]
C_DQMB6	C_DQS6	C_DQ[55:48]
C_DQMB7	C_DQS7	C_DQ[63:56]

Table 11 lists the memory address translations that correspond to the various SDRAM devices supported by TM5700/TM5900 processors.

Table 11: Memory Address Translations

SDRAM Device Config [1]	CS#	BS1	BS0	C10 [2]	C09	C08	C(07-00)	R12	R11	R(10-00)
64M / 4-Bank:										
4M x 16	A25	A23	A11	-	-	-	A(10-03)	-	A24	A(22-12)
8M x 8	A26	A23	A11	-	-	A25	A(10-03)	-	A24	A(22-12)
16M x 4	A27	A23	A11	-	A26	A25	A(10:03)	-	A24	A(22-12)
128M / 4-Bank:										
8M x 16	A26	A23	A11	-	-	A25	A(10-03)	A25	A24	A(22-12)
16M x 8	A27	A23	A11	-	A26	A25	A(10-03)	A25	A24	A(22-12)
32M x 4	A28	A23	A11	A27	A26	A25	A(10-03)	A25	A24	A(22-12)
256M / 4-Bank:										
16M x 16	A27	A23	A11	-	-	A26	A(10-03)	A25	A24	A(22-12)
32M x 8	A28	A23	A11	-	A27	A26	A(10-03)	A25	A24	A(22-12)
64M x 4	A29	A23	A11	A28	A27	A26	A(10-03)	A25	A24	A(22-12)
512M / 4-Bank:										
32M x 16	A28	A23	A11	-	-	A27	A(10-03)	A25	A24	A(22-12)
64M x 8	A29	A23	A11	-	A28	A27	A(10-03)	A25	A24	A(22-12)

1. SDRAM device configuration is as follows: nM, xB = n Mbits, x banks.
2. Column address 10 (C10) is sent out on address signal 11 during CAS cycle rather than address signal 10.

   Key: CS# = Chip select or side select
   Bn = Bank select
   Cnn = SDRAM column address
   Rnn = SDRAM row address
   Ann = Processor address nn

Table 12: PCI Interface Signals

Signal Name	Type	Qty	Description
P_AD[31:0]	I/O	32	**Address/Data** The address is driven with P_FRAME#, and data is written or read with subsequent clocks.
P_CBE[3:0]#	I/O	4	**Command/Byte Enable** Command is driven with P_FRAME#. Byte enables correspond with the appropriate data on the PCI bus during read and write data cycles.
P_CLKRUN#	I/O	1	**Clock Run** This signal is open drain, and an external 2.7 KΩ resistor is required. When asserted low, the PCI clock is enabled to run.
P_DEVSEL#	I/O	1	**Device Select** Driven when a PCI initiator is accessing SDRAM.
P_FRAME#	I/O	1	**Frame** Asserted active low to indicate the beginning of a PCI access (address phase). Forced inactive high to indicate that another transfer is desired by the initiator of the cycle.
P_GNT[5:0]#	O	6	**Grant** Signals that permission is given for a master to use the PCI bus.
P_HLDA#	O	1	**PCI Hold Acknowledge** Driven to a bridge device in response to its P_HOLD# request to indicate that the bridge can take control of the PCI bus.
P_HOLD#	I	1	**PCI Hold** Asserted by an expansion bridge to request use of the PCI bus.
P_IRDY#	I/O	1	**Initiator Ready** Asserted by the initiator to indicate that it is ready for data transfer.
P_LOCK#	I/O	1	**Lock** While asserted, the currently accessed PCI resource is locked.
P_PAR	I/O	1	**Parity** Single bit representing the parity of lines P_AD[31:0] and P_CBE[3:0]#.
P_PCI_RST#	I/O	1	**Reset** Asynchronously resets the module PCI interface and northbridge, and puts all PCI signals into tristate.
P_PCLK	I	1	**PCI Clock** Clock signal for PCI interface.
P_PERR#	I/O	1	**PCI Parity Error** Signals/detects a parity error detected.
P_REQ[5:0]#	I	6	**PCI Request** A PCI master asserts this signal to request access to the PCI bus.
P_SERR#	I	1	**System error** Indicates a system error condition detected.
P_STOP#	I/O	1	**Stop** Asserted by a target device to request the master stop driving the PCI bus.
P_TRDY#	I/O	1	**Target Ready** Asserted by the target to indicate that it is ready for a data transfer.
Total Signals		62	

Table 13: Southbridge Sideband Interface Signals

Signal Name	Type	Qty	Description
FERR#	O	1	**Floating Point Unit Error** Driven by the processor when a floating point error is detected.
IGNNE#	I	1	**Ignore Numeric Error** Driven by the southbridge, this signal instructs the processor to ignore numeric exceptions and to continue to execute non-control floating point instructions.
INIT#	I	1	**Initialize** Asserted by the southbridge for system initialization. If INIT# is asserted, the processor resets internal integer registers.
INTR	I	1	**Interrupt** Driven by the southbridge to the processor to indicate that a maskable interrupt from a device is pending.
NMI	I	1	**Non-Maskable Interrupt** Forces a non-maskable interrupt to the processor.
SLEEP#	I	1	**Sleep** Used to put the processor into a low power Deep Sleep mode. Turns off PCI interface by stopping PCI clock and tri-stating PCI signals. Allows P_PCLK to be stopped.
SMI#	I	1	**System Management Interrupt** This input requests that an interrupt be serviced for system management functions such as power control.
STPCLK#	I	1	**Stop Clock** Stops all processor internal clocks except the internal master controller and the PCI controller.
Total Signals		8	

Table 14: Serial Interface Signals

Signal Name	Type	Qty	Description
S_SCLK	I/O	1	**Serial Clock** Clock for debug serial interface.
S_SDATA	I/O	1	**Serial Data** Data for debug serial interface.
CFG_SCLK	O	1	**Configuration (Mode-Bit) ROM Clock** Clock for the serial interface to the configuration ROM. Reading the configuration ROM is initiated by deassertion of P_RST# and is clocked at a frequency of CLKIN x 1/72.
CFG_SDATA	I/O	1	**Configuration (Mode-Bit) ROM Data** Data for the serial interface to the configuration ROM.
SROM_CS[1:0]#	O	2	**Code Morphing Software Boot ROM Chip Selects** When using two 512 KByte devices, SROM_CS0# selects the lower 512 KBytes and SROM_CS1# selects the upper 512 KBytes. When using a single 1 MByte device, only SROM_CS0# is used.
SROM_SCLK	O	1	**Code Morphing Software Boot ROM Clock** Clock from the processor to the Code Morphing software boot ROM.
SROM_SIN	I	1	**Code Morphing Software Boot ROM Serial Data In** Data from the Code Morphing software boot ROM to the processor.
SROM_SOUT	O	1	**Code Morphing Software Boot ROM Serial Data Out** Data from the processor to the Code Morphing software boot ROM.
Total Signals		9	

Table 15: Thermal/Power/System Management Signals

Signal Name	Type	Qty	Description
DIODE_ANODE	I	1	**Thermal Diode** Anode for the internal thermal diode used to monitor the processor junction temperature.
DIODE_CATHODE	O	1	**Thermal Diode** Cathode for the internal thermal diode used to monitor the processor junction temperature.
PWRGOOD	I	1	**Power Good** Indicates that the processor input clock and power supplies are stable and within operating range specifications.
VRDA[4:0]	O	5	**Voltage Regulator Control** These signals are used by Code Morphing software LongRun power management to control the processor core regulator power supply module output voltage (CVDD).
EPROMA[2:0]	O	3	**BIOS ROM Address Bits** EPROMA[2:1] are used as address bits [19:18] for the BIOS EPROM. EPROMA[0] is not used, and there should be no electrical connection to it.
UNPROTECT	O	1	**Unprotect** Used to unprotect the Code Morphing software ROM to allow authorized upgrades.
RESET#	I	1	**Master Reset** Processor master reset input.
CLKIN	I	1	**Master Clock** Processor master clock input.
Total Signals		14	

Table 16: JTAG Interface and Debug Signals

Signal Name	Type	Qty	Description
TCK	I	1	**JTAG Test Clock** IEEE 1149.1 clock input.
TDI	I	1	**JTAG Test Data In** IEEE 1149.1 data input, has an internal pull-up.
TDO	O	1	**JTAG Test Data Out** IEEE 1149.1 data output.
TMS	I	1	**JTAG Test Mode Select** IEEE 1149.1 test mode select signal, has an internal pull-up.
TRST#	I	1	**JTAG Reset** IEEE 1149.1 reset signal, has an internal pull-up. This signal is an asynchronous input that resets the test logic in the processor. TRST# must be connected to RESET# if the JTAG interface signals are not going to be used.
DEBUG_INT	I	1	**Debug Interrupt Input** This signal is used for debugging purposes only. For proper operation, DEBUG_INT should be connected to GND through a 10 KΩ resistor.
DEBUG_NMI	I	1	**Debug NMI Input** This signal is used for debugging purposes only. For proper operation, DEBUG_NMI should be connected to GND through a 10 KΩ resistor.
Total Signals		7	

Table 17: Reserved and No Connection Signals

Signal Name	Type	Qty	Description
RSV_F4_NC	I	1	**Reserved Inputs** There should be no connection to these reserved signals.
RSV_G17_NC	I	1	
RSV_H2_NC	I	1	
RSV_H3_NC	I	1	
RSV_H17_NC	I	1	
RSV_H18_NC	I	1	
RSV_H19_NC	I	1	
RSV_H20_NC	I	1	
RSV_J1_NC	I	1	
RSV_J17_NC	I	1	
RSV_J18_NC	I	1	
RSV_K3_NC	I	1	
RSV_K17_NC	I	1	
RSV_K18_NC	I	1	
RSV_T3_NC	I	1	
RSV_T4_NC	I	1	
RSV_U13_NC	I	1	
RSV_V19_NC	I	1	
RSV_W12_NC	I	1	
RSV_W20_NC	I	1	
RSV_Y13_NC	I	1	
RSV_G19_PD	I	1	**Reserved Inputs** Connect to 10 KΩ pull-down resistor to GND.
RSV_J3_PD	I	1	
Total Signals		23	

Table 18: Power and Ground Signals

Signal Name	Qty	Description
SNIFF_CVDD	1	**Core Power Supply Sniff** Feedback signal for core voltage supply.
CVDD	36	**Core Power Supply** CVDD = 0.80-1.40 V nominal (depends on SKU and LongRun operating point). See Recommended Operating Conditions on page 56 for detailed CVDD specifications.
IOVDD	15	**3.3 V I/O Power Supply** IOVDD = 3.3 V nominal.
IOVDD25	28	**2.5 V I/O Power Supply** IOVDD25 = 2.5 V nominal.
PLLVDD	1	**PLL Power Supply** PLLVDD tracks the core voltage (CVDD). See Recommended Operating Conditions on page 56 for detailed PLLVDD specifications.
GND	86	**Ground** Reference point for all single-ended signals and power supplies.
Total Signals	167	

2.2 I/O Signal Listings

The following tables summarize signal characteristics for each of the I/O signals. Table 19 lists the input signals, Table 20 lists the output signals and Table 21 lists the bidirectional signals.

Table 19: Input Only Signals

Signal Name	Internal Resistor	Active Level	Clock Domain	DC Specs	AC Specs
C_VREF	-	-	-	Table 26	-
CLKIN	-	-	-	Table 29	*Power On Specifications*,*Input Clocks*
DEBUG_INT	-	High	Asynchronous	Table 42	-
DEBUG_NMI	-	High	Asynchronous	Table 42	-
DIODE_ANODE	-	-	-	Table 32	-
IGNNE#	-	Low	Asynchronous	Table 29	*Southbridge Sidebands and Power Management Interface*
INIT#	-	Low	Asynchronous	Table 29	*Southbridge Sidebands and Power Management Interface*
INTR	-	High	Asynchronous	Table 29	*Southbridge Sidebands and Power Management Interface*
NMI	-	High	Asynchronous	Table 29	*Southbridge Sidebands and Power Management Interface*
P_HOLD#	-	Low	P_PCLK	Table 31	*PCI Interface*
P_PCLK	-	-	-	Table 31	*Power On Specifications*,*Input Clocks*,*PCI Interface*
P_SERR#	-	Low	P_PCLK	Table 31	*PCI Interface*
P_REQ[5:0]#	-	Low	P_PCLK	Table 31	*PCI Interface*
PWRGOOD	-	High	Asynchronous	Table 29	*Power On Specifications*,*Southbridge Sidebands and Power Management Interface*
RESET#	-	Low	Asynchronous	Table 29	*Power On Specifications*
SLEEP#	-	Low	Asynchronous	Table 29	*Southbridge Sidebands and Power Management Interface*

Table 19: Input Only Signals (Continued)

Signal Name	Internal Resistor	Active Level	Clock Domain	DC Specs	AC Specs
SMI#	-	Low	Asynchronous	Table 29	*Southbridge Sidebands and Power Management Interface*
SROM_SIN	-	-	SROM_SCLK	Table 29	*Code Morphing Software Boot ROM Interface*
STPCLK#	-	Low	Asynchronous	Table 29	*Southbridge Sidebands and Power Management Interface*
TCK	-	-	-	Table 29	*JTAG Interface*
TDI	Pull-up	High	TCK	Table 29	*JTAG Interface*
TMS	Pull-up	High	TCK	Table 29	*JTAG Interface*
TRST#	Pull-up	Low	Asynchronous	Table 29	*JTAG Interface*

Table 20: Output Only Signals

Signal Name	Signal Type	Active Level	Clock	Reset State	Doze State[1]	DC Specs	AC Specs
C_A[12:0]	Tri-state	-	C_CLK	1/0	Hi-Z	Table 30	*DDR SDRAM Interface*
C_BA[1:0]	Tri-state	High	C_CLK	1/0	Hi-Z	Table 30	*DDR SDRAM Interface*
C_CAS#	Tri-state	Low	C_CLK	1	Hi-Z	Table 30	*DDR SDRAM Interface*
C_CKE[1:0]	Tri-state	High	C_CLK	0	0	Table 30	*DDR SDRAM Interface*
C_CLKA, C_CLKA#, C_CLKB, C_CLKB#	Tri-state	-	-	Toggle	Hi-Z	Table 30	*DDR SDRAM Interface*
C_CS[3:0]#	Tri-state	Low	C_CLK	1	Hi-Z	Table 30	*DDR SDRAM Interface*
C_DQMB[7:0]	Tri-state	High	C_CLK	0	Hi-Z	Table 30	*DDR SDRAM Interface*
C_RAS#	Tri-state	Low	C_CLK	1	Hi-Z	Table 30	*DDR SDRAM Interface*
C_WE#	Tri-state	Low	C_CLK	1	Hi-Z	Table 30	*DDR SDRAM Interface*
CFG_SCLK	Tri-state	-	-	Hi-Z	Hi-Z	Table 29	*Configuration (Mode-bit) ROM Interface*
DIODE_CATHODE	Tri-state	-	-	Lo-Z	Lo-Z	Table 32	-
EPROMA[2:0]	Tri-state	High	Asynch.	0	Hi-Z	Table 29	-
FERR#	Open drain	Low	Asynch.	Hi-Z	Hi-Z	Table 29	-
P_GNT[5:0]#	Tri-state	Low	P_PCLK	Hi-Z	Hi-Z	Table 31	*PCI Interface*
P_HLDA#	Tri-state	Low	P_PCLK	Hi-Z	Hi-Z	Table 31	*PCI Interface*
SROM_CS[1:0]#	Tri-state	Low	SROM_SCLK	Hi-Z	Hi-Z	Table 29	*Code Morphing Software Boot ROM Interface*
SROM_SCLK	Tri-state	-	-	Hi-Z	Hi-Z	Table 29	*Code Morphing Software Boot ROM Interface*
SROM_SOUT	Tri-state	-	SROM_SCLK	Hi-Z	Hi-Z	Table 29	*Code Morphing Software Boot ROM Interface*
TDO	Tri-state	-	TCK	Hi-Z	Hi-Z	Table 29	*JTAG Interface*
UNPROTECT	Tri-state	High	Asynch.	Hi-Z	Hi-Z	Table 29	-
VRDA[4:0]	Open drain	-	-	1/0	Lo-Z	Table 29	-

1. Doze state refers to the state of the signal during low-power modes when the specific interface is disabled. In the case of the SDRAM interfaces, the doze state refers to the state of the signal while the SDRAM is in self-refresh.

Table 21: Bidirectional Signals

Signal Name	Signal Type	Active Level	Clock	Reset State	Doze State[1]	DC Specs	AC Specs
C_DQ[63:0]		-	C_CLK	Hi-Z	Hi-Z	Table 30	*DDR SDRAM Interface*
C_DQS[7:0]		-	C_CLK	Hi-Z	Hi-Z	Table 30	*DDR SDRAM Interface*
CFG_SDATA		-	CFG_SCLK	Hi-Z	Hi-Z	Table 29	*Configuration (Mode-bit) ROM Interface*
P_AD[31:0]		-	P_PCLK	0	Hi-Z	Table 31	*PCI Interface*
P_CBE[3:0]#		Low	P_PCLK	0	Hi-Z	Table 31	*PCI Interface*
P_CLKRUN#	Open drain	Low	P_PCLK	Hi-Z	Hi-Z	Table 31	*PCI Interface*
P_DEVSEL#		Low	P_PCLK	Hi-Z	Hi-Z	Table 31	*PCI Interface*
P_FRAME#		Low	P_PCLK	Hi-Z	Hi-Z	Table 31	*PCI Interface*
P_IRDY#		Low	P_PCLK	Hi-Z	Hi-Z	Table 31	*PCI Interface*
P_LOCK#		Low	P_PCLK	Hi-Z	Hi-Z	Table 31	*PCI Interface*
P_PAR		High	P_PCLK	0	Hi-Z	Table 31	*PCI Interface*
P_PCI_RST#		Low	Asynch.	-	Hi-Z	Table 31	*Power On Specifications*, *PCI Interface*
P_PERR#		Low	P_PCLK	Hi-Z	Hi-Z	Table 31	*PCI Interface*
P_STOP#		Low	P_PCLK	Hi-Z	Hi-Z	Table 31	*PCI Interface*
P_TRDY#		Low	P_PCLK	Hi-Z	Hi-Z	Table 31	*PCI Interface*
S_SCLK	Open drain	-	-	Hi-Z	Hi-Z	Table 29	*Debug Interface*
S_SDATA	Open drain	-	S_SCLK	Hi-Z	Hi-Z	Table 29	*Debug Interface*

1. Doze state refers to the state of the signal during low-power modes when the specific interface is disabled. In the case of the SDRAM interfaces, the doze state refers to the state of the signal while the SDRAM is in self-refresh.

2.3 Footprint and Ballout Assignments

Figure 9 shows the TM5700/TM5900 processor package footprint. Figure 10 shows the processor package ball assignments. Table 22 and Table 23 list the ballout assignments for each signal on the processor.

Figure 9: Package Footprint - Top Down View

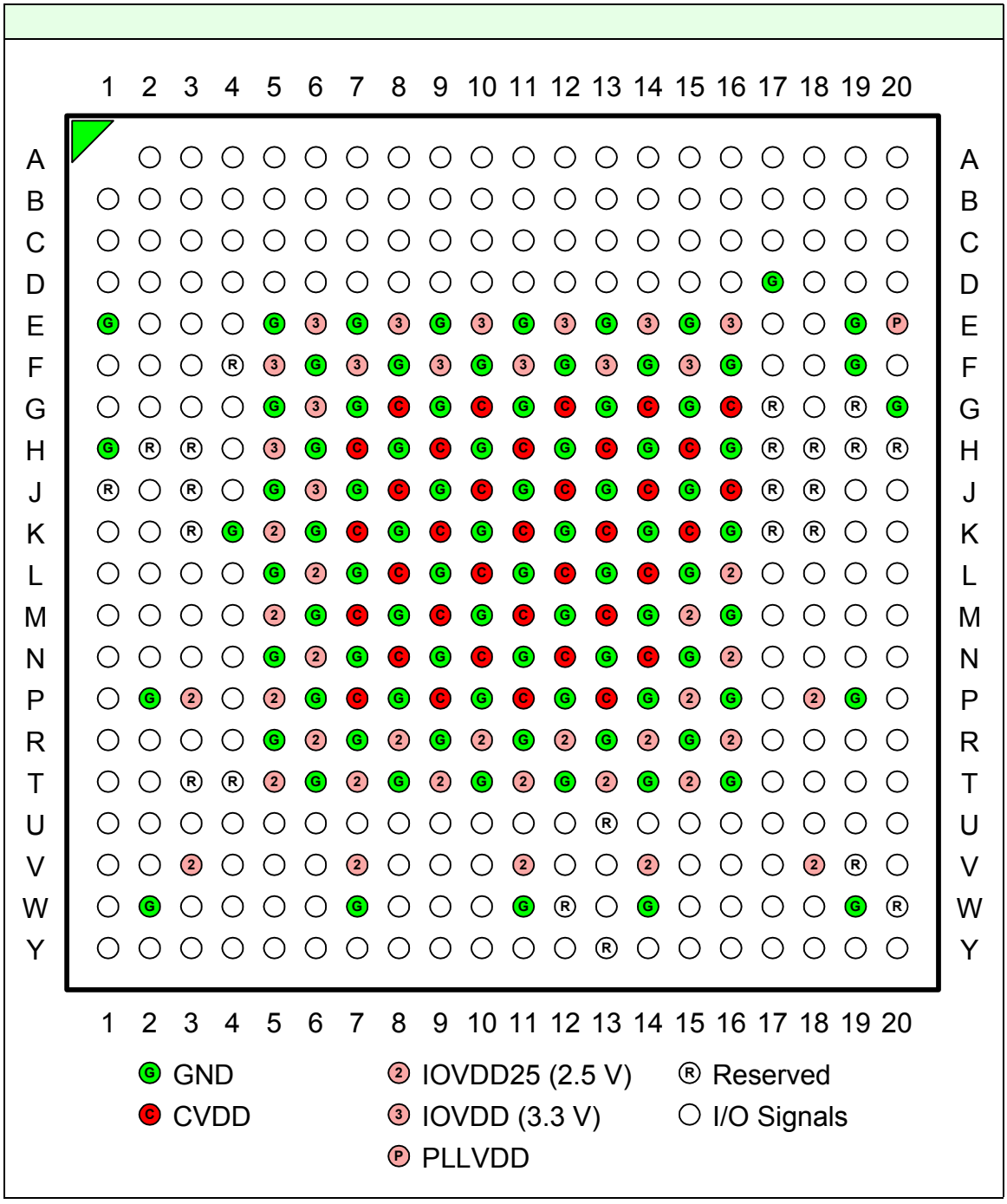


Figure 10: Package Ball-Signal Assignments - Top Down View (Left Half)

	1	2	3	4	5	6	7	8	9	10
A		P_AD3	P_AD5	P_AD8	P_AD9	P_AD15	P_PAR	P_TRDY#	P_IRDY#	P_AD19
B	P_AD1	P_AD0	P_AD2	P_AD7	P_CBE0#	P_AD14	P_CBE1#	P_DEVSEL#	P_CLKRUN#	P_AD18
C	P_PCLK	P_PCI_RST#	P_AD4	P_AD6	P_AD12	P_AD13	P_PERR#	P_STOP#	P_CBE2#	P_AD17
D	NMI	STPCLK#	INTR	EPROMA0	P_AD10	P_AD11	P_SERR#	P_LOCK#	P_FRAME#	P_AD16
E	GND	FERR#	PWRGOOD	EPROMA2	GND	IOVDD	GND	IOVDD	GND	IOVDD
F	DIODE_CATHODE	IGNNE#	SMI#	RSV_F4_NC	IOVDD	GND	IOVDD	GND	IOVDD	GND
G	DIODE_ANODE	SLEEP#	INIT#	EPROMA1	GND	IOVDD	GND	CVDD	GND	CVDD
H	GND	RSV_H2_NC	RSV_H3_NC	RESET#	IOVDD	GND	CVDD	GND	CVDD	GND
J	RSV_J1_NC	UNPROTECT	RSV_J3_PD	CLKIN	GND	IOVDD	GND	CVDD	GND	CVDD
K	C_DQ62	C_DQ63	RSV_K3_NC	GND	IOVDD25	GND	CVDD	GND	CVDD	GND
L	C_DQ59	C_DQ58	C_DQMB7	C_DQ61	GND	IOVDD25	GND	CVDD	GND	CVDD
M	C_DQS7	C_DQ57	C_DQ60	C_DQ55	IOVDD25	GND	CVDD	GND	CVDD	GND
N	C_DQ56	C_DQ51	C_DQ54	C_DQMB6	GND	IOVDD25	GND	CVDD	GND	CVDD
P	C_DQ50	GND	IOVDD25	C_DQ53	IOVDD25	GND	CVDD	GND	CVDD	GND
R	C_DQS6	C_DQ49	C_DQ52	C_DQ47	GND	IOVDD25	GND	IOVDD25	GND	IOVDD25
T	C_DQ48	C_DQ43	RSV_T3_NC	RSV_T4_NC	IOVDD25	GND	IOVDD25	GND	IOVDD25	GND
U	C_DQ42	C_DQS5	C_CLKB	C_CLKB#	C_DQMB5	C_DQ44	C_DQ38	C_DQMB4	C_DQ36	C_A0
V	C_DQ41	C_DQ40	IOVDD25	C_DQ46	C_DQ45	C_DQ39	IOVDD25	C_DQ37	C_BA1	C_A2
W	C_DQ35	GND	C_DQ33	C_CS1#	C_CS2#	C_CAS#	GND	C_BA0	C_A1	C_A5
Y	C_DQ34	C_DQS4	C_DQ32	C_CS0#	C_CS3#	C_RAS#	C_WE#	C_A10	C_A3	C_A7
	1	2	3	4	5	6	7	8	9	10

Figure 11: Package Ball-Signal Assignments - Top Down View (Right Half)

11	12	13	14	15	16	17	18	19	20	
P_AD20	P_AD22	P_CBE3#	P_AD29	P_AD31	P_HOLD#	P_GNT5#	DEBUG_NMI	CFG_SCLK	CFG_SDATA	A
P_AD21	P_AD23	P_AD24	P_AD30	P_REQ5#	P_REQ0#	P_GNT4#	DEBUG_INT	SROM_CS1#	SROM_CS0#	B
P_AD25	P_AD27	P_REQ4#	P_REQ2#	P_GNT3#	P_GNT1#	P_HLDA#	SROM_SCLK	SROM_SOUT	SROM_SIN	C
P_AD26	P_AD28	P_REQ3#	P_REQ1#	P_GNT2#	P_GNT0#	GND	S_SCLK	S_SDATA	SNIFF_CVDD	D
GND	IOVDD	GND	IOVDD	GND	IOVDD	TDI	TDO	GND	PLLVDD	E
IOVDD	GND	IOVDD	GND	IOVDD	GND	TCK	TMS	GND	C_VREF	F
GND	CVDD	GND	CVDD	GND	CVDD	RSV_G17_NC	TRST#	RSV_G19_PD	GND	G
CVDD	GND	CVDD	GND	CVDD	GND	RSV_H17_NC	RSV_H18_NC	RSV_H19_NC	RSV_H20_NC	H
GND	CVDD	GND	CVDD	GND	CVDD	RSV_J17_NC	RSV_J18_NC	VRDA1	VRDA4	J
CVDD	GND	CVDD	GND	CVDD	GND	RSV_K17_NC	RSV_K18_NC	VRDA2	VRDA3	K
GND	CVDD	GND	CVDD	GND	IOVDD25	C_DQMB0	C_DQ5	C_DQ4	VRDA0	L
CVDD	GND	CVDD	GND	IOVDD25	GND	C_DQ7	C_DQ6	C_DQ1	C_DQ0	M
GND	CVDD	GND	CVDD	GND	IOVDD25	C_DQ13	C_DQ12	C_DQ2	C_DQS0	N
CVDD	GND	CVDD	GND	IOVDD25	GND	C_DQMB1	IOVDD25	GND	C_DQ3	P
GND	IOVDD25	GND	IOVDD25	GND	IOVDD25	C_DQ15	C_DQ14	C_DQ9	C_DQ8	R
IOVDD25	GND	IOVDD25	GND	IOVDD25	GND	C_DQ21	C_DQ20	C_DQ10	C_DQS1	T
C_A4	C_A8	RSV_U13_NC	C_DQ31	C_DQMB3	C_DQ28	C_DQ22	C_DQMB2	C_CLKA	C_DQ11	U
IOVDD25	C_A6	C_A11	IOVDD25	C_DQ30	C_DQ29	C_DQ23	IOVDD25	RSV_V19_NC	C_CLKA#	V
GND	RSV_W12_NC	C_CKE1	GND	C_DQ26	C_DQ25	C_DQ19	C_DQS2	GND	RSV_W20_NC	W
C_A9	C_A12	RSV_Y13_NC	C_CKE0	C_DQ27	C_DQS3	C_DQ24	C_DQ18	C_DQ17	C_DQ16	Y
11	12	13	14	15	16	17	18	19	20	

Table 22: Signal Ballout Assignments - Sorted by Ball Number

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	*No Ball*	A2	P_AD3	A3	P_AD5
A4	P_AD8	A5	P_AD9	A6	P_AD15
A7	P_PAR	A8	P_TRDY#	A9	P_IRDY#
A10	P_AD19	A11	P_AD20	A12	P_AD22
A13	P_CBE3#	A14	P_AD29	A15	P_AD31
A16	P_HOLD#	A17	P_GNT5#	A18	DEBUG_NMI
A19	CFG_SCLK	A20	CFG_SDATA	B1	P_AD1
B2	P_AD0	B3	P_AD2	B4	P_AD7
B5	P_CBE0#	B6	P_AD14	B7	P_CBE1#
B8	P_DEVSEL#	B9	P_CLKRUN#	B10	P_AD18
B11	P_AD21	B12	P_AD23	B13	P_AD24
B14	P_AD30	B15	P_REQ5#	B16	P_REQ0#
B17	P_GNT4#	B18	DEBUG_INT	B19	SROM_CS1#
B20	SROM_CS0#	C1	P_PCLK	C2	P_PCI_RST#
C3	P_AD4	C4	P_AD6	C5	P_AD12
C6	P_AD13	C7	P_PERR#	C8	P_STOP#
C9	P_CBE2#	C10	P_AD17	C11	P_AD25
C12	P_AD27	C13	P_REQ4#	C14	P_REQ2#
C15	P_GNT3#	C16	P_GNT1#	C17	P_HLDA#
C18	SROM_SCLK	C19	SROM_SOUT	C20	SROM_SIN
D1	NMI	D2	STPCLK#	D3	INTR
D4	EPROMA0	D5	P_AD10	D6	P_AD11
D7	P_SERR#	D8	P_LOCK#	D9	P_FRAME#
D10	P_AD16	D11	P_AD26	D12	P_AD28
D13	P_REQ3#	D14	P_REQ1#	D15	P_GNT2#
D16	P_GNT0#	D17	GND	D18	S_SCLK
D19	S_SDATA	D20	SNIFF_CVDD	E1	GND
E2	FERR#	E3	PWRGOOD	E4	EPROMA2
E5	GND	E6	IOVDD	E7	GND
E8	IOVDD	E9	GND	E10	IOVDD
E11	GND	E12	IOVDD	E13	GND
E14	IOVDD	E15	GND	E16	IOVDD
E17	TDI	E18	TDO	E19	GND
E20	PLLVDD	F1	DIODE_CATHODE	F2	IGNNE#
F3	SMI#	F4	RSV_F4_NC	F5	IOVDD
F6	GND	F7	IOVDD	F8	GND
F9	IOVDD	F10	GND	F11	IOVDD
F12	GND	F13	IOVDD	F14	GND
F15	IOVDD	F16	GND	F17	TCK
F18	TMS	F19	GND	F20	C_VREF

Table 22: Signal Ballout Assignments - Sorted by Ball Number (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
G1	DIODE_ANODE	G2	SLEEP#	G3	INIT#
G4	EPROMA1	G5	GND	G6	IOVDD
G7	GND	G8	CVDD	G9	GND
G10	CVDD	G11	GND	G12	CVDD
G13	GND	G14	CVDD	G15	GND
G16	CVDD	G17	RSV_G17_NC	G18	TRST#
G19	RSV_G19_PD	G20	GND	H1	GND
H2	RSV_H2_NC	H3	RSV_H3_NC	H4	RESET#
H5	IOVDD	H6	GND	H7	CVDD
H8	GND	H9	CVDD	H10	GND
H11	CVDD	H12	GND	H13	CVDD
H14	GND	H15	CVDD	H16	GND
H17	RSV_H17_NC	H18	RSV_H18_NC	H19	RSV_H19_NC
H20	RSV_H20_NC	J1	RSV_J1_NC	J2	UNPROTECT
J3	RSV_J3_PD	J4	CLKIN	J5	GND
J6	IOVDD	J7	GND	J8	CVDD
J9	GND	J10	CVDD	J11	GND
J12	CVDD	J13	GND	J14	CVDD
J15	GND	J16	CVDD	J17	RSV_J17_NC
J18	RSV_J18_NC	J19	VRDA1	J20	VRDA4
K1	C_DQ62	K2	C_DQ63	K3	RSV_K3_NC
K4	GND	K5	IOVDD25	K6	GND
K7	CVDD	K8	GND	K9	CVDD
K10	GND	K11	CVDD	K12	GND
K13	CVDD	K14	GND	K15	CVDD
K16	GND	K17	RSV_K17_NC	K18	RSV_K18_NC
K19	VRDA2	K20	VRDA3	L1	C_DQ59
L2	C_DQ58	L3	C_DQMB7	L4	C_DQ61
L5	GND	L6	IOVDD25	L7	GND
L8	CVDD	L9	GND	L10	CVDD
L11	GND	L12	CVDD	L13	GND
L14	CVDD	L15	GND	L16	IOVDD25
L17	C_DQMB0	L18	C_DQ5	L19	C_DQ4
L20	VRDA0	M1	C_DQS7	M2	C_DQ57
M3	C_DQ60	M4	C_DQ55	M5	IOVDD25
M6	GND	M7	CVDD	M8	GND
M9	CVDD	M10	GND	M11	CVDD
M12	GND	M13	CVDD	M14	GND
M15	IOVDD25	M16	GND	M17	C_DQ7
M18	C_DQ6	M19	C_DQ1	M20	C_DQ0
N1	C_DQ56	N2	C_DQ51	N3	C_DQ54

Table 22: Signal Ballout Assignments - Sorted by Ball Number (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
N4	C_DQMB6	N5	GND	N6	IOVDD25
N7	GND	N8	CVDD	N9	GND
N10	CVDD	N11	GND	N12	CVDD
N13	GND	N14	CVDD	N15	GND
N16	IOVDD25	N17	C_DQ13	N18	C_DQ12
N19	C_DQ2	N20	C_DQS0	P1	C_DQ50
P2	GND	P3	IOVDD25	P4	C_DQ53
P5	IOVDD25	P6	GND	P7	CVDD
P8	GND	P9	CVDD	P10	GND
P11	CVDD	P12	GND	P13	CVDD
P14	GND	P15	IOVDD25	P16	GND
P17	C_DQMB1	P18	IOVDD25	P19	GND
P20	C_DQ3	R1	C_DQS6	R2	C_DQ49
R3	C_DQ52	R4	C_DQ47	R5	GND
R6	IOVDD25	R7	GND	R8	IOVDD25
R9	GND	R10	IOVDD25	R11	GND
R12	IOVDD25	R13	GND	R14	IOVDD25
R15	GND	R16	IOVDD25	R17	C_DQ15
R18	C_DQ14	R19	C_DQ9	R20	C_DQ8
T1	C_DQ48	T2	C_DQ43	T3	RSV_T3_NC
T4	RSV_T4_NC	T5	IOVDD25	T6	GND
T7	IOVDD25	T8	GND	T9	IOVDD25
T10	GND	T11	IOVDD25	T12	GND
T13	IOVDD25	T14	GND	T15	IOVDD25
T16	GND	T17	C_DQ21	T18	C_DQ20
T19	C_DQ10	T20	C_DQS1	U1	C_DQ42
U2	C_DQS5	U3	C_CLKB	U4	C_CLKB#
U5	C_DQMB5	U6	C_DQ44	U7	C_DQ38
U8	C_DQMB4	U9	C_DQ36	U10	C_A0
U11	C_A4	U12	C_A8	U13	RSV_U13_NC
U14	C_DQ31	U15	C_DQMB3	U16	C_DQ28
U17	C_DQ22	U18	C_DQMB2	U19	C_CLKA
U20	C_DQ11	V1	C_DQ41	V2	C_DQ40
V3	IOVDD25	V4	C_DQ46	V5	C_DQ45
V6	C_DQ39	V7	IOVDD25	V8	C_DQ37
V9	C_BA1	V10	C_A2	V11	IOVDD25
V12	C_A6	V13	C_A11	V14	IOVDD25
V15	C_DQ30	V16	C_DQ29	V17	C_DQ23
V18	IOVDD25	V19	RSV_V19_NC	V20	C_CLKA#
W1	C_DQ35	W2	GND	W3	C_DQ33
W4	C_CS1#	W5	C_CS2#	W6	C_CAS#

Table 22: Signal Ballout Assignments - Sorted by Ball Number (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
W7	GND	W8	C_BA0	W9	C_A1
W10	C_A5	W11	GND	W12	RSV_W12_NC
W13	C_CKE1	W14	GND	W15	C_DQ26
W16	C_DQ25	W17	C_DQ19	W18	C_DQS2
W19	GND	W20	RSV_W20_NC	Y1	C_DQ34
Y2	C_DQS4	Y3	C_DQ32	Y4	C_CS0#
Y5	C_CS3#	Y6	C_RAS#	Y7	C_WE#
Y8	C_A10	Y9	C_A3	Y10	C_A7
Y11	C_A9	Y12	C_A12	Y13	RSV_Y13_NC
Y14	C_CKE0	Y15	C_DQ27	Y16	C_DQS3
Y17	C_DQ24	Y18	C_DQ18	Y19	C_DQ17
Y20	C_DQ16				

Table 23: Signal Ballout Assignments - Sorted by Signal Name

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
C_A0	U10	C_A1	W9	C_A2	V10
C_A3	Y9	C_A4	U11	C_A5	W10
C_A6	V12	C_A7	Y10	C_A8	U12
C_A9	Y11	C_A10	Y8	C_A11	V13
C_A12	Y12	C_BA0	W8	C_BA1	V9
C_CAS#	W6	C_CKE0	Y14	C_CKE1	W13
C_CLKA	U19	C_CLKA#	V20	C_CLKB	U3
C_CLKB#	U4	C_CS0#	Y4	C_CS1#	W4
C_CS2#	W5	C_CS3#	Y5	C_DQ0	M20
C_DQ1	M19	C_DQ2	N19	C_DQ3	P20
C_DQ4	L19	C_DQ5	L18	C_DQ6	M18
C_DQ7	M17	C_DQ8	R20	C_DQ9	R19
C_DQ10	T19	C_DQ11	U20	C_DQ12	N18
C_DQ13	N17	C_DQ14	R18	C_DQ15	R17
C_DQ16	Y20	C_DQ17	Y19	C_DQ18	Y18
C_DQ19	W17	C_DQ20	T18	C_DQ21	T17
C_DQ22	U17	C_DQ23	V17	C_DQ24	Y17
C_DQ25	W16	C_DQ26	W15	C_DQ27	Y15
C_DQ28	U16	C_DQ29	V16	C_DQ30	V15
C_DQ31	U14	C_DQ32	Y3	C_DQ33	W3
C_DQ34	Y1	C_DQ35	W1	C_DQ36	U9
C_DQ37	V8	C_DQ38	U7	C_DQ39	V6
C_DQ40	V2	C_DQ41	V1	C_DQ42	U1
C_DQ43	T2	C_DQ44	U6	C_DQ45	V5
C_DQ46	V4	C_DQ47	R4	C_DQ48	T1
C_DQ49	R2	C_DQ50	P1	C_DQ51	N2
C_DQ52	R3	C_DQ53	P4	C_DQ54	N3
C_DQ55	M4	C_DQ56	N1	C_DQ57	M2
C_DQ58	L2	C_DQ59	L1	C_DQ60	M3
C_DQ61	L4	C_DQ62	K1	C_DQ63	K2
C_DQMB0	L17	C_DQMB1	P17	C_DQMB2	U18
C_DQMB3	U15	C_DQMB4	U8	C_DQMB5	U5
C_DQMB6	N4	C_DQMB7	L3	C_DQS0	N20
C_DQS1	T20	C_DQS2	W18	C_DQS3	Y16
C_DQS4	Y2	C_DQS5	U2	C_DQS6	R1
C_DQS7	M1	C_RAS#	Y6	C_VREF	F20
C_WE#	Y7	CFG_SCLK	A19	CFG_SDATA	A20
CLKIN	J4	CVDD	G8	CVDD	G10
CVDD	G12	CVDD	G14	CVDD	G16
CVDD	H7	CVDD	H9	CVDD	H11

Table 23: Signal Ballout Assignments - Sorted by Signal Name (Continued)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
CVDD	H13	CVDD	H15	CVDD	J8
CVDD	J10	CVDD	J12	CVDD	J14
CVDD	J16	CVDD	K7	CVDD	K9
CVDD	K11	CVDD	K13	CVDD	K15
CVDD	L8	CVDD	L10	CVDD	L12
CVDD	L14	CVDD	M7	CVDD	M9
CVDD	M11	CVDD	M13	CVDD	N8
CVDD	N10	CVDD	N12	CVDD	N14
CVDD	P7	CVDD	P9	CVDD	P11
CVDD	P13	DEBUG_INT	B18	DEBUG_NMI	A18
DIODE_ANODE	G1	DIODE_CATHODE	F1	EPROMA0	D4
EPROMA1	G4	EPROMA2	E4	FERR#	E2
GND	D17	GND	E1	GND	E5
GND	E7	GND	E9	GND	E11
GND	E13	GND	E15	GND	E19
GND	F6	GND	F8	GND	F10
GND	F12	GND	F14	GND	F16
GND	F19	GND	G5	GND	G7
GND	G9	GND	G11	GND	G13
GND	G15	GND	G20	GND	H1
GND	H6	GND	H8	GND	H10
GND	H12	GND	H14	GND	H16
GND	J5	GND	J7	GND	J9
GND	J11	GND	J13	GND	J15
GND	K4	GND	K6	GND	K8
GND	K10	GND	K12	GND	K14
GND	K16	GND	L5	GND	L7
GND	L9	GND	L11	GND	L13
GND	L15	GND	M6	GND	M8
GND	M10	GND	M12	GND	M14
GND	M16	GND	N5	GND	N7
GND	N9	GND	N11	GND	N13
GND	N15	GND	P2	GND	P6
GND	P8	GND	P10	GND	P12
GND	P14	GND	P16	GND	P19
GND	R5	GND	R7	GND	R9
GND	R11	GND	R13	GND	R15
GND	T6	GND	T8	GND	T10
GND	T12	GND	T14	GND	T16
GND	W2	GND	W7	GND	W11
GND	W14	GND	W19	IGNNE#	F2

Table 23: Signal Ballout Assignments - Sorted by Signal Name (Continued)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
INIT#	G3	INTR	D3	IOVDD	E6
IOVDD	E8	IOVDD	E10	IOVDD	E12
IOVDD	E14	IOVDD	E16	IOVDD	F5
IOVDD	F7	IOVDD	F9	IOVDD	F11
IOVDD	F13	IOVDD	F15	IOVDD	G6
IOVDD	H5	IOVDD	J6	IOVDD25	K5
IOVDD25	L6	IOVDD25	L16	IOVDD25	M5
IOVDD25	M15	IOVDD25	N6	IOVDD25	N16
IOVDD25	P3	IOVDD25	P5	IOVDD25	P15
IOVDD25	P18	IOVDD25	R6	IOVDD25	R8
IOVDD25	R10	IOVDD25	R12	IOVDD25	R14
IOVDD25	R16	IOVDD25	T5	IOVDD25	T7
IOVDD25	T9	IOVDD25	T11	IOVDD25	T13
IOVDD25	T15	IOVDD25	V3	IOVDD25	V7
IOVDD25	V11	IOVDD25	V14	IOVDD25	V18
NMI	D1	P_AD0	B2	P_AD1	B1
P_AD2	B3	P_AD3	A2	P_AD4	C3
P_AD5	A3	P_AD6	C4	P_AD7	B4
P_AD8	A4	P_AD9	A5	P_AD10	D5
P_AD11	D6	P_AD12	C5	P_AD13	C6
P_AD14	B6	P_AD15	A6	P_AD16	D10
P_AD17	C10	P_AD18	B10	P_AD19	A10
P_AD20	A11	P_AD21	B11	P_AD22	A12
P_AD23	B12	P_AD24	B13	P_AD25	C11
P_AD26	D11	P_AD27	C12	P_AD28	D12
P_AD29	A14	P_AD30	B14	P_AD31	A15
P_CBE0#	B5	P_CBE1#	B7	P_CBE2#	C9
P_CBE3#	A13	P_CLKRUN#	B9	P_DEVSEL#	B8
P_FRAME#	D9	P_GNT0#	D16	P_GNT1#	C16
P_GNT2#	D15	P_GNT3#	C15	P_GNT4#	B17
P_GNT5#	A17	P_HLDA#	C17	P_HOLD#	A16
P_IRDY#	A9	P_LOCK#	D8	P_PAR	A7
P_PCI_RST#	C2	P_PCLK	C1	P_PERR#	C7
P_REQ0#	B16	P_REQ1#	D14	P_REQ2#	C14
P_REQ3#	D13	P_REQ4#	C13	P_REQ5#	B15
P_SERR#	D7	P_STOP#	C8	P_TRDY#	A8
PLLVDD	E20	PWRGOOD	E3	RESET#	H4
RSV_F4_NC	F4	RSV_G17_NC	G17	RSV_G19_PD	G19
RSV_H2_NC	H2	RSV_H3_NC	H3	RSV_H17_NC	H17
RSV_H18_NC	H18	RSV_H19_NC	H19	RSV_H20_NC	H20
RSV_J1_NC	J1	RSV_J3_PD	J3	RSV_J17_NC	J17

Table 23: Signal Ballout Assignments - Sorted by Signal Name (Continued)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
RSV_J18_NC	J18	RSV_K3_NC	K3	RSV_K17_NC	K17
RSV_K18_NC	K18	RSV_T3_NC	T3	RSV_T4_NC	T4
RSV_U13_NC	U13	RSV_V19_NC	V19	RSV_W12_NC	W12
RSV_W20_NC	W20	RSV_Y13_NC	Y13	S_SCLK	D18
S_SDATA	D19	SLEEP#	G2	SMI#	F3
SNIFF_CVDD	D20	SROM_CS0#	B20	SROM_CS1#	B19
SROM_SCLK	C18	SROM_SIN	C20	SROM_SOUT	C19
STPCLK#	D2	TCK	F17	TDI	E17
TDO	E18	TMS	F18	TRST#	G18
UNPROTECT	J2	VRDA0	L20	VRDA1	J19
VRDA2	K19	VRDA3	K20	VRDA4	J20

Chapter 3

Electrical Specifications

3.1 Absolute Maximum Ratings

The table below provides absolute maximum rating specifications for TM5700/TM5900 processors.

Table 24: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum
CVDD	Core voltage	-0.2 V	1.5 V
IOVDD	3.3V I/O voltage	-0.2 V	3.6 V
IOVDD25	2.5V I/O voltage	-0.2 V	3.6 V
PLLVDD	PLL voltage	-0.2 V	1.5 V
-	IOVDD, IOVDD25 relative to CVDD, PLLVDD	0.0 V	3.465 V
V_{in}	Input voltage	-0.5 V	3.96 V
I_{in}	Input current	-100 mA	100 mA
$T_{storage}$	Storage temperature	-55 °C	150 °C

3.2 Recommended Operating Conditions

This section provides recommended operating condition specifications, including processor supply voltages and temperature range for TM5700/TM5900 processors.

3.2.1 Core Voltage

The table below provides core voltage specifications for TM5700/TM5900 processors.

Table 25: Core Voltage Specifications

Symbol	Description / SKU	Core Voltage Regulator Type					
		Remote Voltage Sense [1]			Voltage Positioning [2]		
		Min	Nominal	Max	Min	Nominal	Max
CVDD [3]	**Core Voltage, Maximum LongRun Setting**						
	TM5900-1000-6.5	1.225 V	1.250 V	1.275 V	1.225 V	1.250 V	1.313 V
	TM5900-1000-7.5	1.274 V	1.300 V	1.326 V	1.274 V	1.300 V	1.365 V
	TM5900-1000-8.5	1.323 V	1.350 V	1.377 V	1.323 V	1.350 V	1.418 V
	TM5900-1000-9.5	1.372 V	1.400 V	1.428 V	1.372 V	1.400 V	1.470 V
	TM5900-933-8.5	1.323 V	1.350 V	1.377 V	1.323 V	1.350 V	1.418 V
	TM5900-800-6.6	1.225 V	1.250 V	1.275 V	1.225 V	1.250 V	1.313 V
	TM5700-667-5.0	1.127 V	1.150 V	1.173 V	1.127 V	1.150 V	1.208 V
	Core voltage, Intermediate LongRun Settings						
	All SKUs	nom-2%	nom	nom+2%	nom-2%	nom	nom+5%
	Core Voltage, Minimum LongRun Setting						
	All SKUs	0.784 V	0.800 V	0.816 V	0.784 V	0.800 V	0.840 V
	Core Voltage, DSX Mode						
	All SKUs	0.612 V	0.625 V	0.638 V	0.612 V	0.625 V	0.656 V

1. When using remote voltage sense core voltage regulators, CVDD tolerance is ±2% from DC to 1 KHz and ±5% above 1 KHz.
2. When using voltage positioning core voltage regulators, CVDD tolerance is +5/-2% from DC to 20 MHz and ±5% above 20 MHz.
3. The CVDD reference measurement point is the SNIFF_CVDD package ball (ball number AE19). The CVDD reference measurement ground is the package GND balls.

3.2.2 Other Voltages and Temperature Range

The table below provides voltage (other than core voltage) and operating temperature range specifications for TM5700/TM5900 processors.

Table 26: Other Voltage and Temperature Specifications

Symbol	Description / SKU	Minimum	Nominal	Maximum
PLLVDD [1]	PLL voltage	CVDD nom - 5%	CVDD nom	CVDD nom + 5%
IOVDD	3.3 V I/O voltage	3.135 V	3.300 V	3.465 V
IOVDD25	2.5 V I/O voltage	2.375 V	2.500 V	2.625 V
C_VREF [2]	DDR SDRAM interface voltage reference	(0.50 x IOVDD25) -1.25%	0.50 x IOVDD25	(0.50 x IOVDD25) +1.25%
V_{in}	Input voltage	GND	-	IOVDD
T_j [3]	**Junction Temperature, CoolRun80 SKUs**			
	Maximum LongRun setting	0 °C	-	80 °C
	Other LongRun settings			100 °C

1. PLLVDD DC tolerance is ±5%. The default PLLVDD configuration for TM5700/TM5900 system designs is to connect the PLLVDD signal through a ferrite bead filter to CVDD.
2. A ferrite bead noise filter is required on the C_VREF signal from the IOVDD25 resistor voltage divider to the C_VREF pin on the processor, as described in DDR Interface Reference Voltage Circuit on page 25.
3. See Package Marking Descriptions on page 84 for details on device temperature package marking identifier.

3.3 Power Supply Current

The table below provides power supply current specifications, used to size TM5700/TM5900 processor power supplies. Power supplies should be capable of providing the current specified in the table below across the full processor operating temperature range and across the full voltage tolerance range specified in Table 25 and Table 26.

Table 27: Power Supply Current Specifications

Specification		Maximum Supply Voltage [1]	Maximum Current [2]	
Symbol	**Description / SKU**		**Dynamic**	**Total**
I_{CVDD}	**Processor Core Supply (CVDD) Current**			
	TM5900-1000-6.5	CVDD = 1.313 V	6.0 A	7.5 A
	TM5900-1000-7.5	CVDD = 1.365 V		
	TM5900-1000-8.5	CVDD = 1.418 V	7.0 A	9.0 A
	TM5900-1000-9.5	CVDD = 1.470 V		
	TM5900-933-8.5	CVDD = 1.418 V	6.5 A	8.5 A
	TM5900-800-6.6	CVDD = 1.313 V	6.0 A	7.5 A
	TM5700-667-5.0	CVDD = 1.208 V		
I_{PLLVDD}	**PLL Supply (PLLVDD) Current**			
	TM5900-1000-6.5	PLLVDD = 1.313 V	-	20 mA
	TM5900-1000-7.5	PLLVDD = 1.365 V		
	TM5900-1000-8.5	PLLVDD = 1.418 V		
	TM5900-1000-9.5	PLLVDD = 1.470 V		
	TM5900-933-8.5	PLLVDD = 1.418 V		
	TM5900-800-6.6	PLLVDD = 1.313 V		
	TM5700-667-5.0	PLLVDD = 1.208 V		
$I_{IOVDD25}$	**2.5 V I/O Supply (IOVDD25) Current**			
	All SKUs	IOVDD25 = 2.625 V	-	400 mA
I_{IOVDD}	**3.3 V I/O Supply (IOVDD) Current**			
	All SKUs	IOVDD = 3.465 V	-	25 mA

1. All supplies at their maximum values.
2. Specifications apply across full operating temperature range of processor.

3.4 Thermal Design and ACPI Power

The table below provides thermal design power (TDP), used to size processor thermal solutions, and ACPI power management state power specifications for TM5700/TM5900 processors.

Table 28: Power Specifications

Specification		Test Conditions [1]			Power [1]	
Symbol	**SKU**	**Frequency**	**CVDD**	**T_j**	**Typical**	**Maximum**
TDP	**Thermal Design Power** [2]					
	TM5900-1000-6.5	1000 MHz	1.25 V	80 °C	-	6.5 W
		900 MHz	1.20 V	100 °C		
	TM5900-1000-7.5	1000 MHz	1.30 V	80 °C	-	7.5 W
		900 MHz	1.25 V	100 °C		
	TM5900-1000-8.5	1000 MHz	1.35 V	80 °C	-	8.5 W
		900 MHz	1.30 V	100 °C		
	TM5900-1000-9.5	1000 MHz	1.40 V	80 °C	-	9.5 W
		900 MHz	1.35 V	100 °C		
	TM5900-933-8.5	933 MHz	1.35 V	80 °C	-	8.5 W
		800 MHz	1.25 V	100 °C		
	TM5900-800-6.6	800 MHz	1.25 V	80 °C	-	6.6 W
		667 MHz	1.15 V	100 °C		
	TM5700-667-5.0	667 MHz	1.15 V	80 °C	-	5.0 W
		533 MHz	1.05 V	100 °C		
P_{C1}	**Auto Halt (ACPI C1) Power** [3, 7]					
	TM5900-1000-6.5	433 MHz	0.80 V	50 °C	0.35 W	-
	All other SKUs	300 MHz				
P_{C2}	**Quick Start (ACPI C2) Power** [4, 7]					
	TM5900-1000-6.5	433 MHz	0.80 V	50 °C	0.30 W	-
	All other SKUs	300 MHz				
P_{C3}	**Deep Sleep (ACPI C3) Power** [5, 7]					
	All SKUs	-	0.80 V	35 °C	0.15 W	0.40 W
P_{DSX}	**DSX Power** [6, 7]					
	All SKUs	-	0.625 V	35 °C	0.10 W	0.25 W

1. All power supplies at their nominal values. All power values are the total of core power and I/O power.
2. Thermal design power is the maximum average power dissipated over a 30 second interval while running publicly available application software at the maximum LongRun setting (for non-CoolRun80 SKUs) or at each of the top two LongRun settings (for CoolRun80 SKUs) at maximum junction temperature (T_j). Thermal design power is the recommended thermal design point and is not the absolute maximum power under worst case conditions.
3. Auto Halt (ACPI C1) is entered by executing a HLT instruction. Typical Auto Halt power is measured at the minimum LongRun setting at 50°C junction temperature.
4. Quick Start (ACPI C2) is entered by asserting STPCLK#. Typical Quick Start power is measured at the minimum LongRun setting at 50°C junction temperature.

5. Deep Sleep (ACPI C3) is entered by asserting SLEEP# and stopping CLKIN while in Quick Start. Processor clocks are stopped in Deep Sleep. Deep Sleep power is measured/specified at the minimum LongRun setting at 35°C junction temperature.
6. DSX (Extended Deep Sleep) is entered by lowering the core voltage (CVDD) to the DSX voltage when in Deep Sleep. Processor clocks are stopped in DSX. DSX power is measured/specified at the nominal DSX voltage at 35°C junction temperature.
7. Not 100% tested. These power specifications come from processor characterization at higher temperatures and extrapolating to the test conditions indicated above.

3.5 DC Specifications for I/O Signals

This section provides DC specifications for I/O signals and the thermal diode for TM5700/TM5900 processors.

Table 29: DC Specifications for All Signals Except PCI and DDR SDRAM Interfaces

Symbol	Description	Condition	Minimum	Maximum	Notes
V_{oh}	Output high voltage	I_{out} = -1 mA	2.4 V	-	
V_{ol}	Output low voltage	I_{out} = 1 mA	-	0.4 V	
V_{ih}	Input high voltage (excluding 2.5V inputs)		2.0 V	IOVDD	1
	Input high voltage for 2.5V inputs		1.7 V	IOVDD	
V_{il}	Input low voltage		-0.3 V	0.7 V	
I_{ih}	Input high leakage current	V_{in} = IOVDD	-	10 µA	2
I_{il}	Input low leakage current	V_{in} = 0 V	-	-100 µA	2
I_{ihz}	Hi-Z high leakage current	V_{in} = IOVDD	-	10 µA	2
I_{ilz}	Hi-Z low leakage current	V_{in} = 0 V	-	-10 µA	2
C_{in}	Input signal capacitance		-	10 pF	

1. The 2.5 V input signals are: CLKIN, IGNNE#, INTR, INIT#, NMI, SMI#, and STPCLK#. The 2.5 V input signals are 3.3 V tolerant.
2. Signals loaded at 2.4 pF.

Table 30: DC Specifications for DDR SDRAM Interface

Symbol	Description	Condition	Minimum	Maximum
V_{oh}	Output high voltage	I_{out} = -5.0 mA	1.85 V	-
V_{ol}	Output low voltage	I_{out} = 7.5 mA	-	0.35 V
V_{ih} [1]	Input high voltage		C_VREF + 0.18 V	IOVDD25 + 0.3 V
V_{il}	Input low voltage		-0.3 V	C_VREF - 0.18 V
I_{ih}	Input high leakage current	V_{in} = IOVDD25	-	10 µA
I_{il}	Input low leakage current	V_{in} = 0 V	-	-100 µA
C_{in}	Input signal capacitance		-	10 pF

1. The DDR SDRAM interface inputs are not 3.3 V tolerant.

Table 31: DC Specifications for PCI Interface

Symbol	Description	Condition	Minimum	Maximum
V_{oh}	Output high voltage	I_{out} = -0.5 mA	0.9 x IOVDD	-
V_{ol}	Output low voltage	I_{out} = 1.5 mA	-	0.1 x IOVDD
V_{ih}	Input high voltage (excluding P_PCLK)		0.5 x IOVDD	IOVDD + 0.5 V
	Input high voltage (P_PCLK only)		2.0 V	IOVDD + 0.5 V
V_{il}	Input low voltage (excluding P_PCLK)		-0.5 V	0.3 x IOVDD
	Input low voltage (P_PCLK only)		-0.5 V	0.8 V
I_{ih}	Input high leakage current	V_{in} = IOVDD	-	10 µA
I_{il}	Input low leakage current	V_{in} = 0 V	-	-100 µA
C_{in}	Input signal capacitance		-	10 pF

Table 32: Thermal Diode Specifications

Symbol	Description	Minimum	Typical	Maximum
V_{100} [1]	Forward biased diode drop forcing 100 µA	-	0.68 V	-
V_{10} [1]	Forward biased diode drop forcing 10 µA	-	0.62 V	-

1. V_{100} and V_{10} typical values are measured at 25°C while DIODE_CATHODE is biased at 0.7 V.

3.6 Timing Specifications for I/O Signals

This section provides AC timing specifications for clock and I/O signals for TM5700/TM5900 processors.

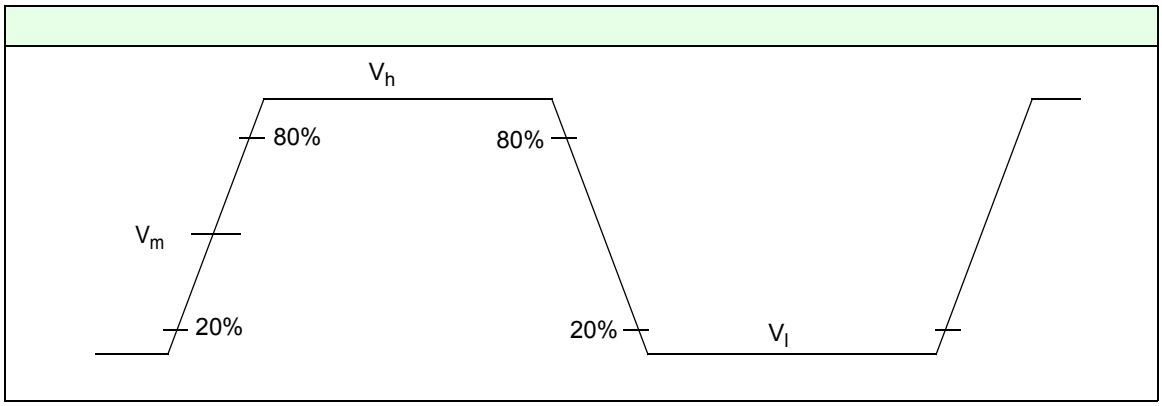
3.6.1 General AC Testing Conditions

Table 33 and Figure 12 specify the general AC test and measurement conditions. These conditions apply unless specified otherwise.

Table 33: General AC Testing Conditions

Parameter	Description	Value
V_l	3.3V input low drive level	0.4 V
	2.5V input low drive level	0.4 V
	DDR interface input low drive level	C_VREF - 0.35 V
V_h	3.3V input high drive level	2.4 V
	2.5V input high drive level	2.0 V
	DDR interface input high drive level	C_VREF + 0.35 V
V_m	3.3 V I/O timing specification measurement level	1.4 V
	2.5 V I/O timing specification measurement level	1.2 V
t_{edge}	Input signal edge rate specified between 20% and 80% of drive levels	1 V/nS

Figure 12: General AC Test and Measurement Conditions



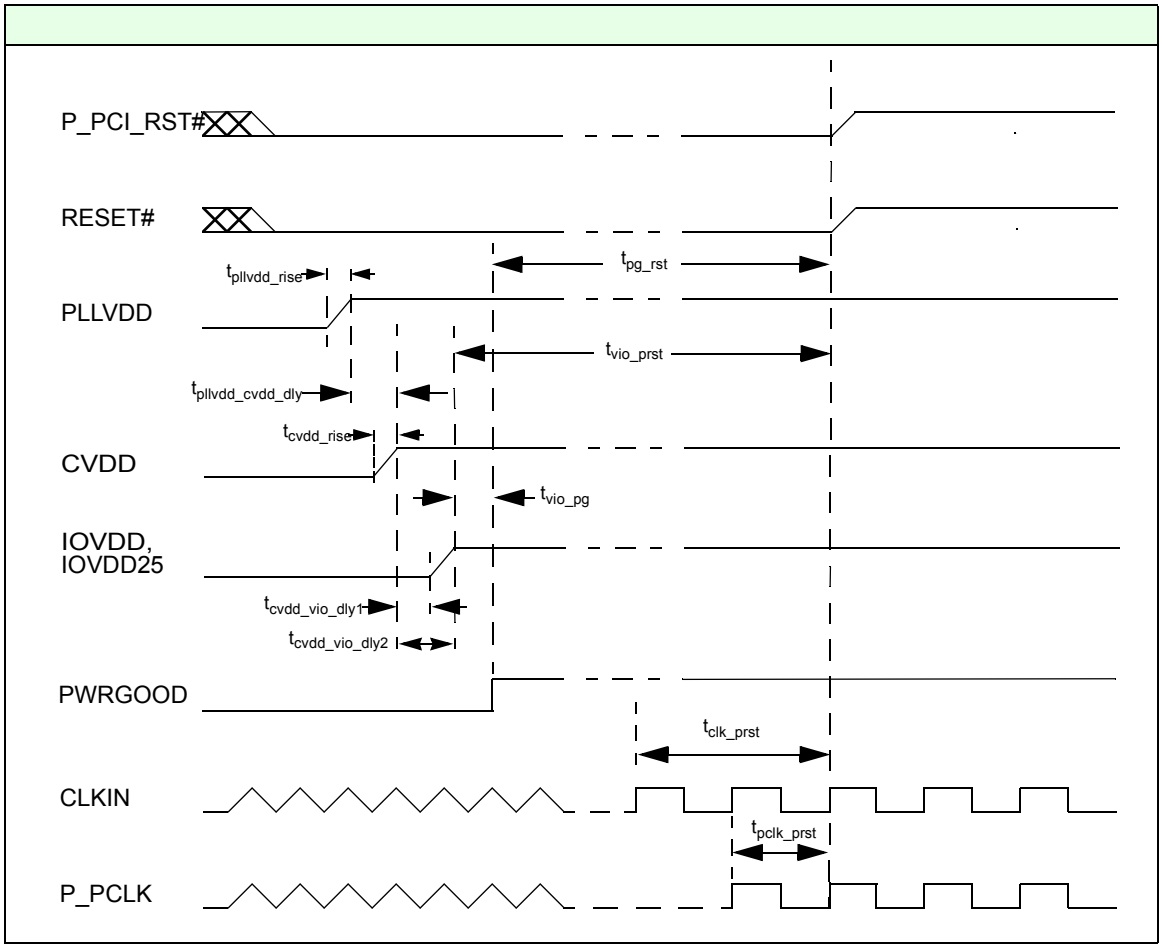
3.6.2 Power On Specifications

Table 34 and Figure 13 document the timing specifications for powering on the processor.

Table 34: Power On Specifications

Parameter	Description	Minimum	Maximum	Notes
t_{pllvdd_rise}	PLL power supply rise time	-	10 mS	
$t_{pllvdd\_cvdd\_dly}$	Required delay between PLLVDD valid and CVDD valid	-10 mS	10 mS	
t_{cvdd_rise}	Core power supply rise time	-	10 mS	
$t_{cvdd\_vio\_dly1}$	Required delay between CVDD valid and beginning of IOVDD/IOVDD25 power supply ramp-up	0 mS	<10 mS	Core supply voltage must reach minimum operating level before ramping I/O supplies to processor.
$t_{cvdd\_vio\_dly2}$	Required delay between CVDD valid and IOVDD/IOVDD25 valid	-	10 mS	
t_{vio_pg}	PWRGOOD asserted after I/O supplies reach valid operating levels	0 mS	-	P_PCI_RST# and RESET# should be active prior to PWRGOOD asserted.
t_{vio_prst}	All power supplies stable prior to P_PCI_RST# deasserted	1 mS	-	I/O supplies are last to reach valid operating levels.
t_{pg_rst}	PWRGOOD asserted to RESET#, P_PCI_RST# deasserted	1 mS	-	
t_{pclk_prst}	P_PCLK stable prior to P_PCI_RST# deasserted	100 µS	-	
t_{clk_prst}	CLKIN stable prior to P_PCI_RST# deasserted	1 mS	-	
t_{prst_rst}	P_PCI_RST# deasserted to RESET# deasserted	0 mS	-	
t_{pg_low}	PWRGOOD inactive pulse width	10 CLKINs	-	

Figure 13: Power On Timing



3.6.3 Input Clocks

Table 35, Table 36, and Figure 14 document the timing specifications for the processor input clocks.

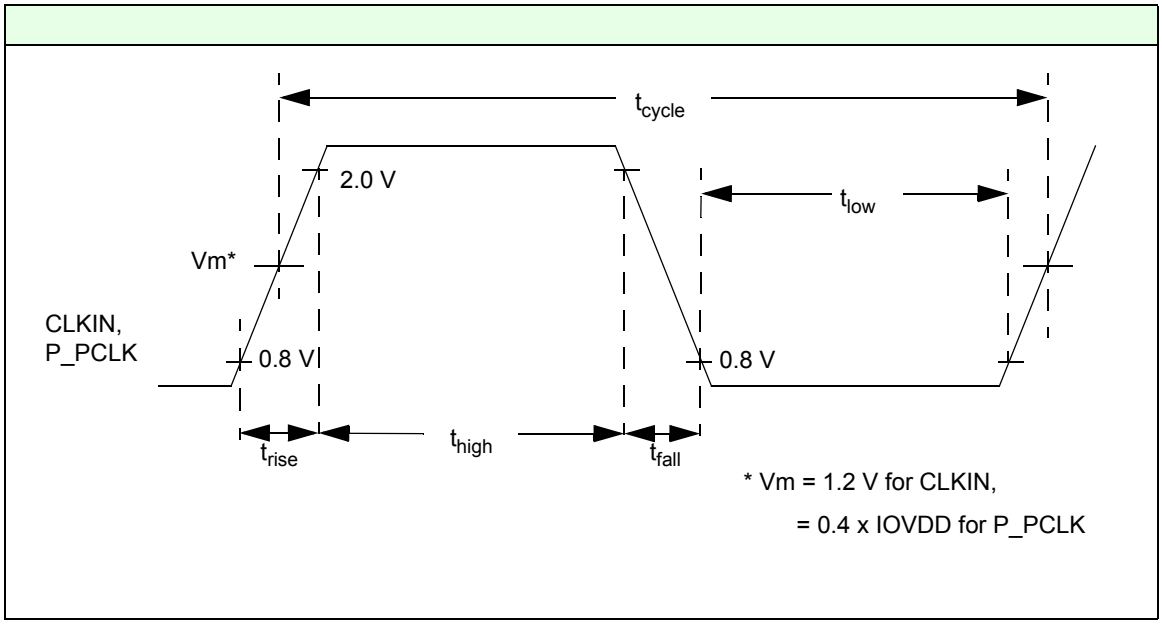
Table 35: Timing Specifications for Input Clocks

Parameter	Minimum	Maximum	Notes
f_{clk} (clock frequency)			
CLKIN	60.0 MHz	66.67 MHz	Clocks may be stopped. Not 100% tested. Guaranteed by design/characterization.
P_PCLK	30.0 MHz	33.33 MHz	
t_{cycle} (clock period)			
CLKIN	15.0 nS	16.67 nS	
P_PCLK	30 nS	-	
t_{high} (clock high time)			
CLKIN	5.2 nS	-	Not 100% tested. Guaranteed by design/characterization.
P_PCLK	11 nS	-	
t_{low} (clock low time)			
CLKIN	5.0 nS	-	Not 100% tested. Guaranteed by design/characterization.
P_PCLK	11 nS	-	
t_{jitter} (clock jitter)			
CLKIN	-	250 pS	See Table 36 below for CLKIN spread spectrum specifications.
P_PCLK	-	500 pS	
$t_{rise/fall}$ (clock rise and fall time)			
CLKIN	0.4 nS	1.6 nS	
P_PCLK	1.0 V/nS	4.0 V/nS	
t_{offset} (CLKIN to P_PCLK offset)	1.5 nS	4.0 nS	
t_{pll_lock} (PLL relock time)	-	20 µS	

Table 36: CLKIN Spread Spectrum Clock Specifications

Description	Minimum	Nominal	Maximum
CLKIN spread spectrum input frequency	-	66.67 MHz	-
CLKIN spread spectrum upspread	-	-	0.0 %
CLKIN spread spectrum downspread	-0.6 %	-	-
CLKIN spread spectrum modulation frequency	-	-	30 KHz
CLKIN spread spectrum clock jitter	-	-	250 pS

Figure 14: Timing Specifications for Input Clocks



3.6.4 DDR SDRAM Interface

Table 37, Table 38, and Table 39, along with Figure 15 and Figure 16 document the timing specifications for the processor DDR SDRAM interface.

Table 37: Timing Specifications for DDR SDRAM Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	C_CLK frequency	-	133 MHz	
t_{cycle}	C_CLK period	7.5 nS	-	1
t_{low}, t_{high}	C_CLK low time, high time	0.45 bus clks	0.55 bus clks	1
t_{jitter}	C_CLK jitter	-	150 pS	1
V_x	Differential cross pt. voltage	1.1 V	1.4 V	1
t_{valid}	C_DQS output valid delay	0.75 bus clks	1.25 bus clks	2,4
t_{valid}	Output valid delay: Data signals CMD signals	 - -	 see Table 38 see Table 39	2,3,4
t_{ohold}	Output hold time: Data signals CMD signals	 see Table 38 see Table 39	 - -	2,3,4
t_{valid_dqs}	C_DQ, C_DQMB valid from C_DQS (writes)	-	3.05 nS	
t_{ohold_dqs}	C_DQ, C_DQMB hold from C_DQS (writes)	0.76 nS	-	
t_{dqs_skew}	C_DQS to C_DQ, C_DQMB skew	-0.76 nS	+0.76 nS	
t_{dqs_low}, t_{dqs_high}	C_DQS input low time, C_DQS input high time	0.45 bus clks	0.55 bus clks	
$t_{dqs\_preamble}$	C_DQS preamble valid time	0.9 bus clks	1.1 bus clks	
t_{off}	Active to float delay C_DQ C_DQS	 0 nS -0.5 nS	 2.5 nS +0.5 nS	2
n_{ras_cas}	C_RAS# to C_CAS# latency	1 bus clock	16 bus clocks	5
n_{cas_read}	C_CAS# to read latency	1 bus clock	16 bus clocks	5
n_{read_pchg}	Read precharge delay	1 bus clock	16 bus clocks	5
n_{wr_pchg}	Write precharge delay	1 bus clock	16 bus clocks	5
n_{row_pchg}	Row precharge time	1 bus clock	16 bus clocks	5,6
n_{idmrs}	Idle cycles after Mode Register Set (MRS) operation	2 bus clocks	17 bus clocks	5
n_{ras_ras}	Row cycle time	2 bus clocks	17 bus clocks	5,7
n_{burst}	Burst length	4 transfers	4 transfers	8
$n_{refresh}$	Refresh rate	128 bus clocks	16k bus clocks	5

1. Clock specifications apply to C_CLKA, C_CLKA#, C_CLKB, C_CLKB#. C_CLKA and C_CLKA# are 180° out of phase. C_CLKB and C_CLKB# are 180° out of phase. C_CLKA and C_CLKB are copies of each other.

2. The data parameters are specified relative to DQS signals and CMD parameters are specified relative to C_CLK/C_CLK# differential cross point voltage.
3. CMD signals are: C_A[12:0], C_BA[1:0], C_CAS#, C_CKE[1:0], C_CS[3:0]#, C_RAS#, C_WE#.
4. Assumes 80 pF maximum load on each CMD signal and 10 pF maximum load on each of C_DQ[63:0].
5. These parameters are programmable within the processor.
6. Row precharge time is the number of bus clocks between the power on precharge and the next time RAS can be asserted.
7. Row cycle time is the number of bus clocks between refresh and the next time RAS can be asserted for other SDRAM operations. This also is the number of cycles the DDR SDRAM controller waits before starting any SDRAM access after it exits clock off mode.
8. The DDR SDRAM controller always performs burst operations.

Table 38 provides the DDR SDRAM interface output hold time (t_{ohold}) minimum timing and output valid delay (t_{valid}) maximum timing specifications for the data signals (relative to the DQS signals) for each processor SKU and LongRun step. Refer to *TM5700/TM5900 Development and Manufacturing Guide* for additional information on memory configuration.

Table 38: t_{ohold} and t_{valid} Timing for DDR SDRAM Data Signals

Processor			DDR Interface / DDR266-CL2.5 Memory		
	Core		Mclk	t_{ohold} (min)	t_{valid} (max)
SKU	MHz	V	MHz	nS	nS
TM5900-1000-6.5	1000	1.250	125	0.75	1.82
	900	1.200	129	0.75	1.82
	800	1.100	133	0.75	1.82
	667	1.000	133	0.75	1.75
	567	0.900	113	0.75	1.75
	433	0.800	108	0.75	1.75
TM5900-1000-7.5	1000	1.300	125	0.75	1.82
	900	1.250	129	0.75	1.82
	800	1.150	133	0.75	1.82
	667	1.050	133	0.75	1.75
	533	0.950	133	0.75	1.75
	433	0.875	108	0.75	1.75
	300	0.800	100	0.75	1.62
TM5900-1000-8.5	1000	1.350	125	0.75	1.82
	900	1.300	129	0.75	1.82
	800	1.200	133	0.75	1.82
	667	1.100	133	0.75	1.75
	533	1.000	133	0.75	1.75
	433	0.925	108	0.75	1.75
	300	0.800	100	0.75	1.62

Table 38: t_{ohold} and t_{valid} Timing for DDR SDRAM Data Signals (Continued)

Processor			DDR Interface / DDR266-CL2.5 Memory		
	Core		Mclk	t_{ohold} (min)	t_{valid} (max)
SKU	MHz	V	MHz	nS	nS
TM5900-1000-9.5	1000	1.400	125	0.75	1.82
	900	1.350	129	0.75	1.82
	800	1.250	133	0.75	1.82
	667	1.150	133	0.75	1.75
	533	1.050	133	0.75	1.75
	433	0.950	108	0.75	1.75
	300	0.800	100	0.75	1.62
TM5900-933-8.5	933	1.350	133	0.75	1.82
	800	1.250	133	0.75	1.82
	667	1.150	133	0.75	1.75
	533	1.050	133	0.75	1.75
	433	0.950	108	0.75	1.75
	300	0.800	100	0.75	1.62
TM5900-800-6.6	800	1.250	133	0.75	1.82
	667	1.150	133	0.75	1.75
	533	1.050	133	0.75	1.75
	433	0.950	108	0.75	1.75
	300	0.800	100	0.75	1.62
TM5700-667-5.0	667	1.150	133	0.75	1.75
	533	1.050	133	0.75	1.75
	433	0.950	108	0.75	1.75
	300	0.800	100	0.75	1.62

Table 39 provides the DDR SDRAM interface output hold time (t_{ohold}) minimum timing and output valid delay (t_{valid}) maximum timing specifications for the CMD signals (relative to the clock signals) for each processor SKU and LongRun step. Refer to *TM5700/TM5900 Development and Manufacturing Guide* for additional information on memory configuration.

Table 39: t_{ohold} and t_{valid} Timing for DDR SDRAM CMD Signals

Processor			DDR Interface / DDR266-CL2.5 Memory		
	Core		Mclk	t_{ohold} (min)	t_{valid} (max)
SKU	MHz	V	MHz	nS	nS
TM5900-1000-6.5	1000	1.250	125	1.60	3.30
	900	1.200	129	1.85	3.50
	800	1.100	133	2.10	4.10
	667	1.000	133	1.60	4.30
	567	0.900	113	2.20	4.80
	433	0.800	108	2.50	5.90
TM5900-1000-7.5	1000	1.300	125	1.60	3.30
	900	1.250	129	1.85	3.50
	800	1.150	133	2.10	4.10
	667	1.050	133	1.60	4.30
	533	0.950	133	2.20	4.80
	433	0.875	108	2.50	5.90
	300	0.800	100	2.40	5.80
TM5900-1000-8.5	1000	1.350	125	1.60	3.30
	900	1.300	129	1.85	3.50
	800	1.200	133	2.10	4.10
	667	1.100	133	1.60	4.30
	533	1.000	133	2.20	4.80
	433	0.925	108	2.50	5.90
	300	0.800	100	2.40	5.80
TM5900-1000-9.5	1000	1.400	125	1.60	3.30
	900	1.350	129	1.85	3.50
	800	1.250	133	2.10	4.10
	667	1.150	133	1.60	4.30
	533	1.050	133	2.20	4.80
	433	0.950	108	2.50	5.90
	300	0.800	100	2.40	5.80
TM5900-933-8.5	933	1.350	133	1.85	3.50
	800	1.250	133	2.10	4.10
	667	1.150	133	1.60	4.30
	533	1.050	133	2.20	4.80
	433	0.950	108	2.50	5.90
	300	0.800	100	2.40	5.80

Table 39: t_{ohold} and t_{valid} Timing for DDR SDRAM CMD Signals (Continued)

Processor			DDR Interface / DDR266-CL2.5 Memory		
	Core		Mclk	t_{ohold} (min)	t_{valid} (max)
SKU	MHz	V	MHz	nS	nS
TM5900-800-6.6	800	1.250	133	2.10	4.10
	667	1.150	133	1.60	4.30
	533	1.050	133	2.20	4.80
	433	0.950	108	2.50	5.90
	300	0.800	100	2.40	5.80
TM5700-667-5.0	667	1.150	133	1.60	4.30
	533	1.050	133	2.20	4.80
	433	0.950	108	2.50	5.90
	300	0.800	100	2.40	5.80

Figure 15: Timing Specifications for DDR SDRAM Interface - Read Cycle

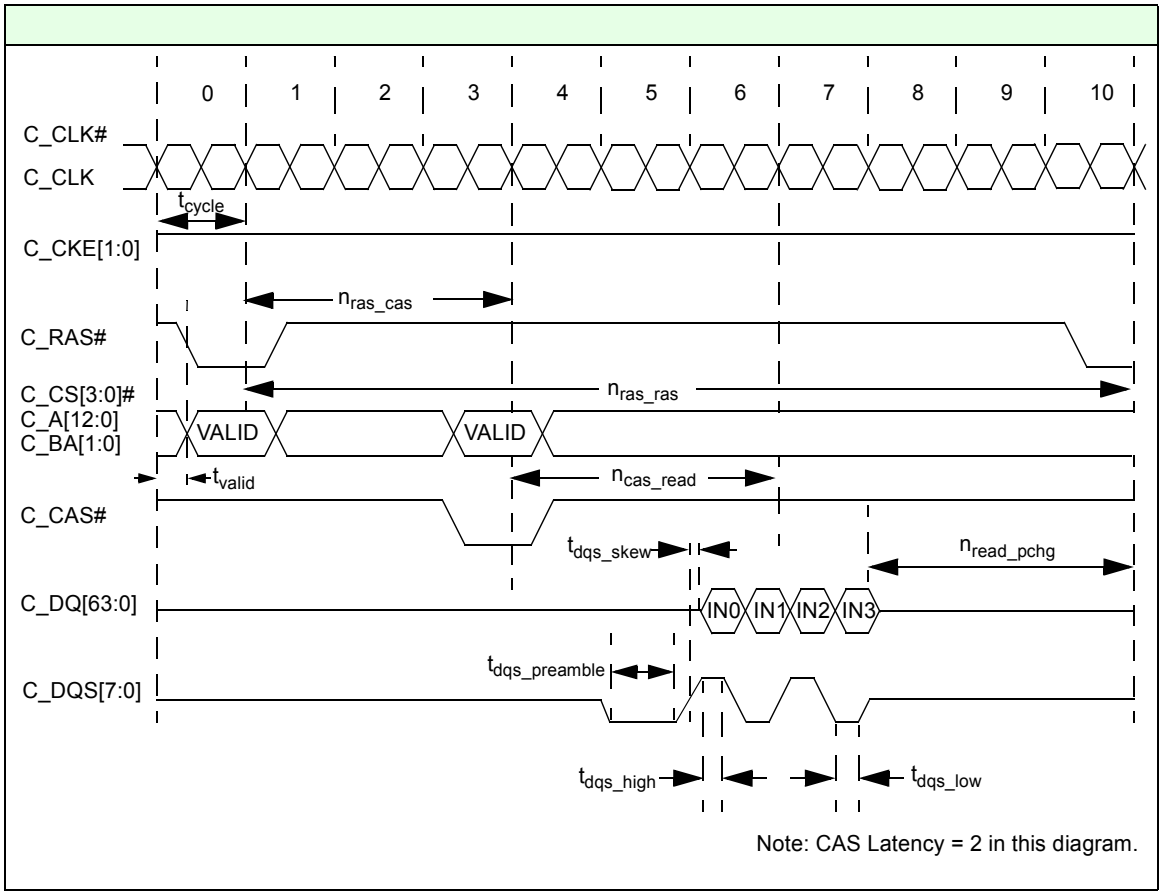
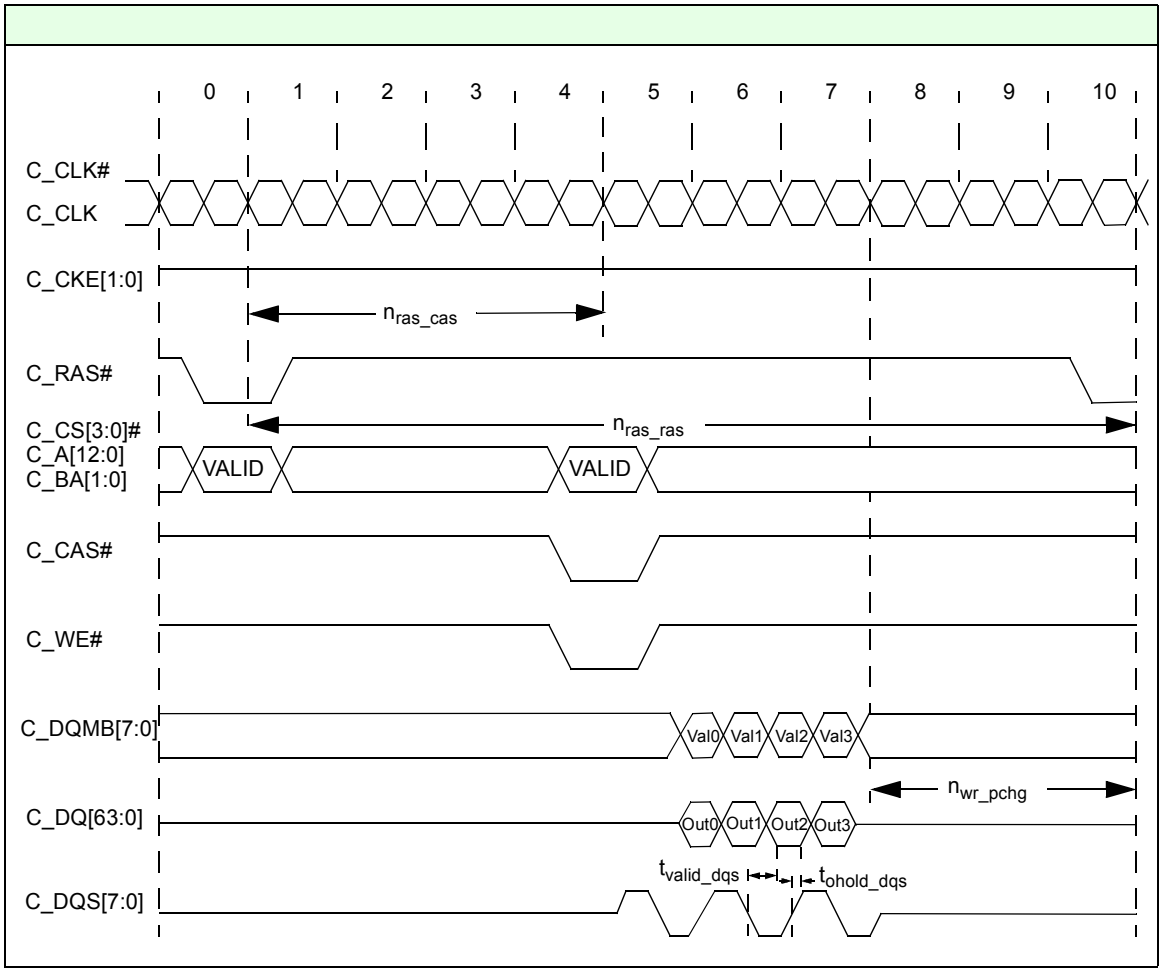


Figure 16: Timing Specifications for DDR SDRAM Interface - Write Cycle



3.6.5 PCI Interface

Table 40 documents the timing specifications for the processor PCI interface. The PCI interface is compliant with revision 2.1 of the PCI Local Bus Specification. Refer to the PCI specification for additional information.

Table 40: Timing Specifications for PCI Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	P_PCLK frequency	30.0 MHz	33.33 MHz	
t_{setup}	Input setup time			
	P_REQ[5:0]#	12 nS	-	1, 2
	All other inputs	7 nS	-	
t_{ihold}	Input hold time	0 nS	-	1, 2
t_{valid}	Output valid delay			
	P_GNT[5:0]#	2 nS	12 nS	1, 3
	All other outputs	2 nS	11 nS	
t_{off}	Active to float delay	-	28 nS	
t_{rst_off}	P_PCI_RST# asserted to output float delay	-	40 nS	

1. These parameters are specified relative to P_PCLK rising edge at 0.4*IOVDD level.
2. Input signals are: P_AD[31:0], P_CBE[3:0]#, P_CLKRUN#, P_DEVSEL#, P_FRAME#, P_HOLD#, P_IRDY#, P_LOCK#, P_PAR, P_PCI_RST#, P_PERR#, P_REQ[5:0]#, P_SERR#, P_STOP#, P_TRDY#.
3. Output signals are: P_AD[31:0], P_CBE[3:0]#, P_CLKRUN#, P_DEVSEL#, P_FRAME#, P_GNT[5:0]#, P_HLDA#, P_IRDY#, P_LOCK#, P_PAR, P_PERR#, P_STOP#, P_TRDY#.

3.6.6 Southbridge Sidebands and Power Management Interface

IGNNE#, INIT#, INTR, NMI, PWRGOOD, SLEEP#, SMI# and STPCLK# are asynchronous input signals. Therefore, these inputs are not required to meet any setup and hold specifications.

3.6.7 Debug Interface

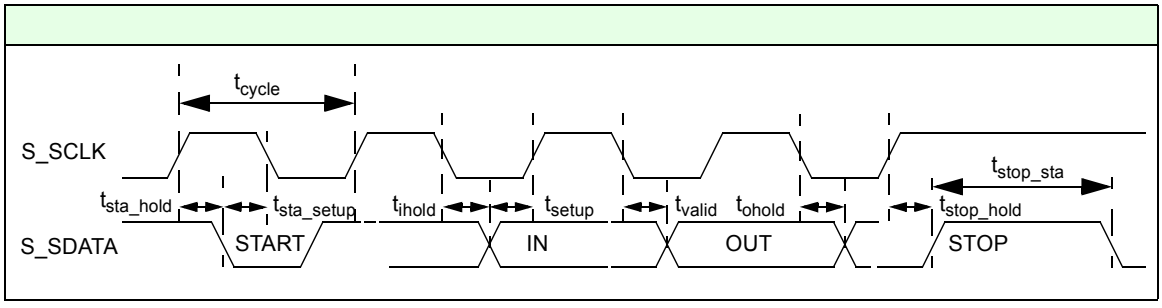
Table 41 and Figure 17 document the timing specifications for the processor debug serial interface.

Table 41: Timing Specifications for Debug Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	S_SCLK frequency	0	400 KHz	1
t_{cycle}	S_SCLK period	2.5 µS	-	
t_{high}	S_SCLK high time	600 nS	-	1
t_{low}	S_SCLK low time	1.3 µS	-	1
t_{rise}	S_SCLK, S_SDATA rise time	-	1 µS	2
t_{fall}	S_SCLK, S_SDATA fall time	-	300 nS	2
t_{stop_sta}	Bus free to new transaction	1.3 µS	-	
t_{sta_setup}	Start condition setup time	600 nS	-	3, 4
t_{sta_hold}	Start condition hold time	600 nS	-	3, 5
t_{stop_hold}	Stop condition setup time	600 nS	-	4, 6
t_{setup}	S_SDATA input setup time	100 nS	-	4
t_{ihold}	S_SDATA input hold time	0 nS	-	5
t_{valid}	S_SDATA output valid delay	-	350 nS	5
t_{ohold}	S_SDATA output hold time	250 nS	-	5

1. Not 100% tested. Guaranteed by design/characterization.
2. Rise and fall times are specified from 20% to 80%.
3. Start condition occurs when S_SDATA transitions from high to low while S_SCLK is high.
4. specified relative to S_SCLK rising edge at 1.5 V level. Assumed loading is 400 pF.
5. specified relative to S_SCLK falling edge at 1.5 V level. Assumed loading is 400 pF.
6. Stop condition occurs when S_SDATA transitions from low to high while S_SCLK is high.

Figure 17: Timing Specifications for Debug Interface



3.6.8 Code Morphing Software Boot ROM Interface

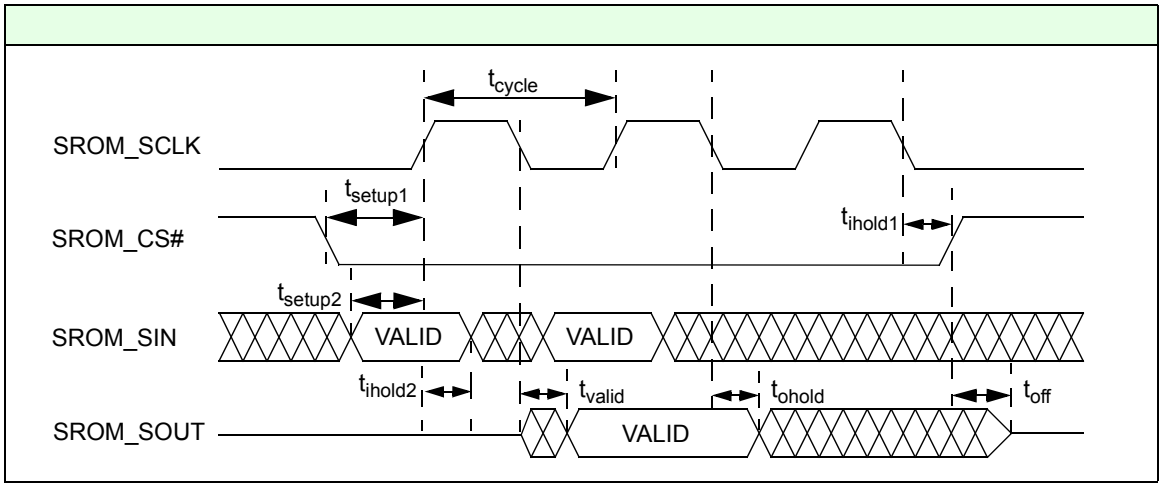
Table 42 and Figure 18 document the timing specifications for the processor Code Morphing software boot ROM serial interface.

Table 42: Code Morphing Software Boot ROM Interface Timing

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	SROM_SCLK frequency	-	11 MHz	
t_{cycle}	SROM_SCLK period	90 nS	-	
t_{high}	SROM_SCLK high time	40 nS	-	
t_{low}	SROM_SCLK low time	40 nS	-	
t_{setup1}	SROM_CS# input setup time	350 nS	-	1
t_{ihold1}	SROM_CS# input hold time	350 nS	-	2
t_{cs_high}	SROM_CS# high time	100 nS	-	
t_{setup2}	SROM_SIN input setup time	20 nS	-	1
t_{ihold2}	SROM_SIN input hold time	0 nS	-	1
t_{valid}	SROM_SOUT output valid delay	-	85 nS	2
t_{ohold}	SROM_SOUT output hold time	35 nS	-	2
t_{off}	SROM_SOUT active to float delay	-	100 nS	

1. These conditions are specified relative to SROM_SCLK rising edge at 1.4 V level.
2. These conditions are specified relative to SROM_SCLK falling edge at 1.4 V level.

Figure 18: Code Morphing Software Boot ROM Interface Timing



3.6.9 Configuration (Mode-bit) ROM Interface

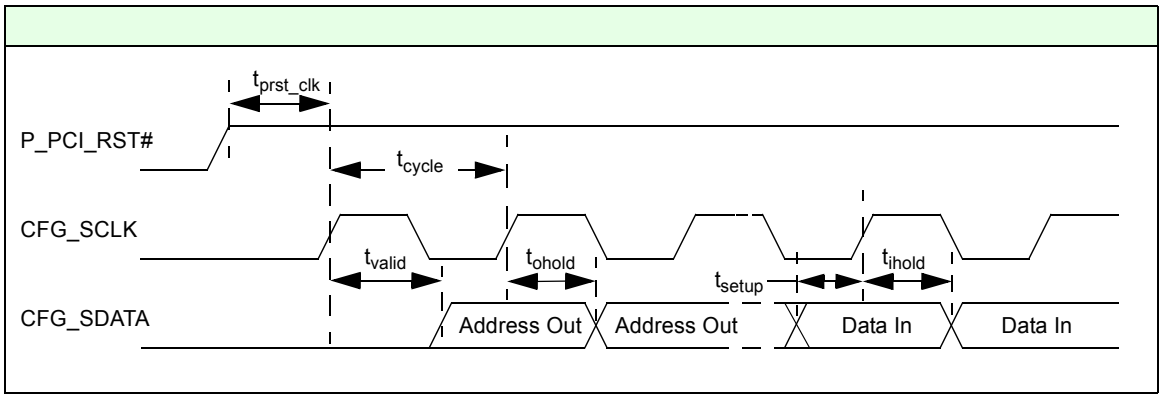
Table 43 and Figure 19 document the timing specifications for the processor configuration (mode-bit) ROM interface.

Table 43: Timing Specifications for Configuration ROM Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	CFG_SCLK frequency	-	2 MHz	
t_{cycle}	CFG_SCLK clock period	0.5 mS	2 mS	1
t_{high}	CFG_SCLK high time	250 nS	-	
t_{low}	CFG_SCLK low time	250 nS	-	
t_{prst_clk}	P_PCI_RST# to CFG_SCLK active high	100 nS	-	
t_{setup}	CFG_SDATA input setup time	600 nS	-	2
t_{ihold}	CFG_SDATA input hold time	0 S	-	2
t_{valid}	CFG_SDATA output valid delay	-	900 nS	2
t_{ohold}	CFG_SDATA output hold time	100 nS	-	2

1. CFG_SCLK period is CLKIN period × 72. For 66 MHz CLKIN, CFG_SCLK period is 1.08 mS.
2. These parameters are specified relative to CFG_SCLK rising edge at 1.4 V level.

Figure 19: Timing Specifications for Configuration ROM Interface



3.6.10 JTAG Interface

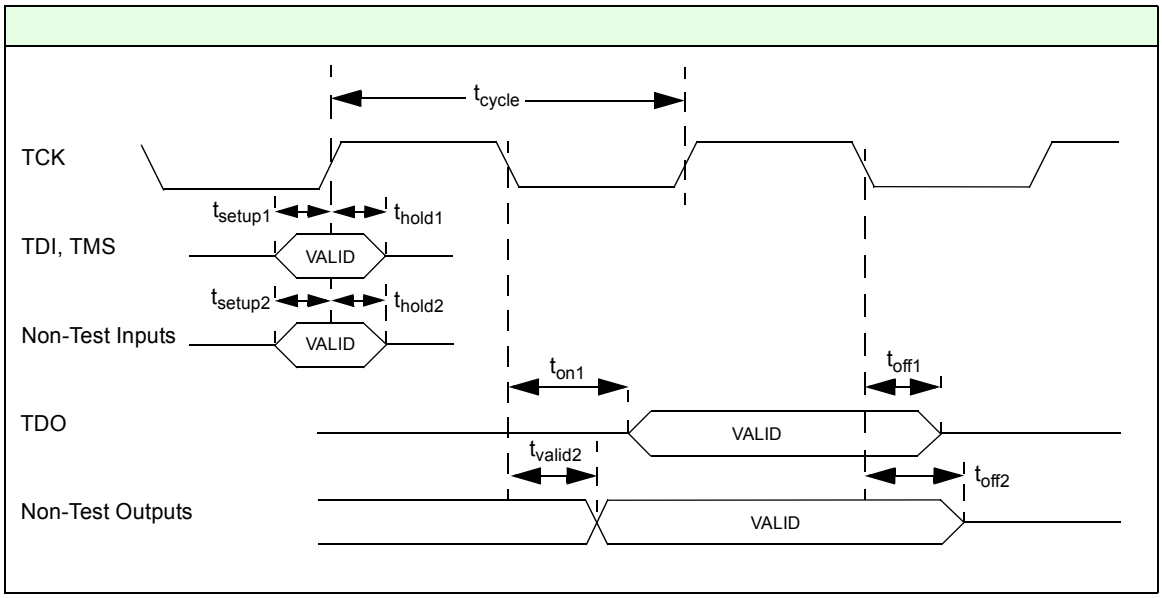
Table 44 and Figure 20 document the timing specifications for the processor JTAG interface. TRST# is an asynchronous signal. Therefore there is no setup or hold time specified for TRST# in Table 44.

Table 44: Timing Specifications for JTAG Interface

Parameter	Description	Minimum	Maximum	Notes
f_{clk}	TCK frequency		50 MHz	
t_{cycle}	TCK clock period	20 nS	-	
t_{low}	TCK low time	8 nS	-	
t_{high}	TCK high time	8 nS	-	
t_{rise}	TCK rise time	-	2 nS	
t_{fall}	TCK fall time	-	2 nS	
t_{reset}	TRST# pulse width	200 nS	-	
t_{setup1}	TDI, TMS input setup time	10 nS	-	1
t_{hold1}	TDI, TMS input hold time	10 nS	-	1
t_{on1}	TDO float to active delay	5 nS	10 nS	2
t_{off1}	TDO active to float delay	-	10 nS	2
t_{setup2}	Non-test inputs setup time	10 nS	-	1
t_{hold2}	Non-test inputs hold time	-	10 nS	1
t_{valid2}	Non-test outputs valid delay	-	10 nS	2
t_{off2}	Non-test outputs active to float delay	-	20 nS	2

1. These parameters are specified relative to TCK rising edge at 1.4 V level.
2. These parameters are specified relative to TCK falling edge at 1.4 V level.

Figure 20: Timing Specifications for JTAG Interface



Chapter 4

Package Specifications

The TM5700/TM5900 processor is packaged in a 21 mm x 21 mm 399-contact flip-chip organic ball grid array (FC-OBGA). This chapter provides information on the TM5700/TM5900 processor package, including thermal and mechanical specifications, a package mechanical drawing, and package marking specifications.

4.1 Package Thermal Specifications

The table below provides the processor package thermal specifications. For detailed information on processor thermal characteristics and thermal solution design, refer to the *TM5700/TM5900 Thermal Design Guide*.

Table 45: Package Thermal Specifications

Symbol	Description	Minimum	Maximum
T_j	Junction temperature, maximum LongRun setting	0 °C	80°C
	Junction temperature, other LongRun settings		100°C
θ_{ja}	Junction-to-ambient thermal resistance, 0 m/s airflow	-	18.8°C/W
	Junction-to-ambient thermal resistance, 1 m/s airflow	-	17.2°C/W
	Junction-to-ambient thermal resistance, 2 m/s airflow	-	15.4°C/W
θ_{jp}	Junction-to-package top (exposed silicon die) thermal resistance	-	0.093°C/W
θ_{jb}	Junction-to-PCB (through solder balls) thermal resistance	-	11.9°C/W

4.2 Package Mechanical Specifications

The table below provides the processor package mechanical specifications.

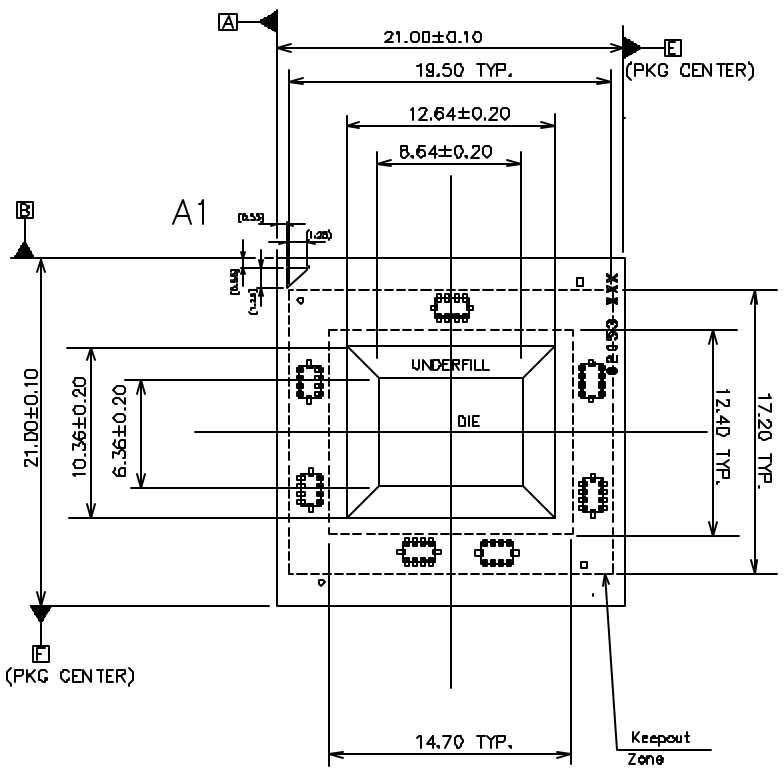
Table 46: Package Mechanical Specifications

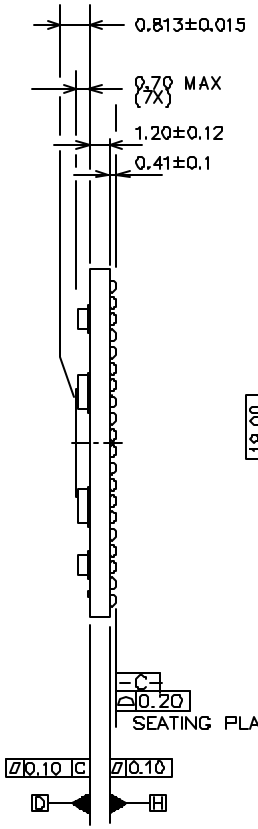
JEDEC Symbol	Description	Nominal	Tolerance	Maximum
A	Height of package top (exposed die) above PCB surface (prior to board mount)	2.42 mm	-	-
A1	Solder ball standoff height (prior to board mount)	0.41 mm	± 0.10 mm	-
e	Ball pitch (distance from ball center-to-ball center of adjacent balls)	1.00 mm BASIC	-	-
fff	Ball pitch tolerance (with respect to adjacent ball)	-	± 0.10 mm	-
	Heatsink attach pressure, centered, normal to package top	-	-	100 PSI 690 kPa
M_p	Mass of package	2.25 g	-	-
ddd	Coplanarity	-	-	0.20 mm

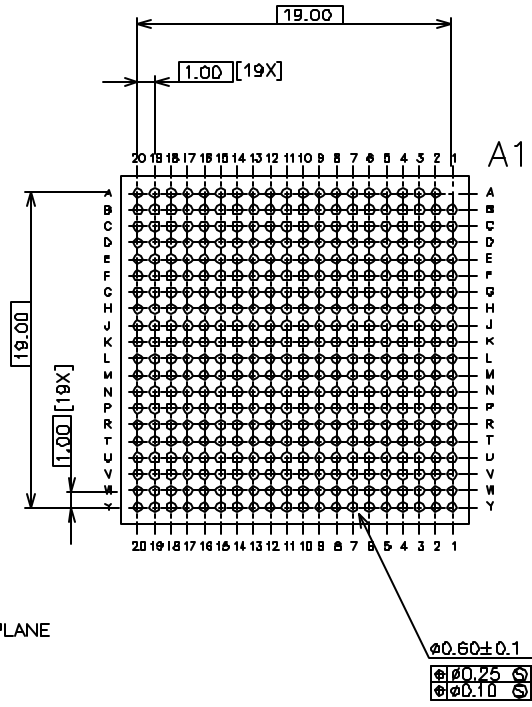
4.3 Package Drawing

A mechanical drawing of the processor package is shown on the following page.

REVISIONS/ENGINEERING CHANGE ORDER				
REV	ECO #	DESCRIPTION	DATE	BY
–	–	PRELIM.–ROTATE DIE. UPD DIE THKNESS.	06/06/03	
–	–	PRELIM.– UPDATED BALL DIMENSIONS	06/11/03	







NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. SOLDER BALL COMPOSITION: 37% Pb/63% Sn.
3. SOLDER BALL COPLANARITY : 0.20 mm MAX.
4. SUBSTRATE BASE MATERIAL: BT
5. PART NUMBER AND PANEL LOCATION NUMBER IS LOCATED ON TOP METAL LAYER AND DEFINED BY OPENINGS IN THE SOLDER RESIST.
6. LOCATION AND QUANTITY OF CAPACITORS IS PRELIMINARY

CONFIDENTIAL

Transmeta Corporation

3940 FREEDOM CIRCLE SANTA CLARA, CALIFORNIA 95054

		TITLE: 21mm x 21 mm – 399 OBGA	
TOLERANCES UNLESS NOTED		SCALE: NONE	PART NUMBER:
LINEAR ±	±0.020	THIRD ANGLE PROJECTION	SHEET: 1 OF 1
ANGLES ±	0° 30'		DESIGNER: Transmeta
RADII UNLESS NOTED			CHECKED BY: GB
EDGE/CORNER BREAKS: OUTSIDE MAX			APPROVED: GB
EDGE/CORNER BREAKS: INSIDE MAX			ACAD #:

4.4 Package Marking

Figure 21 shows the location of the processor package markings, and Table 47 explains the part model, voltage, temperature, frequency, version identifier (5xVFFFFRR) and other package marking fields.

Figure 21: Package Marking Locations - Top View

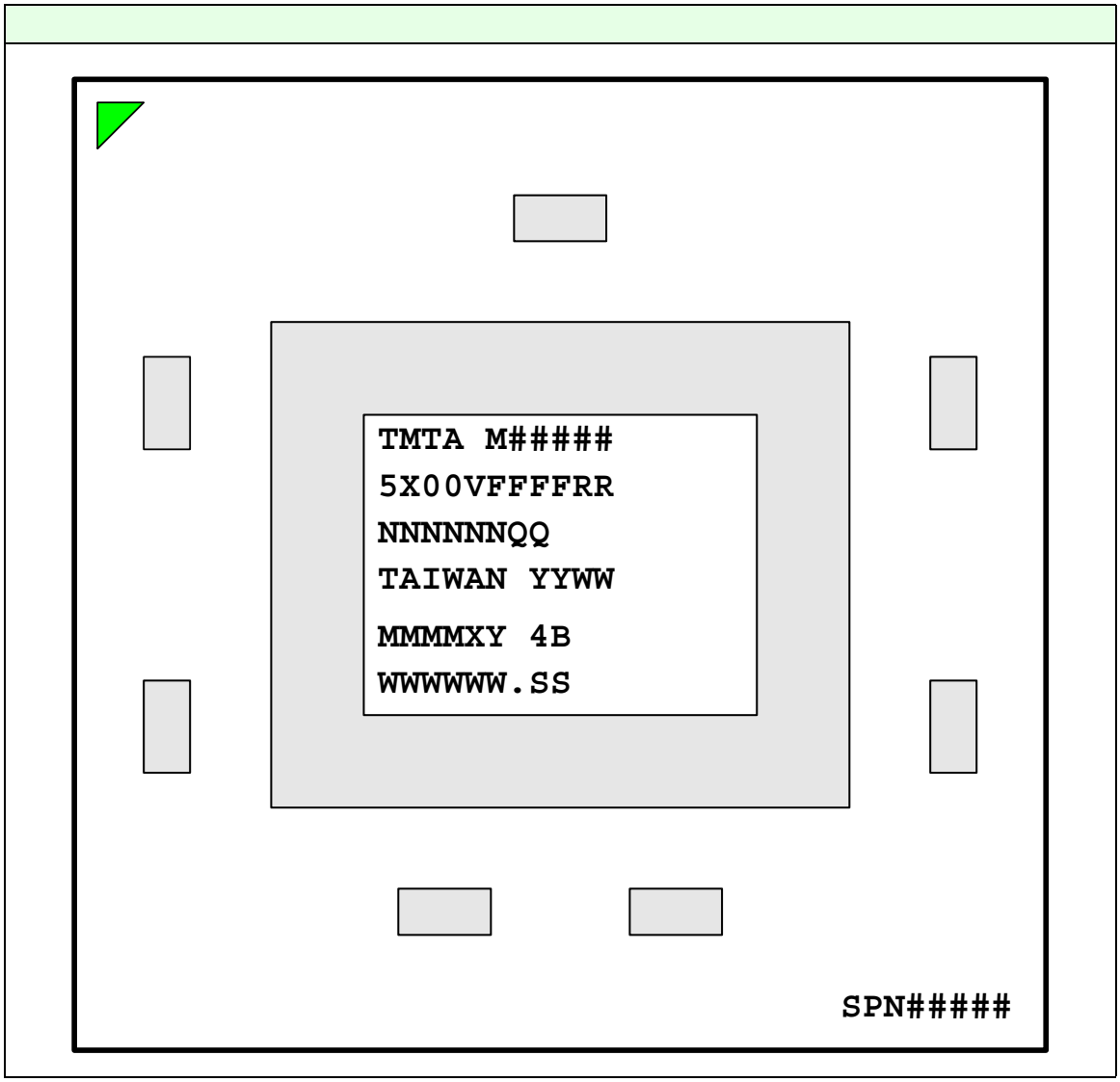


Table 47: Package Marking Descriptions

Field	Description	
5x00VFFFFRR	Model number, voltage, temperature, frequency, and version identifier:	
	5x00	Model number: 5700 = Model TM5700 5900 = Model TM5900
	V	Operating voltage range and temperature: A = 0.80-1.25 V 80/100 °C (CoolRun80) B = 0.80-1.30 V 80/100 °C (CoolRun80) C = 0.80-1.35 V 80/100 °C (CoolRun80) D = 0.80-1.40 V 80/100 °C (CoolRun80) E = 0.80-1.15 V 80/100 °C (CoolRun80)
	FFFF	Operating frequency (MHz): 1000 0933 0800 0667
	RR	Silicon version identifier: 10 = Version 1.0
TMTA M#####	Transmeta identifier and tracking number:	
	TMTA	Transmeta identifier
	M#####	Tracking number
NNNNNNQQ	Transmeta tracking number and quality indicator:	
	NNNNNN	Transmeta tracking number
	QQ	Quality indicator: MS = Mechanical sample ES = Engineering sample Blank = Production level
TAIWAN YYWW	Country of final assembly and date code:	
	TAIWAN	Country of final assembly
	Date code:	
	YY	Year
	WW	Work week
SPN#####	Substrate part number	
MMMMXY 4B **WWWWWW.SS**	Transmeta tracking numbers	