

PLL\_VDD, 1V Minimum Clamping Circuit

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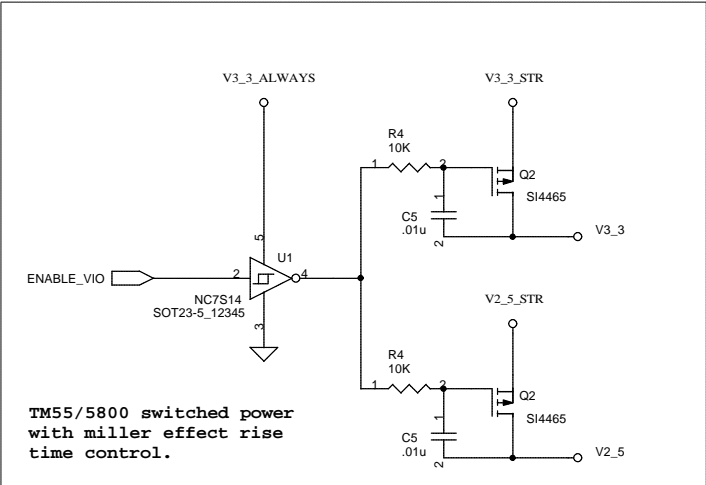
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### Voltage Sequence Option 1 - Delayed

**Note:** Make sure that delay ( $C2 + R1 + R3$ ) is long enough to ensure that V3\_3 and V2\_5 are in regulation before FORCE\_STARTUP\_V goes low.

**See note below**



### Voltage Sequence Option 2- VI/O Monitoring

Voltage Trip Point

V2_5	2.25V
V3_3	3.10V

See note below

**NOTE:**  
Use either Voltage Sequence, Option 1 or Option 2, to generate the "FORCE\_STARTUP\_V" signal. Do not use both.

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Page 1 of 1