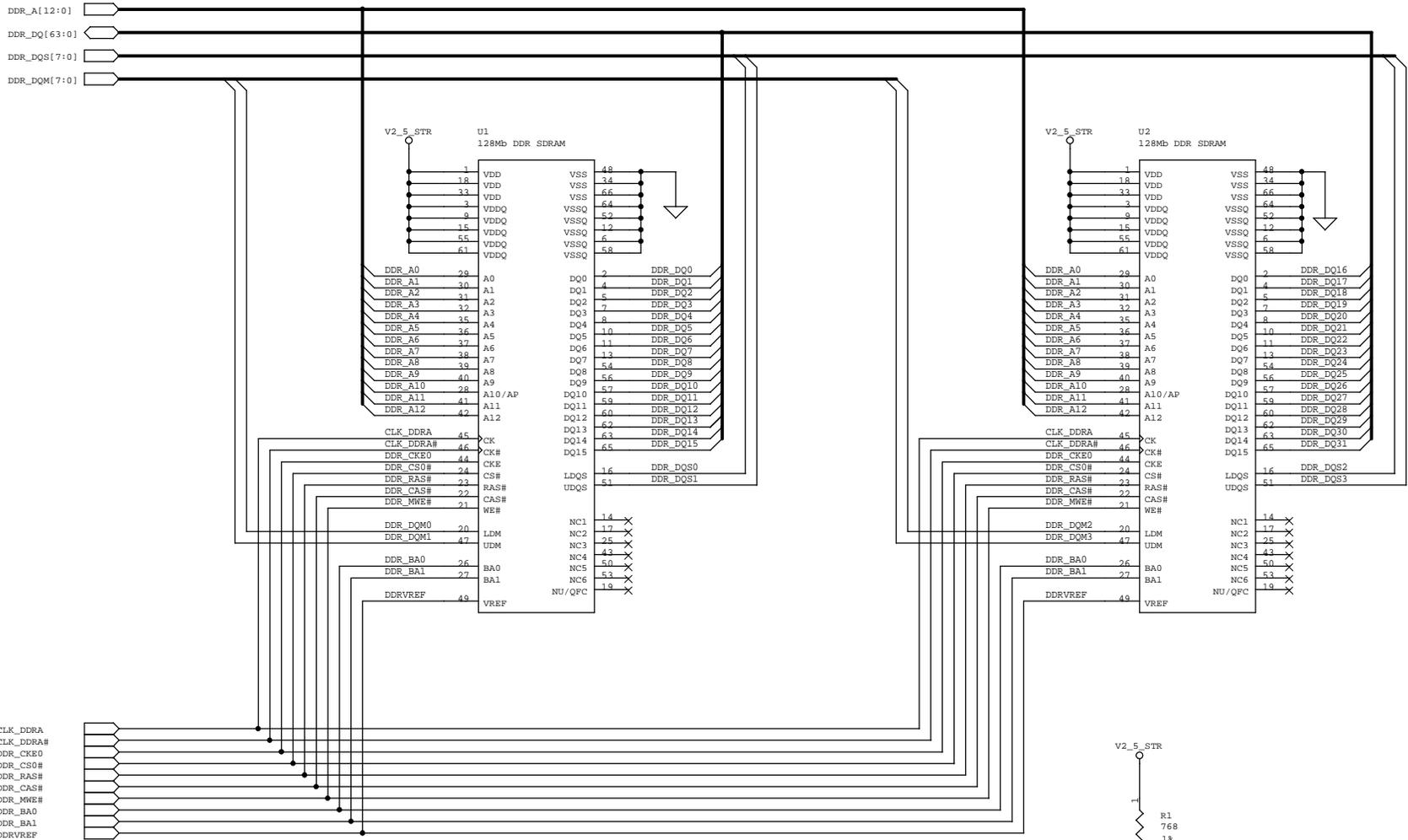


BANK 1



CLK\_DDRA  
 CLK\_DDRA#  
 DDR\_CKE0  
 DDR\_CS0#  
 DDR\_RAS#  
 DDR\_CAS#  
 DDR\_MWE#  
 DDR\_BA0  
 DDR\_BA1  
 DDRVREF

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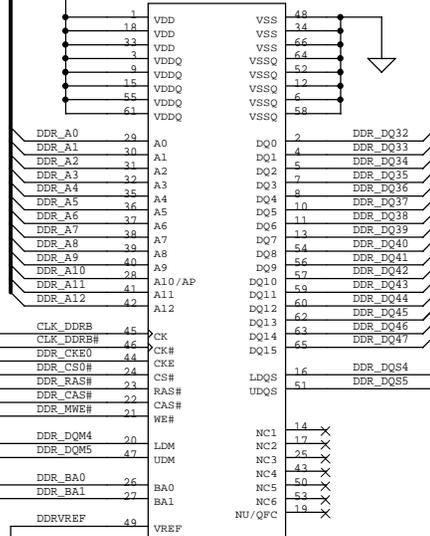
3940 Freedom Circle  
 Santa Clara, CA. 95054  
 (408) 919-3000

Project: <b>TM5800 Design Guide</b>		Revision: <b>A</b>	
Title: <b>Dual Bank DDR Down (1/4)</b>		Document Number: <b>DOCUMENT#</b>	
Size: Custom	Date: Friday, November 30, 2001	Author: Basil	Page 1 of 4

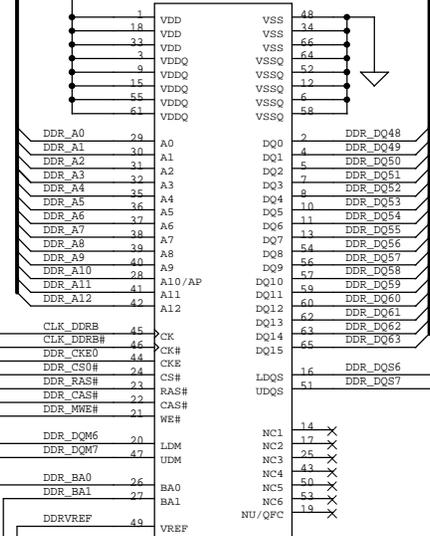
BANK 1

DDR\_A[12:0]  
 DDR\_DQ[63:0]  
 DDR\_DQS[7:0]  
 DDR\_DQM[7:0]

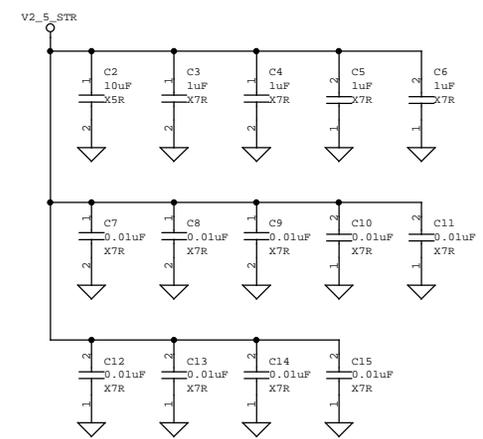
V2\_5\_STR U3  
 128Mb DDR SDRAM



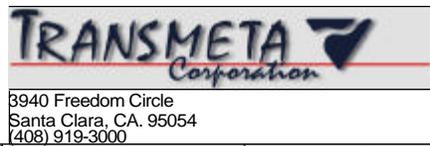
V2\_5\_STR U4  
 128Mb DDR SDRAM



CLK\_DDRB  
 CLK\_DDRB#  
 DDR\_CKE0  
 DDR\_CS0#  
 DDR\_RAS#  
 DDR\_CAS#  
 DDR\_MWE#  
 DDR\_BA0  
 DDR\_BA1  
 DDRVREF

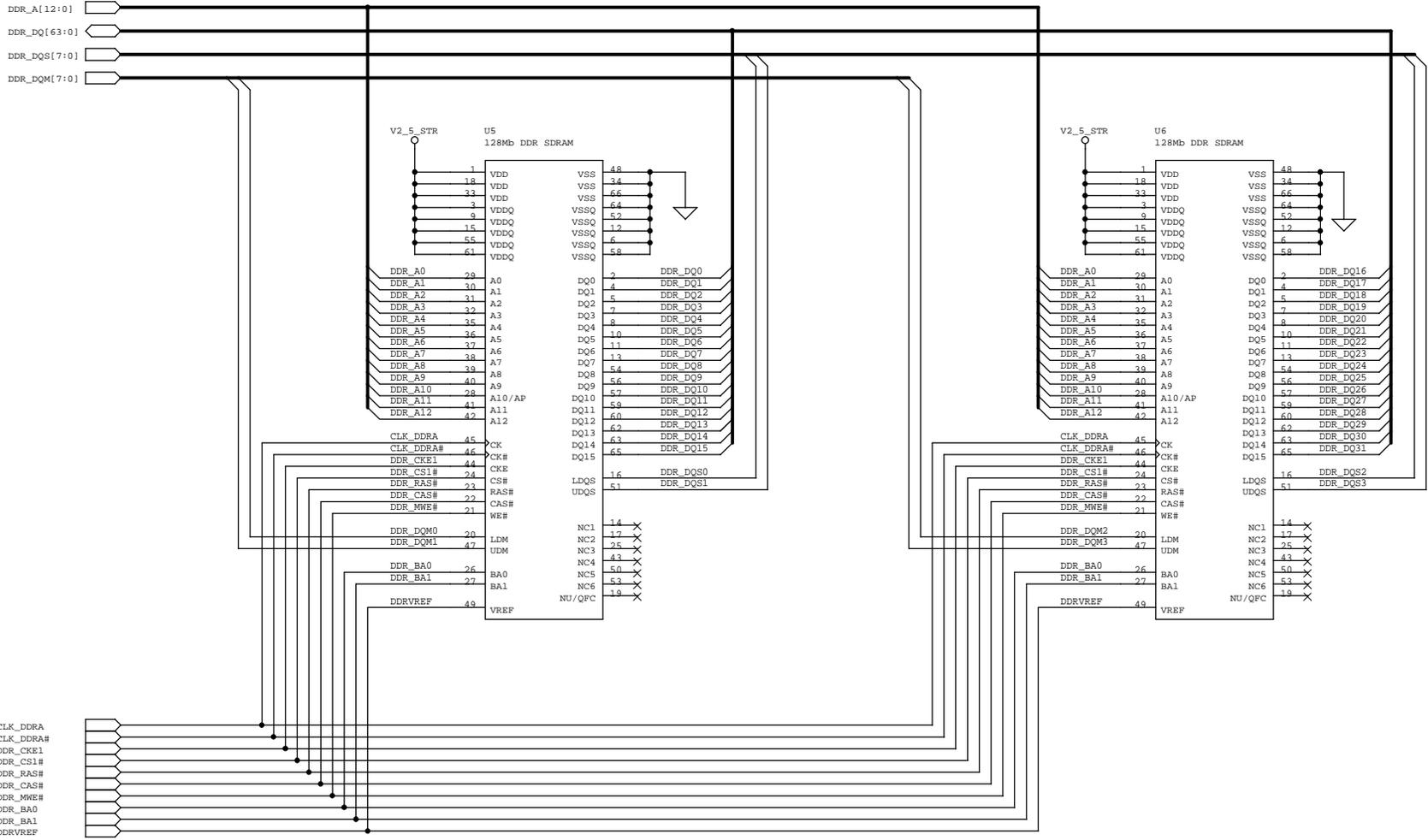


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BANK 2



CLK\_DDRA  
 CLK\_DDRA#  
 DDR\_CKE1  
 DDR\_CS1#  
 DDR\_RAS#  
 DDR\_CAS#  
 DDR\_MWE#  
 DDR\_BA0  
 DDR\_BA1  
 DDRVREF

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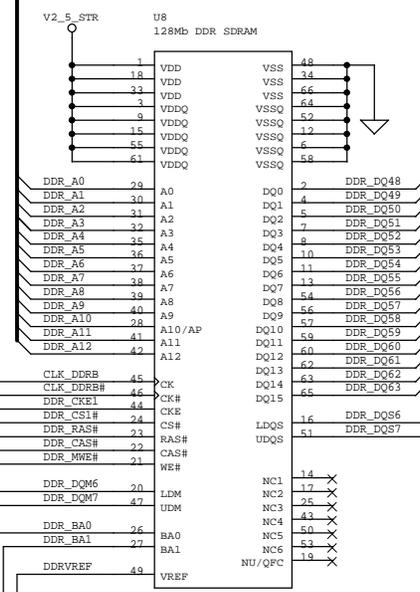
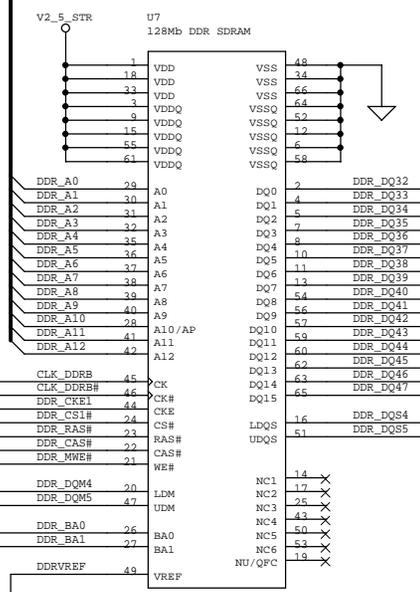
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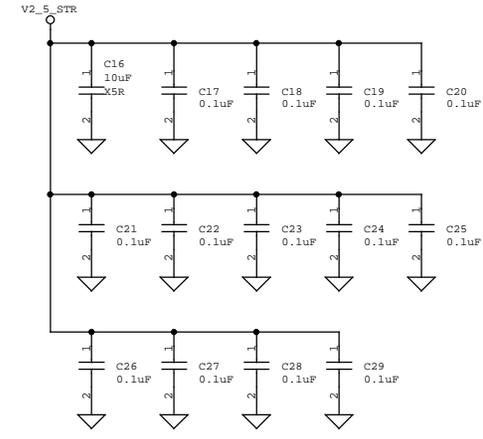
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BANK 2

DDR\_A[12:0]  
 DDR\_DQ[63:0]  
 DDR\_DQS[7:0]  
 DDR\_DQM[7:0]



CLK\_DDRB  
 CLK\_DDRB#  
 DDR\_CKE1  
 DDR\_CS1#  
 DDR\_RAS#  
 DDR\_CAS#  
 DDR\_MWE#  
 DDR\_BA0  
 DDR\_BA1  
 DDRVREF



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