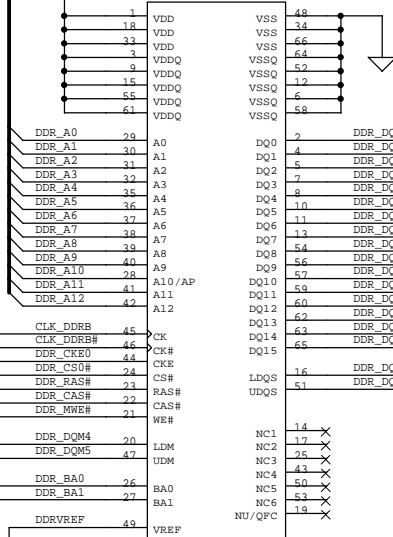


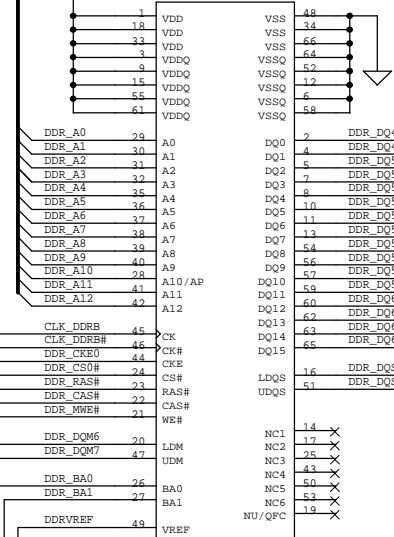
BANK 1

DDR_A[12:0]
DDR_DQ[63:0]
DDR_DQS[7:0]
DDR_DQM[7:0]

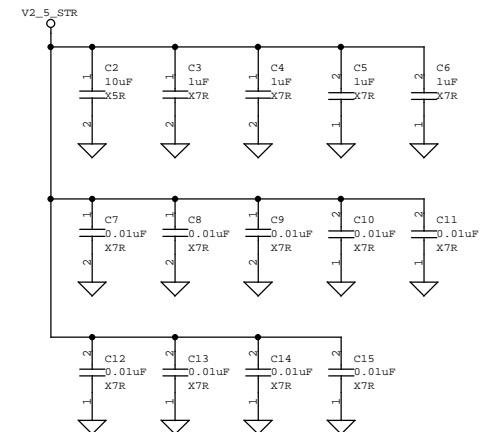
V2_5_STR U3
128Mb DDR SDRAM



V2_5_STR U4
128Mb DDR SDRAM



CLK_DDRB
CLK_DDRB#
DDR_CKE0
DDR_CS0#
DDR_RAS#
DDR_CAS#
DDR_MWE#
DDR_BA0
DDR_BA1
DDRVREF



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Project: TM5800 Design Guide

Title: Dual Bank DDR Down (2/4)

Document Number: **DOCUMENT#**

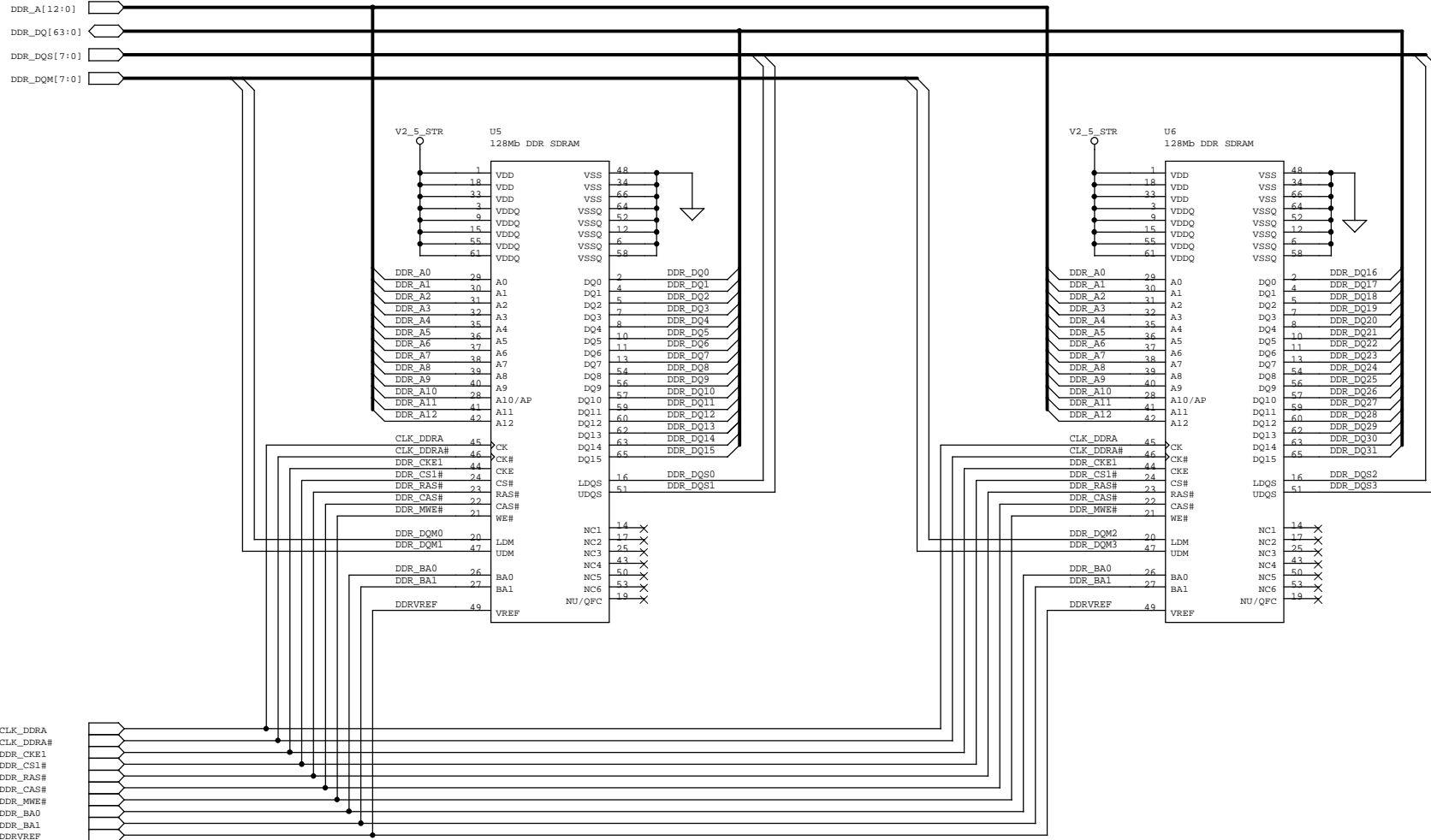
Revision: A

Size: Custom Date: Friday, November 30, 2001

Author: Basil

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BANK 2



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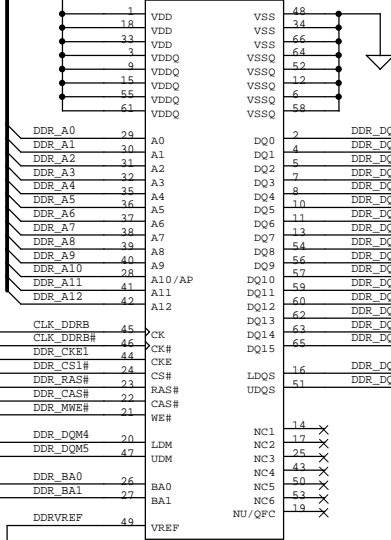


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Size: Custom	Date: Friday, November 30, 2001	Author: Basil	Page 3 of 4

BANK 2

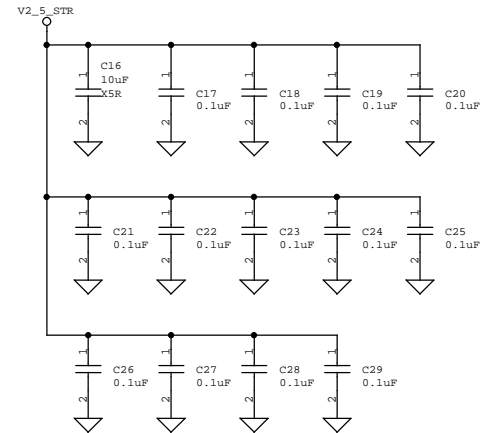
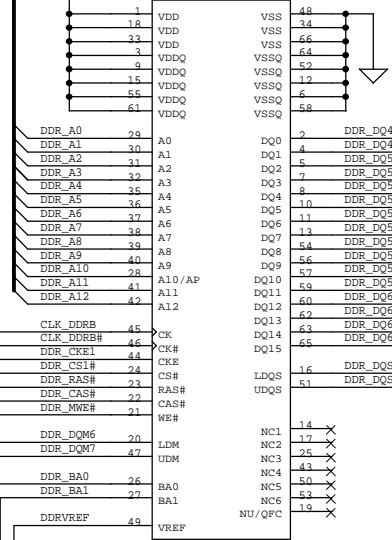
DDR_A[12:0]
DDR_DQ[63:0]
DDR_DQS[7:0]
DDR_DQM[7:0]

V2_5_STR U7
128Mb DDR SDRAM



CLK_DDRB
CLK_DDRB#
DDR_CKE1
DDR_CKE1#
DDR_RAS#
DDR_CAS#
DDR_MWE#
DDR_BA0
DDR_BA1
DDRVREF

V2_5_STR U8
128Mb DDR SDRAM



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