TM5500/TM5800 System Design Guide

July 9, 2002

TRANSMETA™

Crusoe™ Processor Model TM5500/TM5800
System Design Guide
Revision 1.3

Revision History:

1.0 July 2, 2001 - first release

1.1 December 6, 2001 - updated schematics, reorganized and added new information, misc corrections

1.2 June 17, 2002 - changed DDR interface spec to one bank only, removed “Preliminary” mark

1.3 July 9, 2002 - updated MAX1718 core power supply example, removed ISL6211 and FAN5250 examples

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Chapter 1

Introduction and Naming Conventions

1.1 Overview

This design guide is organized into the following sections:

- *Introduction and Naming Conventions* (this chapter) introduces the conventions used in this document, including possible differences between hardware names for power supplies, pins, etc. and the reference schematics used throughout the document.
- Chapter 2, *Example System Block Diagram and Schematics* presents the Crusoe TM5500/TM5800 processor in the context of a block diagram that shows necessary components and their connections. The reference schematic for the processor itself is also provided.
- Chapter 3, *Processor Power Supplies and Power Management* describes the power supply network in detail.
- Chapter 4, *DDR Memory Design* provides design guidelines and layout requirements for incorporating DDR SDRAM memory into a design.
- Chapter 5, *SDR Memory Design* provides design guidelines and layout requirements for incorporating SDR SDRAM memory into a design.
- Chapter 6, *System Design Considerations* describes a variety of design issues, including clocking, reset, ROM interfaces, signal pull-up/pull-down requirements, thermal sensor, and southbridge interfaces.
- Chapter 7, *PCB Layout Guidelines* discusses physical issues related to memory and component interfaces, power supplies, signal integrity, mounting and spacing constraints, tolerances and fabrication guidelines, and footprint and pin escape diagrams.
- Appendix A, *System Design Checklists* includes cross-referenced checklists to follow while designing a system.
- Appendix B, *Serial Write-protection PLD Data* includes the JEDEC fuse map and CUPL source code for the write-protection PLD required for serial-ROM Code Morphing software placement. This issue is described in *Serial Flash ROM Write Protection Circuit* on page 93 in Chapter 6, *System Design Considerations*.
- An *Index* is also included.

Note
The block diagram and reference schematics included in this book offer general guidelines for integrating TM5500/TM5800 processors into product designs. For detailed processor-specific information, consult the reference documents listed below.

1.2 Reference Documents

The following documents are available from Transmeta for use in conjunction with this design guide. Some of these documents are extensively referenced in the design guide, and should be consulted as specified in the text.

- *TM5500/TM5800 Data Book*
- *TM5500/TM5800 Package Specifications and Manufacturing Guide*
- *TM5500/TM5800 Thermal Design Guide*
- *TM5500/TM5800 Development and Manufacturing Guide*
- *TM5500/TM5800 BIOS Programmer's Guide*
- *TM5500/TM5800 IBIS Models*
- *TM5500/TM5800 BSDL file*
- *TM5500/TM5800 Code Morphing Software Release Notes*
- *TM5500/TM5800 Technical Bulletins and Errata documents*

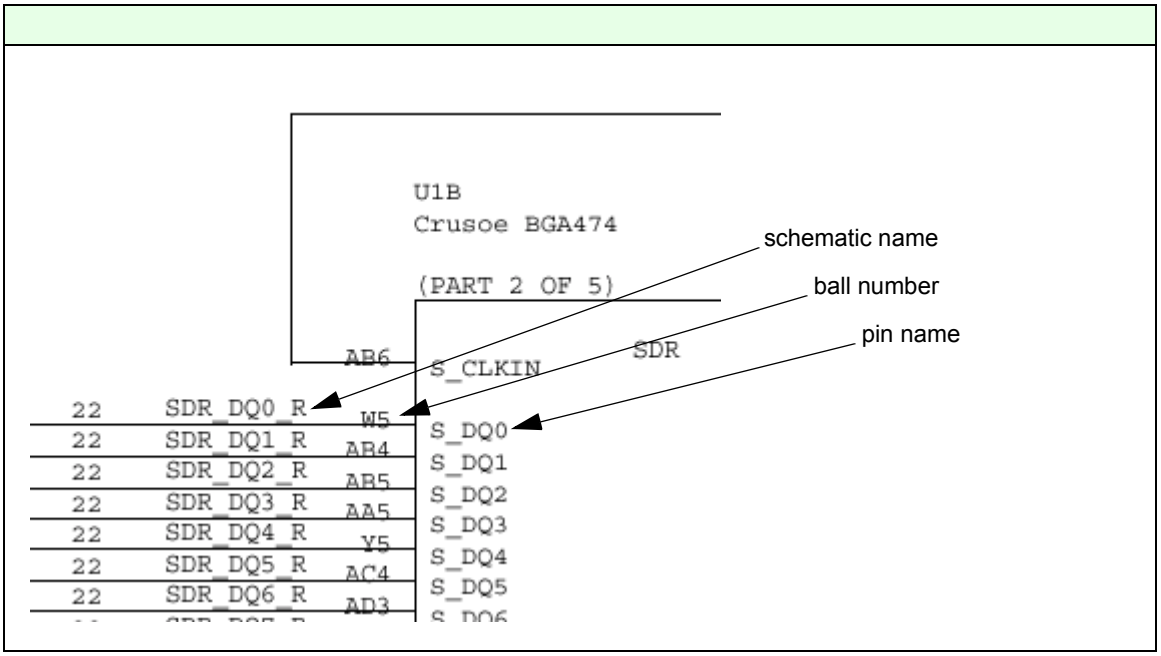
1.3 Naming Conventions

Power supply and signal names used in the *Data Book* and other hardware-specific materials can be different from those used on the reference schematics. This section shows the terms used in the *System Design Guide* and the reference schematics, and correlates them with the hardware-specific names used elsewhere.

In general, the hardware symbols in the schematics show the hardware names for each item (signal or power line). The alphanumeric marker at the connection between symbol and line is the ball number, described in detail in the *Data Book*. The line itself shows the schematic net name, i.e. the name that is used throughout this document to refer to that net/signal/line.

The following diagram shows how to locate the various schematic names:

Figure 1: Example Schematic Naming System



1.3.1 Power Management Mode Terms

The power management modes supported by TM5500/TM5800 processors are discussed in detail in Chapter 1, *Functional Interface Description*, in the *Data Book*. The following tables show the ACPI power and sleep states supported by TM5500/TM5800 processors and referenced in this document.

Table 1: Supported ACPI Processor States

ACPI State	ACPI State Name	Description
C0	Normal	Active power state with processor executing instructions.
C1	Auto Halt	Sleep state entered by processor executing HALT instruction.
C2	Quick Start	Sleep state requiring chipset/hardware support. This state is lower power than C1.
C3	Deep Sleep	Sleep state requiring chipset/hardware support. This state is lower power than C2.

Table 2: Supported ACPI System States

ACPI State	ACPI State Name	Description
S0	Working	Normal active state (not sleeping).
S1	Power-on Suspend	Processor not executing instructions. Processor state and RAM context maintained.
S3	Suspend-to-RAM (STR)	Current processor state is suspended and stored in volatile RAM (that is kept powered). Only _STR and _ALWAYS power supplies are active.

Table 2: Supported ACPI System States (Continued)

ACPI State	ACPI State Name	Description
S4	Suspend-to-Disk (STD)	Current processor state is suspended and saved to non-volatile disk. All power supplies except _ALWAYS are off.
S5	Soft Off	System is turned off. All power supplies except _ALWAYS are off.

Note that some terms must be combined for a full description of system state (e.g. Working/Auto Halt vs. Working/Quick Start). For more details on ACPI states, see the ACPI specification.

For information on timing requirements between states, see *State Transition Timing Requirements* on page 42. Power specifications for each of the supported power management modes are provided in *Chapter 3, Electrical Specifications* in the *Data Book*.

1.3.2 Power Network Names

Transmeta's reference schematics use a standard naming convention for power supply nets, provided in the table below.

Table 3: Power Net Naming Conventions

Convention	Description
V_*name*	A switched voltage such as V_CPU_CORE, off during S3, S4, and S5
V*n_d*_STR	A voltage present in S3 (STR), off during S4 and S5
V*n_d*	A switched voltage at *n.d* volts, off during S3, S4, and S5
V_N*n_d*	A negative voltage at *n.d* volts, off during S3, S4, and S5
V*n_d*_ALWAYS	An always-on voltage, i.e. present in all ACPI sleep states

1.3.3 Signal Names

Transmeta's reference schematics call out many signals which may be named slightly differently in hardware-oriented documents such as the *Data Book*. The following table illustrates the character conventions used in the schematics:

Table 4: Signal Naming Conventions

Character	Description	Example
#	Denotes asserted low signals. Signal names without this suffix are assumed to assert high.	LOWSIG#
.., :	Used to separate elements in a list.	EIGHTBITBUS[7..0] D[7:0]
/	Can be used to separate multiple uses of a pin.	USEA/USEB
[ ]	Delineates bus name from element list.	EIGHTBITBUS[7..0]

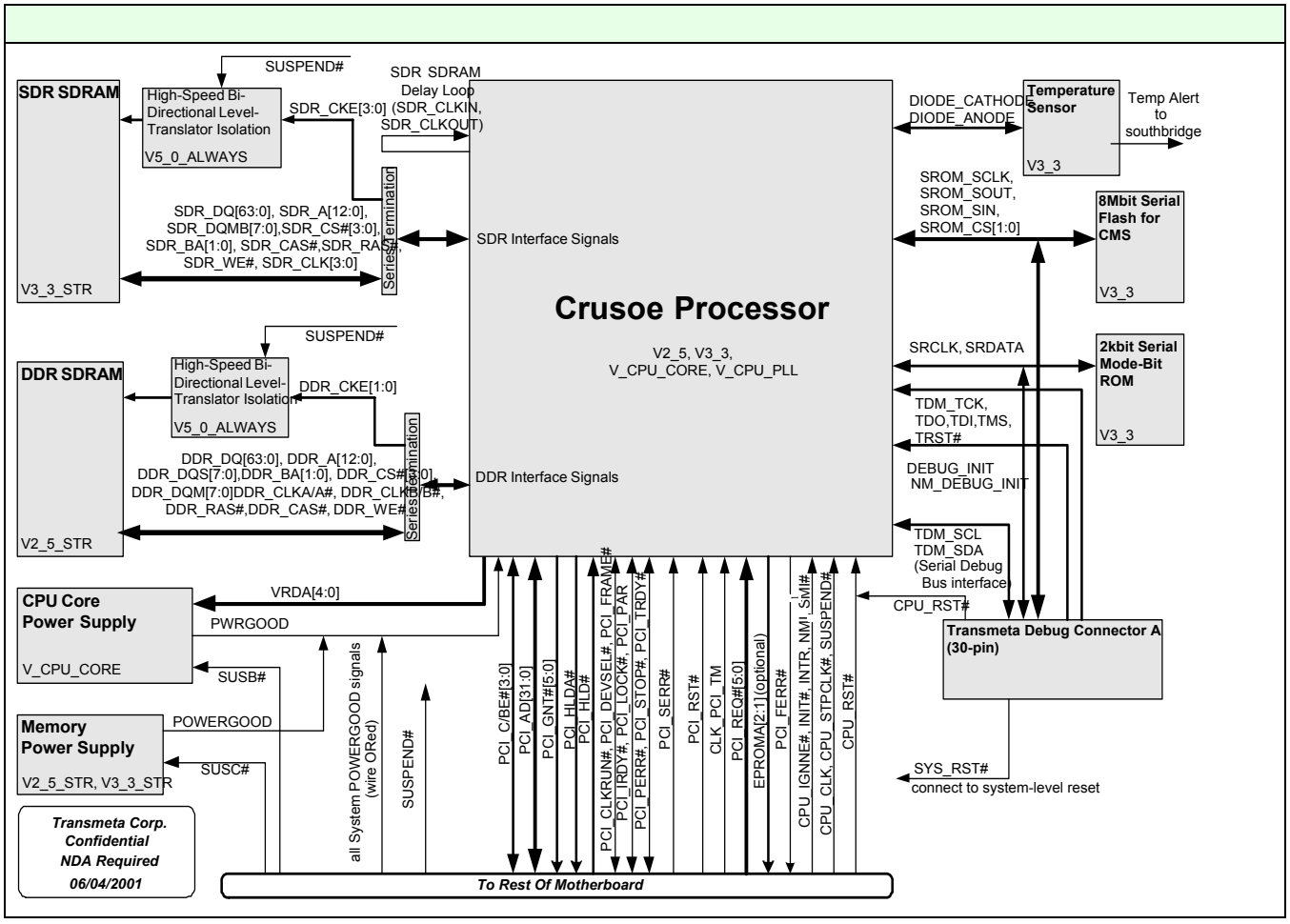
Chapter 2

Example System Block Diagram and Schematics

2.1 System Block Diagram

The block diagram below shows major elements of a TM5500/TM5800 processor-based system design. Signals and bus interconnections are also shown. For detailed circuit design information, see the reference schematics throughout this document (also available in OrCAD format from your Transmeta representative).

Figure 2: Example System Block Diagram



TM5500/TM5800 processors include both core processor and northbridge functionality. For a motherboard designer, this means the processor looks very much like a northbridge. TM5500/TM5800 processors support two DRAM interfaces, one for Double Data Rate (DDR) SDRAMs and the other for Single Data Rate (SDR) SDRAMs. Designers can choose to use either or both SDRAM interfaces, depending on their system cost and performance requirements.

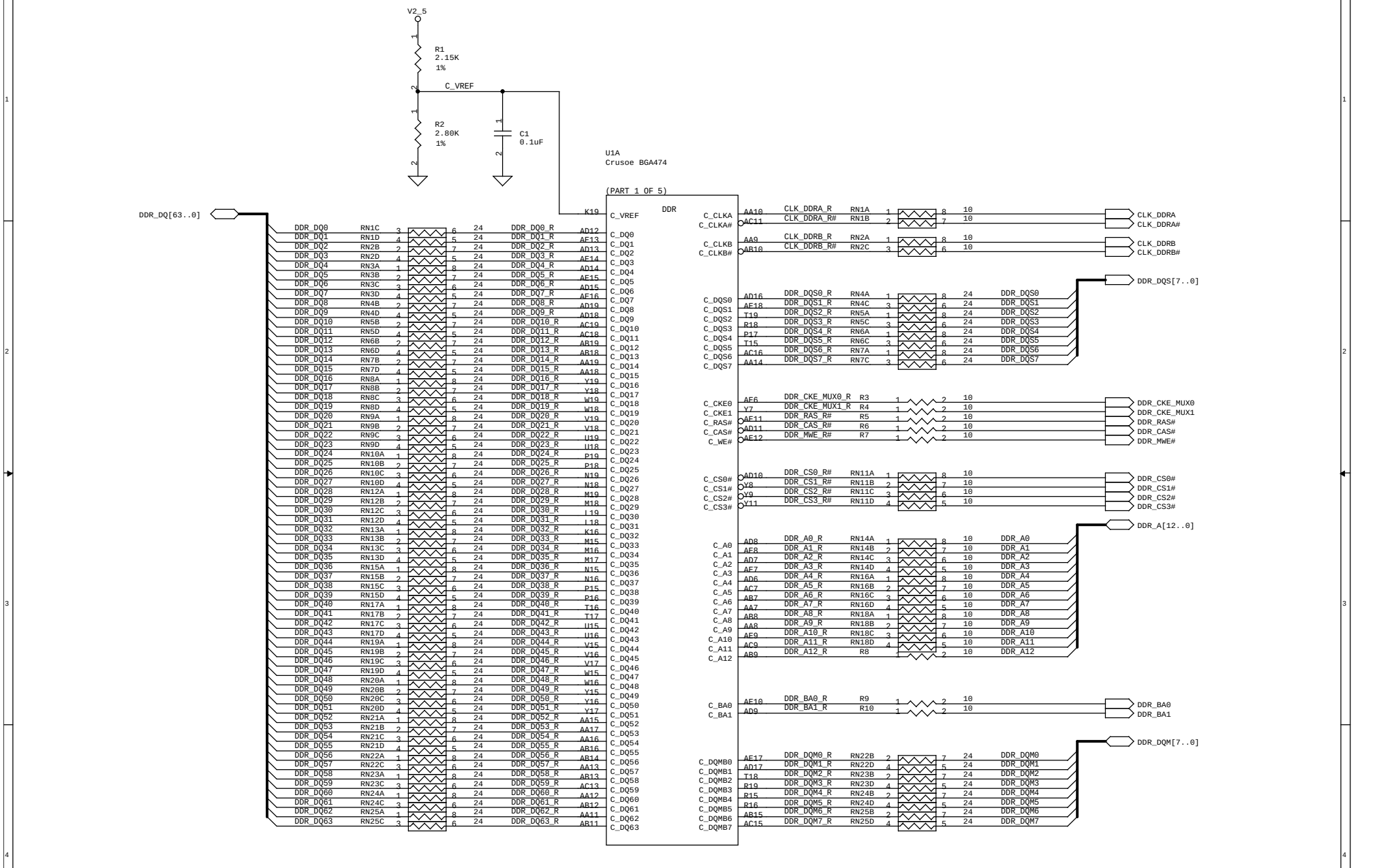
In the block diagram, note that power signals that feed each component are listed in the component's block. This helps to identify suspend and switched power distribution to each component. Descriptions of each supply are described in Chapter 3, *Processor Power Supplies and Power Management*.

The major elements shown in the block diagram are outlined below:

- **Processor Core Power Supply**. The processor core high-efficiency switched-mode power supply. See Chapter 3, *Processor Power Supplies and Power Management*.
- **Memory Power Supplies**. The power supplies for SDR and DDR SDRAM memory. See Chapter 3, *Processor Power Supplies and Power Management*.
- **DDR SDRAM Interface**. The processor can support up to two identical banks of DDR SDRAMs in various configurations of 64-Mbit, 128-Mbit, 256-Mbit, and 512-Mbit devices. See Chapter 4, *DDR Memory Design*.
- **SDR SDRAM Interface**. The processor can support up to four banks of SDR SDRAMs in various configurations of 64-Mbit, 128-Mbit, 256-Mbit, and 512-Mbit devices. See Chapter 5, *SDR Memory Design*.
- **SDRAM High-speed Bidirectional Level-translator Isolation**. Signal isolation is used to ensure that CKE signals to the SDRAMs remain stable during processor power transitions. Since the processor does not have a suspend power well, output signals are undefined during power transitions and subject to glitching.
- **PCI Interface and PCC Signals**. The PCI interface is 33 MHz, 3.3 V. The arbiter supports five REQ/GNT pairs. CLKRUN is supported (see *Using CLKRUN* on page 98). PCC (PC compatibility) signals are used for communication with the southbridge. See *Southbridge* on page 98.
- **Code Morphing Software Serial Flash ROM**. Code Morphing software is stored in this optional (but recommended) 1 Mbyte device. See *Serial Flash ROM Interface* on page 91. Other options for Code Morphing software code storage (such as sharing the BIOS ROM) are also described. See *Combined BIOS/CMS Parallel ROM Interface* on page 96.
- **Serial Flash Write-protection Circuit**. If a serial flash ROM is used for Code Morphing software, a PLD (programmable logic device) write-protection device must be added to the serial flash ROM circuit. See *Serial Flash ROM Write Protection Circuit* on page 93.
- **Mode-bit ROM (required)**. System-dependent configuration options vital to proper processor operation are stored in this required 2 Kbit device and read by the processor at boot time. See *Mode-bit ROM* on page 89.
- **Thermal Sensor**. An external thermal sensor is used in conjunction with a thermal sensing diode built into the processor. See *Thermal Diode and Thermal Sensor* on page 103.
- **Transmeta Debug Module (TDM) Interface**. This adds some low-level debug support to facilitate in-design bring-up, as well as connectivity to the Transmeta Virtual In-Circuit Emulator CE (TMVICE) for software development. See *TDM Debug Interface Connection* on page 107.

2.2 Processor Schematics

The following pages show TM5500/TM5800 processor reference schematics.



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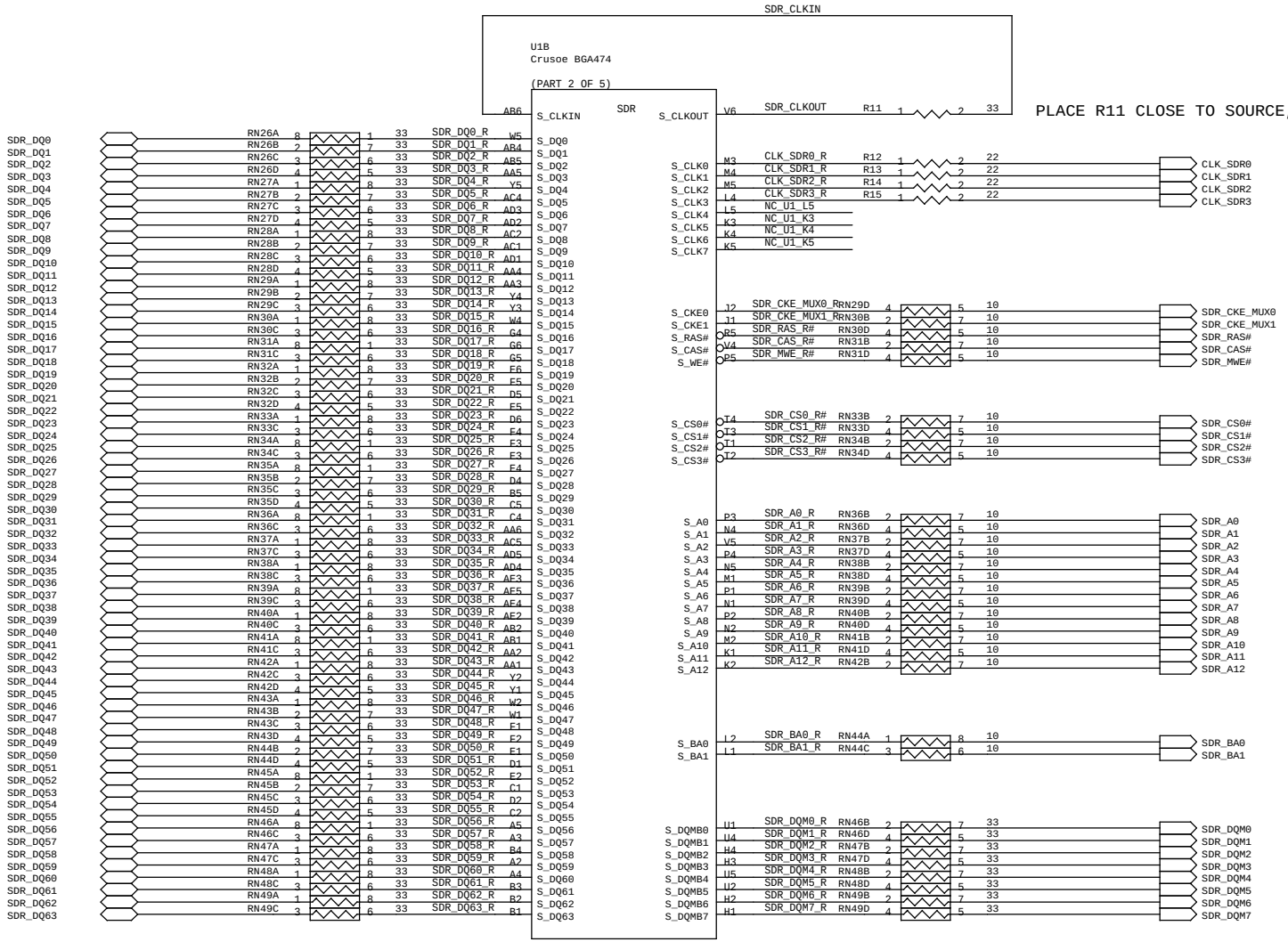
Project: TM5800 Design Guide

Title: TM5800 DDR Interface

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Thursday, November 29, 2001 | Author: Basil | Page 1 of 5



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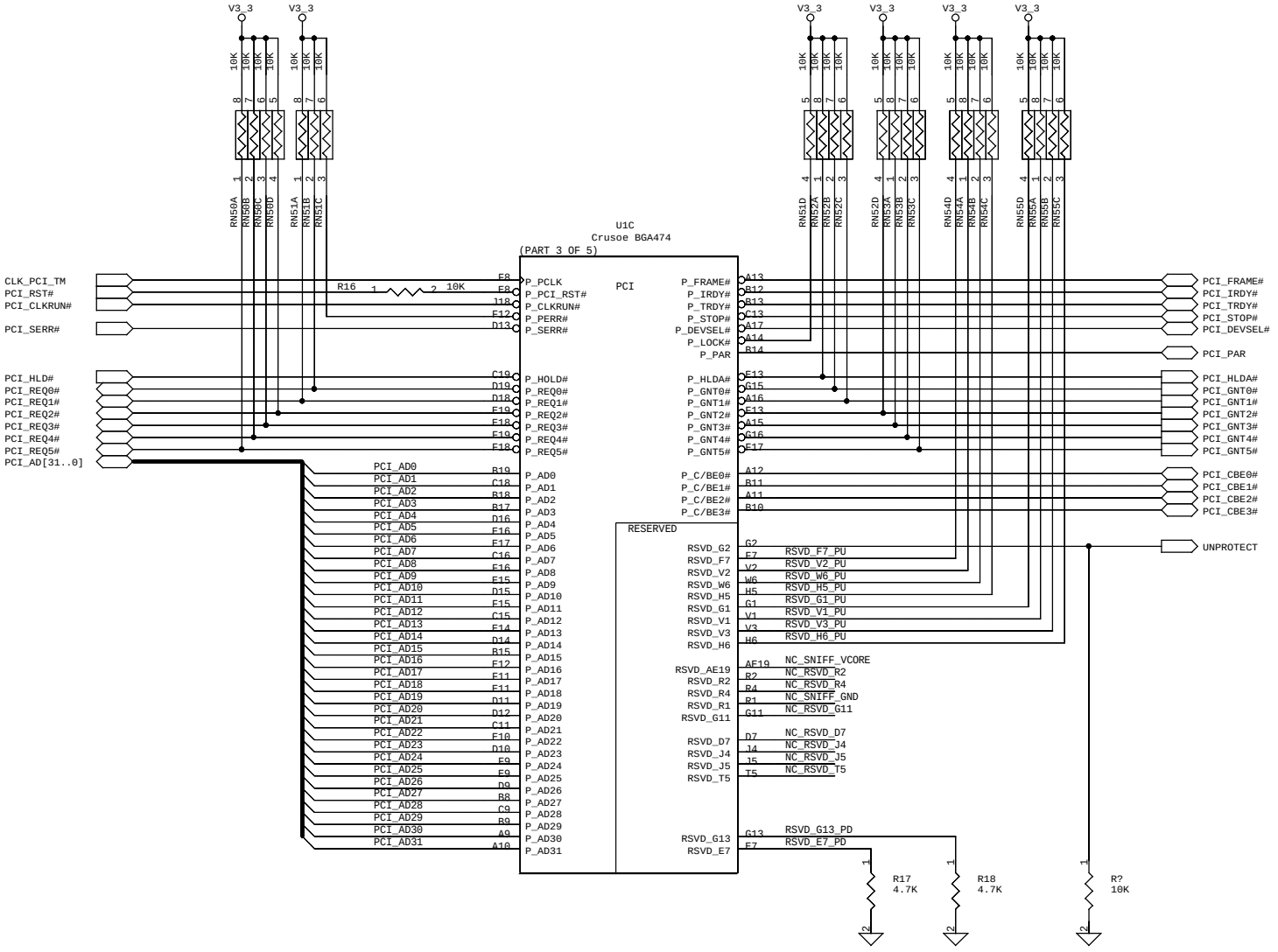

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Project: TM5800 Design Guide

Title: TM5800 PCI Interface

Document Number: **DOCUMENT#** Revision: A

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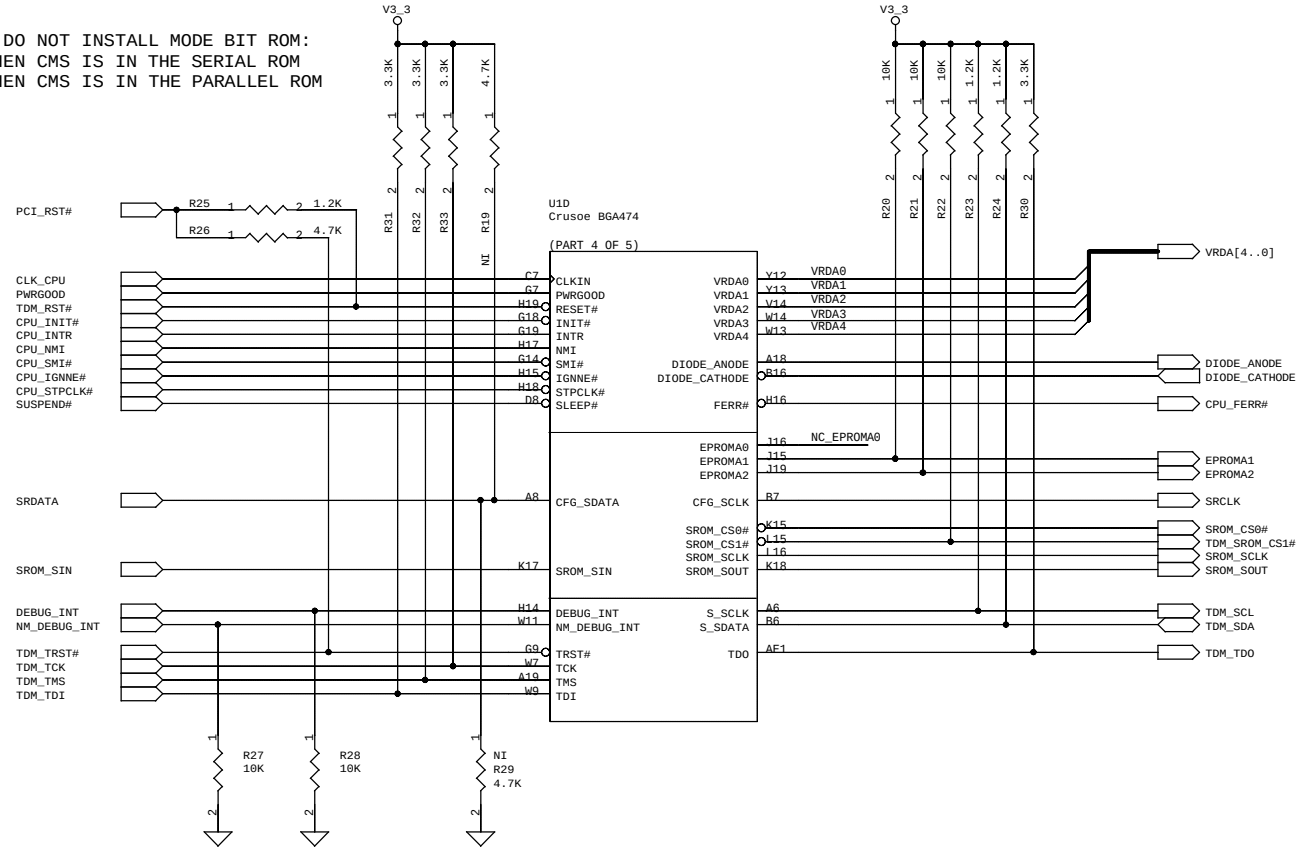
SYSTEMS THAT DO NOT INSTALL MODE BIT ROM:
INSTALL PU WHEN CMS IS IN THE SERIAL ROM
INSTALL PD WHEN CMS IS IN THE PARALLEL ROM



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Project: TM5800 Design Guide

Title: TM5800 Sideband

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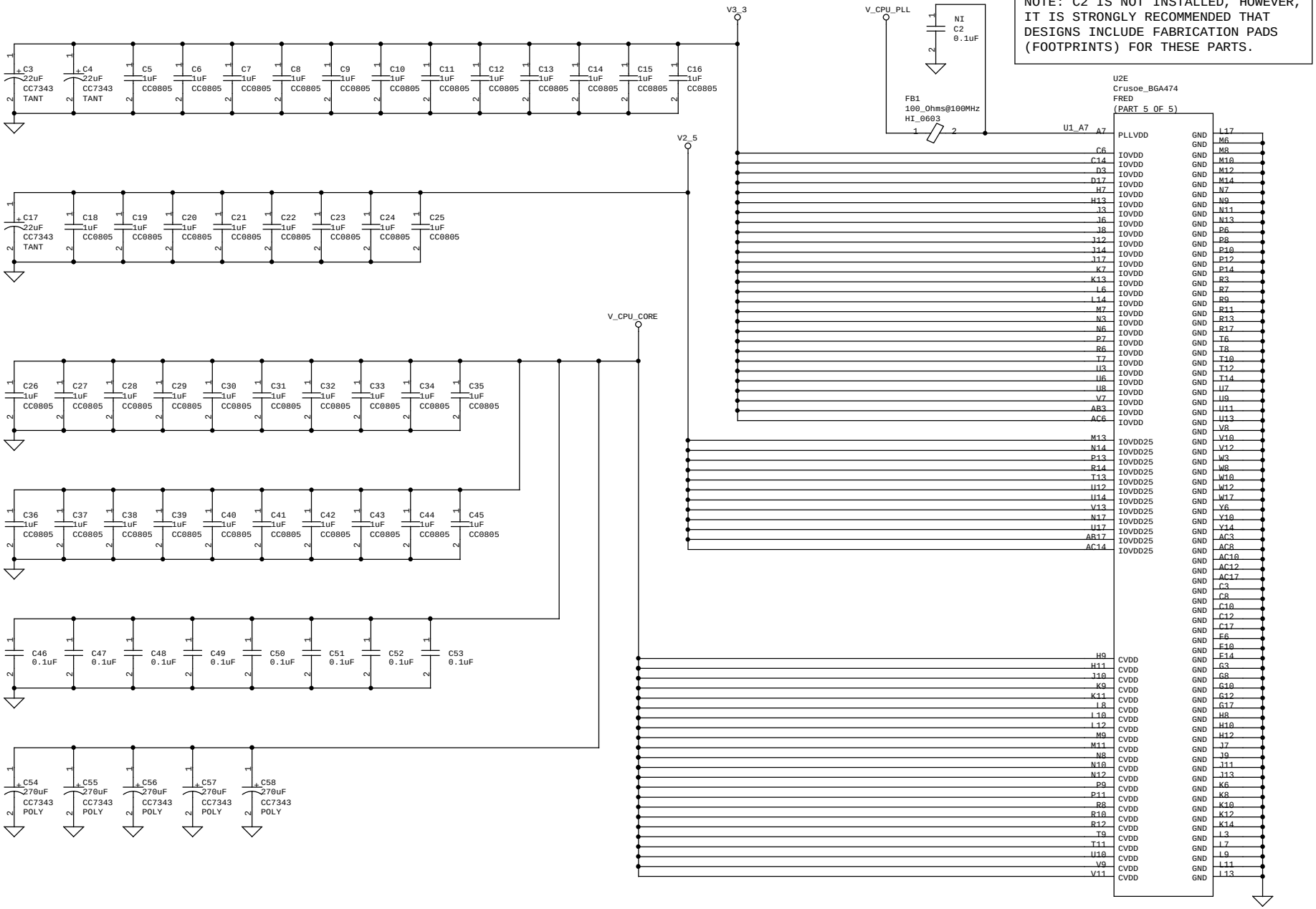

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Project: TM5800 Design Guide

Title: TM5800 PWR & GND

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Thursday, November 29, 2001 | Author: Basil | Page 5 of 5

Chapter 3

Processor Power Supplies and Power Management

This section provides design guidelines for TM5500/TM5800 processor power supplies, power sequencing, and power management circuits. This section also describes processor power supply requirements that must be implemented.

See the *Data Book* for peak current and other power-related processor specifications. The current requirements of each supply should be calculated on a per-design basis.

Note
Follow the power supply sequencing requirements described in *Power Supply Sequencing* on page 35.

3.1 Power Supplies

The block diagram in Chapter 2, *System Block Diagram*, shows the power supplies for each of the major components. The power source for all notebook computers is either a battery (< 20 V) or a DC wall adapter of a comparable voltage. An intelligent switching mechanism is needed to create a stable V_DC or V_SOURCE that is used to supply the regulators that generate system voltages.

There are four power supplies required for TM5500/TM5800 processors:

- Core power supply (V_CPU_CORE)
- PLL power supply (V_CPU_PLL)
- 3.3 V I/O power supply (V3_3)
- 2.5 V I/O power supply (V2_5)

It is important to follow the design recommendations and meet the requirements provided below for TM5500/TM5800 power supply designs.

3.1.1 Core Power Supply Requirements

Note
See the *Data Book* for TM5500/TM5800 voltage and current requirements for this and all power supplies.

Information on low-range VRMs (voltage regulator modules), strongly recommended for new system designs, is available from qualified VRM vendors as indicated in this document.

Note
The only VRM qualified by Transmeta for TM5500/TM5800 processors is the Maxim MAX1718. Refer to the manufacturers VRM data sheet for detailed design information.

Care must be taken to assure the core power supply voltage, V_CPU_CORE, supplied to TM5500/TM5800 processors does not exceed the absolute maximum limit of 1.5 V when evaluating TM5500/TM5800 processor in systems designed for TM5400/TM5600 processors (designed to operate up to 1.6 V).

WARNING
CORE POWER SUPPLY VOLTAGE (V_CPU_CORE) TO TM5500/TM5800 PROCESSORS MUST NOT EXCEED 1.5 V OR PERMANENT DEVICE DAMAGE MAY RESULT.

The table below provides the most significant core power supply requirements for TM5500/TM5800 processors

Table 5: Core Power Supply Requirements for TM5500/TM5800 Processors

Specification	Value	Notes
Core voltage range	0.95 - 1.30/1.35/1.40 V (nominal)	See LongRun™ specifications
Core voltage static regulation	+/- 2% maximum at all voltage settings, across all set points, line, load and temperature	Voltage tolerance for DC load changes
Core voltage dynamic regulation	+/- 5% maximum excursion; return to within 1% of static regulation band for a +/- 6 A load step	Voltage tolerance for dynamic current changes, i.e. short-term voltage excursions that quickly return to the static regulation band described above
Core voltage recovery time	20 μS maximum to return to within 1% of static regulation band for a +/- 6 A load step	Pulse width of voltage spikes
Core voltage periodic and random deviation (PARD), including ripple	+/- 1% maximum	Includes other voltage changes not included above
Core voltage supply slew rate	4.0 mV/μS minimum	Minimum voltage change rate required for LongRun™ power management transitions
Core supply current	10.0 A maximum	For 1 GHz SKU
VRM voltage control mode	Remote sense operation	Using processor core voltage feedback signal (SNIFF_CVDD), processor ball number AE19

Table 5: Core Power Supply Requirements for TM5500/TM5800 Processors (Continued)

Specification	Value	Notes
Source voltage	10.0 V minimum	Required for this particular reference design to meet specifications above
Combined ESR of bulk capacitors	5 mΩ maximum	
Combined capacitance of bulk capacitors	800 µF minimum (nominal) 1100 µF maximum (nominal)	
Distribution resistance from bulk capacitors to processor	2 mΩ maximum	
Inductor inductance	1.8 µH nominal 2.2 µH maximum	
Inductor RMS current	14 A minimum	
Inductor saturation current	20 A minimum	

3.1.1.1 Default Power-on VRDA (VRM VID) Output Codes

TM5500/TM5800 processors have a default power-on VRDA code of 0x0E. This code corresponds to 1.050 V output for a Maxim MAX1718 VRM.

The table below shows the default power-on VRDA code values for TM5x00 processors.

Table 6: Default Power-on Start Voltage VRDA (VID) Output Codes

Processor Model	VID/VRDA Value						Default Startup Voltage
	VRDA [4]	VRDA [3]	VRDA [2]	VRDA [1]	VRDA [0]	Hex	VRM Output
TM5500/TM5800	0	1	1	1	0	0x0E	1.05 V
TM5400/TM5600	0	1	0	1	0	0x0A	1.25 V

3.1.1.2 VID/VRDA Code Table

The VID/VRDA codes for the Maxim MAX1718 VRM are shown in the table below.

Table 7: VID/VRDA Values and Output Voltages for MAX1718 VRM

VID/VRDA Value						
VRDA [4]	VRDA [3]	VRDA [2]	VRDA [1]	VRDA [0]	Hex	VRM Output
0	0	0	0	0	0x00	1.75 V
0	0	0	0	1	0x01	1.70 V
0	0	0	1	0	0x02	1.65 V
0	0	0	1	1	0x03	1.60 V
0	0	1	0	0	0x04	1.55 V
0	0	1	0	1	0x05	1.50 V
0	0	1	1	0	0x06	1.45 V
0	0	1	1	1	0x07	1.40 V
0	1	0	0	0	0x08	1.35 V
0	1	0	0	1	0x09	1.30 V
0	1	0	1	0	0x0A	1.25 V
0	1	0	1	1	0x0B	1.20 V
0	1	1	0	0	0x0C	1.15 V
0	1	1	0	1	0x0D	1.10 V
0	1	1	1	0	0x0E	1.05 V
0	1	1	1	1	0x0F	1.00 V
1	0	0	0	0	0x10	0.975 V
1	0	0	0	1	0x11	0.950 V
1	0	0	1	0	0x12	0.925 V
1	0	0	1	1	0x13	0.900 V
1	0	1	0	0	0x14	0.875 V
1	0	1	0	1	0x15	0.850 V
1	0	1	1	0	0x16	0.825 V
1	0	1	1	1	0x17	0.800 V
1	1	0	0	0	0x18	0.775 V
1	1	0	0	1	0x19	0.750 V
1	1	0	1	0	0x1A	0.725 V
1	1	0	1	1	0x1B	0.700 V
1	1	1	0	0	0x1C	0.675 V
1	1	1	0	1	0x1D	0.650 V
1	1	1	1	0	0x1E	0.625 V
1	1	1	1	1	0x1F	0.600 V

3.1.2 VRM Core Power Supply Example

The sections below provide an example core power supply design using the Maxim MAX1718 VRM. This reference design is recommended by Transmeta for TM5500/TM5800 processor-based system designs.

Note
Vendor part-specific information provided in this *System Design Guide* may be incorrect or out of date. Please consult with the manufacturer for the latest specifications and design information for the VRM and related components used in the design.

3.1.2.1 Maxim MAX1718 Regulator

Maxim provides a VRM that is well-suited for TM5500/TM5800 core power supply designs. This VRM is described below. A reference design, adapted from example circuits in the Maxim MAX1718 data sheet, is provided at the end of this section. Detailed design information for the MAX1718 low-range VRM is available from Maxim in the MAX1718 data sheet, and should be referenced whenever possible.

3.1.2.2 Output Voltage Control

The MAX1718 has three different methods that can be used to program the output voltage by means of three internal resisters:

- ***Normal Operating Mode*** voltage is determined by the logic levels of the VID inputs.
- ***Startup Mode*** voltage is determined by series resistors connected to the VID inputs.
- ***Deep Sleep Extension (DSX) Mode*** voltage is determined by the logic levels on the S0 and S1 inputs.

Which of the three methods is used to control the output voltage is determined by the ZMODE and SUS input signals. These inputs control internal multiplexers that select which register is presented to the DAC to set the output voltage. When high, the SUS input overrides the ZMODE input, forcing the output voltage to the DSX value. The table below describes this selection logic.

Table 8: MAX1718 Core Power Supply Output Control Selector

Core Power Supply Operating Mode	Output Voltage Determined By	Control Signal		
		ZMODE	SUS	CPU_STP#
Normal Operating Mode [1]	Logic level of D0-D4	Low	Low	High
Startup Mode	Impedance of D0-D4	High	Low	High
DSX Mode	Logic level of S0 and S1	Don’t care	High	Low

1. Used for LongRun power management.

Normal Operating Mode

Normal operating mode output voltage is programmed directly by the five VID input signals according to Table 7. There are no internal VID pull-ups to 5 V in the MAX1718 (as there were in the MAX1711), so there is no need for a quickswitch to protect the processor VRDA outputs from the VRM VID inputs. However, because there are no internal pull-ups, external pull-up resistors are required.

Startup Mode

Startup mode is selected when the ZMODE signal is high. In this mode the output voltage is determined by the internal impedance mode resister whose value is set on the rising edge of the ZMODE signal. The device looks at the impedance on the VID inputs. If it is > 90 KΩ it is considered a logic high, and if it is < 1.1 KΩ it is considered a logic low. This process is initiated by the rising edge of the ZMODE signal. During this time the device tries to move its VID inputs by alternately trying to pull the VID inputs high with a pull-up resistor to 5 V, and low through a pull-down resistor to ground. This happens over the period of a few µS. To make the VID input a logic 1 (high), insert a 100 KΩ resistor in series with the VID input. To make the VID input a logic 0 (low), make the series resistor zero Ω. In addition to the series resistors, a pull-up resistor of 1 KΩ must be added to each VID input. If pull-up resistors of > 1 KΩ are used to limit supply current, then a 4.7 nF capacitor must be added across each pull-up resistor to keep the AC impedance < 1 KΩ.

Deep Sleep Extension (DSX) Mode

Note
Although this feature is incorporated in the MAX1718 VRM, it is not yet qualified for the TM5500/TM5800 processor.

The MAX1718 VRM supports a Deep Sleep extension (DSX) mode that can provide a very low output voltage to the TM5500/TM5800 processor core during extended Deep Sleep periods, significantly reducing processor leakage power during long intervals of sustained system inactivity. The reference design example provided at the end of this section shows the DSX mode configured for 0.9 V operation. This can be reconfigured to a lower TM5500/TM5800 DSX voltage specification when it becomes available. See Table 9 for DSX voltage programming information.

Driving the SUS signal high overrides the ZMODE control and sets the output voltage to one of thirteen preset values between 0.600 V and 0.900 V, depending on the state of the S0 and S1 inputs. The S0 and S1 inputs are each effectively quad-state / four-level logic, and can be set by connecting them to either the VRM VCC (+5 V), REF, or GND signals, or leaving the input open. Since each input has four states and there are two inputs, there are 2^4 = 16 possible combinations, of which only thirteen are used here.

The table below provides DSX mode output voltage configuration information for the full range of DSX voltages.

Table 9: MAX1718 DSX Voltage Configuration

DSX Voltage	S0	S1
0.900 V	VCC	GND
0.875 V	GND	REF
0.850 V	REF	REF
0.825 V	OPEN	REF
0.800 V	VCC	REF
0.775 V	GND	OPEN
0.750 V	REF	OPEN
0.725 V	OPEN	OPEN
0.700 V	VCC	OPEN
0.675 V	GND	VCC
0.650 V	REF	VCC
0.625 V	OPEN	VCC
0.600 V	VCC	VCC

3.1.2.3 Current Limit Adjustment (ILIM)

Resistors in the example circuit are used to adjust the output current limit. The values are selected based on the maximum VRM current and the RDS_{on} of the lower switching FET being used. See the MAX1718 data sheet for detailed information on adjusting the output current limit.

3.1.2.4 Output Voltage Offset Control (POS, NEG)

The MAX1718 has a provision to adjust the output voltage a little higher or lower than the programmed value. This is accomplished by means of a differential input amplifier that adds an offset voltage to the programmed value. Since voltage positioning is used in the reference design example, the output will droop below the set value by a negative tolerance. The output voltage offset control feature is used to shift the output voltage up to yield the required +5%, -2% output voltage tolerance.

The actual output offset voltage is the voltage applied between the POS and NEG inputs multiplied by a variable factor that depends on the output voltage, which in the reference design example is approximately 0.85. See the MAX1718 data sheet for detailed information on adjusting the output voltage offset.

3.1.2.5 Switching Frequency/On-time Selection Control (TON)

Note
The MAX1718 VRM has only been tested for TM5500/TM5800 designs at 300 KHz operation.

The VRM switching frequency is selected by means of the TON input. The reference design example shows the MAX1718 configured for 300 KHz operation. The MAX1718 has been tested to operate at 300 KHz only.

3.1.2.6 Output Voltage Slew-rate Adjustment (TIME)

The resistor connected to the TIME input on the device (R_{TIME}) is used to set the slew-rate of the output voltage change when transitioning between programmed output values (see MAX1718 data sheet for details). The recommended range for R_{TIME} is 47 KΩ for a 380 KHz slew-rate clock to 470 KΩ for a 38 KHz slew-rate clock. Slew-rate clock frequency = 150 KHz x (120K / R_{TIME}). The slew rate given by:

$$\frac{dV}{dT} = \frac{450}{R_{TIME}}$$

The slew rate is in mV per µS and the resistor, R_{TIME}, is in KΩ.

3.1.2.7 DH Pull-up Current/Turn-on Time Adjustment (BST)

A resistor connected to the BST input in the reference design example is used when necessary to slow down the turn-on time of the upper FET to minimize ringing.

3.1.2.8 VRM Shutdown Control (SKP/SDN#)

When the SKP/SDN# input is low, the VRM is shut down. When this signal is pulled high to VCC, the VRM operates in skip mode. When this signal is left floating, the VRM operates in PWM mode. The reference design example operates in skip mode to take advantage of the high efficiency of skip mode at low currents.

3.1.2.9 POWERGOOD Status (VGATE)

VGATE is an open-drain output which is high (floating) when the output voltage is in regulation. This output thus indicates a POWERGOOD status, and is used during power-up in the reference design example to enable the processor I/O power supplies (V3_3_STR and V2_5_STR) to begin ramping up, as required by TM5500/TM5800 power sequencing specifications. VGATE has an internal sense circuit to force it high during programmed transitions such as normal LongRun voltage step transitions, without the need for an external deglitching circuit.

3.1.2.10 Voltage Positioning

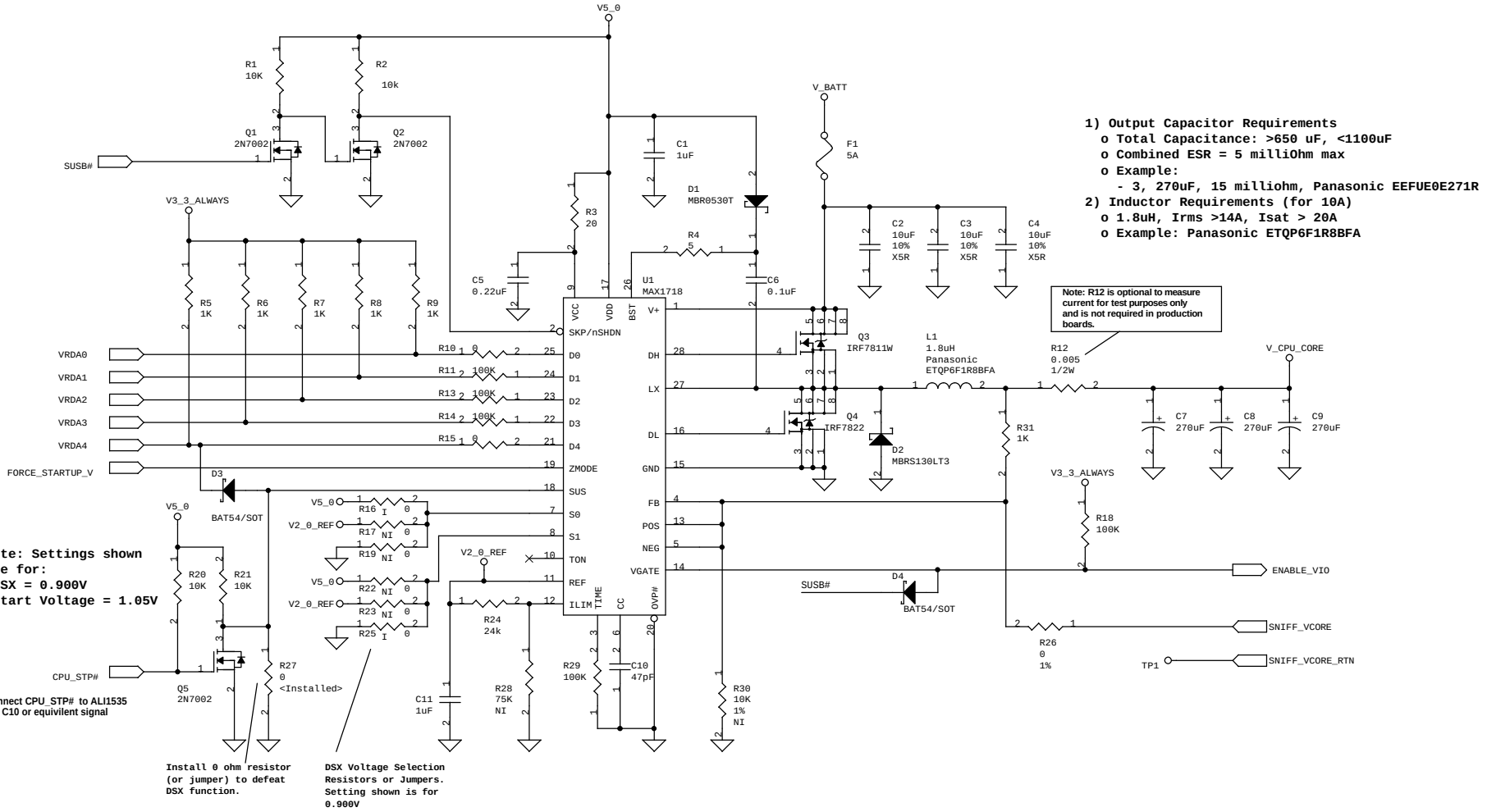
TM5500/TM5800 processors should not be used with voltage positioning core power supplies. The MAX1718 VRM in this reference design is configured for remote sense operation.

3.1.2.11 MAX1718 Core Supply Reference Design Schematic

A MAX1718 core power supply reference design schematic, recommended for TM5500/TM5800 processors, is provided on the following page.

Note that the output from this reference design power supply is labeled V_CPU_CORE. This output is connected to the processor core supply (CVDD) balls. The SNIFF_VCORE voltage sense signal in the reference design is connected to the processor SNIFF_CVDD signal (ball number AE19).

Salient Features



1) Output Capacitor Requirements
- **o Total Capacitance: >650 uF, <1100uF**
- **o Combined ESR = 5 milliOhm max**
- **o Example:**
  - **- 3, 270uF, 15 milliohm, Panasonic EEFUE0E271R**

2) Inductor Requirements (for 10A)
- **o 1.8uH, Irms >14A, Isat > 20A**
- **o Example: Panasonic ETQP6F1R8BFA**

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Size: Custom	Date: Tuesday, July 02, 2002
Author: Ron	Page 1 of 1

3.1.3 PLL Power Supply

Note
See the *Data Book* for the voltage and current requirements for this and all power supplies.

For new system designs, V_CPU_PLL for TM5500/TM5800 processors must track the core voltage from the maximum V_CPU_CORE value down to 1.0 V. The lower bound for V_CPU_PLL is 1.0 V. As the core voltage drops below 1.0 V, V_CPU_PLL must remain at 1.0 V.

V_CPU_PLL should be routed on the same side of the PCB that the processor is mounted on.

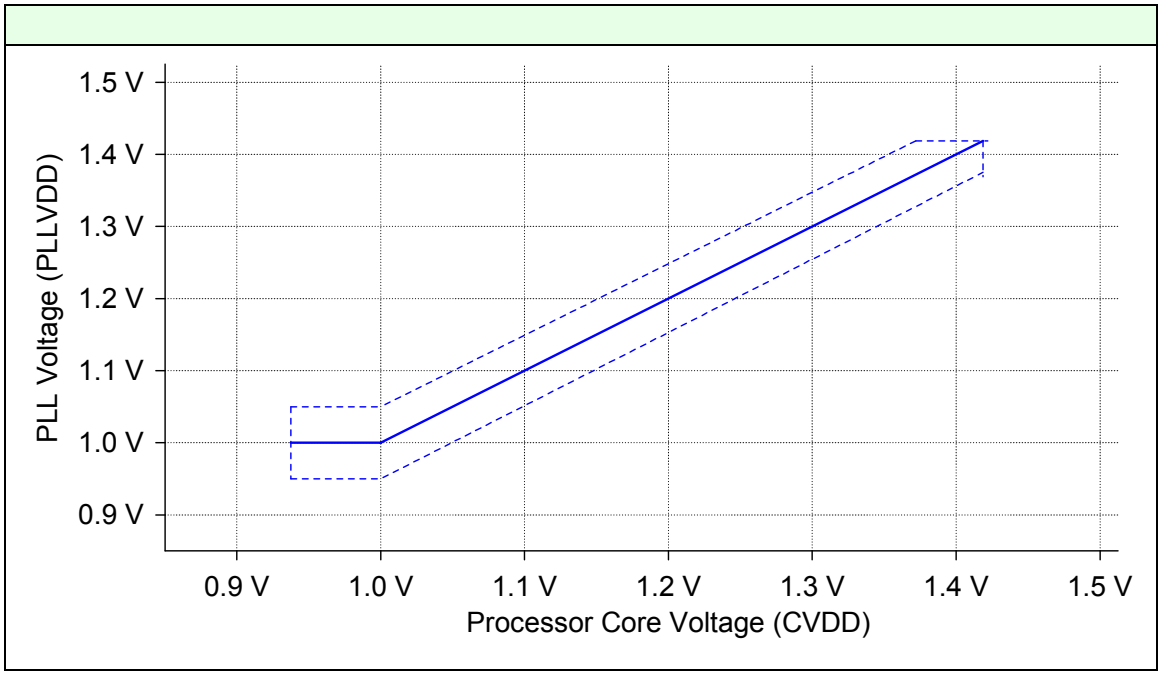
3.1.3.1 PLL Supply Core Voltage Tracking Requirement

V_CPU_PLL must track the core supply voltage, V_CPU_CORE, within ± 50 mV across a nominal core operating voltage range of 1.0 V to 1.3 V, while staying within the minimum/maximum voltage limits of each supply. V_CPU_PLL must remain at 1.0 V ± 50 mV across a nominal core operating voltage range of 0.9 V to 1.0 V.

For transitions in the core voltage (e.g. during LongRun power management voltage steps), V_CPU_PLL must settle to within the ± 50 mV V_CPU_CORE voltage tracking specification within ± 25 µS.

The figure below graphically shows the TM5500/TM5800 processor PLL power supply tracking requirement.

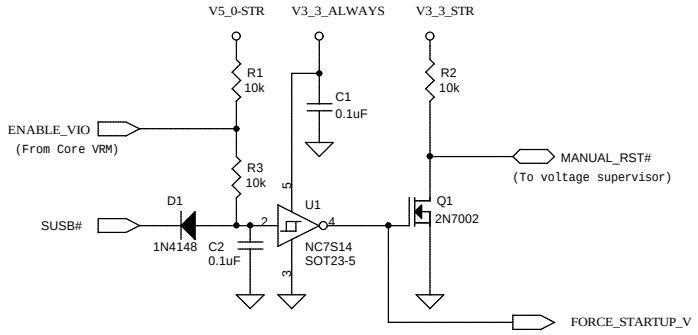
Figure 3: PLL / Processor Core Voltage Tracking Requirement



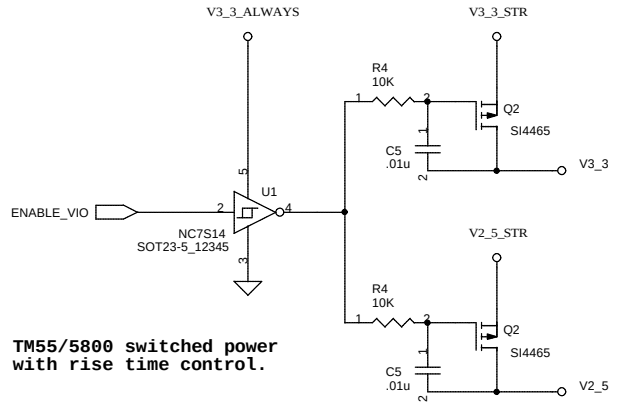
3.1.3.2 PLL Power Supply Example

A PLL power supply design example is provided below that meets the requirements shown above, providing proper V_CPU_PLL vs. V_CPU_CORE tracking. The circuit includes an enable switch, output buffer, and a low-pass noise filter.

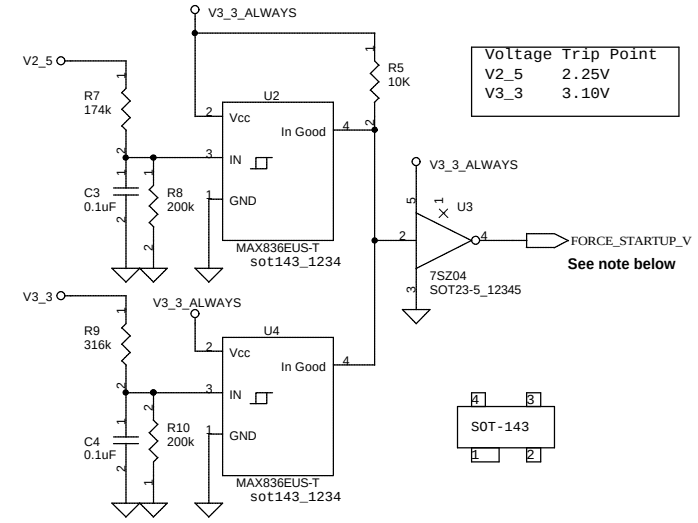
Voltage Sequence Option 1 - Delayed



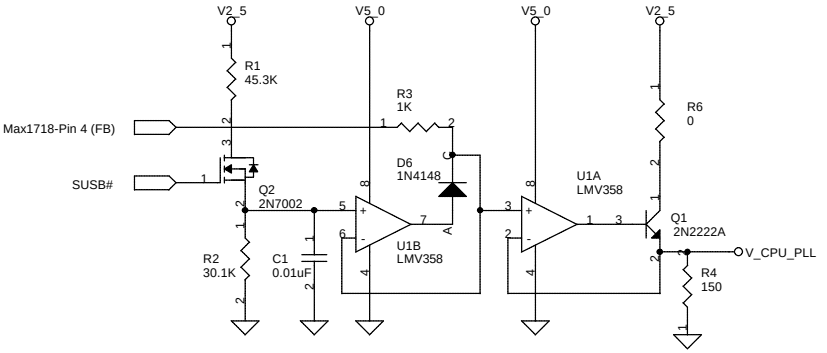
TM55/5800 switched power with rise time control.



Voltage Sequence Option 2- VI/O Monitoring



VPLL_VDD, 1V Minimum Clamping Circuit



NOTE:
Use either Voltage Sequence, Option 1 or Option 2, to generate the "FORCE_STARTUP_V" signal. Do not use both.

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Example PLL Power Supply Circuit Description

R1/Q2 and R2 form a voltage divider to create a 1.0 V reference for the minimum V_CPU_PLL operating voltage. A high on START_SEQ (typically connected to the POWERGOOD output of the V_CPU_CORE regulator) turns on the PLL supply via FET Q2. U1A and Q1 are connected as a unity-gain voltage follower so that V_CPU_PLL will equal the positive input of the opamp U1A at pin 3. U1A pin 3 is then connected to V_CPU_CORE through resistor R3. The purpose of R3 is to separate the U1A input node from V_CPU_CORE. The circuit described so far is an accurate voltage follower, where V_CPU_PLL tracks V_CPU_CORE. U1B is also connected as a voltage follower for the 1.0 V reference circuit, and D6 allows U1B to take control of the loop if V_CPU_PLL goes below 1.0 V. R4 provides a load for the U1A-Q1 follower and C2 provides a pole for the follower amp. The PLL power supply circuit should be located as close to the processor V_CPU_PLL pin as possible, and the V_CPU_PLL/GND loop length should be minimized.

Circuit Operation

During operation, the V5_0 (5.0 V) supply to the opamp and V2_5 (2.5 V) supply to Q1 must be on whenever the processor core voltage (V_CPU_CORE) is on. Normal circuit operation is as follows:

Operation above 1.0 V: U1A regulates the V_CPU_PLL output to the voltage on its positive input (pin 3). If V_CPU_CORE is higher than 1.0 V, then V_CPU_PLL follows it. This makes the negative input of U1B (pin 6) greater than the 1.0 V reference on its positive input (pin 5), driving its output (pin 7) low. When pin 7 goes low it back-biases D6, disconnecting the U1B output from the U1A positive input and allowing V_CPU_PLL to track V_CPU_CORE.

Operation below 1.0 V: When V_CPU_CORE goes below 1.0 V, V_CPU_PLL attempts to track it, causing the negative input (pin 6) of U1B to fall below the 1.0 V reference on the U1B positive input (pin 5). This in turn causes the U1B output (pin 7) to increase, which forward biases D6 and allows it to take control of the loop. U1B now regulates V_CPU_PLL to its 1.0 V reference value as long as V_CPU_CORE is below the 1.0 V reference.

3.1.3.3 PLL Voltage Requirement in New and Existing Designs

New System Designs

Note
Do not connect V_CPU_PLL to the processor core power supply (V_CPU_CORE), as was allowed for TM5400/TM5600 processors.

For new system designs, follow the new PLL voltage requirements specified above. Do not tie V_CPU_PLL to the processor core power supply (V_CPU_CORE), as was allowed with TM5400/TM5600 processors. Applications that violate the PLL voltage tracking specification are not guaranteed.

Existing (TM5400/TM5600) System Designs

For existing TM5400/TM5600 processor-based system designs, V_CPU_PLL can be tied to V_CPU_CORE, but this will limit the low voltage range for the processor core power supply (V_CPU_CORE). Applications that violate the PLL voltage tracking specification are not guaranteed.

3.1.4 I/O Power Supplies

TM5500/TM5800 processors require a 3.3 V power supply (V3_3) and a 2.5 V power supply (V2_5) to power the I/O sections of the processor. If these supplies are derived from V3_3_STR and V2_5_STR, care must be taken to ensure the voltages are not glitched when these supplies are turned on. Glitching can be minimized by controlling the turn-on rise-time of the V3_3 and V2_5 supplies.

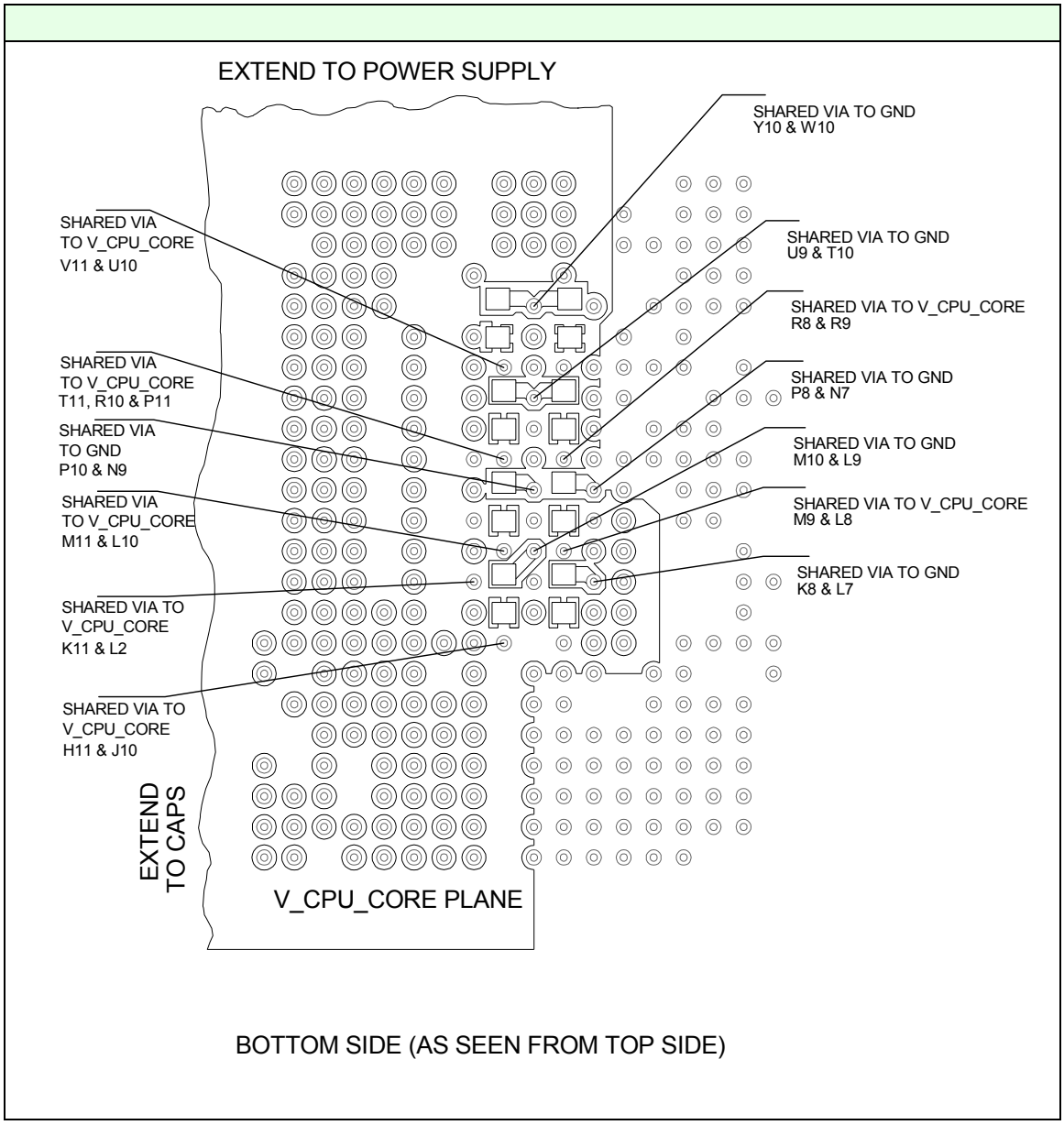
Note
See the *Data Book* for the voltage and current requirements for this and all power supplies.

Note
Power supply sequencing recommendations provided in *Power Supply Sequencing* on page 35 must be followed.

3.1.5 Decoupling Capacitors

V_CPU_CORE decoupling capacitors (8 x 0.1 µF X7R 0603) should be placed directly underneath the processor on the opposite PCB side (shown below). The V_CPU_CORE plane shown in the diagram below should extend significantly beyond the processor for connection to other peripheral decoupling capacitors.

V_CPU_CORE Underside BGA Decoupling Example



3.2 Power Supply Sequencing

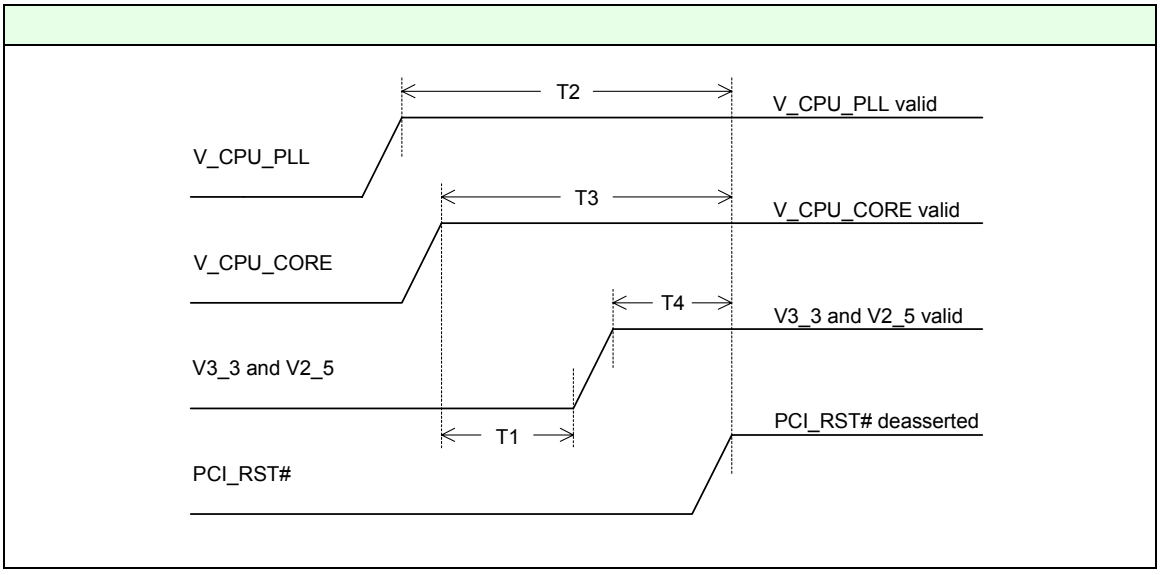
Note
See the *Data Book* for more information on power sequencing requirements for TM5500/TM5800 processors.

3.2.1 Power Sequencing Requirements

In order to prevent a high startup current condition on the processor I/O power supplies, it is required that the processor core power supply (V_CPU_CORE) be turned on first and reach a level of $V\_CPU\_CORE_{MIN}$ or greater, prior to applying the processor 2.5 V and 3.3 V I/O voltages (V2_5 and V3_3, respectively). After V_CPU_CORE has reached $V\_CPU\_CORE_{MIN}$ or greater, V3_3 and V2_5 can be supplied to the processor in any order.

A diagram of the power supply sequencing required for TM5500/TM5800 processors is shown in the figure below. System designs for TM5500/TM5800 processors must also meet the power-on requirements specified in the *Data Book*.

Figure 4: Power Supply Sequencing



The table below provides timing specifications for the power supply sequencing figure above.

Table 10: Power Supply Sequencing Timing Specifications

Timing Value	Description	Min	Max
T1	Time from V_CPU_CORE valid to beginning ramp of V3_3 and V2_5	0 mS	50 mS
T2	Time from V_CPU_PLL valid to PCI_RST# deassertion	20 mS	-
T3	Time from V_CPU_CORE valid to PCI_RST# deassertion	20 mS	-
T4	Time from V3_3 and V2_5 valid to PCI_RST# deassertion	1 mS	-

Under the above startup conditions the processor VDRA signals (that go to the VRM VID inputs) are not valid until the processor I/O voltages are present. Therefore, another method must be provided to supply valid VID signals to the VRM from the time the V_CPU_CORE core supply is enabled to the time the processor I/O voltages are within specifications. Once the processor I/O voltages are valid, the processor-suppled VDRA signals are valid and can be used to control the V_CPU_CORE core supply voltage.

When using TM5500/TM5800 processors with existing TM5400/TM5600 system designs, the existing power supply sequencing should not be used unless it meets the TM5500/TM5800 sequencing requirements described above, due to the likelihood for current surges on the I/O power supplies if the I/O voltages are applied to the processor prior to the V_CPU_CORE core supply reaching $V\_CPU\_CORE_{MIN}$.

With the previously recommended TM5400/TM5600 power supply circuit, a high current on the I/O power supply circuits has been observed for about 3-10 ms, and its magnitude can be up to the current limit of the particular 3.3 V or 2.5 V regulator used (testing has shown up to 3.5 A). The excess current is not due to I/O contention, but rather current flow through the power supply pins of the processor.

This could possibly have the following negative effects for the system:

- DDR SDRAM data corruption when exiting STR (suspend-to-RAM).
- The 2.5 V or 3.3 V regulator may go into under-voltage shutdown or over-current protection, in which case system operation may only be recoverable if power-cycled.
- The 2.5 V or 3.3 V supply voltage may dip enough to cause memory corruption and power supply latch-off.
- The current spike may trigger other system-level protection circuits or result in I/O contention.

3.2.2 Power Sequencing Circuit Examples

As explained above in *Power Sequencing Requirements* on page 35, TM5500/TM5800 processors must have the core voltage (V_CPU_CORE) turned on prior to the I/O voltages (V3_3 and V2_5). However, the processor VRDA output code presented to the VRM VID inputs is not valid until the I/O voltages reach regulation. The processor core VRM must rely on another method for setting the VRM output voltage during processor power-up.

The fundamental requirement is to force the processor core VRM to a fixed startup supply voltage by a means other than the VID inputs, and then use the VRDA outputs from the processor to control the core VRM output only when these VRDA signals are valid.

The processor core VRM designs shown in this document each have the ability to force the startup supply voltage (FORCE_STARTUP_V) without having a valid VID input code available from the processor. Two methods for using this capability are provided in the power supply sequencing reference design schematics below. Only one method is necessary for any system design, at the option of the designer. These two methods are described below:

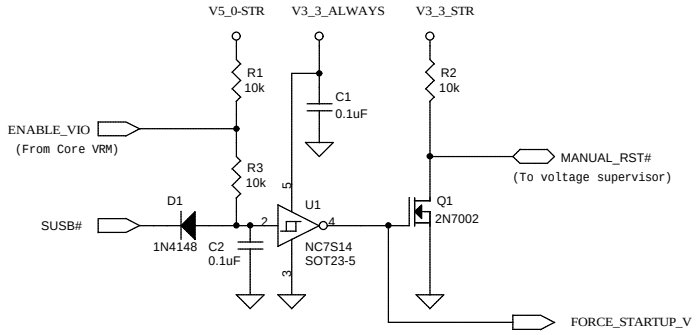
Method 1 (Delay): This method uses a delay to drive the FORCE_STARTUP_V signal long enough for the I/O voltages to reach regulation. The advantage of this solution is lower cost and fewer components than Method 2.

Method 2 (Monitor): This method measures the I/O voltages to insure they are in regulation before releasing the FORCE_STARTUP_V signal. The advantage of this method over Method 1 is that it relies on actual voltage levels for control and is not susceptible to potential delay timing variability issues.

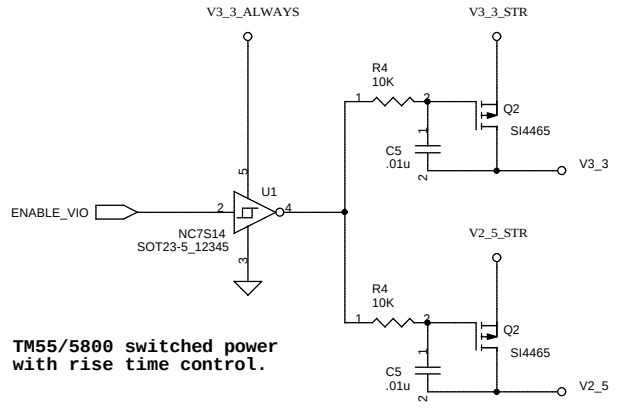
Power Supply Sequencing Reference Design Schematic

Two possible power supply sequencing circuits, as described above, are shown in the reference design schematic on the following page.

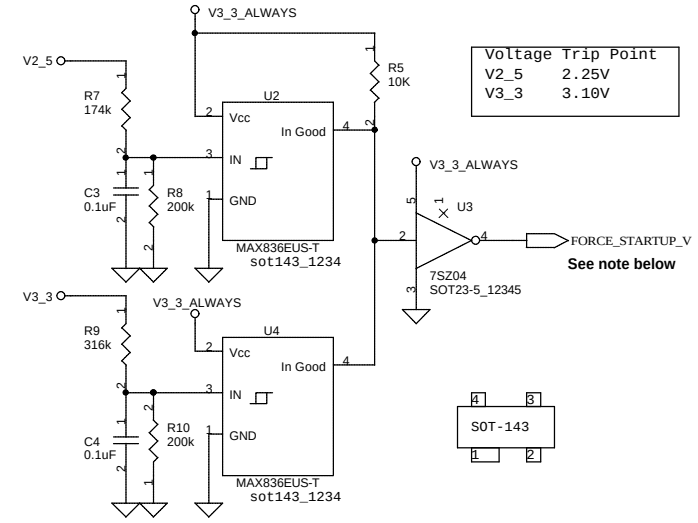
Voltage Sequence Option 1 - Delayed



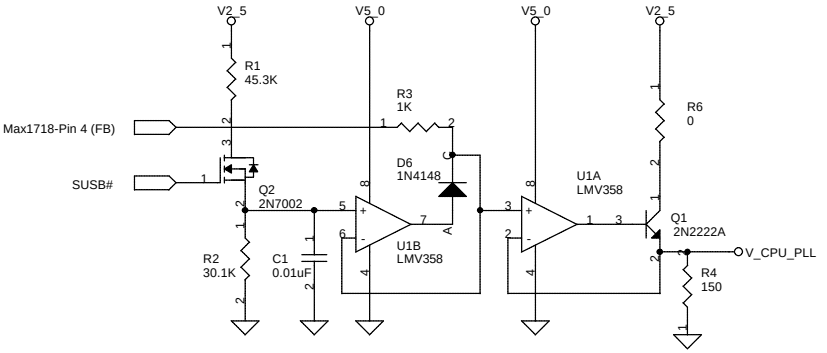
TM55/5800 switched power with rise time control.



Voltage Sequence Option 2- VI/O Monitoring



VPLL_VDD, 1V Minimum Clamping Circuit



NOTE:
Use either Voltage Sequence, Option 1 or Option 2, to generate the "FORCE_STARTUP_V" signal. Do not use both.

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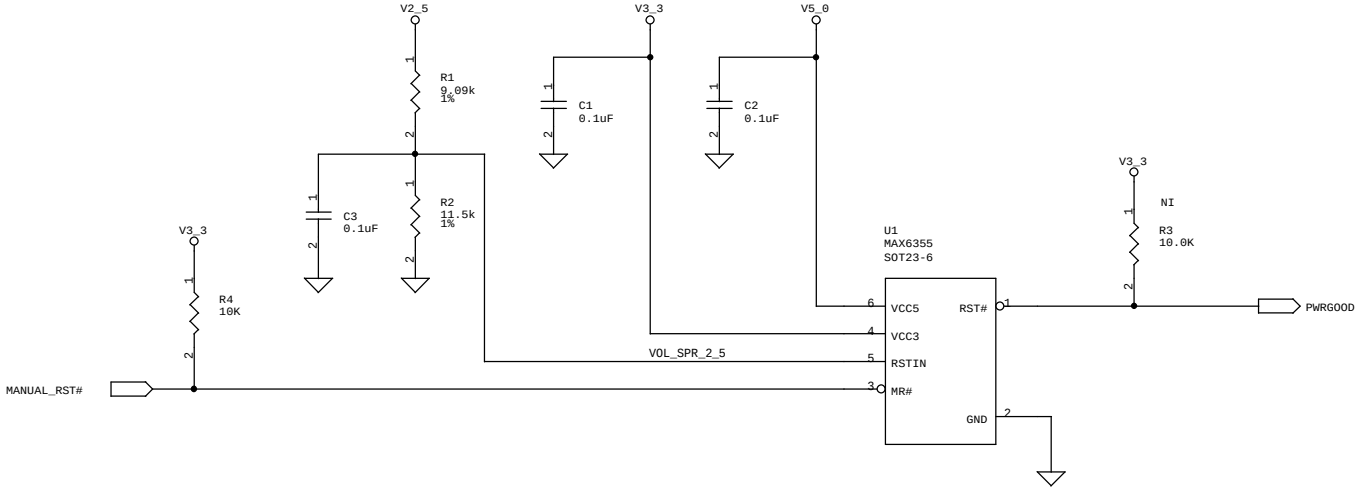
Author: RJB	Page 1 of 1

3.3 Power Supply Voltage Supervisor

The following page shows a power supply voltage supervisor reference design schematic.

TRIP POINT FOR
2_5V RAIL IS 2.19V



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Project: TM5800 Design Guide

Title: Voltage Supervisor

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Thursday, June 14, 2001 | Author: Basil | Page 1 of 1

3.4 POWERGOOD Block Diagram Example

The following page shows an example block diagram for possible system POWERGOOD circuits.

NOTE:
THIS CAN BE SYSTEM IMPLEMENTATION SPECIFIC, HOWEVER, CUSTOMERS ARE ENCOURAGED TO USE A SINGLE SYSTEM LEVEL POWERGOOD TO THE TM5800 CPU AND SOUTHBRIDGE

THE PWRGOOD OUTPUT OF THE CORE VOLTAGE REGULATOR IS USED TO ENABLE THE I/O VOLTAGES TO THE CPU *AND* CONTROL THE VOLTAGE SUPERVISOR

WHEN ENABLE_VIO/MANUAL_RST# IS HIGH, THE CORE VOLTAGE IS AT LEVEL.

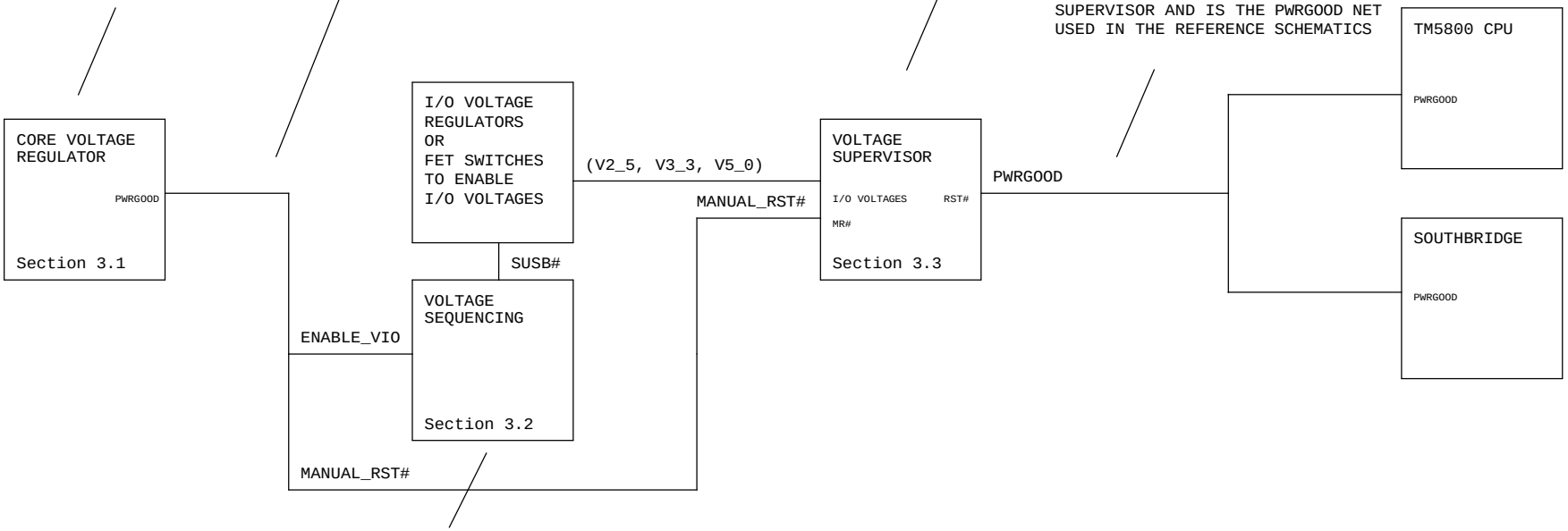
ENABLE_VIO IS THEN USED WITH THE VOLTAGE SEQUENCING CIRCUITRY TO ENABLE THE I/O VOLTAGES TO THE PROCESSOR.

MANUAL_RST# IS THEN USED TO CONTROL THE VOLTAGE SUPERVISOR.

THIS IS THE CPU CORE VOLTAGE REGULATOR

THIS SUPERVISOR MONITORS THE I/O VOLTAGES TO THE PROCESSOR

THIS IS THE RST# OUTPUT OF THE SUPERVISOR AND IS THE PWRGOOD NET USED IN THE REFERENCE SCHEMATICS



THIS CIRCUIT ENSURES THAT THE CORE VOLTAGE IS AT LEVEL PRIOR TO ENABLING THE I/O VOLTAGES TO THE CPU

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Project: TM5800 Design Guide
Title: Block Diagram Of Powergood
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3.5 State Transition Timing Requirements

This section describes the state transition timing requirements for TM5500/TM5800 processors. Note that the various signal names used in this document are typically written from the perspective of the processor. For example, STPCLK# and SLEEP# refer to the processor input signals for Stop Clock and Sleep.

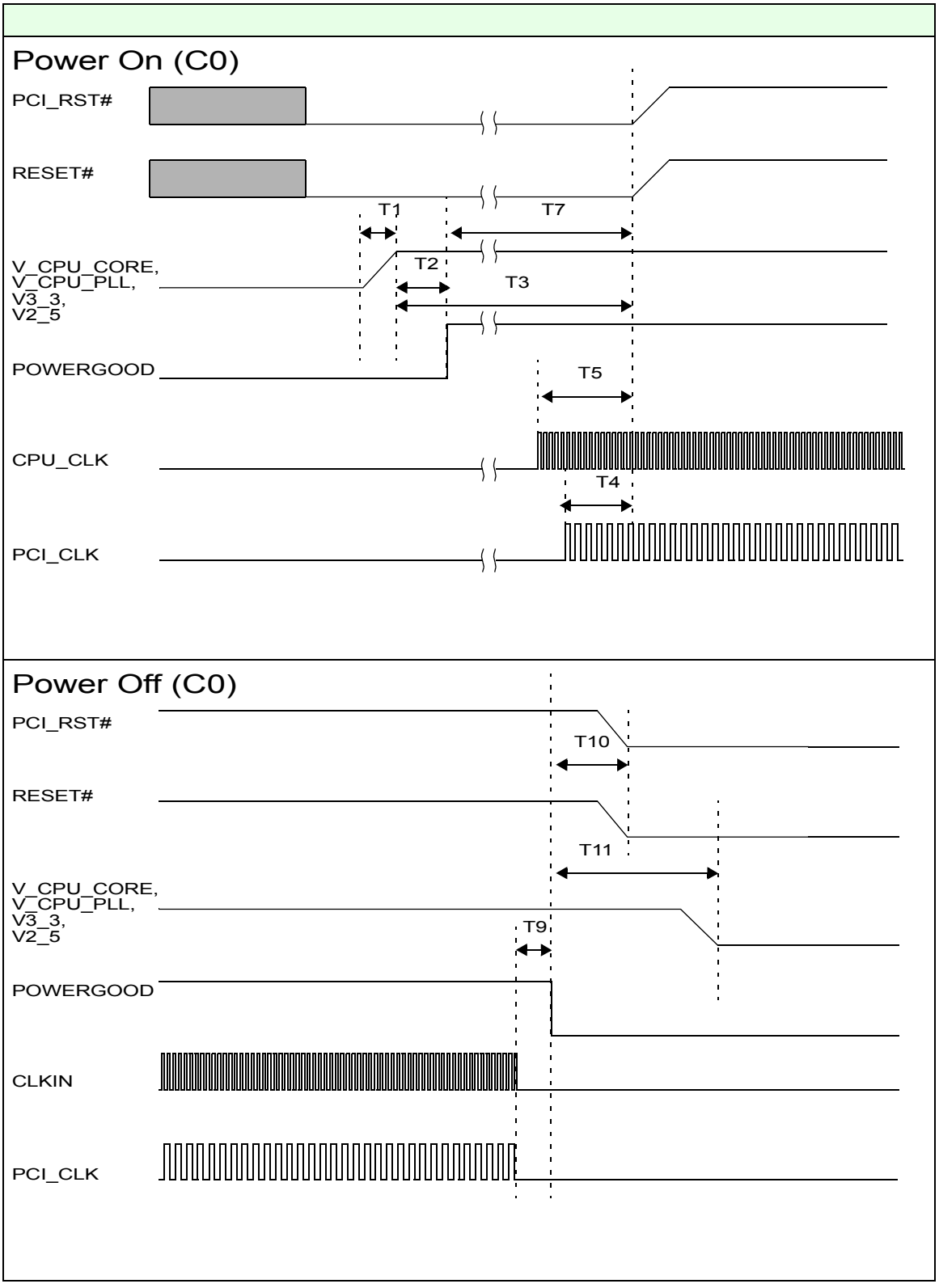
ACPI Active State (C0)

The details of the TM5500/TM5800 processor power-on sequence are described in the *Data Book* and associated references. Only the timing diagram and critical latencies for the power-on sequence are provided here.

Parameter	Description	Min	Max	Diagram Note
t_{vdd_rise}	Supply delay and rise time [1]	-	250 mS	T1
t_{vdd_pg}	POWERGOOD asserted after supplies reach 95% of final value	0 S	-	T2
t_{vdd_prst}	Supplies stable prior to PCI_RST# deasserted	1 mS	-	T3
t_{pclk_prst}	PCI_CLK stable prior to PCI_RST# deasserted	100 µS	-	T4
t_{clk_prst}	CLKIN stable prior to PCI_RST# deasserted	1 mS	-	T5
t_{prst_rst}	PCI_RST# deasserted to RESET# deasserted	0 S	-	T6
t_{pg_rst}	POWERGOOD asserted to RESET#, PCI_RST# deasserted	1 mS	-	T7
t_{pg_low}	POWERGOOD inactive pulse width	10 CLKINs	-	not shown
-	Clocks off to POWERGOOD deassertion	0 nS	-	T9
-	POWERGOOD deassertion to PCI_RST# and RESET# assertion	0 nS	-	T10
-	POWERGOOD to all voltages off	0 nS	-	T11

1. Refer to Figure 4 and Table 10 for details on power supply sequencing timing.

Refer to the above table for a description of the notes in the diagrams below. Refer to Figure 4 and Table 10 for details on power supply sequencing timing.

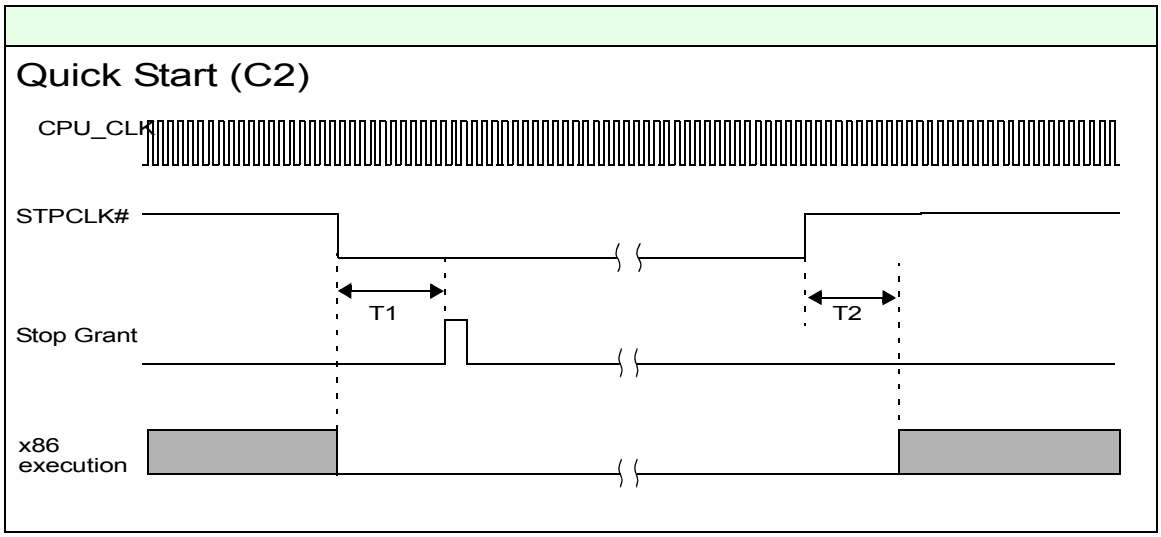


ACPI Quick Start State (C2)

The C0 to C2 transition is caused by the assertion of the STPCLK# signal. The processor issues a Stop Grant cycle in response to the STPCLK# assertion, then enters the C2 state. The C2 to C0 transition is caused by the deassertion of the STPCLK# signal.

State Transition	Timing Information/Requirements	Diagram Note
STPCLK# assertion to Stop Grant cycle	3.5 µS typical 8 µS maximum	T1
STPCLK# deassertion to C0	3 µS typical 5 µS maximum	T2

Refer to the above table for a description of the notes in the diagram below:



ACPI Deep Sleep State (C3)

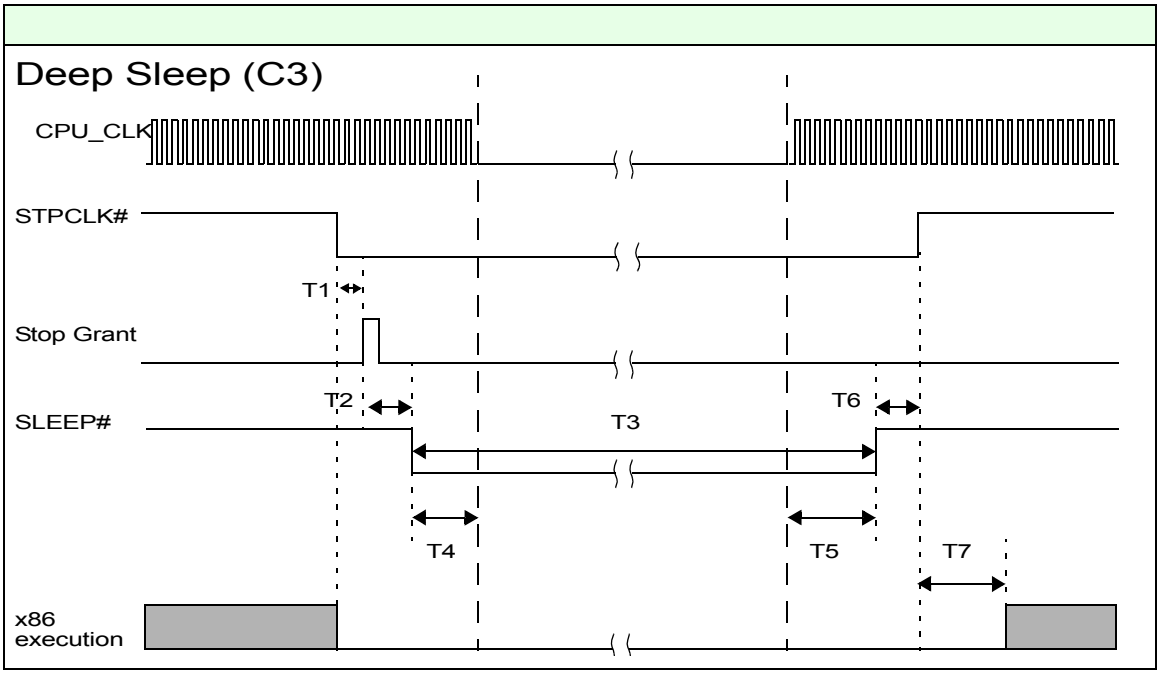
The C0 to C3 transition is caused by an I/O cycle to the power management controller, followed by the assertion of the STPCLK# signal, followed by the assertion of the SLEEP# signal, and then the shutdown of the host clock. The C3 to C0 transition is accomplished by the opposite sequence of signals (restart processor clock, deassert SLEEP#, deassert STPCLK#).

The I/O cycle that initiates the C3 power state is typically snooped by the processor. The processor integrated northbridge must be properly configured to snoop this I/O cycle, and the power management software must not use or employ any other means aside from this I/O cycle to trigger a state transition to C3. The power management controller must allow the I/O cycle to complete before asserting STPCLK#.

State Transition	Timing Information/Requirements	Diagram Note
STPCLK# assertion to Stop Grant cycle	3.5 µS typical 8 µS maximum	T1
Stop Grant to SLEEP# assertion latency	2 µS minimum	T2
SLEEP# hold time	100 nS minimum required	T3
SLEEP# assertion to host clock shutdown	17 nS minimum required	T4
Host clock restart to SLEEP# deassertion	20 µS minimum required	T5

State Transition	Timing Information/Requirements	Diagram Note
SLEEP# deassertion to STPCLK# deassertion	320 nS minimum recommended	T6
STPCLK# deassertion to C0	3 µS typical 5 µS maximum	T7

Refer to the above table for a description of the notes in the diagram below:



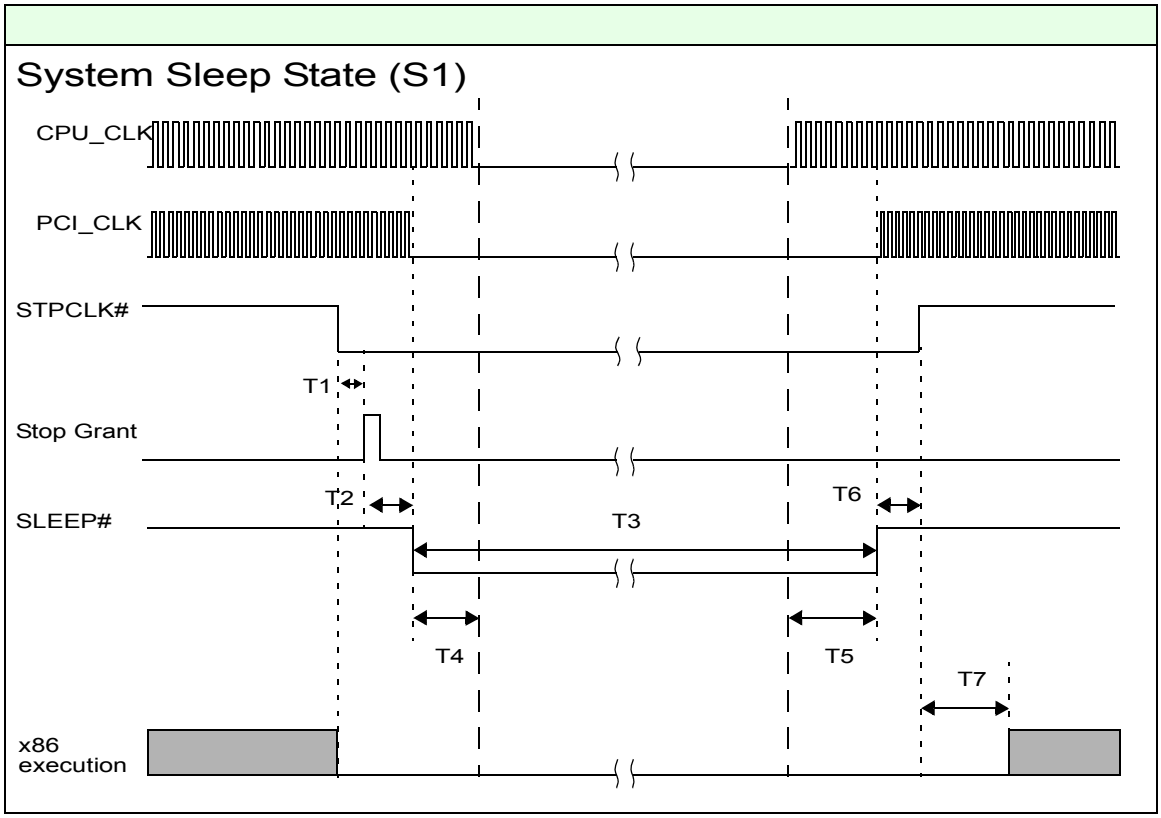
ACPI System Sleep State (S1)

The S1 signaling is like C3, except that in S1 the PCI clock is typically shut down while SLEEP# is asserted.

All the C3 requirements also apply for S1. The PCI clocks should be running any time SLEEP# is not asserted.

State Transition	Timing Information/Requirements	Diagram Note
STPCLK# assertion to Stop Grant cycle	3.5 µS typical 8 µS maximum	T1
Stop Grant to SLEEP# assertion	2 µS minimum	T2
SLEEP# hold time, PCI clock typically shut down	100 nS minimum required	T3
SLEEP# assertion to host clock shut down	17 nS minimum required	T4
Host clock restart to SLEEP# deassertion	20 µS minimum required	T5
SLEEP# deassertion to STPCLK# deassertion	320 nS minimum recommended	T6
STPCLK# deassertion to C0	3 µS typical 5 µS maximum	T7

Refer to the above table for a description of the notes in the diagram below:



ACPI Suspend-to-RAM State (S3)

The C0 to S3 transition is typically caused by an I/O cycle to the power management controller.

The I/O cycle that initiates the S3 sleep state is typically snooped by the processor. The processor integrated northbridge must be properly configured to snoop this I/O cycle, and the power management software must not use any other means aside from this I/O cycle to trigger a state transition to S3.

The processor will place the DRAMs into self-refresh by the time the I/O cycle reaches the power management controller. There are no special requirements for the power management signaling between the I/O cycle and the removal of main power.

Total System Latency

The total latency for entering and exiting the C2 and C3 states is largely a function of the overall system design. Here are some examples of system characteristics and the expected total entrance and exit latencies.

Example 1 (C2)

A system designer may implement a system with the following C2 characteristic:

- In response to a wake event from C2, the power management controller de-asserts the processor STPCLK# signal no earlier than 2 µS after receiving the Stop Grant cycle.

This type of system is expected to have a typical C2 entrance + exit latency of 8.5 µS, and a worst-case C2 entrance + exit latency of 15 µS.

Example 2 (C3)

A system designer may implement a system with the following C3 characteristics:

- The power management controller waits 64 µS after receiving the Stop Grant cycle before it asserts the processor SLEEP# signal.
- The power management controller waits 32 µS between asserting the processor SLEEP# signal and asserting the clock generator CPU_STP# signal.
- In response to a wake event from C3, the power management controller de-asserts the clock generator CPU_STP# signal no earlier than 2 µS after it asserted the clock generator CPU_STP# signal.
- The clock generator requires < 12 µS for restarting the processor CPU_CLK# upon deassertion of the clock generator CPU_STP# signal.
- The power management controller waits 32 µS between de-asserting the clock generator CPU_STP# signal and de-asserting the processor SLEEP# signal.
- The power management controller waits 64 µS between de-asserting the processor SLEEP# signal and de-asserting the processor STPCLK# signal.

This type of system is expected to have a worst-case C3 entrance + exit latency of 207 µS.

Example 3 (C3)

A system designer may implement a system with the following C3 characteristics:

- The power management controller waits 2 µS after receiving the Stop Grant cycle before it asserts the processor SLEEP# signal.
- The power management controller waits 32 µS between asserting the processor SLEEP# signal and asserting the clock generator CPU_STP# signal.
- In response to a wake event from C3, the power management controller de-asserts the clock generator CPU_STP# signal no earlier than 2 µS after it asserted the clock generator CPU_STP# signal.
- The clock generator requires < 12 µS for restarting the processor HCLK# upon deassertion of the clock generator CPU_STP# signal.
- The power management controller waits 32 µS between de-asserting the clock generator CPU_STP# signal and de-asserting the processor SLEEP# signal.
- The power management controller waits 60 nS between de-asserting the processor SLEEP# signal and de-asserting the processor STPCLK# signal.

This type of system is expected to have a worst-case C3 entrance + exit latency of 82 µS.

LongRun Power Management

LongRun power management is a power saving feature of TM5500/TM5800 processors that allows the processor to dynamically change its operating frequency and voltage in response to the instantaneous performance demands of running applications. The basic goal is to provide just-sufficient performance for the task at hand, without expending any more energy than is strictly necessary.

In Code Morphing software, LongRun power management defines up to eight *performance levels*, each consisting of a unique operating frequency and a unique operating voltage. Each successive performance level has a higher frequency and voltage than the previous one. When LongRun power management is enabled, it will raise and lower the performance level based on the amount of idle time in the system.

The algorithms that LongRun power management uses to determine when to raise or lower the performance level are fairly complex, and beyond the scope of this document. This document will only focus on how LongRun power management relates to hardware signals external to the processor.

Frequency Change Mechanism

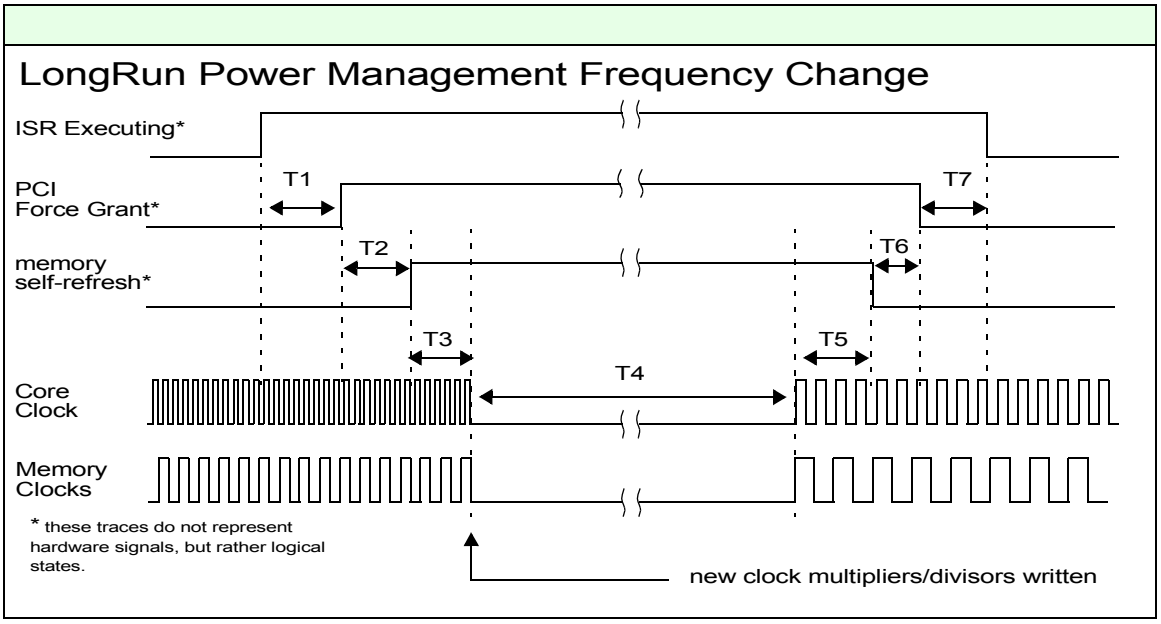
When the core and memory frequencies are changed, LongRun power management must start by ensuring that there is no external activity in the system during the frequency change. This is accomplished by flushing any queued PCI or memory writes, and force-granting the PCI bus to the processor.

In addition, since the memory frequencies may be changed at the same time as the core frequency, the memories must not be accessed during the frequency change process. LongRun power management thus places the memories into self-refresh, and then writes new multipliers/divisors for the core and memory frequencies. Then the clocks are stopped, and hardware commences the frequency change, after which the processor wakes up and starts running with the new core and memory frequencies.

Finally, the memories are brought out of self-refresh, and the force-granted PCI bus is released.

Latency	Timing Information/Requirements	Diagram Note
ISR execution to PCI Force Grant	1 µS typical 2 µS maximum	T1
PCI Force Grant to memories in self-refresh	1 µS typical 2 µS maximum	T2
Memory self-refresh to clocks off	1 µS typical 2 µS maximum	T3
PLL relock time	10 µS minimum required value configurable	T4
Clocks on to memory out of self-refresh	1 µS typical 2 µS maximum	T5
Memory out of self-refresh to PCI Force Grant deassert	1 µS typical 2 µS maximum	T6
PCI Force Grant deassert to end of ISR execution	2 µS typical 4 µS maximum	T7
Voltage regulator settling time	64 µS default value configurable [1]	T8

1. This value may be required to be set to 256 µS for some silicon revisions

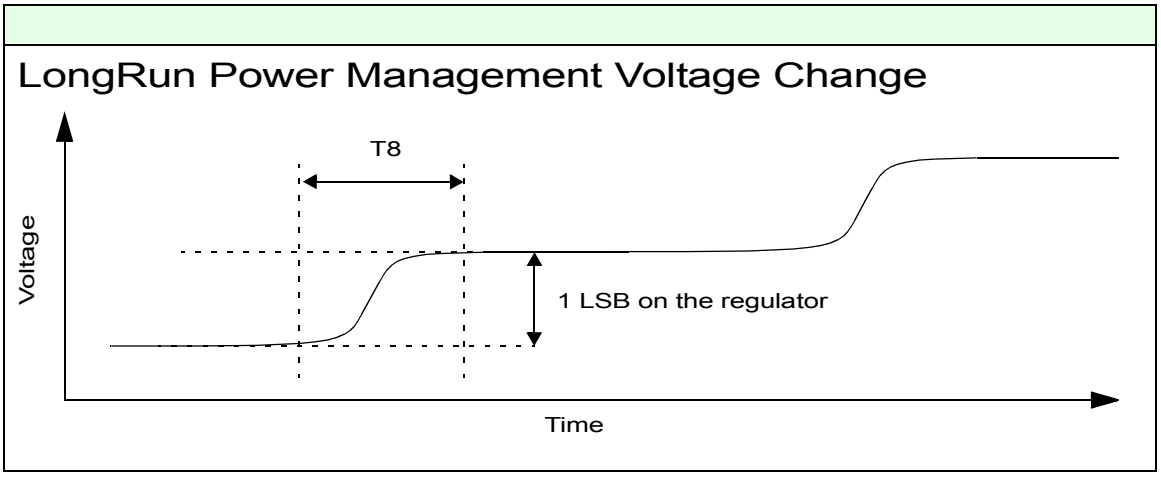


Voltage Change Mechanism

The voltage change mechanism is extremely simple when compared to the frequency change mechanism. In essence, the processor just writes a value to the 5 pins on the regulator, and the voltage changes.

The only complication from the hardware side is that some voltage regulators may deassert POWERGOOD if they change their output too rapidly, resulting in a system reset. Thus, LongRun power management only changes the voltages in 1 LSB increments, and incorporates a delay between increments to account for the regulator settling time. The default LongRun power management parameters assume a 64 µS settling time, which is compatible with the voltage regulators referenced in this document.

Note that though LongRun power management requires a minimum regulator settling time to operate correctly, this settling time does not result in processor dead time, since the processor continues to execute x86 instructions during the voltage change.



Chapter 4

DDR Memory Design

This chapter provides guidelines for implementing DDR SDRAM memory interface designs for TM5500/TM5800 processors. Following the recommended DDR memory interface design rules and layout procedures will result in reliable system designs that maximize performance while minimizing power consumption. Signal descriptions and timing specifications for the TM5500/TM5800 DDR SDRAM memory interface can be found in the *Data Book*.

4.1 DDR Memory Interface

The DDR SDRAM interface is the highest performance memory interface available on TM5500/TM5800 processors. The DDR controller supports only DDR SDRAM and transfers data at a rate that is twice the clock frequency of the interface. The DDR SDRAM controller supports the equivalent of one DIMM (one bank only) of DDR SDRAM using a 64-bit wide interface. The DDR SDRAM interface does not support parity bits.

The DDR SDRAM can be populated with 64-Mbit, 128-Mbit, 256-Mbit, or 512-Mbit devices. For the highest performance, it is recommended that the DDR SDRAM devices be soldered down to the circuit board, rather than incorporated on DIMMs. The DDR SDRAM interface supports only x8 or x16 devices. The table below shows possible TM5500/TM5800 DDR SDRAM configurations.

Table 11: DDR SDRAM Memory Configurations

DDR Device Size	DDR Device Configuration	Devices per Bank	Mbytes per Bank	Maximum Banks	Maximum Memory Size
64 Mbit	4M x 16	4	32	1	32 Mbytes
	8M x 8	8	64	1	64 Mbytes
128 Mbit	8M x 16	4	64	1	64 Mbytes
	16M x 8	8	128	1	128 Mbytes
256 Mbit	16M x 16	4	128	1	128 Mbytes
	32M x 8	8	256	1	256 Mbytes
512 Mbit	32M x 16	4	256	1	256 Mbytes
	64M x 8	8	512	1	512 Mbytes

The frequency setting for the DDR SDRAM interface is initialized during the boot sequence from data stored in the configuration ROM. DDR interface frequency settings vary at each LongRun power management step. DDR interface timing specifications and operating frequencies at various LongRun power management steps are provided in the *Data Book*. The *Data Book* also provides DDR memory interface configuration constraints, as well as recommended and example system memory configurations. See the *OEM Configuration Table* chapter of the *Development and Manufacturing Guide* for further LongRun configuration and memory frequency information.

4.2 Clock Enable Isolation

The processor DDR_CKE clock enable signals must be isolated from the DDR SDRAM. This is because power states exist where the processor is powered down and the DDR SDRAM remains powered (e.g. STR).

Since TM5500/TM5800 processors do not have a suspend power well, output signals are undefined during power transitions and subject to glitching. The SUSPEND_STATUS signal from the southbridge remains asserted while in STR mode, and is therefore used to control the isolation switches.

4.3 Signal Termination

Series termination is recommended on all signals. Termination impedance should be calculated on a per-design basis.

4.4 DDR Reference Voltage

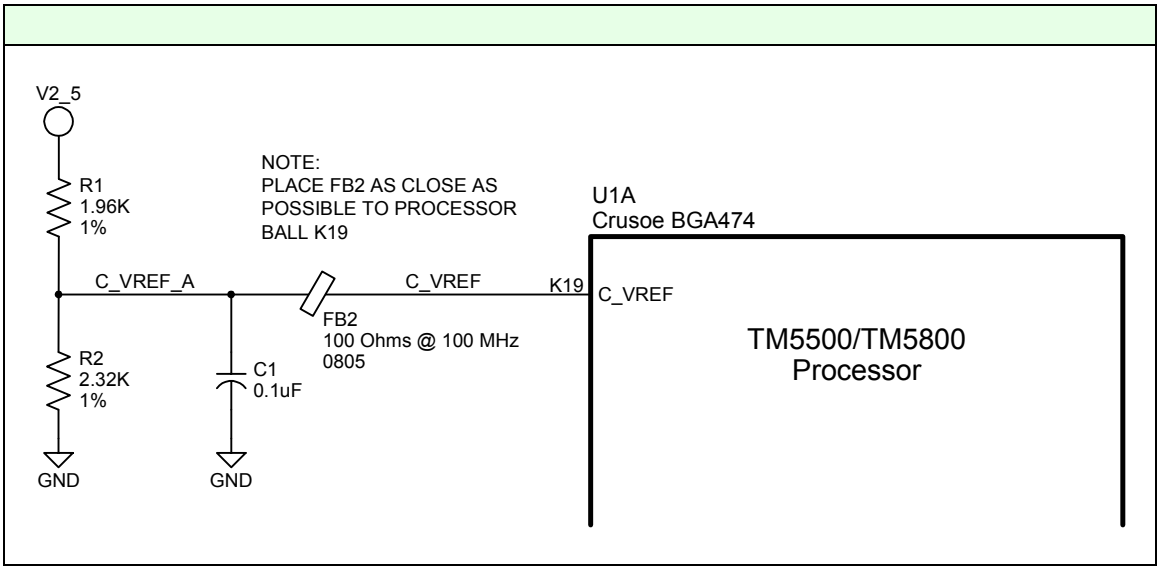
The VDDIO25 power supply pins of the processor are connected to V2_5. The DDR interface has a DDR_VREF pin whose input should be derived from that power supply using a 1% resistor voltage divider. The specification for this input is described in the *Data Book*. Two examples are provided below for selecting DDR_VREF divider resistor values.

- For a DDR_VREF specification of 1.25 V, the recommended V2_5 voltage divider network for deriving DDR_VREF is: upper resistor (tied to V2_5) = 2490 Ω, and lower resistor (tied to ground) = 2490 Ω.
- For a DDR_VREF specification of 1.35 V, the recommended V2_5 voltage divider network for deriving DDR_VREF is: upper resistor (tied to V2_5) = 1960 Ω, and lower resistor (tied to ground) = 2320 Ω.

4.4.1 DDR Reference Voltage Noise Filter Circuit

TM5500/TM5800 processors require a ferrite bead noise filter on the C_VREF DDR interface reference voltage signal. C_VREF is derived from IOVDD25 (2.5 V I/O power supply) using a resistive voltage divider. The recommended noise filter circuit is shown below.

Figure 5: Recommended DDR Reference Voltage Circuit with Ferrite Bead Noise Filter



4.5 DDR Memory Interface Design Guidelines

The DDR SDRAM interface operates at frequencies of 100-133 MHz. Use standard high-speed design, layout, and routing practices. Some specific guidelines in DDR memory layout are provided below.

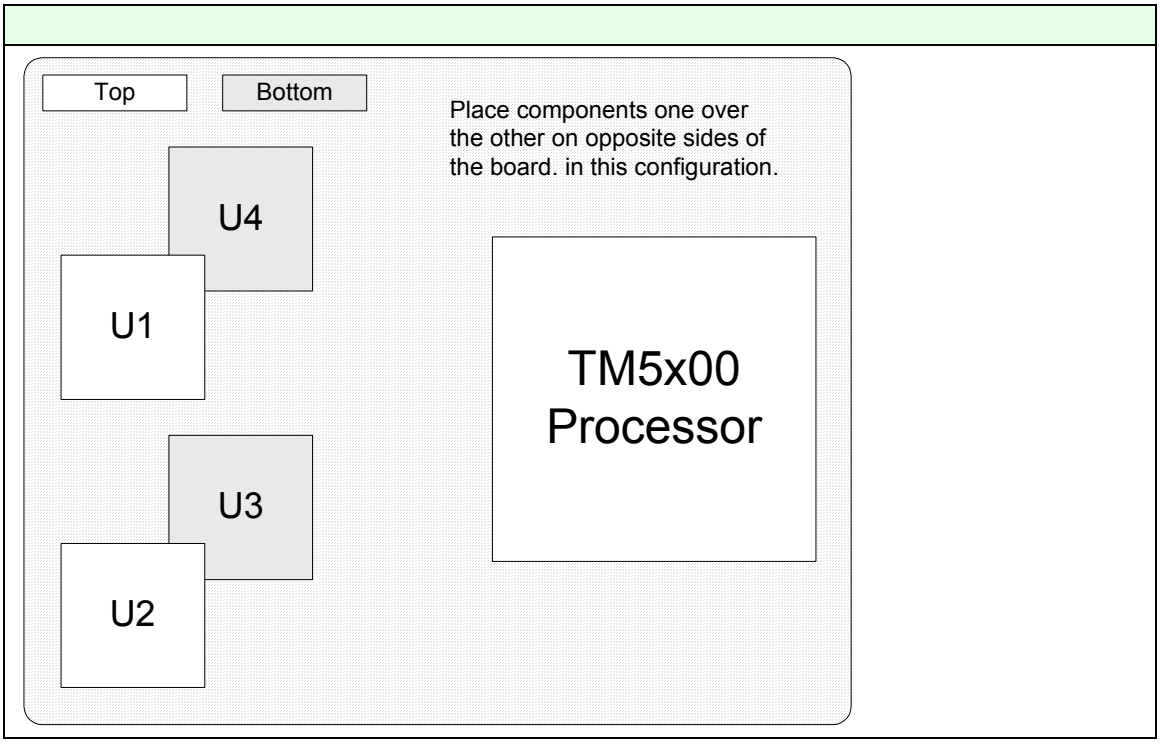
- To achieve the most ideal DDR layout possible, the TM5500/TM5800 DDR interface and memory layout should be completed first, with trace lengths as short as possible, before other sections of the design layout complicate DDR signal routing.
- A nominal DDR SDRAM layout must have trace lengths less than 4”.
- Data traces are routed in groups. Each group consists of one DDR_DQS, one DDR_DQMB, and eight DDR_DQ lines.
- The DDR_DQ and DDR_DQMB signals within each group must be routed such that the maximum difference in their lengths is 0.4” or less. The DDR_DQS signal for the group must have a length that is within 0.1” of the longest other trace in that group. The length of all DQS signals must be within a 2” range and within 1” of the length of the clocks.
- The differential clocks (DDR_CLKA/A#, DDR_CLKB/B#) must be routed such that the length of each clock signal to each SDRAM is the same length within 0.05”. The length of the clocks must be within 1.0” of all DQS signals.
- All byte groups may be swapped with other byte groups and all data bits within each byte may be swapped to facilitate meeting length requirements.
- Characteristic impedance should be 60 Ω ± 10%.
- Layout components as shown in the example below. The components should be exactly on top of one another in the following specified order. Devices 0-1 get differential clock pair DDR_CLKA/DDR_CLKA# and devices 2-3 get differential clock pair DDR_CLKB/DDR_CLKB#.

4.6 PCB Placement and Routing Example

Device Placement

The figure below shows the recommended TM5500/TM5800 processor and four DDR memory device placement using both sides of the PCB.

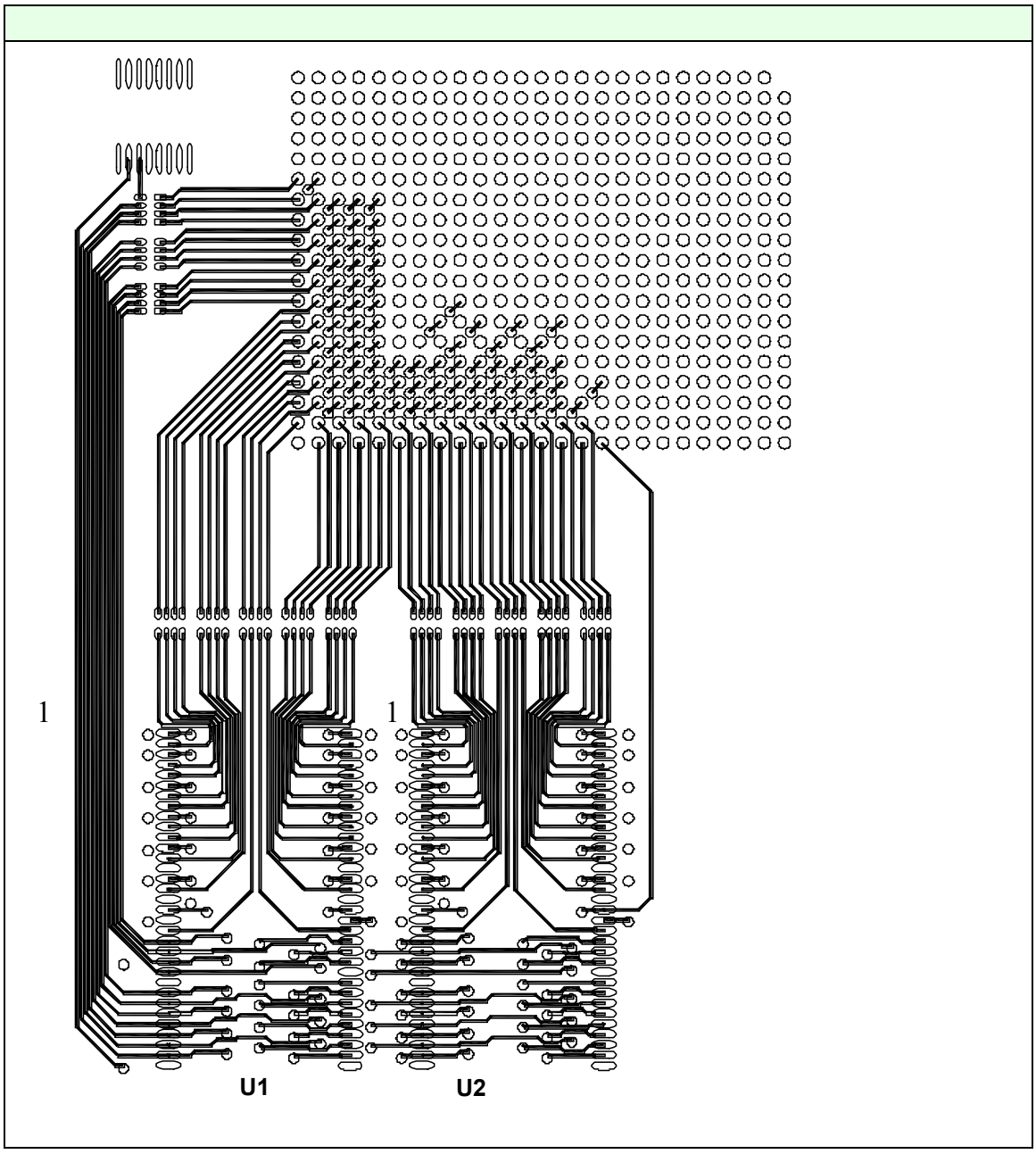
Figure 6: Recommended 4-Device DDR Memory Chip Placement



Primary Side (Top Layer) Signal Routing

The figure below shows the connections from the TM5500/TM5800 processor to the DDR memory on the primary (top layer) side of the board.

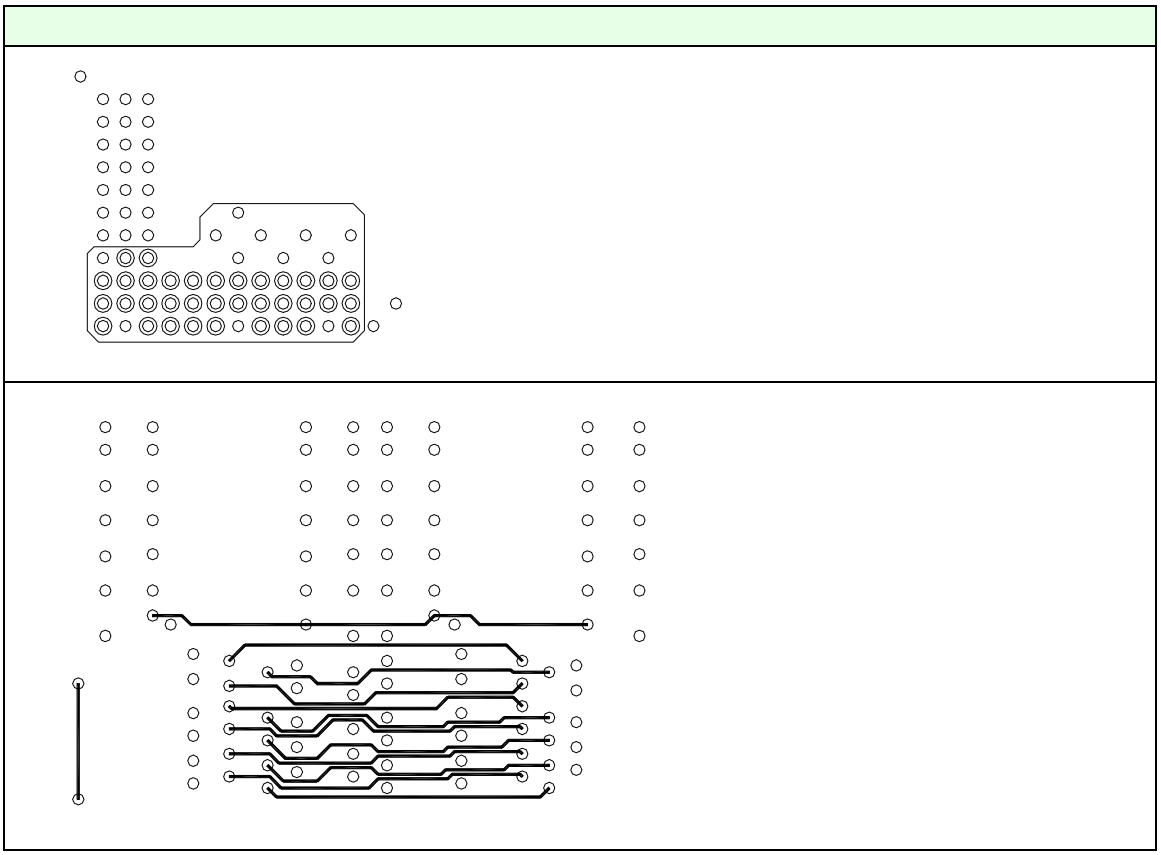
Figure 7: Recommended 4-Device DDR Memory Signal Routing - Top Layer



Internal Layer Signal Routing

The figure below shows the connections from the TM5500/TM5800 processor to the DDR memory on an internal layer of the board.

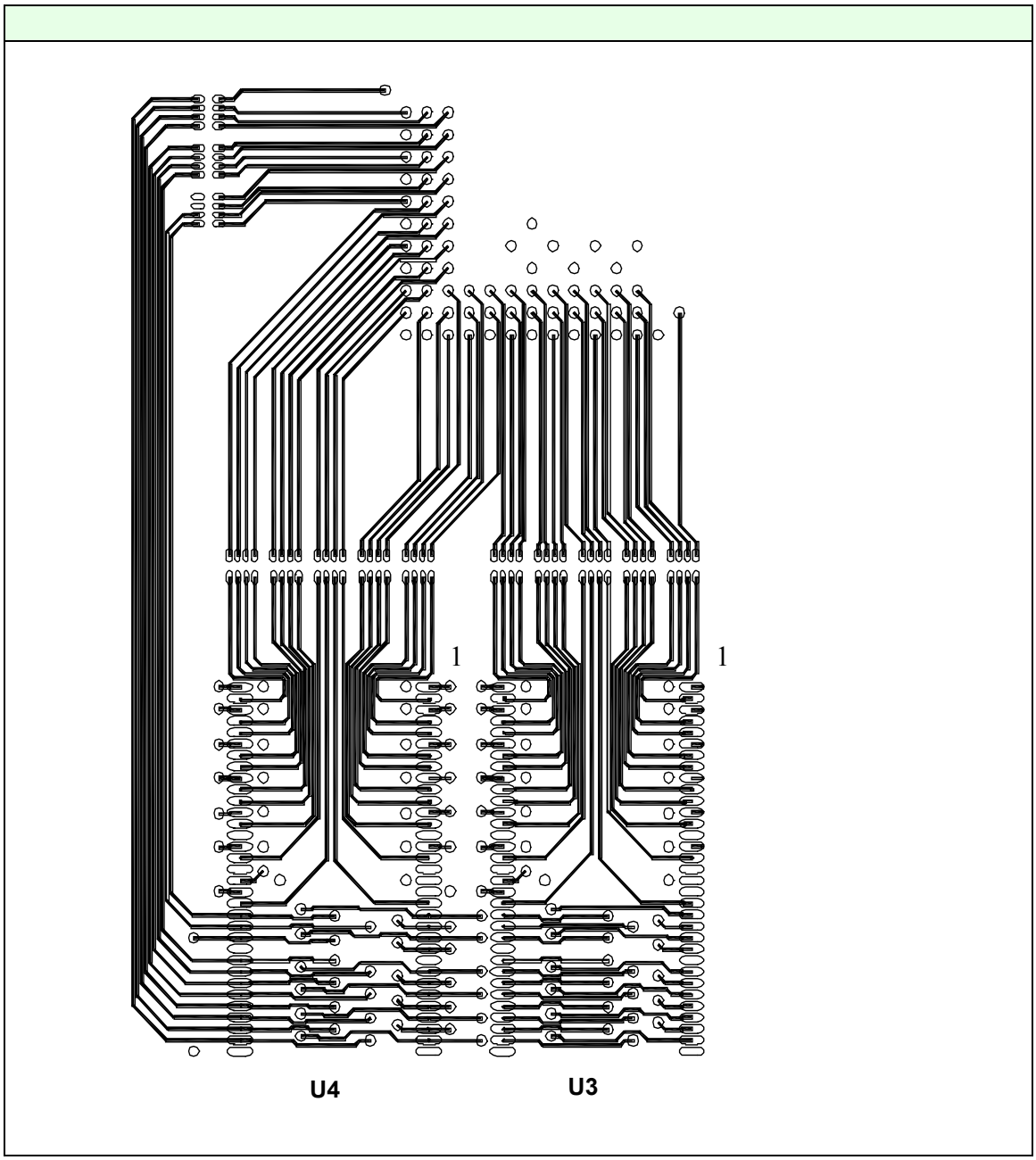
Figure 8: Recommended 4-Device DDR Memory Signal Routing - Internal Layer



Secondary Side (Bottom Layer) Signal Routing

The figure below shows connections from the TM5500/TM5800 processor to the DDR memory on the secondary (bottom layer) side of the board.

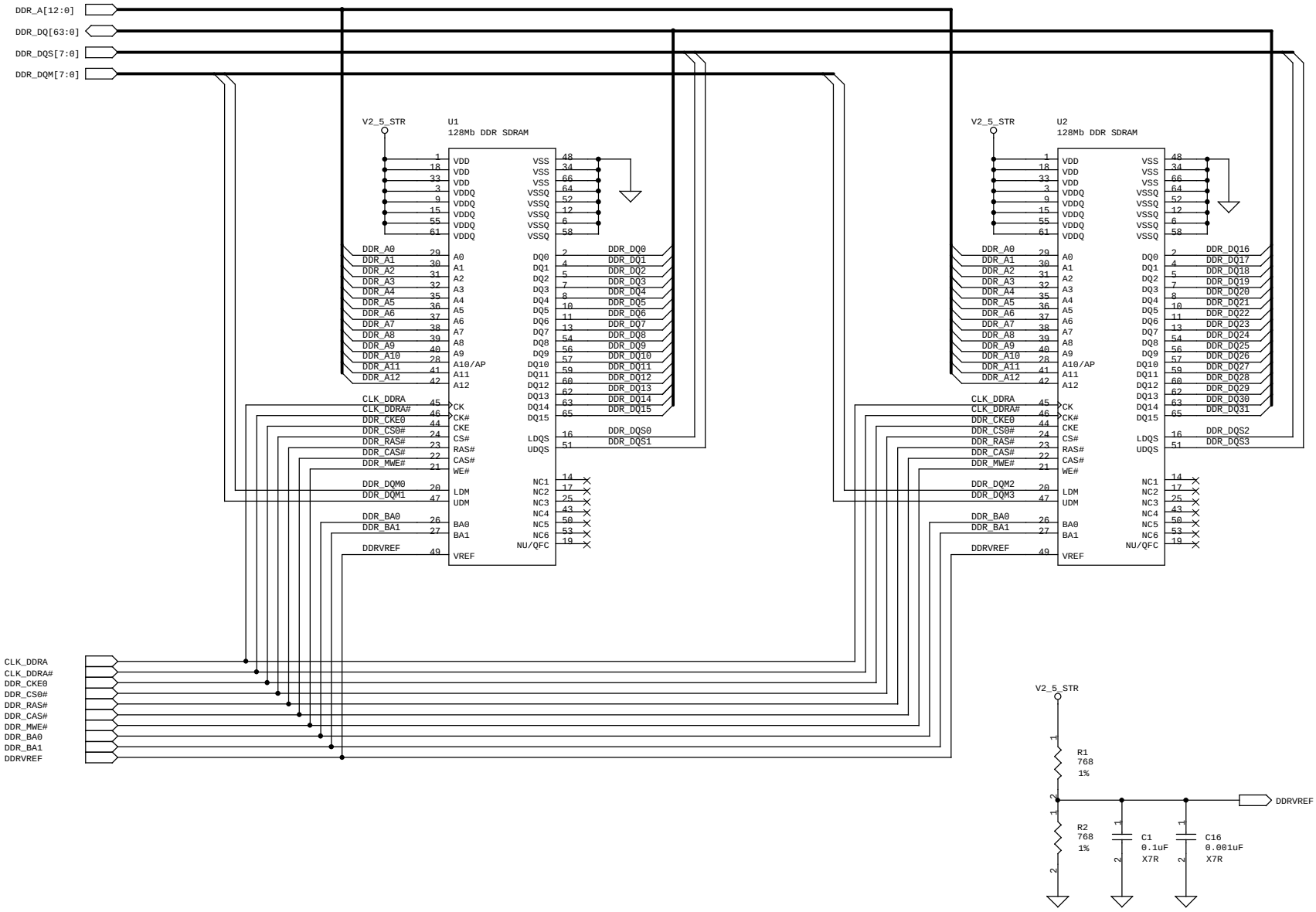
Figure 9: Recommended 4-Device DDR Memory Signal Routing - Bottom Layer



4.7 DDR SDRAM Schematics

The following pages show DDR SDRAM reference schematics.

- Single bank DDR soldered down (2 pages)
- Single bank DDR SODIMM (2 pages)
- DDR clock enable isolation circuit (1 page)



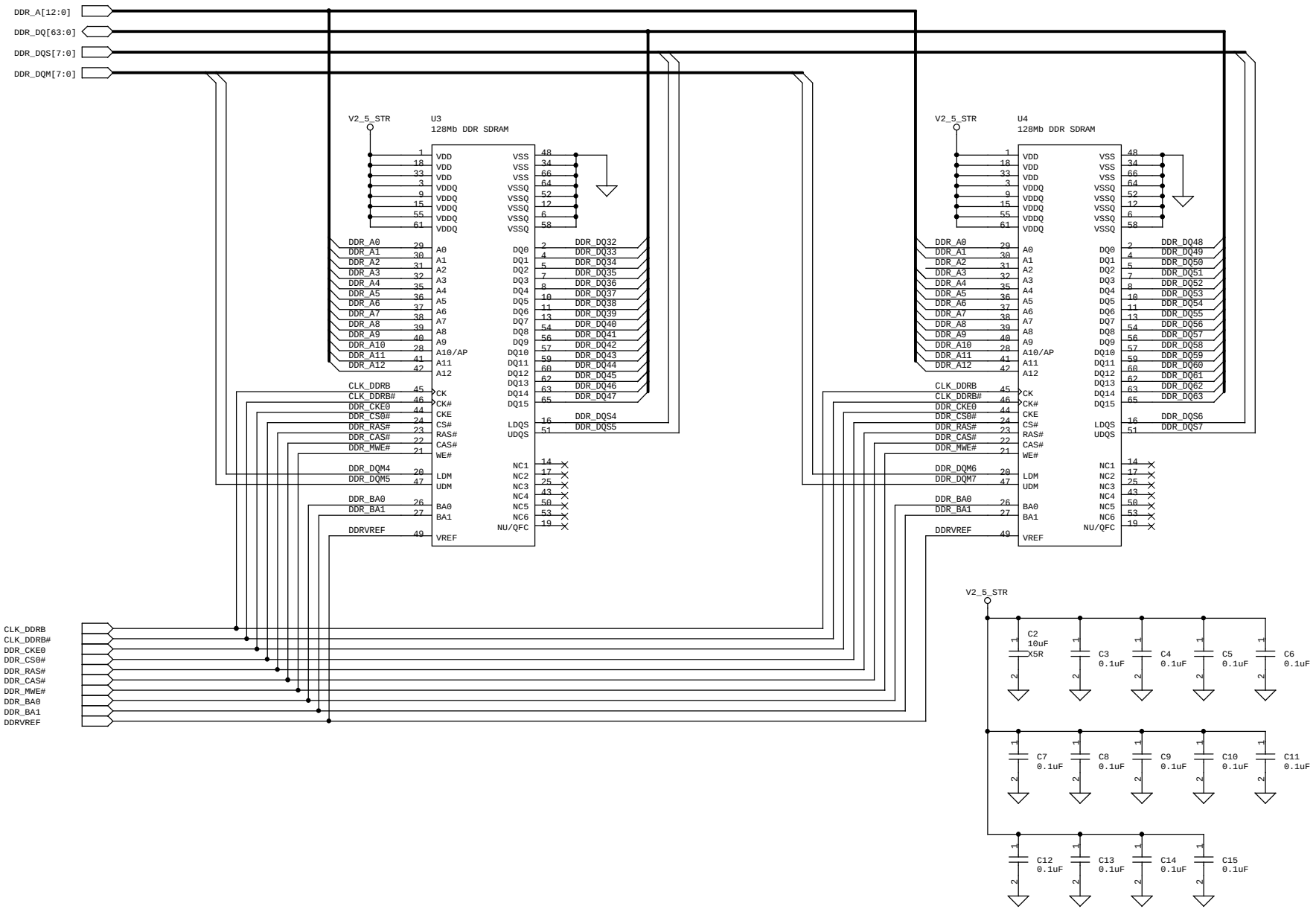
TRANSMETA Corporation
3940 Freedom Circle
Santa Clara, CA. 95054
(408) 919-3000

Project: TM5800 Design Guide

Title: Single Bank DDR Down (1/2)

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Friday, November 30, 2001 | Author: Basil | Page 1 of 2



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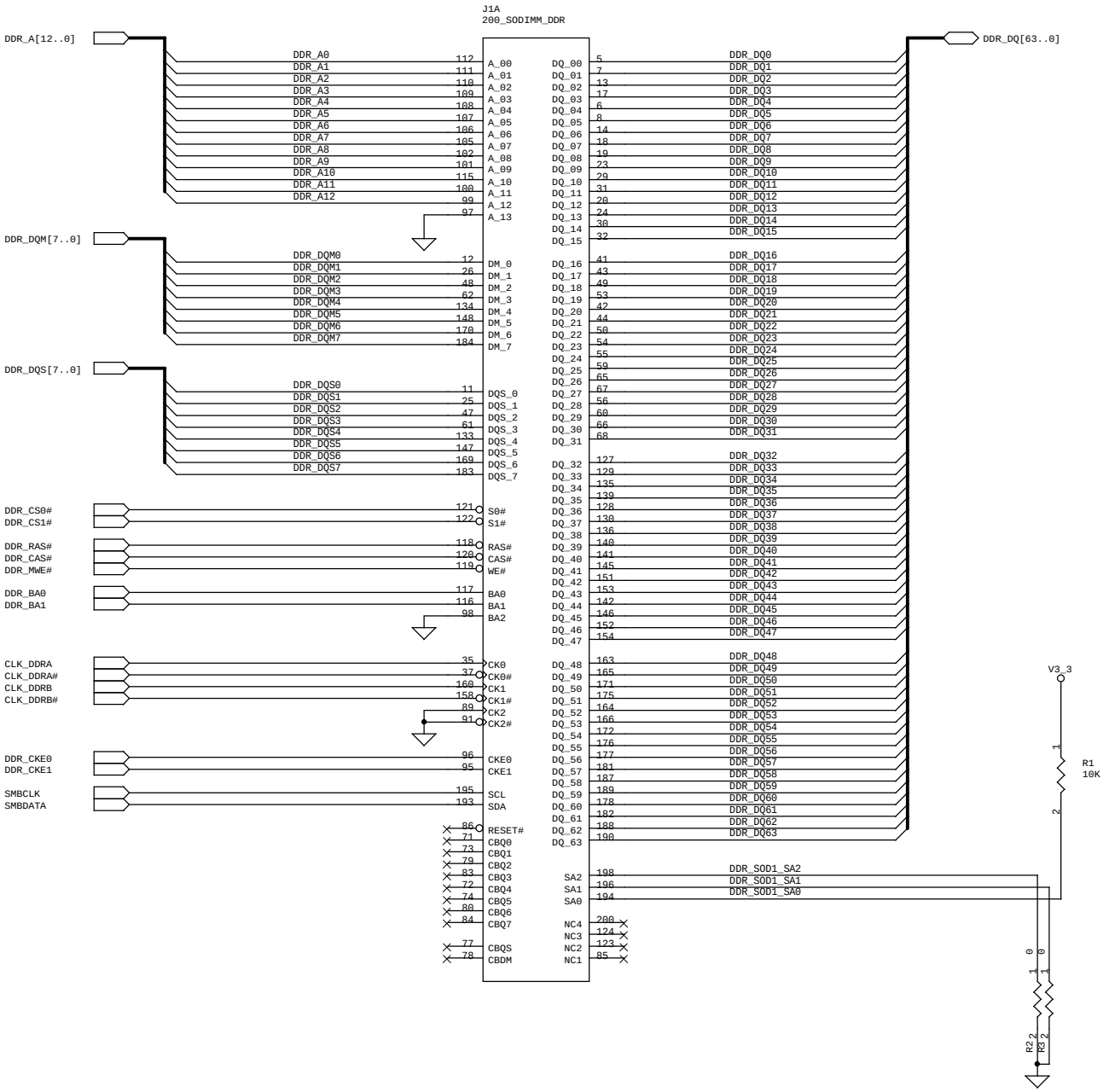
Project: TM5800 Design Guide

Title: Single Bank DDR Down (2/2)

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Thursday, June 14, 2001 | Author: Basil | Page 2 of 2



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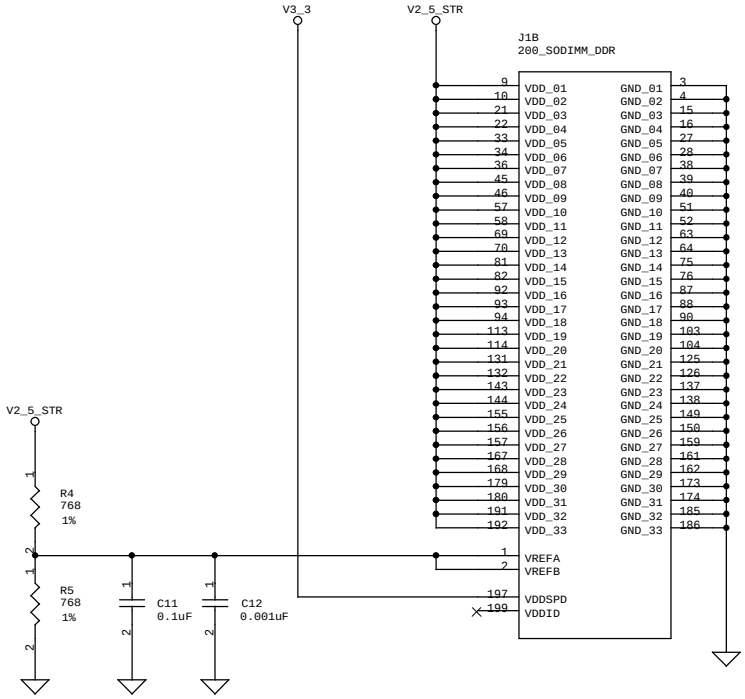
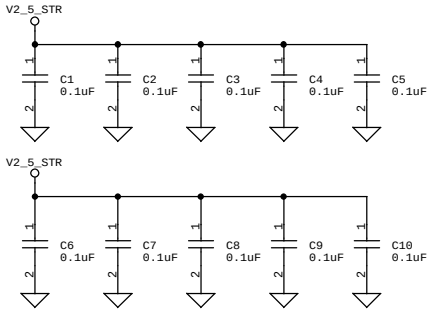
Project: TM5800 Design Guide

Title: Single DDR SODIMM (1/2)

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Thursday, June 14, 2001 | Author: Basil | Page 1 of 2





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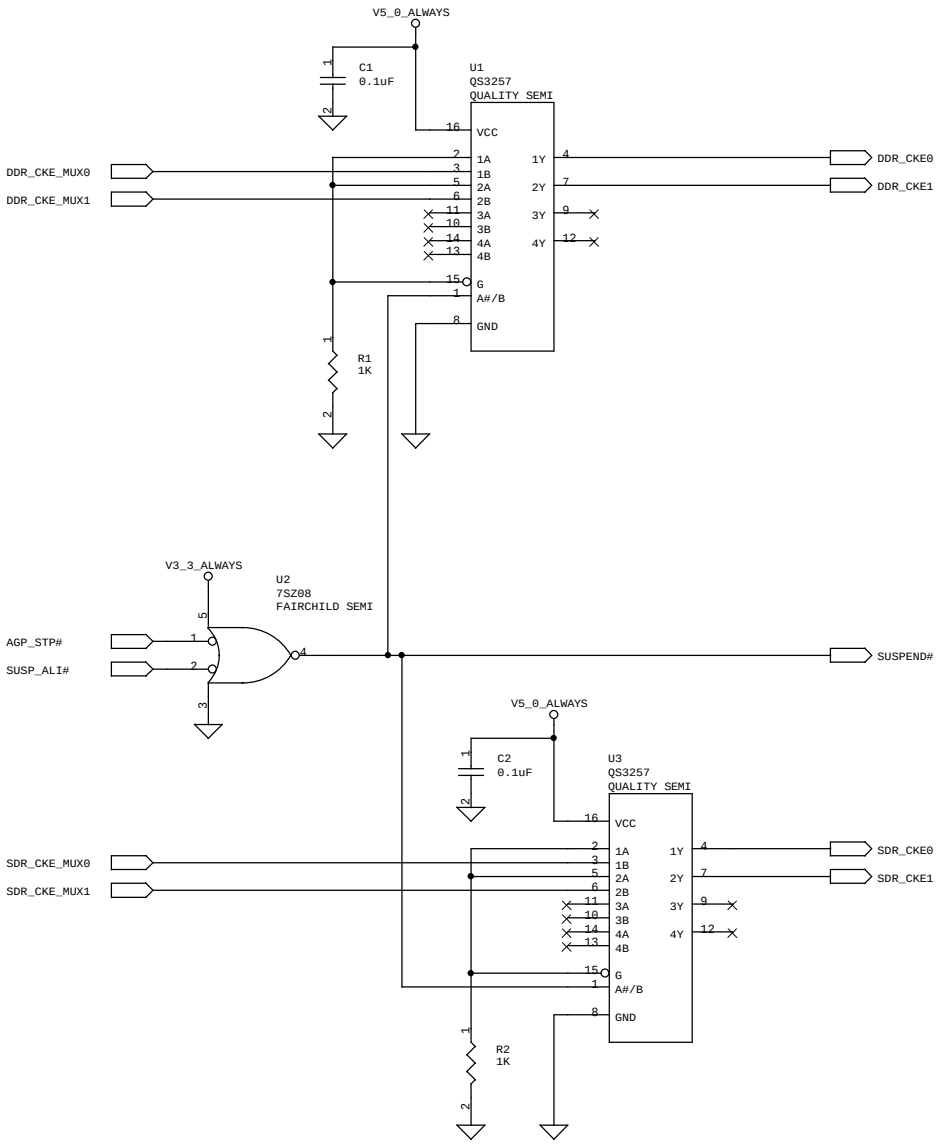
Project: TM5800 Design Guide

Title: Single DDR SODIMM (2/2)

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Tuesday, August 14, 2001 | Author: Basil | Page 2 of 2

TWO DISCRETE QUICKSWITCHES ARE USED
TO FACILITATE LAYOUT PLACEMENT.



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3940 Freedom Circle
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Project: TM5800 Design Guide

Title: CKE Quickswitch

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Thursday, November 29, 2001 | Author: Basil | Page 1 of 1

Chapter 5

SDR Memory Design

This chapter provides guidelines for implementing SDR SDRAM memory interface designs for TM5500/TM5800 processors. Following the recommended SDR memory interface design guidelines and layout procedures will result in reliable system designs that maximize performance while minimizing power consumption. Signal descriptions and timing specifications for the TM5500/TM5800 SDR SDRAM memory interface can be found in the *Data Book*.

5.1 SDR Memory Interface

The SDR SDRAM controller supports up to two 64-bit DIMMS (up to four banks) of single data rate SDRAM. The SDR SDRAM interface does not support parity bits. SDR SDRAM DIMMs can be populated with 64-Mbit, 128-Mbit, 256-Mbit, or 512-Mbit devices. All DIMMs must use the same frequency SDRAMs, but there are no restrictions on mixing different DIMM configurations into the two DIMM slots.

Table 12 shows possible SDR SDRAM configurations for a TM5500/TM5800 processor-based system. The maximum memory size in Table 12 assumes two double-sided DIMMs of identical configuration and a maximum of 8 total devices per DIMM.

Table 12: SDR SDRAM Memory Configurations

SDR Device Size	SDR Device Configuration	Devices per Bank	MBytes per Bank	Maximum Banks	Maximum Memory Size
64 Mbits	4M x 16	4	32	4	128 MBytes
	8M x 8	8	64	2	
	16M x 4	16	128	1	
128 Mbits	8M x 16	4	64	4	256 MBytes
	16M x 8	8	128	2	
	32M x 4	16	256	1	
256 Mbits	16M x 16	4	128	4	512 MBytes
	32M x 8	8	256	2	
	64M x 4	16	512	1	
512 Mbits	32M x 16	4	256	4	1024 MBytes
	64M x 8	8	512	2	

The frequency setting for the SDR SDRAM interface is initialized during the boot sequence from data stored in the configuration ROM. SDR interface frequency settings vary at each LongRun power management step. SDR interface timing specifications and operating frequencies at various LongRun power management steps are provided in the *Data Book*. The *Data Book* also provides SDR memory interface configuration constraints, as well as recommended and example system memory configurations. See the *OEM Configuration Table* chapter of the *Development and Manufacturing Guide* for further LongRun configuration and memory frequency information.

5.2 SDR Memory Interface Design Guidelines

The SDR SDRAM interface operates at frequencies up to 133 MHz and with edge rates as fast as 100 pS. Use careful high-speed design, layout, and routing practices to minimize inductance and crosstalk, maintaining the integrity of the transmission line structure throughout. Some specific guidelines for SDR memory layout are provided below.

- Place the memory as close as possible to the processor and oriented to reduce routing lengths.
- A nominal SDR layout is based on the total trace length of any SDR address or command signal (motherboard plus DIMM, if used). For a given number of loads, the rules are as follows:
  - For up to 16 loads the maximum total trace length must be <= 5”.
  - For up to 12 loads the maximum total trace length must be <= 8”.
- Source termination of 33 Ω (at the processor) is recommended for the data and mask signals.
- Source termination of 10 Ω (at the processor) is recommended for the address and command signals.
- The clock signals should be of matched lengths. Source termination of 22 Ω (at the processor) is recommended for the clock signals.
- The SDR_CLKOUT signal should have a 33 Ω source termination resistor. The trace routing from the output of this resistor to the SDR_CLKIN processor input is a timing delay. This trace length should be equal to the sum of the total length of a clock trace and the length of the shortest data signal route. This is explained in detail in *SDR SDRAM Layout Notes* on page 67.
- Characteristic impedance should be 55 Ω ± 10% for SDR-only systems. If DDR is present, the characteristic impedance should be 60 Ω ± 10%.
- For specific information about memory timing, see the *Data Book*. Refer to the *Development and Manufacturing Guide* for additional information on memory configuration.

5.2.1 Bank Selection

The memory banks are selected with the SD_CS[3:0] signals. Use them in-order from highest to lowest. For example, if only one bank of memory is used, connect it to SD_CS[3]. For one DIMM, which may have two banks, connect SD_CS[3:2]. If both soldered-down memory and DIMM are used, connect the highest-order bits to the soldered-down memory.

5.2.2 Clock Enable Isolation During Power-down States

The processor SD_CKE[3:0] clock enable signals must be isolated from the SDR SDRAM. This is because power states exist where the processor is powered down and the SDR SDRAM remains powered (e.g. STR). The processor does not have a suspend power well, and like any CMOS circuit, the outputs are undefined for short periods of time during power transitions. It is likely that all the signals glitch as power is applied or removed from the processor. If the clock enable signal on the SDRAM remains at a stable state, preventing activity within the SDRAM during power transitions, data integrity is maintained.

The SUSPEND_STATUS signal from the southbridge remains asserted while in STR mode, and is therefore used to control the isolation. The output should multiplex between a pull-down resistor and the SD_CKE signal from the processor, controlled by SUSPEND_STATUS.

5.2.3 Signal Termination

Series termination is recommended for all signals. Termination impedance should be calculated on a per-design basis.

5.2.4 Miscellaneous Notes

If DIMMs are used, the serial presence detect (SPD) bus must be connected to the southbridge (not shown in the block diagram).

All SDR SDRAM power supply inputs should be connected to V3_3_STR.

5.3 SDR SDRAM Layout Notes

This section describes procedures and guidelines for implementing SDR memory interface designs for TM5500/TM5800 processors. Following the recommended SDR memory interface design rules and layout procedures will result in reliable system designs that maximize performance while minimizing power consumption.

5.3.1 SDR SDRAM Memory Interface Timing

The TM5500/TM5800 processor SDR SDRAM memory controller is capable of addressing up to four banks of memory. The SDRAM configuration and size of each bank may be different.

The four clocks from the memory controller are copies of the SDR SDRAM clock. It does not matter which clock goes to which bank, as bank selection is done with the CKE# and select lines. The clocks always have four loads, making their behavior very predictable.

The critical timing parameters of the processor memory controller and SDR SDRAM devices are shown in Table 13. The design rules described in this document satisfy these timings.

Table 13: SDR SDRAM Interface Device Specifications

Device	Output Hold Time	Input Setup Time	Input Hold Time
TM5500/TM5800 (800 MHz SKU) [1]	1.38-1.96 nS	1.7 nS	1.9 nS
JEDEC-compliant SDRAM	2.2-5.0 nS	1.5 nS	0.8 nS

1. The figures listed here are examples only. See the *Data Book* for processor memory timing specifications.

Careful placement and routing of the SSDR DRAM interface signals results in the best possible memory performance. Trace lengths can be controlled and clock feedback delays correctly calculated. If provision is made to compensate for layout and timing uncertainties with zero Ω resistors, it is possible to attain PC133 data rates on TM5500/TM5800 processor-based system designs.

5.3.2 Example Design Strategy

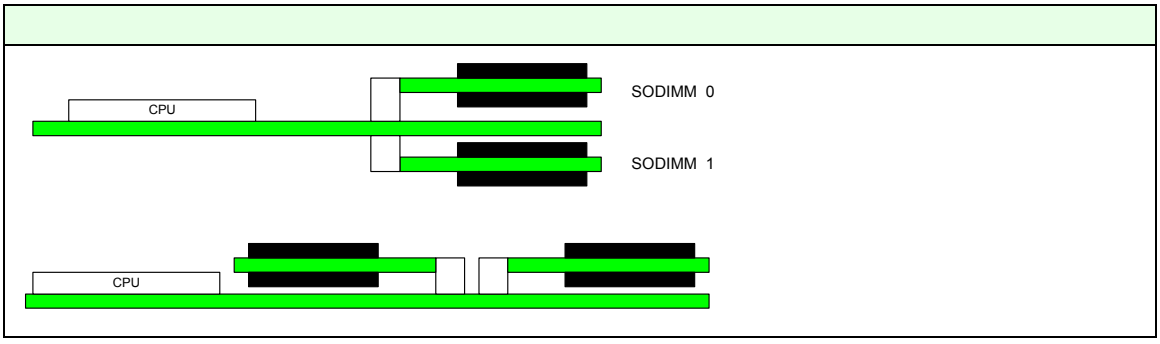
Layout of the TM5500/TM5800 processor SDR SDRAM interface is simplified with the application of one basic strategy:

Critical Rule
The TM5500/TM5800 processor SDR SDRAM layout works optimally with SODIMMs, specifically JEDEC-compliant SODIMMs.

Laying out the SDR SDRAM design using only JEDEC-compliant SODIMMs is very straightforward. Place the SODIMMs close together, using reverse-image connectors, routing signals from the processor to the SODIMMs.

Note that if the SODIMM connectors are placed in close proximity, it does not matter whether a star or daisy-chain topology is used.

Figure 10: Physical SDRAM Configurations



If the SDR SDRAM memory is laid out in this way, the system has the best possible performance, as long as the read and write timings are carefully controlled.

5.3.3 Write Timing

Critical Rule
A design can have no more than 450 pS of negative skew between the clock (at the SDR SDRAM) and all other inputs.

The minimum output hold time of the processor exceeds the input hold time of the SDRAM by:

1.25 nS – 0.80 nS = 0.45 nS

Because of this, the flight time of the clock must not exceed the latest data, address or control signal by more than 450 pS. Unfortunately, compensation must be made for the negative skew built into the JEDEC specification.

The clock length on an SODIMM is specified as 2.50”, or 445 pS (routed on inner traces). All the other signals on the SODIMM are some distance less than this. This difference must be added to each trace on the motherboard as timing compensation, as specified in Table 14 below.

Table 14: Write Timing Compensation

Signal Group	Minimum Length	Delay as Outer Trace	Delay Added to Motherboard
Data	0.60”	92 pS	353 pS
Data Mask	1.00”	153 pS	292 pS
Address/Control	0.75”	115 pS	330 pS
Select	1.00”	153 pS	292 pS
Clock Enable	1.00”	153 pS	292 pS

As an example of this required timing compensation, the data lines on the motherboard must all be at least 353 pS longer than the clocks.

Critical Rule
If 16 SDRAMS are used, the longest trace cannot be more than 5” in length, including the trace on the SODIMM. If the number of SDRAM chips is limited to 12, this maximum trace length can be increased to 8”.

This rule ensures that the maximum capacitive loading on each driver does not exceed the driver’s specified capacity.

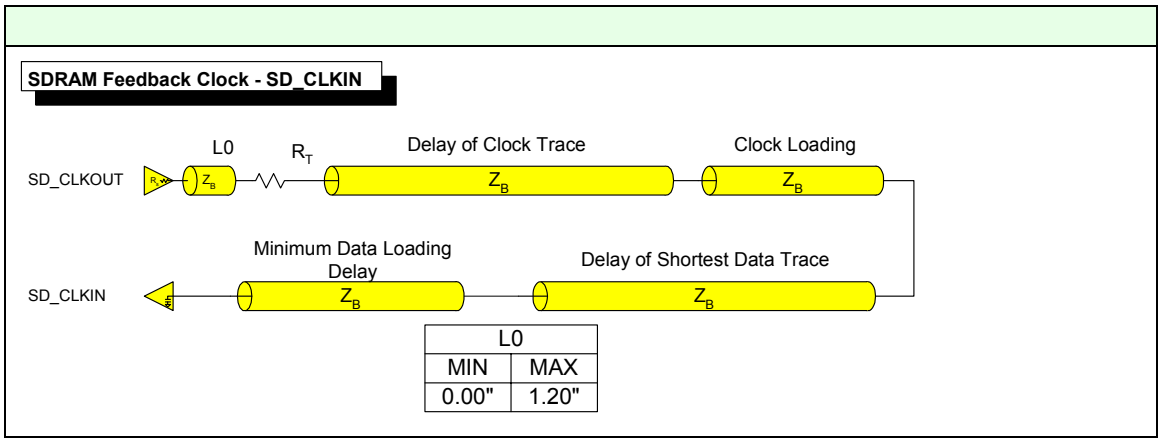
It is important to note that this restriction is an original design limitation. The system may well be capable of successfully driving a longer line. However, Transmeta has not simulated this or designed for it, so violating this rule is done at the designer's risk.

Finally, the clocks traces must be as short as possible. This minimizes potential EMI and signal integrity problems.

5.3.4 Read Timing

The processor memory controller has no information concerning the distance (and therefore delay) to and from the memory chips, but it must know when to expect valid data that is read from memory. The board designer must communicate this information by providing a carefully calibrated delay loop to resynchronize the data to the clock. The processor CLKOUT and SLKIN signal pins provide this function. The critical components of read timing compensation using CLKOUT and CLKIN are detailed in Figure 11 below.

Figure 11: Read Timing Compensation



The delay of the CLKIN line is equal to the round-trip delay of the read command and data. This delay has three components:

- The delay of the clock trace.
- The delay of the shortest data trace.
- A factor to allow for different capacitive loading of the clock and feedback traces, and for capacitive loading of the data trace.

These elements are described as delays, and not as lengths. Signals on the surface of a board travel at a different velocity (~150 pS/in) from the traces inside the board (~180 pS/in), due to the influence of the dielectric constant of the surrounding air.

Note also that these delays are from chip to chip. The trace delay on the SODIMM must be part of this calculation.

Looking at each component of the delay, the first two elements are easily understood. The delay of the clock trace is necessary to account for the timing of the signal to the chip. The delay of the data is needed to account for the return trip. The shortest data line is used to provide sufficient setup time without compromising hold time.

The loading of the clock and data can be quite different, and failure to account for this loading difference will skew the timing. The clock will almost always have four loads, and though actual loads must be determined from the manufacturer specifications, one load is usually about 2-4 pF.

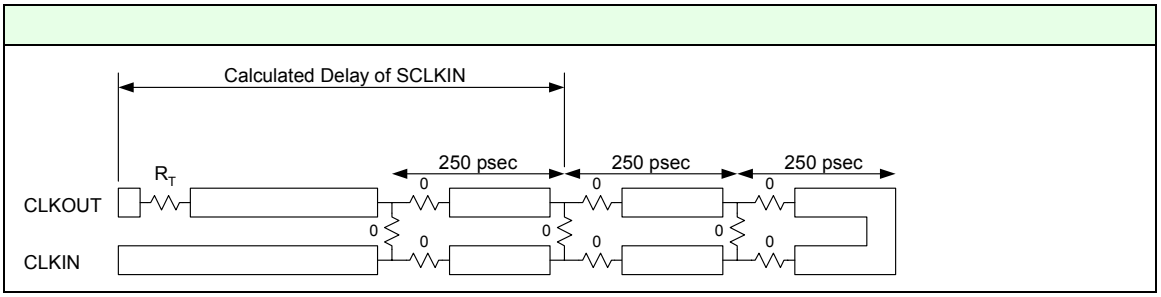
The delay due to clock and data loading is determined by the amount of loading, the drive current, and the termination resistance. Rather than calculate this in each instance, it is often simpler to rely on past experience to determine delay values. Experience has shown these capacitive delays cause a skew of approximately 500 pS. Therefore, a 500 pS delay element must be added to the clock feedback.

5.3.5 Uncertainty in the Feedback Calculation

The JEDEC specification is very specific about the layout of the clock trace on the SODIMM, but only gives the total length of the other lines, including data. There will also be some variation of capacitive delays in boards due to geometry, number of vias, etc. There may also be some variation in the actual delays of data and clock lines depending on how well the designer controls the return path integrity.

To address delay variation possibilities, a structure in the CLKIN feedback path that allows for some adjustment of the final configuration is strongly recommended. As shown in Figure 12, zero Ω jumpers can be used to add or remove delays from the line. Testing can be done during the prototyping stage to determine the optimum delay setting. For manufacturing, either the bill-of-materials (BOM) can be selected to give the optimum delay, or the board layout can be revised to remove the unneeded jumpers and delay elements.

Figure 12: Adjustment of CLKIN Delay



5.3.6 Using Soldered-down Memory

The previous sections have established the basis for an effective layout of the SDR SDRAM subsystem in a TM5500/TM5800 processor-based system. However, the method discussed requires the use of two SODIMMs. Code Morphing software cannot dynamically configure memory, and if a factory-installed memory module is replaced by a different module, Code Morphing software could fail to load or operate reliably. Another memory solution possibility uses soldered-down memory on the system motherboard. It is often desirable to place one or two banks of memory on the motherboard to provide a minimum system memory configuration and assure that Code Morphing software can always operate in this permanent memory section.

The design approach for soldered-down memory is straightforward. Having established that the two SODIMM design method previously discussed delivers optimal performance, soldered-down memory can be treated from the design perspective *as if it was an SODIMM*, using exactly the same routing topology used for the all-SODIMM solution. This topology results in a component placement that keeps the SODIMM connector and the on-board SDRAM in close proximity, as shown in Figure 13 and Figure 14.

The layout in Figure 13 is the simplest from a routing perspective. Signals are routed from the processor to the SODIMM connector and then to the on-board SDR SDRAM (passing through any needed termination resistors on the way). If the SODIMM connector is facing the other direction, as shown in Figure 14, the traces are routed from the processor to the connector, then back to the SDR SDRAM chips. In this sub-optimal placement, routing congestion occurs, possibly increasing the number of required board layers.

It is possible to place the SODIMM connector as in Figure 13 and avoid routing congestion. Placing the on-board memory on the far side of the SODIMM from the processor yields the optimum routing solution.

Figure 13: Optimum Placement and Routing

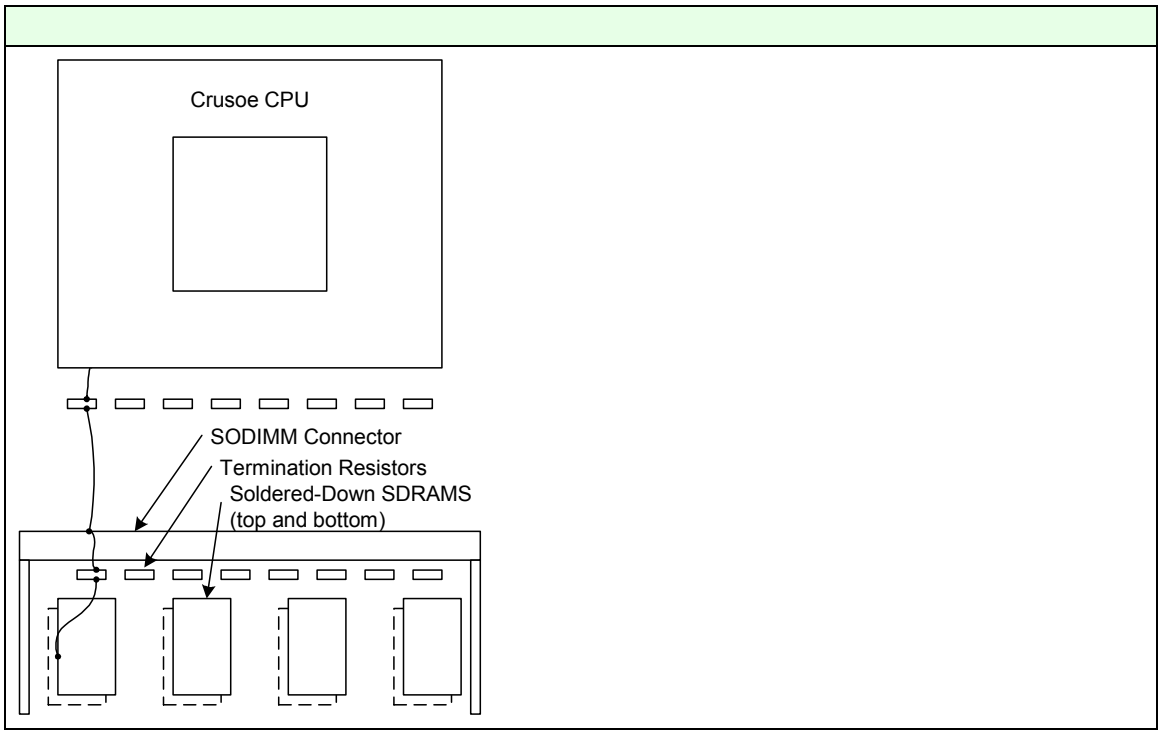
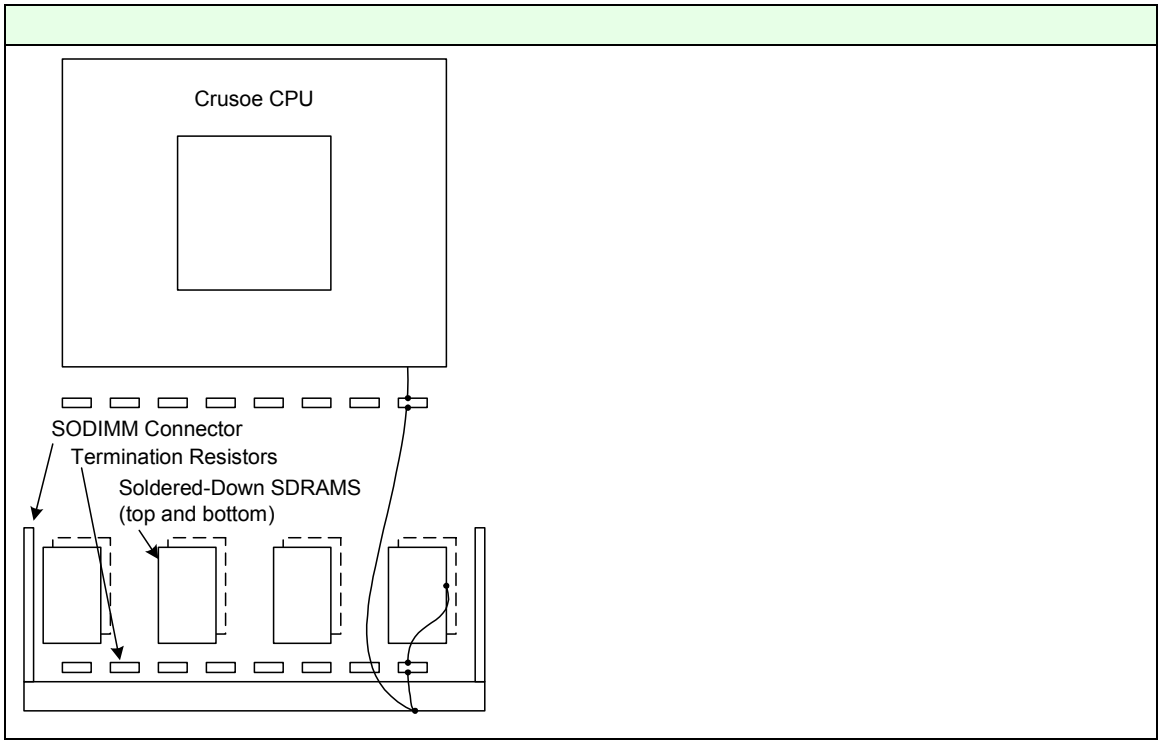


Figure 14: Sub-optimal Placement

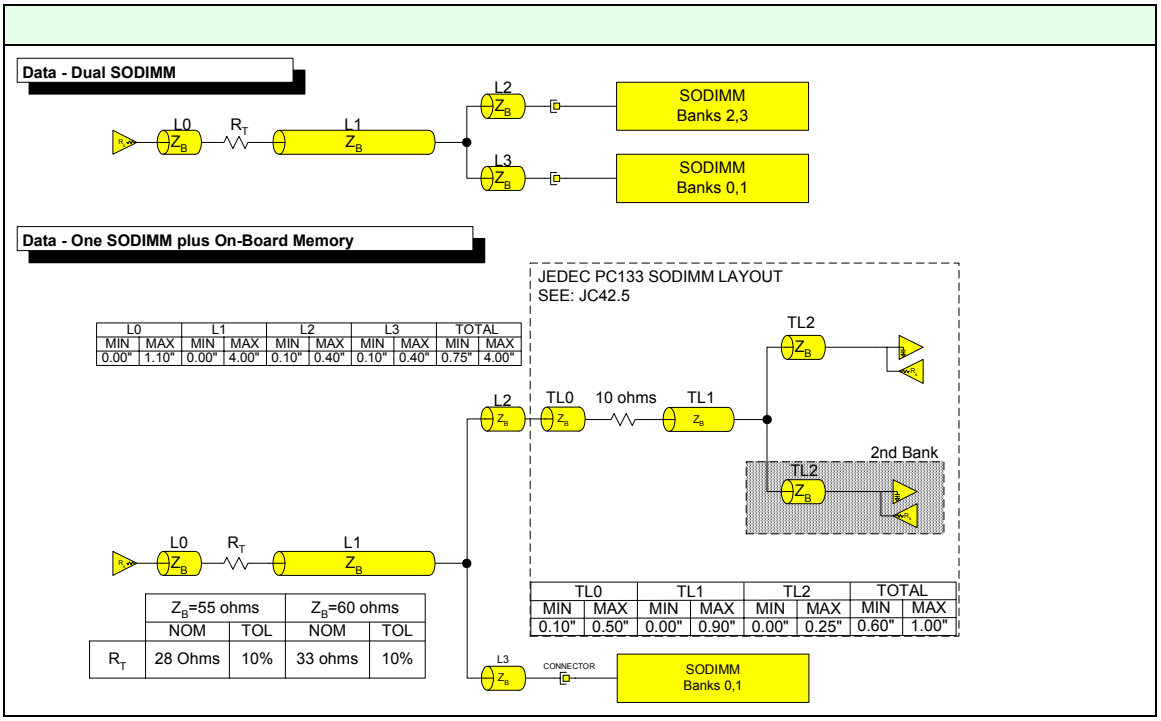


The JEDEC specification for SDRAM SODIMMs (JEDEC spec # JC42.5) is used to determine how to lay out the soldered-down memory traces to mimic the structure of an SODIMM. In the JEDEC specification the structure diagrams, with maximum and minimum lengths for each branch, are given for each trace.

These structure diagrams may be substituted into the circuit for each trace. If an advanced CAD software package is used to lay out the board, these branches may be assigned length rules. Routing the board in a manner different from the JEDEC specification will result in design rule violations.

Substituting the one SODIMM on a data line with the equivalent net structure from the JEDEC specification results in the structure shown in Figure 15. Note that this adds a termination resistor to the circuit.

Figure 15: Data Structure Diagram



L0		L1		L2		L3		TOTAL	
MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
0.00"	1.10"	0.00"	4.00"	0.10"	0.40"	0.10"	0.40"	0.75"	4.00"

TL0		TL1		TL2		TOTAL	
MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
0.10"	0.50"	0.00"	0.90"	0.00"	0.25"	0.60"	1.00"

	Z_B=55 ohms		Z_B=60 ohms	
	NOM	TOL	NOM	TOL
R_T	28 Ohms	10%	33 ohms	10%

It is important also to note the board impedance of the SODIMM. The JEDEC specification requires a trace impedance of 55 Ω ± 15%. However, the target motherboard may have a different characteristic impedance. The tolerance is unimportant, most board fabricators can easily meet a 10% tolerance at no additional cost.

Termination resistors are sized to match the board impedance to minimize reflections. If a characteristic impedance other than 55 Ω is used, the termination value must be similarly adjusted. Thus for a 60 Ω board, the value of the termination resistor at the memory end of the data line would be increased by five to 15 Ω.

These values are based on a 55 Ω characteristic impedance. If any other board impedance is used, these termination values must be adjusted accordingly using the following formulas.

$$Z_T = Z_S + Z_0,$$

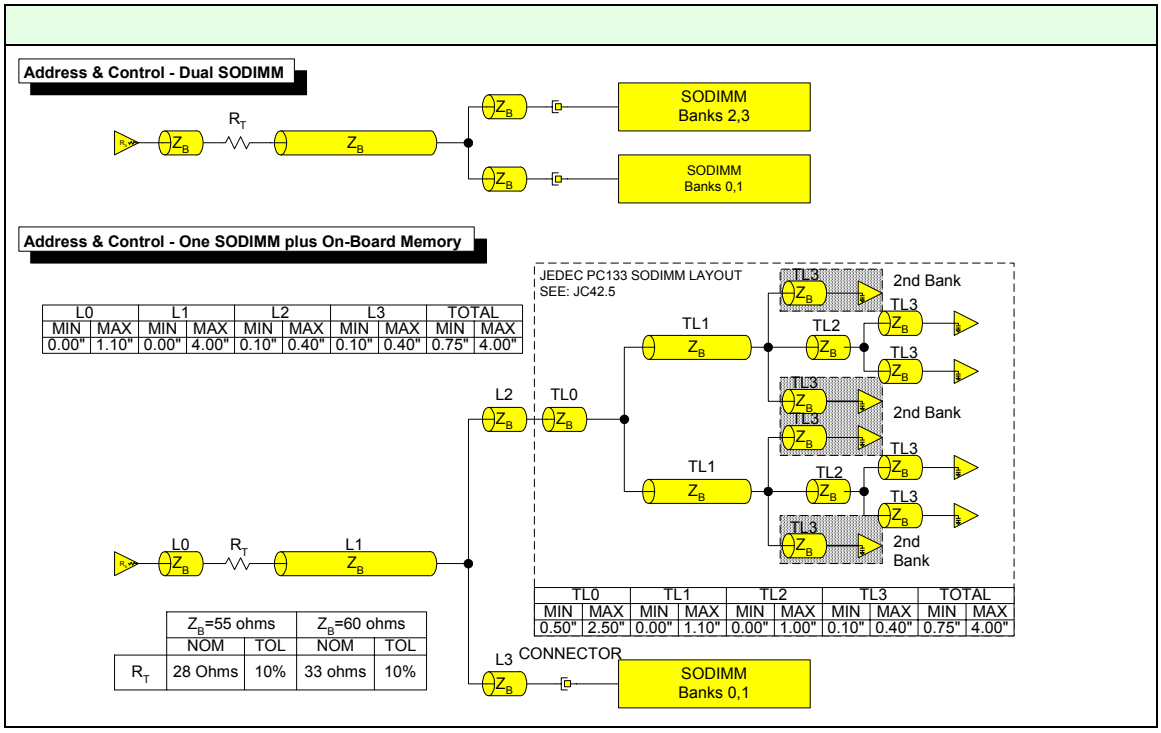
and

$$\Delta Z_T = \Delta Z_0$$

Termination values are given in this document for 60 Ω and 55 Ω boards. If a different impedance is used, all termination impedances must be recalculated.

The figures below show structure diagrams for each of the remaining SDRAM interface signals.

Figure 16: Address Line Structure Diagram

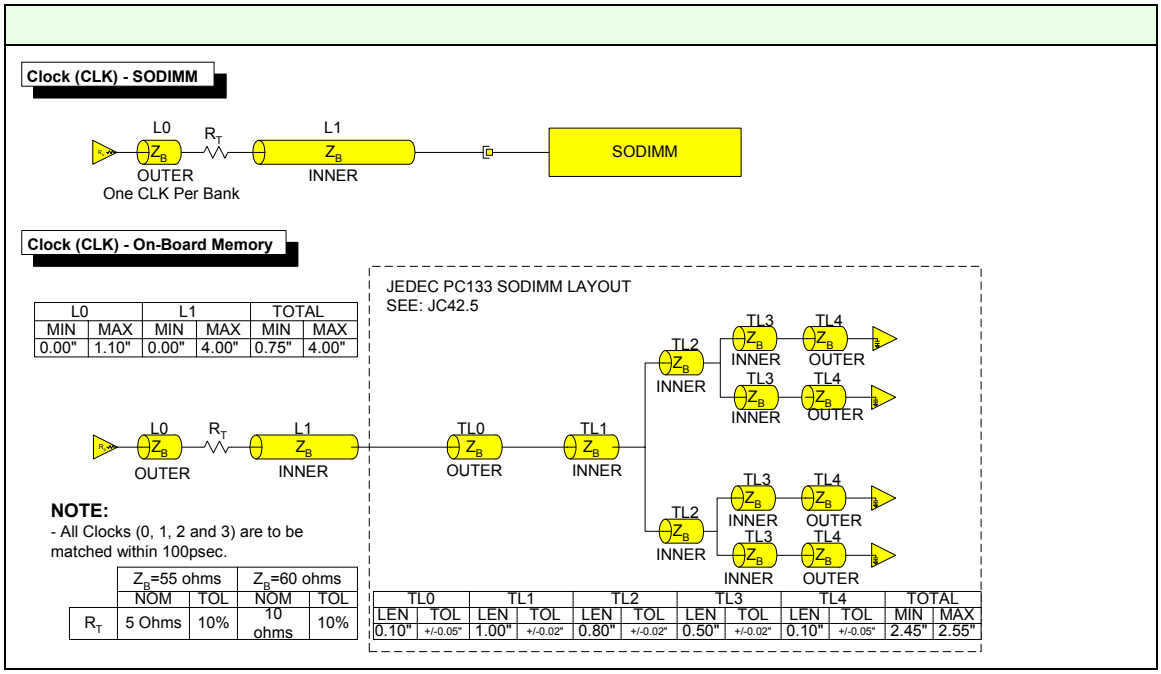


L0		L1		L2		L3		TOTAL	
MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
0.00"	1.10"	0.00"	4.00"	0.10"	0.40"	0.10"	0.40"	0.75"	4.00"

TL0		TL1		TL2		TL3		TOTAL	
MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
0.50"	2.50"	0.00"	1.10"	0.00"	1.00"	0.10"	0.40"	0.75"	4.00"

	Z_B=55 ohms		Z_B=60 ohms	
	NOM	TOL	NOM	TOL
R_T	28 Ohms	10%	33 ohms	10%

Figure 17: Clock Line Structure Diagram

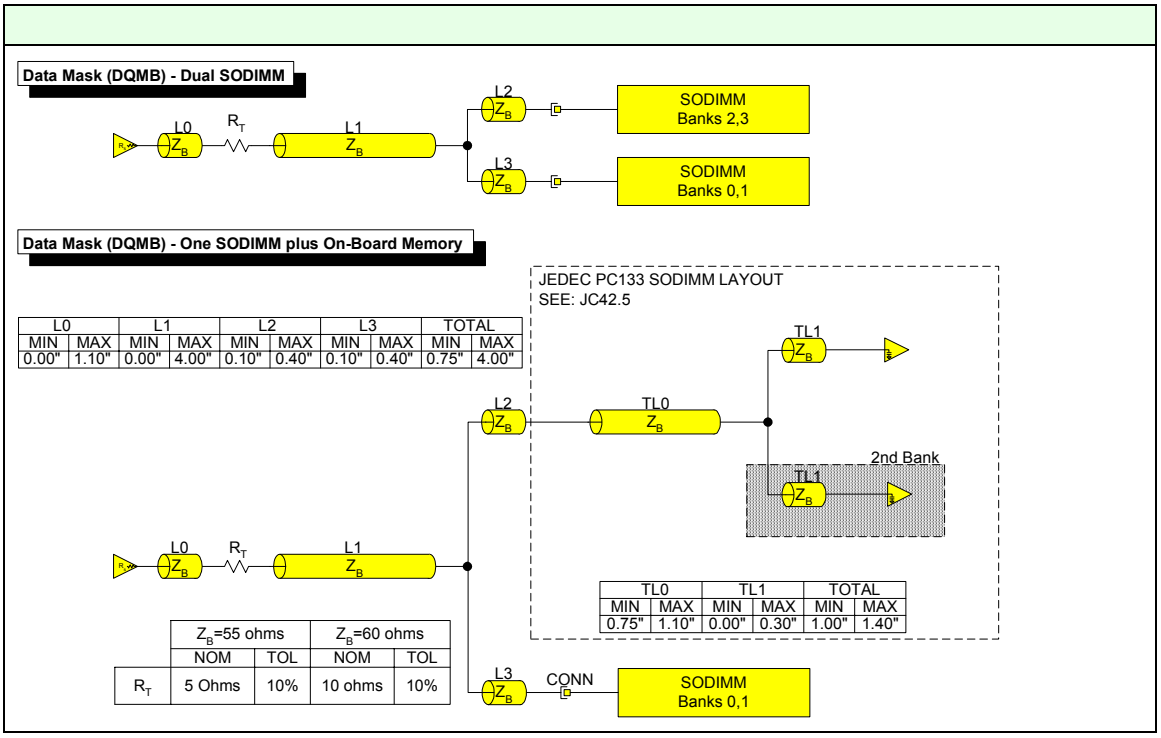


L0		L1		TOTAL	
MIN	MAX	MIN	MAX	MIN	MAX
0.00"	1.10"	0.00"	4.00"	0.75"	4.00"

	Z_B=55 ohms		Z_B=60 ohms	
	NOM	TOL	NOM	TOL
R_T	5 Ohms	10%	10 ohms	10%

TL0		TL1		TL2		TL3		TL4		TOTAL	
LEN	TOL	LEN	TOL	LEN	TOL	LEN	TOL	LEN	TOL	MIN	MAX
0.10"	+/-0.05"	1.00"	+/-0.02"	0.80"	+/-0.02"	0.50"	+/-0.02"	0.10"	+/-0.05"	2.45"	2.55"

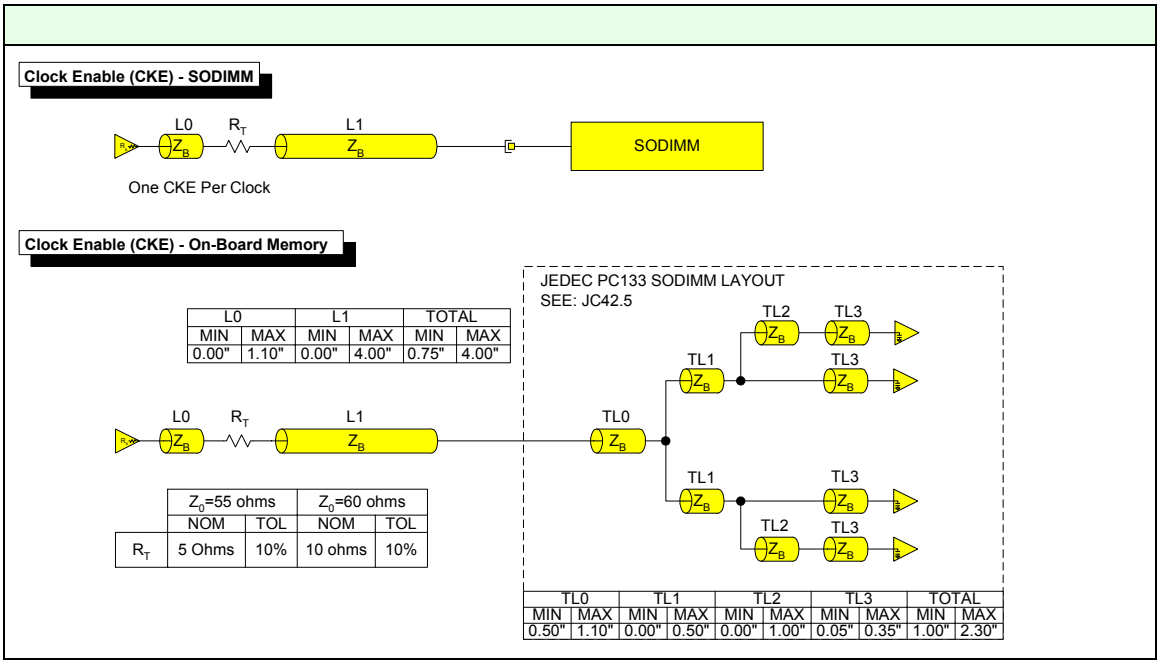
Figure 18: Data Mask Structure Diagram



L0		L1		L2		L3		TOTAL	
MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
0.00"	1.10"	0.00"	4.00"	0.10"	0.40"	0.10"	0.40"	0.75"	4.00"

TL0		TL1		TOTAL	
MIN	MAX	MIN	MAX	MIN	MAX
0.75"	1.10"	0.00"	0.30"	1.00"	1.40"

Figure 19: Clock Enable Structure Diagram



L0		L1		TOTAL	
MIN	MAX	MIN	MAX	MIN	MAX
0.00"	1.10"	0.00"	4.00"	0.75"	4.00"

TL0		TL1		TL2		TL3		TOTAL	
MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
0.50"	1.10"	0.00"	0.50"	0.00"	1.00"	0.05"	0.35"	1.00"	2.30"

5.3.7 Recommended Design Procedure

1. Determine the required memory configuration, soldered-down vs. SODIMM.

2. Generate schematics. If soldered-down memory is used, the second resistor for termination of data lines must be added. If an advanced CAD package is used, apply delay rules to memory lines per Table 14. Also, add delay rules to match line lengths within signal groups. Apply structures to soldered-down memory per the JEDEC SODIMM specification.

3. Determine the board stack-up to yield the desired characteristic impedance. Recalculate termination resistor values as needed.

4. Place SDR SDRAM close to the processor (no further than 4” from processor), preferably orthogonal with the processor, center-lines aligned. Place termination resistors as close to their source as possible.

5. Route clock lines, as direct and short as possible, splitting off in equal-length branches at the farthest point (starburst pattern).

6. Route CKEs, selects, data, address and control lines. If delay rules were not added in step 2, match line length within signal groups and add skew-correction values from Table 14.

7. From line length data, calculate the time needed for the CLKIN delay.

5.3.8 Design Example

The design example below assumes there is one bank of x8 memory soldered onto a 55 Ω board. The silicon is placed such that the Manhattan distance from most of the drivers is 4”.

Follow the steps in the *Recommended Design Procedure* on page 76 to calculate length data to include in the feedback path (CLKIN).

The length of clock on the motherboard is 3.22", routed on internal layers only. The resulting delay is:

3.22 in x 180 pS/in = 580 pS

The delay on the SODIMM is:

2.50 in x 180 pS/in = 450 pS, for a total of 1030 pS

The length of shortest data line on the motherboard is 4.24", half external, half internal. The delay of this line is:

((4.24"/2) x 180 pS/in) + ((4.24"/2) x 151 pS/in) = 701 pS

The length of this trace on the SODIMM is 0.6-1.0”. Assume a length of 0.8” on a surface trace. The delay on the SODIMM is:

0.8 in x 151 pS/in = 121 pS, for a total of 822 pS

Using only one bank of x8 parts on the board, both CLK 3 and CLK 2 can be used, ensuring 4 loads per clock. Applying the estimate of 500 pS for clock/data loading delay gives the required delay on CLKIN:

1030 pS + 822 pS + 500 pS = 2352 pS

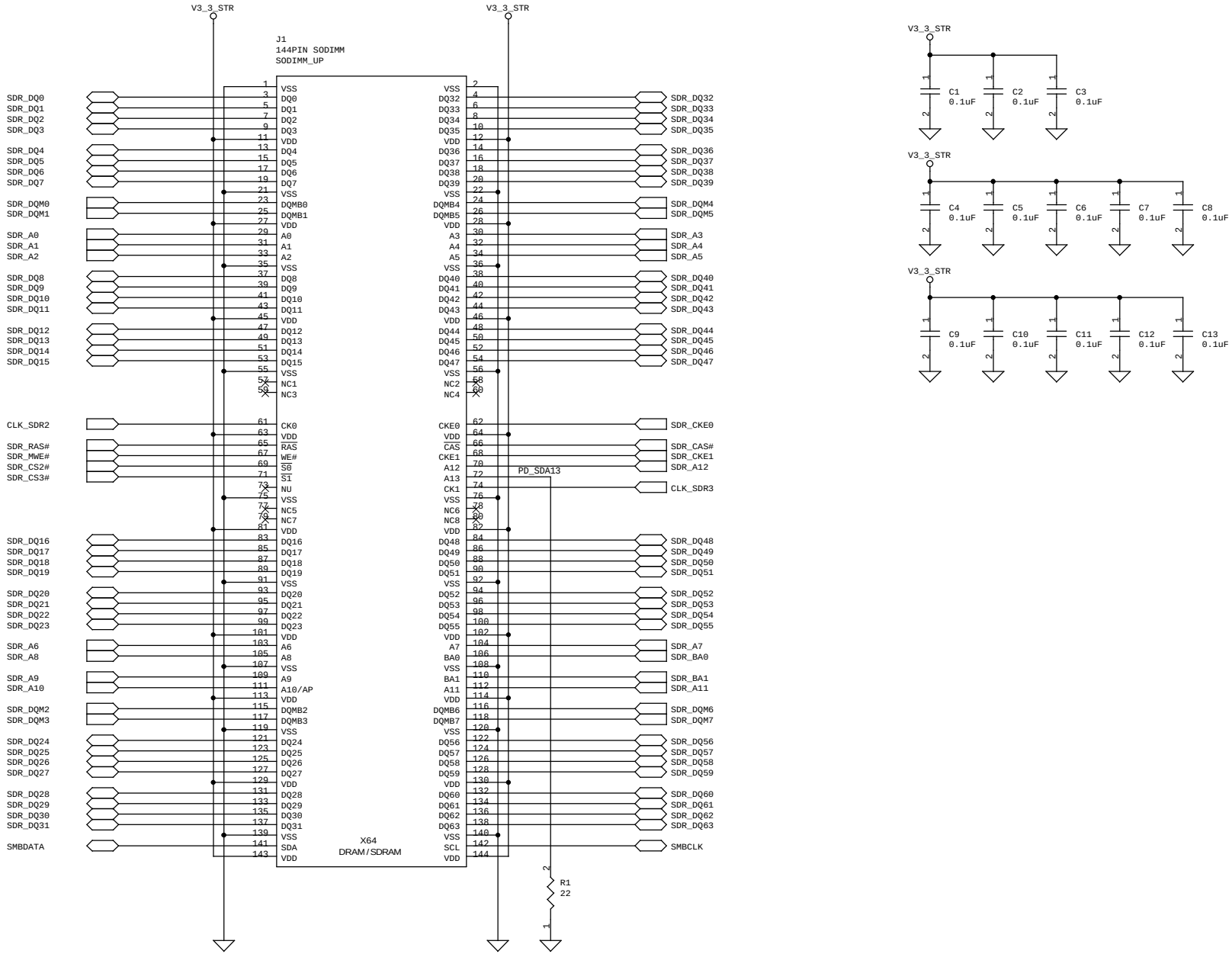
If routed entirely on internal traces, the line length is:

2352 pS / 180 pS/in = 13 in

5.4 SDR SDRAM Schematics

The following pages show SDR SDRAM reference schematics.

- Single SDR SODIMM (1 page)
- Dual SDR SODIMM (2 pages)
- SMBus isolation circuit (1 page)
- SDR clock enable isolation circuit (1 page)



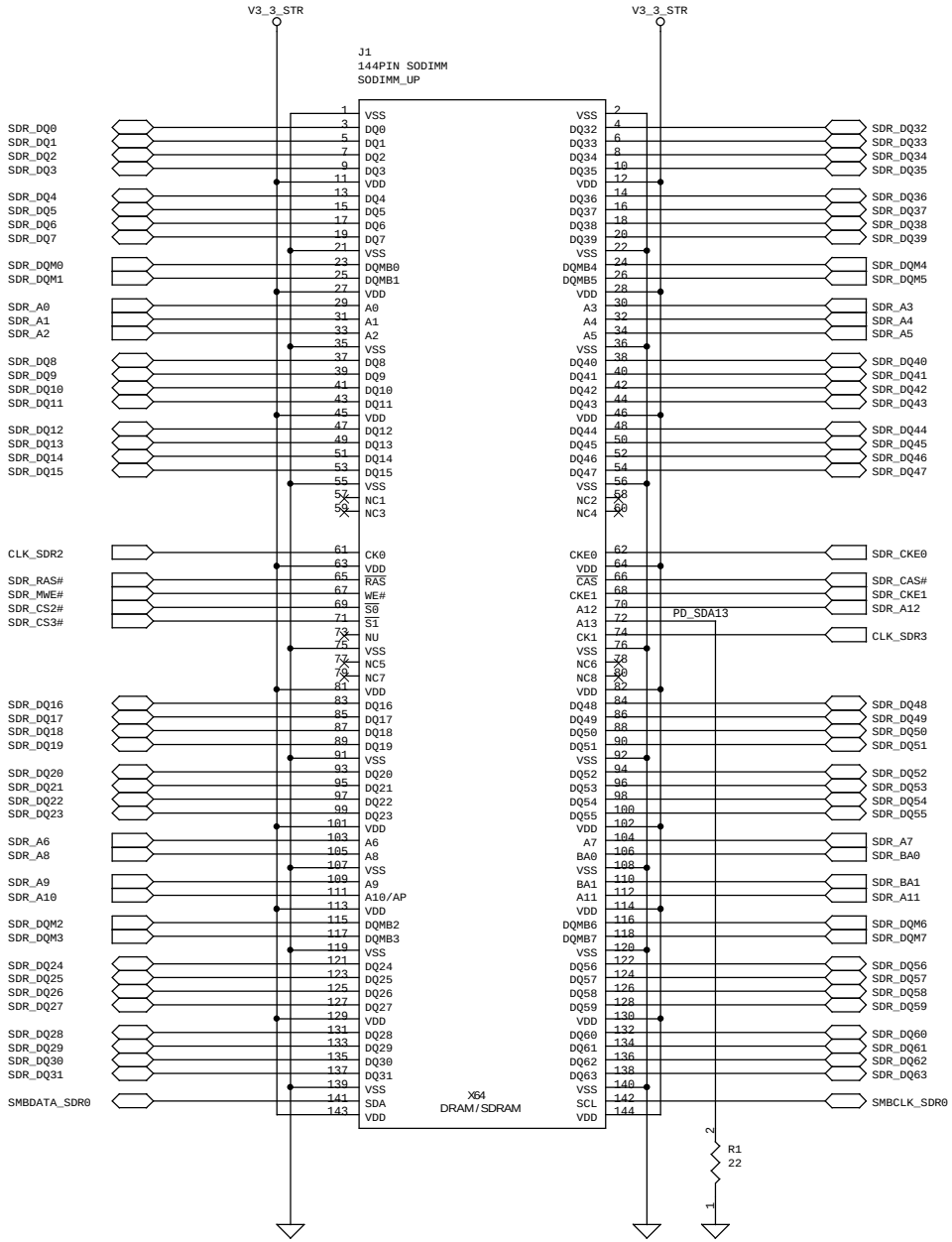
TRANSMETA Corporation
3940 Freedom Circle
Santa Clara, CA. 95054
(408) 919-3000

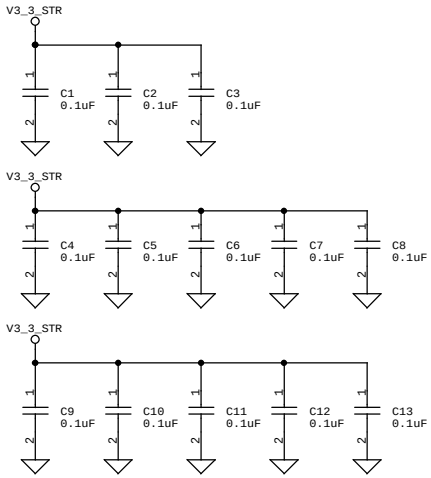
Project: TM5800 Design Guide

Title: Single SDR SODIMM

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Thursday, June 14, 2001 | Author: Basil | Page 1 of 1





TRANSMETA Corporation
3940 Freedom Circle
Santa Clara, CA. 95054
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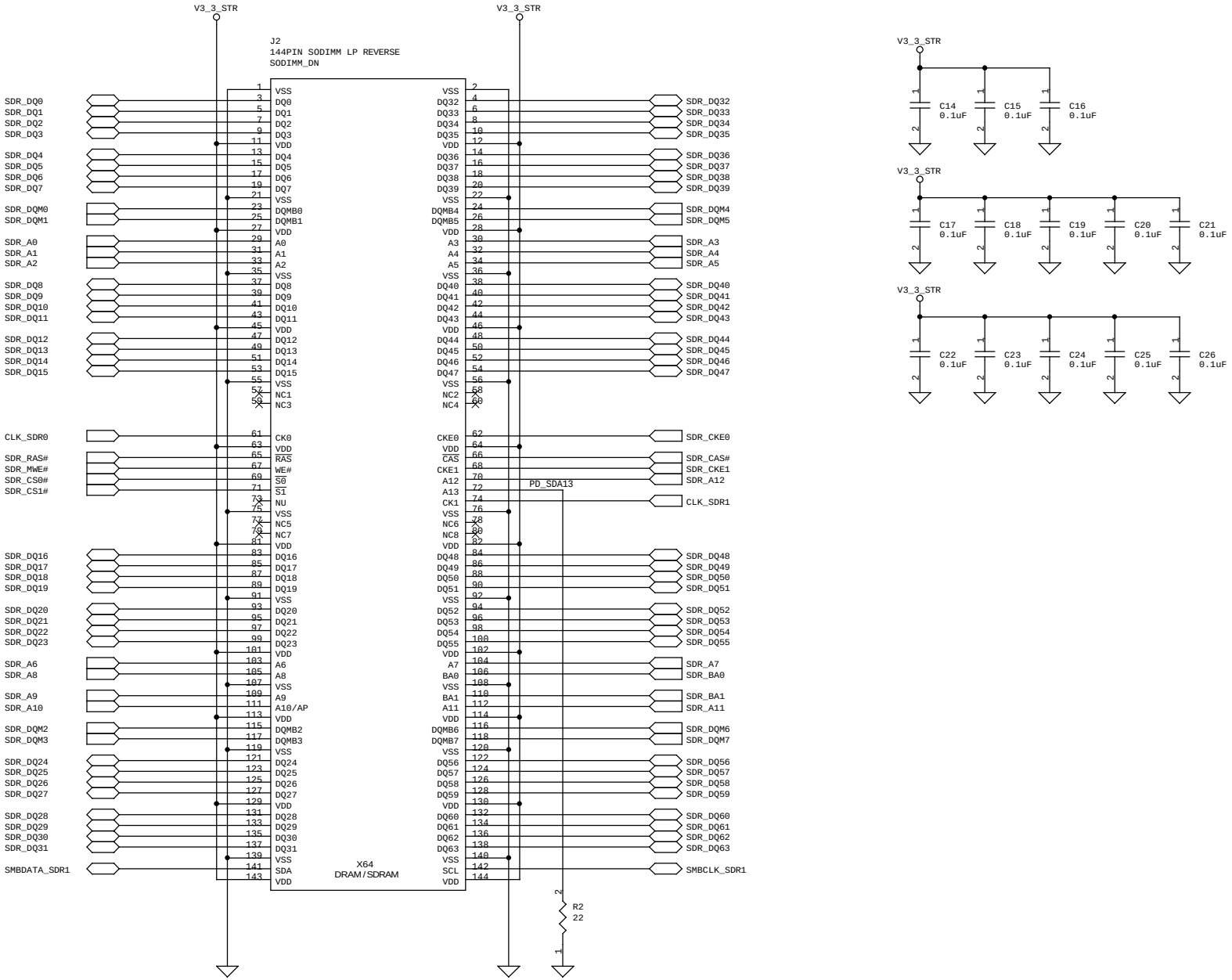
Project: TM5800 Design Guide

Title: Dual SDR SODIMM (1/2)

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Thursday, June 14, 2001 | Author: Basil | Page 1 of 3



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3940 Freedom Circle
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Project: TM5800 Design Guide

Title: Dual SDR SODIMM (2/2)

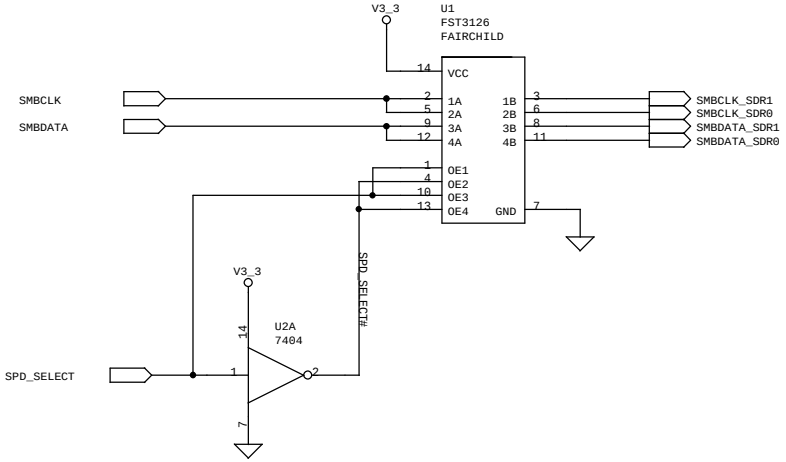
Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Thursday, June 14, 2001 | Author: Basil | Page 2 of 3

DUAL SDR SODIMM CONFIGURATIONS:

THE SYSTEM NEEDS THE ABILITY TO ISOLATE
THE SMBCLK AND SMBDATA TO EACH SDR SODIMM

IN THIS CIRCUIT A 1 BIT BUS SWITCH IS USED IN
CONJUNCTION WITH AN INVERTER AND A GPIO



TRANSMETA Corporation
3940 Freedom Circle
Santa Clara, CA. 95054
(408) 919-3000

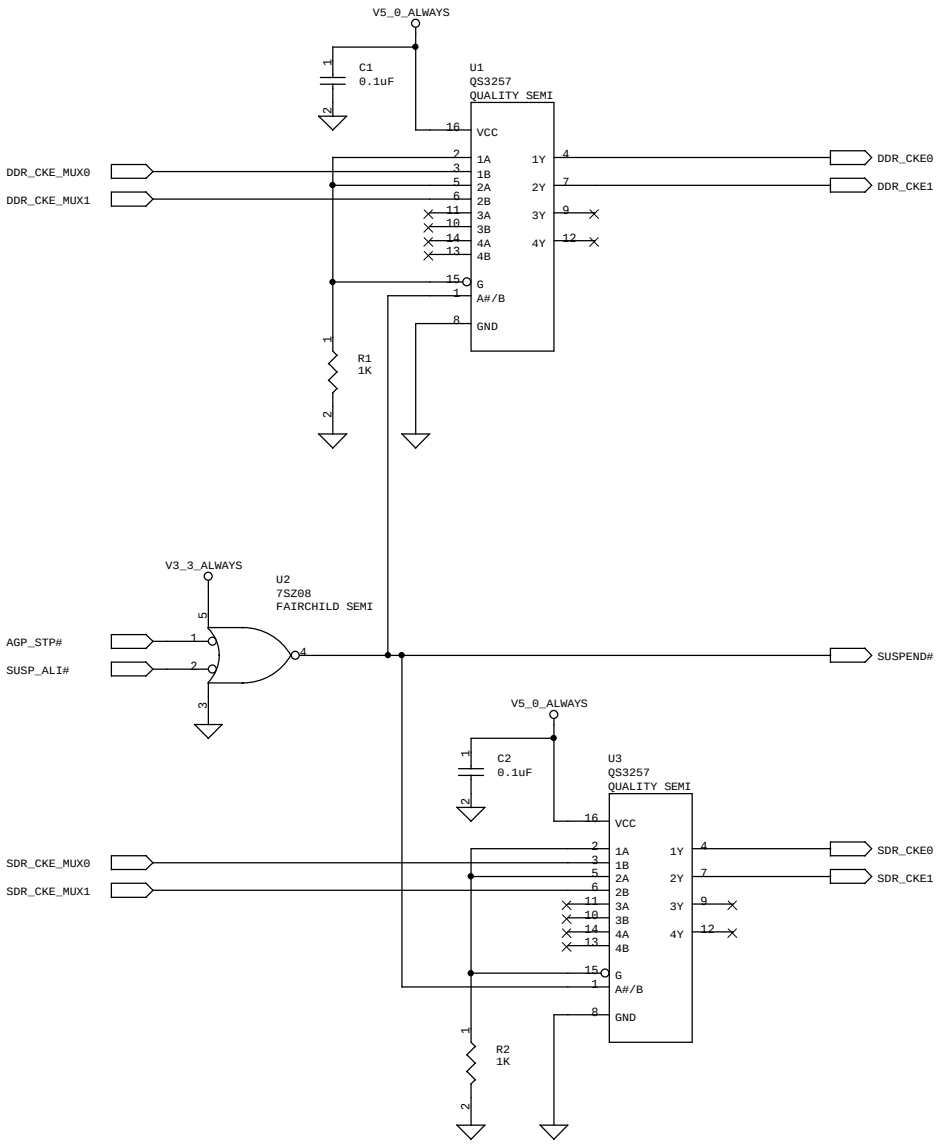
Project: TM5800 Design Guide

Title: SMBus Isolation

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Thursday, June 14, 2001 | Author: Basil | Page 3 of 3

TWO DISCRETE QUICKSWITCHES ARE USED
TO FACILITATE LAYOUT PLACEMENT.



TRANSMETA Corporation
3940 Freedom Circle
Santa Clara, CA. 95054
(408) 919-3000

Project: TM5800 Design Guide

Title: CKE Quickswitch

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Thursday, November 29, 2001 | Author: Basil | Page 1 of 1

Chapter 6

System Design Considerations

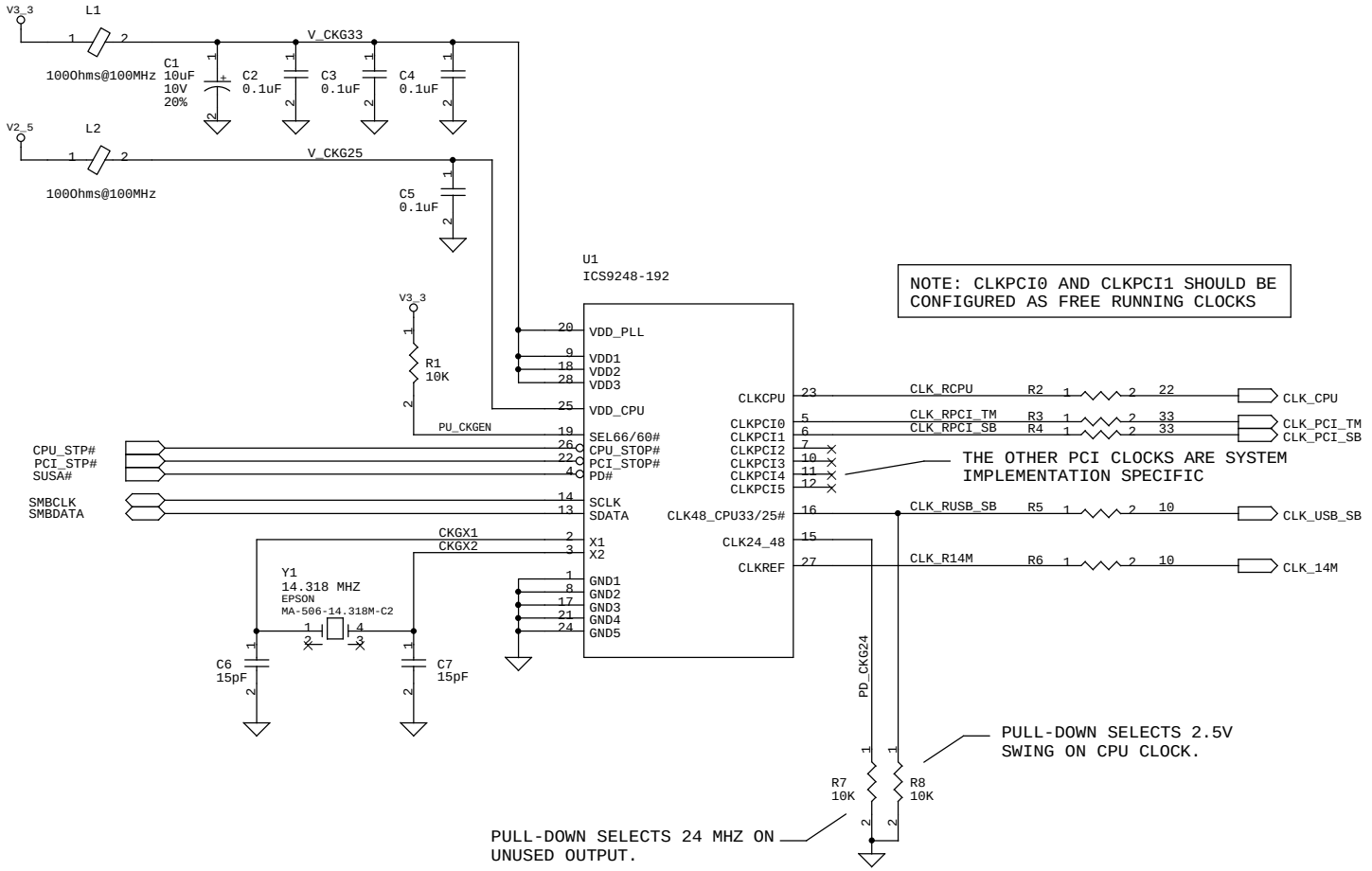
6.1 Clocking

Note
For detailed TM5500/TM5800 processor clock specifications see the *Input Clocks* section in the *Data Book*.

The TM5500/TM5800 processor primary clock input (CLK_CPU0) requires a 60 or 66 MHz clock signal. This clock input is compatible with Pentium™ class clock generators. The processor generates the internal processor core clock and the SDRAM clocks for both memory interfaces from the primary clock input.

The processor also expects a PCI clock (CLK_PCI_TM) input of CLK_CPU/2. The phase relationship between the processor and PCI clocks should be such that the CLK_CPU leads CLK_PCI_TM by 3.3 nS (typical). The clock traces (including CLK_CPU and CLK_PCI_TM) from the clock generator to each PCI connector or device should be of equal lengths.

The schematics on the following pages illustrate two possible clock generation circuits. One uses an Integrated Circuit Systems ICS9248-192 clock generator. The other uses an International Microcircuits IMIXG571CYB clock generator. The ICS clock generator solution has a much smaller overall footprint.



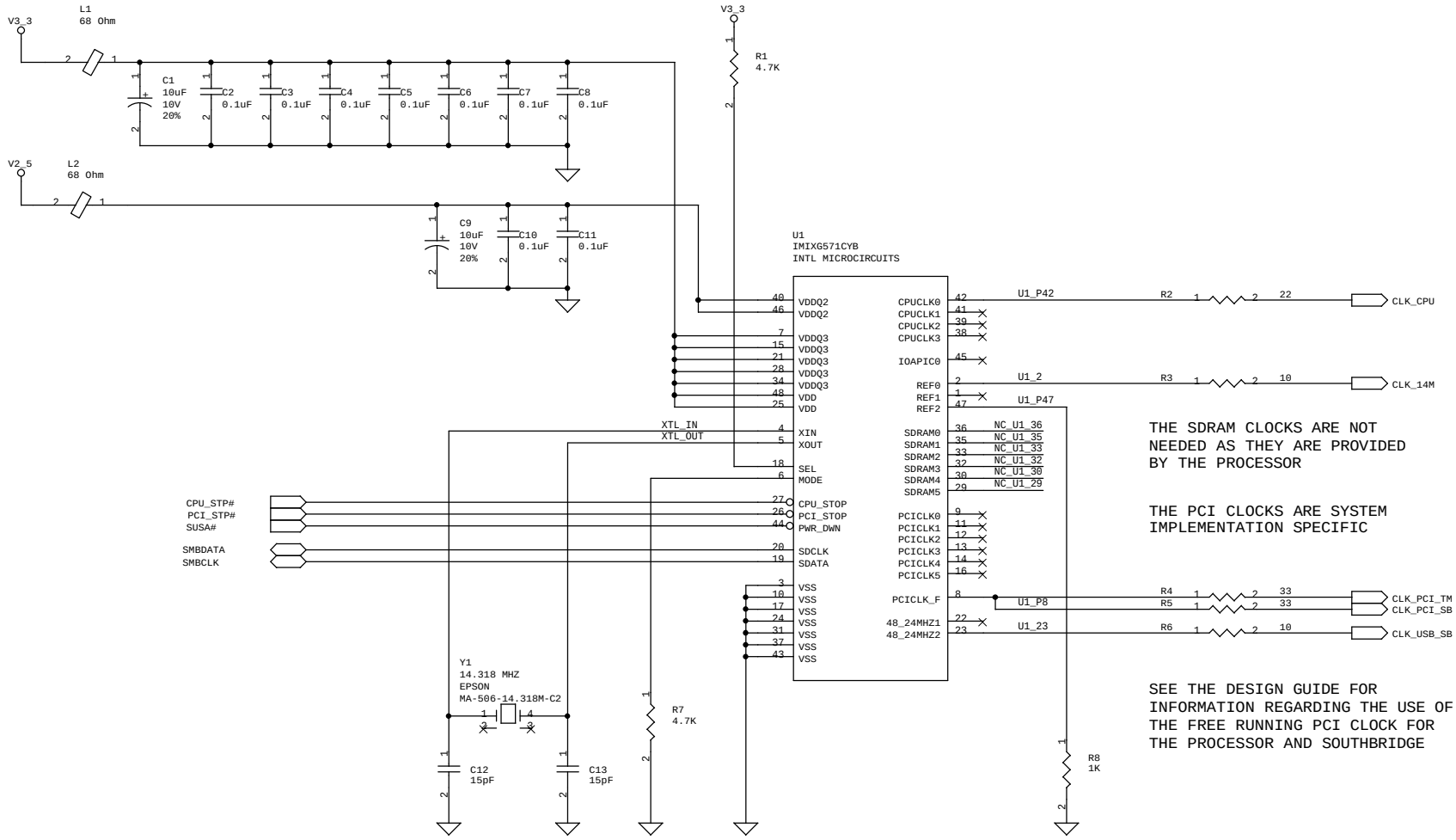
TRANSMETA Corporation
3940 Freedom Circle
Santa Clara, CA. 95054
(408) 919-3000

Project: TM5800 Design Guide

Title: ICS Clock Generator

Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Tuesday, February 19, 2002 | Author: Basil | Page 1 of 1



THE SDRAM CLOCKS ARE NOT NEEDED AS THEY ARE PROVIDED BY THE PROCESSOR

THE PCI CLOCKS ARE SYSTEM IMPLEMENTATION SPECIFIC

SEE THE DESIGN GUIDE FOR INFORMATION REGARDING THE USE OF THE FREE RUNNING PCI CLOCK FOR THE PROCESSOR AND SOUTHBRIDGE

TRANSMETA Corporation
3940 Freedom Circle
Santa Clara, CA. 95054
(408) 919-3000

Project: TM5800 Design Guide

Title: IMI Clock Generator

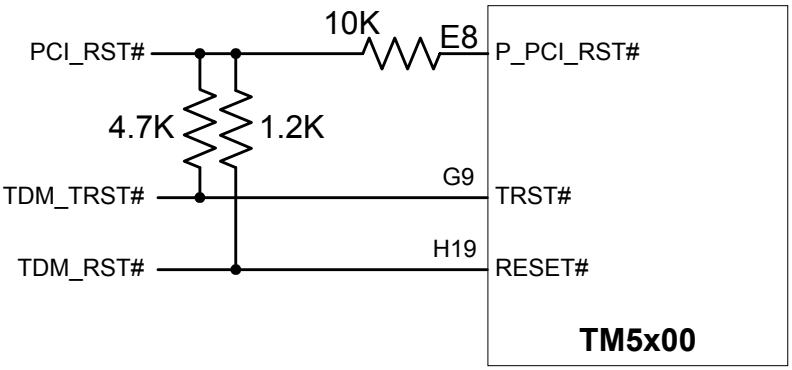
Document Number: **DOCUMENT#** Revision: A

Size: Custom | Date: Thursday, January 03, 2002 | Author: Basil | Page 1 of 1

6.2 System Reset

TM5500/TM5800 processors require the reset connections shown below for proper operation. This allows the Transmeta Debug Module (TDM) to assert JTAG reset and RESET# (needed for some debugging functions) without asserting PCI_RST#. A system-level PCI reset will also assert JTAG_TRST# and RESET#, which is needed for normal operation.

Figure 20: System Reset Diagram



Note

During system power-up, TM5500/TM5800 processors drive the P_PCI_RST# pin invalid (high) when V3_3 (3.3 V I/O power supply) is powered and V_CPU_CORE (processor core supply) is not powered. In some systems the southbridge can also be driving PCI_RESET# valid (low) during this time period, creating a conflict if these signals are directly tied together. The 10 KΩ resistor in the circuit above prevents the processor P_PCI_RST# high-level output signal during power-up from driving against the southbridge PCI_RESET# signal.

6.3 Signal Pull-ups and Pull-downs

The following signals should be pulled up to V2_5: IGNNE#, INTR, INIT#, NMI, FERR#, and SMI#.

During the Deep Sleep power management state, the processor clock is stopped and most I/O pins are tri-stated (see the ACPI specification). Care must be taken to ensure that all signals going to sections of the system that are powered on during suspend must be pulled up/down to a valid state when the processor tri-states its outputs.

Specifically, PCI_GNT# and other PCI control signals are most important, so that the PCI agent is not confused when the grant lines float low.

TM5500/TM5800 processor signals should be pulled up or down as shown in the table below. Many of these signals are outputs from the processor, and all non-DRAM processor outputs are tri-stated (float) during Deep Sleep.

Table 15: Signal Pull-up/Pull-down Requirements

Processor Signal			Pull-up / Pull-down Resistor Value / Configuration
Name	**Pin Number**	**Type**	
FERR#	H16	Output	10 KΩ pull-up to V2_5
IGNNE#	H15	Input	
INIT#	G18	Input	
INTR	G19	Input	
NMI	H17	Input	
SMI#	G14	Input	
STPCLK#	H18	Input	
EPROMA[0]	J16	Output	None (test point only)
EPROMA[1]	J15	Outputs	10 KΩ pull-up to V3_3
EPROMA[2]	J19	Output	
P_CLKRUN#	J18	Bidirectional	
P_GNT#[0]	G15	Output	
P_GNT#[1]	A16	Output	
P_GNT#[2]	F13	Output	
P_GNT#[3]	A15	Output	
P_GNT#[4]	G16	Output	
P_GNT#[5]	F17	Output	
P_HOLDA#	E13	Output	
SROM_CS#[0]	K15	Output	
SROM_CS#[1] [1]	L15	Output	
TCK	W7	Input	
SROM_SCLK	L16	Output	10 KΩ pull-up to V3_3 -or- 10 KΩ pull-down to ground
SROM_SOUT	K18	Output	
CFG_SDATA	A8	Bidirectional	1.2 KΩ pull-up to V3_3 -or- 4.7 KΩ pull-down to ground [2]

Table 15: Signal Pull-up/Pull-down Requirements (Continued)

Processor Signal			Pull-up / Pull-down Resistor Value / Configuration
Name	**Pin Number**	**Type**	
CFG_SCLK [3]	B7	Output	10 KΩ pull-down to ground
DEBUG_INT	H14	Input	
DEBUG_NMI	W11	Input	
SROM_SIN [3]	K17	Input	
Reserved and No Connection Signals			
RSV_F7	F7	-	10 KΩ pull-up to V3_3
RSV_G1	G1	-	
RSV_H5	H5	-	
RSV_H6	H6	-	
RSV_V1	V1	-	
RSV_V2	V2	-	
RSV_V3	V3	-	
RSV_W6	W6	-	
RSV_E7	E7	-	4.7 KΩ pull-down to ground
RSV_G13	G13	-	
RSV_G2 [4]	G2	-	10 KΩ pull-down to ground
RSV	D7	-	None (test point only)
RSV	G11	-	
RSV	J4	-	
RSV	J5	-	
RSV	R1	-	
RSV	R2	-	
RSV	R4	-	
RSV	T5	-	
RSV	AE19	-	
RSV	K3	-	No connection
RSV	K4	-	
RSV	K5	-	
RSV	L5	-	

1. During C3, all processor outputs are tri-stated. It is important to pull up SROM_CS#[1] to avoid the possibility of asserting serial ROM chip select.
2. When no mode-bit ROM is populated: use pull-up on CFG_SDATA to force Code Morphing software to boot from serial flash ROM, use pull-down on CFG_SDATA to force Code Morphing software to boot from parallel flash ROM.
3. May be pulled up or down. The recommended action is a pull-down, since the processor normally holds this signal low when idle. The goal is to prevent the signal from floating during C3.
4. If pin G2 is being used to unprotect the parallel ROM through a +12 V switch circuit, then it needs a pull-down. If the pin is not used, either a pull-up or pull-down is OK. Since the pin powers up as an input, the goal is to prevent the signal from floating.

6.4 Mode-bit ROM

Note
An external 2 Kbit mode-bit ROM is required for all TM5500/TM5800 processor-based systems.

TM5500/TM5800 processors use a 2-wire serial interface to download the configuration mode-bits from this device at boot-up. The configuration mode-bits instruct the processor on several important boot and initialization options. The contents of the mode-bit ROM are read into the processor at power-on, configuring the processor to begin execution with optimal performance timings over a large range of system operating configurations.

Use of the external mode-bit ROM is required for guaranteed operation of all production parts. For more information, see the *Development and Manufacturing Guide* section *Mode-Bit ROM Settings*.

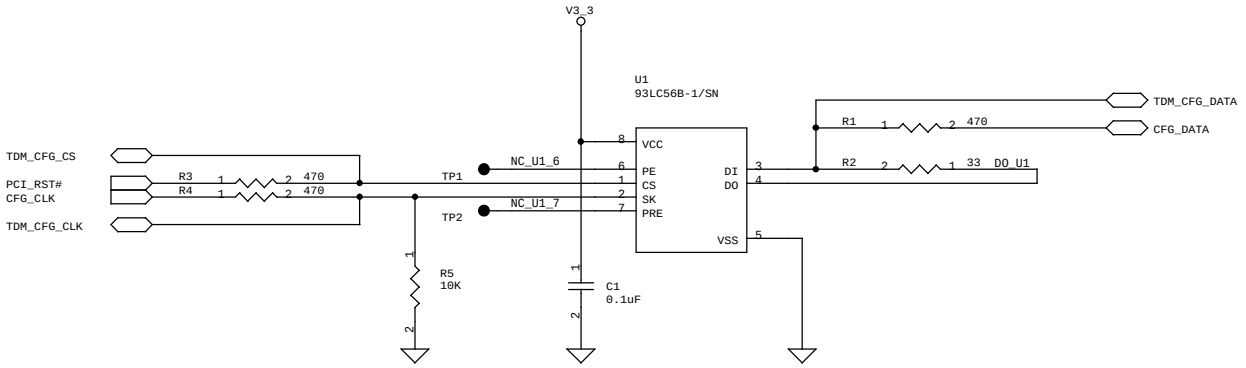
Currently, the only Transmeta-approved configuration mode-bit ROMs are:

- Microchip Semiconductor 93LC56B (128 x 16, 2 Kbit serial flash ROM).
- STMicro M93C56-WMN6 (128 x 16, 2 Kbit serial flash ROM).

The configuration mode-bit ROM is powered from V3_3.

The schematic on the following page illustrates the configuration mode-bit ROM circuit.

2Kb SROM



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6.5 Code Morphing Software ROM

TM5500/TM5800 processors use a combination of hardware and software to create an x86-compatible processor. A memory device of at least 1 MByte is required for storing Code Morphing software in compressed form prior to decompression and loading into RAM. There are two basic approaches to storing Code Morphing software: in a serial flash ROM, or combined together with the system BIOS into a parallel ROM. These two Code Morphing software ROM configurations are described below.

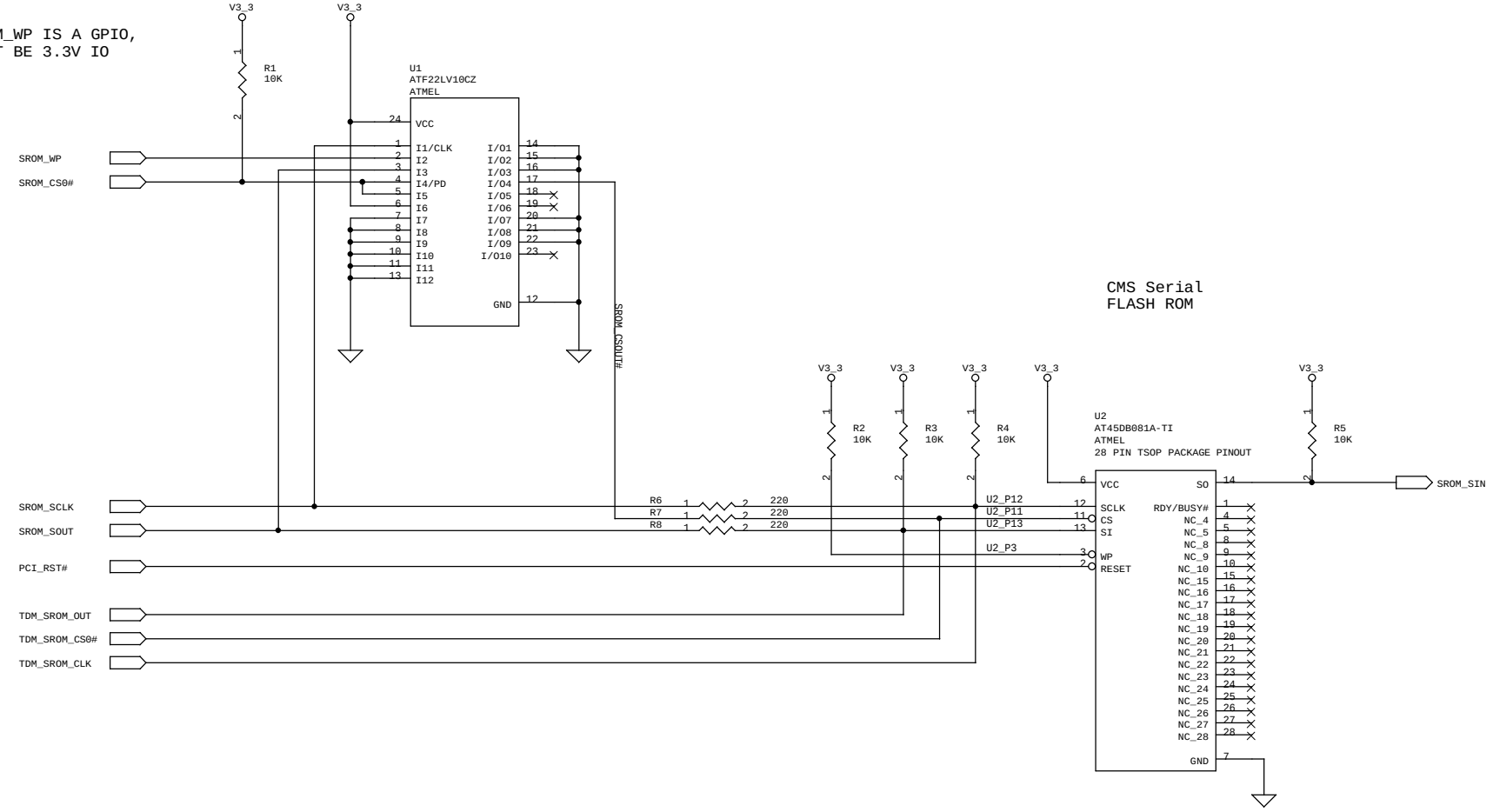
6.5.1 Serial Flash ROM Interface

Code Morphing software can be optionally stored in its own 8 Mbit (1 Mbyte) serial flash ROM. The SROM interface has all the signals needed to interface to Atmel serial flash ROM devices. Atmel provides up to 8 Mbit devices for which only one chip select is needed. The serial flash ROM uses the V3_3 power supply because it must be powered off when the processor is off.

The schematic on the following page illustrates a serial Code Morphing software flash ROM circuit.

SERIAL WRITE
PROTECT DEVICE

SROM_WP IS A GPIO,
MUST BE 3.3V IO



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6.5.2 Serial Flash ROM Write Protection Circuit

The serial flash ROM used with TM5500/TM5800 processors does not provide a secure mechanism for protecting the contents from accidental erasure or accidental writes. This creates a potential risk for the serial flash ROM to be inadvertently erased or modified in-system, which affects the Code Morphing software boot image stored in that ROM. Therefore, to ensure a high level of system security and integrity, Transmeta requires a special write protection circuit for the serial flash ROM. Systems using a parallel ROM to store the Code Morphing software boot image do not have this risk and do not require this write protection circuit.

Note
For JEDEC source code and CUPL source code, see Appendix B, *Serial Write-protection PLD Data*.

Note
Due to a potential race condition, do not use an ATF22LV10C part for this application.

The write protection circuit uses a 22LV10 PLD to filter the chip select signals from the processor to the ROM. The PLD intercepts write cycles to the ROM when writes are not authorized. A southbridge GPIO pin signals the PLD when writes are authorized. The features of this circuit are:

- It provides security.
- It fully write protects the entire serial flash ROM.
- It ensures that the Code Morphing software boot image is not accidentally overwritten.
- It allows for field upgrades of Code Morphing software should they be needed.

6.5.2.1 Circuit Operation

The write protection PLD works by gating the chip select signal to the serial ROM when a write or erase command is detected. The device has an input pin (named WP) to enable and disable this feature. When WP is asserted, write and erase commands are not allowed to complete. When WP is negated, write and erase commands function normally. Read commands are always unaffected by the PLD.

The polarity of the WP input is selectable with another input pin (named WPNEG). When WPNEG is pulled up, the WP input is active-low. When WPNEG is pulled down, the WP input is active-high. WPNEG should be pulled up if the signal driving the WP input powers up in the low state. WPNEG should be pulled down if the signal powers up in the high state.

The PLD also has an input pin (named SEL) to select the type of serial ROM in use. The SEL pin should be pulled down for the Atmel flash device, which is the only device currently supported.

6.5.2.2 PLD Pinout

The full pinout of the PLD is described in the following table:

Table 16: PLD Pinout

TSSOP Pin Number	Signal Name	Signal Description
1	CKIN	Serial flash clock input
2	WP	Write protect input
3	DIN	Serial flash data input
4	PD	Power-down pin, implied by device selection
5	CS0IN#	Serial flash 0 chip select input
6	CS1IN#	Serial flash 1 chip select input (tie high if unused)
7	WPNEG	Write protect negate input: Low = WP is active-high High = WP is active-low
8	SEL	Select serial flash interface input: Low = Atmel
9, 10, 11	-	Unused inputs, tied to ground
12	GND	Device ground
13	-	Unused input, tied to ground
14, 15, 16	-	Unused tri-stated outputs, tied to ground
17	CS0OUT#	Serial flash 0 chip select output
18, 19	-	Reserved, no connects
20, 21, 22	-	Unused tri-stated outputs, tied to ground
23	CS1OUT#	Serial flash 1 chip select output (no connect if unused)
24	VCC	Device power - connect to 3.3 V

6.5.2.3 PLD Device Selection

Note
Due to a potential race condition, do not use an ATF22LV10C part for this application.

The following should be considered when selecting a PLD device to implement the write protection circuit:

- **Package**. The state machine in the PLD design is very simple, and it could fit into a very small device. However, an asynchronous flip-flop reset is absolutely necessary for this PLD design to function, and the smallest PLD with this feature is a 22LV10. For tightly constrained board layouts, Atmel makes a 22LV10 in a 24-pin TSSOP. The Atmel part number is ATF22LV10CZ, and the device's pinout and fuse map are the same as in a standard DIP 22LV10.

- **Propagation delay**. Transmeta successfully tested a part with a 15 ns propagation delay. Although a slower part may work, Transmeta cannot guarantee it because a slower part was not tested.

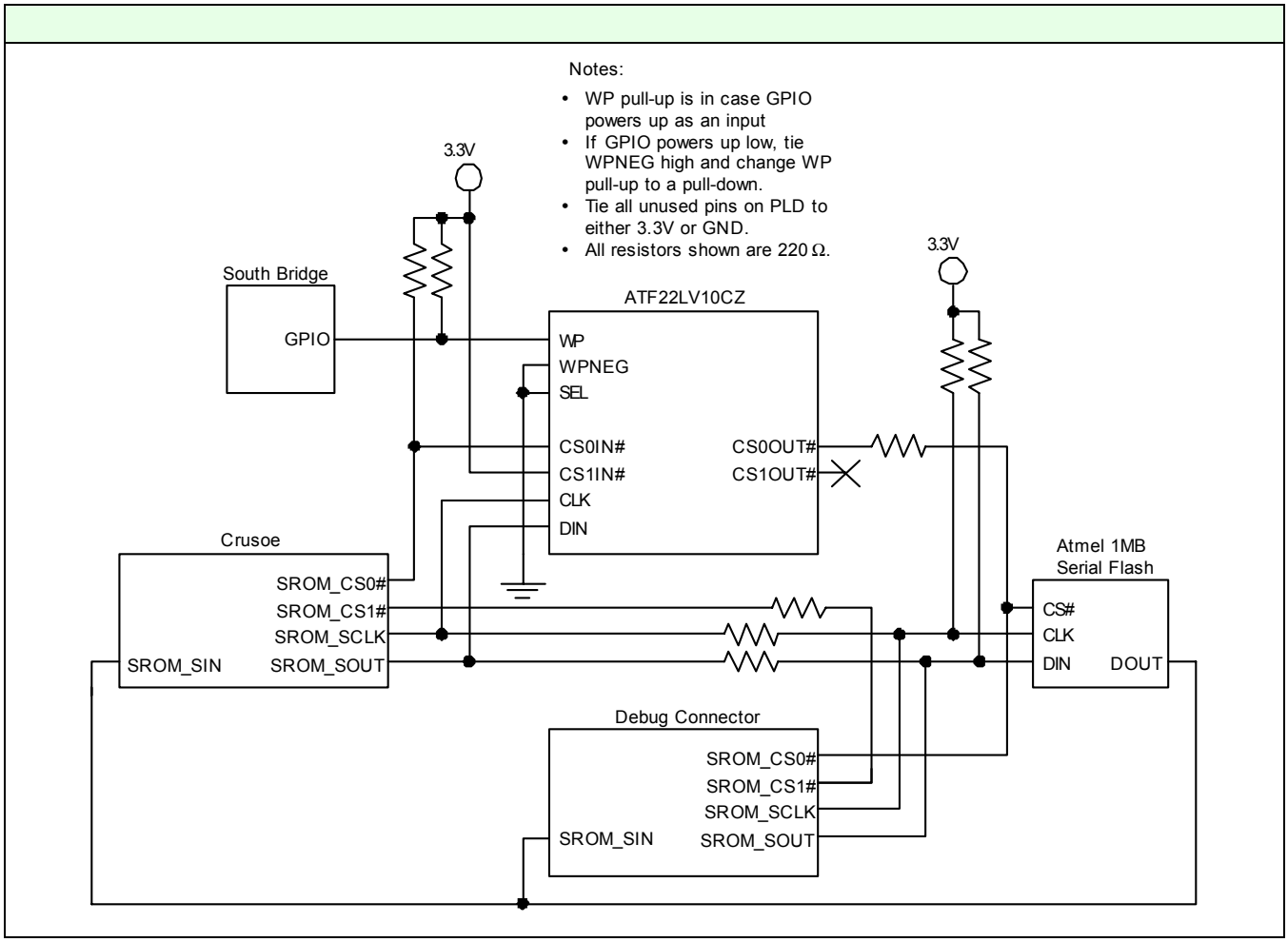
- **Voltage**. The PLD must have 3.3 V outputs because the serial flash ROM is not 5 V-tolerant.

- **Power**. Since the standard 22LV10 draws at least 70-90 mA from 3.3 V, Transmeta recommends a part with a power saving feature be used. Many vendors sell 22LV10 parts with power saving features. Transmeta recommends the Atmel ATF22LV10CZ.

6.5.2.4 Schematic

The schematic below shows the serial flash ROM write-protection PLD circuit.

Figure 21: Schematic Diagram of Serial Flash Write-protection PLD in System



6.5.3 Combined BIOS/CMS Parallel ROM Interface

TM5500/TM5800 processors support use of the BIOS parallel ROM memory for Code Morphing Software (CMS) storage, thus eliminating the need for a 1 MByte serial Flash ROM to store Code Morphing software.

This is accomplished by connecting the processor EPROMA[2:1] signals to the highest-order address bits of a 2 MByte parallel flash ROM, in the usual way for a system BIOS interface (Xbus or similar). Code Morphing software is stored in the lower ¾ of the ROM, and the upper ¼ is used for the system BIOS. The processor controls the EPROMA[2:1] signals during Code Morphing software decompression, and then sets EPROMA[2:1] to 11b to enable access to the x86 BIOS code.

There is an important security issue arising from the use of a parallel ROM for Code Morphing software that must be addressed by the system designer. This issue relates to the use of JEDEC flash ROMs that have an *erase-all* command that erases all unprotected sectors in the ROM. This allows the possibility for x86 software (applications or viruses) to erase the entire ROM, including the Code Morphing software portion.

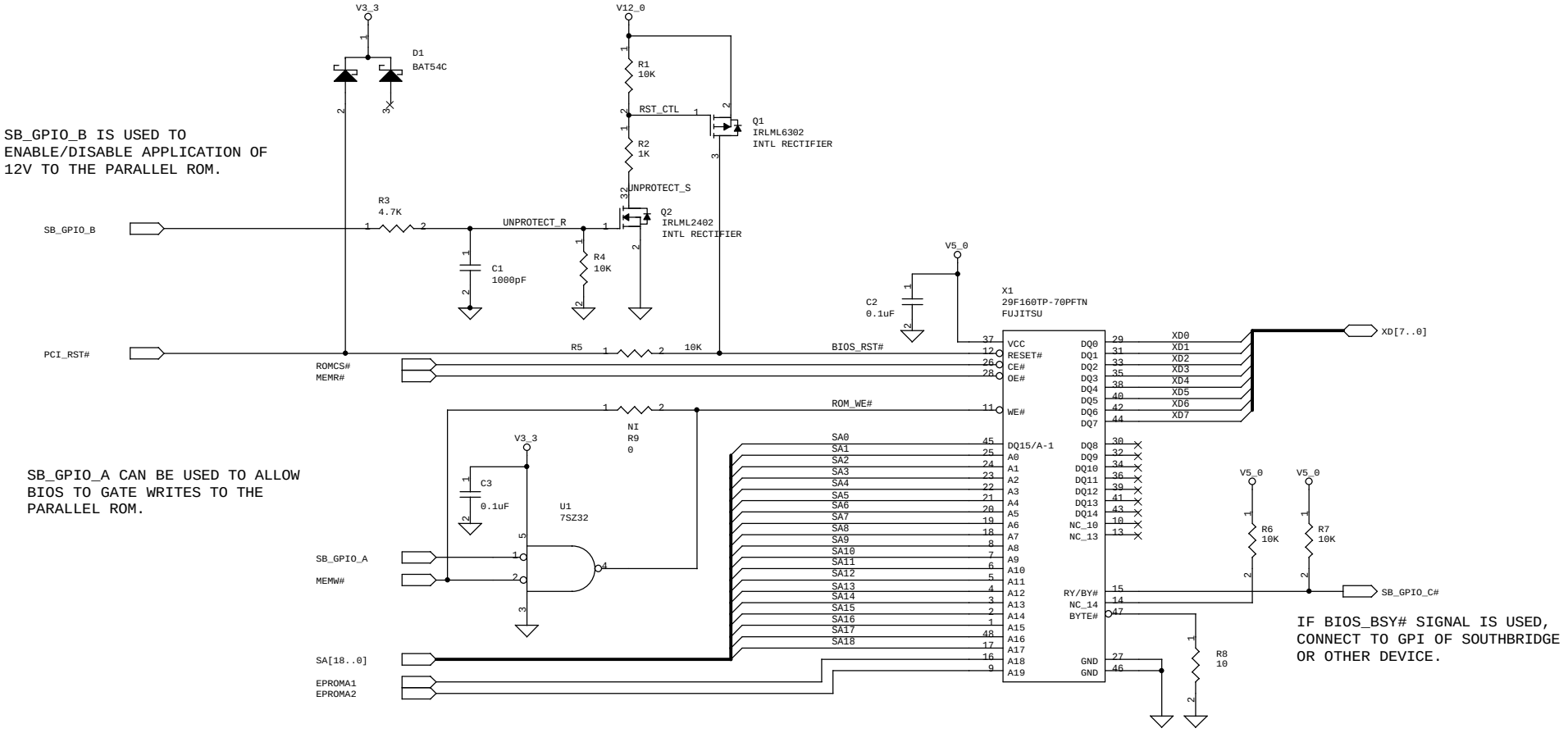
To protect against unauthorized Code Morphing software erasure, the Code Morphing software sectors of the ROM should be protected by enabling the ROM sector protection feature. The ROM sector protection feature is enabled by the ROM programming equipment at the OEM manufacturing site.

JEDEC flash ROMs have a temporary sector unprotection method that involves raising the reset pin of the ROM to +12 V. This method is used for Code Morphing software field upgrades. A pin on the processor (not accessible by x86 code) is used to control the temporary unprotect ROM feature during the upgrade process.

Future versions of parallel ROMs may allow the *erase-all* feature to be disabled, and some may also support software programmable protection of sectors. These enhancements eliminate the need for this protection circuit.

For debugging purposes, retain the serial flash connections to the Transmeta Debug Module (TDM) interface. The TDM has built-in serial flash and allows developers to boot from the TDM-based flash device.

The schematic on the following page illustrates a combined BIOS and Code Morphing software parallel flash ROM circuit.



If used for System BIOS only, install 512K (or 256K).
If used for System BIOS and CMS, install 2M.
In TM5X00 systems, the lower 3/4 of the ROM are protected and unable to be erased (i.e. by an 'erase all' command to the ROM). The unprotect circuit allows CMS to reprogram protected sectors during a CMS upgrade (TM5X00 only). Note how EPROMA[2..1] signals are connected to the 2MB ROM. These signals act as bank selects to select either CMS sectors or BIOS. When CMS has decompressed and is ready to run x86 code, these signals select the highest bank (11) to allow access to the BIOS code.

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6.6 Southbridge

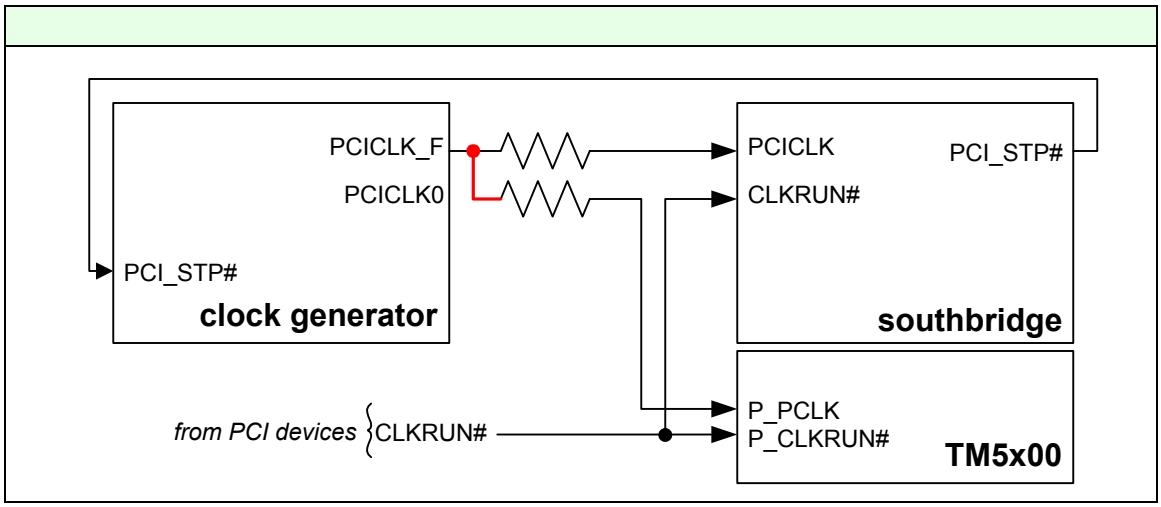
6.6.1 Qualified Southbridge Devices

The Acer ALI M1535 southbridge has been fully qualified by Transmeta for use with TM5500/TM5800 processors, and is the recommended southbridge solution. Other PCI-interface southbridge devices can also be used with TM5500/TM5800 processors. Contact your Transmeta representative for qualification status of other southbridge devices.

6.6.2 Using CLKRUN

Refer to the following figure for the recommended CLKRUN implementation.

Figure 22: Recommended CLKRUN Circuit



6.6.3 Southbridge Schematics

The schematic diagrams on the following four pages illustrate the southbridge circuit using the ALI M1535.

NOTE: THIS SCHEMATIC IS FOR THE ALI 1535 SOUTHBRIDGE ONLY. SEE THE VENDOR DOCUMENTATION FOR ALI 1535+ AND OTHER SOUTHBRIDGE DIFFERENCES.

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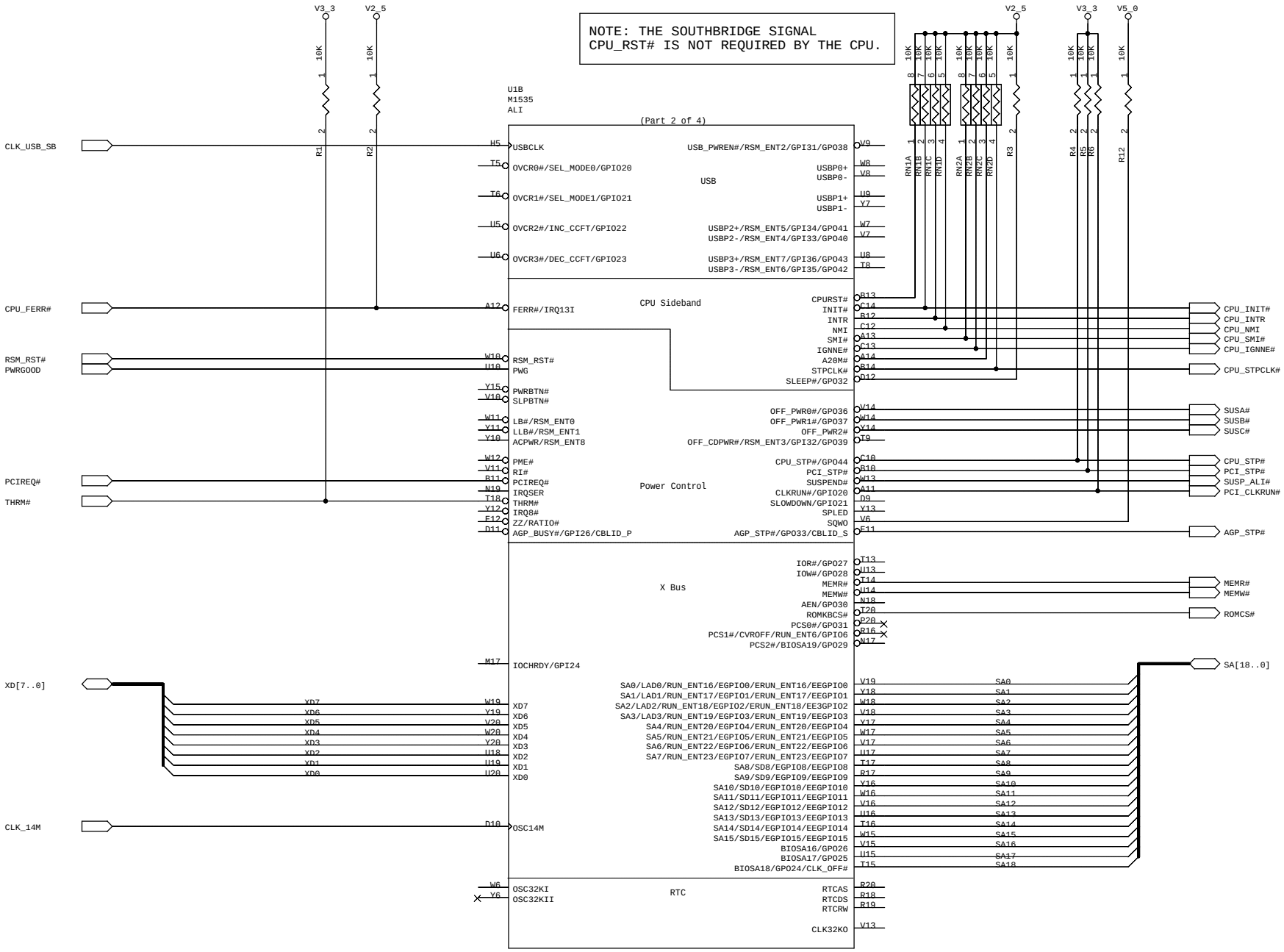

NOTE: THIS SCHEMATIC IS FOR THE ALI 1535 SOUTHBRIDGE ONLY. SEE THE VENDOR DOCUMENTATION FOR ALI 1535+ AND OTHER SOUTHBRIDGE DIFFERENCES.

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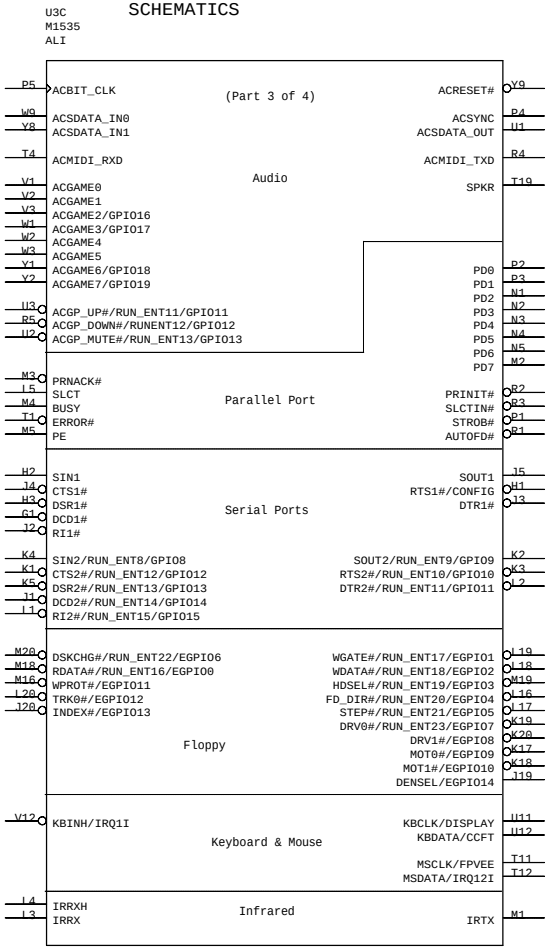
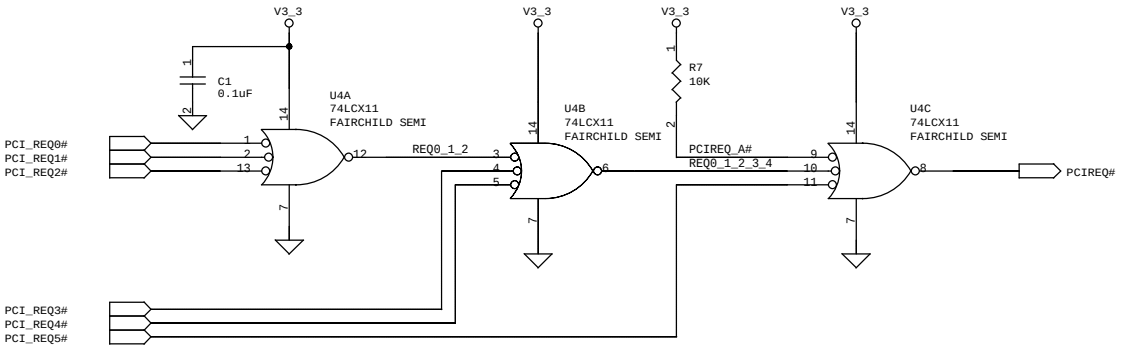
SCHEMATICS





NOTE: THIS SCHEMATIC IS FOR THE ALI 1535 SOUTHBRIDGE ONLY. SEE THE VENDOR DOCUMENTATION FOR ALI 1535+ AND OTHER SOUTHBRIDGE DIFFERENCES.

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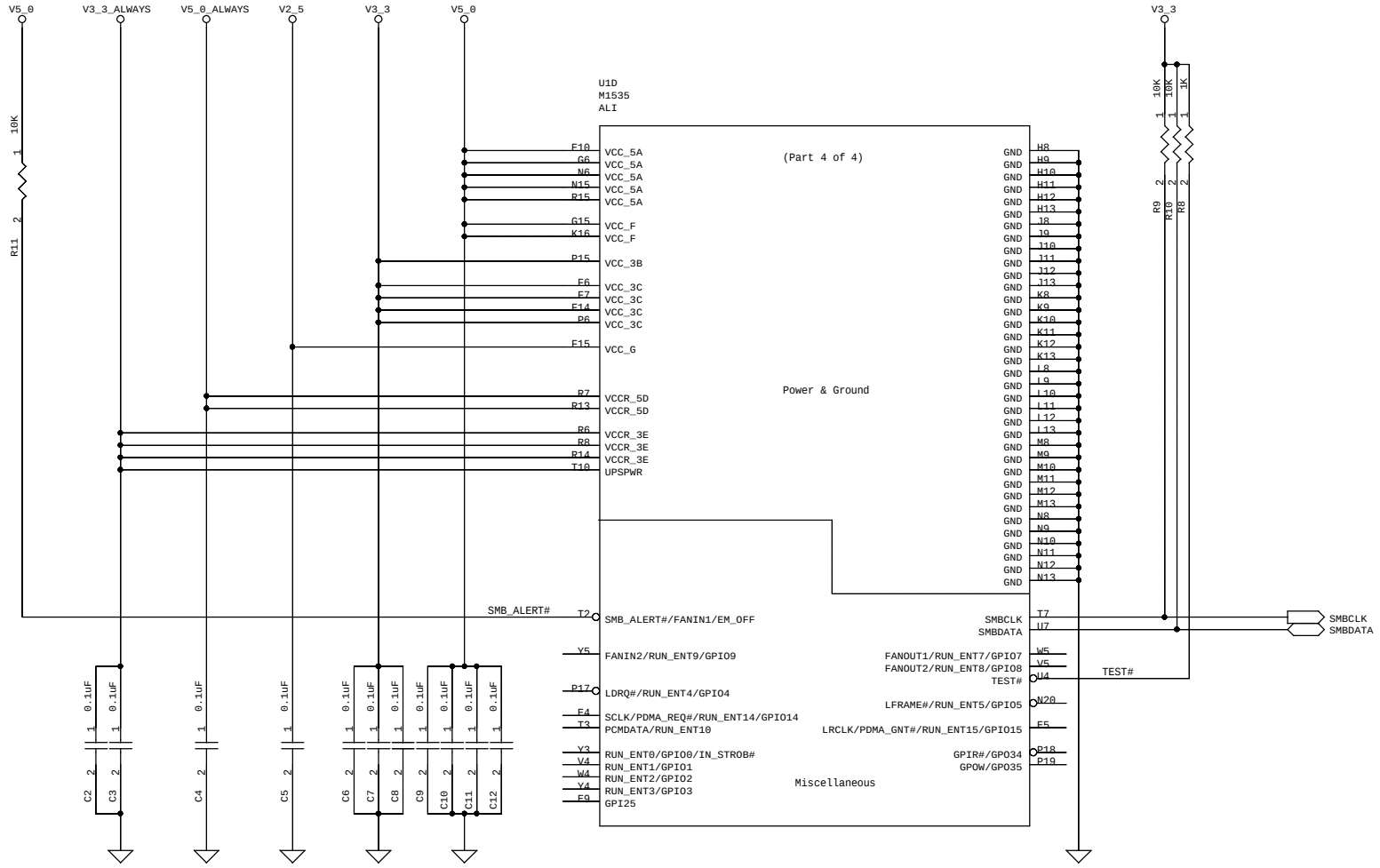

NOTE: THIS SCHEMATIC IS FOR THE ALI 1535 SOUTHBRIDGE ONLY. SEE THE VENDOR DOCUMENTATION FOR ALI 1535+ AND OTHER SOUTHBRIDGE DIFFERENCES.

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6.7 Thermal Design

TM5500/TM5800 processors use a new 474-pin CBGA package. The solder footprint and pinout is identical to the TM5400/TM5600 474-pin CBGA package. The location and dimensions of the exposed silicon die and bypass capacitors on the top of the package have changed on this new TM5500/TM5800 package compared to the previous TM5400/TM5600 package. Note that the exposed silicon die contact area available for the thermal solution has decreased on the TM5500/TM5800 processor (compared to TM5400/TM5600) due to the smaller device die produced by the 0.13µ process technology used to manufacture TM5500/TM5800 processors.

Transmeta strongly recommends die-referenced thermal solutions over PCB-referenced thermal solutions for new systems designed for TM5500/TM5800 processors. Die-referenced thermal solutions allow for possible improved packages with slightly different *Z*-axis dimensions in the future.

Note
Refer to the *Thermal Design Guide* for detailed thermal design information. Thermal design power (TDP) specifications can be found in the *Data Book*

6.8 Thermal Diode and Thermal Sensor

Note
The signals from the thermal diode operate at very low voltage and current levels and are susceptible to induced noise. Transmeta recommends following each manufacturer's design guidelines when incorporating their thermal sensors.

The external thermal sensor device connects to the DIODE_CATHODE and DIODE_ANODE pins of the processor. The ALERT# signal from the temperature sensor is connected to the dedicated THRM# input on the southbridge. This device is powered from V3_3.

Careful layout is required to ensure the lowest noise and greatest accuracy of the thermal sensor/diode.

6.8.1 Thermal Sensor Circuit

The thermal sensing circuit on a TM5500/TM5800 processor-based system has three components: a diode on the processor die, a thermal sensor chip (in a separate package), and the interconnecting circuitry.

The on-chip diode is operated in forward-bias mode with a carefully-controlled (and very small) bias current. In this mode the voltage-temperature curve is essentially linear within the processor operating temperature range.

The thermal sensor chip provides the bias current to the diode, measures the resulting voltage, and sends the information via the SMBUS to the system (usually the southbridge). This chip is available from Maxim (the MAX1617) or from Analog Devices (AD1021). The two chips generate slightly different bias currents, but otherwise operate in the same fashion.

6.8.2 Thermal Sensor Issues

As mentioned, the thermal sensor chip generates a bias current for the diode. This current is on the order of 10-200 nA. This current is carried along the interconnect circuitry to the diode.

On the way from the sensor to the diode (and back again) the current encounters two major sources of noise:

- Crosstalk from adjacent high-speed circuits. The EM fields of nearby circuits can couple inductively into the thermal connector wiring, causing voltage noise on the circuit.

- Leakage currents from power, ground, or signal circuits. There is always some surface resistance on a PCB board in the order of 10 MΩ or more. This means that some leakage current is always present, but is small relative to the current on the sensor. However, surface contamination local to the thermal sensor circuit can lower the surface resistance to 10-100 KΩ. This creates a much larger leakage current. If the source of the current is a power rail, the result is a fairly constant offset of the temperature from the correct reading.

  The thermal connection does allow for a low-pass filter (a 2200 pF capacitor) to filter out some of the noise. However, this is not sufficient to ensure a good reading. It is necessary to lay the board out so that the opportunities for noise to enter the circuit are eliminated, or at least minimized.

6.8.3 Thermal Sensor Layout

There are a number of rules to ensure minimal noise in the thermal sensor circuits:

- Minimize the distance from the processor to the sensor chip.

  This rule minimizes crosstalk because the parallelism with other lines is reduced, and the area of the inductive loop of the circuit is also at a minimum. The opportunities for that area of the system board to become contaminated are also kept to a minimum. If possible, place the sensor chip *directly adjacent* to the processor.

- Route the sensor lines as a differential pair.

  A differential pair is a structure that places the signal and its complement directly adjacent to each other. Route the anode and cathode connections as close as the PCB manufacturing process will allow, 0.004-0.005” is reasonable for most fabricators. Follow this structure from the point that the two signals emerge from the sensor chip to the point the signals enter the processor. Any electromagnetic disturbance that the two lines are subjected to should be rejected by the sensor chip as common-mode noise.

- Route the circuit on internal layers.

  This allows the power planes to act as a shield. If possible, have a layer reserved for sensitive circuitry. Do not run digital lines on the layer adjacent to the thermal circuit.

- Use guard traces.

  Surround the differential pair with a copper trace connected every 0.250” to ground. Do this on ALL layers, not just the routing layers. This serves two purposes:

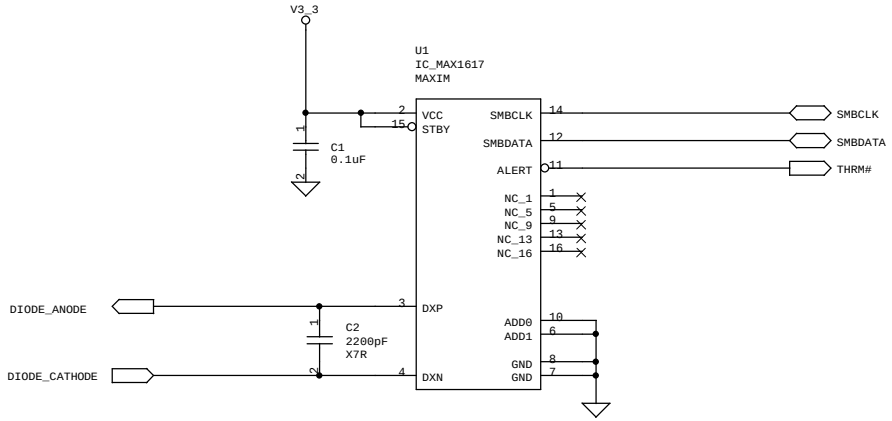
  - Any leakage current that does occur is shorted to ground.
  - It ensures extra distance from noisy circuits to the thermal circuit.

- Keep signal traces away from the thermal circuit.

Do not allow other traces within 0.050” of the thermal pair. While electromagnetic fields may still be present, the gradient of those fields drops exponentially with distance. If the gradient is too large, the two traces are exposed to different field strengths, and the common-mode rejection of the sensor chip has no effect on this noise. Keep the gradient small by separating noise sources from the sensor circuit.

6.8.4 Thermal Sensor Example Schematic

The schematic on the following page illustrates the thermal sensor circuit.



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6.9 TDM Debug Interface Connection

Connect TDCA RESET# directly to the processor RESET# signal, and also to P_PCI_RST# through a 1.2 KΩ resistor. This allows the TDM to override the PCI reset signal and issue a processor reset.

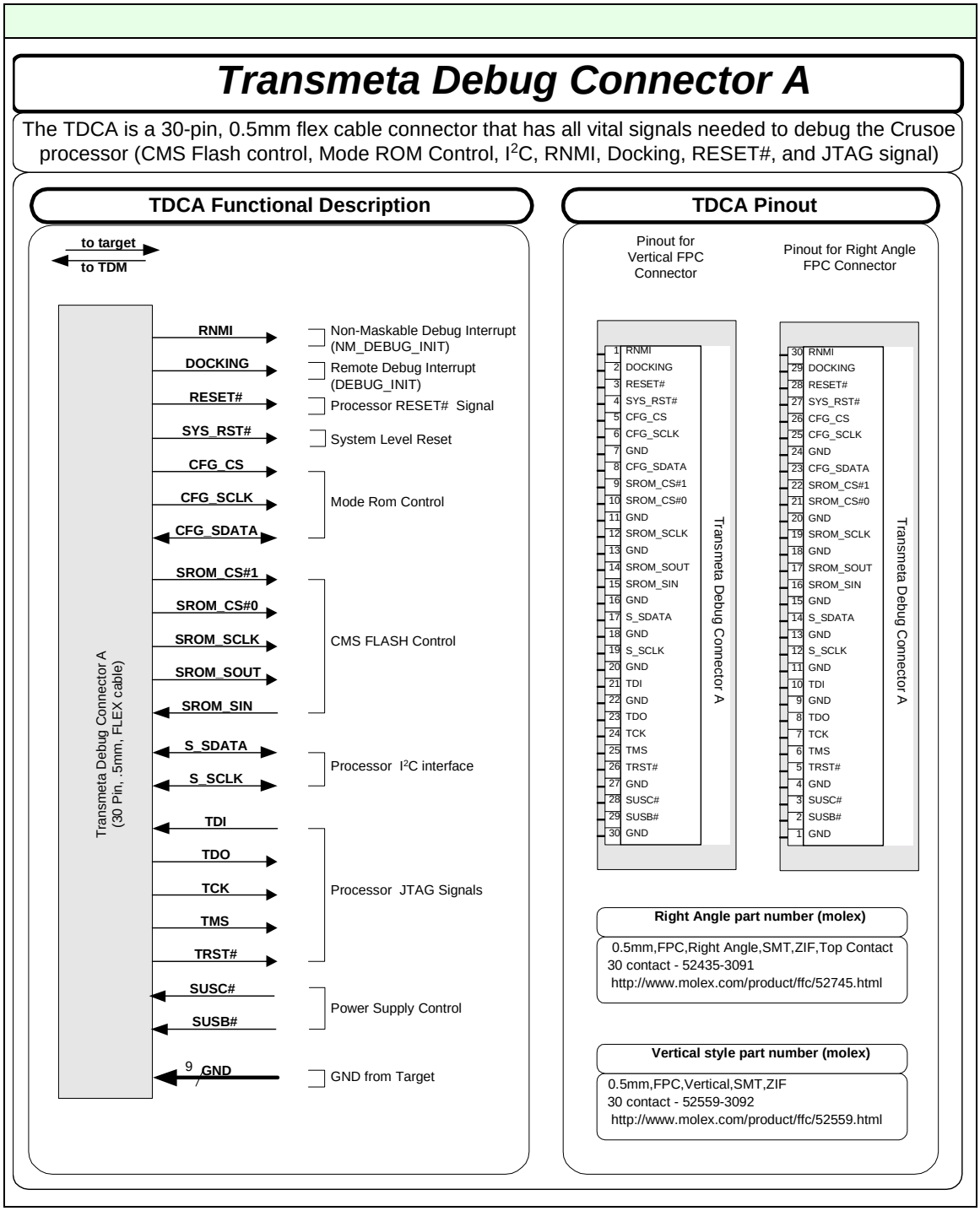
In general, TDM connections to serial ROM devices require a resistor between the processor signal and the ROM device to allow the TDM to override the active signal.

The Transmeta Debug Module (TDM) communicates to the target through a high-density 30-pin flex cable known as TDCA. The TDCA is shown with connections to the core system. The TDM and the debug connection is used for flashing Code Morphing software ROM and the mode-bit ROM, connecting to the Transmeta ICE, and for other debugging purposes.

Note
Exercise caution when plugging or unplugging the TDCA ribbon cable. The pins that make up the interface can be easily bent, and the cable itself is delicate. If problems arise with the TDM unit, try changing the cable first, as it is much more likely to show problems than the TDM.

See the diagram below for the TDM interface pinout and signal descriptions.

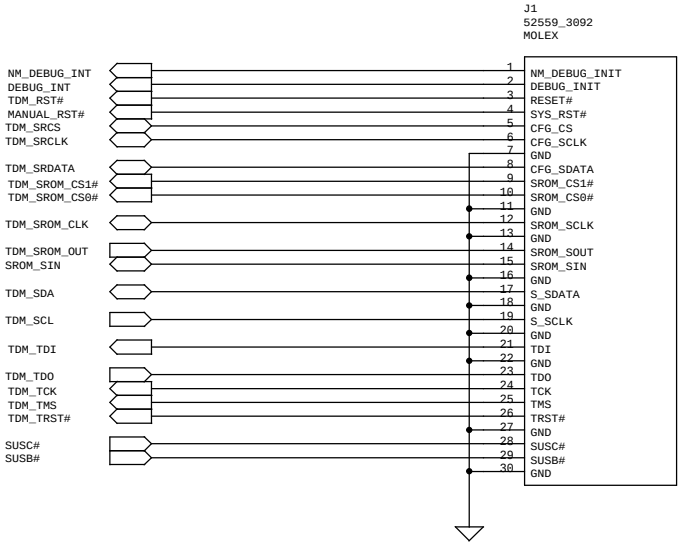
Figure 23: Transmeta Debug Connector (TDCA)



The schematic diagram on the following page shows the TDM interface circuit.

TRANSMETA DEBUG CONNECTOR

NOTE: Pinout depends on type of connector used. The pinout below is for the vertical TDC connector. See the Design Guide for the pinout of the right angle connector.



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Chapter 7

PCB Layout Guidelines

Note
The guidelines in this chapter must be followed for the design to meet specified TM5500/TM5800 processor operating frequencies.

7.1 PCB Design Layout

- For thermal sensor/diode signal routing make sure to follow the guidelines in *Thermal Diode and Thermal Sensor* on page 103.
- V_CPU_CORE is placed on the bottom layer (Signal 4). All other supply voltages are placed on the PWR layer. If possible, place a V_CPU_CORE plane on as many layers as possible.
- GND 1 is the signal return path for traces on Signal 1 and 2. GND 1 plane is to be solid, with no breaks or cuts.
- GND 3 is the signal return path for traces on Signal 3 and 4 (6 and 5 for ten layer stack-ups). The GND 1, GND2, and GND 3 Planes are to be solid, with no breaks or cuts.
- Anti-pad treatment for vias on GND 1, GND 2, GND 3, and PWR layers. Pad diameter is to be smaller than the via hole. With 0.007" to 0.008" clearance from the via hole to the plane. This results in 0.022" to 0.023" copper between vias under the processor. If normal anti-pad treatments were allowed, the amount of copper under the chip would be severely decreased, limiting processor performance.
- Material between PWR and GND 2 layers must be a maximum of 0.005" thick. Thinner is desirable (0.003” should be attainable).
- If the previous note is followed, signals run on Signal 2 (Inner Layer 3) may cross cuts or breaks on the PWR plane (Inner Layer 4). Critical signals may also then be placed on any signal layer.
- HCLK and PCI_CLK to the processor should have matched lengths. Also, each PCI device/slot clock should be matched to this same length.
- All vias on the pad side of the PCB processor BGA footprint must be covered with solder mask. Failure to do so will potentially short signals together during the soldering process.
- Keep trace lengths as short as possible.

- When transitioning signals between the return paths, insert a ground via next to the signal via, i.e. when transitioning from Signal 1 or Signal 2 to Signal 3, or when transitioning from Signal 3 or Signal 4 to Signal 1. This will maintain return path continuity.
- For improved manufacturing of the PCB, 0.006” traces and 0.006” spaces is recommend for the outer two layers (top and bottom), with 0.005” traces and 0.005” spaces on the internal layers.
- DO NOT match impedances on traces wider than 0.006”.
- DO NOT allow cutouts in the ground planes.

7.2 Example PCB Fabrication Notes

- The finished printed circuit board shall meet the requirements of IPC-A-600.
- Configuration of the printed circuit board not specifically dimensioned on the drawing shall be controlled by the Gerber data.
- Material: 0.056” ± 0.006” thick glass epoxy, natural color. Laminated NEMA grade FR4. See layer stack-up for copper weight and layer orientation. Core and prepreg combinations are optional to the manufacturer unless otherwise specified in the layer stack-up.
- Plating: all holes and conductive surfaces shall be plated with 0.001” copper minimum. All copper areas not covered by solder mask shall be solder coated 0.0003” minimum.
- All hole diameters are stated as finished hole sizes.
- Solder mask: photo-imaged liquid polymer on both sides of board in accordance with IPC-SM-840, type B Class 2 over bare copper.
- Component marking: silk-screen component side (and solder side) white, non-conductive epoxy ink. Lands and exposed plated areas to be free of ink.
- Bow and twist: shall not exceed 0.005” per lineal inch.
- Electrical test: the printed wiring board shall be electrically tested for opens and shorts. The results of the electrical test shall be documented and delivered along with each lot.
- Identification: vendor logo to be etched on the solder side, silk-screen date code on the bottom side.
- Characteristic impedance: 55 Ω ± 10%. Note: this will be 60 Ω ± 10% when DDR SDRAM is used in the design.

7.3 Board Design Guidelines

The guidelines provided below were taken from TM5500/TM5800 processor-based reference designs using Allegro PCB layout tools. The dimensions are given in mils (1 mil = 1/1000 = 0.001 inch).

7.3.1 Printed Circuit Board Stackup

Table 17: Recommended Eight Layer PCB Stackup

	Signal/Layer	Material
1	Signal 1	½ oz. copper
2	GND 1	1 oz. copper
3	Signal 2	½ oz. copper
4	PWR	1 oz. copper
5	GND 2	1 oz. copper
6	Signal 3	½ oz. copper
7	GND 3	1 oz. copper
8	Signal 4	½ oz. copper

7.3.2 Allegro Standard Spacing Constraints

Table 18: Standard Spacing/Line/Via Constraints [1]

Constraint Name	Constraint Value
Line-to-line	5 mils
Line-to-pad	5 mils
Pad-to-pad	5 mils
Line width	5 mils
Default via	25/12 mils
Primary/secondary signal via	12/12 mils
Etch on subclass	Allowed
Same net DRC	On

1. Data taken from Allegro.

7.3.3 Allegro Extended Spacing Constraints

Table 19: Extended Global Spacing/Line/Via Constraints [1]

Constraint Name	Default Constraint Value	BGA Constraint Value
Pin-to-pin	5 mils	5 mils
Line-to-pin	5 mils	5 mils
Line-to-line	5 mils	5 mils
Via-to-pin	Note [2]	Note [2]
Via-to-via	10 mils	10 mils
Via-to-line	5 mils	5 mils
Shape-to-pin	5 mils	5 mils
Shape-to-via	5 mils	Note [2]
Shape-to-line	5 mils	5 mils
Shape-to-shape	5 mils	5 mils
Thru pin-to-thru pin	5 mils	5 mils
Thru pin-to-SMD pin	5 mils	5 mils
Thru pin-to-test pin	5 mils	5 mils
Thru pin-to-thru via	10 mils	6 mils
Thru pin-to-test via	10 mils	6 mils
Thru pin-to-buried blind via	10 mils	6 mils
Thru pin-to-line	5 mils	5 mils
Thru pin-to-shape	5 mils	5 mils
SMD pin-to-SMD pin	5 mils	5 mils
SMD pin-to-test pin	5 mils	5 mils
SMD pin-to-thru via	8 mils	7 mils
SMD pin-to-test	8 mils	7 mils
SMD pin-to-buried blind via	8 mils	7 mils
SMD pin-to-line	5 mils	5 mils
SMD pin-to-shape	5 mils	5 mils
Test pin-to-test pin	5 mils	5 mils
Test pin-to-thru via	10 mils	6 mils
Test pin-to-test via	10 mils	6 mils
Test pin-to-buried blind via	10 mils	6 mils
Test pin-to-line	5 mils	5 mils
Test pin-to-shape	5 mils	5 mils
Thru via-to-thru via	10 mils	10 mils
Thru via-to-test via	10 mils	10 mils
Thru via-to-buried blind via	10 mils	10 mils
Thru via-to-line	5 mils	5 mils
Thru via-to-shape	5 mils	Note [2]
Test via-to-test via	10 mils	10 mils
Test via-to-buried blind via	10 mils	10 mils

Table 19: Extended Global Spacing/Line/Via Constraints [1] (Continued)

Constraint Name	Default Constraint Value	BGA Constraint Value
Test via-to-line	5 mils	5 mils
Test via-to-shape	5 mils	Note [2]
Buried blind via-to-buried blind via	10 mils	10 mils
Buried blind via-to-line	5 mils	5 mils
Buried blind via-to-shape	5 mils	Note [2]
Line-to-line	5 mils	5 mils
Line-to-shape	5 mils	5 mils
Shape-to-shape	5 mils	5 mils

1. All etch/layers. Data taken from Allegro.
2. Defined as differential in other places.

7.3.4 Allegro Extended Physical (Lines/Vias) Constraints

Table 20: Extended Physical Constraints [1]

Constraint Name	Default Value	PCI Net Value	CLK Net Value
Maximum line width	5 mils	5 mils	5 mils
Minimum neck width	5 mils	5 mils	5 mils
Maximum neck length	0 mils	0 mils	0 mils
Allow on etch subclass	Allowed	Allowed	Allowed
T-junctions	Anywhere	Pins and vias only	Pins and vias only
Minimum blind buried via stagger	5 mils	5 mils	5 mils
Maximum blind buried via stagger	5 mils	5 mils	5 mils
Pad-pad direct connect	Not allowed	Not allowed	Not allowed
Current via	25/12 mils	25/12 mils	25/12 mils

1. All etch/layers. Data taken from Allegro.

7.3.5 Allegro Extended Electrical (Lines/Vias) Constraints

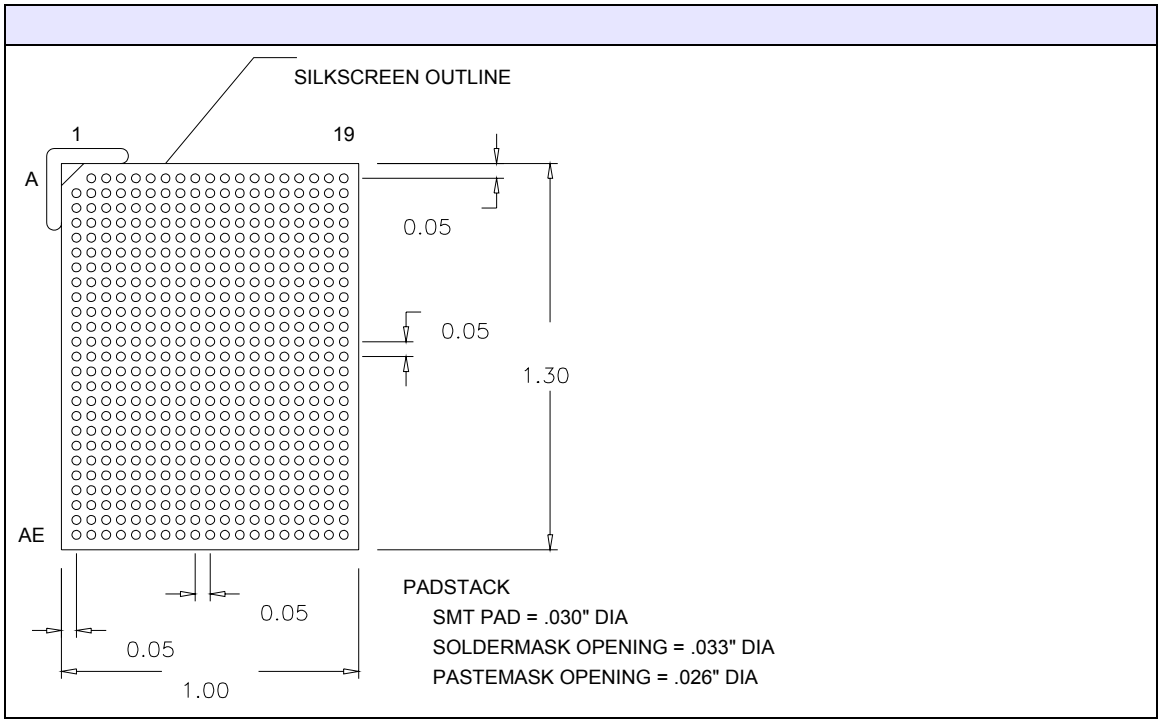
Table 21: Extended Electrical Constraints [1]

Net Category	Maximum Stub Length	Maximum Via Count/Net
Default	Unlimited	Unlimited
PCI	1500 mils	6
CLK	600 mils	5
DDR	300 mils	4
SDR	300 mils	4

1. All etch/layers. Data taken from Allegro.

7.4 Footprint and Pin Escape Diagram

Figure 24: Mechanical Footprint



Appendix A

System Design Checklists

The checklist **Status** field is for designers and implementers to use as the project progresses. Use as follows:

Status	Description
P	Task is pending (waiting for other assistance, etc.)
C	Coding - implementation/testing in progress
V	Implementation verified
O	Other group's function
blank	Task not begun

Power Supply Checklist

Item	Description	Status
1.	Processor power supply ramp-up must be properly sequenced. See Chapter 3, *Power Supply Sequencing* in the *System Design Guide* for details on power sequencing requirements.	
2.	The VRDA (VID) pin connections between the processor and the V_CPU_CORE (CVDD) regulator should meet the following requirements: • The processor VRDA outputs are open-drain, and therefore require pull-ups. If the VRM controller does not have internal pull-ups on its VID inputs, then external pull-up resistors must be used. At no time can the VRDA signals be pulled up to a voltage greater than 3.3 V plus a diode drop. • Ensure that VRDA signals are connected to the correct corresponding VID pins (VRDA[0] to VID[0], etc.)	
3.	The POWERGOOD output of the V_CPU_CORE (CVDD) regulator must not glitch during LongRun power management transitions. Designs that do glitch must include a low pass filter, isolated from down-stream logic, to remove the glitch from the regulator POWERGOOD output. Note that regulators qualified by Transmeta for TM5500/TM5800 processor have their POWERGOOD output blanked during transitions to alleviate this problem.	

Power Supply Checklist

Item	Description	Status
4.	If an independent voltage monitor is used to generate POWERGOOD, the signals below should be connected correctly: • All power inputs should be connected to ACPI System S0 State power (not STR or always-on power). • Manual reset (if supported) - no isolation resistors are needed between different sources driving that pin (unless a source is push-pull instead of open-drain). No capacitor is needed on the manual reset pin either. The device should have a guaranteed 100 mS negation of POWERGOOD that acts as a much better debounce filter than an external capacitor. The manual reset input of an independent monitor is an ideal place to connect the SYS-RST# pin of the Transmeta debug connector.	
5.	ACPI System Power state support: • All ACPI System S0 State power in the system, including all processor power, should be controlled by the OFF_PWR1# pin on the ALI 1535. • ACPI System S3 State power (DRAM power) supplies should be controlled by the OFF_PWR2# pin on the ALI 1535. Rise time control should be used to minimize glitching/drooping of S0 power.	
6.	Make sure all voltage regulators operate within the specified tolerance range printed in the *Data Book*. Verify that these voltages remain within tolerance across all operating conditions for the system.	
7.	All ceramic decoupling capacitors should be X7R dielectric material. No Y5V or Y5U material should be used.	
8.	V_CPU_CORE (CVDD) decoupling: • High frequency: at least 8 low-ESL ceramic capacitors on the back side of the board directly underneath the processor. The case size should be as small as possible - 0402, 0306, or 0603 are recommended. The dielectric should be X7R, and the value should be the highest supported in the chosen case size with an X7R dielectric. Typically, this value is 0.22 µF or 0.1 µF. • Mid frequency: approximately 14 low-ESL ceramic capacitors as close to the processor as possible. Recommended value is 1 µF with 0805 case size and X7R dielectric. • Low frequency: at least 800 µF. The combined ESR of all the low frequency capacitors together must be less than 0.005 Ω.	
9.	3.3 V (IOVDD) switched supply decoupling at the processor: • High frequency: none required. • Mid frequency: approximately 10 low-ESL ceramic capacitors as close to the processor as possible. Recommended value is 1 µF with 0805 case size and X7R dielectric. • Low frequency: two low-ESR capacitors, 22 µF each.	
10.	2.5 V (IOVDD25) switched supply decoupling at the processor: • High frequency: none required. • Mid frequency: if DDR memory is supported, approximately 8 low-ESL ceramic capacitors as close to the processor as possible. If DDR memory is not supported, only 1 such capacitor is needed. For each of these capacitors, the recommended value is 1 µF with 0805 case size and X7R dielectric. • Low frequency: if DDR memory is supported, one low-ESR capacitor of 22 µF. If DDR memory is not supported, no low frequency decoupling on 2.5 V switched is required.	

Power Supply Checklist

Item	Description	Status
11.	If DDR memory is supported, the decoupling on 2.5 V STR at the DRAMs should be: • High frequency: approximately 3 low-ESL ceramic capacitors as close as possible to the power pins of each DRAM. Recommended value is 0.1 µF with 0603 case size and X7R dielectric. • Mid frequency: none required. • Low frequency: one 10 µF capacitor for approximately every 2 DRAMs. Each capacitor should be either ceramic or low-ESR tantalum.	
12.	Ensure that PLLVDD tracking circuit has been incorporated.	

DRAM Checklist

Item	Description	Status
1.	Designs with no DDR should connect the high-order SDR chip selects to the most permanent bank of memory. That is, CS[3:2], CLK[3:2], and CKE1 should connect to the most permanent banks of SDR.	
2.	The CKE high-speed bidirectional level-translator should be: • Controlled by SUS_STAT1# (pin T17) on the iPIIX4 or SUSPEND# (pin W13) on the ALI 1535 . • Controlled by the same signal that is connected to the processor SLEEP# pin. • Powered by at least 4.3 V. If less than 4.3 V is used, the signals will be clamped, and noise margin will be reduced.	
3.	There can be no more than 8 DDR devices.	
4.	DDR and SDR x32 memory is not supported.	

SDR SDRAM Address Line Connections[1]

Processor Signal		DRAM Signal	JEDEC SODIMM-144 Pin Number	JEDEC DIMM-168 Pin Number
Name	Pin Number			
S_A[0]	P3	A0	29	33
S_A[1]	N4	A1	31	117
S_A[2]	V5	A2	33	34
S_A[3]	P4	A3	30	118
S_A[4]	N5	A4	32	35
S_A[5]	M1	A5	34	119
S_A[6]	P1	A6	103	36
S_A[7]	N1	A7	104	120
S_A[8]	P2	A8	105	37
S_A[9]	N2	A9	109	121
S_A[10]	M2	A10 / AP	111	38
S_A[11]	K1	A11	112	123
S_A[12]	K2	A12	70	126
S_BA[0]	L2	BA0	106	122
S_BA[1]	L1	BA1	110	39

1. Designs containing an SDR SODIMM should connect the address lines as shown in this table.

PCI Checklist

Item	Description	Status
1.	All the PCI REQ and GNT signals must have pull-ups to V3_3 (IOVDD).	
2.	All IDSEL series resistors should be 100 Ω.	
3.	The PCI LOCK# pin on the processor should be pulled up to 3.3 V switched and not connected to anything else. TM5500/TM5800 processors do not support locked PCI cycles. All other PCI LOCK# pins in the system should be connected together and pulled up.	
4.	No PCI signal should rise above 3.3 V because the processor is not 5 V tolerant. If the design contains any components that drive 5 V PCI signals, a high-speed bidirectional level-translator is needed at the processor to clamp it to 3.3 V. Such a translator is also needed if a PCI edge connector is present that is keyed for 5 V.	

Serial Bus Checklist

Item	Description	Status
1.	The SMBus from the southbridge should not be connected to the Serial Debug Bus (i.e. pins SD_SCLK and SD_SDATA). The Serial Debug Bus must be connected to the Transmeta debug connector and be pulled up to V3_3 (IOVDD).	
2.	If the Code Morphing software serial ROM is supported, the write protection PLD should be implemented. Check for the following: • The pull-up on CS# should be at the PLD input and not its output. The processor tri-states the PLD input during Deep Sleep, but the PLD always drives the output. • The latest reference design pinout should be supported. The write protect signal should connect to pin 2 of the DIP/TSOP or pin 3 of the PLCC. The CS# signal should connect to pins 4 and 5 on the DIP/TSOP and pins 5 and 6 on the PLCC. • None of the pins are 5 V tolerant, so the signal driving the write protect line should have a 3.3 V swing. • The PLD should be a 3.3 V part with a feature to reduce power consumption when inputs are not toggling. • All unused inputs and tri-stated outputs should be connected to ground. Pins 18, 19, and 23 on the DIP/TSOP and pins 20, 21, and 27 on the PLCC should be no-connected.	
3.	All new designs must include a mode-bit ROM circuit. For older system designs that did not provide mode bit ROM support, a strapping resistor should be present on the mode bit ROM data line (i.e. pin CFG_SDATA) to support each applicable boot option below: • Boot from serial Code Morphing software ROM: 10 KΩ pull-up to 3.3 V switched. • Boot from parallel ROM: 10 KΩ pull-down.	
4.	The debug connector should be wired properly to both the mode-bit ROM and serial Code Morphing software ROM: • Series resistors (220 Ω each) on all the signals between the processor (or PLD) and the ROMs. • No series resistor on all the signals between the debug connector and the ROMs. • Correct pinout on the debug connector. The most common mistakes are reversing the pin order and swapping SROM_CS[1:0]#. On the vertical connector, pin 1 is RNMI. On the right angle connector, pin 1 is GND. SROM_CS1# should be on pin 9, and SROM_CS0# should be on pin 10.	
5.	If the serial Code Morphing software ROM is implemented, the 28-pin Atmel part should be used. The 32-pin Atmel part and the Macronix part have both been discontinued.	

Other Signals Checklist

Item	Description	Status
1.	Correct pull-up and pull-down resistors should be configured as described in Chapter 6, *Signal Pull-ups and Pull-downs* in the *System Design Guide*.	
2.	The SLEEP# pin should be driven by the proper signal on the southbridge: • ALI 1535: an AND gate whose inputs are SUSPEND# (pin W13) and AGP_STP# (pin E11). The AND gate must have 5 V tolerant inputs and a 3.3 V output. • The processor Reserved pin G2 should control the unprotect feature of the parallel ROM.	
3.	If a unified ROM (i.e. Code Morphing software and BIOS in a parallel ROM) is supported: • EPROMA[2:1] should connect to the highest order address lines on the parallel ROM. • The processor's GPIO should switch 12 V onto the parallel ROM.	
4.	The Maxim thermal sensor should be connected as follows: • MAX1617 pin 3 to processor pin A18. • MAX1617 pin 4 to processor pin B16. • MAX1617 alert output to THERM# input of ALI 1535. • If a MAX1619 is supported, the OVERH# output should not be used.	
5.	The free running PCI clock (PCICLK_F) should connect to the processor's PCI clock input as well as the southbridge PCI clock input. Since most clock generators have only one free running PCI clock, special routing considerations are necessary. See also Chapter 6, *Using CLKRUN* in the *System Design Guide*.	
6.	The RESET# pin on the Transmeta debug connector must be connected to reset only the processor. The SYS_RST# pin on the Transmeta debug connector should be connected in such a manner as to reset the entire system when asserted. All processor reset pins should be connected as shown in the Chapter 6, *System Reset*, in the *System Design Guide.*	

Appendix B

Serial Write-protection PLD Data

JEDEC Fuse Map and CUPL Source Code

24-Pin TSSOP

The following text is the JEDEC file representing the fuse map for the write protection PLD. It was produced by the CUPL PLD design compiler for a 24-pin TSSOP package. CUPL source code is also shown below.

.

Figure 25: Write Protection TSSOP-24 JEDEC Fuse Map

```
QP24*
QF5892*
G0*
F0*
L00000 11111111111111101110111111111111*
L00032 11111111111111111111111111111111*
L00064 11111111111111111111111111111111*
L00096 11111111110110111111111111111111*
L00128 11111111111111111111111110101111*
L00160 11111111111111111111101111111111*
L00192 11111011101111111111111111111111*
L00224 01111111111111111011011111111111*
L00256 11111111000000000000000000000000*
L02144 00000000000011111111111111111111*
L02176 11111111111111111111111111111111*
L02208 11111111111011011111111111111111*
L02240 11111111111101111111110111011111*
L02272 11111111111111111111111101111111*
L02304 11101110111111111111111111110000*
L02880 00000000000000000000000011111111*
L02912 11111111111111111111111111111111*
L02944 11111111111110111111110111011111*
L02976 11111111111111111111111111111111*
L03008 11011110111111111111111111111111*
L03040 11110111111111011101111101111111*
L03072 11111111111111111011111111101110*
L03104 11111111111111111111000000000000*
L03648 00001111111111111111111111111111*
L03680 11111111111111111111111111111111*
L03712 10011111111111111111111111111111*
L03744 11111111111110111110111111111111*
L03776 11111111111110111111111110111111*
L03808 10111111111111111111111101111111*
L03840 11111011111101111111111111111111*
L05792 00000000000000000100000010100100*
L05824 00000011000000000000000000000000*
C6A76*
```

Figure 26: Write Protection TSSOP-24 CUPL Source Code

```
Name     wrprotpd;
PartNo   0;
Date     8/09/00;
Revision 3;
Designer Transmeta;
Company  Transmeta;
Assembly 1;
Location 1;
Format   j;          /* Use JEDEC output format */
Device   G22V10CP;   /* This is the code for a 24-pin TSSOP package. */
                     /* The powerdown function on pin 4 is implied by */
                     /* this description. */

/*****************************************************************
 *
 * This device protects against writes and erases to the serial flash
 * when the WP pin is asserted.  It works by forcing the chip select
 * to negate when a write or erase command is detected.  The WPNEG
 * pin causes the WP input to be inverted in case WP is active-low on
 * the circuit board.  Two chip selects are handled for the case of
 * two half-size serial ROMs.
 *
 * A select input pin is used to choose between Atmel and Macronix.
 * The reason this is needed is the opcodes between the two parts are
 * similar enough to require detection of all 8 bits of the opcode.
 * If the chip select is negated after the 8th bit of the opcode, the
 * flash device will execute the command with bogus address and data.
 * The select input allows write or erase opcodes to be detected in as
 * few as two bits.
 *
 * This design file is written for the CUPL programmable logic
 * compiler.  A free, functional, demo version of the compiler is
 * available from http://www.logicaldevices.com/.
 *
 *****************************************************************/

/*
 *  Input pins
 *
 *  All unused inputs should be tied high or low on the circuit board.
 *  Active-low pins are denoted by the ! prefix.  After the input and
 *  output sections of this file, all syntax refers to the logical
 *  level of a pin and not its physical level.
 */
PIN  1 =  CKIN;    /* Serial flash clock */
PIN  2 =  WP;      /* Write protect */
PIN  3 =  DIN;     /* Serial flash data input */
/* PIN 4 = PD;     Powerdown pin, implied by device selection */
PIN  7 =  WPNEG;   /* Write protect negate: */
                   /*   Tie low  if WP is active-high */
                   /*   Tie high if WP is active-low */
PIN  8 =  SEL;     /* Select type of flash: */
                   /*   High = Macronix */
                   /*   Low  = Atmel */
PIN  5 = !CS0IN;   /* Intercepted serial flash chip selects.  If */
PIN  6 = !CS1IN;   /*   one is unused, it should be tied high. */
```

Figure 26: Write Protection TSSOP-24 CUPL Source Code (Continued)

```
/*
 *  Output pins
 */
PIN [18,19] = [Q0..1];   /* Flip-flops for the state machine */
PIN 17      = !CS0OUT;   /* New serial flash */
PIN 23      = !CS1OUT;   /*    chip selects */

/*
 *  Assign asynchronous reset (AR) controls on all flip-flops
 *
 *  When both chip selects are negated, the state machine needs to
 *  reset to the BIT7 state.  Otherwise, it will never know when bit 7
 *  of the opcode occurs.
 */
Q0.AR = !CS0IN & !CS1IN;
Q1.AR = !CS0IN & !CS1IN;

/*
 *  Assign synchronous preset (SP) and output enable (OE) controls on
 *  all flip flops
 */
Q0.SP = 'b'0;
Q1.SP = 'b'0;
Q0.OE = 'b'1;
Q1.OE = 'b'1;

/*
 *  State names and numbers
 *
 *  To guard against output glitches, the state numbers are assigned so
 *  that most transitions only change one flip-flop.
 */
$DEFINE BIT7         'b'00
$DEFINE BIT6         'b'11
$DEFINE PAT_MATCH    'b'10
$DEFINE NO_PAT_MATCH 'b'01

/*
 *  State transitions
 *
 *  The write or erase opcodes used by Crusoe are:
 *    Macronix:
 *      F2h    Page Program
 *      F1h    Sector Erase
 *    Atmel:
 *      82h    Direct Program through Buffer
 *  The read opcodes used by Crusoe are:
 *    Macronix:
 *      83h    Read Status
 *      52h    Read Array
 *    Atmel:
 *      57h    Read Status
 *      52h    Main Memory Page Read
 */
```

Figure 26: Write Protection TSSOP-24 CUPL Source Code (Continued)

```
SEQUENCE [Q1..0]
{
  PRESENT BIT7
    IF !DIN        NEXT NO_PAT_MATCH;  /* No write or erase opcode */
                                       /*   has bit 7=0 */
    IF  DIN & !SEL NEXT PAT_MATCH;     /* For Atmel, bit 7=1 means a */
                                       /*   write or erase */
    IF  DIN &  SEL NEXT BIT6;          /* For Macronix, need to keep */
                                       /*   checking */
  PRESENT BIT6
    IF  DIN NEXT PAT_MATCH;            /* Must be F1h or F2h */
    IF !DIN NEXT NO_PAT_MATCH;         /* Can't be F1h or F2h */
  PRESENT PAT_MATCH
    NEXT PAT_MATCH;                    /* Only way out is reset */
  PRESENT NO_PAT_MATCH
    NEXT NO_PAT_MATCH;                 /* Only way out is reset */
}

/*
 *  Output equations
 *
 *  Each chip select is copied from input to output unless the current
 *  state is PAT_MATCH and the WP input is asserted.  In that case,
 *  both chip selects are negated.  If WPNEG is asserted, the sense of
 *  WP is reversed.
 *
 *  For the unusual case of WP being asserted after a write or erase
 *  opcode but before the end of the bus cycle, both chip selects will
 *  immediately negate.
 */
CS0OUT = CS0IN & !((WP $ WPNEG) & Q1 & !Q0);
CS1OUT = CS1IN & !((WP $ WPNEG) & Q1 & !Q0);
/*                     ^-- $ is the XOR operator in CUPL */
```

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