System Design Guide

Transmeta Crusoe™ Processor

Model TM5400/TM5600

Preliminary Information

Confidential Information—NDA Required

TRANSMETA Corporation

Crusoe™ Processor Model TM5400/TM5600

System Design Guide
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Confidential Information—NDA Required

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Overview

This design guide describes the specific details of a notebook PC motherboard design for the Crusoe™ Processor Model TM5400/TM5600 (hereafter known as TM5400/TM5600).

The core block diagram (see Figure 1) shows the major elements of a design that connect to a Transmeta TM5400/TM5600 Processor. All connectivity, with a few exceptions, between the processor and other core elements has been shown. Special considerations and signals not shown in the diagram are described in the text. TM5400/TM5600 Reference Schematics that show detailed electrical connectivity are available. A full description of the schematics is provided in this text. The description at the block diagram level is intended to provide a broad overview of processor design issues. For specific details about the TM5400/TM5600 reference design see the descriptions of the schematics in Chapter 5, *Crusoe Processor Reference Schematics Description*. Note that schematics describe both the TM3200 and TM5400/TM5600 processors.

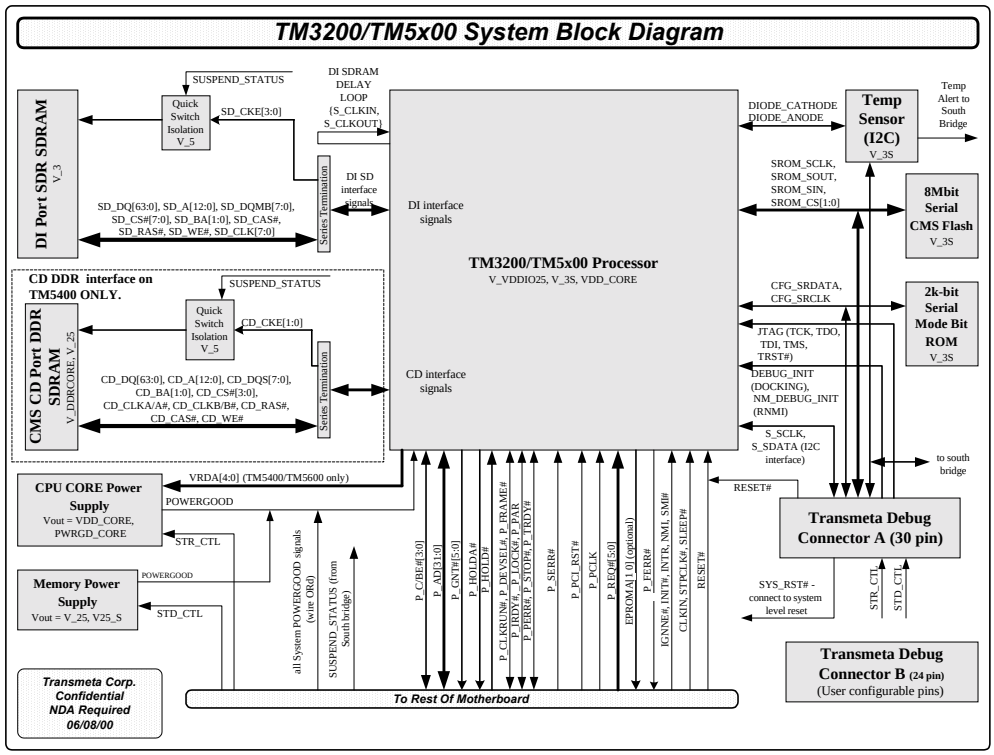
These are some of the terms used in this book:

SUSPEND_STATUS	Status output from the south bridge to signal that a power suspend state is being entered. (SUS_STAT# from the Intel PIIX4 and SUSPENDJ from the ALI M1535)
STR_CTL	Suspend to RAM control signal output from power management section of south bridge. (SUSB# from the Intel PIIX4 and OFF_PWR2 from the ALI M1535).
STD_CTL	Suspend to disk control signal output from the power management section of south bridge. (SUSC# from the Intel PIIX4 and OFF_PWR3 from the ALI M1535).
STR	Suspend to RAM power down state. In this power management state, system state is preserved in RAM while power to the processor is removed. (RAM remains powered on in self-refresh mode). AKA Power state S3.
STD	Suspend to disk power down state. In this power management state, system state is preserved in the hard disk and power is off to the rest of the system (including RAM). AKA power state S4.
V_3	3.3V power supply, always on.
V_3S	3.3V power supply, switched. This supply is turned off during STR and STD power down states.

Chapter 1

System Block Diagram

FIGURE 1 Core System Block Diagram



The TM5400/TM5600 includes both the CPU and the North Bridge functionality. To a motherboard designer, this means that the processor looks very much like a north bridge. The TM5400/TM5600 supports two DRAM interfaces, one for DDR (Double Data Rate) SDRAMs (CD DRAM port), and the other for regular SDRAMs (DI DRAM port). On the TM5400/TM5600, designers can choose to use either SDRAM interfaces, together or independently, depending on their design's cost and performance requirements.

In the diagram, note how the power signals that feed the component are listed in each block. This helps the reader to identify suspend and switched power distribution to core components. Descriptions of each supply are described in *Power Supply Requirements* on page 14.

The major elements shown in the block diagram are as follows:

- CD Port DDR SDRAM. Can support up to 2 banks of DDR DRAMs in various configurations of 64Mbit, 128Mbit, or 256Mbit devices.
- DI Port SDR SDRAM. The TM5400/TM5600 can support up to 4 banks of various configurations of 64Mbit, 128Mbit or 256Mbit devices.
- The CPU core switched mode high efficiency power supply.
- The 2.5V power supplies for the I/O power pins on the DDR SDRAMs and TM5400/TM5600 DDR interface. On the TM3200, connect IOVDD25 and C_VREF to VDDCORE.
- The Thermal Sensor. This connects to a thermal sensing diode built into the processor.
- The 2Kbit Mode Bit SROM. System dependent configuration options vital to proper chip operation are stored in this device and read by the processor at boot time.
- The 1Mbyte serial flash ROM for CMS. This is optional but recommended. CMS is stored in this device. Other options for CMS code (such as sharing BIOS ROM) are described in the text.
- The Transmeta Debug Module (TDM) connector. This adds some low level debug support to facilitate in design bring up as well as connectivity to the Transmeta ICE for software development.
- SDRAM Quick Switch Isolation. These are used to ensure that CKE signals to the SDRAMs remain stable during processor power transitions. Since the Crusoe processor does not have a suspend-power well, output signals are undefined during power transitions and subject to glitch.
- There are several elements and signals not shown but are described in the text below.

1.1 Power Supply Requirements

The block diagram shows the power supplies for each of the major components. The power source for all notebook computers is either a battery (< 20V) or a DC wall adapter of a comparable voltage. An intelligent switching mechanism is needed to create a stable V_DC or V_SOURCE that is used to supply the regulators that generate system voltages.

The power supply network must be capable of generating the following supplies for the system:

TABLE 1 Power Supply Requirements

Power Supply	Description
V_3	3.3V that is valid for all power states except for Suspend to Disk(STD)/Soft off (SOFF) states (controlled by STD_CTL Power Management control signal)
V_3S	3.3V Switched that is valid for all states except Suspend to RAM (STR) and STD/SOFF (controlled by STR_CTL)
V_25	2.5V that is valid for all power states except for STD/SOFF (controlled by STD_CTL)
V_25S	2.5V Switched that is valid for all power states except for STR and STD/SOFF (controlled by STR_CTL)
V_5	5V that is valid for all power states except STD/SOFF (controlled by STD_CTL)
V_5S	5V Switched that is valid for all power states except STR and STD/SOFF (controlled by STR_CTL).
VDD_CORE	The TM5400/TM5600 has VRDA pins which can be connected to the VDD_CORE regulator to do dynamic power management.
POWERGOOD_CORE	Reset type signal that is the wire OR of the POWERGOOD signals from each of the system supplies. Signal is valid when all of the system voltages are stable.

The block does not show the supply that generates V_3, V_3S, V_5, and V_5S.

NOTE All power supplies to the processor must be powered on at the same time. All supplies must have similar switch on and off characteristics within 10ms of each other.

Current requirements of each supply should be calculated on a per design basis.

There are several ways to design a power supply that can accomplish the above requirements. See the Reference Schematics for an example of the supplies.

Power supply connections made to each system block are discussed within the individual block discussions.

1.2 Description of Elements in System Block Diagram

1.2.1 Processor

PCI and PC Compatibility

- The PCI interface is 33MHz, 3.3V. The arbiter supports five REQ/GNT pairs. CLKRUN is supported.
- The PCC (PC compatibility) signals are used in communication with the south bridge. These include INIT, NMI, SMI, STPCLK, IGNNE, FERR, CPURST, INTR

Power Supply

The processor uses V_25S for IOVDD25 (2.5V used for CD interface I/O), V_3S for IOVDD (I/O supply for all 3.3V pins), and VDD_CORE for CVDD (variable core voltage).

See power supply layout and decoupling section for recommendations.

1.2.2 CD DDR SDRAM

The CD DDR SDRAM port is only supported on the TM5400/TM5600.

The TM5400/TM5600 CD memory port supports 64Mbit, 128Mbit, or 256Mbit DDR SDRAM devices. It is capable of running at extremely fast rates (see processor spec for details). The frequency at which DDR is capable of running depends on several factors. Loading is critical and it is recommended that only 1 bank of x16 bit devices be used to minimize load count. Also, it is not recommended to use DDR memory on a DIMM or other expansion method since this can load the signals too much. The interface is capable of 2 banks of DDR memory and, although the interface can function with more loading than recommended, it will be at the cost of speed and performance. The recommended configuration, again, is 4 devices of x16 bit memory, soldered to the PC board incorporating the layout guidelines described in the Layout Considerations part of this document.

Clock enable isolation during power down states

The CD_CKE[] clock enable signals need to be isolated between the TM5400/TM5600 and the SDRAM. This is because power states exist where the TM5400/TM5600 is powered down and the SDRAM remains powered (STR). The TM5400/TM5600 does not have a suspend-power well and, like any CMOS circuitry, the outputs are undefined for short periods of time during power transitions. It is likely that all the signals glitch as power is applied or removed from the chip. If the clock enable signal on the SDRAM remains at a stable state, which prevent activity within the SDRAM during power transitions, the data integrity is ensured. The SUSPEND_STATUS signal from the south bridge remains asserted while in STR

mode and is therefore used to control the isolation. It is recommended that a Quicklogic QS3257 quick switch MUX or similar part be used. The output should MUX between a pull-down and the CD_CKE[] signal from the TM5400/TM5600; controlled by SUSPEND_STATUS. See TM3200/TM5400/TM5600 Reference Schematics for example circuit.

Signal termination

Series termination is recommended on all signals. Impedance should be calculated per specific designs. See Reference Schematics for example termination.

Power Supply

The VDDIO25 power supply pins of the DDR memory are connected to V_25. Currently, there are 2 types of DDR SDRAM that operate from different CORE voltages. V_DDRCORE should be connected to either V_25 for 2.5V or V_3 for 3.3V depending on the type of DDR used in the design.

Connect the TM5400/TM5600 VDDIO25 to V25S. The CD interface for a TM5400/TM5600 has a C_VREF input which requires VDDIO25/2. This should be generated with a 1% voltage divider from V25S as in the Reference Schematics.

1.2.3 DI SDR SDRAM

NOTE DI memory termination values have changed. Use 22 ohms on data lines, 10 ohms on addr/control signals. PCB trace impedance of all signals should be 60 ohms. See *DI PCB Layout Guidelines* on page 27.

The TM5400/TM5600 DI single data rate SDRAM port is very similar to the CD port but less restrictive since the clock rates are lower. The frequency at which the DI port is run is dependent upon the loading so care must still be taken to ensure that it is minimized.

The TM5400/TM5600 DI port supports only 4 banks of SDRAM. There are 4 clocks and 2 clock enables.

Recommended Configurations

Timing is the main consideration in DI SDRAM selection. In order to operate at the highest speeds, it is recommended that only homogeneous solutions of either socketed DIMM memory or soldered down memory be used. When using DIMMs, it is recommended that the memory boards use x16-bit devices to lower the overall device count and signal loading. Also, it is recommended that only a maximum of 2 DIMM slots be used to meet high speed loading requirements and also retain compatibility with Crusoe processors.

Bank Selection

The Crusoe architecture forces CMS memory to be in the highest physical addresses. The banks are paired to support up to 2 DIMMs on the TM5400/TM5600. If the permanent memory in the system is soldered down, use S_CS#[2]. If a DIMM is used, connect S_CS#[3:2] to it.

Signal Delay Loop

On the SDR interface, the clock output named S_CLKOUT feeds back to the input named S_CLKIN. The propagation delay of this feedback signal is used to adjust the setup and hold time of SDR read data. It should be terminated just like the other SDR clocks: with a 33 ohm series resistor at the source. The total propagation delay of this signal includes the portion before and after the series resistor. That total should be equal to the sum of the average data line length and the average clock line length.

Clock Enable Isolation During Power Down States

The S_CKE#[] clock enable signals need to be isolated between the processor and the SDRAM. This is because power states exist where the processor is powered down and the SDRAM remains powered (STR). The processor does not have a suspend-power well and, like any CMOS circuitry, the outputs are undefined for short periods of time during power transitions. It is likely that all the signals glitch as power is applied or removed from the chip. If the clock enable signal on the SDRAM remains at a stable state, which prevent activity within the SDRAM during power transitions, the data integrity is ensured.

The SUSPEND_STATUS signal from the south bridge remains asserted while in STR mode and is therefore used to control the isolation. It is recommended that a Quicklogic QS3257 quick switch MUX or similar part be used. The output should MUX between a pull-down and the S_CKE#[] signal from the processor; controlled by SUSPEND_STATUS. See the Core Reference Schematics for example circuit.

Signal Termination

Series termination is recommended on all signals. Impedance should be calculated per specific design. See the Reference Schematics for termination example.

Miscellaneous Notes

If DIMMs are used, be sure to connect serial presence detect bus to the south bridge (not shown).

All SDRAM power supplies should be connected to V_3 (controlled by STD_CTL).

8Mbit Serial CMS Flash

Since the Crusoe processors are hybrids that uses a blend of hardware and software to emulate an x86 processor, the hardware requires a serial flash memory device where the CMS (Code Morphing Software) is stored. CMS needs 1MB of memory in its compressed state. The SROM interface has all the signals needed to interface to 2 manufacturer's serial flash ROM devices (Macronix and Atmel). There is no standardized

format for serial flash devices at the time of the processor's design, so the format that was common to these manufacturers was selected as the interface.

To date, Atmel has up to 8Mbit devices and Macronix has up to 4Mbit devices. If using a single 8Mbit device, only one chip select is needed, else, both are used to interface to the memory.

See the Reference Schematics for circuit example using Atmel 8Mbit device.

The serial flash uses V_3S power supply since it needs to be powered off when the processor is off.

2kb Mode Bit ROM

Crusoe processors use a 2-wire serial interface to download the Configuration Mode bits from this device at boot-up. The Configuration Mode bits instruct the CPU on several important boot and initialization options.

The contents of the mode-bit ROM are read into the processor at power-on, configuring the processor to begin execution with optimal performance timings over a large range of system operating configurations. Compensating for process variation device sensitivity for current TM5400/TM5600 processors requires the use of the external mode-bit ROM with a particular mode-bit parameter configuration that is slightly different than the default parameters hard-wired into the processors. Use of the external mode-bit ROM with the mode-bit parameters described in this document is required for guaranteed operation of all current TM5400/TM5600 production parts. For more information, see *Mode Bit ROM Settings* on page 40.

Currently, the only approved part for use as a Config Mode bit SROM is Microchip Semiconductors' 93LC56B 128x16 2kb serial flash ROM.

This device is powered from V_3S.

Write-Protect PLD addition to CMS Serial Flash ROM

A 22LV10 PLD is added to intercept the SROM_CS[1:0]# signals to the serial Flash SROM device(s). The PLD intercepts write cycles to the device when writes are not authorized (controlled by a GPIO pin from the south bridge chip). This addition is required for all systems using serial Flash ROM for CMS storage; systems using the parallel ROM for CMS storage do not require a PLD. For more information, see *Serial Flash Write Protection Circuit* on page 31.

Core Temperature Sensor

This device connects to the DIODE_CATHODE and DIODE_ANODE pins of the processor. The temperature sensor should be I2C compatible to connect to south bridge SMBUS or similar. Also, connect temp sensor ALERT# signal to south bridge.

See the Reference Schematics for example device and circuit.

This device is powered from V_3S.

TDM Debug Connection

The Transmeta Debug Module (TDM) communicates to the target through two, high density Flex cables; TDCA (30pin) and TDCB (options 24pin user connection). The TDCA is shown with it's connections to the core system. See the TDM spec for more information on TDCB or see the Reference Schematics for an example of how TDCA connects and how TDCB can be used.

The TDM and the debug connection is used for:

- Flashing CMS ROM
- Flash Mode Bit ROM
- Connecting the Transmeta ICE
- Debugging

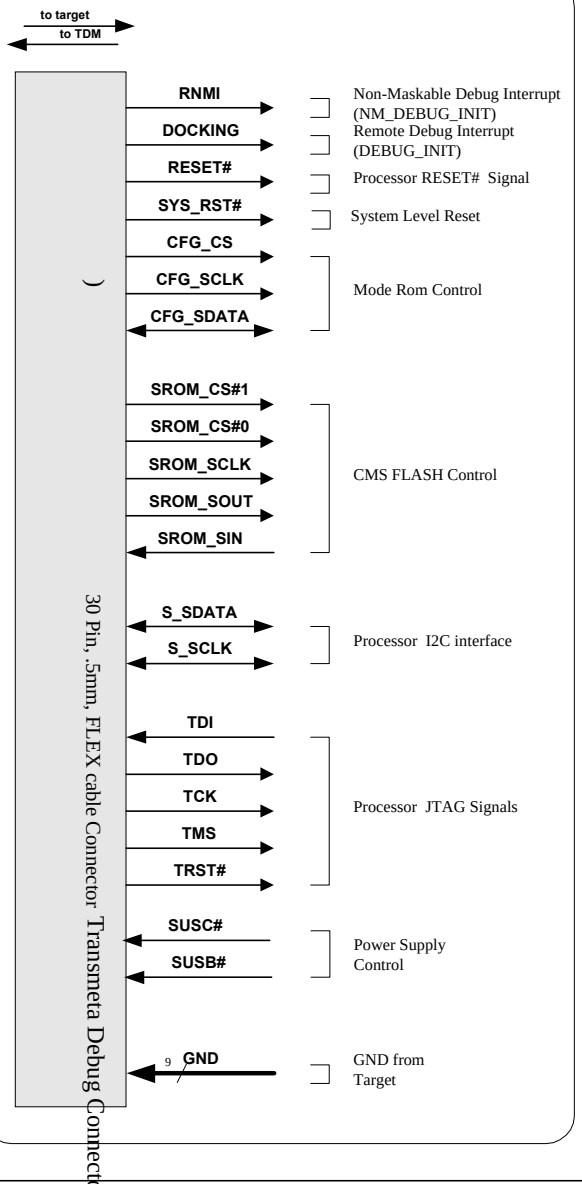
See diagram below for pinout and signal descriptions.

FIGURE 2 Transmeta Debug Connector A

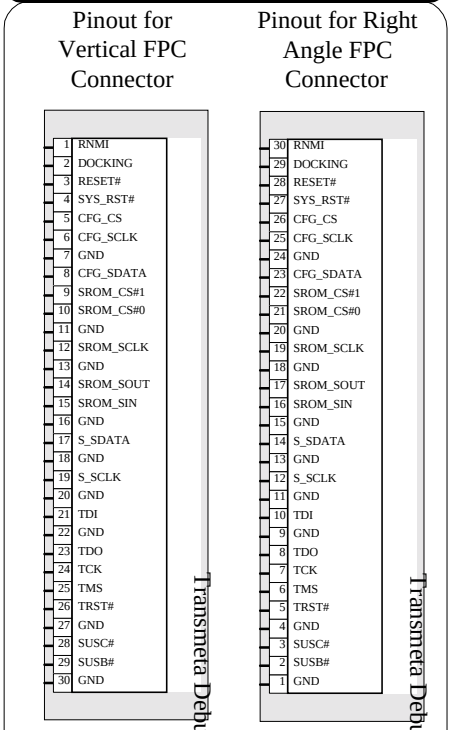
Transmeta Debug Connector A

The TDC-A is a 30-pin, .5mm flex cable connector that has all vital signals to debug the TM processor (CMS Flash control, Mode ROM Control, I2C, RNMI, Docking, RESET#, and JTAG signal) If additional debug control is needed for specific designs, the optional TDC-B may be used.

TDC-A Functional Description



TDC-A Pinout



Right Angle part number (molex)

0.5mm,FPC,Right Angle,SMT,ZIF,Top Contact
30 contact - 52435-3091
http://www.molex.com/product/ffc/52745.html

Vertical style part number (molex)

0.5mm,FPC,Vertical,SMT,ZIF
30 contact - 52559-3092
http://www.molex.com/product/ffc/52559.html

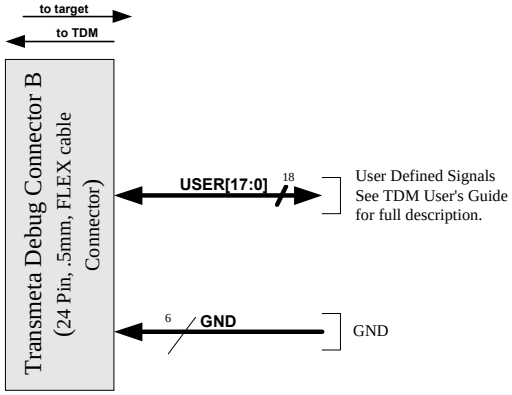
FIGURE 3 Transmeta Debug Connector B

Transmeta Debug Connector B

The TDC-B is a 24 pin, .5mm flex cable/connector that supplies 18 user defined control bits to be used for debug of a design. Each pin is configurable as either an input or output and can be open-drain or tristate type. The generic pin assignments are given below as well as an example pinout used in the Transmeta Processor Core Reference Design.

Note : connector pinouts are dependent upon the type of connector used (vertical or right angle)

TDC-B Functional Description



Right Angle part number (molex)

0.5mm,FPC,Right Angle,SMT,ZIF,Top Contact
24 contact - 52435-2491
http://www.molex.com/product/ffc/52745.html

Vertical style part number (molex)

0.5mm,FPC,Vertical,SMT,ZIF
24 contact - 52559-2492
http://www.molex.com/product/ffc/52559.html

TDC-B General Pinout

General Pinout for TDC-B (vertical connector)

1	GND
2	USER0
3	USER1
4	USER2
5	GND
6	USER3
7	USER4
8	USER5
9	GND
10	USER6
11	USER7
12	USER8
13	GND
14	USER9
15	USER10
16	USER11
17	GND
18	USER12
19	USER13
20	USER14
21	GND
22	USER15
23	USER16
24	USER17

Transmeta Debug Connector B (vertical connector - general pinout)

General Pinout for TDC-B (right angle connector)

24	GND
23	USER0
22	USER1
21	USER2
20	GND
19	USER3
18	USER4
17	USER5
16	GND
15	USER6
14	USER7
13	USER8
12	GND
11	USER9
10	USER10
9	USER11
8	GND
7	USER12
6	USER13
5	USER14
4	GND
3	USER15
2	USER16
1	USER17

Transmeta Debug Connector B (right angle connector - general pinout)

TDC-B Reference Design Pinout

See System Design Guide and Reference Schematics for more detail.

Reference Design Pinout (vertical connector)

1	GND
2	STR_WAKEUP#
3	TEMP INTCPT
4	CLK_GEN FREQ SEL
5	GND
6	USER3
7	CPU_VDD_SEL 4
8	CPU_VDD_SEL 3
9	GND
10	CPU_VDD_SEL 2
11	CPU_VDD_SEL 1
12	CPU_VDD_SEL 0
13	GND
14	DIS_CPU_VDD_SEL
15	USER10
16	USER11
17	GND
18	USER12
19	USER13
20	USER14
21	GND
22	USER15
23	USER16
24	USER17

Transmeta Debug Connector B (Reference Design - vertical connector)

Reference Design Pinout (right angle connector)

24	GND
23	STR_WAKEUP#
22	TEMP INTCPT
21	CLK_GEN FREQ SEL
20	GND
19	USER3
18	CPU_VDD_SEL 4
17	CPU_VDD_SEL 3
16	GND
15	CPU_VDD_SEL 2
14	CPU_VDD_SEL 1
13	CPU_VDD_SEL 0
12	GND
11	DIS_CPU_VDD_SEL
10	USER10
9	USER11
8	GND
7	USER12
6	USER13
5	USER14
4	GND
3	USER15
2	USER16
1	USER17

Transmeta Debug Connector B (Reference Design - right angle connector)

1.2.4 Clocking

The processor expects a primary clock input called HCLK, at either 60MHz or 66MHz, compatible with Pentium™ class clock generators. From this clock, the processor generates the CPU clock and the SDRAM clocks. The processor also expects a PCI clock input of HCLK/2. The phase relationship between the CPU and PCI clocks should be such that the CPU_CLK leads the PCI_CLK by 3.3ns (typical).

Note, make sure that the PCI_CLK which is connected to the processor is not 'always on' (PCICLK_F) but is controllable by power states.

HCLK and PCI_CLK PC board trace lengths to the processor should be matched. Also, PCI_CLK traces to PCI slots and devices should also be matched with each other as well as HCLK and PCI_CLK to the processor. In other words, HCLK and PCI_CLK to the processor should be the same length as all the traces to each PCI device/slot.

The processor generates the clocks for both DRAM interfaces.

See the Reference Schematics for a clock chip example where the TDCB connects to it to allow the debugger to control system frequency.

1.2.5 Using BIOS ROM for CMS storage

The TM5400/TM5600 supports using the BIOS parallel ROM memory for CMS storage, thus eliminating the need for a 1MB serial Flash ROM to store CMS.

This is accomplished by connecting the Crusoe EPROMA[2:1] signals up to the highest order address bits of a 2MB parallel Flash which is the usual way for BIOS (xbus or similar). CMS is stored in the lower ¾ of the ROM and the upper ¼ is used for the BIOS. The TM5400/TM5600 controls the EPROMA[2:1] during the CMS decompression phase and then sets EPROMA[2:1] to 11b to enable access to the x86 BIOS code.

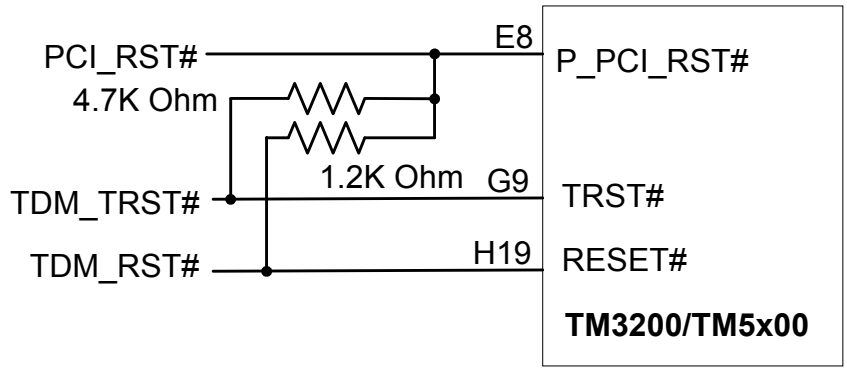
One problem with using a parallel ROM for CMS is that JEDEC Flash ROMs have an 'erase all' command which erases all unprotected sectors in the ROM. To protect against this, the CMS sectors of the ROM should be protected, and the use of the un-protection circuit shown in the Reference Schematics will allow the CMS upgrade utility to unprotect CMS sectors during upgrades. This circuit is only available on the TM5400/TM5600. When using parallel flash in a TM3200 system, the lower ½ of the ROM should be protected. This will not allow for field upgrades to protected sectors but it will protect CMS from being erased in the event of an 'erase all' command.

Future versions of parallel ROMs may allow the 'erase all' feature to be disabled and some may also support software programmable protection of sectors. These enhancements may do away with the need for this protection circuit. For debugging purposes, retain the serial flash connections to the TDM (Transmeta Debug Module) connection. The TDM has serial flash and allows developers to boot from it.

1.2.6 System Reset

The processor requires the reset connections shown in Figure 4 for proper operation. This allows the TDM to assert JTAG reset and RESET# (needed for some debugging functions) without asserting PCI_RST#. A system level PCI reset will also assert TRST# and RESET# which is needed for normal operation.

FIGURE 4 System Reset



Chapter 2

Design Considerations

2.1 Important Processor Considerations

- If the CD DDR port is not used, IOVDD25 *must* still be connected to 2.5V. In this case, the supply must produce 200mA at 2.5V minimum.

- TM5400/TM5600 C_VREF pin for the CD DDR interface requires an IOVDD25/2 (1.25V) reference at this pin. A 4.99k/4.99k resistor divider from V_25S with a 0.01uF filter cap is recommended.

- Special Considerations for VDDCORE supply:

  When using the MAX1711 as supply for VDDCORE and Longrun is used, a quickswitch as shown in the reference schematics must be used to protect the TM5400/TM5600 VRDA[] pins during power down states. Also, use 1k pull-ups to switched 3.3V supply to provide fast edge rates needed by the MAX1711. Put a 1ms RC filter on POWERGOOD output of MAX1711 since it has a bug which causes POWERGOOD to be asserted during valid transitions of VRDA[] signals (see reference schematics).

  When using the LTC1736, connect VIDvcc to switched 3.3V supply. No external pull-ups on VID[] inputs or quickswitches are needed. Also, put a 1ms RC filter on POWERGOOD output since it negates for short pulses during transitions of VRDA[] signals (see reference schematics).

- Using Linear LTC1736 regulator for VDDCORE:

  The LTC1736 from Linear Technologies can be used as a VDDCORE supply for TM3200 and TM5400/TM5600 systems. When using TM3200 and TM5400/TM5600 (without LongRun), bootstrap the VID[] inputs to the desired voltage. For TM5400/TM5600 systems with Longrun, connect TM5400/TM5600 VRDA[] outputs directly to VID[] inputs of the LTC1736. Connect LTC1736 VIDVCC pin to switched 3.3V. Longrun will operate correctly with no external pull-ups on the VRDA[] lines. There are internal 40k pull-ups on the VID[] inputs that are connected to the VIDVCC pin. This allows direct connection to the 3.3v tolerant VRDA[] signals.

  A 1ms RC filter is required on the POWERGOOD output to filter short pulsed negations caused by VRDA[] transitions. See Reference Schematics for example circuit.

- JTAG TRST# should be connected to P_PCI_RST# through a 4.7k ohm resistor. When P_PCI_RST# is asserted, so will the JTAG interface. The resistor allows a JTAG reset from the TDCA

without resetting the chip and the PCI bus. If the debugger is not to be used, simply ground TRST# instead of tying it to P_PCI_RST#.

- All reserved pins should be pulled-up/down as shown in the Reference Schematics.
- DI port S_CLKIN and S_CLKOUT should be connected together through a 33 ohm resistor at the source (CLKOUT) and the remaining trace should have a calculated length equal to the average of all the data line trace lengths.
- PLL_VDD should be connected to VDD_CORE through a 4.7ohm resistor and filtered with a 0.1uF ceramic cap.
- If using TDCA debug connector, connect TDCA RESET# directly to the processor's RESET# and also to P_PCI_RST# through a 1.2k ohm resistor. This allows the TDM to override the PCI reset signal and issue a processor reset. Otherwise, connect P_PCI_RST# directly to RESET#.
- In general, TDM connections to serial ROM devices will require a resistor in between the processor signal and the ROM device to allow the TDM to override the active signal. See reference schematics.
- No x32 bit memory devices are supported on either the DI or the CD SDRAM interface.
- The following signals should be pulled up to 2.5V: IGNNE#, INTR, INIT#, NMI, and SMI, as well as FERR# on the TM5400/TM5600 only (it's an output on TM3200 but open drain on TM5400/TM5600)). See the Reference Schematics.
- HCLK and PCI_CLK PC board trace lengths to the processor should be matched. Also, PCI_CLK traces to PCI slots and devices should also be matched with each other as well as HCLK and PCI_CLK to the processor. In other words, HCLK and PCI_CLK to the processor should be the same length as all the traces to each PCI device/slot.

  Make sure the 'always on' PCI_CLK (PCICLK_F) from the clock controller is not supplied to the processor if you are running CMS 4.1.3 or earlier. If you are running CMS 4.1.4 or later and are experiencing a PCI bus hang when using CLKRUN with Serial IRQ, see *Errata: Potential PCI Bus Controller Hang When Utilizing CLKRUN and Serial IRQ*.

NOTE A 22LV10 PLD is added to intercept the TM5400/TM3200 SROM_CS[1:0]# signals to the serial Flash SROM device(s). The PLD intercepts write cycles to the device when writes are not authorized (controlled by a GPIO pin from the south bridge chip). This addition is required for all systems using serial Flash ROM for CMS storage; systems using the parallel ROM for CMS storage do not require a PLD.

2.2 Important Power Management Issues

This section contains important design info regarding Crusoe design requirements regarding power management and processor power supplies. These are several details of the processor specification that might be overlooked and should be given strict attention.

- All power supplies to the processor must switch up or down within 25ms of each other, as follows: IOVDD, IOVDD25, and PLLVDD should be valid within 10ms of each other. IOVDD and IOVDD25 should be valid 10ms prior to VDDCORE coming out of soft-start (this differs for MAX1711 and LT1737 (variable)) or before the VCORE voltage reaches .7V.

- All power supplies to the processor must be powered on at all times. No supplies may be switched off independent of the others (3.3V, 2.5V, and core).

- During deep sleep power management state (the processor clock is stopped and most I/O pins are tri-stated; see specification). This means that care must be taken to ensure that all signals going to sections of the system that are powered on during suspend must be pulled up/down to a valid state when the processor tri-states its outputs.

  Specifically, P_GNT[] and other PCI control signals are the most important examples.

- All signals connected to the processor must be powered off, grounded, or disconnected during power down states in which all power is removed. Voltage cannot be applied to the processor when power supplies are off.

- Core power supply must be designed to accommodate rapid large transitions in current when switching in and out of power management modes.

2.3 DI PCB Layout Guidelines

Use series source termination scheme in layout of DI memory. In series source termination, place source termination resistor as close to the driver (source) as possible. The sum of the driver impedance and the source termination resistance should match the PCB line impedance.

TM5400 DI PC Board Layout Guidelines:

- Use 22 ohm source termination resistors on DI data lines

- Use 10 ohm termination resistors on DI address and control signals

- PCB trace impedance should be 60 ohms on all DI signals

- A nominal DI layout is based on the total trace length of any DI signal (data/addr/control/clk). Total trace length is calculated as the sum of all trace stubs.

  - for 16 loads: max total trace length must be <= 5"
  - for 12 or fewer loads: max total trace length must be <= 8"

  The DI layout is considered sub-nominal or conservative if:

  - for 16 loads: max trace lenght is > 5"

- for 12 or fewer loads: max trace length is > 8"

2.4 TM5400/TM5600 LongRun™ Design Considerations

LongRun controls the processor voltage and frequency dynamically to adjust to the needs of applications.

In order to support LongRun™ Technology, the VRDA pins of the TM5400/TM5600 must be connected to the VCORE power supply voltage control inputs (MAX1711 or similar power supply). LongRun dynamically adjusts CPU frequency and voltage to conserve power. In order to do this, the TM5400/ TM5600 VRDA[4:0] signals must be connected to the VDDCORE supply regulator (see below).

TM3200 Reserved pins shown in Table 2 connect to MAX1711 voltage select inputs D[0:4] (VRDA0->D0,. VRDA1->D1, etc).

TABLE 2 TM3200 to TM5400/TM5600 VRDA Pins

Pin #	TM3200 Name	TM5400/TM5600 Name
Y12	Reserved_(Y12)	VRDA[0]
Y13	Reserved_(Y13)	VRDA[1]
V14	Reserved_(V14)	VRDA[2]
W14	Reserved_(W14)	VRDA[3]
W13	Reserved_(W13)	VRDA[4]

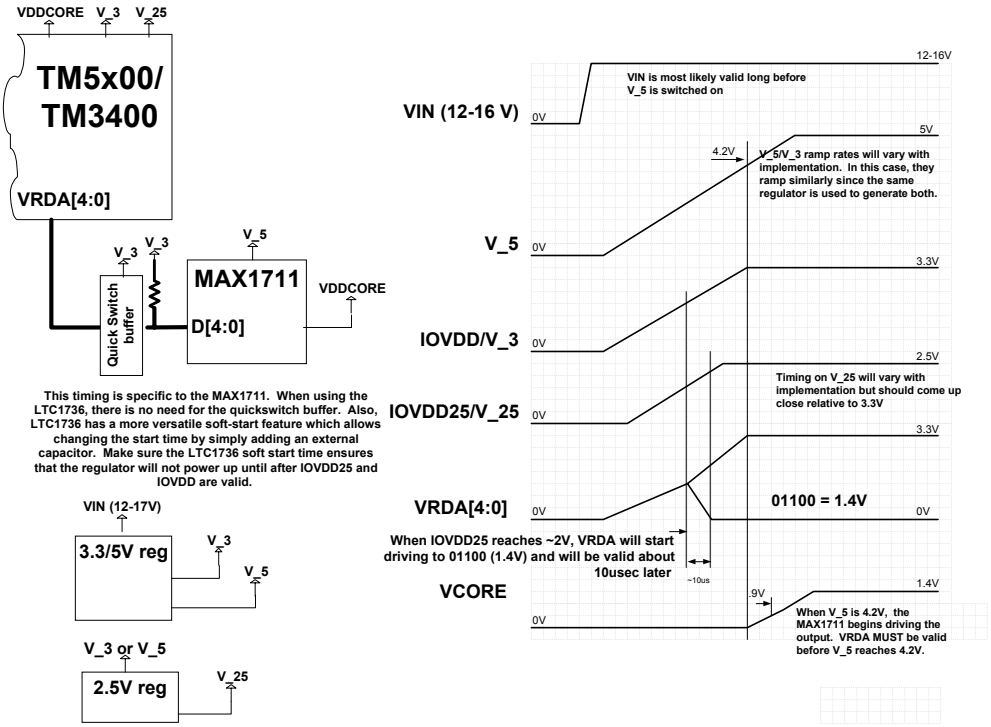
The VRDA outputs are open-drain. These are pulled up to V_3S with 1k ohm resistors.

2.4.1 About LongRun™ Technology

Voltage is controlled via the VRDA[4:0] outputs to the VDDCORE power supply. A quickswitch is needed to protect the VRDA pins from the 5V pull-ups inside the MAX1711 (or similar) power supply. Also, the MAX1711 requires that the VREF inputs be changed within 100ns (see specification) of each other.

NOTE Since the VRDA outputs are open-drain, 1k ohm pull-ups on these signals must be used to ensure that all VRDA signals will switch quickly enough with respect to one another.

FIGURE 5 TM5400/TM5600 VRDA Connection and Timing Diagram for LongRun™



2.4.2 LongRun Power Supply

The VDDCORE regulator must support dynamic voltage adjustment through VSET[] inputs. The Maxim MAX1711 and Linear Tech LTC1736 both support this.

MAX1711

When using the MAX1711, connect the MAX1711 D[4:0] inputs through a quickswitch (see Reference Schematics). The D[] inputs have internal 5V pull-ups and the VRDA[] signals are only 3.3V tolerant. In addition, the internal pull-ups are too weak to support the transition speeds required on the D[] inputs from the open-drain VRDA[] signals. This, combined with the fact that the VRDA[] signals are only 3.3V tolerant, requires 1k pull-ups to switched 3.3V on each of the VRDA[] lines (on the MAX1711 side of the quickswitch).

Another important note when using the MAX1711: add a 1ms RC filter directly on the output of the POWERGOOD pin. This is required since the POWERGOOD signal negates for short durations during VRDA[] transitions. The POWERGOOD negation lasts for approximately 2-6us so a 1ms RC is a conservative filter value given current data but MAXIM is investigating this issue to determine the maximum possible assertion within the Longrun use scenario.

LTC1736

The LTC1736 also has internal pull-ups on the VID[] inputs. This part works well with only these pull-ups. The internal pull-ups connect to the VIDVCC pin which.allows the designer to decide on the pull-up voltage. In this case, connect it to switched 3.3V. This allows the VID[] inputs to be connected directly to the TM5400/TM5600 VRDA[] outputs.

Also, add a 1ms RC filter directly on the output of the POWERGOOD pin. This is required since the POWERGOOD signal negates for short durations during VRDA[] transitions. Current data show that the POWERGOOD negation lasts for approximately 2-6us so a 1ms should be sufficient to filter any pulses. The design is under investigation to fortify the value of the RC needed.

2.4.3 VDDCORE Supply Transition Rates and LongRun

LongRun is continuously ramping VDDCORE up and down, along with the frequency. During an upward transition, for example, from 1.4V 400Mhz to 1.55 533Mhz, Longrun ramps the VCORE voltage to 1.55 slowly. Slow step by step transitions are made to try to prevent POWERGOOD negations by the regulator (currently, this is not 100% successful which is why the RC filter is required). LongRun changes VCORE one step at a time until it reaches the target. The time between each change is programmed in the OEM_CONFIG Table. Once it's there, it changes the frequency to 533Mhz (voltage must be changed first since the CPU won't work at 533Mhz, 1.4V). The OEM_CONFIG table value for upward transitions should be greater than the slowest slew rate of the regulator. The regulator design should take this into account to try to achieve fast slew rates.

A downward transition is similar but the VDDCORE bulk capacitance comes into play. A transition from 1.55 533Mhz to 1.4 400Mhz happens in reverse. First, the frequency is changed from 533Mhz to 400Mhz. Then, Longrun controls the VRDA[] outputs to step down to 1.4V. The VDDCORE bulk capacitance will store energy at each voltage step and must bleed off between each step. The bleed time is also a function of load, which is a function of frequency and voltage. This makes it more complex since the capacitors will settle faster at higher frequencies. The TM5400/TM5600 can't monitor VDDCORE and must rely on the value in the OEM_CONFIG table to determine the time between each transition (transition times are independently programmable for up and downward transitions). Work is currently being done to develop clear settings for the OEM_CONFIG fields as well as the recommended amount of bulk capacitance on VDDCORE.

2.4.4 CVDD Rise and Fall Times

Note that there is no specification on how fast CVDD must rise or fall, but the design provides sufficiently small durations as long as the VCORE regulator is designed following the schematics in this document. Rise time is controlled by the frequency of the regulator as well as the capacitance and the inductor size, and fall time is almost completely due to output capacitance.

2.5 Thermal Design Considerations

See Chapter 4, *Thermal Design Considerations* for thermal design information.

2.6 South Bridge Recommendation

To date, Crusoe processors have been successfully tested with the Intel PIIX4 and Acer ALI M1535 southbridges. The reference schematics show how the PIIX4 and the M1535 connect to the TM5400/ TM5600.

2.7 Power Planes and Power Supply Decoupling

NOTE To achieve the frequencies specified in the TM5400/TM5600 Specifications, the power supplies must deliver voltages within the specified margins (+/- 5%). Strict attention must be given to decoupling and power and ground plane layout as discussed in this document in order to achieve this.

- VDDCORE: Use 8 x.1uf 0603 X7R ceramic caps directly under the TM5400/TM5600. 20 x 1uF 1206/0805 X7R ceramic caps surrounding the chip. 6 x 220uF low ESR (100m ohm or less) cap as bulk capacitance as close to the chip as possible.

- VDD_IO: Use 14 x 1uF X7R 1206/0805 ceramic caps as close to the chip as possible. Use 2 x 22uF low ESR caps for bulk.

  VDD_25: 8 x 1uF X7R 1206/0805 ceramic caps as close to the chip as possible. 1 x 22uF tantalum low ESR cap for bulk capacitance.

2.8 Serial Flash Write Protection Circuit

Transmeta's Systems Engineering organization has determined that there is a potential risk for serial flash ROM devices to be inadvertently erased or modified in-system affecting the CMS control program stored in the serial flash ROM. This technical bulletin describes a write protection circuit that controls write accesses to the serial flash ROM device containing the CMS control program.

2.8.1 Overview

The serial flash ROM devices available today do not provide a secure mechanism to protect the serial flash ROM from accidental erasure or accidental writes. The handshake mechanism commonly available in parallel flash ROM devices to guard against accidental erasure or writes is not utilized on serial flash ROM devices. Therefore, to ensure a high level of system security and integrity, Transmeta requires a special write protection circuit to provide a more thorough mechanism for write protecting the serial flash ROM that stores the CMS memory image.

The purpose of the write protection circuit is to:

- provide security
- fully write protect the entire serial flash device
- ensure that the CMS control program is not accidentally overwritten
- allow for field upgrades of CMS should it be needed

2.8.2 Serial Flash Write Protection Circuitry

The write protection PLD works by gating the chip select signal to the serial ROM when a write or erase command is detected. The device has an input pin (named WP) to enable and disable this feature. When WP is asserted, write and erase commands are not allowed to complete. When WP is negated, write and erase commands function normally. Read commands are always unaffected by the PLD.

The polarity of the WP input is selectable with another input pin (named WPNEG). When WPNEG is pulled up, the WP input is active-low. When WPNEG is pulled down, the WP input is active-high. WPNEG should be pulled up if the signal driving the WP input powers up in the low state. WPNEG should be pulled down if the signal powers up in the high state.

The PLD also has an input pin (named SEL) to select the type of serial ROM in use. The SEL pin should be pulled up for Macronix flash, and it should be pulled down for Atmel flash.

Customers should consider the following when selecting a PLD device to implement the write protection circuit:

- **Package**. The state machine in the PLD design is very simple, and it could fit into a very small device. However, an asynchronous flip-flop reset is absolutely necessary for this PLD design to function, and the smallest PLD with that feature is a 22LV10. For tightly constrained board layouts, Atmel makes a 22LV10 in a 24-pin TSSOP. Their part number is ATF22LV10C, and their pinout and fuse map are the same as in a standard DIP 22LV10.
- **Propagation delay**. Transmeta successfully tested a part with a 15 ns propagation delay. Although a slower part may work, Transmeta can not guarantee it because a slower part was not tested.
- **Voltage**. The PLD must have 3.3V outputs because the serial ROM is not 5V-tolerant.

- **Power**. Many vendors sell 22LV10 parts with power saving features. Although Transmeta did not test such a part, customers should consider using a lower power device. The standard 22LV10 draws at least 70 to 90 mA from 3.3V.

2.8.3 Schematic Diagram of the PLD in a System

2.8.4 Pinout

DIP Pin	PLCC Pin	Name	Description
24	28	3.3V	Power
12	14	GND	Ground
1	2	CKIN	Serial flash clock input.
3	4	DIN	Serial flash data input.
4	5	WP	Write protect input.
7	9	WPNEG	Write protect negate input: Low = WP is active-high High = WP is active-low
8	10	SEL	Select serial flash interface (input): Low = Atmel High = Macronix
5	6	CS0IN#	Serial flash 0 chip select input.
6	7	CS1IN#	Serial flash 1 chip select input. Tie high if unused.
17	20	CS0OUT#	Serial flash 0 chip select output.
23	27	CS1OUT#	Serial flash 1 chip select output. No connect if unused.
9, 10, 11, 13, 14, 15, 16, 20, 21, 22	11, 12, 13, 16, 17, 18, 19, 24, 25, 26	Unused	Unused inputs and tri-stated outputs that should be tied to ground

2.8.5 JEDEC Fuse Map

The following text is the JEDEC file representing the fuse map for the write protection PLD. It was produced by the CUPL PLD design compiler for a 24-pin DIP package. To use it with a 28-pin PLCC package, simply change the line "*QP24" to "*QP28". The fuse maps are the same for the DIP and PLCC packages.

```
CUPL(WM)        5.0a  Serial# 10000000
Device          g22v10  Library DLIB-h-40-2
Created         Tue May 23 00:50:17 2000
Name            wr_prot
Partno          0
Revision        2
Date            5/23/00
Designer        Transmeta
Company         Transmeta
Assembly        1
Location        1
*QP24
*QF5892
*G0
*F0
*L00000 11111111111111110111011111111111
*L00032 11111111111111111111111111111111
*L00064 11111111111111111111111111111111
*L00096 11111111110110111111111111111111
*L00128 11111111111111111111111110101111
*L00160 11111111111111111111111111111011
*L00192 11111011101111111111111111111111
*L00224 11111111011111111011011111111111
*L00256 11111111000000000000000000000000
*L02144 00000000000011111111111111111111
*L02176 11111111111111111111111111111111
*L02208 11111111111011011111111111111111
*L02240 11111111111101111111110111011111
*L02272 11111111111111111111111101111111
*L02304 11101110111111111111111111110000
*L02880 00000000000000000000000011111111
*L02912 11111111111111111111111111111111
*L02944 11111111111110111111110111011111
*L02976 11111111111111111111111111111111
*L03008 11011110111111111111111111111111
*L03040 11110111111111011101111101111111
*L03072 11111111111111111011111111101110
*L03104 11111111111111111111000000000000
*L03648 00001111111111111111111111111111
*L03680 11111111111111111111111111111111
*L03712 10011111111111111111111111111111
*L03744 11111111111110111111011111111111
*L03776 11111111111111111111101110111111
*L03808 10111111111111111111111111111111
*L03840 01111011111101111111111111111111
*L05792 00000000000000000100000010100100
*L05824 00000011000000000000000000000000
```

```
*C6A76
*4926
```

2.8.6 CUPL Source Code

```
Name     wr_prot;
PartNo   0;
Date     5/23/00;
Revision 2;
Designer Transmeta;
Company  Transmeta;
Assembly 1;
Location 1;
Format   j;          /* Use JEDEC output format */
Device   G22V10LCC;  /* This is the code for a 28-pin PLCC package. */
                     /* Other packages require different pin */
                     /* assignments.  The code for a 24-pin DIP is */
                     /* G22V10. */

/*****************************************************************
 * This device protects against writes and erases to the serial flash
 * when the WP pin is asserted.  It works by forcing the chip select
 * to negate when a write or erase command is detected.  The WPNEG
 * pin causes the WP input to be inverted in case WP is active-low on
 * the circuit board.  Two chip selects are handled for the case of
 * two half-size serial ROMs.
 *
 * A select input pin is used to choose between Atmel and Macronix.
 * The reason this is needed is the opcodes between the two parts are
 * similar enough to require detection of all 8 bits of the opcode.
 * If the chip select is negated after the 8th bit of the opcode, the
 * flash device will execute the command with bogus address and data.
 * The select input allows write or erase opcodes to be detected in as
 * few as two bits.
 *
 * This design file is written for the CUPL programmable logic
 * compiler.  A free, functional, demo version of the compiler is
 * available from http://www.logicaldevices.com/.
  *****************************************************************/

/*
 *  Input pins
 *
 *  All unused inputs should be tied high or low on the circuit board.
 *  Active-low pins are denoted by the ! prefix.  After the input and
 *  output sections of this file, all syntax refers to the logical
 *  level of a pin and not its physical level.
 */
PIN  2 =  CKIN;    /* (DIP pin 1) Serial flash clock */
PIN  4 =  DIN;     /* (DIP pin 3) Serial flash data input */
PIN  5 =  WP;      /* (DIP pin 4) Write protect */
PIN  9 =  WPNEG;   /* (DIP pin 7) Write protect negate: */
```

```
                    /*              Tie low  if WP is active-high */
                    /*              Tie high if WP is active-low */
PIN 10 =  SEL;      /* (DIP pin 8) Select type of flash: */
                    /*              High = Macronix */
                    /*              Low  = Atmel */
PIN  6 = !CS0IN;    /* (DIP pin 5) Intercepted serial flash chip */
PIN  7 = !CS1IN;    /* (DIP pin 6)   selects.  If one is unused, it */
                    /*              should be tied high. */

/*
 *  Output pins
 */
PIN [21,23] = [Q0..1];   /* (DIP pins 18..19) Flip-flops for the */
                         /*                       state machine */
PIN 20      = !CS0OUT;   /* (DIP pin 17) New serial flash */
PIN 27      = !CS1OUT;   /* (DIP pin 23)   chip selects */

/*
 *  Assign asynchronous reset (AR) controls on all flip-flops
 *
 *  When both chip selects are negated, the state machine needs to
 *  reset to the BIT7 state.  Otherwise, it will never know when bit 7
 *  of the opcode occurs.
 */
Q0.AR = !CS0IN & !CS1IN;
Q1.AR = !CS0IN & !CS1IN;

/*
 *  Assign synchronous preset (SP) and output enable (OE) controls on
 *  all flip flops
 */
Q0.SP = 'b'0;
Q1.SP = 'b'0;
Q0.OE = 'b'1;
Q1.OE = 'b'1;

/*
 *  State names and numbers
 *
 *  To guard against output glitches, the state numbers are assigned so
 *  that most transitions only change one flip-flop.
 */
$DEFINE BIT7         'b'00
$DEFINE BIT6         'b'11
$DEFINE PAT_MATCH    'b'10
$DEFINE NO_PAT_MATCH 'b'01

/*
 *  State transitions
 *
 *  The write or erase opcodes used by Crusoe are:
 *    Macronix:
 *      F2h    Page Program
 *      F1h    Sector Erase
```

```
 *    Atmel:
 *      82h    Direct Program through Buffer
 *  The read opcodes used by Crusoe are:
 *    Macronix:
 *      83h    Read Status
 *      52h    Read Array
 *    Atmel:
 *      57h    Read Status
 *      52h    Main Memory Page Read
 */
SEQUENCE [Q1..0]
{
  PRESENT BIT7
    IF !DIN        NEXT NO_PAT_MATCH;  /* No write or erase opcode */
                                       /*   has bit 7=0 */
    IF  DIN & !SEL NEXT PAT_MATCH;     /* For Atmel, bit 7=1 means a */
                                       /*   write or erase */
    IF  DIN &  SEL NEXT BIT6;          /* For Macronix, need to keep */
                                       /*   checking */
  PRESENT BIT6
    IF  DIN NEXT PAT_MATCH;            /* Must be F1h or F2h */
    IF !DIN NEXT NO_PAT_MATCH;         /* Can't be F1h or F2h */
  PRESENT PAT_MATCH
    NEXT PAT_MATCH;                    /* Only way out is reset */
  PRESENT NO_PAT_MATCH
    NEXT NO_PAT_MATCH;                 /* Only way out is reset */
}

/*
 *  Output equations
 *
 *  Each chip select is copied from input to output unless the current
 *  state is PAT_MATCH and the WP input is asserted.  In that case,
 *  both chip selects are negated.  If WPNEG is asserted, the sense of
 *  WP is reversed.
 *
 *  For the unusual case of WP being asserted after a write or erase
 *  opcode but before the end of the bus cycle, both chip selects will
 *  immediately negate.
 */
CS0OUT = CS0IN & !((WP $ WPNEG) & Q1 & !Q0);
CS1OUT = CS1IN & !((WP $ WPNEG) & Q1 & !Q0);
/*                     ^-- $ is the XOR operator in CUPL */
```

2.8.7 Software Support

In order to enable CMS upgrades, the WP pin needs to be controllable through software. By connecting it to a GPO somewhere in the system, the signal can be negated before a CMS upgrade starts and re-asserted after it finishes. No changes are needed to the upgrade software for this process to work because the init_cycles field is in the OEM configuration table, inside the serial ROM.

The init_cycles fields should be used to tell CMS what PCI bus cycles to generate in order to control the WP signal. Each field contains an `action` parameter that tells CMS when to execute that particular PCI bus cycle. When bit 1 of the action is set to 1, the bus cycle runs before a CMS upgrade starts. When bit 2 of the action is set to a 1, the bus cycle runs after a CMS upgrade finishes.

Once a GPO is selected to connect to the WP pin, the PCI bus cycles to negate and assert that GPO should be programmed into the init_cycles fields of the OEM configuration table. The init_cycles fields to negate WP should have bit 1 of the action set to a 1, and the init_cycles fields to assert WP should have bit 2 of the action set to a 1. The *Development and Manufacturing Guide* has more complete instructions on how to use the init_cycles fields.

It is important to note that the init_cycles fields cannot perform a read-modify-write function. That is, Boolean logic functions are not available to manipulate individual data bits within a byte. This implies that the byte controlling the GPO connected to WP must be in a known state when a CMS upgrade occurs. If that GPO control byte contains bits that could be either 0 or 1 during a CMS upgrade, and if changing those bits would have an undesirable effect on the system, then another GPO should be selected instead.

init_cycles Example

The following example shows how to set the init_cycles fields to control the WP pin of the write protection PLD. Please note that this example does not represent any actual system design. The numbers used were invented only for the purpose of illustration.

Example selection of GPO

- The GPO connected to WP is controlled by bit 5 at offset 0x42h in PCI device 4, function 1. Setting the bit to a 1 asserts WP.
- Before a CMS upgrade is performed, the value of the entire byte at offset 0x42 is observed to be 0xE9. This is important to know because only bit 5 should be changed, and the smallest quantity that can be written is the entire byte.
- The OEM config. table already has 6 entries (numbered 0 through 5) in the init_cycles table. In other words, the first available entry is number 6.

Example values for the corresponding init_cycles

- `init_cycles[6].addr = 0x00008140`

  The PCI device number is encoded by setting only one bit out of bits 31:11. Bit 15 is set because 11 + 4 = 15. Bits 10:8 contain the function number. Bits 7:2 are the offset of the 32-bit word containing the desired byte. Bits 1:0 are always zero.

- `init_cycles[6].cmd = 0x0B`

  This is the PCI command number for a configuration write.

- `init_cycles[6].be = 0x04`

Setting bit 2 of the PCI byte enable selects the desired byte within the 32-bit word addressed above.

- `init_cycles[6].data = 0x00C90000`

  The data byte written is the value previously observed at that location before a CMS upgrade, but bit 5 is cleared to 0. The data byte must be positioned in the 32-bit word as described by the byte enable field above.

- `init_cycles[6].action = 0x02`

  Setting bit 1 causes this bus cycle to execute immediately before a CMS upgrade starts.

- `init_cycles[7].addr = 0x00008140`

  The address on the bus cycle to re-assert WP is the same as on the bus cycle to negate it above.

- `init_cycles[7].cmd = 0x0B`

  This is the PCI command number for a configuration write.

- `init_cycles[7].be = 0x04`

  Setting bit 2 of the PCI byte enable selects the desired byte within the 32-bit word addressed above.

- `init_cycles[7].data = 0x00E90000`

  The data byte written is the same as init_cycles[6].data, but bit 5 is set to a 1.

- `init_cycles[7].action = 0x04`

  Setting bit 2 causes this bus cycle to execute immediately after a CMS upgrade finishes.

2.9 Mode Bit ROM Settings

2.9.1 Programming the Mode Bit ROM with WinTMM

The mode-bit ROM can be programmed using the Transmeta Debug Module (TDM) in conjunction with the Transmeta configuration software utility WinTMM. See the *TM5400/TM5600 Development and Manufacturing Guide* for information on the use of the WinTMM configuration utility with the TDM. Follow the instructions below to program the mode-bit ROM with the recommended start-up configuration parameters.

To read the current mode-bit ROM parameter settings using WinTMM, enter:

wintmm -D

WinTMM should display a mode-bit ROM parameter value table similar to that shown below. The mode-bit ROM field `DCT_CK_RISE`, highlighted below, is the parameter to be changed from a value of 1 to a value of 0.

```
IGNORED[3:0]      = 0  Ignored
BOOT_OPT[1:0]     = 1  modebits: SROM=01,10/default=00 (parallel boot),11
LT_SCLK_RISE[3:0] = 3  Load adjust for tag sense clock
LF_SCLK_RISE[3:0] = 8  Load adjust for Flook sense clock
CD_DIV[3:0]       = 4  CD Frequency = TM120 Frequency / CD_DIV
ICD_CK_RISE[3:0]  = 3  I cache data Sclk rise mode
IC_BYP_EN[0:0]    = 0  I cache Sclk bypass enable
ICT_CK_RISE[3:0]  = 1  I cache tag Sclk rise mode
ICT_CK_FALL[3:0]  = 0  I cache tag Sclk fall mode
DCD_CK_RISE[3:0]  = 3  D cache data Sclk rise mode
DC_BYP_EN[0:0]    = 0  D cache Sclk bypass enable
DCT_CK_RISE[3:0]  = 1  D cache tag Sclk rise mode  --> set to 0
DCT_CK_FALL[3:0]  = 0  D cache tag Sclk fall mode
KILL_CLKOUT[0:0]  = 1  Kill clkout pin
CK_STP_EN[4:0]    = 31 Clock Stop Enables (Core, PI, DI, CD, unused)
NO_CK_CTL[0:0]    = 0  No Clock Control
CLKIN_FREQ[1:0]   = 3  CLKIN Frequency (0=30, 1=60, 2=66, 3=33)
CD_FALL[0:0]      = 0  N/A (actually controlled by TM160 CSR)
IC_BOOT[0:0]      = 0  I-Cache boot
CK_MULT[4:0]      = 12 TM120 Frequency = CLKIN Frequency * CK_MULT
CP_MOMITR[1:0]    = 0  Control of loop resistor in the PLL
CP_RADJ[0:0]      = 0  Add phase delay to PLL reference path
CP_FADJ[0:0]      = 0  Add phase delay to PLL feedback path
IO_LO_V[0:0]      = 0  Adjust level converter bias on the voltage shifter
LA_SCLK_RISE[3:0] = 3  Load adjust for D-cache sense clock
DI_DIV[3:0]       = 4  DI Frequency = TM120 Frequency / DI_DIV
PLL_TRIM[1:0]     = 2  Main PLL current trim
NO_PLL_CHOP[0:0]  = 0  Don't chop main PLL
DIS_PLL_HYP[0:0]  = 0  Disable main PLL hyperactivity
HCLK_DIV[0:0]     = 1  HCLKIN input divide by 2
PCI_DIV[4:0]      = 12 PCI Frequency = TM120 Frequency / PCI_DIV
RESERVED2[0:0]    = 0  Reserved
CD_OLD_RST[0:0]   = 0  CD unit old reset
EPROMA[2:0]       = 1  EPROMA (EPROMA[0] = 1 -> Serial Flash boot)
SROM_TYPE[1:0]    = 3  SROM type (0=Mac., 2=0.5MB At., 3=1MB At.)
DI_OLD_RST[0:0]   = 0  DI unit old reset
DRV_PCI_PADS[0:0] = 0  Drive PCI pads during power management
CD_CONFIG[2:0]    = 0  CD SDRAM Configuration
HCLK_66MHZ[0:0]   = 1  PCI CLK is 33MHz
RESERVED3[1:0]    = 0  Reserved
PCI_SAFE_DLY[2:0] = 6  PCI_SAFE_DLY
RESERVED4[1:0]    = 0  Reserved
TLB_SENSE_CK[2:0] = 2  Tlb sense clk
RESERVED5[2:0]    = 0  Reserved
NO_DOZE[0:0]      = 0  Prevent IO drivers from going into 'DOZE' state
INSOMNIA[0:0]     = 0  Disables 'Sleep' mode
DI_FALL[0:0]      = 0  N/A (actually controlled by TM160 CSR)
```

To program the mode-bit ROM with the improved parameter settings, enter:

wintmm -S DCT_CK_RISE 0

2.9.2 Programming the Mode-Bit ROM with a Device Programmer

The mode-bit ROM can be programmed using standard serial flash ROM device programmers. Follow the instructions below and the procedures appropriate for the device programmer used to program the mode-bit flash ROM device.

The current default mode-bit ROM value (in hex) is:

Default mode-bit ROM value = e104200c0f61c0d8451ac1818030

Program the mode-bit ROM device with the following improved value (in hex):

Improved mode-bit ROM value = e104200c0f60c0d8451ac1818030

Chapter 3

PWB Layout

3.1 Very Important Layout Requirements

These items are required if the design is to meet specified operating frequencies.

- VDDCORE is placed on PWR/GND layer and bottom layer. If possible place a VDDCORE plane on as many layers as possible.
- GND 1, signal return path for traces on Signal 1 and 2. GND 1 Plane is to be solid, no breaks or cuts.
- GND 2, signal return path for traces on Signal 3 and 4 (6 and 5 for ten layer stack-ups). GND 2 Plane is to be solid, no breaks or cuts.
- Anti-Pad treatment for vias on GND 1, GND 2, PWR and PWR/GND layers. Pad diameter is to be smaller than the via hole. With .007" to .008" clearance from the via hole to the plane. This will result in .022" to .023" copper between vias under the CPU.

  NOTE: If normal anti-pad treatments were used, the amount of copper under the chip is severely decreased which limits processor performance.
- Prepreg material between PWR and PWR/GND layers should be .003" to .005".
- Signals run on Signal 3 (Inner Layer 5) are not to cross any cuts or breaks on the PWR/GND plane (Inner Layer 4)
- Non-critical signals to be placed on Signal 4 and Signal 3, Traces on Signal 4 are not to cross any cuts or breaks on PWR/GND layer.
- HCLK and PCI_CLK to the processor should have matched lengths. Also, each PCI device/slot clock should be matched to this same length.
- All vias on the pad side of the PCB CPU BGA footprint must be covered with soldermask. Failure to do so will potentially short signals together during the soldering process.

3.2 Layout Guidelines

- Keep trace lengths as short as possible.
- For improved manufacturing of the PWB, 6 mil traces and 6 mil spaces is recommend for the outer two layers (top and Bottom), with 5 mil traces and 5 mil spaces on the internal layers.
- No cutouts in the outer two ground planes.
- When routing signals between the inner signal layers, insert a ground via next to the signal via.

3.2.1 Recommended Eight Layer PWB Stackup

Signal	Layer	Material
Signal 1	Top	½ oz. copper
GND 1	Inner Layer 1	1 oz. copper
Signal 2	Inner Layer 2	½ oz. copper
PWR	Inner Layer 3	1 oz. copper
PWR/GND	Inner Layer 4	1 oz. copper
Signal 3	Inner Layer 5	½ oz. copper
GND 2	Inner Layer 6	1 oz. copper
Signal 4	Bottom	½ oz. copper

3.2.2 Recommended Ten Layer PWB Stackup

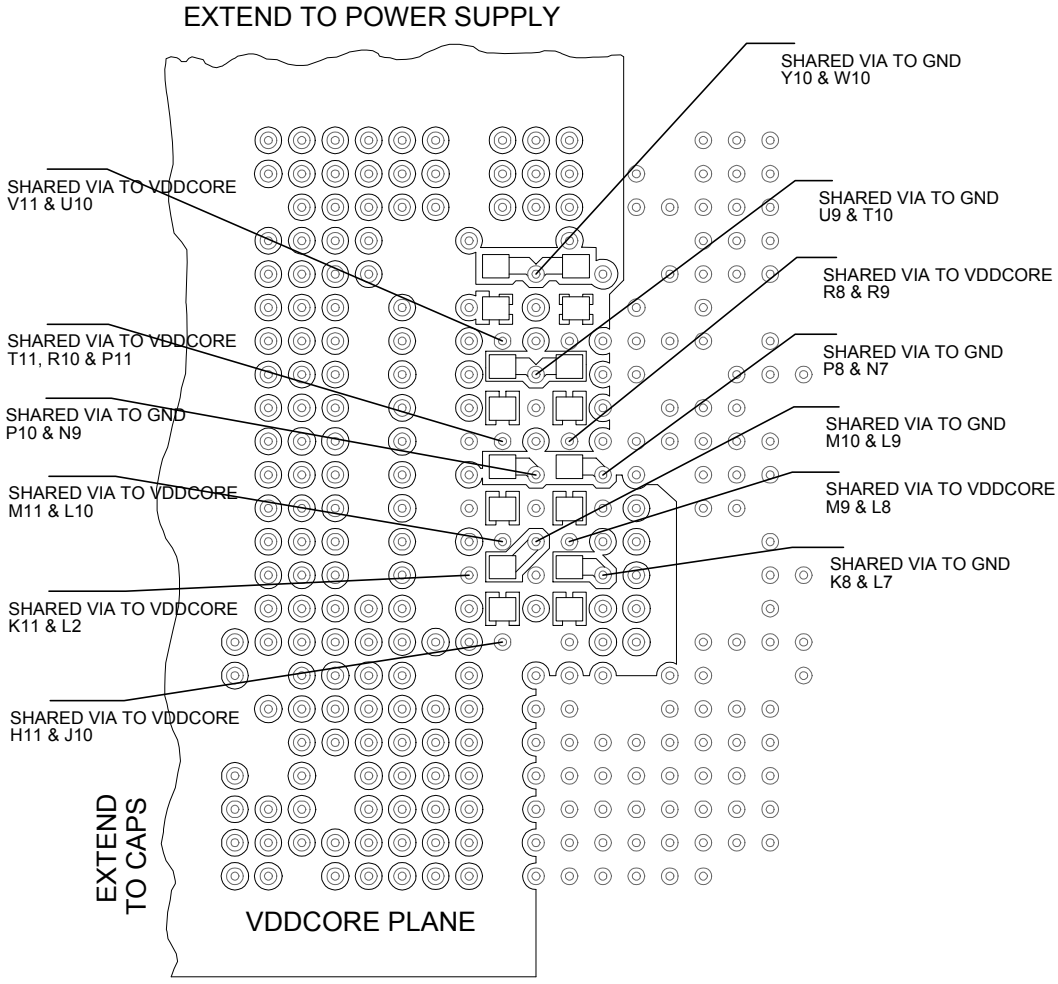
Signal	Layer	Material
Signal 1	Top	½ oz. copper
GND 1	Inner Layer 1	1 oz. copper
Signal 2	Inner Layer 2	½ oz. Copper
Signal 3	Inner Layer 3	½ oz. Copper
PWR	Inner Layer 4	1 oz. copper
PWR/GND	Inner Layer 5	1 oz. Copper
Signal 4	Inner Layer 6	½ oz. Copper
Signal 5	Inner Layer 7	½ oz. copper

GND 2	Inner Layer 8	1 oz. copper
Signal 6	Bottom	½ oz. copper

3.3 Power Supply Decoupling Layout

TM5400/TM5600 VDDCORE decoupling caps (8 x .22uf X7R 0603) should be placed directly underneath the processor on the opposite PCB side (shown below). VDDCORE plane shown in diagram should extend significantly beyond the processor for connection to other peripheral decoupling caps.

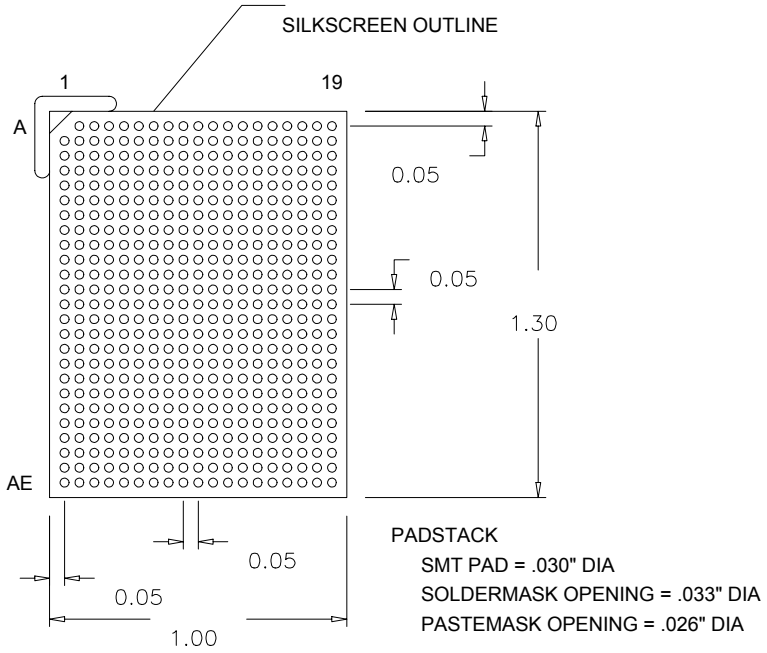
FIGURE 6 TM5400/TM5600 VDDCORE Underside BGA Decoupling Example



BOTTOM SIDE (AS SEEN FROM TOP SIDE)

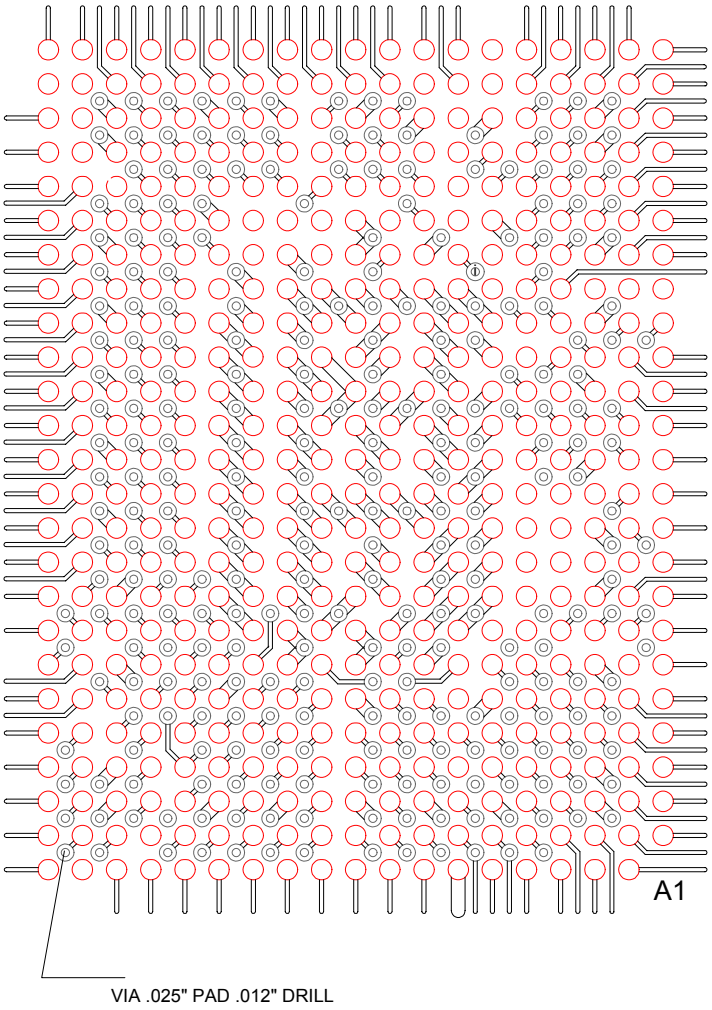
3.4 Processor Footprint

FIGURE 7 TM5400/TM5600 Mechanical Footprint



3.5 BGA Pin Escape Diagram

FIGURE 8 BGA Pin Escape Example



PIN ESCAPE EXAMPLE (TOP SIDE SHOWN)

3.6 Recommended Standard Spacing/Line/Via Constraints

All data is taken from Allegro.

Line to Line	5 mils
Line to Pad	5 mils
Pad to Pad	5 mils
Line width	5 mils
Via	25/12
Etch on subclass	allowed
Same net DRC	off

3.6.1 Allegro Extended Spacing Constraints

Default - Global (all etch/layers)

Pin to Pin	5
Line to Pin	5
Line to Line	5
Via to Pin	**
Via to Via	10
Via To Line	5
Shape to Pin	5
Shape to Via	5
Shape to Line	5
Shape to Shape	5

Thru Pin	5	5	5	10	10	10	5	5
SMD Pin	5	5	5	8	8	8	5	5
Test Pin	5	5	5	10	10	10	5	5
Thru Via	10	8	10	10	10	10	5	5
Test Via	10	8	10	10	10	10	5	5
B/B Via	10	8	10	10	10	10	5	5
Line	5	5	5	5	5	5	5	5

Shape	5	5	5	5	5	5	5	5
	Thru Pin	SMD Pin	Test Pin	Thru Via	B/B Via	Test Via	Line	Shape

BGA - Global (all etch/layers)

Pin to Pin	5
Line to Pin	5
Line to Line	5
Via to Pin	**
Via to Via	10
Via To Line	5
Shape to Pin	5
Shape to Via	**
Shape to Line	5
Shape to Shape	5

Thru Pin	5	5	5	6	6	6	5	5
SMD Pin	5	5	5	7	7	7	5	5
Test Pin	5	5	5	6	6	6	5	5
Thru Via	6	7	6	10	10	10	5	**
Test Via	6	7	6	10	10	10	5	**
B/B Via	6	7	6	10	10	10	5	**
Line	5	5	5	5	5	5	5	5
Shape	5	5	5	**	**	**	5	5
	Thru Pin	SMD Pin	Test Pin	Thru Via	B/B Via	Test Via	Line	Shape

CLKS - Global (all etch/layers)

Pin to Pin	5
Line to Pin	5
Line to Line	15
Via to Pin	**
Via to Via	10
Via To Line	5

Shape to Pin	5
Shape to Via	5
Shape to Line	15
Shape to Shape	15

Thru Pin	5	5	5	10	10	10	5	5
SMD Pin	5	5	5	8	8	8	5	5
Test Pin	5	5	5	10	10	10	5	5
Thru Via	10	8	10	10	10	10	5	5
Test Via	10	8	10	10	10	10	5	5
B/B Via	10	8	10	10	10	10	5	5
Line	5	5	5	5	5	5	15	15
Shape	5	5	5	5	5	5	15	15
	Thru Pin	SMD Pin	Test Pin	Thru Via	B/B Via	Test Via	Line	Shape

NOTE Constraint set values not the same for all subclasses.

Allegro Extended Physical (Lines/Vias) Constraints

Default—All etch

Min Line Width	5
Min Neck Width	5
Max Neck Length	0
Allow on Etch Subclass	Allowed
'T' Junctions	Anywhere
Min BBvia Stagger	5
Max BBvia Stagger	5
Pad/Pad Direct Connect	All Allowed
Current Via	25/12

PCI—All etch

Min Line Width	5
Min Neck Width	5
Max Neck Length	0

Allow on Etch Subclass	Allowed
'T' Junctions	Pins & Vias Only
Min BBvia Stagger	5
Max BBvia Stagger	5
Pad/Pad Direct Connect	All Allowed
Current Via	25/12

CLKS—All etch

Min Line Width	5
Min Neck Width	5
Max Neck Length	0
Allow on Etch Subclass	Allowed
'T' Junctions	Pins & Vias Only
Min BBvia Stagger	5
Max BBvia Stagger	5
Pad/Pad Direct Connect	All Allowed
Current Via	25/12

Allegro Extended Electrical (Lines/Vias) Constraints

	Max Stub Length	Max Via Count
Default	0 mils	0
CD	0 mils	0
CLKS	600 mils	5
PCI	1500 mils	6
SDRAM_D	300 mils	4
SDRAM	600 mils	4

3.7 Recommended PWB Fabrication Notes

- The finished printed circuit board shall meet the requirements of IPC-A-600.
- Configuration of the printed circuit board not specifically dimensioned on the drawing shall be controlled by the gerber data.

- Material: .056 +/- .006 thick glass epoxy, natural color. Laminated NEMA grade FR4. See layer stack-up for copper weight and layer orientation. Core and prepreg combinations are optional to the manufacturer unless otherwise specified in the layer stack-up.
- Plating: All holes and conductive surfaces shall be plated with .001 copper minimum. All copper areas not covered by solder mask shall be solder coated .0003 minimum.
- All hole diameters are stated as finished hole sizes.
- Fabrication tolerances: End product trace widths and lands shall not vary more than the smaller of .002 or 20% of the trace width from the gerber data.
- Solder Mask: Photo-imaged liquid polymer on both sides of board in accordance with IPC-SM-840, type B Class 2 over bare copper.
- Component Marking: Silkscreen component side (and solder side) white, non-conductive epoxy ink. Lands and exposed plated areas to be free of ink.
- Bow and Twist: Shall not exceed .005 inch per inch.
- Electrical Test: The printed wiring board shall be electrically tested for opens and shorts. The results of the electrical test shall be documented and delivered along with each lot.
- Identification: Vendor logo to be etched on the solder side, silkscreen data code on the bottom side.
- Characteristic Impedance: 55 ohms +/- 10%.
- Do NOT match impedances on traces wider than 6 mils.

3.8 DDR SDRAM

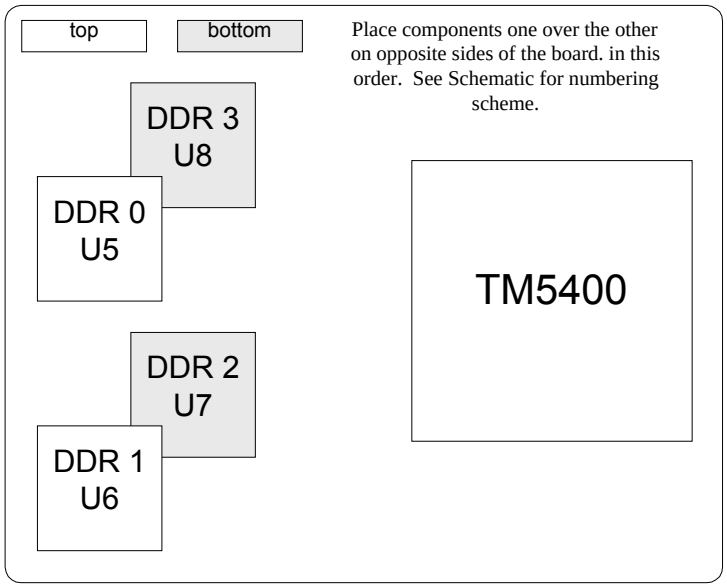
The CD port DDR SDRAM operates at frequencies of 133Mhz or more. Use standard high speed layout design practices.

Some general guidelines in DDR memory layout are:

- Traces are routed in groups: DQS, DQMB, and 8 DQ lines.
- The DQ lines within each byte must be the same length as DQS and DQMB lines in that group to within +/- 0.4”
- Layout components as shown below (numbers refer to schematics). The components should be exactly on top of one another in this order. Devices 0-1 get clock A/A# and devices 2-3 get differential clock pair B/B#

- A nominal DDR SDRAM layout must have CD signals less than 2 to 3 inches. It is recommended to layout the TM5x00 and the CD memory first with trace lengths as short as possible in order to obtain a nominal layout.
- DQ and DQMB signals must be shorter than DQS signals by 5% of the trace length. (i.e., DQS must be longer than DQ/DQMB by +5%).

FIGURE 9 Recommended DDR Layout



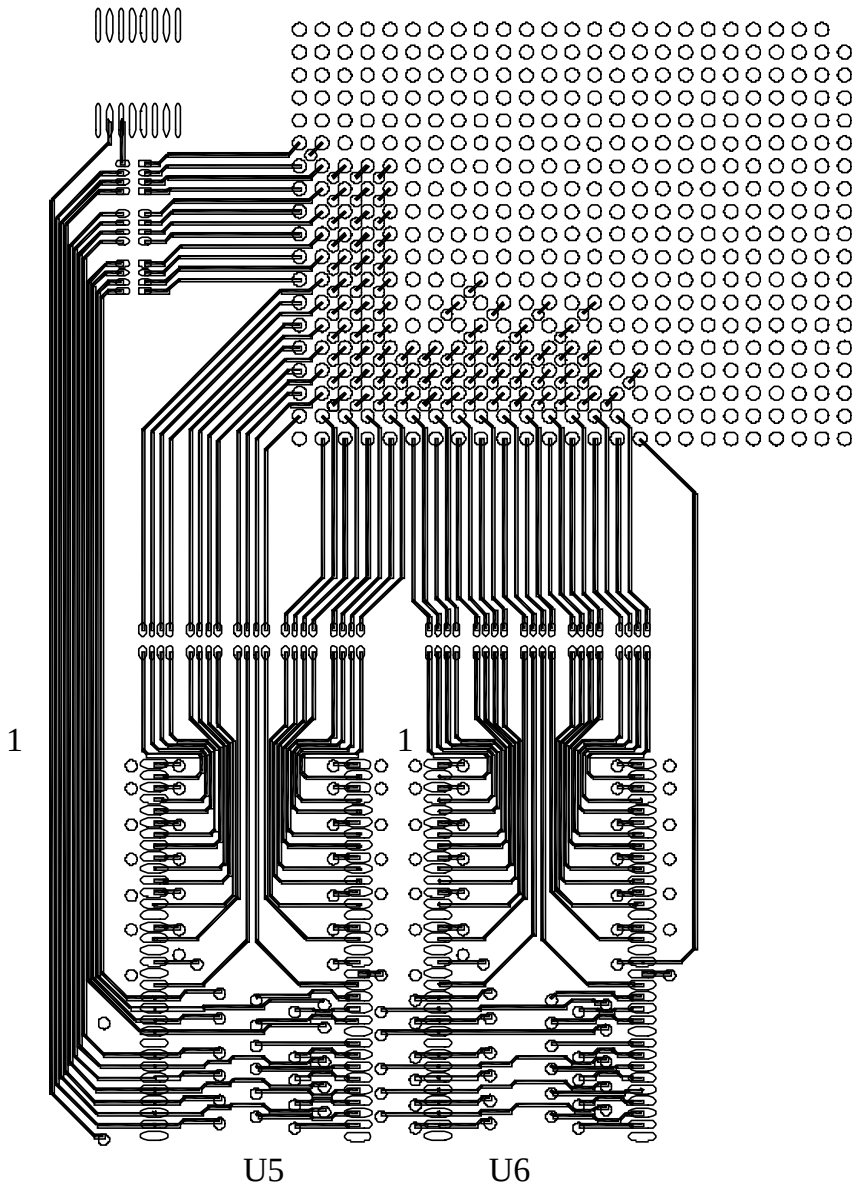
- The differential clocks should be as close to exactly the same length as possible.
- All byte groups are swappable with other byte groups and all data bits within each byte are swappable to facilitate meeting length requirements.

3.8.1 DDR Trace Route Examples

Primary Side (Top)

The figure below shows connections from the TM5400/TM5600 to the DDR memory on the primary (top) side of the board.

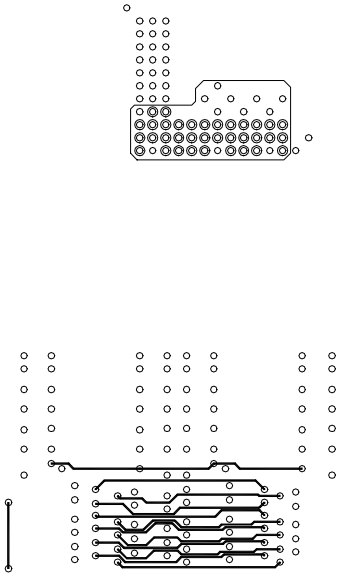
FIGURE 10 4-Chip DDR Memory Layout, Top Layer



Internal Layer

The figure below shows connections from the TM5400/TM5600 to the DDR memory on an internal side layer of the board.

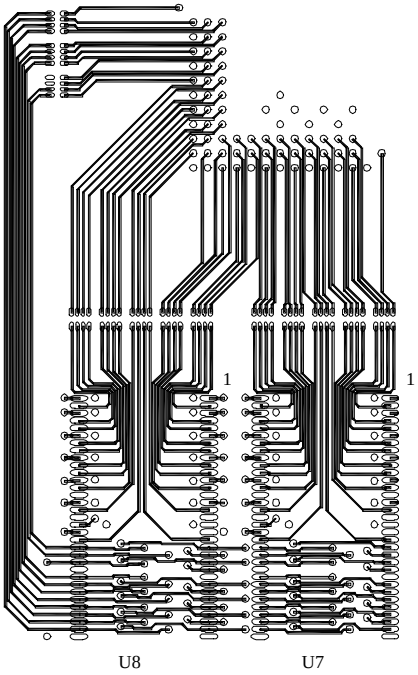
FIGURE 11 4-Chip DDR Memory Layout, Internal Layer



3.8.2 Secondary Side (Bottom)

The figure below shows connections fromthe TM5400/TM5600 to the DDR memory on the secondary (bottom) side of the board.

FIGURE 12 4-Chip DDR Memory Layout, Bottom Layer



Chapter 4

Thermal Design Considerations

This chapter outlines an example of a thermal solution for Transmeta processors in a laptop computer environment.

4.1 Overview

The processor is typically the most concentrated heat generating component in a computer system. In order for the component to operate within specified temperature limits (<85 degrees Celsius for the TM5400/ TM5600), the heat must be pulled away from the chip. This can be accomplished in a variety of ways, the most popular are cooling fans and metal heat sinks which conduct heat to other parts of the product.

Transmeta processors are extremely low-power and require only a heat sink or Thermal Transfer Device (TTD) to sufficiently cool the chip to operating temperature ranges. Each product is a unique problem, however. The mechanical characteristics and PCB layout play an important role in the heat of a system and may require more elaborate cooling methods. Conversely, some systems might not require any thermal solution at all. Thermal design guidelines are discussed later in this document.

Also, the effectiveness of this example solution (TTD) is demonstrated. The design of this TTD is shown for reference.

4.2 Thermal Design Guidelines

- Use a heat transfer plate to conduct heat away from the processor into the bulk of the portable device.
- Most portable electronic devices (laptops, Internet appliances, etc.) do not have a lot of bulk metal in the case or rest of the design for weight and cost reasons. In order to provide a bulk region in the device to absorb the processor's and other component's heat, thermally conductive magnesium cases can be used in addition to thicker PCB ground planes.
- The keyboard of a laptop device often has a metal frame which serves as a good place to redistribute processor heat.
- Thermal transfer device (TTD) should bolt to the PCB and preferably connect to the ground plane of the PCB to increase thermal conductivity to the PCB. The TTD should come within 20 mils (.02") of

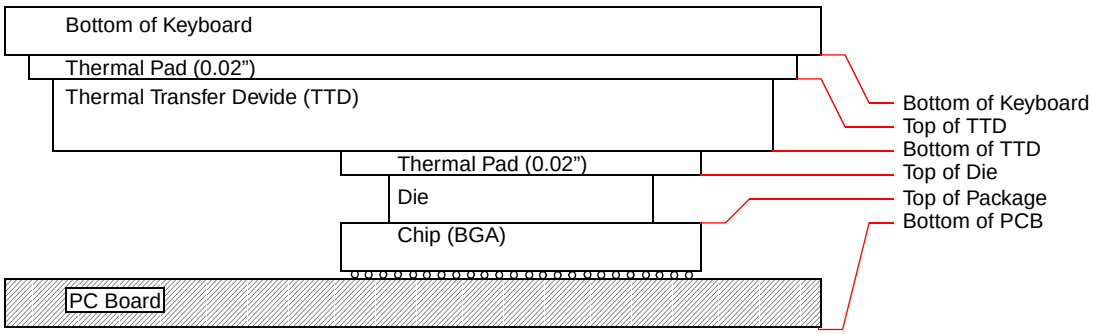
the top of the processor die. Use of a thermally conductive pad should be used between the top of the die and the TTD (Bergquist Gap Pad for instance).

- TTD shown is made of aluminum with gold flash or other metal with high thermal conductivity.
- TTD contact surface area to case or other device heat sink (i.e. bottom of keyboard) should be as big as possible for most efficient heat redistribution; about 3-5 in^2 should be sufficient. Square or rectangular shape oriented similar to the die is preferable shape to offer the most uniform heat distribution.
- Use of thermally conductive pad (i.e. Bergquist Gap Pad) should be used between TTD and device heat sink or case. ('heat sink' meaning the bulk material to which heat is being redistributed inside the device)
- Locate the processor as close as possible to the TTD heat transfer point (i.e. keyboard bottom, case, etc). This increases the effectiveness of the TTD as well as simplifies its design. Also, reduce the cost of the overall thermal solution by not requiring a heat pipe or other heat channeling device to transfer the processor heat over a long distance.

4.3 Thermal Transfer Device (TTD) Example Design

The TTD is screwed into the PCB near the 4 corners of the BGA. (For PWB and mechanical guidelines, see Chapter 3, *PWB Layout*.) A Berquist Gap Pad (.02" thick) is used to make contact between the die and the TTD. In this design, the processor is underneath the keyboard which has a metal base. The TTD was designed to come within .02" of the bottom of the keyboard and .02" from the top of the die. Thermally conductive pad is used to make contact to the bottom of the keyboard. The surface area of the TTD is as big as possible given space restraints (about 3" square). This TTD is about .1" thick. See the mechanical drawings below for more information.

FIGURE 13 Thermal Measurement Probe Placement in Laptop System



Temperature measurements shown in Figure 14 and Figure 15 display temperature of measurements points marked in Figure 13 taken over a short time. The system had been running for a long time in both cases and temperatures were stable around the measurements shown.

The system running Windows idle is relatively cool since not much processing is going on. Conversely, a DOS Prompt running under Windows is one of the most power hungry programs available and makes a good high power/heat benchmark.

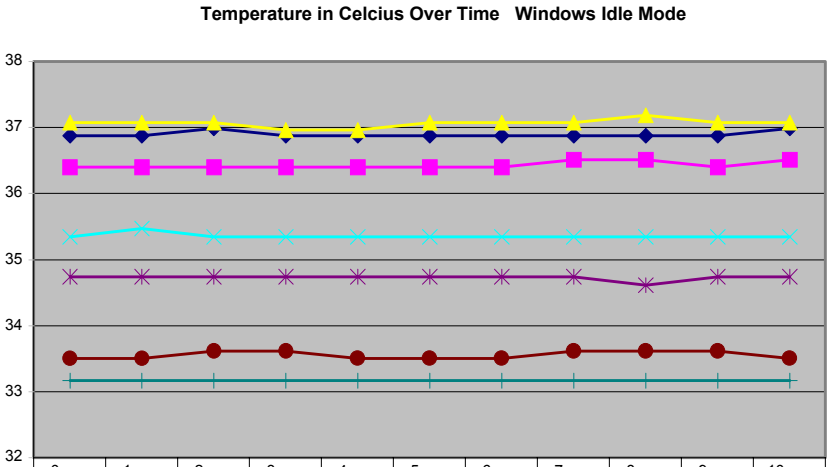
The TTD does a good job of redistributing the heat from the die into the bottom of the keyboard (and eventually to the ambient temperature. Without the TTD, the processor would be near recommended operating temperature limits.

4.4 Thermal Measurements

4.4.1 400Mhz TM120 at 1.7V

Windows Idle

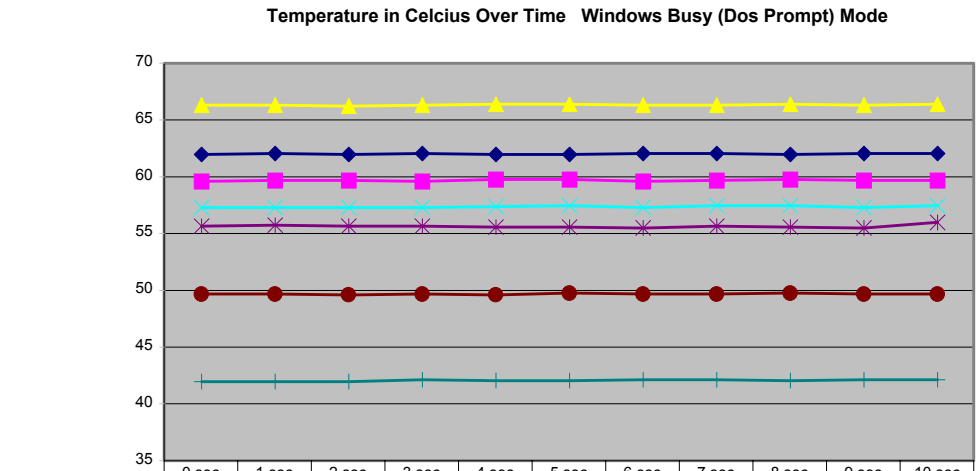
FIGURE 14 Thermal Measurements of TTD in Laptop System–Running Windows (Idle)



	0 sec	1 sec	2 sec	3 sec	4 sec	5 sec	6 sec	7 sec	8 sec	9 sec	10 sec
Bot of PCB	36.876	36.876	36.993	36.876	36.876	36.876	36.876	36.876	36.876	36.876	36.993
Top of PKG	36.394	36.394	36.394	36.394	36.394	36.394	36.394	36.511	36.511	36.394	36.511
Top of Die	37.072	37.072	37.072	36.955	36.955	37.072	37.072	37.072	37.189	37.072	37.072
Bot of TTD	35.351	35.469	35.351	35.351	35.351	35.351	35.351	35.351	35.351	35.351	35.351
Top of TTD	34.735	34.735	34.735	34.735	34.735	34.735	34.735	34.735	34.618	34.735	34.735
Bot of Keyboard	33.498	33.498	33.616	33.616	33.498	33.498	33.498	33.616	33.616	33.616	33.498
Ambient	33.16	33.16	33.16	33.16	33.16	33.16	33.16	33.16	33.16	33.16	33.16

Windows Busy (Dos Prompt)

FIGURE 15 Thermal Measurements of TTD in Laptop System–Running DOS in Windows (Busy)



	0 sec	1 sec	2 sec	3 sec	4 sec	5 sec	6 sec	7 sec	8 sec	9 sec	10 sec
Bot of PCB	61.93	62.041	61.93	62.041	61.972	61.972	62.041	62.041	61.972	62.041	62.041
Top of PKG	59.562	59.674	59.674	59.562	59.716	59.716	59.562	59.674	59.716	59.674	59.674
Top of Die	66.323	66.323	66.212	66.323	66.364	66.364	66.323	66.323	66.364	66.323	66.433
Bot of TTD	57.336	57.336	57.336	57.336	57.378	57.491	57.336	57.448	57.491	57.336	57.448
Top of TTD	55.617	55.73	55.617	55.617	55.546	55.546	55.504	55.617	55.546	55.504	55.955
Bot of Keyboard	49.672	49.672	49.558	49.672	49.601	49.715	49.672	49.672	49.715	49.672	49.672
Ambient	41.98	41.98	41.98	42.096	42.023	42.023	42.096	42.096	42.023	42.096	42.096

4.5 Power Measurements

TABLE 3 Power Consumption of TM3200 at Thermal Measurement Operating conditions

TM3200 Speed	TM3200 Voltage	Power Consumed (Windows Idle) (with power management)	Power Consumed (Windows Busy)
400MHz	1.5V	1.44W	3.36W
400MHz	1.7V	1.77W	4.32W
500MHz	1.8V	TBD	TBD

4.6 TTD Mechanical Specifications

FIGURE 16 Thermal Transfer Device Mechanical Cross Section

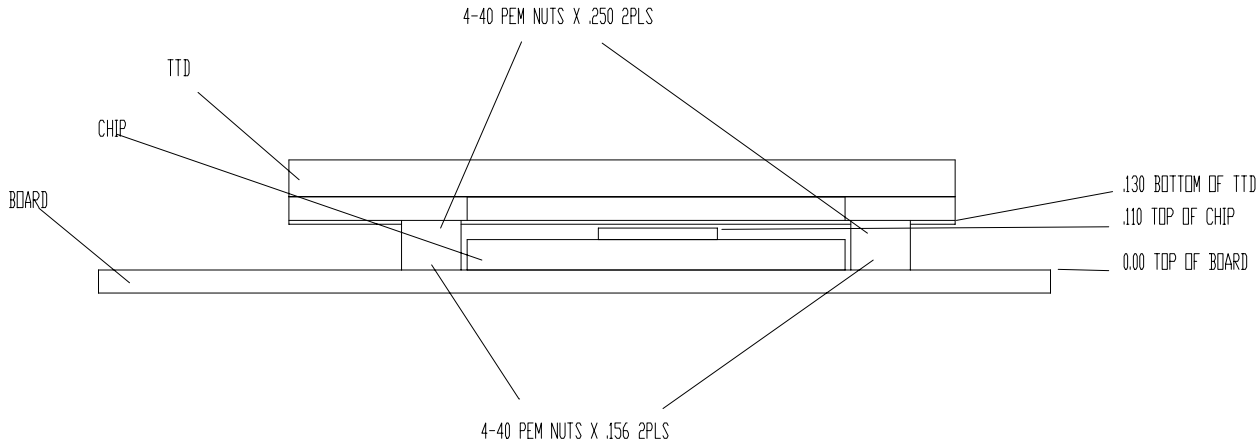


FIGURE 17 TTD Mechanical Top View

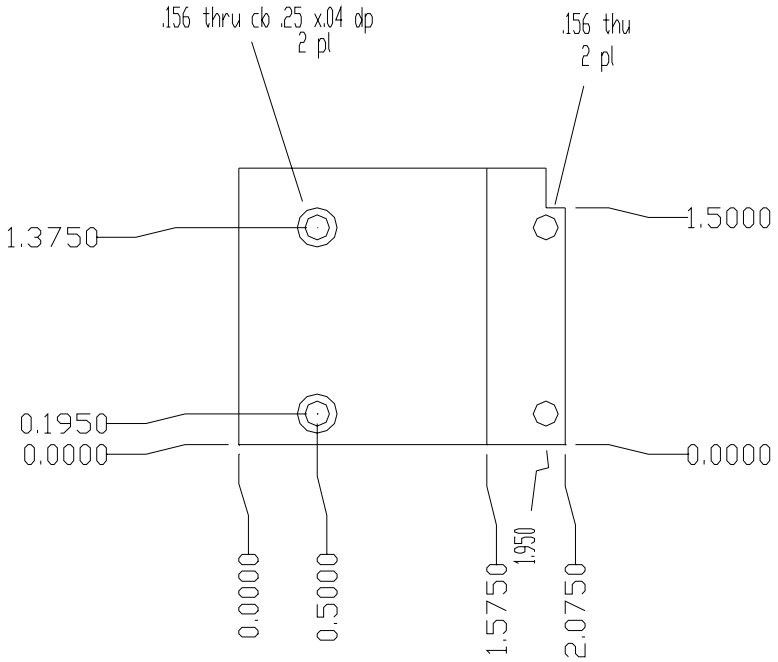


FIGURE 18 TTD Mechanical Bottom View

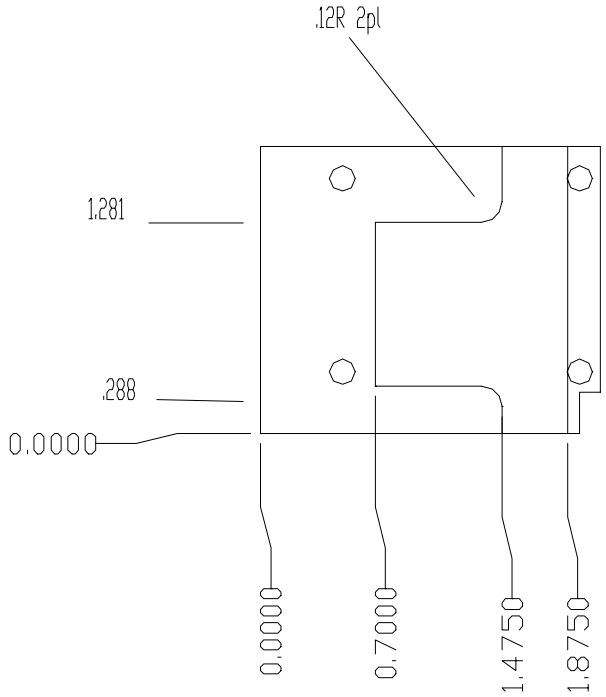
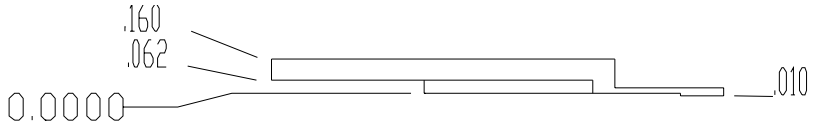


FIGURE 19 TTD Mechanical Bottom View



4.7 Thermal Transfer Device Pictures

FIGURE 20 Crusoe Processor and TTD Mounting Holes

FIGURE 21 TTD Over the Crusoe Processor

FIGURE 22 TTD In Place Over the Crusoe Processor

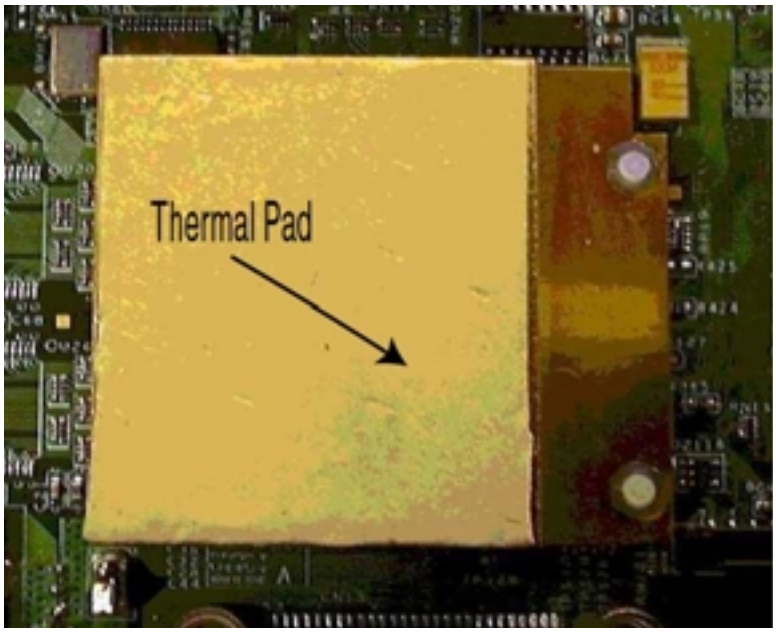
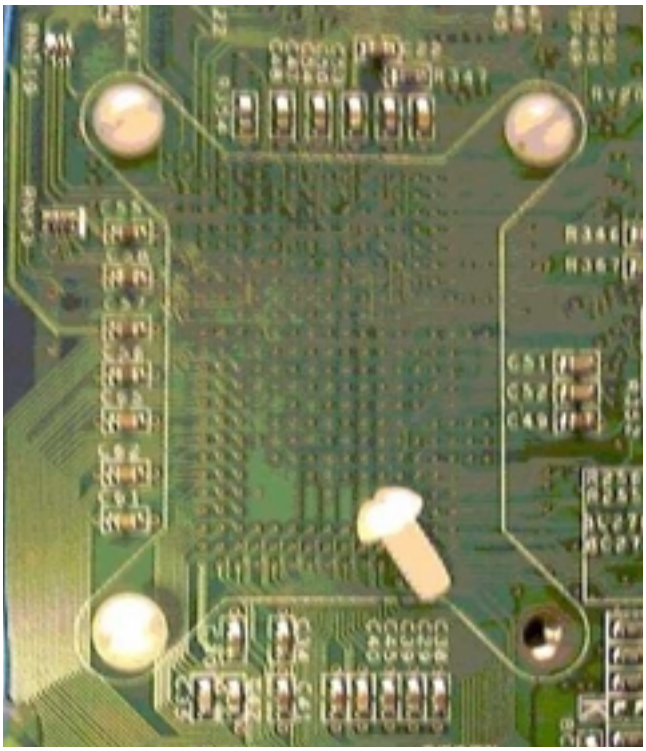


FIGURE 23 Bottom of PC Board, Screws for TTD



Chapter 5

Crusoe Processor Reference Schematics Description

The reference schematics are a fully implemented core design with all elements shown in the block diagram in Chapter 1, *System Block Diagram*.

The schematics were designed in Orcad Capture V9 and the source is available to customers. The processor was split apart into 4 schematic symbols that span pages 2-5. Layout issues of the DRAM are discussed in the Layout section.

NOTE The Reference Schematics describe both TM3200 and TM5400/TM5600 processors.

5.1 Core Schematics

Page 1. Index

Index page of schematics.

Page 2. TM3200 and TM5400/TM5600 CD (CMS Dram) Connections

This page shows all the signals and off page connectors which go to the CD termination resistors and eventually to the DDR dram. The CD interface of the TM5400/TM5600 has differential clock drivers and requires a reference of IOVDD25/2 (1.25V) to the C_VREF pin. 1% resistor divider from the V_25S supply generates the reference.

Page 3. TM3200 and TM5400/TM5600 DI (DRAM Interface) port

- This section also includes other TM3200 or TM5400/TM5600 signals like clocks and resets. The DI connections are shown with off page connectors that go to terminations resistors and to the DI memory in the design. The DI interface of the TM3200 has 8 chip selects, 8 clocks, and 4 clock enables for SDRAM. The DI interface of the TM5400/TM5600 has only 4 chip selects, 4 clocks, and 2 clock enables. All the clocks and clock enables are identical and are provided for loading reasons. Each clock and chip select is capable of driving up to 8 loads, but for highest speed operation, x16 memory devices are recommended to reduce the amount of loading to 4 devices per chip select. To design a TM3200 system compatible with the TM5400/TM5600, use only S_CS#[3:0], S_CLK[3:0], and S_CKE#[1:0] on the TM3200.

The schematics show connections to 2 SO-DIMM slots. If only one SO-DIMM slot is to be used and soldered down memory is used as well, connect the signals from SO-DIMM#1 to the soldered down memory. By convention, the highest order bank chip select S_CS#[3:2] should be connected to the most permanent DI memory. Chip selects 1-0 go to SO-DIMM slot 0, 3-2 go to SO-DIMM slot 1, and chip select 2 is used also for the soldered down bank of SDRAM if a second SO-DIMM is not used. The OEM configuration table must reflect this info so CMS will know where to look for memory at boot time. Clock enable signals have strong drivers and only one clock enable is needed per pair of chip selects.

- The S_CLKOUT and S_CLKIN signals are used for loop timing by the DI port. Connect these signals with a 33 ohm resistor at the source (S_CLKOUT) and make the trace length a calculated length equal to the average of all the data line trace lengths.

- The TDM connects to the TM3200 or TM5400/TM5600 here at S_SDATA and S_SCLK pins (I2C). The TM3200 or TM5400/TM5600 use P_RST# for its master RESET# signal. The TDM is also able to assert P_RST# by connecting it via 1.2k resistor to TDM_RST# since P_RST# is not an open collector signal.

- If designing for TM5400/TM5600 compatibility, note the test point connections to reserved pins that become 'SNIFF' pins on the TM5400/TM5600.

- TM5400/TM5600 SNIFF pins should be connected to test points if it is desired to inspect these signals.

- The SLEEP# signal is connected to the south bridge SUSPEND_STATUS signal (SUS_STAT1# on the PIIX4 or SUSPENDJ output on the ALI M1535). Make sure that, depending on which south bridge you are using, the signal is not over 3.3V. The ALI M1535, for example, has a 5V SUSPENDJ signal and must be level translated to 3.3V before going to the TM3200 or TM5400/TM5600. This is accomplished with a quickswitch with a 4.3v power supply as shown on the M1535 page.

Page 4. TM3200 and TM5400/TM5600 PCI and Other Misc. Connections

- P_LOCK# is pulled-up to V_3S but not connected to any other system component.

- TM3200 or TM5400/TM5600 JTAG connections to the TDM are shown. TDM_TRST# is also connected to P_PCI_RST# pin (P_RST# signal) through a 4.7k resistor. This is so the debugger can issue a JTAG reset without asserting P_RST#.

- P_PERR# connects to PCI connectors and/or PC card interface which is out of the scope of the core.

- Isolation Quickswitch on P_HOLD# signal is there to fix a chip errata and is required for TM3200. Please implement this circuit exactly as shown. A install the bypass resistor for TM5400/TM5600 (which doesn't need this fix).

- All reserved pins should be pulled up/down or left unconnected as shown. Also, Reserved_(G2) is connected to the P_HOLD# quickswitch and also pulled down as shown. This signal is used by CMS with the quickswitch to implement ISA_REQ# compatibility.

- EPROMA[2:1] are ROM bank select pins that connect to a parallel ROM for CMS/BIOS if no serial ROM is used. Example connections are shown in subsequent pages.

- PCI connections connect outside of the core but examples of connections to several south bridges are also shown in other pages.

- The Maxim MAX1617 Temperature sensor is shown connecting to the DIODE_CATHODE/ ANODE pins of the processor. The QS3257 MUX shows an optional way to intercept this device from a south bridge SMBUS I2C bus and temporarily reroute the ATF I2C signals to the TDM debugger to be read. The ATF_INTCPT signal comes from the TDC connections on "Page 11. CMS and Mode ROMs, TDM Debug connectors" on page 70.

- The TM5400/TM5600 requires a pull-up to V_25S on FERR# and be sure to include a resistor pad for TM5400/TM5600 compatibility. Also, on initial versions of the TM5400/TM5600, the VRDA[] pins are 2.5V only and will require a level translation to 2.5V at the TM5400/TM5600 for protection.

- The P_REQ[5..0]# inputs of the TM3200 and TM5400/TM5600 are pulled up to V_3S.

- P_GNT#[] outputs will be tri-stated when the TM3200 or TM5400/TM5600 is in deep sleep. Ensure they are pulled up for other system components that the P_GNT[] signals connect to (pull-ups must be tied to V_3S (IOVDD).

Page 5. TM3200 and TM5400/TM5600 Power connections

This page shows all the power connections and recommended decoupling for the TM3200 and TM5400/ TM5600.

For VDDCORE: Use 8 x.1uf 0603 X7R ceramic caps under the TM3200 and TM5400/TM5600. 20 x 1uF 1206/0805 X7R ceramic caps surrounding the chip. 6 x 220uF Tantalum low ESR (100m ohm or less) as bulk capacitance as close to the chip as possible.

IOVDD : use 14 x 1uF X7R 1206/0805 ceramic caps as close to the chip as possible. Use 2 x 22uF Tantalum low ESR caps for bulk.

IOVDD25: 8 x 1uF X7R 1206/0805 ceramic caps as close to the chip as possible. 1 x 22uF Tantalum low ESR cap for bulk capacitance.

The connection between V_25S and IOVDD25 is shown.

Page 6. CD Memory

One bank of DDR Memory is shown with it's connections to the TM5400/TM5600 CD memory port. V_REFCD should be V_DDRCORE/2. A layout block diagram is also shown. This is addressed in more detail in the layout section of this document.

Page 7. CD Memory Termination

All memory signals are series terminated. 33 ohms is appropriate for this configuration. If more than 1 bank of DDR were used, impedance should be verified.

DDR clock enable signals need to be filtered through the QS3257 MUX which will select a pull-down for the device's signal when SUSPEND_STATUS is asserted (notifying that the system is in STR/STD mode). This MUX scheme protects the DDR from signal transitions on the clock enable signals as the processor comes in and out of a power down state.

Page 8. DI Memory Bank 0-3 (SO-DIMM slots #0 and #1).

2 SO-DIMM slots are shown with their connections. Decoupling caps should be placed as close to the connectors as possible.

TM3200 and TM5400/TM5600 DI Chip selects 0 and 1 control slot #0 and 2 and 3 control slot #1.

Since SO-DIMM DRAM use a fixed address I2C SPD (serial presence detect), the I2C connections to the south bridge SMBUS I2C bus must be multiplexed. The DIMM_B_SEL# control signal for the MUX should come from a GPO pin on the south bridge. If only one SO-DIMM slot is to be used, the MUX is not needed and SMBUS can simply be connected directly to the SO-DIMM. Also note that the SO-DIMM SPD bus does not have an I2C address so the MUX enable is used (DIMM_B_SEL_EN#) and should be controlled by a GPO pin from the south bridge.

Page 9. DI Soldered Down Memory Bank

Four x16 bit devices are shown as soldered down DI memory and connected to CS2# from the TM3200 or TM5400/TM5600. The most 'stable' or known memory configuration should be at the highest order DI chip select.

Use this memory only in place of one SO-DIMM#2 slot if designing for TM5400/TM5600 compatibility.

Page 10. DI Memory Termination

Every DI memory signal is source series terminated. 18 ohms should be fine for this example but designer should recalculate based on specific design.

Like in the CD memory terminations, the DI clock enable signals are fed through a SUSPEND_STATUS controlled quickswitch MUX to avoid signal glitches during TM3200 or TM5400/TM5600 power transitions.

Page 11. CMS and Mode ROMs, TDM Debug connectors

Typical connections to the 8Mb CMS ROM and 2Kb serial Mode Bit ROM are shown as well as TDCA and TDCB (Transmeta Debug Connectors A and B) to the TDM. For this serial ROM device, only one chip select is needed but the other is shown for reference. The TDM connects to these devices through

directly while a 220 ohm resistor separates the TM3200 or TM5400/TM5600 signal from the TDC signal. This is so the TDM can drive these signals without contention to the processor's signals. Note how P_RST# and PWRGD_CORE are used as reset for the mode ROM and the CMS ROM, respectively.

TDCA has a predefined pinout. If using the vertical style, top-contact connector, this pinout is used but reverse the pinout if using the right angle, top-contact FPC connector in your design (which also applies to the TDCB).

TDCB is an optional 24pin debugger cable. All pins are user defined. (see TDM spec for more detail). These schematics show the pinout of both connectors using the vertical style connector.

TDCB is shown in a typical use scenario but it is up to the designer exactly how this connection might be used.

Note that it is important to ensure that any connection going to the TDM connectors should be pulled up or down as needed somewhere in the design.

Write Protect PLD addition to CMS Serial Flash ROM

NOTE A 22LV10 PLD is added to intercept the TM5400/TM3200 SROM_CS[1:0]# signals to the serial Flash SROM device(s). The PLD intercepts write cycles to the device when writes are not authorized (controlled by a GPIO pin from the south bridge chip). This addition is required for all systems using serial Flash ROM for CMS storage; systems using the parallel ROM for CMS storage do not require a PLD. The programming file and code can be obtained from Transmeta.

5.2 System Level Reference Schematics

NOTE The following schematics are not part of the strict Crusoe CORE but are shown for reference to see typical connections to components that interact intimately with the core.

Page 12. Power Supply : VDD_CORE—LTC1736
Page 13. Power Supply : VDD_CORE—MAX1711

The Maxim MAX1711 is used to generate VDD_CORE for the TM3200. Connector TDC-B (Transmeta Debug Connector) connects to the D[] inputs which allow the debugger to dynamically vary CPU core voltage for testing. This device has an internal pull-up on the D[] to 5V so only a pull-down is required in determining the boot up voltage. SHDN# is controlled by the south bridge STR_CTL signal which is asserted during CPU power down modes. Circuit should be modified if needed to match exact user requirements.

NOTE Ton pin should be left open (300kHz operation). High Side FET is FDS4410. Low side FET is FDS6680A. (FDS4410 may also be used as a low side FET but is not as good a choice as the 6680A for overall efficiency). The inductor is 1.8uH, 7A. Rlim is 270k for FDS6680A (use 440k if FDS4410 is used). Use 6x220uF 50mohm ESR or less.

These changes are important in order for the supply to meet the current requirements of a TM5400 using Longrun. See reference schematics for details.

NOTE Added schmitt trigger/FET circuit as shown to 1736/1711 powergood filter to sharpen the edges on PGOOD.

outputPage 14. BIOS Boot ROM with CMS option

This circuit uses the Fujitsu 29F160 2MB Flash ROM. Shown are connections of the TM3200 or TM5400/TM5600 EPROMA[2:1] signals to the highest order address bits of the ROM to act as bank selects. These signals allow the TM3200 or TM5400/TM5600 to control the lower 3/4 of the device for CMS and allow only the upper 1/4 to be accessible to the x86 BIOS code.

Also shown is the ROM un-protection circuit used to release protected sectors in the ROM and allow them to be updated. The CMS sectors should all be protected which will prevent them from from erasure by an 'erase all' command (issued by x86 code). During a CMS upgrade, the CPU will assert the 'UNPROTECT' signal, which is connected to the TM5400/TM5600 RSVD_G2 pin, in order to unlock the protected CMS sectors. (This is accomplished by providing 12V to the ROM chip). This un-protection circuit is not used in TM3200 systems since the RSVD_G2 pin is not available. To allow CMS upgrades in a TM3200 system, the lower ½ of the ROM should be protected and will not be upgradeable in the field. The remaining, unprotected, CMS sector(s) will store upgrades to CMS.

Page 15. Power Supply : Memory

Maxim's MAX1655 is used to generate the V_25 and V_25S needed for the TM3200 or TM5400/ TM5600 CD interface and the 2.5V DDR Memory. The south bridge STD_CTL signal is used to control SHDN# control signal since STD_CTL (SUSC# from the PIIX4) is only asserted during power down states where the memory is powered down. Circuit values should be changed if needed to meet the designs specific power requirements.

- V_25 is generated directly from the MAX1655 but the STR_CTL signal is used to control a p-channel FET gate to generate V_25S (2.5v switched supply).
- Need to invert STR_CTL for proper FET operation.

Page 16. Clock Generator

Here is a typical clock generator and some example connections.

South Bridge Examples

Only the core connections are shown. There are many variables in the configuration and connection of this device. The signals to the processor and some other core components are shown to help better demonstrate how a TM3200 or TM5400/TM5600 interface to a south bridge.

Some general notes: CPURST# output from each south bridge is not used to control the RESET# of the processor. PCI RESET# is used to reset the TM3200 or TM5400/TM5600 at the chip level. PWRGD_SYS comes from the system level power supply.

Additions to System Clock Generator Chip

The existing circuit shows connections necessary when using a IMI571 clock generator. The schematics have been updated to show the additional connections needed when using the pin compatible ICS9148-12 device (CK66 compatible). Details include a pull-up on the select pin as well as a pull-down on pin 47 which is a voltage select for the CPUCLK on the ICS part.

Page 17. Intel PIIX4 South Bridge

- The PIIX4 South Bridge connections are relatively straightforward. SO-DIMM SPD MUX control signals are shown here for reference (not shown in other south bridge examples but should be similar). PWRGD_SYS should come from the system level logic power supply (not shown).
- PCI connections are as shown. AD18 is used here as IDSEL, connect to AD18 through a 100 ohm resistor. The resistor value is important for the TM3200 or TM5400/TM5600.
- The PWR_BTN_PRESSED# signal from the TDM connectors connects to the PWRBTN# pin so the debugger can initiate that function remotely as a wake command.
- Ensure proper SMBUS pull-ups (not shown).
- Use a 7SH08 (single 2-input AND gate) to AND M1535 SUSPEND# and AGP_STP# signals together. Output of AND gate is used as the system SUSPEND# signal. The AND gate should be powered from 3.3V supply that is powered during C3 power state. Also, the gate acts as a 5-3.3v level translator and must have 5V tolerant inputs. The quickswitch used for level translation of SUSPEND# is no longer used and was removed from the schematics.

Page 18. Acer ALI M1535 South Bridge (part A)

This is similar to the M1533 in several ways. Namely, it requires external OR gates to connect all PCI_REQ#[5:0] signals from the TM3200 and TM5400/TM5600 as well as any other requesting signals.

NOTE The VCC_G pin of the 1535 must be connected to 2.5v for proper operation. There is a bug which causes problems when this pin is connected to 3.3V. Also, a pull-up to 2.5V is required on ZZ/RATIOJ pin.

Page 19. Acer ALI M1535 South Bridge (part B)

Note the parallel line termination on the clock signals shown as an example. Use the appropriate termination for the specific design.

Other connections may vary depending on specific design.

CORE COMPONENTS

1. 000-01 Index
2. 010-01 TM3200/5400 CD Interface
3. 010-02 TM3200/5400 DI Interface
4. 010-03 TM3200/5400 PCI & Misc
5. 010-04 TM3200/5400 Power Connections
6. 012-01 CD Memory
7. 012-02 CD Memory Terminators
8. 012-03 DI Memory Bank 0-3
9. 012-04 Soldered DI Memory Bank
10. 012-05 DI Memory Terminators
11. 012-06 ROM & DEBUG

NON-CORE REFERENCE COMPONENTS

12. 0XX-01 Power Supply: VDD_CORE LTC1736
13. 0XX-02 Power Supply: VDD_CORE MAX1711
14. 0XX-03 Power Supply: Memory
15. 0XX-04 BIOS Boot ROM with CMS option
16. 0XX-05 Clock Generator
17. 0XX-06 PIIX4 Southbridge
18. 0XX-07 ALI M1535 Southbridge (A)
19. 0XX-08 ALI M1535 Southbridge (B)

SEE DESIGN GUIDE FOR SYSTEM BLOCK DIAGRAM

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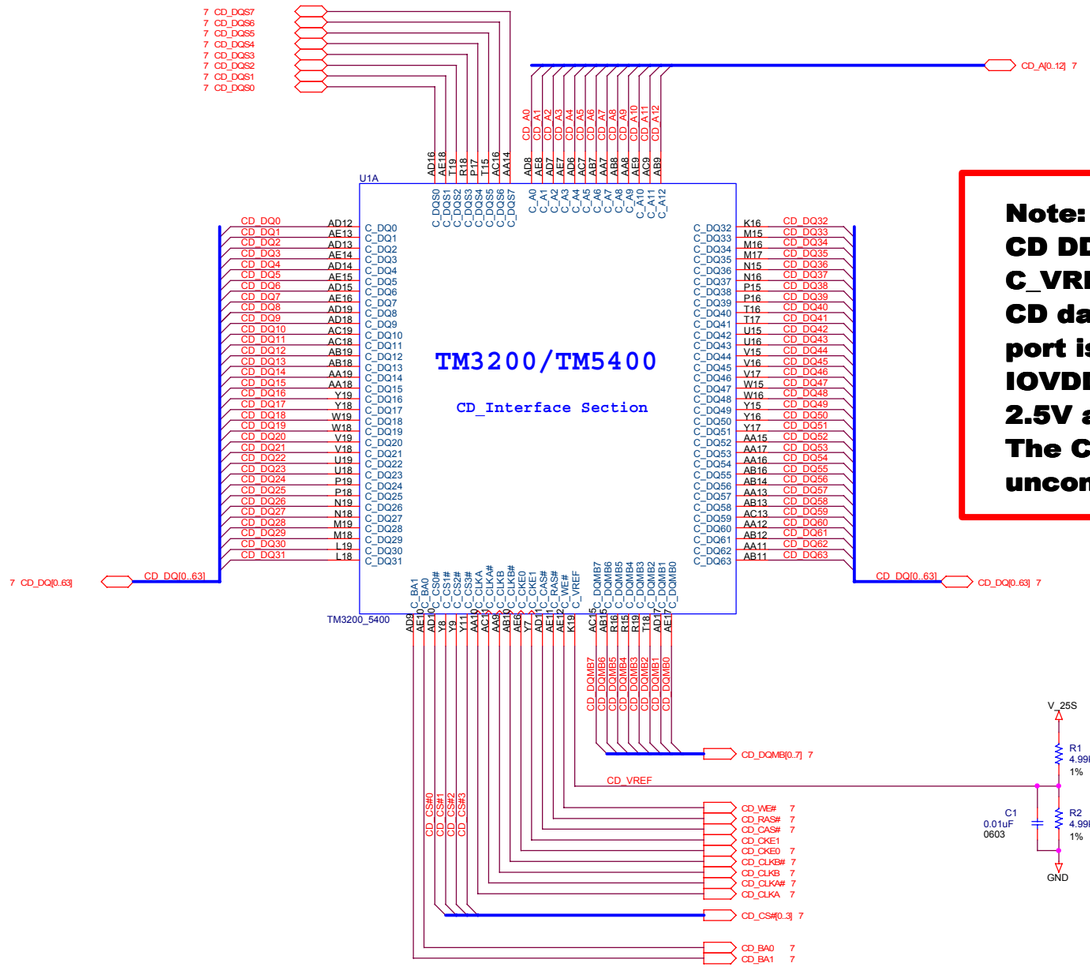

Note: The TM3200 does not support the CD DDR interface. Connect IOVDD25 and C_VREF to VDDCORE for TM3200. Leave CD data pins unconnected. When CD port is not used in a TM5400 system, IOVDD25 must still be supplied with 2.5V and C_VREF should be IOVDD25/2. The CD data pins may be left unconnected.

TM5400 requires IOVDD25/2 threshhold for CD_VREF (1.25 ideal) as shown. In a TM3200 system, connect CD_VREF and IOVDD25 to VDDCORE.

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V_25S

RN70A 8 1 10K

sus_stat1# and STPCLK# come from southbridge — 17,18 STPCLK# / 7,10,17,18 SUS_STAT1#

clk H0 comes from clock generator — 16 CLK_H0

pwr_good comes from power supply. it is open drain and SYS_RST# from the debug connector also controls this signal to reset the processor during system level reset. — 11,13 PWRGD_CORE

TDM_RST# comes from TDM debugger — 11 TDM_RST# — R3 1.2K

P_RST# from Southbridge — 4,11,17,18 P_RST#

VDD_CORE — R4 4.7 — VDD_PLL — C2 0.1uF — GND

SRCLK 11
DEBUG_INIT 11
NM_DEBUG_INIT 11
SROM_CS0# 11
SROM_CS1# 11
SROM_SCLK 11
SROM_SIN 11
SROM_SOUT 11

R5 4.7K — GND
R6 4.7K — GND

TM5400

Note: using Modebit SROM: pull-up on SRDATA instructs CMS to boot from 1MB Atmel Serial Flash (0.0 and 1.0).

V_3S — R137 4.7K — SRDATA 11

pull-down on SRDATA instructs CMS to boot from parallel ROM (1.0 only).

R159 4.7K — GND

U1B

PLLVDD A7, PWRGOOD G7, CLKIN G7, CFG_SCLK B7, CFG_SDATA A8, SLEEP# D8, RESET# H19, STPCLK# H18, DEBUG_INIT H14, NM_DEBUG_INIT W11, SROM_CS# K15, SROM_CS1# L15, SROM_SCLK L16, SROM_SIN K17, SROM_SOUT K18

Clk/Serial Control Signal

S_DQ0 W5, S_DQ1 AB4, S_DQ2 AB5, S_DQ3 AA5, S_DQ4 Y5, S_DQ5 AC4, S_DQ6 AD3, S_DQ7 AD2, S_DQ8 AC2, S_DQ9 AC1, S_DQ10 AD1, S_DQ11 AA4, S_DQ12 AA3, S_DQ13 Y4, S_DQ14 Y3, S_DQ15 W4, S_DQ16 G4, S_DQ17 G6, S_DQ18 G5, S_DQ19 E6, S_DQ20 F5, S_DQ21 D5, S_DQ22 E5, S_DQ23 D6, S_DQ24 F4, S_DQ25 F3, S_DQ26 E3, S_DQ27 E4, S_DQ28 D4, S_DQ29 B5, S_DQ30 C5, S_DQ31 C4

10 SD_DQ[0.63]

S_DQ32 AA6, S_DQ33 AC5, S_DQ34 AD5, S_DQ35 AD4, S_DQ36 AE3, S_DQ37 AE5, S_DQ38 AE4, S_DQ39 AE2, S_DQ40 AB2, S_DQ41 AB1, S_DQ42 AA2, S_DQ43 AA1, S_DQ44 Y2, S_DQ45 Y1, S_DQ46 W2, S_DQ47 W1, S_DQ48 F1, S_DQ49 F2, S_DQ50 E1, S_DQ51 D1, S_DQ52 E2, S_DQ53 C1, S_DQ54 D2, S_DQ55 C2, S_DQ56 A5, S_DQ57 A3, S_DQ58 B4, S_DQ59 A2, S_DQ60 A4, S_DQ61 B3, S_DQ62 B2, S_DQ63 B1

SD_DQ[0.63] 10

TM3200/TM5400

DI_Interface Section

10 SD_A[0..12]

S_A0 P3, S_A1 N4, S_A2 V5, S_A3 P4, S_A4 N5, S_A5 M1, S_A6 P1, S_A7 N1, S_A8 P2, S_A9 N2, S_A10 M2, S_A11 K1, S_A12 K2

S_CLK0 M3, S_CLK1 M4, S_CLK2 M5, S_CLK3 L4, S_CLK4 L5, S_CLK5 K3, S_CLK6 K4, S_CLK7 K5, S_CKE0 J2, S_CKE1 J1, TM5400_RES/S_CKE2 J4, TM5400_RES/S_CKE3 J5

SD_CLK0 10, SD_CLK1 10, SD_CLK2 10, SD_CLK3 10, SD_CKE0 10, SD_CKE1 10

TM3200
Note:
To remain compatible with TM5400, use S_CLK[3:0] and S_CKE#[1:0] signals only and leave S_CLK[7:4] and S_CKE#[3:2] unconnected

TM5400_SNIFF_VDD25/S_CS7#, TM5400_RES/S_CS6#, TM5400_SNIFF_VDD33/S_CS5#, TM5400_SNIFF_GND/S_CS4#

S_DQM7 H1, S_DQM6 H2, S_DQM5 U2, S_DQM4 U5, S_DQM3 H3, S_DQM2 H4, S_DQM1 U4, S_DQM0 U1

TM3200_5400

S_CS2# T2, S_CS1# T3, S_CS0# T4

S_WE# P5, S_SDATA B6, S_SCLK A6, S_RAS# R5, S_CLKOUT V6, S_CLKIN AB6, S_CAS# V4, S_BA1 L1, S_BA0 L2

V_3S — R7 1.2K — R8 1.2K

SD_BA0 10, SD_BA1 10, SD_CAS# 10

Resistor should go close to processor at S_CLKOUT. Trace length should be calculated to be equal to the average of all the data line trace lengths.

CLK_S_IN — R9 33 — CLK_S_OUT

SD_RAS# 10

TDM_SCL 4,11, TDM_SDA 4,11

SD_WE# 10

SD_CS#0, SD_CS#1, SD_CS#2, SD_CS#3

SD_CS#0 10, SD_CS#1 10, SD_CS#2 10, SD_CS#3 10

TM3200
Note:
To remain compatible with TM5400, use SD_CS#[0:3] and leave SD_CS#[4:7] unconnected.

SD_DQMB0, SD_DQMB1, SD_DQMB2, SD_DQMB3, SD_DQMB4, SD_DQMB5, SD_DQMB6, SD_DQMB7

TP12, TP13, TP14

TM5400 SNIFF GND TEST POINT
TM5400 SNIFF VDD 3.3 TEST POINT
TM5400 SNIFF VDD 2.5 TEST POINT

USE test points only for TM5400. Make trace low impedance to test point.

SD_DQMB[0..7] 10

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TM5400 Note:

V_25S — FERR# needs to be pulled up to V_25S only on TM5400

R138 8.2K

JTAG signals connect to Debugger

11 TDM_TRST#
11 TDM_TMS
11 TDM_TCK
11 TDM_TDI
11 TDM_TDO

R11 10K
R12 4.7K
R10 4.7K
GND

RN1A 4.7K
RN1B 4.7K
RN1C 4.7K
RN1D 4.7K
RN4A 4.7K
RN4B 4.7K
RN4C 4.7K
RN4D 4.7K

TMRSVD6
TMRSVD5
TMRSVD4
TMRSVD3
TMRSVD2
TMRSVD1
TMRSVD0
TMRSVD7
TMRSVD8

RN71C 10K
RN71D 10K
RN70B 10K
RN70C 10K
RN70D 10K
RN71A 10K
RN71B 10K

EPROMA[2:0] is used if BIOS ROM is to be used as CMS ROM also. Used as ROM bank selects. Needs pull-up to V_3S so lines are stable when processor is in deep sleep (outputs are tristated).

R13 2.7K
R14 2.7K
R15 2.7K
R16 2.7K
R17 2.7K
R18 2.7K
R19 2.7K
R20 2.7K
R21 2.7K
R22 8.2K

U1C

JTAG
RESERVED
TM3200/TM5400
PCI_Interface Section
RFU
TM3200_5400

EPROMA0
EPROMA1
EPROMA2
FERR#
IGNNE#
INIT#
INTR
NMI
SMI#
P_TRDY#
P_STOP#
P_SERR#
P_PCI_RST#
P_PERR#
P_PCLK
P_PAR
P_LOCK#
P_IRDY#
P_FRAME#
P_DEVSEL#
P_CLKRUN#
P_GNT5#
P_GNT4#
P_GNT3#
P_GNT2#
P_GNT1#
P_GNT0#
P_REQ5#
P_REQ4#
P_REQ3#
P_REQ2#
P_REQ1#
P_REQ0#
P_C/BE3#
P_C/BE2#
P_C/BE1#
P_C/BE0#
P_HLDA#
P_HOLD#
THRMD
THRMD#

P_AD[0..31]

TP1
CPU_INIT# 17,18
CPU_INTR 17,18
SMI# 17,18
CLK_PCI_NB 16

All PCI signals connect outside of core. Make sure that all PCI signals are powered off, grounded, or disconnected during power down states where power is removed from processor. Also, when processor is in deep sleep, all outputs are tristated so ensure that inputs on other devices are properly pulled up or down, specifically P_GNT[].

P_GNT#[0..5]

P_CBE#[0..3] 17,18
P_ISA_GNT# 17,18

ROUTE AS DIFFERENTIAL PAIR

C3 1000pF
C4 1000pF

U55 Temp Sensor
DXP
DXN
ADD1
ADD0
SMBCLK
SMBDATA
ALERT
VCC
STBY
GND
NC1
NC2
NC3
NC4
NC5
MAX1617

ATF_SCL
ATF_SDA
ALERT#
ATF_INT# 17,18

TM5400_VRDA4 12,13
TM5400_VRDA3 12,13
TM5400_VRDA2 12,13
TM5400_VRDA1 12,13
TM5400_VRDA0 12,13

TMRSVD9
TMRSVD10
TMRSVD11
R23 4.7K
R24 4.7K
TP2
TP15 TM5400 SNIFF VDDCORE

Test point is only used for TM5400. Make low impedance trace to test point.

RN5A 8.2K
RN5B 8.2K
RN5C 8.2K
RN5D 8.2K

R149 0 NI
U3 NC7SZD384
+5V
C5 0.1uF 0603

Quickswitch is used only with TM3200 Reserved I/O pin to disconnect ISA_REQ# signal from TM3200 during power down states. Install bypass resistor for TM5400

P_ISA_REQ# 17,18

RN6A 2.7K
RN6B 2.7K
RN6C 2.7K
RN6D 2.7K
RN7A 2.7K
RN7B 2.7K
RN7C 2.7K
RN7D 2.7K

P_REQ#[0..5] 17,18

OPTIONAL
Do NOT use in production!

D1 BAW56
R26 10K
C6 0.1uF
R27 0 NI
R28 0 NI

U4 QS3257

8,16,17,19 SMBUS_SCL
3,11 TDM_SCL
8,16,17,19 SMBUS_SDA
3,11 TDM_SDA
11 ATF_INTCPT
R29 4.7K

This block allows the temp sensor I2C to be intercepted and read from a debugger.

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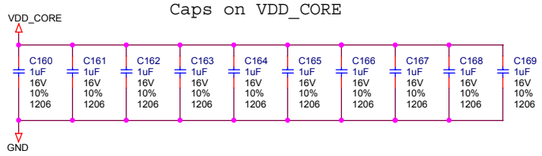
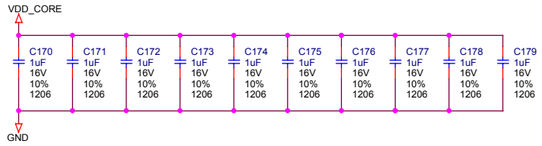
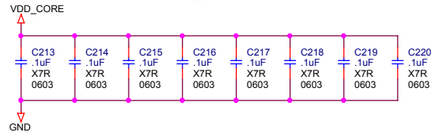
1uF X7R caps are recommended on all supplies. Use at least recommended number shown here. 1uF caps are also available in 0805. Depending on power supply proximity, bulk capacitors may also be needed near the processor.

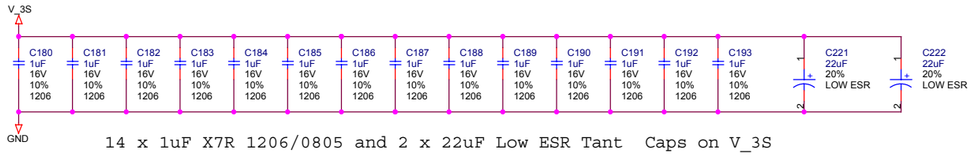
20 x 1uF X7R 1206/0805 Caps on VDD_CORE



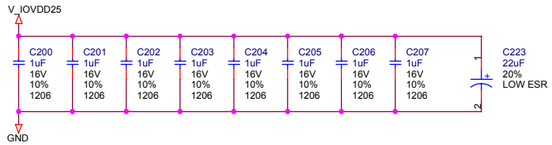


8 x .1uF X7R 0603 Caps on VDD_CORE

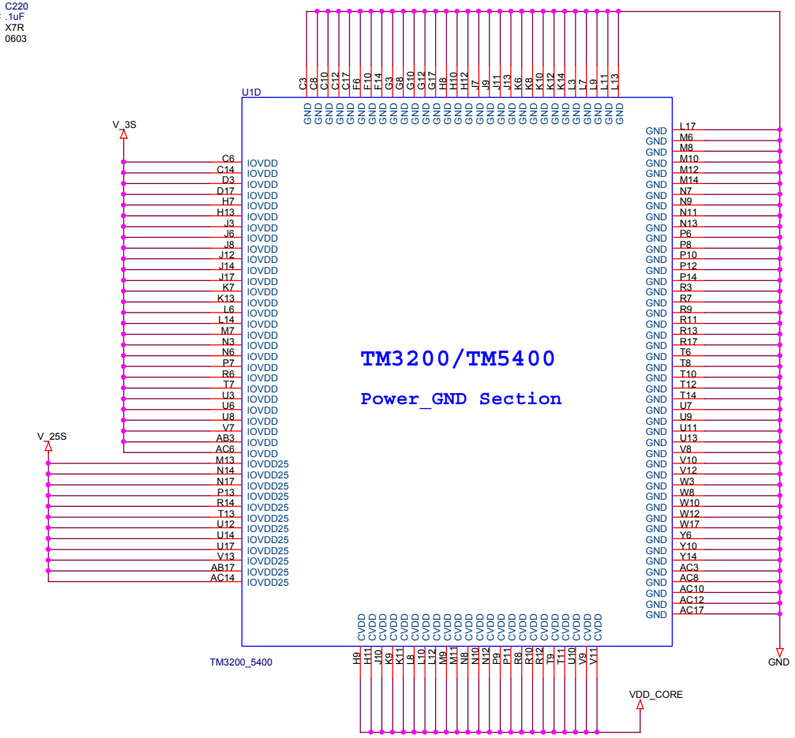




14 x 1uF X7R 1206/0805 and 2 x 22uF Low ESR Tant Caps on V_3S



8 x 1uF X7R 1206/0805 and 1 x 22uF Low ESR Tant Caps on V_3S



TM3200/TM5400

Power_GND Section

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Project:	TM3200/5400 Reference Schematics
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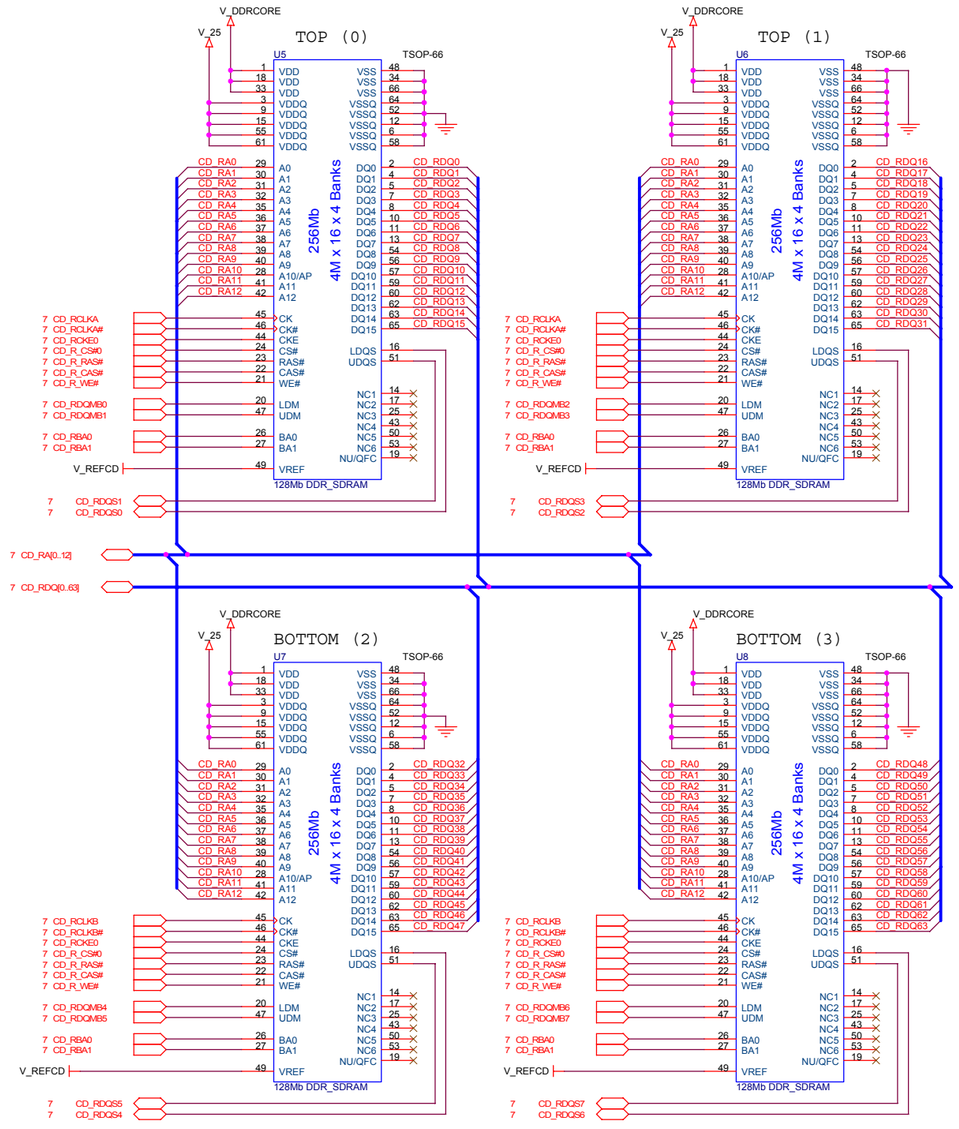
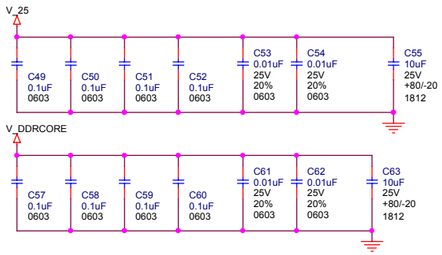
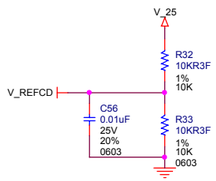
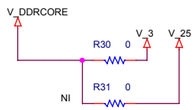
BANK 0

256Mb pinout shown.
Stuff options:
NI, 64Mb, 128Mb, 256Mb



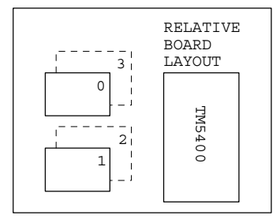






FOR DDR CORE VOLTAGE INSTALL APPROPRIATE RESISTOR

See design guide for more layout info



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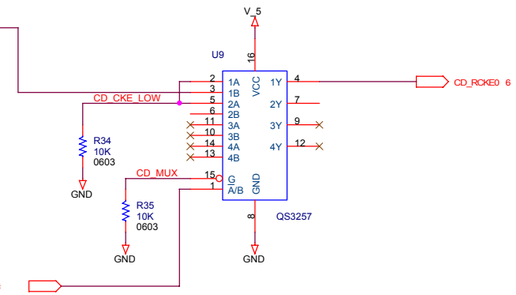
2 CD_DQ00	RN8A	1	8	33	CD_RDQ00 6	2 CD_A0	RN9A	8	1	SRN33-1	CD_RA0 6
2 CD_DQ01	RN8B	2	7	33	CD_RDQ01 6	2 CD_A1	RN9B	7	2	SRN33-1	CD_RA1 6
2 CD_DQ02	RN8C	3	6	33	CD_RDQ02 6	2 CD_A2	RN9C	6	3	SRN33-1	CD_RA2 6
2 CD_DQ03	RN8D	4	5	33	CD_RDQ03 6	2 CD_A3	RN9D	5	4	SRN33-1	CD_RA3 6
2 CD_DQ04	RN10A	1	8	33	CD_RDQ04 6	2 CD_A4	RN11A	1	8	SRN33-1	CD_RA4 6
2 CD_DQ05	RN10B	2	7	33	CD_RDQ05 6	2 CD_A5	RN11B	2	7	SRN33-1	CD_RA5 6
2 CD_DQ06	RN10C	3	6	33	CD_RDQ06 6	2 CD_A6	RN11C	3	6	SRN33-1	CD_RA6 6
2 CD_DQ07	RN10D	4	5	33	CD_RDQ07 6	2 CD_A7	RN11D	4	5	SRN33-1	CD_RA7 6
2 CD_DQ08	RN12A	1	8	33	CD_RDQ08 6	2 CD_A8	RN13A	1	8	SRN33-1	CD_RA8 6
2 CD_DQ09	RN12B	2	7	33	CD_RDQ09 6	2 CD_A9	RN13B	2	7	SRN33-1	CD_RA9 6
2 CD_DQ10	RN12C	3	6	33	CD_RDQ10 6	2 CD_A10	RN13C	6	3	SRN33-1	CD_RA10 6
2 CD_DQ11	RN12D	4	5	33	CD_RDQ11 6	2 CD_A11	RN13D	4	5	SRN33-1	CD_RA11 6
2 CD_DQ12	RN14A	1	8	33	CD_RDQ12 6	2 CD_A12	RN15A	1	8	SRN33-1	CD_RA12 6
2 CD_DQ13	RN14B	2	7	33	CD_RDQ13 6						
2 CD_DQ14	RN14C	3	6	33	CD_RDQ14 6						
2 CD_DQ15	RN14D	4	5	33	CD_RDQ15 6	2 CD_BA0	RN15B	7	2	SRN33-1	CD_RBA0 6
						2 CD_BA1	RN15C	6	3	SRN33-1	CD_RBA1 6
2 CD_DQ16	RN16A	1	8	33	CD_RDQ16 6						
2 CD_DQ17	RN16B	2	7	33	CD_RDQ17 6						
2 CD_DQ18	RN16C	3	6	33	CD_RDQ18 6						
2 CD_DQ19	RN16D	4	5	33	CD_RDQ19 6	2 CD_RAS#	RN15D	5	4	SRN33-1	CD_R_RAS# 6
						2 CD_CAS#	RN17A	8	1	SRN33-1	CD_R_CAS# 6
2 CD_DQ20	RN18A	1	8	33	CD_RDQ20 6	2 CD_WE#	RN17B	7	2	SRN33-1	CD_R_WE# 6
2 CD_DQ21	RN18B	2	7	33	CD_RDQ21 6						
2 CD_DQ22	RN18C	3	6	33	CD_RDQ22 6	2 CD_CS#0	RN17C	6	3	SRN33-1	CD_R_CS#0 6
2 CD_DQ23	RN18D	4	5	33	CD_RDQ23 6	2 CD_CKE0	RN17D	5	4	SRN33-1	
2 CD_DQ24	RN19A	1	8	33	CD_RDQ24 6						
2 CD_DQ25	RN19B	2	7	33	CD_RDQ25 6						
2 CD_DQ26	RN19C	3	6	33	CD_RDQ26 6						
2 CD_DQ27	RN19D	4	5	33	CD_RDQ27 6						
2 CD_DQ28	RN20A	1	8	33	CD_RDQ28 6						
2 CD_DQ29	RN20B	2	7	33	CD_RDQ29 6						
2 CD_DQ30	RN20C	3	6	33	CD_RDQ30 6						
2 CD_DQ31	RN20D	4	5	33	CD_RDQ31 6						
2 CD_DQ32	RN21A	1	8	33	CD_RDQ32 6	2 CD_DQS0	RN22A	1	8	SRN33-1	CD_RDQS0 6
2 CD_DQ33	RN21B	2	7	33	CD_RDQ33 6	2 CD_DQS1	RN22B	2	7	SRN33-1	CD_RDQS1 6
2 CD_DQ34	RN21C	3	6	33	CD_RDQ34 6	2 CD_DQS2	RN22C	3	6	SRN33-1	CD_RDQS2 6
2 CD_DQ35	RN21D	4	5	33	CD_RDQ35 6	2 CD_DQS3	RN22D	5	4	SRN33-1	CD_RDQS3 6
2 CD_DQ36	RN23A	1	8	33	CD_RDQ36 6	2 CD_DQS4	RN24A	1	8	SRN33-1	CD_RDQS4 6
2 CD_DQ37	RN23B	2	7	33	CD_RDQ37 6	2 CD_DQS5	RN24B	2	7	SRN33-1	CD_RDQS5 6
2 CD_DQ38	RN23C	3	6	33	CD_RDQ38 6	2 CD_DQS6	RN24C	3	6	SRN33-1	CD_RDQS6 6
2 CD_DQ39	RN23D	4	5	33	CD_RDQ39 6	2 CD_DQS7	RN24D	4	5	SRN33-1	CD_RDQS7 6
2 CD_DQ40	RN25A	1	8	33	CD_RDQ40 6	2 CD_DQMB0	RN26A	1	8	SRN33-1	CD_RDQMB0 6
2 CD_DQ41	RN25B	2	7	33	CD_RDQ41 6	2 CD_DQMB1	RN26B	2	7	SRN33-1	CD_RDQMB1 6
2 CD_DQ42	RN25C	3	6	33	CD_RDQ42 6	2 CD_DQMB2	RN26C	3	6	SRN33-1	CD_RDQMB2 6
2 CD_DQ43	RN25D	4	5	33	CD_RDQ43 6	2 CD_DQMB3	RN26D	4	5	SRN33-1	CD_RDQMB3 6
2 CD_DQ44	RN27A	1	8	33	CD_RDQ44 6	2 CD_DQMB4	RN28A	1	8	SRN33-1	CD_RDQMB4 6
2 CD_DQ45	RN27B	2	7	33	CD_RDQ45 6	2 CD_DQMB5	RN28B	2	7	SRN33-1	CD_RDQMB5 6
2 CD_DQ46	RN27C	3	6	33	CD_RDQ46 6	2 CD_DQMB6	RN28C	3	6	SRN33-1	CD_RDQMB6 6
2 CD_DQ47	RN27D	4	5	33	CD_RDQ47 6	2 CD_DQMB7	RN28D	4	5	SRN33-1	CD_RDQMB7 6
2 CD_DQ48	RN29A	1	8	33	CD_RDQ48 6						
2 CD_DQ49	RN29B	2	7	33	CD_RDQ49 6						
2 CD_DQ50	RN29C	3	6	33	CD_RDQ50 6						
2 CD_DQ51	RN29D	4	5	33	CD_RDQ51 6						
2 CD_DQ52	RN30A	1	8	33	CD_RDQ52 6						
2 CD_DQ53	RN30B	2	7	33	CD_RDQ53 6						
2 CD_DQ54	RN30C	3	6	33	CD_RDQ54 6						
2 CD_DQ55	RN30D	4	5	33	CD_RDQ55 6						
2 CD_DQ56	RN31A	1	8	SRN33-1	CD_RDQ56 6						
2 CD_DQ57	RN31B	2	7	SRN33-1	CD_RDQ57 6						
2 CD_DQ58	RN31C	3	6	SRN33-1	CD_RDQ58 6						
2 CD_DQ59	RN31D	4	5	SRN33-1	CD_RDQ59 6						
2 CD_DQ60	RN32C	3	6	SRN33-1	CD_RDQ60 6						
2 CD_DQ61	RN33A	1	8	SRN33-1	CD_RDQ61 6						
2 CD_DQ62	RN33C	3	6	SRN33-1	CD_RDQ62 6						
2 CD_DQ63	RN33D	4	5	SRN33-1	CD_RDQ63 6	2 CD_CLKB#	RN32A	1	8	SRN33-1	CD_RCLKB# 6
						2 CD_CLKB	RN32B	2	7	SRN33-1	CD_RCLKB 6
						2 CD_CLKA#	RN32D	4	5	SRN33-1	CD_RCLKA# 6
						2 CD_CLKA	RN33B	2	7	SRN33-1	CD_RCLKA 6

Use same quickswitch for CD and DI depending on routing.



STR MUX to avoid glitches on CLK ENABLEs during power transitions

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Project: TM3200/5400 Reference Schematics

Title: 012-02 CD Memory Terminations

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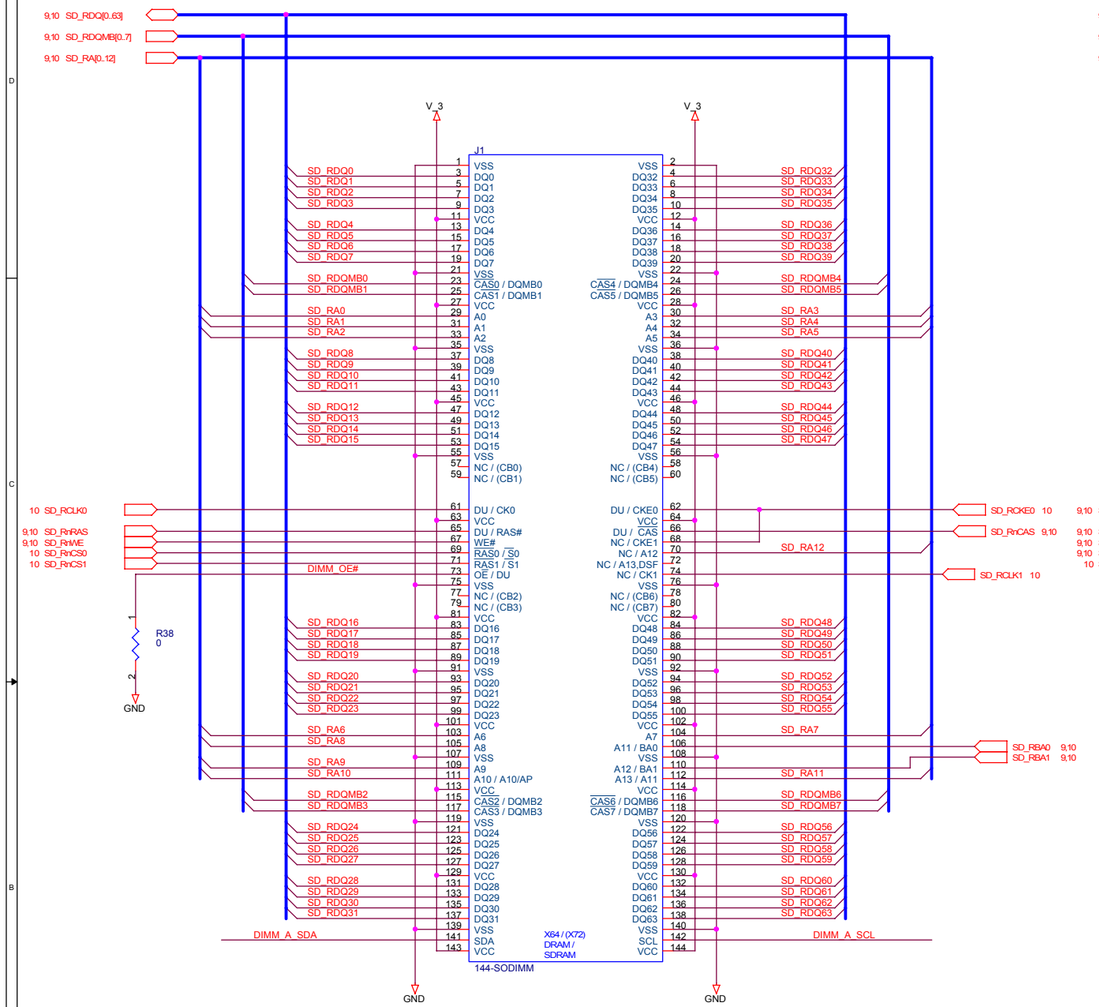
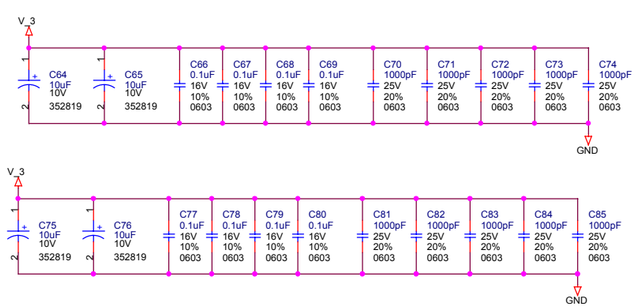
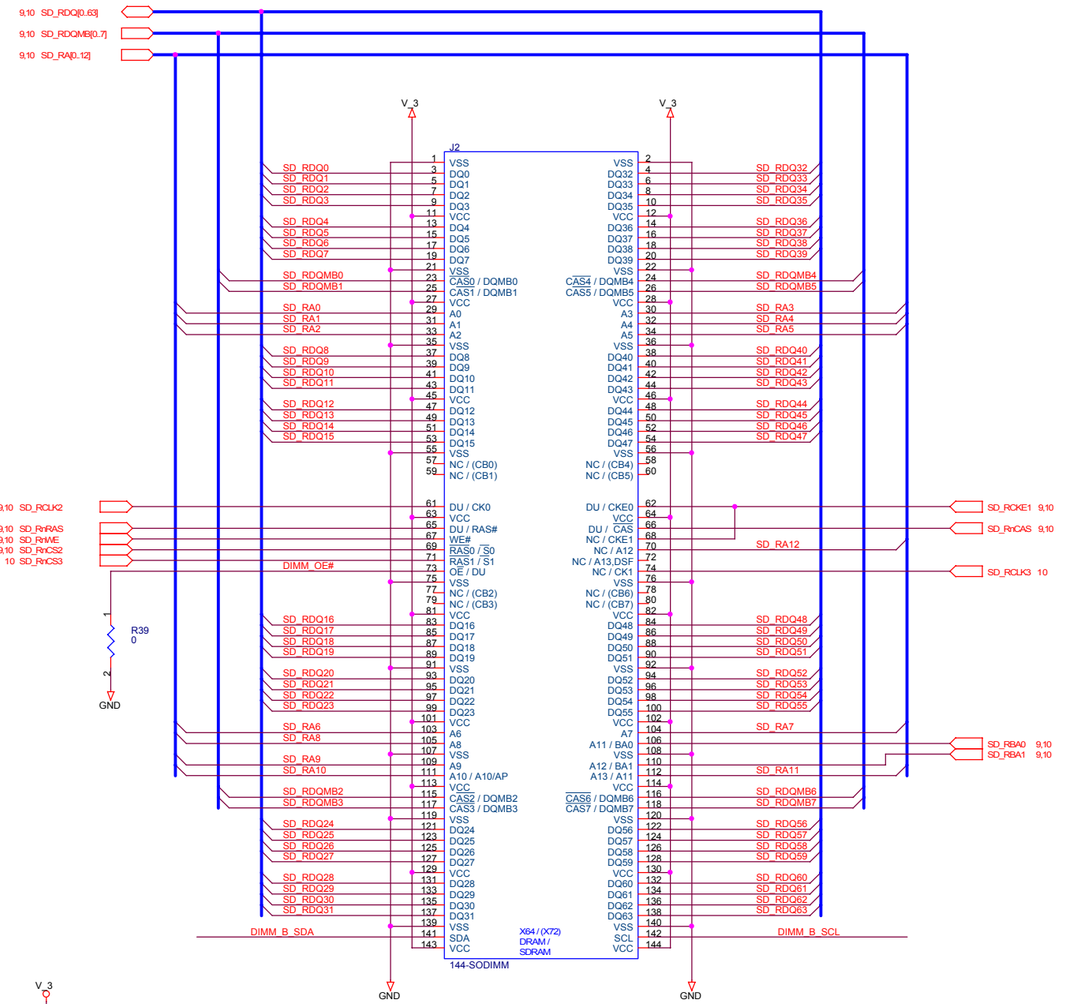
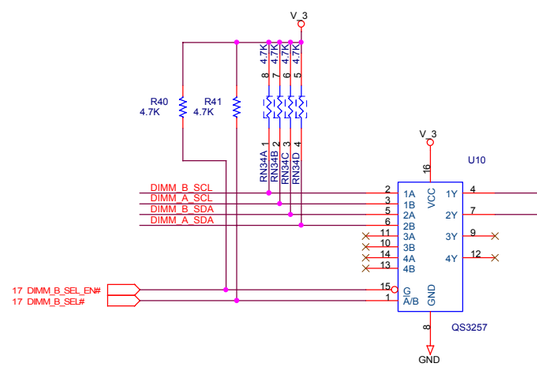


DI PORT SO-DIMM A
BANK 0-1





DI PORT SO-DIMM B
BANK 2-3



Use I2C Serial Presence Detect mux only if SO-DIMM B is used. Mux control (DIMM_B_SEL#) should come from a Southbridge GPIO pin. SMBUS_SDA/SCL I2C lines should come from the Southbridge or other I2C controller.

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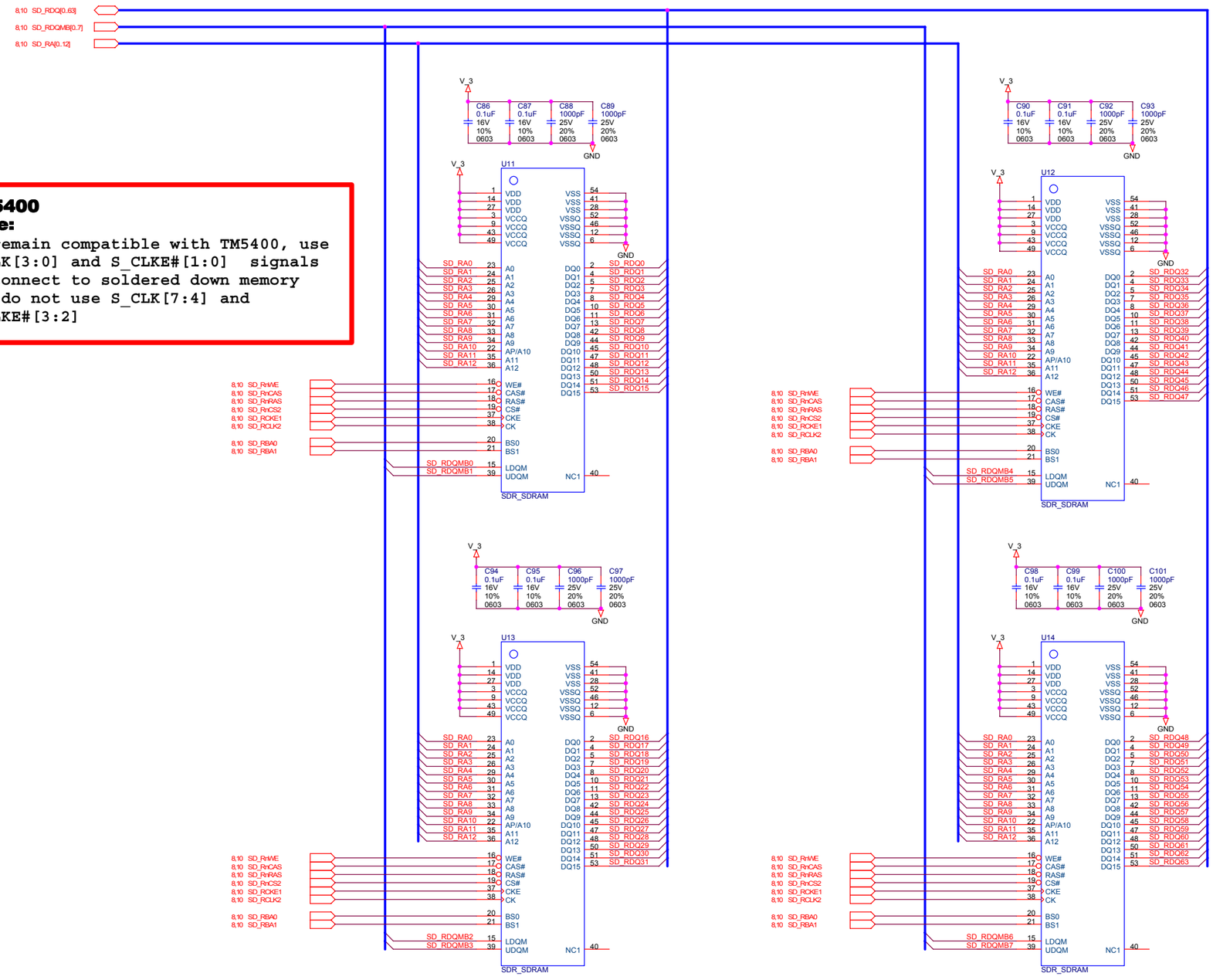
Soldered Down DI PORT MEMORY Soldered Down DI PORT MEMORY

TM5400 Note: It is recommended that either only 2 SO-DIMMS or 1 DIMM and 1 bank of soldered memory be used to remain upward compatible with TM5400 which only has support for 4 banks (2 SO-DIMMs). Use either soldered down memory as shown or SO-DIMM #1

TM5400 Note:
To remain compatible with TM5400, use S_CLK[3:0] and S_CLKE#[1:0] signals to connect to soldered down memory and do not use S_CLK[7:4] and S_CLKE#[3:2]



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Title: 012-04 DI Memory Bank 6
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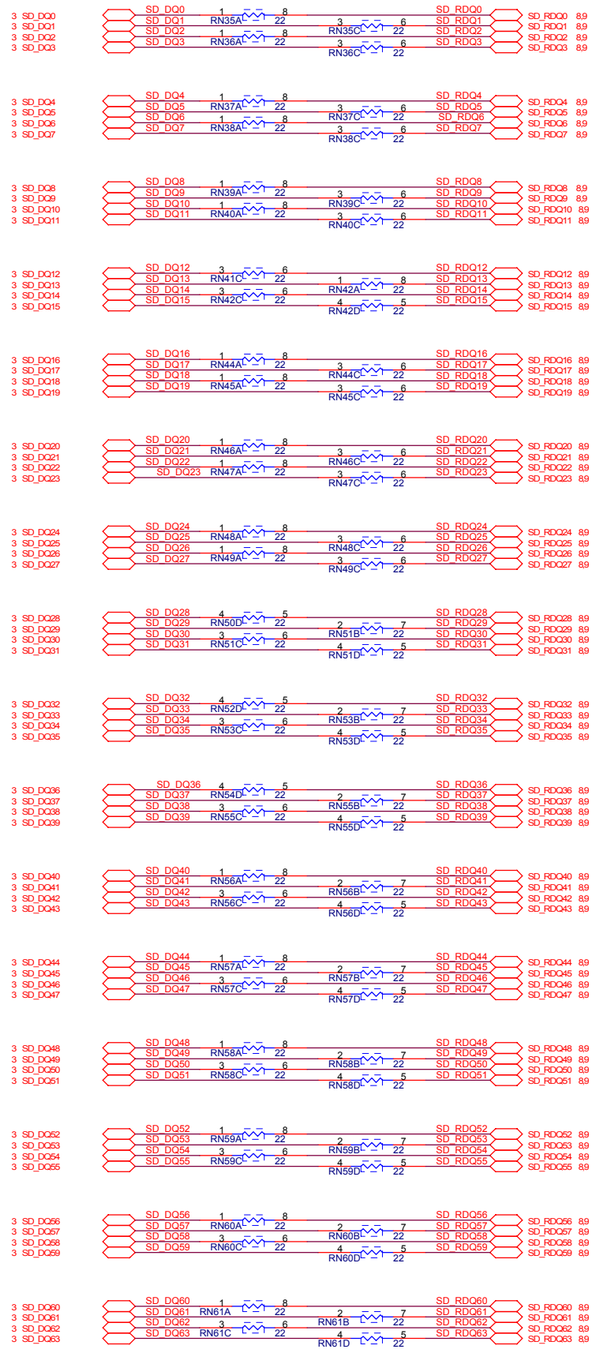
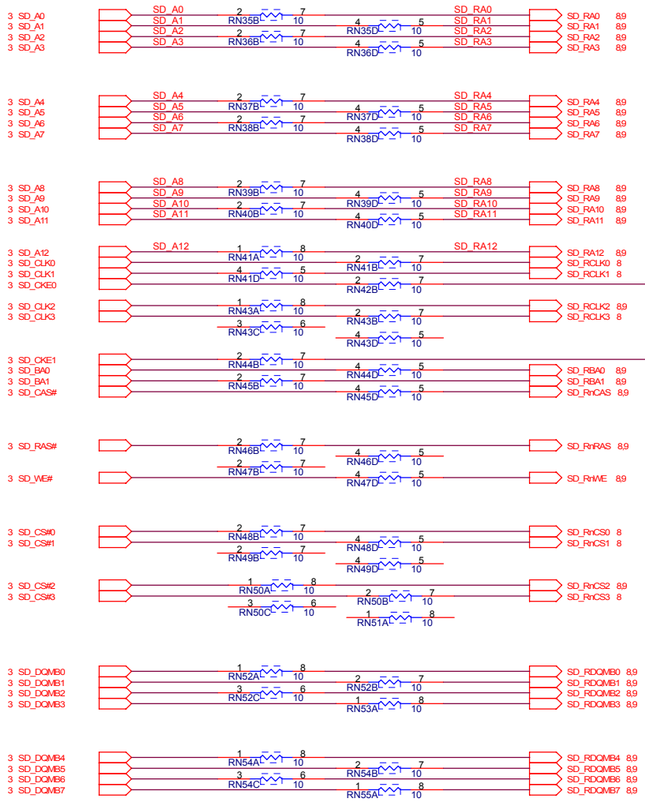
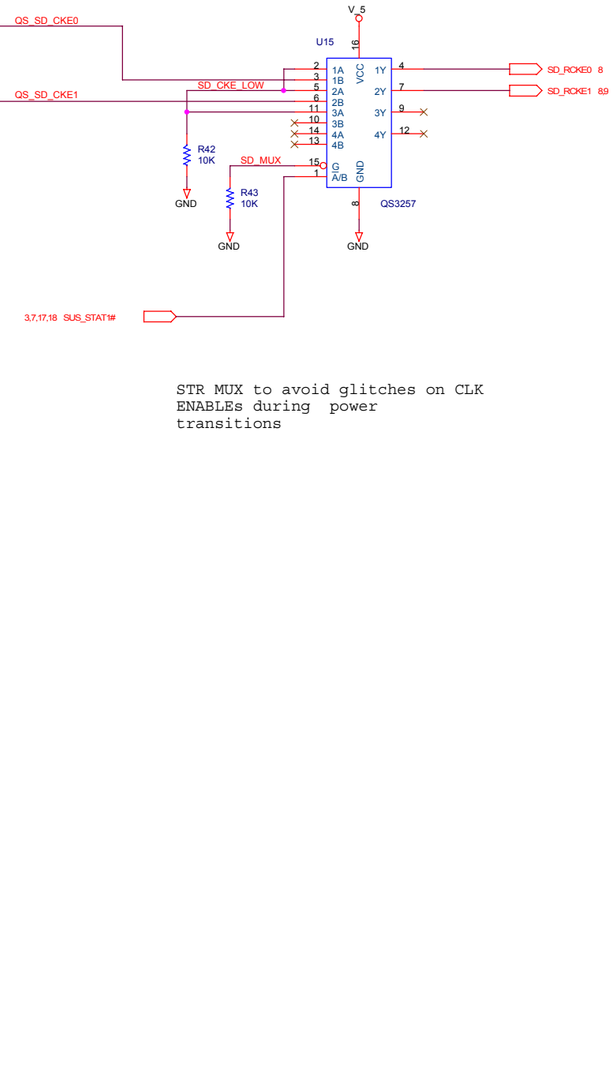
For TM5400 and TM3200, use 10 ohm source termination on DI ADDR/CTRL signals. Use 22 ohm source termination on data signals. PCB line impedance should be 60ohms. All DI traces should be as short as possible (ideally, no more than 2" to the SO-DIMM if possible). Max trace lengths can also be calculated on a per design basis depending on memory speed used.





Use same quickswitch for CD and DI depending on routing.



STR MUX to avoid glitches on CLK ENABLEs during power transitions

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Project: TM3200/5400 Reference Schematics
Title: 012-05 DI Memory Terminations
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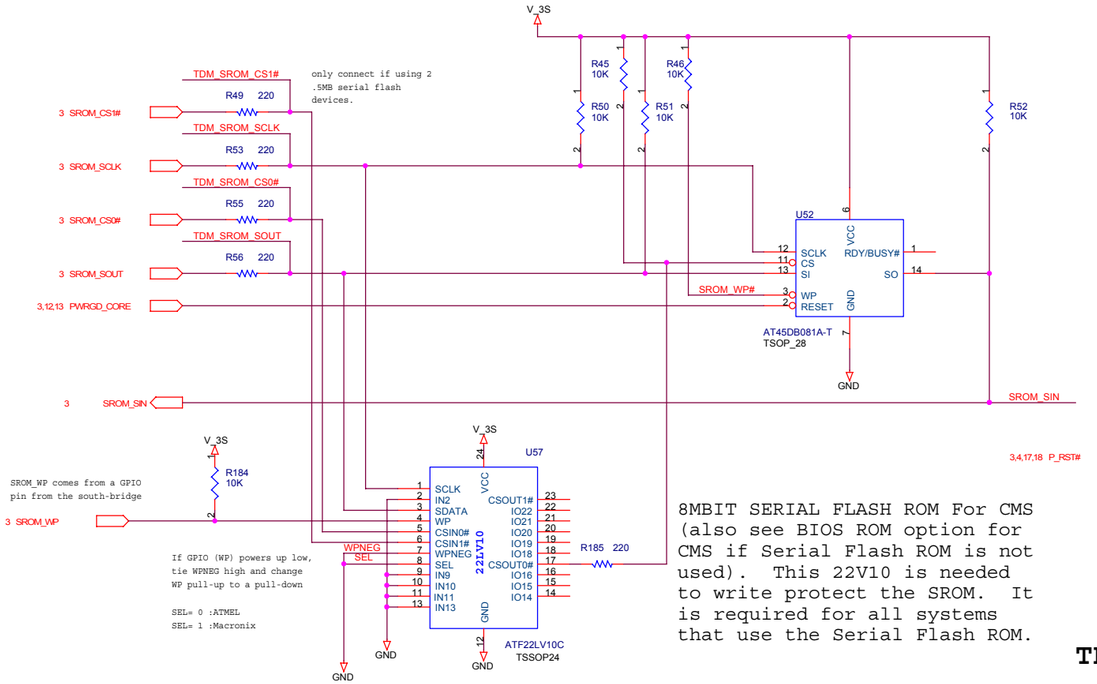
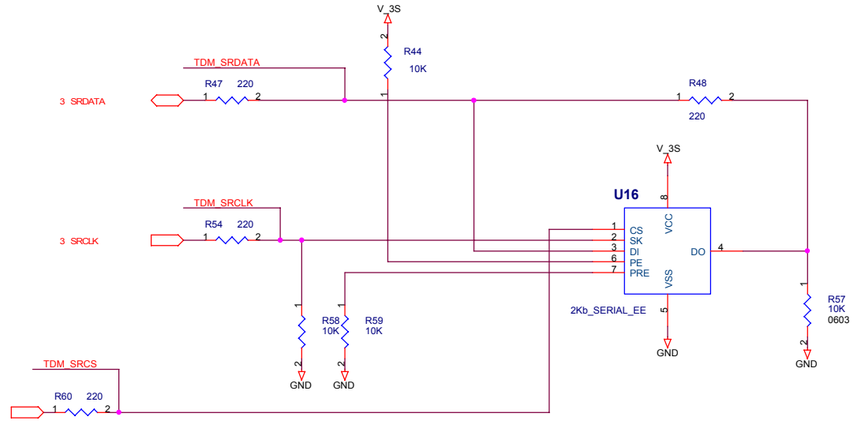


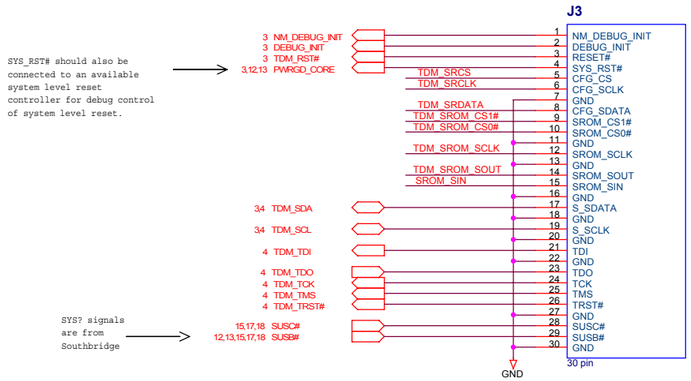
8MBIT SERIAL FLASH ROM For CMS (also see BIOS ROM option for CMS if Serial Flash ROM is not used). This 22V10 is needed to write protect the SROM. It is required for all systems that use the Serial Flash ROM.



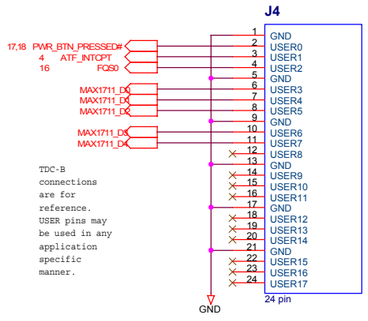
2K-BIT SROM

TRANSMETA DEBUG CONNECTORS

NOTE, pinout depends on type of connector used... Use this pinout for Vertical connector. reverse the pinouts for Right Angle TDC connectors. See TDM Guide for description.



PRIMARY DEBUG CONNECTOR



SECONDARY DEBUG CONNECTOR

Signals on TDC-A are fixed but TDC-B may be used for system specific needs. SEE TDM Guide for further description.

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Project: TM3200/5400 Reference Schematics			
Title: 012-06 ROM & DEBUG			
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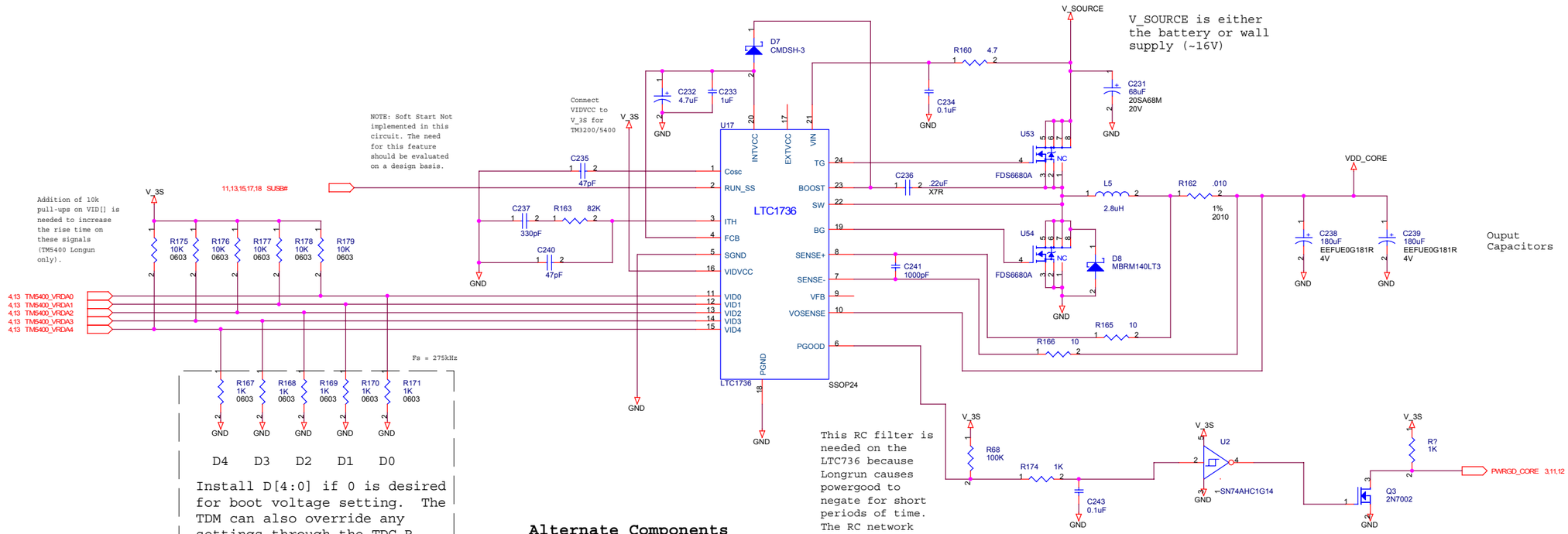
NOTE, Components on this page are not part are the processor CORE but have been included for reference of integral system components that interact closely with the CORE and it's operation.



Alternate Components

Diode (D8)
MBRM140LT3, 1A, 40V, MOTOROLA
MBRS130LT3, 1A, 30V, MOTOROLA
MBRM120LT3, 1A, 20V, MOTOROLA
UPS120, 1A, 20V, MICROSEMI
10BQ040, 1A, 40V, IR

MOSFET H (U53)
IRF7807, IR
Si4884DY, Siliconix
FDS6680A, Fairchild

MOSFET L (U54)
IRF7805, IR
Si4874DY, Siliconix
FDS6680A, Fairchild

Input Capacitor (>5v)
1X Sanyo, 20SA68M, 68uF/20V
3X AVX, TPSE476M020R0150, 47uF/20V
3X Kemet, T495X476K020AS, 47uF/20V
1X MARCON, THCR60E1E226ZT, 22uF/25V
2X TAIYO-YUDEN, TMK432BJ106MM, 10uF/25V

Input Capacitor (5v input)
2X AVX, TPSD107M010R0065, 100uF/10V
3X AVX, TPSD107M010R0100, 100uF/10V
1X Sanyo, 6SV220M, 220uF/10V
1X Sanyo, 10TPB220M, 220uF/6.3V
1X Kemet, T510X337K010AS, 330uF/10V
2X TAIYO-YUDEN, JMK325BJ226MM, 22uF/6.3V

Output Capacitors
2x PANASONIC, EEFUE0G181R, 180uF/4V
4X SANYO POSCAP, 2R5TPC220M, 220uF/2.5V
3X KEMET T510E687K006AS, 680uF/4V
3X CORNELL DUBLIER ESRE221M0EB, 220uF/2.5V

Rs (R162)
LRF2010-R010, 0.010 OHM, 1/2W, IRC
WSL-2010, 0.010 OHM, 1/2W, DALE

Inductor (L5)
D104C 919AS-2R8M, 2.8uH, TOKO
CDRH104R-2R5, 2.5uH, SUMIDA
UP2B-3R3, 3.3uH, Coiltronics
SMP3316-331M, 3.3uH, GOWANDA
IHLP-5050CE-01-3.3uH, 3.3uH, VISHAY

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Project:	TM3200/5400 Reference Schematics
Title:	0XX-01 Power Supply: VDD_CORE
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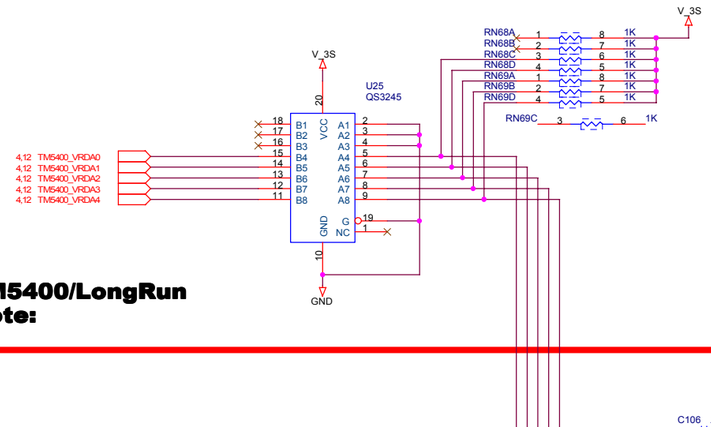
NOTE, Components on this page are not part are the processor CORE but have been included for reference of integral system components that interact closely with the CORE and it's operation.

When using Longrun with the MAX1711, install QS3245 or similar to protect processor VRDA pins since power supply Vcontrol pins are on and pulled up to 5v. (sometimes even when uP is off depending on Vsource for MAX1711). The quickswitch also level translates 3.3V pull-up voltage to 2.5V for TM5400 0.0 (1.0 has 3.3V tolerant inputs, but QS must still be used to protect from 5V. Pull-ups to 3.3V must be 1k to meet timing specs of Vcontrol inputs of MAX1711 and LongRun since VRDA signals are open-drain and rely on pullup for fast transition times.

TM5400/LongRun Note:



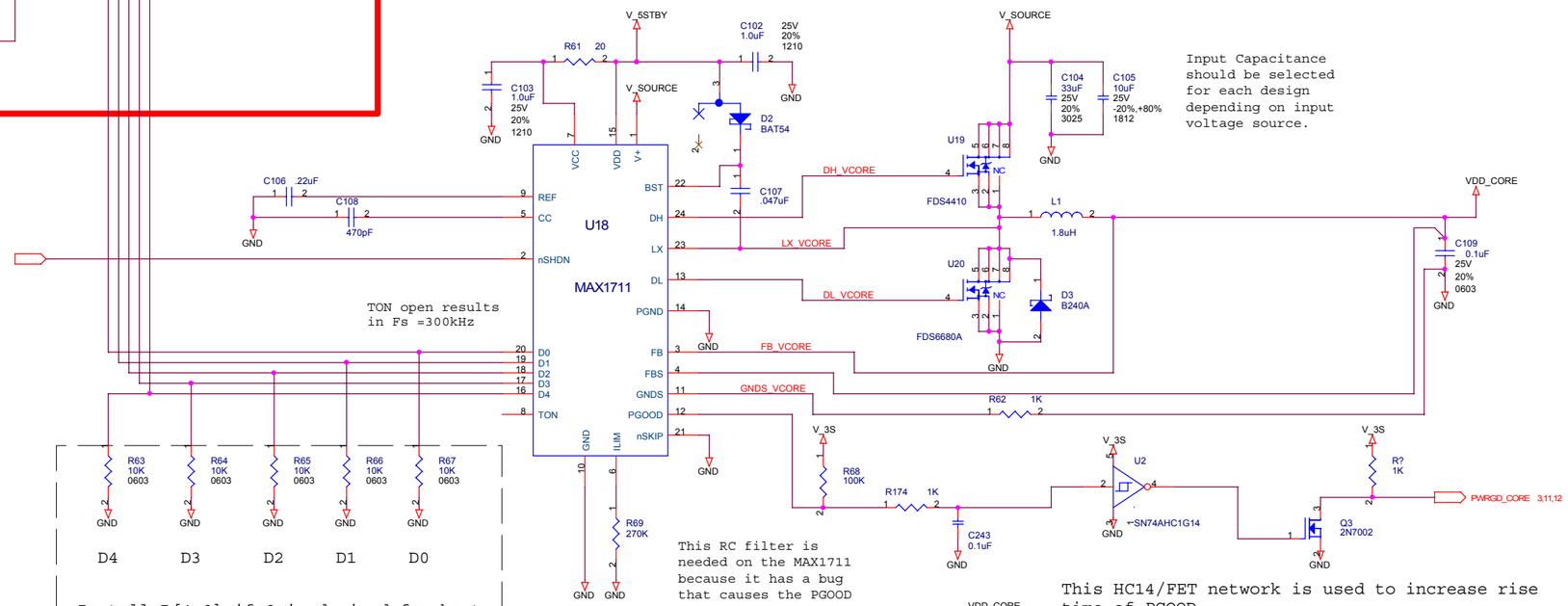
Power Supply specs

- **Vrange: 1.2 - 1.7v**
- **Imax: 7A, 8.1 peak**
- **Vripple: +/- 1%, -5% max droop on 0 to 7A swing**

V_5STBY is 5V that is always powered.

V_SOURCE is either the battery or wall supply (~16V)

Input Capacitance should be selected for each design depending on input voltage source.



TON open results in Fs =300kHz

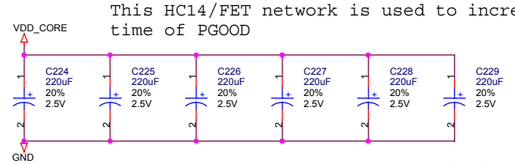
Install D[4:0] if 0 is desired for boot voltage setting (when Longrun is not used). The TDM can also override any settings through the TDC-B.
Avoid D[4:0] = 01111 or 11111

Vout = 2.00V - D[4:0] * .05V

i.e., for D[4:0] = 01001 (9),
Vout = 2-(9*.05) = 1.55

This RC filter is needed on the MAX1711 because it has a bug that causes the PGOOD signal to deasserted during valid voltage transitions caused by Longrun. (use only in a TM5400 system with Longrun).

This HC14/FET network is used to increase rise time of PGOOD



4 to 6 x 220uF BULK TANT Caps on VDD_CORE (4 for <600Mhz operation). 50m ohm ESR or less Output Capacitance. This may change depending on capacitor choices.

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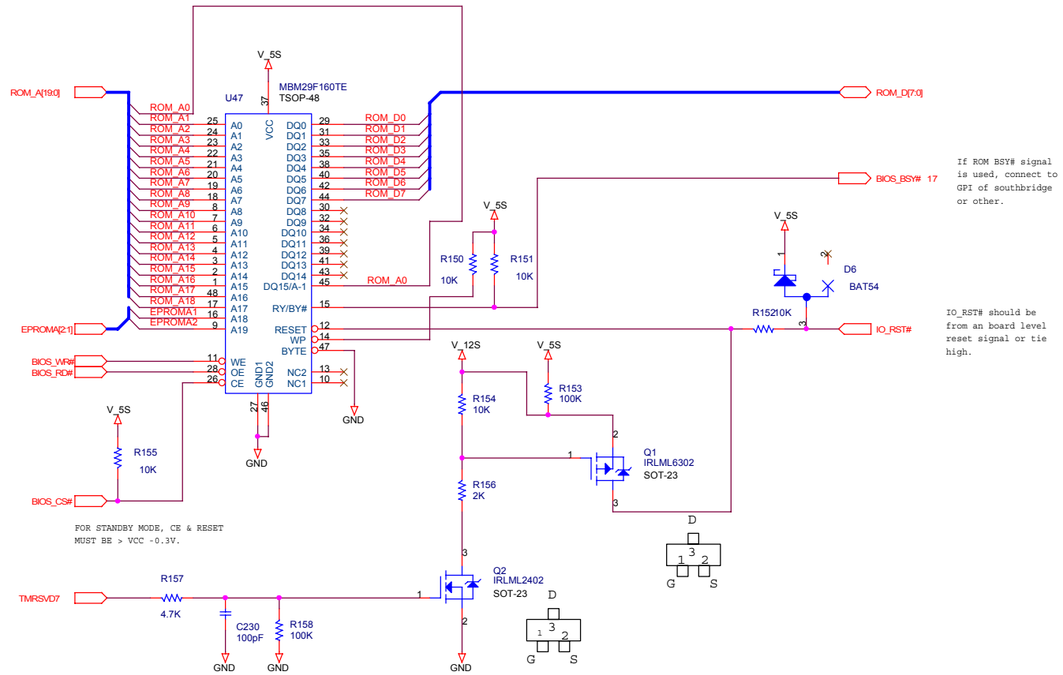
ROM_D[], ROM_A[] and BIOS_XX control signals come from xbus controller.

EPROMA[] signals from the TM3200/5400 are bank selects for the BIOS ROM.



Unprotect is available only on the TM5400.

TM5400: connect to RSVD_G2

TM3200: RSVD_G2 is already used, so eliminate unprotect circuit.

If used only for System BIOS, install 512K (or 256k)
If used for CMS and System Bios, install 2M. In TM5400 systems, the lower 3/4 of the ROM are protected so and unable to be erased (by i.e. an 'erase all' command to the ROM). The unprotect circuit allows CMS to reprogram protected sectors during a CMS upgrade (TM5400 only). The GPIO pin used for 'unprotect' is not availabe on TM3200. Therefore, eliminate the unprotect circuit in TM3200 systems and ensure that only the lower 1/2 of the ROM is protected. This allows a known good copy of CMS to remain protected and allow the unprotected CMS section to be reprogrammed during CMS upgrades. Note how EPROMA[2:1] signals are connected to the 2MB ROM. These signals act as bank selects to select either CMS sectors or BIOS. When CMS has decompressed and is ready to run x86 code, these signals select the highest bank (11) to allow access to the BIOS code.

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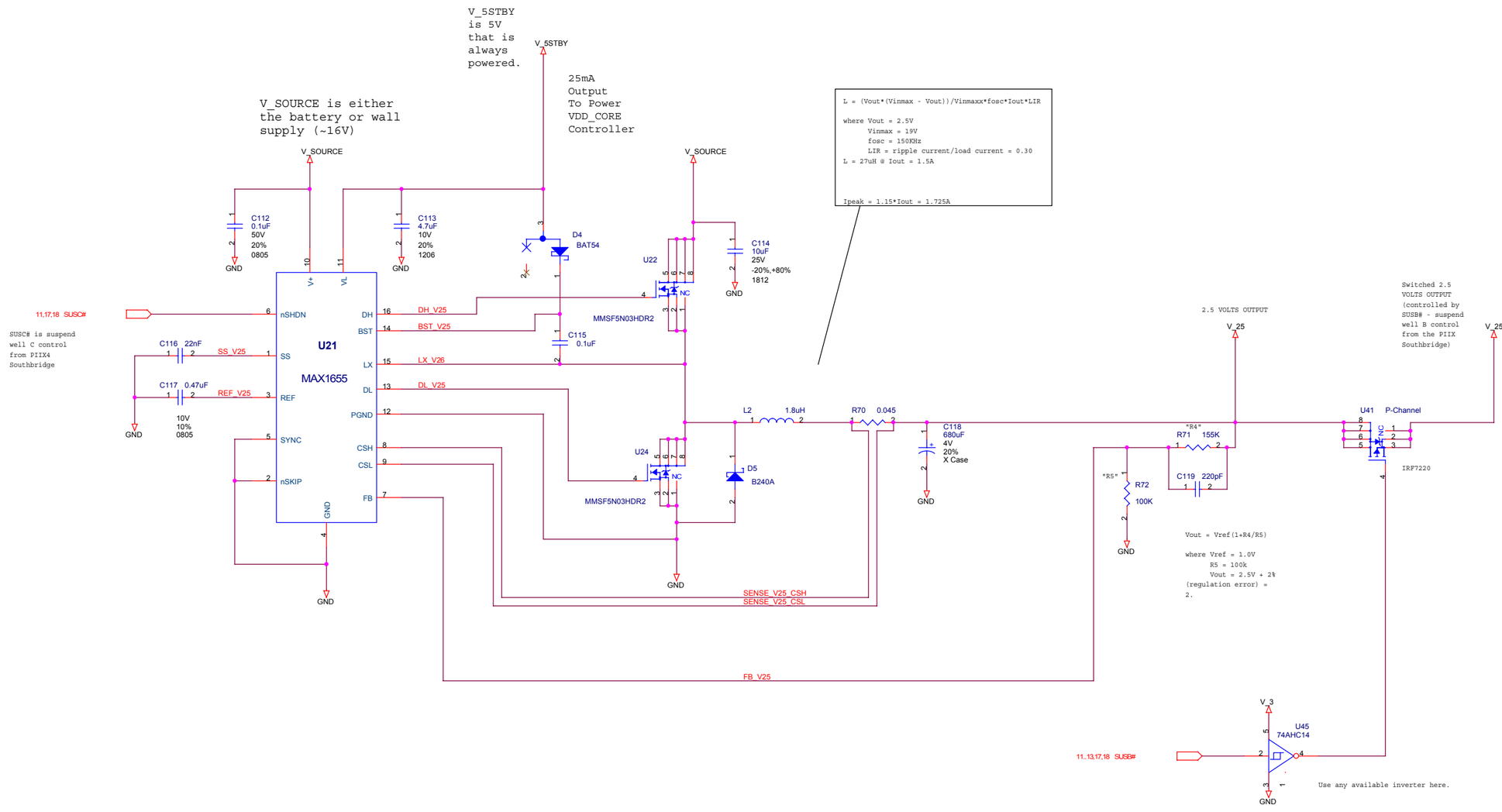

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Project: TM3200/5400 Reference Schematics
Title: 0XX-02 Power Supply: Memory
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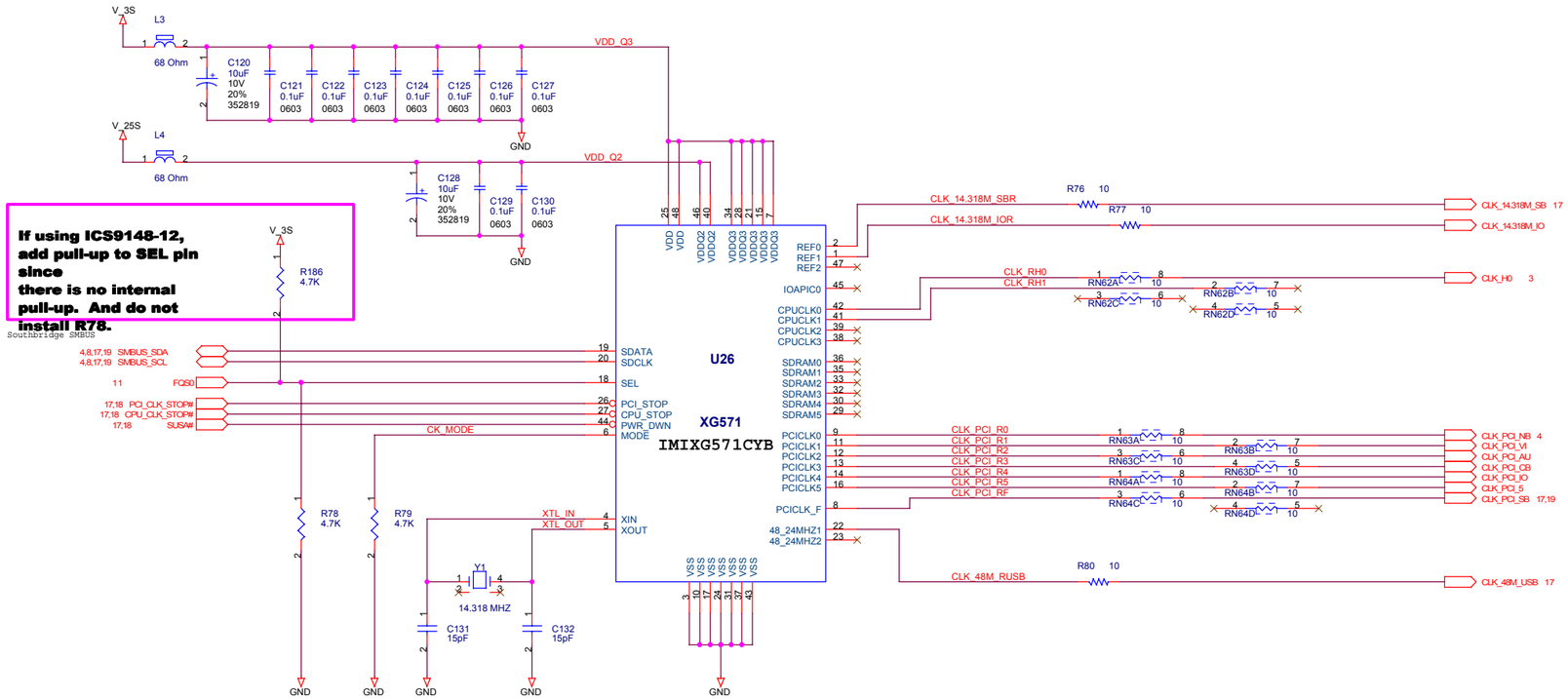

This is for reference. The clock generator is not an integral piece of the core but is shown for reference.

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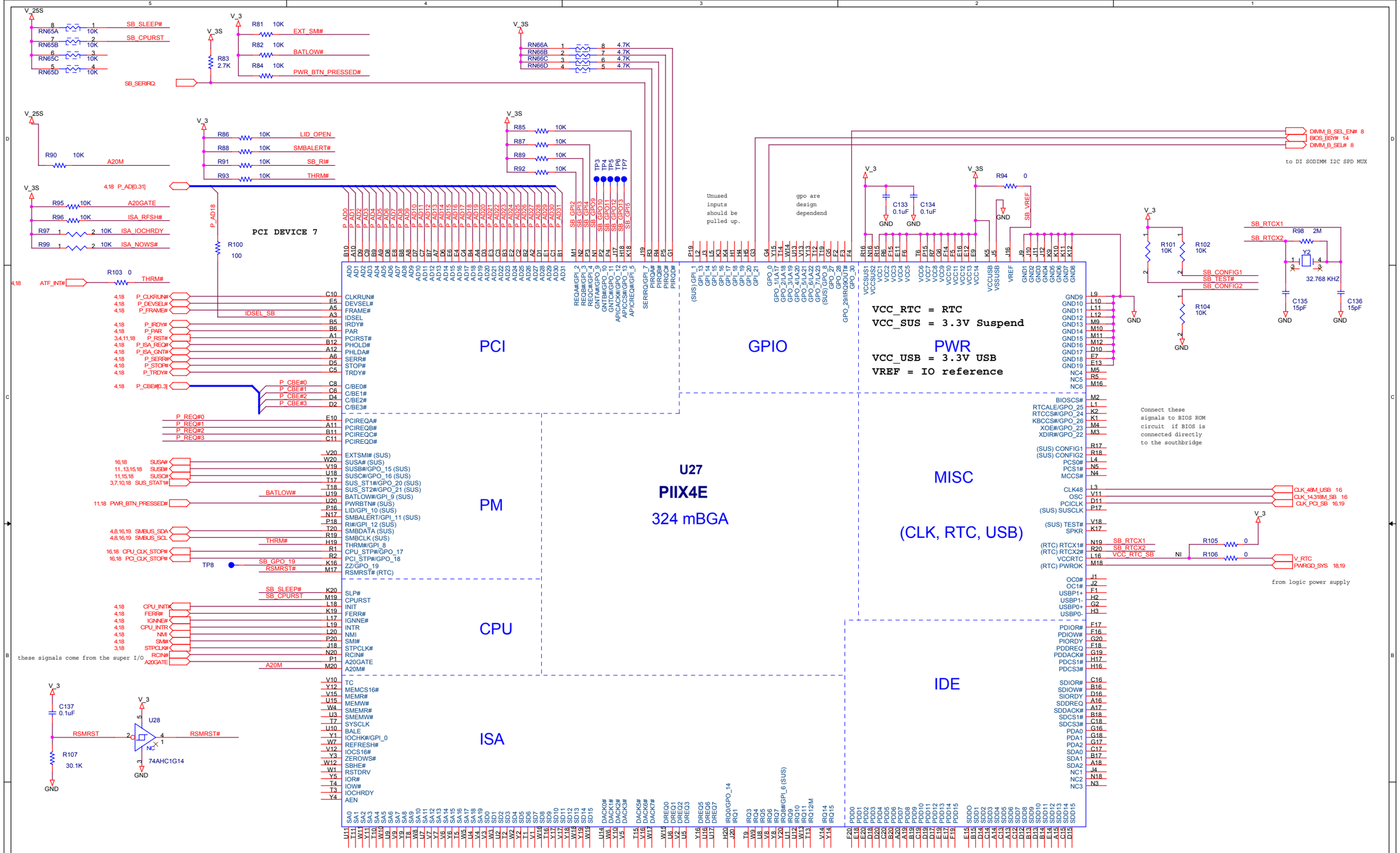

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These pulldowns are needed so PCI_REQ# inputs to the PIIX4 do not float when V_3S is off. If PCI_REQ# is used as a wakeup event during powerdown modes, then these gates and the pullups on P_REQ[] must be powered from V_3 and isolated from the processor when it is powered down.

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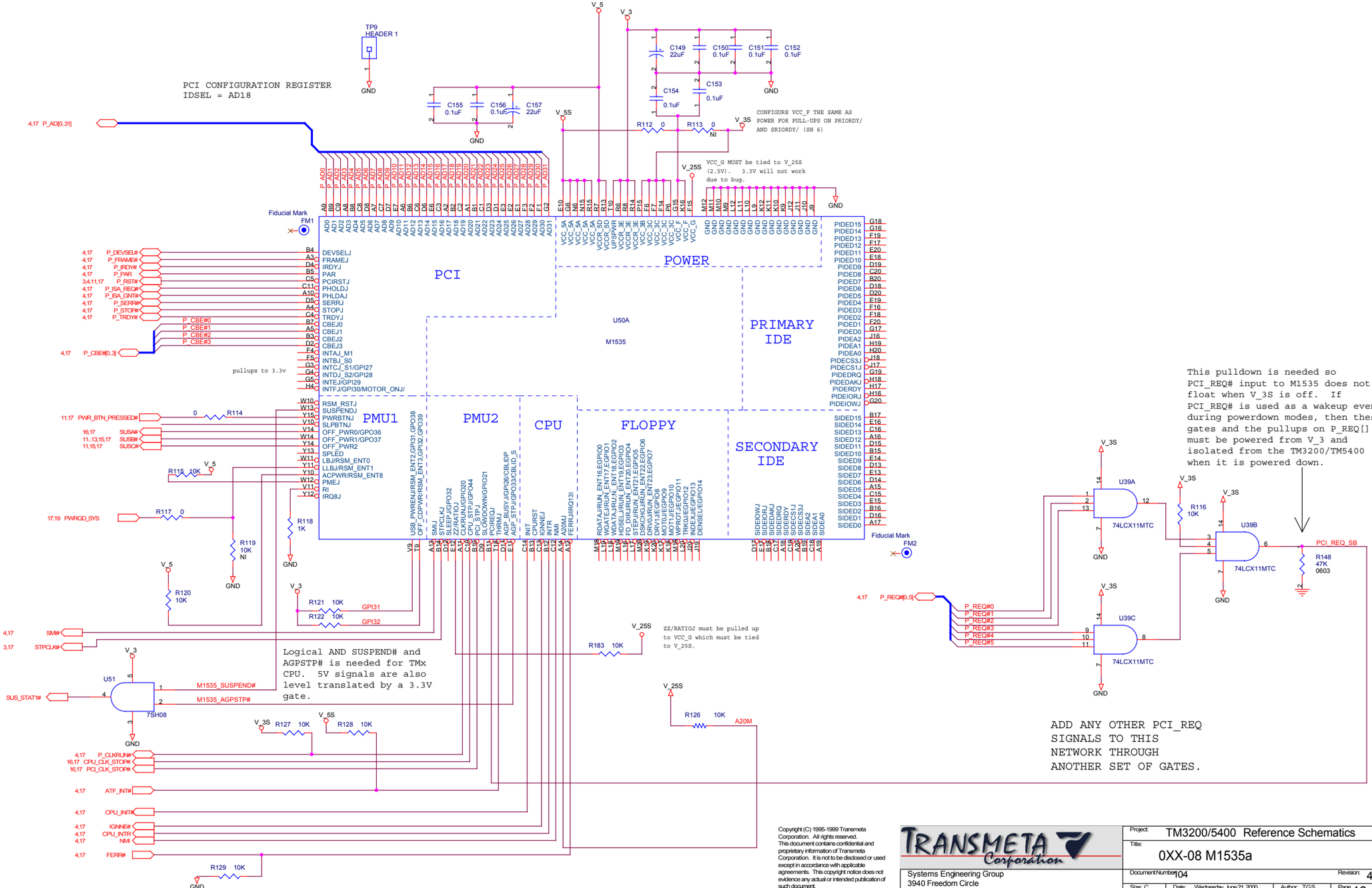

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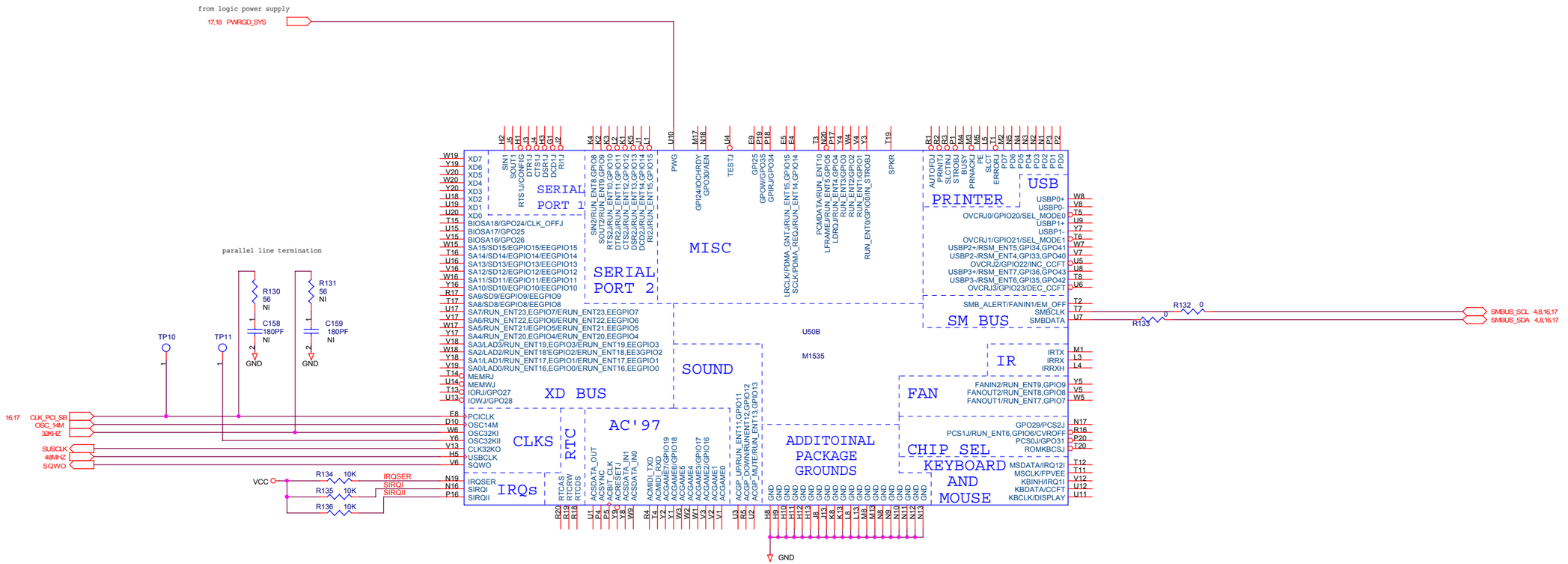

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Project:	TM3200/5400 Reference Schematics
Title:	0XX-09 M1535b
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