4.4 TMS70C02, TMS70C42, and TMS70C82 Specifications (Wide Voltage)

Table 4–20. Absolute Maximum Ratings Over Operating Free-Air Temperature Range for the TMS70C02, TMS70C42, and TMS70C82 (Unless Otherwise Noted)

Supply voltage range, V_{CC}† . . . . . – 0.3V to 7 V
Input voltage range . . . . . – 0.3 V to V_{CC}+0.3 V
Output voltage range . . . . . – 0.3V to V_{CC}+0.3 V
Maximum I/O buffer current (per pin) . . . . . ±10 mA
Storage temperature range . . . . . – 55°C to 150°C
I_{CC}, I_{SS} (maximum into pin 25 or 40) . . . . . ±60 mA
Continuous power dissipation . . . . . 0.5 W

† Unless otherwise noted, all voltages are with respect to V_{SS}.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 4–21. Recommended Operating Conditions for the TMS70C02, TMS70C42, and TMS70C82

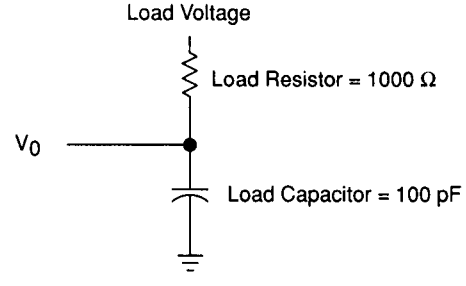
			Min	Nom	Max	Unit
V_{CC}	Supply voltage		2.5		6.0	V
V_{IH}	High-level input voltage	MC and XTAL2 pins, V_{CC} = 2.5 to 6 V	0.8V_{CC}			V
		All other input pins, V_{CC} = 3 to 6 V	0.70V_{CC}			V
		All other input pins, V_{CC} = 2.5 to 3 V	0.75V_{CC}			V
V_{IL}	Low-level input voltage	MC and XTAL2 pins, V_{CC} = 2.5 to 6 V			0.2V_{CC}	V
		All other input pins, V_{CC} = 2.5 to 6 V			0.3V_{CC}	V
T_A	Operating free-air temperature	Commercial (TMS70C42NL)	0		70	°C
		Industrial (TMS70C42NA)	– 40		85	°C

Table 4–22. Electrical Characteristics Over Full Range of Operating Conditions for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Test Conditions	Min	Typ†	Max	Unit
I_I	Input current	MC pin, $V_{IN} = V_{SS}$ or V_{CC} All others, $V_{IN} = V_{SS}$ to V_{CC}		±0.1	±5	µA
C_I	Input capacitance			5		pF
V_{OH}	High-level output voltage ‡	V_{CC} = 2.5 V, I_{OH} = – 50 mA	2.25	2.4		V
		V_{CC} = 4.0 V, I_{OH} = – 0.4 mA	3.2	3.6		V
		V_{CC} = 5.0 V, I_{OH} = – 0.7 mA	3.9	4.5		V
		V_{CC} = 6.0 V, I_{OH} = – 1.0 mA	4.6	5.4		V
V_{OL}	Low-level output voltage ‡	V_{CC} = 2.5 V, I_{OL} = 0.4 mA		0.2	0.35	V
		V_{CC} = 4.0 V, I_{OL} = 1.6 mA		0.4	0.8	V
		V_{CC} = 5.0 V, I_{OL} = 2.5 mA		0.6	1.1	V
		V_{CC} = 6.0 V, I_{OL} = 3.4 mA		0.8	1.4	V
I_{OH}	Output source current	V_{CC} = 2.5 V, V_{OH} = 2.25 V	–50	–200		µA
		V_{CC} = 4.0 V, V_{OH} = 3.2 V	–0.4	–1.4		mA
		V_{CC} = 5.0 V, V_{OH} = 3.9 V	–0.7	–2.2		mA
		V_{CC} = 6.0 V, V_{OH} = 4.6 V	–1.0	–3.3		mA
I_{OL}	Output sink current	V_{CC} = 2.5 V, V_{OL} = 0.35 V	0.4	0.9		mA
		V_{CC} = 4.0 V, V_{OL} = 0.8 V	1.6	3.5		mA
		V_{CC} = 5.0 V, V_{OL} = 1.1 V	2.5	5.5		mA
		V_{CC} = 6.0 V, V_{OL} = 1.4 V	3.4	8.0		mA

† V_{CC} = 5 V, T_A = 25°C
‡ Output levels ensure 400 mV of noise margin over specified input levels.

Figure 4–15. Output Loading Circuit for Test for the TMS70C02, TMS70C42, and TMS70C82



Note: Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points.

Table 4–23. Supply Current Requirements for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{CC}	Operating mode	f_{osc} = 7.0 MHz,	V_{CC} = 5.0 V		17	24.5	mA
		f_{osc} = 3.0 MHz,	V_{CC} = 5.0 V		7.2	10.5	mA
		f_{osc} = 0.5 MHz,	V_{CC} = 5.0 V		1.2	1.8	mA
		f_{osc} = Z MHz,	V_{CC} = 5.0 V		2.4	3.5	mA/ MHz
		f_{osc} = 0.5 MHz,	V_{CC} = 2.5 V		0.4	1.2	mA
I_{CC}	Wake-up mode 1 (one timer and UART active)	f_{osc} = 7.0 MHz,	V_{CC} = 5.0 V		2400	5600	µA
		f_{osc} = 3.0 MHz,	V_{CC} = 5.0 V		1200	3300	µA
		f_{osc} = 0.5 MHz,	V_{CC} = 5.0 V		250	800	µA
I_{CC}	Wake-up mode 2 (one timer active and UART inactive)	f_{osc} = 7.0 MHz,	V_{CC} = 5.0 V		960	3400	µA
		f_{osc} = 3.0 MHz,	V_{CC} = 5.0 V		480	2000	µA
		f_{osc} = 0.5 MHz,	V_{CC} = 5.0 V		140	550	µA
I_{CC}	Wake-up mode 3 (UART active only)	f_{osc} = 7.0 MHz,	V_{CC} = 5.0 V		1500	2400	µA
		f_{osc} = 3.0 MHz,	V_{CC} = 5.0 V		800	1500	µA
		f_{osc} = 0.5 MHz,	V_{CC} = 5.0 V		180	600	µA
I_{CC}	Halt OSC-ON	f_{osc} = 7.0 MHz,	V_{CC} = 5.0 V		560	1280	µA
		f_{osc} = 3.0 MHz,	V_{CC} = 5.0 V		240	560	µA
		f_{osc} = 1.0 MHz,	V_{CC} = 5.0 V		80	200	µA
		f_{osc} = Z MHz			(See Note 2)		µA
I_{CC}	Halt OSC-OFF				5	10	µA

Notes: 1) All inputs = V_{CC} or V_{SS} (except XTAL2). All I/O and output pins are open.
2) Maximum current = 180(Z) + 20 µA.

Table 4–24. Recommended Crystal/Clockin Operating Conditions Over Full Operating Range for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Test Conditions	Min	Typ†	Max	Unit
f_{osc}	Crystal frequency	V_{CC} = 2.5 V	0.5		0.8	MHz
		V_{CC} = 4.0 V	0.5		5.0	MHz
		V_{CC} = 5.0 V	0.5		7.0	MHz
		V_{CC} = 6.0 V	0.5		7.5	MHz
	CLKIN duty cycle		47		53	%
$t_{c(P)}$	CLKIN cycle time	V_{CC} = 2.5 V	333		2000	ns
		V_{CC} = 4.0 V	167		2000	ns
		V_{CC} = 5.0 V	143		2000	ns
		V_{CC} = 6.0 V	133		2000	ns
$t_{c(C)}$	Internal state cycle time	V_{CC} = 2.5 V	666		4000	ns
		V_{CC} = 4.0 V	333		4000	ns
		V_{CC} = 5.0 V	286		4000	ns
		V_{CC} = 6.0 V	267		4000	ns
$t_{w(PH)}$	CLKIN pulse duration high		50			ns
$t_{w(PL)}$	CLKIN pulse duration low		50			ns
t_r	CLKIN rise time				30	ns
t_f	CLKIN fall time				30	ns
$t_{d(PL-CH)}$	CLKIN fall to CLKOUT rise			110	250	ns

† V_{CC} = 5 V, T_A = 25°C.

Figure 4–16. Clock Timing for the TMS70C02, TMS70C42, and TMS70C82

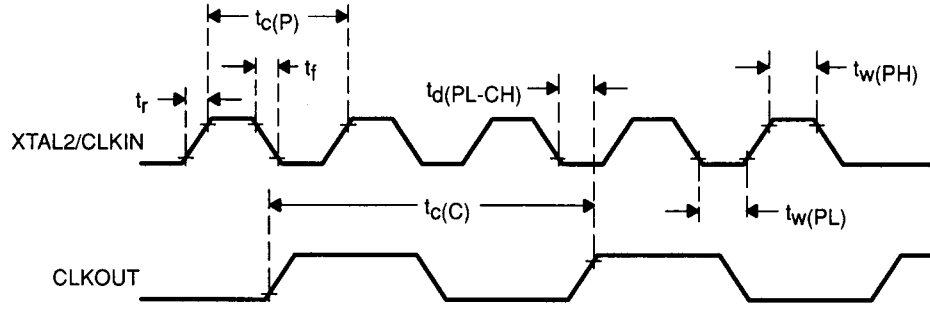


Figure 4–17. Operating Frequency Range for the TMS70C02, TMS70C42, and TMS70C82

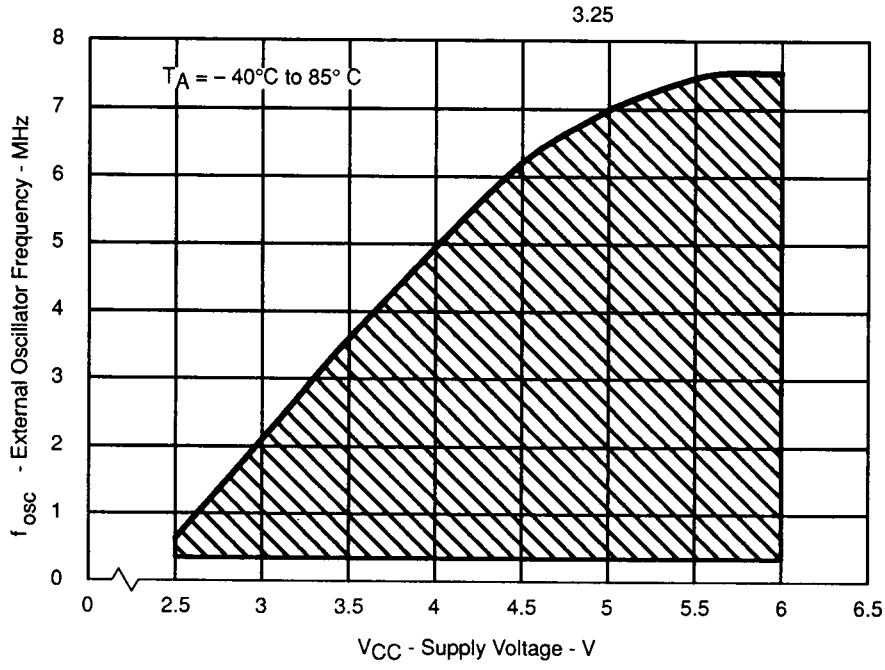


Figure 4–18. Typical Operating Current vs. Supply Voltage for the TMS70C02, TMS70C42, and TMS70C82

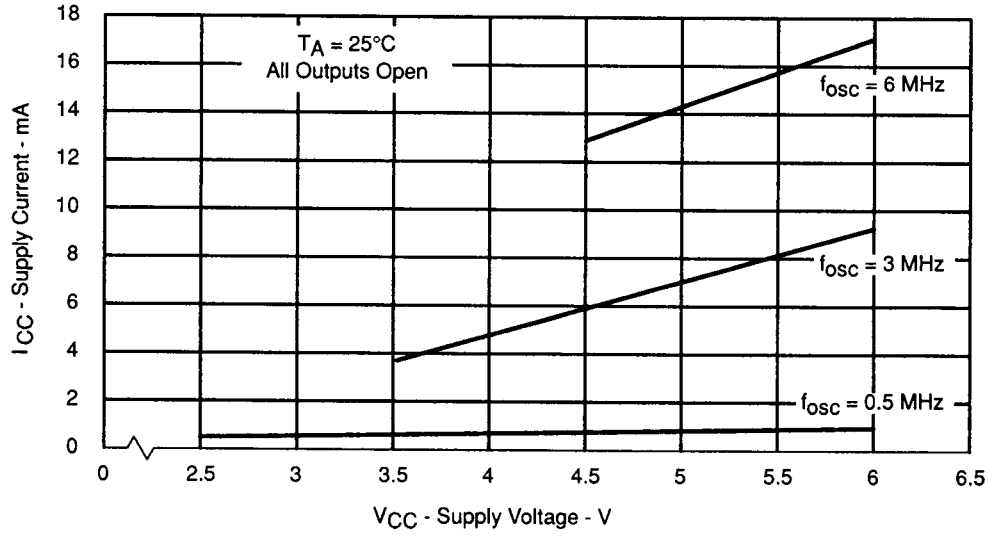


Figure 4–19. Typical Operating I_{CC} vs. Oscillator Frequency for the TMS70C02, TMS70C42, and TMS70C82

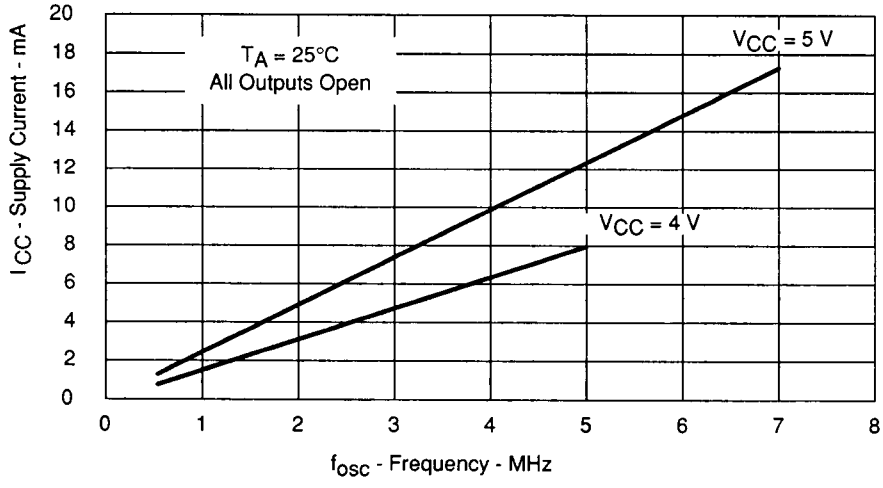


Figure 4–20. Typical Operating Current vs. Supply Voltage for the TMS70C02, TMS70C42, and TMS70C82

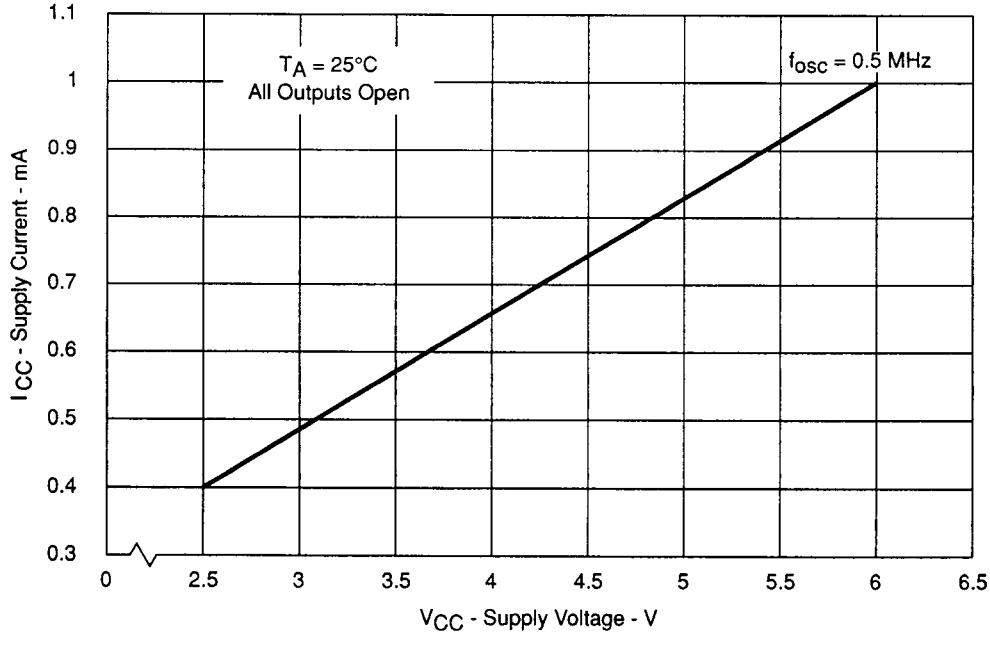


Figure 4–21. Typical Output Source Characteristics for the TMS70C02, TMS70C42, and TMS70C82

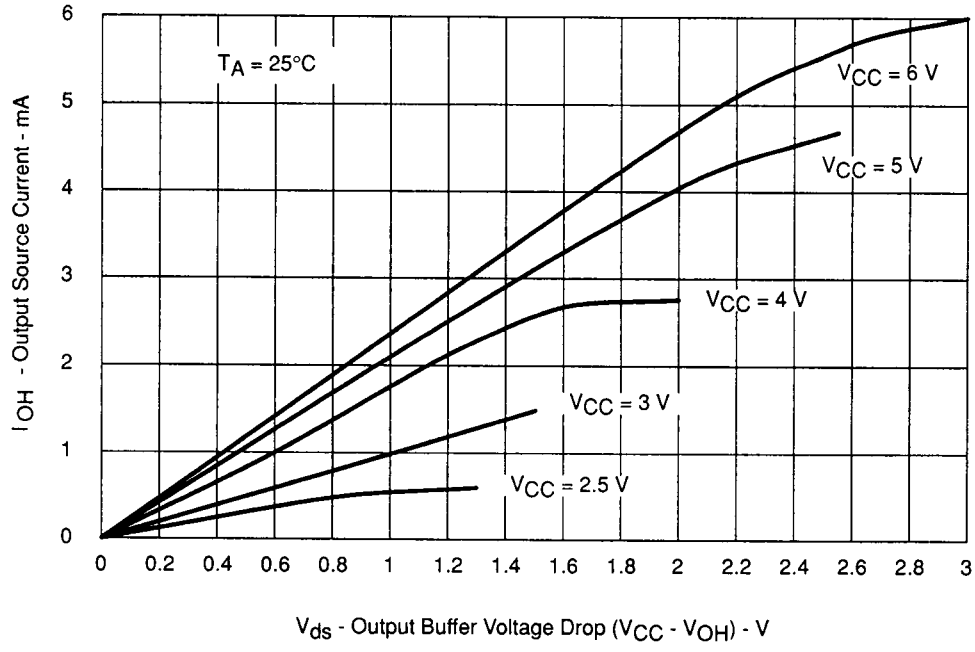
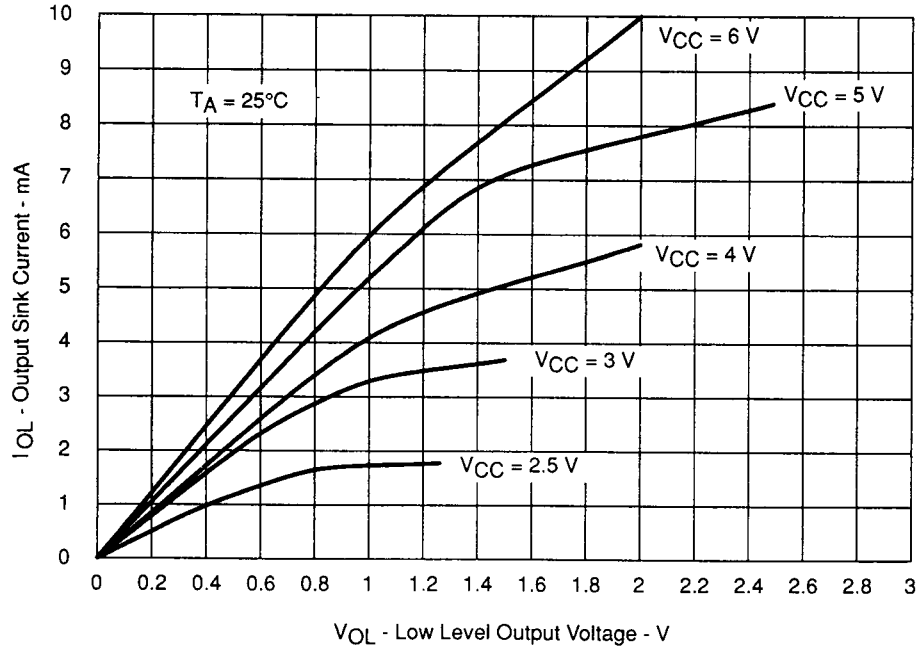


Figure 4–22. Typical Output Sink Characteristics for the TMS70C02, TMS70C42, and TMS70C82



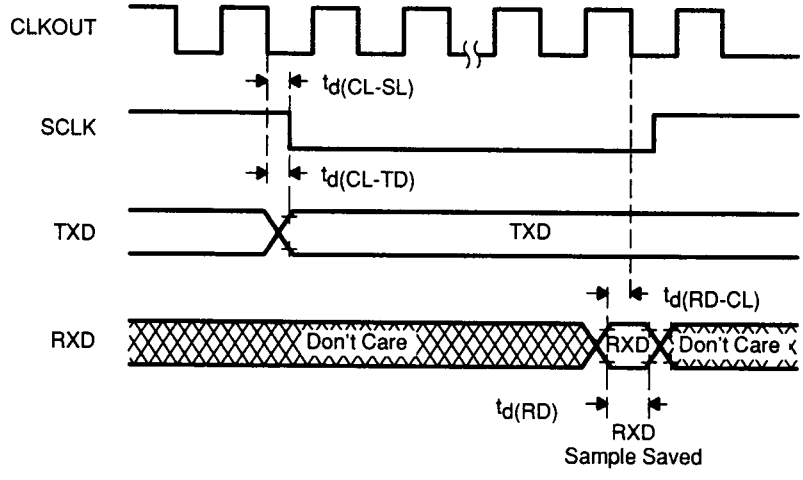
4.4.1 Serial Port Timing

4.4.1.1 *Internal Serial Clock*

Table 4–25. Timing Parameters for Internal Serial Clock for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Typ	Unit
$t_{d(CL-SL)}$	CLKOUT low to SCLK low	1/4 $t_{c(C)}$	ns
$t_{d(CL-TD)}$	CLKOUT low to new TXD data	1/4 $t_{c(C)}$	ns
$t_{d(RD-CL)}$	RXD data valid before CLKOUT low	1/4 $t_{c(C)}$	ns
$t_{d(RD)}$	RXD data valid time	1/2 $t_{c(C)}$	ns

Figure 4–23. Timing Diagram for Internal Serial Clock for the TMS70C02, TMS70C42, and TMS70C82



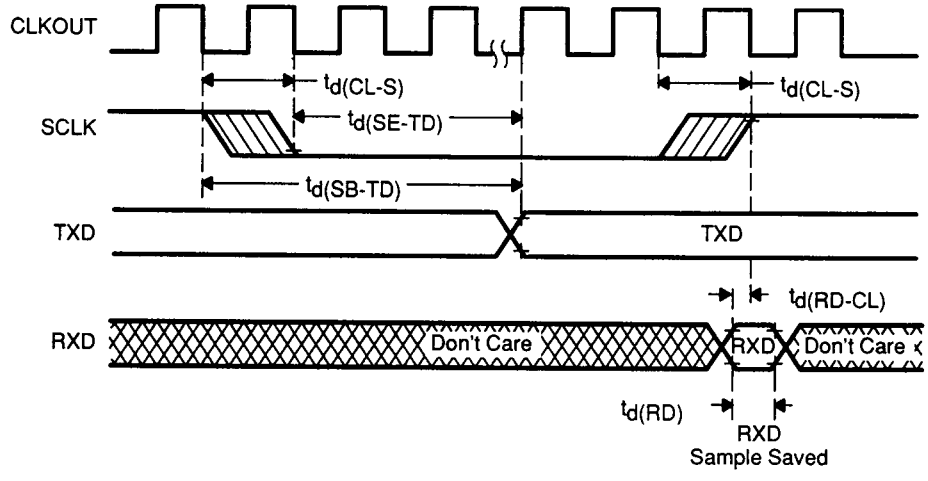
Notes: 1) The CLKOUT signal is not available in single-chip mode.
2) CLKOUT = $t_{c(C)}$.

4.4.1.2 External Serial Clock

Table 4–26. Timing Parameters for External Serial Clock for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Typ	Unit
$t_{d(RD-CL)}$	RXD data valid before CLKOUT low	1/4 $t_{c(C)}$	ns
$t_{d(RD)}$	RXD data valid time	1/2 $t_{c(C)}$	ns
$t_{d(SB-TD)}$	Start of SCLK sample to new TXD data	3 1/4 $t_{c(C)}$	ns
$t_{d(SE-TD)}$	End of SCLK sample to new TXD data	2 1/4 $t_{c(C)}$	ns
$t_{d(CL-S)}$	Clockout low to SCLK transition	$t_{c(C)}$	ns

Figure 4–24. Timing Diagram for External Serial Clock for the TMS70C02, TMS70C42, and TMS70C82



Notes: 1) The CLKOUT signal is not available in single-chip mode.
2) CLKOUT = $t_{c(C)}$.
3) SCLK sampled; if SCLK = 1 then 0, fall transition found.
4) SCLK sampled; if SCLK = 0 then 1, rise transition found.

4.5 TMS70C02, TMS70C42, and TMS70C82 Specifications (5V ±10%)

Table 4–27. Absolute Maximum Ratings Over Operating Free-Air Temperature Range for the TMS70C02, TMS70C42, and TMS70C82 (Unless Otherwise Noted)

Supply voltage range, V_{CC}† . . . . . – 0.3 V to 7 V
Input voltage range . . . . . – 0.3 V to V_{CC}+0.3 V
Output voltage range . . . . . – 0.3 V to V_{CC}+0.3 V
Maximum I/O buffer current (per pin) . . . . . ±10 mA
Storage temperature range . . . . . – 55°C to 150°C
I_{CC}, I_{SS} (maximum into pin 25 or 40 . . . . . ±60 mA
Continuous power dissipation . . . . . 0.5 W

† Unless otherwise noted, all voltages are with respect to V_{SS}.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 4–28. Recommended Operating Conditions for the TMS70C02, TMS70C42, and TMS70C82

			Min	Nom	Max	Unit
V_{CC}	Supply voltage		4.5		5.5	V
V_{IH}	High-level input voltage	MC and XTAL2 pins	$0.8V_{CC}$			V
		All other input pins	$0.7V_{CC}$			V
V_{IL}	Low-level input voltage	MC and XTAL2 pins			$0.3V_{CC}$	V
		All other input pins			$0.2V_{CC}$	V
T_A	Operating temperature	Commercial (TMS70C42NL)	0		70	°C
		Industrial (TMS70C42NA)	–40		85	°C

Table 4–29. Electrical Characteristics Over Full Range of Operating Conditions for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Test Conditions	Min	Typ†	Max	Unit
I_I	Input leakage current	MC pin, $V_{IN} = V_{SS}$ or V_{CC} All others, $V_{IN} = V_{SS}$ to V_{CC}		±0.1	±5	µA
C_I	Input capacitance			5		pF
V_{OH}	High-level output voltage	V_{CC} = 5.0 V, I_{OH} = – 0.3 mA	V_{CC}–0.05	4.7		V
V_{OL}	Low-level output voltage	V_{CC} = 5.0 V, I_{OL} = 1.4 mA		0.2	0.4	V
I_{OH}	High-level output source current	$V_{OH} = V_{CC}$ – 0.5 V	–0.3	–1.2		mA
		V_{OH} = 2.5 V min	–1.0	–3.0		mA
I_{OL}	Output sink current	V_{OL} = 0.4 V	1.4	2.0		mA

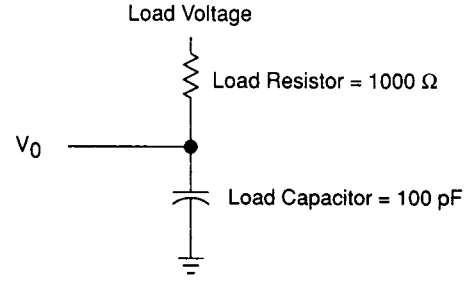
† Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points.

Table 4–30. AC Characteristics for Input/Output Ports† for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Test Conditions	Min	Typ†	Max	Unit
$t_{r(IO)}$	I/O port output rise time	C_{load} = 15 pF, V_{CC} = 5 V		35	60	ns
$t_{f(IO)}$	I/O port output fall time	C_{load} = 15 pF, V_{CC} = 5 V		20	50	ns

† Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points.

Figure 4–25. Output Loading Circuit for Test for the TMS70C02, TMS70C42, and TMS70C82



Note: Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points.

Figure 4–26. Measurement Points for Switching Characteristics for the TMS70C02, TMS70C42, and TMS70C82

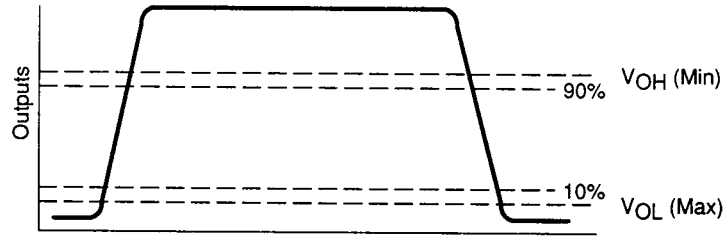


Table 4–31. Supply Current Requirements for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Test Conditions	Min	Typ	Max	Unit
I_{CC}	Supply current	f_{osc} = 6.0 MHz		15	24	mA
		f_{osc} = 3.0 MHz		7.2	12	mA
		f_{osc} = 1.0 MHz		2.4	4.0	mA
		f_{osc} = Z MHz		2.4	4.0	mA/ MHz
I_{CC}	Wake-up mode 1 (one timer and UART active)	f_{osc} = 6.0 MHz		2400	5400	µA
		f_{osc} = 3.0 MHz		1200	2900	µA
		f_{osc} = 1.0 MHz		650	1500	µA
I_{CC}	Wake-up mode 2 (one timer active, and UART inactive)	f_{osc} = 6.0 MHz		960	3200	µA
		f_{osc} = 3.0 MHz		480	1800	µA
		f_{osc} = 1.0 MHz		350	1000	µA
I_{CC}	Wake-up mode 3 (UART active only)	f_{osc} = 6.0 MHz		1500	2200	µA
		f_{osc} = 3.0 MHz		800	1300	µA
		f_{osc} = 1.0 MHz		400	1100	µA
I_{CC}	Halt OSC-ON	f_{osc} = 6.0 MHz		480	1120	µA
		f_{osc} = 3.0 MHz		240	560	µA
		f_{osc} = 1.0 MHz		80	200	µA
		f_{osc} = Z MHz			(See Note 2)	µA
I_{CC}	Halt OSC-OFF			5	10	µA

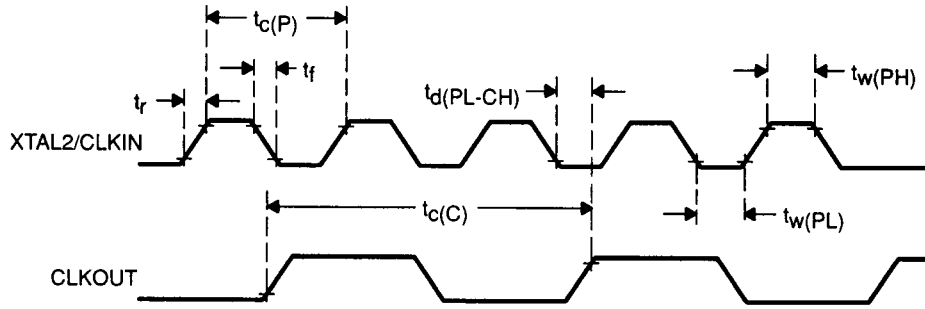
Notes: 1) All inputs = V_{CC} or V_{SS} (except XTAL2). All output pins are open.
2) Maximum current = 180(Z) + 20 µA.

Table 4–32. Recommended Crystal/Clockin Operating Conditions Over Full Operating Range for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Min	Typ	Max	Unit
f_{osc}	CLKIN frequency	0.5		6.0	MHz
	CLKIN duty cycle	45		55	%
$t_{c(P)}$	CLKIN cycle time	167		2000	ns
$t_{c(C)}$	Internal state cycle time	333		4000	ns
$t_{w(PH)}$	CLKIN pulse duration high	70			ns
$t_{w(PL)}$	CLKIN pulse duration low	70			ns
t_r	CLKIN rise time			30	ns
t_f	CLKIN fall time			30	ns
$t_{d(PL-CH)}$	CLKIN fall to CLKOUT rise delay		110	250	ns

† V_{CC} = 5 V, T_A = 25°C

Figure 4–27. Clock Timing for the TMS70C02, TMS70C42, and TMS70C82



Note: Period of internal clock $t_{c(C)} = 2 \times t_{c(P)} = 2 / f_{osc}$. Timings are given in $t_{c(C)}$.

Table 4–33. Memory Interface Timings† for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Min	Typ†	Max	Unit
$t_{c(C)}$	CLKOUT cycle time	333		4000	ns
$t_{w(CH)}$	CLKOUT high pulse duration	$0.5t_{c(C)}-90$	$0.5t_{c(C)}$	$0.5t_{c(C)}+90$	ns
$t_{w(CL)}$	CLKOUT low pulse duration	$0.5t_{c(C)}-90$	$0.5t_{c(C)}$	$0.5t_{c(C)}+90$	ns
$t_{d(CH-JL)}$	Delay time, CLKOUT rise to ALATCH fall	$0.5t_{c(C)}-50$	$0.5t_{c(C)}$		ns
$t_{w(JH)}$	ALATCH high pulse duration	$0.25t_{c(C)}-50$	$0.25t_{c(C)}$		ns
$t_{su(HA-JL)}$	Setup time, high address valid before ALATCH fall	$0.25t_{c(C)}-45$	$0.25t_{c(C)}$		ns
$t_{su(LA-JL)}$	Setup time, low address valid before ALATCH fall	$0.25t_{c(C)}-45$	$0.25t_{c(C)}$		ns
$t_{d(JL-LA)}$	Delay time, low address valid after ALATCH fall	$0.5t_{c(C)}-35$	$0.5t_{c(C)}$		ns
$t_{su(RW-JL)}$	Setup time, R/$\overline{W}$ valid before ALATCH fall	$0.25t_{c(C)}-40$	$0.25t_{c(C)}$		ns
$t_{h(EH-RW)}$	Hold time, R/$\overline{W}$ valid after $\overline{ENABLE}$ rise	$0.5t_{c(C)}-60$	$0.5t_{c(C)}$		ns
$t_{h(EH-HA)}$	Hold time, high address valid after $\overline{ENABLE}$ rise	$0.5t_{c(C)}-60$	$0.5t_{c(C)}$		ns
$t_{su(Q-EH)}$	Setup time, data out valid before $\overline{ENABLE}$ rise	$0.5t_{c(C)}-70$	$0.5t_{c(C)}$		ns
$t_{h(EH-Q)}$	Hold time, data out valid after $\overline{ENABLE}$ rise	$0.5t_{c(C)}-60$	$0.5t_{c(C)}$		ns
$t_{d(LA-EL)}$	Delay time, low address high-Z to $\overline{ENABLE}$ fall	$.25t_{c(C)}-45$	$0.25t_{c(C)}$		ns
$t_{d(EH-A)}$	Delay time, $\overline{ENABLE}$ rise to next address drive	$0.5t_{c(C)}-60$	$0.5t_{c(C)}$		ns
$t_{d(EL-D)}$	Delay time, data in after $\overline{ENABLE}$ fall	$0.75t_{c(C)}-160$	$0.75t_{c(C)}$		ns
$t_{a(A-D)}$	Access time, data in from valid address	$1.5t_{c(C)}-200$	$1.5t_{c(C)}-100$		ns
$t_{d(A-EH)}$	Delay time, $\overline{ENABLE}$ high after address valid	$1.5t_{c(C)}-50$	$1.5t_{c(C)}$		ns
$t_{h(EH-D)}$	Hold time, Data input valid after $\overline{ENABLE}$ rise	0			ns
$t_{d(EH-JH)}$	Delay time, $\overline{ENABLE}$ rise to ALATCH rise	$0.5t_{c(C)}-60$	$0.5t_{c(C)}$		ns
$t_{d(CH-EL)}$	Delay time, CLKOUT rise to $\overline{ENABLE}$ fall		30		ns

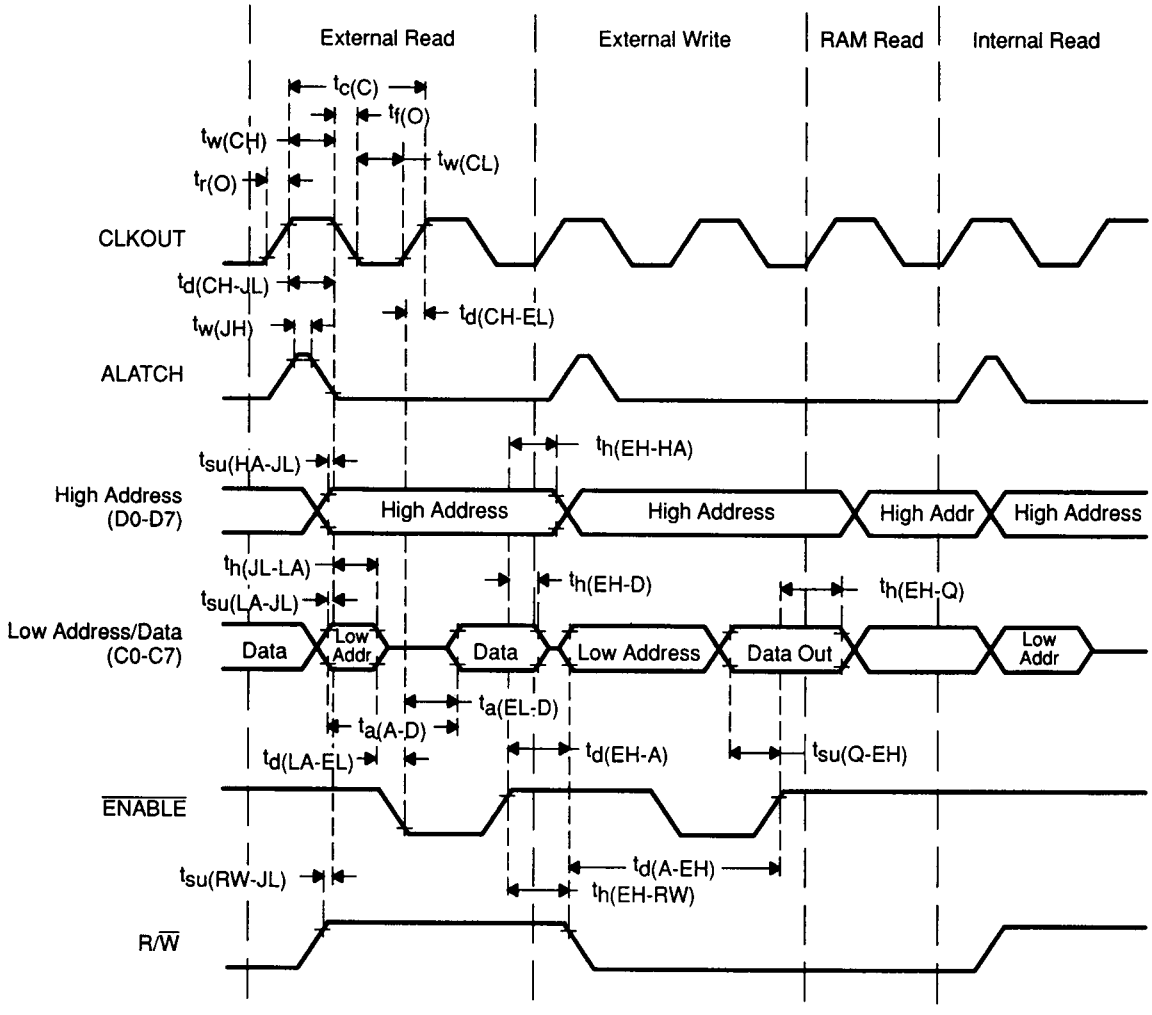
† V_{CC} = 5 V ±10%, $t_{c(C)}$ = 2/freq
CLKIN duty cycle = 50%
f_{osc} = 0.5 to 6.0 MHz

Table 4–34. Memory Interface Timings at 6 MHz† for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Min	Typ†	Max	Unit
$t_{c(C)}$	CLKOUT cycle time		333		ns
$t_{w(CH)}$	CLKOUT high pulse duration	76	166	252	ns
$t_{w(CL)}$	CLKOUT low pulse duration	76	162	252	ns
$t_{d(CH-JL)}$	Delay time, CLKOUT rise to ALATCH fall	116	166		ns
$t_{w(JH)}$	ALATCH active duration	33	83		ns
$t_{su(AH-JL)}$	Setup time, high address valid before ALATCH fall	38	83		ns
$t_{su(LA-JL)}$	Setup time, low address valid before ALATCH fall	38	83		ns
$t_{d(JL-LA)}$	Delay time, low address hold after ALATCH fall	131	166		ns
$t_{d(RW-JL)}$	Delay time, R/$\overline{W}$ valid before ALATCH fall	43	83		ns
$t_{h(EH-RW)}$	Hold time, R/$\overline{W}$ valid after $\overline{ENABLE}$ rise	106	166		ns
$t_{h(EH-HA)}$	Hold time, high address valid after $\overline{ENABLE}$ rise	106	166		ns
$t_{su(Q-EH)}$	Setup time, data out valid before $\overline{ENABLE}$ rise	96	166		ns
$t_{h(EH-Q)}$	Hold time, data out valid after $\overline{ENABLE}$ rise	106	166		ns
$t_{d(LA-EL)}$	Delay time, low address high-Z to $\overline{ENABLE}$ fall	38	83		ns
$t_{d(EH-A)}$	Delay time, $\overline{ENABLE}$ rise to next address drive	106	166		ns
$t_{d(EL-D)}$	Delay time, data in after $\overline{ENABLE}$ fall	90	250		ns
$t_{a(A-D)}$	Access time, data in from valid address	300	400		ns
$t_{d(A-EH)}$	Delay time, $\overline{ENABLE}$ high after address valid	450	500		ns
$t_{h(EH-D)}$	Hold time, data input valid after $\overline{ENABLE}$ rise	0			ns
$t_{d(EH-JH)}$	Delay time, $\overline{ENABLE}$ rise to ALATCH rise	106	166		ns
$t_{d(CH-EL)}$	Delay time, CLKOUT rise to $\overline{ENABLE}$ fall		30		ns

† V_{CC} = 5 V ±10%, $t_{c(C)}$ = 2/freq
CLKIN duty cycle = 50%
f_{osc} = 0.5 to 6.0 MHz

Figure 4–28. Read and Write Cycle Timing for the TMS70C02, TMS70C42, and TMS70C82



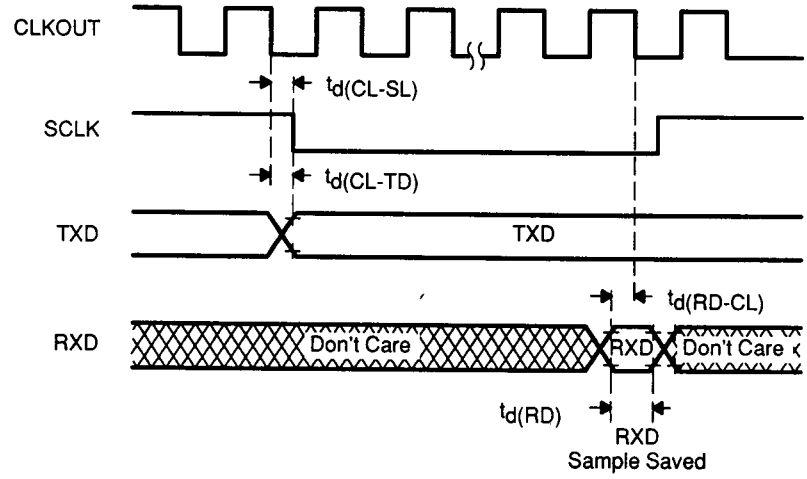
4.5.1 Serial Port Timing

4.5.1.1 Internal Serial Clock

Table 4–35. Timing Parameters for Internal Serial Clock for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Typ	Unit
$t_{d(CL-SL)}$	CLKOUT low to SCLK low	1/4 $t_{c(C)}$	ns
$t_{d(CL-TD)}$	CLKOUT low to new TXD data	1/4 $t_{c(C)}$	ns
$t_{d(RD-CL)}$	RXD data valid before CLKOUT low	1/4 $t_{c(C)}$	ns
$t_{d(RD)}$	RXD data valid time	1/2 $t_{c(C)}$	ns

Figure 4–29. Timing Diagram for Internal Serial Clock for the TMS70C02, TMS70C42, and TMS70C82



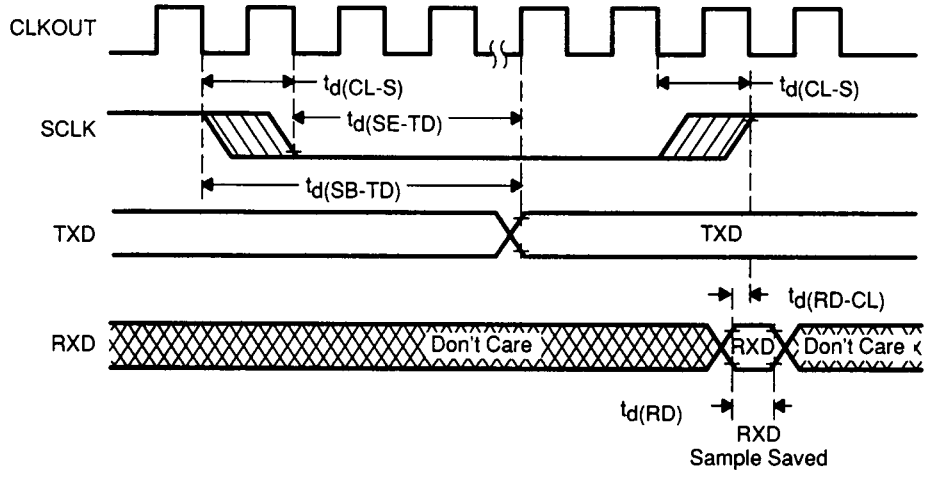
Notes: 1) The CLKOUT signal is not available in single-chip mode.
2) CLKOUT = $t_{c(C)}$.

4.5.1.2 External Serial Clock

Table 4–36. Timing Parameters for External Serial Clock for the TMS70C02, TMS70C42, and TMS70C82

Parameter		Typ	Unit
$t_{d(RD-CL)}$	RXD data valid before CLKOUT low	1/4 $t_{c(C)}$	ns
$t_{d(RD)}$	RXD data valid time	1/2 $t_{c(C)}$	ns
$t_{d(SB-TD)}$	Start of SCLK sample to new TXD data	3 1/4 $t_{c(C)}$	ns
$t_{d(SE-TD)}$	End of SCLK sample to new TXD data	2 1/4 $t_{c(C)}$	ns
$t_{d(CL-S)}$	Clockout low to SCLK transition	$t_{c(C)}$	ns

Figure 4–30. Timing Diagram for External Serial Clock for the TMS70C02, TMS70C42, and TMS70C82



Notes: 1) The CLKOUT signal is not available in single-chip mode.
2) CLKOUT = $t_{c(C)}$.
3) SCLK sampled; if SCLK = 1 then 0, fall transition found.
4) SCLK sampled; if SCLK = 0 then 1, rise transition found.