1. THE SINGLE-CHIP MICROCOMPUTERS FROM TEXAS INSTRUMENTS

1.1 DESCRIPTION

The TMS 1000 family of microcomputers from Texas Instruments offers a low cost, high reliability, single chip solution for many applications. Low development costs and the accumulation of product experience favor the microcomputer approach. Currently there are over 600 TMS 1000 Programmations or 60 million units installed in the field making the TMS 1000 the most pervasive microcomputer in the world.

The TMS 1000 series is a family of MOS/LSI four-bit microcomputers with a ROM, a RAM, and an arithmetic logic unit on a single semiconductor chip. A customer's specification determines the software that is reproduced during wafer processing by a single-level mask technique that defines a fixed ROM pattern. As summarized in 1.4, the TMS 1000 and TMS 1200 are the basic 1024-instruction ROM microcomputers. The TMS 1070 and TMS 1270 interface directly to high-voltage displays and use instructions identical to the TMS 1000/1200 devices. To increase the software capacity in one chip, the TMS 1100/TMS 1300 and TMS 1170/TMS 1370 provide twice the ROM and RAM size of the TMS 1000/TMS 1200 while the TMS 1400/1600, TMS 1470/1670 microcomputers have a 4096 eight-bit instruction ROM.

1.2 FEATURES

- 4-bit architecture
- 0.5K X 8 to 4K X 8 program ROM
- 32 X 4 to 128 X 4 scratchpad RAM
- 6 to 16 independent R-output lines
- 5 to 8 decoded O-output lines
- 4 unlatched inputs
- 4 latched inputs (TMS 1600/1670, TMS 1200C/1300C)
- Onboard input frequency divider (TMS 1400 series)
- 9 or 15 V PMOS operation or 5 V CMOS
- VF display interfacing (TMS 1X70)
- PMOS power consumption from 36 mW
- CMOS power consumption from 0.5 μW

1.3 DESIGN SUPPORT

TI provides support for the entire TMS 1000 series:

- System evaluators with an external EPROM.
- Complete stand-alone development system for program development.
- Microcomputer application specialists nationwide for local design assistance.
- Regional Technology Centers.

A staff of experienced application programmers is available at Texas Instruments to assist customers in evaluating applications, in training designers to program the TMS 1000 series, and in simulating programs. TI will also contract to write programs to customer's specifications.

Figure 1 is a flow diagram for software development through prototyping and production release.

A TMS 1000 series program (see flowchart, Figure 1) is written in assembly language using standard mnemonics. The assembler converts the source code (assembly language program) into machine code, which is transferred to an AMPL emulator. Also, the assembler produces a machine code object file. The object file is used for hardware simulation or for generating prototype tooling.

The TMS 1000 series programs are checked by system evaluators and hardware simulation. The hardware simulation offers the designer the advantages of real-time simulation and testing asynchronous inputs. System evaluators are suited for field testing and limited production volumes.

After the algorithms have been checked and approved by the customer, the final object code and machine options statements are supplied to TI. A gate mask is generated and slices produced. After assembly and testing, the prototypes are shipped to the customer for approval. Upon receiving final approval, the part is released for volume production at the required rate as one unique version of the TMS 1000 family.

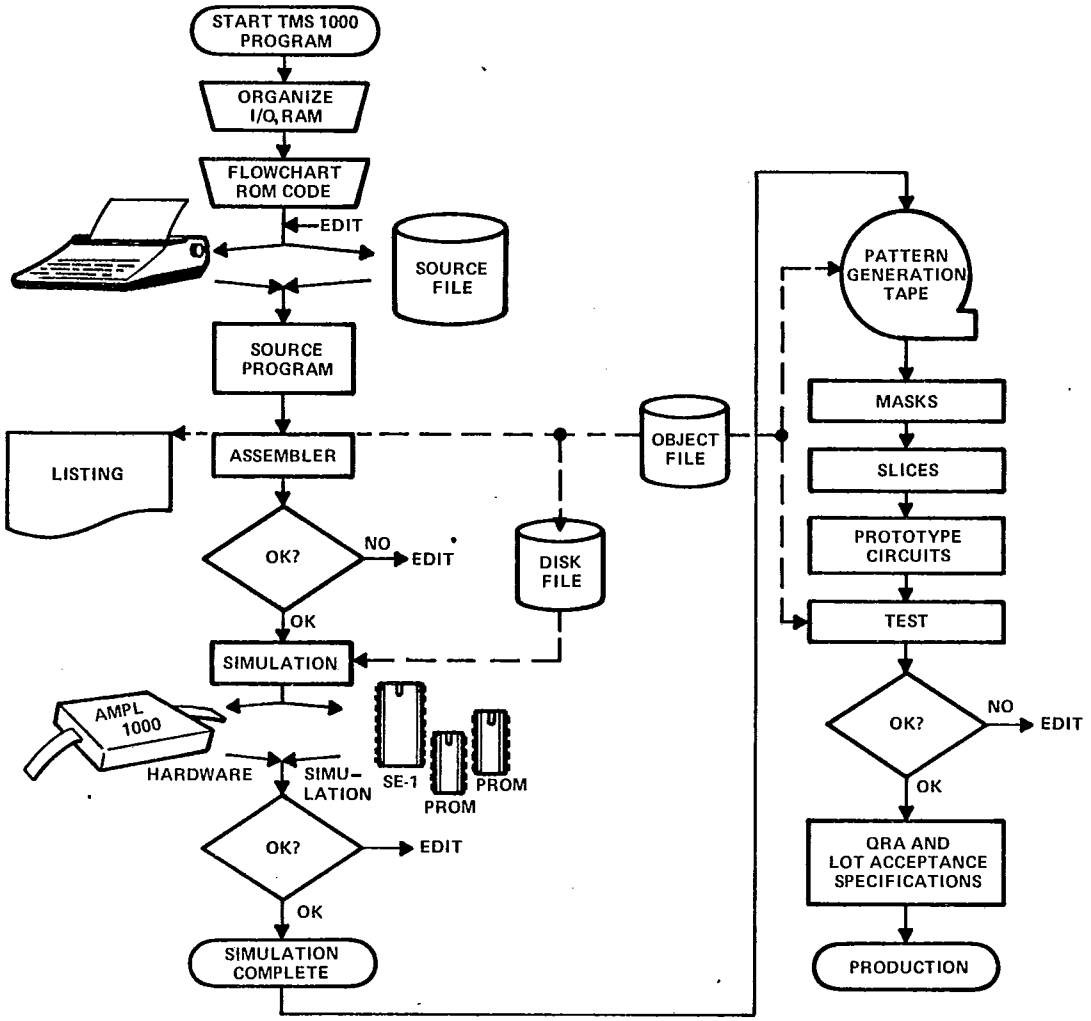


FIGURE 1 – DESIGN RELEASE FLOWCHART

1.4 TMS 1000 FAMILY SUMMARY

TABLE 1 – TMS 1000 FAMILY SUMMARY

DEVICE	ROM 8 BIT	RAM 4 BIT	I/O FEATURES		STACK LEVELS	PACK PINS	DISPLAY VOLTAGE	SUPPLY VOLTAGE	TECH.	EVALUATION ROM-LESS CHIP	AMPL 1000 EMULATOR
			INPUTS	OUTPUTS R/O							
1700	512	32	4	9/8	1	28	VLED	9/15	PMOS	SE-1000P	PMOS
1000	1024	64	4	11/8	1	28	VLED	9/15	PMOS	SE-1000P	PMOS
1200	1024	64	4	13/8	1	40	VLED	9/15	PMOS	SE-1000P	PMOS
1070	1024	64	4	11/8	1	28	VF	9/15	PMOS	SE-1000P	PMOS
1270	1024	64	4	13/10	1	40	VF	9/15	PMOS	SE-1000P	PMOS
1100	2048	128	4	11/8	1	28	VLED	9/15	PMOS	SE-1100P	PMOS
1300	2048	128	4	16/8	1	40	VLED	9/15	PMOS	SE-1100P	PMOS
1170	2048	128	4	11/8	1	28	VF	9/15	PMOS	SE-1100P	PMOS
1370	2048	128	4	16/8	1	40	VF	9/15	PMOS	SE-1100P	PMOS
1400	4096	128	4	11/8	3	28	VLED	9/15	PMOS	SE-1400P	1400
1600	4096	128	8	16/8	3	40	VLED	9/15	PMOS	SE-1400P	1400
1470	4096	128	4	10/8	3	28	VF	9/15	PMOS	SE-1400P	1400
1670	4096	128	8	16/8	3	40	VF	9/15	PMOS	SE-1400P	1400
1000C	1024	64	4	10/8	3	28	LOGIC	5	CMOS	SE-1000C	CMOS
1200C	1024	64	8	16/8	3	40	LOGIC	5	CMOS	SE-1000C	CMOS
1070C	1024	64	4	10/8	3	28	VF	5	CMOS	SE-1000C	CMOS
1270C	1024	64	8	16/8	3	40	VF	5	CMOS	SE-1000C	CMOS
1100C	2048	128	4	10/8	3	28	LOGIC	5	CMOS	SE-1100C	CMOS
1300C	2048	128	8	16/8	3	40	LOGIC	5	CMOS	SE-1100C	CMOS

1.5 QUICK-REFERENCE PRODUCT SELECTION

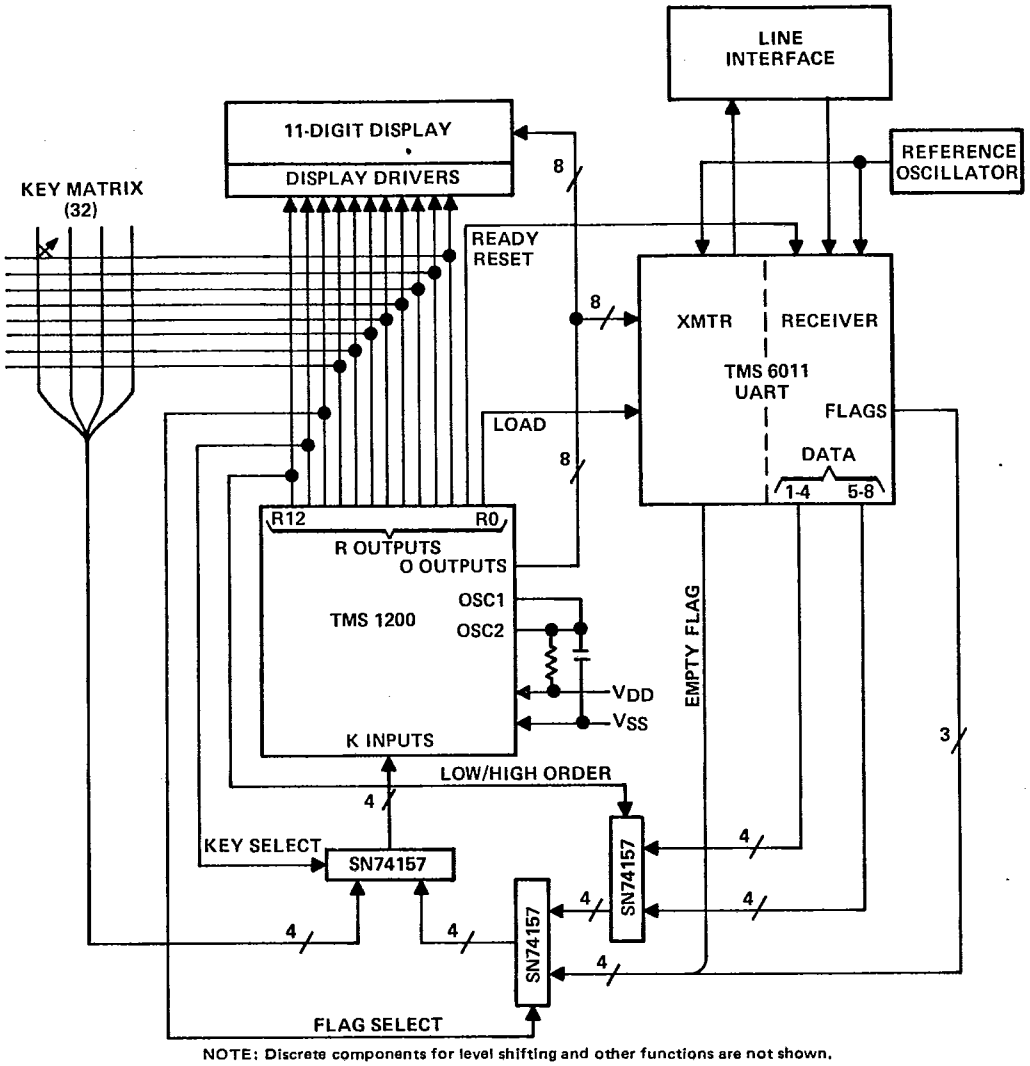
TABLE 2 – QUICK-REFERENCE SELECTION GUIDE

PART NUMBER			10XX	11XX	12XX	13XX	14XX	16XX	17XX
ROM		512 X 8 bits							P, L
		1024 X 8 bits	P, L, C		P, L, C				
		2048 X 8 bits		P, L, C		P, L, C			
		4046 X 8 bits					P, L	P, L	
RAM		32 X 4 bits							P, L
		64 X 4 bits	P, L, C		P, L, C				
		128 X 4 bits		P, L, C		P, L, C	P, L	P, L	
OUTPUTS	R lines	9 lines							P, L
		10 lines	C	C			1470P		
		11 lines	P, L	P, L			1400P/ 1400L		
		13 lines			P, L				
		16 lines			C	P, L, C		P, L	
	O lines	8 lines	P, L, C	P, L, C	P, L, C	P, L, C	P, L	P, L	P, L
		10 lines			1270P				
INPUTS	K lines	non-latching	P, L, C	P, L, C	P, L, C	P, L, C	P, L	P, L	P, L
	L lines	latching			C	C		P, L	
SUBROUTINES		1 level, same page	P, L	P, L	P, L	P, L			P, L
		3 levels, any page	C	C	C	C	P, L	P, L	

P: 15 VOLT PMOS L: 9 VOLT PMOS C: CMOS

1.6 APPLICATIONS

One major advantage of the TMS 1000 series is flexibility. The TMS 1000 series is effective in applications such as printer controllers, data terminals, remote sensing systems, cash registers, appliance controls, and automotive applications. A data terminal is a useful example. In Figure 2, a sample interconnect diagram shows how the R outputs control a universal asynchronous receiver/transmitter (UART), display scan, and keyboard scan. The ROM controls data output to the appropriate display digit or to the transmitter section of the UART. A routine in the ROM program controls selection of incoming data through the K-input ports. Two dedicated R outputs (load and ready reset) control the UART's transmit and receive modes. The remaining R outputs both scan the display and select inputs. The SN74157 TTL devices multiplex eight bits of the incoming data word, four bits of UART status, and the four key input lines. Through the TMS 1000 series' versatility, a wide range of systems realize reduced costs, fewer parts, and high reliability.



NOTE: Discrete components for level shifting and other functions are not shown.

FIGURE 2 – BLOCK DIAGRAM OF TYPICAL APPLICATION–TERMINAL CONTROLLER

2. TMS 1000/1200 AND TMS 1070/1270 MICROCOMPUTERS

2.1 INTRODUCTION

The TMS 1000/1200 and TMS 1070/1270 are identical except for maximum voltage ratings for the K inputs and the O and R outputs, and the TMS 1270 has a total of ten O outputs.

The microcomputer's ROM program controls data input, storage, processing, and output. Data processing takes place in the arithmetic logic unit. K input data goes into the ALU, as shown in Figure 3, and is stored in the four-bit accumulator. The accumulator output accesses the output latches, the RAM storage cells, and the adder input. Data storage in the 256-bit RAM is organized into 64 words, four bits per word. The four-bit words are conveniently grouped into four 16-word files addressed by a two-bit register. A four-bit register addresses one of the 16 words in a file by ROM control.

The O outputs and the R outputs are the output channels. The eight parallel O outputs are decoded from five data latches. The O outputs serve many applications because the decoder is a programmable logic array (PLA) that is modified by changing the gate-level mask tooling. Each of the thirteen R outputs of the TMS 1200 and the eleven R outputs on the TMS 1000 has an individual storage element that can be set or reset by program control. The R outputs send status or enable signals to external devices. The R outputs strobe the O outputs to displays, to other TMS 1000 series chips, or to TTL and other interface circuits. The same R outputs multiplex data into the K inputs whenever necessary.

There are 43 basic instructions that handle I/O, constant data from the ROM, bit control, internal data transfer, arithmetic processing, branching, looping, and subroutines. The eight-bit instruction word performs 256 unique operations for maximum efficiency. Section 2.8 defines the standard instruction set, which is optimized for most programs.

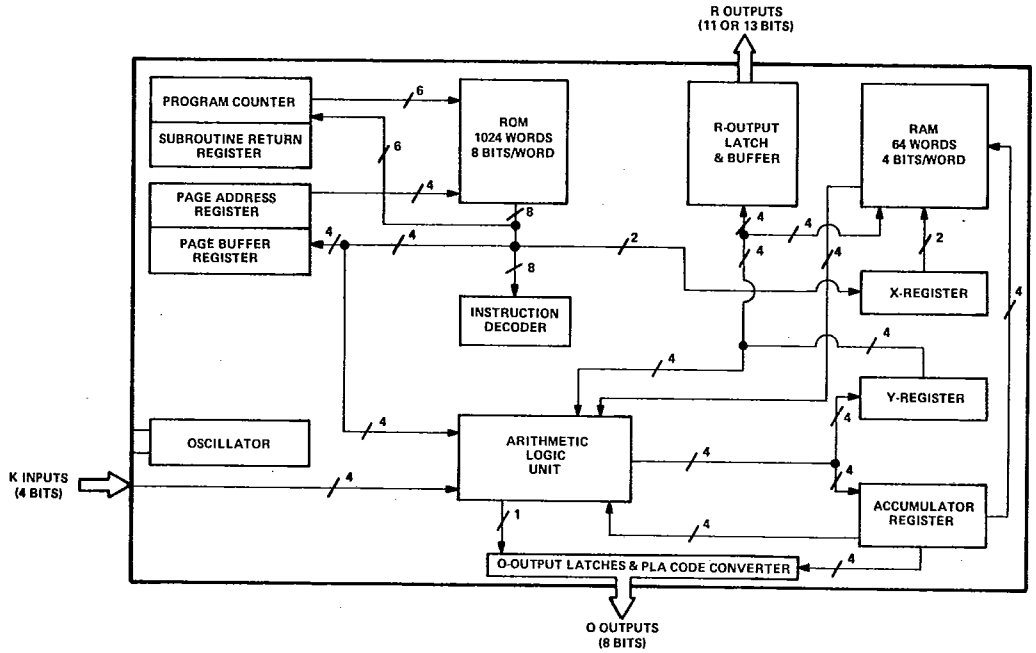


FIGURE 3 – TMS 1000/TMS 1200 LOGIC BLOCKS

2.2 ROM OPERATION

The sequence of the 1024 eight-bit ROM instructions determines the device operation. There are 16 pages of instructions with 64 instructions on each page. After power-up the program execution starts at a fixed instruction address. Then a shift-register program counter sequentially addresses each ROM instruction on a page. A conditional branch or call subroutine instruction may alter the six-bit program-counter address to transfer software control. One level of subroutine return address is stored in the subroutine return register. The page address register (four bits) holds the current address for one of the 16 ROM pages. To change pages, a constant from the ROM loads into the page buffer register (four bits), and upon a successful branch or call, the page buffer loads into the page address register. The page buffer register also holds the return page address in the call subroutine mode.

2.3 RAM OPERATION

There are 256 addressable bits of RAM storage available. The RAM is comprised of four files, each file containing 16 four-bit words. The RAM is addressed by the Y register and the X register. The Y register selects one of the 16 words in a file and is completely controllable by the arithmetic unit. The TMS 1000 series has instructions that: Compare Y to a constant, set Y to a constant, increment or decrement Y, and/or perform data transfer to or from Y. Two bits in the X register select one of the four 16-word files. The X register is set to a constant or is complemented. A four-bit data word goes to the RAM location addressed by X and Y from the accumulator or from the constants in the ROM. The RAM output words go to the arithmetic unit and can be operated on and loaded into Y or the accumulator in one instruction interval. Any selected bit in the RAM can be set, reset, or tested.

2.4 ARITHMETIC LOGIC UNIT OPERATION

Arithmetic and logic operations are performed by the four-bit adder and associated logic. The arithmetic unit performs logical comparison, arithmetic comparison, add, and subtract functions. The arithmetic unit and interconnects are shown in Figure 4. The operations are performed on two sets of inputs, P and N. The two four-bit parallel inputs may be added together or logically compared. The accumulator has an inverted output to the N selector for subtraction by two's complement arithmetic. The other N inputs are from the true output of the accumulator, the RAM, constants, and the K inputs. The P inputs come from the Y register, the RAM, the constants, and the K inputs.

Addition and subtraction results are stored in either the Y register or the accumulator. An arithmetic function may cause a carry output to the status logic. Logical comparison may generate an output to status. If the comparison functions are used, only the status bit affects the program control, and neither the Y register's nor the accumulator register's contents are affected. If the status feedback is a logic one, which is the normal state, then the conditional branch or call is executed successfully. If an instruction calls for a carry output to status and the carry does not occur,

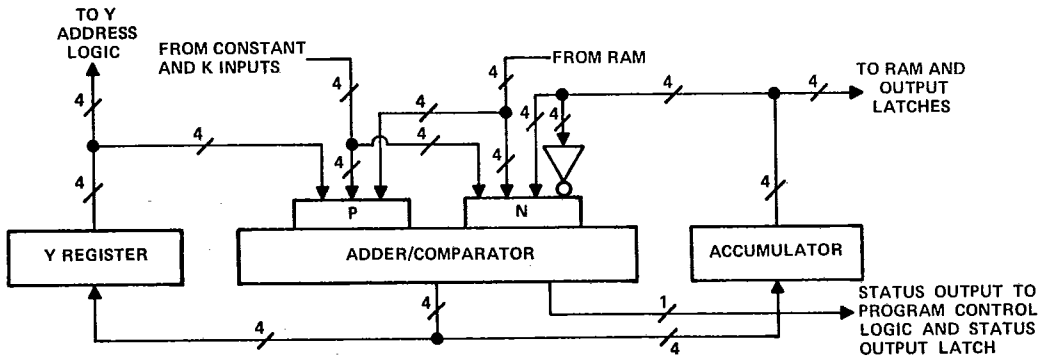


FIGURE 4 – ALU AND ASSOCIATED DATA PATHS

then status will go to a zero state for one instruction cycle. Likewise, if an instruction calls for the logical-comparison function and the bits compared are all equal, then status will go to a zero state for one instruction cycle. If status is a logic zero, then branches and calls are not performed successfully.

2.5 INPUT

There are four data inputs to the TMS 1000-series circuit, K1, K2, K4, and K8. Each time an input word is requested, the data path from the K inputs is enabled to the adder. The inputs are either tested for a high level ($\approx V_{SS}$), or the input data are stored in the accumulator for further use. The R outputs usually multiplex inputs such as keys and other data. Other input interfaces are possible. An external device that sends data out to the K-input bus at a fixed rate may be used with the TMS 1000 series when an initiating "handshake" signal is given from an R output. Data from the K inputs is stored periodically in synchronization with the predetermined data rate of the external device. Thus, multiple four-bit words can be requested and stored with only one R output supplying the control signal.

2.6 OUTPUT

There are two output channels with multiple purposes, the R outputs and the O outputs. Thirteen latches store the R output data. The eight parallel O outputs come from a five-bit-to-eight-bit code converter, which is the O-output PLA. The R outputs are individually addressed by the Y register. Each addressed bit can be set or reset.

The R outputs are normally used to multiplex inputs and strobe O output data to displays, external memories, and other devices. Also, one R output can strobe other R outputs that represent variable data, because every R output may be set or reset individually. For example, the Y register addresses each latch in turn; the variable data R outputs are set or reset; and finally, the data strobe R latch is set.

The eight O outputs usually send out display or binary data that are encoded from the O output latches. The O latches contain five bits. Four bits load from the accumulator in parallel. The fifth bit comes from the status latch, which is selectively loaded from the adder output (see Figure 4). The load output command sends the status latch and accumulator information into the five output latches. The five bits are available in true or complementary form to 20 programmable-input NAND gates in the O output PLA. Each NAND gate can simultaneously select any combination of O0 through O7 as an output. The user defines this PLA's decoding to suit an optimum output configuration. As an illustration, the O output PLA can encode any 16 characters of eight-segment display information and additionally can transfer out a four-bit word of binary data. Figure 5 shows a display interface example (SL = 1) and also illustrates binary data transmission (SL = 0).

2.7 TIMING RELATIONSHIPS

The TMS 1000 Family output, input and instruction timing is given in Figure 6. Six oscillator pulses constitute one instruction cycle. All instructions are executed in one instruction cycle. The actual machine cycle period is determined by either a fixed external resistor and capacitor connected to the OSC1 and OSC2 pins, or an external clock input frequency.

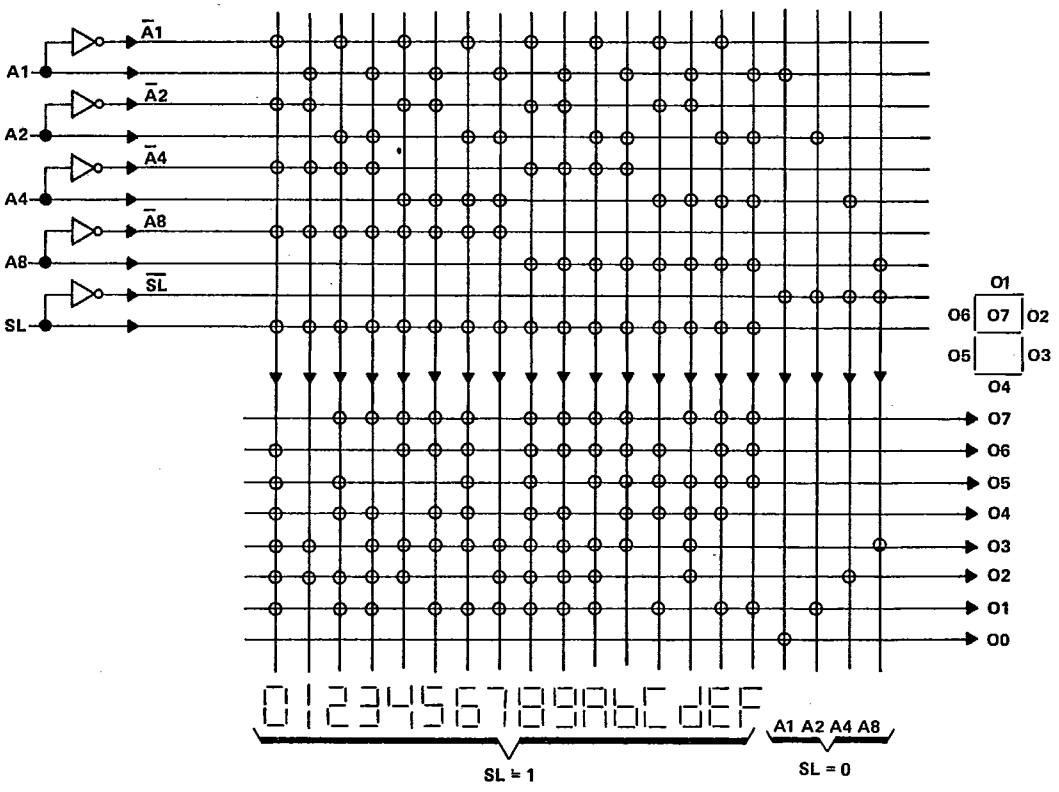
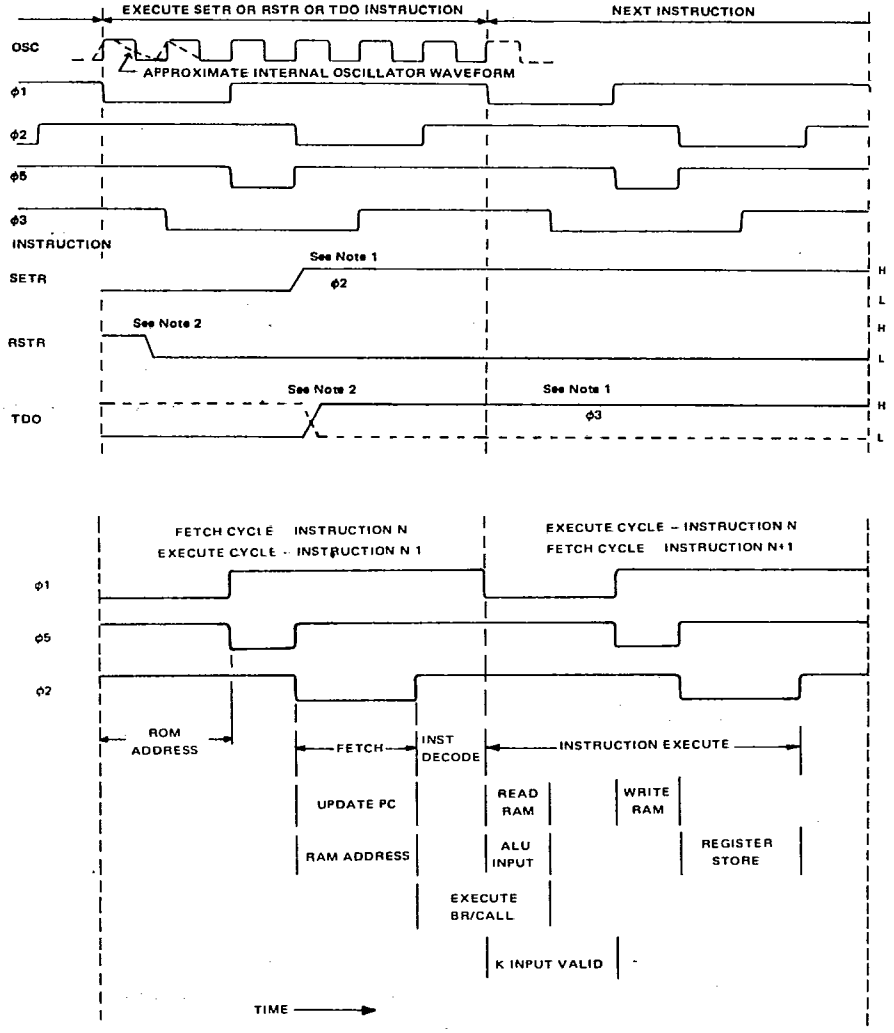


FIGURE 5 – O OUTPUT PLA FOR BINARY AND SEVEN-SEGMENT ENCODING



NOTES: 1. Initial rise time is load dependent. The high level output voltage, V_{OH}, is characterized following the indicated clock period.
2. Rise and fall times are load dependent.

FIGURE 6 – TMS 1000 FAMILY OUTPUT, INPUT AND INSTRUCTION TIMING

2.8 SOFTWARE SUMMARY

Table 3 defines the TMS 1000/1200 and TMS 1700 standard instruction set with a description, mnemonic, and status effect. The mnemonics were defined for easy reference to the functional description. Eighteen mnemonics use an identifier to indicate the condition that satisfies the status requirement for a successful branch or call if the instruction is followed immediately by a branch or call command. "C" means that if the instruction generates a carry (status = one), then a following branch or call is executed. If a branch instruction does not follow or if there is no carry (status = zero), then the program counter proceeds to the next address without changing the normal counting sequence. "N" means that if no borrow (equal to a carry in two's complement arithmetic) is generated, an ensuing branch or call is taken. "Z" indicates that if the two's complement of zero in the accumulator (instruction CPAIZ) is attempted with a branch or call following, then the branch or call is taken. "1", "LE", "NE", and "NEZ" are used to indicate conditions for branch and call for seven test instructions. The test instructions do not modify data at all; tests are used solely in conjunction with subsequent branches or calls.

If an instruction that does not affect status is placed between an instruction that does affect status and a branch or call instruction, then the branch or call is always successful. This is true because status always returns to its normal state (status = one) after one instruction cycle, and branches and calls are taken if status equals one.

TABLE 3 – TMS 1000/TMS 1200 AND TMS 1700 STANDARD INSTRUCTION SET

FUNCTION	MNEMONIC	STATUS EFFECTS		DESCRIPTION
		C	N	
Register to Register	TAY			Transfer accumulator to Y register.
	TYA			Transfer Y register to accumulator.
	CLA			Clear accumulator.
Transfer Register to Memory	TAM			Transfer accumulator to memory.
	TAMIY			Transfer accumulator to memory and increment Y register.
	TAMZA			Transfer accumulator to memory and zero accumulator.
Memory to Register	TMY			Transfer memory to Y register.
	TMA			Transfer memory to accumulator.
	XMA			Exchange memory and accumulator.
Arithmetic	AMAAC	Y		Add memory to accumulator, results to accumulator. If carry, one to status.
	SAMAN	Y		Subtract accumulator from memory, results to accumulator. If no borrow, one to status.
	IMAC	Y		Increment memory and load into accumulator. If carry, one to status.
	DMAN	Y		Decrement memory and load into accumulator. If no borrow, one to status.
	IA			Increment accumulator, no status effect.
	IYC	Y		Increment Y register. If carry, one to status.
	DAN	Y		Decrement accumulator. If no borrow, one to status.
	DYN	Y		Decrement Y register. If no borrow, one to status.
	A6AAC	Y		Add 6 to accumulator, results to accumulator. If carry, one to status.
	A8AAC	Y		Add 8 to accumulator, results to accumulator. If carry, one to status.
	A10AAC	Y		Add 10 to accumulator, results to accumulator. If carry, one to status.
	CPAIZ	Y		Complement accumulator and increment. If then zero, one to status.
Arithmetic Compare	ALEM	Y		If accumulator less than or equal to memory, one to status.
	ALEC	Y		If accumulator less than or equal to a constant, one to status.
Logical Compare	MNEZ		Y	If memory not equal to zero, one to status.
	YNEA		Y	If Y register not equal to accumulator, one to status and status latch.
	YNEC		Y	If Y register not equal to a constant, one to status.

– CONTINUED –

TABLE 3 – TMS 1000/TMS 1200 AND TMS 1700 STANDARD INSTRUCTION SET (Continued)

FUNCTION	MNEMONIC	STATUS EFFECTS		DESCRIPTION
		C	N	
Bits in Memory	SBIT			Set memory bit.
	RBIT			Reset memory bit.
	TBIT1		Y	Test memory bit. If equal to one, one to status.
Constants	TCY			Transfer constant to Y register.
	TCMIY			Transfer constant to memory and increment Y.
Input	KNEZ		Y	If K inputs not equal to zero, one to status.
	TKA			Transfer K inputs to accumulator.
Output	SETR			Set R output addressed by Y.
	RSTR			Reset R output addressed by Y.
	TDO			Transfer data from accumulator and status latch to O outputs.
	CLO			Clear O-output register.
RAM 'X' Addressing	LDX			Load 'X' with a constant.
	COMX			Complement 'X'.
ROM Addressing	BR			Branch on status = one.
	CALL			Call subroutine on status = one.
	RETN			Return from subroutine.
	LDP			Load page buffer with constant.

NOTES: C-Y (Yes) means that if there is a carry out of the MSB, status output goes to the one state. If no carry is generated, status output goes to the zero state.

N-Y (Yes) means that if the bits compared are not equal, status output goes to the one state. If the bits are equal, status output goes to the zero state.

A zero in status remains through the next instruction cycle only. If the next instruction is a branch or call and status is a zero, then the branch or call is not executed successfully.

2.9 SAMPLE PROGRAM

The following example shows register addition of up to fifteen BCD digits. The add routine (flow charted in Figure 7) can use the entire RAM, which is divided into two pairs of registers. The definition of registers, for the purpose of illustration, is expanded to include the concept of a variable-length word that is a subset of a 16-digit file. Addition proceeds from the least-significant digit (LSD) to the most-significant digit (MSD), and carry ripples through the accumulator. The decrement-Y instruction is used to index the numbers in a register. The initial Y value sets the address for the LSD's of two numbers to be added. Thus, if Y equals eight at the start, the LSD is defined to be stored in M(X,8), [M(X, Y) ≡ contents of RAM word location X equals 0, 1, 2, or 3, and Y equals 0 to 15]. If Y is eight initially, M(X,7) is the next-most-significant digit.

RAM DATA MAP BEFORE EXECUTING SAMPLE ROUTINE

FILE ADDRESS	REGISTER	Y-REGISTER ADDRESS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X = 00	D	OV 0	MSD 9	8	7	6	5	4	3	LSD 2							
X = 01	E	OV 0	MSD 1	2	3	4	5	6	7	8	9	0	1	2	3	4	LSD 5
X = 10	F	OV 0	MSD 5	4	3	2	1	0	9	8	7	6	5	4	3	2	LSD 1
X = 11	G	OV 0	MSD 8	7	6	5	4	3	2	LSD 1							

OV ≡ overflow, MSD ≡ most-significant digit, and LSD ≡ least-significant digit

In the preceeding RAM register assignment map, registers D and G are nine digits long, and registers E and F are 16 digits long. The sample routine calls the D plus G → D subroutine and the E plus F → E subroutine. After executing the two subroutines, the RAM contents are the following:

RAM DATA MAP AFTER EXECUTING SAMPLE ROUTINE

FILE ADDRESS	REGISTER	Y-REGISTER ADDRESS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		OV	MSD							LSD							
X = 00	D	1	8	6	4	1	9	7	5	3							
		OV	MSD														LSD
X = 01	E	0	6	6	6	6	6	7	7	7	6	6	6	6	6	6	6
		OV	MSD														LSD
X = 10	F	0	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1
		OV	MSD							LSD							
X = 11	G	0	8	7	6	5	4	3	2	1							

NOTE: Shaded areas indicate locations in the RAM that are unaffected by executing the example routine.

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                    LABEL   OPCODE   OPERAND   COMMENT
MAIN PROGRAM        
PRESETS Y,          
AND CALL            
SUBROUTINES                 *TCY     8         Transfer 8 → Y
                            CALL     ADGD      Add: D + G → D
                            TCY      15        Transfer 15 → Y
                            CALL     AEFE      Add: E + F → E

                    ADGG    LDX      3         3 → X; Set up for D + G → G.
                            BR       BCDADD    Branch to BCD add.
MULTIPLE ENTRY      AEFF    LDX      2         2 → X; Set up for E + F → F.
POINTS FOR                  BR       BCDADD    Branch to BCD add.
SUBROUTINES         AEFE    LDX      1         1 → X; Set up for E + F → E.
                            BR       BCDADD    Branch to BCD add.
                    ADGD    LDX      0         0 → X; Add D + G → D.
                    BCDADD  CLA                Clear accumulator (A).
                    LOOP    COMX               X̄ → X.
                            AMAAC              M(X,Y) + A → A; A contains
                                               possible carry if in loop.
                            COMX               X̄ → X.
                            AMAAC              Add digits:
                                               M(X, Y) + [M(X̄,Y) + Carry] → A.
BASE                        BR       GT9       Branch if sum >15.
SUBROUTINE                  ALEC     9         If A ≤ 9, one to status.
CONTAINS                    BR       LT10      Branch if sum < 10.
LOOPING             GT9     A6AAC              Sum > 9, A + 6 → A;
AND                                            BCD Correction.
BCD                         TAMZA              Transfer corrected sum
CORRECTION                                     to memory, 0 → A.
                            IA                 1 → A; to propagate carry
                    DECY    DYN                Y − 1 → Y; index next digit.
                            BR       LOOP      If no borrow, continue.
                            RETN               If borrow, return to
                                               instruction after call.
                    LT10    TAMZA              Sum < 9, A → M(X,Y); 0 → A;
                                               No carry propagated.
                            BR       DECY
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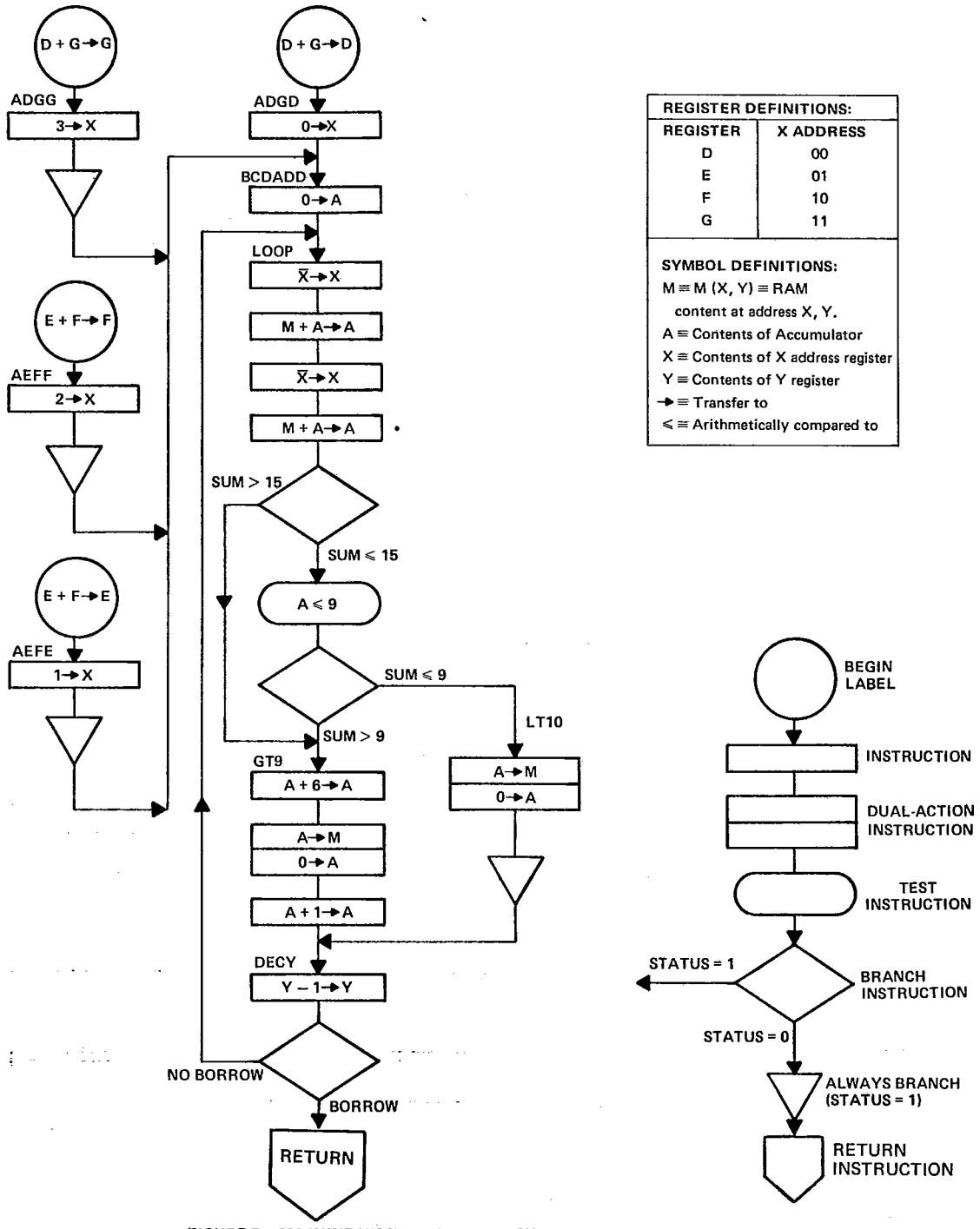


FIGURE 7 – MACHINE INSTRUCTION FLOWCHART BCD ADDITION SUBROUTINE

3. TMS 1700 MICROCOMPUTERS

3.1 INTRODUCTION

The TMS 1700 is identical to the TMS 1000 except that the TMS 1700 has half as much ROM and RAM as the TMS 1000, and has nine R-outputs, as opposed to eleven R-outputs on the TMS 1000 (See Figure 8).

3.2 ROM OPERATION

The TMS 1700 ROM is organized into eight pages, each page containing 64 instruction words. The instruction word in ROM is comprised of eight bits. Each page is addressed by a three-bit Page Address Register. The Page Buffer Register, which is loaded with a constant from ROM in order to change pages upon a successful branch or call, is also three bits wide. With these exceptions, the TMS 1700 ROM is identical to ROM operations of the TMS 1000.

3.3 RAM OPERATION

There are 128 bits of RAM on the TMS 1700. The RAM is comprised of four files, each file containing eight four-bit words. The RAM is addressed by the X-register and the Y-register. The two-bit X-register selects one of the four 8-word files. The three least significant bits of the 4-bit Y-register select one of the eight words in the file. The most significant bit of the Y-register is not used for RAM addressing.

3.4 OUTPUT

The TMS 1700 has two output channels, the R-outputs and the O-outputs. Nine latches store the R-output data and are addressed by the four bits of the Y-register. The eight parallel O-outputs come from a five-bit-to-eight-bit code converter, which is the O-output PLA identical to the PLA on the TMS 1000.

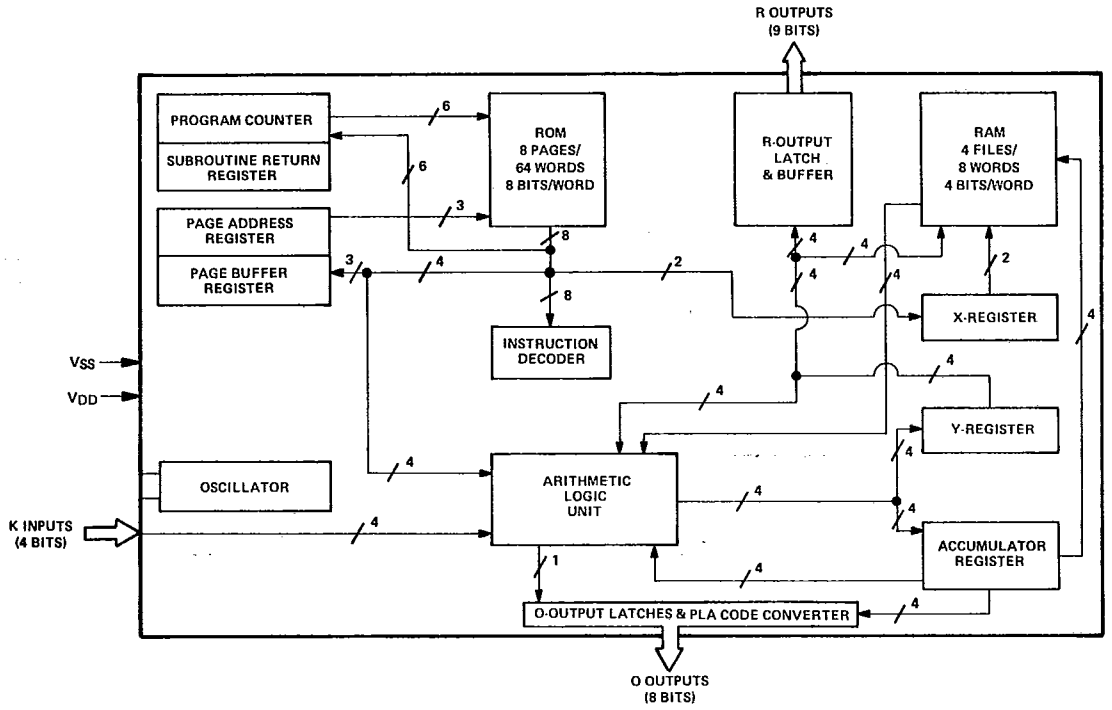


FIGURE 8 – TMS 1700 LOGIC BLOCKS

4. TMS 1100/1300 AND TMS 1170/1370 MICROCOMPUTERS

4.1 INTRODUCTION

Texas Instruments increased the four-bit microprocessor capability with an expanded one-chip microcomputer containing all of the TMS 1000 features plus twice the ROM and RAM capacity (see Figure 9). Two versions of the expanded memory device are available.

TMS 1100/1170

- Pin-for-pin interchangeable with the TMS 1000
- 16,384-bit ROM, 2048 eight-bit instruction words
- 512-bit RAM, 128 four-bit data words
- 11 individually latched R outputs, 28-pin package

TMS 1300/1370

- 16,384-bit ROM
- 512-bit RAM
- 16 individually latched R outputs, 40-pin package

Many industrial, consumer, and business applications can be implemented with a microcomputer having the capabilities of two TMS 1000 devices. With considerably lower system cost, the TMS 1100/1300 single-device microcomputers enable a number of applications that previously required two TMS 1000's or external read/write memory. In the 40-pin version, the TMS 1300, the maximum number of R outputs is increased to 16. Displays 16 characters long as well as a 64-position keyboard or switch matrix (16 X 4) are scanned directly by the TMS 1300.

The TMS 1100/1300 operation is identical to that of the TMS 1000/1200 except where noted otherwise in the following paragraphs. Since the TMS 1100/1300 has identical hardware to the TMS 1000/1200 but contains twice the RAM and ROM capacity, considerable software flexibility is available to the designer.

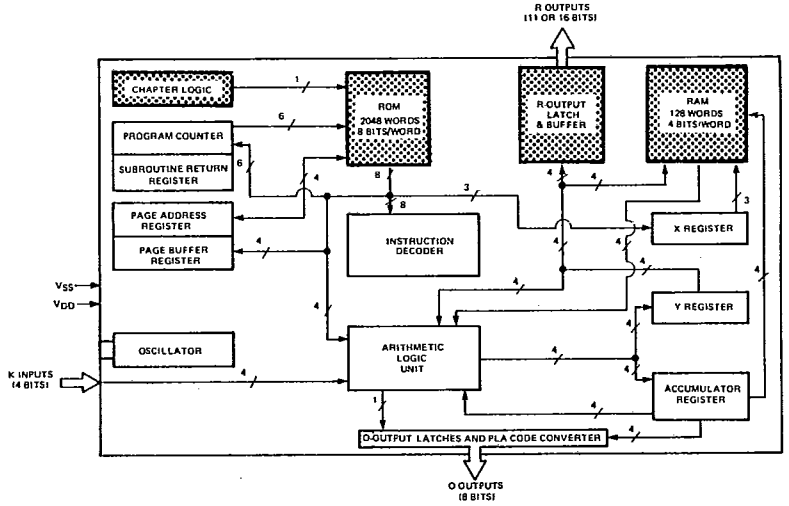


FIGURE 9 – TMS 1100/1300 LOGIC BLOCKS

4.2 ROM OPERATION

The TMS 1100/1300 instruction ROM contains two chapters of 16 pages each. A page contains 64 eight-bit words. The chapter logic consists of three control bits, chapter address, chapter buffer, and chapter subroutine. The chapter buffer bit is controlled by a complement chapter buffer instruction (see COMC in Table 4). The chapter buffer bit transfers into the current chapter address if a branch or call executes successfully. If a call is successful, the return chapter is saved in a chapter subroutine latch. Since the buffer bit is changeable without affecting the chapter subroutine-return address, up to 128 words that are contained on two pages of alternate chapters are available in a single subroutine. The program counter and page addressing operation is identical to the TMS 1000/1200 explained in 2-2.

TABLE 4
TMS 1100/1300 STANDARD INSTRUCTION SET

FUNCTION	MNEMONIC	STATUS EFFECT		DESCRIPTION
		C	N	
Register-to-Register Transfer	TAY			Transfer accumulator to Y register
	TYA			Transfer Y register to accumulator
	CLA			Clear accumulator
Register to Memory	TAM			Transfer accumulator to memory
	TAMIYC	Y		Transfer accumulator to memory and increment Y register. If carry, one to status.
	TAMDYN	Y		Transfer accumulator to memory and decrement Y register. If no borrow, one to status.
	TAMZA			Transfer accumulator to memory and zero accumulator
Memory to Register	TMY			Transfer memory to Y register
	TMA			Transfer memory to accumulator
	XMA			Exchange memory and accumulator
Arithmetic	AMAAC	Y		Add memory to accumulator, results to accumulator. If carry, one to status.
	SAMAN	Y		Subtract accumulator from memory, results to accumulator. If no borrow, one to status.
	IMAC	Y		Increment memory and load into accumulator. If carry, one to status.
	DMAN	Y		Decrement memory and load into accumulator. If no borrow, one to status.
	IAC	Y		Increment accumulator. If carry, one to status.
	DAN	Y		Decrement accumulator. If no borrow, one to status.
	A2AAC	Y		Add 2 to accumulator. Results to accumulator. If carry, one to status.
	A3AAC	Y		Add 3 to accumulator. Results to accumulator. If carry, one to status.
	A4AAC	Y		Add 4 to accumulator. Results to accumulator. If carry, one to status.
	A5AAC	Y		Add 5 to accumulator. Results to accumulator. If carry, one to status.
	A6AAC	Y		Add 6 to accumulator. Results to accumulator. If carry, one to status.
	A7AAC	Y		Add 7 to accumulator. Results to accumulator. If carry, one to status.
	A8AAC	Y		Add 8 to accumulator. Results to accumulator. If carry, one to status.
	A9AAC	Y		Add 9 to accumulator. Results to accumulator. If carry, one to status.
	A10AAC	Y		Add 10 to accumulator. Results to accumulator. If carry, one to status.
	A11AAC	Y		Add 11 to accumulator. Results to accumulator. If carry, one to status.
	A12AAC	Y		Add 12 to accumulator. Results to accumulator. If carry, one to status.
	A13AAC	Y		Add 13 to accumulator. Results to accumulator. If carry, one to status.
	A14AAC	Y		Add 14 to accumulator. Results to accumulator. If carry, one to status.
	IYC	Y		Increment Y register. If carry, one to status.
	DYN	Y		Decrement Y register. If no borrow, one to status.
	CPAIZ	Y		Complement accumulator and increment. If then zero, one to status.

– CONTINUED –

TABLE 4
TMS 1100/1300 STANDARD INSTRUCTION SET (Continued)

FUNCTION	MNEMONIC	STATUS EFFECT		DESCRIPTION
		C	N	
Arithmetic Compare	ALEM	Y		If accumulator less than or equal to memory, one to status.
Logical Compare	MNEA		Y	If memory is not equal to accumulator, one to status.
	MNEZ		Y	If memory not equal to zero, one to status.
	YNEA		Y	If Y register not equal to accumulator, one to status and status latch.
	YNEC		Y	If Y register not equal to a constant, one to status.
Bits in Memory	SBIT			Set memory bit
	RBIT			Reset memory bit
	TBIT1		Y	Test memory bit. If equal to one, one to status.
Constants	TCY			Transfer constant to Y register
	TCMIY			Transfer constant to memory and increment Y
Input	KNEZ		Y	If K inputs not equal to zero, one to status.
	TKA			Transfer K inputs to accumulator
Output	SETR			Set R output addressed by Y
	RSTR			Reset R output addressed by Y
	TDO			Transfer data from accumulator and status latch to O-outputs
RAM X Addressing	LDX			Load X with file address
	COMX			Complement the MSB of X
ROM Addressing	BR			Branch on status = one
	CALL			Call subroutine on status = one
	RETN			Return from subroutine
	LDP			Load page buffer with constant
	COMC			Complement chapter

NOTES: C-Y (Yes) means that if there is a carry out of the MSB, status output goes to the one state. If no carry is generated, status output goes to the zero state.

N-Y (Yes) means that if the bits compared are not equal, status output goes to the one state. If the bits are equal status output goes to the zero state.

A zero in status remains through the next instruction cycle only. If the next instruction is a branch or call and status is a zero, then the branch or call is not executed successfully.

4.3 RAM OPERATION

The TMS 1100/1300 devices contain a 512-bit RAM for data storage. The matrix consists of eight files, each file containing 16 four-bit words. Similar to the TMS 1000/1200, the X and Y registers address the RAM. The Y register selects one of the 16 words in a file and the X register (three bits long) selects one of eight possible files. When using the set or reset R instructions, the X register must be less than four.

4.4 OUTPUT

The TMS 1100 is pin-for-pin interchangeable with the TMS 1000 and contains eleven R outputs and eight O outputs.

The R-output capability in the TMS 1300 is increased to 16 output latches. These extra latches perform control functions directly that would have required external decoding logic in the TMS 1100 device. These additional R outputs can be set to any combination. For example, Figure 2 shows an O-output data bus going into the transmitter section of the UART. If the O-output PLA is programmed to send out four bits of binary data (when directed to do so by the status latch), then three additional R outputs connected to the UART transmitter input provides the user with full seven-bit ASCII output capability.

5. TMS 1400/1600 AND TMS 1470/1670 MICROCOMPUTERS

5.1 ROM ORGANIZATION/CHAPTER CONTROL

The sequence of the 4096 eight-bit ROM instructions determines the device operation. Instruction ROM contains four chapters of 16 pages each. A page contains 64 eight-bit words. After power-up the program execution starts at a fixed instruction address. A shift-register program counter sequentially addresses each ROM instruction on a page. A conditional branch or call subroutine instruction may alter the six-bit program-counter address to transfer software control. Three levels of subroutine return address may be stored in the subroutine return register.

The page address register (four bit) holds the current address for one of the 16 ROM pages. To change pages, a constant from ROM loads into the page buffer register (four bits), and upon a successful branch or call, the page buffer loads into the page address register. The page subroutine register, which is a three-level stack, holds the return page address in the call subroutine mode.

The chapter logic consists of three control registers, chapter address, chapter buffer, and chapter subroutine with a three level stack. The chapter buffer data is controlled by the TPC instruction, which transfers the page buffer to the chapter buffer. The chapter buffer transfers into the current chapter address if a branch or call executes successfully. If a call is successful, the return chapter is saved in a chapter subroutine latch.

5.2 RAM OPERATION

There are 512 addressable bits of RAM storage. The RAM is composed of eight files, each containing 16 four-bit words. The RAM is addressed by the X and Y registers. The Y register selects one of the 16 words in a file and is completely controllable by the ALU. The TMS 1000 Family has instructions within the standard instruction set that compare Y to a constant, set Y to a constant, increment or decrement Y, and/or perform data transfer to or from Y. Three bits in the X register select one of the eight 16-word files. The X register is set to a constant or is complemented. A four-bit data word goes to the RAM location addresses by X and Y from the accumulator or from the constants in the ROM. The RAM output words go to the ALU and can be operated on and loaded into Y or the accumulator in one instruction interval. Any selected bit in the RAM can be set, reset, or tested.

5.3 TMS 1400/TMS 1470 DATA INPUT

There are four data inputs to the TMS 1400/TMS 1470 circuit: K1, K2, K4 and K8 (see Figure 10). Each time an input word is requested, the data path from the K-inputs is enabled to the adder. The inputs are either tested for a high level ($\approx V_{SS}$) or the input data is stored in the accumulator for future use. The R-outputs usually multiplex inputs such as keys and other data onto the K-input lines. Other input interfaces are possible. Data from the K-inputs can be stored periodically in synchronization with the predetermined data rate of the external device. Thus, multiple four-bit words can be requested and stored with only one R-output supplying the control signal.

5.4 TMS 1600/TMS 1670 DATA INPUT

The TMS 1600/TMS 1670 devices have eight data inputs: K1, K2, K4, K8 and L1, L2, L4, L8 (see Figure 11). These two ports are multiplexed internally into a four-bit input bus. In addition, the TMS 1600/TMS 1670 have two control inputs: the K/L selector and SE Mode Selector. The K/L control has an internal pull-down resistor so that when no input is applied, or when the K/L input is at low level, the K-input is selected.

When the K/L input is at a high level, the four-bit L-input port is selected. The L-input port has two modes: a pass mode and a sense mode. The SE Mode Selector input has an internal pull-down resistor, and normally the pass mode is selected. When the SE Mode Selector is at a high level, the sense mode is selected. During sense mode, positive momentary inputs are latched. Table 5 summarizes functions of K/L and SE Mode Selector inputs. K/L selects requires one instruction setup time minimum.

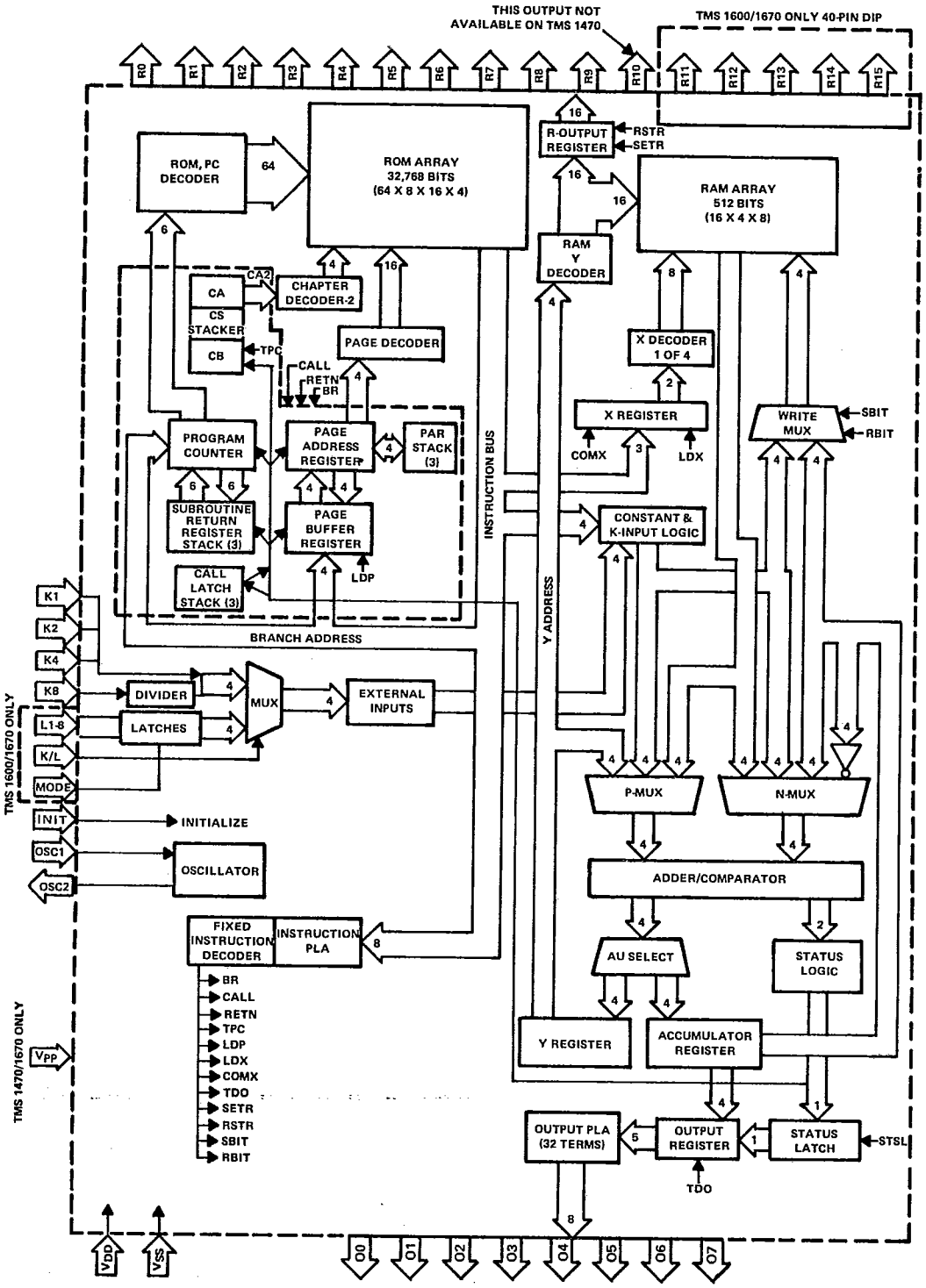


FIGURE 10 – TMS 1400 SERIES BLOCK DIAGRAM

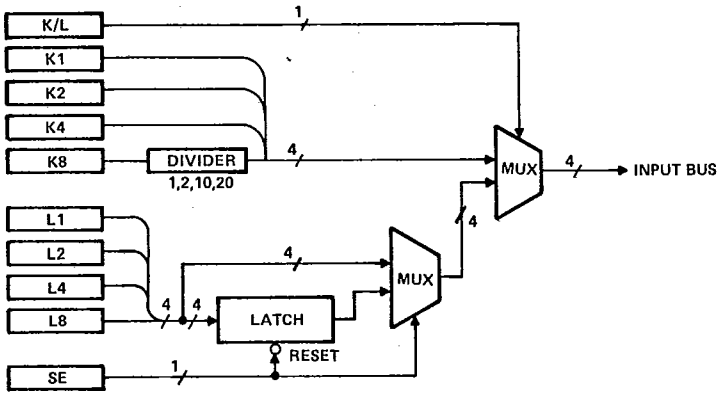


FIGURE 11 – TMS 1600/TMS 1670 INPUT BUS CONFIGURATION

TABLE 5
K/L SELECTOR AND SE MODE SELECTOR FUNCTIONS
(TMS 1600/TMS 1670 ONLY)

K/L SELECTOR	SE MODE SELECTOR	OPERATION
0	0	K-Input Data to Input Bus Latches are Reset
0	1	K-Input Data to Input Bus Latches are Active
1	0	L-Input Data to Input Bus Latches are Reset
1	1	L-Latch Data to Input Bus Latches are Active

5.5 K8 FREQUENCY DIVIDER

A frequency divider has been incorporated into the K8 input. Any one of four options (K8 direct pass, divided by factors of 2, 10, or 20) can be defined during device manufacture. This count is reset when the INIT signal goes to a high level.

5.6 DATA OUTPUT

All devices in the TMS 1400 PMOS series have two types of output channels, each of which have multiple purposes: the R-outputs and the O-outputs. The R-outputs are addressed by the Y-register and each output can be set or reset individually. The eight parallel O-outputs come from a five-bit-to-eight-bit code converter, which is the O-output PLA.

5.7 R-DATA OUTPUT

There are eleven R-outputs for the TMS 1400, ten for the TMS 1470, and sixteen for the TMS 1600/TMS 1670. The R-outputs are addressed by the Y-register. (The R addressing is not affected by the X register.)

The R-outputs are typically used to multiplex inputs and strobe O-output data to displays, external memories, and other devices. Additionally one R-output can strobe other R-outputs that represent variable data, since every R-output may be set or reset individually. For example, the Y register addresses each latch in turn; the variable data R-outputs are set or reset; and finally, the data strobe R-latch is set.

5.8 O-DATA OUTPUT

The internally latched eight parallel O-outputs may be used for a wide variety of applications: driving displays, driving speakers, communicating with external memories or processors, and a host of other functions. Thirty-two unique eight-bit patterns can be configured by the user.

5.9 DEVICE SOFTWARE OPERATION

5.9.1 Instruction Set

The TMS 1400 series standard instruction set is identical to the TMS 1100 instruction set, however, in order to extend addressing into the four chapters of ROM, the complement chapter instruction (COMC) has been replaced by a transfer page buffer to chapter buffer (TPC) which moves the two least significant bits of the page address buffer into the chapter address buffer.

5.9.2 O-Output PLA

The user defines a five-bit-to-eight-bit converter, called the O-output PLA, which specifies the state of the O lines for a given input. The four bits of the accumulator, and the output of the status latch provide for 32 unique O-output, eight-bit patterns.

5.9.3 Subroutine Calls

The TMS 1400 PMOS series devices have a three-level subroutine stack, and long branches can be executed during any level of subroutine. Subroutines can be of any length. Long branches can be executed at any time. Figure 12 is a flow diagram of subroutine calls.

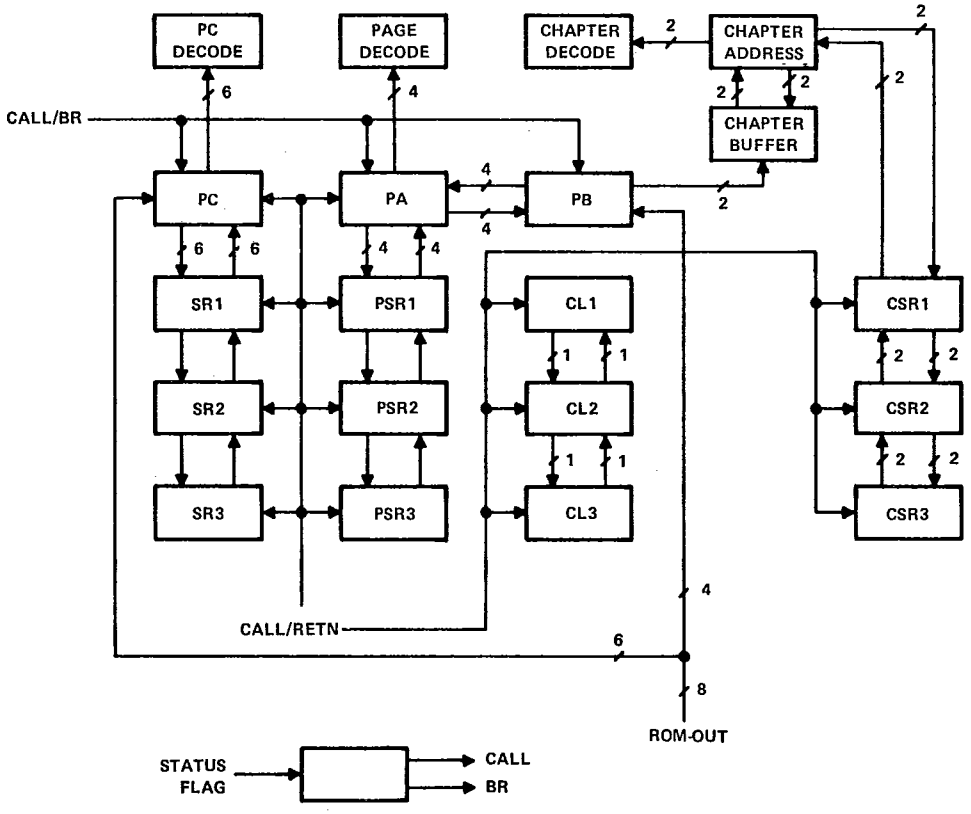


FIGURE 12 – SUBROUTINE/CALL FLOW

5.9.3.1 Action of Calls

a) IF S = 1

SR2 → SR3
SR1 → SR2
PC+1 → SR1
I(W) → PC

PSR2 → PSR3
PSR1 → PSR2
PA → PSR1
PB → PA

CL2 → CL3
CL1 → CL2
1 → CL1

CSR2 → CSR3
CSR1 → CSR2
CA → CSR1
CB → CA

b) IF S = 0

PC+1 → PC
1 → S

PA → PB

CA → CB

5.9.3.2 Action of RETN

a) IF CL1 = 1

SR1 → PC
SR2 → SR1
SR3 → SR2

PSR1 → PA,PB
PSR2 → PSR1
PSR3 → PSR2

CL2 → CL1
CL3 → CL2
0 → CL3
1 → S

CSR1 → CA, CB
CSR2 → CSR1
CSR3 → CSR2

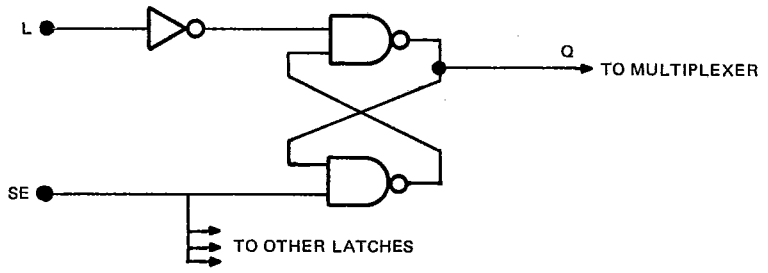
b) IF CL1 = 0

PC+1 → PC
1 → S

5.10 TMS 1400 NOTES

1. LATCH CIRCUITRY

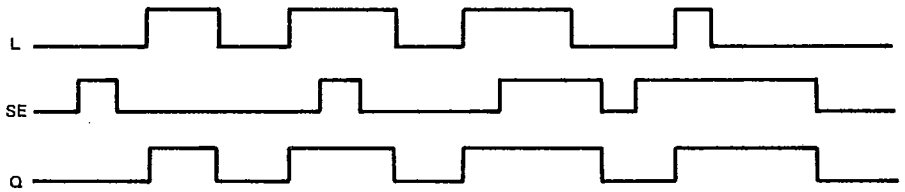
The latch circuitry at an input L is as follows:



This basically means that when (1) SE is low, Q follows L (i.e. the signal is passed)

(2) When SE is high, any high input on L is latched until SE goes low. If L is still high Q will remain high. If L had previously gone low and is still low, Q will not go low.

The following diagram shows what happens to Q for the various combinations of levels and pulses on L and SE.



2. K8 DIVIDER

There are divider options on K8. The division ratio can be 1, 2, 10 or 20.

6. TMS 1X70 MICROCOMPUTERS

6.1 INTRODUCTION

The TMS 1000 series flexibility is augmented by versions of high-voltage (35-volt) microcomputers, the TMS 1X70. The standard instruction set and operation is identical to that of the TMS 1X00. Architecturally, the devices are identical to the TMS 1X00 except that two additional O-output OR-matrix terms were added to provide a total of ten O outputs in the TMS 1270, a 40-pin package unit. The TMS 1X70 provides direct interface to low-voltage fluorescent displays. The TMS 1X70 interfaces with all circuits requiring up to 35-volt levels.

Figure 13, shows an interface to a 30-volt fluorescent display.

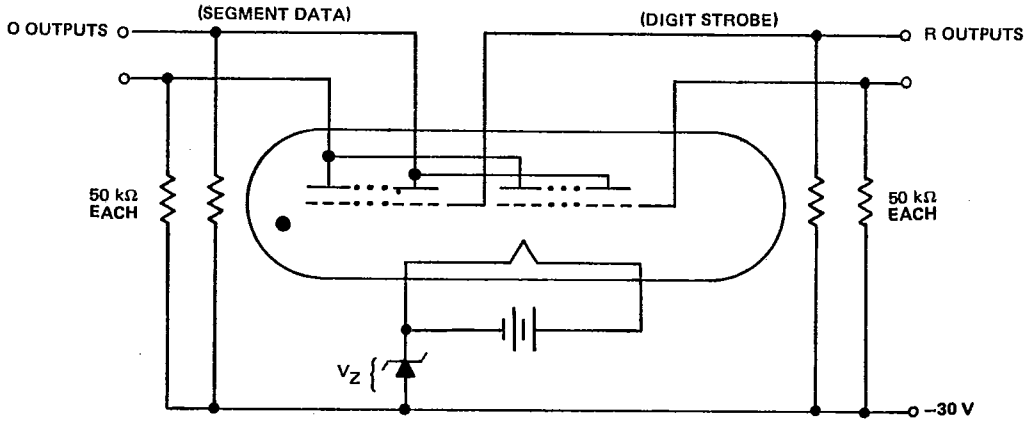


FIGURE 13 – STROBED FLUORESCENT DISPLAY INTERCONNECT

7. TMS 1X00 FAMILY POWER-UP AND INITIALIZATION (RESET)

7.1 INTRODUCTION

Power-up refers to when the power supply voltages are initially applied to the CPU. INITIALIZATION (RESET) is when the power supply voltage have already been applied and it's desired to restart program execution at the beginning of the algorithm.

7.2 POWER-UP

The TMS 1X00 family has the following two methods to clear the chip when the power supply voltages are properly applied.

7.2.1 Self-Contained Power-Up Latch

The TMS 1X00 family contains the internal power-up latch that automatically clears the chip at the time when power supply voltages are applied.

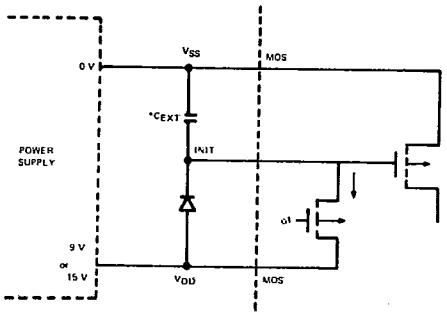
The power-up latch presets the program counter (PC ←0), page address register and page buffer register (PA and PB ←F_{16}), and call latch (CL ←0), as well as resetting O and R outputs registers to all ZEROes. Then program begins execution at fixed ROM address, PA = F, PC = 0. The RAM is not preset by power-up.

The system reset depends on the ROM program after the starting address.

One requirement of the internal power-up latch is that the power-up rise time must not exceed one millisecond.

7.2.2 INIT Input Pin

The INT input can be used to override the internal power-up latch. This method is recommended because it can be made independent of the power-rise time requirement, thereby providing a more reliable power-up. As shown in Figure 14, to control power-up requires up to two external components, a capacitor and diode. To ensure this function, a minimum of V_{SS}-1 volt is applied to the INIT input when the power supply voltages are initially applied to the chip. CPU clear is active while the INIT input maintains voltage level of V_{SS}-1 volt. The INIT input must remain at logical "1" level for at least 1 ms from the time when the power supply voltages reach at V_{DD} min.



*C_{EXT} (μF) = (0.06) X (Power supply rise time (msec))
CONDITIONS:
INIT
FUNCTIONS:
PC ←0, PA, PB ←F_{16}
Reset O and R outputs registers to all ZEROes CL ←0

FIGURE 14 – POWER-UP CLEAR BY INIT INPUT

7.3 Initialization (External Reset)

This function can be performed externally when the power supply voltages have already been applied. To perform an external reset the INIT input pin must remain within V_{SS-1} volt for a minimum of six instruction cycles. Both the K-inputs and R-outputs must be logical "0" level for a minimum of six instruction cycles preceding INIT going logical "0" level. A switch can be used for manual reset.

Power-up clear and manual reset circuit examples are shown in Figure 15.

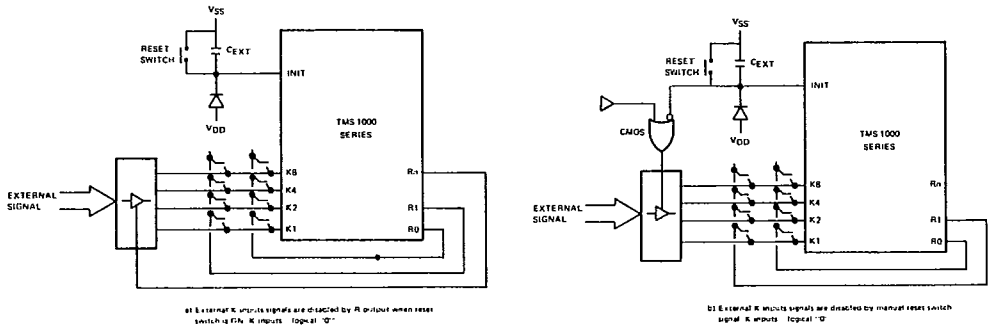


FIGURE 15 – EXAMPLE OF MANUAL RESET CIRCUIT
(Pull-down resistors are not shown on this circuit)

NOTES:
1. While power-up function is active, O_7 outputs pulses that are not related by user's algorithm. Care must be taken for peripheral interface circuits.
2. O-output register is reset to ZERO when power-up clear function is active, however, care must be taken for O-output because of user's defined O-output PLA code.
   If user defines ZERO to AND term for output PLA definition card, PLA outputs (O-output(O_0–O_7)) are user's defined eight-bit output code during power-up clear.
   For example:

$$\text{OUT (b) } 00 = \frac{O_7\ O_6\ O_5\ O_4\ O_3\ O_2\ O_1\ O_0}{0\ 0\ 1\ 1\ 1\ 1\ 1\ 1}$$

   In this example, O-output, O_5, O_4, O_3, O_2, O_1 and O_0 are logical "1" during power-up.
3. The following conditions must be required to ensure power-up clear when the power supply voltages are initially applied.
   - K inputs must be stayed at logical "0" level.
   - R outputs must not be pulled up to logical "1" level by external circuit.

8. TMS TMS 1000 CMOS MICROPROCESSOR FAMILY

8.1 INTRODUCTION

The TMS 1000C, TMS 1200C, TMS 1100C, and TMS 1300C are family members of the TMS 1000-series of four bit microcomputers. These CMOS microcomputers are designed for applications requiring lower power and/or higher speed than can be achieved with the PMOS series devices. The TMS 1000C and TMS 1200C contain a 1024-word instruction ROM, 64-word RAM, and a four-bit arithmetic logic unit (ALU) on a single semiconductor chip. The TMS 1100C and the TMS 1300C contain a 2048-word instruction ROM, 128-word RAM, and a four-bit ALU on a single chip. The customer's specifications determine the software program to be imbedded in the ROM during chip manufacture. This unique characteristic is produced in wafer processing by changing a single-level mask pattern. The basic characteristics of the TMS 1000 CMOS Series are listed in Table 6.

The TMS 1100C is architecturally similar to the TMS 1000C, except that it contains twice the memory capacity – 16,384 bits of ROM and 512 bits of RAM. The instruction set for the TMS 1100C, shown in Table 4, is identical to the TMS 1100 PMOS instruction set.

The TMS 1300C is an expanded I/O version of the TMS 1100, with input/output features identical to the TMS 1200 CMOS. The TMS 1300C has two 4-bit input ports, 16 individually addressable R lines, and 8 parallel O lines.

TABLE 6 – TMS 1000 CMOS SERIES FEATURES

	TMS 1000C	TMS 1200C	TMS 1100C	TMS 1300C
Package Pin Count	28 Pins	40 Pins	28 Pins	40 Pins
Instruction Read Only Memory	1024 X 8 Bits (8,192 Bits)		2048 X 8 Bits (16,384 Bits)	
Data Random Access Memory	64 X 4 Bits (256 Bits)		128 X 4 Bits (512 Bits)	
Input/Sense Input	4/0	8/4	4/0	8/4
"R" Individually Addressed Output Latches	10	16	10	16
"O" Parallel Latched Data Outputs Latches	8 Bits			
Working Registers	2-4 Bits Each			
Standard Instruction Set	See Table 3		See Table 4	
HALT Mode (Power Down)	Yes			
On-Chip Oscillator	Yes			
Power Supply/Typical Dissipation	5 V/3.5 mW		5 V/5 mW	

8.2 TIMING RELATIONSHIPS AND OSCILLATOR OPERATION

Six clock pulses constitute one instruction cycle. The actual machine cycle period is determined by either a fixed external resistor and capacitor connected to the OSC1 and OSC2 pins, or an external clock input frequency.

If the internal oscillator is used, OSC1 and OSC2 are connected with a resistor; and a capacitor is connected between OSC1 and V_{SS}. The frequency of operation for given components is shown in Figure 41. The current drain I_{DD} is greatly affected by the resistor selected; hence for lowest power consumption a resistor greater than 10K ohms is recommended, and the user should select a capacitor value for the desired clock frequency.

If an external clock is desired, the clock source should be connected to OSC1. OSC2 should not be connected but allowed to float.

8.3 INITIALIZATION

Power-up refers to the initial application of the power supply voltage to the device. Reset consists of restarting program execution at the beginning of the algorithm any time after the initial power-up sequence.

The TMS 1000C/1200C power-up mode and reset mode differ only in that during power-up mode the K-inputs are in a don't care condition; whereas, during reset mode the K-inputs must be at zero level.

8.3.1 Power-Up

Initializing the TMS 1000C/1200C consists of resetting the page address register, the program counter and the O and R-outputs. The internal power-up latch will execute a power-up with no external components so long as the power-supply rise time does not exceed 300 μsec. INIT must be tied to V_{SS} and no external components are needed. A circuit similar to Figure 16 may be used with slower power-supplies. Some of the components are optional depending upon the application.

8.3.2 External Reset

To perform an external reset the INIT-input pin must remain high for a minimum of six instruction cycles. The K-inputs must be low for a minimum of six instruction cycles preceding INIT going low, which resets the ROM address. While INIT is high, the O and R-outputs are reset.

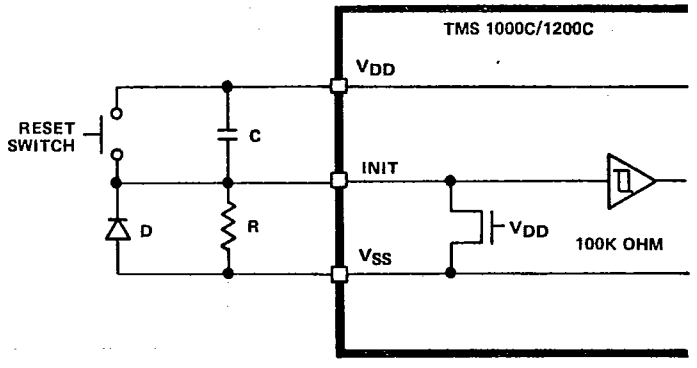


FIGURE 16 – TYPICAL RESET CIRCUIT

8.4 HALT

HALT is used to reduce power consumption in the standby state. Normal operation of the TMS 1000C/1200C devices requires 3.5 mW, but HALT mode typically consumes less than 0.5 μW. This capability is advantageous for use in battery operated portable systems or battery/capacitor operated backup systems. The TMS 1000C/1200C goes into the HALT mode at the end of the machine cycle after the HALT-input is brought to a high level. Output lines are unaffected by the HALT mode. When HALT is returned to a low level, the TMS 1000C/1200C starts execution from the next program counter location. The HALT mode is normally a high impedance input and must be tied to V_{SS} if not used. When the INIT-pin is high the HALT-input is pulled low internally.

8.5 DATA INPUT

8.5.1 TMS 1000C Data Input

There are four data inputs to the TMS 1000C circuit: K1, K2, K4 and K8. Each time an input word is requested, the data path from the K-inputs is enabled to the adder. The inputs are either tested for a high level ($\approx V_{DD}$) or the input data is stored in the accumulator for future use. The R-outputs usually multiplex inputs such as keys and other data onto the K-input lines. Other input interfaces are possible. Data from the K-inputs can be stored periodically in synchronization with the predetermined data rate of the external device. Thus, multiple four-bit words can be requested and stored with only one R-output supplying the control signal.

8.5.2 TMS 1200C Data Input

The TMS 1200C device has eight data inputs: K1, K2, K4, K8 and L1, L2, L4, L8 (see Figure 17). These two ports are multiplexed internally into a four-bit bus. In addition, the TMS 1200C has two control inputs: the K/L selector and the SE Mode Selector. The K/L control input has an internal pull-down resistor so that when no input is applied or when the K/L input is a low level, the K-input is selected.

When the K/L input is at a high level, the four-bit L-input port is selected. The L-input port has two modes: a pass mode and a sense mode. The SE Mode Selector input has an internal pull-down resistor, and normally the pass mode is selected. When the SE Mode Selector is at a high level, the sense mode is selected. During sense mode, positive momentary inputs are latched. Table 7 summarizes functions of K/L and SE Mode Selector inputs.

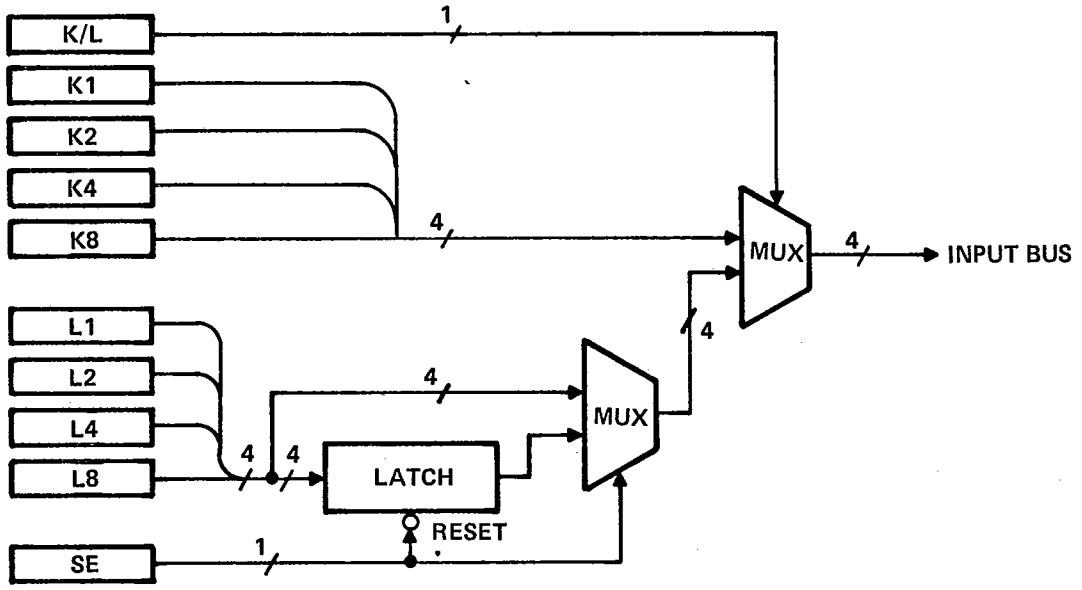


FIGURE 17 – TMS 1200C INPUT BUS CONFIGURATION

TABLE 7
K/L SELECTOR AND SE MODE SELECTOR FUNCTIONS
(TMS 1200C ONLY)

K/L SELECTOR	SE MODE SELECTOR	OPERATION
0	0	K-Input Data to Input Bus Latches are Reset
0	1	K-Input Data to Input Bus Latches are Active
1	0	L-Input Data to Input Bus Latches are Reset
1	1	L-Latch Data to Input Bus Latches are Active

8.6 DATA OUTPUT

Both devices have two output channels with multiple purposes: the R-outputs and the O-outputs. Ten (TMS 1000C) or sixteen (TMS 1200C) internal latches store the R-output data. The R-outputs are individually addressed by the Y register. Each addressed bit can be set or reset individually. The eight parallel latched O-outputs come from a five-bit-to-eight-bit code converter, which is the O-output PLA.

8.6.1 R-Data Output

The R-outputs are typically used to multiplex inputs and strobe O-output data to displays, external memories, and other devices. Also, one R-output can strobe other R-outputs that represent variable data, because every R-output may be set or reset individually. For example, the Y register addresses each latch in turn; the variable data R-outputs are set or reset; and finally, the data strobe R-latch is set.

8.6.2 O-Data Output

The internally latched eight parallel O-outputs may be used for a wide variety of applications: driving displays, driving speakers, communicating with external memories or processors, and hosts of other functions. Thirty-two unique eight-bit patterns can be configured by the user.

8.7 INSTRUCTION SETS

8.7.1 Standard Instruction Set

Table 3 defines the TMS 1000C/1200C standard instruction set with description, mnemonic, and status effect. The instruction mnemonics are identical to the TMS 1000/1200 PMOS series which are intended for easy reference to the functional description. Most routines may be transferred from the PMOS to the CMOS device with minimal changes.

8.8 O-OUTPUT PLA

The user defines a five-bit-to-eight-bit converter, called the O-output PLA, which specifies the state of the O lines for a given input. The four bits of the accumulator, and the output of the status latch provide for 32 unique O-output, eight-bit patterns.

8.9 SUBROUTINE CALLS

The TMS 1000C/1200C devices have a three-level subroutine stack, and long branches can be executed during any level of subroutine. Subroutines can be of any length and are not restricted to 64 words as is the case with the TMS 1000/1200 PMOS series. Long branches can be executed at any time. Figure 18 is a flow diagram of subroutine calls.

8.9.1 Action of Call

a) IF S = 1

SR2 → SR3	PSR2 → PSR3	CL2 → CL3
SR1 → SR2	PSR1 → PSR2	CL1 → CL2
PC+1 → SR1	PA → PSR1	1 → CL1
I(W) → PC	PB → PA	

b) IF S = 0

PC+1 → PC	PA → PB
1 → S	

8.9.2 Action of RETN

a) CL1 = 1

SR1 → PC
SR2 → SR1
SR3 → SR2

PSR1 → PA
PSR2 → PSR1
PSR3 → PSR2
PA → PB

CL2 → CL1
CL3 → CL2
0 → CL3
1 → S

b) CL1 = 0

PC+1 → PC
1 → S

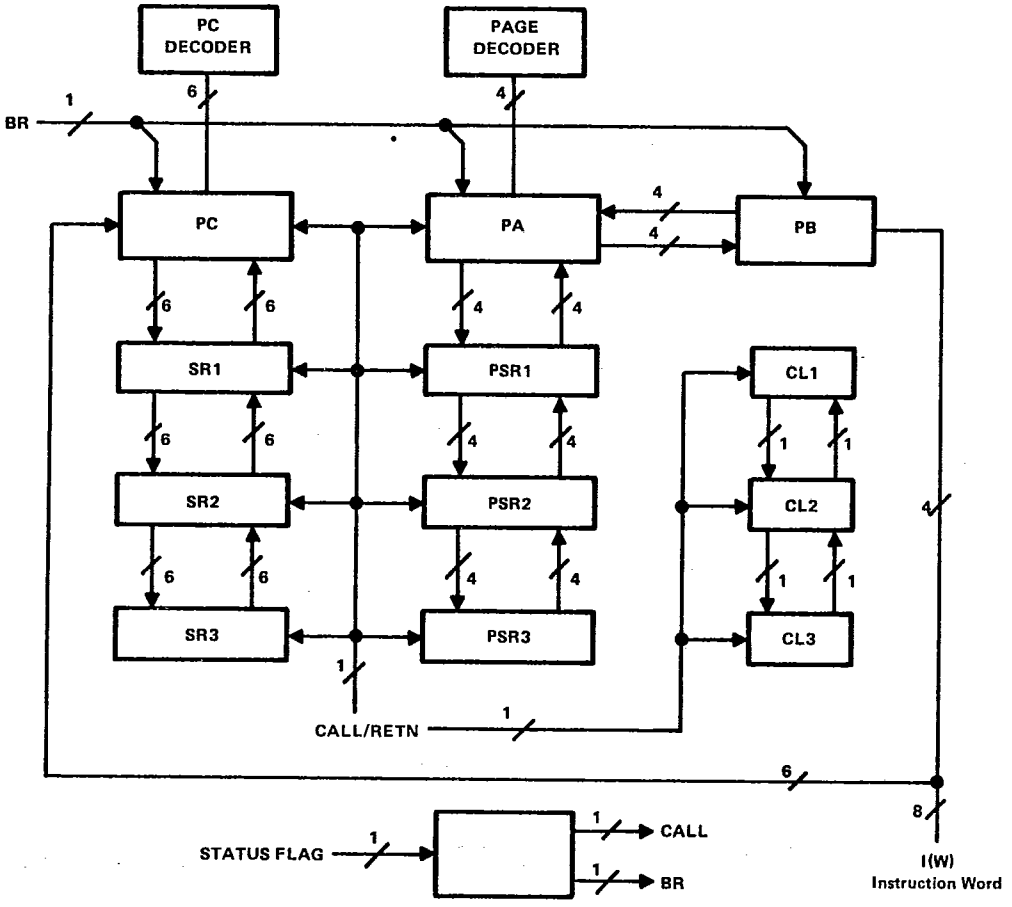


FIGURE 18 – SUBROUTINE/CALL FLOW

8.10 FUTURE CMOS SERIES PRODUCTS

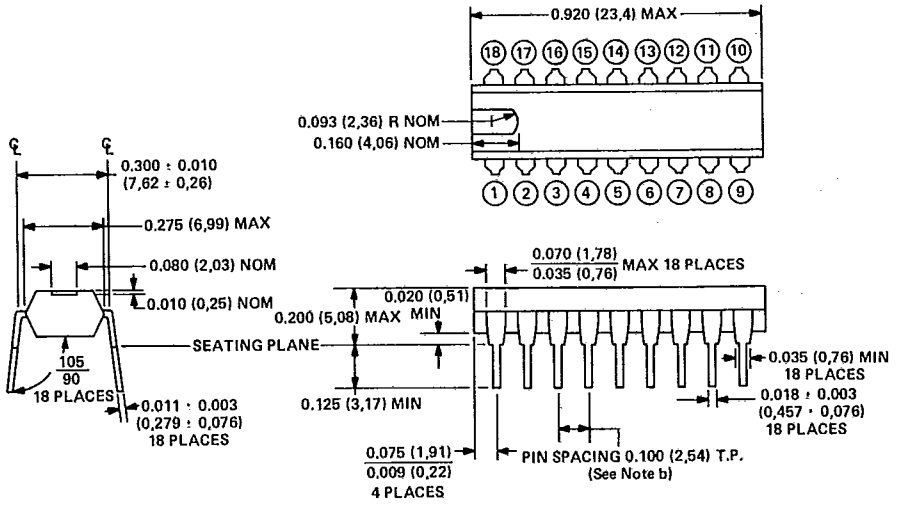
Future products in the CMOS Series will offer outputs that interface to the high-voltage required for displays. These devices will be software compatible with the standard CMOS products, but will be manufactured with both inputs and outputs which can withstand 25 V. Features of these devices are outlined below:

Feature \ Device	1070C	1270C
Output Voltage (Note 1)	-25V	-25V
Package Pin Count	28	40
Instruction ROM	1K x 8	1K x 8
Data RAM	64 x 4	64 x 4
K/L Inputs	4/0	4/4
R Lines	10	16
O Lines	8	8
Power Supply & Dissipation	5V/5mW	5V/5mW
Maximum Oscillator Frequency	1MHz	1MHz
Temperature Range	0°-70°C	0°-70°C
Software Evaluator With External Instruction Memory	SE 1000C	SE 1000C
AMPL 1000	YES	YES

NOTE 1: For the VF version, with appropriate current limiting, the absolute maximum supply voltage that may be applied to the output terminal at V_{DD} = 5V.

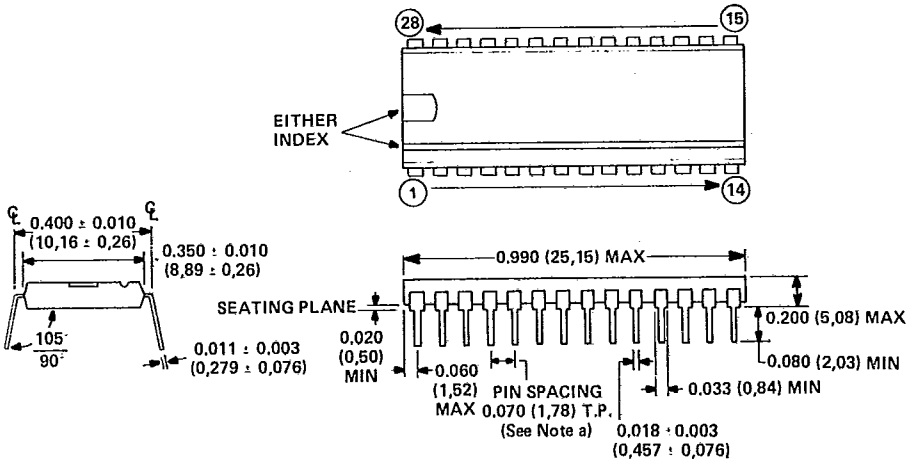
18. MECHANICAL DATA

PLASTIC					CERAMIC
18-PIN	28-PIN		40-PIN		84-PIN
100 MIL PIN CENTER	70 MIL PIN CENTER	100 MIL PIN CENTER	70 MIL PIN CENTER	100 MIL PIN CENTER	100 MIL PIN CENTER
N	NF	N	NF	N	J
1976	1000	1000	1200	1200	SE-1000P
	1070	1070	1270	1270	SE-1100P
	1100	1100	1300	1300	SE-1000C
	1170	1170	1600	1370	SE-1100C
	1400	1400	1670	1600	SE-1400P
	1470	1470	1200C	1670	
	1700	1700	1270C	1200C	
	1000C	1000C	1300C	1270C	
	1070C	1070C		1300C	
	1100C	1100C		1025	
		1121		1027	
		1117			
		1024			
		1026			



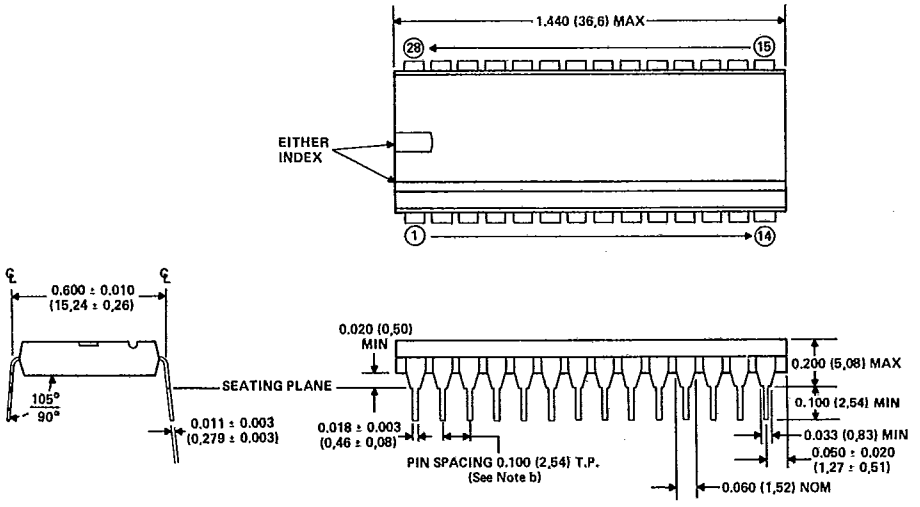
NOTES: a. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0.26) of its true longitudinal position.

FIGURE 50 – 18-PIN N PLASTIC PACKAGE, 0.100" PIN CENTER SPACING, 0.300" PIN ROW SPACING



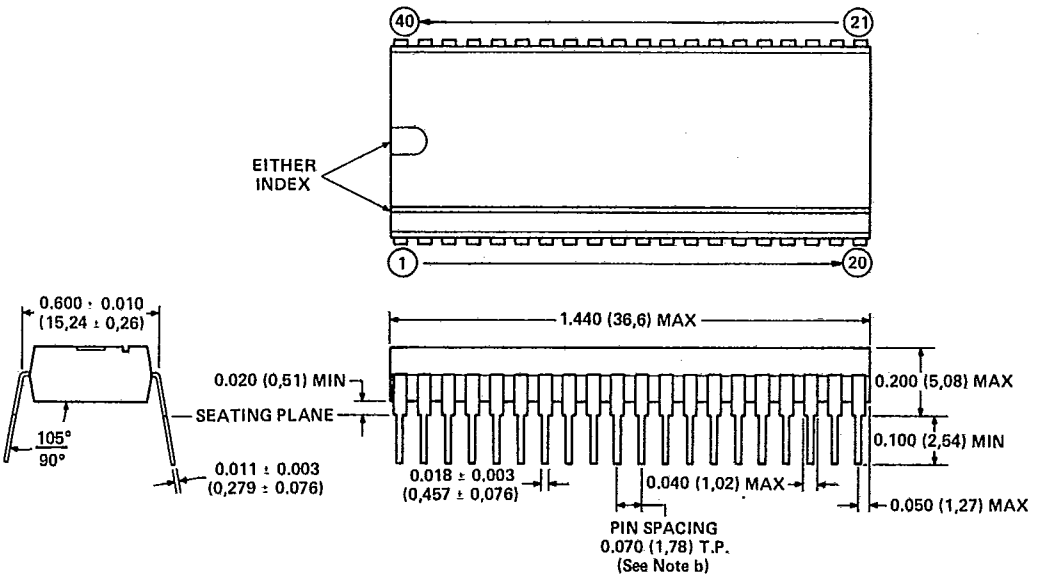
NOTES: a. All linear dimensions are in inches and parenthetically in millimeters, Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0.26) of its true longitudinal position.

FIGURE 51 – 28-PIN NF PLASTIC PACKAGE, 0.070" PIN CENTER SPACING, 0.400" PIN ROW SPACING



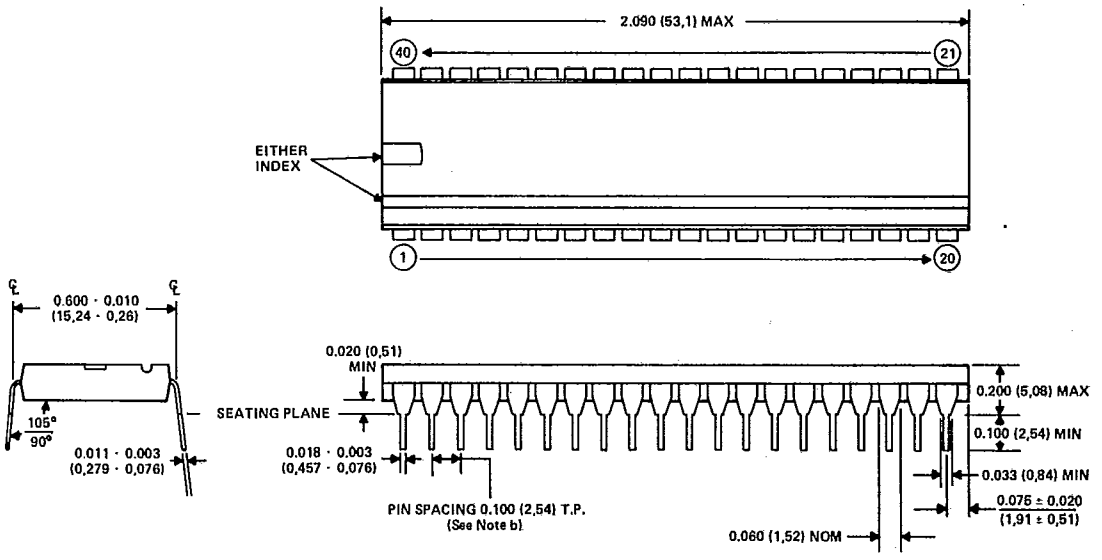
NOTES: a. All linear dimensions are in inches and parenthetically in millimeters, Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0.26) of its true longitudinal position.

FIGURE 52 – 28-PIN N PLASTIC PACKAGE 0.100" PIN CENTER SPACING, 0.600" PIN ROW SPACING



NOTES: a. All linear dimensions are in inches and parenthetically in millimeters, inch dimensions govern.
b. Each pin centerline is located within 0.010 (0.26) of its true longitudinal position.

FIGURE 53 – 40-PIN NF PLASTIC PACKAGE, 0.070" PIN CENTER SPACING, 0.600" PIN ROW SPACING



NOTES: a. All linear dimensions are in inches and parenthetically in millimeters, inch dimensions govern.
b. Each pin centerline is located within 0.010 (0.26) of its true longitudinal position.

FIGURE 54 – 40-PIN N PLASTIC PACKAGE, 0.100" PIN CENTER SPACING, 0.600" PIN ROW SPACING

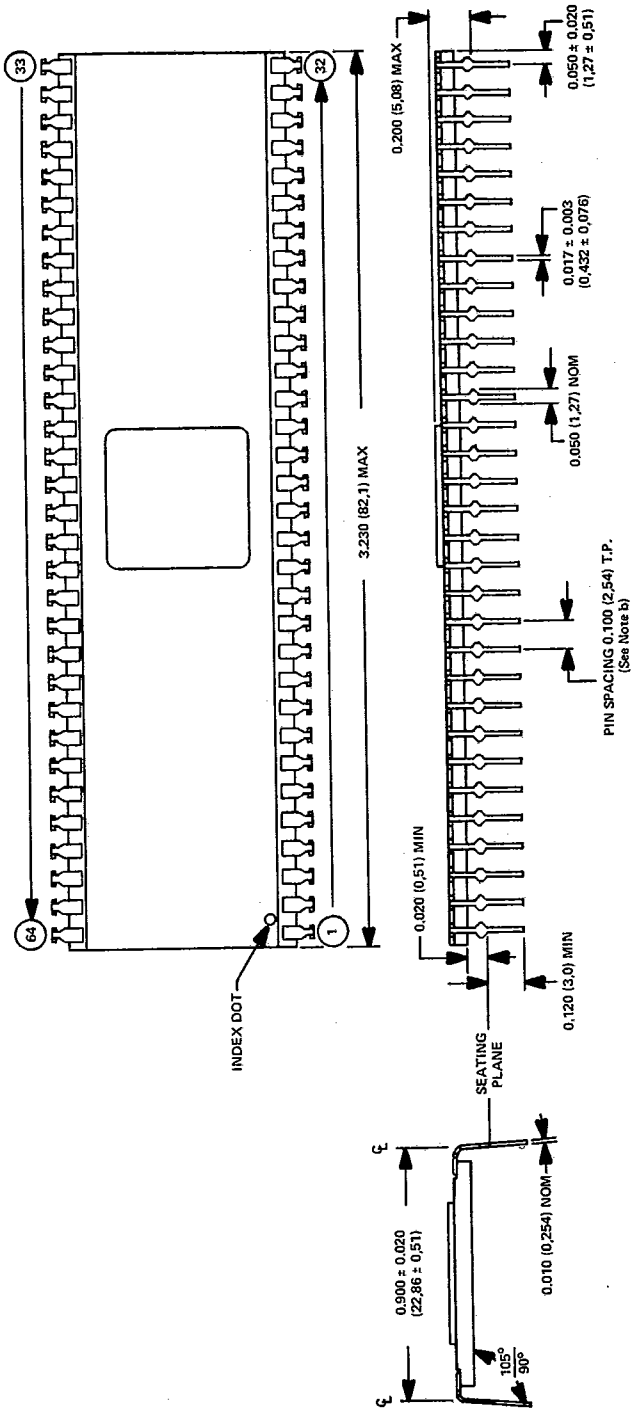


FIGURE 55 – 64-PIN J CERAMIC PACKAGE, 0.100'' PIN CENTER SPACING, 0.900'' PIN ROW SPACING

NOTES: a. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0.26) of its true longitudinal position.