UltraSPARC® IV Processor

Designed for mission-critical enterprise, high performance technical computing (HPTC), and compute-intensive applications.

Key Highlights

- 64-bit open standards-based SPARC® V9 architecture compatible with VIS™ Instruction Set

- First milestone in the CMT processor roadmap from Sun

- Dual-threaded processor based on UltraSPARC III pipeline

- Provides up to 2 times the application throughput of UltraSPARC III processor

- Binary compatibility with previous generations of SPARC processors

- Can provide an upgrade path for servers powered by UltraSPARC III processor

- On-chip tags for 16 MBs of off-chip level 2 cache (8 MB per pipeline)

- On-chip memory controller supporting up to 16 GBs of DRAM

- Shared system interface to the Sun™ Fireplane interconnect

- Maximum power consumption: 108 W at 1.35 V, 1.2 GHz

- 1368-pin LGA package

- Clock frequencies: 1.05 and 1.2 GHz

Executing on Sun's Throughput Computing Strategy

Throughput Computing is the underlying strategy of Sun's new family of UltraSPARC® processors, which are designed to significantly increase real-world application processing throughput. At the heart of this new strategy is Chip Multithreading (CMT), a design concept that would eventually allow processors to execute tens of threads simultaneously. The dual-threaded UltraSPARC IV processor marks the first milestone in Sun's CMT processor roadmap.

Developed in concert with the Solaris™ Operating Environment to meet the performance, reliability, and scalability requirements of mission-critical enterprise, HPTC, and other compute-intensive applications, the UltraSPARC IV processor can almost double the current UltraSPARC III processor-based system throughput.

The UltraSPARC IV processor is binary compatible with previous generations of SPARC processors and will support both versions 8 and 9 of the Solaris Operating Environment. This is consistent with Sun's commitment to protecting customers' investments in software and training. The UltraSPARC IV processor can also provide an upgrade path for servers powered by the existing UltraSPARC III processor.

UltraSPARC IV Processor

UltraSPARC® IV Processor Features and Benefits

Processor Features

Dual thread execution based on two UltraSPARC III pipelines

L1 cache (per pipeline): 64 KB data, 32 KB instruction, 2 KB write, 2KB prefetch

Level 2 cache : On-chip tags for 16 MBs off-chip, 2-way set-associative, LRU eviction policy, and reduced sub-blocked cache. Exclusive access to 8MB per pipeline

On-chip SDRAM memory controller

Shared system interface to Sun Fireplane interconnect system bus

Enhanced Floating Point Unit with additional hardware support for IEEE 754-1985 exceptions

CMT enhancements support Sun Standard CMT model helping to assure compatibility with current and future operating system interaction

Pipeline Design

14-stage non-stalling pipeline

Sustainable 4-way superscalar

Six parallel execution units (2 integer, 1 branch, 1 load/store, 2 FP/VIS)

Speculative execution of instructions after branches

Speculative memory loads

95% branch prediction accuracy (16 K-entry branch prediction table)

Data Integrity

EDC (Error Detection and Correction) using ECC (Error Correction Codes) or parity on all major SRAMs and data buses inside and outside the processor

Error removal and recovery system to help prevent the propagation of copy-back errors

Diagnostic bus to monitor processor internals and address system errors, independent of the main system interface

Memory Subsystem

Integrated memory controller

Memory size: 16 GB per processor

Memory Interface: SDRAM

Enhanced Support from Solaris

Multiprocessor (MP) support provided by the Solaris Operating Environment

System models for tightly coupled, shared memory and for large multi-processor clustered architectures (snoop and directory-based)

System Bus Architecture

150 MHz clock frequency with peak bandwidth of 2.4 GB/s

Distributed bus arbitration

Fast on-chip snoop tags to maintain system bus performance

Large, wide data crossbar switches

Processor memory bandwidth scales with number of processors

Physical Characteristics

Package: 1368-pin LGA

Transistor count: 66 million

Maximum power dissipation: 108 W at 1.35 V, 1.2 GHz

Process: TI's CMOS 0.13μ, 7-layer copper
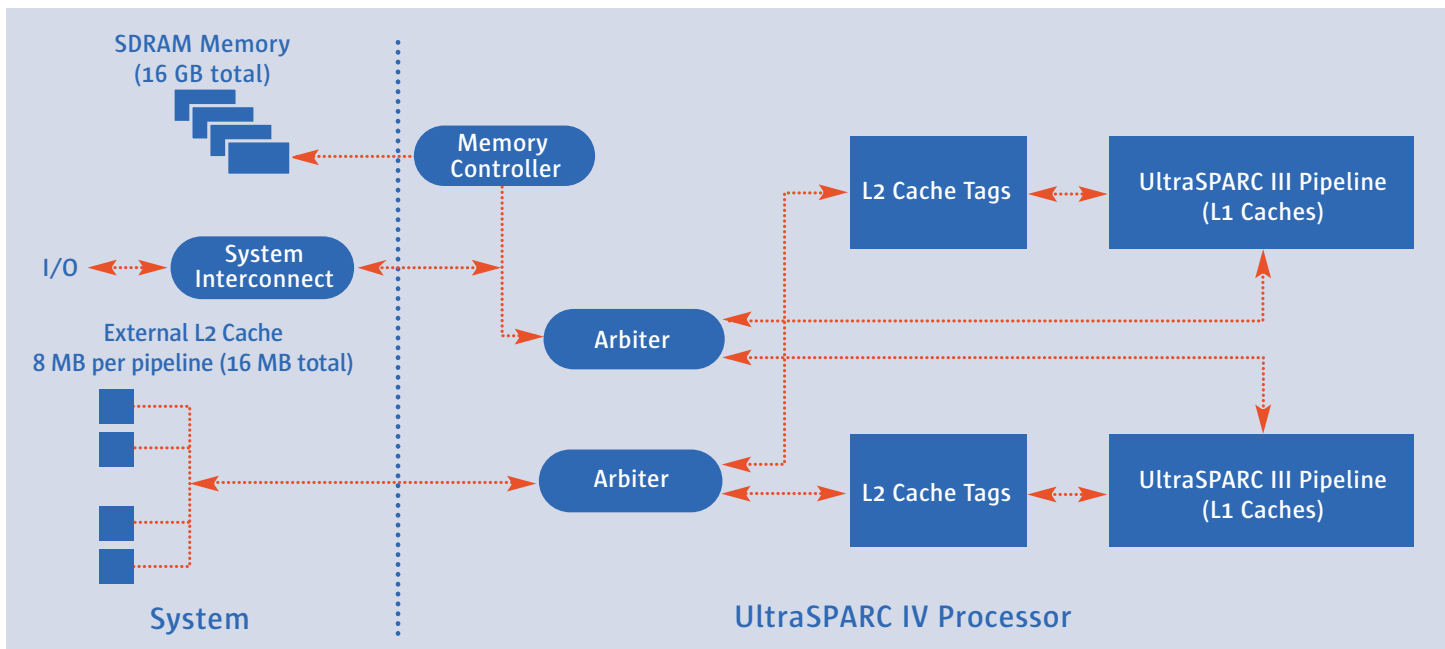
UltraSPARC IV Processor Block Diagram

We make the net work.