Ordering number : ENN*6697

CMOS IC

LC865520B/16B/12B/08B/04B

8-Bit Single Chip Microcontroller with On-Chip 20/16/12/08/04K-Byte ROM and 512-Byte RAM

Preliminary

Overview

The LC865520B/16B/12B/08B/04B are 8-bit single chip microcontrollers with the following one-chip features:

- CPU : Operable at a minimum bus cycle time of 0.5µs
- On-chip ROM Capacity : 20K/16K/12K/8K/4K bytes
- On-chip RAM Capacity : 512 bytes (LC865520B/16B/12B/08B/04B)
- 16-bit timer/counter (can be divided into two 8 bit timers)
- 16-bit timer/PWM (can be divided into two 8 bit timers)
- 8-channel × 8-bit AD converter
- Two 8-bit synchronous serial-interface circuits
- 13-source 10-vectored interrupt system

Features

(1) Read Only Memory (ROM)
: LC865520B 20480 × 8 bits
: LC865516B 16384 × 8 bits
: LC865512B 12288 × 8 bits
: LC865508B 8192 × 8 bits
: LC865504B 4096 × 8 bits

(2) Random Access Memory (RAM) : LC865520B/16B/12B/08B/04B 512 × 8 bits

(3) Bus Cycle Time/Instruction Cycle Time

The LC865520B/16B/12B/08B/04B are constructed to read ROM twice within one instruction cycle. It has 1.7 times the performance capability for the same instruction cycle compared to our 4-bit microcontrollers (LC66000 series).
Bus cycle time indicates the speed to read ROM.

Bus cycle time	Instruction cycle time	Clock divider	System clock oscillation	Oscillation Frequency	Voltage
0.5µs	1µs	1/1	Ceramic (CF)	6MHz	4.5V to 6.0V
2µs	4µs	1/2	Ceramic (CF)	3MHz	2.5V to 6.0V
7.5µs	15µs	1/2	Internal RC	800kHz	2.5V to 6.0V
183µs	366µs	1/2	Crystal (XTAL)	32.768kHz	2.5V to 6.0V

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(4) Ports

- Input/output ports : 3 ports (16 terminals : port 1,7,8)
  Input/output programmable for each bit individually
- Maximum 15V withstand tolerance input/output port : 2 ports (15 terminals)
  Input/output programmable in nibble units : 1 port (8 terminals : port 0)
  (When the N-channel open drain output is selected, input/output can be specified by bit.)
  Input/output programmable for each bit individually : 1 port (7 terminals : port 3)
- Input ports : 2 ports (6 terminals : port 7,8)

(5) AD converter

- 8-channel × 8-bit AD converter

(6) Serial interface

- 1 channel × 16-bit serial interface (8-bit transmission available by program)
- 1 channel × 8-bit serial interface
  LSB first/MSB first-function available
- An internal 8-bit baud-rate generator is common to both serial-interface circuits.

(7) Timer

- Timer 0
  16-bit timer/counter
  2-bit prescaler + 8-bit programmable prescaler
  Mode 0 : Two 8-bit timers with programmable prescaler
  Mode 1 : 8-bit timer with programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of Timer is tCYC. (tCYC: cycle time)

- Timer 1
  16-bit timer/PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable-bit PWM (9-16bits)
  In Mode 0 and Mode 1, the resolution of Timer and PWM is tCYC.
  In Mode 2 and Mode 3, the resolution of Timer and PWM is selectable by program: tCYC or 1/2 tCYC.

- Base timer
  Generates an overflow every 500ms for a clock application (using 32.768kHz crystal oscillation for the base timer oscillator).
  Generates an overflow every 976μs, 3.9ms, 15.6ms or 62.5ms (using 32.768kHz crystal oscillation for the base timer clock)
  Clock for the base timer is selectable from 32.768kHz crystal oscillation, system clock, or programmable prescaler output of Timer 0.

(8) Buzzer output

- Built-in 4KHz and 2KHz buzzer generation function (using 32.768kHz crystal oscillation for the base timer oscillator)

(9) Remote receiver circuit (share with P73/INT3/T0IN terminal)

- Noise Rejection function (The filtering time of the noise rejection filter (1tCYC/16tCYC/64tCYC) can be switched by program.) (tCYC: instruction-cycle-time)
- Polarity switch function

(10) Watchdog timer

- External RC circuit is required.
- Interrupt or system reset is activated when the timer overflows.

(11) Interrupt

- 13-source and 10-vectored interrupt function:
  1. External interrupt INT0 (including watchdog timer)
  2. External interrupt INT1
  3. External interrupt INT2, Timer/counter T0L (lower 8 bits of Timer 0)
  4. External interrupt INT3, Base timer
  5. Timer/counter T0H (upper 8 bits of Timer 0)
  6. Timer T1L (lower 8 bits of Timer 1), Timer T1H (upper 8 bits of Timer 1)
  7. Serial interface SIO0
  8. Serial interface SIO1
  9. AD converter
  10. Port 0
- Built-in Interrupt Priority control register

  Three interrupt priorities are supported (low, high and highest) and multi-level nesting is possible. Low or high priority level can be assigned to the 11 interrupt sources of interrupts 3 to 10 shown above by the interrupt priority control register. For the external interrupt INT0 and INT1(interrupt 1 and 2), low or highest can be set regardless of the interrupt priority register.

(12) Sub-routine stack levels

- A maximum of 128 levels (set stack inside RAM)

(13) Multiplication and division

16 bits × 8-bit (7 instruction-cycle-times)
16 bits / 8-bit (7 instruction-cycle-times)

(14) 3 types of oscillation circuits

- Built-in RC oscillation circuit used for the system clock.
- CF oscillation circuit used for the system clock.
- Crystal oscillation circuit used for the system clock and the time-base clock.

(15) Standby function

- HALT mode

  The HALT mode stops the program execution, which minimizes power consumption. This operation mode can be released by a system reset or an interrupt request.
- HOLD mode

  The HOLD mode stops all oscillation circuits: CF, RC and Crystal oscillations. This mode can be released by the following conditions.
  - Feed "L" level to the reset terminal ($\overline{\text{RES}}$)
  - Feed the selected level to P70/INT0, P71/INT1 terminals
  - Feed "L" level to the Port 0

(16) Shipping form

- DIP42S
- QIP48E

(17) Development tools

Evaluation (EVA) chip	:	LC866096
EPROM version	:	LC86E5420
One time version	:	LC86P5420
Emulator	:	EVA-86000 + ECB867100 (Evaluation chip board) + POD865400 (POD)

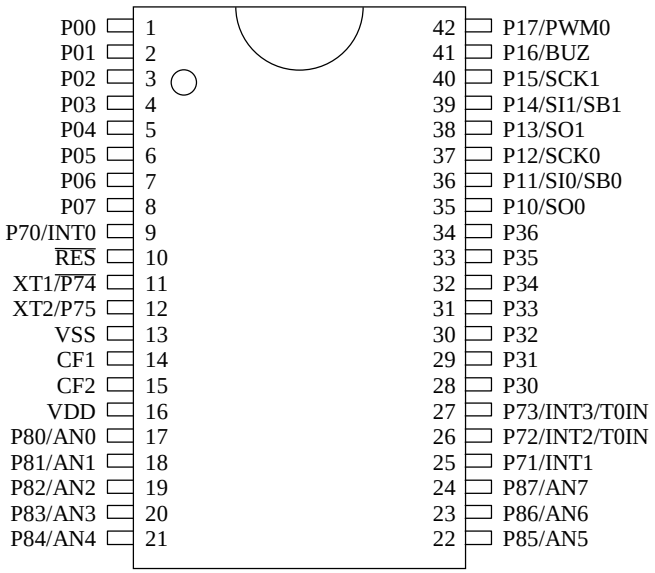
Notice for use

1. The following must be taken into consideration by the user:

Oscillation frequency range for system clock.	Supply voltage range	Clock Divider	Notes
15kHz to 30kHz	4.5V to 6.0V	1/1	Can not use 1/2 divider
30kHz to 6MHz		1/1,1/2	
15kHz to 30kHz	2.5V to 6.0V	1/1	Can not use 1/2 divider
30kHz to 1.5MHz		1/1,1/2	
1.5MHz to 3MHz		1/2	Can not use 1/1 divider
Internal RC oscillation	4.5V to 6.0V	1/1,1/2	
	2.5V to 6.0V	1/2	Can not use 1/1 divider

Pin Assignment

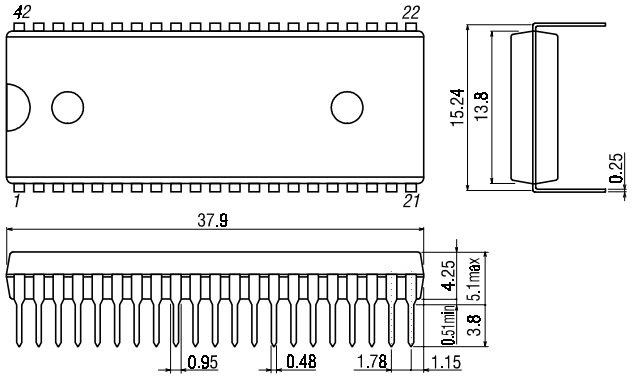
•DIP42S



Package Dimension

(unit : mm)

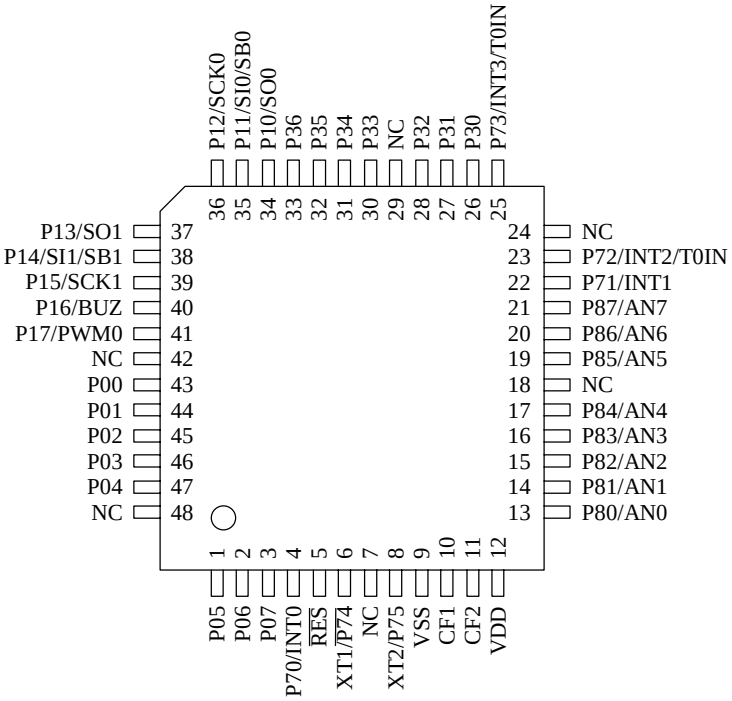
3025B



SANYO : DIP-42S(600mil)

Pin Assignment

•QIP48E

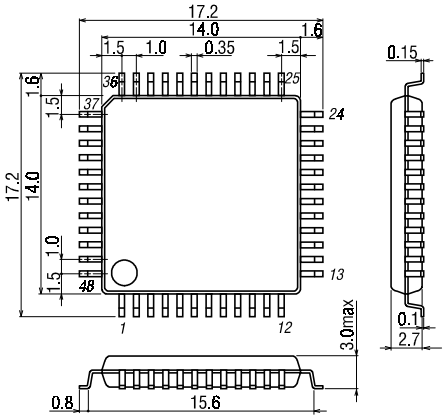


*Leave NC pins open.

Package Dimension

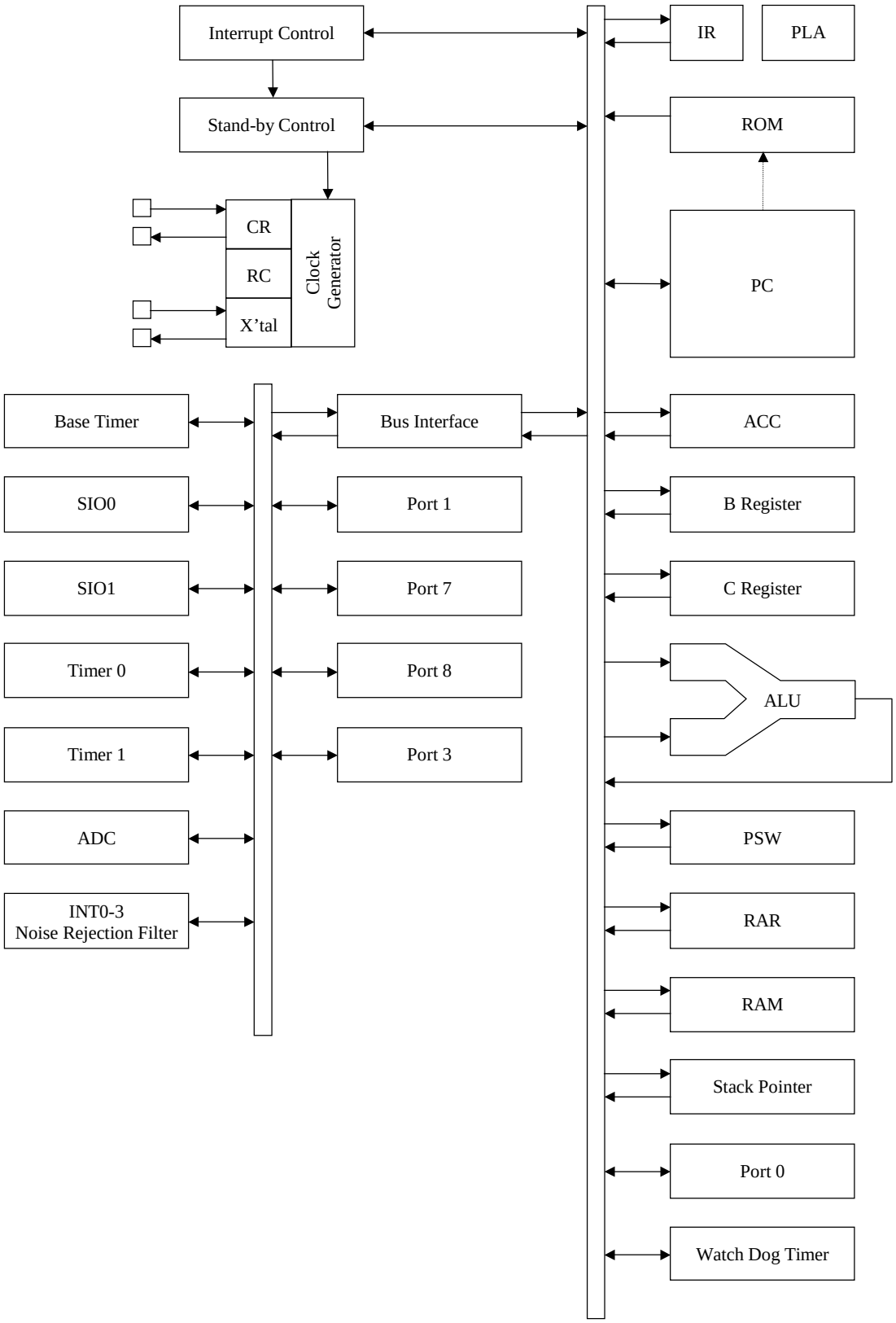
(unit : mm)

3156



SANYO : QIP-48E

System Block Diagram



Pin description

<table>
<tr><th>Name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>VSS</td><td>-</td><td>Power terminal (-)</td><td>-</td></tr>
<tr><td>VDD</td><td>-</td><td>Power terminal (+)</td><td>-</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>• 8-bit input/output port
• Port 0 interrupt input
• Data direction programmable in nibble units
• HOLD release input
• A withstand tolerance of 15V when selecting N-channel open drain output</td><td>• Pull-up resistor :
Provided/Not provided
(specified in nibble units)
• Output form :
CMOS/N-channel open drain
(specified by bit)</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable for each bit individually
• Other functions
P10 SIO0 data output
P11 SIO0 data input, bus input/output
P12 SIO0 clock input/output
P13 SIO1 data output
P14 SIO1 data input, bus input/output
P15 SIO1 clock input/output
P16 Buzzer output
P17 Timer 1 output (PWM0 output)</td><td>• Output form :
CMOS/N-channel open drain
(specified by bit)</td></tr>
<tr><td>PORT3
P30 to P36</td><td>I/O</td><td>• 7-bit input/output port
• Data direction programmable for each bit individually
• A withstand tolerance of 15V when selecting N-channel open drain output</td><td>• Pull-up resistor :
Provided/Not provided
(specified by bit)
• Output form :
CMOS/N-channel open drain
(specified by bit)</td></tr>
<tr><td>PORT7

P70 to P73

$\overline{P74}$, P75</td><td>

I/O

I</td><td>• 4-bit input/output port
• Data direction programmable for each bit individually
• 2-bit input port
• Other functions
P70 : INT0 input/HOLD release input/N-ch Tr. output for watchdog timer
P71 : INT1 input/HOLD release input
P72 : INT2 input/timer 0 event input
P73 : INT3 input with noise filter/timer 0 event input
$\overline{P74}$: Input terminal XT1 for 32.768kHz X'tal oscillation
P75 : Output terminal XT2 for 32.768kHz X'tal oscillation
• Interrupt detection style, vector address
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ Falling</th><th>H level</th><th>L level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td></td></tr>
</table>

Continue.

Name	I/O	Function description	Option
PORT8 P80 to 83 P84 to 87	 I I/O	• 4-bit input port • Data direction programmable for each bit individually • 4-bit input/output port • Other function AD converter input port (8 pins)	-
$\overline{RES}$	I	Reset	-
XT1/$\overline{P74}$	I	• Input terminal for 32.768kHz X'tal oscillation • Other function XT1 : Input port $\overline{P74}$ • When not in use, connect terminal to VDD	-
XT2/P75	O	• Output terminal for 32.768kHz X'tal oscillation • Other function XT2 : Input port P75 • When not in use - If set as port, connect terminal to VDD. - If set as oscillation, leave terminal open.	-
CF1	I	Input terminal for ceramic resonator	-
CF2	O	Output terminal for ceramic resonator	-

* All port options (except pull-up resistor of port 0) can be specified by bit.

A state of port terminals at reset

Name	Input/output mode	Style of pull-up resistors when pull-up option is enabled
Port 0	Input	Fixed pull-up resistor OFF
Ports 1,3	Input	Programmable pull-up resistor OFF

1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Supply voltage		VDDMAX	VDD	VDD		-0.3		+7.0	V
Input voltage		VI(1)	• Ports $\overline{74}$,75 • Ports 80,81,82,83 • $\overline{RES}$			-0.3		VDD+0.3	
Input/Output voltage		VIO(1)	• Port 1 • Ports 70,71,72,73 • Ports 84,85,86,87 • Ports 0, 3 of CMOS output			-0.3		VDD+0.3	
		VIO(2)	Ports 0, 3 of N-ch open drain output			-0.3		15	
High level output current	Peak output current	IOPH	• Ports 0, 1, 3 • Ports 71,72,73 • Ports 84,85,86,87	• CMOS output • For each pin		-10			mA
	Total output current	ΣIOAH(1)	Ports 0, 1	Total of all pins		-30			
		ΣIOAH(2)	Port 3	Total of all pins		-15			
		ΣIOAH(3)	• Ports 71,72,73 • Ports 84,85,86,87	Total of all pins		-10			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 3	For each pin				20	
		IOPL(2)	• Ports 70,71,72,73 • Ports 84,85,86,87	For each pin				15	
	Total output current	ΣIOAL(1)	Ports 0,1,70	Total of all pins				60	
		ΣIOAL(2)	Port 3	Total of all pins				40	
		ΣIOAL(3)	• Ports 71,72,73 • Ports 84,85,86,87	Total of all pins				20	
Maximum power consumption		Pdmax(1)	DIP42S	Ta= -30 to+70°C				630	mW
		Pdmax(2)	QFP48E	Ta= -30 to+70°C				350	
Operating temperature range		Topr				-30		70	°C
Storage temperature range		Tstg				-55		125	

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	typ.	max.	unit
Operating Supply voltage range	VDD(1)	VDD	0.98μs ≤ tCYC ≤ 400μs		4.5		6.0	V
	VDD(2)		3.9μs ≤ tCYC ≤ 400μs		2.5		6.0	
Hold voltage	VHD	VDD	RAM and register data are kept in HOLD mode.		2.0		6.0	
Input high voltage	VIH(1)	Port 0 of CMOS output	Output disable	2.5 to 6.0	0.33VDD +1.0		VDD	
	VIH(2)	Port 0 of N-ch open drain output	Output disable	4.0 to 6.0	0.75VDD		13.5	
				2.5 to 4.0	0.8VDD		13.5	
	VIH(3)	• Port 1 • Ports 72,73 • Port 3 of CMOS output	Output disable	2.5 to 6.0	0.75VDD		VDD	
	VIH(4)	Port 3 of N-ch open drain output	Output disable	4.0 to 6.0	0.75VDD		13.5	
				2.5 to 4.0	0.8VDD		13.5	
	VIH(5)	• Port 70 Port input/interrupt • Port 71 • $\overline{RES}$	Output disable	2.5 to 6.0	0.75VDD		VDD	
	VIH(6)	Port 70 Watchdog timer	Output disable	2.5 to 6.0	0.9VDD		VDD	
	VIH(7)	• Port 8 • Ports $\overline{74}$,75	• Output disable • Using as port	2.5 to 6.0	0.75VDD		VDD	
Input low voltage	VIL(1)	Port 0 of CMOS output	Output disable	2.5 to 6.0	VSS		0.2VDD	
	VIL(2)	Port 0 of N-ch open drain output	Output disable	2.5 to 6.0	VSS		0.25VDD	
	VIL(3)	• Ports 1,3 • Ports 72,73	Output disable	2.5 to 6.0	VSS		0.25VDD	
	VIL(4)	• Port 70 Port input/interrupt • Port 71 • $\overline{RES}$	Output disable	2.5 to 6.0	VSS		0.25VDD	
	VIL(5)	Port 70 Watchdog timer	Output disable	2.5 to 6.0	VSS		0.8VDD to 1.0	
	VIL(6)	• Port 8 • Ports $\overline{74}$,75	• Output disable • Using as port	2.5 to 6.0	VSS		0.25VDD	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	μs
				2.5 to 6.0	3.9		400	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	• 6MHz (ceramic resonator) • Refer to figure 1	4.5 to 6.0	5.88	6	6.12	MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator) • Refer to figure 1	2.5 to 6.0	2.94	3	3.06	
	FmRC		Internal RC oscillation	2.5 to 6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) • Refer to figure 2	2.5 to 6.0		32.768		kHz

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Oscillation stabilizing time (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator) • Refer to figure 3	4.5 to 6.0				ms
	tmsCF(2)	CF1, CF2	•3MHz (ceramic resonator) • Refer to figure 3	4.5 to 6.0				
				2.5 to 6.0				
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) • Refer to figure 3	4.5 to 6.0				s
				2.5 to 6.0				

(Note 1) The oscillation parameters are shown on table 1 and 2.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Input high current	IIH(1)	Ports 0,3 of open drain output	• Output disable • VIN=13.5V (including the off-leak current of the output Tr.)	2.5 to 6.0			5	μA
	IIH(2)	• Port 0 without pull-up MOS Tr. • Ports 1,3 • Ports 70,71,72,73 • Port 8	• Output disable • Pull-up MOS Tr. OFF. • VIN=VDD (including the off-leak current of the output Tr.)	2.5 to 6.0			1	
	IIH(3)	$\overline{RES}$	VIN=VDD	2.5 to 6.0			1	
	IIH(4)	Ports $\overline{74}$,75	• VIN=VDD • Using as port	2.5 to 6.0			1	
Input low current	IIL(1)	• Ports 1,3 • Port 0 without pull-up MOS Tr. • Ports 70,71,72,73 • Port 8	• Output disable • Pull-up MOS Tr. OFF. • VIN=VSS (including the off-leak current of the output Tr.)	2.5 to 6.0	-1			
	IIL(2)	$\overline{RES}$	VIN=VSS	2.5 to 6.0	-1			
	IIL(3)	Ports $\overline{74}$,75	• VIN=VSS • Using as port	2.5 to 6.0	-1			
Output high voltage	VOH(1)	• Ports 0,1,3 of CMOS output	IOH=-1.0mA	4.5 to 6.0	VDD-1			V
	VOH(2)	• Ports 71,72,73 • Ports 84,85,86,87	IOH=-0.1mA	2.5 to 6.0	VDD-0.5			
Output low voltage	VOL(1)	Ports 0,1,3	IOL=10mA	4.5 to 6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5 to 6.0			0.4	
	VOL(3)		• IOL=1.0mA • Every pin's IOL ≤ 1mA	2.5 to 6.0			0.4	
	VOL(4)	• Ports 71,72,73 • Ports 84,85,86,87	IOL=1.6mA	4.5 to 6.0			0.4	
	VOL(5)		• IOL=0.5mA • Every pin's IOL ≤ 1mA	2.5 to 6.0			0.4	
	VOL(6)	Port 70	IOL=1mA	4.5 to 6.0			0.4	
	VOL(7)		• IOL=0.5mA • Every pin's IOL ≤ 1mA	2.5 to 6.0			0.4	
Pull-up MOS Tr. resistor	Rpu	• Ports 0,1,3 • Ports 70,71,72,73 • Ports 84,85,86,87	VOH=0.9VDD	4.5 to 6.0	15	40	70	kΩ
				2.5 to 4.5	25	70	150	
Hysteresis voltage	VHIS	• Port 1 • Ports 70,71,72,73 • $\overline{RES}$	Output disable	2.5 to 6.0		0.1VDD		V
Pin capacitance	CP	All pins	• f=1MHz • All pins except the measured terminal: VIN=VSS • Ta=25°C	2.5 to 6.0		10		pF

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0,SCK1	Refer to figure 5	2.5 to 6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	SCK0,SCK1	• Use a 1kΩ pull-up resistor in the open drain output. • Refer to figure 5	2.5 to 6.0	2			
		Low Level pulse width	tCKL(2)					1/2tCKCY		
		High Level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set-up time		tICK	• SI0,SI1 • SB0,SB1	• Data set-up to SCK0,1 • Data hold from SCK0,1 • Refer to figure 5	4.5 to 6.0	0.1			µs
						2.5 to 6.0	0.4			
	Data hold time		tCKI			4.5 to 6.0	0.1			
						2.5 to 6.0	0.4			
Serial output	Output delay time (External clock used for serial transfer clock)		tCKO(1)	• SO0,SO1 • SB0,SB1	• Use a 1kΩ pull-up resistor in the open drain output. • Data hold from SCK0,1 • Refer to figure 5	4.5 to 6.0			7/12 tCYC +0.2	
						2.5 to 6.0			7/12 tCYC +1	
	Output delay time (Internal clock used for serial transfer clock)		tCKO(2)			4.5 to 6.0			1/3 tCYC +0.2	
						2.5 to 6.0			1/3 tCYC +1	

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	• INT0, INT1 • INT2/T0IN	• Interrupt acceptable • Timer0-countable	2.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is selected to 1/1.)	• Interrupt acceptable • Timer0-countable	2.5 to 6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is selected to 1/16.)	• Interrupt acceptable • Timer0-countable	2.5 to 6.0	32			
	tPIH(4) tPIL(4)	INT3/T0IN (The noise rejection clock is selected to 1/64.)	• Interrupt acceptable • Timer0-countable	2.5 to 6.0	128			
	tPIL(5)	$\overline{\text{RES}}$	Reset acceptable	2.5 to 6.0	200			μs

6. AD Converter Characteristics at Ta=-30°C to + 70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Resolution	N			4.5 to 6.0		8		bit
Absolute precision (Note 2)	ET						±1.5	LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)		15.68 (tCYC= 0.98μs)		65.28 (tCYC= 4.08μs)	μs
			AD conversion time = 32 × tCYC (if ADCR2=1) (Note 3)		31.36 (tCYC= 0.98μs)		130.56 (tCYC= 4.08μs)	
Analog input voltage range	VAIN	AN0 - AN7			VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD				1	μA
	IAINL		VAIN=VSS		-1			

(Note 2) Absolute precision excludes the quantizing error (±1/2 LSB).

(Note 3) The conversion time is the time from executing the AD conversion instruction to setting the complete digital conversion value in the register.

7. Sample Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Current drain during basic operation (Note 4)	IDDOP(1)	VDD	• FmCF=6MHz by ceramic resonator • FsXtal=32.768kHz by crystal oscillation • System clock : CF oscillation (6MHZ) • Internal RC oscillation stops • 1/1 divided	4.5 to 6.0		12	22	mA
	IDDOP(2)		• FmCF=3MHz by ceramic resonator • FsXtal=32.768kHz by crystal oscillation • System clock : CF oscillation (3MHz) • Internal RC oscillation stops • 1/2 divided	4.5 to 6.0		3	7	
	IDDOP(3)			2.5 to 4.5		2.0	5	
	IDDOP(4)		• FmCF=0Hz (when oscillation stops) • FsXtal=32.768kHz by crystal oscillation • System clock : RC oscillation • 1/2 divided	4.5 to 6.0		1.2	3	
	IDDOP(5)			2.5 to 4.5		1.0	2.5	
	IDDOP(6)		• FmCF=0Hz (when oscillation stops) • FsXtal=32.768kHz by crystal oscillation • System clock : X'tal oscillation (32.768kHz) • Internal RC oscillation stops • 1/2 divided	4.5 to 6.0		35	130	μA
	IDDOP(7)			2.5 to 4.5		25	70	

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings Max.	unit
Current drain in HALT mode (Note 4)	IDDHALT(1)	VDD	• HALT mode • FmCF=6MHz by ceramic resonator • FsXtal=32.768kHz by crystal oscillation • System clock : CF oscillation (6MHz) • Internal RC oscillation stops • 1/1 divided	4.5 to 6.0		7	12	mA
	IDDHALT(2)		• HALT mode • FmCF=3MHz by ceramic resonator • FsXtal=32.768kHz by crystal oscillation • System clock : CF oscillation (3MHz) • Internal RC oscillation stops • 1/2 divided	4.5 to 6.0		2.2	5	
	IDDHALT(3)			2.5 to 4.5		1.2	3	
	IDDHALT(4)		• HALT mode • FmCF=0Hz (when oscillation stops) • FsXtal=32.768kHz by crystal oscillation • System clock : RC oscillation •1/2 divided	4.5 to 6.0		800	2000	μA
	IDDHALT(5)			2.5 to 4.5		500	1500	
	IDDHALT(6)		• HALT mode • FmCF=0Hz (when oscillation stops) • FsXtal=32.768kHz by crystal oscillation • System clock : X'tal oscillation (32.768kHz) • Internal RC oscillation stops • 1/2 divided	4.5 to 6.0		25	100	
	IDDHALT(7)			2.5 to 4.5		12	55	
Current drain in HOLD mode (Note 4)	IDDHOLD(1)	VDD	HOLD mode	4.5 to 6.0		0.06	30	
	IDDHOLD(2)			2.5 to 4.5		0.02	20	

(Note 4) The current of the output transistors and pull-up MOS transistors are excluded.

Recommended Oscillation Circuit and Characteristics

The recommended circuit parameters are verified by an oscillator manufacturer using a SANYO provided oscillation evaluation board.

Table 1. Recommended circuit parameters for the main system clock using the ceramic resonator

Frequency	Manufacturer	Oscillator	Recommended circuit parameter			Operating supply voltage range	Note
			C1	C2	Rd1		
6MHz	MURATA	CSA6.00MG	33pF	33pF	470Ω	4.5V to 6.0V	
		CSTS0600MG03	(15pF)	(15pF)	470Ω	4.5V to 6.0V	Internal C1, C2
3MHz	MURATA	CSA3.00MG	33pF	33pF	470Ω	2.5V to 6.0V	
		CST3.00MGW	(30pF)	(30pF)	470Ω	2.5V to 6.0V	Internal C1, C2

Table 2. Recommended circuit parameters for the sub system clock using the crystal oscillation

Frequency	Manufacturer	Oscillator	Recommended circuit parameter			Operating supply voltage range	Note
			C3	C4	Rd2		
32.768kHz	SEIKO EPSON	MC-306	18pF	18pF	560Ω	2.5V to 6.0V	

The recommended circuit parameter may vary according to the applications. For further assistance, please contact the oscillator manufacturer keeping the following in mind.

- Since the oscillation frequency precision is affected by the wiring capacitance of the application board, etc., is it required to adjust the oscillation frequency on the production board.
- The oscillation frequency and the recommended circuit parameter shown above apply when the operating temperature range is -30°C to +70°C. When using the clock oscillation circuit under the conditions which exceed the operating temperature range or in applications that require precision tolerances, please contact the oscillator manufacturer.
- If using other circuit parameter than listed above, please contact SANYO.

Since the gain of oscillation circuit is reduced in order to minimize the power consumption of the circuit and the circuit can be affected by the noise, wiring capacity, etc., it is suggested to take the followings into consideration.

- The distance between the clock I/O terminals (XT1, XT2) and external parts should be as short as possible.
- The capacitors' (C1, C2) VSS should be placed close to the microcontroller's GND terminal and away from any other GND.
- The signal lines with large current or with rapid state changes should be placed away from the oscillation circuit.

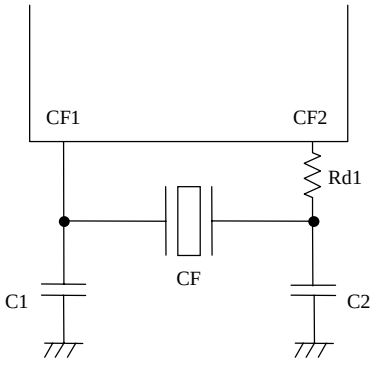


Figure 1 Ceramic oscillation circuit

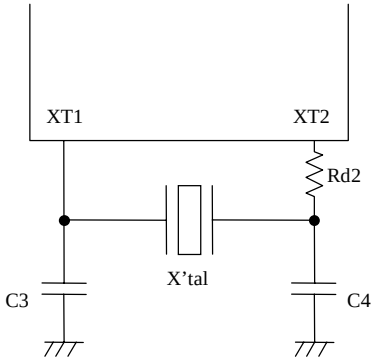


Figure 2 Crystal oscillation circuit

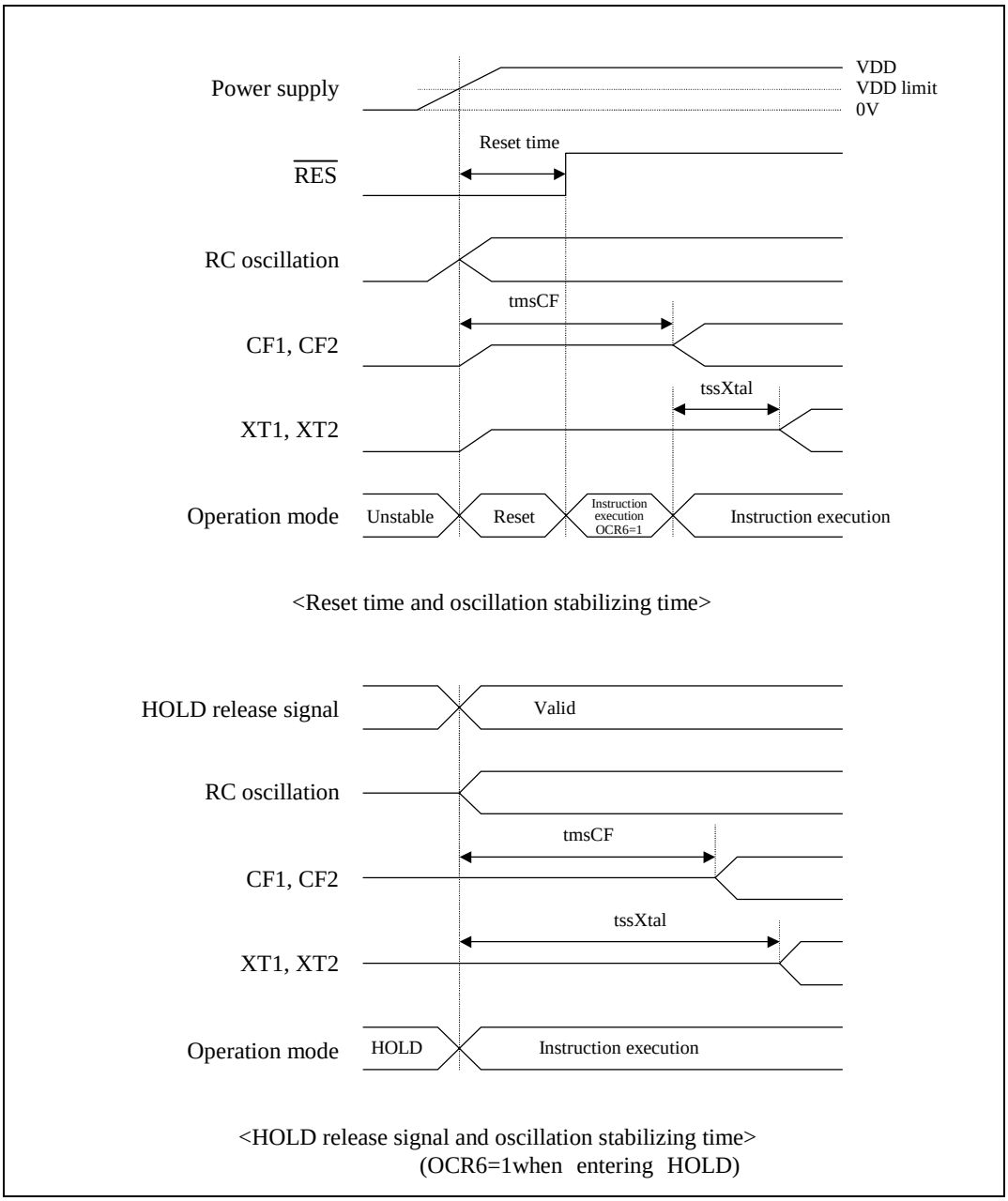
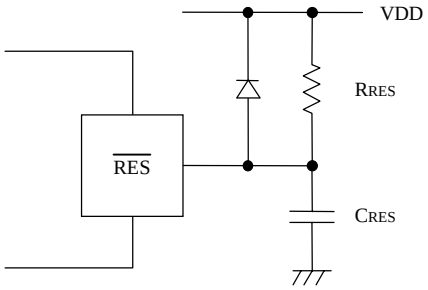


Figure 3 Oscillation stabilizing time



(Note) Select CRES and RRES value to assure that at least 200μs reset time is generated after the VDD becomes higher than the minimum operating voltage.

Figure 4 Reset circuit

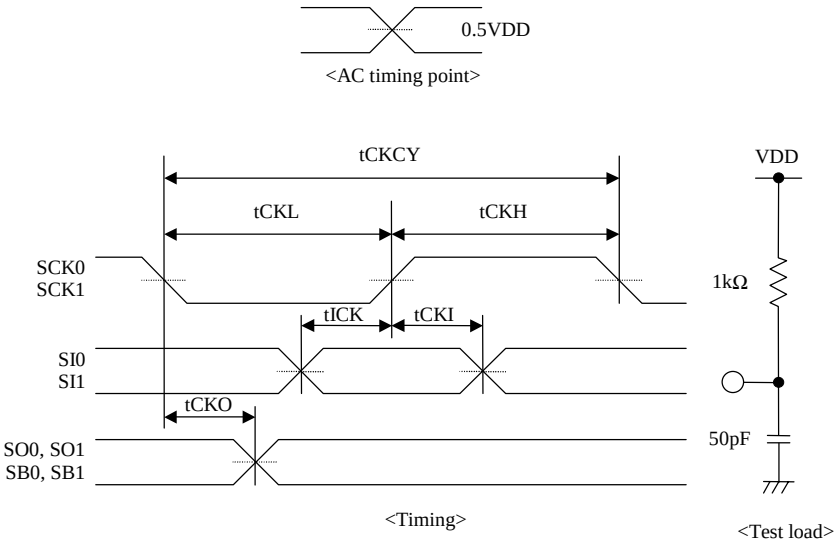


Figure 5 Serial input / output test condition

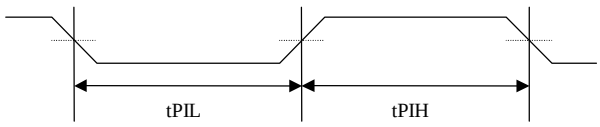


Figure 6 Pulse input timing condition

memo: