Low power 64-bit CPU

1GHz, power-efficient, MIPS-based CPU for affordable computing, thin clients and web appliances

STMicroelectronics' (ST) STLS is a family of processors addressing all the applications requiring high levels of performance and low power dissipation. The STLS processors are based on the Loongson™ core technology and they are the outcome of a successful collaboration begun in 2004 between ST and the Institute of Computing Technology (ICT), part of the Chinese Academy of Sciences.

The STLS processors deliver the best performance per dollar and watt in the industry today, along with the combined versatility of MIPS-64 architecture and Linux software. The STLS processors are the perfect choice for price and power sensitive computer systems, thin clients, web appliances and home media center devices.

Key features

- 64-bit four-issue, out-of-order superscalar architecture
- 9 stage pipeline organized in fetch, predecode, decode, reg map, dispatch, issue, reg-read, execution and commit
- Up to 1 GHz clock frequency
- Single/double precision floating point units
- New streaming multimedia instruction set support (SIMD)
- Integrated DDR memory controller
- 64 KB instruction cache, 64 KB data cache, on-chip 512 KB unified L2 cache
- Best in class for power management:
  - Voltage/frequency scaling
  - Standby mode support
  - L2 cache shutdown support
- Leading-edge 90 nm process technology
- MIPS-based instruction set
- Fanless

General advantages

- **Performance:** for demanding, multipurpose desktops and servers
- **Energy efficient:** for mobile and embedded applications
- **Low system cost:** for affordable computing products
- **Multimedia extensions:** for audiovisual-centric devices
- **High integration:** for single-chip server clients and embedded computers

www.st.com/STLS

Affordable personal computing and server client applications

Specifically designed to run on Linux operating systems, to extend battery life and to cut system costs, the STLS are the ideal processors for affordable laptop and desktop PC's and, in general, for all applications requiring a high level of performance with low power dissipation.
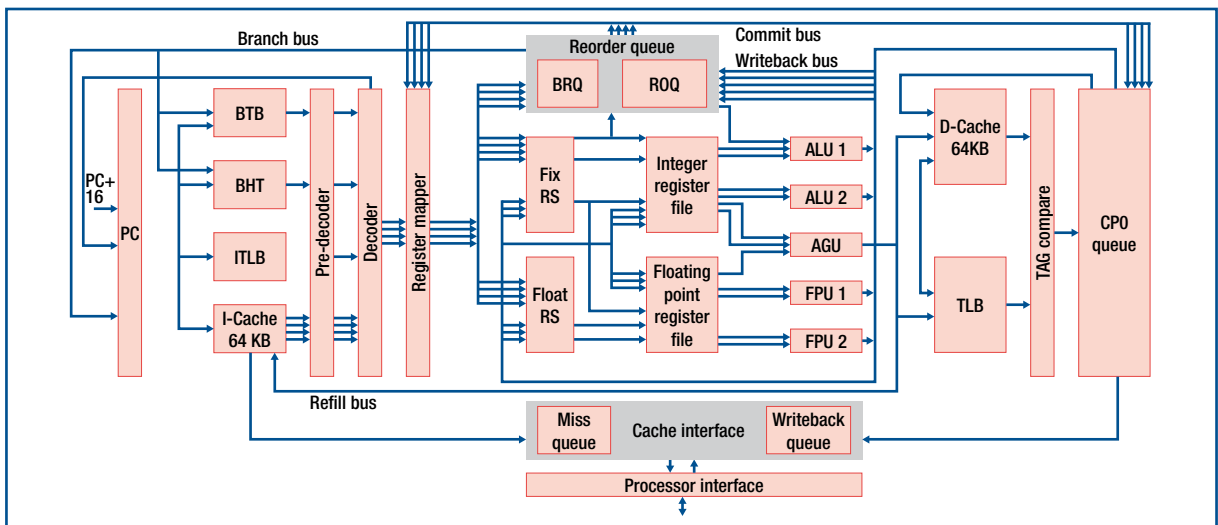
The STLS processors deliver the performance of other sophisticated processors, but they do so more efficiently and affordably. Freedom for product developers is ensured through the broad choice of open source software and the established MIPS technology ecosystem. The STLS is therefore a perfect choice for internet appliances or home media center devices.

STLS-based thin clients are formidable access devices for server-based applications in public administration offices, small and mid-size business offices, interactive kiosks, school computing labs and Internet cafes. STLS processors also excel in embedded applications where performance, reliability, security and energy efficiency are imperative.

Advanced architecture

The STLS is a MIPS-based, 64-bit superscalar microprocessor, able to issue four instructions per clock cycle among six functional units: two integer, two single-/double-precision floating point, one 64-bit SIMD and one load/store unit. The microarchitecture is organized with nine stages of pipeline and the support of dynamic branch prediction. The memory hierarchy is composed of the first level of 64 KB four-way set associative cache for instructions and data, the second level of 512 KB unified four-way set associative cache, and the memory management unit with table lookside buffer.

CPU block diagram

MIPS compatibility

Based on the MIPS instruction set, the STLS processors take advantage of the rich MIPS ecosystem, which includes software development tools, operating systems, middleware, EDA tools and application software.

	Part number	Clock frequency	L1 cache	L2 cache	DDR memory controller	TDP (no fan)	Package
Loongson2E	STLS2E02	700 MHz	128 KB	512 KB	Integrated DDR1-333	4 W @ 700 MHz	35 x 35 BGA
Loongson2F	STLS2F01	1 GHz	128 KB	512 KB	Integrated DDR2-667	4 W @ 1 GHz	27 x 27 BGA

Order code: FLOONGSON1007

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