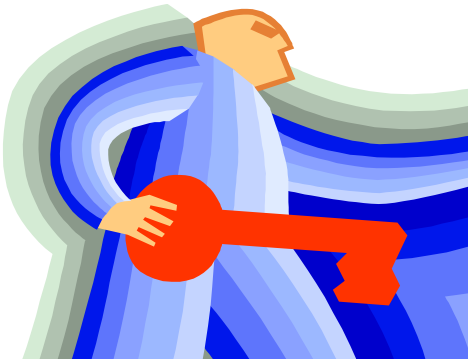
iDRAGON™ mP6 IA PROCESSOR



A Key Innovation for Information Appliances

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iDragon™ mP6 IA Processor

The Rise™ *iDragon™* mP6 IA processor is the first sixth generation x86-compatible processor optimized for low power consumption, high-performance information appliance applications such as set-top box, internet box, thin client, home gateway, iPVR and others. The innovative *iDragon™* mP6 IA processor is a superscalar and superpipelined IA procesor featuring 3 integer units, 3–way MMX technology and a fully pipelined floating point unit giving the users the utmost JAVA*, multimedia, video streaming and browsing experiences. The innovative circuitry of the *iDragon™* mP6 IA processor is optimized for low power consumption with the highest execution parallelism, which provides the excellent system thermal efficiency for enhanced system reliability.

- **x86 Instruction Set Enhanced with MMX™ Technology**
- **Superscaler & Superpipelined Integer and MMX Architecture**
  - Excellent JAVA*, Multimedia and Browsing Performance
  - Efficient MPEG4 video Streaming
- **Advanced On-chip and System Power Management for Excellent Thermal Efficiency and Reliability**
  - Facility Gating
  - Necessity Switching Only
  - Required Selection Only
  - SMM Compatible
  - Clock Control
  - ACPI Compliant
- **Advanced Architecture Features**
  - Advanced Data Dependency Removal Technique
  - Innovative Instruction Decode and Branch Prediction
  - Dynamic Allocation of Resources
- **Separate Code and Data Caches**
  - 8KB Code and 8KB Data
  - Split Line Access Mechanism
  - Filtered Tag Prefetching
- **High Performance FPU**
  - IEEE 854 Compliant
  - 80 Bit or 64 Bit Precision Results
- **IEEE 1149.1 Boundary Scan**
- **ISO 9001 Wafer Fabrication, Assembly and Test**
- **Support for Bus Frequencies of 60, 66, 75, 83, 95, and 100 MHz**
- **CPU/Host Bus Ratio 2X, 2.5X, 3X, 3.5X**
- **0.18um CMOS Technology with 3.3V I/O and 2.0V Core**
- **Low Profile 387-Terminal BGA Package**

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1 Processor Architecture Overview

The Rise™ *iDragon™* mP6 IA Processor provides a unique combination of exceptional performance and low power. Designed with the entire personal computing system in mind, the Rise™ *iDragon™* mP6 IA Processor is the ideal choice for power-efficient embedded consumer information appliance, thin server and thin client. The Rise™ *iDragon™* mP6 IA Processor provides software compatibility with Microsoft* Windows*, Windows CE*, MS-DOS*, QNX* and UNIX* along with the large installed base of x86 operating environments and applications. The Rise™ *iDragon™* mP6 IA Processor is also hardware compatible with existent X86 platforms, it offers IA designers the time-to-market advantage by minimizing the application software porting efforts since most of the internet applications were developed based on X86 platforms.

1.1 *iDragon™* mP6 IA Processor Architecture

The 3-way superscalar architecture of the Rise™ *iDragon™* mP6 IA Processor, utilizing three integer and MMX* superpipelines, enables instruction tripling. With instruction tripling, three instructions can be issued and completed in a single clock cycle, greatly increasing system throughput. Aggressive instruction pairing and tripling rules combined with advanced branch prediction algorithms ensure that three pipelines of the processor are utilized to their fullest. Figure 1 shows a block diagram of the Rise™ *iDragon™* mP6 IA Processor.

The Rise™ *iDragon™* mP6 IA Processor has an eight-stage superpipelined architecture. Each integer pipeline contains six stages. Supporting the integer pipelines is a three–stage, non–interlocking instruction fetch pipeline and a two–stage non–interlocking data cache pipeline which is de-coupled from the decoder. The third stage of the instruction fetch is a buffer that is bypassed when the buffer is empty, resulting in a total of eight stages for the combined pipeline. These supporting pipelines and the eight–stage integer pipelines provide superpipelined efficiency that greatly reduces pipeline stalls, and increases the aggregate instruction completion rate.

To effectively manage its pipeline architecture, the Rise™ *iDragon™* mP6 IA Processor uses innovative branch prediction and instruction decode techniques. A large 512 entry Branch Target Buffer (BTB), and an 8–entry call–return stack provide the base from which advanced branch prediction algorithms operate. By storing return addresses in its deep call–return stack, the Rise™ *iDragon™* mP6 IA Processor is able to accurately predict return targets, even from nested subroutines.

Dual Instruction Stream Execution (DISE) is a unique feature that allows instructions to be decoded from three streams and issued from two different instruction streams simultaneously. Up to eight unresolved branches may simultaneously be operated upon by instruction fetch and integer pipelines. Pairing and tripling rules combined with the ability to decode from multiple streams tremendously increases the total instruction throughput.

To reduce pipeline stalls and to improve data movement efficiency, the Rise™ *iDragon™* mP6 IA Processor resolves data dependency conflicts with the following features:

- Register Re–mapping
- Operand Forwarding
- Result Forwarding
- Zero Cycle Data Bypass
- Arithmetic Pairing

Each of these features reduces typical read after write, write after read, and write after write types of data dependencies. This allows the Rise™ *iDragon™* mP6 IA Processor to simultaneously execute pairs of instructions that other processors cannot.

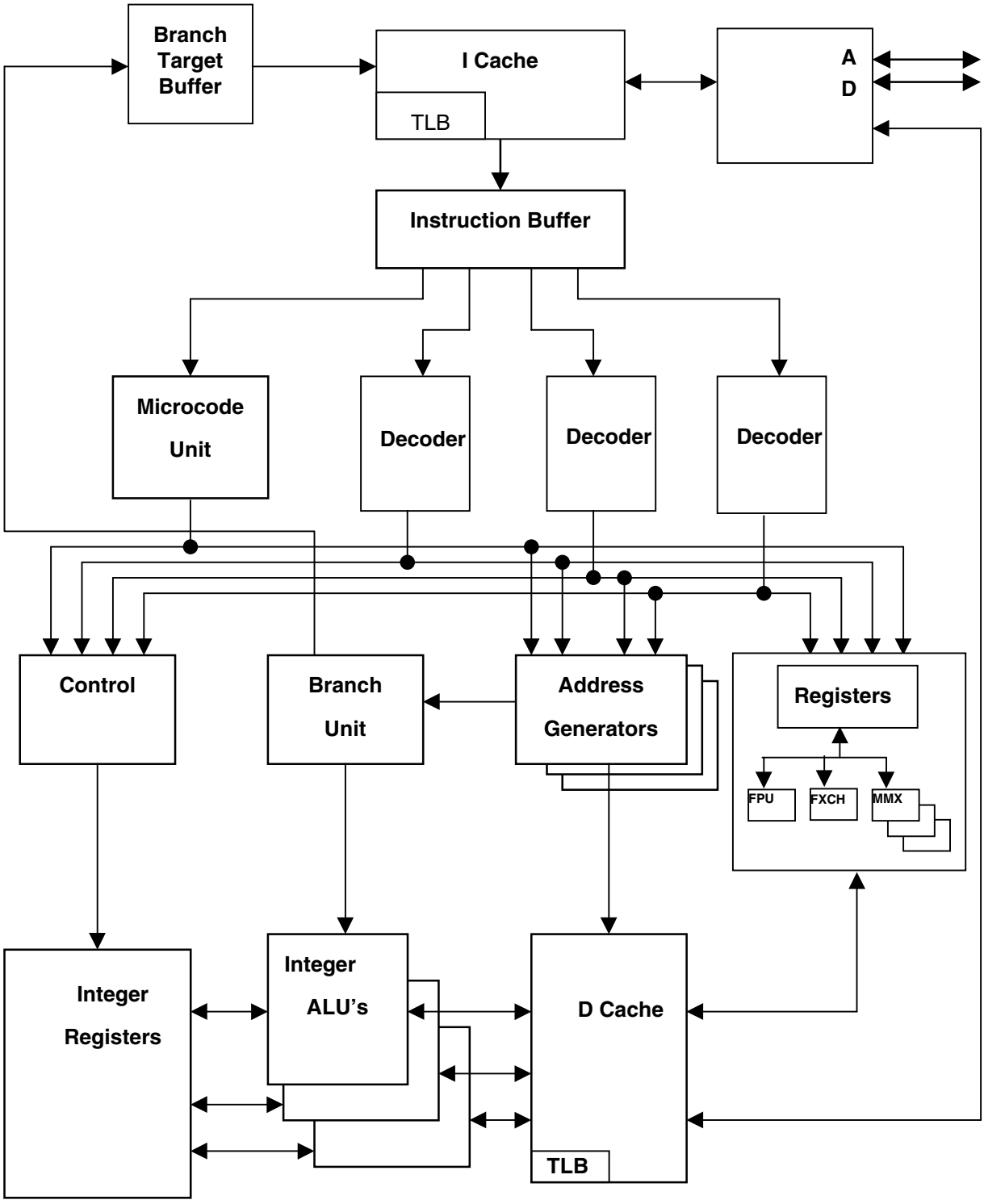


FIGURE 1. *iDragon™* mP6 IA PROCESSOR BLOCK DIAGRAM

The integrated Floating Point Unit (FPU) of the processor has been designed as a four stage parallel operation pipeline. This high performance FPU produces 80 bit results and conforms to IEEE Standards 854 and 754. The Rise™ *iDragon™* mP6 IA Processor can execute up to two floating point operations in the same cycle.

Three pipelines in the MMX* Unit can execute up to three instructions per cycle in parallel and can resolve data dependency (twinning) to increase performance. The MMX Unit is geared for high performance multimedia such as image processing, video conferencing, soft DVD, and soft modem. Figure 2 depicts the multimedia features.

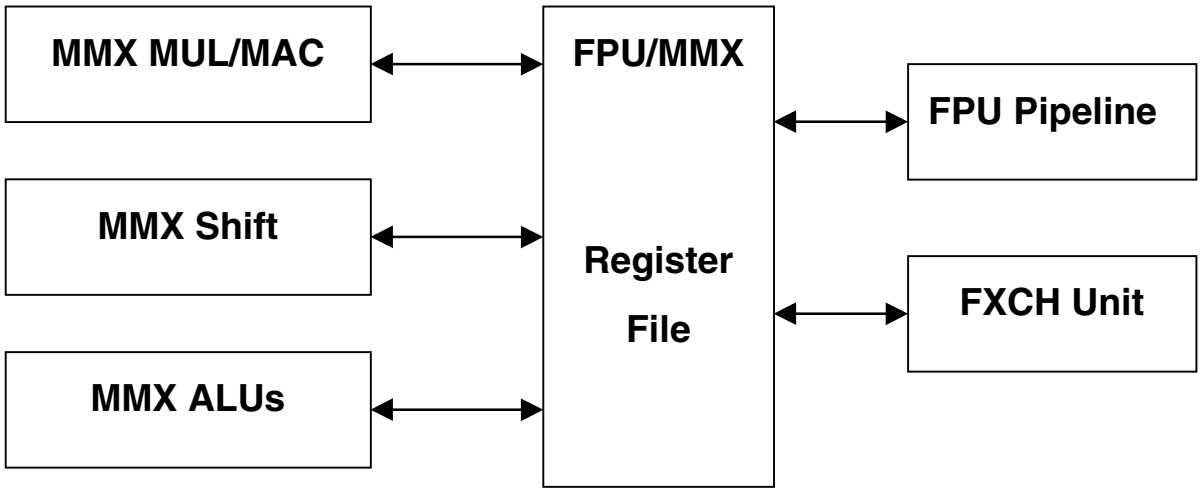


FIGURE 2. FPU/MMX UNIT

A 16 KByte L1 split cache design improves instruction and data handling, depending on the individual need. The instruction ("I") cache, uses a split–line access mechanism to ensure that up to 16 bytes of data can be accessed with each cycle, even if the data spans multiple lines.

The data ("D") cache utilizes eight interleaved banks to minimize conflicts between accesses. The "D" cache is dual ported (the tags are triple ported) to allow two read accesses, two write accesses, and a snoop access — all in the same cycle.

The "D" cache also contains a filtered tag prefetching mechanism to prefetch data while minimizing bus traffic and cache pollution. There is no misalignment penalty — an important factor for multimedia (e.g., MPEG playback).

The Integer Arithmetic Logic Units (ALUs) implement features that eliminate data dependency. The three major units in the ALU include the MUL/DIV/Shift Units, the 3–legged inputs, and the MOV/Jcc Units, which are illustrated in Figure 3.

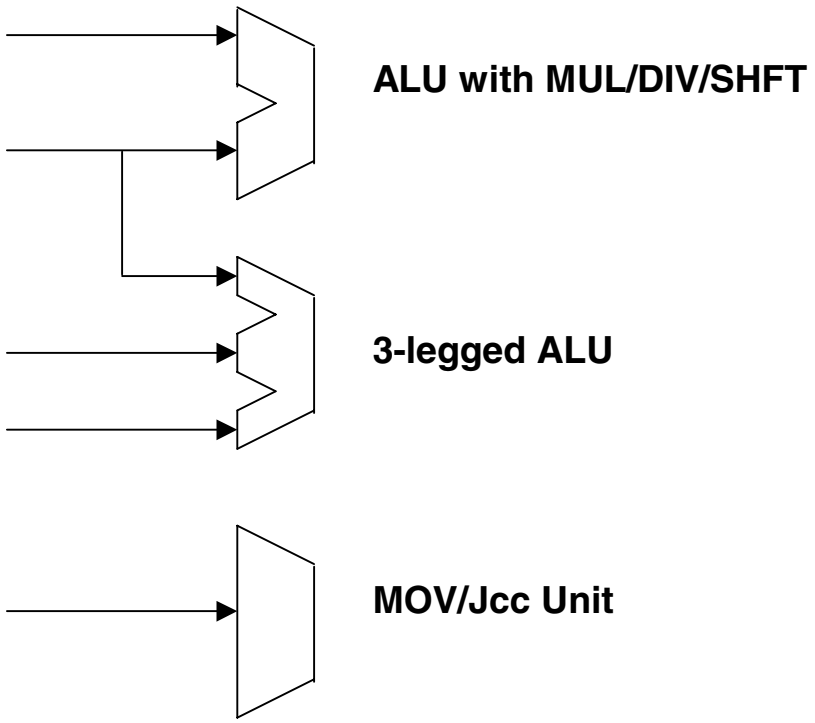
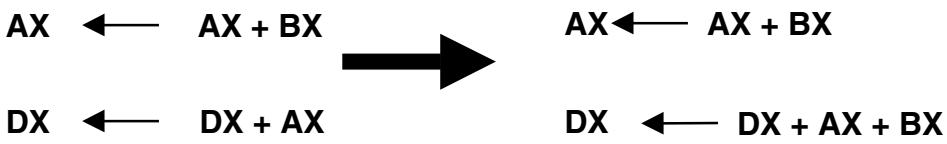


FIGURE 3. ARITHMETIC LOGIC UNITS

The following instruction stream can be accomplished in one cycle as the 3–legged ALU helps to collapse dependencies:



Dynamic Allocation of Resources (DAR) is a unique feature which provides an out–of–sequence–like execution technique utilized by the Rise™ *iDragon™* mP6 IA Processor to improve instruction throughput. DAR breaks the typical resource–to–pipeline affinity found in most superscalar designs by allowing address generators, execution units, etc. of the processor to be allocated to various pipelines. Through DAR, resource utilization increases and instruction throughput is maximized.

1.2 Power Management

The Rise™ *iDragon™* mP6 IA Processor is instruction and pin compatible with the Pentium processor implementation of the System Management Mode (SMM), Stop Grant State, Auto Halt Power Down State and Stop Clock State. The Rise™ *iDragon™* mP6 IA Processor is also compliant with the Advanced Configuration and Power Interface (ACPI) Specification.

In addition to system level power saving facilities, the Rise™ *iDragon™* mP6 IA Processor has the following internal architectural mechanisms that minimize power dissipation:

- Facility Gating — Facility Gating turns off the clocks to portions of the processor that are not needed for the current operation.
- Necessity Switching Only (NSO) — NSO reduces dynamic power dissipation by preventing unnecessary circuit switching.
- Required Selection Only (RSO) — RSO allows the processor to address and access only the minimum required amount of data from its various cache and ROM structures. RSO minimizes dynamic power dissipation by limiting the number of sense amplifiers driven per access.

No action is required by the system designer or the end user to realize the power saving benefits of these architectural features.

1.3 Testability

To assist in board level testing, the Rise™ *iDragon™* mP6 IA Processor implements IEEE Standard 1149.1 Boundary Scan (JTAG). Electrical specifications for the JTAG interface are defined in Table 29.

1.4 Compatibility

In general, the Rise™ *iDragon™* mP6 IA Processor is instruction and pin compatible with other advanced Socket 7– or Super Socket 7–based x86 processor such as the Pentium® processor with MMX* Technology. However, certain features of the Pentium processor that are not needed or used in embedded IA applications are not supported. Such features include multiprocessor and server capabilities as well as certain extended model–specific features as defined by the CPUID instruction.

1.4.1 Omitted Multiprocessing and Server Capabilities

The Rise™ *iDragon™* mP6 IA Processor is designed to specifically meet the needs of the power-efficient environments. The Rise™ *iDragon™* mP6 IA Processor does not provide the Pentium compatible server environment features of multiprocessing, APIC, and Master/Checker functional redundancy.

1.4.2 CPUID Instruction

The CPUID instruction is supported on the Rise™ *iDragon™* mP6 IA Processor, and return values for the CPUID instruction are shown in Tables 1 through 3. For comparison, the Intel P55C processor return values are included in the tables.

TABLE 1. CPUID RETURN VALUES WITH EAX == 0

REGISTER	*iDragon™mP6*	P55C
EAX	1	1
EBX:ECX:EDX	RiseRiseRise	GenuineIntel

TABLE 2. CPUID EAX RETURN VALUES WITH EAX == 1

PROCESSOR	[13:12] Type ID	[11:8] Family ID	[7:4] Model ID	[3:0] Stepping ID
iDragon™ mP6	0	5	2	Varies
P55C	0	5	4	Varies

TABLE 3. CPUID EDX RETURN VALUES WITH EAX == 1

EDX Bits – Meaning	*iDRAGON™ mP6*	P55C	Notes
0 – FP present	1	1	
1 – VM86 Extensions (VME)	0	1	
2 – Debugging Extensions	0	1	
3 – Page Size Extensions	0	0	
4 – Time Stand Counter (TSC) supported	1	1	
5 – Model Specific Registers present	0	1	
6 – PAE supported	0	0	
7 – Machine Check Exception	0	1	
8 – CMPXCHG8B instruction	0	1	1
9 – APIC supported	0	1	
10:11 – RESERVED	-	-	
12 – Memory Range Registers	0	0	
13 – PTE global Bit supported	0	0	
14 – Machine Check Architecture supported	0	0	
15 – Conditional Move supported	0	0	
16:22 – RESERVED	-	-	
23 – MMX supported	1	1	
24:31 – RESERVED	-	-	

Notes:

1. The CMPXCHG8B instruction is supported and always enabled on the *iDragon™* mP6 IA Processor; however, the default CPUID function bit is set to 0 to circumvent a reported bug in Windows NT*.

2 Pin References

The Rise™ *iDragon™* mP6 IA Processor is available in ball grid array package. (BGA) to provide excellent solutions for reduced footprint, lower profile Information Appliances. This BGA package has 387 balls arranged as an array matrix placement. The BGA ball references are depicted in the following figures and listed in the following tables.

2.1 BGA Package Ball Assignment

TOP VIEW SEE THROUGH

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A		VSS	VCCi	VCCi	D41	D39	D36	D33	D31	D28	D25	D23	D21	VCCc	D18	DP1	D13	D10	DP0	D5	D2	VCCc	VCCc	NC	VSS	VSS	A
B	VSS	VSS	VCCi	VCCi	D42	DP4	D37	D34	DP3	D29	D26	DP2	D22	VCCc	D17	D15	D12	D9	D7	D4	D1	VCCc	INC	NC	VSS	VSS	B
C	VCCi	VCCi	VSS	VCCi	VCCi	D40	D38	D35	D32	D30	D27	D24	D20	VCCc	D16	D14	D11	D8	D6	D3	D0	VCCc	NC	VSS	VCCc	VCCc	C
D	VCCi	VCCi	VCCi	VSS	VCCi	VCCi	VSS	VSS	VSS	VSS	VSS	VSS	D19	VCCc	VSS	VSS	VSS	VSS	VSS	VSS	VCCc	VCCc	VSS	VCCc	VCCc	VCCc	D
E	D43	VCCi	VCCi	VCCi																			VCCc	VCCc	VCCc	INC	E
F	D46	D45	D44	VCCi																			VCCc	VCCc	VCCc	INC	F
G	D48	DP5	D47	VSS																			VCCc	NC	INC	INC	G
H	D51	D50	D49	VSS																			VSS	NC	TCK	TD0	H
J	D54	D53	D52	VSS																			VSS	TDI	TMS	TRST#	J
K	D56	DP6	D55	VSS																			VSS	NC	STPCLK#	NC	K
L	D58	D59	D57	VSS							VSS	VSS	VSS	VSS	VSS	VSS							VSS	BF1	BF0	INC	L
M	D60	D62	D61	VSS							VSS	VSS	VSS	VSS	VSS	VSS							VSS	INIT	IGNNE#	SMI#	M
N	VCC3	VCC3	VCC3	VCC3							VSS	VSS	VSS	VSS	VSS	VSS							NMI	A21	INTR	NC	N
P	IERR#	FERR#	D63	DP7							VSS	VSS	VSS	VSS	VSS	VSS							VCCi	VCCi	VCCi	VCCi	P
R	NC	NC	NC	VSS							VSS	VSS	VSS	VSS	VSS	VSS							VSS	A22	A23	A24	R
T	NC	CACHE#	MIO#	VSS							VSS	VSS	VSS	VSS	VSS	VSS							VSS	A26	A25	A27	T
U	EWBE#	INV	KEN#	VSS																			VSS	A29	A28	A30	U
V	AHOLD	BRDY#	NA#	VSS																			VSS	A3	A31	A4	V
W	BOFF#	WBWT#	BRDYC#	VSS																			VSS	A6	A5	A7	W
Y	HOLD	INC	INC	VSS																			VCCi	A9	A8	A10	Y
AA	VCCc	INC	INC	VCCc																			VCCi	VCCi	INC	A11	AA
AB	VCCc	VCCc	VCCc	VCCc																			VCCi	VCCi	VCCi	VCCi	AB
AC	VCCc	VCCc	VCCc	VSS	VCCc	VCCc	VSS	VSS	VSS	VSS	VSS	VSS	VCCc	BE2#	VSS	PLL2	PLL3	VSS	VSS	VSS	VCCi	VCCi	VSS	VCCi	VCCi	VCCi	AC
AD	VCCc	VCCc	VSS	VCCc	VCCc	NC	BREQ	LOCK#	DC#	HITM#	INC	BE0#	VCCc	BE1#	BE7#	PLL2	PLL3	NC	A20	A18	A15	VCCi	VCCi	VSS	VCCi	VCCi	AD
AE	VSS	VSS	VCCc	VCCc	VCCc	SMIACT#	APCHK#	AP	PWT	ADS#	WR#	A20M#	VCCc	BE4#	BE6#	PLL2	PLL3	CLK	RESET	A17	A14	A12	VCCi	VCCi	VSS	VSS	AE
AF	VSS	VSS	VCCc	VCCc	VCCc	ADSC#	PCHK#	HLDA	PCD	EADS#	HIT#	FLUSH#	VCCc	BE3#	BE5#	PLL2	PLL3	SCYC	A19	A16	A13	VCCi	VCCi	VCCi	VSS	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

FIGURE 6. BGA PACKAGE TOP VIEW

2.2 BGA Ball References by Type

TABLE 4. BGA ADDRESS BALL REFERENCE

ADDRESS									
Addr	**Loc**	**Addr**	**Loc**	**Addr**	**Loc**	**Addr**	**Loc**	**Addr**	**Loc**
A3	V24	A9	Y24	A15	AD21	A21	N24	A27	T26
A4	V26	A10	Y26	A16	AF20	A22	R24	A28	U25
A5	W25	A11	AA26	A17	AE20	A23	R25	A29	U24
A6	W24	A12	AE22	A18	AD20	A24	R26	A30	U26
A7	W26	A13	AF21	A19	AF19	A25	T25	A31	V25
A8	Y25	A14	AE21	A20	AD19	A26	T24		

TABLE 5. BGA DATA BALL REFERENCE

DATA									
Data	**Loc**	**Data**	**Loc**	**Data**	**Loc**	**Data**	**Loc**	**Data**	**Loc**
D0	C21	D13	A17	D26	B11	D39	A6	D52	J3
D1	B21	D14	C16	D27	C11	D40	C6	D53	J2
D2	A21	D15	B16	D28	A10	D41	A5	D54	J1
D3	C20	D16	C15	D29	B10	D42	B5	D55	K3
D4	B20	D17	B15	D30	C10	D43	E1	D56	K1
D5	A20	D18	A15	D31	A9	D44	F3	D57	L3
D6	C19	D19	D13	D32	C9	D45	F2	D58	L1
D7	B19	D20	C13	D33	A8	D46	F1	D59	L2
D8	C18	D21	A13	D34	B8	D47	G3	D60	M1
D9	B18	D22	B13	D35	C8	D48	G1	D61	M3
D10	A18	D23	A12	D36	A7	D49	H3	D62	M2
D11	C17	D24	C12	D37	B7	D50	H2	D63	P3
D12	B17	D25	A11	D38	C7	D51	H1		

TABLE 6. BGA CONTROL BALL REFERENCE

CONTROL								
Signal	**Loc**	**Type**	**Signal**	**Loc**	**Type**	**Signal**	**Loc**	**Type**
A20M#	AE12	I	DP0	A19	I/O	INV	U2	I
ADS#	AE10	O	DP1	A16	I/O	KEN#	U3	I
ADSC#	AF6	O	DP2	B12	I/O	LOCK#	AD8	O
AHOLD	V1	I	DP3	B9	I/O	M/IO#	T3	O
AP	AE8	I/O	DP4	B6	I/O	NA#	V3	I
APCHK#	AE7	O	DP5	G2	I/O	NMI	N23	I
BE0#	AD12	O	DP6	K2	I/O	PCD	AF9	O
BE1#	AD14	O	DP7	P4	I/O	PCHK#	AF7	O
BE2#	AC14	O	EADS#	AF10	I	PWT	AE9	O
BE3#	AF14	O	EWBE#	U1	I	RESET	AE19	I
BE4#	AE14	O	FERR#	P2	O	SCYC	AF18	O
BE5#	AF15	O	FLUSH#	AF12	I	SMI#	M26	I
BE6#	AE15	O	HIT#	AF11	O	SMIACT#	AE6	O
BE7#	AD15	O	HITM#	AD10	O	TCK	H25	I
BOFF#	W1	I	HLDA	AF8	O	TDI	J24	I
BRDY#	V2	I	HOLD	Y1	I	TDO	H26	O
BRDYC#	W3	I	IERR#	P1	O	TMS	J25	I
BREQ	AD7	O	IGNNE#	M25	I	TRST#	J26	I
CACHE#	T2	O	INIT	M24	I	WR#	AE11	O
D/C#	AD9	O	INTR	N25	I	WB/WT#	W2	I

TABLE 7. BGA VCC_{IO} BALL REFERENCE

VCC_{IO}							
A3	A4	B3	B4	C1	C2	C4	C5
D1	D2	D3	D5	D6	E2	E3	E4
F4	N1	N2	N3	N4	P23	P24	P25
P26	Y23	AA23	AA24	AB23	AB24	AB25	AB26
AC21	AC22	AC24	AC25	AC26	AD22	AD23	AD25
AD26	AE23	AE24	AF22	AF23	AF24		

TABLE 8. BGA VCC_{CORE} BALL REFERENCE

VCCCORE							
A14	A22	A23	B14	B22	C14	C22	C25
C26	D14	D21	D22	D24	D25	D26	E23
E24	E25	F23	F24	F25	G23	AA1	AA4
AB1	AB2	AB3	AB4	AC1	AC2	AC3	AC5
AC6	AC13	AD1	AD2	AD4	AD5	AD13	AE3
AE4	AE5	AE13	AF3	AF4	AF5	AF13	

TABLE 9. BGA VSS BALL REFERENCE

VSS								
A2	A25	A26	B1	B2	B25	B26	C3	C24
D4	D7	D8	D9	D10	D11	D12	D15	D16
D17	D18	D19	D20	D23	G4	H4	H23	J4
J23	K4	K23	L4	L11	L12	L13	L14	L15
L16	L23	M4	M11	M12	M13	M14	M15	M16
M23	N11	N12	N13	N14	N15	N16	P11	P12
P13	P14	P15	P16	R4	R11	R12	R13	R14
R15	R16	R23	T4	T11	T12	T13	T14	T15
T16	T23	U4	U23	V4	V23	W4	W23	Y4
AC4	AC7	AC8	AC9	AC10	AC11	AC12	AC15	AC18
AC19	AC20	AC23	AD3	AD24	AE1	AE2	AE25	AE26
AF1	AF2	AF25	AF26					

TABLE 10. BGA PLL BALL REFERENCE

PLL3 - VCCIO			
AC17	AD17	AE17	AF17
PLL2 - VCCCORE			
AC16	AD16	AE16	AF16

TABLE 11. BGA RESERVED BALL REFERENCE

RESERVED (NC)					
T1	R2	R3	R1	C23	A24
B24	G24	H24	K24	K26	N26
AD18	AD6				

TABLE 12. BGA INC BALL REFERENCE

INC						
AD11	E26	G26	AA25	L26	G25	F26
AA3	AA2	Y2	Y3	B23		

TABLE 13. BGA CLOCK BALL REFERENCE

CLOCK							
Signal	**Loc**	**Signal**	**Loc**	**Signal**	**Loc**	**Signal**	**Loc**
BF0	L25	BF1	L24	CLK	AE18	STPCLK#	K25

2.3 Signal Description

The following table lists all signals supported by the. Rise™ *iDragon™* mP6 IA Processor. Since multiprocessor and server–related features are not supported by the Rise™ *iDragon™* mP6 IA Processor, signals are not listed for them.

TABLE 23. RISE™ *iDragon™* mP6 IA PROCESSOR SIGNAL DESCRIPTION

SIGNAL	I/O TYPE	DESCRIPTION
A20M#	I	The **address bit 20 mask** causes the Rise™ *iDragon™* mP6 IA Processor to emulate the address wraparound at 1 Mbyte which occurs on the 8086 by masking physical address bit 20 (A20) before performing an internal cache access or driving a memory cycle. A20M# is asserted when the Rise™ *iDragon™* mP6 IA Processor is in real mode and is undefined when it is in protected mode.
A31-A3	I/O	**Address** lines and **byte enables (BE#7–BE#0)** define memory or I/O access. The external system drives A31–A5 for cache inquiry cycles.
ADS#	O	The **address strobe** indicates that a new valid memory or I/O bus cycle is currently being driven by the Rise™ *iDragon™* mP6 IA Processor.
ADSC#	O	The **address strobe copy** is functionally identical to ADS#.

SIGNAL	I/O TYPE	DESCRIPTION
AHOLD	I	The **address hold** input allows another bus master access to the address of the Rise™ *iDragon™* mP6 IA Processor. The Rise™ *iDragon™* mP6 IA Processor stops driving the address lines (A31–A3) and AP in the next clock, while the rest of the bus remains active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven with even parity information on Rise™ *iDragon™* mP6 IA Processor –generated cycles in the same clock that the address is driven. During cache inquire cycles, this pin is sampled in the same clock as EADS# to ensure that correct parity check status is indicated by **APACHK#** of the Rise™ *iDragon™* mP6 IA Processor.
APCHK#	O	If the Rise™ *iDragon™* mP6 IA Processor detects a parity error on the address bus during inquire cycles, the **address parity check** status pin is asserted two clocks after EADS# is sampled active and it remains active for one clock cycle.
BE7#-BE0#	O	**Byte enables** determine which data bytes are transferred for the current cycle. Byte enables and address lines A31–A3 are driven in the same clock.
BF[1:0]	I	The **bus frequency** inputs are sampled at **RESET** to determine the CPU-to-bus frequency ratio. See Table 24 for Host Bus Frequency Selections.
BOFF#	I	The **backoff** input forces the Rise™ *iDragon™* mP6 IA Processor to abort all outstanding bus. The Rise™ *iDragon™*mP6 IA Processor floats all pins to enter the bus hold state in the next clock. When BOFF# is negated, the Rise™ *iDragon™* mP6 IA Processor restarts the aborted bus cycles.
BRDY#	I	**Burst ready** input indicates that the external system has presented valid data on the data pins in response to a read, or that the external system has accepted Rise™ *iDragon™* mP6 IA Processor data in response to a write request. The processor samples BRDY# in the second and subsequent clocks of a bus cycle.
BRDYC#	I	The **burst ready (copy)** is functionally identical to BRDY#.
BREQ	O	The **bus request** output indicates to the external system that the Rise™ *iDragon™* mP6 IA Processor has a bus cycle pending internally.
CACHE#	O	The **cache** pin indicates internal “cache–ability” of a read cycle or a burst write–back cycle. If this pin is driven inactive during a read cycle, the Rise™ *iDragon™* mP6 IA Processor does not cache the returned data, regardless of the state of the KEN# pin. The **cache** pin is also used to determine the cycle length.
CLK	I	**Clock** input provides the fundamental timing for the Rise™ *iDragon™* mP6 IA Processor. External timing parameters are specified with reference to the rising edge of CLK.

SIGNAL	I/O TYPE	DESCRIPTION
D63-D0	I/O	**Data lines** are three–state, bi-directional signals. Lines D7–D0 define the least significant byte of the data bus, and lines D63–D56 define the most significant. The data bus is driven only while a write cycle is active. During reads, the CPU samples the data bus when BRDY# is returned.
D/C#	O	The **data/code** is driven valid in the same clock that the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
DP7-DP0	I/O	The **data parity** signals provide parity for the data bus — one for each byte of the data bus. These signals are driven by the Rise™ *iDragon™* mP6 IA Processor with even parity information on writes in the same clock as the data. Even parity information must be driven back to the Rise™ *iDragon™* mP6 IA Processor on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Rise™ *iDragon™* mP6 IA Processor. DP7 applies to D63-D56.
EADS#	I	The **external address strobe** indicates a valid cache inquiry address is being driven onto the Rise™ *iDragon™* mP6 IA Processor address bus in an inquire cycle.
EWBE#	I	The **external write buffer empty** indicates that there are no pending write cycles in the external system.
FEER#	O	The **floating-point error** pin is driven active when an unmasked floating point error occurs during the execution of the FPU instruction.
FLUSH#	I	The **flush** input forces the Rise™ *iDragon™* mP6 IA Processor to flush the cache by writing back all modified lines in the data cache and invalidating its internal caches.
HIT#	O	**Hit** indicates that a current cache inquiry address has been found on a valid line in either the data or instruction cache. This pin is valid two clocks after EADS# is sampled as asserted, and remains valid until the next cache inquiry cycle.
HITM#	O	The **hit modified line** indicates that a current cache inquiry address has been found in the cache and dirty data exists in the cache line. It inhibits another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** indicates that a hold request being driven to the Rise™ *iDragon™* mP6 IA Processor on the **HOLD** pin. When leaving bus hold, the Rise™ *iDragon™* mP6 IA Processor resumes driving the bus and HLDA is driven inactive. If a bus cycle pending, the Rise™ *iDragon™* mP6 IA Processor is driven one clock cycle after HLDA is de-asserted.
HOLD	I	The **bus hold request** indicates that another bus master has requested the control of the Rise™ *iDragon™* mP6 IA Processor host bus. After completing all outstanding bus cycles, the Rise™ *iDragon™* mP6 IA Processor enters a bus hold state until HOLD is de-asserted. The Rise™ *iDragon™* mP6 IA Processor recognizes HOLD during RESET but not in LOCK cycles.

SIGNAL	I/O TYPE	DESCRIPTION
IERR#	O	The **internal error** pin indicates internal parity errors.
IGNNE#	I	The **ignore numeric error** forces the Rise™ *iDragon™* mP6 IA Processor to ignore any pending unmasked numeric exception and to continue executing floating-point instructions as long as this pin is asserted.
INIT	I	The **initialization** input forces the Rise™ *iDragon™* mP6 IA Processor to begin execution in a known state which is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain their values. If INIT is sampled high when RESET transitions from high to low, the processor performs the build–in self test prior to initiating program execution.
INTR	I	The **maskable interrupt** input indicates that an external interrupt has been generated. When the IF bit of the EFLAGS register is set, the Rise™ *iDragon™* mP6 IA Processor generates two locked interrupt acknowledge bus cycles and begins execution of an interrupt service routine after executing the current instruction.
INV	I	The **invalidation** input ascertains the final cache line state to be invalid or shared in a cache inquiry hit. It is sampled in the same clock with the cache inquiry address and the **EADS#.**
KEN#	I	The **cache enable** input allows the data being returned from the current cycle to be cacheable. When the Rise™ *iDragon™* mP6 IA Processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle is transformed into a 32–byte cache line fill cycle.
LOCK#	O	The **lock** pin indicates that the current bus cycle is locked. The Rise™ *iDragon™* mP6 IA Processor does not accept a bus hold request from another bus master while LOCK# is asserted
M/IO#	O	The **memory/input–output** is driven valid in the same clock as the **ADS#**. M/IO# distinguishes between memory and I/O cycles.
NA#	I	The **next address** input indicates that the external memory system is ready to accept a new bus cycle, even though all data transfers for the current cycle are not yet complete. The Rise™ *iDragon™* mP6 IA Processor issues ADS# for a pending cycle two clocks after NA# is asserted.
NMI	I	The **non–maskable interrupt** request signal indicates that an external non–maskable interrupt has been generated. The Rise™ *iDragon™* mP6 IA Processor suspends execution of the current instruction stream and begins execution of a NMI interrupt service routine.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The PCD provides an external cache–ability indication on a page–by–page basis.

SIGNAL	I/O TYPE	DESCRIPTION
PCHK#	O	The **parity check** output indicates a data bus parity error in a data read cycle. It is driven with parity status two clocks after BRDY# is returned. Parity is checked only for the bytes on which valid data are returned.
PWT	O	The **page write through** pin reflects the state of the PWT bit in CR3, the page Directory Entry, or the Page Table Entry. The PWT pin is used to provide an external write back indication on a page–by–page basis. **PWT** has higher priority than **WB/WT#.**
RESET	I	**RESET** forces the Rise™ *iDragon™* mP6 IA Processor to begin execution at a known state. All data in the internal caches is invalidated.
SCYC	O	The **split cycle** is asserted during misaligned LOCKed transfers to indicate that more than two cycles are locked together. This signal is defined for locked cycles only.
SMI#	I	The **system management interrupt** causes the Rise™ *iDragon™* mP6 IA Processor to System Management Mode. **SMI** has higher priority than **NMI.**
SMIACT#	O	The **system management interrupt active** indicates that the Rise™ *iDragon™* mP6 IA Processor is in System Management Mode.
STPCLK#	I	The **stop clock** input is a request from the system to stop the internal clock of the Rise™ *iDragon™* mP6 IA Processor. When the Rise™ *iDragon™* mP6 IA Processor recognizes STPCLK#, it stops execution on the next instruction boundary and generates a stop grant acknowledge cycle. When STPCLK# is asserted, the Rise™ *iDragon™* mP6 IA Processor still responds to external snoop requests.
TCK	I	The **testability clock (JTAG)** provides the clocking function for the Rise™ *iDragon™* mP6 IA Processor boundary scan in accordance with the IEEE1149.1 Boundary Scan interface. It is used to clock state information and data into and out of the Rise™ *iDragon™* mP6 IA Processor during boundary scan.
TDI	I	The **test data input (JTAG)** is a serial data input for the test logic. Data and instructions are shifted into the Rise™ *iDragon™* mP6 IA Processor on this pin on the rising edge of TCK for testing.
TDO	O	The **test data output (JTAG)** is a serial data output of the test logic. Data and instructions are shifted out of the Rise™ *iDragon™* mP6 IA Processor on this pin on the falling edge of TCK for testing.
TMS	I	The **test mode select (JTAG)** signal sampled on the rising edge of TCK controls the sequence of state changes of the boundary scan test logic.
TRST#	I	**Test reset (JTAG)** input asynchronously initializes boundary scan test logic.
VCC2DET#	O	**VCC2 detect** is always driven low by the Rise™ *iDragon™* mP6 IA Processor. It is not available in regular package, only available in OEM BPGA package.

SIGNAL	I/O TYPE	DESCRIPTION
W/R#	O	**Write/read** is driven valid in the same clock period that the ADS# signal is asserted. It distinguishes between write and read cycles for the current memory or I/O bus access.
WB/WT#	I	The **write back/write through** input defines the cache write policy to a data cache line as either write back or write through on a line-by-line basis.

2.4 Pin Connections

For reliable operation, any unused active high input must be tied to GND (VSS) and any unused active low input must be tied to VCC_{IO}; however, if an unused input has an internal pull–up or pull–down resistor, then no external connection is required. Signals with internal pull–up or pull–down resistors are listed below (all internal pull–up and pull–down resistors are 33 KΩ ± 50%). If an external connection is made to an input with an internal resistor, it must be a direct connection (< 1 kΩ resistance). Unused inputs that do not have internal resistors should be connected to GND or VCC_{IO} using a 20 kΩ resistor.

Signals with internal pull–down resistors include: BF0, CLK

Signals with internal pull–up resistors include: BF1, BRDY#, BRDYC#, SMI#, STPCLK#, TCK#, TDI#, TMS#, TRST#

2.4.1 RESERVED Pins

Pins labeled RESERVED must not be connected; if they are connected, they can cause the processor to produce unexpected results or to otherwise malfunction.

2.4.2 INC Pins

Pins labeled INC have no connection to the processor die and it is recommended (though not required) that these pins be left unconnected.

2.4.3 Processor and Host Bus Frequency Control

The Rise™ *iDragon™* mP6 IA Processor operates at a multiple of the host bus frequency. Table 24 lists the relationship between BF1–BF0 values and the consequent CPU–to–host bus ratios. Both BF0 and BF1 are active high signals so the corresponding pins should be tied to VCC_{IO} or VSS to obtain the desired CPU–to–host bus ratio. The processor uses internal pull–up/pull–down resistors to force a default CPU–to–host bus ratio of 2:1.

Table 24. CPU and Host Bus Frequency Control

			EXAMPLES	
BFI	BFO	CPU:HOST BUS RATIO	PERFORMANCE RATING	HOST BUS FREQUENCY
1	0	2:1	500 MIPS	100 MHz
0	0	2.5:1	600 MIPS	100 MHz

3 Electrical Specifications

3.1 Maximum Ratings

The values in Table 25 are worst-case stress ratings. CPU operation and reliability can be impaired and failure can occur if maximum ratings are exceeded. The CPU is not warranted, expressed or implied, to perform beyond these parameters. For best results, adhere to the operating conditions defined in the DC and AC specification tables listed below. The Rise™ *iDragon™* mP6 IA Processor resists latch-up or circuit damage caused by electrostatic discharge (ESD). However, it is not possible to prevent all failures that can result from excessive ESD, and precautions to avoid E/M fields and static shocks should always be taken when handling, storing, or operating the Rise™ *iDragon™* mP6 IA Processor.

TABLE 25. MIN/MAX RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS
T_s	Storage temperature	-65	150	°C
T_{CASE}	Case temperature under bias or voltage applied	-65	110	°C
VCC_{IO}	3.3 V supply voltage relative to VSS	-0.5	3.9	V
VCC_{CORE}	2.0 V supply voltage relative to VSS	-0.5	2.1[1]	V
VIN_{IO}[1]	DC input voltage at any pin	-0.5	VCC_{IO} + 0.5	V

Notes:

1. To avoid CPU damage, do not exceed the MAX voltage under any circumstances.

3.2 DC Specifications

TABLE 26. DC SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
T_{CASE}	Operating case temperature	0		70	°C	1
VCC_{CORE}	Core voltage	1.95	2.0	2.05	V	
VCC_{IO}	I/O voltage	3.135	3.3	3.465	V	3.3V ± 5% [2]
ICC_{CORE}	Power supply current			2	A	600 MIPS [3]
ICC_{IO}	Power supply current			1	A	500 MIPS [3]
V_{IL_IO}	Input low voltage	-0.3		0.8	V	4
V_{IH_IO}	Input high voltage	2.0		VCC_{IO} + 0.3	V	4
V_{OL_IO}	Output low voltage			0.4	V	4,5
V_{OH_IO}	Output high voltage	2.4	–	–	V	4, 6
I_{LI}	Input leakage current	–	–	± 15	µA	$0 \le V_{IN} \le VCC_{IO}$ [7]
I_{LO}	Output leakage current	–	–	± 15	µA	$0 \le V_{IN} \le VCC_{IO}$ [8]
I_{IH}	Input Leakage Current	–	–	200	µA	V_{IN}=2.4 V [9]
I_{IL}	Input leakage current	–	–	- 400	µA	10
C_{IN}	Input Capacitance	–	–	15	pF	11
C_{OUT}	Output Capacitance	–	–	20	pF	11
$C_{I/Output}$	I/Output Capacitance	–	–	25	pF	11
C_{CLK}	CLK Input Capacitance	–	–	15	pF	11
C_{TIN}	Test Input Capacitance	–	–	15	pF	11
C_{TOUT}	Test Output Capacitance	–	–	20	pF	11
C_{TCK}	Test Clock Capacitance	–	–	15	pF	9

Notes:

1. Assuming case was setup in average room temp.
2. Unit not guaranteed to work beyond the MAX operating voltage in the MAX temperature.
3. These values should be used for power supply design.
4. All signals are 3.3 V TTL levels.
5. Measured with a 4 mA load.
6. Measured with a –3 mA load.
7. For signals without an internal pull up or pull down resistor.
8. For signals with an internal pull up or pull down resistor.
9. For inputs with an internal pull down resistor.
10. For inputs with an internal pull up resistor.
11. Not 100% tested, guaranteed by design.

TABLE 27. POWER DISSIPATION SPECIFICATIONS

PARAMETER	TYP[1]	MAX	UNITS	PERFORMANCE RATING
Active power dissipation	1.34 1.07	4.05 3.24	W W	600 MIPS 500 MIPS
Stop Grant and Auto Halt Power Down power dissipation	–	–	W W	600 MIPS 500 MIPS
Stop Clock power dissipation	–	–	W	All

Notes

1. Typical system power dissipation running a typical sequence of instructions with 20% of active time. Power dissipation varies across applications. System thermal solutions should be designed to dissipate the maximum power dissipation.

3.3 AC Specifications

The AC specifications are listed in two tables (28A and 28B). Table 28A lists the AC specifications of processors for host buses that run at 60MHz, 66MHz, and 75MHz, while Table 28B lists the AC specifications of processors for host buses that run at 83MHz, 95MHz, and 100MHz. The two tables are divided into several parts, each of which is followed by a related timing diagram in the following pages.

TABLE 28A. AC SPECIFICATIONS

See Table 26 for recommended operating range, C_L = 50 pF

SYMBOL	PARAMETER	60 MHz		66 MHz		75 MHz		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
f	CLK Frequency	30.0	60.0	33.3	66.7	37.5	75	MHz	
t_1	CLK Period	16.7	33.3	15.0	30.0	13.33	26.7	nS	
t_2	CLK Period Stability	–	±250	–	±250	–	±250	pS	
t_3	CLK High Time	4.0	–	4.0	–	4.0	–	nS	
t_4	CLK Low Time	4.0	–	4.0	–	4.0	–	nS	
t_5	CLK Fall Time	0.15	1.5	0.15	1.5	0.15	1.5	nS	
t_6	CLK Rise Time	0.15	1.5	0.15	1.5	0.15	1.5	nS	

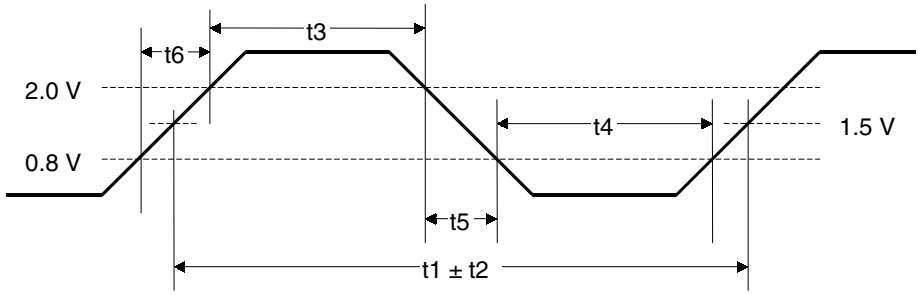


FIGURE 7A. CLOCK INPUT WAVEFORM

TABLE 28B. AC SPECIFICATIONS

See Table 26 for recommended operating range, C_L = 0 pF

Symbol	Parameter	83 MHZ		95 MHZ		100 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
f	CLK Frequency	41.5	83	47.5	95	50	100	MHz	
t_1	CLK Period	12.1	24.1	10.5	21.1	10	20	ns	
t_2	CLK Period Stability	–	±250	–	±250	–	±250	ps	
t_3	CLK High Time	3.0	–	3.0	–	3.0	–	ns	
t_4	CLK Low Time	3.0	–	3.0	–	3.0	–	ns	
t_5	CLK Fall Time	0.15	1.5	0.15	1.5	0.15	1.5	ns	
t_6	CLK Rise Time	0.15	1.5	0.15	1.5	0.15	1.5	ns	

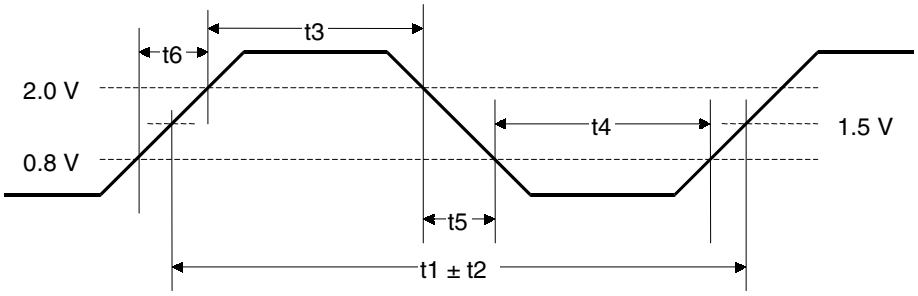


FIGURE 7B. CLOCK INPUT WAVEFORM

TABLE 28A. AC SPECIFICATIONS (CONTINUED)

See Table 26 for recommended operating range, C_L = 50 pF

Symbol	Parameter	60 MHZ		66 MHZ		75 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
t_{10}	A31-3, ADSC#, BE7-BE0#, CACHE#, D/C#, LOCK3, PCD, PWT, SCYC, W/R# Valid Delay	1.0	7.0	1.0	7.0	1.0	6.0	nS	
t_{10}	AP Valid Delay	1.0	8.5	1.0	8.5	1.0	7.5	nS	
t_{10}	ADS#, M/IO# Valid Delay	1.0	7.0	1.0	6.0	1.0	6.0		
t_{10}	APCHK#, FERR#, IERR# Valid Delay	1.0	8.0	1.0	8.0	1.0	7.0	nS	
t_{10}	PCHK# Valid Delay	1.0	7.0	1.0	7.0	1.0	6.0	nS	
t_{10}	BREQ, HLDA, SMIACT# Valid Delay	1.0	8.0	1.0	8.0	1.0	6.0	nS	
t_{10}	HIT# Valid Delay	1.0	8.0	1.0	8.0	1.0	6.0	nS	
t_{10}	HITM# Valid Delay	1.0	6.0	1.0	6.0	1.0	6.0	nS	
t_{10}	D63-D0, DP7-DP0 Write Data Valid Delay	1.0	8.0	1.0	8.0	1.0	7.0	nS	

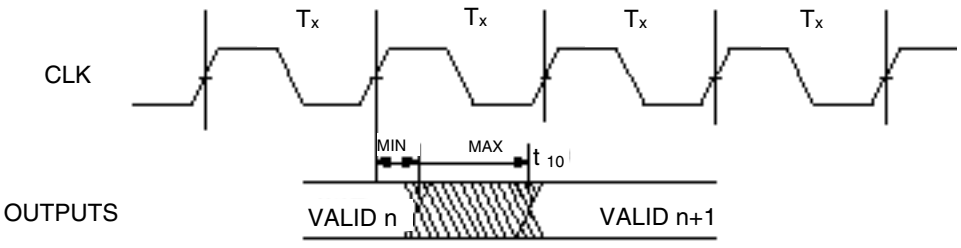


FIGURE 8A. OUTPUT VALID DELAY WAVEFORM

TABLE 28B. AC SPECIFICATIONS (CONTINUED)

See Table 26 for recommended operating range, C_L = 0 pF

Symbol	Parameter	83 MHZ		95 MHZ		100 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
t_{10}	A31-A3 Valid Delay	1.1	4.0	1.1	4.0	1.1	4.0	ns	
t_{10}	AP Valid Delay	1.0	5.5	1.0	5.5	1.0	5.5	ns	
t_{10}	ADS#, ADSC#, D/C#, M/IO#, W/R# Valid Delay	1.0	4.0	1.0	4.0	1.0	4.0	ns	
t_{10}	APCHK#, FERR#, IERR# Valid Delay	1.0	4.5	1.0	4.5	1.0	4.5	ns	
t_{10}	PCHK# Valid Delay	1.0	4.5	1.0	4.5	1.0	4.5	ns	
t_{10}	BREQ, HLDA, SMIACT# Valid Delay	1.0	4.0	1.0	4.0	1.0	4.0	ns	
t_{10}	HIT# Valid Delay	1.0	4.0	1.0	4.0	1.0	4.0	ns	
t_{10}	BE7-BE0#, CACHE#, PCD, PWT, SCYC Valid Delay	1.0	4.0	1.0	4.0	1.0	4.0	ns	
t_{10}	D63-D0, DP7-DP0 Write Data Valid Delay	1.3	4.5	1.3	4.5	1.3	4.5	ns	
t_{10}	HITM# Valid Delay	1.0	5.5	1.1	4.0	1.1	4.0	ns	
t_{10}	LOCK# Valid Delay	1.0	6.0	1.1	4.0	1.1	4.0	ns	

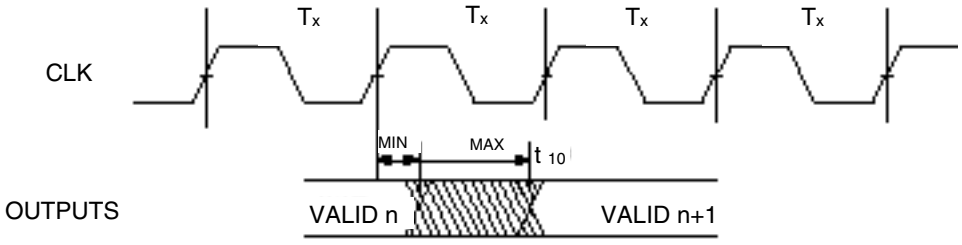


FIGURE 8B. OUTPUT VALID DELAY WAVEFORM

TABLE 28A. AC SPECIFICATIONS (CONTINUED) SEE TABLE 26 FOR RECOMMENDED OPERATING RANGE, C_L = 50 PF

Symbol	Parameter	60 MHZ		66 MHZ		75 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
t_{20}	A31-A3, ADS#, ADSC#, AP, BE7-BE0#, CACHE#, D/C#, LOCK#, M/IO#, PCD, PWT, SCYC, W/R# D63-D0, DP7-DP0 Write Data Float Delay		7.0		7.0		7.0	ns	1

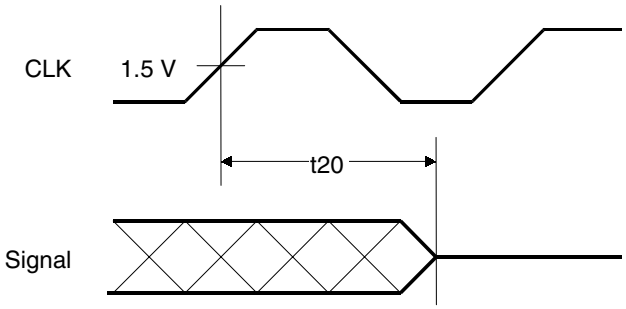


FIGURE 9A. OUTPUT FLOAT DELAY WAVEFORM

TABLE 28B. AC SPECIFICATIONS (CONTINUED) SEE TABLE 26 FOR RECOMMENDED OPERATING RANGE, C_L = 50 PF

Symbol	Parameter	83 MHZ		95 MHZ		100 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
t_{20}	A31-A3, ADS#, ADSC#, AP, BE7-BE0#, CACHE#, D/C#, LOCK#, M/IO#, PCD, PWT, SCYC, W/R#, D63-D0, DP7-DP0 Write Data Float Delay		7.0		7.0		7.0	ns	1

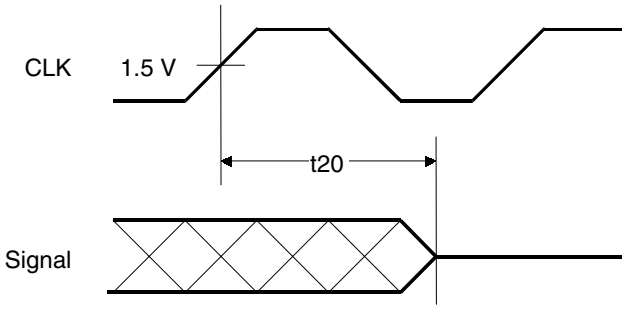


FIGURE 9B. OUTPUT FLOAT DELAY WAVEFORM

TABLE 28A. AC SPECIFICATIONS (CONTINUED)

See Table 26 for recommended operating range, C_L = 50 pF

Symbol	Parameter	60 MHZ		66 MHZ		75 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
t_{30}	D63-D0, DP7-DP0 Read Data Setup Time	3.0		3.0		3.0		nS	
t_{30}	NA#, WB/WT# Setup Time	4.5		4.5		3.3		nS	
t_{30}	A31-A5, A20M#, AHOLD, AP, BOFF#, BRDY#, BRDYC#, EWBE#, HOLD, INTR, INV, KEN#, STPCLK# Setup Time	5.0		5.0		3.3		nS	
t_{30}	FLUSH#, IGNNE#, INIT, NMI, SMI# Setup Time	5.0		5.0		3.3		nS	2
t_{30}	EADS# Setup Time	5.0		5.0		4.0		nS	
t_{40}	A20M#, AHOLD, AP, BOFF#, BRDY#, BRDYC#, EADS#, EWBE#, FLUSH#, HOL, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, SMI#, STPCL, WB/WT#, D63-D0, DP7-DP0, Read Data Hold Time	1.0		1.0		1.0		ns	
t_{45}	FLUSH#, INIT, NMI, SMI#, IGNNE# Pulse Width, Async.	2		2		2		CLKs	2

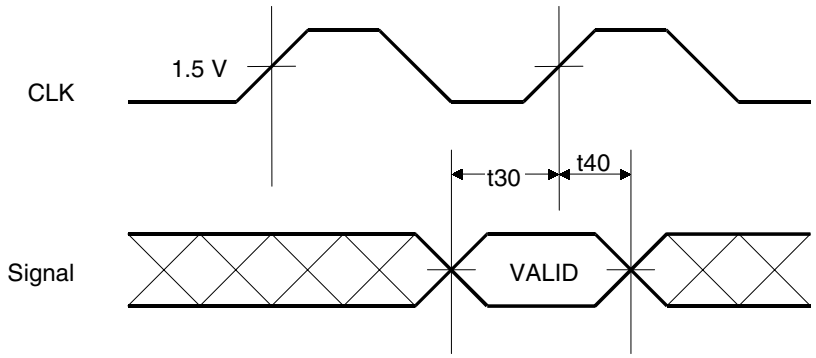


FIGURE 10A. INPUT SETUP AND HOLD WAVEFORM

TABLE 28B. AC SPECIFICATIONS (CONTINUED)

See Table 26 for recommended operating range, C_L = 0 pF

Symbol	Parameter	83 MHZ		95 MHZ		100 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
t_{30}	STPCLK# Setup Time, and DP7-DP0 Read Data Setup Time	1.7		1.7		1.7		ns	
t_{30}	D63-D0 Read Data Setup Time	1.8		1.8		1.8		ns	
t_{30}	NMI, SMI# Setup Time	1.7		1.7		1.7		ns	2
t_{30}	A31-A5, A20M#, AP, BRDY#, BRDYC#, EADS#, EWBE#, FLUSH#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, WB/WT# Setup Time	3.0		3.0		3.0		ns	
t_{30}	AHOLD, BOFF# Setup Time	3.5		3.5		3.5		ns	
t_{40}	A31-A5, A20M#, AHOLD, AP, BOFF#, BRDY#, BRDYC#, EADS#, EWBE#, FLUSH#, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, SMI#, STPCLK#, WB/WT#, D63-D0, DP7-DP0, HOLD Read Data Hold Time	1.0		1.0		1.0		ns	
t_{45}	FLUSH#, INIT, NMI, SMI#, IGNNE# Pulse Width, Async.	2		2		2		CLKs	2

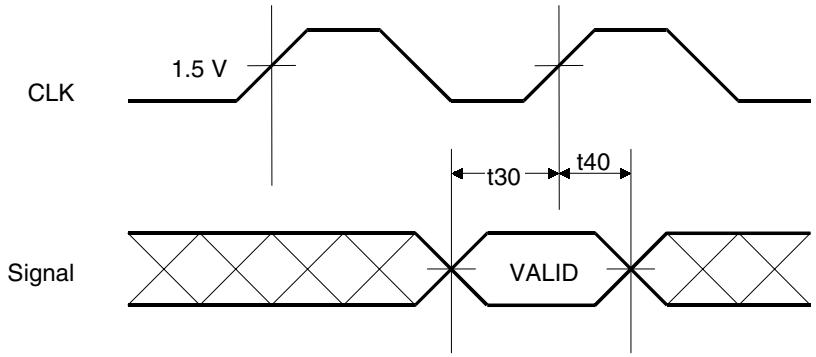


FIGURE 10B. INPUT SETUP AND HOLD WAVEFORM

TABLE 28A. AC SPECIFICATIONS (CONTINUED)

See Table 26 for recommended operating range, C_L = 50 pF

Symbol	Parameter	60 MHZ		66 MHZ		75 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
t_{50}	RESET Setup Time	5.0		5.0		5.0		ns	
t_{51}	RESET Hold Time	1.0		1.0		1.0		ns	
t_{52}	RESET Pulse Width, VCC & CLK Stable	15		15		15		CLKs	2
t_{52}	RESET Active After VCC & CLK Stable	1.0		1.0		1.0		ms	7
t_{53}	RESET Configuration Signals (BRDY#, BRDYC#, FLUSH#, INIT) Setup Time	2.0		2.0		2.0		CLKs	3, 4
t_{54}	RESET Configuration Signals (BRDY#, BRDYC#, FLUSH#, INIT) Hold Time	2.0		2.0		2.0		CLKs	3, 4
t_{53}	BF0, BF1 Setup Time	1.0		1.0		1.0		ms	5, 6
t_{54}	BF0, BF1 Hold Time	2		2		2		CLKs	5, 6

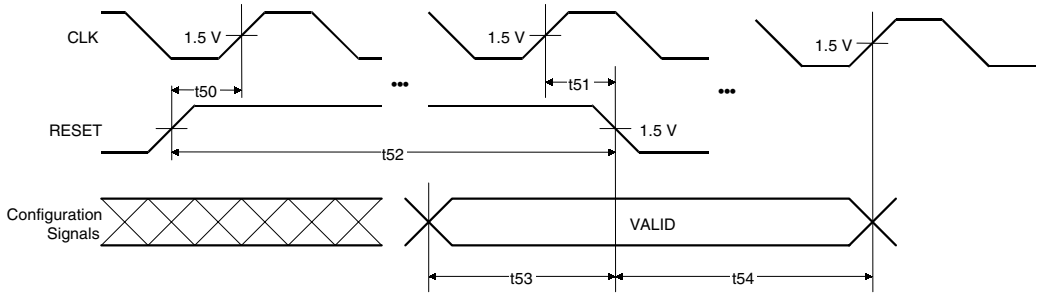


FIGURE 11A. RESET-CONFIGURATION WAVEFORMS

Notes:

1. Not 100% tested, guaranteed by design.
2. To provide proper asynchronous operation, RESET, NMI, FLUSH#, INIT and SMI# must be inactive for a minimum of 2 clocks before returning to the active state.
3. If FLUSH# is sampled active (low) at the falling edge of RESET, the output drivers will be put into tristate mode.
4. If INIT is sampled active (high) at the falling edge of RESET, the processor will execute its BIST algorithm.
5. Timing is relative to the falling edge of RESET.
6. BF1 and BF0 should be tied to VCC_{IO} or VSS. Also see Table 24. Defaults via internal pull up / pull down resistors are BF1=1, BF0=0.
7. Active period at system power up.

TABLE 28B. AC SPECIFICATIONS (CONTINUED)

See Table 26 for recommended operating range, C_L = 0 pF

Symbol	Parameter	83 MHZ		95 MHZ		100 MHz		UNIT	NOTES
		MIN	MAX	Min	Max	Min	Max		
t_{50}	RESET Setup Time	1.7		1.7		1.7		ns	
t_{51}	RESET Hold Time	1.0		1.0		1.0		ns	
t_{52}	RESET Pulse Width, VCC & CLK Stable	15		15		15		CLKs	2
t_{52}	RESET Active After VCC & CLK Stable	1.0		1.0		1.0		ms	7
t_{53}	RESET Configuration Signals (BRDY#, BRDYC#, FLUSH#, INIT) Setup Time	2		2		2		CLKs	3, 4
t_{54}	RESET Configuration Signals (BRDY#, BRDYC#, FLUSH#, INIT) Hold Time	2		2		2		CLKs	3, 4
t_{53}	BF0, BF1 Setup Time	1.0		1.0		1.0		ms	5, 6
t_{54}	BF0, BF1 Hold Time	2		2		2		CLKs	5, 6

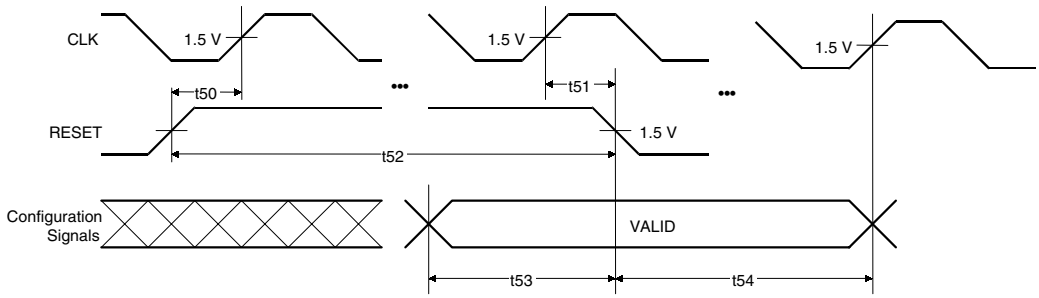


FIGURE 11B. RESET-CONFIGURATION WAVEFORMS

Notes:

1. Not 100% tested, guaranteed by design.
2. To provide proper asynchronous operation, RESET, NMI, FLUSH#, INIT and SMI# must be inactive for a minimum of 2 clocks before returning to the active state.
3. If FLUSH# is sampled active (low) at the falling edge of RESET, the output drivers will be put into tristate mode.
4. If INIT is sampled active (high) at the falling edge of RESET, the processor will execute its BIST algorithm.
5. Timing is relative to the falling edge of RESET.
6. BF1 and BF0 should be tied to VCC_{IO} or VSS. Also see Table 24. Defaults via internal pull up / pull down resistors are BF1=1, BF0=0.
7. Active period at system power up.

TABLE 29. JTAG AC SPECIFICATIONS

See Table 16 for recommended operating range, C_L = 50 pF

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
f_{TCK}	TCK Frequency		16.0	MHz		
t_{61}	TCK Period	62.5		ns		
t_{63}	TCK High Time	25.0		ns		
t_{64}	TCK Low Time	25.0		ns		
t_{65}	TCK Fall Time		5.0	ns		
t_{66}	TCK Rise Time		5.0	ns		
t_{69}	TRST# Pulse Width – Asynchronous	40.0		ns		1
t_{71}	TDI, TMS Setup Time	10.0		ns		2
t_{72}	TDI, TMS Hold Time	13.0		ns		2
t_{73}	TDO Valid Delay	3.0	20.0	ns		3
t_{74}	TDO Float Delay		25.0	ns		3
t_{75}	All outputs (excluding test) Valid Delay	3.0	20.0	ns		3,4
t_{76}	All outputs (excluding test) Float Delay		25.0	ns		3,4
t_{77}	All inputs (excluding test) Setup Time	10.0		ns		2,4
t_{78}	All inputs (excluding test) Hold Time	13.0		ns		2,4

Notes:

1. Not 100% tested, guaranteed by design.
2. Referenced to rising edge of TCK.
3. Referenced to falling edge of TCK.
4. Test input and outputs are TCK, TRST#, TDI, TDO, and TMS. Timing for the normal inputs and outputs are in response to JTAG boundary scan operations.

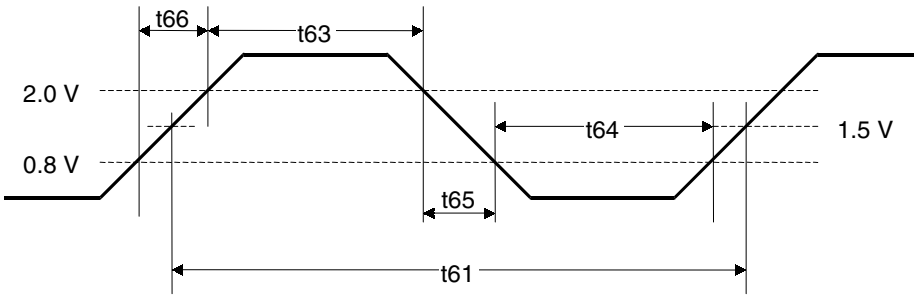


FIGURE 12. TEST CLOCK INPUT WAVEFORM

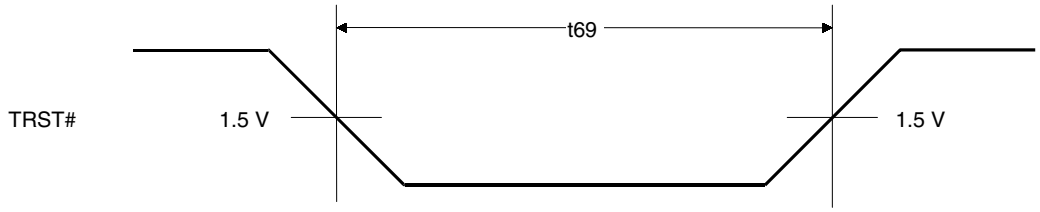


FIGURE 13. TEST RESET WAVEFORM

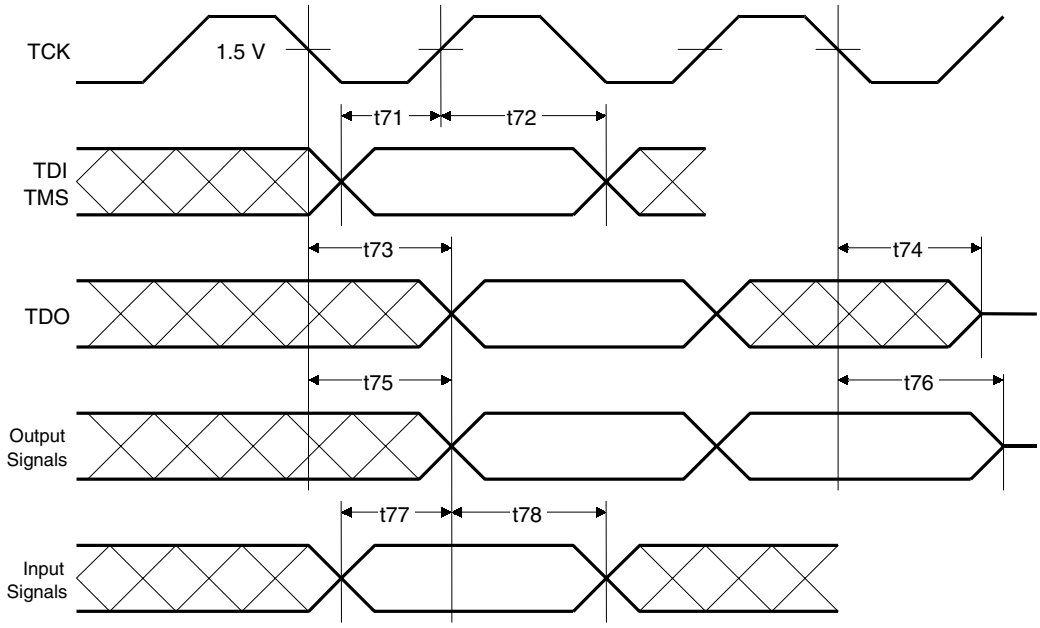
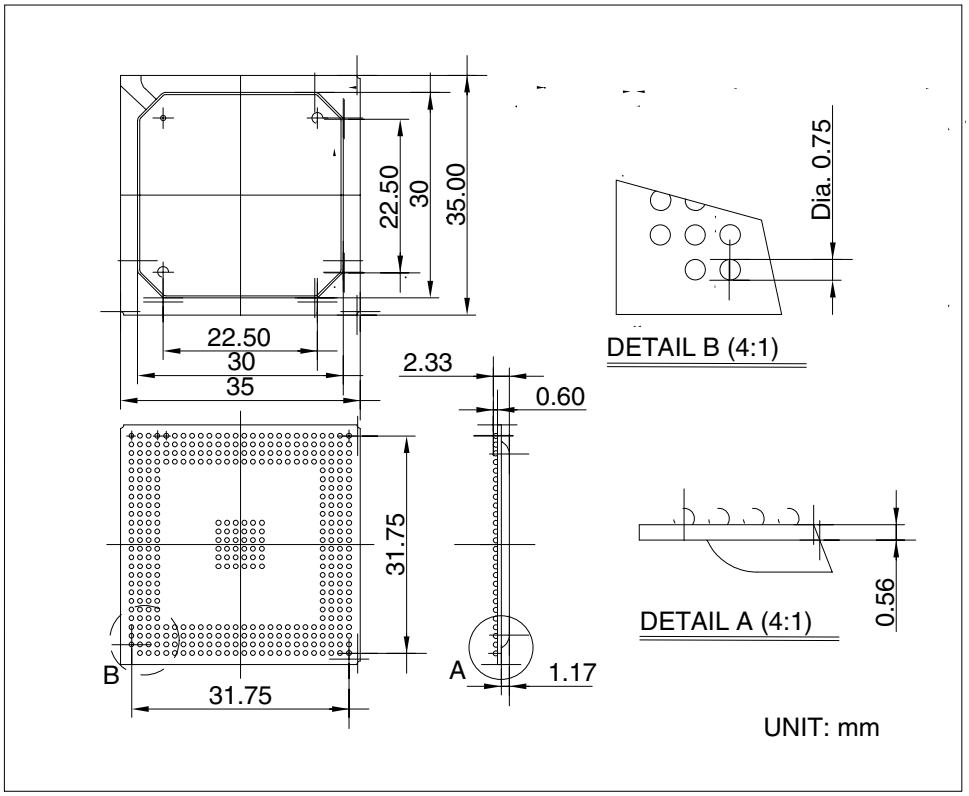


FIGURE 14. JTAG TEST WAVEFORMS

4 Mechanical Specifications

4.1 387 Ball PBGA (35X35 mm) Mechanical Drawing

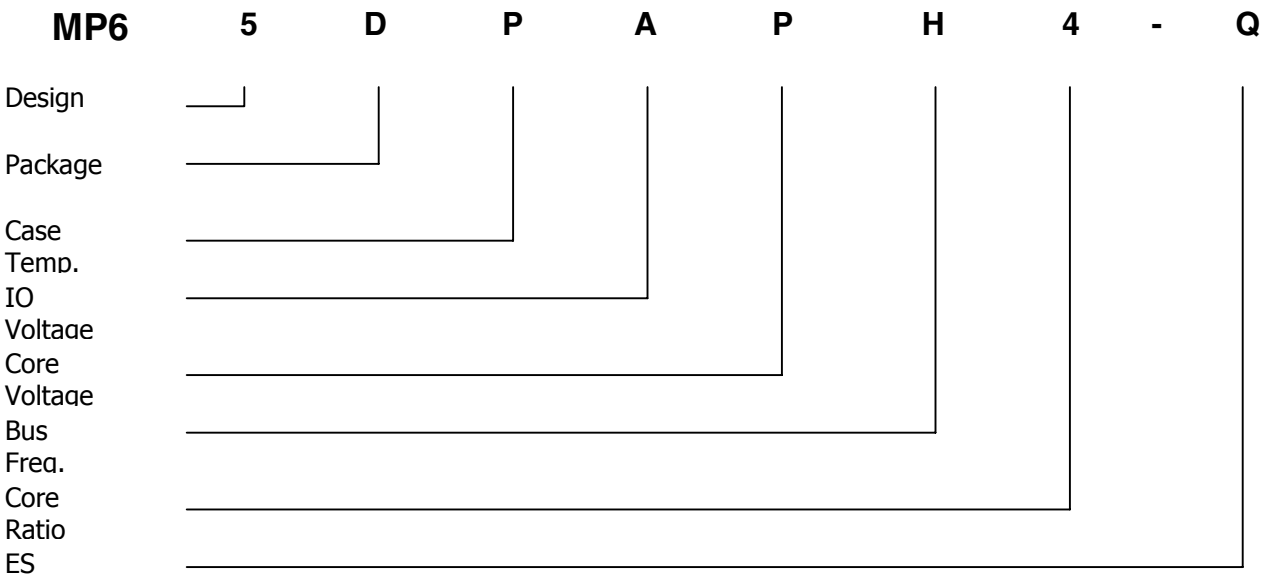


NOTE:

1. Controlling dimension: Millimeter.
2. There shall be a minimum clearance of 0.25 mm between the edge of the solder ball and the body edge.

5 Part Number

For mP6-500MIPS:



For mP6-600MIPS: MP6 5 D P A P H 5 - Q

Design	5
Package	D = BGA
Case Temp.	P = 0 C° ~ 70 C°
IO Voltage	A = 3.3 V
Core Voltage	P = 2.0 V
Bus Freq. (MHz)	E = 83 G = 95 H = 100

Core Ratio	4 = 2X bus 5 = 2.5X bus 6 = 3X bus 7 = 3.5X bus
ES	ES = Eng. Sample Q = Mass Production