What technology do you use for this iDragon SCX501?
We have selected to use our mature HCMOS6 technology to optimize yield and chip costs. This technology allows less than 4 Watts of power dissipation, and is packed in a Plastic Ball Grid Array package that requires no fan!

Is HCMOS6 a 0.35µm technology?
Yes.

What are the advantages of a fully static design?
It is used to minimize power consumption.

What are the advantages of the unified memory architecture?
It permits graphics on a 64-bit local bus and also reduces the pin count of the IC, so reducing the cost of the packaging.

What core is in the chip? Is it a Pentium?
It is a single pipeline, five stage x86 microprocessor with 8KB of write back cache. The iDragon SCX501 devices use Pentium architecture in that the CPU local bus interface is 64 bits wide. The design takes the best features of the Pentium-class chipset and the advantages of Unified Memory Architecture (UMA) and marries them with the space saving of a single-pipeline x86 processor.

How can I shutdown the FPU to reduce power consumption?
There is no FPU power control available by software, it automatically shuts down when unused.

Is it possible to connect directly a 3.3V DRAM? a 5V DRAM?
The SDRAM Interface is designed for 3.3V devices and is not 5V I/O tolerant.

What VGA controller is integrated into the iDragon SCX501 devices?
A fully compatible VGA and SVGA controller and a 2D accelerator - see databook.

What is the minimum dot frequency of the VGA output?
Minimum DCLK frequency is 8MHz.

Is it possible to disable the on-chip VGA controller?
Yes, by software or hardware. See datasheet and BIOS Writer's Guide.

What REF voltage does the internal RAMDAC need?
1.235v (LM385BZ) typical.

Is there an internal voltage references for VGA DAC's?
No.

Can I use the VIP at a frequency lower than 27 MHz?
Yes.

Should I feed video data to memory through the PCI bus?
No, we absolutely do not recommend using PCI to feed the decoded stream into the iDragon SCX501. It clogs the bus and slugs the processor. You should use the CCIR 601/656 port to read into the video frame buffer.

You support both CCIR601 and CCIR656 modes. What is the difference?
In CCIR656 mode, you just have an 8-bit data bus and a clock. Synchronization information is provided by video timing reference codes within the video data stream.
In CCIR601 mode, the synchronization information is provided by 2 additional signals: Horizontal Synchronization and Vertical Synchronization
.
Does the VIP interface support interlaced and non-interlaced video input?
Yes. This is programmable.

Does iDragon SCX501 supports Picture In Picture?
Yes, thanks to CCIR video input port and video Pipeline.

Is it possible to switch off the color space conversion?
No.

I do not use the PCI interface. Can I leave it unconnected?
No. Even if you do not need the external PCI interface, you have to pull-up FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, LOCK#, SERR# to 5V (or 3.3V) through 2K2 resistors. You also have to connect PCI_CLKO to PCI_CLKI through a 50 to 100 Ohms resistor.

Is the PCI bus speed programmable?
Yes. It can be 1/2 or 1/3 of system speed (HCLK) selectable by strap option at Power On.

Is it possible to disable the PCI-bus interface?
No. It is used internally.

What are VDD5 pins?
They are 5 volts supplies to the PCI bus driver pads. They are used to make the PCI pads 5V tolerant. They can be connected to 3.3V in case PCI bus is unused, or used only with 3.3V devices.

When do I have to put a '245 buffer between ISA bus and the BIOS Flash?
When the Flash can not drive the ISA data bus. If there is no ISA connector on the application, it is OK. If the potential load on this bus is important, it is better to keep this it.

I don't need the external ISA Bus. Can I use DMA Channels 0 and 1 for something else?
Yes, you can. There is no hardware constraint.

How could I use the GPIOCS# signal?
The General Purpose IO Chip Select is controlled by the 8-bit General Purpose Register (Index 7Bh, CPC). A write to this register will assert the GPIOCS# signal while the data are driven to the ISA SD[ ] bus, updating the optional external '373 latch. Reads of this register return the value of this internal register without asserting the GPIOCS# signal. See Databook for more details.

How can I address additional Flash memory via the ISA bus? Can I use GPIOCS# signals?
GPIOCS# decoding is incompatible with the required access when you want to erase/program a Flash. You need to use external programmable Logic.

Do you support 16-bit I/O-decode?
No. The device supports 10-bit I/O decodes.

I'm not using the IDE interface. Can I remove the external buffers driven by ISAOE#?
When NO IDE interface is used, there is no need to take care of the ISAOE# signal and the SA[8:19] are directly driving the ISA bus; they have 6mA current capability on a TTL load.
Could you provide IBIS model for iDragon SCX501 devices?
Yes.

Do you need to add anything to make a PC with this IC?
The only things you need to add are memory and a super I/O chip. RISE decided not to integrate the super I/O chip because it would have added a lot of pins (and therefore cost) to the iDragon SCX501.

What audio device should I use with the iDragon SCX501?
We do not recommend any particular audio device. Any PC compatible one should work.

On the evaluation board, why RTC is externally attached?
The Real Time Clock is not included in the iDragon SCX501. On the evaluation board, it is in the Super I/O chip. But the iDragon SCX501 provides also signals to handle an external RTC in case it is not integrated into the Super I/O.

On the evaluation board, IRQ8 is active high. Why no pull-down is used as for the others IRQs?
Because it is driven by the Super I/O. The others are coming from the ISA bus and can't be left floating. Interrupts are active either on rising edge or on low level.

What is the frequency of the external Quartz/Oscillator?
14.31818MHz.

Does it need any other clock beside the master 14MHz quartz/oscillator?
No in most cases. An external 27MHz oscillator is needed when using the composite TV output.

Is there a thermal register?
No.

Are the iDragon SCX501 devices compliant with year 2000?
The devices do not store date information that is taken care of by the BIOS and the real time clock. Neither of which are in our devices, so that iDragon SCX501 compliance is not relevant.

Does RISE will support BIOS?
RISE works closely with all major BIOS providers to have them supporting iDragon SCX501.

What operating systems are available for the iDragon SCX501?
Like any x86 compatible CPU, the iDragon SCX501 is compatible with all O.S. that run on x86 architecture. Today we have Windows 3.xx, 95, 98, Windows CE, QNX, DOS, ROM-DOS, VxWorks, Linux and many others running on the iDragon SCX501 devices.

Do I need specific driver for my OS to use VGA?
If you just use VGA no specific driver is necessary. If you want to use the 2D accelerator, you need a graphics driver for your OS.

Do I need specific driver for my OS to use IDE?
If you use a HD no driver is needed for legacy IDE but EIDE needs an OS driver for optimum performance.

Do I need specific driver for my OS to use video capture?
Yes.

Is it possible to disable dynamically the video controller to give DRAM bandwidth for applications instead?
Yes. See databook for details.

How to access the iDragon SCX501 INTERNET site?
http://www.rise.com/

Does RISE offer reference designs, evaluation boards and other development tools?
Evaluation boards and applications notes will be available for each device.

In terms of price/performance, how does this compare with Intel's latest microprocessors?
This comparison is meaningless. These products are not aimed at replacing the latest product from Intel or being used in a standard desktop PC

Does RISE expect to design iDragon SCX501 with a DX4 core?
No. It is not the best approach to higher performance for an integrated CPU core/chipset product.

Does RISE expect to design iDragon SCX501 devices with 16-bit memory interface?
No. Pentium architecture means 64-bit. We may design external 32-bit DRAM interface

As iDragon SCX501 looks like IBM PC/AT architecture. Who has to pay royalties to IBM?
There is no need to pay any royalty to anybody. IBM PC/AT architecture is open. IBM holds some patents on key pieces of the PC architecture but the iDragon SCX501 devices are designed in such a way that RISE avoids infringing them. In addition, RISE has several cross patents.

What are the typical applications targeted by the iDragon SCX501's customers?
Internet browsers, set-top boxes, point of sale terminals, educational PCs, in car entertainment, gaming machines, in flight entertainment systems, thin clients, ATM machines, and many more applications