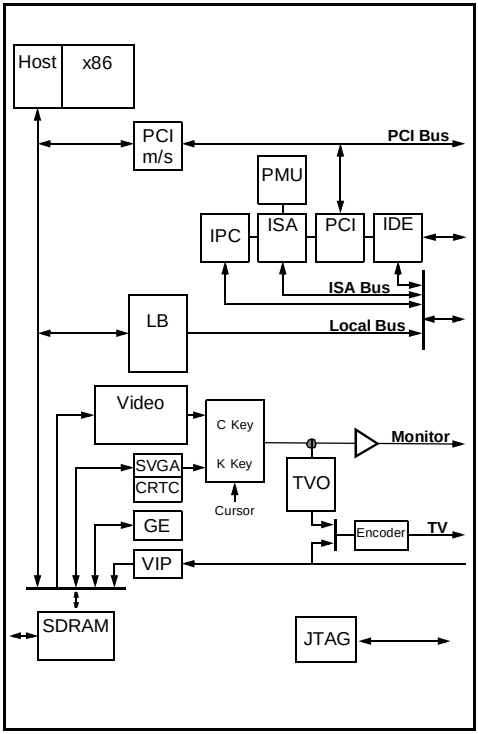
- POWERFUL x86 PROCESSOR
- 64-BIT SDRAM UMA CONTROLLER
- VGA & SVGA CRT CONTROLLER
- 135MHz RAMDAC
- 2D GRAPHICS ENGINE
- VIDEO INPUT PORT
- VIDEO PIPELINE
  - UP-SCALER
  - VIDEO COLOR SPACE CONVERTER
  - CHROMA & COLOUR KEY SUPPORT
- TV OUTPUT
  - 3-LINE FLICKER FILTER
  - CCIR 601/656 SCAN CONVERTER
  - NTSC / PAL COMPOSITE, RGB, S-VIDEO
- PCI MASTER / SLAVE / ARBITER
- ISA MASTER / SLAVE
- OPTIONAL 16-BIT LOCAL BUS INTERFACE
- EIDE CONTROLLER
- I²C INTERFACE
- IPC
  - DMA CONTROLLER
  - INTERRUPT CONTROLLER
  - TIMER / COUNTERS
- POWER MANAGEMENT UNIT
- JTAG IEEE1149.1


PBGA388

**Figure 0-1. Logic Diagram**




## DESCRIPTION

The iDragon SCX502 integrates a standard 5th generation x86 core, a Synchronous DRAM controller, a graphics subsystem, a video pipeline, and support logic including PCI, ISA, and IDE controllers to provide a single consumer orientated PC compatible subsystem on a single device.
The device is based on a tightly coupled Unified Memory Architecture (UMA), sharing memory between the CPU, the graphics and the video.

The iDragon SCX502 is packaged in a 388 Plastic Ball Grid Array (PBGA).

- **X86 Processor core**
- Fully static 32-bit 5-stage pipeline, x86 processor fully PC compatible.
- Can access up to 4GB of external memory.
- 8Kbyte unified instruction and data cache with write back and write through capability.
- Parallel processing integral floating point unit, with automatic power down.
- Runs up to 100MHz (x1) or 133 MHz (x2).
- Fully static design for dynamic clock control.
- Low power and system management modes.
- Optimized design for 2.5V operation.

- **SDRAM Controller**
- 64-bit data bus.
- Up to 100MHz SDRAM clock speed.
- Integrated system memory, graphic frame memory and video frame memory.
- Supports 2MB up to 128 MB system memory.
- Supports 16-, 64-, and 128-Mbit SDRAMs.
- Supports 8, 16, 32, 64, and 128 MB DIMMs.
- Supports buffered, non buffered, and registered DIMMs
- 4-line write buffers for CPU to SDRAM and PCI to SDRAM cycles.
- 4-line read prefetch buffers for PCI masters.
- Programmable latency
- Programmable timing for SDRAM parameters.
- Supports -8, -10, -12, -13, -15 memory parts
- Supports memory hole between 1MB and 8MB for PCI/ISA busses.

- **2D Graphics Controller**
- 64-bit windows accelerator.
- Backward compatibility to SVGA standards.
- Hardware acceleration for text, bitblts, transparent blts and fills.
- Up to 64 x 64 bit graphics hardware cursor.
- Up to 4MB long linear frame buffer.
- 8-, 16-, 24- and 32-bit pixels.
- Drivers availables for various OSes.

- **CRT Controller**
- Integrated 135MHz triple RAMDAC allowing for 1280 x 1024 x 75Hz display.
- Requires external frequency synthesizer and reference sources.
- 8-, 16-, 24-bit pixels.
- Interlaced or non-interlaced output.
- Requires no external frequency synthesizer.
- Requires only external reference source.

- **Video Input port**
- Accepts video inputs in CCIR 601 mode.
- Optional 2:1 decimator
- Stores captured video in off setting area of the onboard frame buffer.
- Video pass through to the TV output for full screen video images.
- HSYNC and B/T generation or lock onto external video timing source.

- **Video Pipeline**
- Two-tap interpolative horizontal filter.
- Two-tap interpolative vertical filter.
- Color space conversion (RGB to YUV and YUV to RGB).
- Programmable window size.
- Chroma and color keying for integrated video overlay.

- **Video Output**
- NTSC-M; PAL-B, D, G, H, I, M, N encoding.
- 4 analog outputs in two configurations:
  - R,G,B + CVBS
  - C,YS,CVBS1 + CVBS2
- Flicker-free interlaced output.
- Programmable two tap filter with gamma correction or three tap flicker filter.
- Interlaced operation mode.
- Progressive to interlaced scan converter.
- Cross color reduction by specific trap filtering on luma within CVBS flow.
- Power down mode available on each DAC.

- **PCI Controller**
- Fully compliant with PCI 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. ExternalPAL allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- PCI clock is 1/2, 1/3 or 1/4 cpu bus clock.

- **ISA master/slave**
- Generates the ISA clock from either 14.318MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus.

- **Local Bus interface**
- Multiplexed with ISA/DMA interface.
- Low latency asynchronous bus
- 22-bit address bus.
- 16-bit data bus with word steering capability.
- Programmable timing (Host clock granularity)
- 2 Programmable Flash Chip Select.
- 4 Programmable I/O Chip Select.
- Supports 32-bit Flash burst.
- 2-level hardware key protection for Flash boot block protection.
- Supports 2 banks of 16MB flash devices with boot block shadowed to 0x000F0000.

- **IDE Interface**
- Supports PIO
- Transfer Rates to 22 MBytes/sec
- Supports up to 4 IDE devices
- Concurrent channel operation (PIO modes) - 4 x 32-Bit Buffer FIFOs per channel
- Support for PIO mode 3 & 4.
- Individual drive timing for all four IDE devices
- Supports both legacy & native IDE modes
- Supports hard drives larger than 528MB
- Support for CD-ROM and tape peripherals
- Backward compatibility with IDE (ATA-1).
- Drivers for Windows and other Operating Systems

- **Integrated Peripheral Controller**
- 2X8237/AT compatible 7-channel DMA controller.
- 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel port.
- 128K SM_RAM address space from 0xA0000 to 0xB0000

- **JTAG**
- Boundary Scan compatible IEEE1149.1.
- Scan Chain control.
- Bypass register compatible IEEE1149.1.
- ID register compatible IEEE1149.1.
- RAM BIST control.

# 1 GENERAL DESCRIPTION

At the heart of the iDragon SCX502 is an advanced 64-bit x86 processor block. It includes a 64-bit SDRAM controller, advanced 64-bit accelerated graphics and video controller, a high speed PCI local-bus controller and Industry standard PC chip set functions (Interrupt controller, DMA Controller, Interval timer and ISA bus).

The iDragon SCX502 has in addition, an EIDE Controller, $I^2C$ Interface, a Local Bus interface and a JTAG interface.

The iDragon SCX502 makes use of a tightly coupled Unified Memory Architecture (UMA), where the same memory array is used for CPU main memory and graphics frame-buffer. This means a reduction in total system memory for system performances that are equal to that of a comparable frame buffer and system memory based system, and generally much better, due to the higher memory bandwidth allowed by attaching the graphics engine directly to the 64-bit processor host interface running at the speed of the processor bus rather than the traditional PCI bus. The 64-bit wide memory array provides the system with 528MB/s peak bandwidth. This allows for higher resolution screens and greater color depth.

The 'standard' PC chipset functions (DMA, interrupt controller, timers, power management logic) are integrated together with the x86 processor core; additional functions such as communications ports are accessed by the iDragon SCX502 via internal ISA bus.

The PCI bus is the main data communication link to the iDragon SCX502 chip. The iDragon SCX502 translates appropriate host bus I/O and Memory cycles onto the PCI bus. It also supports generation of Configuration cycles on the PCI bus. The iDragon SCX502, as a PCI bus agent (host bridge class), fully complies with PCI specification 2.1. The chip-set also implements the PCI mandatory header registers in Type 0 PCI configuration space for easy porting of PCI aware system BIOS. The device contains a PCI arbitration function for three external PCI devices.

The iDragon SCX502 has two functional blocks *sharing the same balls* : The ISA / IPC / IDE block and the Local Bus / IDE block (see Table 3). Any board with the iDragon SCX502 should be built using only one of these two configurations. The IDE pins are dynamically multiplexed in each of the blocks in ISA mode only.

Configuration is done by 'strap options'. It is a set of pull-up or pull-down resistors on the memory data bus, checked on reset, which auto-configure the iDragon SCX502.

**GRAPHICS FUNCTIONS**

Graphics functions are controlled through the on chip SVGA controller and the monitor display is produced through the 2D graphics display engine.

This Graphics Engine is tuned to work with the host CPU to provide a balanced graphics system with a low silicon area cost. It performs limited graphics drawing operations which include hardware acceleration of text, bitblts, transparent blts and fills. The results of these operations change the contents of the on-screen or off-screen frame buffer areas of SDRAM memory. The frame buffe can occupy a space up to 4 Mbytes anywhere in the physical main memory.

The graphics resolution supported is a maximum of 1280x1024 in 16M colors and 16M colors at 75Hz refresh rate, VGA and SVGA compatible. Horizontal timing fields are VGA compatible while the vertical fields are extended by one bit to ac commodate above display resolution.

**VIDEO FUNCTIONS**

The iDragon SCX502 provides several additional functions to handle MPEG or similar video streams. The Video Input Port accepts an encod ed digital video stream in one of a number of in dustry standard formats, decodes it, optionally decimates it, and deposits it into an off screen area of the frame buffer. An interrupt request can be generated when an entire field or frame has been captured. The video output pipeline incorpo rates a video-scaler and color space converte function and provisions in the CRT controller to display a video window. While repainting the screen the CRT controller fetches both the video as well as the normal non-video frame buffer in two separate internal FIFOs. The video stream can be color-space converted (optionally) and smooth scaled. Smooth interpolative scaling in both horizontal and vertical direction are imple mented. Color and Chroma key functions are also implemented to allow mixing video stream with non-video frame buffer.

The video output passes directly to the RAMDA for monitor output or through another optional color space converter (RGB to 4:2:2 YCrCb) to the programmable anti-flicker filter. The flicker filter is

configured as either a two line filter with gamma correction (primarily designed for DOS type text) or a 3 line flicker filter (primarily designed for Windows type displays). The fliker filter is optional and can be software disabled for use with large screen area's of video.

The Video output pipeline of the iDragon SCX502 interfaces directly to the internal digital TV encoder. It takes a 24 bit RGB non-interlaced pixel stream and converts to a multiplexed 4:2:2 YCrCb 8 bit output stream, the logic includes a progressive to interlaced scan converter and logic to insert appropriate CCIR656 timing reference codes into the output stream. It facilitates the high quality display of VGA or full screen video streams received via the Video input port to standard NTSC or PAL televisions.

The digital PAL/NTSC encoder outputs interlaced or non-interlaced video in PAL-B,D,G,H,I PAL-N, PAL-M or NTSC-M standards and "NTSC- 4.43" is also possible.

The four frame (for PAL) or 2 frame (for NTSC) burst sequences are internally generated, subcarrier generation being performed numerically with CKREF as reference. Rise and fall times of synchronisation tips and burst envelope are internally controlled according to the relevant ITU-R and SMPTE recommendations.

Video output signals are directed to four analog output pins through internal D/A converters giving, simultaneous R,G,B and composite CVBS outputs.

## MEMORY CONTROLLER

The iDragon handles the memory data (DATA) bus directly, controlling from 2 to 128 MBytes. The SDRAM controller supports accesses to the Memory Banks to/from the CPU (via the host), from the VMI, to/from the CRTC, to the VIDEO & to/from the GE. (Banks 0 to 3) which can be populated with either single or double sided 72-bit (4 bit parity) DIMMs. Parity is not supported.

The SDRAM controller only supports 64 bit wide Memory Banks.

Four Memory Banks (if DIMMS are used; Single sided or two double-sided DIMMs) are supported in the following configurations (see Table 1-1)

**Table 1-1. Memory configurations**

| Memory Bank size | Number | Organisation | Device Size |
|---|---|---|---|
| 1Mx64 | 4 | 1Mx16 | 16Mbits |
| 2Mx64 | 8 | 2Mx8 | |
| 4Mx64 | 16 | 4Mx4 | |
| 4Mx64 | 4 | 2Mx16x2 | 64Mbits |
| 8Mx64 | 8 | 4Mx8x2 | |
| 16Mx64 | 16 | 8Mx4x2 | |
| 4Mx64 | 4 | 1Mx16x4 | |
| 8Mx64 | 8 | 2Mx8x4 | |
| 32Mx64 | 16 | 4Mx4x4 | |
| 16Mx64 | 8 | 2Mx16x2 | 128Mbits |
| 32Mx64 | 16 | 4Mx8x4 | |

The SDRAM Controller supports buffered or un buffered SDRAM but not EDO or FPM modes. SDRAMs must support Full Page Mode Type access.

The iDragon Memory Controller provides various programmable SDRAM parameters to allow the SDRAM interface to be optimized for different processor bus speeds SDRAM speed grades and CAS Latency.

## IDE INTERFACE

An industry standard EIDE (ATA 2) controller is built into the iDragon SCX502. The IDE port is capable of supporting a total of four devices.

## POWER MANAGEMENT

The iDragon SCX502 core is compliant with the Advanced Power Management (APM) specification to provide a standard method by which the BIOS can control the power used by personal computers. The Power Management Unit module (PMU) controls the power consumption providing a comprehensive set of features that control the power usage and supports compliance with the United States Environmental Protection Agency's Energy Star Computer Program. The PMU provides following hardware structures to assist the software in managing the power consumption by the system.

- System Activity Detection.
- Three power down timers.

- Doze timer for detecting lack of system activity for short durations.
- Stand-by timer for detecting lack of system activity for medium durations
- Suspend timer for detecting lack of system activity for long durations.
- House-keeping activity detection.
- House-keeping timer to cope with short bursts of house-keeping activity while dozing or in stand-by state.
- Peripheral activity detection.
- Peripheral timer for detecting lack of peripheral activity
- SUSP# modulation to adjust the system performance in various power down states of the system including full power on state.
- Power control outputs to disable power from different planes of the board.

Lack of system activity for progressively longer period of times is detected by the three power down timers. These timers can generate SMI interrupts to CPU so that the SMM software can put the system in decreasing states of power consumption. Alternatively, system activity in a power down state can generate SMI interrupt to allow the software to bring the system back up to full power on state. The chip-set supports up to three power down states: Doze state, Stand-by state and Suspend mode. These correspond to decreasing levels of power savings.

**POWER DOWN**

Power down puts the iDragon SCX502 into suspend mode. The processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. During the suspend mode, internal clocks are stopped. Removing power down, the processor resumes instruction fetching and begins execution in the instruction stream at the point it had stopped. Because of the static nature of the core, no internal data is lost.

**Figure 1-1. Functionnal description.**

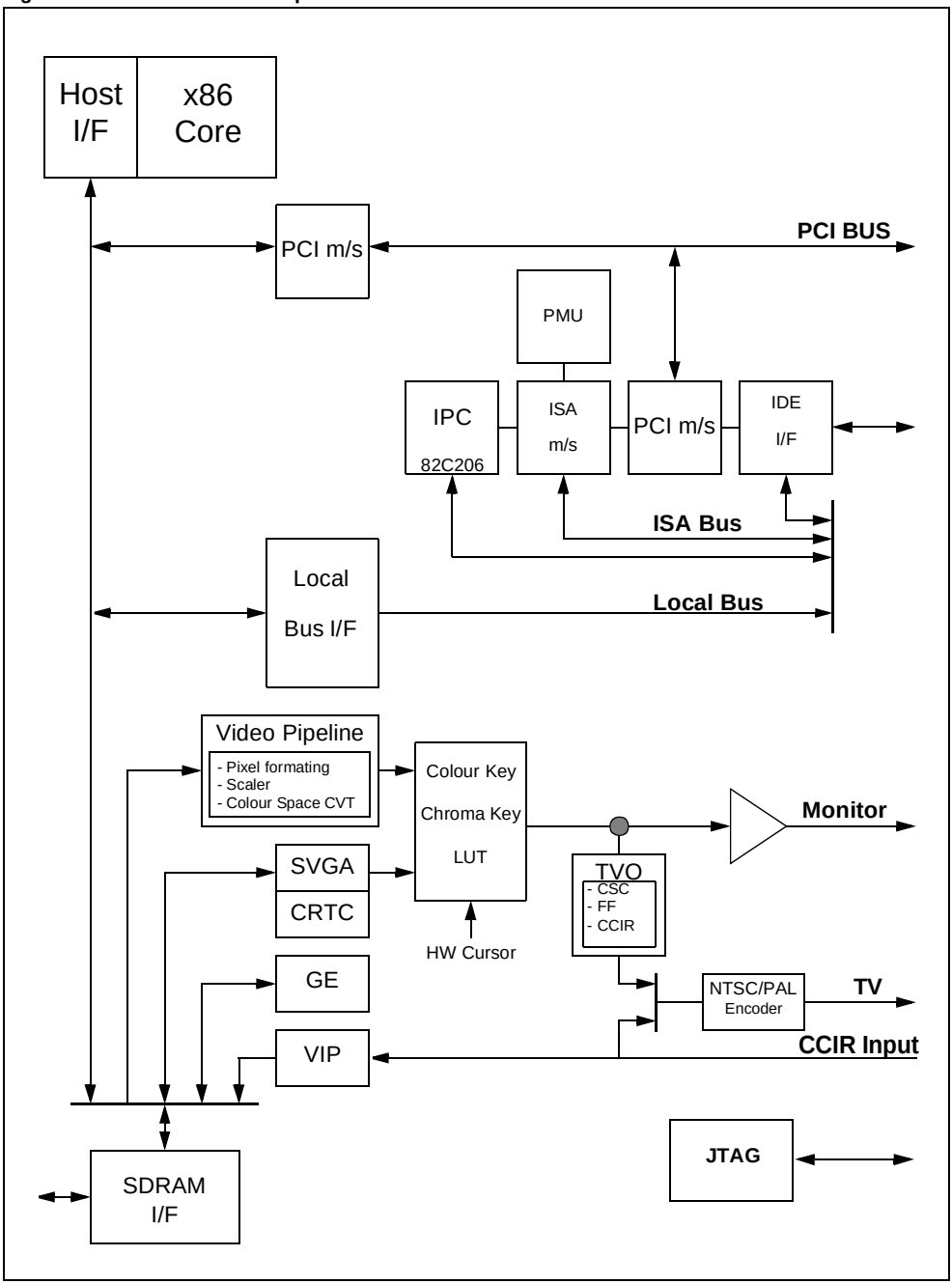
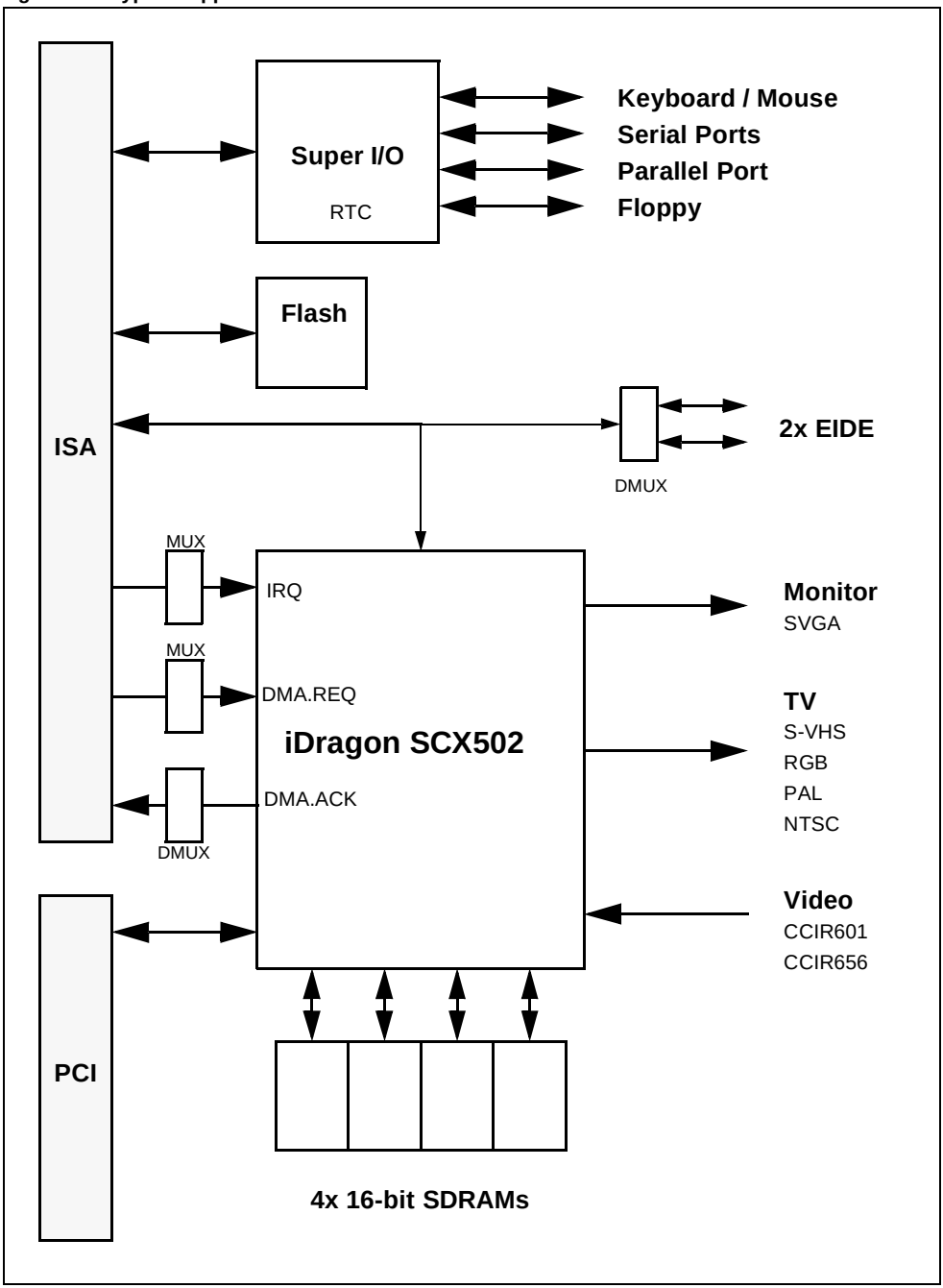


**Figure 1-2. Typical Application**



# 2 PIN DESCRIPTION

## 2.1 INTRODUCTION

The iDragon SCX502 integrates most of the functionalities of the PC architecture. As a result, many of the traditional interconnections between the host PC microprocessor and the peripheral devices are totally internal to the iDragon SCX502. This offers improved performance due to the tight coupling of the processor core and these peripherals. As a result many of the external pin connections are made directly to the on-chip peripheral functions.

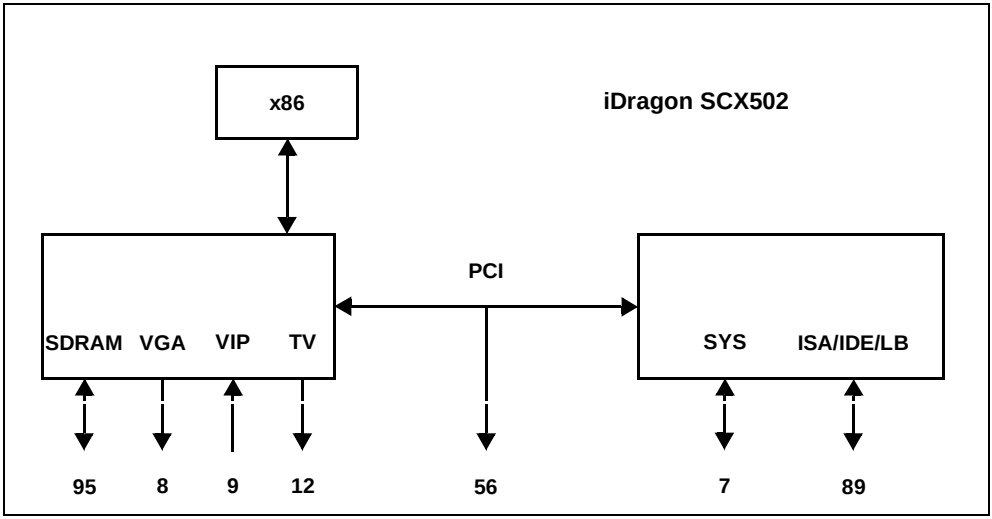
Figure 2-1 shows the iDragon SCX502 external interfaces. It defines the main busses and their function. Table 2-1 describes the physical implementation listing signals type and their functionality. Table 2-2 provides a full pin listing and description of pins. Table 2-5 provides a full listing of pin locations of the iDragon SCX502 package by physical connection.

**Table 2-1. Signal Description**

| Group name | Qty | |
|---|---|---|
| Basic Clocks reset & Xtal (SYS) | | 7 |
| SDRAM Controller | | 95 |
| PCI interface | | 56 |
| ISA | 79 | 89 |
| IDE | 34 | |
| Local Bus | 49 | |
| Video Input | | 9 |
| TV Output | | 12 |
| VGA Monitor interface | | 8 |
| Grounds | | 71 |
| $V_{DD}$ | | 26 |
| Miscellaneous | | 9 |
| Unconnected | | 6 |
| Total Pin Count | | 388 |

Note: Several interface pins are multiplexed with other functions, refer to Table 2-3 and Table 2-4 for further details

**Figure 2-1. iDragon SCX502 External Interfaces**



### Table 2-2. Definition of Signal Pins

| Signal Name | Dir | Description | Qty |
|---|---|---|---|
| BASIC CLOCKS AND RESETS | | | |
| SYSRSETI# | I | System Power Good Input | 1 |
| SYSRSTO# | O | System Reset Output | 1 |
| XTALI | I | 14.3MHz Crystal Input | 1 |
| XTALO | I/O | 14.3MHz Crystal Output - External Oscillator Input | 1 |
| HCLK[2] | I/O | Host Clock (Test) | 1 |
| DEV_CLK | O | 24MHz Peripheral Clock (floppy drive) | 1 |
| DCLK[2] | I/O | 27-135MHz Graphics Dot Clock | 1 |
| $V_{DD}$_xxx_PLL[1] | | Power Supply for PLL Clocks | |
| | | | |
| **SDRAM CONTROLLER** | | | |
| MCLKI | I | Memory Clock Input | 1 |
| MCLKO | O | Memory Clock Output | 1 |
| CS#[1:0] | O | DIMM Chip Select | 2 |
| CS2# / MA11 | O | DIMM Chip Select/ Memory Address/ Bank Address | 1 |
| CS3# / MA12 / BA1 | O | DIMM Chip Select/ Bank Address | 1 |
| BA[0] | O | Bank Address | 1 |
| MA[10:0][2] | O | Memory Row & Column Address | 12 |
| MD[63:0][3] | I/O | Memory Data | 64 |
| RAS#[1:0][2] | O | Row Address Strobe | 2 |
| CAS#[1:0][2] | O | Column Address Strobe | 2 |
| MWE#[2] | O | Write Enable | 1 |
| DQM[7:0] | O | Data Input/Output Mask | 8 |
| | | | |
| **PCI CONTROLLER** | | | |
| PCI_CLKI[2] | I | 33MHz PCI Input Clock | 1 |
| PCI_CLKO | O | 33MHz PCI Output Clock (from internal PLL) | 1 |
| AD[31:0][2] | I/O | PCI Address / Data | 32 |
| CBE[3:0][2] | I/O | Bus Commands / Byte Enables | 4 |
| FRAME#[2] | I/O | Cycle Frame | 1 |
| IRDY#[2] | I/O | Initiator Ready | 1 |
| TRDY# | I/O | Target Ready | 1 |
| LOCK#[2] | I | PCI Lock | 1 |
| DEVSEL#[2] | I/O | Device Select | 1 |
| STOP# | I/O | Stop Transaction | 1 |
| PAR[2] | I/O | Parity Signal Transactions | 1 |
| SERR# | O | System Error | 1 |
| PCIREQ#[2:0][2] | I | PCI Request | 3 |
| PCIGNT#[2:0][2] | O | PCI Grant | 3 |
| PCI_INT[3:0][2] | I | PCI Interrupt Request | 4 |
| | | | |
| **ISA INTERFACE** | | | |
| ISA_CLK | O | ISA Clock Output - Multiplexer Select Line For IPC | 1 |
| ISA_CLK2X | O | ISA Clock x2 Output - Multiplexer Select Line For IPC | 1 |
| OSC14M[2] | O | ISA bus synchronisation clock | 1 |

Note[1]; These pins are must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.

Note[2]; Denotes that the pin is $V_{5T}$ (see Section 4 )

Note [3]; see Table 2-5 for $V_{5T}$ signals

**Table 2-2. Definition of Signal Pins**

| Signal Name | Dir | Description | Qty |
|---|---|---|---|
| LA[23:17][2] | O | Unlatched Address | 7 |
| SA[19:0] | I/O | Latched Address | 20 |
| SD[15:0] | I/O | Data Bus | 16 |
| ALE[2] | O | Address Latch Enable | 1 |
| MEMR#[2], MEMW#[2] | I/O | Memory Read and Memory Write | 2 |
| SMEMR#, SMEMW# | O | System Memory Read and Memory Write | 2 |
| IOR#[2], IOW#[2] | I/O | I/O Read and Write | 2 |
| MCS16#[2], IOCS16#[2] | I | Memory/IO Chip Select16 | 2 |
| BHE#[2] | O | System Bus High Enable | 1 |
| ZWS# | I | Zero Wait State | 1 |
| REF# | O | Refresh Cycle. | 1 |
| MASTER#[2] | I | Add On Card Owns Bus | 1 |
| AEN[2] | O | Address Enable | 1 |
| IOCHCK#[2] | I | I/O Channel Check. | 1 |
| IOCHRDY[2] | I/O | I/O Channel Ready (ISA) - Busy/Ready (IDE) | 1 |
| ISAOE#[2] | O | ISA/IDE Selection | 1 |
| GPIOCS#[2] | I/O | General Purpose Chip Select | 1 |
| IRQ_MUX[3:0][2] | I | Time-Multiplexed Interrupt Request | 4 |
| DREQ_MUX[1:0][2] | I | Time-Multiplexed DMA Request | 2 |
| DACK_ENC[2:0][2] | O | Encoded DMA Acknowledge | 3 |
| TC | O | ISA Terminal Count | 1 |
| RTCAS# | O | Real Time Clock Address Strobe | 1 |
| RMRTCCS# | I/O | ROM/RTC Chip Select | 1 |
| KBCS#[2] | I/O | Keyboard Chip Select | 1 |
| RTCRW# | I/O | RTC Read/Write | 1 |
| RTCDS | I/O | RTC Data Strobe | 1 |
| | | | |
| **LOCAL BUS INTERFACE** | | | |
| PA[23:0] | O | Address Bus | 24 |
| PD[15:0] | I/O | Data Bus | 16 |
| PRD1#,PRD0# | O | Peripheral Read Control | 2 |
| PWR1#,PWR0# | O | Peripheral Write Control | 2 |
| PRDY# | I | Data Ready | 1 |
| FCS1#, FCS0# | O | Flash Chip Select | 2 |
| IOCS#[3:0] | O | I/O Chip Select | 4 |
| | | | |
| **IDE CONTROLLER** | | | |
| DA[2:0] | O | Address Bus | 3 |
| DD[15:0] | I/O | Data Bus | 16 |
| PCS3#,PCS1#,SCS3#,SCS1# | O | Primary & Secondary Chip Selects | 4 |
| DIORDY | O | Data I/O Ready | 1 |
| PIRQ, SIRQ | I | Primary & Secondary Interrupt Request | 2 |
| PDRQ[2], SDRQ | I | Primary & Secondary DMA Request | 2 |
| PDACK#[2], SDACK# | O | Primary & Secondary DMA Acknowledge | 2 |
| PDIOR#, SDIOR# | O | Primary & Secondary I/O Channel Read | 2 |
| Note[1]; These pins are must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply. | | | |
| Note[2]; Denotes that the pin is $V_{5T}$ (see Section 4 ) | | | |
| Note [3]; see Table 2-5 for $V_{5T}$ signals | | | |

### Table 2-2. Definition of Signal Pins

| Signal Name | Dir | Description | Qty |
|---|---|---|---|
| PDIOW#, SDIOW# | O | Primary & Secondary I/O Channel Write | 2 |
| | | | |
| **VGA CONTROLLER** | | | |
| RED, GREEN, BLUE | O | Analog Red, Green, Blue | 3 |
| VSYNC | O | Vertical Sync | 1 |
| HSYNC[2] | O | Horizontal Sync | 1 |
| VREF_DAC[1] | I | DAC Voltage reference | 1 |
| RSET | I | Resistor Set | 1 |
| COMP | I | Compensation | 1 |
| | | | |
| **VIDEO INPUT PORT** | | | |
| VCLK | I | 27-33MHz Video Input Port Clock | 1 |
| VIN[7:0] | I | CCIR 601 or 656 YUV Video Data Input | 8 |
| | | | |
| **ANALOG TV OUTPUT PORT** | | | |
| RED_TV, GREEN_TV, BLUE_TV | O | Analog RGB or S-VHS outputs | 3 |
| CVBS | O | Analog video composite output | 1 |
| IREF1_TV | I | Reference current of 9bit DAC for CVBS | 1 |
| VREF1_TV | I | Reference voltage of 9bit DAC for CVBS | 1 |
| IREF2_TV | I | Reference current of 8bit DAC for R,G,B | 1 |
| VREF2_TV | I | Reference voltage of 8bit DAC for R,G,B | 1 |
| VSSA_TV | I | Analog Vss for DAC | 1 |
| VDDA_TV[2] | I | Analog Vdd for DAC | 1 |
| VCS | I/O | Composite Synch or Horizontal line SYNC output | 1 |
| ODD_EVEN[2] | I/O | Frame Synchronisation | 1 |
| | | | |
| **MISCELLANEOUS** | | | |
| SPKRD | O | Speaker Device Output | 1 |
| SCL | I/O | I²C Interface - Clock / Can be used for VGA DDC[1] signal | 1 |
| SDA | I/O | I²C Interface - Data / Can be used for VGA DDC[0] signal | 1 |
| SCAN_ENABLE | I | Reserved (Test pin) | 1 |
| COL_SEL[2] | O | Colour Select | 1 |
| VDD_CORE | | | |
| TCLK | I | Test Clock | 1 |
| TDI | I | Test Data Input | 1 |
| TMS | I | Test Mode Set | 1 |
| TDO | O | Test Data output | 1 |

Note[1]; These pins are must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.
Note[2]; Denotes that the pin is $V_{5T}$ (see Section 4 )
Note [3]; see Table 2-5 for $V_{5T}$ signals

## 2.2 SIGNAL DESCRIPTIONS

### 2.2.1 BASIC CLOCKS AND RESETS

**SYSRSTI#** *System Reset/Power good.* This input is low when the reset switch is depressed. Otherwise, it reflects the power supply's power good signal. This input is asynchronous to all clocks, and acts as a negative active reset. The reset circuit initiates a hard reset on the rising edge of this signal.

**SYSRSTO#** *Reset Output to System.* This is the system reset signal and is used to reset the rest of the components (not on Host bus) in the system. The ISA bus reset is an externally inverted buffered version of this output and the PCI bus reset is an externally buffered version of this output.

**XTALI** *14.3MHz Crystal Input*
**XTALO** *14.3MHz Crystal Output.* These pins are connected to the 14.318 MHz crystal to provide the reference clock for the internal frequency synthesizer to generate all the other clocks.
A 14.318 MHz Series Cut Quartz Crystal should be connected between these two pins. Balance capacitors of 15 pF should also be added. In the event of an external oscillator providing the master clock signal to the iDragon SCX502 device, the LVTTL signal should be provided on XTALO.

**HCLK** *Host Clock.* This clock supplies the CPU and the host related blocks. This clock can e doubled inside the CPU and is intended to operate in the range of 25 to 100 MHz. This clock in generated internally from a PLL but can be driven directly from the external system.

**DEV_CLK** *24MHz Peripheral Clock.* This 24MHZ signal is provided as a convenience for the system integration of a Floppy Disk driver function in an external chip.

**DCLK** *135MHz Dot Clock.* This is the dot clock, which drives graphics display cycles. Its frequency can go from 8MHz (using internal PLL) up to 135 MHz, and it is required to have a worst case duty cycle of 60-40.
This signal is either driven by the internal pll (VGA) or an external 27MHz oscillator (when the composite video output is enabled). The direction can be controlled by a strap option or an internal register bit.

### 2.2.2 SDRAM CONTROLLER

**MCLKO** *Memory Clock Output.* This clock is driving the DIMMs on board and is generated from an internal PLL. The default value is 66MHz.

**MCLKI** *Memory Clock Input.* This clock is driving the SDRAM controller, the graphics engine and display controller. This input should be a buffered version of the MCLKO signal with the track lengths between the buffer and the pin matched with the track lengths between the buffer and the DIMMs.

**CS#[1:0]** *Chip Select* These signals are used to disable or enable device operation by masking o enabling all SDRAM inputs except MCLK, CKE, and DQM.

**CS#[2]/MA[11]** *Chip Select/ Bank Address* This pin is CS#[2] in the case when 16Mbit devices are used. For all other densities, it becomes MA[11].

**CS#[3]/MA[12]/BA[1]** *Chip Select/ Memory Address/ Bank Address* This pin is CS#[3] in the case when 16Mbit devices are used. For all other densities, it becomes MA[12] when 2 internal banks devices are used and BA[1] when 4 internal bank devices are used.

**MA[10:0]** *Memory Address.* Multiplexed row and column address lines.

**BA[0]** *Memory Bank Address.*

**MD[63:0]** *Memory Data.* This is the 64-bit memory data bus. MD[40-0] are read by the device strap option registers during rising edge of SYSRSTI#.

**RAS#[1:0]** *Row Address Strobe.* These signals enable row access and precharge. Row address is latched on rising edge of MCLK when RAS# is low.

**CAS#[1:0]** *Column Address Strobe.* These signals enable column access. Column address is latched on rising edge of MCLK when CAS# is low.

**MWE#** *Write Enable.* Write enable specifies whether the memory access is a read (MWE# = H) or a write (MWE# = L).

**DQM#[7:0]** *Data Mask.* Makes data output Hi-Z after the clock and masks the SDRAM outputs. Blocks SDRAM data input when DQM active.

### 2.2.3 PCI CONTROLLER

**PCI_CLKI** *33MHz PCI Input Clock.* This signal is the PCI bus clock input and should be driven from the PCI_CLKO pin.

**PCI_CLKO** *33MHz PCI Output Clock.* This is the master PCI bus clock output.

**AD[31:0]** *PCI Address/Data.* This is the 32-bit multiplexed address and data bus of the PCI. This bus is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions.

**CBE#[3:0]** *Bus Commands/Byte Enables.* These are the multiplexed command and byte enable signals of the PCI bus. During the address phase they define the command and during the data phase they carry the byte enable information. These pins are inputs when a PCI master other than the iDragon SCX502 owns the bus and outputs when the iDragon SCX502 owns the bus.

**FRAME#** *Cycle Frame.* This is the frame signal of the PCI bus. It is an input when a PCI master owns the bus and is an output when iDragon SCX502 owns the PCI bus.

**IRDY#** *Initiator Ready.* This is the initiator ready signal of the PCI bus. It is used as an output when the iDragon SCX502 initiates a bus cycle on the PCI bus. It is used as an input during the PCI cycles targeted to the iDragon SCX502 to determine when the current PCI master is ready to complete the current transaction.

**TRDY#** *Target Ready.* This is the target ready signal of the PCI bus. It is driven as an output when the iDragon SCX502 is the target of the current bus transaction. It is used as an input when iDragon SCX502 initiates a cycle on the PCI bus.

**LOCK#** *PCI Lock.* This is the lock signal of the PCI bus and is used to implement the exclusive bus operations when acting as a PCI target agent.

**DEVSEL#** *I/O Device Select.* This signal is used as an input when the iDragon SCX502 initiates a bus cycle on the PCI bus to determine if a PCI slave device has decoded itself to be the target of the current transaction. It is asserted as an output either when the iDragon SCX502 is the target of the current PCI transaction or when no other device asserts DEVSEL# prior to the subtractive decode phase of the current PCI transaction.

**STOP#** *Stop Transaction.* Stop is used to implement the disconnect, retry and abort protocol of the PCI bus. It is used as an input for the bus cycles initiated by the iDragon SCX502 and is used as an output when a PCI master cycle is targeted to the iDragon SCX502.

**PAR** *Parity Signal Transactions.* This is the parity signal of the PCI bus. This signal is used to guarantee even parity across AD[31:0], CBE#[3:0], and PAR. This signal is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions. (Its assertion is identical to that of the AD bus delayed by one PCI clock cycle)

**SERR#** *System Error.* This is the system error signal of the PCI bus. It may, if enabled, be asserted for one PCI clock cycle if target aborts a iDragon SCX502 initiated PCI transaction. Its assertion by either the iDragon SCX502 or by another PCI bus agent will trigger the assertion of NMI to the host CPU. This is an open drain output.

**PCIREQ#[2:0]** *PCI Request.* This pin are the three external PCI master request pins. They indicates to the PCI arbiter that the external agents desire use of the bus.

**PCIGNT#[2:0]** *PCI Grant.* These pins indicate that the PCI bus has been granted to the master requesting it on its PCIREQ#.

**PCI_INT[3:0]** *PCI Interrupt Request.* These are the PCI bus interrupt signals.

### 2.2.4 ISA INTERFACE

**ISA_CLK, ISA_CLKX2** *ISA Clock x1, x2.* These pins generate the Clock signal for the ISA bus and a Doubled Clock signal. They are also used as the multiplexor control lines for the Interrupt Controlle Interrupt input lines. ISA_CLK is generated from either PCICLK/4 or OSC14M/ 2.

**OSC14M** *ISA bus synchronisation clock Output.* This is the buffered 14.318 Mhz clock for the ISA bus.

**LA[23:17]** *Unlatched Address.* When the ISA bus is active, these pins are ISA Bus unlatched address for 16-bit devices. When ISA bus is accessed by any cycle initiated from PCI bus, these pins are in output mode. When an ISA bus master owns the bus, these pins are in input mode.

**SA[19:0]** *ISA Address Bus.* System address bus of ISA on 8-bit slot. These pins are used as an in

put when an ISA bus master owns the bus and are outputs at all other times.

**SD[15:0]** *I/O Data Bus.* These pins are the external databus to the ISA bus.

**ALE** *Address Latch Enable.* This is the address latch enable output of the ISA bus and is asserted by the iDragon SCX502 to indicate that LA23-17, SA19-0, AEN and SBHE# signals are valid. The ALE is driven high during refresh, DMA master or an ISA master cycles by the iDragon SCX502. ALE is driven low after reset.

**MEMR#** *Memory Read.* This is the memory read command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.
The MEMR# signal is active during refresh.

**MEMW#** *Memory Write.* This is the memory write command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.

**SMEMR#** *System Memory Read.* The iDragon SCX502 generates SMEMR# signal of the ISA bus only when the address is below one megabyte or the cycle is a refresh cycle.

**SMEMW#** *System Memory Write.* The iDragon SCX502 generates SMEMW# signal of the ISA bus only when the address is below one megabyte.

**IOR#** *I/O Read.* This is the IO read command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

**IOW#** *I/O Write.* This is the IO write command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

**MCS16#** *Memory Chip Select16.* This is the decode of LA23-17 address pins of the ISA address bus without any qualification of the command signal lines. MCS16# is always an input. The iDragon SCX502 ignores this signal during IO and refresh cycles.

**IOCS16#** *IO Chip Select16.* This signal is the decode of SA15-0 address pins of the ISA address bus without any qualification of the command signals. The iDragon SCX502 does not drive IOCS16# (similar to PC-AT design). An ISA master access to an internal register of the iDragon SCX502 is executed as an extended 8-bit IO cycle.

**BHE#** *System Bus High Enable.* This signal, when asserted, indicates that a data byte is being transferred on SD15-8 lines. It is used as an input when an ISA master owns the bus and is an output at all other times.

**ZWS#** *Zero Wait State.* This signal, when assert ed by addressed device, indicates that current cycle can be shortened.

**REF#** *Refresh Cycle.* This is the refresh command signal of the ISA bus. It is driven as an output when the iDragon SCX502 performs a refresh cycle on the ISA bus. It is used as an input when an ISA master owns the bus and is used to trigger a refresh cycle.
The iDragon SCX502 performs a pseudo hidden refresh. It requests the host bus for two host clocks to drive the refresh address and capture it in external buffers. The host bus is then relin quished while the refresh cycle continues on the ISA bus.

**MASTER#** *Add On Card Owns Bus.* This signal is active when an ISA device has been granted bus ownership.

**AEN** *Address Enable.* Address Enable is enabled when the DMA controller is the bus owner to indi cate that a DMA transfer will occur. The enabling of the signal indicates to IO devices to ignore the IOR#/IOW# signal during DMA transfers.

**IOCHCK#** *IO Channel Check.* IO Channel Check is enabled by any ISA device to signal an erro condition that can not be corrected. NMI signal be comes active upon seeing IOCHCK# active if the corresponding bit in Port B is enabled.

**IOCHRDY** *Channel Ready.* IOCHRDY is the IO channel ready signal of the ISA bus and is driven as an output in response to an ISA master cycle targeted to the host bus or an internal register of the iDragon SCX502. The iDragon SCX502 moni tors this signal as an input when performing an ISA cycle on behalf of the host CPU, DMA maste or refresh.
ISA masters which do not monitor IOCHRDY are not guaranteed to work with the iDragon SCX502 since the access to the system memory can be considerably delayed due UMA architecture.

**ISAOE#** *Bidirectional OE Control.* This signal con trols the $\overline{OE}$ signal of the external transceiver that connects the IDE DD bus and ISA SA bus.

**GPIOCS#** *I/O General Purpose Chip Select.* This output signal is used by the external latch on ISA bus to latch the data on the SD[7:0] bus. The latch can be use by PMU unit to control the external peripheral devices or any other desired function.

**IRQ_MUX[3:0]** *Multiplexed Interrupt Request.* These are the ISA bus interrupt signals. They have to be encoded before connection to the iDragon SCX502 using ISACLK and ISACLKX2 as the input selection strobes.
Note that IRQ8B, which by convention is connected to the RTC, is inverted before being sent to the interrupt controller, so that it may be connected directly to the $\overline{IRQ}$ pin of the RTC.

**DREQ_MUX[1:0]** *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the iDragon SCX502 using ISACLK and ISACLKX2 as the input selection strobes.

**DACK_ENC[2:0]** *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the iDragon SCX502 before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

**TC** *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the byte count expires.

**RTCAS#** *Real time clock address strobe.* This signal is asserted for any I/O write to port 70H.

**RMRTCCS#** *ROM/Real Time clock chip select.* This signal is asserted if a ROM access is decoded during a memory cycle. It should be combined with MEMR# or MEMW# signals to properly access the ROM. During a IO cycle, this signal is asserted if access to the Real Time Clock (RTC) is decoded. It should be combined with IOR or IOW# signals to properly access the real time clock.

**KBCS#** *Keyboard Chip Select.* This signal is asserted if a keyboard access is decoded during a I/O cycle.

**RTCRW#** *Real Time Clock R$\overline{W}$.* This pin is a multifunction pin. When ISAOE# is active, this signal is used as RTCRW#. This signal is asserted for any I/O write to port 71H.

**RTCDS#** *Real Time Clock D* . This pin is a multifunction pin. When ISAOE# is active, this signal is used as RTCDS. This signal is asserted for any I/O read to port 71H.

Note: RMRTCCS#, KBCS#, RTCRW# and RTCDS# signals must be ORed externally with ISAOE# and then connected to the external device. An LS244 or equivalent function can be used if OE# is connected to ISAOE# and the output is provided with a weak pull-up resistor as shown in Figure 2-2.

### 2.2.5 LOCAL BUS INTERFACE

**PA[23:0]** *Address Bus Output.*

**PD[15:0]** *Data Bus.* This is the 16-bit data bus. D[7:0] is the LSB and PD[15:8] is the MSB.

**PRD#[1:0]** *Read Control output.* PRD0# is used to read the LSB and PRD1# to read the MSB.

**PWR#[1:0]** *Write Control output.* PWR0# is used to write the LSB and PWR1# to write the MSB.

**PRDY#** *Data Ready input.* This signal is used to create wait states on the bus. When low, it completes the current cycle.

**FCS#[1:0]** *Flash Chip Select output.* These are the Programmable Chip Select signals for up to 2 banks of Flash memory.

**IOCS#[3:0]** *I/O Chip Select output.* These are the Programmable Chip Select signals for up to 4 external I/O devices.

### 2.2.6 IDE INTERFACE

**SCS1#, SCS3#** *Secondary Chip Select.* These signals are used as the active high secondary master & slave IDE chip select signals. These signals must be externally ANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

**DA[2:0]** *Address.* These signals are connected to DA[2:0] of IDE devices directly or through a buffer. If the toggling of signals are to be masked during ISA bus cycles, they can be externally ORed with ISAOE# before being connected to the IDE devices.

**DD[15:0]** *Databus.* When the IDE bus is active, they serve as IDE signals DD[11:0]. IDE devices are connected to SA[19:8] directly and ISA bus is connected to these pins through two LS245 transceivers as described in Figure 2-2.

**PCS1#, PCS3#** *Primary Chip Select.* These signals are used as the active high primary master & slave IDE chip select signals. These signals must be externally ANDed with the ISAOE# signal be-

fore driving the IDE devices to guarantee it is active only when ISA bus is idle.

**DIORDY** *Busy/Ready.* This pin serves as IDE signal DIORDY.

**PIRQ** *Primary Interrupt Request.*
**SIRQ** *Secondary Interrupt Request.*
Interrupt request from IDE channels.

**PDRQ** *Primary DMA Request.*
**SDRQ** *Secondary DMA Request.*
DMA request from IDE channels.

**PDACK#** *Primary DMA Acknowledge.*
**SDACK#** *Secondary DMA Acknowledge.*
DMA acknoledge to IDE channels.

**PDIOR#, PDIOW#** *Primary I/O Read & Write.*
**SDIOR#, SDIOW#** *Secondary I/O Read & Write.*
Primary & Secondary channel read & write.

### 2.2.7 VGA CONTROLLER

**RED, GREEN, BLUE** *RGB Video Outputs.* These are the 3 analog color outputs from the RAMDACs. These signals are sensitive to interference, therefore they need to be properly shielded.

**VSYNC** *Vertical Synchronisation Pulse.* This is the vertical synchronization signal from the VGA controller.

**HSYNC** *Horizontal Synchronisation Pulse.* This is the horizontal synchronization signal from the VGA controller.

**VREF_DAC** *DAC Voltage reference.* An external voltage reference is connected to this pin to bias the DAC.

**RSET** *Resistor Current Set.* This reference current input to the RAMDAC is used to set the full-scale output of the RAMDAC.

**COMP** *Compensation.* This is the RAMDAC compensation pin. Normally, an external capacitor (typically 10nF) is connected between this pin and $V_{DD}$ to damp oscillations.

### 2.2.8 VIDEO INPUT PORT

**VCLK** *Pixel Clock Input.*This signal is used to synchronise data being transfered from an external video device to either the frame buffer, or alternatively out the TV output in bypass mode. This pin can be sourced from iDragon if no external VCLK is detected, or can be input from an external video clock source.

**VIN[7:0]** *YUV Video Data Input CCIR 601 or 656.* Time multiplexed 4:2:2 luminance and chrominance data as defined in ITU-R Rec601-2 and Rec656 (except for TTL input levels). This bus typically carries a stream of Cb,Y,Cr,Y digital video at VCLK frequency, clocked on the rising edge (by default) of VCLK.

### 2.2.9 ANALOG TV OUTPUT PORT

**RED_TV / C_TV** *Analog video outputs synchronized with CVBS.* This output is current-driven and must be connected to analog ground over a load resistor ($R_{LOAD}$). Following the load resistor, a simple analog low pass filter is recommended. In S-VHS mode, this is the Chrominance Output.

**GREEN_TV / Y_TV** *Analog video outputs synchronized with CVBS.* This output is current-driven and must be connected to analog ground over a load resistor ($R_{LOAD}$). Following the load resistor, a simple analog low pass filter is recommended. In S-VHS mode, this is the Luminance Output.

**BLUE_TV / CVBS** *Analog video outputs synchronized with CVBS.* This output is current-driven and must be connected to analog ground over a load resistor ($R_{LOAD}$). Following the load resistor, a simple analog low pass filter is recommended. In S-VHS mode, this is a second composite output.

**CVBS** *Analog video composite output (luminance/chrominance).* CVBS is current-driven and must be connected to analog ground over a load resistor ($R_{LOAD}$). Following the load resistor, a simple analog low pass filter is recommended.

**IREF1_TV** *Ref. current* for CVBS 10-bit DAC.

**IREF2_TV** *Reference current* for RGB 9-bit DAC.

**VREF1_TV** *Ref. voltage* for CVBS 10-bit DAC.

**VREF2_TV** *Reference voltage* for RGB 9-bit DAC.

**VSSA_TV** *Analog* $V_{SS}$ for DACs.

**VDDA_TV** *Analog* $V_{DD}$ for DACs.

JTAG Signals

**VCS** *Line synchronisation Output.* This pin is an input in ODDEV+HSYNC or VSYNC + HSYNC or VSYNC slave modes and an output in all other modes (master/slave)

**ODD_EVE** *Frame Synchronisation Ourput.* This pin supports the Frame synchronisation signal. It is an input in slave modes, except when sync is

extracted from YCrCbdata, and an output in master mode and when sync is extracted from YCrCb data
The signal is synchronous to rising edge of DCLK. The default polarity for this pin is:
- odd (not-top) field : LOW level
- even (bottom) field : HIGH level

### 2.2.10 MISCELLANEOUS

**SPKRD** *Speaker Drive.* This the output to the speaker. It is an AND of the counter 2 output with bit 1 of Port 61, and drives an external speaker driver. This output should be connected to 7407 type high voltage driver.

**SCL, SDA** I²C Interface. These bidirectional pins are connected to CRTC register 3Fh to implement DDC capabilities. They conform to I $^2$C electrical specifications, they have open-collector output drivers which are internally connected to $V_{DD}$ through pull-up resistors.
They can be used for the DDC1 (SCL) and DDC0 (SDA) lines of the VGA interface.

**SCAN_ENABLE** *Reserved*. The pin is reserved for Test and Miscellaneous functions.

**COL_SEL** *Colour Select.* Can be use for Picture in Picture function

**VDD_CORE** *2.5V Power Supply.* These power pins are necessary to supply the core with 2.5V.

**TCLK** *Test clock*

**TDI** *Test data input*

**TMS** *Test mode input*

**TDO** *Test data output*

**Table 2-3. ISA / IDE dynamic multiplexing**

| ISA BUS (ISAOE# = 0) | IDE (ISAOE# = 1) |
|---|---|
| RMRTCCS# | DD[15] |
| KBCS# | DD[14] |
| RTCRW# | DD[13] |
| RTCDS | DD[12] |
| SA[19:8] | DD[11:0] |
| LA[23] | SCS3# |
| LA[22] | SCS1# |
| SA[21] | PCS3# |
| SA[20] | PCS1# |
| LA[19:17] | DA[2:0] |
| IOCHRDY | DIORDY |

**Table 2-4. ISA / Local Bus pin sharing**

| ISA / IPC | LOCAL BUS |
|---|---|
| SD[15:0] | PD[15:0] |
| DREQ_MUX[1:0] | PA[21:20] |
| SMEMR# | PA[19] |
| MEMW# | PA[18] |
| BHE# | PA[17] |
| AEN | PA[16] |
| ALE | PA[15] |
| MEMR# | PA[14] |
| IOR# | PA[13] |
| IOW# | PA[12] |
| REF# | PA[11] |
| IOCHCK# | PA[10] |
| GPIOCS# | PA[9] |
| ZWS# | PA[8] |
| SA[7:4] | PA[7:4] |
| TC, DACK_ENC[2:0] | PA[3:0] |
| SA[3] | PRDY |
| ISAOE#,SA[2:0] | IOCS#[3:0] |
| DEV_CLK, RTCAS# | FCS#[1:0] |
| IOCS16#, MASTER# | PRD#[1:0] |
| SMEMW#, MCS16# | PWR#[1:0] |
| ISACLK, ISA_CLK2X | |

**Figure 2-2. Typical ISA/IDE Demultiplexing**

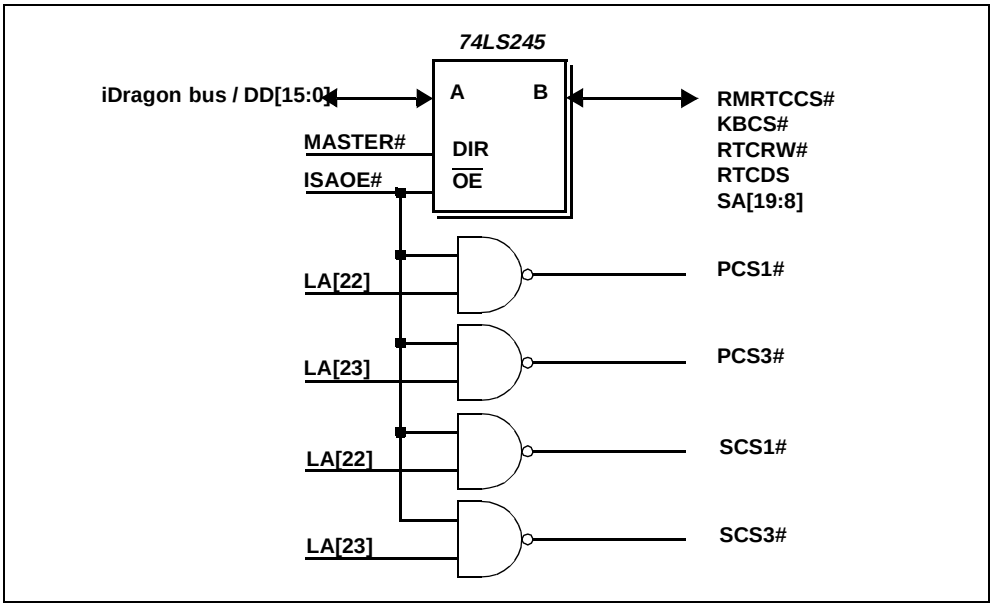


**Table 2-5. Pinout.**

| Pin # | Pin name |
|---|---|
| AF3 | SYSRSETI# |
| AE4 | SYSRSETO# |
| A3 | XTALI |
| C4 | XTALO |
| G23 | HCLK |
| H24 | DEV_CLK |
| AD11 | DCLK |
| AF15 | MCLKI |
| AB23 | MCLKO |
| AE16 | MA[0] |
| AD15 | MA[1] |
| AF16 | MA[2] |
| AE17 | MA[3] |
| AD16 | MA[4] |
| AF17 | MA[5] |
| AE18 | MA[6] |
| AD17 | MA[7] |
| AF18 | MA[8][3] |
| AE19 | MA[9][3] |
| AE20 | MA[10] |
| AC19 | BA[0] |
| AF22 | CS#[0] |
| AD21 | CS#[1] |
| AE24 | CS#[2]/MA[11] |
| AD23 | CS#[3]/MA[12]/BA[1] |
| AF23 | RAS#[0] |
| AD22 | RAS#[1] |
| AE21 | CAS#[0] |
| AC20 | CAS#[1] |
| AF20 | DQM#[0] |
| AD19 | DQM#[1] |
| AF21 | DQM#[2] |
| AD20 | DQM#[3] |
| AE22 | DQM#[4] |
| AE23 | DQM#[5] |
| AF19 | DQM#[6] |
| AD18 | DQM#[7] |
| AC22 | MWE# |
| R1 | MD[0][3] |
| T2 | MD[1][3] |
| R3 | MD[2] |
| T1 | MD[3] |
| R4 | MD[4] |
| U2 | MD[5] |
| T3 | MD[6] |
| U1 | MD[7] |
| U4 | MD[8] |
| V2 | MD[9] |
| U3 | MD[10] |
| V1 | MD[11] |
| W2 | MD[12] |
| V3 | MD[13] |
| Y2 | MD[14] |
| W4 | MD[15] |
| Y1 | MD[16] |
| W3 | MD[17] |
| AA2 | MD[18] |
| Y4 | MD[19] |
| AA1 | MD[20] |
| Y3 | MD[21] |
| AB2 | MD[22] |
| AB1 | MD[23] |
| AA3 | MD[24] |
| AB4 | MD[25] |
| AC1 | MD[26] |
| AB3 | MD[27] |
| AD2 | MD[28] |
| AC3 | MD[29] |
| AD1 | MD[30] |
| AF2 | MD[31] |
| AF24 | MD[32] |
| AE26 | MD[33] |
| AD25 | MD[34] |
| AD26 | MD[35] |
| AC25 | MD[36] |
| AC24 | MD[37] |
| AC26 | MD[38] |
| AB25 | MD[39] |
| AB24 | MD[40] |
| AB26 | MD[41] |
| AA25 | MD[42] |
| Y23 | MD[43] |
| AA24 | MD[44] |
| AA26 | MD[45] |
| Y25 | MD[46] |
| Y26 | MD[47] |
| Y24 | MD[48] |
| W25 | MD[49][3] |
| V23 | MD[50][3] |
| W26 | MD[51][3] |
| W24 | MD[52][3] |
| V25 | MD[53][3] |
| V26 | MD[54][3] |
| U25 | MD[55][3] |
| V24 | MD[56][3] |
| U26 | MD[57][3] |
| U23 | MD[58][3] |
| T25 | MD[59][3] |
| U24 | MD[60][3] |
| T26 | MD[61][3] |
| R25 | MD[62][3] |
| R26 | MD[63][3] |
| F24 | PCI_CLKI |
| D25 | PCI_CLKO |
| B20 | AD[0] |
| C20 | AD[1] |
| B19 | AD[2] |
| A19 | AD[3] |
| C19 | AD[4] |
| B18 | AD[5] |
| A18 | AD[6] |
| B17 | AD[7] |
| C18 | AD[8] |
| A17 | AD[9] |
| D17 | AD[10] |
| B16 | AD[11] |
| C17 | AD[12] |
| B15 | AD[13] |
| A15 | AD[14] |
| C16 | AD[15] |
| B14 | AD[16] |
| D15 | AD[17] |
| A14 | AD[18] |
| B13 | AD[19] |
| D13 | AD[20] |
| A13 | AD[21] |
| C14 | AD[22] |
| B12 | AD[23] |
| C13 | AD[24] |
| A12 | AD[25] |
| C12 | AD[26] |
| A11 | AD[27] |
| D12 | AD[28] |
| B10 | AD[29] |
| C11 | AD[30] |
| A10 | AD[31] |
| D10 | CBE[0] |
| C10 | CBE[1] |
| A9 | CBE[2] |
| B8 | CBE[3] |
| A8 | FRAME# |
| B7 | TRDY# |
| D8 | IRDY# |
| A7 | STOP# |
| C8 | DEVSEL# |
| B6 | PAR |

| Pin # | Pin name |
|---|---|
| D7 | SERR# |
| A6 | LOCK# |
| D20 | PCI_REQ#[0] |
| C21 | PCI_REQ#[1] |
| A21 | PCI_REQ#[2] |
| C22 | PCI_GNT#[0] |
| A22 | PCI_GNT#[1] |
| B21 | PCI_GNT#[2] |
| A5 | PCI_INT[0] |
| C6 | PCI_INT[1] |
| B4 | PCI_INT[2] |
| D5 | PCI_INT[3] |
| | |
| F2 | LA[17]/DA[0] |
| G4 | LA[18]/DA[1] |
| F3 | LA[19]/DA[2] |
| F1 | LA[20]/PCS1# |
| G2 | LA[21]/PCS3# |
| G1 | LA[22]/SCS1# |
| H2 | LA[23]/SCS3# |
| J4 | SA[0] |
| H1 | SA[1] |
| H3 | SA[2] |
| J2 | SA[3] |
| J1 | SA[4] |
| K2 | SA[5] |
| J3 | SA[6] |
| K1 | SA[7] |
| K4 | SA[8] |
| L2 | SA[9] |
| K3 | SA[10] |
| L1 | SA[11] |
| M2 | SA[12] |
| M1 | SA[13] |
| L3 | SA[14] |
| N2 | SA[15] |
| M4 | SA[16] |
| M3 | SA[17] |
| P2 | SA[18] |
| P4 | SA[19] |
| K25 | SD[0] |
| L24 | SD[1] |
| K26 | SD[2] |
| K23 | SD[3] |
| J25 | SD[4] |
| K24 | SD[5] |
| J26 | SD[6] |
| H25 | SD[7] |
| H26 | SD[8] |

| Pin # | Pin name |
|---|---|
| J24 | SD[9] |
| G25 | SD[10] |
| H23 | SD[11] |
| D24 | SD[12] |
| C26 | SD[13] |
| A25 | SD[14] |
| B24 | SD[15] |
| | |
| AD4 | ISA_CLK |
| AF4 | ISA_CLK2X |
| C9 | OSC14M |
| P25 | ALE |
| AE8 | ZWS# |
| R23 | BHE# |
| P26 | MEMR# |
| R24 | MEMW# |
| N25 | SMEMR# |
| N23 | SMEMW# |
| N26 | IOR# |
| P24 | IOW# |
| N24 | MCS16# |
| M26 | IOCS16# |
| M25 | MASTER# |
| L25 | REF# |
| M24 | AEN |
| L26 | IOCHCK# |
| T24 | IOCHRDY |
| M23 | ISAOE# |
| A4 | RTCAS# |
| P3 | RTCDS# |
| R2 | RTCRW# |
| P1 | RMRTCCS# |
| AE3 | GPIOCS# |
| | |
| G26 | PA[22][3] |
| A20 | PA[23][3] |
| B1 | PIRQ |
| C2 | SIRQ |
| C1 | PDRQ |
| D2 | SDRQ |
| D3 | PDACK# |
| D1 | SDACK# |
| E2 | PDIOR# |
| E4 | PDIOW# |
| E3 | SDIOR# |
| E1 | SDIOW# |
| | |
| E23 | IRQ_MUX[0] |
| D26 | IRQ_MUX[1] |

| Pin # | Pin name |
|---|---|
| E24 | IRQ_MUX[2] |
| C25 | IRQ_MUX[3] |
| A24 | DREQ_MUX[0] |
| B23 | DREQ_MUX[1] |
| C23 | DACK_ENC[0] |
| A23 | DACK_ENC[1] |
| B22 | DACK_ENC[2] |
| D22 | TC |
| N3 | KBCS# |
| | |
| AF9 | RED |
| AE9 | GREEN |
| AD8 | BLUE |
| AC5 | VSYNC |
| AE5 | HSYNC |
| AC10 | VREF_DAC |
| AE10 | RSET |
| AD7 | COMP |
| | |
| AE15 | VCLK |
| AD5 | VIN[0] |
| AF7 | VIN[1] |
| AF5 | VIN[2] |
| AE6 | VIN[3] |
| AC7 | VIN[4] |
| AD6 | VIN[5] |
| AF6 | VIN[6] |
| AE7 | VIN[7] |
| | |
| AD10 | RED_TV |
| AF11 | GREEN_TV |
| AE12 | BLUE_TV |
| AE13 | VCS |
| AC12 | ODD_EVEN |
| AF14 | CVBS |
| AE11 | IREF1_TV |
| AF12 | VREF1_TV |
| AE14 | IREF2_TV |
| AC14 | VREF2_TV |
| | |
| | |
| C5 | SPKRD |
| B5 | SCL |
| C7 | SDA |
| B3 | SCAN_ENABLE |
| C15 | COL_SEL |
| G3 | TCLK |
| N1 | TMS |
| W1 | TDI |

| Pin # | Pin name |
|---|---|
| AC2 | TDO |
| | |
| AD12 | VDDA_TV |
| AF8 | VDD_DAC1 |
| G24 | VDD_CPUCLK_PLL[1] |
| AD13 | VDD_DCLK_PLL[1] |
| F25 | VDD_DEVCLK_PLL[1] |
| AC17 | VDD_MCLKI_PLL[1] |
| AC15 | VDD_MCLKO_PLL[1] |
| F26 | VDD_HCLK_PLL[1] |
| E25 | VDD_SKEW_PLL[1] |
| | |
| D11 | VDD_CORE[1] |
| L23 | VDD_CORE[1] |
| T4 | VDD_CORE[1] |
| AC6 | VDD_CORE[1] |
| | |
| D6 | VDD |
| D16 | VDD |
| D21 | VDD |
| F4 | VDD |
| F23 | VDD |
| AC11 | VDD |
| AC16 | VDD |
| AC21 | VDD |
| AA4 | VDD |
| AA23 | VDD |
| T23 | VDD |
| L4 | VDD |
| | |
| AF13 | VSSA_TV |
| AC9 | VSS_DAC1 |
| A1:2 | VSS |
| A26 | VSS |
| B2 | VSS |
| B25:26 | VSS |
| C3 | VSS |
| C24 | VSS |
| D4 | VSS |
| D9 | VSS |
| D14 | VSS |
| D19 | VSS |
| D23 | VSS |
| H4 | VSS |
| J23 | VSS |
| L11:16 | VSS |
| M11:16 | VSS |
| N4 | VSS |
| N11:16 | VSS |

| Pin # | Pin name |
|---|---|
| P11:16 | VSS |
| P23 | VSS |
| R11:16 | VSS |
| T11:16 | VSS |
| V4 | VSS |
| W23 | VSS |
| AC4 | VSS |
| AC8 | VSS |
| AC13 | VSS |
| AC18 | VSS |
| AC23 | VSS |
| AD3 | VSS |
| AD14 | VSS |
| AD24 | VSS |
| AE1:2 | VSS |
| AE25 | VSS |
| AF1 | VSS |
| AF25 | VSS |
| AF26 | VSS |
| | |
| A16 | *Unconnected* |
| B9 | *Unconnected* |
| B11 | *Unconnected* |
| D18 | *Unconnected* |
| E26 | *Unconnected* |
| AD9 | *Unconnected* |
| AF10 | *Unconnected* |

Note[1]; These pins must be connected to the 2.5Vpower supply. They **must not** be connected to the 3.3V supply.

# 3 STRAP OPTIONS

This chapter defines the iDragon SCX502 Strap Options and their location. Some strap options are left programmable for future versions of silicon. .

| Memory Data Lines | Refer to | Designation | Location | Actual Settings[1] | Set to '0' | Set to '1' |
|---|---|---|---|---|---|---|
| **MD1** | - | Reserved | Index 4A, bit 1 | - | - | - |
| **MD2** | Host Clock | HCLK PLL Speed | Index 5F, bit 6 | User defined | see Section 3.1.4 bit 6 | |
| **MD3** | Host Clock | HCLK PLL Speed | Index 5F, bit 7 | User defined | see Section 3.1.4 bit 7 | |
| **MD4** | PCICLK | PCICLKO Division | Index 4A, bit 4 | User defined | see Section 3.1.3 bit 1 | |
| **MD5** | MCLK | MCLK/HCLK Synch | Index 4A, bit 5 | User defined | Unsynch | Synch |
| **MD6** | PCICLK | PCICLK frequency | Index 4A, bit 6 | User defined | see Section 3.1.1 bit 6 | |
| **MD7** | PCICLK | PCICLK frequency | Index 4A, bit 7 | User defined | see Section 3.1.1 bit 7 | |
| **MD8** | - | Reserved | - | - | - | - |
| **MD9** | - | Reserved | - | - | - | - |
| **MD10** | - | Reserved | Index 4B, bit 2 | Pull down | - | - |
| **MD11** | - | Reserved | Index 4B, bit 3 | Pull up | - | - |
| **MD12** | - | Reserved | Index 4B, bit 4 | Pull up | - | - |
| **MD13** | - | Reserved | Index 4B, bit 5 | Pull up | - | - |
| **MD14** | - | Reserved | Index 4B, bit 6 | Pull up | - | - |
| **MD15** | - | Reserved | Index 4B, bit 7 | - | - | - |
| **MD16** | - | Reserved | Index 4C,bit0 | Pull up | - | - |
| **MD17** | PCI Clock | PCI_CLKO Divisor | Index 4C,bit 1 | User defined | see Section 3.1.3 bit 1 | |
| **MD18** | Host Clock | HCLK Pad Direction | Index 4C,bit 2 | User defined | External | Internal |
| **MD19** | Memory Clock | MCLK Pad Direction | Index 4C,bit 3 | User defined | External | Internal |
| **MD20** | Dot Clock | DCLK Pad Direction | Index 4C, bit4 | User defined | External | Internal |
| **MD21** | - | *Reserved* | Index 5F, bit 0 | Pull up | - | - |
| **MD22** | - | Reserved | Index 5F, bit 1 | Pull up | - | - |
| **MD23** | - | Reserved | Index 5F,bit 2 | Pull up | - | - |
| **MD24** | HCLK | HCLK PLL Speed | Index 5F,bit 3 | User defined | see Section 3.1.4 bit 3 | |
| **MD25** | | | Index 5F,bit 4 | User defined | see Section 3.1.4 bit 4 | |
| **MD26** | | | Index 5F,bit 5 | User defined | see Section 3.1.4 bit 5 | |
| **MD27** | - | *Reserved* | - | - | - | - |
| **MD28** | - | *Reserved* | - | - | - | - |
| **MD29** | - | *Reserved* | - | - | - | - |
| **MD30** | - | *Reserved* | - | - | - | - |
| **MD31** | - | *Reserved* | - | - | | |
| **MD32** | - | *Reserved* | - | - | - | - |
| **MD33** | - | *Reserved* | - | - | - | - |
| **MD34** | - | *Reserved* | - | - | - | - |
| **MD35** | - | *Reserved* | - | - | - | - |
| **MD36** | - | *Reserved* | - | - | - | - |
| **MD37** | - | *Reserved* | - | - | - | - |
| **MD38** | - | *Reserved* | - | - | - | - |
| **MD39** | - | *Reserved* | - | - | - | - |
| **MD40** | CPU | CPU Mode | Hardware | User defined | DX1 | DX2 |

Note[1]; Where a strap is represented by a 'Pull up' or 'Pull down', these have to be adhered to. If it is represented as a '-' it can be left unconnected. Where 'User defined', the strap is set by the user.

| Memory Data Lines | Refer to | Designation | Location | Actual Settings[1] | Set to '0' | Set to '1' |
|---|---|---|---|---|---|---|
| MD41 | - | *Reserved* | Hardware | Pull down | - | - |
| MD42 | - | *Reserved* | Hardware | Pull up | - | - |
| MD43 | - | *Reserved* | Hardware | Pull down | - | - |
| MD44 | Section 3.1.7 | *ISA/Local Bus select* | Hardware | User defined | ISA | Local |
| MD45 | - | *Reserved* | Hardware | Pull down | - | - |
| MD46 | - | *Reserved* | Hardware | Pull uo | - | - |
| MD47 | - | *Reserved* | Hardware | Pull down | - | - |
| MD48 | - | *Reserved* | Hardware | Pull up | - | - |
| Note[1]; Where a strap is represented by a 'Pull up' or 'Pull down', these have to be adhered to. If it is represented as a '-' it can be left unconnected. Where 'User defined', the strap is set by the user. | | | | | | |

### 3.1 Power on strap registers description

#### 3.1.1 Strap register 0 Configuration Index 4A (Strap0)

Bits 7-6 This bit reflcts the **value sampled on MD[7:6] pins** and controlles the PCICLK Programming.The PLL setup will vary depending on the PCICLK frequency;

| MD[7] | MD[6] | Description |
|---|---|---|
| 0 | 0 | PCICLK frequency between 16 & 32 MHz |
| 0 | 1 | PCICLK frequency between 32 & 64 MHz |
| 1 | 0 | PCICLK frequency greater than 64 MHz |
| 1 | 1 | Reserved |

Bit 5 This bit reflects the **value sampled on MD[5] pin** and controls the MCLK/HCLK Synchronization. When MCLK and HCLK frequency are the same, this bit when 1 unifies HCLK and MCLK and it will improve system performances.

Bit 4 This bit reflects the **value sampled on MD[4] pin** and controls the PCICLKO division. It works with MD[17]. refer to 4.17.3 bit 1 for a detailed description.

Bits 3-2 These bits are the same as Index 5F bit 7:6.

Bits 1-0 *Reserved.*

#### 3.1.2 Strap register 1 Configuration Index 4Bh (Strap1)

Bits 7-0 *Reserved*

#### 3.1.3 Strap register 2 Configuration Index 4Ch (Strap2)

Bits 7-5 *Reserved*

Bit 4 This bit reflects the **value sampled on MD[20] pin** and controls the Dot clock (DCLK) source as follows:

0: External. DCLK pin is an input.
1: Internal. DCLK pin is an output and is connected to the internal frequen cy synthesizer output.

Note this bit is writeable as well as readable.

Bit 3 This bit reflects the **value sampled on MD[19] pin** and controls the Memory clock output (MCLKO) source as follows:

0: External. MCLKO pin is tristated.
1: Internal. MCLKO pin is an output and is connected to the internal fre quency synthesizer output.

Bit 2 This bit reflects the **value sampled on MD[18] pin** and controls the Host/CPU clock source as follows:

0: External. HCLK pin is an input.
1: Internal. HCLK pin is an output and is connected to the internal frequen cy synthesizer output.

Bit 1 This bit reflects the value sampled on MD[17] pin and controls the PCI clock output as follows:

| MD[4] | MD[17] | Description |
|---|---|---|
| 0 | 0 | Reserved |
| 0 | 1 | PCI clock output = HCLK / 4 |

| MD[4] | MD[17] | Description |
|---|---|---|
| 1 | 0 | PCI clock output = HCLK / 3 |
| 1 | 1 | PCI clock output = HCLK / 2 |

Bit 0 *Reserved*

This register defaults to the values sampled on MD[23] & MD[20:16] pins after reset.

### 3.1.4 Strap register 0 Configuration Index 5Fh (HCLK_Strap)

Bits 7-3 These pins reflect the **value sampled on MD[3:2] and MD[26:24] pins** respectively and control the Host clock frequency synthesizer as follows:

| MD[3] | MD[2] | MD[26] | MD[25] | MD[24] | HCLK Speed |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 25 MHz |
| 0 | 0 | 0 | 0 | 1 | 50 MHz |
| 0 | 0 | 0 | 1 | 0 | 60 MHz |
| 0 | 0 | 0 | 1 | 1 | 66 MHz |
| 0 | 1 | 0 | 0 | 1 | 75 MHz |
| 1 | 0 | 0 | 1 | 1 | 90 MHz |
| 1 | 0 | 0 | 1 | 1 | 100 MHz |
| 1 | 1 | 1 | 1 | 1 | 133 MHz |

Bit 2-0 *Reserved*

### 3.1.5 HCLKI Programming (HCLK_Prog)

The HCLKI clock signal is selected and programmed through strap values on MD[46:45]. MD[46:45]

| MD[46] | MD[45] | HCLKI Source |
|---|---|---|
| 0 | 0 | HCLKI PLL enabled & HCLKI frequency between 16 & 32 MHz |
| 0 | 1 | HCLKI PLL enabled & HCLKI frequency between 32 & 64 MHz |
| 1 | 0 | HCLKI PLL enabled & HCLKI frequency greater than 64 MHz |
| 1 | 1 | *Reserved* |

### 3.1.6 486 Clock Programming (486_Prog)

The bit MD[40] is used to set the clock multiplication factor of the 486 core. With the MD[40] pin pulled low the 486 will run in DX (x1) mode, while with the MD[40] pin pulled high the 486 will run in DX2 (x2) mode. The default value of the resistor on this strap input should be a resister to gnd (DX mode).

MD[43:41] are used to set the clock tic input value for the 486 core DLL.

The recommended value for these three bits is 010.

### 3.1.7 MD44 ISA/Local Bus selection

This pin is pulled down to select ISA Bus operation, pulled up to select Local Bus operation. Note that the Local Bus is totally disabled when in ISA mode, and vive versa.

# 4 ELECTRICAL SPECIFICATIONS

## 4.1 Introduction

The electrical specifications in this chapter are valid for the iDragon SCX502.

## 4.2 Electrical Connections

### 4.2.1 Power/Ground Connections/Decoupling

Due to the high frequency of operation of the iDragon SCX502, it is necessary to install and test this device using standard high frequency techniques. The high clock frequencies used in the iDragon SCX502 and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the VSS and VDD pins.

### 4.2.2 Unused Input Pins

All inputs not used by the designer and not listed in the table of pin connections in Chapter 3 should be connected either to VDD or to VSS. Connect active-high inputs to VDD through a 20 k W (±10%) pull-down resistor and active-low inputs to VSS and connect active-low inputs to VCC through a 20 kW (±10%) pull-up resistor to prevent spurious operation.

### 4.2.3 Reserved Designated Pins

Pins designated reserved should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

## 4.3 Absolute Maximum Ratings

The following table lists the absolute maximum ratings for the iDragon SCX502 device. Stresses beyond those listed under Table 4-1 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those specified in section "Operating Conditions".

Exposure to conditions beyond Table 4-1 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings (Table 4-1) may also result in reduced useful life and reliability.

**Table 4-1. Absolute Maximum Ratings**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $V_{DDx}$ | DC Supply Voltage | -0.3 | 4.0 | V |
| $V_{CORE}$ | DC Supply Voltage for Core | | 2.75 | V |
| $V_I$, $V_O$ | Digital Input and Output Voltage | -0.3 | VDD + 0.5 | V |
| $V_{5T}$ | 5Volt Tolerance | | 5.5 | V |
| $V_{ESD}$ | ESD Capacity (Human body mode) | - | 2000 | V |
| $T_{STG}$ | Storage Temperature | -40 | +150 | °C |
| $T_{OPER}$ | Operating Temperature (Tcase) (Note 1) | -40 | +115° | °C |
| $P_{TOT}$ | Total Power Dissipation (package) | | 5 | W |

Note 1 : -40°C limit of $T_{CASE}$ (extended temperature range) is given a s a preliminary specification and so as all the -40°C related data.

### 4.4 DC Characteristics

**Table 4-2. DC Characteristics**

Recommended Operating conditions : VDD = 3.3V±0.3V, Vcore = 2.5V ±0.25V, Tcase = 0 to 85°C (Commercial Range) or -40 to 100°C (Industrial Range) unless otherwise specified

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating Voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{CORE}$ | Operating Voltage | | 2.25 | 2.50 | 2.75 | V |
| $V_{DD5}$ | 5V operating voltage | Note 3 | 4.5 | 5 | 5.5 | V |
| $P_{DD}$ | Supply Power | $V_{DD}$= 3.3V,$V_{CORE}$=2.5V$H_{CLK}$= 133MHz | | 2.5 | | W |
| $H_{CLK}$ | Internal Clock | (Note 1) | | | 133 | MHz |
| $V_{REF}$ | DAC Voltage Reference | | 1.215 | 1.235 | 1.255 | V |
| $V_{OL}$ | Output Low Voltage | $I_{Load}$ =1.5 to 8mA depending of the pin | | | 0.5 | V |
| $V_{OH}$ | Output High Voltage | $I_{Load}$ =-0.5 to -8mA depending of the pin | 2.4 | | | V |
| $V_{IL}$ | Input Low Voltage | Except XTALI | -0.3 | | 0.8 | V |
| | | XTALI | -0.3 | | 0.9 | V |
| $V_{IH}$ | Input High Voltage | Except XTALI | 2 | | $V_{DD}$+0.5 | V |
| | | XTALI | 2.35 | | $V_{DD}$+0.5 | V |
| $I_{LK}$ | Input Leakage Current | Input, I/O | -1 | | 2 | µA |
| $C_{IN}$ | Input Capacitance | (Note 2) | | | | pF |
| $C_{OUT}$ | Output Capacitance | (Note 2) | | | | pF |
| $C_{CLK}$ | Clock Capacitance | (Note 2) | | | | pF |

**Notes:**

1. MHz ratings refer to CPU clock frequency.

2. Not 100% tested.

3. Detail of pins refer to Table 2-2

### 4.5 AC Characteristics

Table 4-4 through Table 4-9 list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 and Figure 4-2. The rising clock edge reference level VREF , and other reference levels are shown in Table 4-3 below for the iDragoniDragon SCX502. Input or output signals must cross these levels during testing.

Figure 4-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for cor rect operation.

**Table 4-3. Drive Level and Measurement Points for Switching Characteristics**

| Symbol | Value | Units |
|---|---|---|
| $V_{REF}$ | 1.5 | V |
| $V_{IHD}$ | 3.0 | V |
| $V_{ILD}$ | 0.0 | V |

Note: Refer to Figure 4-1.

**Figure 4-1. Drive Level and Measurement Points for Switching Characteristics**

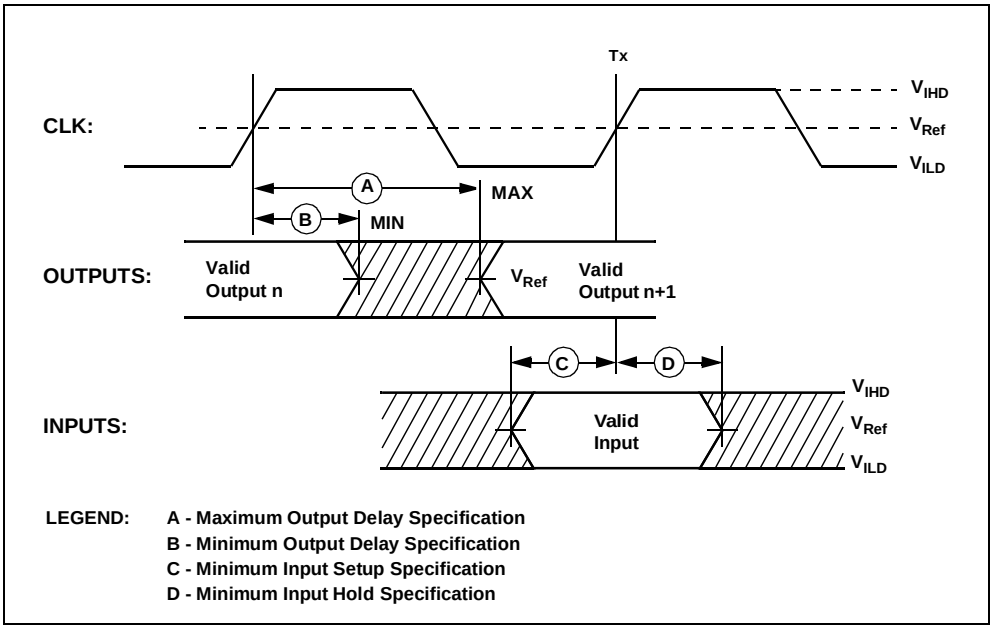
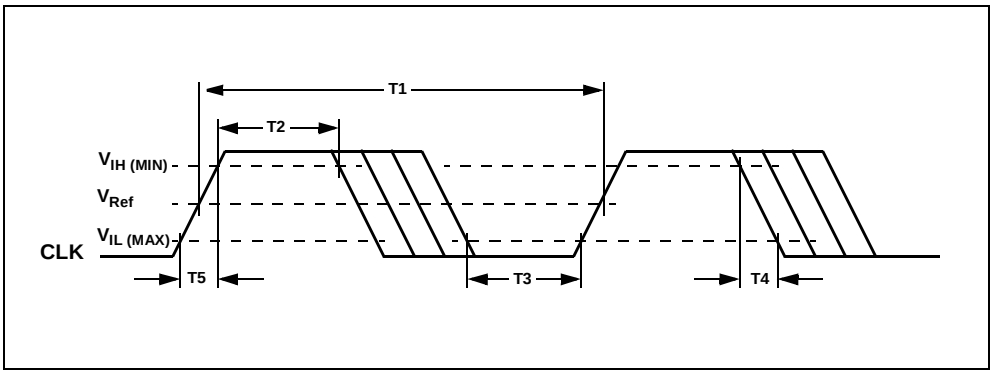
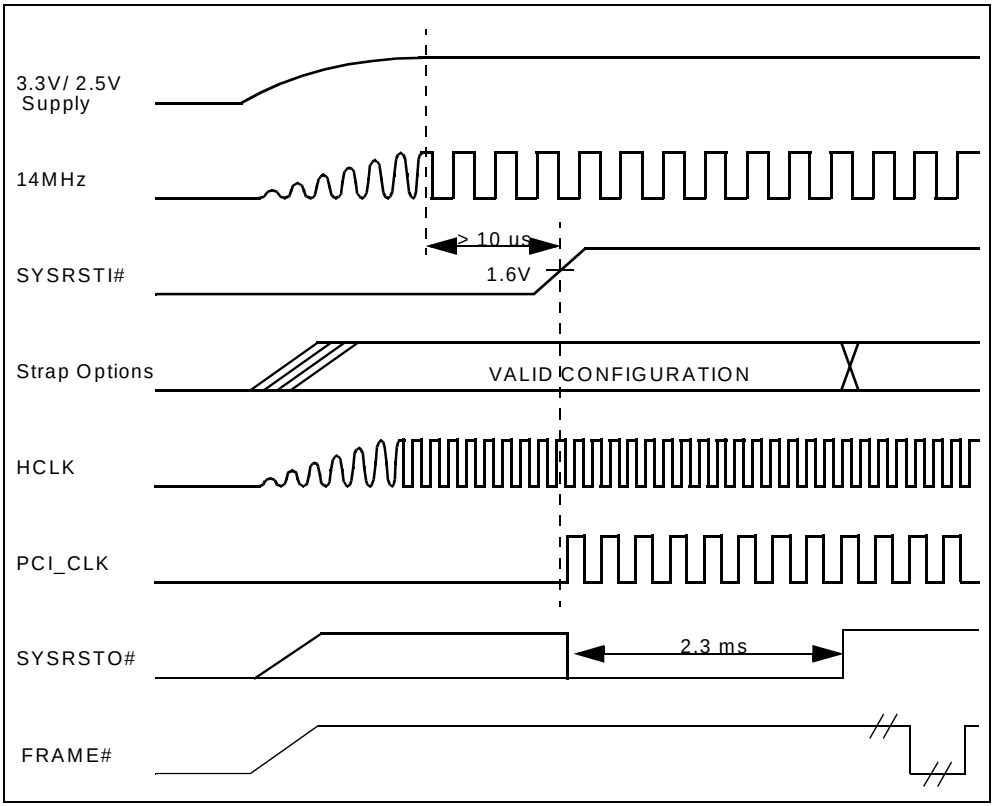



**Figure 4-2. CLK Timing Measurement Points**



### 4.5.1 Power on sequence




SYSRSTI# has no constraint on its rising time but needs to be set to high at least 10μs after power supply is stable.

Strap Options are continuously sampled during SYSRSTI# low and should be stable. Once SYSRSTI# is high, they MUST NOT CHANGE until SYSRSTO# is high.

**Table 4-4. PCI Bus AC Timing**

| Name | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| t1 | PCI_CLKI to AD[31:0] valid | 2 | 11 | ns |
| t2 | PCI_CLKI to FRAME# valid | 2 | 11 | ns |
| t3 | PCI_CLKI to CBE#[3:0] valid | 2 | 12 | ns |
| t4 | PCI_CLKI to PAR valid | 2 | 11 | ns |
| t5 | PCI_CLKI to TRDY# valid | 2 | 11 | ns |
| T6 | PCI_CLKI to IRDY# valid | 2 | 11 | ns |
| T7 | PCI_CLKI to STOP# valid | 2 | 11 | ns |
| T8 | PCI_CLKI to DEVSEL# valid | 2 | 11 | ns |
| T9 | PCI_CLKI to PCI_GNT# valid | 2 | 14 | ns |
| t10 | AD[31:0] bus setup to PCI_CLKI | 7 | | ns |
| t11 | AD[31:0] bus hold from PCI_CLKI | 0 | | ns |
| t12 | PCI_REQ#[2:0] setup to PCI_CLKI | 10 | | ns |
| t13 | PCI_REQ#[2:0] hold from PCI_CLKI | 1 | | ns |
| t14 | CBE#[3:0] setup to PCI_CLKI | 0 | | ns |
| t15 | CBE#[3:0] hold to PCI_CLKI | 5 | | ns |
| t16 | IRDY# setup to PCI_CLKI | 7 | | ns |
| t17 | IRDY# hold to PCI_CLKI | 0 | | ns |
| t18 | FRAME# setup to PCI_CLKI | 7 | | ns |
| t19 | FRAME# hold from PCI_CLKI | 0 | | ns |

**Table 4-5. SDRAM Bus AC Timing**

| Name | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| t22 | MCLKI to RAS#[1:0] Output Valid | 1.5 | 6.2 | ns |
| t23 | MCLKI to CAS#[1:0] Output Valid | 1.5 | 6.2 | ns |
| t24 | MCLKI to CS#[3:0] Output Valid | 1.5 | 7.6 | ns |
| t25 | MCLKI to DQM#[7:0] Output Valid | 1.5 | 8.1 | ns |
| t26 | MCLKI to MA[11:0] Output Valid | 1.5 | 6.2 | ns |
| t27 | MCLKI to MWE# Output Valid | 1.5 | 6.2 | ns |

Note, the SDRAM parameters are to be defined

**Table 4-6. IDE Bus AC Timing**

| Name | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| t28 | PCI_CLKI to SA[19:8] Active | 0 | 42 | ns |
| t29 | PCI_CLKI to RMRTCCS# Active | 0 | 42 | ns |
| t30 | PCI_CLKI to KBCS# Active | 0 | 42 | ns |
| t31 | PCI_CLKI to RTCRW# Active | 0 | 42 | ns |
| t32 | PCI_CLKI to RTCDS Active | 0 | 42 | ns |
| t33 | SA[19:8] Input Setup to SIOR# Rising | -10 | 10 | ns |
| t34 | SA[19:8] Input Hold to SIOR# Rising | -10 | 10 | ns |
| t35 | RMRTCCS# Input Setup to SIOR# Rising | -10 | 10 | ns |
| t36 | RMRTCCS# Input Hold to SIOR# Rising | -10 | 10 | ns |
| t37 | KBCS# Input Setup to SIOR# Rising | -10 | 10 | ns |
| t38 | KBCS# Input Hold to SIOR# Rising | -10 | 10 | ns |

### Table 4-6. IDE Bus AC Timing

| | | | | |
|---|---|---|---|---|
| t39 | RTCRW# Input Setup to SIOR# Rising | -10 | 10 | ns |
| t40 | RTCRW# Input Hold to SIOR# Rising | -10 | 10 | ns |
| t41 | RTCDS Input Setup to SIOR# Rising | -10 | 10 | ns |
| t42 | RTCDS Input Hold to SIOR# Rising | -10 | 10 | ns |
| t43 | PCI_CLKI to LA[23:17] Active | 0 | 28 | ns |
| t44 | PCI_CLKI to PDACK# Active | 0 | 32 | ns |
| t45 | PCI_CLKI to SDACK Active | 0 | 32 | ns |
| t46 | PCI_CLKI to PIOR# Active | 0 | 28 | ns |
| t47 | PCI_CLKI to PIOW# Active | 0 | 28 | ns |
| t48 | PCI_CLKI to SIOR# Active | 0 | 28 | ns |
| t49 | PCI_CLKI to SIOW# Active | 0 | 28 | ns |

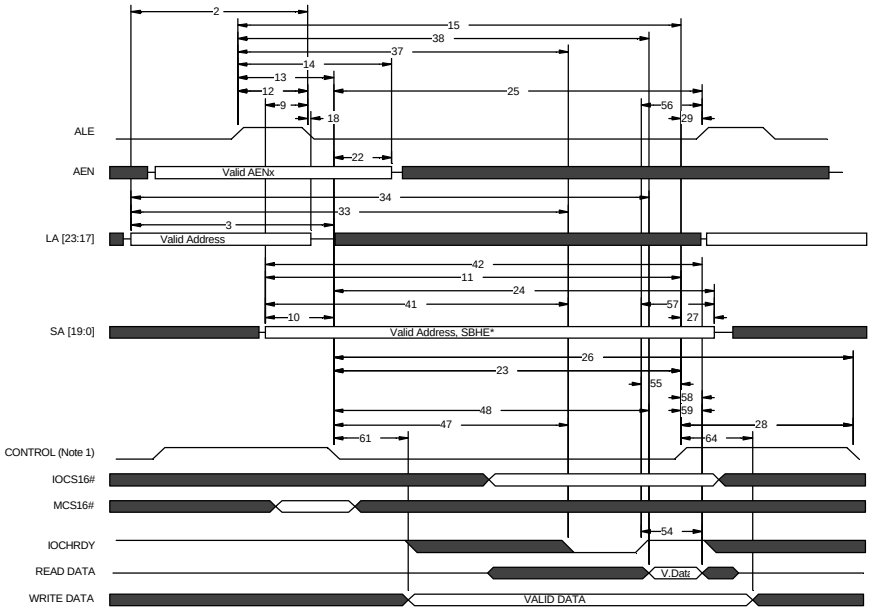
### Table 4-7. Video Input/TV Output AC Timing

| Name | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| t50 | DCLK to TV_YUV[7:0] bus valid | | 18 | ns |
| t51 | VIDEO_D[7:0] setup to VCLK | 5 | | ns |
| t52 | VIDEO_D[7:0] hold from VCLK | 3 | | ns |
| t53 | VCLK to VTV_BT# valid | | 21 | ns |
| t54 | VCLK to VTV_HSYNC valid | | 21 | ns |
| t55 | VTV_BT# setup to VCLK | 10 | | ns |
| t56 | VTV_BT# hold from VCLK | 5 | | ns |
| t57 | VTV_HSYNC setup to VCLK | 10 | | ns |
| t58 | VTV_HSYNC hold from VCLK | 5 | | ns |

### Table 4-8. Graphics Adapter (VGA) AC Timing

| Name | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| t59 | DCLK to VSYNC valid | | 45 | ns |
| t60 | DCLK to HSYNC valid | | 45 | ns |

**Figure 4-3. ISA Cycle (ref table Table 4-9)**




Note 1; Stands for SMEMR#, SMEMW#, MEMR#, MEMW#, IOR# & IOW#.

Note; The clock has not been represented as it cannot be accuratly represented depending on the ISA Slave mode.

**Table 4-9. ISA Bus AC Timing**

| Name | Parameter | Min | Max | Units |
|---|---|---|---|---|
| 2[4] | LA[23:17] valid before ALE# negated | 5T | | Cycles |
| **3[4]** | **LA[23:17] valid before MEMR#, MEMW# asserted** | | | |
| 3a[4] | Memory access to 16 bit ISA Slave | 5T | | Cycles |
| 3b[4] | Memory access to 8 bit ISA Slave | 5T | | Cycles |
| 9[4] | SA[19:0] & SBHE valid before ALE# negated | 1T | | Cycles |
| **10[4]** | **SA[19:0] & SBHE valid before MEMR#, MEMW# asserted** | | | |
| 10a[4] | Memory access to 16 bit ISA Slave | 2T | | Cycles |
| 10b[4] | Memory access to 8 bit ISA Slave | 2T | | Cycles |
| **10[4]** | **SA[19:0] & SHBE valid before SMEMR#, SMEMW# asserted** | | | |
| 10c[4] | Memory access to 16 bit ISA Slave | 2T | | Cycle |
| 10d[4] | Memory access to 8 bit ISA Slave | 2T | | Cycle |
| 10e[4] | SA[19:0] & SBHE valid before IOR#, IOW# asserted | 2T | | Cycles |
| **11[4]** | **XTALO to IOW# valid** | | | |
| 11a[4] | Memory access to 16 bit ISA Slave - 2BCLK | 2T | | Cycles |
| 11b[4] | Memory access to 16 bit ISA Slave - Standard 3BCLK | 2T | | Cycles |

Note; The signal numbering refers to Table 4-3

**Note 4; These timings are extracted from simulations and are not garanteed by testing**

### Table 4-9. ISA Bus AC Timing

| Name | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| | 11c[4] | Memory access to 16 bit ISA Slave - 4BCLK | 2T | | Cycles |
| | 11d[4] | Memory access to 8 bit ISA Slave - 2BCLK | 2T | | Cycles |
| 11e[4] | | Memory access to 8 bit ISA Slave - Standard 3BCLK | 2T | | Cycles |
| 12[4] | ALE# asserted before ALE# negated | | 1T | | Cycles |
| **13[4]** | **ALE# asserted before MEMR#, MEMW# asserted** | | | | |
| | 13a[4] | Memory Access to 16 bit ISA Slave | 2T | | Cycles |
| | 13b[4] | Memory Access to 8 bit ISA Slave | 2T | | Cycles |
| **13[4]** | **ALE# asserted before SMEMR#, SMEMW# asserted** | | | | |
| | 13c[4] | Memory Access to 16 bit ISA Slave | 2T | | Cycles |
| | 13d[4] | Memory Access to 8 bit ISA Slave | 2T | | Cycles |
| 13e[4] | ALE# asserted before IOR#, IOW# asserted | | 2T | | Cycles |
| **14[4]** | **ALE# asserted before AL[23:17]** | | | | |
| | 14a[4] | Non compressed | 15T | | Cycles |
| | 14b[4] | Compressed | 15T | | Cycles |
| **15[4]** | **ALE# asserted before MEMR#, MEMW#, SMEMR#, SMEMW# negated** | | | | |
| | 15a[4] | Memory Access to 16 bit ISA Slave- 4 BCLK | 11T | | Cycles |
| | 15e[4] | Memory Access to 8 bit ISA Slave- Standard Cycle | 11T | | Cycles |
| 18a[4] | ALE# negated before LA[23:17] invalid (non compressed) | | 14T | | Cycles |
| 18a[4] | ALE# negated before LA[23:17] invalid (compressed) | | 14T | | Cycles |
| **22[4]** | **MEMR#, MEMW# asserted before LA[23:17]** | | | | |
| | 22a[4] | Memory access to 16 bit ISA Slave. | 13T | | Cycles |
| | 22b[4] | Memory access to 8 bit ISA Slave. | 13T | | Cycles |
| **23[4]** | **MEMR#, MEMW# asserted before MEMR#, MEMW# negated** | | | | |
| | 23b[4] | Memory access to 16 bit ISA Slave Standard cycle | 9T | | Cycles |
| | 23e[4] | Memory access to 8 bit ISA Slave Standard cycle | 9T | | Cycles |
| **23[4]** | **SMEMR#, SMEMW# asserted before SMEMR#, SMEMW# negated** | | | | |
| | 23h[4] | Memory access to 16 bit ISA Slave Standard cycle | 9T | | Cycles |
| | 23l[4] | Memory access to 16 bit ISA Slave Standard cycle | 9T | | Cycles |
| **23[4]** | **IOR#, IOW# asserted before IOR#, IOW# negated** | | | | |
| | 23o[4] | Memory access to 16 bit ISA Slave Standard cycle | 9T | | Cycles |
| | 23r[4] | Memory access to 8 bit ISA Slave Standard cycle | 9T | | Cycles |
| **24[4]** | **MEMR#, MEMW# asserted before SA[19:0]** | | | | |
| | 24b[4] | Memory access to 16 bit ISA Slave Standard cycle | 10T | | Cycles |
| | 24d[4] | Memory access to 8 bit ISA Slave - 3BLCK | 10T | | Cycles |
| | 24e[4] | Memory access to 8 bit ISA Slave Standard cycle | 10T | | Cycles |
| | 24f[4] | Memory access to 8 bit ISA Slave - 7BCLK | 10T | | Cycles |
| **24[4]** | **SMEMR#, SMEMW# asserted before SA[19:0]** | | | | |
| | 24h | Memory access to 16 bit ISA Slave Standard cycle | 10T | | Cycles |
| | 24i[4] | Memory access to 16 bit ISA Slave - 4BCLK | 10T | | Cycles |
| | 24k[4] | Memory access to 8 bit ISA Slave - 3BCLK | 10T | | Cycles |
| | 24l[4] | Memory access to 8 bit ISA Slave Standard cycle | 10T | | Cycles |
| **24[4]** | **IOR#, IOW# asserted before SA[19:0]** | | | | |
| | 24o[4] | I/O access to 16 bit ISA Slave Standard cycle | 19T | | Cycles |
| | 24r[4] | I/O access to 16 bit ISA Slave Standard cycle | 19T | | Cycles |
| **25[4]** | **MEMR#, MEMW# asserted before next ALE# asserted** | | | | |
| Note; The signal numbering refers to Table 4-3 | | | | | |
| **Note 4; These timings are extracted from simulations and are not garanteed by testing** | | | | | |

**Table 4-9. ISA Bus AC Timing**

| Name | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| | 25b[4] | Memory access to 16 bit ISA Slave Standard cycle | 10T | | Cycles |
| | 25d[4] | Memory access to 8 bit ISA Slave Standard cycle | 10T | | Cycles |
| **25[4]** | **SMEMR#, SMEMW# asserted before next ALE# aserted** | | | | |
| | 25e[4] | Memory access to 16 bit ISA Slave - 2BCLK | 10T | | Cycles |
| | 25f[4] | Memory access to 16 bit ISA Slave Standard cycle | 10T | | Cycles |
| | 25h[4] | Memory access to 8 bit ISA Slave Standard cycle | 10T | | Cycles |
| **25[4]** | **IOR#, IOW# asserted before next ALE# asserted** | | | | |
| | 25i[4] | I/O access to 16 bit ISA Slave Standard cycle | 10T | | Cycles |
| | 25k[4] | I/O access to 16 bit ISA Slave Standard cycle | 10T | | Cycles |
| **26[4]** | **MEMR#, MEMW# asserted before next MEMR#, MEMW# asserted** | | | | |
| | 26b[4] | Memory access to 16 bit ISA Slave Standard cycle | 12T | | Cycles |
| | 26d[4] | Memory access to 8 bit ISA Slave Standard cycle | 12T | | Cycles |
| **26[4]** | **SMEMR#, SMEMW# asserted before next SMEMR#, SMEMW# asserted** | | | | |
| | 26f[4] | Memory access to 16 bit ISA Slave Standard cycle | 12T | | Cycles |
| | 26h[4] | Memory access to 8 bit ISA Slave Standard cycle | 12T | | Cycles |
| **26[4]** | **IOR#, IOW# asserted before next IOR#, IOW# asserted** | | | | |
| | 26i[4] | I/O access to 16 bit ISA Slave Standard cycle | 12T | | Cycles |
| | 26k[4] | I/O access to 8 bit ISA Slave Standard cycle | 12T | | Cycles |
| **28[4]** | **Any command negated to MEMR#, SMEMR#, MEMR#, SMEMW# asserted** | | | | |
| | 28a[4] | Memory access to 16 bit ISA Slave | 3T | | Cycles |
| | 28b[4] | Memory access to 8 bit ISA Slave | 3T | | Cycles |
| **28[4]** | **Any command negated to IOR#, IOW# asserted** | | | | |
| | 28c[4] | I/O access to ISA Slave | 3T | | Cycles |
| 29a[4] | MEMR#, MEMW# negated before next ALE# asserted | | 1T | | Cycles |
| 29b[4] | SMEMR#, SMEMW# negated before next ALE# asserted | | 1T | | Cycles |
| 29c[4] | IOR#, IOW# negated before next ALE# asserted | | 1T | | Cycles |
| **33[4]** | **LA[23:17] valid to IOCHRDY negated** | | | | |
| | 33a[4] | Memory access to 16 bit ISA Slave - 4 BCLK | 8T | | Cycles |
| | 33b[4] | Memory access to 8 bit ISA Slave - 7 BCLK | 14T | | Cycles |
| **34[4]** | **LA[23:17] valid to read data valid** | | | | |
| | 34b[4] | Memory access to 16 bit ISA Slave Standard cycle | 8T | | Cycles |
| | 34e[4] | Memory access to 8 bit ISA Slave Standard cycle | 14T | | Cycles |
| **37[4]** | **ALE# asserted to IOCHRDY# negated** | | | | |
| | 37a[4] | Memory access to 16 bit ISA Slave - 4 BCLK | 6T | | Cycles |
| | 37b[4] | Memory access to 8 bit ISA Slave - 7 BCLK | 12T | | Cycles |
| | 37c[4] | I/O access to 16 bit ISA Slave - 4 BCLK | 6T | | Cycles |
| | 37d[4] | I/O access to 8 bit ISA Slave - 7 BCLK | 12T | | Cycles |
| **38[4]** | **ALE# asserted to read data valid** | | | | |
| | 38b[4] | Memory access to 16 bit ISA Slave Standard Cycle | 4T | | Cycles |
| | 38e[4] | Memory access to 8 bit ISA Slave Standard Cycle | 10T | | Cycles |
| | 38h[4] | I/O access to 16 bit ISA Slave Standard Cycle | 4T | | Cycles |
| | 38l[4] | I/O access to 8 bit ISA Slave Standard Cycle | 10T | | Cycles |
| **41[4]** | **SA[19:0] SBHE valid to IOCHRDY negated** | | | | |
| | 41a[4] | Memory access to 16 bit ISA Slave | 6T | | Cycles |
| | 41b[4] | Memory access to 8 bit ISA Slave | 12T | | Cycles |
| Note; The signal numbering refers to Table 4-3 | | | | | |
| **Note 4; These timings are extracted from simulations and are not garanteed by testing** | | | | | |

### Table 4-9. ISA Bus AC Timing

| Name | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| | 41c[4] | I/O access to 16 bit ISA Slave | 6T | | Cycles |
| | 41d[4] | I/O access to 8 bit ISA Slave | 12T | | Cycles |
| **42[4]** | **SA[19:0] SBHE valid to read data valid** | | | | |
| | 42b[4] | Memory access to 16 bit ISA Slave Standard cycle | 4T | | Cycles |
| | 42e[4] | Memory access to 8 bit ISA Slave Standard cycle | 10T | | Cycles |
| | 42h[4] | I/O access to 16 bit ISA Slave Standard cycle | 4T | | Cycles |
| | 42l[4] | I/O access to 8 bit ISA Slave Standard cycle | 10T | | Cycles |
| **47[4]** | **MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW# asserted to IOCHRDY negated** | | | | |
| | 47a[4] | Memory access to 16 bit ISA Slave | 2T | | Cycles |
| | 47b[4] | Memory access to 8 bit ISA Slave | 5T | | Cycles |
| | 47c[4] | I/O access to 16 bit ISA Slave | 2T | | Cycles |
| | 47d[4] | I/O access to 8 bit ISA Slave | 5T | | Cycles |
| **48[4]** | **MEMR#, SMEMR#, IOR# asserted to read data valid** | | | | |
| | 48b[4] | Memory access to 16 bit ISA Slave Standard Cycle | 2T | | Cycles |
| | 48e[4] | Memory access to 8 bit ISA Slave Standard Cycle | 5T | | Cycles |
| | 48h[4] | I/O access to 16 bit ISA Slave Standard Cycle | 2T | | Cycles |
| | 48l[4] | I/O access to 8 bit ISA Slave Standard Cycle | 5T | | Cycles |
| **54[4]** | **IOCHRDY asserted to read data valid** | | | | |
| | 54a[4] | Memory access to 16 bit ISA Slave | 1T(R)/2T(W) | | Cycles |
| | 54b[4] | Memory access to 8 bit ISA Slave | 1T(R)/2T(W) | | Cycles |
| | 54c[4] | I/O access to 16 bit ISA Slave | 1T(R)/2T(W) | | Cycles |
| | 54d[4] | I/O access to 8 bit ISA Slave | 1T(R)/2T(W) | | Cycles |
| 55a[4] | IOCHRDY asserted to MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW# negated | | 1T | | Cycles |
| 55b[4] | IOCHRY asserted to MEMR#, SMEMR# negated (refresh) | | 1T | | Cycles |
| 56[4] | IOCHRDY asserted to next ALE# asserted | | 2T | | Cycles |
| 57[4] | IOCHRDY asserted to SA[19:0], SBHE invalid | | 2T | | Cycles |
| 58[4] | MEMR#, IOR#, SMEMR# negated to read data invalid | | 0T | | Cycles |
| 59[4] | MEMR#, IOR#, SMEMR# negated to daabus float | | 0T | | Cycles |
| **61[4]** | **Write data before MEMW# asserted** | | | | |
| | 61a[4] | Memory access to 16 bit ISA Slave | 2T | | Cycles |
| | 61b[4] | Memory access to 8 bit ISA Slave (Byte copy at end of start) | 2T | | Cycles |
| **61[4]** | **Write data before SMEMW# asserted** | | | | |
| | 61c[4] | Memory access to 16 bit ISA Slave | 2T | | Cycles |
| | 61d[4] | Memory access to 8 bit ISA Slave | 2T | | Cycles |
| **61[4]** | **Write Data valid before IOW# asserted** | | | | |
| | 61e[4] | I/O access to 16 bit ISA Slave | 2T | | Cycles |
| | 61f[4] | I/O access to 8 bit ISA Slave | 2T | | Cycles |
| 64a[4] | MEMW# negated to write data invalid - 16 bit | | 1T | | Cycles |
| 64b[4] | MEMW# negated to write data invalid - 8 bit | | 1T | | Cycles |
| 64c[4] | SMEMW# negated to write data invalid - 16 bit | | 1T | | Cycles |
| 64d[4] | SMEMW# negated to write data invalid - 8 bit | | 1T | | Cycles |
| 64e[4] | IOW# negated to write data invalid | | 1T | | Cycles |

Note; The signal numbering refers to Table 4-3

**Note 4; These timings are extracted from simulations and are not garanteed by testing**

**Table 4-9. ISA Bus AC Timing**

| Name | Parameter | Min | Max | Units |
|---|---|---|---|---|
| 64f[4] | MEMW# negated to copy data float, 8 bit ISA Slave, odd Byte by ISA Master | 1T | | Cycles |
| 64g[4] | IOW# negated to copy data float, 8 bit ISA Slave, odd Byte by ISA Master | 1T | | Cycles |
| Note; The signal numbering refers to Table 4-3<br>**Note 4; These timings are extracted from simulations and are not garanteed by testing** | | | | |

# 5. MECHANICAL DATA

## 5.1 388-Pin Package Dimension

Dimensions are shown in Figure 5-2, Table 5-1 and Figure 5-3, Table 5-2.

The pin numbering for the iDragon 388-pin Plastic BGA package is shown in Figure 5-1.

**Figure 5-1. 388-Pin PBGA Package - Top View**

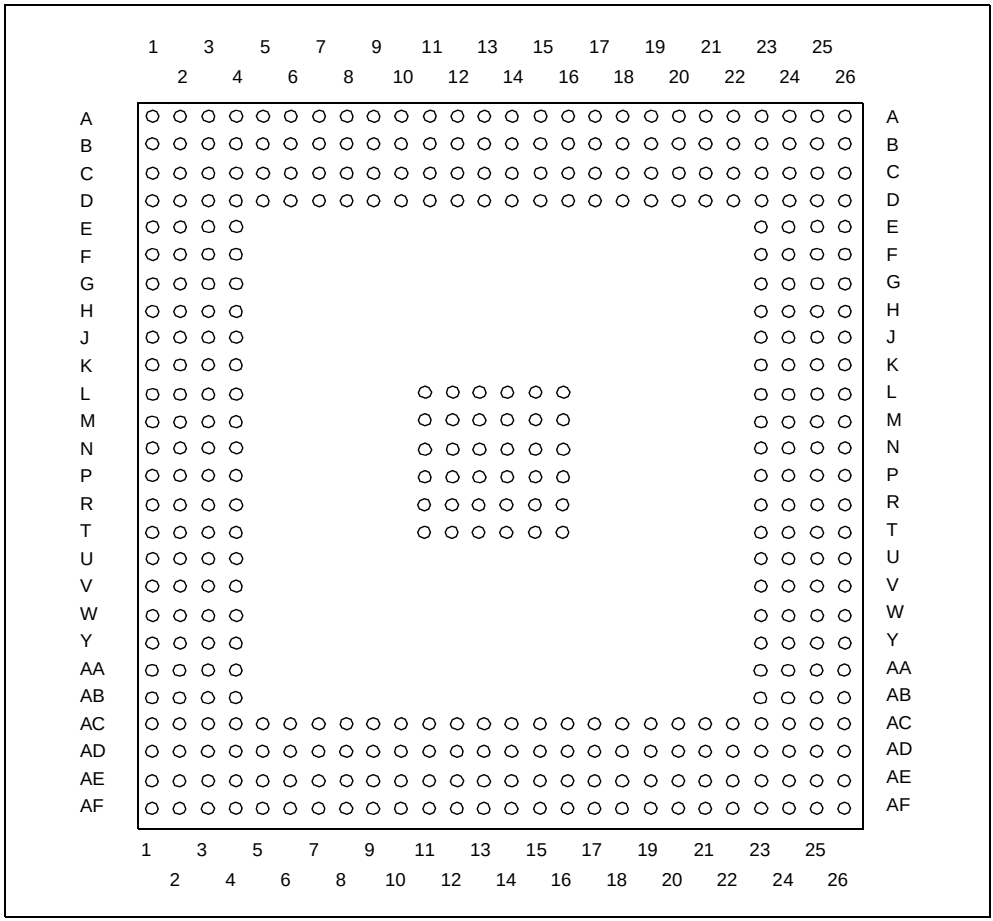


**Figure 5-2. 388-pin PBGA Package - PCB Dimensions**

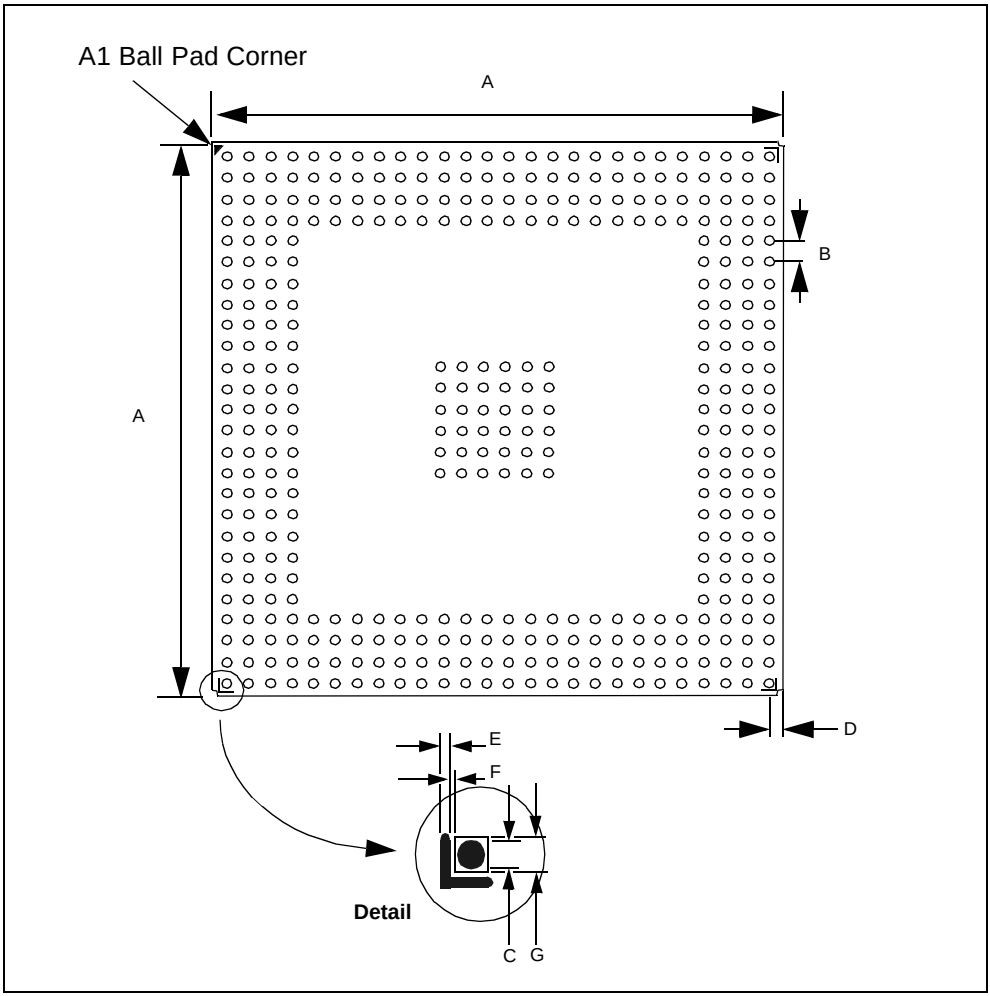



**Table 5-1. 388-pin PBGA Package - PCB Dimensions**

| Symbols | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 34.95 | 35.00 | 35.05 | 1.375 | 1.378 | 1.380 |
| B | 1.22 | 1.27 | 1.32 | 0.048 | 0.050 | 0.052 |
| C | 0.58 | 0.63 | 0.68 | 0.023 | 0.025 | 0.027 |
| D | 1.57 | 1.62 | 1.67 | 0.062 | 0.064 | 0.066 |
| E | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.001 |
| F | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| G | 0.75 | 0.80 | 0.85 | 0.030 | 0.032 | 0.034 |

**Figure 5-3. 388-pin PBGA Package - Dimensions**

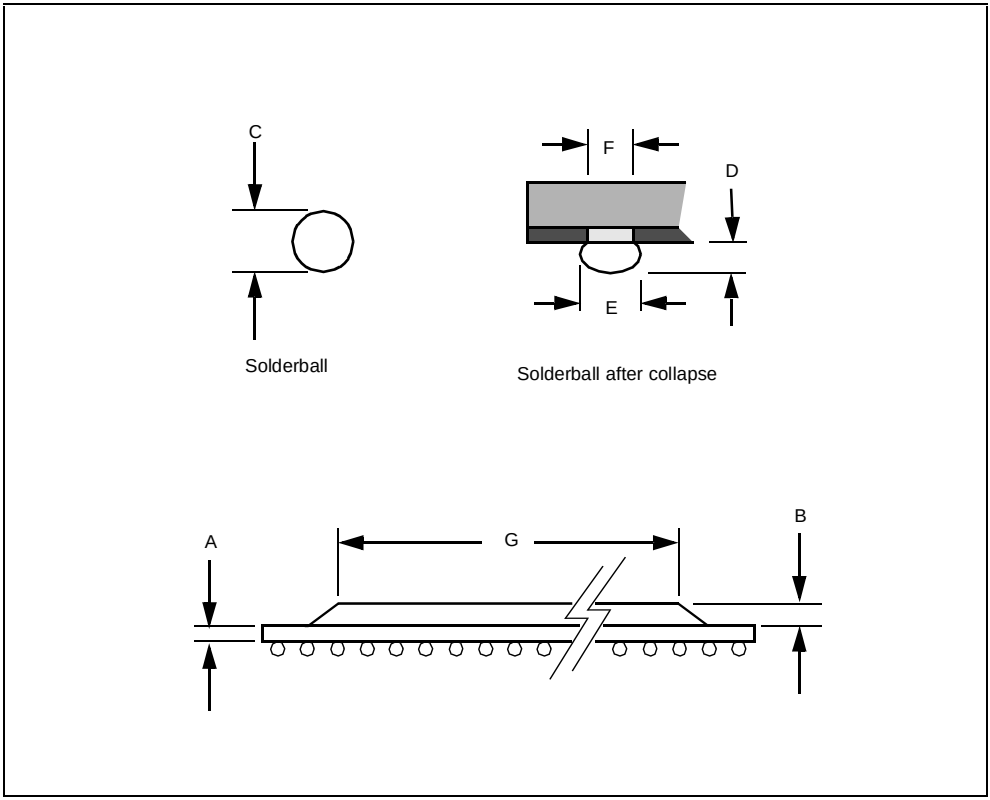



**Table 5-2. 388-pin PBGA Package - Dimensions**

| Symbols | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.50 | 0.56 | 0.62 | 0.020 | 0.022 | 0.024 |
| B | 1.12 | 1.17 | 1.22 | 0.044 | 0.046 | 0.048 |
| C | 0.60 | 0.76 | 0.92 | 0.024 | 0.030 | 0.036 |
| D | 0.52 | 0.53 | 0.54 | 0.020 | 0.021 | 0.022 |
| E | 0.63 | 0.78 | 0.93 | 0.025 | 0.031 | 0.037 |
| F | 0.60 | 0.63 | 0.66 | 0.024 | 0.025 | 0.026 |
| G | | 30.0 | | | 11.8 | |

### 5.2 388-Pin Package thermal data

388-pin PBGA package has a Power Dissipation Capability of 4.5W which increases to 6W when used with a Heatsink.

Structure in shown in Figure 5-4.

Thermal dissipation options are illustrated in Figure 5-5 and Figure 5-6.

**Figure 5-4. 388-Pin PBGA structure**

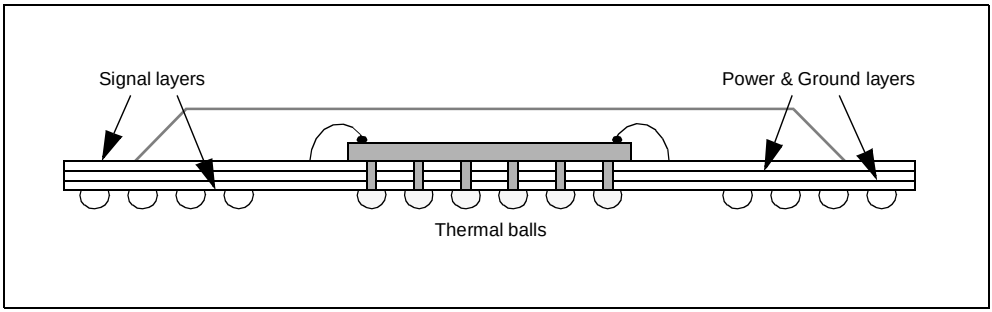



**Figure 5-5. Thermal dissipation without heatsink**

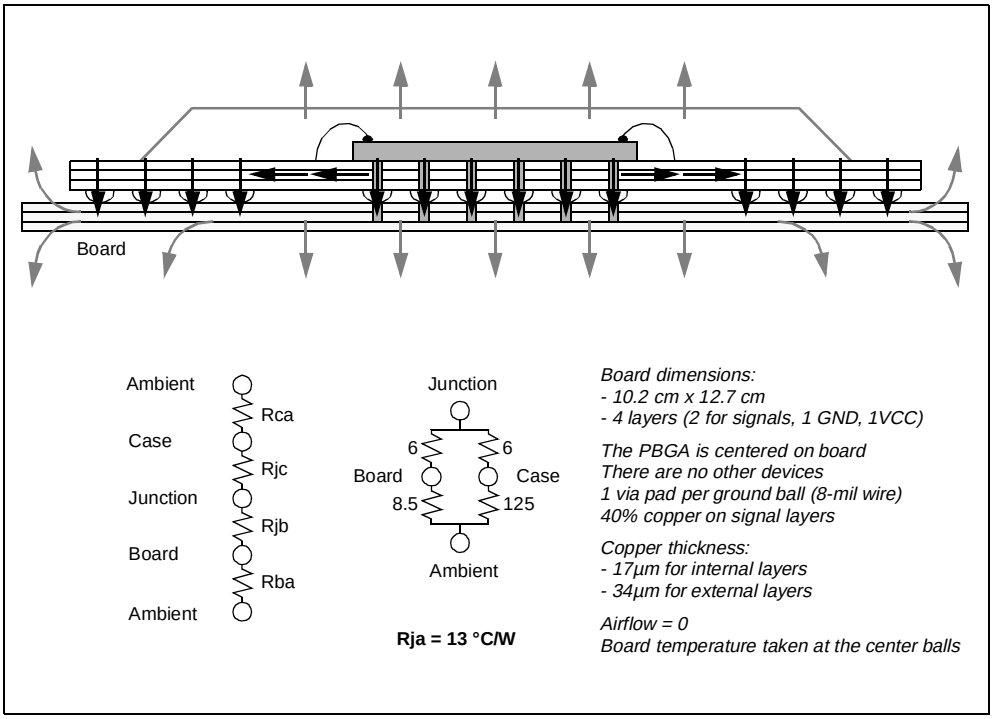
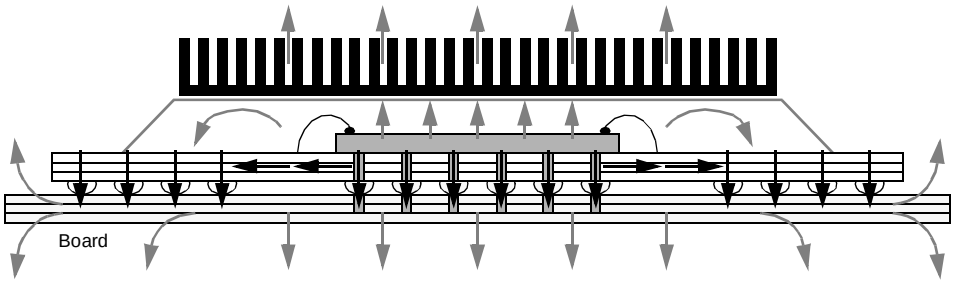
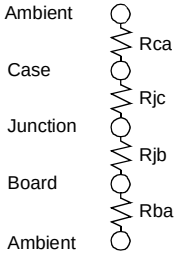
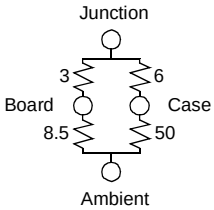


**Figure 5-6. Thermal dissipation with heatsink**




**Rja = 9.5 °C/W**

*Board dimensions:*
*- 10.2 cm x 12.7 cm*
*- 4 layers (2 for signals, 1 GND, 1VCC)*

*The PBGA is centered on board*
*There are no other devices*
*1 via pad per ground ball (8-mil wire)*
*40% copper on signal layers*

*Copper thickness:*
*- 17µm for internal layers*
*- 34µm for external layers*

*Airflow = 0*
*Board temperature taken at the center balls*
*Heat sink is 11.1°C/W*

# 6. BOARD LAYOUT

## 6.1 Thermal dissipation

Thermal dissipation of the iDragon depends mainly on supply voltage. As a result, when the system does not need to work at 3.45V, it is interesting to reduce the voltage to 3.15V, for example, if it is possible. This may save few 100's of mW.

The second area to look at is unused interfaces and functions. Depending on the application, some input signals can be grounded, and some blocks not powered or shutdown. Clock speed dynamic adjustment is also a solution that can be used along with the integrated power management unit.

The standard way to route thermal balls to internal ground layer implements only one via pad for each ball pad, connected using a 8-mil wire.

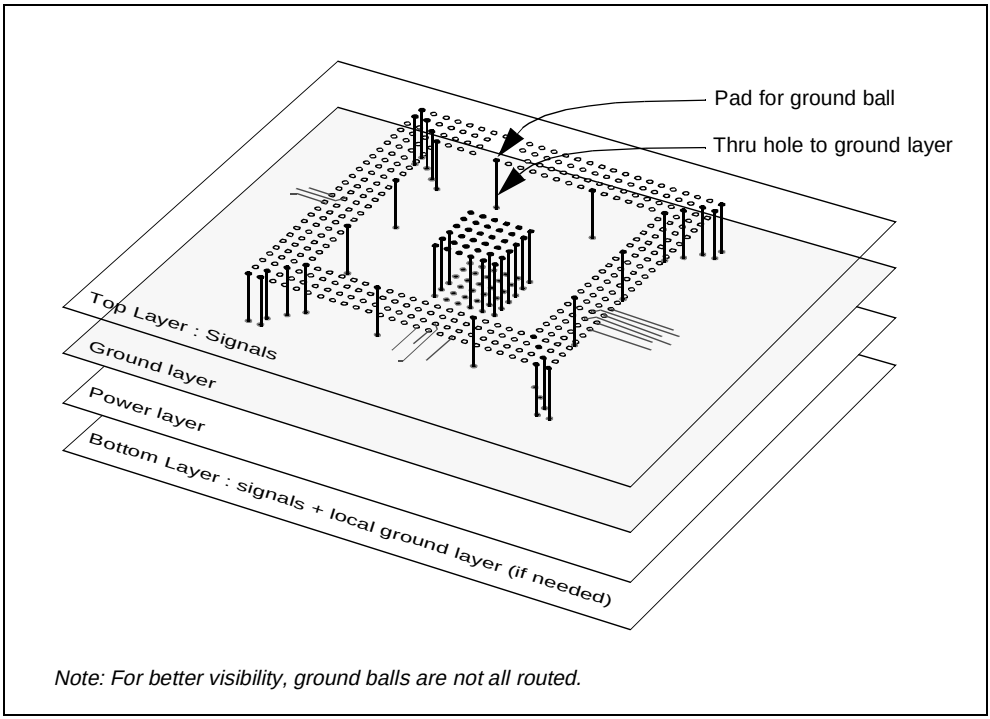
With such configuration the Plastic BGA 388 package does 90% of the thermal dissipation through the ground balls, and especially the central thermal balls which are directly connected to the die, the remaining 10% is dissipated through the case. Adding a heat sink reduces this value to 85%.

As a result, some basic rules has to be applied when routing the iDragon in order to avoid thermal problems.

First of all, the whole ground layer acts as a heat sink and ground balls must be directly connected to it as illustrated in Figure 6-1.

If one ground layer is not enough, a second ground plane may be added on solder side.

**Figure 6-1. Ground routing**




*Note: For better visibility, ground balls are not all routed.*

When considering thermal dissipation, the most important - and not the more obvious - part of the layout is the connection between the ground balls and the ground layer.

A 1-wire connection is shown in Figure 6-2. The use of a 8-mil wire results in a thermal resistance of 105°C/W assuming copper is used (418 W/m.°K). This high value is due to the thickness (34 µm) of the copper on the external side of the PCB.

Considering only the central matrix of 36 thermal balls and one via for each ball, the global thermal resistance is 2.9°C/W. This can be easily improved using four 10 mil wires to connect to the four vias around the ground pad link as in Figure 6-3. This gives a total of 49 vias and a global resistance for the 36 thermal balls of 0.6°C/W.

The use of a ground plane like in Figure 6-4 is even better.

To avoid solder wicking over to the via pads during soldering, it is important to have a solder mask of 4 mil around the pad (NSMD pad), this gives a diameter of 33 mil for a 25 mil ground pad.

To obtain the optimum ground layout, place the vias directly under the ball pads. In this case no local boar d distortion is tolerated.

The thickness of the copper on PCB layers is typically 34 µm for external layers and 17 µm for internal layers. That means thermal dissipation is not good and temperature of the board is concentrated around the devices and falls quickly with increased distance.

When it is possible to place a metal layer inside the PCB, this improves dramatically the heat spreading and hence thermal dissipation of the board.

**Figure 6-2. Recommended 1-wire ground pad layout**

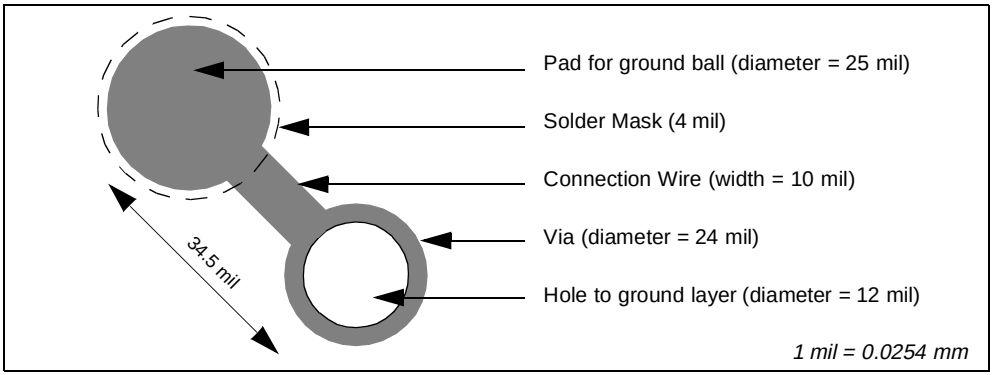



**Figure 6-3. Recommended 4-wire ground pad layout**

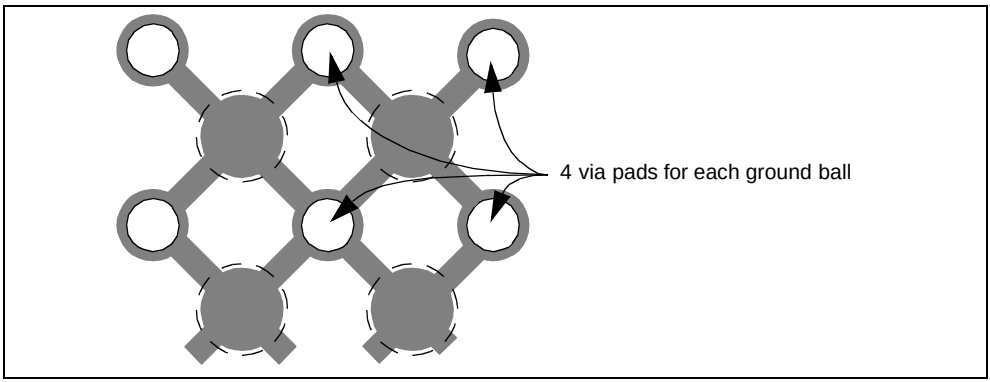
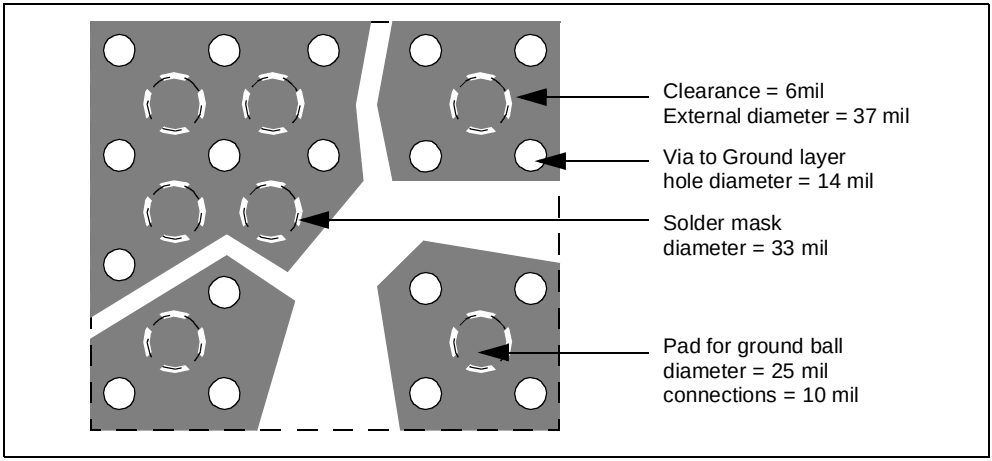


**Figure 6-4. Optimum layout for central ground ball**




The PBGA Package dissipates also through peripheral ground balls. When a heat sink is placed on the device, heat is more uniformely spread throughout the moulding increasing heat dissipation through the peripheral ground balls.

The more via pads are connected to each ground ball, the more heat is dissipated . The only limitation is the risk of lossing routing channels.

Figure 6-5 shows a routing with a good trade off between thermal dissipation and number of routing channels.

A local ground plane on opposite side of the board as shown in Figure 6-6 improves thermal dissipation. It is used to connect decoupling capacitances but can also be used for connection to a heat sink or to the system's metal box for better dissipation.

This possibility of using the whole system's box for thermal dissipation is very usefull in case of high temperature inside the system and low temperature outside. In that case, both sides of the PBGA should be thermally connected to the metal chassis in order to propagate the heat flow through the metal. Figure 6-7 illustrates such implementation.

### 6.2 High speed signals

Some Interfaces of the iDragon run at high speed and have to be carefully routed or even shielded.

Here is the list of these interfaces, in decreasing speed order:

1) Memory Interface.

2) Graphics and video interfaces

3) PCI bus

4) 14MHz oscillator stage

All the clocks haves to be routed first and shielded for speeds of 27MHz or more. The high speed signals follow the same contrainsts, like the memory control signals and the PCI control signals.

The next interfaces to be routed are Memory, Vid eo/graphics, and PCI.

All the analog noise sensitive signals have to be routed in a separate area and hence can be rout ed indepedently.

**Figure 6-5. Global ground layout for good thermal dissipation**

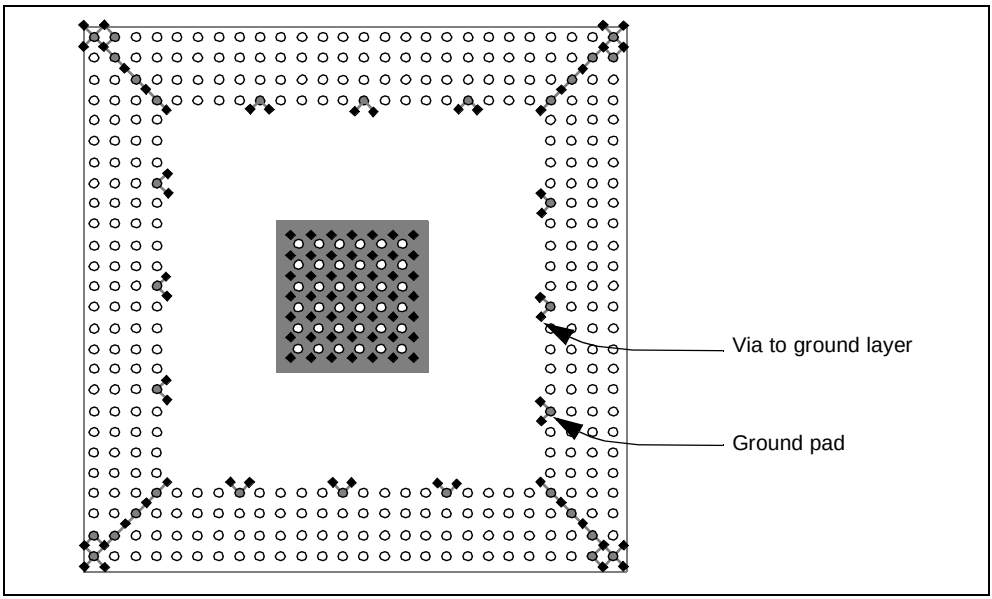



**Figure 6-6. Bottom side layout and decoupling**

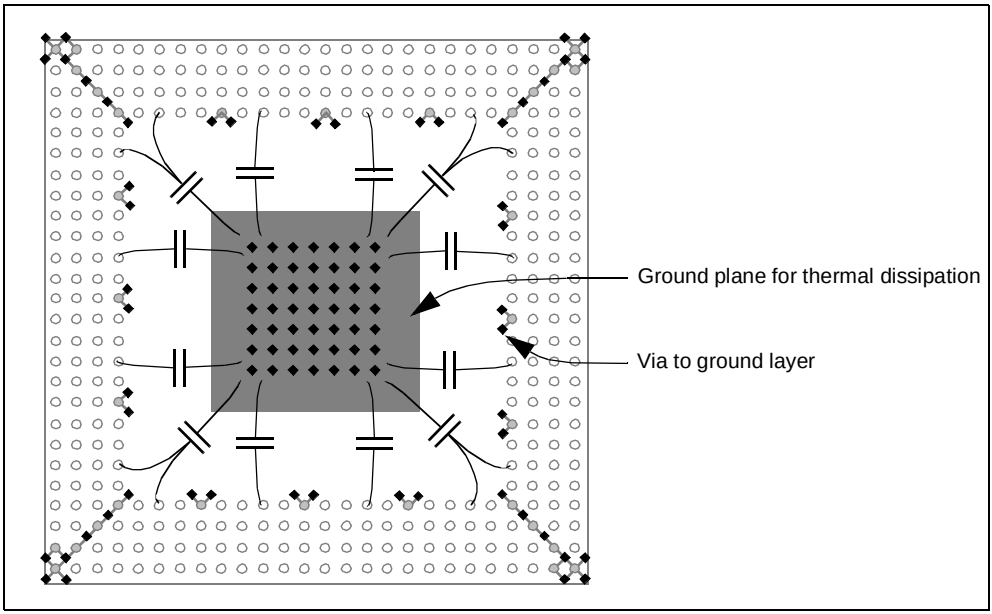


**Figure 6-7. Use of metal plate for thermal dissipation**

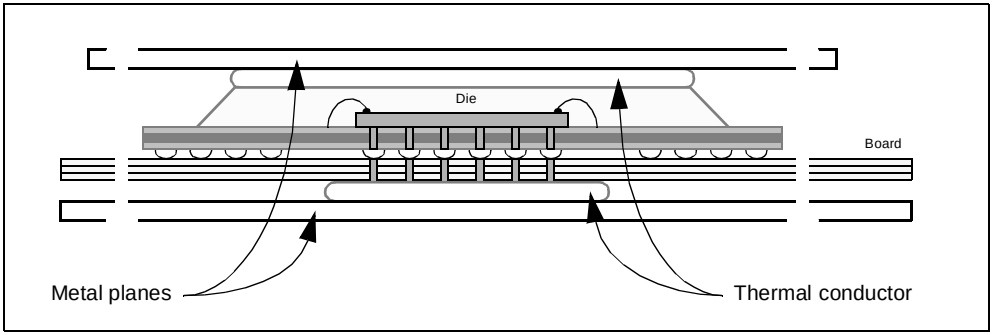
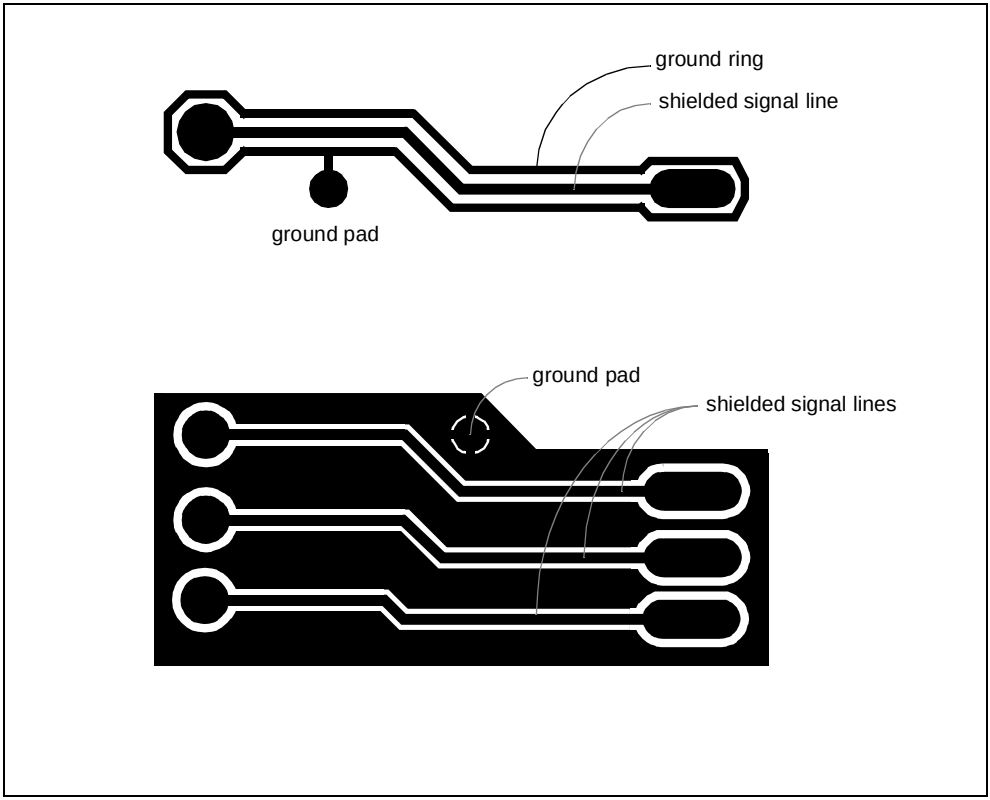



**Figure 6-8. Shielding signals**



### 6.3 Memory interface

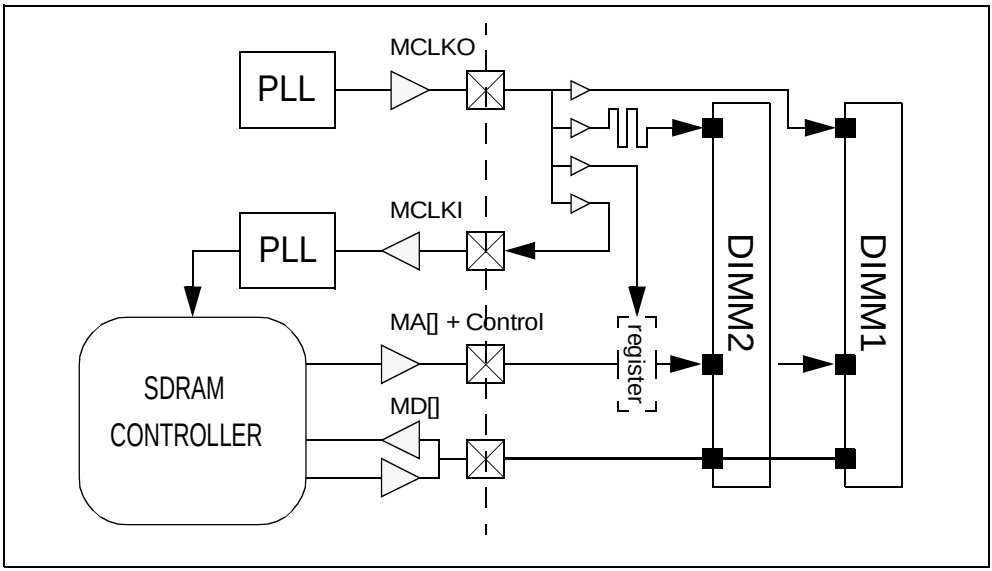
#### 6.3.1 Introduction

In order to achieve SDRAM memory interfaces which work at clock frequencies of 100MHz and above, careful consideration has to be given to the timing of the interface with all the various electrical and physical constraints taken into consideration. The guidelines described below are related to SDRAM components on DIMM modules. For applications where the memories are directly soldered to the motherboard, the PCB should be laid out such that the trace lengths fit within the constraints shown here. The traces could be slightly longer since the extra routing on the DIMM PCB is no longer present but it is then up to the user to verify the timings.

#### 6.3.2 SDRAM Clocking Scheme

The SDRAM Clocking Scheme deserves a special mention here. Basically the memory clock is gen erated on-chip through a PLL and goes directly to the MCLKO output pin of the iDragon. The nomi nal frequency is 100MHz. Because of the high load presented to the MCLK on the board by the DIMMs it is recommeded to rebuffer the MCLKO signal on the board and balance the skew to the clock ports of the different DIMMs and the MCLKI input pin of iDragon.

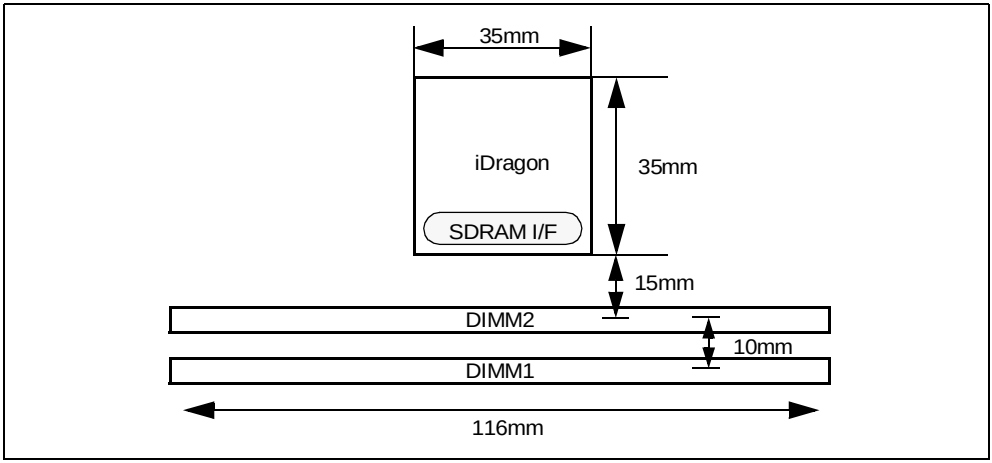
**Figure 6-9. Clock scheme**



### 6.3.3 Board Layout Issues

The physical layout of the motherboard PCB assumed in this presentation is as shown in Figure 6-10. Because all the memory interface signal balls are located in the same region of the iDragon device it is possible to orientate the device to reduce the trace lengths. The worst case routing length to the DIMM1 is estimated to be 100mm.

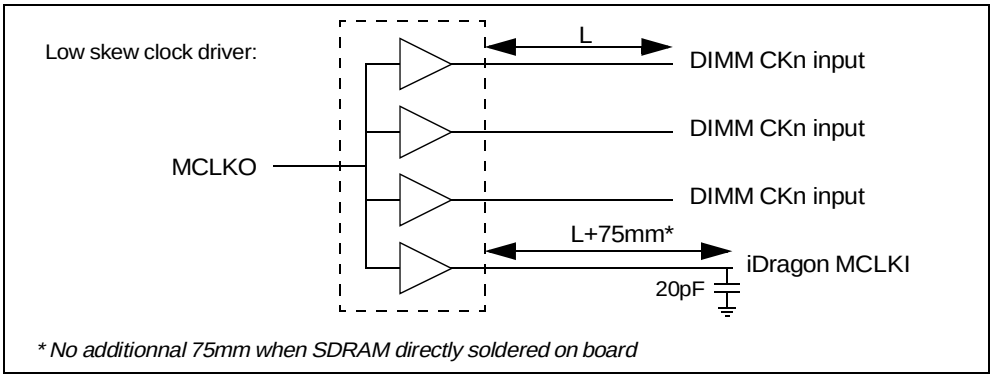
**Figure 6-10. DIMM placement**




Solid power and ground planes are a must in order to provide good return paths for the signals and to reduce EMI and noise. Also there should be ample high frequency decoupling between the power and ground planes to provide a low impedance path between the planes for the return paths for signal routings which change layers. If possible the traces should be routed adjacent to the same power or ground plane for the length of the trace.

For the SDRAM interface the most critical signal is the clock. Any skew between the clocks at the SDRAM components and the memory controlle will impact the timing budget. In order to get well matched clocks at all the components it is recommended that all the DIMM clock pins, iDragon memory clock input (MCLKI) and any other com ponent using the memory clock are individually driven from a low skew clock driver with matched routing lengths. This is shown in Figure 6-11.

**Figure 6-11. Clock routing**




** No additionnal 75mm when SDRAM directly soldered on board*

The maximum skew between pins for this part is 250ps. The important factors for the clock buffer are a consistent drive strength and low skew between the outputs. The delay through the buffer is not important so it does not have to be a zero delay PLL type buffer. The trace lengths from the clock driver to the DIMM CKn pins should be matched exactly. Since the propagation speed can vary between PCB layers the clocks should be routed in a consistent way. The routing to the iDragon memory input should be longer by 75mm to compensate for the extra clock routing on the DIMM. Also a 20pF capacitor should be placed as near as possible to the clock input of the iDragon to compensate for the DIMM's higher clock load. The impedance of the trace used for the clock routing should be matched to the DIMM clock trace impedance (60-75 ohms). To minimise crosstalk the clocks should be routed with spacing to adjacent tracks of at least twice the clock trace width. For designs which use SDRAMs directly mounted on the motherboard PCB all the clock trace lengths should be matched exactly.

The DIMM sockets should be populated starting with the furthest DIMM from the iDragon device first (DIMM1). There are 2 types of DIMM devices; single row and dual row. The dual row devices require 2 chip select signals to select between the two rows. A iDragon device with 4 chip select control lines could control either 4 single row DIMMs or 2 dual row DIMMs.

When using DIMM modules, schematics have to be done carefully in order to avoid data busses completely crossed on the board. This has to be checked at the library level. In order to achive layout shown in Figure 6-12, schematics have to implement the crossing described on Figure 6-13. The DQM signals must be exchanged using the same order.

**Figure 6-12. Optimum data bus layout for DIMM**

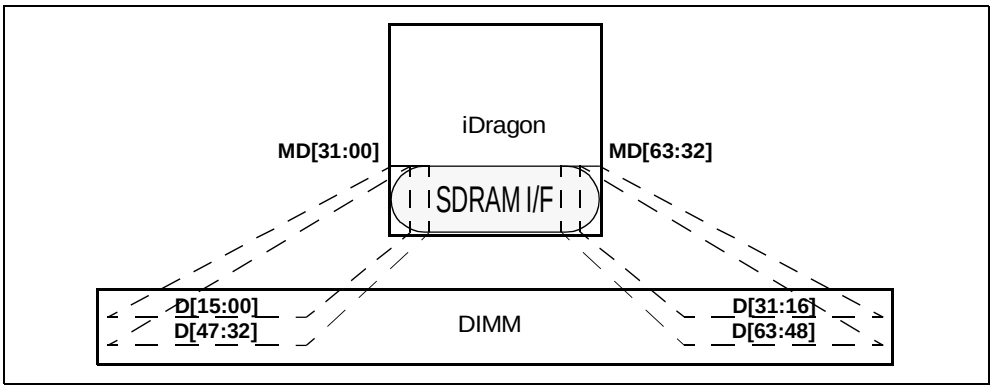
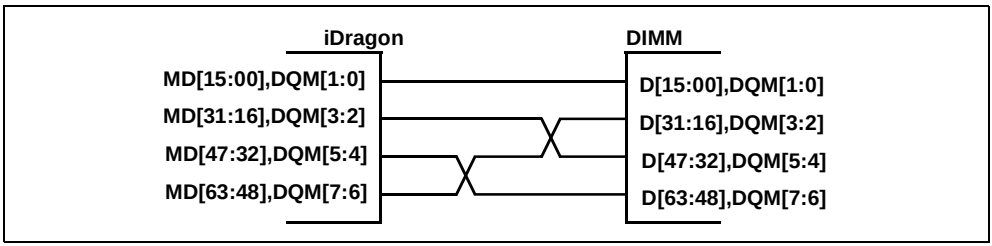


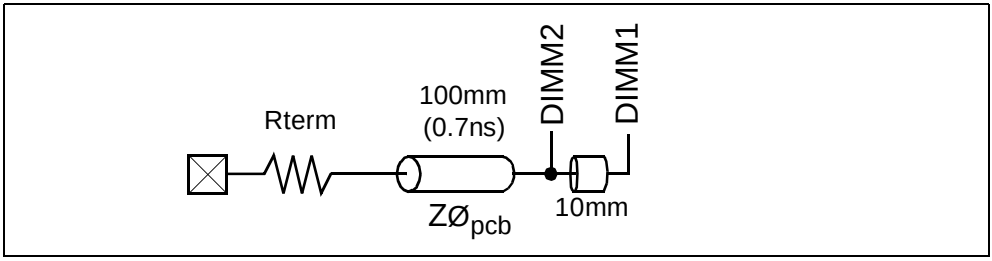

**Figure 6-13. Schematics for optimum data bus layout for DIMM**



### 6.3.4 Address & Control Signals

This group encompasses the memory address MA[10:0], bank address BA[0], RAS, CAS and write enable WE signals. The load of the DIMM module on these signals is the most important one and depends upon the type of SDRAM components used (x4, x8 or x16) and whether the DIMM module is single or dual row. The capacitive loading of the SDRAM inputs alone for an x8 single row DIMM will be about 30-40pF. An equivalent circuit for the timing simulation is shown in Figure 6-14 Most of the delays are due to the PCB traces and loading rather than the pad itself.

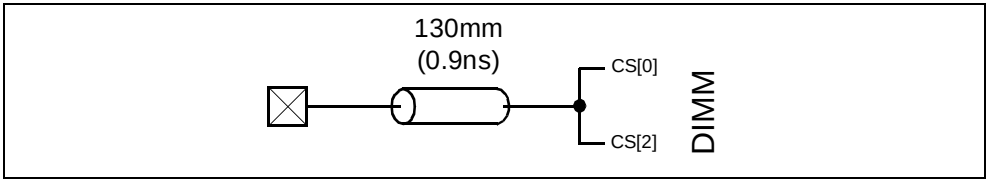
**Figure 6-14. Address/control equivalent circuit**



### 6.3.5 Chip Select Signals (CS#[3:0])

There are 4 chip select pins per DIMM. Chip selects 0 and 2 are always used to select the first row of SDRAMs and chip selects 1 and 3 select the second row on dual bank SDRAMs. The chip select outputs only have to drive one DIMM each

**Figure 6-15. CS# equivalent circuit**



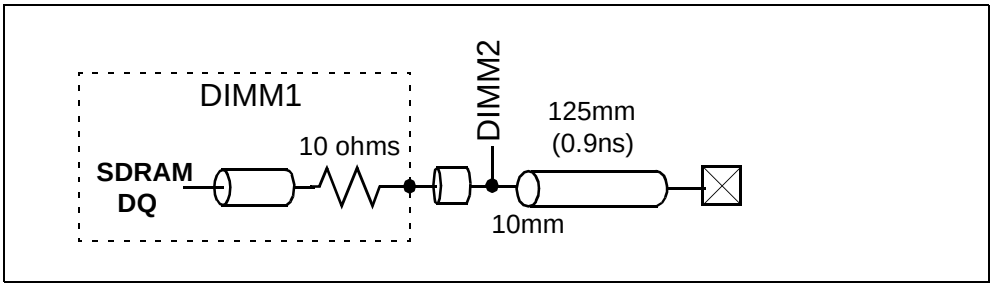
### 6.3.6 Data Write (MD[63:0])

The load on the data signals is much lower than the address/control signals for an unbuffered DIMM. For a registered DIMM the data signals are the only memory pins of the DIMM which are not registered. For the design to get maximum benefit from using registered DIMMs the timings should be compared to the timings for registered DIMMs for the other pins.

### 6.3.7 Data Read (MD[63:0])

The data read simulation circuit is shown below..

**Figure 6-16. Data read equivalent circuit**



### 6.3.8 Data Mask (DQM[7:0])

The data mask load is quite similar to that of the data signals.

### 6.3.9 Summary

For unbuffered DIMMs the address/control signals will be the most critical for timing. The simulations show that for these signals the best way to drive them is to use a parallel termination. For applications where speed is not so critical series termination can be used as this will save power. Using a low impedance such as 50Ω for these critical traces is recommended as it both reduces the delay and the overshoot.

The other memory interface signals will typically be not as critical as the address/control signals for unbuffered DIMMs. When using registered DIMMs the other signals will probably be just as critical as the address/control signals so to gain maximum benefit from using registered DIMMs the timings should also be considered in that situation. Using lower impedance traces is also beneficial for the other signals but if their timing is not as critical as the address/control signals they could use the default value. Using a lower impedance implies using wider traces which may have an impact on the routing of the board.

## 6.4 SDRAM LAYOUT EXAMPLES

The iDragon provides MA, RAS#, CAS#, WE#, CS#, DQM#, BA0 (MA[11])and MD for SDRAM control. From 2 to 128 MBytes of main memory are supported in 1 to 4 banks. All Banks must be 64 bits wide.

The following memory devices are supported:

4Mbit x 4, 8Mbit x 2 & 16Mbit x 1 or if in the case of two internal bank chips, 2Mbit x 4 x 2, 4Mbit x 2 x 2 & 8Mbit x 1 x 2 .

The following Figure 6-17 and Figure 6-18, shows two possible SDRAM organizations based on one or two bank configurations.

Notes for Figure 6-17 and Figure 6-18;

All buffers must be low skew clock buffers

One clock driver can operate upto four memory chips.

All the clock lines must follow the rules below;

MCLKI = MCLK0 + MCLK0A

= .....

= MCLK0 + MCLK0

= MCLK1 + MCLK1A

= .....

= MCLK1 + MCLK1

This means that all line lengths must go from the buffer to the memory chips (MCLK1 or MCLK0 o ...) and from the buffer to the iDragon (MCLKI must be identical.

### 6.4.1 Host Address to MA bus Mapping

Graphics memory resides at the beginning of Bank 0. Host memory begins at the top of graphics memory and extends to the top of populated SDRAM.

The bank attributes can be retrieved from a lookup table to select the final SDRAM row and column address mappings. ( Table 6-2). Also Table 6-1 shows the Standard DIMM Pinout for the users that wish to design with DIMMs.

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**Figure 6-17. One memory Bank with eight chips (8-Bit)**

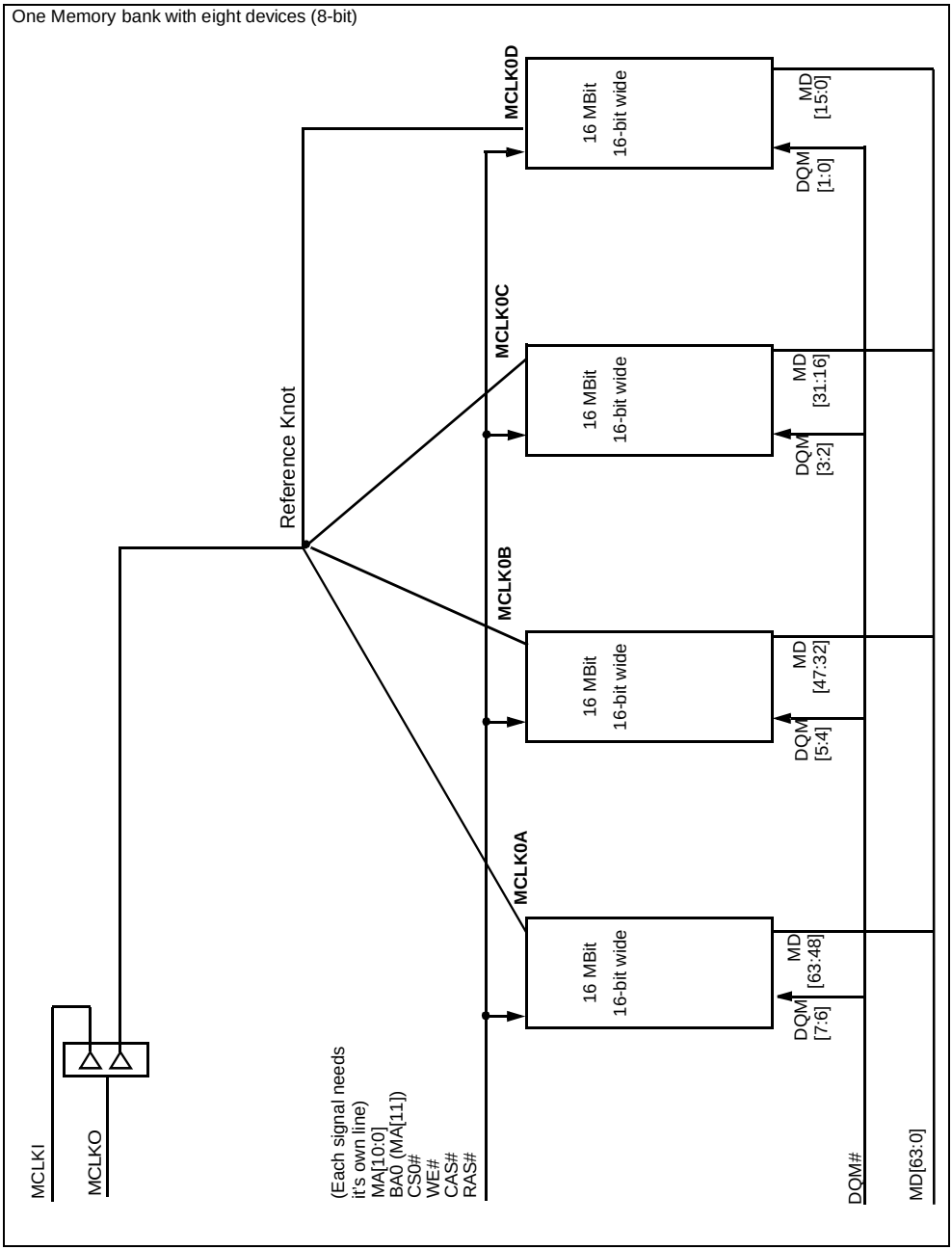


**Figure 6-18. Two memory banks with eight chips on each (8-Bit)**

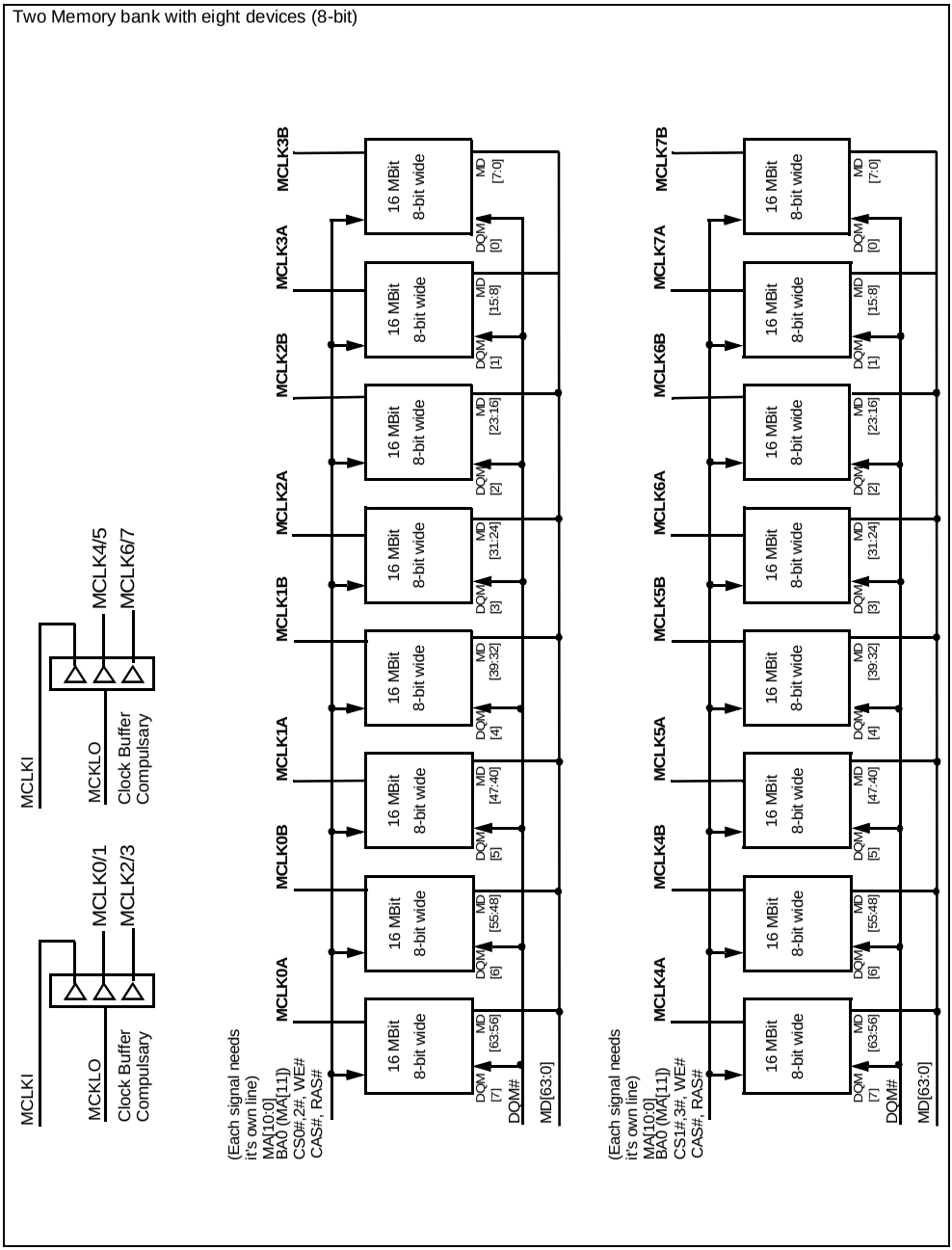


**Table 6-1. Standard Memory DIMM Pinout**

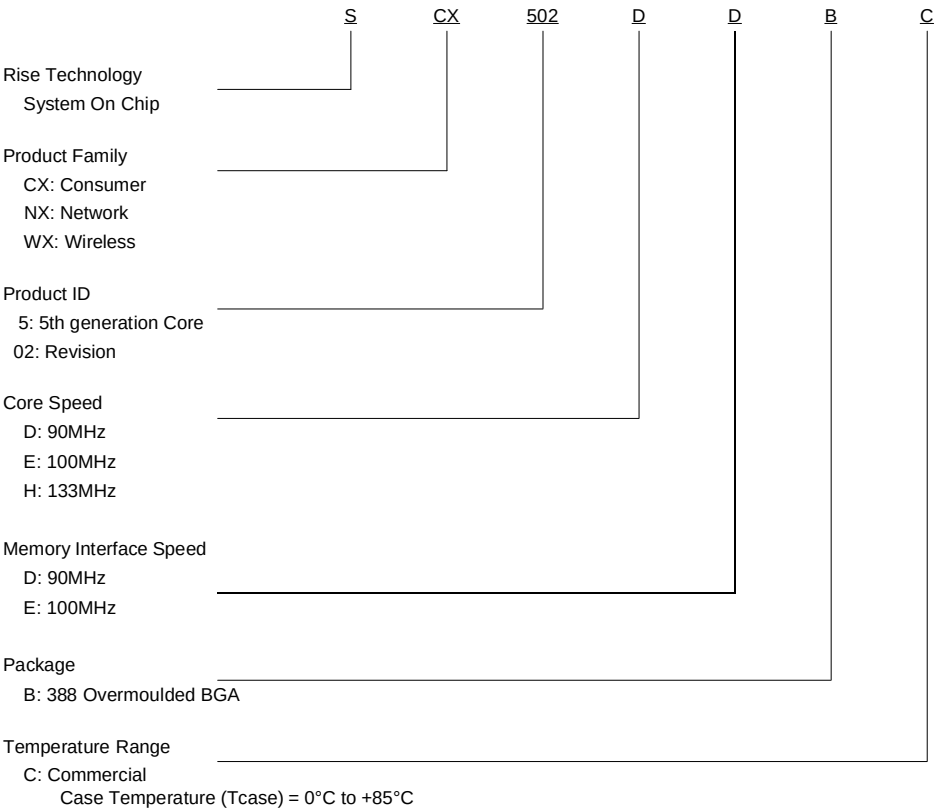
| Memory Banks pin number | 16Mbit(2 banks) |
|---|---|
| ... | MA[10:0] |
| 123 | - |
| 126 | - |
| 39 | - |
| 122 | BA0(MA11) |

**Table 6-2. Address Mapping**

| **Address Mapping: 16 Mbit - 2 banks** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| iDragon I/F | BA0(MA11) | MA10 | MA9 | MA8 | MA7 | MA6 | MA5 | MA4 | MA3 | MA2 | MA1 | MA0 |
| RAS ADDRESS | A11 | A22 | A21 | A2 | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 |
| CAS ADDRESS | A11 | 0 | A24 | A23 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 |

# 7 ORDERING DATA

## 7.1 Ordering Codes



### 7.2 Available Part Numbers

| Part Number | Core Frequency ( MHz ) | CPU Mode ( X1 / X2 ) | Interface Speed (MHz) | Tcase Range ( °C ) |
|---|---|---|---|---|
| SCX502DDBC | 90 | X1 | 90 | 0°C to +85° |
| SCX502EEBC | 100 | X1 | 100 | |
| SCX502HDBC | 133 | X2 | 90 | |

### 7.3 Customer Service

More informations are available on Rise Technology internet site *http://www.rise.com*.