SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The MAB80XXH family of single-chip 8-bit microcontrollers is fabricated in NMOS. Three interchangeable (pin compatible) versions are available:

- MAB8048H: 1 K bytes mask-programmed ROM, 64 bytes RAM
- MAB8035HL: ROM-less version of the MAB8048H
- MAB8049H: 2 K bytes mask-programmed ROM, 128 bytes RAM
- MAB8039HL: ROM-less version of the MAB8049H
- MAB8050H: 4 K bytes mask-programmed ROM, 256 bytes RAM
- MAB8040HL: ROM-less version of the MAB8050H

These microcontrollers are designed to be efficient control processors as well as arithmetic processors. Their instruction set allows the user to directly set and reset individual I/O lines as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions enable efficient implementation of standard logic functions. Code efficiency is high; over 70% of the instructions are single byte; all others are two byte.

An on-chip 8-bit counter is provided, which can count either machine cycles (÷32) or external events. The counter can be used to generate an interrupt to the processor.
Program and data memories plus input/output capabilities can be expanded using standard TTL compatible memories and logic. For more detailed information see the 8048 family specification.

Features

- 8-bit CPU, ROM, RAM and I/O
- 8-bit counter/timer
- On-chip oscillator and clock driver circuits
- Single-level interrupts: external and counter/timer
- 17 internal registers: accumulator, 16 addressable registers
- Over 90 instructions: 70% single byte
- All instructions 1 or 2 cycles
- Easily expandable memory and 27 I/O lines
- TTL compatible inputs and outputs
- Single 5 V supply
- Standard and extended temperature ranges (see Table 5): MAB80XX: 0 to +70 °C
  MAF80XX: −40 to +85 °C
  MAF80AXX: −40 to +110 °C

Applications

- Peripheral interfaces and controllers
- Test and measuring instruments
- Sequencers
- Modems and data enciphering
- Environmental control systems
- Audio/video systems

PACKAGE OUTLINES

All versions: with type no. suffix P (see Table 5): 40-lead DIL; plastic (SOT-129).
MAB8035/8048/8039/8049H/HLWP : 44-lead PLCC; plastic leaded chip-carrier (SOT187AA).

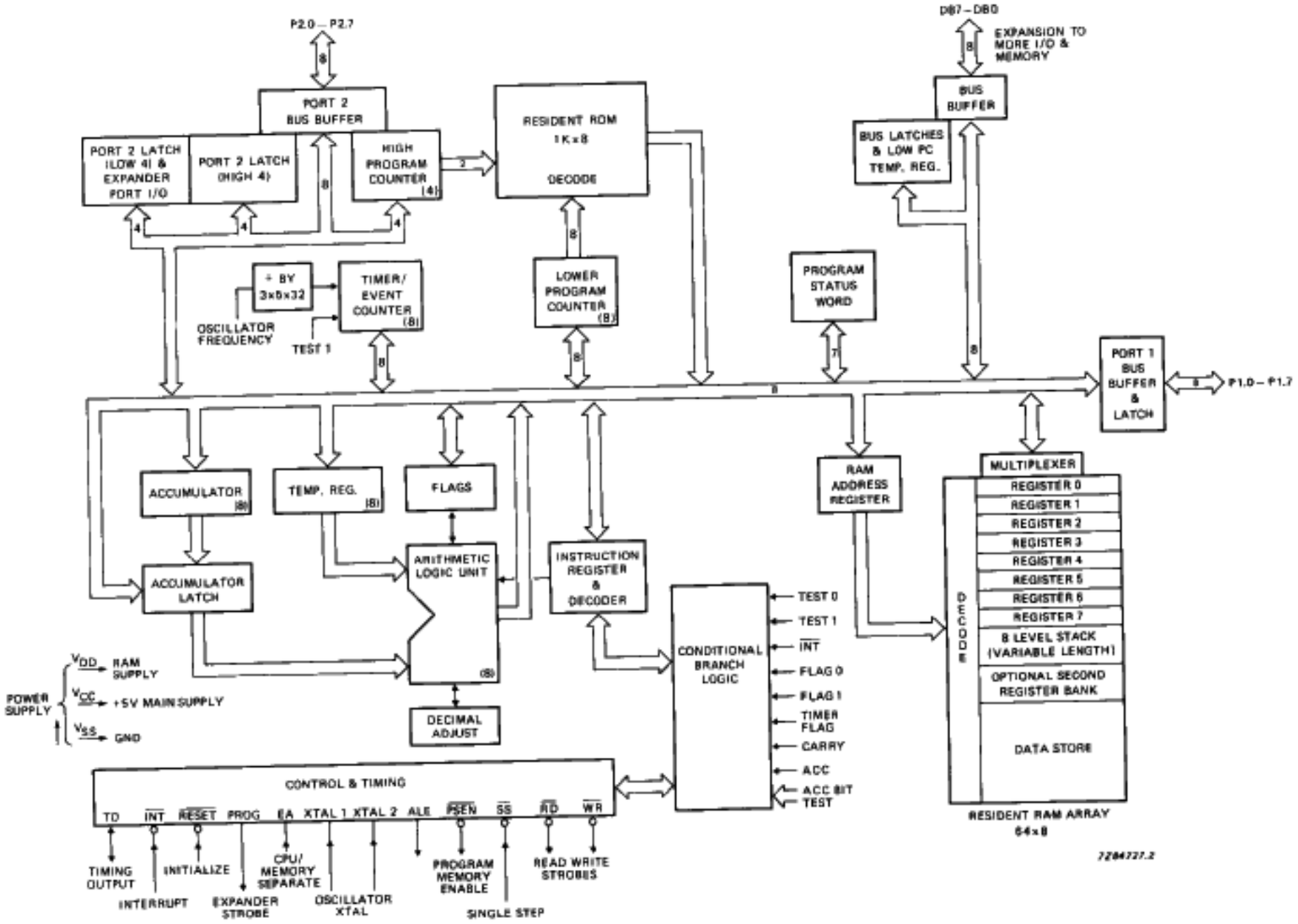


Fig. 1 Block diagram.

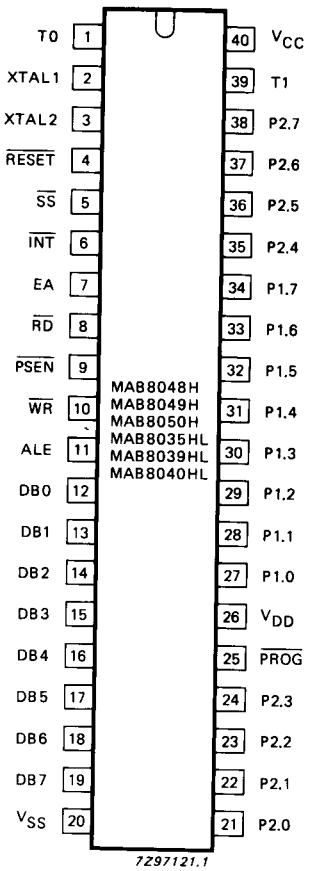


Fig. 2a Pinning diagram; for pin designation see next page.

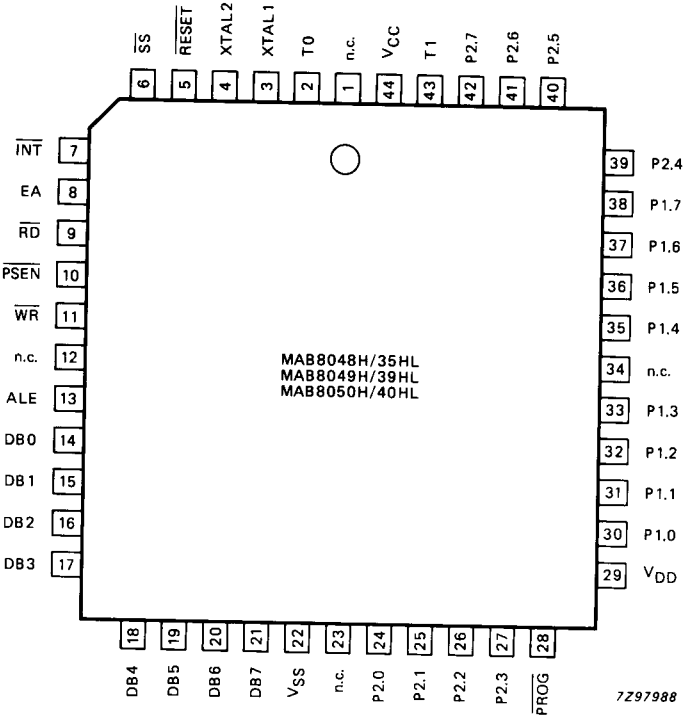


Fig. 2b Pinning diagram for MAB80XXHWP; for pin designation see next page.

Product type numbering European and USA cross-reference scheme

Type numbering reference used mainly in Europe	Type numbering equivalent reference used mainly in USA
MAB8039HLP/HLWP	SCN8039HCB N40/A44
MAF8039HLP/HLWP	SCN8039HAB N40/A44
MAB8049HP/HWP	SCN8049HCB N40/A44
MAF8049HP/HWP	SCN8049HAB N40/A44
MAB8040HLP/HLWP	SCN8040HCB N40/A44
MAF8050HP/HWP	SCN8050HCB N40/A44

PINNING

12–19	DB0–DB7	**Data Bus:** true bidirectional I/O port which can be written or read using the $\overline{RD}$ and $\overline{WR}$ strobes. This port can also be used as an 8-bit latch. It contains the 8 low order address bits during an external memory access and receives the addressed instruction under control of $\overline{PSEN}$. This multiplexed address/data port also contains the address and data during external RAM accesses.
27–34	P1.0–P1.7	**Port 1:** 8-bit quasi-bidirectional I/O port (note 1).
21–24	P2.0–P2.7	**Port 2:** 8-bit quasi-bidirectional I/O port (note 1).
35–38		P2.0–P2.3 contains the 4 higher order address bits during an external program memory access and provides a 4-bit bus for 8243 I/O expanders.
25	$\overline{PROG}$	**Output strobe:** active LOW for 8243 I/O expanders.
1	T0	**Test 0:** input pin which can be tested by the JT0 and JNT0 instructions. **Clock:** T0 can be configured as a clock output using the ENT0 CLK instruction.
39	T1	**Test 1:** input pin which can be tested using the JT1 and JTN1 instructions. T1 can be configured as the timer/counter input using the STRT CNT instruction.
6	$\overline{INT}$	**Interrrupt:** interrupt input pin which can initiate an interrupt if the external interrupt is enabled. Can also be tested using the JNI instruction. Interrupt is disabled during and after $\overline{RESET}$.
4	$\overline{RESET}$	**Reset:** active LOW input used to initialize the microcontroller. During program verification, the address is latched by a 0– to –1 transition on $\overline{RESET}$ and the data at the addressed location is output on BUS (note 2).
11	ALE	**Address latch enable:** occurs each cycle and is useful as a clock output. During an external program or data memory access, ALE is used to latch the address information multiplexed on the DB0 to DB7 outputs.
8	$\overline{RD}$	**Read BUS:** active LOW strobe used to gate data on to BUS lines when reading from an external source.
10	$\overline{WR}$	**Write BUS:** active LOW strobe used to write data from BUS lines to an external designation.
7	EA	**External access input:** when HIGH, all instruction fetches are from external memory.
9	$\overline{PSEN}$	**Program store enable:** active LOW strobe that occurs only during a fetch from external memory.
5	$\overline{SS}$	**Single step:** active LOW input used with ALE to cause the microcontroller to execute a single instruction.
2 3	XTAL 1 XTAL 2	**Crystal inputs:** inputs for a crystal, LC-network or an external timing signal to determine the internal oscillator frequency (note 2).
20	V_{SS}	**Ground:** circuit earth potential.
40	V_{CC}	**Power supply:** + 5 V main power supply pin.
26	V_{DD}	**Power supply:** + 5 V RAM standby power supply; low power

Notes

1. Each port line can be individually configured as an input or an output. A line is designated as an input by first writing a logic 1 to the line. $\overline{\text{RESET}}$ sets all port lines to logic 1.
2. Non-standard TTL V_{IH}.

FUNCTIONAL DESCRIPTION

The following sections provide a detailed functional description of the MAB80XXH microcontroller as shown in Fig. 1. The generic term "MAB80XXH" is used to refer collectively to the MAB8048H/35HL, MAB8049H/39HL and MAB8050H/40HL.

Program memory (see Fig. 3)

The on-chip program memory consists of 1024, 2048 or 4096 bytes of mask programmed ROM (MAB8048H/49H/50H); the MAB8035HL/39HL/40HL versions do not have on-chip program memory. The total addressing capability is 4096 bytes.
The program memory address space is divided into two 2048-byte banks MB0 and MB1. These two 2048 byte banks are each divided into 8 pages of 256 bytes for conditional branches. There are three locations in program memory of special interest. These are:

- Location 0 — contains the first instruction to be executed after a $\overline{\text{RESET}}$
- Location 3 — contains the first instruction of an external interrupt routine
- Location 7 — contains the first instruction of a timer/counter interrupt routine

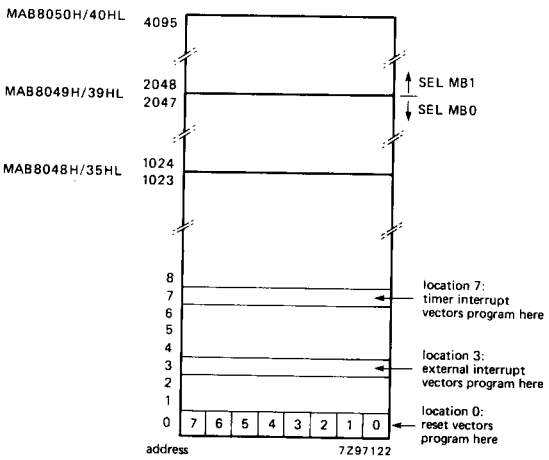


Fig. 3 Program memory map.

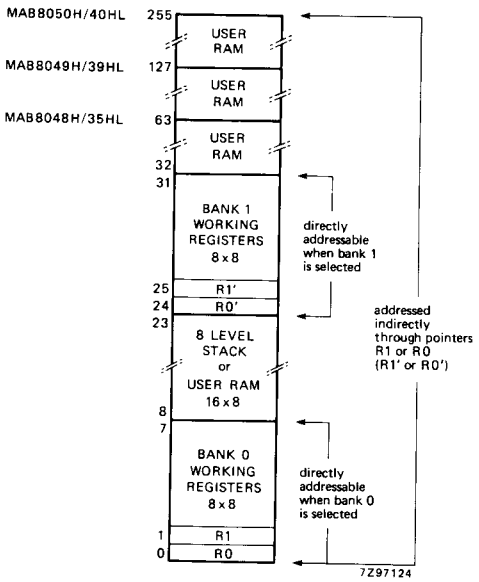


Fig. 4 Data memory map.

FUNCTIONAL DESCRIPTION (continued)

Data memory (see Fig. 4)

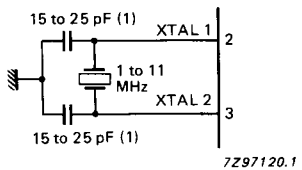
The on-chip data memory consists of a 64, 128 or 256 byte RAM. All locations are indirectly addressable using two RAM pointer registers R0, R1 or R0', R1'. The first 8 RAM locations (0 to 7) are designated as working register bank 0 and are directly addressable. By selecting register bank 1, RAM locations 24 to 31 become the working registers. RAM locations 8 to 23 are designated as the stack. Two bytes are used per CALL allowing up to 8 levels of subroutine nesting.
An extra 256 bytes of RAM may be added and addressed directly using the MOVX instructions.
If more RAM is required, I/O port lines may be used to select additional (256 byte) banks of external memory.

Program counter and stack

The program counter (PC) is a 12-bit counter/register that points to the location from which the next instruction is to be fetched. When EA is logic 0 the PC can address locations 0 to 1023 (8048H), 2047 (8049H) or 4095 (8050H) of internal program memory. At the 1 K (8048H), 2 K (8049H) boundary, an automatic switch-over to external memory occurs. When EA is logic 1 all fetches are from external program memory. The total address space is 4 K bytes. An interrupt or subroutine CALL causes the contents of the program counter to be stored in one of the 8 register pairs of the program counter stack. A 3-bit stack pointer which is part of the program status word (PSW) points to the relevant register pair. Data RAM locations 8 to 23 are available as stack registers and are used to store the program counter and 4 bits of the PSW register. The stack pointer, when initialized to 000, points to RAM locations 8 and 9. The first subroutine jump or interrupt results in the program counter contents being transferred to locations 8 an 9 of the RAM array. The stack pointer is then incremented by one to point to locations 10 and 11. Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111. The end of a subroutine, which is signalled by a return instruction (RET or RETR), causes the stack pointer to be decremented and the contents of the appropriate register pair to be transferred to the program counter.

Oscillator and clock (see Figs 5, 6 and 7)

The MAB80XXH has on-chip oscillator and clock driver circuitry. A crystal, LC-network or external timing signal (pulse generator) determines the oscillator frequency. The output of the oscillator is divided-by-three and is available at T0 (pin 1) by executing the ENT0 CLK instruction. This clock signal (CLK) is divided-by-five to define a machine (instruction) cycle. It is available at ALE (pin 11).



(1) Including crystal-socket stray capacities.

Fig. 5 Crystal oscillator mode. Crystal series impedance should be $< 75\ \Omega$ at 6 MHz and $< 180\ \Omega$ at 3,6 MHz. When using a ceramic oscillator both capacitors should be 30 pF.

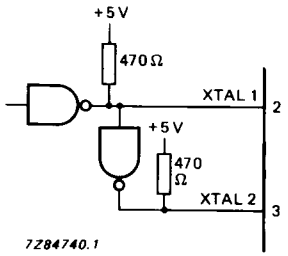
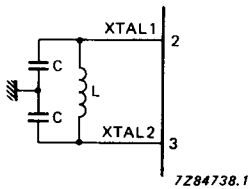


Fig. 6 External clock source. Both XTAL 1 and XTAL 2 should be driven. Resistors to V_{CC} (+ 5 V) are required to ensure V_{IH} = 3,8 V if TTL circuitry is used.
The minimum HIGH and LOW times are 45%.



$$f \approx \frac{1}{2\pi\sqrt{LC'}} \; ; \; C' = \frac{C + 3C_{pp}}{2}$$

L (μH)	C (pF)	nom. f (MHz)
45	20	5,2
120	20	3,2

Fig. 7 LC oscillator. Each capacitor should be ≈ 20 pF including stray capacitance C_{pp} ≈ 5 to 10 pF (pin-to-pin capacitance).

Timer/event counter

An internal counter is available which can count either external events or machine cycles (÷32). The machine cycles are divided-by-32 before they are applied to the input of the 8-bit counter. External events are applied directly to the input of the counter. The maximum clock rate is one third of the machine cycle frequency. The minimum positive duty cycle that can be detected is 0,2 times the cycle period. The counter can be configured to generate an interrupt to the processor when it overflows.

Interrupt

An interrupt may be generated by:

- An external input $\overline{INT}$ (pin 6)
  or
- A timer/counter overflow, when enabled.

In either event, the processor completes execution of the present instruction and then calls the interrupt service routine.
At the end of the interrupt service routine, a RETR instruction restores the machine to the state it was in prior to the interrupt. The external interrupt has priority over the timer/counter interrupt.

Input/output

The MAB80XXH has 27 I/O lines arranged as three 8-bit ports and 3 'test' inputs that can alter program sequences when tested by conditional jump instructions.
Each port line can be individually configured as an input or output.

FUNCTIONAL DESCRIPTION (continued)

Ports 1 and 2 are both 8-bits wide and have identical characteristics. Data written to these ports is latched and remains unchanged until rewritten. In the input mode, these ports are non-latching; inputs must be present until read by an input instruction. Inputs are fully TTL compatible and outputs will drive one standard TTL load.

Ports 1 and 2 are called quasi-bidirectional because they are not high impedance when configured as inputs. Each line is pulled up to + 5 V through a resistor (≈ 50 Ω). This pull-up provides sufficient source current for a TTL HIGH level, yet can be pulled LOW by a standard TTL gate, thus allowing the pin to be used both as an input and an output. To provide fast switching times during a logic 0 - to - 1 transition, transistor TR 2 is switched on for one fifth of a machine cycle when a logic 1 is written to the line. When a logic 0 is written, transistor TR 1 overcomes the pull-up and provides TTL current sinking capability. Since the pull-down transistor is low impedance, a logic 1 must first be written to any line which is to used as an input. $\overline{\text{RESET}}$ initializes all lines to the high impedance logic 1 state. This structure allows input and output on the same pin. Individual port lines can be read and written using the ANL and ORL instructions.

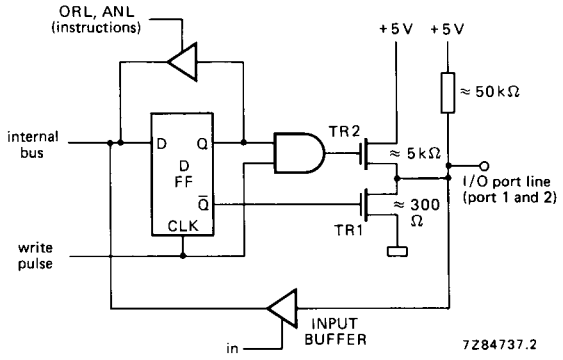
BUS (DB0–DB7)

BUS is a true bidirectional 8-bit port with associated input and output strobes. The BUS port can operate in three different modes: as a latched I/O port, as a bidirectional bus port, or in an expanded system as a program memory address output port. If the bidirectional feature is not needed, BUS can serve as either a statically latched output port or non-latching input port. Input and output lines on this port cannot be mixed. The BUS port lines are either active HIGH, active LOW, or high impedance (floating).

As a static port, data is written and latched using the OUTL instruction and input using the INS in instruction. The INS and OUTL instructions generate pulses on the corresponding $\overline{\text{RD}}$ and $\overline{\text{WR}}$ output strobe lines; however, in the static port mode they are generally not used. As a bidirectional port, the MOVX instructions are used to read and write the port. A write to the port generates a pulse on the $\overline{\text{WR}}$ output line and output data is valid at the trailing edge of $\overline{\text{WR}}$. A read of the port generates a pulse on the $\overline{\text{RD}}$ output line and input data must be valid at the trailing edge of $\overline{\text{RD}}$.

The latched mode (INS, OUTL) is intended for use in the single-chip configuration, where BUS is not being used as an expanded port. OUTL and MOVX instructions can be mixed if required. However, when using a MOVX instruction a previously latched output will be lost and BUS will be left in the high impedance state. INS does not put the BUS in a high impedance state. Therefore, in order to read an external byte (and not the previously latched value) using an INS instruction, it is necessary to precede INS with a MOVX instruction.

OUTL should never be used in a system with external program memory, since latching BUS may cause the next instruction to be incorrectly fetched.



N.B The OUTL, ANL and the ORL instructions relating to BUS are for use with internal program memory only.

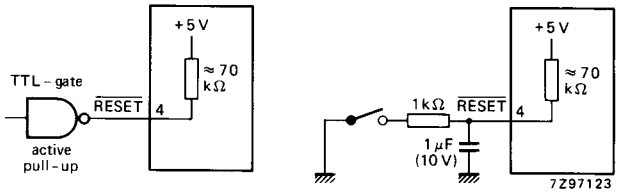
Fig. 8 Quasi-bidirectional port structure.

Test (T0, T1) and $\overline{INT}$

These three pins serve as inputs and may be tested by the conditional jump instruction. They allow inputs to cause program branches without the necessity of loading an input port into the accumulator.

$\overline{RESET}$ (see Fig. 9)

This active LOW input is used to initialize the microcontroller.
This Schmitt-trigger input has an internal pull-up resistor which, in combination with an external 1 μF capacitor, provides an internal reset pulse of sufficient duration to reset all circuitry. If the reset pulse is generated externally, the reset pin must be held at ground (0,45 V) for at least 10 ms after the power supply is within tolerance. Only 5 machine cycles (12,5 μs at 6 MHz) are required if power is already on and the oscillator has stabilized.



(a) (b)

Fig. 9 An external reset is shown in (a) and power-on reset in (b).

Single step ($\overline{SS}$)

This active LOW input when used in combination with ALE will cause the microcontroller to execute a single instruction, then wait until $\overline{SS}$ is reactivated.

Power-down mode (see Fig. 10)

In the MAB80XXH, power can be removed from all but the data RAM array, for low power standby operation. In the power-down mode the contents of the data RAM can be maintained while drawing typically 10% to 15% of the normal operating supply voltage. V_{CC} serves as the + 5 V supply pin for the bulk of the circuitry, while the V_{DD} pin supplies only the RAM array. In normal operation, both pins are at + 5 V. In the standby mode, V_{CC} is at ground and only V_{DD} is maintained at + 5 V. Applying $\overline{RESET}$ to the microcontroller through the reset pin inhibits any access to the RAM and ensures that the RAM cannot be inadvertently altered as power is removed from V_{CC}.

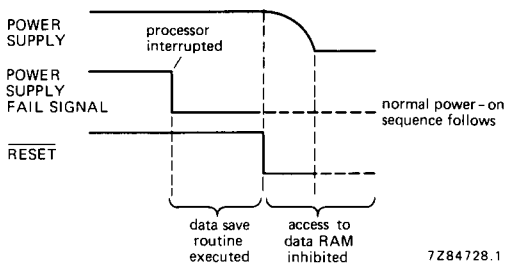


Fig. 10 Power down sequence.

FUNCTIONAL DESCRIPTION (continued)

Instruction set (see Tables 1, 2, 3 and 4)

The MAB80XXH instruction set consists of over 90 one and two-byte instructions. Program code efficiency is high because:

- Working registers and program variables are stored in RAM locations 0 to 127, which require only a single byte to address
- Program memory is divided into pages of 256 bytes, which means that branch destination addresses require only one byte

The instruction set performs logical, arithmetic and test operations on bytes. It also manipulates and tests bits. A set of MOVE instructions operate indirectly on either RAM or ROM, which permits efficient access of pointers and data tables. The indirect jump instruction performs a multi-way branch (up to 256) on the contents of the accumulator to addresses stored in a look-up table. The 'decrement register and jump if not zero' instruction saves a byte each time it is used as opposed to using separate increment and test instructions. The on-chip counter provides the facility for external events or time to be counted by hardware which does not interfere with the main program. The MAB80XXH can either test the counter (under program control) or cause its overflow to generate an interrupt. These features are essential for real-time applications.

Table 1 Symbols and definitions used in Table 2.

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0–7)
RBS	register bank select
C	carry (bit CY)
CNT	event counter
D	mnemonic for 4-bit digit (nibble)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1, 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0–7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0	test 0 input
T1	test 1 input
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

Table 2 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addresses by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) − 1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data	r = 0–7	
	MOV @rR, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((R0_{0-3}))$ $(A_{0-3})\leftrightarrow((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator contents to PSW	(PSW)←(A)		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	(A)←((A))		
	MOVP3 A,@A	E3	1/2	move data in page 3 to A	(A)←((A))	in page 3	

	MOVX A,@Rr	80 81	1/2	move indirect the contents of external memory to A	(A)←((R))	r = 0–1	
	MOVX @Rr,A	90 91	1/2	move indirect the contents of A to external memory	((R))←(A)	r = 0–1	
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
FLAGS	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1	r = 0–7	
REGISTER	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1		
REGISTER	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) −1	r = 0–7	
BRANCH	JMP addr	● 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1		
BRANCH	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))		
BRANCH	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) −1 if (Rr) not zero (PC_{0-7})←addr	r = 0–7	
BRANCH	JF0 addr	B6 address	2/2	jump to addr if F0 = 1	if F0 = 1: (PC_{0-7})←addr		
BRANCH	JF1 addr	76 address	2/2	jump to addr if F1 = 1	if F1 = 1: (PC_{0-7})←addr		
BRANCH	JNI addr	86 address	2/2	jump to addr if $\overline{INT}$ = 0	if $\overline{INT}$ = 0: (PC_{0-7})←addr		
BRANCH	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1: (PC_{0-7})←addr	b = 0–7	
BRANCH	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1: (PC_{0-7})←addr		
BRANCH	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0: (PC_{0-7})←addr		
BRANCH	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0: (PC_{0-7})←addr		
BRANCH	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A ≠0: (PC_{0-7})←addr		
BRANCH	JT0 addr	36 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr		
BRANCH	JNT0 addr	26 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr		
BRANCH	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr		
BRANCH	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr		
BRANCH	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr		4

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	ENT0 CLK	75	1/1	enable clock output onto T0		
SUBROUTINE	CALL addr	▲4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4, 6, 7}$) (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) –1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) –1 ($PSW_{4, 6, 7}$) + (PC)←((SP))	6

INPUT/OUTPUT	OUTL BUS,A	02	1/2	output accumulator to BUS	(BUS)←A		
	IN A,Pp	09 0A	1/2	input port p data to accumulator	(A)←(P1) (A)←(P2)	p = 1–2	7
	INS A,BUS	08	1/2	input strobed BUS data into accumulator	(A)←(BUS)		
	OUTL Pp,A	39 3A	1/2	output accumulator data to port p	(P1)←(A) (P2)←(A)	p = 1–2	
	ANL BUS, # data	98	2/2	logical AND immediate data with BUS	(BUS)←(BUS) AND data		
	ANL Pp, # data	99 9A	2/2	AND port p data with immediate data	(P1)←(P1) AND data (P2)←(P2) AND data	p = 1–2	
	ORL Pp, # data	89 8A	2/2	OR port p data with immediate data	(P1)←(P1) OR data (P2)←(P2) OR data	p = 1–2	
	ORL BUS, # data	88	2/2	logical OR immediate data with BUS	(BUS)←(BUS) OR data		
	MOVD A,Pp	0C 0D 0E 0F	1/2	move contents of designated port (4–7) to A	(A_{0-3})←(Pp) (A_{4-7})←0	p = 4–7	
	MOVD Pp,A	3C 3D 3E 3F	1/1	move contents of A to designated port (4–7)	(Pp)←(A_{0-3})	p = 4–7	
	ANLD Pp,A	9C 9D 9E 9F	1/2	logical AND contents of A with designated port (4–7)	(Pp)←(Pp) AND (A_{0-3})	p = 4–7	
	ORLD Pp,A	8C 8D 8E 8F	1/1	logical OR contents of A with designated port (4–7)	(Pp)←(Pp) OR (A_{0-3})	p = 4–7	
	NOP	00	1/1	no operation			

Notes to Table 2.

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instruction resets the Timer Flag (TF).
5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 111 P23, P22, P21, P20.
8. (S1) has a different meaning for read and write operation, see serial I/O interface.

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

Table 3 Instruction timing (see also Figs 11 and 12)

	cycle 1					cycle 2				
instruction	S1	S2	S3	S4	S5	S1	S2	S3	S4	S5
IN A,P	fetch instruction	increment program counter	–	increment timer	–	–	read port	* –	–	–
OUTL P,A	¦	¦	–	¦	output to port	–	–	* –	–	–
ANL P,#data	¦	* ¦	–	¦	read port	fetch immediate data	–	*increment program counter	output to port	–
ORL P,#data	¦	* ¦	–	¦	read port	fetch immediate data	–	*increment program counter	output to port	–
INS A,BUS	¦	¦	–	¦	–	–	read port	* –	–	–
OUTL BUS,A	¦	¦	–	¦	output to port	–	–	* –	–	–
ANL BUS,#data	¦	* ¦	–	¦	read port	fetch immediate data	–	*increment program counter	output to port	–
ORL BUS,#data	¦	* ¦	–	¦	read port	fetch immediate data	–	*increment program counter	output to port	–
MOVX @R,A	¦	¦	output RAM address	¦	output data to RAM	–	–	* –	–	–
MOVX A,@R	¦	¦	output RAM address	¦	–	–	read data	* –	–	–
MOVD A,P	fetch instruction	increment program counter	output opcode/ address	increment timer	–	–	read P2 lower	* –	–	–

	cycle 1					cycle 2				
instruction	S1	S2	S3	S4	S5	S1	S2	S3	S4	S5
MOVD P,A	fetch instruction	increment program counter	output opcode/ address	increment timer	output data to P2 lower	–	–	* –	–	–
ANLD P,A	¦		output opcode/ address	¦	output data	–	–	* –	–	–
ORLD P,A	¦		output opcode/ address	¦	output data	–	–	* –	–	–
J (conditional)	¦	*	sample condition	increment timer	–	fetch immediate data	–	* opdata program counter	–	–
STRT CNT STRT T	¦	*	–	–	start counter					
STOP TCNT	¦	*	–	–	stop counter					
EN I	¦	*	–	enable interrupt	–					
DIS I	¦	*	–	disable interrupt	–					
ENT0 CLK	fetch instruction	* increment program counter	–	enable clock	–					

* Valid instruction addresses are output at this time if external program memory is being accessed.

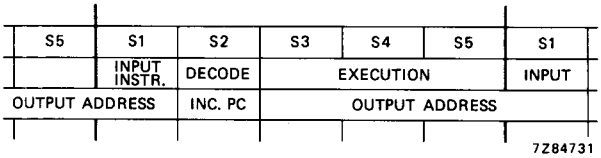


Fig. 11 Instruction cycle.

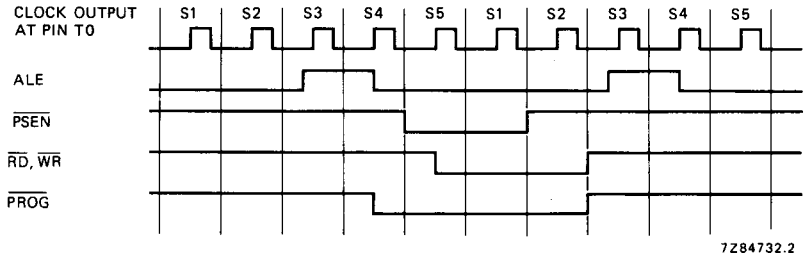


Fig. 12 Instruction cycle timing.

Table 4 Instruction map.

first hexadicimal character of opcode	second hexadicimal character of opcode														
	0 1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	OUTL BUS,A	ADD A, #data	JMP page 0	EN I		DEC A	INS A,BUS	IN A, Pp 1	2		MOVD A,Pp 4	5	6	7
1	INC @Rr 0 1	JB0 addr	ADDC A, #data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	1	2	3	4	5	6	7
2	XCH A, @Rr 0 1		MOV A, #data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr 0	1	2	3	4	5	6	7
3	XCHD A, @Rr 0 1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A		OUTL Pp,A 1	2		MOVD Pp,A 4	5	6	7
4	ORL A, @Rr 0 1	MOV A, T	ORL A, #data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0	1	2	3	4	5	6	7
5	ANL A, @Rr 0 1	JB2 addr	ANL A, #data	CALL page 2	STRT T	JT1 addr	DA, A	ANL A,Rr 0	1	2	3	4	5	6	7
6	ADD A, @Rr 0 1	MOV T,A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0	1	2	3	4	5	6	7
7	ADDC A, @Rr 0 1	JB3 addr		CALL page 3	ENT0 CLK	JF1 addr	RR A	ADDC A,Rr 0	1	2	3	4	5	6	7
8	MOVX A, @Rr 0 1		RET	JMP page 4	CLR F0	JNI addr		ORL BUS, #data	ORL Pp, #data 1	2		ORLD Pp,A 4	5	6	7
9	MOVX @Rr,A 0 1	JB4 addr	RETR	CALL page 4	CPL F0	JNZ addr	CLR C	ANL BUS, #data	ANP Pp, #data 1	2		ANLD Pp,A 4	5	6	7
A	MOV @Rr, A 0 1		MOVP A, @A	JMP page 5	CLR F1		CPL C	MOV Rr,A 0	1	2	3	4	5	6	7
B	MOV @Rr, #data 0 1	JB5 addr	JMPP @A	CALL page 5	CPL F1	JF0 addr		MOV R, #data 0	1	2	3	4	5	6	7
C				JMP page 6	SEL RB0	JZ addr	MOV A, PSW	DEC Rr 0	1	2	3	4	5	6	7
D	XRL A, @Rr 0 1	JB6 addr	XRL A, #data	CALL page 6	SEL RB1		MOV PSW, A	XRL A,Rr 0	1	2	3	4	5	6	7
E			MOVP3 A @A	JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr 0	1	2	3	4	5	6	7
F	MOV A, @Rr 0 1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0	1	2	3	4	5	6	7

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Input voltage with respect to V_{SS}			
except input EA	V_I	−0,5 to + 7	V
input EA	V_I	−0,5 to + 12	V
DC current into any input or output	$\pm I_I, \pm I_O$	max. 10	mA
Total power dissipation	P_{tot}	max. 1	W
Storage temperature range	T_{stg}	−65 to +150	°C
Operating ambient temperature range	T_{amb}	see Table 5	

Table 5 MAB80XXH versions.

version	internal memory		RAM st/by.	frequency (MHz)		temperature range (°C)
				min.	max.	
MAB8048H	1 K x 8 ROM	64 byte RAM	yes	1,0	11,0	0 to +70
MAB8035HL	none	64 byte RAM	yes	1,0	11,0	0 to +70
MAF8048H	1 K x 8 ROM	64 byte RAM	yes	1,0	11,0	−40 to +85
MAF8035HL	none	64 byte RAM	yes	1,0	11,0	−40 to +85
MAF80A48H	1 K x 8 ROM	64 byte RAM	yes	1,0	10,0	−40 to +110
MAF80A35HL	none	64 byte RAM	yes	1,0	10,0	−40 to +110
MAB8049H	2 K x 8 ROM	128 byte RAM	yes	1,0	11,0	0 to +70
MAB8039HL	none	128 byte RAM	yes	1,0	11,0	0 to +70
MAF8049H	2 K x 8 ROM	128 byte RAM	yes	1,0	11,0	−40 to +85
MAF8039HL	none	128 byte RAM	yes	1,0	11,0	−40 to +85
MAF80A49H	2 K x 8 ROM	128 byte RAM	yes	1,0	10,0	−40 to +110
MAF80A39HL	none	128 byte RAM	yes	1,0	10,0	−40 to +110
MAB8050H	4 K x 8 ROM	256 byte RAM	yes	1,0	11,0	0 to +70
MAB8040HL	none	256 byte RAM	yes	1,0	11,0	0 to +70
MAF8050H	4 K x 8 ROM	256 byte RAM	yes	1,0	11,0	−40 to +85
MAF8040HL	none	256 byte RAM	yes	1,0	11,0	−40 to +85
MAF80A50H	4 K x 8 ROM	256 byte RAM	yes	1,0	10,0	−40 to +110
MAF80A40HL	none	256 byte RAM	yes	1,0	10,0	−40 to +110

DC CHARACTERISTICS (MAB8048H/35HL; MAB8049H/39HL; MAB8050H/40HL)

$V_{CC} = V_{DD} = 5$ V (± 10%); $V_{SS} = 0$ V; $T_{amb} = 0$ to + 70 °C; all voltages with respect to V_{SS} unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current at $V_{DD} = 5$ V ± 10%; $V_{SS} = V_{CC} = 0$ V					
MAB8048H/35HL	I_{DD}	–	–	6	mA
MAB8049H/39HL	I_{DD}	–	–	8	mA
MAB8050H/40HL	I_{DD}	–	–	15	mA
Supply current (total) at $V_{DD} = V_{CC} = 5$ V ± 10%; $V_{SS} = 0$ V					
MAB8048H/35HL	$I_{DD} + I_{CC}$	–	–	80	mA
MAB8049H/39HL	$I_{DD} + I_{CC}$	–	–	90	mA
MAB8050H/40HL	$I_{DD} + I_{CC}$	–	–	100	mA
Inputs					
Input voltage LOW all inputs except XTAL 1, XTAL 2, $\overline{\text{RESET}}$	V_{IL}	−0,5	–	0,8	V
Input voltage LOW XTAL 1, XTAL 2, $\overline{\text{RESET}}$	V_{IL1}	−0,5	–	0,6	V
Input voltage HIGH all inputs except XTAL 1, XTAL 2, $\overline{\text{RESET}}$	V_{IH}	2,0	–	V_{CC}	V
Input voltage HIGH XTAL 1, XTAL 2, $\overline{\text{RESET}}$	V_{IH1}	3,8	–	V_{CC}	V
Outputs					
Output voltage LOW (DB0 to DB7) at $I_{OL} = 2$ mA	V_{OL}	–	–	0,45	V
Output voltage LOW ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE) at $I_{OL1} = 1{,}8$ mA	V_{OL1}	–	–	0,45	V
Output voltage LOW ($\overline{\text{PROG}}$) at $I_{OL2} = 1$ mA	V_{OL2}	–	–	0,45	V
Output voltage LOW (all other outputs) at $I_{OL3} = 1{,}6$ mA	V_{OL3}	–	–	0,45	V
Output voltage HIGH (DB0 to DB7) at $-I_{OH} = 400\ \mu$A	V_{OH}	2,4	–	–	V
Output voltage HIGH ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE) at $-I_{OH1} = 100\ \mu$A	V_{OH1}	2,4	–	–	V
Output voltage HIGH (all other outputs) at $-I_{OH} = 40\ \mu$A	V_{OH2}	2,4	–	–	V

DC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Input leakage current (T1, $\overline{INT}$) at $V_{SS} < V_I < V_{CC}$	$\pm I_{IL}$	–	–	10	μA
Output leakage current (DB0 to DB7, T0; high impedance) at $V_{SS} + 0{,}45\ V < V_I < V_{CC}$	$\pm I_{OZ}$	–	–	10	μA
Input load current (P1.0 to P1.7, P2.0 to P2.7, EA, $\overline{SS}$) at $V_{SS} + 0{,}45\ V < V_I < V_{CC}$	$-I_{LI}$	–	–	500	μA
Input load current ($\overline{RESET}$) at $V_{SS} < V_I < V_{CC}$	$-I_{LI1}$	20	–	300	μA

DC CHARACTERISTICS

MAF8048H/35HL; MAF8049H/39HL; MAF8050H/40HL (at $T_{amb} = -40$ to $+85\ ^oC$)
MAF80A48H/A35HL; MAF80A49H/A39HL; MAF80A50H/A40HL (at $T_{amb} = -40$ to $+110\ ^oC$)

$V_{CC} = V_{DD} = 5\ V\ (\pm 10\%)$; $V_{SS} = 0\ V$; T_{amb} as above; all voltages with respect to V_{SS} unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current at $V_{DD} = 5\ V \pm 10\%$; $V_{SS} = V_{CC} = 0\ V$					
MAF8048H/35HL; MAF80A48H/A35HL	I_{DD}	–	–	8	mA
MAF8049H/39HL; MAF80A49H/A39HL	I_{DD}	–	–	10	mA
MAF8050H/40HL; MAF80A50H/A40HL	I_{DD}	–	–	18	mA
Supply current (total) at $V_{DD} = V_{CC} = 5\ V \pm 10\%$; $V_{SS} = 0\ V$					
MAF8048H/35HL; MAF80A48H/A35HL	$I_{DD} + I_{CC}$	–	–	90	mA
MAF8049H/39HL; MAF80A49H/A39HL	$I_{DD} + I_{CC}$	–	–	100	mA
MAF8050H/40HL; MAF80A50H/A40HL	$I_{DD} + I_{CC}$	–	–	120	mA
Inputs					
Input voltage HIGH all inputs except XTAL 1, XTAL 2, $\overline{RESET}$	V_{IH}	2,2	–	V_{CC}	V
Input load current (P1.0 to P1.7, P2.0 to P2.7, EA, $\overline{SS}$) at $V_{SS} + 0{,}45\ V < V_I < V_{CC}$	$-I_{LI}$	–	–	0,6	mA

AC CHARACTERISTICS (MAB8048H/35HL; MAB8049H/39HL; MAB8050H/40HL)

$V_{CC} = V_{DD} = 5$ V (± 10%); $V_{SS} = 0$ V; $T_{amb} = 0$ to + 70 °C; note 1.
See waveforms Figs 14, 15, 16, 17 and 18

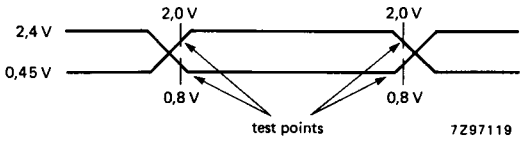
parameter	symbol	f(t_{CL}) (note 2)	11 MHz		unit
			min.	max.	
Clock period (note 2)	t_{CL}	$1/(f_{XTAL})$	90,9	1000	ns
ALE pulse duration	t_{LL}	$3{,}5t_{CL}-170$	150	–	ns
Address set-up time to ALE (note 3)	t_{AL}	$2t_{CL}-110$	70	–	ns
Address hold time after ALE	t_{LA}	$t_{CL}-40$	50	–	ns
Control pulse duration $\overline{RD}$, $\overline{WR}$	t_{CC1}	$7{,}5t_{CL}-200$	480	–	ns
Control pulse duration $\overline{PSEN}$	t_{CC2}	$6t_{CL}-200$	350	–	ns
Data set-up time before $\overline{WR}$	t_{DW}	$6{,}5t_{CL}-200$	390	–	ns
Data set-up time after $\overline{WR}$	t_{WD}	$t_{CL}-50$	40	–	ns
Data hold time					
$\overline{RD}$, $\overline{PSEN}$	t_{DR}	$1{,}5t_{CL}-30$	0	110	ns
$\overline{RD}$ to data input	t_{RD1}	$6t_{CL}-170$	–	350	ns
$\overline{PSEN}$ to data input	t_{RD2}	$4{,}5t_{CL}-170$	–	190	ns
Address set-up time to $\overline{WR}$	t_{AW}	$5t_{CL}-150$	300	–	ns
Address set-up time to data input ($\overline{RD}$)	t_{AD1}	$10{,}5t_{CL}-220$	–	730	ns
Address set-up time to data input ($\overline{PSEN}$)	t_{AD2}	$7{,}5t_{CL}-200$	–	460	ns
Address floating to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	$2t_{CL}-40$	140	–	ns
Address floating to $\overline{PSEN}$ (note 3)	t_{AFC2}	$0{,}5t_{CL}-40$	10	–	ns
ALE to control pulse $\overline{RD}$, $\overline{WR}$	t_{LAFC1}	$3t_{CL}-75$	200	–	ns
ALE to control pulse $\overline{PSEN}$	t_{LAFC2}	$1{,}5t_{CL}-75$	60	–	ns
Control pulse to ALE $\overline{RD}$, $\overline{WR}$, $\overline{PROG}$	t_{CA1}	$t_{CL}-40$	50	–	ns
Control pulse to ALE $\overline{PSEN}$	t_{CA2}	$4t_{CL}-40$	320	–	ns
Port control set-up to $\overline{PROG}$	t_{CP}	$1{,}5t_{CL}-80$	50	–	ns
Port control hold to $\overline{PROG}$	t_{PC}	$4t_{CL}-260$	100	–	ns
$\overline{PROG}$ to Port 2 input must be valid	t_{PR}	$8{,}5t_{CL}-120$	–	650	ns
Input data hold time from $\overline{PROG}$	t_{PF}	$1{,}5t_{CL}$	0	150	ns
Output data set-up time	t_{DP}	$6t_{CL}-290$	250	140	ns
Output data hold time	t_{PD}	$1{,}5t_{CL}-90$	40	–	ns
$\overline{PROG}$ pulse duration	t_{PP}	$10{,}5t_{CL}-250$	700	–	ns
Port 2 I/O data set-up time to ALE	t_{PL}	$4t_{CL}-200$	160	–	ns
Port 2 I/O data hold time to ALE	t_{LP}	$1{,}5t_{CL}-120$	15	–	ns

AC CHARACTERISTICS (continued)

parameter	symbol	$f(t_{CL})$ (note 2)	11 MHz		unit
			min.	max.	
Port output from ALE	t_{PV}	$4{,}5t_{CL}+100$	–	510	ns
T0 repetition rate	t_{0PRR}	$3t_{CL}$	270	–	ns
Cycle time	t_{CY}	$15/f_{XTAL}$	1,36	15	μs
MAF8048H/35HL; MAF8049H/39HL; MAF8050H/40HL					
Clock period (note 2)	t_{CL}	$1/(f_{XTAL})$	90,8	1000	ns

Notes to AC characteristics

1. Control outputs: C_L = 80 pF.
   Bus outputs: C_L = 150 pF.
2. $f(t_{CL})$ assumes 50% duty cycle on XTAL 1 and XTAL 2; minimum frequency = 1 MHz.
3. Bus high-impedance load: 20 pF.



A.C. testing inputs are driven at 2,4 V for a logic 1 and 0,45 V for a logic 0. Output timing measurements are taken 2,0 V for a logic 1 and 0,8 V for a logic 0.

Fig. 13 A.C. testing input, output waveform.

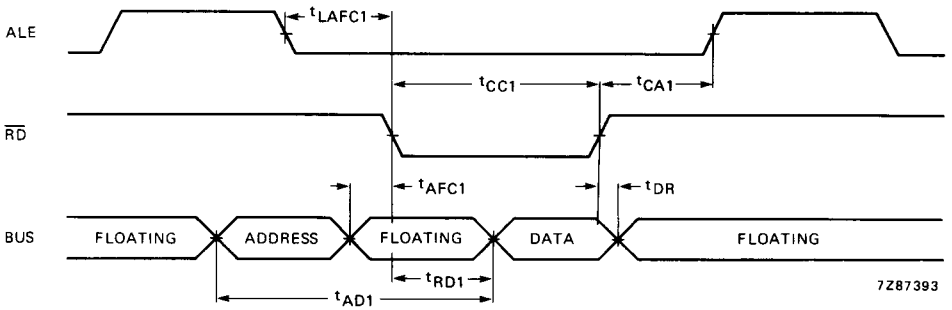


Fig. 14 Read from external data memory.

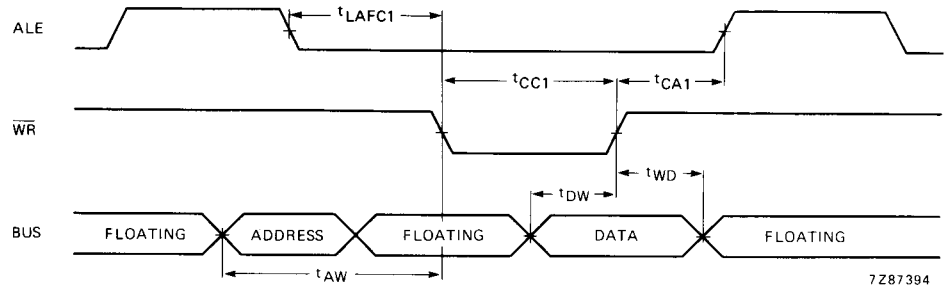


Fig. 15 Write to external memory.

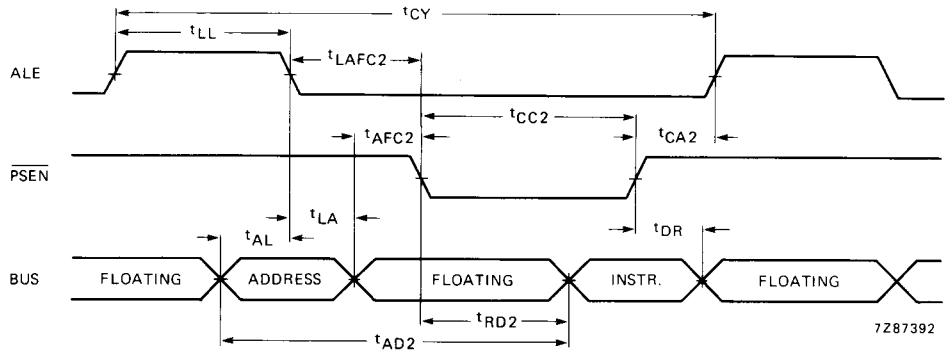


Fig. 16 Instruction fetch from program memory.

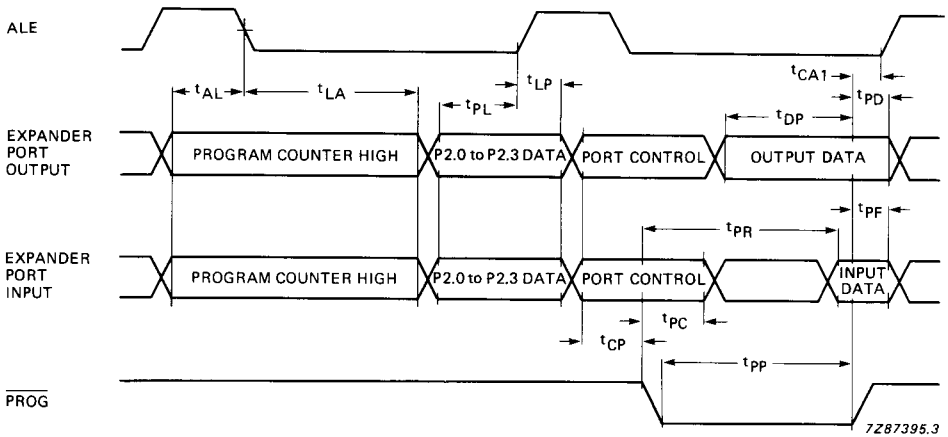


Fig. 17 Port 2 timing.

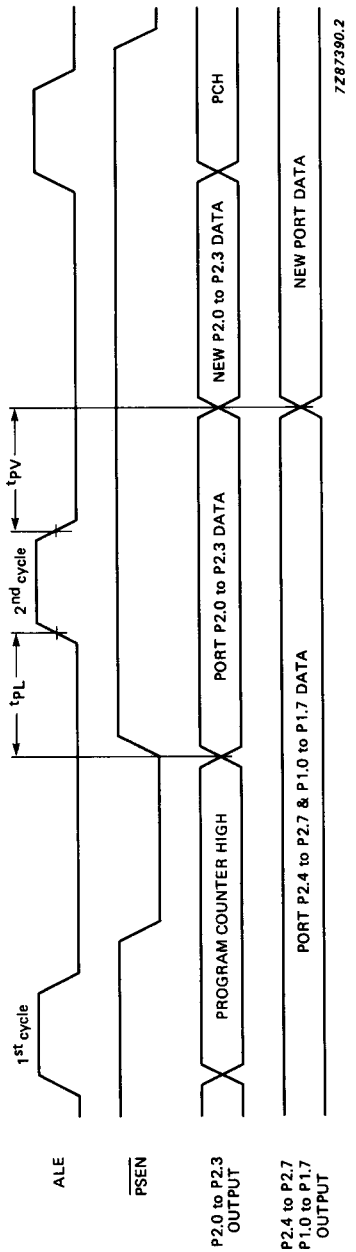


Fig. 18 I/O port timing.