Description

The μPD8086 is a 16-bit microprocessor that has both 8-bit and 16-bit attributes. It has a 16-bit wide physical path to memory for high performance. Its architecture allows higher throughput than the 5 MHz μPD8085A-2.

The maximum operating frequency of the μPD8086 is 5 MHz. The μPD8086-2 is an 8-MHz version.

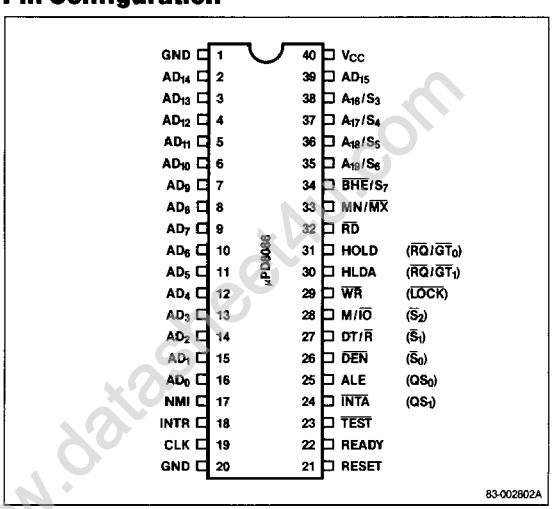
Features

- ☐ Can directly address 1 megabyte of memory
- ☐ Fourteen 16-bit registers with symmetrical operations
- ☐ Bit, byte, word, and block operations
- ☐ 8- and 16-bit signed and unsigned binary or decimal arithmetic operations
- ☐ Multiply and divide instructions
- ☐ 24 operand addressing modes
- ☐ Assembly language compatible with the μPD8080/8085
- ☐ Complete family of components for design flexibility

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD8086D	40-pin ceramic DIP	5 MHz
μPD8086D	40-pin cerdip	5 MHz
μPD8086D-2	40-pin cerdip	8 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 20	GND	Ground
2–16, 39	AD_0–AD_{15}	Address / data bus
17	NMI	Non-maskable interrupt
18	INTR	Interrupt request
19	CLK	Clock
21	RESET	Reset
22	READY	Ready
23	$\overline{TEST}$	Test
24	$\overline{INTA}$	Interrupt acknowledge
25	ALE	Address latch enable
26	$\overline{DEN}$	Data enable
27	DT / $\overline{R}$	Data transmit / receive
28	M / $\overline{IO}$	Memory / IO status
29	$\overline{WR}$	Write
30	HLDA	Hold acknowledge
31	HOLD	Hold
32	$\overline{RD}$	Read
33	MN / $\overline{MX}$	Minimum / maximum
34	$\overline{BHE}$ / S_7	Bus / high enable
35–38	A_{16}–A_{19}	Most significant address bits
26–28, 34–38	S_0–S_7	Status outputs
24, 25	QS_1, QS_0	Queue status
29	$\overline{LOCK}$	Lock
30, 31	$\overline{RQ}$ / $\overline{GT}_0$ $\overline{RQ}$ / $\overline{GT}_1$	Request / grant
40	V_{CC}	Power supply

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Pin Functions

Ground

Ground.

Address/Data Bus

Multiplexed address (T1) and data (T2, T3, TW, T4) bus. 8-bit peripherals tied to the lower 8 bits use A_0 to condition chip select functions. These lines are three-state during interrupt acknowledge and hold states.

Non-Maskable Interrupt

This is an edge-triggered input causing a type 2 interrupt. A look-up table is used by the processor for vectoring information.

Interrupt Request

A level-triggered input sampled on the last clock cycle of each instruction. Vectoring is via an interrupt look-up table. INTR can mask in software by resetting the interrupt enable bit.

Clock

The clock input is a 1/3 duty cycle input basic timing for the processor and bus controller.

Reset

This active high signal must be high for 4 clock cycles. When it returns low, the processor restarts execution.

Ready

An acknowledgement from memory or I/O that data will be transferred. Synchronization is done by the μPD8284 clock generator.

Test

This input is examined by the WAIT instruction, and if low, execution continues. Otherwise the processor waits in an idle state. Synchronized by the processor on the leading edge of CLK.

Interrupt Acknowledge

This is a read strobe for reading vectoring information. During T2, T3, and TW of each interrupt acknowledge cycle it is low.

Address Latch Enable

This is used in conjunction with the μPD8282/8283 latches to latch the address, during T1 of any bus cycle.

Data Enable

This is the output enable for the μPD8282/8287 transceivers. It is active low during each memory and I/O access and $\overline{\text{INTA}}$ cycles.

Data Transmit/Receive

Used to control the direction of data flow through the transceivers.

Memory/IO Status

This is used to separate memory access from I/O access.

Write

Depending on the state of the M/$\overline{\text{IO}}$ line, the processor is either writing to I/O or memory.

Hold Acknowledge

A response to the HOLD input, causing the processor to three-state the local bus. The bus becomes active one cycle after HOLD goes low again.

Hold

When another device requests the local bus, driving HOLD high will cause the μPD8086 to issue a HLDA.

Read

Depending on the state of the M/$\overline{\text{IO}}$ line, the processor is reading from either memory or I/O.

Minimum/Maximum

This input is to tell the processor which mode it is to be used in. This effects some of the pin descriptions.

Bus/High Enable

This is used in conjunction with the most significant half of the data bus. Peripheral devices on this half of the bus use $\overline{\text{BHE}}$ to condition chip select functions.

Most Significant Address Bits

These are the four most significant address bits for memory operations. Low during I/O operations.

Status Outputs

These are the status outputs from the processor. They are used by the μPD8288 to generate bus control signals.

Queue Status

Used to track the internal μPD8086 instruction queue.

Lock

This output is set by the LOCK instruction to prevent other system bus masters from gaining control.

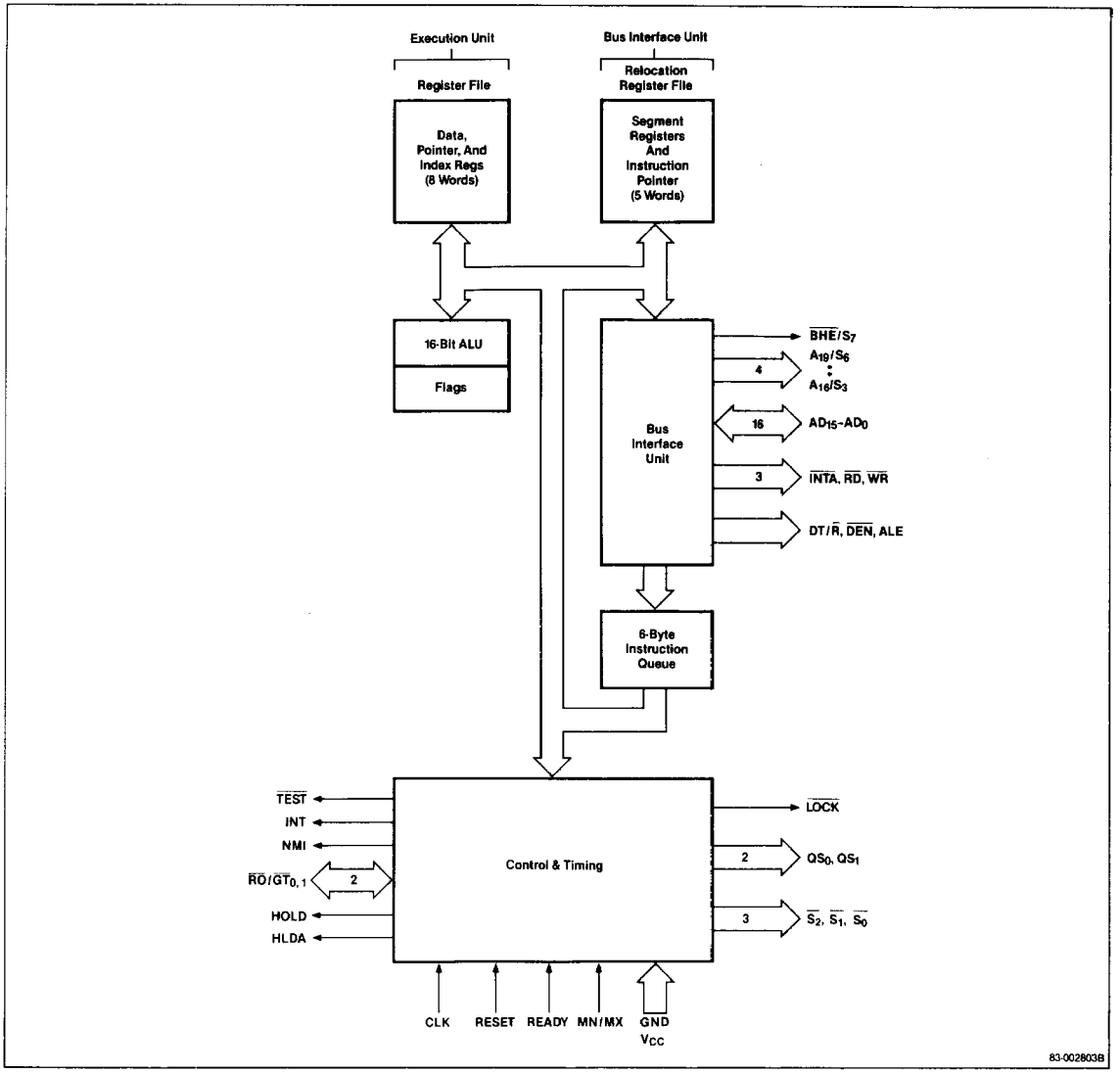
Request/Grant

Other local bus masters can force the processor to rebase the local bus at the end of the current bus cycle.

V_{CC}

This is the +5 V power supply.

Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{CC}	−1.0 V to +7 V
Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Power dissipation, P_D	2.5 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$f_c = 1.0$ MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	(Note 1)
I/O capacitance	C_{IO}			15	pF	(Note 2)

Note:
(1) All input pins except AD_0-AD_{15} and $\overline{RQ}/\overline{GT}$.
(2) Only input pins AD_0-AD_{15} and $\overline{RQ}/\overline{GT}$.

DC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.5		+0.8	V	
Input voltage high	V_{IH}	2		$V_{CC}+0.5$	V	
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 2.5$ mA
Output voltage high	V_{OH}	2.4			V	$I_{OH} = -400\,\mu A$
Input clock voltage low	V_{CL}	−0.5		+0.6	V	
Output clock voltage high	V_{CH}	3.9		$V_{CC}+1.0$	V	
Input leakage current	I_{LI}			±10	μA	$0\,V < V_{IN} < V_{CC}$
Output leakage current	I_{LO}			±10	μA	$0.45\,V \leq V_{OUT} \leq V_{CC}$
Power supply current μPD8086/	I_{CC}			340	mA	$T_A = 25°C$
μPD8086-2				350	mA	$T_A = 25°C$

AC Characteristics

Minimum Complexity System

μPD8086: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits μPD8086 Min	μPD8086 Max	μPD8086-2 Min	μPD8086-2 Max	Unit	Test Conditions
CLK cycle period	t_{CLCL}	200	500	125	500	ns	
CLK low time	t_{CLCH}	$(2/3\,t_{CLCL})-15$		$(2/3\,t_{CLCL})-15$		ns	
CLK high time	t_{CHCL}	$(1/3\,t_{CLCL})+2$		$(1/3\,t_{CLCL})+2$		ns	
CLK rise time	t_{CH1CH2}		10		10	ns	From 1.0 V to 3.5 V
CLK fall time	t_{CL2CL1}		10		10	ns	From 3.5 V to 1.0 V
Data in setup time	t_{DVCL}	30		20		ns	
Data in hold time	t_{CLDX}	10		10		ns	
READY setup time into μPD8284	t_{R1VCL}	35		35		ns	(Notes 1 & 2)
READY hold time into μPD8284	t_{CLR1X}	0		0		ns	(Notes 1 & 2)
READY setup time into μPD8086	t_{RYHCH}	$(2/3\,t_{CLCL})-15$		$(2/3\,t_{CLCL})-15$		ns	
READY hold time into μPD8086	t_{CHRYX}	30		20		ns	
READY inactive to CLK	t_{RYLCL}	−8		−8		ns	(Note 3)
HOLD setup time	t_{HVCH}	35		20		ns	
INTR, NMI, $\overline{TEST}$ setup time	t_{INVCH}	30		15		ns	(Note 2)
Input rise time	t_{ILIH}		20		20	ns	From 0.8 V to 2.0 V
Input fall time	t_{IHIL}		12		12	ns	From 2.0 V to 0.8 V

AC Characteristics (cont)

Timing Responses

μPD8086: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits μPD8086 Min	Limits μPD8086 Max	Limits μPD8086-2 Min	Limits μPD8086-2 Max	Unit	Test Conditions
Address valid delay	t_{CLAV}	10	110	10	60	ns	(Note 4)
Address hold time	t_{CLAX}	10		10		ns	(Note 4)
Address float delay	t_{CLAZ}	t_{CLAX}	80	t_{CLAX}	50	ns	(Note 4)
ALE width	t_{LHLL}	$t_{CLCH}-20$		$t_{CLCH}-10$		ns	(Note 4)
ALE active delay	t_{CLLH}		80		50	ns	(Note 4)
ALE inactive delay	t_{CHLL}		85		55	ns	(Note 4)
Address hold time to ALE inactive	t_{LLAX}	$t_{CHCL}-10$		$t_{CHCL}-10$		ns	(Note 4)
Data valid delay	t_{CLDV}	10	110	10	60	ns	(Note 4)
Data hold time	t_{CHDX}	10		10		ns	(Note 4)
Data hold time after WR	t_{WHDX}	$t_{CLCH}-30$		$t_{CLCH}-30$		ns	(Note 4)
Control active delay 1	t_{CVCTV}	10	110	10	70	ns	(Note 4)
Control active delay 2	t_{CHCTV}	10	110	10	60	ns	(Note 4)
Control active delay	t_{CVCTX}	10	110	10	70	ns	(Note 4)
Address float to READ active	t_{AZRL}	0		0		ns	(Note 4)
$\overline{RD}$ active delay	t_{CLRL}	10	165	10	80	ns	(Note 4)
$\overline{RD}$ inactive delay	t_{CLRH}	10	150	10	80	ns	(Note 4)
$\overline{RD}$ inactive to next address active	t_{RHAV}	$t_{CLCL}-45$		$t_{CLCL}-40$		ns	(Note 4)
HLDA valid delay	t_{CLHAV}	10	160	10	100	ns	(Note 4)
$\overline{RD}$ width	t_{RLRH}	$2t_{CLCL}-75$		$2t_{CLCL}-50$		ns	(Note 4)
$\overline{WR}$ width	t_{WLWH}	$2t_{CLCL}-60$		$2t_{CLCL}-40$		ns	(Note 4)
Address valid to ALE low	t_{AVAL}	$t_{CLCH}-60$		$t_{CLCH}-40$		ns	(Note 4)
Output rise time	t_{OLOH}		20		20	ns	From 0.8 V to 2.0 V
Output fall time	t_{OHOL}		12		12	ns	From 2.0 V to 0.8 V

Note:

(1) Signal at μPD8284 shown for reference only.

(2) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

(3) Applies only to T2 state. (8 ns into T3)

(4) $C_L = 20$–100 pF for all μPD8086 outputs (in addition to μPD8086 self-load).

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AC Characteristics (cont)

Maximum Mode System with μPB8288 Bus Controller

μPD8086: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\,V \pm 10\%$

		Limits					
		μPD8086		μPD8086-2			Test
Parameter	Symbol	Min	Max	Min	Max	Unit	Conditions
CLK cycle period	t_{CLCL}	200	500	125	500	ns	
CLK low time	t_{CLCH}	$(2/3\,t_{CLCL})-15$		$(2/3\,t_{CLCL})-15$		ns	
CLK high time	t_{CHCL}	$(1/3\,t_{CLCL})+2$		$(1/3\,t_{CLCL})+2$		ns	
CLK rise time	t_{CH1CH2}		10		10	ns	From 1.0 V to 3.5 V
CLK fall time	t_{CL2CL1}		10		10	ns	From 3.5 V to 1.0 V
Data in setup time	t_{DVCL}	30		20		ns	
Data in hold time	t_{CLDX}	10		10		ns	
READY setup time into μPD8284	t_{R1VCL}	35		35		ns	(Notes 1 & 2)
READY hold time into μPD8284	t_{CLR1X}	0		0		ns	(Notes 1 & 2)
READY setup time into μPD8086	t_{RYHCH}	$(2/3\,t_{CLCL})-15$		$(2/3\,t_{CLCL})-15$		ns	
READY hold time into μPD8086	t_{CHRYX}	30		20		ns	
READY inactive to CLK	t_{RYLCL}	−8		−8		ns	(Note 5)
INTR, NMI, $\overline{TEST}$ setup time	t_{INVCH}	30		15		ns	(Note 2)
$\overline{RQ}$ / $\overline{GT}$ setup time	t_{GVCH}	30		15		ns	
$\overline{RQ}$ hold time into μPD8086	t_{CHGX}	40		30		ns	
Input rise time	t_{ILIH}		20		20	ns	From 0.8 V to 2.0 V
Input fall time	t_{IHIL}		12		12	ns	From 2.0 V to 0.8 V

AC Characteristics (cont)

Timing Responses

μPD8086: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits μPD8086 Min	Limits μPD8086 Max	Limits μPD8086-2 Min	Limits μPD8086-2 Max	Unit	Test Conditions
Command active delay	t_{CLML}	10	35	10	35	ns	(Notes 1 & 4)
Command inactive delay	t_{CLMH}	10	35	10	35	ns	(Notes 1 & 4)
READY active to status passive	t_{RYHSH}		110		65	ns	(Notes 3 & 4)
Status active delay	t_{CHSV}	10	110	10	60	ns	(Note 4)
Status inactive delay	t_{CLSH}	10	130	10	70	ns	(Note 4)
Address valid delay	t_{CLAV}	10	110	10	60	ns	(Note 4)
Address hold time	t_{CLAX}	10		10		ns	(Note 4)
Address float delay	t_{CLAZ}	t_{CLAX}	80	t_{CLAX}	50	ns	(Note 4)
Status valid to ALE high	t_{SVLH}		15		15	ns	(Notes 1 & 4)
Status valid to MCE high	t_{SVMCH}		15		15	ns	(Notes 1 & 4)
CLK low to ALE valid	t_{CLLH}		15		15	ns	(Notes 1 & 4)
CLK low to MCE high	t_{CLMCH}		15		15	ns	(Notes 1 & 4)
ALE inactive delay	t_{CHLL}		15		15	ns	(Notes 1 & 4)
MCE inactive delay	t_{CLMCL}		15		15	ns	(Notes 1 & 4)
Data valid delay	t_{CLDV}	10	110	10	60	ns	(Note 4)
Data hold time	t_{CHDX}	10		10		ns	(Note 4)
Control active delay	t_{CVNV}	5	45	5	45	ns	(Notes 1 & 4)
Control inactive delay	t_{CVNX}	10	45	10	45	ns	(Notes 1 & 4)
Address float to READ active	t_{AZRL}	0		0		ns	(Note 4)
$\overline{RD}$ active delay	t_{CLRL}	10	165	10	100	ns	(Note 4)
$\overline{RD}$ inactive delay	t_{CLRH}	10	150	10	80	ns	(Note 4)
$\overline{RD}$ inactive to next address active	t_{RHAV}	$t_{CLCL} - 45$		$t_{CLCL} - 40$		ns	(Note 4)
Direction control active delay	t_{CHDTL}		50		50	ns	(Notes 1 & 4)
Direction control inactive delay	t_{CHDTH}		30		30	ns	(Notes 1 & 4)
$\overline{GT}$ active delay	t_{CLGL}	0	85	0	50	ns	(Note 4)
$\overline{GT}$ inactive delay	t_{CLGH}	0	85	0	50	ns	(Note 4)
$\overline{RD}$ width	t_{RLRH}	$2t_{CLCL} - 50$		$2t_{CLCL} - 50$		ns	(Note 4)
Output rise time	t_{OLOH}		20		20	ns	From 0.8 V to 2.0 V
Output fall time	t_{OHOL}		12		12	ns	From 2.0 V to 0.8 V

Note:

(1) Signal at μPB8284 or μPB8288 shown for reference only.

(2) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

(3) Applies only to T3 and wait states.

(4) $C_L = 20$-100 pF for all μPD8086 outputs (in addition to μPD8086 self-load).

(5) Applies only to T2 state. (8 ns into T3).

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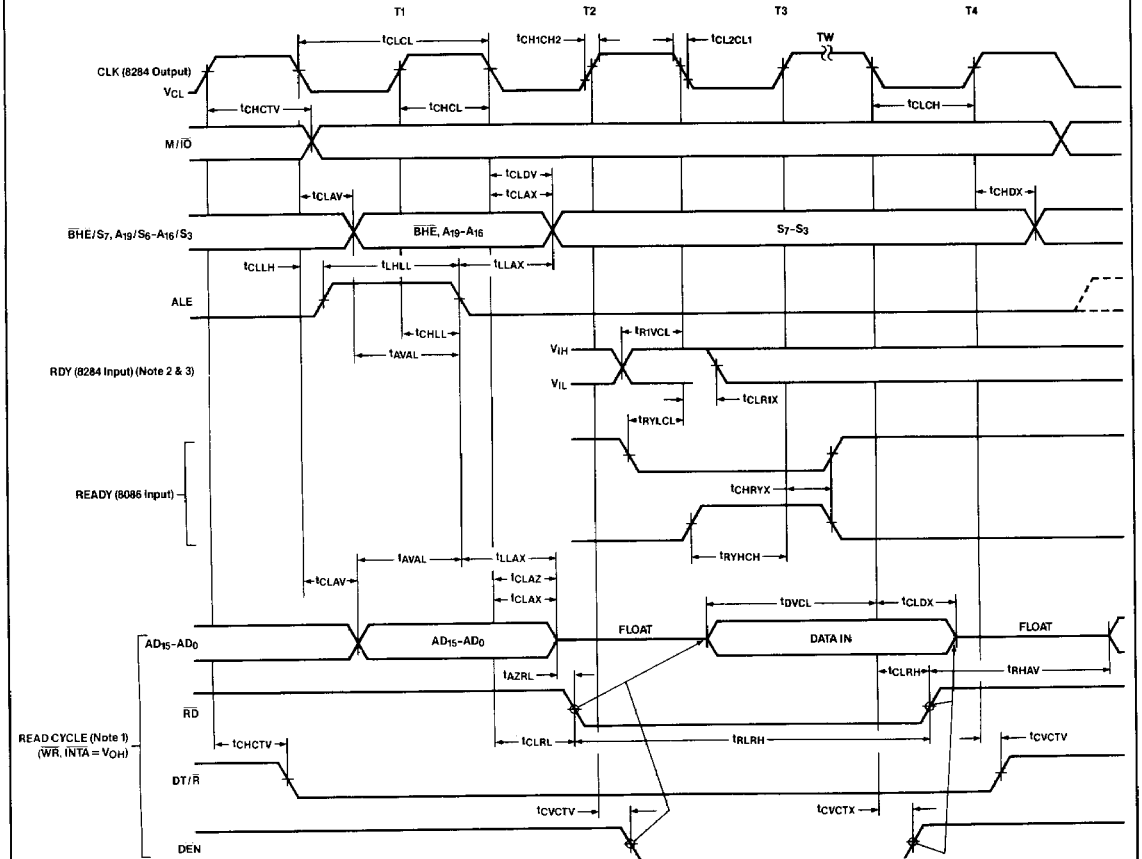
AC Timing Waveforms

Minimum Complexity Systems (Note 4)



Note:
(1) All signals switch between V_{OH} and V_{OL} unless otherwise specified.
(2) RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
(3) Signals at μPD8284 are shown for reference only.
(4) All timing measurements are made at 1.5 V unless otherwise noted.

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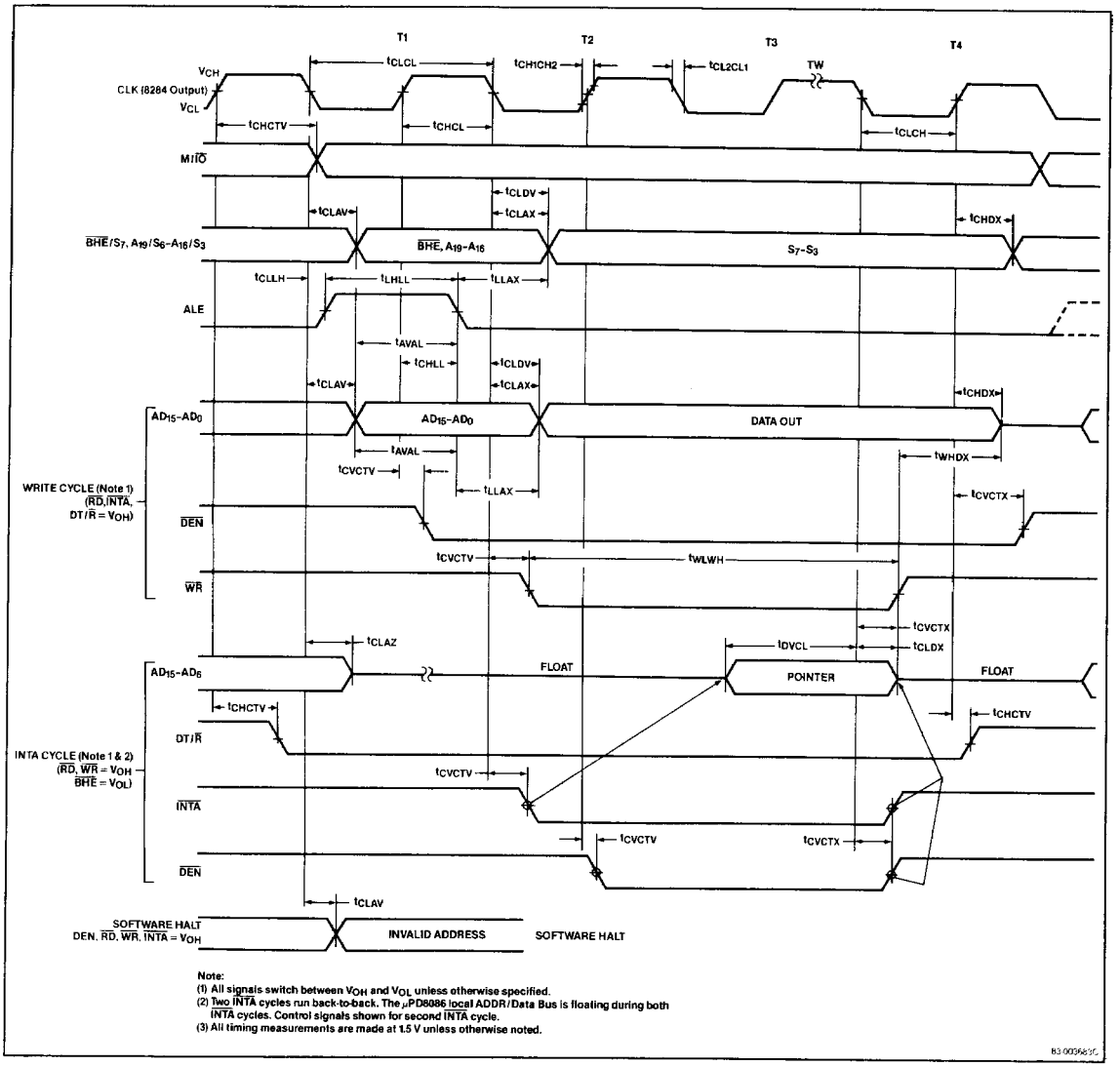
AC Timing Waveforms (cont)

Minimum Complexity Systems (Note 3)



Note:
(1) All signals switch between V_{OH} and V_{OL} unless otherwise specified.
(2) Two $\overline{INTA}$ cycles run back-to-back. The μPD8086 local ADDR/Data Bus is floating during both $\overline{INTA}$ cycles. Control signals shown for second $\overline{INTA}$ cycle.
(3) All timing measurements are made at 1.5 V unless otherwise noted.

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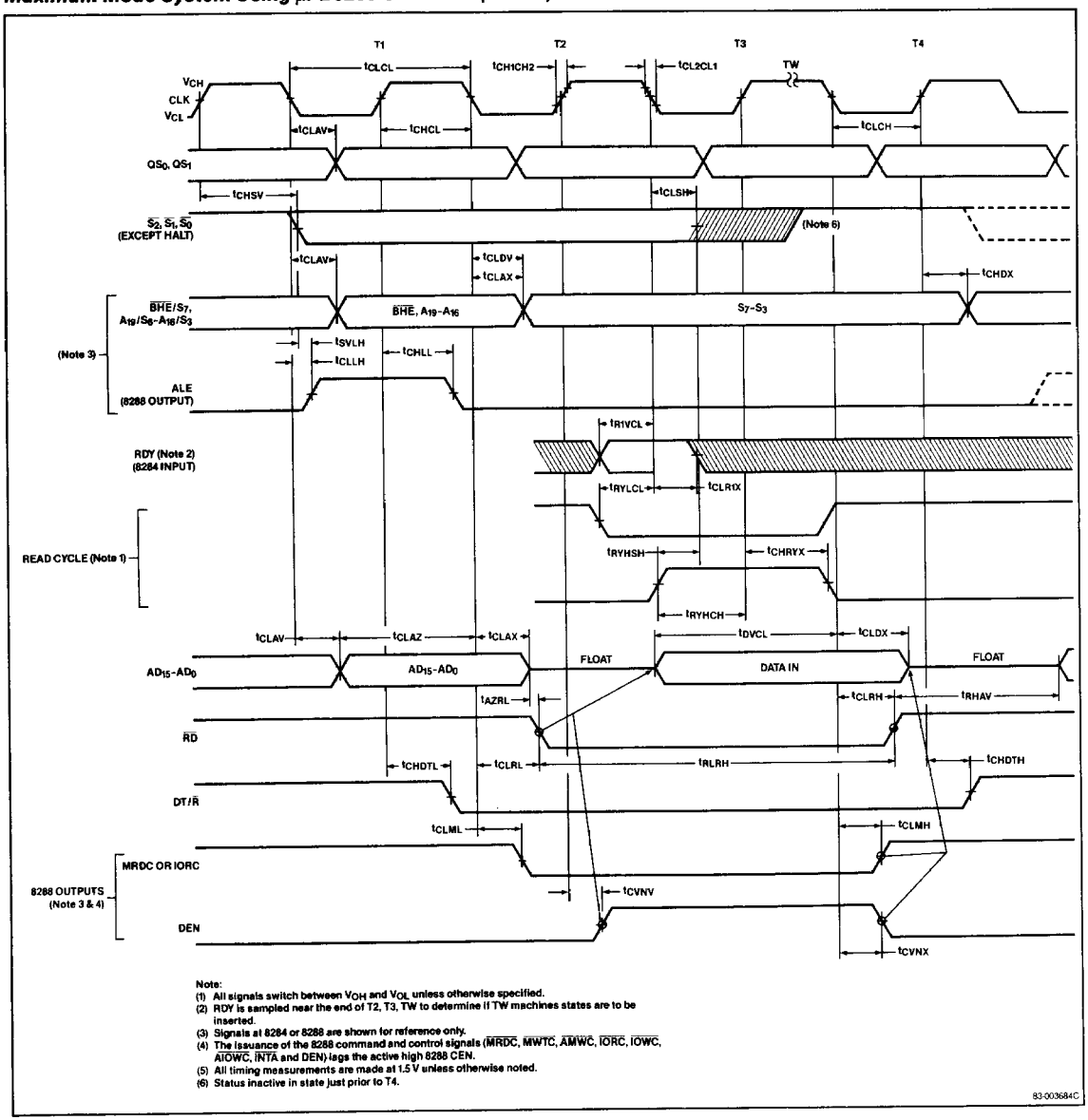
AC Timing Waveforms (cont)

Maximum Mode System Using μPB8288 Controller (Note 5)



Note:
(1) All signals switch between V_{OH} and V_{OL} unless otherwise specified.
(2) RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
(3) Signals at 8284 or 8288 are shown for reference only.
(4) The issuance of the 8288 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ and DEN) lags the active high 8288 CEN.
(5) All timing measurements are made at 1.5 V unless otherwise noted.
(6) Status inactive in state just prior to T4.

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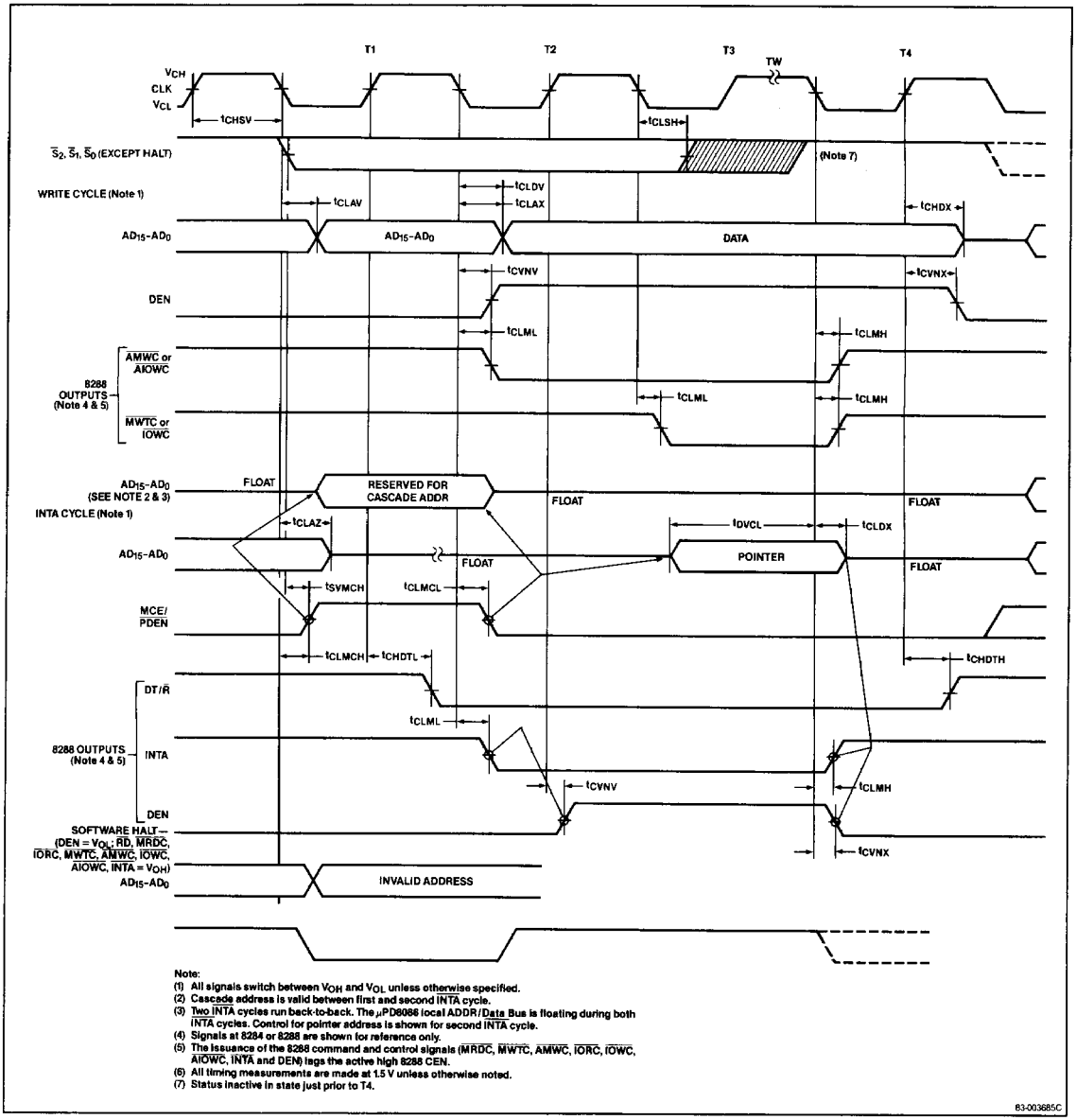
AC Timing Waveforms (cont)

Maximum Mode System Using μPB8288 Controller (Note 6)



Note:
(1) All signals switch between V_{OH} and V_{OL} unless otherwise specified.
(2) Cascade address is valid between first and second INTA cycle.
(3) Two INTA cycles run back-to-back. The μPD8086 local ADDR/Data Bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
(4) Signals at 8284 or 8288 are shown for reference only.
(5) The issuance of the 8288 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 8288 CEN.
(6) All timing measurements are made at 1.5 V unless otherwise noted.
(7) Status inactive in state just prior to T4.

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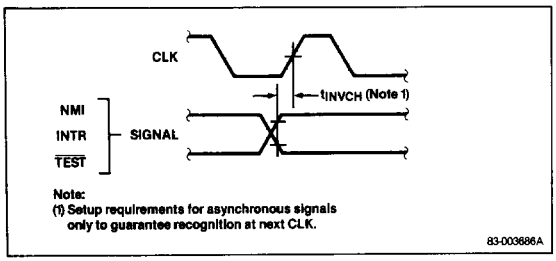
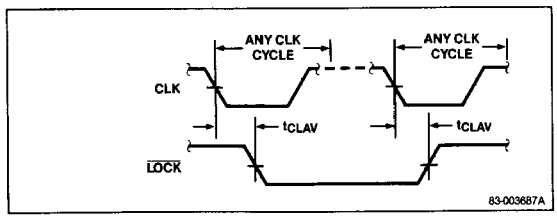
Timing Waveforms

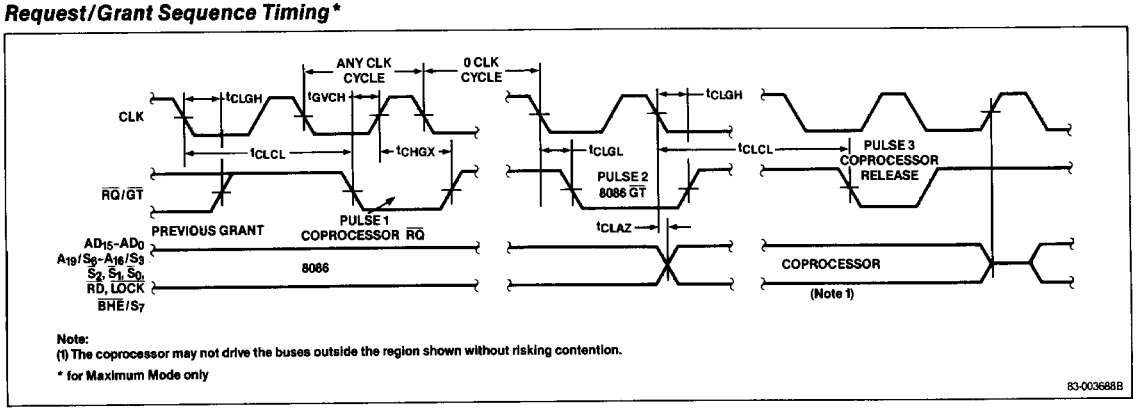
Asynchronous Signal Recognition



Bus Lock Signal Timing



Request/Grant Sequence Timing*



Hold/Hold Acknowledge Timing*