NEC
NEC Electronics Inc.

μPD78C10/C11/C14 8-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS WITH A/D CONVERTER

November 1987

Description

The μPD78C10, μPD78C11, and μPD78C14 single-chip microcomputers integrate sophisticated on-chip peripheral functions normally provided by external components. Their internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make the devices appropriate in data processing as well as control applications.

The devices integrate a 16-bit ALU, 4K-byte ROM, 256-byte RAM, an eight-channel A/D converter, a multifunction 16-bit timer/ event counter, two 8-bit timers, a USART, and two zero-cross detect inputs on a single die, allowing their use in fast, high-end processing applications. This involves analog signal interface and processing.

The μPD78C11 is a 4K-byte mask ROM device embedded with a custom customer program. The μPD78C14 is a 16K-byte mask ROM device. The μPD78C10 is the ROM-less version.

Features

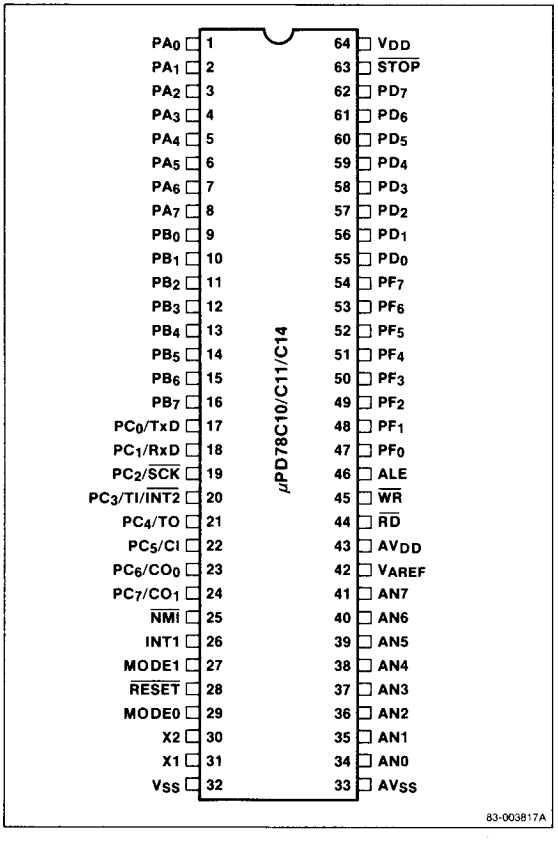
- ☐ CMOS technology
  - — 25 mA operating current (78C10/C11)
  - — 30 mA operating current (78C14)
- ☐ Complete single-chip microcomputer
  - — 16-bit ALU
  - — 4K x 8 ROM (78C11)
  - — 16K x 8 ROM (78C14)
  - — 256-byte RAM
- ☐ 44 I/O lines
- ☐ Two zero-cross detect inputs
- ☐ Two 8-bit timers
- ☐ Expansion capabilities
  - — 8085A-like bus
  - — 60K-byte external memory address range
- ☐ Eight-channel, 8-bit A/D converter
  - — Autoscan mode
  - — Channel select mode
- ☐ Full-duplex USART
  - — Synchronous and asynchronous
- ☐ 154 instructions
  - — 16-bit arithmetic, multiply, and divide
  - — HALT and STOP instructions
- ☐ 0.8-μs instruction cycle time (15-MHz operation)
- ☐ Prioritized interrupt structure
  - — Three external
  - — Eight internal
- ☐ Standby function
- ☐ On-chip clock generator
- ☐ 64-pin plastic QUIP, shrink DIP, or miniflat; 68-pin PLCC

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD78C10G-36 μPD78C11G-36 μPD78C14G-36	64-pin plastic QUIP	15 MHz
μPD78C10CW μPD78C11CW μPD78C14CW	64-pin plastic shrink DIP	15 MHz
μPD78C10G-1B μPD78C11G-1B μPD78C14G-1B	64-pin plastic miniflat	15 MHz
μPD78C10L μPD78C11L μPD78C14L	68-pin PLCC	15 MHz

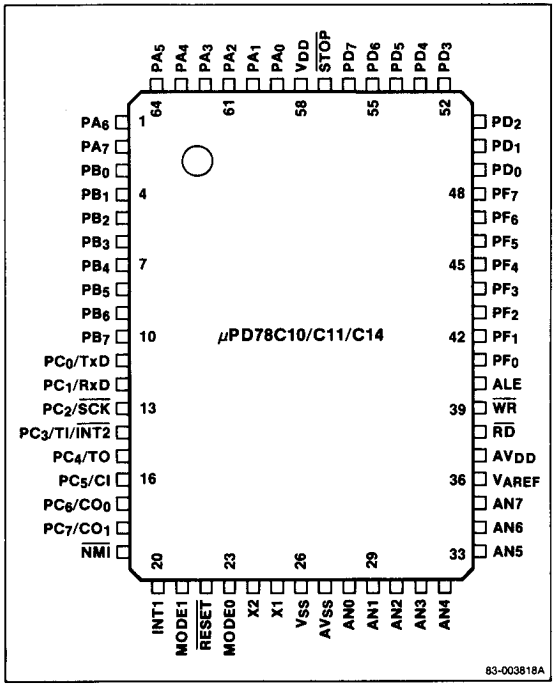
Pin Configurations

64-Pin Plastic QUIP or Shrink DIP



Pin Configurations (cont)

64-Pin Plastic Miniflat



Pin Identification

Symbol	Function
ALE	Address latch enable output
AN0-AN7	A/D converter analog inputs 0-7
INT1	Interrupt request 1 input
MODE1	Mode 1 input
MODE0	Mode 0 input/I/O/Memory output
$\overline{NMI}$	Nonmaskable interrupt input
PA_7-PA_0	Port A I/O
PB_7-PB_0	Port B I/O
PC_0/TxD	Port C I/O line 0/Transmit data output
PC_1/RxD	Port C I/O line 1/Receive data input
$PC_2/\overline{SCK}$	Port C I/O line 2/Serial clock I/O
PC_3/TI/$\overline{INT2}$	Port C I/O line 3/Timer input/Interrupt request 2 input
PC_4/TO	Port C I/O line 4/Timer output
PC_5/CI	Port C I/O line 5/Counter input
PC_6, PC_7/CO_0, CO_1	Port C I/O lines 6, 7/Counter outputs 0, 1
PD_7-PD_0	Port D I/O/Expansion memory address/data bus (bits AD_7-AD_0)
PF_7-PF_0	Port F I/O/Expansion memory address bus (bits AB_{15}-AB_8)
$\overline{RD}$	Read strobe output
$\overline{RESET}$	Reset input
$\overline{STOP}$	Stop mode control input
V_{AREF}	A/D converter reference voltage
$\overline{WR}$	Write strobe output
X1, X2	Crystal connections 1, 2
AV_{DD}	A/D converter power supply voltage
AV_{SS}	A/D converter power supply ground
V_{DD}	5 V power supply
V_{SS}	Ground
IC	Internal connection

Pin Functions

ALE [Address Latch Enable]

The ALE output is used to latch the address of PD_7-PD_0 into an external latch.

AN0-AN7 [Analog Inputs]

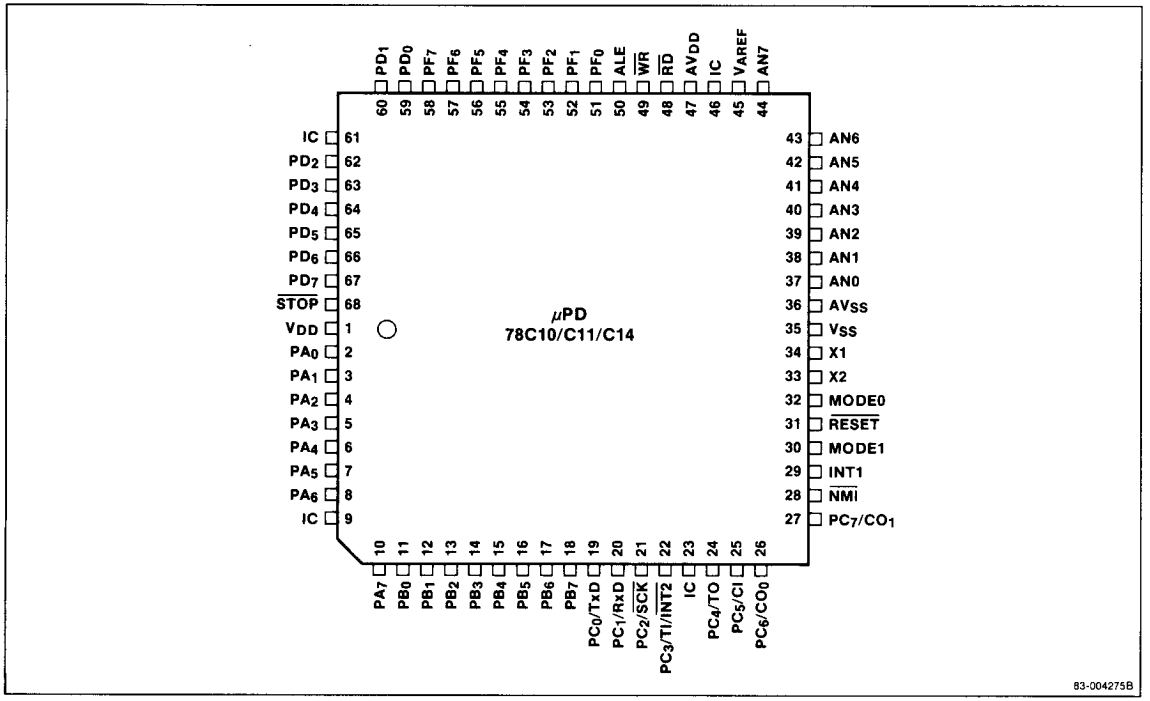
These are the eight analog inputs to the A/D converter. AN4-AN7 can also be used as a digital input for falling edge detection.

CI [Counter Input]

External pulse input to timer/event counter.

Pin Configurations (cont)

68-Pin PLCC



CO_0, CO_1 [Counter Outputs 0, 1]

Programmable waveform outputs based on timer/event counter.

INT1 [Interrupt Request 1]

INT1 is a rising-edge-triggered, maskable interrupt input. It is also an ac-input, zero-cross detection terminal.

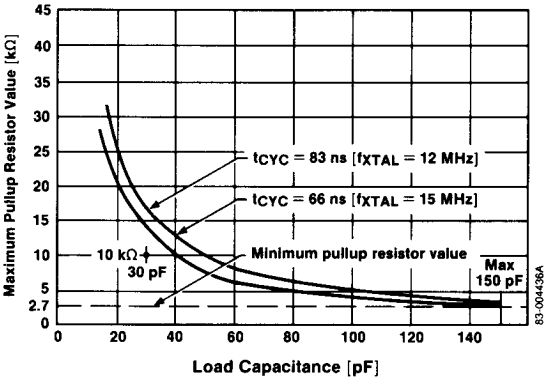
$\overline{INT2}$ [Interrupt Request 2]

$\overline{INT2}$ is a falling-edge-triggered, maskable interrupt input. It is also an ac-input, zero-cross detection terminal.

MODE1, MODE0 [Mode 1, 0]

The MODE1 and MODE0 inputs select the amount of external memory. MODE0 outputs the $\overline{IO}$ signal, and MODE1 outputs the $\overline{M1}$ signal. An external pullup resistor to V_{DD} is required if the input is to be a logic high. For exact value of pullup resistor see the following graph.

Maximum Pullup Resistor Value vs Load Capacitance at MODE0 or MODE1 Pin



$\overline{NMI}$ [Nonmaskable Interrupt]

Falling-edge, Schmitt-triggered nonmaskable interrupt input.

PA_7-PA_0 [Port A]

Port A is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port A inputs.

PB_7-PB_0 [Port B]

Port B is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port B inputs.

PC_7-PC_0 [Port C]

Port C is an 8-bit three-state port. Each bit is independently programmable as either input or output. Alternatively, the lines of port C can be used as control lines for the USART, interrupts, and timer. Reset makes all lines of port C inputs.

PD_7-PD_0 [Port D]

Port D is an 8-bit three-state port. It can be programmed as either 8 bits of input or 8 bits of output. When external expansion memory is used, port D acts as the multiplexed address/data bus.

PF_7-PF_0 [Port F]

Port F is an 8-bit three-state port. Each bit is independently programmable as an input or output. When external expansion memory is used, port F outputs the high-order address bits.

$\overline{RD}$ [Read Strobe]

The three-state $\overline{RD}$ output goes low to gate data from external devices onto the data bus. $\overline{RD}$ goes high during reset.

$\overline{RESET}$ [Reset]

When the Schmitt-triggered $\overline{RESET}$ input is brought low, it initializes the device.

RxD [Receive Data]

Serial data input terminal.

$\overline{SCK}$ [Serial Clock]

Output for the serial clock when internal clock is used. Input for serial clock when external clock is used.

$\overline{STOP}$ [Stop Mode Control Input]

A low-level input on $\overline{STOP}$ (Schmitt-triggered input) stops the system clock oscillator.

TI [Timer Input]

Timer input terminal.

TO [Timer Output]

The output of TO is a square wave with a frequency determined by the timer/counter.

TxD [Transmit Data]

Serial data output terminal.

V_{AREF} [A/D Converter Reference]

V_{AREF} sets the upper limit for the A/D conversion range.

$\overline{WR}$ [Write Strobe]

The three-state $\overline{WR}$ output goes low to indicate that the data bus holds valid data. It is a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes high during reset.

X1, X2 [Crystal Connections 1, 2]

X1 and X2 are the system clock crystal oscillator terminals. X1 is the input for an external clock.

AV_{DD} [A/D Converter Power]

This is the power supply voltage for the A/D converter.

AV_{SS} [A/D Converter Power Ground]

AV_{SS} is the ground potential for the A/D converter power supply.

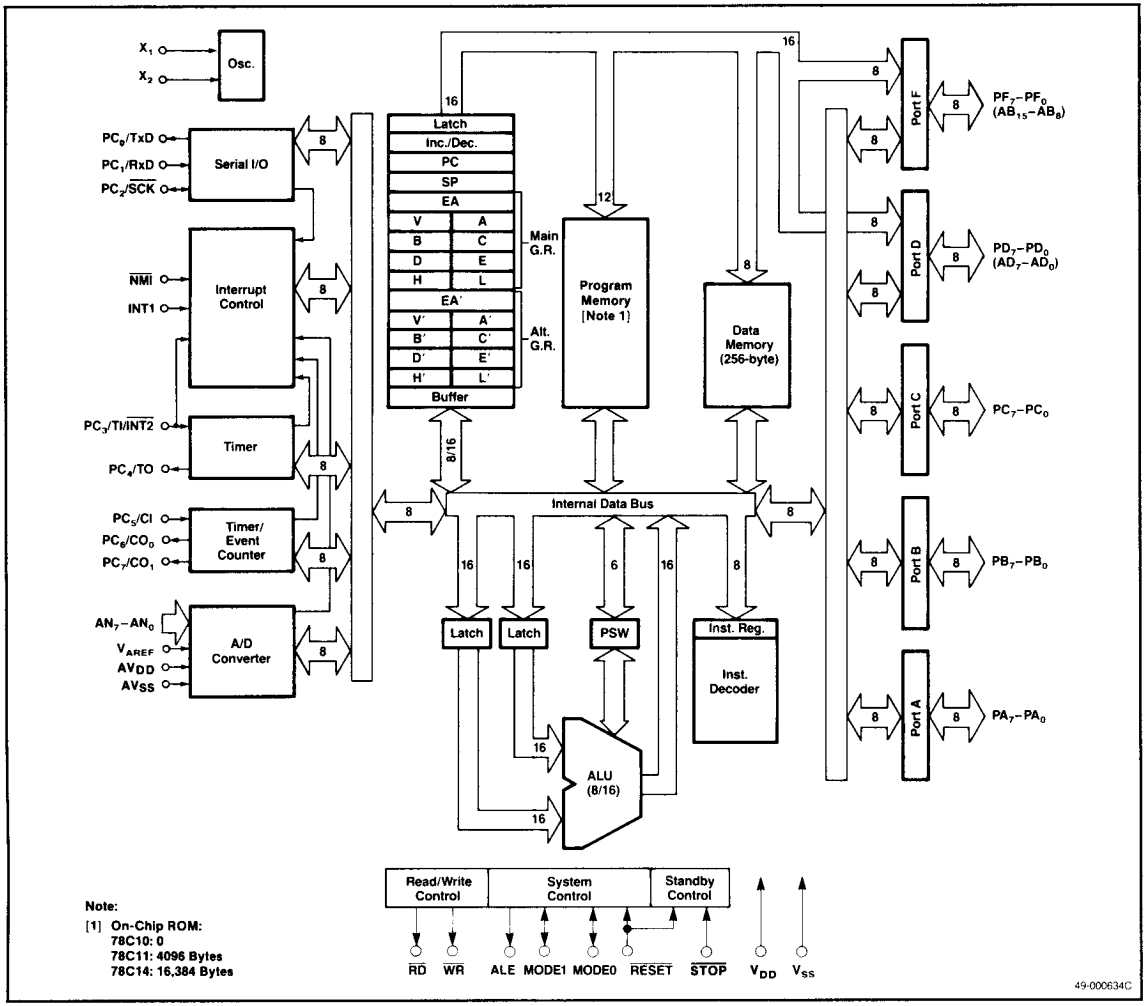
V_{SS} [Ground]

Ground potential.

V_{DD} [Power Supply]

+5-volt power supply.

Block Diagram



Functional Description

Memory Map

The μPD78C11 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-4095) and RAM (FF00H-FFFFH), any memory location can be used as ROM or RAM. The memory map, figure 1, defines the 0 to 64K byte memory space for the μPD78C11. On-chip ROM is located from 0-16,383 in the μPD78C14.

Input/Output

The μPD78C10/C11/C14 has 44 digital I/O lines, five 8-bit ports (port A, port B, port C, port D, port F), and four digital input lines (AN4-AN7).

Analog Input Lines. AN0-AN7 are configured as analog input lines for the on-chip A/D converter. Lines AN4-AN7 can be used as digital input lines for falling-edge detection.

Port A, Port B, Port C, Port F. Each line of these ports can be individually programmed as an input or output. When used as I/O ports, all have latched outputs and high-impedance inputs.

Port D. Port D can be programmed as a byte input or a byte output.

Control Lines. Under software control, each line of port C can be configured individually as a control line for the serial interface, timer, and timer/counter or as an I/O port.

Memory Expansion. In addition to the single-chip operation mode, the μPD78C11 has four memory expansion modes. Under software control, port D can provide a multiplexed low-order address and data bus; port F can provide a high-order address bus. Table 1 shows the relation between memory expansion modes and the pin configurations of port D and port F.

Table 1. Memory Expansion Modes and Port Configurations

Memory Expansion	Port	Port Configuration
None	Port D	I/O port
	Port F	I/O port
256 bytes	Port D	Multiplexed address/data bus
	Port F	I/O port
4K bytes	Port D	Multiplexed address/data bus
	Port F (PF_3-PF_0)	Address bus
	Port F (PF_7-PF_4)	I/O port
16K bytes	Port D	Multiplexed address/data bus
	Port F (PF_5-PF_0)	Address bus
	Port F (PF_7-PF_6)	I/O port
60K bytes	Port D	Multiplexed address/data bus
	Port F	Address bus

Timers

The two 8-bit timers may be programmed independently or cascaded as a 16-bit timer. The timer can be software set to increment at intervals of four machine cycles (0.8 μs at 15-MHz operation) or 128 machine cycles (25.6 μs at 15-MHz), or to increment on receipt of a pulse at TI. Figure 2 is the block diagram for the timer.

Timer/Event Counter

The 16-bit multifunctional timer/event counter (figure 3) can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse width measurement
- Programmable frequency and duty cycle waveform output

8-Bit A/D Converter

- 8 input channels
- 4 conversion result registers
- 2 powerful operation modes
  - — Autoscan mode
  - — Channel select mode
- Successive approximation technique
- Absolute accuracy: 0.6% FSR ±1/2 LSB
- Conversion range: 0 to 5 V
- Conversion time: 38.4 μs
- Interrupt generation

Figure 1. Memory Map

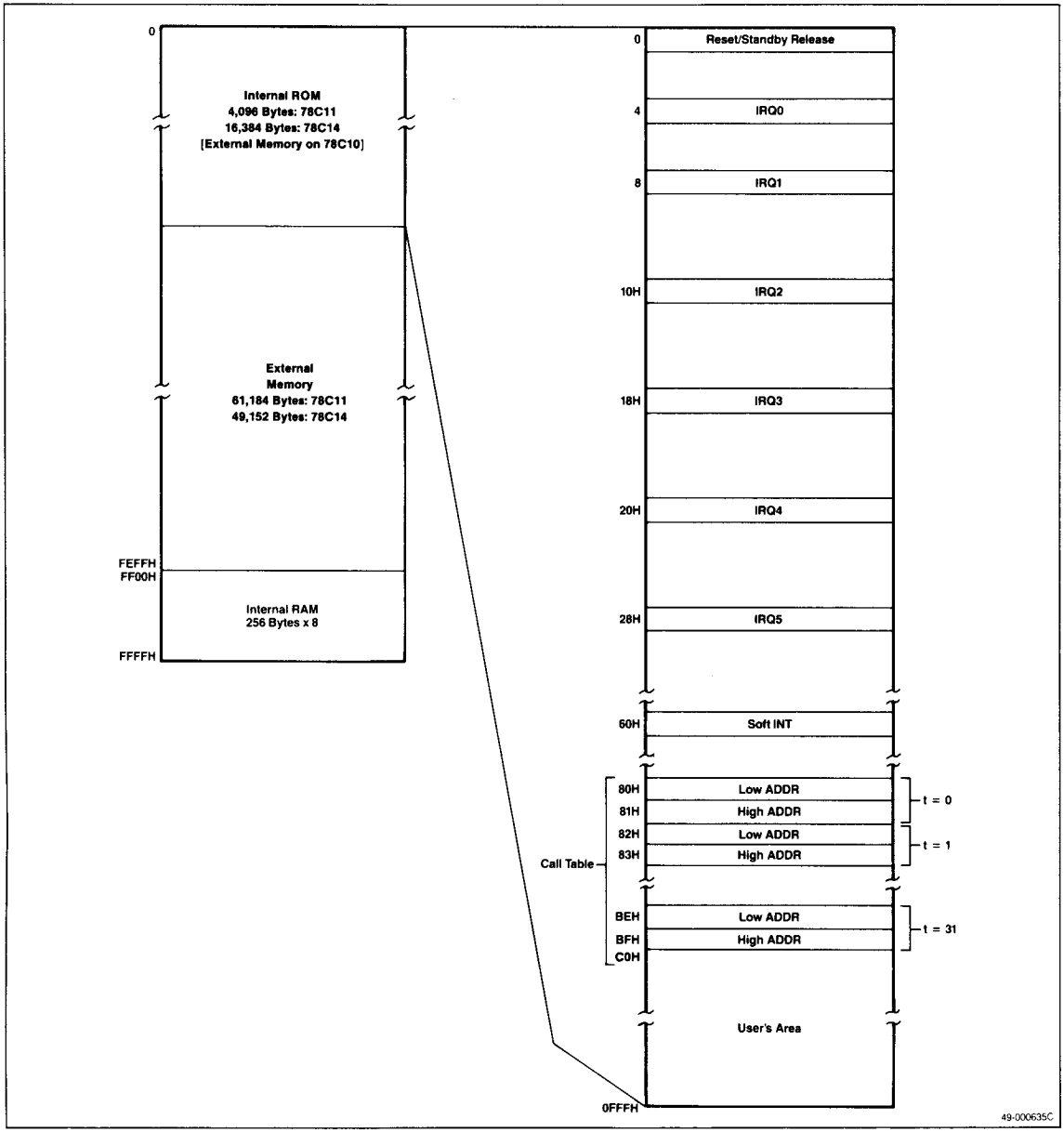


Figure 2. Timer Block Diagram

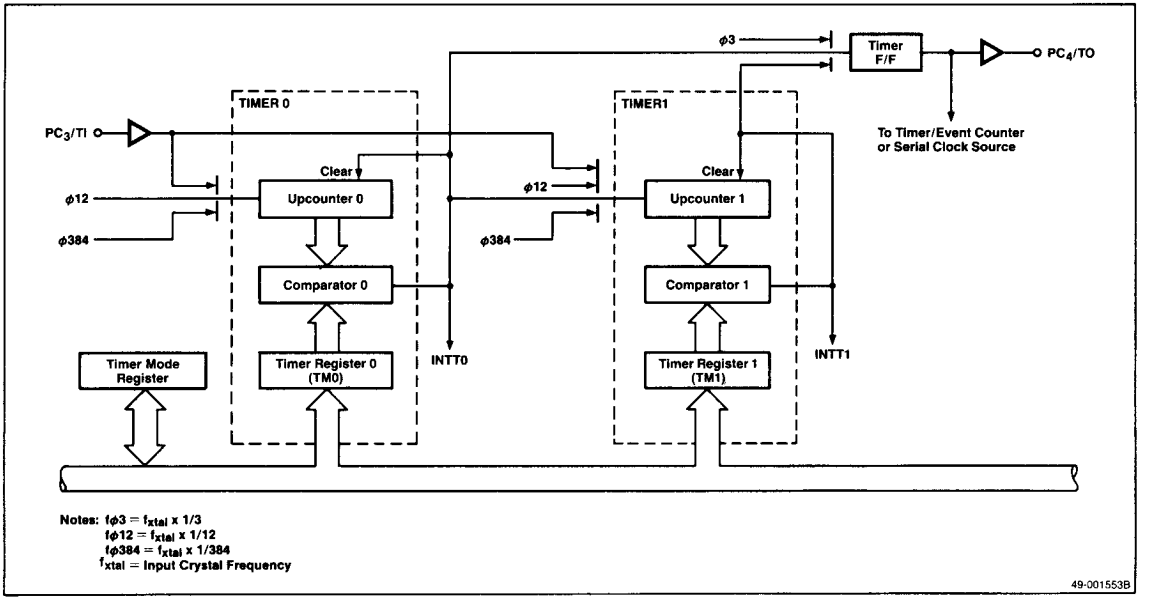
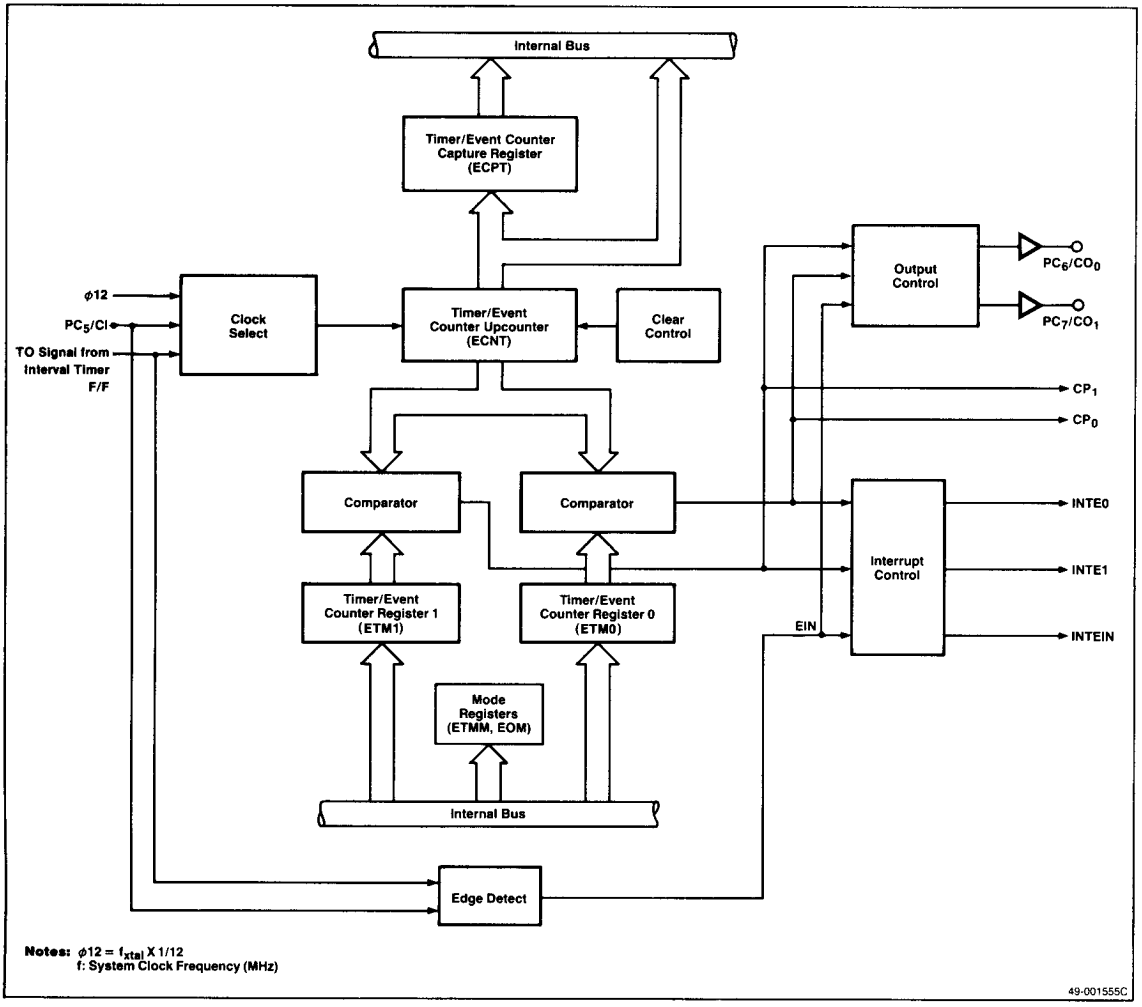


Figure 3. Block Diagram for Timer/Event Counter

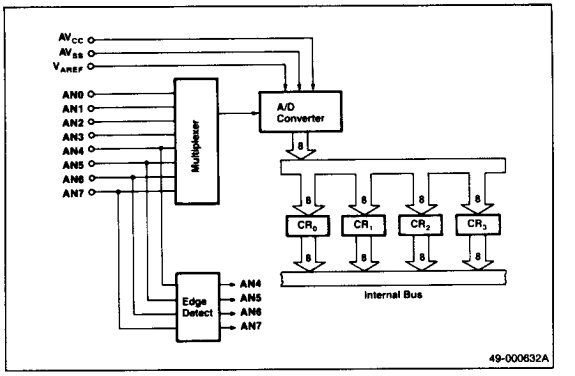


Analog/Digital Converter

The μPD78C10/C11/C14 features an 8-bit, high-speed, high-accuracy A/D converter. The A/D converter is made up of a 256-resistor ladder and a successive approximation register (SAR). There are four conversion result registers (CR0-CR3).

The eight-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR0-CR3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers. Figure 4 is the block diagram for the A/D converter. To stop the operation of the A/D converter and thus reduce power consumption, set $V_{AREF} = 0$ V.

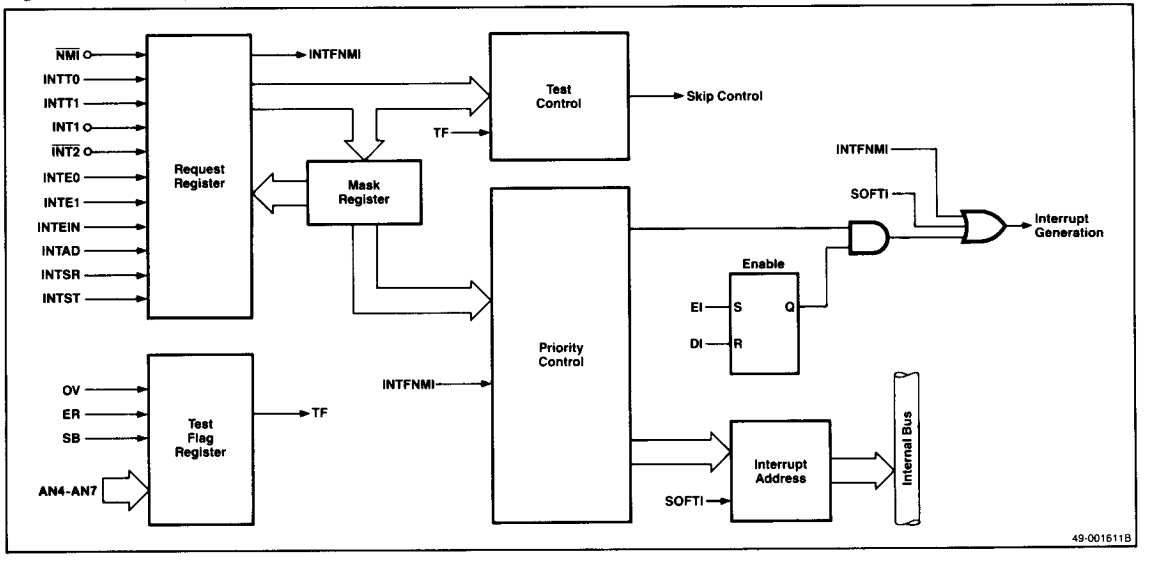
Figure 4. A/D Converter Block Diagram



Interrupt Structure

There are 12 interrupt sources. Three are external interrupts and nine are internal. Table 2 shows 11 interrupt sources divided into seven priority levels where IRQ0 is the highest and 1RQ6 is the lowest. See figure 5.

Figure 5. Interrupt Structure Block Diagram



Standby Function

The μPD78C10/C11/C14 has two standby modes: HALT and STOP. The HALT mode reduces power consumption to 50% of normal operating requirements, while maintaining the contents of on-chip registers, RAM, and control status. The system clock and on-board peripherals continue to operate, but the CPU stops executing instructions. The HALT mode is initiated by executing the HLT instruction. The HALT mode can be released by any nonmasked interrupt or by $\overline{\text{RESET}}$.

The STOP mode reduces power consumption to less than 0.1% of normal operating requirements. There are two STOP modes: type A and type B.

Type A is initiated by executing a STOP instruction. If V_{DD} is held above 2.5 V, the on-board RAM is saved. The oscillator is stopped. The STOP mode can be released by an input on $\overline{\text{NMI}}$ or $\overline{\text{RESET}}$. The user can program oscillator stabilization time up to 52.4 ms via timer 1. By checking the standby flag (SB), the user can determine whether the processor has been in the standby mode or has been powered up.

Type B is initiated by inputting a low level on the $\overline{\text{STOP}}$ input. The RAM contents are saved if V_{DD} is held above 2.5 V. The oscillator is stopped. The STOP mode is released by raising $\overline{\text{STOP}}$ to a high level. The oscillator stabilization time is fixed at 52.4 ms; 52.4 ms after $\overline{\text{STOP}}$ is raised, instruction execution will automatically begin at location 0. You can increase the stabilization time by holding $\overline{\text{RESET}}$ low for the required time period.

Table 2. Interrupt Sources

Interrupt Request	Interrupt Address	Type of Interrupt	Internal/ External
IRQ0	4	$\overline{\text{NMI}}$ (Nonmaskable interrupt)	Ext
IRQ1	8	INTT0 (Coincidence signal from timer 0)	Int
		INTT1 (Coincidence signal from timer 1)	
IRQ2	16	INT1 (Maskable interrupt)	Ext
		$\overline{\text{INT2}}$ (Maskable interrupt)	
IRQ3	24	INTE0 (Coincidence signal from timer/event counter)	Int
		INTE1 (Coincidence signal from timer/event counter)	
IRQ4	32	INTEIN (Falling signal of CI or TO into the timer/event counter)	Int/Ext
		INTAD (A/D converter interrupt)	
IRQ5	40	INTSR (Serial receive interrupt)	Int
		INST (Serial send interrupt)	
IRQ6	96	SOFTI instruction	Int

Universal Serial Interface

The serial interface can operate in one of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first, for easy interfacing to certain NEC peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception: search and nonsearch. In the search mode, data is transferred one bit at a time from the serial register to the receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from the serial register to the transmit buffer occurs eight bits at a time. Figure 6 shows the universal serial interface block diagram.

Zero-Crossing Detector

The INT1 and $\overline{\text{INT2}}$ terminals (used common to TI and PC_3) can detect the zero-crossing point of low-frequency ac signals. When driven directly, these pins respond as a normal digital input. Figure 7 shows the zero-crossing detection circuitry.

The zero-crossing detection capability allows you to make the 50-60 Hz power signal the basis for system timing and to control voltage phase-sensitive devices.

To use the zero-cross detection mode, an ac signal of 1.0 to 1.8 V (peak-to-peak) and a maximum frequency of 1 kHz is coupled through an external capacitor to the INT1 and $\overline{\text{INT2}}$ pins.

For the INT1 pin, the internal digital state is sensed as a 0 until the rising edge crosses the average dc level, when it becomes a 1 and INT1 interrupt is generated.

For the $\overline{\text{INT2}}$ pin, the state is sensed as a 1 until the falling edge crosses the average dc level, when it becomes a 0 and $\overline{\text{INT2}}$ interrupt is generated.

Figure 6. Universal Serial Interface Block Diagram

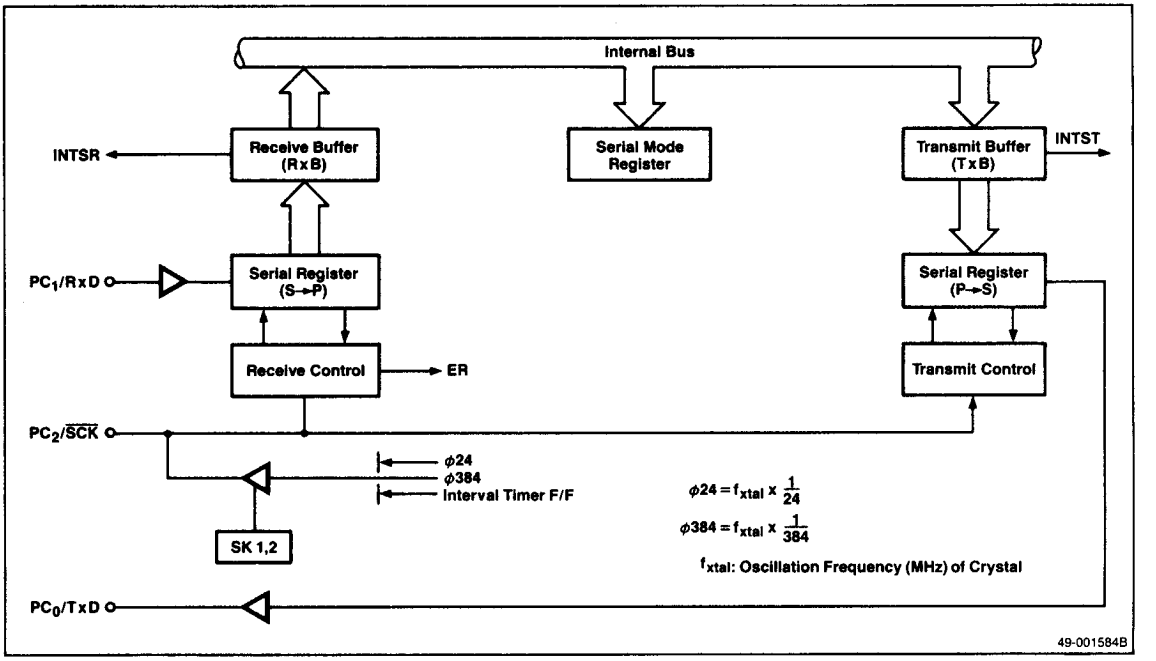
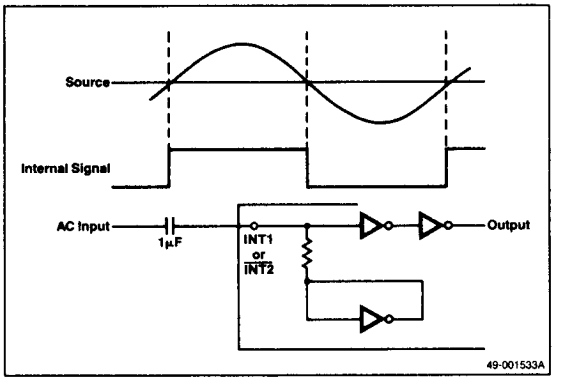


Figure 7. Zero-Crossing Detection Circuit



Capacitance

$T_A = 25°C$; $V_{DD} = V_{SS} = 0$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			10	pF	f_c = 1 MHz. Unmeasured pins returned to 0 V.
Output capacitance	C_O			20	pF	
I/O capacitance	C_{IO}			20	pF	

Absolute Maximum Ratings

Power supply voltages, V_{DD}		−0.5 to +7.0 V
	AV_{DD}	AV_{SS} to V_{DD} + 0.5 V
	AV_{SS}	−0.5 to +0.5 V
Input voltage, V_I		−0.5 V to V_{DD} + 0.5 V
Output voltage, V_O		−0.5 V to V_{DD} + 0.5 V
Output current low, I_{OL}		4.0 mA
Output current low, total for all pins		100 mA
Output current high, I_{OH}		−2.0 mA
Output current high, total for all pins		−50 mA
Reference input voltage, V_{AREF}		−0.5 V to AV_{DD} + 0.3 V
Operating temperature, T_{OPR} $f_{XTAL} \leq 15$ MHz		−40 to +85°C
Storage temperature, T_{STG}		−65 to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Oscillation Characteristics

($T_A = -40$ to $+85°C$, $V_{DD} = AV_{DD} = 5\ V \pm 10\%$, $V_{SS} = AV_{SS} = 0\ V$, $V_{DD} - 0.8\ V \leqq AV_{DD} \leqq V_{DD}$, $3.4\ V \leqq V_{AREF} \leqq AV_{DD}$)

Resonator	Recommended Circuits	Parameter	Min	Typ	Max	Unit	Test Conditions
Ceramic resonator (Note 1) or XTAL (Note 2)	(Note 3)	Oscillation frequency (f_{XX})	4		15	MHz	A/D converter not used
			5.8		15	MHz	A/D converter used
External clock	(Note 4)	X1 input frequency (f_X)	4		15	MHz	A/D converter not used
			5.8		15	MHz	A/D converter used
		X1 input rise, fall time (t_r, t_f)	0		20	ns	
		X1 input high, low level width ($t_{\phi H}$, $t_{\phi L}$)	20		250	ns	

Notes:

(1) Recommended ceramic resonators

Manufacturer	Product Name	External Capacitance C1 (pF)	External Capacitance C2 (pF)
Murata	CSA15.00MX3	22	22
	CSA12.00MT	30	30
	CST12.00MT	—	—

CST12.00MT has capacitance internally

(2) For XTAL, the following external capacitances are recommended:

$$C1 = C2 = 10\ pF$$

(3) See the following recommended XTAL oscillation circuit diagram

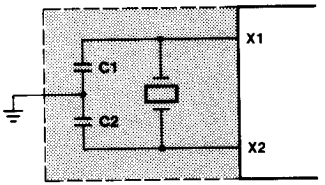
(4) See the following recommended external clock diagram

When using an external crystal, it should be a parallel-resonant, fundamental mode, "AT cut" crystal. Capacitors C1 and C2 are required for frequency stability. The values of C1 and C2 (C1 = C2) can be calculated from the load capacitance (C_L) specified by the crystal manufacturer:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_S$$

Where C_S is any stray capacitance in parallel with the crystal, such as the 78C10, 78C11, or 78C14 input capacitance between X1 and X2.

Recommended XTAL or Ceramic Resonator Oscillation Circuit Diagram



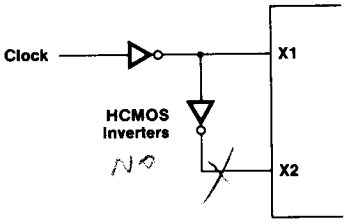
Notes:

[1] External oscillation circuit should be as close to the X1 and X2 pins as possible.

[2] Do not place other signal lines in the shaded area.

83-004303A

Recommended External Clock Diagram



83-004277A

DC Characteristics

$T_A = -40$ to $+85°C$; $V_{DD} = +5.0\ V \pm 10\%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL1}	0		0.8	V	All except Note 1 inputs.
	V_{IL2}	0		0.2 V_{DD}	V	Note 1 inputs.
Input high voltage	V_{IH1}	2.2		V_{DD}	V	All except X1, X2, and Note 1 inputs.
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	X1, X2, and Note 1 inputs.
Output low voltage	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output high voltage	V_{OH}	$V_{DD} - 1.0$			V	$I_{OH} = -1.0$ mA
		$V_{DD} - 0.5$			V	$I_{OH} = -100\ \mu A$
Data retention voltage	V_{DDDR}	2.5			V	STOP mode
Input current	I_I			±200	μA	INT1 (Note 2), TI(PC_3) (Note 3); $0\ V \le V_I \le V_{DD}$
Input leakage current	I_{LI}			±10	μA	All except INT1, TI(PC_3); $0\ V \le V_I \le V_{DD}$
Output leakage current	I_{LO}			±10	μA	$0\ V \le V_O \le V_{DD}$
AV_{DD} supply current	AI_{DD1}		0.5	1.3	mA	f = 15 MHz
	AI_{DD2}		10	20	μA	STOP mode
V_{DD} supply current (78C10/C11)	I_{DD1}		13	25	mA	Normal operation f = 15 MHz
	I_{DD2}		7	13	mA	HALT mode f = 15 MHz
V_{DD} supply current (78C14)	I_{DD1}		16	30	mA	Normal operation f = 15 MHz
	I_{DD2}		8	15	mA	HALT mode f = 15 MHz
Data retention current	I_{DDDR}		1	15	μA	$V_{DDDR} = 2.5$ V (Note 4)
			10	50	μA	$V_{DDDR} = 5$ V ± 10% (Note 4)

Notes:

(1) Inputs $\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$, INT1, TI, and AN4-AN7.

(2) Assuming ZCM register is set to self-bias.

(3) Assuming ZCM register is set to self-bias and the MCC register is set to control mode.

(4) Hardware/software STOP mode and assuming ZCM register is set to self-bias not selected.

Serial Operation

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
$\overline{\text{SCK}}$ cycle time	t_{CYK}	0.8		μs	$\overline{\text{SCK}}$ input (1), (3)
		0.4		μs	$\overline{\text{SCK}}$ input (2)
		1.6		μs	$\overline{\text{SCK}}$ output (3)
$\overline{\text{SCK}}$ width low	t_{KKL}	335		ns	$\overline{\text{SCK}}$ input (1), (3)
		160		ns	$\overline{\text{SCK}}$ input (2)
		700		ns	$\overline{\text{SCK}}$ output (3)
$\overline{\text{SCK}}$ width high	t_{KKH}	335		ns	$\overline{\text{SCK}}$ input (1), (3)
		160		ns	$\overline{\text{SCK}}$ input (2)
		700		ns	$\overline{\text{SCK}}$ output (3)
RxD setup time to $\overline{\text{SCK}}\uparrow$	t_{RXK}	80		ns	(Note 1)
RxD hold time after $\overline{\text{SCK}}\uparrow$	t_{KRX}	80		ns	(Note 1)
$\overline{\text{SCK}}\downarrow$ TxD delay time	t_{KTX}		210	ns	(Note 1)

Notes:

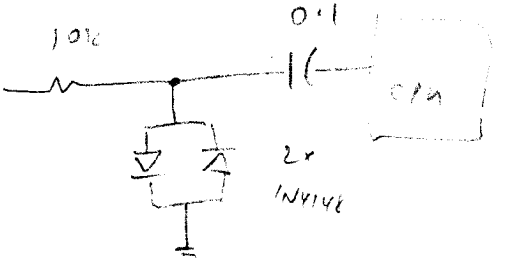
(1) 1x baud rate in synchronous or I/O interface mode.

(2) 16x baud rate or 64x baud rate in asynchronous mode.

(3) $f_{XTAL} = 15$ MHz.

Zero-Cross Characteristics

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Zero-cross detection input	V_{ZX}	1	1.8	VAC_{p-p}	Ac coupled 60-Hz sine wave
Zero-cross accuracy	A_{ZX}		±135	mV	
Zero-cross detection input frequency	f_{ZX}	0.05	1	kHz	



AC Characteristics

Read/Write Operation

$T_A = -40$ to $+85$°C; $V_{DD} = AV_{DD} = +5.0$ V ±10%; $V_{SS} = 0$ V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
$\overline{RESET}$ pulse width high, low	t_{RSH}, t_{RSL}	10		μs	
$\overline{NMI}$ pulse width high, low	t_{NIH}, t_{NIL}	10		μs	
X1 Input cycle time	t_{CYC}	66	250	ns	
Address setup to ALE↓	t_{AL}	30		ns	(Notes 1 and 2)
Address hold after ALE↓	t_{LA}	35		ns	
Address to $\overline{RD}$↓ delay time	t_{AR}	100		ns	
$\overline{RD}$↓ to address floating	t_{AFR}		20	ns	(Note 1)
Address to data input	t_{AD}		250	ns	(Notes 1 and 2)
ALE↓ to data input	t_{LDR}		135	ns	
$\overline{RD}$↓ to data input	t_{RD}		120	ns	
ALE↓ to $\overline{RD}$↓ delay time	t_{LR}	15		ns	
Data hold time to $\overline{RD}$↑	t_{RDH}	0		ns	(Note 1)
$\overline{RD}$↑ to ALE↑ delay time	t_{RL}	80		ns	(Notes 1 and 2)
$\overline{RD}$ width low	t_{RR}	215		ns	Data read; (notes 1 and 2)
		415		ns	Opcode fetch; (notes 1 and 2)
ALE width high	t_{LL}	90		ns	(Notes 1 and 2)
$\overline{M1}$ setup time to ALE↓	t_{ML}	30		ns	(Note 2)
$\overline{M1}$ hold time after ALE↓	t_{LM}	35		ns	
$\overline{IO}$/M setup time to ALE↓	t_{IL}	30		ns	
$\overline{IO}$/M hold time after ALE↓	t_{LI}	35		ns	
Address to $\overline{WR}$↓ Delay	t_{AW}	100		ns	(Notes 1 and 2)
ALE↓ to data output	t_{LDW}		180	ns	
$\overline{WR}$↓ to data output	t_{WD}		100	ns	(Note 1)
ALE↓ to $\overline{WR}$↓ delay	t_{LW}	15		ns	(Notes 1 and 2)
Data setup time to $\overline{WR}$↑	t_{DW}	165		ns	
Data hold time to $\overline{WR}$↑	t_{WDH}	60		ns	
$\overline{WR}$↑ to ALE↑ delay time	t_{WL}	80		ns	
$\overline{WR}$ width low	t_{WW}	215		ns	

Notes:

(1) Load capacitance $C_L = 150$ pF.

(2) Values are for 15-MHz operation. For operation at other frequencies, refer to "Bus Timing Depending on t_{CYC}" on the following page.

A/D Converter Characteristics

$T_A = -40$ to $+85°C$; $V_{DD} = AV_{DD} = +5.0\ V \pm 10\%$,
$V_{SS} = AV_{SS} = 0\ V$; $V_{DD} - 0.5\ V \leqq AV_{DD} \leqq V_{DD}$; $3.4\ V \leqq V_{AREF} \leqq AV_{DD}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Resolution		8			Bits	
Absolute accuracy (Note 1)				±0.4	%FSR (2)	$T_A = -10$ to $+70°C$, 66 ns ≦ t_{CYC} ≦ 170 ns, 4.0 V ≦ $V_{AREF} \leqq AV_{DD}$
				±0.6	%FSR (2)	66 ns ≦ t_{CYC} ≦ 170 ns, 4.0 V ≦ $V_{AREF} \leqq AV_{DD}$
				±0.8	%FSR (2)	66 ns ≦ t_{CYC} ≦ 170 ns, 3.4 V ≦ $V_{AREF} \leqq AV_{DD}$
Conversion time	t_{CONV}	576			t_{CYC}	66 ns ≦ t_{CYC} ≦ 110 ns
		432			t_{CYC}	110 ns ≦ t_{CYC} ≦ 170 ns
Sampling time	t_{SAMP}	96			t_{CYC}	66 ns ≦ t_{CYC} ≦ 110 ns
		72			t_{CYC}	110 ns ≦ t_{CYC} ≦ 170 ns
Analog input voltage	V_{IAN}	0		V_{AREF}	V	
Analog input impedance	R_{AN}		1000		MΩ	
		leakage ± 10μA (Equiv ± 500k)				
Reference voltage	V_{AREF}	3.4		AV_{DD}	V	
V_{AREF} current	I_{AREF1}		1.5	3.0	mA	Operation mode
	I_{AREF2}		0.7	1.5	mA	STOP mode
AV_{DD} supply current	AI_{DD1}		0.5	1.3	mA	Operation mode
	AI_{DD2}		10	20	μA	STOP mode

Notes:

(1) Quantizing error (±1/2 LSB) is not included.

(2) FSR = Full-scale resolution.

Bus Timing Depending on t_{CYC}

Symbol	Calculating Expression	Min/Max (ns)
t_{TIH}, t_{TIL}	6T (TI input – PC_3)	Min
t_{CI1H}, t_{CI1L} (Note 2)	6T (CI input – PC_5)	Min
t_{CI2H}, t_{CI2L} (Note 3)	48T (CI input – PC_5)	Min
t_{I1H}, t_{I1L}	36T (INT1)	Min
t_{I2H}, t_{I2L}	36T ($\overline{INT2}$)	Min
t_{AL}	2T – 100	Min
t_{LA}	T – 30	Min
t_{AR}	3T – 100	Min
t_{AD}	7T – 220	Max
t_{LDR}	5T – 200	Max
t_{RD}	4T – 150	Max
t_{LR}	T – 50	Min
t_{RL}	2T – 50	Min
t_{RR}	4T – 50 (Data Read)	Min
	7T – 50 (Opcode Fetch)	Min
t_{LL}	2T – 40 (95ns)	Min
t_{ML}	2T – 100	Min
t_{LM}	T – 30	Min
t_{IL}	2T – 100	Min
t_{LI}	T – 30	Min
t_{AW}	3T –100	Min
t_{LDW}	T + 110	Max
t_{LW}	T – 50	Min
t_{DW}	4T – 100	Min
t_{WDH}	2T – 70	Min
t_{WL}	2T – 50	Min
t_{WW}	4T – 50	Min
t_{CYK}	12T ($\overline{SCK}$ input) (Note 1)	Min
	24T ($\overline{SCK}$ output)	Min
t_{KKL}	5T + 5 ($\overline{SCK}$ input) (Note 1)	Min
	12T – 100 ($\overline{SCK}$ output)	Min
t_{KKH}	5T + 5 ($\overline{SCK}$ input) (Note 1)	Min
	12T – 100 ($\overline{SCK}$ output)	Min

Notes:

(1) 1x baud rate in synchronous or I/O interface mode.
$T = t_{CYC} = 1/f_{XTAL}$.
The items not included in this list are independent of oscillator frequency (f_{XTAL}).

(2) Event counter mode.

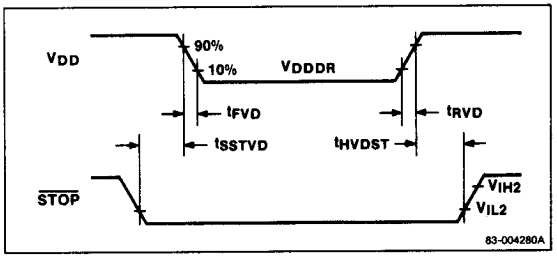
(3) Pulse width measurement mode.

Data Memory STOP Mode Data Retention Characteristics

$T_A = -40$ to $+85$°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention power supply voltage	V_{DDDR}	2.5		5.5	V	
Data retention power supply current	I_{DDDR}		1	15	μA	$V_{DDDR} = 2.5$ V
			15	50	μA	$V_{DDDR} = 5$ V ±10%
V_{DD} rise, fall time	t_{RVD}, t_{FVD}	200			μs	
$\overline{STOP}$ setup time to V_{DD}	t_{SSTVD}	12T +0.5			μs	
$\overline{STOP}$ hold time from V_{DD}	t_{HVDST}	12T +0.5			μs	

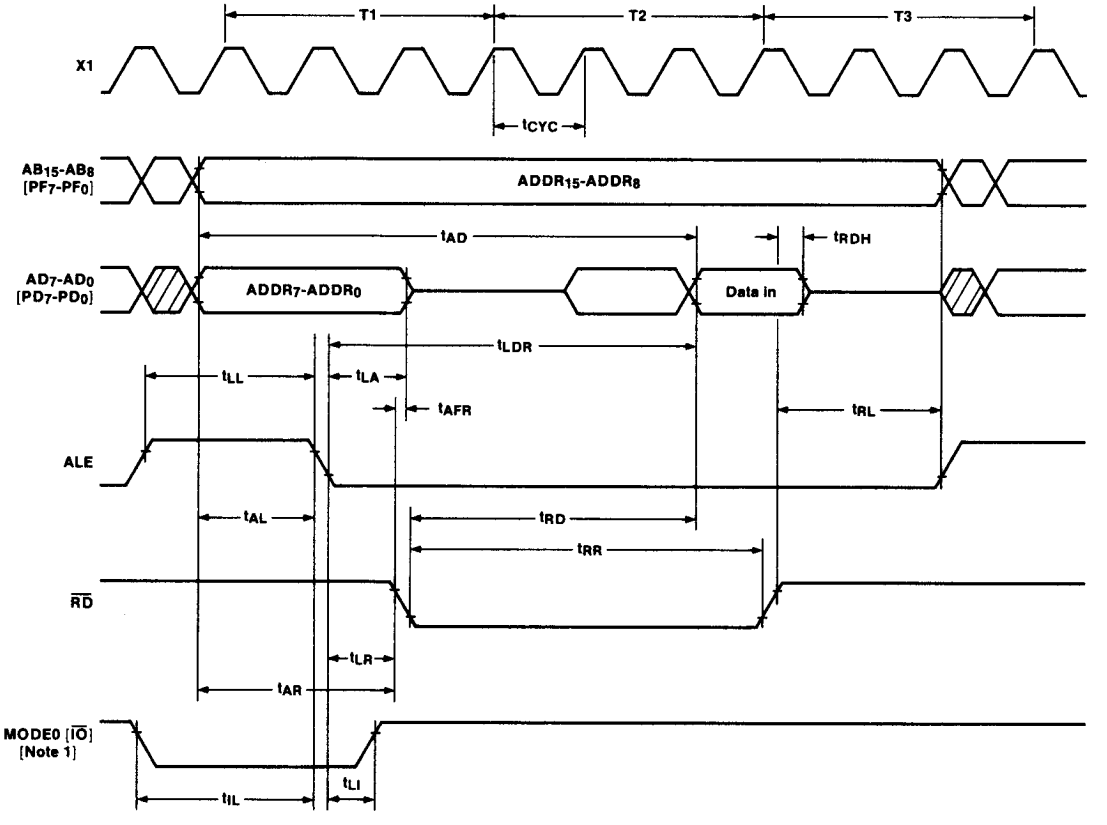
Data Retention Timing



T = 67.8 ns @ 14.7456 MHz

Timing Waveforms

Read Operation



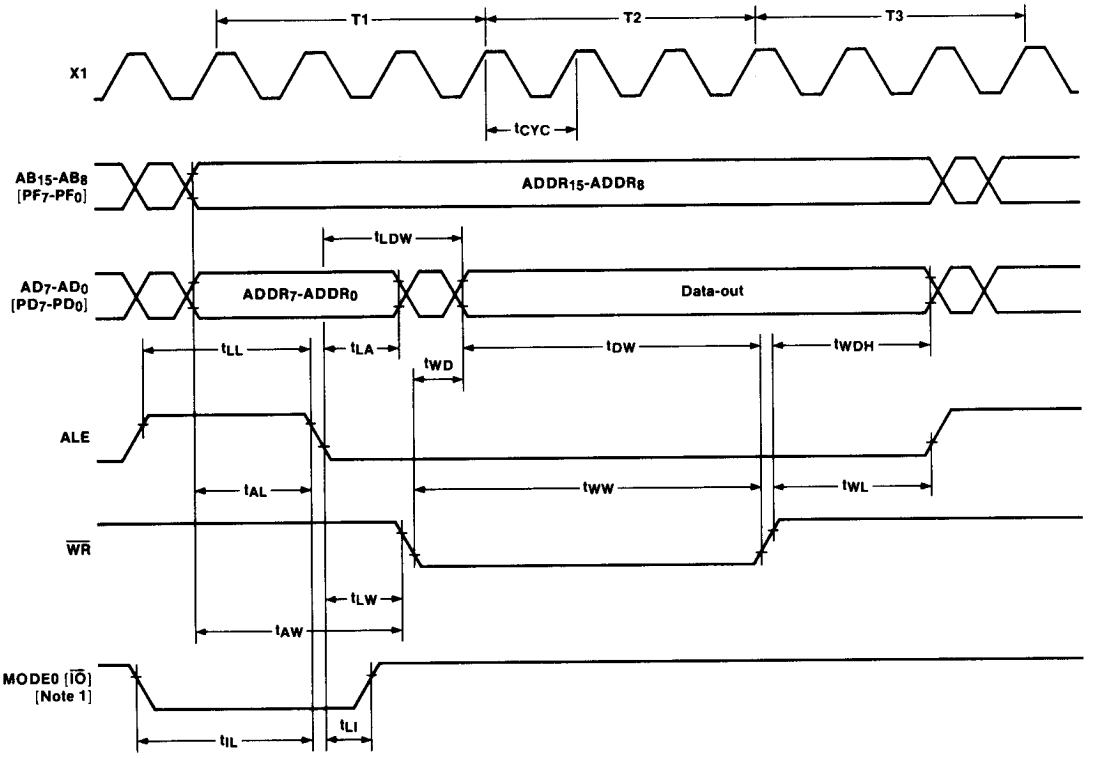
Note:

[1] $\overline{IO}$ signal is output to the MODE0 pin [if MODE0 is pulled up to V_{DD}] during a read or write of special registers sr-sr2 or a write to register MM or MF. Refer to description of Port Emulation Mode [PEM] in the User's Manual for further explanation.

83-004276B

Timing Waveforms (cont)

Write Operation



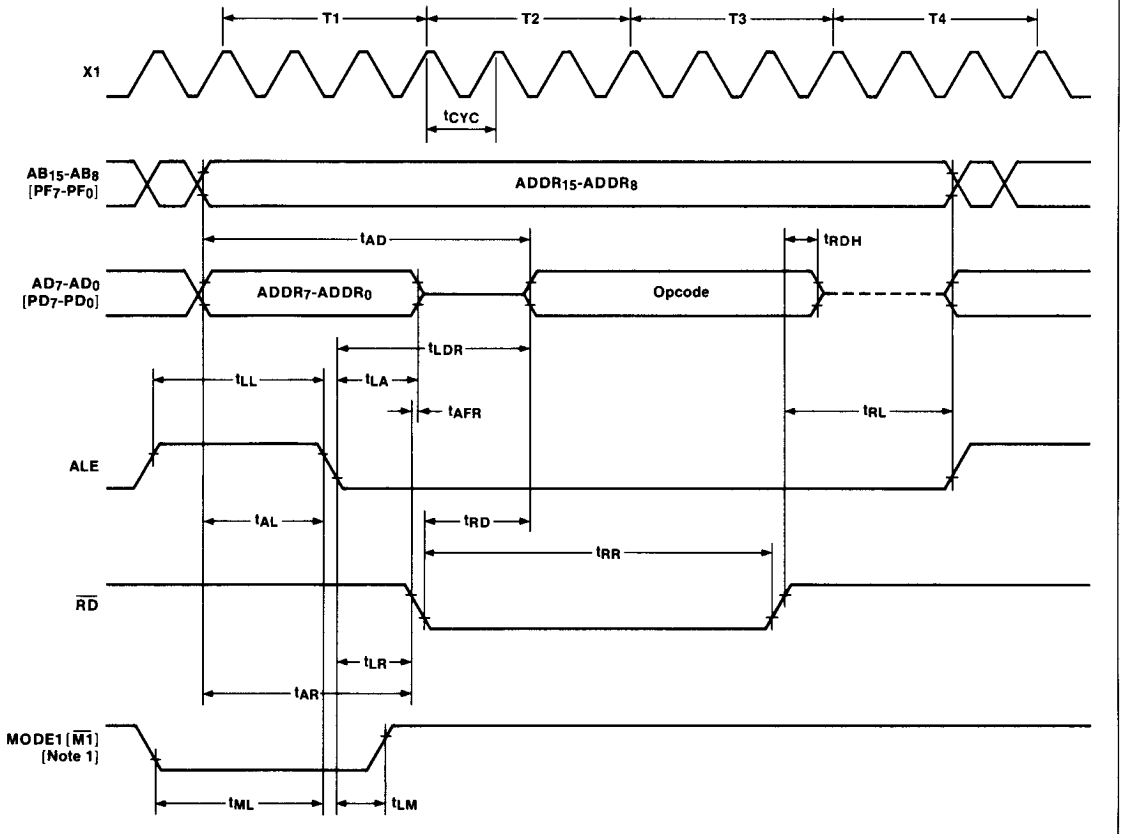
Note:

[1] $\overline{IO}$ signal is output to the MODE0 pin [if MODE0 is pulled up to V_{DD}] during a read or write of special registers sr-sr2 or a write to register MM or MF. Refer to description of Port Emulation Mode [PEM] in the User's Manual for further explanation.

83-004278B

Timing Waveforms (cont)

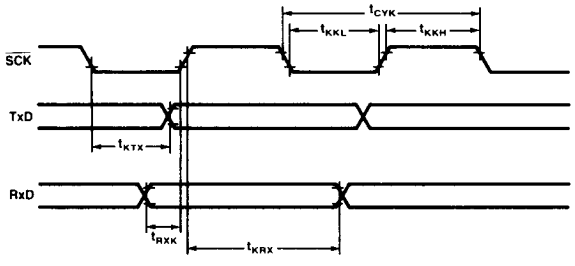
Opcode Fetch Operation



Note:
[1] $\overline{M1}$ signal is output to the MODE1 pin during every Opcode Fetch if MODE1 pin is pulled up to V_{DD}.

83-004279B

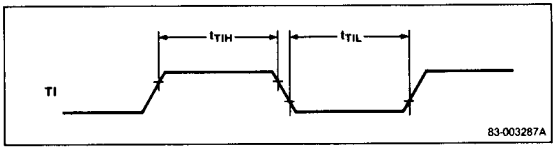
Serial Operation Transmit/Receive Timing



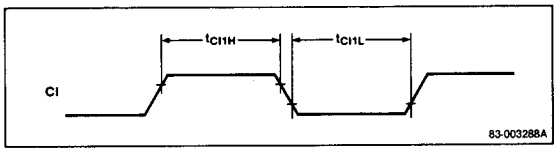
49-000546B

Timing Waveforms (cont)

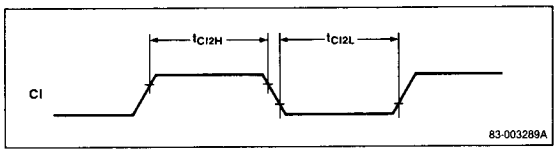
Timer Input Timing



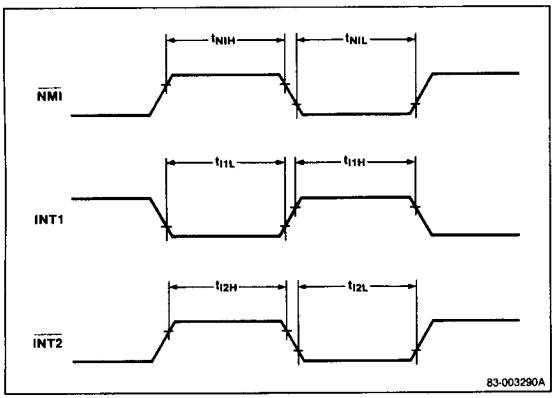
Timer/Event Counter Input Timing: Event Counter Mode



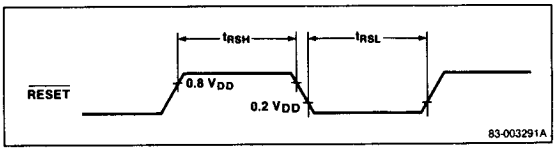
Timer/Event Counter Input Timing: Pulse Width Measurement Mode



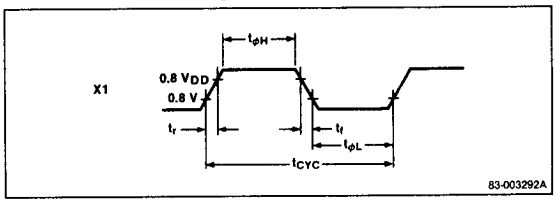
Interrupt Input Timing



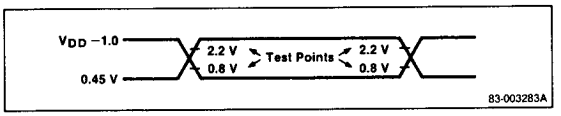
$\overline{\text{RESET}}$ Input Timing



External Clock Timing



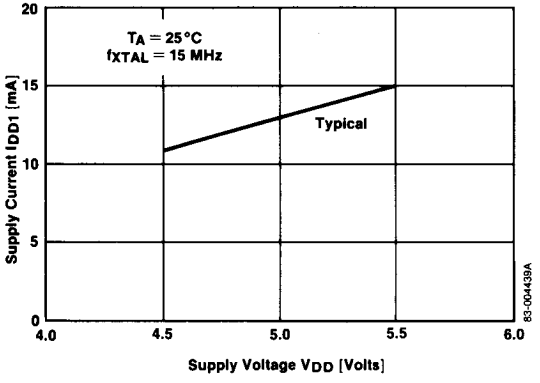
AC Timing Test Points



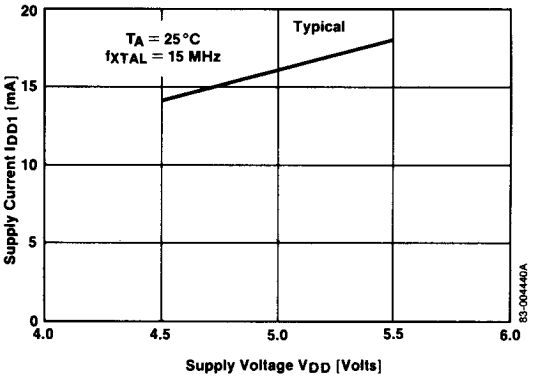
Operating Characteristics

(T_A = 25°C, V_{DD} = 5 V)

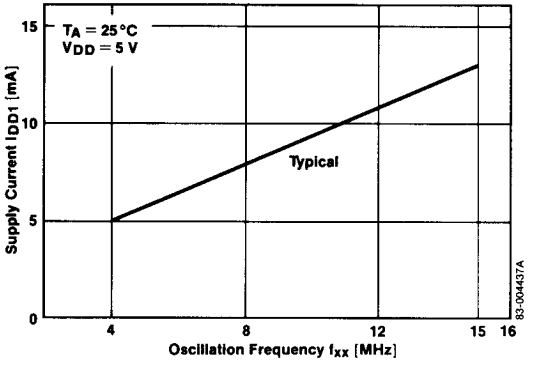
I_{DD1} vs V_{DD} [78C10 and 78C11 only]



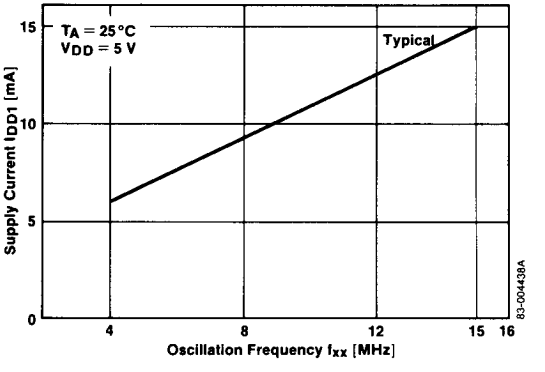
I_{DD1} vs V_{DD} [78C14 only]



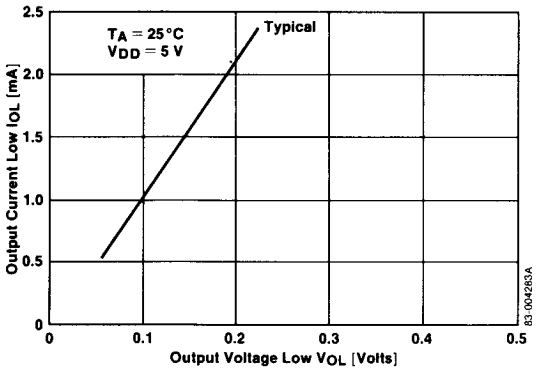
I_{DD1} vs f_{XX} [78C10 and 78C11 only]



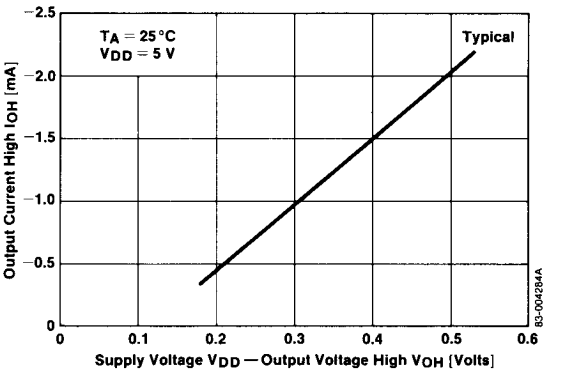
I_{DD1} vs f_{XX} [78C14 only]



I_{OL} vs V_{OL}



I_{OH} vs [V_{DD}-V_{OH}]



Operand Symbols

Symbol	Allowable Operands
Registers	
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
Special Registers	
sr	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TXB, TM0, TM1, ZCM
sr1	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM, RXB, CR0, CR1, CR2, CR3
sr2	PA, PB, PC, PD, PF, MKH, ANM, MKL, SMH, EOM, TMM
sr3	ETM0, ETM1
sr4	ECNT, ECPT
Register Pairs	
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
Register Pair Addressing	
rpa	B, D, H, D+ , H+ , D–, H–
rpa1	B, D, H
rpa2	B, D, H, D+, H+, D–, H–, D+byte, H+A, H+B, H+EA, H+byte
rpa3	D, H, D++, H++, D+byte, H+A, H+B, H+EA, H+byte
Flags	
f	CY, HC, Z
Interrupt Flags	
irf	INTFNMI, INTFT0, INTFT1, INTF1, INTF2, INTFE0, INTFE1, INTFEIN, INTFAD, INTFSR, INTFST, ER, OV, AN4, AN5, AN6, AN7, SB
Immediate Data	
wa	8-bit immediate data (low byte of working register address)
word	16-bit immediate data
byte	8-bit immediate data
bit	3-bit immediate data (b_2, b_1, b_0)

Operand Definitions

Special Registers (sr-sr4)

PA = Port A
PB = Port B
PC = Port C
PD = Port D
PF = Port F
MA = Mode A
MB = Mode B
MC = Mode C
MCC = Mode control C
MF = Mode F

MM = Memory mapping
TM0 = Timer register 0
TM1 = Timer register 1
TMM = Timing mode
ETM0 = Timer/event counter register 0
ETM1 = Timer/event counter register 1
ZCM = Zero-cross mode control register

ECNT = Timer/event counter upcounter
ECPT = Timer/event counter capture
ETMM = Timer/event counter mode

EOM = Timer/event counter output mode

TXB = Transmit buffer
RXB = Receive buffer
SMH = Serial mode high
SML = Serial mode low
MKH = Mask high
MKL = Mask low
ANM = A/D channel mode
CR0 to CR3= A/D conversion result 0-3

Register Pairs (rp-rp3)

SP = Stack pointer
B = BC
D = DE
H = HL
V = VA
EA = Extended accumulator

Register Pair Addressing (rpa-rpa3)

B = (BC)
D = (DE)
H = (HL)
D+ = (DE)+
H+ = (HL)+
D– = (DE)–
H– = (HL)–
D++ = (DE)++
H++ = (HL)++
D+byte = (DE+byte)
H+byte = (HL+byte)
H+A = (HL+A)
H+B = (HL+B)
H+EA = (HL+EA)

Flags (f)

CY = Carry
HC = Half-carry
Z = Zero

Interrupt Flags (Irf)

INTFNMI = NMI interrupt flag

INTFT0 = FT0
INTFT1 = FT1
INTF1 = F1
INTF2 = F2
INTFE0 = FE0
INTFE1 = FE1

INTFEIN = FEIN
INTFAD = FAD
INTFSR = FSR
INTFST = FST
ER = Error
OV = Overflow
AN4 to AN7 = Analog input 4-7
SB = Standby

Operand Codes

Registers (r, r2)

R_2	R_1	R_0	Reg	r	r2
0	0	0	V		
0	0	1	A		
0	1	0	B		
0	1	1	C		
1	0	0	D		
1	0	1	E		
1	1	0	H		
1	1	1	L		

Registers (r1)

T_2	T_1	T_0	Reg
0	0	0	EAH
0	0	1	EAL
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

Special Registers (sr, sr1, sr2)

S_5	S_4	S_3	S_2	S_1	S_0	Special Reg	sr	sr1	sr2
0	0	0	0	0	0	PA			
0	0	0	0	0	1	PB			
0	0	0	0	1	0	PC			
0	0	0	0	1	1	PD			
0	0	0	1	0	1	PF			
0	0	0	1	1	0	MKH			
0	0	0	1	1	1	MKL			
0	0	1	0	0	0	ANM			
0	0	1	0	0	1	SMH			
0	0	1	0	1	0	SML			
0	0	1	0	1	1	EOM			
0	0	1	1	0	0	ETMM			
0	0	1	1	0	1	TMM			
0	1	0	0	0	0	MM			
0	1	0	0	0	1	MCC			
0	1	0	0	1	0	MA			
0	1	0	0	1	1	MB			
0	1	0	1	0	0	MC			
0	1	0	1	1	1	MF			
0	1	1	0	0	0	TXB			
0	1	1	0	0	1	RXB			
0	1	1	0	1	0	TM0			
0	1	1	0	1	1	TM1			
1	0	0	0	0	0	CR0			
1	0	0	0	0	1	CR1			
1	0	0	0	1	0	CR2			
1	0	0	0	1	1	CR3			
1	0	1	0	0	0	ZCM			

Special Registers (sr3)

U_0	Special Reg
0	ETM0
1	ETM1

Special Registers (sr4)

V_0	Special Reg
0	ECNT
1	ECPT

Register Pairs (rp, rp2, rp3)

P_2	P_1	P_0	Reg Pair	rp	rp2	rp3
0	0	0	SP			
0	0	1	BC			
0	1	0	DE			
0	1	1	HL			
1	0	0	EA			

Register Pairs (rp1)

Q_2	Q_1	Q_0	Reg Pair
0	0	0	VA
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA

Register Pair Addressing (rpa, rpa1, rpa2)

A_3	A_2	A_1	A_0	Addressing	rpa	rpa1	rpa2
0	0	0	0	—			
0	0	0	1	(BC)			
0	0	1	0	(DE)			
0	0	1	1	(HL)			
0	1	0	0	(DE)+			
0	1	0	1	(HL)+			
0	1	1	0	(DE)−			
0	1	1	1	(HL)−			
1	0	1	1	(DE+byte)			
1	1	0	0	(HL+A)			
1	1	0	1	(HL+B)			
1	1	1	0	(HL+EA)			
1	1	1	1	(HL+byte)			

Register Pair Addressing (rpa3)

C_3	C_2	C_1	C_0	Addressing
0	0	1	0	(DE)
0	0	1	1	(HL)
0	1	0	0	(DE)++
0	1	0	1	(HL)++
1	0	1	1	(DE+byte)
1	1	0	0	(HL+A)
1	1	0	1	(HL+B)
1	1	1	0	(HL+EA)
1	1	1	1	(HL+byte)

Operand Codes (cont)

Flags (f)

F_2	F_1	F_0	Flag
0	0	0	—
0	1	0	CY
0	1	1	HC
1	0	0	Z

Interrupt Flags (irf)

I_4	I_3	I_2	I_1	I_0	Flag
0	0	0	0	0	NMI
0	0	0	0	1	FT0
0	0	0	1	0	FT1
0	0	0	1	1	F1
0	0	1	0	0	F2
0	0	1	0	1	FE0
0	0	1	1	0	FE1
0	0	1	1	1	FEIN
0	1	0	0	0	FAD
0	1	0	0	1	FSR
0	1	0	1	0	FST
0	1	0	1	1	ER
0	1	1	0	0	OV
1	0	0	0	0	AN4
1	0	0	0	1	AN5
1	0	0	1	0	AN6
1	0	0	1	1	AN7
1	0	1	0	0	SB

Graphic Symbols

Symbol	Description
←	Transfer direction, result
∧	Logical product (logical AND)
∨	Logical sum (logical OR)
∀	Exclusive-OR
—	Complement
•	Concatenation

Instruction Set

Mnemonic	Operand	Operation	Operation Code B1 / B3								Operation Code B2 / B4								State (Note 1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
8-Bit Data Transfer																					
MOV	r1,A	(r1) ← (A)	0	0	0	1	1	T_2	T_1	T_0									4	1	
	A, r1	(A) ← (r1)	0	0	0	0	1	T_2	T_1	T_0									4	1	
	*sr,A	(sr) ← (A)	0	1	0	0	1	1	0	1	1	1	S_5	S_4	S_3	S_2	S_1	S_0	10	2	
	*A,sr1	(A) ← (sr1)	0	1	0	0	1	1	0	0	1	1	S_5	S_4	S_3	S_2	S_1	S_0	10	2	
	r,word	(r) ← (word)	0	1	1	1	0	0	0	0	0	1	1	0	1	R_2	R_1	R_0	17	4	
			Low addr								High addr										
	word,r	(word) ← (r)	0	1	1	1	0	0	0	0	0	1	1	1	1	R_2	R_1	R_0	17	4	
			Low addr								High addr										
MVI	*r,byte	(r) ← byte	0	1	1	0	1	R_2	R_1	R_0	Data								7	2	
	sr2,byte	(sr2) ← byte	0	1	1	0	0	1	0	0	S_3	0	0	0	0	S_2	S_1	S_0	14	3	
			Data																		
MVIW	*wa, byte	((V)•(wa)) ← byte	0	1	1	1	0	0	0	1	Offset								13	3	
			Data																		
MVIX	*rpa1,byte	(rpa1) ← byte	0	1	0	0	1	0	A_1	A_0	Data								10	2	
STAW	*wa	((V)•(wa)) ← (A)	0	1	1	0	0	0	1	1	Offset								10	2	
LDAW	*wa	(A) ← ((V)•(wa))	0	0	0	0	0	0	0	1	Offset								10	2	
STAX	*rpa2	((rpa2)) ← (A)	A_3	0	1	1	1	A_2	A_1	A_0	Data (Note 2)								7/13 (Note 3)	2	
LDAX	*rpa2	(A) ← ((rpa2))	A_3	0	1	0	1	A_2	A_1	A_0	Data (Note 2)								7/13 (Note 3)	2	
EXX		(B) ↔ (B'), (C) ↔ (C'), (D) ↔ (D') (E) ↔ (E'), (H) ↔ (H'), (L) ↔ (L')	0	0	0	1	0	0	0	1									4	1	
EXA		(V) ↔ (V'), (A) ↔ (A'), (EA) ↔ (EA')	0	0	0	1	0	0	0	0									4	1	
EXH		(H) ↔ (H'), (L) ↔ (L')	0	1	0	1	0	0	0	0									4	1	
BLOCK		((DE)) ← ((HL)), (DE) ← (DE) + 1, (HL) ← (HL) + 1, (C) ← (C) − 1 End if borrow	0	0	1	1	0	0	0	1									13 x (C + 1)	1	
16-Bit Data Transfer																					
DMOV	rp3, EA	($rp3_L$) ← (EAL), ($rp3_H$) ← (EAH)	1	0	1	1	0	1	P_1	P_0									4	1	
	EA,rp3	(EAL) ← ($rp3_L$), (EAH) ← ($rp3_H$)	1	0	1	0	0	1	P_1	P_0									4	1	

Notes:

(1) For the skip condition, the idle states are as follows:
- 1-byte instruction: 4 states
- 2-byte instruction: 8 states
- 3-byte instruction: 11 states
- 2-byte instruction (with *): 7 states
- 3-byte instruction (with *): 10 states
- 4-byte instruction: 14 states

(2) B2 (Data): rpa2 = D+byte or H+byte.

(3) Right side of slash (/) in states indicates case rpa2 or rpa3 = D+byte, H+A, H+B, H+EA, or H+byte.

(4) B3 (Data): rpa3 = D+byte or H+byte.

NEC

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3	Operation Code B2 / B4	State (Note 1)	Bytes	Skip Condition
16-Bit Data Transfer (cont)							
DMOV	sr3, EA	(sr3) ← (EA)	0 1 0 0 1 0 0 0	1 1 0 1 0 0 1 U_0	14	2	
	EA,sr4	(EA) ← (sr4)	0 1 0 0 1 0 0 0	1 1 0 0 0 0 0 V_0	14	2	
SBCD	word	(word) ← (C), (word + 1) ← (B)	0 1 1 1 0 0 0 0 Low addr	0 0 0 1 1 1 1 0 High addr	20	4	
SDED	word	(word) ← (E), (word + 1) ← (D)	0 1 1 1 0 0 0 0 Low addr	0 0 1 0 1 1 1 0 High addr	20	4	
SHLD	word	(word) ← (L), (word + 1) ← (H)	0 1 1 1 0 0 0 0 Low addr	0 0 1 1 1 1 1 0 High addr	20	4	
SSPD	word	(word) ← (SP_L), (word + 1) ← (SP_H)	0 1 1 1 0 0 0 0 Low addr	0 0 0 0 1 1 1 0 High addr	20	4	
STEAX	rpa3	((rpa3)) ← (EAL), (((rpa3)) + 1)) ← (EAH)	0 1 0 0 1 0 0 0 Data (Note 4)	1 0 0 1 C_3 C_2 C_1 C_0	14/20 (Note 3)	3	
LBCD	word	(C) ← (word), (B) ← (word + 1)	0 1 1 1 0 0 0 0 Low addr	0 0 0 1 1 1 1 1 High addr	20	4	
LDED	word	(E) ← (word), (D) ← (word + 1)	0 1 1 1 0 0 0 0 Low addr	0 0 1 0 1 1 1 1 High addr	20	4	
LHLD	word	(L) ← (word), (H) ← (word + 1)	0 1 1 1 0 0 0 0 Low addr	0 0 1 1 1 1 1 1 High addr	20	4	
LSPD	word	(SP_L) ← (word), (SP_H) ← (word + 1)	0 1 1 1 0 0 0 0 Low addr	0 0 0 0 1 1 1 1 High addr	20	4	
LDEAX	rpa3	(EAL) ← ((rpa3)), (EAH) ← (((rpa3) + 1))	0 1 0 0 1 0 0 0 Data (Note 4)	1 0 0 0 C_3 C_2 C_1 C_0	14/20 (Note 3)	3	
PUSH	rp1	(((SP) − 1)) ← ($rp1_H$), (((SP) − 2)) ← ($rp1_L$), (SP) ← (SP) − 2	1 0 1 1 0 Q_2 Q_1 Q_0		13	1	
POP	rp1	($rp1_L$) ← ((SP)), ($rp1_H$) ← (((SP) + 1)), (SP) ← (SP) + 2	1 0 1 0 0 Q_2 Q_1 Q_0		10	1	
LXI	*rp2,word	(rp2) ← (word)	0 P_2 P_1 P_0 0 1 0 0 High byte	Low byte	10	3	
TABLE		(C) ← (((PC) + 3 + (A))), (B) ← (((PC) + 3 + (A) + 1))	0 1 0 0 1 0 0 0	1 0 1 0 1 0 0 0	17	2	
8-Bit Arithmetic [Register]							
ADD	A,r	(A) ← (A) + (r)	0 1 1 0 0 0 0 0	1 1 0 0 0 R_2 R_1 R_0	8	2	
	r,A	(r) ← (r) + (A)	0 1 1 0 0 0 0 0	0 1 0 0 0 R_2 R_1 R_0	8	2	
ADC	A,r	(A) ← (A) + (r) + (CY)	0 1 1 0 0 0 0 0	1 1 0 1 0 R_2 R_1 R_0	8	2	
	r,A	(r) ← (r) + (A) + (CY)	0 1 1 0 0 0 0 0	0 1 0 1 0 R_2 R_1 R_0	8	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code																State (Note 1)	Bytes	Skip Condition
			B1 / B3								B2 / B4										
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
8-Bit Arithmetic [Register] (cont)																					
ADDNC	A,r	(A) ← (A) + (r)	0	1	1	0	0	0	0	0	1	0	1	0	0	R_2	R_1	R_0	8	2	No carry
	r,A	(r) ← (r) + (A)	0	1	1	0	0	0	0	0	0	0	1	0	0	R_2	R_1	R_0	8	2	No carry
SUB	A,r	(A) ← (A) − (r)	0	1	1	0	0	0	0	0	1	1	1	0	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) − (A)	0	1	1	0	0	0	0	0	0	1	1	0	0	R_2	R_1	R_0	8	2	
SBB	A,r	(A) ← (A) − (r) − (CY)	0	1	1	0	0	0	0	0	1	1	1	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) − (A) − (CY)	0	1	1	0	0	0	0	0	0	1	1	1	0	R_2	R_1	R_0	8	2	
SUBNB	A,r	(A) ← (A) − (r)	0	1	1	0	0	0	0	0	1	0	1	1	0	R_2	R_1	R_0	8	2	No borrow
	r,A	(r) ← (r) − (A)	0	1	1	0	0	0	0	0	0	0	1	1	0	R_2	R_1	R_0	8	2	No borrow
ANA	A,r	(A) ← (A) ∧ (r)	0	1	1	0	0	0	0	0	1	0	0	0	1	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∧ (A)	0	1	1	0	0	0	0	0	0	0	0	0	1	R_2	R_1	R_0	8	2	
ORA	A,r	(A) ← (A) ∨ (r)	0	1	1	0	0	0	0	0	1	0	0	1	1	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∨ (A)	0	1	1	0	0	0	0	0	0	0	0	1	1	R_2	R_1	R_0	8	2	
XRA	A,r	(A) ← (A) ⊻ (r)	0	1	1	0	0	0	0	0	1	0	0	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ⊻ (A)	0	1	1	0	0	0	0	0	0	0	0	1	0	R_2	R_1	R_0	8	2	
GTA	A,r	(A) − (r) − 1	0	1	1	0	0	0	0	0	1	0	1	0	1	R_2	R_1	R_0	8	2	No borrow
	r,A	(r) − (A) − 1	0	1	1	0	0	0	0	0	0	0	1	0	1	R_2	R_1	R_0	8	2	No borrow
LTA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	0	1	1	1	R_2	R_1	R_0	8	2	Borrow
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	0	1	1	1	R_2	R_1	R_0	8	2	Borrow
NEA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	1	1	0	1	R_2	R_1	R_0	8	2	No zero
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	1	1	0	1	R_2	R_1	R_0	8	2	No zero
EQA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	1	1	1	1	R_2	R_1	R_0	8	2	Zero
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	1	1	1	1	R_2	R_1	R_0	8	2	Zero
ONA	A,r	(A) ∧ (r)	0	1	1	0	0	0	0	0	1	1	0	0	1	R_2	R_1	R_0	8	2	No zero
OFFA	A,r	(A) ∧ (r)	0	1	1	0	0	0	0	0	1	1	0	1	1	R_2	R_1	R_0	8	2	Zero
8-Bit Arithmetic (Memory)																					
ADDX	rpa	(A) ← (A) + ((rpa))	0	1	1	1	0	0	0	0	1	1	0	0	0	A_2	A_1	A_0	11	2	
ADCX	rpa	(A) ← (A) + ((rpa)) + (CY)	0	1	1	1	0	0	0	0	1	1	0	1	0	A_2	A_1	A_0	11	2	
ADDNCX	rpa	(A) ← (A) + ((rpa))	0	1	1	1	0	0	0	0	1	0	1	0	0	A_2	A_1	A_0	11	2	No carry
SUBX	rpa	(A) ← (A) − ((rpa))	0	1	1	1	0	0	0	0	1	1	1	0	0	A_2	A_1	A_0	11	2	
SBBX	rpa	(A) ← (A) − ((rpa)) − (CY)	0	1	1	1	0	0	0	0	1	1	1	1	0	A_2	A_1	A_0	11	2	
SUBNBX	rpa	(A) ← (A) − ((rpa))	0	1	1	1	0	0	0	0	1	0	1	1	0	A_2	A_1	A_0	11	2	No borrow
ANAX	rpa	(A) ← (A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	0	1	A_2	A_1	A_0	11	2	
ORAX	rpa	(A) ← (A) ∨ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	1	1	A_2	A_1	A_0	11	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1	B2	B3	B4	State (Note 1)	Bytes	Skip Condition
8-Bit Arithmetic (Memory) (cont)									
XRAX	rpa	(A) ← (A)∀((rpa))	01110000	10010	A_2 A_1 A_0		11	2	
GTAX	rpa	(A) − ((rpa)) − 1	01110000	10101	A_2 A_1 A_0		11	2	No borrow
LTAX	rpa	(A) − ((rpa))	01110000	10111	A_2 A_1 A_0		11	2	Borrow
NEAX	rpa	(A) − ((rpa))	01110000	11101	A_2 A_1 A_0		11	2	No zero
EQAX	rpa	(A) − ((rpa))	01110000	11111	A_2 A_1 A_0		11	2	Zero
ONAX	rpa	(A) ∧ ((rpa))	01110000	11001	A_2 A_1 A_0		11	2	No zero
OFFAX	rpa	(A) ∧ ((rpa))	01110000	11011	A_2 A_1 A_0		11	2	Zero
Immediate Data									
ADI	*A,byte	(A) ← (A) + byte	01000110	Data			7	2	
	r,byte	(r) ← (r) + byte	01110100	Data	01000	R_2 R_1 R_0	11	3	
	sr2, byte	(sr2) ← (sr2) + byte	01100100	Data	S_3 10000	S_2 S_1 S_0	20	3	
ACI	*A,byte	(A) ← (A) + byte + (CY)	01010110	Data			7	2	
	r,byte	(r) ← (r) + byte + (CY)	01110100	Data	01010	R_2 R_1 R_0	11	3	
	sr2,byte	(sr2) ← (sr2) + byte + (CY)	01100100	Data	S_3 10100	S_2 S_1 S_0	20	3	
ADINC	*A,byte	(A) ← (A) + byte	00100110	Data			7	2	No carry
	r,byte	(r) ← (r) + byte	01110100	Data	00100	R_2 R_1 R_0	11	3	No carry
	sr2,byte	(sr2) ← (sr2) + byte	01100100	Data	S_3 01000	S_2 S_1 S_0	20	3	No carry
SUI	*A,byte	(A) ← (A) − byte	01100110	Data			7	2	
	r,byte	(r) ← (r) − byte	01110100	Data	00110	R_2 R_1 R_0	11	3	
	sr2,byte	(sr2) ← (sr2) − byte	01100100	Data	S_3 11000	S_2 S_1 S_0	20	3	
SBI	*A,byte	(A) ← (A) − byte − (CY)	01110110	Data			7	2	
	r,byte	(r) ← (r) − byte − (CY)	01110100	Data	00111	R_2 R_1 R_0	11	3	
	sr2,byte	(sr2) ← (sr2) − byte − (CY)	01100100	Data	S_3 11100	S_2 S_1 S_0	20	3	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3								Operation Code B2 / B4								State (Note 1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
Immediate Data (cont)																					
SUINB	*A,byte	(A) ← (A) – byte	0	0	1	1	0	1	1	0	Data								7	2	No borrow
	r,byte	(r) ← (r) – byte	0	1	1	1	0	1	0	0	0	0	1	1	0	R_2	R_1	R_0	11	3	No borrow
			Data																		
	sr2,byte	(sr2) ← (sr2) – byte	0	1	1	0	0	1	0	0	S_3	0	1	1	0	S_2	S_1	S_0	20	3	No borrow
			Data																		
ANI	*A,byte	(A) ← (A) ∧ byte	0	0	0	0	0	1	1	1	Data								7	2	
	r,byte	(r) ← (r) ∧ byte	0	1	1	1	0	1	0	0	0	0	0	0	1	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) ∧ byte	0	1	1	0	0	1	0	0	S_3	0	0	0	1	S_2	S_1	S_0	20	3	
			Data																		
ORI	*A,byte	(A) ← (A) V byte	0	0	0	1	0	1	1	1	Data								7	2	
	r,byte	(r) ← (r) V byte	0	1	1	1	0	1	0	0	0	0	0	1	1	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) V byte	0	1	1	0	0	1	0	0	S_3	0	0	1	1	S_2	S_1	S_0	20	3	
			Data																		
XRI	*A,byte	(A) ← (A) ∀ byte	0	0	0	1	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) ∀ byte	0	1	1	1	0	1	0	0	0	0	0	1	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) ∀ byte	0	1	1	0	0	1	0	0	S_3	0	0	1	0	S_2	S_1	S_0	20	3	
			Data																		
GTI	*A,byte	(A) – byte – 1	0	0	1	0	0	1	1	1	Data								7	2	No borrow
	r,byte	(r) – byte – 1	0	1	1	1	0	1	0	0	0	0	1	0	1	R_2	R_1	R_0	11	3	No borrow
			Data																		
	sr2,byte	(sr2) – byte – 1	0	1	1	0	0	1	0	0	S_3	0	1	0	1	S_2	S_1	S_0	14	3	No borrow
			Data																		
LTI	*A,byte	(A) – byte	0	0	1	1	0	1	1	1	Data								7	2	Borrow
	r,byte	(r) – byte	0	1	1	1	0	1	0	0	0	0	1	1	1	R_2	R_1	R_0	11	3	Borrow
			Data																		
	sr2,byte	(sr2) – byte	0	1	1	0	0	1	0	0	S_3	0	1	1	1	S_2	S_1	S_0	14	3	Borrow
			Data																		
NEI	*A,byte	(A) – byte	0	1	1	0	0	1	1	1	Data								7	2	No zero
	r,byte	(r) – byte	0	1	1	1	0	1	0	0	0	1	1	0	1	R_2	R_1	R_0	11	3	No zero
			Data																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3								Operation Code B2 / B4								State (Note 1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
Immediate Data (cont)																					
NEI	sr2,byte	(sr2) – byte	0	1	1	0	0	1	0	0	S_3	1	1	0	1	S_2	S_1	S_0	14	3	No zero
			Data																		
EQI	*A,byte	(A) – byte	0	1	1	1	0	1	1	1	Data								7	2	Zero
	r,byte	(r) – byte	0	1	1	1	0	1	0	0	0	1	1	1	1	R_2	R_1	R_0	11	3	Zero
			Data																		
	sr2,byte	(sr2) – byte	0	1	1	0	0	1	0	0	S_3	1	1	1	1	S_2	S_1	S_0	14	3	Zero
			Data																		
ONI	*A,byte	(A) ∧ byte	0	1	0	0	0	1	1	1	Data								7	2	No zero
	r,byte	(r) ∧ byte	0	1	1	1	0	1	0	0	0	1	0	0	1	R_2	R_1	R_0	11	3	No zero
			Data																		
	sr2,byte	(sr2) ∧ byte	0	1	1	0	0	1	0	0	S_3	1	0	0	1	S_2	S_1	S_0	14	3	No zero
			Data																		
OFFI	*A,byte	(A) ∧ byte	0	1	0	1	0	1	1	1	Data								7	2	Zero
	r,byte	(r) ∧ byte	0	1	1	1	0	1	0	0	0	1	0	1	1	R_2	R_1	R_0	11	3	Zero
			Data																		
	sr2,byte	(sr2) ∧ byte	0	1	1	0	0	1	0	0	S_3	1	0	1	1	S_2	S_1	S_0	14	3	Zero
			Data																		
Working Register																					
ADDW	wa	(A) ← (A) + ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	0	0	0	0	0	0	14	3	
			Offset																		
ADCW	wa	(A) ← (A) + ((V)•(wa)) + (CY)	0	1	1	1	0	1	0	0	1	1	0	1	0	0	0	0	14	3	
			Offset																		
ADDNCW	wa	(A) ← (A) + ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	1	0	0	0	0	0	14	3	No carry
			Offset																		
SUBW	wa	(A) ← (A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	1	0	0	0	0	0	14	3	
			Offset																		
SBBW	wa	(A) ← (A) – ((V)•(wa)) – (CY)	0	1	1	1	0	1	0	0	1	1	1	1	0	0	0	0	14	3	
			Offset																		
SUBNBW	wa	(A) ← (A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	1	1	0	0	0	0	14	3	No borrow
			Offset																		
ANAW	wa	(A) ← (A) ∧ ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	0	0	1	0	0	0	14	3	
			Offset																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3 7 6 5 4 3 2 1 0	Operation Code B2 / B4 7 6 5 4 3 2 1 0	State (Note 1)	Bytes	Skip Condition
Working Register (cont)							
ORAW	wa	(A) ← (A) V ((V)•(wa))	0 1 1 1 0 1 0 0 / Offset	1 0 0 1 1 0 0 0	14	3	
XRAW	wa	(A) ← (A)⊻((V)•(wa))	0 1 1 1 0 1 0 0 / Offset	1 0 0 1 0 0 0 0	14	3	
GTAW	wa	(A) – ((V)•(wa)) – 1	0 1 1 1 0 1 0 0 / Offset	1 0 1 0 1 0 0 0	14	3	No borrow
LTAW	wa	(A) – ((V)•(wa))	0 1 1 1 0 1 0 0 / Offset	1 0 1 1 1 0 0 0	14	3	Borrow
NEAW	wa	(A) – ((V)•(wa))	0 1 1 1 0 1 0 0 / Offset	1 1 1 0 1 0 0 0	14	3	No zero
EQAW	wa	(A) – ((V)•(wa))	0 1 1 1 1 1 0 0 / Offset	1 1 1 1 1 0 0 0	14	3	Zero
ONAW	wa	(A) ∧ ((V)•(wa))	0 1 1 1 0 1 0 0 / Offset	1 1 0 0 1 0 0 0	14	3	No zero
OFFAW	wa	(A) ∧ ((V)•(wa))	0 1 1 1 0 1 0 0 / Offset	1 1 0 1 1 0 0 0	14	3	Zero
ANIW	*wa,byte	((V)•(wa)) ← ((V)•(wa)) ∧ byte	0 0 0 0 0 1 0 1 / Data	Offset	19	3	
ORIW	*wa,byte	((V)•(wa)) ← ((V)•(wa)) V byte	0 0 0 1 0 1 0 1 / Data	Offset	19	3	
GTIW	*wa,byte	((V)•(wa)) – byte – 1	0 0 1 0 0 1 0 1 / Data	Offset	13	3	No borrow
LTIW	*wa,byte	((V)•(wa)) – byte	0 0 1 1 0 1 0 1 / Data	Offset	13	3	Borrow
NEIW	*wa,byte	((V)•(wa)) – byte	0 1 1 0 0 1 0 1 / Data	Offset	13	3	No zero
EQIW	*wa,byte	((V)•(wa)) – byte	0 1 1 1 0 1 0 1 / Data	Offset	13	3	Zero
ONIW	*wa,byte	((V)•(wa)) ∧ byte	0 1 0 0 0 1 0 1 / Data	Offset	13	3	No zero
OFFIW	*wa,byte	((V)•(wa)) ∧ byte	0 1 0 1 0 1 0 1 / Data	Offset	13	3	Zero

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3								Operation Code B2 / B4								State (Note 1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
16-Bit Arithmetic																					
EADD	EA,r2	(EA) ← (EA) + (r2)	0	1	1	1	0	0	0	0	0	1	0	0	0	0	R_1	R_0	11	2	
DADD	EA,rp3	(EA) ← (EA) + (rp3)	0	1	1	1	0	1	0	0	1	1	0	0	0	1	P_1	P_0	11	2	
DADC	EA,rp3	(EA) ← (EA) + (rp3) + (CY)	0	1	1	1	0	1	0	0	1	1	0	1	0	1	P_1	P_0	11	2	
DADDNC	EA,rp3	(EA) ← (EA) + (rp3)	0	1	1	1	0	1	0	0	1	0	1	0	0	1	P_1	P_0	11	2	No carry
ESUB	EA,r2	(EA) ← (EA) − (r2)	0	1	1	1	0	0	0	0	0	1	1	0	0	0	R_1	R_0	11	2	
DSUB	EA,rp3	(EA) ← (EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	0	0	1	P_1	P_0	11	2	
DSBB	EA,rp3	(EA) ← (EA) − (rp3) − (CY)	0	1	1	1	0	1	0	0	1	1	1	1	0	1	P_1	P_0	11	2	
DSUBNB	EA,rp3	(EA) ← (EA) − (rp3)	0	1	1	1	0	1	0	0	1	0	1	1	0	1	P_1	P_0	11	2	No borrow
DAN	EA,rp3	(EA) ← (EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	0	0	0	1	1	P_1	P_0	11	2	
DOR	EA,rp3	(EA) ← (EA) ∨ (rp3)	0	1	1	1	0	1	0	0	1	0	0	1	1	1	P_1	P_0	11	2	
DXR	EA,rp3	(EA) ← (EA) ∨̄ (rp3)	0	1	1	1	0	1	0	0	1	0	0	1	0	1	P_1	P_0	11	2	
DGT	EA,rp3	(EA) − (rp3) − 1	0	1	1	1	0	1	0	0	1	0	1	0	1	1	P_1	P_0	11	2	No borrow
DLT	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	0	1	1	1	1	P_1	P_0	11	2	Borrow
DNE	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	0	1	1	P_1	P_0	11	2	No zero
DEQ	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	1	1	1	P_1	P_0	11	2	Zero
DON	EA,rp3	(EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	1	0	0	1	1	P_1	P_0	11	2	No zero
DOFF	EA,rp3	(EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	1	0	1	1	1	P_1	P_0	11	2	Zero
Multiply/Divide																					
MUL	r2	(EA) ← (A) x (r2)	0	1	0	0	1	0	0	0	0	0	1	0	1	1	R_1	R_0	32	2	
DIV	r2	(EA) ← (EA) ÷ (r2), (r2) ← Remainder	0	1	0	0	1	0	0	0	0	0	1	1	1	1	R_1	R_0	59	2	
Increment/Decrement																					
INR	r2	(r2) ← (r2) + 1	0	1	0	0	0	0	R_1	R_0									4	1	Carry
INRW	*wa	((V)•(wa)) ← ((V)•(wa)) + 1	0	0	1	0	0	0	0	0				Offset					16	2	Carry
INX	rp	(rp) ← (rp) + 1	0	0	P_1	P_0	0	0	1	0									7	1	
	EA	(EA) ← (EA) + 1	1	0	1	0	1	0	0	0									7	1	
DCR	r2	(r2) ← (r2) − 1	0	1	0	1	0	0	R_1	R_0									4	1	Borrow
DCRW	*wa	((V)•(wa)) ← ((V)•(wa)) − 1	0	0	1	1	0	0	0	0				Offset					16	2	Borrow
DCX	rp	(rp) ← (rp) − 1	0	0	P_1	P_0	0	0	1	1									7	1	
	EA	(EA) ← (EA) − 1	1	0	1	0	1	0	0	1									7	1	
Others																					
DAA		Decimal Adjust Accumulator	0	1	1	0	0	0	0	1									4	1	
STC		(CY) ← 1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	1	8	2	
CLC		(CY) ← 0	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	0	8	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	State (Note 1)	Bytes	Skip Condition
			B1			B3					B2			B4							
Others (cont)																					
NEGA		(A) ← $(\overline{A})$ + 1	0	1	0	0	1	0	0	0	0	0	1	1	1	0	1	0	8	2	
Rotate and Shift																					
RLD		Rotate left digit (A_{3-0}) ← $((HL))_{7-4}$, $((HL))_{7-4}$ ← $((HL))_{3-0}$, $((HL))_{3-0}$ ← (A_{3-0})	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	0	17	2	
RRD		Rotate right digit (A_{3-0}) ← $((HL))_{3-0}$, $((HL))_{7-4}$ ← $((HL))_{3-0}$, $((HL))_{7-4}$ ← (A_{3-0})	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	1	17	2	
RLL	r2	$(r2_{m+1})$ ← $(r2_m)$, $(r2_0)$ ← (CY), (CY) ← $(r2_7)$	0	1	0	0	1	0	0	0	0	0	1	1	0	1	R_1	R_0	8	2	
RLR	r2	$(r2_{m-1})$ ← $(r2_m)$, $(r2_7)$ ← (CY), (CY) ← $(r2_0)$	0	1	0	0	1	0	0	0	0	0	1	1	0	0	R_1	R_0	8	2	
SLL	r2	$(r2_{m+1})$ ← $(r2_m)$, $(r2_0)$ ← 0, (CY) ← $(r2_7)$	0	1	0	0	1	0	0	0	0	0	1	0	0	1	R_1	R_0	8	2	
SLR	r2	$(r2_{m-1})$ ← $(r2_m)$, $(r2_7)$ ← 0, (CY) ← $(r2_0)$	0	1	0	0	1	0	0	0	0	0	1	0	0	0	R_1	R_0	8	2	
SLLC	r2	$(r2_{m+1})$ ← $(r2_m)$, $(r2_0)$ ← 0, (CY) ← $(r2_7)$	0	1	0	0	1	0	0	0	0	0	0	0	0	1	R_1	R_0	8	2	Carry
SLRC	r2	$(r2_{m-1})$ ← $(r2_m)$, $(r2_7)$ ← 0, (CY) ← $(r2_0)$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	R_1	R_0	8	2	Carry
DRLL	EA	(EA_{n+1}) ← (EA_n), (EA_0) ← (CY), (CY) ← (EA_{15})	0	1	0	0	1	0	0	0	1	0	1	1	0	1	0	0	8	2	
DRLR	EA	(EA_{n-1}) ← (EA_n), (EA_{15}) ← (CY), (CY) ← (EA_0)	0	1	0	0	1	0	0	0	1	0	1	1	0	0	0	0	8	2	
DSLL	EA	(EA_{n+1}) ← (EA_n), (EA_0) ← 0, (CY) ← (EA_{15})	0	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0	8	2	
DSLR	EA	(EA_{n-1}) ← (EA_n), (EA_{15}) ← 0, (CY) ← (EA_0)	0	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	8	2	
Jump																					
JMP	*word	(PC) ← word	0	1	0	1	0	1	0	0	Low addr								10	3	
			High addr																		
JB		(PC_H) ← (B), (PC_L) ← (C)	0	0	1	0	0	0	0	1									4	1	
JR	word	(PC) ← (PC) + 1 + jdisp 1	1	1	← jdisp1 →														10	1	
JRE	*word	(PC) ← (PC) + 2 + jdisp	0	1	0	0	1	1	1	← jdisp →									10	2	
JEA		(PC) ← (EA)	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	0	8	2	
Call																					
CALL	*word	((SP) − 1) ← $((PC) + 3)_H$, ((SP) − 2) ← $((PC) + 3)_L$, (PC) ← word, (SP) ← (SP) − 2	0	1	0	0	0	0	0	0	Low addr								16	3	
			High addr																		
CALB		((SP) − 1) ← $((PC) + 2)_H$, ((SP) − 2) ← $((PC) + 2)_L$, (PC_H) ← (B), (PC_L) ← (C), (SP) ← (SP) − 2	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	1	17	2	

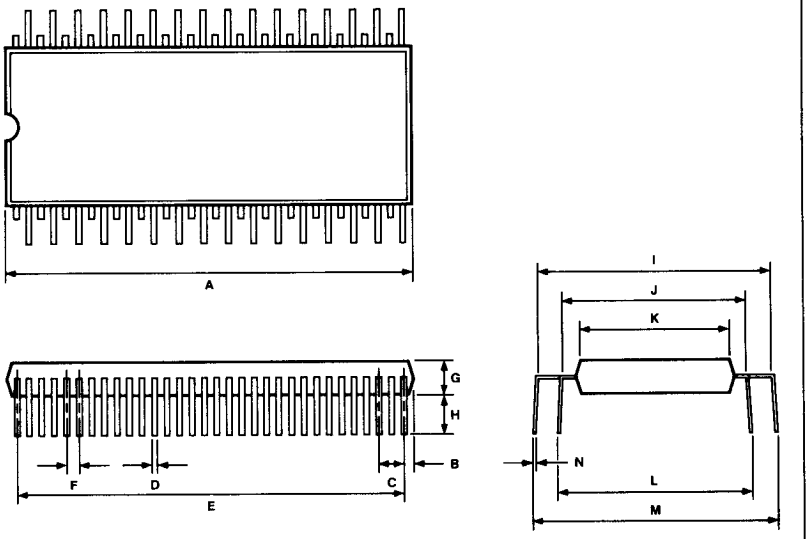
Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code (B1/B3 7 6 5 4 3 2 1 0 — B2/B4 7 6 5 4 3 2 1 0)	State (Note 1)	Bytes	Skip Condition
Call (cont)						
CALF	*word	((SP) − 1) ← ((PC) + 2)$_H$, ((SP) − 2) ← ((PC) + 2)$_L$, (PC_{15-11}) ← 00001, (PC_{10-0}) ← fa, (SP) ← (SP) − 2	0 1 1 1 1 ← fa →	13	2	
CALT	word	((SP) − 1) ← ((PC) + 1)$_H$, ((SP) − 2) ← ((PC) + 1)$_L$, (PC_L) ← (128 + 2ta), (PC_H) ← (129 + 2ta), (SP) ← (SP) − 2	1 0 0 ← ta →	16	1	
SOFTI		((SP) − 1) ← (PSW), ((SP) − 2) ← ((PC) + 1)$_H$, ((SP) − 3) ← ((PC) + 1)$_L$, (PC) ← 0060H, (SP) ← (SP) − 3	0 1 1 1 0 0 1 0	16	1	
Return						
RET		(PC_L) ← ((SP)), (PC_H) ← ((SP) + 1) (SP) ← (SP) + 2	1 0 1 1 1 0 0 0	10	1	
RETS		(PC_L) ← ((SP)), (PC_H) ← ((SP) + 1) (SP) ← (SP) + 2, (PC) ← (PC) + n	1 0 1 1 1 0 0 1	10	1	Unconditional Skip
RETI		(PC_L) ← ((SP)), (PC_H) ← ((SP) + 1) (PSW) ← ((SP) + 2), (SP) ← (SP) + 3	0 1 1 0 0 0 1 0	13	1	
Skip						
BIT	*bit, wa	Skip if ((V)•(wa)) bit = 1	0 1 0 1 1 B_2 B_1 B_0 ← Offset →	10	2	Bit Test
SK	f	Skip if f = 1	0 1 0 0 1 0 0 0 0 0 0 0 1 F_2 F_1 F_0	8	2	f = 1
SKN	f	Skip if f = 0	0 1 0 0 1 0 0 0 0 0 0 1 1 F_2 F_1 F_0	8	2	f = 0
SKIT	irf	Skip if irf = 1, then reset irf	0 1 0 0 1 0 0 0 0 1 0 I_4 I_3 I_2 I_1 I_0	8	2	irf = 1
SKNIT	irf	Skip if irf = 0 Reset irf if irf = 1 and don't skip	0 1 0 0 1 0 0 0 0 1 1 I_4 I_3 I_2 I_1 I_0	8	2	irf = 0
CPU Control						
NOP		No operation	0 0 0 0 0 0 0 0	4	1	
EI		Enable interrupt	1 0 1 0 1 0 1 0	4	1	
DI		Disable interrupt	1 0 1 1 1 0 1 0	4	1	
HLT		Set HALT mode	0 1 0 0 1 0 0 0 0 0 1 1 1 0 1 1	12	2	
STOP		Set STOP mode	0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1	12	2	

Package Drawings

64-Pin Plastic QUIP

Item	Millimeters	Inches
A	41.8 max	1.65 max
C	2.54	.100
D	.5 ±.1	.020 ±.004
E	39.37	1.55
F	1.27 min	.050 min
G	3.6	.142
H	3.2 min	.126 min
I	24.13 ±1.05	.950 ±.041
J	19.05 ±1.05	.750 ±.041
K	16.5	.650
N	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.002}$

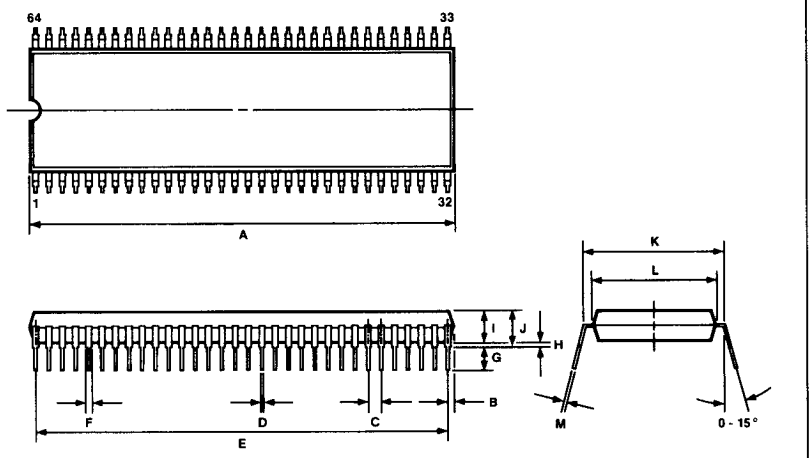


64-Pin Plastic Shrink DIP (750 mil)

Item	Millimeters	Inches
A	58.68 max	2.311 max
B	1.78 max	.07 max
C	1.778 [TP]	.07 [TP]
D	.5 ±.10	.02 $^{+.004}_{-.005}$
E	55.12	2.17
F	.9 min	.035 min
G	3.2 ±.3	.126 ±.012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.08 max	.2 max
K	19.05 [TP]	.75 [TP]
L	17	.669
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Notes:

1. Each lead centerline is located within .17 mm [.0007 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.



Package Drawings (cont)

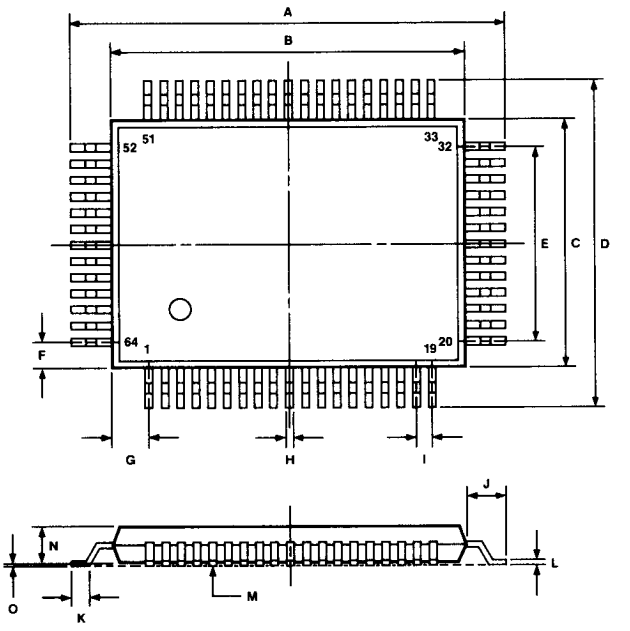
64-Pin Plastic Miniflat

Item	Millimeters	Inches
A	24.7 ±.4	.972 $^{+.017}_{-.016}$
B	20 ±.2	.795 $^{+.009}_{-.008}$
C	14 ±.2	.551 $^{+.009}_{-.008}$
D	18.7 ±.4	0.736 ±.016
E	12.0	.472
F	1.0	.039
G	1.0	.039
H	.40 ±.10	.016 $^{+.004}_{-.005}$
I	1.0 [TP] Note 1	.039 [TP]
J	2.35 ±.2	.093 $^{+.008}_{-.009}$
K	1.2 ±.2	.047 $^{+.009}_{-.008}$
L	.15 $^{+.10}_{-.05}$	.006 $^{+.004}_{-.003}$
M	.15 Note 2	.006
N	2.05 $^{+.2}_{-.1}$	.081 $^{+.008}_{-.005}$
O	0.1 ±.1	0.004 ±.004

Note:

[1] Each lead centerline is located within .20 mm [.008 inch] of its true position [TP] at maximum material condition.

[2] Flat within .15 mm [.006 inch] total.



83-000933B

Package Drawings (cont)

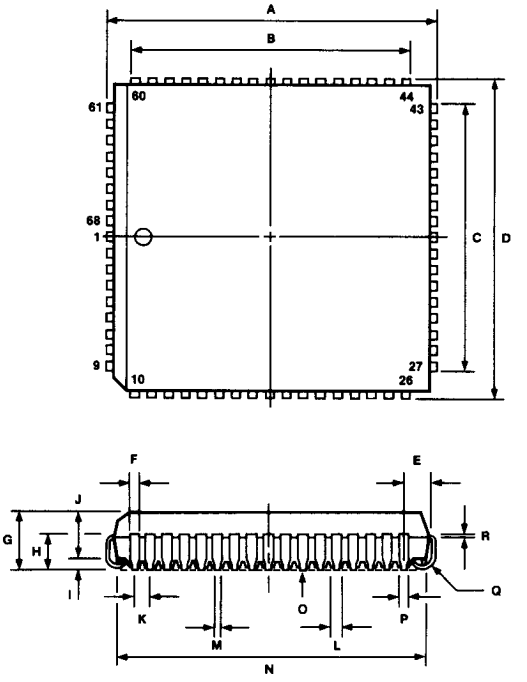
68-Pin Plastic Leaded Chip Carrier (PLCC)

Item	Millimeters	Inches
A	25.2 ±.2	.992 ±.008
B	24.20	.953
C	24.20	.953
D	25.2 ±.2	.992 ±.008
E	1.94 ±.15	.076 $^{+.007}_{-.006}$
F	.6	.024
G	4.4 ±.2	.173 $^{+.009}_{-.008}$
H	2.8 ±.2	.110 $^{+.009}_{-.008}$
I	.7 min	.028 min
J	3.6	.142
K	1.27 [TP] Note 1	.050 [TP]
L	.7	.028
M	.40 ±.10	.016 $^{+.004}_{-.005}$
N	23.12 ±.20	.910 $^{+.009}_{-.008}$
O	.15 Note 2	.006
P	1.0	.040
Q	R .8	R .031
R	.20 $^{+.10}_{-.06}$	.008 $^{+.004}_{-.002}$

Note:

[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.

[2] Flat within .15 mm [.006 inch] total.



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