NEC

MOS INTEGRATED CIRCUIT

μPD30541

VR5432™
64-/32-BIT MICROPROCESSOR

DESCRIPTION

The μPD30541 (VR5432) is a member of the VR Series™ RISC (Reduced Instruction Set Computer) microprocessors. It is a high-performance 64-/32-bit microprocessor employing the RISC architecture developed by MIPS™.

The VR5432 employs a 32-bit bus for the system interface and can operate with a protocol compatible to that of the VR4300 Series™.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.

- **VR5432 User's Manual (U13751E)**

FEATURES

- MIPS 64-bit RISC architecture
- High-speed operation processing
  - Two-way superscaler 5-stage pipeline
  - 6.6 SPECint95, 3.6 SPECfp95, 316 MIPS
- High-speed translation lookaside buffer (TLB) (48 entries)
- Address space Physical: 32 bits, Virtual: 40 bits
- Floating-point unit (FPU)
  - Supports sum-of-products instructions
- On-chip primary cache memory
  (instruction/data: 32 KB each)
- 32-bit address/data multiplexed bus
  - Operates with protocol compatible to VR4300 Series
- Maximum operating frequency
  - Internal 167 MHz, external 83.3 MHz
  - External/internal multiple selectable from ×2 to ×4
- Conforms MIPS I, II, III, and IV instruction sets. Also supports multimedia instructions
- Supply voltage
  Core block: 2.5 V ±5%
  I/O block: 3.3 V ±0.3 V

APPLICATIONS

- Set-top-box
- Page printer controller
- Amusement machines, etc.

ORDERING INFORMATION

Part Number	Package	Maximum Operating Frequency (MHz)
μPD30541GD-167-WML	208-pin plastic QFP (fine pitch) (28 × 28)	167

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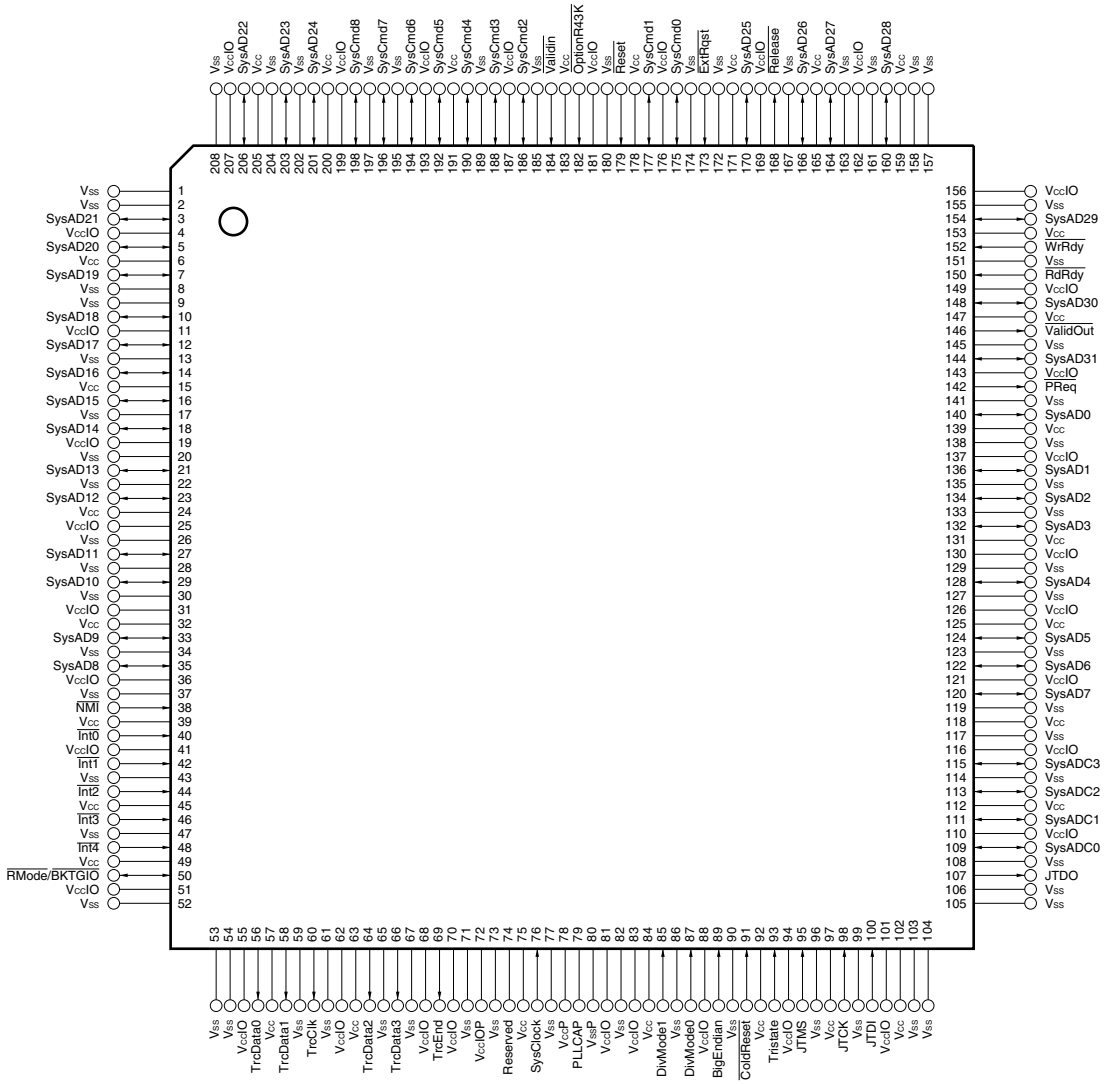
Printed in Japan

The mark ★ shows major revised points.

PIN CONFIGURATION

- 208-pin plastic QFP (fine pitch) (28 × 28)
  μPD30541GD-167-WML

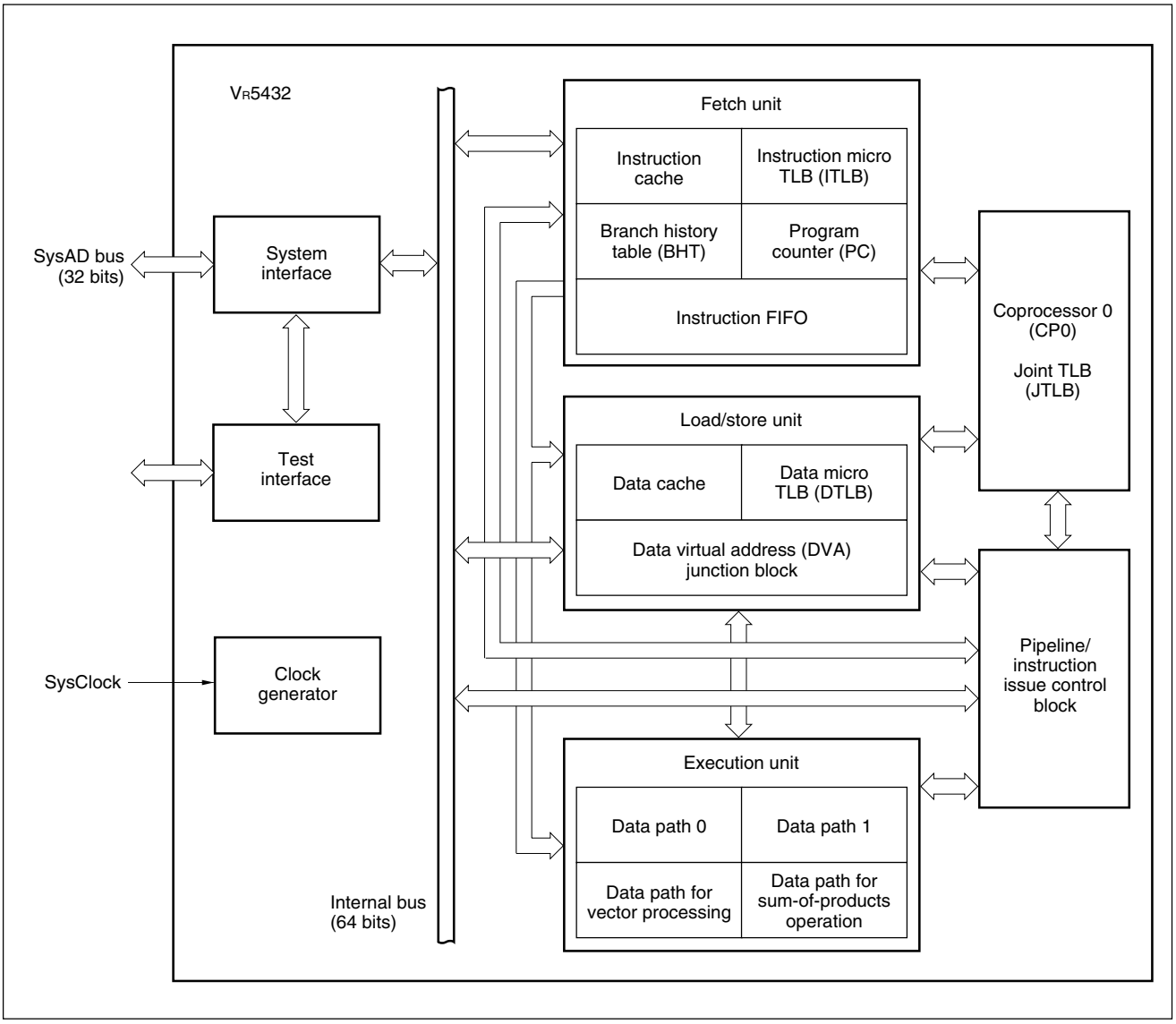


Caution Leave open for the Reserved pin.

PIN NAMES

BigEndian:	Endian mode select
$\overline{\text{BKTGIO}}$:	Break/trigger I/O
$\overline{\text{ColdReset}}$:	Cold reset
DivMode (1:0):	Divide mode
$\overline{\text{ExtRqst}}$:	External request
$\overline{\text{Int}}$ (4:0):	Interrupt request
JTCK:	JTAG clock
JTDI:	JTAG data input
JTDO:	JTAG data output
JTMS:	JTAG mode select
$\overline{\text{OptionR43K}}$:	V_R4300^{TM} mode select
$\overline{\text{NMI}}$:	Non-maskable interrupt request
PLLCAP:	PLL capacitor
$\overline{\text{PReq}}$:	Processor request
$\overline{\text{RdRdy}}$:	Read ready
$\overline{\text{Release}}$:	Release interface
$\overline{\text{Reset}}$:	Reset
Reserved:	Reserved
$\overline{\text{RMode}}$:	Reset mode
SysAD (31:0):	System address/data bus
SysADC (3:0):	System address/data check bus
SysClock:	System clock
SysCmd (8:0):	System command/data identifier
TrcClk:	Trace clock
TrcData (3:0):	Trace data
TrcEnd:	Trace end
Tristate:	3-state
$\overline{\text{ValidIn}}$:	Valid input
$\overline{\text{ValidOut}}$:	Valid output
V_{CC}:	Power supply for processor core
$V_{CC}IO$:	Power supply for processor I/O
$V_{CC}IOP$:	Quiet $V_{CC}IO$ for PLL
$V_{CC}P$:	Quiet V_{CC} for PLL
V_{SS}:	Ground
$V_{SS}P$:	Quiet V_{SS} for PLL
$\overline{\text{WrRdy}}$:	Write ready

★ INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 List of Pin Functions

Caution The functions of some pins change depending on the status of the $\overline{\text{OptionR43K}}$ signal. If this signal is low, the signal names same as those of the VR4300 Series are used because these pins have functions compatible to those of the VR4300 Series.

(1/4)

Pin Name	I/O	$\overline{\text{OptionR43K}}$ Signal	Signal Name	Function
SysAD (31:0)	I/O	High level/low level	SysAD (31:0)	System address/data bus A 32-bit bus for communication between the processor and external agent
SysADC (3:0)	I/O	High level	SysADC (3:0)	System address/data check bus A parity bus for SysAD bus
		Low level	–	Not used
SysCmd (8:0)	I/O	High level	SysCmd (8:0)	System command/data ID bus A 9-bit bus that transfers commands and data identifiers between the processor and external agent
		Low level	SysCmd (4:0) (SysCmd (8:5) are not used.)	System command/data ID bus A 5-bit bus that transfers commands and data identifiers between the processor and external agent
$\overline{\text{ValidIn}}$	Input	High level	$\overline{\text{ValidIn}}$	Valid In A signal indicating that the external agent is driving a valid address or data onto the SysAD bus, and a valid command or data identifier onto the SysCmd bus
		Low level	$\overline{\text{EValid}}$	External valid A signal indicating that the external agent is driving a valid address or data onto the SysAD bus, and a valid command or data identifier onto the SysCmd bus
$\overline{\text{ValidOut}}$	Output	High level	$\overline{\text{ValidOut}}$	Valid out A signal indicating that the processor is driving a valid address or data onto the SysAD bus, and a valid command or data identifier onto the SysCmd bus
		Low level	$\overline{\text{PValid}}$	Processor valid A signal indicating that the processor is driving a valid address or data onto the SysAD bus, and a valid command or data identifier onto the SysCmd bus
$\overline{\text{ExtRqst}}$	Input	High level	$\overline{\text{ExtRqst}}$	External request A signal allowing the external agent to request the right to use the system interface
		Low level	$\overline{\text{EReq}}$	External request A signal allowing the external agent to request the right to use the system interface

(2/4)

Pin Name	I/O	$\overline{\text{OptionR43K}}$ Signal	Signal Name	Function
$\overline{\text{Release}}$	Output	High level	$\overline{\text{Release}}$	Releases interface A signal indicating that the processor releases the system interface to a slave state
		Low level	$\overline{\text{PMaster}}$	Processor master A signal indicating that the processor has a right to control the system interface
$\overline{\text{PReq}}$	Output	High level	$\overline{\text{PReq}}$	Processor request A signal indicating that the processor has a request that is pending
		Low level	$\overline{\text{PReq}}$	Processor request A signal allowing the processor to request the right to use the system interface
$\overline{\text{WrRdy}}$	Input	High level	$\overline{\text{WrRdy}}$	Write ready A signal indicating that the external agent is ready to accept a processor write request
		Low level	$\overline{\text{EOK}}$	External OK A signal indicating that the external agent is ready to accept a processor read/write request
$\overline{\text{RdRdy}}$	Input	High level	$\overline{\text{RdRdy}}$	Read ready A signal indicating that the external agent is ready to accept a processor read request
		Low level	–	Not used
SysClock	Input	High level	SysClock	System clock Clock input to the processor
		Low level	MasterClock	Master clock Clock input to the processor
$\overline{\text{Int (4:0)}}$	Input	High level/low level	$\overline{\text{Int (4:0)}}$	Interrupts These are general-purpose processor interrupt requests. The input states can be checked by bits 14 to 10 of the Cause register.
$\overline{\text{NMI}}$	Input	High level/low level	$\overline{\text{NMI}}$	Non-maskable interrupt This is the non-maskable interrupt request.
$\overline{\text{ColdReset}}$	Input	High level/low level	$\overline{\text{ColdReset}}$	Cold reset This signal completely initializes the internal status of the processor. Deassert it in synchronization with SysClock.
$\overline{\text{Reset}}$	Input	High level/low level	$\overline{\text{Reset}}$	Reset This signal logically initializes the internal status of the processor. Deassert it in synchronization with SysClock.

(3/4)

Pin Name	I/O	$\overline{\text{OptionR43K}}$ Signal	Signal Name	Function
$\overline{\text{OptionR43K}}$	Input	–	$\overline{\text{OptionR43K}}$	VR4300 mode Assert this signal when the system interface of the VR5432 operates with a protocol compatible to the VR4300 Series. Set the input level of this signal before the power-on reset. Make sure that the level of this signal does not change while the VR5432 is operating.
DivMode (1:0)	Input	High level/low level	DivMode (1:0)	Division mode These signals set the division ratio of PClock and SysClock as follows: 11: 4:1 10: 3:1 01: 5:2 00: 2:1 Set the input levels of these signals before the power-on reset. Make sure that the levels of these signals do not change while the VR5432 operates.
BigEndian	Input	High level/low level	BigEndian	Endian mode This signal sets a byte ordering for addressing. A big endian mode is selected when this signal is active; a little endian mode is selected when it is inactive. Set the input level of this signal before the power-on reset. Make sure that the level of this signal does not change while the VR5432 is operating.
TrcData (3:0)	Output	High level/low level	TrcData (3:0)	Trace data Data output by the test interface
TrcEnd	Output	High level/low level	TrcEnd	Trace end A signal indicates the end of a trace data packet.
TrcClk	Output	High level/low level	TrcClk	Trace clock Clock for the test interface. The same clock as SysClock is output.
$\overline{\text{RMode}}$/$\overline{\text{BKTGIO}}$	I/O	High level/low level	$\overline{\text{RMode}}$/$\overline{\text{BKTGIO}}$	Reset mode/break trigger I/O This signal serves as a debug reset input signal on Cold Reset. It serves as a break or trigger I/O signal during normal operation.
Tristate	Input	High level/low level	Tristate	3-state This signal sets all output signals to a high-impedance state.
JTDI	Input	High level/low level	JTDI	JTAG data input Serial data input for JTAG
JTDO	Output	High level/low level	JTDO	JTAG data output Serial data output for JTAG

(4/4)

Pin Name	I/O	$\overline{\text{OptionR43K}}$ Signal	Signal Name	Function
JTMS	Input	High level/low level	JTMS	JTAG mode select This signal selects a JTAG test mode.
JTCK	Input	High level/low level	JTCK	JTAG clock input Serial clock input for JTAG
PLLCAP	–	High level/low level	PLLCAP	PLL capacitor Connect a capacitor to this pin to adjust the internal PLL.
$V_{CC}P$	–	High level/low level	$V_{CC}P$	PLL V_{CC} This pin supplies 2.5 V to the internal PLL.
$V_{CC}IOP$	–	High level/low level	$V_{CC}IOP$	PLL $V_{CC}IO$ This pin supplies 3.3 V to the internal PLL.
$V_{SS}P$	–	High level/low level	$V_{SS}P$	PLL V_{SS} This is the ground pin of the internal PLL.
V_{CC}	–	High level/low level	V_{CC}	Power supply pin for core
$V_{CC}IO$	–	High level/low level	$V_{CC}IO$	Power supply pin for I/O
V_{SS}	–	High level/low level	V_{SS}	Ground pin

★ 1.2 Recommended Connection of Unused Pins

(1) Test interface pins

Pin Name	Recommended Connection of Unused Pins
JTCK	Pull up
JTMS	Pull up
JTDI	Pull up
JTDO	Open
TrcData (3:0)	Open
TrcEnd	Open
TrcClk	Open
$\overline{\text{RMode}}/\overline{\text{BKTGIO}}$	Pull up
Tristate	Pull down

(2) Other pins

Pull up or pull down for the input pins and I/O pins.

Leave open for the output pins.

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}IO$		−0.5 to +4.0	V
	$V_{CC}IOP$		−0.5 to +4.0	V
	V_{CC}		−0.5 to +3.0	V
	$V_{CC}P$		−0.5 to +3.0	V
Input voltage[Note]	V_I		−0.5 to $V_{CC}IO$ + 0.3	V
		Pulse of less than 10 ns	−1.5 to $V_{CC}IO$ + 0.3	V
Operating case temperature	T_C		−10 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Note The upper-limit input voltage ($V_{CC}IO$ + 0.3) is +4.0 V.

Cautions 1. Do not short-circuit two or more outputs at the same time.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The specifications and conditions shown in the following DC Characteristics and AC Characteristics sections are the ranges within which the product can normally operate and the quality can be guaranteed.

DC Characteristics (T_C = –10 to +85°C, $V_{CC}IO = V_{CC}IOP$ = 3.3 V ±0.3 V, $V_{CC} = V_{CC}P$ = 2.5 V ±5%)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output voltage, high	V_{OH}	$V_{CC}IO$ = MIN., I_{OH} = –4 mA	2.4		V
Output voltage, low	V_{OL}	$V_{CC}IO$ = MIN., I_{OL} = 4 mA		0.4	V
Input voltage, high[Note 1]	V_{IH}		2.0	$V_{CC}IO$ + 0.3	V
Input voltage, low[Note 1]	V_{IL}		–0.5	+0.8	V
		Pulse of less than 10 ns	–1.5	+0.8	V
Input voltage, high[Note 2]	V_{IHC}		0.8 × $V_{CC}IO$	$V_{CC}IO$ + 0.3	V
Input voltage, low[Note 2]	V_{ILC}		–0.5	0.2 × $V_{CC}IO$	V
		Pulse of less than 10 ns	–1.5	0.2 × $V_{CC}IO$	V
Supply current	I_{CC}	During internal operation at 167 MHz, $V_{CC}IO = V_{CC}IOP$ = 3.6 V, $V_{CC} = V_{CC}P$ = 2.625 V		0.80	A
	$I_{CC}IO$	During internal operation at 167 MHz, $V_{CC}IO = V_{CC}IOP$ = 3.6 V, $V_{CC} = V_{CC}P$ = 2.625 V		0.15	A
Power consumption	Pd	During internal operation at 167 MHz, $V_{CC}IO = V_{CC}IOP$ = 3.6 V, $V_{CC} = V_{CC}P$ = 2.625 V		2.10	W
	PdIO	During internal operation at 167 MHz, $V_{CC}IO = V_{CC}IOP$ = 3.6 V, $V_{CC} = V_{CC}P$ = 2.625 V		0.54	W
Input leakage current, high	I_{LIH}	$V_I = V_{CC}IO$		5.0	μA
Input leakage current, low	I_{LIL}	V_I = 0 V		–5.0	μA
Output leakage current, high	I_{LOH}	$V_O = V_{CC}IO$		5.0	μA
Output leakage current, low	I_{LOL}	V_O = 0 V		–5.0	μA

Notes 1. Not applied to the SysClock pin.

2. Applied to the SysClock pin only.

Remark The supply current during operation is almost proportional to the operating clock frequency.

Power-On Sequence

The VR5432 uses two systems of power supplies. These power supplies can be turned on any sequence. ★ However, make sure that one power supply is not turned on for 100 ms or longer while the other power supply is turned off.

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
★ Power-on delay	t_{DF}		0	100	ms

Capacitance (T_A = 25°C, $V_{CC}IO = V_{CC}IOP = V_{CC} = V_{CC}P$ = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_{IN}	f_C = 1 MHz Unmeasured pins returned to 0 V		5.0	pF
Output capacitance	C_{OUT}			7.0	pF

AC Characteristics (T_C = –10 to +85°C, $V_{CC}IO = V_{CC}IOP$ = 3.3 V ±0.3 V, $V_{CC} = V_{CC}P$ = 2.5 V ±5%)

Clock parameter

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
System clock high-level width	t_{CH}		3.0		ns
System clock low-level width	t_{CL}		3.0		ns
System clock frequency[Note]		DivMode = 2:1	41.7	83.3	MHz
		DivMode = 5:2	33.3	66.6	MHz
		DivMode = 3:1	27.7	55.5	MHz
		DivMode = 4:1	20.8	41.6	MHz
System clock cycle	t_{CP}	DivMode = 2:1	12	24	ns
		DivMode = 5:2	15	30	ns
		DivMode = 3:1	18	36	ns
		DivMode = 4:1	24	48	ns
System clock jitter	t_J			±250	ps
System clock rise time	t_{CR}			2.0	ns
System clock fall time	t_{CF}			2.0	ns
JTAG clock frequency				33	MHz

Note This is the frequency at which the operation of the internal PLL is guaranteed.

Remark The JTAG clock runs asynchronously to the system clock.

System interface parameter

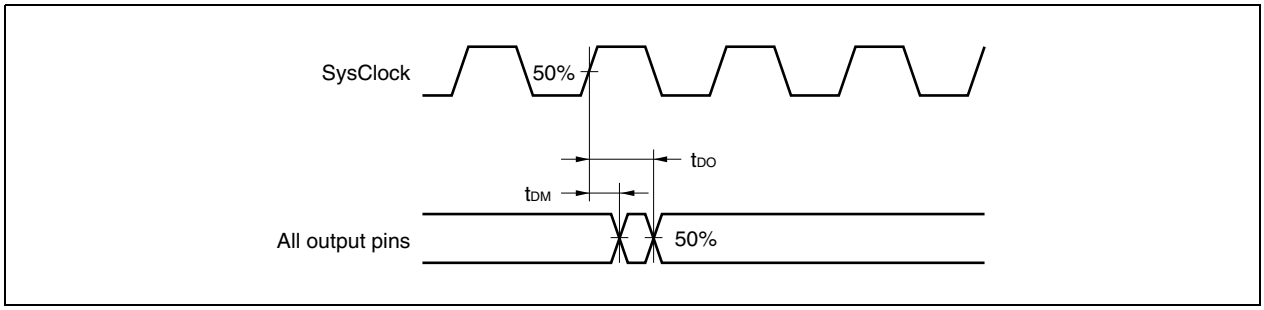
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data output hold time	t_{DM}		1.0		ns
Data output delay time	t_{DO}			5.0	ns
Data input setup time	t_{DS}		2.0		ns
Data input hold time	t_{DH}		1.5		ns

Load coefficient

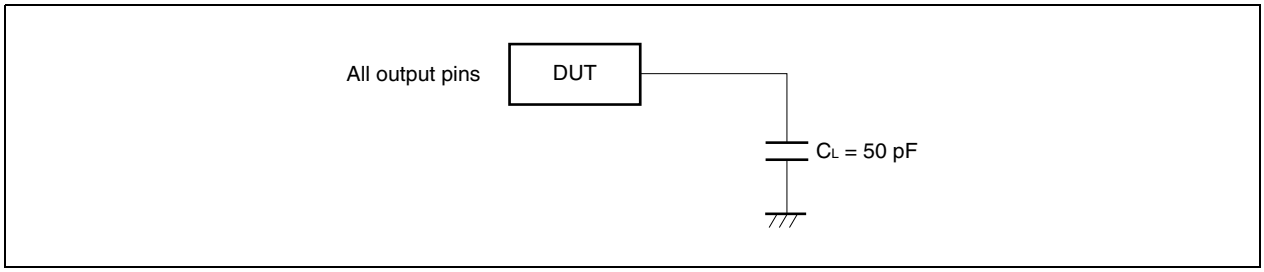
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Load coefficient	CLD			1.0	ns/25 pF

Measurement Conditions

Measurement point

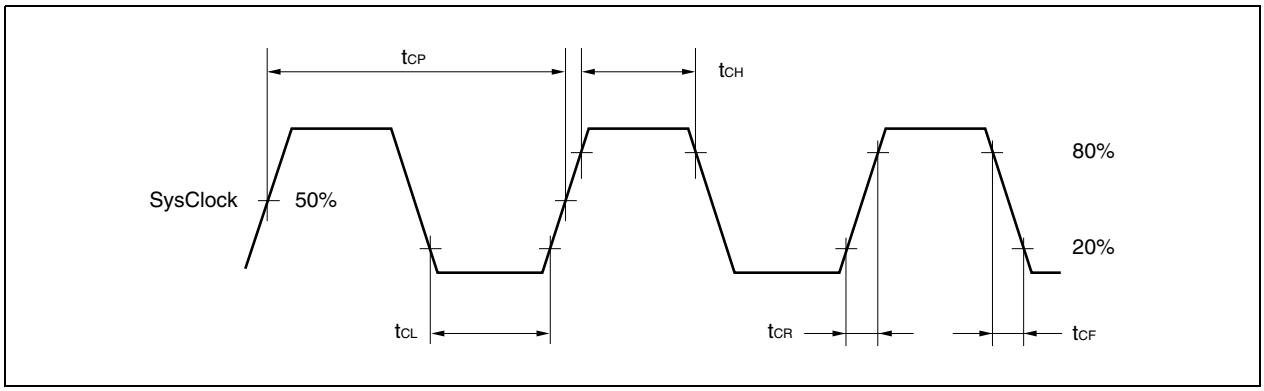


Load condition

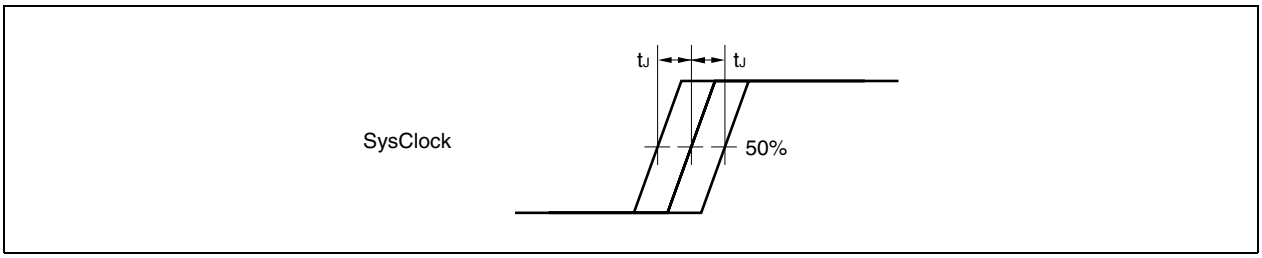


Timing Charts

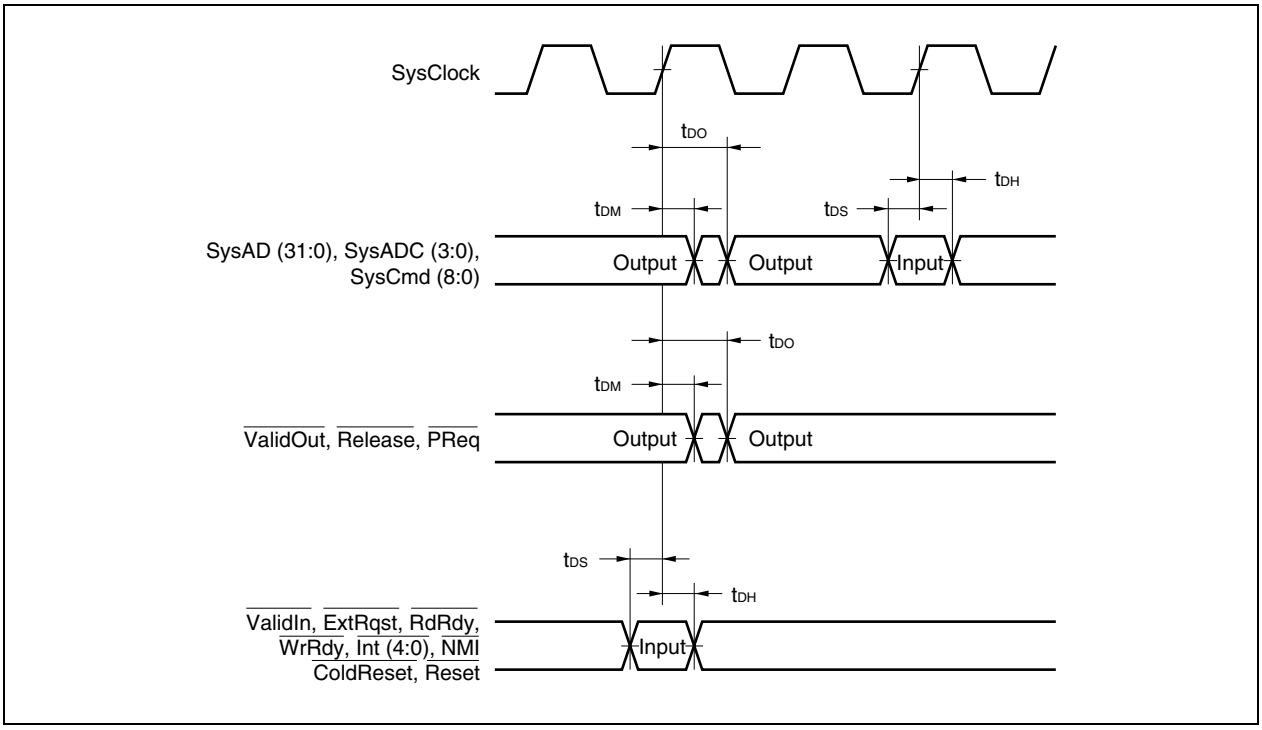
Clock timing



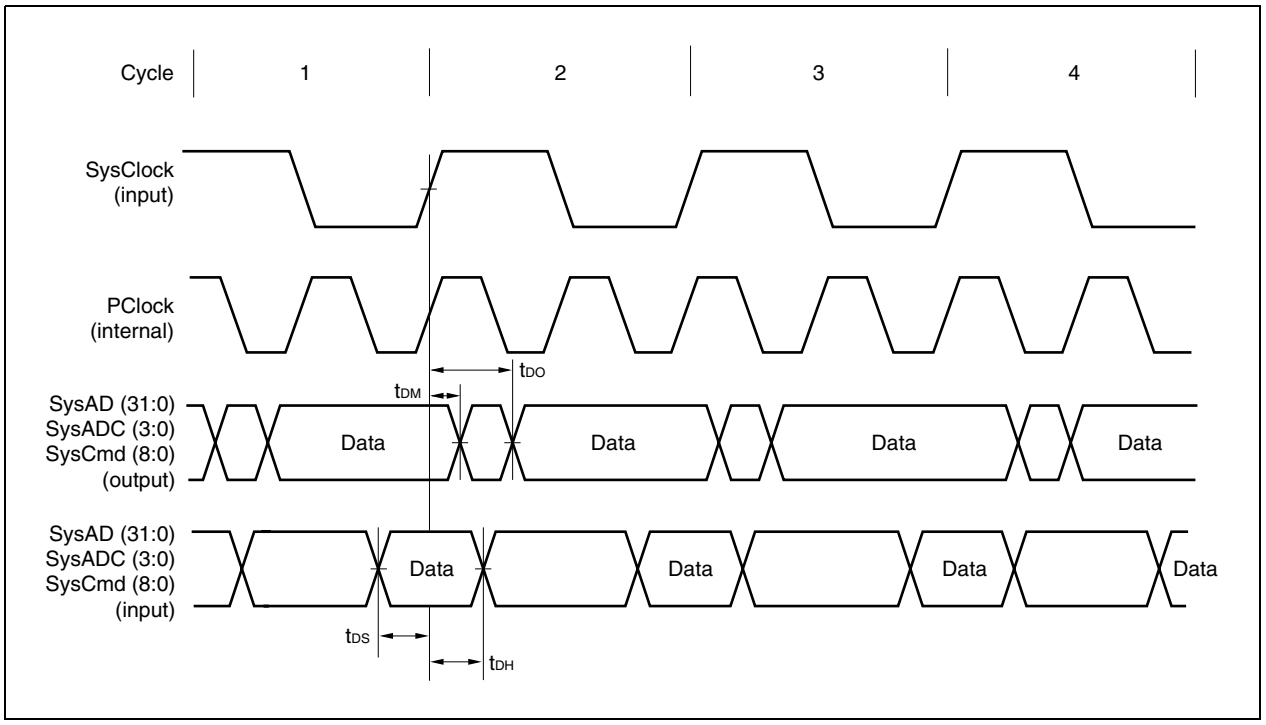
Clock jitter



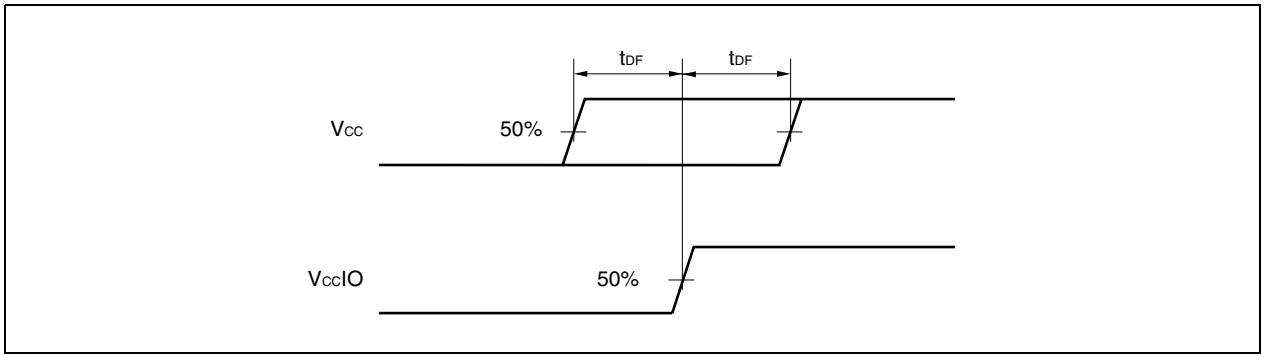
System interface edge timing



Clock relations (DivMode = 2:1)

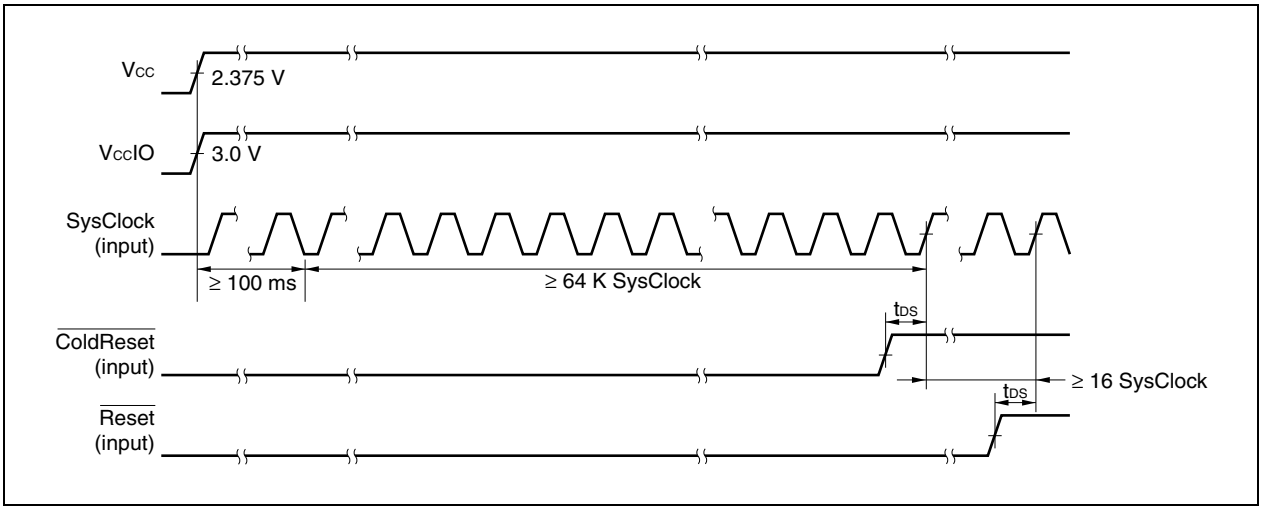


Power-on sequence

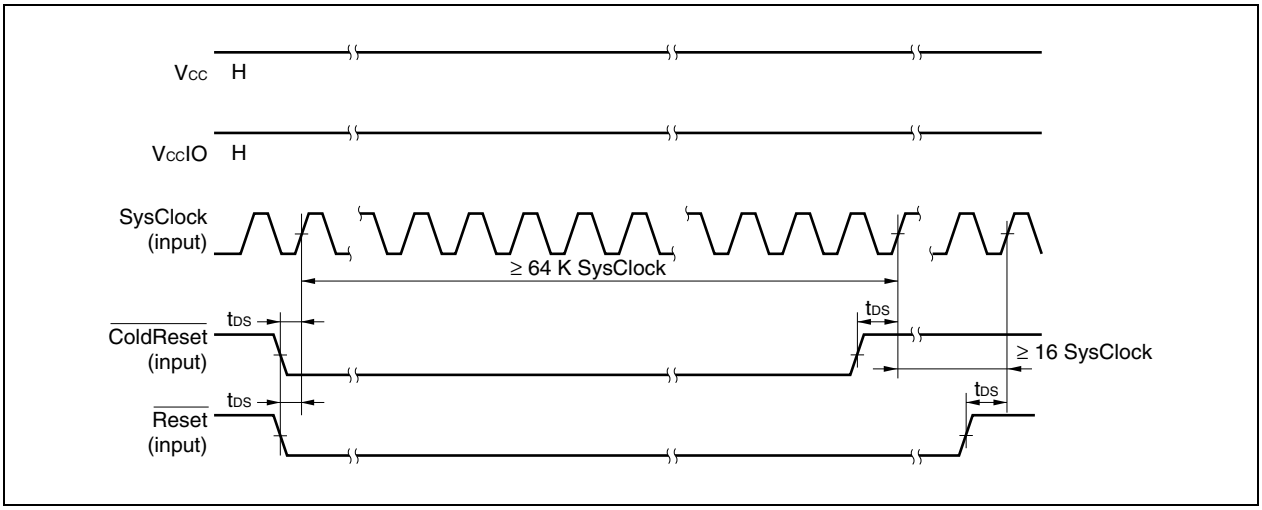


Reset Timing

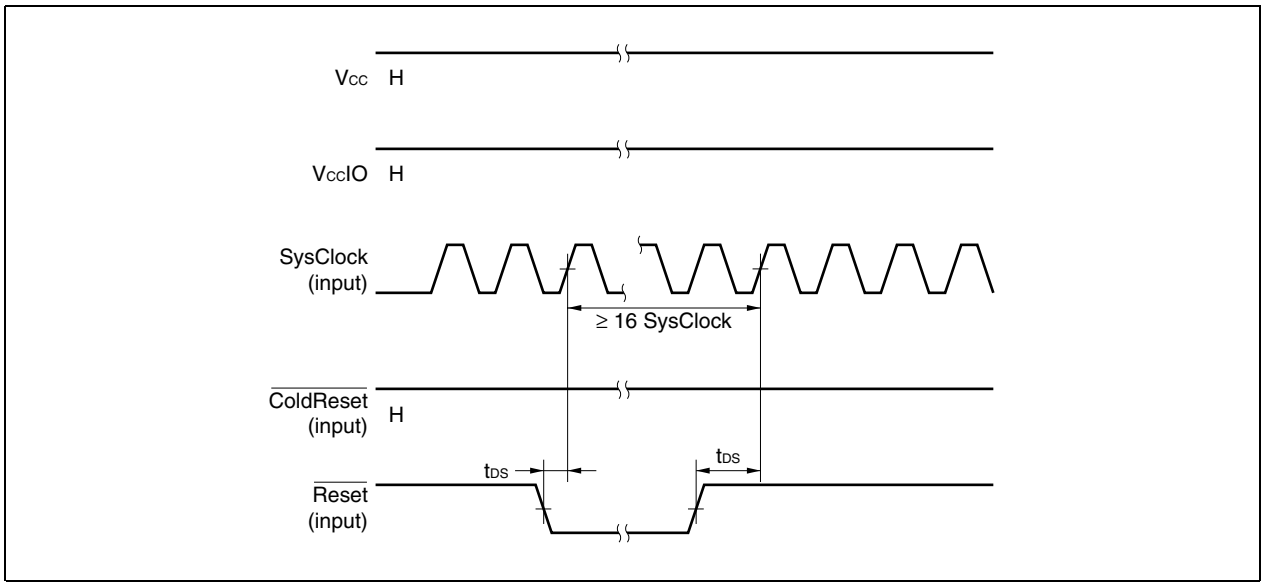
Power-on reset timing



Cold Reset timing

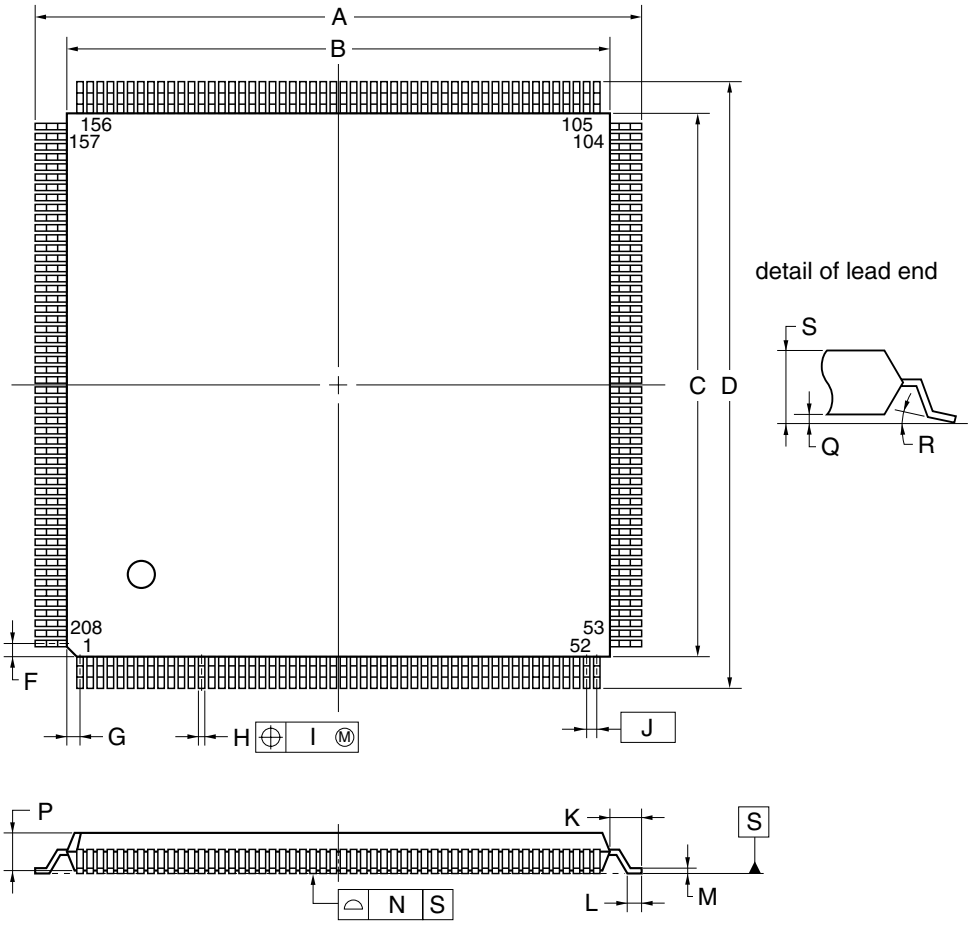


Warm Reset timing



3. PACKAGE DRAWING

208-PIN PLASTIC QFP (FINE PITCH) (28x28)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	30.6±0.2
B	28.0±0.2
C	28.0±0.2
D	30.6±0.2
F	1.25
G	1.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.3±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	3.2±0.1
Q	0.4±0.1
R	5°±5°
S	3.8 MAX.

P208GD-50-LML,MML,SML,WML-7

4. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 4-1. Surface Mounting Type Soldering Conditions

μPD30541GD-167-WML: 208-pin plastic QFP (fine pitch) (28 × 28)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds MAX. (at 210°C or higher), Count: Three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 36 to 72 hours)	IR35-367-3
Partial heating	Pin temperature: 300°C MAX., Time: 3 seconds MAX. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

APPENDIX DIFFERENCES AMONG VR5432, VR5000™, AND VR4310™

Item		VR5432	VR5000	VR4310
Maximum operating frequency	Internal	167 MHz	200 MHz	167 MHz
	External	83.3 MHz	100 MHz	83.3 MHz
Pipeline		2-way superscaler 5-stage pipeline		5-stage pipeline
Cache	Primary instruction cache	32 KB		16 KB
	Primary data cache	32 KB		8 KB
	Secondary cache interface	None	Provided	None
	Data protection	Byte parity/none	Byte parity	None
System bus	Bus width	32 bits	64 bits	32 bits
	Data protection	Byte parity/none	Byte parity	None
	Status after last data write	Completes access./Holds last data on setting of transfer rate.	Completes access.	Holds last data on setting of transfer rate.
Pins for initial setting at reset		DivMode (1:0), BigEndian, $\overline{\text{OptionR43K}}$	ModeIn (dedicated serial pin)	DivMode (2:0)
Instruction set		MIPS I, II, III, IV + multimedia + sum-of-products operation	MIPS I, II, III, IV	MIPS I, II, III
Branch prediction mechanism		Provided	None	
Hardware debug function		JTAG, N-Wire	None	JTAG
SyncOut-SyncIn path		None		Provided
Clock interface	Input vs. internal multiple	2, 2.5, 3, 4	2, 3, 4, 5, 6, 7, 8	2, 2.5, 3, 4, 5, 6
	Internal vs. bus division ratio	2, 2.5, 3, 4	2, 3, 4, 5, 6, 7, 8	2, 2.5, 3, 4, 5, 6
	Clock output	None		TClock
Power management mode		None	Standby mode	None
PRId register		Imp = 0x54	Imp = 0x23	Imp = 0x0B

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference document Electrical Characteristics for Microcomputer (U15170J)[Note]

Note This document number is that of Japanese version.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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Fax: 408-588-6130
800-729-9288

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Duesseldorf, Germany
Tel: 0211-65 03 01
Fax: 0211-65 03 327

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Tel: 040-244 58 45
Fax: 040-244 45 80

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Fax: 08-63 80 388

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Fax: 01-3067-58-99

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Fax: 091-504-28-60

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Hong Kong
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Seoul Branch
Seoul, Korea
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Novena Square, Singapore
Tel: 253-8311
Fax: 250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

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Electron Devices Division
Guarulhos-SP, Brasil
Tel: 11-6462-6810
Fax: 11-6462-6829

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