SECTION 10
ELECTRICAL AND THERMAL CHARACTERISTICS

This section provides information on the maximum rating and thermal characteristics for the MC68000, MC68HC000, MC68HC001, MC68EC000, MC68008, and MC68010.

10.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 7.0	V
Input Voltage	V_{in}	−0.3 to 7.0	V
Maximum Operating Temperature Range Commerical Extended "C" Grade Commerical Extended "I" Grade	T_A	T_L to T_H 0 to 70 −40 to 85 0 to 85	°C
Storage Temperature	T_{stg}	−55 to 150	°C

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

10.2 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Symbol	Value	Rating
Thermal Resistance	θ_{JA}		θ_{JC}		°C/W
Ceramic, Type L/LC		30		15*	
Ceramic, Type R/RC		33		15	
Plastic, Type P		30		15*	
Plastic, Type FN		45*		25*	

*Estimated

10.3 POWER CONSIDERATIONS

The average die-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot {}^{\theta}J_A) \quad (1)$$

where:

T_A = Ambient Temperature, °C
${}^{\theta}J_A$ = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{CC} \times V_{CC}$, Watts — Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications, $P_{I/O} < P_{INT}$ and can be neglected.

An appropriate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \quad (2)$$

Solving Equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + {}^{\theta}JA \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at thermal equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equations (1) and (2) iteratively for any value of T_A.

The curve shown in Figure 10-1 gives the graphic solution to the above equations for the specified power dissipation of 1.5 W over the ambient temperature range of -55 °C to 125 °C using a maximum ${}^{\theta}J_A$ of 45 °C/W. Ambient temperature is that of the still air surrounding the device. Lower values of ${}^{\theta}J_A$ cause the curve to shift downward slightly; for instance, for ${}^{\theta}J_A$ of 40 °/W, the curve is just below 1.4 W at 25 °C.

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The total thermal resistance of a package (${}^{\theta}J_A$) can be separated into two components, ${}^{\theta}J_C$ and ${}^{\theta}C_A$, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (${}^{\theta}J_C$) and from the case to the outside ambient air (${}^{\theta}C_A$). These terms are related by the equation:

$${}^{\theta}J_A = {}^{\theta}J_C + {}^{\theta}C_A \quad (4)$$

${}^{\theta}J_C$ is device related and cannot be influenced by the user. However, ${}^{\theta}C_A$ is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management on the part of the user can significantly reduce ${}^{\theta}C_A$ so that ${}^{\theta}J_A$ approximately equals ;${}^{\theta}J_C$. Substitution of ${}^{\theta}J_C$ for ${}^{\theta}J_A$ in equation 1 results in a lower semiconductor junction temperature.

Table 10-1 summarizes maximum power dissipation and average junction temperature for the curve drawn in Figure 10-1, using the minimum and maximum values of ambient temperature for different packages and substituting $^{\theta}J_C$ for $^{\theta}J_A$ (assuming good thermal management). Table 10-2 provides the maximum power dissipation and average junction temperature assuming that no thermal management is applied (i.e., still air).

NOTE

Since the power dissipation curve shown in Figure 10-1 is negatively sloped, power dissipation declines as ambient temperature increases. Therefore, maximum power dissipation occurs at the lowest rated ambient temperature, but the highest average junction temperature occurs at the maximum ambient temperature where *power dissipation is lowest*.

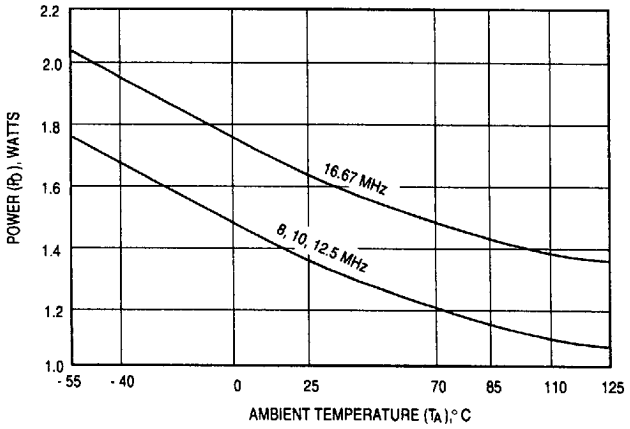

Figure 10-1. MC68000 Power Dissipation (P_D) vs Ambient Temperature (T_A) (Not Applicable to MC68HC000/68HC001/68EC000)

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Table 10-1. Power Dissipation and Junction Temperature vs Temperature ($\theta J_C = \theta J_A$)

Package	T_A Range	θJ_C (°C/W)	P_D (W) @ T_A Min.	T_J (°C) @ T_A Min.	P_D (W) @ T_A Max.	T_J (°C) @ T_A Max.
L/LC	0°C to 70°C	15	1.5	23	1.2	88
	-40°C to 85°C	15	1.7	-14	1.2	103
	0°C to 85°C	15	1.5	23	1.2	103
P	0°C to 70°C	15	1.5	23	1.2	88
R/RC	0°C to 70°C	15	1.5	23	1.2	88
	-40°C to 85°C	15	1.7	-14	1.2	103
	0°C to 85°C	15	1.5	23	1.2	103
FN	0°C to 70°C	25	1.5	38	1.2	101

NOTE: Table does not include values for the MC68000 12F.
Does not apply to the MC68HC000, MC68HC001, and MC68EC000.

Table 10-2. Power Dissipation and Junction Temperature vs Temperature ($\theta J_C \neq \theta J_C$)

Package	T_A Range	θJ_A (°C/W)	P_D (W) @ T_A Min.	T_J (°C) @ T_A Min.	P_D (W) @ T_A Max.	T_J (°C) @ T_A Max.
L/LC	0°C to 70°C	30	1.5	23	1.2	88
	-40°C to 85°C	30	1.7	-14	1.2	103
	0°C to 85°C	30	1.5	23	1.2	103
P	0°C to 70°C	30	1.5	23	1.2	88
R/RC	0°C to 70°C	33	1.5	23	1.2	88
	-40°C to 85°C	33	1.7	-14	1.2	103
	0°C to 85°C	33	1.5	23	1.2	103
FN	0°C to 70°C	40	1.5	38	1.2	101

NOTE: Table does not include values for the MC68000 12F.
Does not apply to the MC68HC000, MC68HC001, and MC68EC000.

Values for thermal resistance presented in this manual, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843 "Thermal Resistance Measurement Method for MC68XXX Microcomponent Devices" and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User-derived values for thermal resistance may differ.

10.4 CMOS CONSIDERATIONS

The MC68HC000, MC68HC001, and MC68EC000, with it significantly lower power consumption, has other considerations. The CMOS cell is basically composed of two complementary transistors (a P channel and an N channel), and only one transistor is turned on while the cell is in the steady state. The active P-channel transistor sources current when the output is a logic high and presents a high impedance when the output is logic low. Thus, the overall result is extremely low power consumption because no power

is lost through the active P-channel transistor. Also, since only one transistor is turned on during the steady state, power consumption is determined by leakage currents.

Because the basic CMOS cell is composed of two complementary transistors, a virtual semiconductor controlled rectifier (SCR) may be formed when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become latched in a mode that may result in excessive current drain and eventual destruction of the device. Although the MC68HC000 and MC68EC000 is implemented with input protection diodes, care should be exercised to ensure that the maximum input voltage specification is not exceeded. Some systems may require that the CMOS circuitry be isolated from voltage transients; other may require additional circuitry.

The MC68HC000 and MC68EC000, implemented in CMOS, is applicable to designs to which the following considerations are relevant:

1. The MC68HC000 and MC68EC000 completely satisfies the input/output drive requirements of CMOS logic devices.
2. The HCMOS MC68HC000 and MC68EC000 provides an order of magnitude reduction in power dissipation when compared to the HMOS MC68000. However, the MC68HC000 does not offer a "power-down" mode.

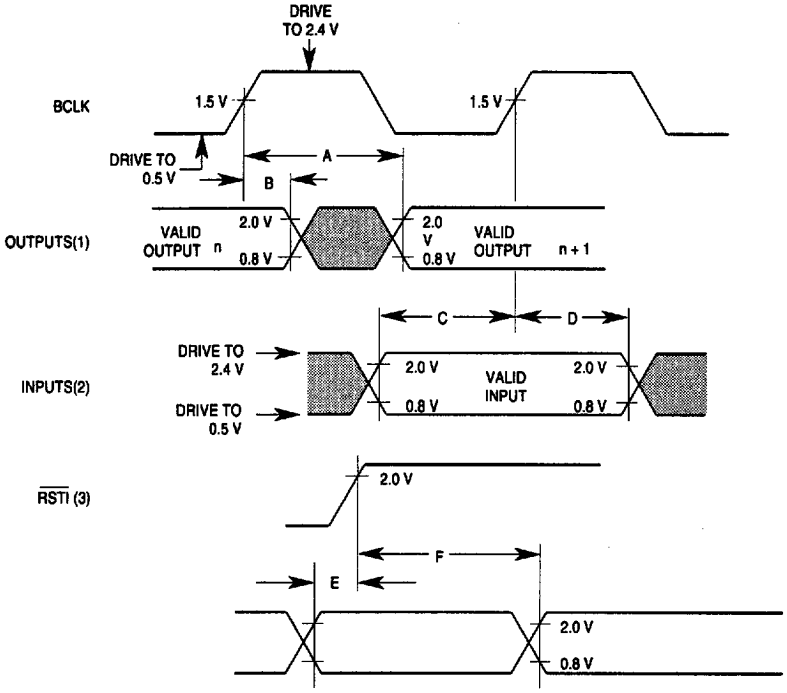
10.5 AC ELECTRICAL SPECIFICATION DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in Figure 10-2. To test the parameters guaranteed by Motorola, inputs must be driven to the voltage levels specified in the figure. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs are specified with minimum setup and hold times, and are measured as shown. Finally, the measurement for signal-to-signal specifications are shown.

NOTE

The testing levels used to verify conformance to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



NOTES:

1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
3. This timing is applicable to all parameters specified relative to the negation of the RESET signal.

LEGEND:

A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Mode select setup time to RESET negated.
F. Mode select hold time from RESET negated.

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Figure 10-2. Drive Levels and Test Points for AC Specifications

10.6 MC68000/68008/68010 DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0 VDC±5%; GND=0 VDC; T_A=T_L TO T_H)

Characteristic		Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	2.0	V_{CC}	V
Input Low Voltage		V_{IL}	GND-0.3	0.8	V
Input Leakage Current @ 5.25 V	$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, CLK, $\overline{IPL0}$—$\overline{IPL2}$, $\overline{VPA}$	I_{IN}	— —	2.5 20	μA
	$\overline{HALT}$, $\overline{RESET}$				
Three-State (Off State) Input Current @ 2.4 V/0.4 V	$\overline{AS}$, A1—A23, D0—D15, FC0—FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	I_{TSI}	—	20	μA
Output High Voltage (I_{OH} = −400 μA)	E*	V_{OH}	V_{CC} −0.75	—	V
(I_{OH} = -400 μA)	$\overline{AS}$, A1–A23, $\overline{BG}$, D0–D15, FC0–FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$		2.4	2.4	
Output Low Voltage		V_{OL}			V
(I_{OL}= 1.6 mA)	$\overline{HALT}$		—	0.5	
(I_{OL} = 3.2 mA)	A1—A23, $\overline{BG}$, FC0-FC2		—	0.5	
(I_{OL} = 5.0 mA)	$\overline{RESET}$		—	0.5	
(I_{OL} = 5.3 mA)	E, $\overline{AS}$, D0—D15, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$		—	0.5	
Power Dissipation (see POWER CONSIDERATIONS)		P_D***	—	—	W
Capacitance (V_{in}=0 V, T_A=25°C, Frequency=1 MHz)**		C_{in}	—	20.0	pF
Load Capacitance	$\overline{HALT}$	C_L	—	70	pF
	All Others		—	130	

*With external pullup resistor of 1.1 Ω.
**Capacitance is periodically sampled rather than 100% tested.
***During normal operation, instantaneous V_{CC} current requirements may be as high as 1.5 A.

10.7 DC ELECTRICAL CHARACTERISTICS (V_{CC}=5.0 VDC±5%; GND=0 VDC; T_A=T_L TO T_H) (Applies To All Processors Except The MC68EC000)

Characteristic		Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	2.0	V_{CC}	V
Input Low Voltage		V_{IL}	GND-0.3	0.8	V
Input Leakage Current @ 5.25 V	$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, CLK, $\overline{IPL0}$—$\overline{IPL2}$, $\overline{VPA}$	I_{IN}	—	2.5	μA
	MODE, $\overline{HALT}$, $\overline{RESET}$		—	20	
Three-State (Off State) Input Current @ 2.4 V/0.4 V	$\overline{AS}$, A0—A23, D0—D15, FC0–FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	I_{TSI}	—	20	μA
Output High Voltage	E, $\overline{AS}$, A0–A23, $\overline{BG}$, D0–D15, FC0–FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	V_{OH}	V_{CC} –0.75	—	V
Output Low Voltage		V_{OL}			V
(I_{OL} = 1.6 mA)	$\overline{HALT}$		—	0.5	
(I_{OL} = 3.2 mA)	A0—A23, $\overline{BG}$, FC0-FC2		—	0.5	
(I_{OL} = 5.0 mA)	$\overline{RESET}$		—	0.5	
(I_{OL} = 5.3 mA)	E, $\overline{AS}$, D0—D15, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$		—	0.5	
Current Dissipation*	f = 8 MHz	I_D	—	25	mA
	f = 10 MHz		—	30	
	f = 12.5 MHz		—	35	
	f = 16.67 MHz		—	50	
	f = 20 MHz		—	70	
Power Dissipation	f = 8 MHz	P_D	—	0.13	W
	f = 10 MHz			0.16	
	f = 12.5 MHz			0.19	
	f = 16.67 MHz			0.26	
	f = 20 MHz			0.38	
Capacitance (V_{in} = 0 V, T_A=25°C, Frequency=1 MHz)**		C_{in}	—	20.0	pF
Load Capacitance	$\overline{HALT}$	C_L	—	70	pF
	All Others		—	130	

* Current listed are with no loading.
** Capacitance is periodically sampled rather than 100% tested.

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10.8 AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING (See Figure 10-3)

(Applies To All Processors Except The MC68EC000)

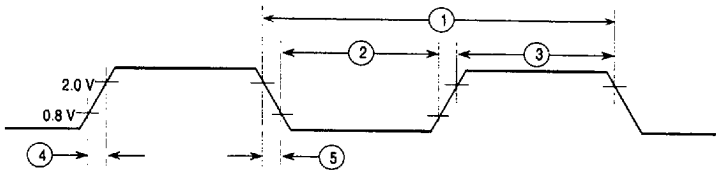
Num	Characteristic	8 MHz*		10 MHz*		12.5 MHz*		16.67 MHz 12F		16 MHz		20 MHZ**		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
	Frequency of Operation	4.0	8.0	4.0	10.0	4.0	12.5	8.0	16.7	8.0	16.7	8.0	20.0	MHz
1	Cycle Time	125	250	100	250	80	250	60	125	60	125	50	125	ns
2,3	Clock Pulse Width	55	125	45	125	35	125	27	62.5	27	62.5	21	62.5	ns
	(Measured from 1.5 V to 1.5 V for 12F)	55	125	45	125	35	125	27	62.5	27	62.5	21	62.5	
4,5	Clock Rise and Fall Times	—	10	—	10	—	5	—	5	—	5	—	4	ns
		—	10	—	10	—	5	—	5	—	5	—	4	

*These specifications represent an improvement over previously published specifications for the 8-, 10-, and 12.5-MHz MC68000 and are valid only for product bearing date codes of 8827 and later.
**This frequency applies only to MC68HC000 and MC68EC000 parts.

10.9 MC68008 AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING (See Figure 10-3)

Num	Characteristic	8 MHz*		10 MHz*		Unit
		Min	Max	Min	Max	
	Frequency of Operation	2.0	8.0	2.0	10.0	MHz
1	Cycle Time	125	500	100	500	ns
2,3	Clock Pulse Width	55	250	45	250	ns
4,5	Clock Rise and Fall Times	—	10	—	10	ns

*These specifications represent an improvement over previously published specifications for the 8-, and 10-MHz MC68008 and are valid only for product bearing date codes of 8827 and later



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 V and 2.0 V.

Figure 10-3. Clock Input Timing Diagram

10.10 AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

(V_{CC}=5.0 VDC±5+; GND=0 V; T_A=T_L to T_H; (see Figures 10-4 and 10-5) (Applies To All Processors Except The MC68EC000)

Num	Characteristic	8 MHz*		10 MHz*		12.5 MHz*		16.67 MHz 12F		16 MHz		20 MHz**		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
6	Clock Low to Address Valid	—	62	—	50	—	50	—	50		30	—	25	ns
6A	Clock High to FC Valid	—	62	—	50	—	45	—	45	0	30	0	25	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	—	80	—	70	—	60	—	50		50	—	42	ns
8	Clock High to Address, FC Invalid (Minimum)	0	—	0	—	0	—	0	—	0	—	0	—	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Asserted	3	60	3	50	3	40	3	40	3	30	3	25	ns
11[2]	Address Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read)/AS Asserted (Write)	30	—	20	—	15	—	15	—	15	—	10	—	ns
11A[2]	FC Valid to $\overline{AS}$), $\overline{DS}$ Asserted (Read)/$\overline{AS}$) Asserted (Write)	90	—	70	—	60	—	30	—	45	—	40	—	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	—	62	—	50	—	40	—	40	3	30	3	25	ns
13[2]	$\overline{AS}$ $\overline{DS}$ Negated to Address, FC Invalid	40	—	30	—	20	—	10	—	15	—	10	—	ns
14[2]	$\overline{AS}$and $\overline{DS}$ Read) Width Asserted	270	—	195	—	160	—	120	—	120	—	100	—	ns
14A	$\overline{DS}$ Width Asserted (Write)	140		95		80		60		60	—	50	—	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width Negated	150	—	105	—	65	—	60	—	60	—	50	—	ns
16	Clock High to Control Bus High Impedance	—	80	—	70	—	60	—	50	—	50	—	42	ns
17[2]	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	40	—	30	—	20	—	10	—	15	—	10	—	ns
18[1]	Clock High to R/$\overline{W}$ High (Read)	0	55	0	45	0	40	0	40	0	30	0	25	ns
20[1]	Clock High to R/$\overline{W}$ Low (Write)	0	55	0	45	0	40	0	40	0	30	0	25	ns
20A[2,6]	$\overline{AS}$ Asserted to R/$\overline{W}$ Valid (Write)	—	10	—	10	—	10	—	10	—	10	—	10	ns
21[2]	Address Valid to R/$\overline{W}$ Low (Write)	20	—	0	—	0	—	0	—	0	—	0	—	ns
21A[2]	FC Valid to R/$\overline{W}$ Low (Write)	60	—	50	—	30	—	20	—	30	—	25	—	ns
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	80	—	50	—	30	—	20	—	30	—	25	—	ns
23	Clock Low to Data-Out Valid (Write)	—	62	—	50	—	50	—	550	—	30	—	25	ns
25[2]	$\overline{AS}$, $\overline{DS}$) Negated to Data-Out Invalid (Write)	40[1] 0	—	30	—	20	—	15	—	15	—	10	—	ns

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Num	Characteristic	8 MHz*		10 MHz*		12.5 MHz*		16.67 MHz 12F		16 MHz		20 MHz**		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
26[2]	Data-Out Valid to $\overline{DS}$ Asserted (Write)	40	—	30	—	20	—	15	—	15	—	10	—	ns
27[5]	Data-In Valid to Clock Low (Setup Time on Read)	10	—	10	—	10	—	7	—	5	—	5	—	ns
27A[5]	Late $\overline{BERR}$ Asserted to Clock Low (setup Time)	45	—	45	—	45	—	—	—	—	—	—	—	ns
28[2]	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Asynchronous Hold)	0	240[1] [1]	0	190	0	150	0	110	0	110	0	95	ns
28A	$\overline{AS}$, $\overline{DS}$ Negated to Data-In High Impedance	—	187	—	150	—	120	—	110	—	110	—	95	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	0	—	0	—	0	—	0	—	0	—	0	—	ns
29A	$\overline{AS}$, $\overline{DS}$ Negated to Data-In High Impedance	—	187	—	150	—	120	—	90	—	90	—	75	ns
30	$\overline{AS}$, $\overline{DS}$) Negated to $\overline{BERR}$ Negated	0	—	0	—	0	—	0	—	0	—	0	—	ns
31[2,5]	$\overline{DTACK}$ Asserted to Data-In Valid (Setup Time)	—	90	—	65	—	50	—	40	—	50	—	42	ns
32	$\overline{HALT}$) and $\overline{RESET}$ Input Transition Time	0	200	0	200	0	200	0	150	—	150	0	150	ns
33	Clock High to $\overline{BG}$ Asserted	—	62	—	50	—	40	—	40	0	30	0	25	ns
34	Clock High to $\overline{BG}$ Negated	—	62	—	50	—	40	—	40	0	30	0	25	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
36[7]	$\overline{BR}$ Negated to$\overline{BG}$ Negated	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37A[8]	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	20	1.5 Clks	20	1.5 Clks	20	1.5 Clks	10	1.5 Clks	10	1.5 Clks	10	1.5 Clks	ns
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)	—	80	—	70	—	60	—	50	—	50	—	42	ns
39	$\overline{BG}$ Width Negated	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	clks
40	Clock Low to $\overline{VMA}$ Asserted	—	70	—	70	—	70	—	50	—	50	—	40	ns
41	Clock Low to E Transition	—	55[12]	—	45	—	35	—	35	—	35	—	30	ns
42	E Output Rise and Fall Time	—	15	—	15	—	15	—	15	—	15	—	12	ns
43	$\overline{VMA}$ Asserted to E High	200	—	150	—	90	—	80	—	80	—	60	—	ns
44	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{VPA}$ Negated	0	120	0	90	0	70	0	50	0	50	0	42	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	30	—	10	—	10	—	10	—	10	—	10	—	ns
46	$\overline{BGACK}$ Width Low	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns

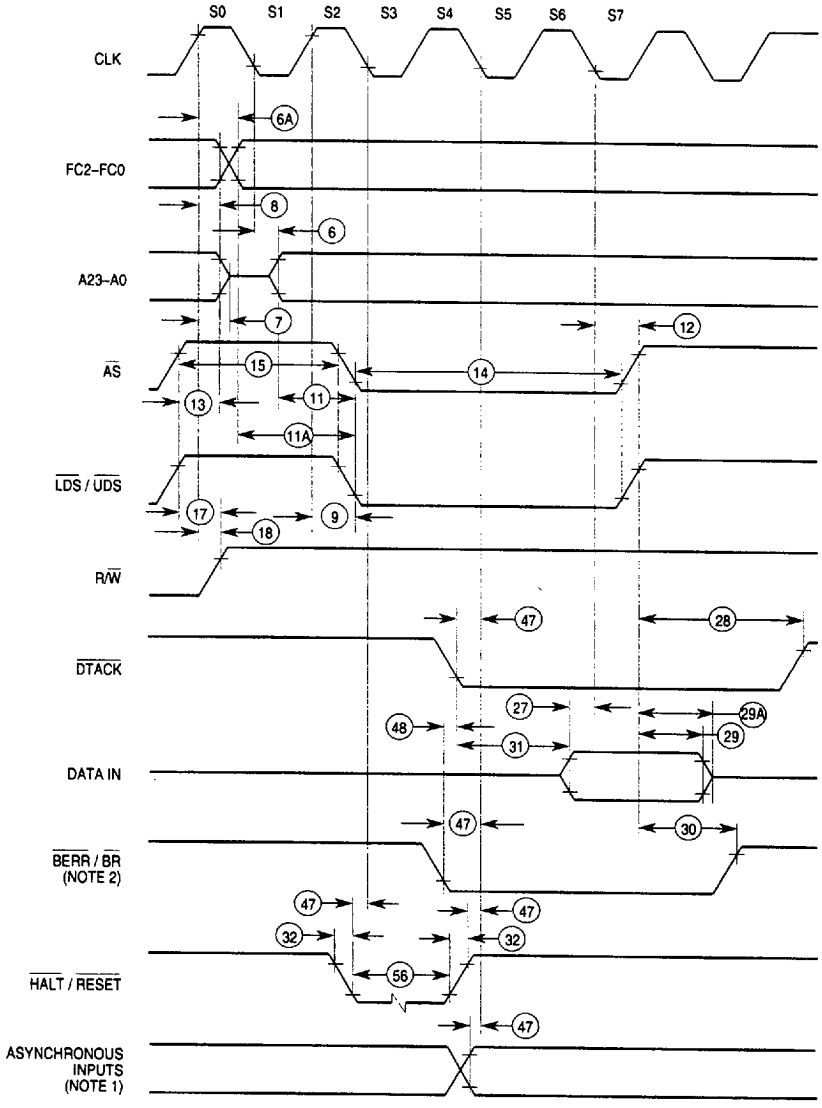
Num	Characteristic	8 MHz*		10 MHz*		12.5 MHz*		16.67 MHz 12F		16 MHz		20 MHz**		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
47[5]	Asynchronous Input Setup Time	10	—	10	—	10	—	10	—	5	—	5	—	ns
48[2,3]	$\overline{BERR}$ Asserted to $\overline{DTACK}$ Asserted	20	—	20	—	20	—	10	—	10	—	10	—	ns
48[2,3,5]	$\overline{DTACK}$ Asserted to $\overline{BERR}$ Asserted (MC68010 Only)	—	80	—	55	—	35	—	—	—	—	—	—	ns
49[9]	$\overline{AS}$, $\overline{DS}$, Negated to E Low	-70	70	-55	55	-45	45	-35	35	-35	35	–30	30	ns
50	E Width High	450	—	350	—	280	—	220	—	220	—	190	—	ns
51	E Width Low	700	—	550	—	440	—	340	—	340	—	290	—	ns
53	Data-Out Hold from Clock High	0	—	0	—	0	—	0	—	0	—	0	—	ns
54	E Low to Data-Out Invalid	30	—	20	—	15	—	10	—	10	—	5	—	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	30	—	20	—	10	—	0	—	0	—	0	—	ns
56[4]	$\overline{HALT}$ ($\overline{RESET}$Pulse Width	10	—	10	—	10	—	10	—	10	—	10	—	clks
57	$\overline{BGACK}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	clks
57A	$\overline{BGACK}$ Negated to FC, $\overline{VMA}$ Driven	1	—	1	—	1	—	1	—	1	—	1	—	clks
58[7]	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	clks
58A[7]	$\overline{BR}$ Negated to FC, $\overline{AS}$ Driven	1	—	1	—	1	—	1	—	1	—	1	—	clks

*These specifications represent improvement over previously published specifications for the 8-, 10-, and 12.5-MHz MC68000 and are valid only for product bearing date codes of 8827 and later.

** This frequency applies only to MC68HC000 and MC68HC001.

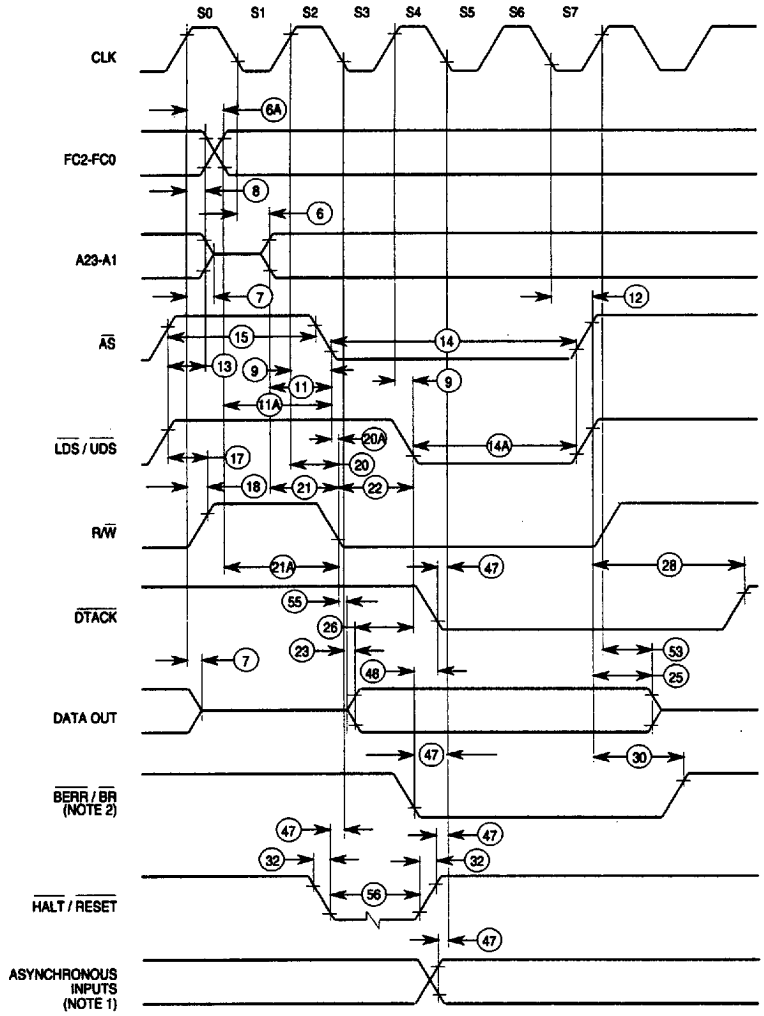
NOTES:

1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.
2. Actual value depends on clock period.
3. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may be ignored. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (#47).
4. For power-up, the MC68000 must be held in the reset state for 100 ms to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the processor.
5. If the asynchronous input setup time (#47) requirement is satisfied for $\overline{DTACK}$, the $\overline{DTACK}$ asserted to data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle.
6. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20;pc), subtract 5 ns from the values given in these columns.
7. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
8. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.
9. The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and $\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of E.
10. 245 ns for the MC68008.
11. 50 ns for the MC68008
12. 50 ns for the MC68008.



NOTES:
1. Setup time for the asynchronous inputs $\overline{IPL2}$–$\overline{IPL0}$ and $\overline{AVEC}$ (#47) guarantees their recognition at the next falling edge of the clock.
2. $\overline{BR}$ need fall at this time only to insure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.

Figure 10-4. Read Cycle Timing Diagram
(Applies To All Processors Except The MC68EC000)



NOTES:
1. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.
2. Because of loading variations, R/$\overline{W}$ may be valid after $\overline{AS}$ even though both are initiated by the rising edge of S2 (specification #20A).

Figure 10-5. Write Cycle Timing Diagram
(Applies To All Processors Except The MC68EC000)

10.11 AC ELECTRICAL SPECIFICATIONS—MC68000 TO M6800 PERIPHERAL (V_{CC} = 5.0 Vdc ±5%; GND=0 Vdc; $T_A = T_L$ TO T_H; refer to figures 10-6)

(Applies To All Processors Except The MC68EC000)

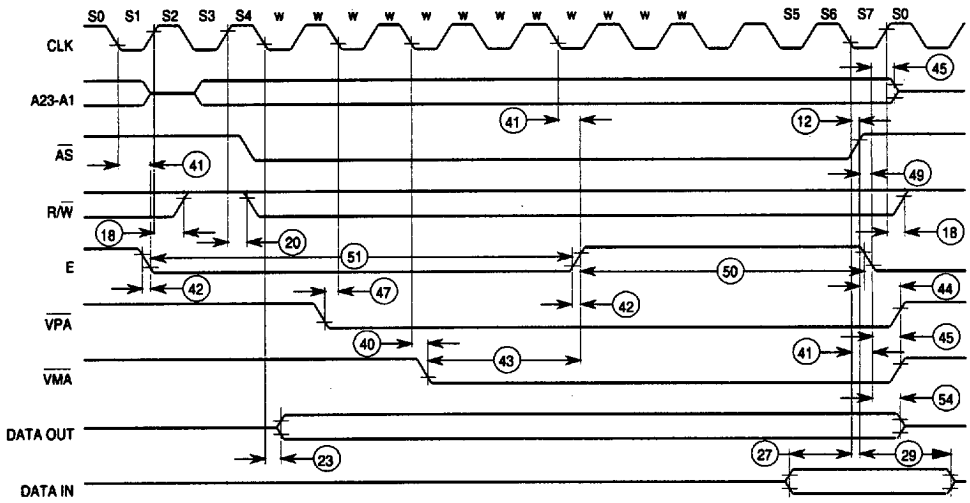
Num	Characteristic	8 MHz*		10 MHz*		12.5 MHz*		16.67 MHz `12F'		16 MHz		20 MHz**		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	—	62	—	50	—	40	—	40	3	30	3	25	ns
18[1]	Clock High to R/$\overline{W}$ High (Read)	0	55	0	45	0	40	0	40	0	30	0	25	ns
20[1]	Clock High to R/$\overline{W}$ Low (Write)	0	55	0	45	0	40	0	40	0	30	0	25	ns
23	Clock Low to Data-Out Valid (Write)	—	62	—	50	—	50	—	50	—	30	—	25	ns
27	Data-In Valid to Clock Low (Setup Time on Read)	10	—	10	—	10	—	7	—	5	—	5	—	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	0	—	0	—	0	—	0	—	0	—	0	—	ns
40	Clock Low to $\overline{VMA}$ Asserted	—	70	—	70	—	70	—	50	—	50	—	40	ns
41	Clock Low to E Transition	—	55	—	45	—	35	—	35	—	35	—	30	ns
42	E Output Rise and Fall Time	—	15	—	15	—	15	—	15	—	15	—	12	ns
43	$\overline{VMA}$ Asserted to E High	200	—	150	—	90	—	80	—	80	—	60	—	ns
44	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{VPA}$ Negated	0	120	0	90	0	70	0	50	0	50	0	42	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	30	—	10	—	10	—	10	—	10	—	10	—	ns
47	Asynchronous Input Setup Time	10	—	10	—	10	—	10	—	10	—	5	—	ns
49[2]	$\overline{AS}$, $\overline{DS}$, Negated to E Low	-70	70	-55	55	-45	45	-35	35	-35	35	-30	30	ns
50	E Width High	450	—	350	—	280	—	220	—	220	—	190	—	ns
51	E Width Low	700	—	550	—	440	—	340	—	340	—	290	—	ns
54	E Low to Data-Out Invalid	30	—	20	—	15	—	10	—	10	—	5	—	ns

*These specifications represent improvement over previously published specifications for the 8-, 10-, and 12.5-MHz MC68000 and are valid only for product bearing date codes of 8827 and later.

** This frequency applies only to MC68HC000 and MC68HC001.

NOTES:
1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.
2. The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and $\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specificaton #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

10



NOTE: This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the best case possible attainable

Figure 10-6. MC68000 to M6800 Peripheral Timing Diagram (Best Case)
(Applies To All Processors Except The MC68EC000)

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10.12 AC ELECTRICAL SPECIFICATIONS — BUS ARBITRATION (V_{CC}=5.0 VDC±5%; GND=0 VDC, T_A=T_L TO T_H; See Figure s 10-7 – 10-11) (Applies To All Processors Except The MC68EC000)

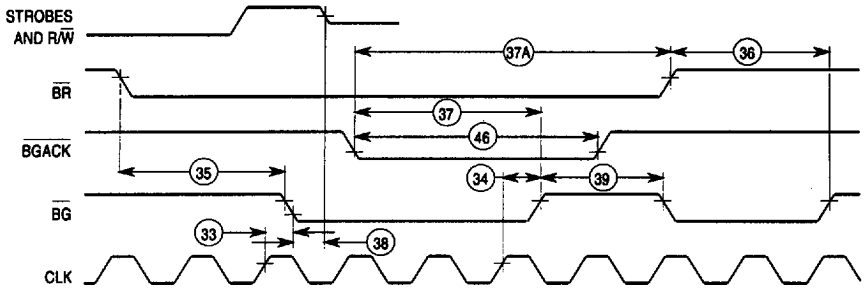
Num	Characteristic	8 MHz*		10 MHz*		12.5 MHz*		16.67 MHz 12F		16 MHz		20 MHz**		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
7	Clock High to Address, Data Bus High Impedance (Maximum)	—	80	—	70	—	60	—	50	—	50	—	42	ns
16	Clock High to Control Bus High Impedance	—	80	—	70	—	60	—	50	—	50	—	42	ns
33	Clock High to $\overline{BG}$ Asserted	—	62	—	50	—	40	0	40	0	30	0	25	ns
34	Clock High to $\overline{BG}$ Negated	—	62	—	50	—	40	0	40	0	30	0	25	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
36[1]	$\overline{BR}$ Negated to $\overline{BG}$ Negated	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37A[2]	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	20	1.5 Clks	20	1.5 Clks	20	1.5 Clks	10	1.5 Clks	10	1.5 Clks	10	1.5 Clks	Clks/ ns
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)		80		70		60	—	50	—	50	—	42	ns
39	$\overline{BG}$ Width Negated	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
46	$\overline{BGACK}$ Width Low	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
47	Asynchronous Input Setup Time	10	—	10	—	10	—	5	—	5	—	5	—	ns
57	$\overline{BGACK}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
57A	$\overline{BGACK}$ Negated to FC, $\overline{VMA}$ Driven	1	—	1	—	1	—	1	—	1	—	1	—	Clks
58[1]	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
58A[1]	$\overline{BR}$ Negated to FC, $\overline{VMA}$ Driven	1	—	1	—	1	—	1	—	1	—	1	—	Clks

*These specifications represent improvement over previously published specifications for the 8-, 10-, and 12.5-MHz MC68000 and are valid only for product bearing date codes of 8827 and later.

** Applies only to the MC68HC000 and MC68HC001.

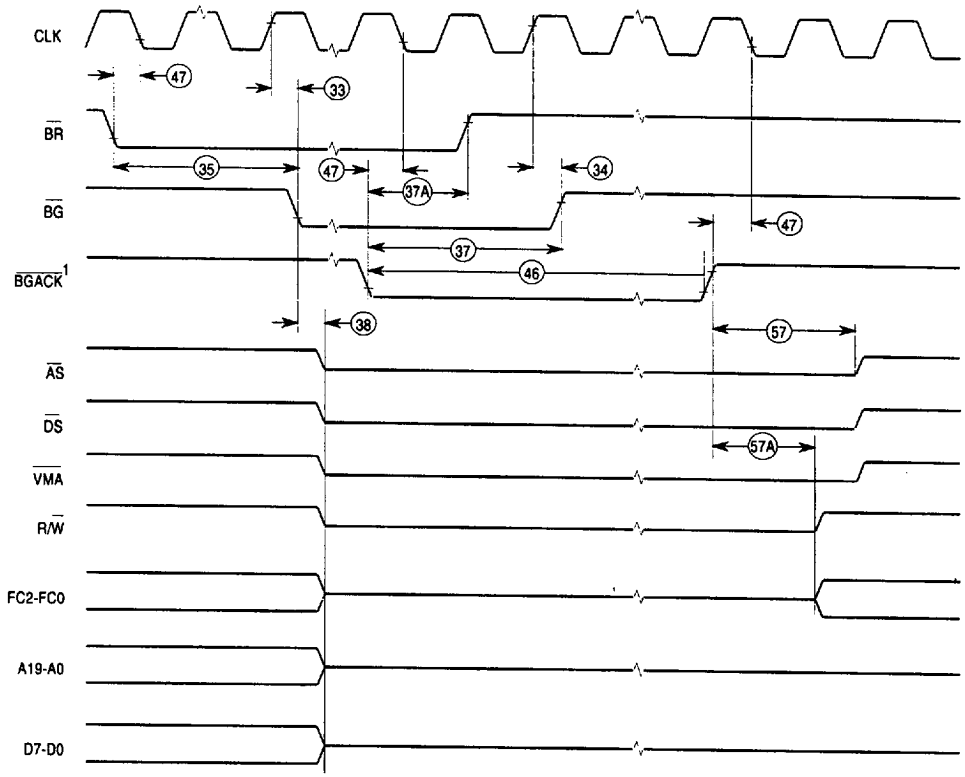
NOTES:

1. Setup time for the synchronous inputs $\overline{BGACK}$, $\overline{IPL0}$-$\overline{IPL2}$ and $\overline{VPA}$ guarantees their recognition at the next falling edge of the clock.
2. $\overline{BR}$ need fall at this time only in order to insure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be lienar between 0.8 volt and 2.0 volts.
4. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
5. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.



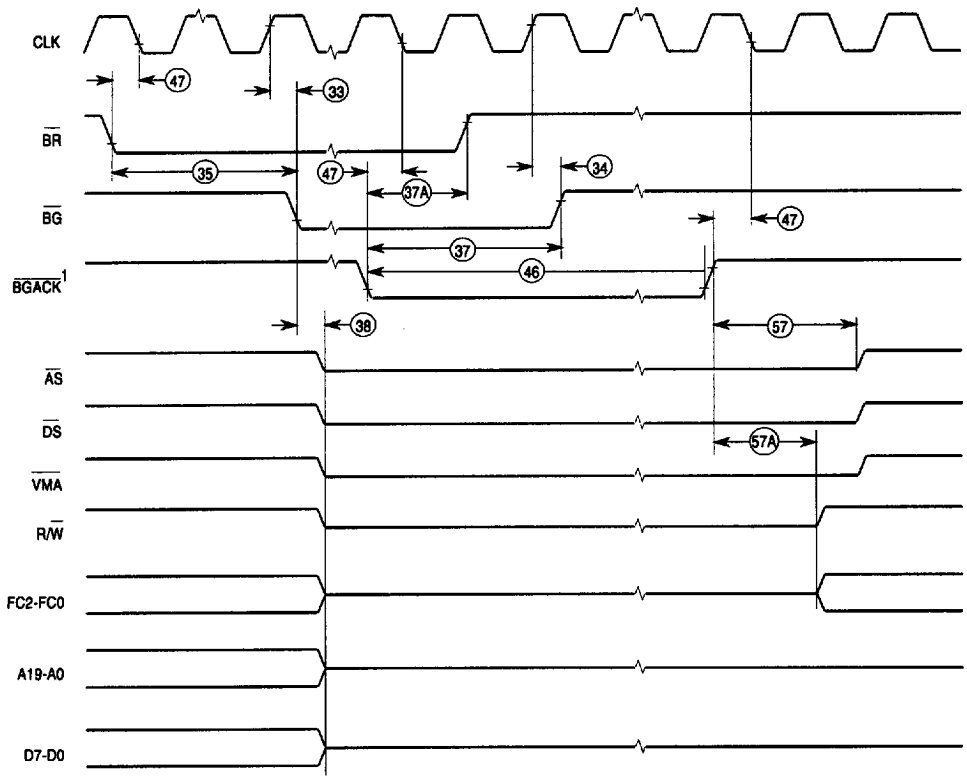
NOTE: Setup time to the clock (#47) for the asynchronous inputs BERR, BGACK, BR, DTACK, IPL2-IPL0, and VPA guarantees their recognition at the next falling edge of the clock.

Figure 10-7. Bus Arbitration Timing
(Applies To All Processors Except The MC68EC000)



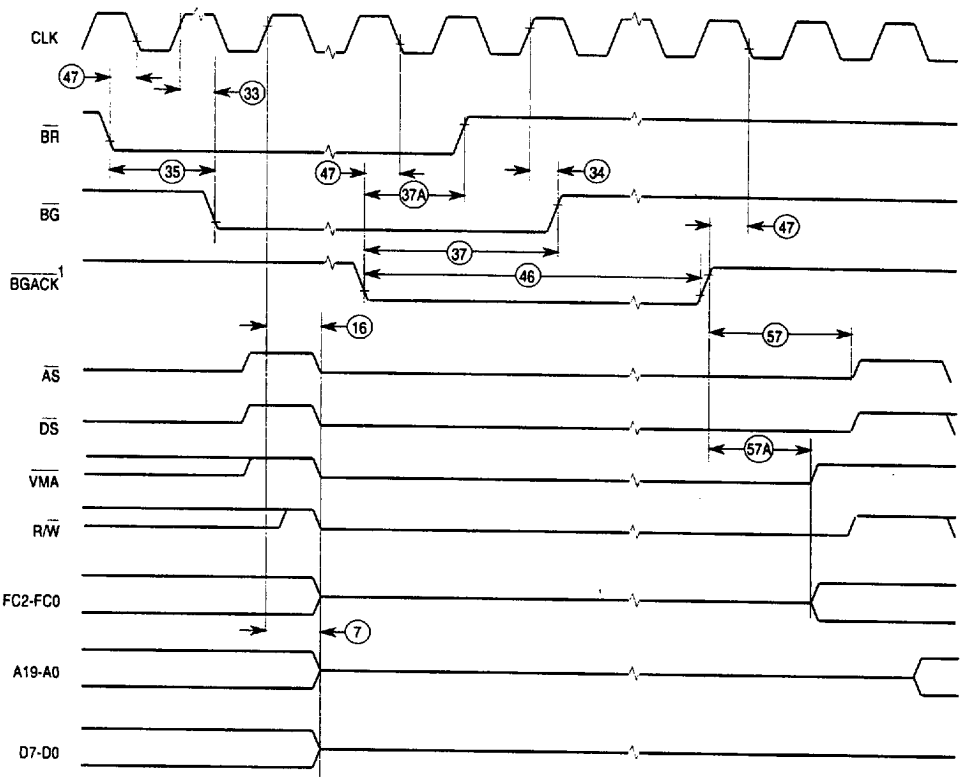
NOTES: Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.
1. MC68008 52-Pin Version only.

Figure 10-8. Bus Arbitration Timing
(Applies To All Processors Except The MC68EC000)



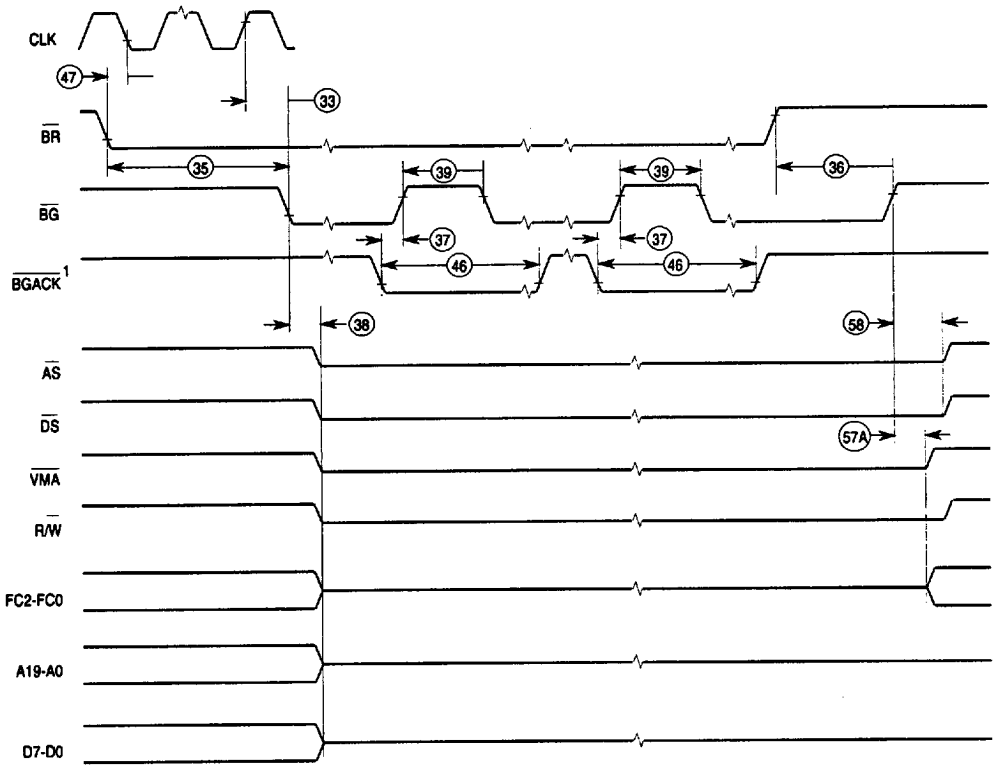
NOTES: Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.
1. MC68008 52-Pin Version only.

Figure 10-9. Bus Arbitration Timing — Idle Bus Case
(Applies To All Processors Except The MC68EC000)



NOTE: Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.
1 MC68008 52-Pin Version Only.

Figure 10-10. Bus Arbitration Timing — Active Bus Case
(Applies To All Processors Except The MC68EC000)



NOTES: Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.
1. MC68008 52-Pin Version only.

Figure 10-11. Bus Arbitration Timing — Multiple Bus Request
(Applies To All Processors Except The MC68EC000)

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10.13 MC68EC000 DC ELECTRICAL SPECIFICATIONS (VCC=5.0 VDC ± 5;PC; GND=0 VDC; $T_A = T_L$ TO T_H)

Characteristic		Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	2.0	V_{CC}	V
Input Low Voltage		V_{IL}	GND–0.3	0.8	V
Input Leakage Current @5.25 V	$\overline{BERR}$, $\overline{BR}$, $\overline{DTACK}$, CLK, $\overline{IPL2}$–$\overline{IPL0}$, $\overline{AVEC}$	I_{in}	—	2.5	μA
	MODE, $\overline{HALT}$, $\overline{RESET}$		—	20	
Three-State (Off State) Input Current @2.4 V/0.4 V	AS, A23–A0, D15–D0, FC2–FC0, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$	I_{TSI}	—	20	μA
Output High Voltage (I_{OH}=–400 μA)	AS, A23–A0, $\overline{BG}$, D15–D0, FC2–FC0, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$	V_{OH}	VCC –0.75	—	V
Output Low Voltage		V_{OL}			V
(IOL = 1.6 mA)	$\overline{HALT}$		—	0.5	
(IOL = 3.2 mA)	A23–A0, $\overline{BG}$, FC2–FC0		—	0.5	
(IOL = 5.0 mA)	$\overline{RESET}$		—	0.5	
(IOL = 5.3 mA)	$\overline{AS}$, D15–D0, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$		—	0.5	
Current Dissipation*	f=8 MHz	I_D	—	25	mA
	f=10 MHz		—	30	
	f=12.5 MHz		—	35	
	f=16.67 MHz		—	50	
	f= 20 MHz		—	70	
Power Dissipation	f=8 MHz	P_D	—	0.13	W
	f=10 MHz		—	0.16	
	f=12.5 MHz		—	0.19	
	f=16.67 MHz		—	0.26	
	f=20 MHz		—	0.38	
Capacitance (Vin=0 V, TA=25°C, Frequency=1 MHz)**		C_{in}	—	20.0	pF
Load Capacitance	$\overline{HALT}$	C_L	—	70	pF
	All Others		—	130	

*Currents listed are with no loading.

**Capacitance is periodically sampled rather than 100% tested.

10

10.14 MC68EC000 AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (VCC=5.0 VDC ± 5;PC; GND = 0 VDC; $T_A = T_L$ TO T_H; (See Figures 10-12 and 10-13)

Num	Characteristic	8 MHz		10 MHz		12.5 MHz		16.67 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
6	Clock Low to Address Valid	—	35	—	35	—	35	—	30	—	25	ns
6A	Clock High to FC Valid	—	35	—	35	—	35	—	30	0	25	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	—	55	—	55	—	55	—	50	—	42	ns
8	Clock High to Address, FC Invalid (Minimum)	0	—	0	—	0	—	0	—	0	—	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Asserted	3	35	3	35	3	35	3	30	3	25	ns
11[2]	Address Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read)/$\overline{AS}$ Asserted (Write)	30	—	20	—	15	—	15	—	10	—	ns
11A[2]	FC Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read)/ $\overline{AS}$ Asserted (Write)	45	—	45	—	45	—	45	—	40	—	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	3	35	3	35	3	35	3	30	3	25	ns
13[2]	$\overline{AS}$, $\overline{DS}$ Negated to Address, FC Invalid	15	—	15	—	15	—	15	—	10	—	ns
14[2]	$\overline{AS}$ (and $\overline{DS}$ Read) Width Asserted	270	—	195	—	160	—	120	—	100	—	ns
14A[2]	$\overline{DS}$ Width Asserted (Write)	140	—	95	—	80	—	60	—	50	—	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width Negated	150	—	105	—	65	—	60	—	50	—	ns
16	Clock High to Control Bus High Impedance	—	55	—	55	—	55	—	50	—	42	ns
17[2]	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	15	—	15	—	15	—	15	—	10	—	ns
18[1]	Clock High to R/$\overline{W}$ High (Read)	0	35	0	35	0	35	0	30	0	25	ns
20[1]	Clock High to R/$\overline{W}$ Low (Write)	0	35	0	35	0	35	0	30	0	25	ns
20A[2,6]	$\overline{AS}$ Asserted to R/$\overline{W}$ Low (Write)	—	10	—	10	—	10	—	10	—	10	ns
21[2]	Address Valid to R/$\overline{W}$ Low (Write)	0	—	0	—	0	—	0	—	0	—	ns
21A[2]	FC Valid to R/$\overline{W}$ Low (Write)	60	—	50	—	30	—	30	—	25	—	ns
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	80	—	50	—	30	—	30	—	25	—	ns
23	Clock Low to Data-Out Valid (Write)	—	35	—	35	—	35	—	30	—	25	ns
25[2]	$\overline{AS}$, $\overline{DS}$ Negated to Data-Out Invalid (Write)	40	—	30	—	20	—	15	—	10	—	ns
26[2]	Data-Out Valid to $\overline{DS}$ Asserted (Write)	40	—	30	—	20	—	15	—	10	—	ns
27[5]	Data-In Valid to Clock Low (Setup Time on Read)	5	—	5	—	5	—	5	—	5	—	ns
28[2]	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Asynchronous Hold)	0	110	0	110	0	110	0	110	0	95	ns
28A	Clock High to $\overline{DTACK}$ Negated	0	110	0	110	0	110	0	110	0	95	ns

Num	Characteristic	8 MHz		10 MHz		12.5 MHz		16.67 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
29	AS, DS Negated to Data-In Invalid (Hold Time on Read)	0	—	0	—	0	—	0	—	0	—	ns
29A	AS, DS Negated to Data-In High Impedance	—	187	—	150	—	120	—	90	—	75	ns
30	AS, DS Negated to BERR Negated	0	—	0	—	0	—	0	—	0	—	ns
31[2,5]	DTACK Asserted to Data-In Valid (Setup Time)	—	90	—	65	—	50	—	50	—	42	ns
32	HALT and RESET Input Transition Time	0	150	0	150	0	150	0	150	0	150	ns
33	Clock High to BG Asserted	—	35	—	35	—	35	0	30	0	25	ns
34	Clock High to BG Negated	—	35	—	35	—	35	0	30	0	25	ns
35	BR Asserted to BG Asserted	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
36[7]	BR Negated to BG Negated	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
38	BG Asserted to Control, Address, Data Bus High Impedance (AS Negated)	—	55	—	55	—	55	—	50	—	42	ns
39	BG Width Negated	1.5		1.5		1.5		1.5		1.5	—	Clks
44	AS, DS Negated to VPA Negated	0	55	0	55	0	55	0	50	0	42	ns
47[5]	Asynchronous Input Setup Time	5	—	5	—	5	—	5	—	5	—	ns
48[2,3]	BERR Asserted to DTACK Asserted	20	—	20	—	20	—	10	—	10	—	ns
53	Data-Out Hold from Clock High	0	—	0	—	0	—	0	—	0	—	ns
55	R/W Asserted to Data Bus Impedance Change	30	—	20	—	10	—	0	—	0	—	ns
56[4]	HALT/RESET Pulse Width	10	—	10	—	10	—	10	—	10	—	Clks
58[7]	BR Negated to AS, DS, R/W Driven	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
58A[7]	BR Negated to FC, VMA Driven	1	—	1	—	1	—	1	—	1	—	Clks

NOTES:1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.

2. Actual value depends on clock period.

3.I f #47 is satisfied for both DTACK and BERR, #48 may be ignored. In the absence of DTACK, BERR is an asynchronous input using the asynchronous input setup time (#47).

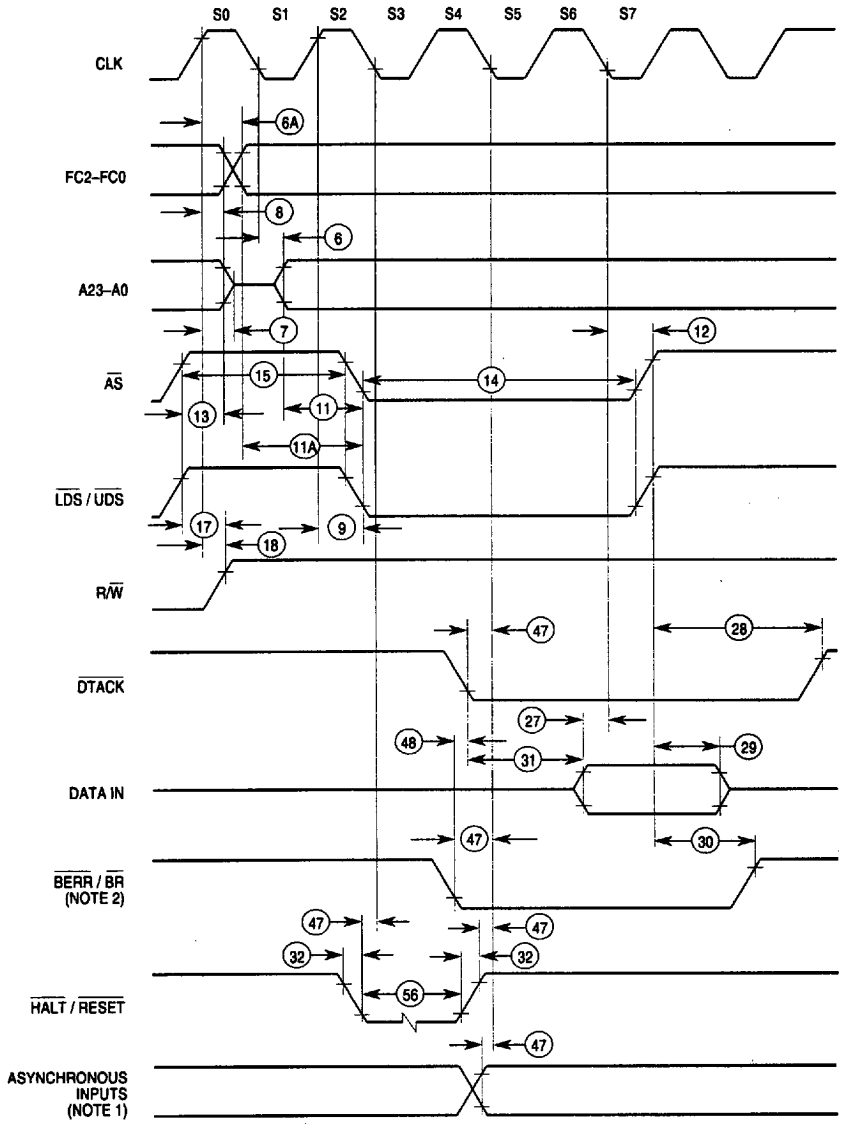
4. For power-up, the MC68EC000 must be held in the reset state for 520 clocks to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the processor.

5. If the asynchronous input setup time (#47) requirement is satisfied for DTACK, the DTACK-asserted to data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle.

6. When AS and R/W are equally loaded (±20;pc), subtract 5 ns from the values given in these columns.

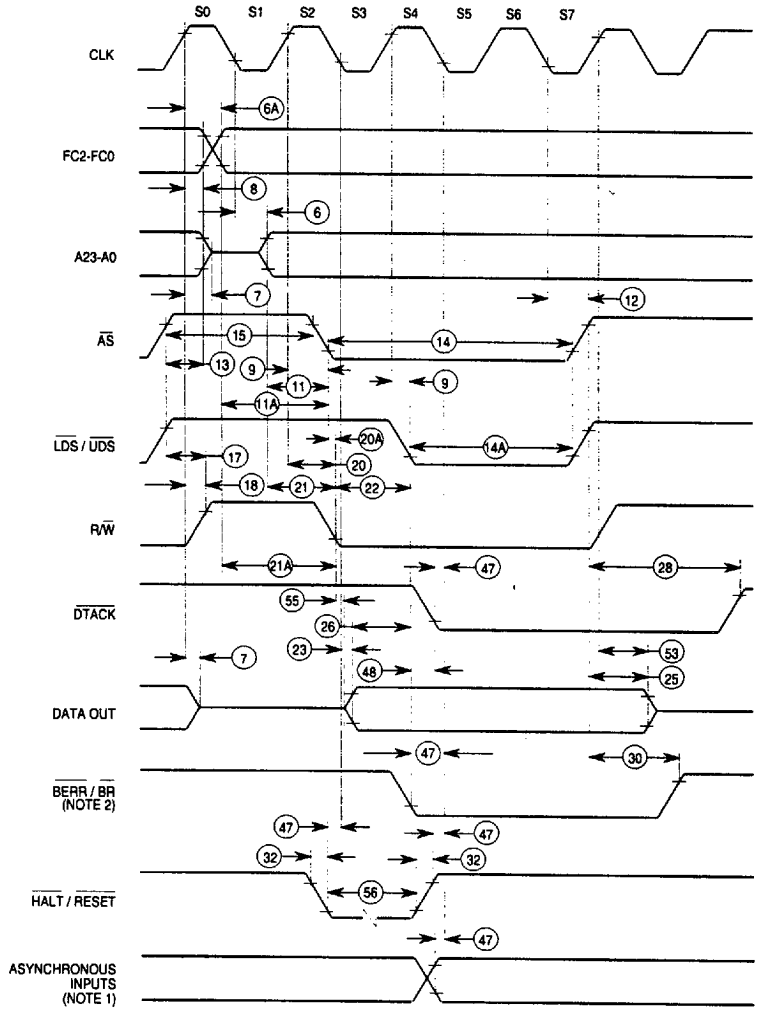
7. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, BG may be reasserted.

8. DS is used in this specification to indicate UDS and LDS.



NOTES:
1. Setup time for the asynchronous inputs $\overline{IPL2}$–$\overline{IPL0}$ and $\overline{AVEC}$ (#47) guarantees their recognition at the next falling edge of the clock.
2. $\overline{BR}$ need fall at this time only to insure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.

Figure 10-12. MC68EC000 Read Cycle Timing Diagram



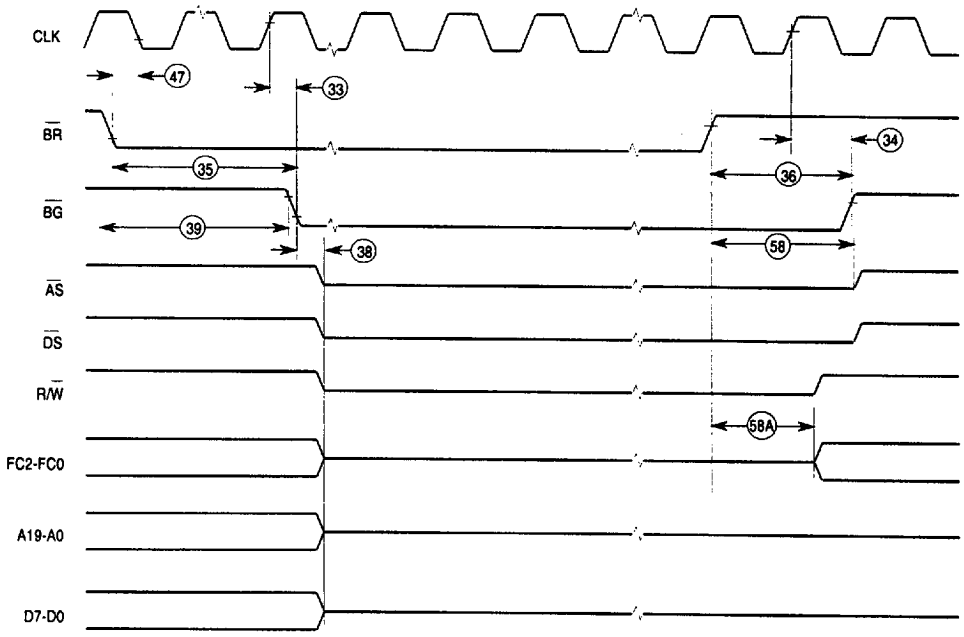
NOTES:
1. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.
2. Because of loading variations, R/W may be valid after AS even though both are initiated by the rising edge of S2 (specification #20A).

Figure 10-13. MC68EC000 Write Cycle Timing Diagram

10.15 MC68EC000 AC ELECTRICAL SPECIFICATIONS—BUS ARBITRATION (VCC=5.0VDC ± 5%; GND=0 VDC; $T_A = T_L$ TO T_H; see Figure 10-14)

Num	Characteristic	8 MHz		10 MHz		12.5 MHz		16.67 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
7	Clock High to Address, Data Bus High Impedance (Maximum)	—	55	—	55	—	55	—	50	—	42	ns
16	Clock High to Control Bus High Impedance	—	55	—	55	—	55	—	50	—	42	ns
33	Clock High to $\overline{BG}$ Asserted	—	35	—	35	—	35	0	30	0	25	ns
34	Clock High to $\overline{BG}$ Negated	—	35	—	35	—	35	0	30	0	25	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
36[7]	$\overline{BR}$ Negated to $\overline{BG}$ Negated	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)	—	55	—	55	—	55	—	50	—	42	ns
39	$\overline{BG}$ Width Negated	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
47	Asynchronous Input Setup Time	5	—	5	—	5	—	5	—	5	—	ns
58[1]	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	Clks
58A[1]	$\overline{BR}$ Negated to FC Driven	1	—	1	—	1	—	1	—	1	—	Clks

NOTES: 1. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.
2. $\overline{DS}$ is used in this specification to indicate $\overline{UDS}$ and $\overline{LDS}$.



NOTES: Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.

Figure 10-14. MC68EC000 Bus Arbitration Timing Diagram